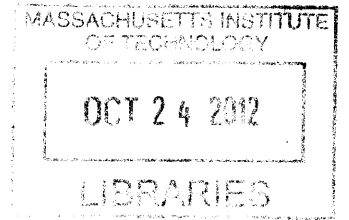


**Phase Manipulation for Efficient Radio Frequency  
Transmission**

ARCHIVES



by

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S.B., Massachusetts Institute of Technology (2006)  
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Submitted to the Department of Electrical Engineering and Computer  
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## Abstract

Power amplifiers (PAs) for microwave communications are generally the most power-hungry element of a transmitter. High linearity is required for modern digital communications standards, and often is achieved at the expense of efficiency. Outphasing architectures, which combine multiple nonlinear but efficient switching PAs into a system with an overall linear response, represent a promising strategy for breaking the efficiency/linearity tradeoff inherent to conventional PAs.

This work explores methods for efficient PA design using outphasing techniques. Two aspects of outphasing design are considered. First, a wide-band phase modulator is introduced that uses a single current-steering digital to analog converter (DAC) structure and discrete clock prerotation. This topology takes advantage of specifications particular to outphasing architectures to reduce matching requirements as compared to a two-DAC phase modulator while providing wideband capability. The phase modulator is demonstrated in 65-nm CMOS, operates over a carrier frequency range of 1.2-4.2 GHz and has a 12-bit phase resolution and sample rate of 160 MSamples/second.

The second technique is a novel four-way lossless power combiner and outphasing system which provides ideally lossless power combining along with resistive loading of switching power amplifiers over a wide output range. This work presents the first-ever demonstration of this system at microwave frequencies. Particular attention is paid to the microwave-specific aspects of implementation. A 60-W GaN prototype demonstrates the outphasing and dynamic performance, which closely matches the expected performance despite the challenges of operating at microwave frequencies.

Thesis Supervisor: James K. Roberge  
Title: Professor of Electrical Engineering



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# Contents

- 1 Introduction** **19**
  
- 2 Background and Related Work** **25**
  - 2.1 Polar Architecture . . . . . 25
  - 2.2 Doherty Power Amplifier . . . . . 27
  - 2.3 Outphasing . . . . . 28
    - 2.3.1 Chireix Outphasing . . . . . 29
    - 2.3.2 Multi-level LINC . . . . . 32
  - 2.4 Asymmetric Multilevel Outphasing . . . . . 33
  - 2.5 Resistance Compression Networks for Power Recovery . . . . . 34
    - 2.5.1 Resistance Compression Network . . . . . 36
    - 2.5.2 Power Recovery . . . . . 39
  
- 3 Digital to RF Phase Modulator** **41**
  - 3.1 Phase Modulator Overview . . . . . 42
  - 3.2 Core Circuit Design . . . . . 43
    - 3.2.1 Current Source Array . . . . . 44
    - 3.2.2 Data/Quadrant Switches and Latching . . . . . 46
    - 3.2.3 Multiplication by Carrier . . . . . 48
  - 3.3 Clock Prerotation . . . . . 50
  - 3.4 Additional Blocks . . . . . 52
  
- 4 DRFPM Experimental Results** **55**

4.1	Phase Modulator Measurement Setup . . . . .	55
4.2	Carrier Frequency Operating Range . . . . .	57
4.3	Static Measurement Results . . . . .	57
4.4	Dynamic Performance . . . . .	60
4.4.1	Transient Response . . . . .	60
4.4.2	Simplified 8-PSK . . . . .	62
4.4.3	GSM . . . . .	62
4.4.4	Outphasing Measurements . . . . .	65
<b>5</b>	<b>Four-Way Lossless Outphasing Combiner: Theoretical Development</b>	<b>69</b>
5.1	Theory of Operation . . . . .	70
5.2	Phase Control Strategies . . . . .	73
5.2.1	IRCN Control . . . . .	74
5.2.2	Optimal Susceptance Outphasing Control . . . . .	75
5.2.3	Optimal Phase Outphasing Control . . . . .	78
5.3	Combiner Design with Parameter $k$ . . . . .	79
<b>6</b>	<b>Four-Way Lossless Outphasing Combiner: Prototype Development</b>	<b>81</b>
6.1	Baseband Signal Processing . . . . .	81
6.2	Class Inverse F Power Amplifier . . . . .	82
6.3	Discrete Combiner Design . . . . .	87
6.4	Connector Lengths . . . . .	89
<b>7</b>	<b>Four-Way Lossless Outphasing Combiner: Measured Results</b>	<b>93</b>
7.1	Static Performance . . . . .	96
7.2	Dynamic Performance . . . . .	98
7.2.1	Transient Response . . . . .	100
7.2.2	Predistortion for Modulated Tests . . . . .	100
7.2.3	W-CDMA Modulation . . . . .	102
<b>8</b>	<b>Conclusions and Future Work</b>	<b>105</b>
8.1	Summary of Contributions . . . . .	105



8.2 Future Work . . . . .	106
<b>Bibliography</b>	<b>109</b>
<b>A List of Variables Relating to Four-Way Lossless Combiner</b>	<b>113</b>

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# List of Figures

1-1 Simplified power amplifier topology for class A/B/AB/C/D amplifiers. The class of operation depends on the conduction angle, defined graphically in (b). . . . . 21

1-2 The efficiency of the power amplifier in Figure 1-1 is always less than 100% when the device is operated as a current source [27]. . . . . 22

1-3 Constellation diagrams with increasingly aggressive modulation schemes: binary phase-shift keying (BPSK), quadrature phase-shift keying (QPSK), and 16- and 64-quadrature amplitude modulation (QAM). . . . . 22

2-1 Polar transmitter architecture. . . . . 26

2-2 The Doherty power amplifier architecture. A 50-Ω load impedance is assumed.[40] . . . . . 27

2-3 Doherty operating regions (a) and theoretical drain efficiency (b) [40]. 28

2-4 Generalized outphasing transmitter architecture. . . . . 29

2-5 Ideal efficiency curve for outphasing transmitter with isolating combiner over a range of power output levels and ideal ( $\eta_D = 100\%$ ) PAs. 30

2-6 Chireix architecture . . . . . 31

2-7 Chireix combiner behavior with  $R_L = 13 \Omega$ ,  $X = 13.6 \Omega$  (solid);  $R_L = 15 \Omega$ ,  $X = 17 \Omega$  (dashed); and  $R_L = 19.4 \Omega$ ,  $X = 45 \Omega$  (dotted). . . . 31

2-8 Efficiency of ML-LINC transmitter when four supply levels are used (solid), compared to basic outphasing (dashed). . . . . 33

2-9 The complete AMO architecture. . . . . 33

2-10	Ideal efficiency of AMO transmitter when four supply levels are used (solid), compared to ML-LINC (dashed) and basic outphasing (dotted).	35
2-11	Comparison of LINC, Multilevel-LINC, and AMO efficiencies for the AMO prototype, including the effect of supply voltage backoff on the PA power added efficiency. A WLAN power level probability density function is included for comparison. . . . .	35
2-12	Baseband vector decomposition comparison between (a) LINC, (b) ML-LINC, and (c) AMO architectures. . . . .	36
2-13	A single stage resistance compression network. . . . .	37
2-14	A two-stage resistance compression network, made up of three of the single-stage networks in Figure 2-13. . . . .	38
2-15	Input resistance and load voltage phasors for the two-stage resistance compression network. . . . .	39
2-16	Outphasing transmitter architectures with isolating combiner and power recovery. . . . .	40
3-1	Phase modulator block diagram. The phase-modulated signal is $S_{out} = \pm a \cos(\omega t) \pm (1 - a) \sin(\omega t)$ , where coefficient $0 \leq a < 1$ is controlled by digital input $\phi[0 : 9]$ . . . . .	42
3-2	The constraint $b = 1 - a$ results in a linear approximation to the ideal circle. . . . .	43
3-3	The multiple levels of vector decomposition in the AMO system with proposed phase modulator. . . . .	44
3-4	Simplified schematic of the fabricated phase modulator. . . . .	45
3-5	Current sources are generated by grouping unit transistors. . . . .	46
3-6	Current source array layout. The layout consists of 1292 unit transistors with width $20 \mu\text{m}$ and length $4 \mu\text{m}$ , grouped as indicated in (b). . . . .	47
3-7	Latch structure used for data bits and quadrant selection . . . . .	48
3-8	Current-steering switches and latches layout. . . . .	49

3-9	Carrier multiplication circuit detail for MSB and four LSB currents. The unit cell switches multiply the four LSB currents ( $I_{a,LSB} = I_{a0} + I_{a1} + I_{a2} + I_{a3}$ ). Higher bits use binary-scaled multiplicities, with a $32\times$ multiplicity switch for the MSB. . . . .	49
3-10	One solution to the dead zone problem inherent to high-accuracy phase-interpolation DRFPMS [30]. . . . .	51
3-11	By providing two reference angles, the range of output phases is made continuous despite missing codes. . . . .	51
3-12	Pre-rotation path, used to generate pre-rotated versions of $I$ and $Q$ . . . . .	53
4-1	Die photo. The DRFPM consumes $0.26\text{ mm}^2$ on the $2\text{mm} \times 2\text{mm}$ die. Unlabeled areas are occupied by circuits not relevant to the DRFPM testing. . . . .	56
4-2	Block diagram of the experimental setup for the DRFPM chip. . . . .	56
4-3	Phase modulator output over entire operating range. The pre-rotated data amplitude is scaled down in (a) so that phase gaps can be seen. . . . .	59
4-4	DRFPM step responses, computed by downloading oscilloscope trace data and demodulating to amplitude/phase data in MATLAB. . . . .	61
4-5	Spectrum and EVM measurement for sequential 8-PSK signal. . . . .	63
4-6	Example waveforms showing the evolution of MSK. [36] . . . . .	64
4-7	Measured spectrum for GMSK. . . . .	66
4-8	Outphasing system output for a 90-degree step in outphasing angle. The phase step is performed by switching a single quadrant bit so that no DAC glitches are present. The output settles within 2.5 ns. . . . .	67
4-9	250-kHz sinusoid generated by outphasing, 25 MSPS. The glitches visible at the step changes are a result of the timing errors in the digital portion of the DAC design. . . . .	67
4-10	16-QAM signal at 6.25 MSymbols/sec and with $2\times$ oversampling (12 MSPS total). The poor spectral performance is due to a combination of the low oversampling rate and glitches. . . . .	68

5-1	The four-way outphasing and combining architecture. The PAs are represented as ideal, constant-amplitude voltage sources with the phasor relationship shown. The transmission lines represent interconnects from the PA reference planes to the combiner input reference planes. All sources are operated at the same time and with equal amplitudes.	70
5-2	Effective input port admittances when IRCN control is used, with $R_L = 50 \Omega$ , $V_s = 1\text{ V}$ , and $k = 1.05$ .	76
5-3	Phase commands over output power range when IRCN is used, with $R_L = 50 \Omega$ , $V_s = 1\text{ V}$ , and $k = 1.05$ .	76
5-4	Effective input port admittances when OS control is used, with $R_L = 50 \Omega$ , $V_s = 1\text{ V}$ , and $k = 1.05$ .	78
5-5	Phase commands over entire valid output power range when OS is used, with $R_L = 50 \Omega$ , $V_s = 1\text{ V}$ , and $k = 1.05$ .	79
5-6	PA load magnitude and phase for a range of $k$ values. A larger $k$ gives an increased output power range but also increased deviation in the load phase.	80
6-1	Photograph of the baseband stage prototype.	82
6-2	Class inverse F power amplifier schematic, reproduced from [16].	83
6-3	Class inverse F power amplifier, with layout reproduced from [16]. Not to scale.	83
6-4	Measurement method. First, the stub tuner insertion loss and input impedance for a $50\text{-}\Omega$ termination is measured, then the PA is loaded with that impedance and output power and drain efficiency are measured.	84
6-5	PA drain efficiency and output power under load modulation with $V_g = -3.4\text{ V}$ and $V_{DD} = 20\text{ V}$ .	86
6-6	Photograph of the class inverse F power amplifier.	86
6-7	Discrete-component combiner implementation. The output (center) connector is on the reverse side.	87

6-8	The complete RF power stage with connector lengths that provide a net $\lambda/4$ between the PA and combiner boards. . . . .	89
6-9	Contour plot of system performance with different connector lengths between the PA and combiner PCBs. The angle of each dataset corresponds to the connector rotation, the radius is the normalized output power, and the shaded contours indicate lines of constant drain efficiency. . . . .	91
7-1	Measurement setup block diagram. . . . .	94
7-2	Four-way lossless outphasing and combining system measurement setup. . . . .	95
7-3	Measured drain efficiency and output power of the outphasing system (black) and single inverse class-F PA under load modulation (grey, dashed). . . . .	97
7-4	Percentage of total drain current provided by each PA over the range of measured outphasing commands. . . . .	97
7-5	Output power and drain efficiency measurements and calculated contours when the outphasing angles are swept around the values calculated from the OS control law. . . . .	99
7-6	System step responses under a range of operating conditions, both measured and simulated using ideal voltage sources and a simulated finite-Q discrete-component combiner. . . . .	101
7-7	Example signal amplitude measurements over four iterations. The system is particularly nonlinear near low amplitudes, as can be seen during the portion of the curve where normalized amplitude is 0.1 . . . . .	103
7-8	W-CDMA signal output spectrum, with and without sequence-based predistortion. . . . .	104
8-1	Versions of the combiner using microstrips are of interest for applications at microwave frequencies. . . . .	107

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# List of Tables

4.1	Comparison of DRFPM performance with the state of the art. . . . .	60
6.1	Component values for the implemented combiner. . . . .	87
6.2	Measured and simulated ( $k = 1.05$ ) port amplitudes and phases when output is driven and input ports are terminated in $50 \Omega$ . . . . .	88
7.1	Comparison of measured four-way combiner results to the state of the art. . . . .	104

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# Chapter 1

## Introduction

Modern digital communications systems encode data by modulating a carrier signal in amplitude and phase. The receiver decodes the transmitted signal by using an alphabet of agreed-upon values known as the constellation. One way to increase the data rate of a system without requiring a higher bandwidth for the baseband signal processing paths is to increase the density of this constellation, so that each transmitted signal is differentiated from a larger number of potential values. As the constellation becomes denser, that is as the number of possible values for the signal to represent increases, the transmitter and receiver must operate with increasingly precise linearity. In particular, the transmitter must be able to produce a precisely controlled output amplitude and phase over a high dynamic range. Ideally the transmitter's efficiency will remain high over the entire range of output powers.

As the most power-hungry and typically most nonlinear element of the transmitter, the power amplifier (PA) has efficiency and linearity requirements that become increasingly challenging for aggressively modulated signals. PAs of the general model in Figure 1-1(a) exhibit a *tradeoff* between linearity and efficiency [29]. This circuit is a general model for a variety of classes of PAs, where the class is determined by the input signal drive amplitude and the active device conduction angle. Conduction angle, defined graphically in Figure 1-1(b), is equal to the fraction of the carrier cycle over which the transistor is turned on, and is set by the bias point  $V_{\text{bias}}$  relative to the device pinch-off voltage  $V_p$ . The various classes of operation are summarized in

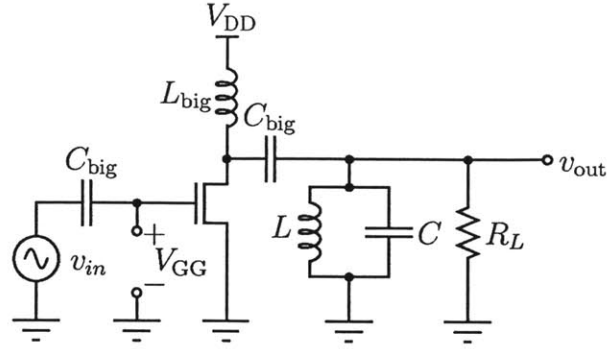
Figure 1-1(c), with Class-A PAs operating in a highly linear but inefficient regime, and switching PAs such as Class-D operating at a theoretical efficiency of 100% but with no output amplitude control [29]. The relationship between angle of conduction and theoretical maximum drain efficiency is shown in Figure 1-2 [27].

The linearity requirement for power amplifiers is directly related to the modulation and spectrum mask requirements of the transmitted standard. Figure 1-3 shows a selection of different modulation schemes with increasing complexity. Each dot represents an entry in the alphabet of codes for that modulation scheme. In the case of binary phase-shift keying (BPSK), the constellation points represent a single bit value of 1 or 0. The number of bits represented by each point increases by one each time the number of constellation points doubles. Thus if symbols are transmitted at a constant rate, the data rate (in bits/second) can be increased by using a denser modulation scheme. The advantage of this approach is that the required bandwidth of the transmitter building blocks is held constant while the data rate is increased. At the same time, an increased constellation density requires better linearity performance. Digital filtering is applied to the baseband signal to shape the transmitter's output spectrum in order to meet spectral mask requirements. The filtering further increases the linearity and dynamic range requirements for the power amplifier. This effect can be seen qualitatively in Figure 1-3, where the signal trajectories are shown for random ergodic<sup>1</sup> data when a raised-cosine filter and 10× oversampling rate (OSR) is used.

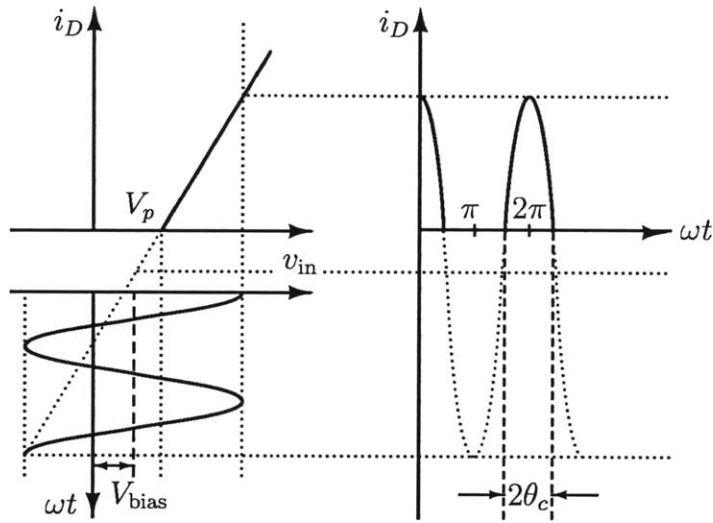
One strategy to break to linearity/efficiency tradeoff of the topology in Figure 1-1 is to combine multiple switching PAs in a way that has an overall linear response. The inherent efficiency advantage of switching PAs, along with ideally lossless power combining, can result in efficient overall performance. The two PA architectures in this work, Asymmetric Multilevel Outphasing (AMO) and the new four-way lossless outphasing and combining system, are examples of outphasing architectures. Both use phase-shift controlled switching amplifiers and power combining to modulate the output power.

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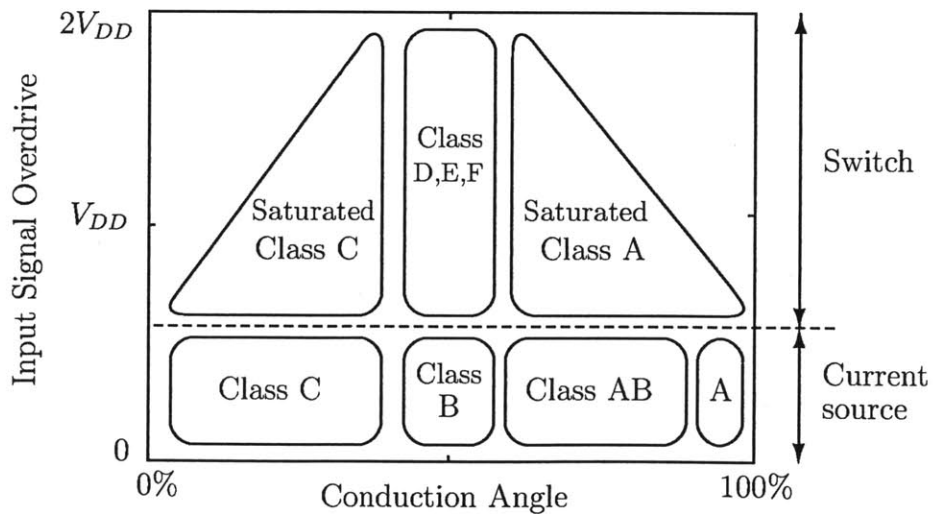
<sup>1</sup>*ergodic* – having equal probabilities



(a) General power amplifier model [29].



(b) Graphical definition of conduction angle  $\theta_c$  [17].



(c) Operating Regimes

Figure 1-1: Simplified power amplifier topology for class A/B/AB/C/D amplifiers. The class of operation depends on the conduction angle, defined graphically in (b).

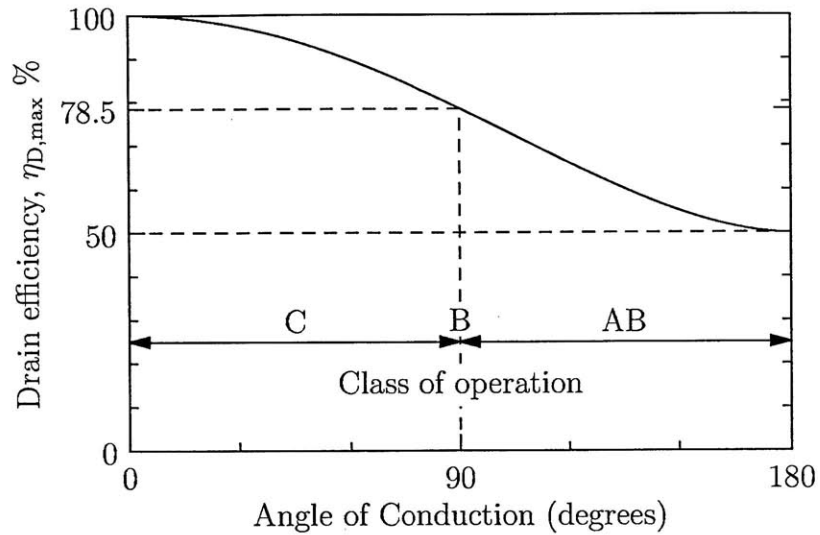


Figure 1-2: The efficiency of the power amplifier in Figure 1-1 is always less than 100% when the device is operated as a current source [27].

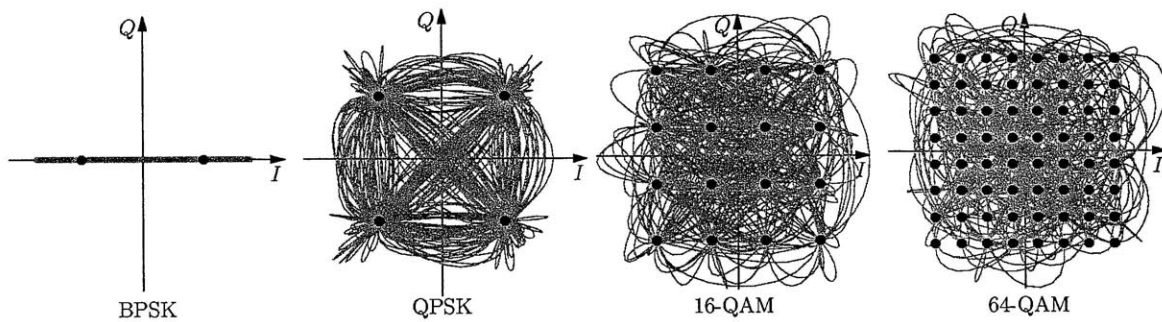


Figure 1-3: Constellation diagrams with increasingly aggressive modulation schemes: binary phase-shift keying (BPSK), quadrature phase-shift keying (QPSK), and 16- and 64-quadrature amplitude modulation (QAM).

The primary contributions of this work are a high-speed phase modulator for outphasing applications, and a new outphasing technique which provides ideally lossless power combining along with resistive loading of switching power amplifiers over a wide output range. The digital-to-RF phase modulator (DRFPM) is designed for AMO or AMO-like systems. The design takes advantage of the particular requirements of these applications, which are introduced in Chapter 2, for reduced area and matching requirements as compared to conventional designs. The DRFPM design and measurement results in 65-nm CMOS are presented in Chapters 3 and 4. A theoretical discussion of the four-way lossless outphasing and combining system follows in Chapter 5, with particular focus on the aspects of the system peculiar to microwave design. Finally, combiner implementation and measured results are presented in Chapters 6 and 7. The new four-way lossless combiner measured performance matches the expected behavior, and provides a considerable improvement over conventional techniques.

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# Chapter 2

## Background and Related Work

An RF transmitter for communications has two simultaneous and conflicting requirements of linearity and efficiency. In standard transmitter architectures, the block which most influences both of these characteristics is the power amplifier. In particular, the transmitter's efficiency performance is dominated by the efficiency of the power-hungry PA. Thus it is sensible when high efficiency is required to use a PA topology in which the transistor is operated as a switch. Although a switching PA does not provide linear control over the output power, it has a theoretical efficiency of 100%, and, in practice, demonstrated drain efficiencies on the order of 44% in CMOS [7] and 84% with GaN HEMT devices [35]. By contrast, a linear Class A PA has a theoretical maximum efficiency of only 50%. With this promise of high efficiency, there has been considerable longstanding research effort towards power amplifier architectures which combine multiple switching PAs in a way that results in overall system linearity.

### 2.1 Polar Architecture

In a polar architecture, the transmitted signal is characterized in terms of its amplitude ( $A$ ) and phase ( $\theta$ ) components instead of the more standard in-phase ( $I$ ) and quadrature ( $Q$ ) components. This architecture, shown in Figure 2-1, is also known as envelope elimination and restoration (EER) [25]. The signal to be transmitted is

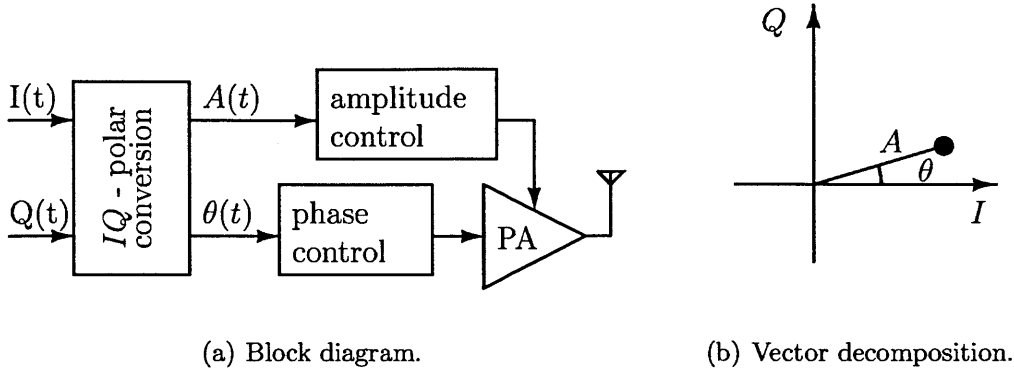


Figure 2-1: Polar transmitter architecture.

converted from Cartesian to polar coordinates by

$$A(t) = \sqrt{I(t)^2 + Q(t)^2} \quad (2.1)$$

$$\theta(t) = \arctan(Q(t)/I(t)) \quad (2.2)$$

The gate of the switching PA is driven with the phase information  $\theta(t)$ , and the supply voltage is modulated to control the amplitude.

A disadvantage of the polar transmitter architecture is that it requires a high-bandwidth, high-power amplifier in the amplitude path to supply power to the output. The bandwidth requirement for this amplifier is somewhat above that of the signal bandwidth due to frequency spreading caused by the nonlinear transformation from  $I, Q$  to  $A$  [41]. Thus for a wideband transmitter, the problem of designing a linear, efficient power amplifier is not avoided by using a polar architecture. Nonetheless, the drain modulator does not have as strict bandwidth requirements as the original RF PA, and the architecture allows for alternative approaches such as  $\Delta\Sigma$  modulation [6]. Finally, the decomposition of the RF input introduces a need for accurate time alignment between the two dissimilar paths, which generates some amount of practical difficulty.

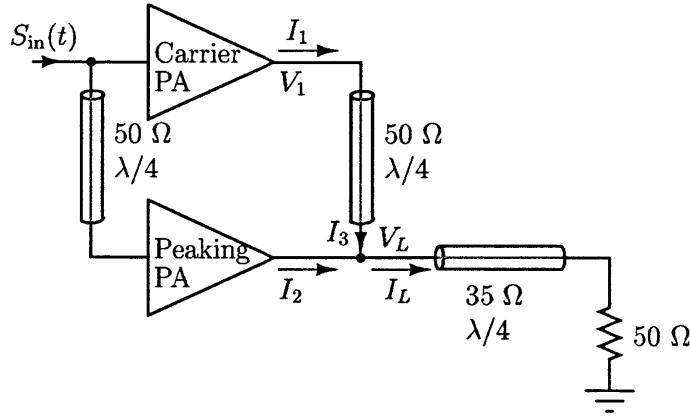


Figure 2-2: The Doherty power amplifier architecture. A 50- $\Omega$  load impedance is assumed.[40]

## 2.2 Doherty Power Amplifier

The Doherty power amplifier, shown in Figure 2-2, combines the output of a switching PA, the “carrier amplifier,” and a linear “peaking amplifier” for an overall-linear behavior [11]. The two PAs are biased with different gate voltages so that the peaking (auxiliary) PA operates in Class-C mode, and the carrier (main) PA as Class B. When the input signal is small (low-power regime) only the Class-B PA operates. In this case, the peaking amplifier output looks like an open circuit, and the 50- $\Omega$  load impedance is transformed by the two quarter-wave lines into a 100- $\Omega$  load, assuming the impedances indicated in Figure 2-2. When the input signal becomes large enough, the peaking amplifier turns on and begins to provide current  $I_2$ . Because  $I_2$  and  $I_3$  add in phase, the effect of  $I_2$  is to increase the apparent load impedance at  $V_L$ . This increased load impedance is transformed into a decreasing load impedance at the carrier PA output. As the input signal increases to peak envelope power (PEP), therefore, the loading on the carrier PA decreases from 100  $\Omega$  to 50  $\Omega$ . The resulting efficiency curve is shown in Figure 2-3 for ideal amplifiers and matching networks [40].

The classic Doherty topology in Figure 2-2 can be extended to include more than two PAs for an increased range of output powers where efficiency is high. Both three- and four-way Doherty amplifiers have been demonstrated [34, 16]. Discrete supply modulation, where the drain voltage of the two power amplifiers is selected

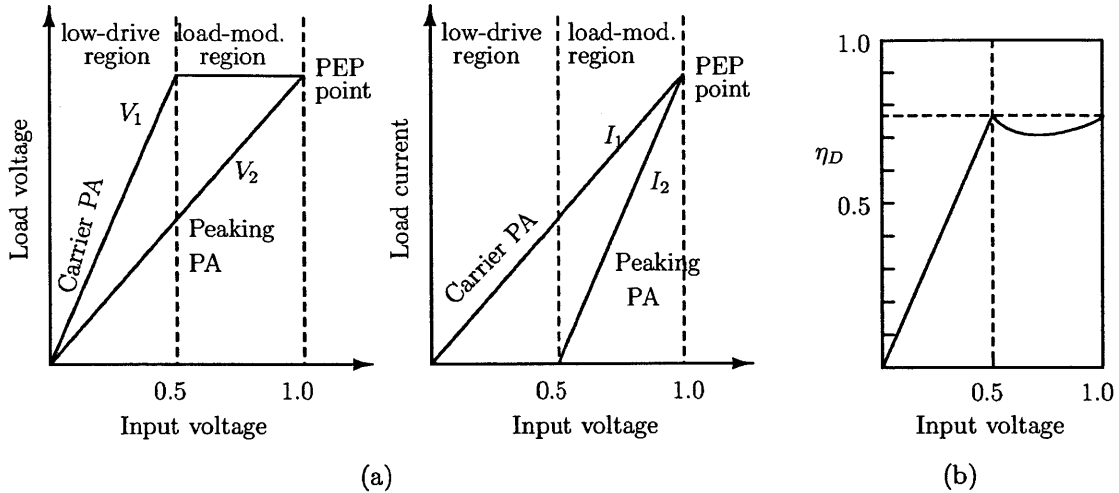


Figure 2-3: Doherty operating regions (a) and theoretical drain efficiency (b) [40].

from two levels depending on signal amplitude, can be used to further extend the range of high efficiency for low power amplitudes [26]. This technique is similar to multi-level LINC (see Section 2.3.2). Although Doherty PAs depend on quarter-wave transmission lines which have inherently narrow bandwidth, a Doherty amplifier with a fractional bandwidth of 35% (640 MHz bandwidth centered at 1.82 GHz) has been reported [2].

## 2.3 Outphasing

An outphasing approach eliminates the problematic high-bandwidth, linear power amplifier of the polar architecture. Originally described by Chireix in the 1930's [5], this technique is also known as "Linear amplification with Nonlinear Components" (LINC) [8]. The input signal is decomposed into two constant-amplitude, phase-modulated signals that are amplified and then passively recombined to produce an output signal that is an amplified version of the input. The overall characteristic of a outphasing transmitter can be made linear even when the PAs themselves are nonlinear switching amplifiers.

The block diagram in Figure 2-4 shows an outphasing transmitter using an isolating combiner. In this system the input signal  $S_{in}$ , represented by the dot in Figure

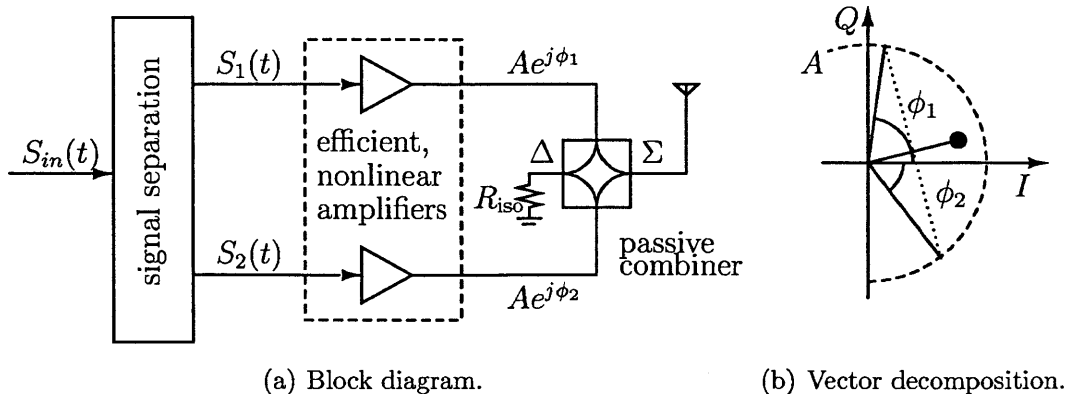


Figure 2-4: Generalized outphasing transmitter architecture.

2-4(b), is decomposed into two vector signals  $S_1(t)$  and  $S_2(t)$  which are amplified by efficient but nonlinear amplifiers to constant envelope signals with amplitudes  $A$  and phases  $\phi_1(t)$  and  $\phi_2(t)$ . The outphasing angle is defined as the angle between these two vectors,  $\psi(t) = \phi_1(t) - \phi_2(t)$ .

An isolating power combiner has a constant resistive impedance at its input terminal regardless of the phase of the signal at the other input and provides constant  $50\text{-}\Omega$  loading to each of the individual PAs. The components of the two inputs that are in phase are added and go to the sum ( $\Sigma$ ) output of the combiner; the components with opposing phase are delivered to the isolation resistor  $R_{iso}$  at the difference ( $\Delta$ ) output. Since each PA operates at a constant power level, the sum of the powers delivered to the  $\Sigma$  and  $\Delta$  loads must be constant. As a result, the efficiency drops off as output power is decreased, i.e. as the outphasing angle increases. Figure 2-5 captures this efficiency performance when ideal ( $\eta_D = 100\%$ ) PAs are used.

### 2.3.1 Chireix Outphasing

The Chireix combiner is an outphasing approach that uses a lossless, non-isolating combiner [5]. A Chireix combiner presents a load impedance to each PA that varies depending on the outphasing angle. The real component of the PA load impedance varies directly with the commanded power level and determines the amount of power delivered to the load. The reactive part of the PA load impedance is zero for at most

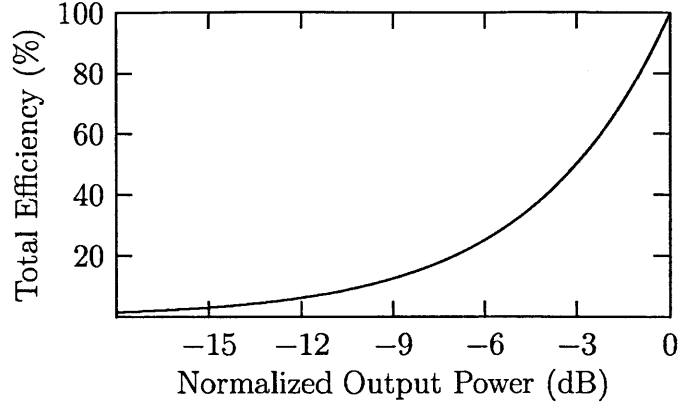


Figure 2-5: Ideal efficiency curve for outphasing transmitter with isolating combiner over a range of power output levels and ideal ( $\eta_D = 100\%$ ) PAs.

two outphasing angles, determined by the two components  $+jX$  and  $-jX$  shown in Figure 2-6. In general the PA performance will degrade as the reactive component deviates from zero. The varying reactance has the further drawback of giving rise to large reactive currents.

From the derivation in [18], the load impedance to one PA varies with outphasing angle  $\phi$  as

$$Y_{in,1} = \frac{1}{jX} + \frac{j \sin(2\phi)}{R_L} + \frac{2 \sin^2 \phi}{R_L} \quad (2.3)$$

and the efficiency as

$$\eta = \left[ \sqrt{1 + \frac{1}{4} \left( \frac{2 \sin(2\phi) - R_L/X}{\sin^2(\phi)} \right)^2} \right] \quad (2.4)$$

The plots in Figure 2-7 show the variation in load impedance and efficiency for different choices of  $R_L$  and  $X$ . It can be seen from this figure that there is a tradeoff between the power range over which efficiency is high, and the load reactance over that range.

The reactive loading of the PAs in the Chireix architecture can be mitigated by modulating the PA output matching networks with the outphasing angle. In [33], capacitive banks are used to compensate for reactive PA loading on a sample-by-sample basis to improve the overall average efficiency of an outphasing system.

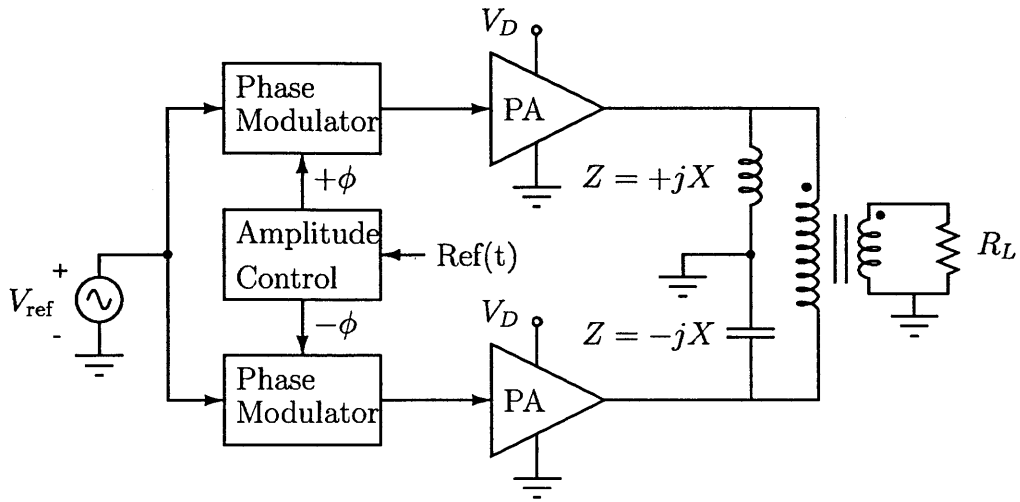


Figure 2-6: Chireix architecture

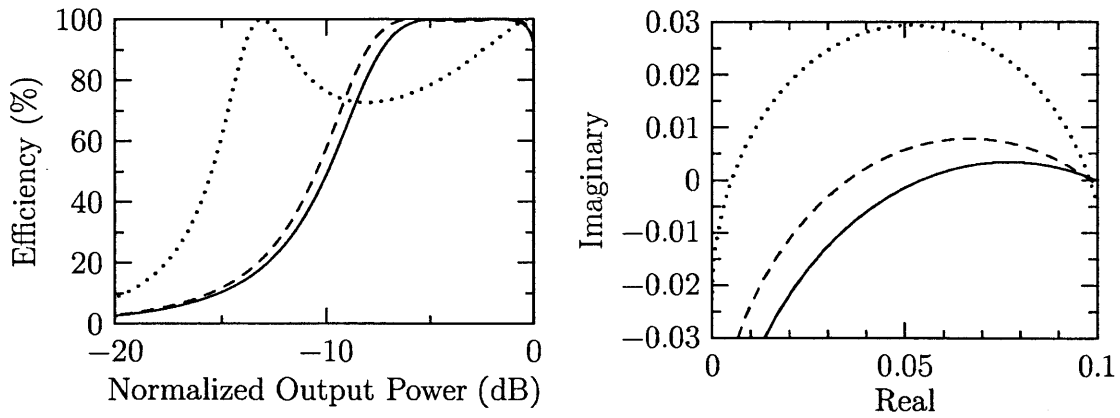


Figure 2-7: Chireix combiner behavior with  $R_L = 13 \Omega$ ,  $X = 13.6 \Omega$  (solid);  $R_L = 15 \Omega$ ,  $X = 17 \Omega$  (dashed); and  $R_L = 19.4 \Omega$ ,  $X = 45 \Omega$  (dotted).

For this and other outphasing architectures, the output dynamic range can be augmented by backing off the PA drive into Class-B operation at lower power levels. By transitioning to Class-B operation at output powers just below the power at which Chireix outphasing has its second efficiency peak (corresponding to the compensation angle determined by the chosen shunt reactances in the Chireix architecture) an extended dynamic range with improved average efficiency over pure outphasing can be achieved. The optimal power level for a transition from outphasing to Class-B operation can be found based on the PAR of the transmitted signal [39].

### 2.3.2 Multi-level LINC

The multi-level LINC architecture improves on basic outphasing by incorporating a simplified type of envelope tracking. The architecture is similar to the generalized outphasing type of Figure 2-4, but the supply voltage for the two power amplifiers can be switched between multiple discrete levels [4]. Whereas a polar/envelope tracking approach requires a (typically inefficient) wideband linear power amplifier for the PA drain voltage, for this architecture highly efficient DC-DC converters are used. For this and the Asymmetric Multilevel Outphasing architecture below, an isolating combiner is assumed.

Figure 2-8 shows the ML-LINC efficiency for an ideal system when four power supplies are used. The efficiency curve is made up of four LINC-like segments, with the peaks in efficiency corresponding to the output power levels for which the outphasing angle is zero. The dramatic improvement in average efficiency over LINC comes at the cost of a more complex system. In particular, ML-LINC requires precise time alignment of the dissimilar amplitude and phase paths.

In a nonideal system, the efficiency of the PA will generally degrade as the supply level is decreased, so that the efficiency peaks decrease in magnitude as the output power level is decreased. A reduced power supply is nonetheless favorable in terms of total system efficiency over a large outphasing angle.



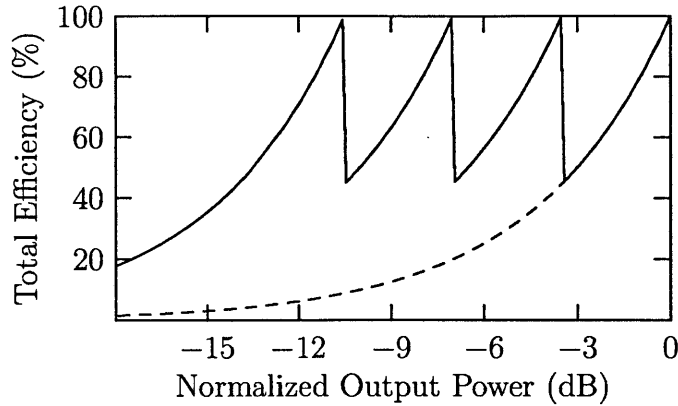


Figure 2-8: Efficiency of ML-LINC transmitter when four supply levels are used (solid), compared to basic outphasing (dashed).

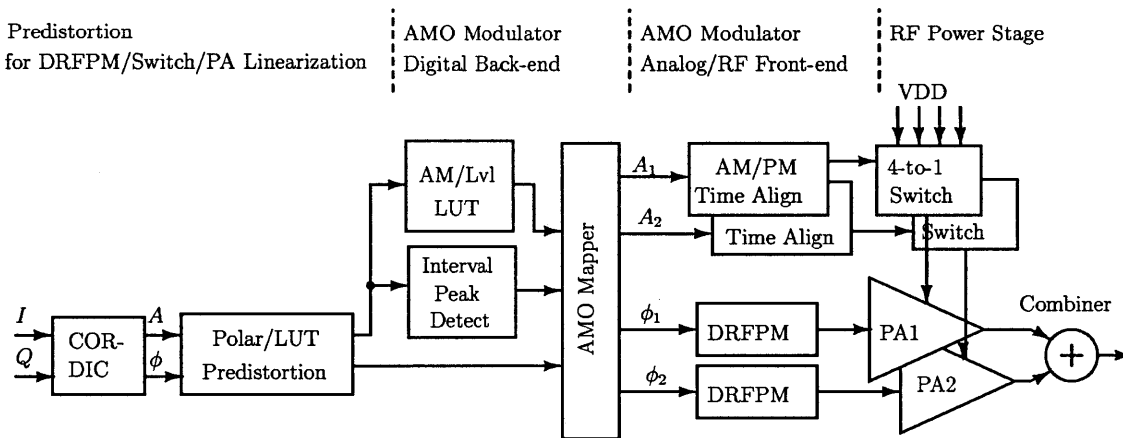


Figure 2-9: The complete AMO architecture.

## 2.4 Asymmetric Multilevel Outphasing

The AMO architecture employs a strategy similar to ML-LINC, but the power supply levels are not constrained to be equal. A detailed AMO block diagram is shown in Figure 2-9, including the coordinate rotation digital computer (CORDIC) and digital predistortion required to correct for and linearize different PA behavior at different supply levels.

Asymmetrically controlling the supplies increases the number of points of peak efficiency over the ML-LINC system as the output power level changes. Although the two supply levels could take on any combination of values, it is practical to limit the

possibilities to either adjacent or equal supply levels. This limit is chosen both because the combiner efficiency depends on the difference in amplitude of the two inputs as well as to reduce the complexity of the digital predistortion. The resulting efficiency curve is plotted in Figures 2-10 and 2-11. Figure 2-10 reflects the loss in the combiner when different supply levels are used; all other system components are assumed to be ideal. The system measurements in Figure 2-11 are reproduced from [14] and show that the efficiency peaks are limited by the PAE of the PAs over the supply voltage range. Also shown in this plot is a probability density function for a typical WLAN signal. The AMO supply levels have been chosen so that the efficiency peaks coincide with high probability output power levels for maximum average efficiency. The comparison of vector decompositions for LINC, ML-LINC, and AMO in Figure 2-12 indicates the efficiency advantage of the AMO architecture: for the same output vector, AMO uses the smallest outphasing angle.

Experimental systems demonstrating the AMO architecture for wireless communications were developed both in CMOS and with discrete GaN HEMTs [13]. The CMOS version delivers 27.7 dBm peak output power and a drain efficiency of 31.9% for a 20-MHz WLAN OFDM signal with 7.5-dB PAPR. The discrete prototype was implemented with class-E GaN PAs, targeting a radio basestation (RBS) application. It delivers 42.6 dBm peak output power at a 1.95-GHz carrier, and has a drain efficiency of 42.8% for a 16-QAM signal with 20-MHz signal bandwidth. The AMO architecture is a topic of ongoing research in the Dawson group, with particular focus on improving the behavior around supply voltage transitions, as well as applying the technique to higher (45-GHz+) carrier frequencies.

## 2.5 Resistance Compression Networks for Power Recovery

A resistance compression network (RCN) is a class of matching networks that can be used to reduce the load sensitivity in a resonant power amplifier [20]. Although not

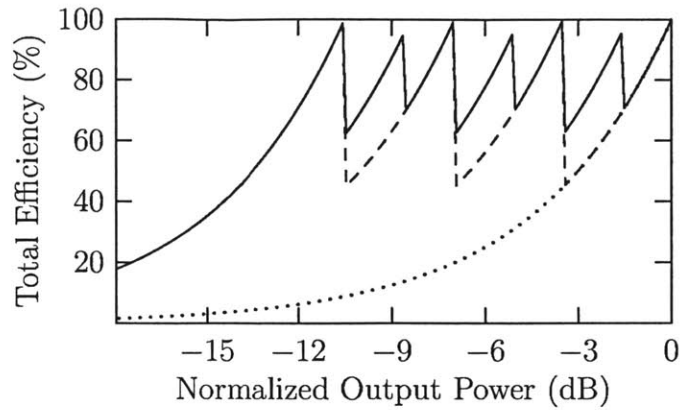


Figure 2-10: Ideal efficiency of AMO transmitter when four supply levels are used (solid), compared to ML-LINC (dashed) and basic outphasing (dotted).

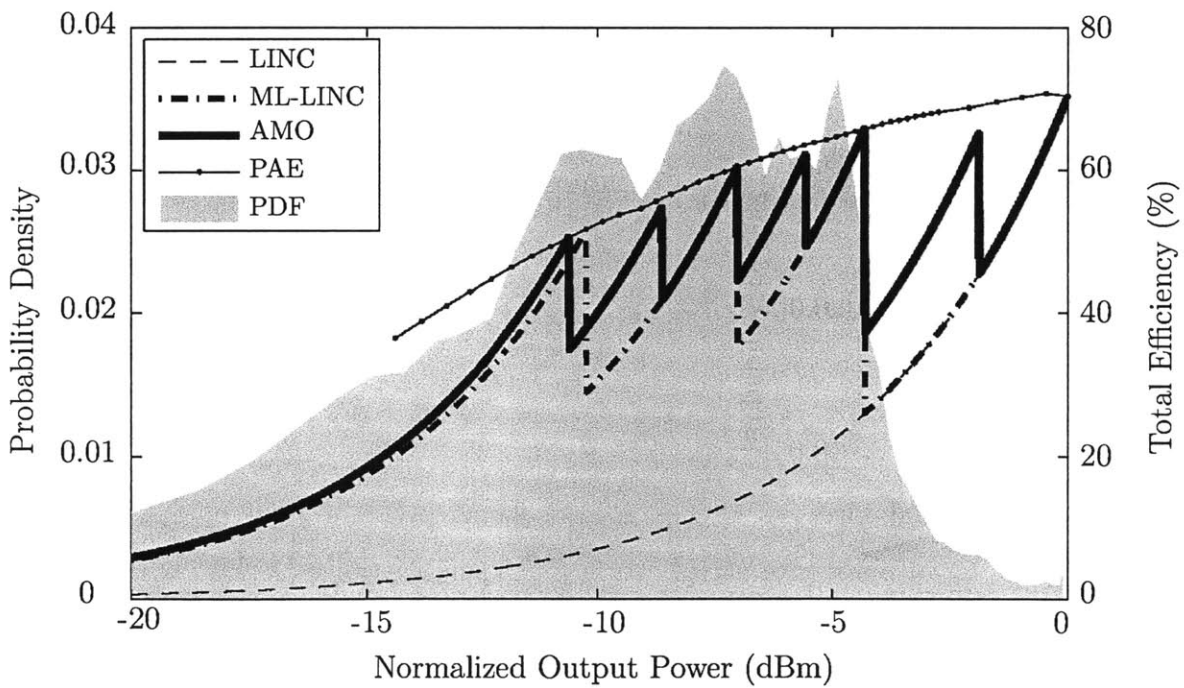


Figure 2-11: Comparison of LINC, Multilevel-LINC, and AMO efficiencies for the AMO prototype, including the effect of supply voltage backoff on the PA power added efficiency. A WLAN power level probability density function is included for comparison.

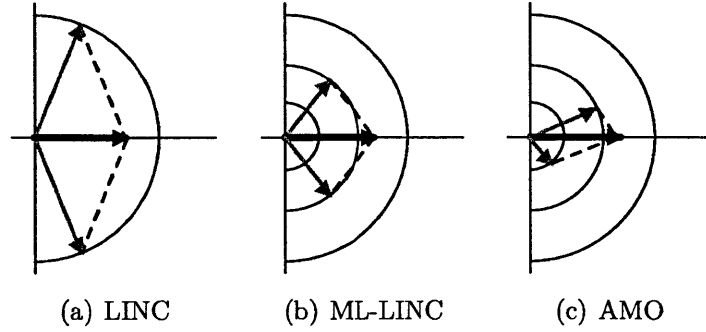


Figure 2-12: Baseband vector decomposition comparison between (a) LINC, (b) ML-LINC, and (c) AMO architectures.

itself a power amplifier, it is included here because it can be used to mitigate some of the drawbacks of an isolating outphasing transmitter. The RCN is also closely related to the new outphasing combiner presented in this work. One application is described in Section 2.5.2.

### 2.5.1 Resistance Compression Network

The input impedance of the RCN in Figure 2-13 at the operating frequency can be found to be

$$Z_{in} = (R_0 + jX) || (R_0 - jX) = \frac{R_0^2 + X^2}{2R_0} \quad (2.5)$$

As the two identical load resistances  $R_0$  are swept over a range centered on  $X$ ,  $[X/b, bX]$ , the input resistance varies over a much smaller range  $[X, kX]$  where

$$b = k + \sqrt{k^2 - 1} \quad \text{and} \quad k = \frac{1 + b^2}{2b} \quad (2.6)$$

In a system with two identically-varying loads, this network can therefore be used to reduce the apparent load variation by a factor of  $b^2/k$ . For example, if  $R_0$  varies over a total range of 100:1 (i.e. if  $b = 10$ ), the input impedance varies only over a 5.05:1 range.

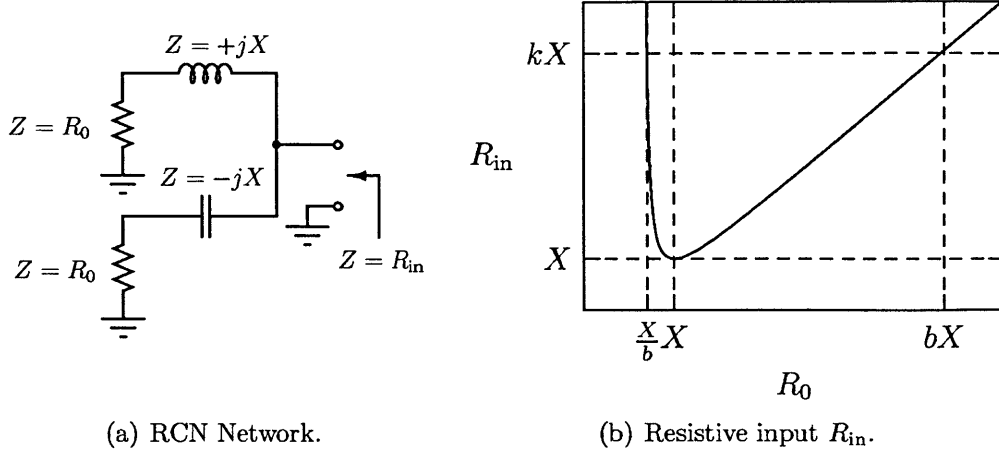


Figure 2-13: A single stage resistance compression network.

## Two-Stage Resistance Compression Network

Multiple resistance compression networks can be cascaded to increase the degree of compression. Following the methodology in [37], the two-stage RCN of Figure 2-14 can be designed to have an input resistance of  $R_{in,2}$  within  $\pm\Delta R$  of a desired median value  $R_{in,2,med}$  by selecting a value  $k_2$  of

$$k_2 = \frac{R_{in,2,med} + \Delta R}{R_{in,2,med} - \Delta R} \quad (2.7)$$

and a stage two reactance of

$$X_2 = \frac{2R_{in,2,med}}{k_2 + 1}. \quad (2.8)$$

This gives

$$R_{in,2,med} = \frac{k_2 + 1}{2} X_2 \quad \text{and} \quad \Delta R = \frac{k_2 - 1}{2} X_2. \quad (2.9)$$

Working backwards from the desired value for  $k_2$ , the corresponding value for  $b_2$  can be found from the relationship in Equation 2.6. With this  $b_2$ , the minimum value of  $R_{in,1}$  corresponds to the low end of the range of load resistor for the second stage; that is,

$$X_1 = \frac{1}{b_2} X_2 = \frac{X_2}{k_2 + \sqrt{k_2^2 - 1}} \quad (2.10)$$

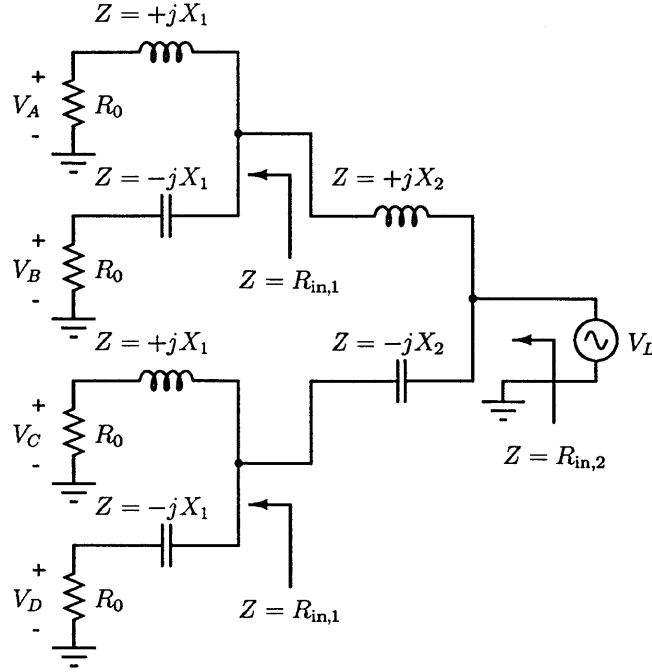


Figure 2-14: A two-stage resistance compression network, made up of three of the single-stage networks in Figure 2-13.

The maximum value of the input resistance to the first stage is  $R_{in,1} = k_1 X_1$ . Equating this value to the the maximum load to the second stage for which the desired degree of compression is attained, i.e.  $b_2 X_2$ , the value for  $k_1$  is found to be:

$$k_1 = \frac{b_2 X_2}{X_1} \quad (2.11)$$

The maximum range  $[X_1/b_1, b_1 X_1]$  for  $R_0$  for which the two-stage RCN input resistance is within  $\pm \Delta R$  of  $R_{in,2,med}$  is found using the relationship in Equation 2.6 and the expressions for  $X_1$ ,  $b_2$ , and  $X_2$  in Equations 2.10, 2.6, and 2.8, respectively. Figure 2-15 shows how the input resistance  $R_{in,2}$  varies as a function of load resistance  $R_0$ . An example of values achievable with this technique are  $(\Delta R)/R_{in,2,med} = 2.5\%$  for  $b_1^2 = 12$ ; that is, an input resistance within  $\pm 2.5\%$  of the median value for a 12:1 variation in the load resistance [20, 37].

The behavior of the load voltages  $V_A - V_D$  at the resonant frequency can be shown

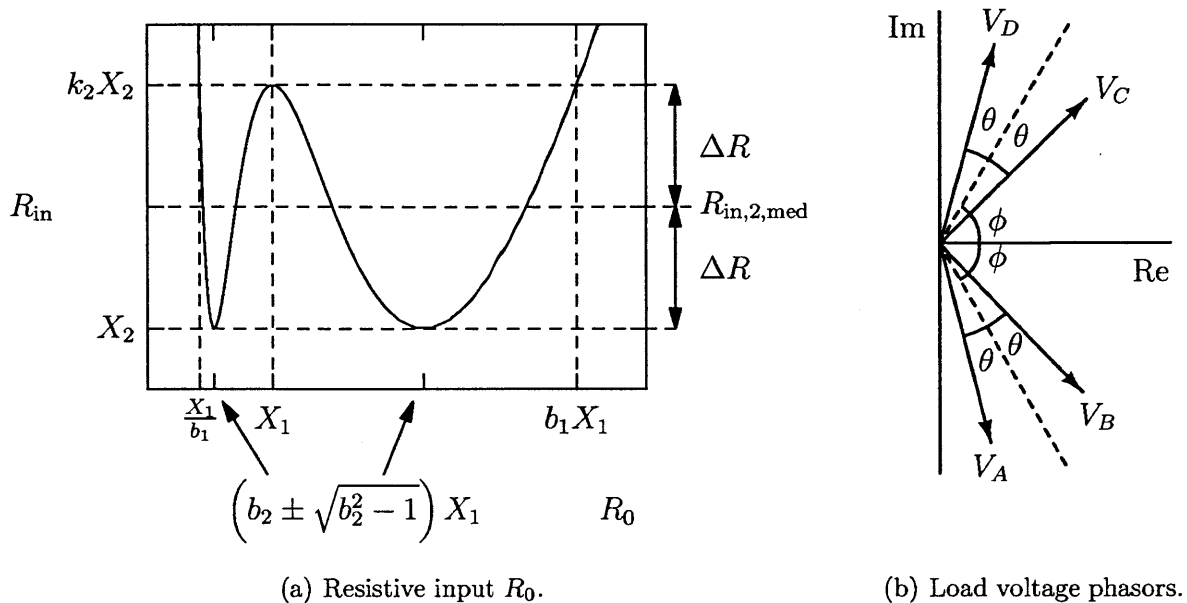


Figure 2-15: Input resistance and load voltage phasors for the two-stage resistance compression network.

to be [37]

$$\begin{bmatrix} V_A \\ V_B \\ V_B \\ V_D \end{bmatrix} = V_L \frac{\sqrt{R_0^2 + X_1^2}}{2\sqrt{\left(\frac{R_0^2 + X_1^2}{2R_0}\right) + X_2^2}} \begin{bmatrix} e^{-j\phi} e^{-j\theta} \\ e^{j\phi} e^{-j\theta} \\ e^{-j\phi} e^{j\theta} \\ e^{j\phi} e^{j\theta} \end{bmatrix} = V_S \begin{bmatrix} e^{-j\phi} e^{-j\theta} \\ e^{j\phi} e^{-j\theta} \\ e^{-j\phi} e^{j\theta} \\ e^{j\phi} e^{j\theta} \end{bmatrix} \quad (2.12)$$

where

$$\theta = \arctan\left(\frac{2R_0 X_2}{R_0^2 + X_1^2}\right) \quad \text{and} \quad \phi = \arctan\left(\frac{X_1}{R_0}\right). \quad (2.13)$$

The relationship among these voltages is shown in Figure 2-15(b).

## 2.5.2 Power Recovery

In an outphasing architecture, the advantage of an isolating combiner is that it presents a constant load impedance to each PA, regardless of the state of the other PA. This constant load impedance is critical to the operation of switched-mode RF

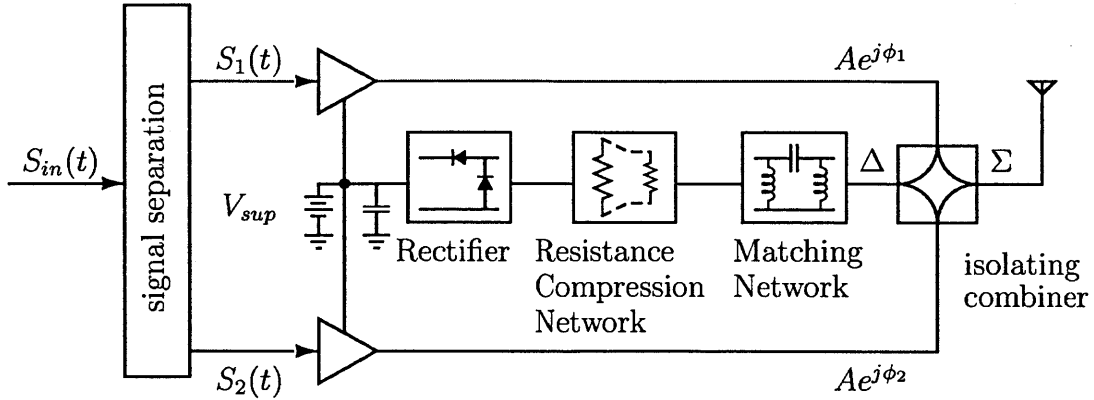


Figure 2-16: Outphasing transmitter architectures with isolating combiner and power recovery.

power amplifiers (e.g. classes E, F,  $\Phi$ , etc.). On the other hand, it results in an inefficient outphasing system because the constant load necessarily means that the power amplifiers are each operating at a constant power level even as the outphasing angle increases. In order to counteract the poor efficiency of an isolating combiner outphasing system, a power recycling technique replacing the isolating resistor with a rectifier was proposed in [28]. Because the input impedance to the rectifier depends on the amplitude of its input, however, this topology reduces the effectiveness of the combiner as an isolating block. As a result, the topology can lead to inefficient operation and nonlinearity in the PAs. The outphasing energy recovery architecture (OPERA) system shown in Figure 2-16 includes a RCN to minimize the variation in the impedance seen at the  $\Delta$  terminal of the combiner [15].



## Chapter 3

# Digital to RF Phase Modulator

A phase modulator is a necessary building block for the polar and outphasing transmitter architectures described in Chapter 2. The maximum signal bandwidth of these transmitters is determined by that of the phase paths and the amplitude paths, if they exist. The high-bandwidth digital-to-RF phase modulator (DRFPM) presented in this work is designed to enable wideband communications systems using outphasing-type architectures. With AMO-like applications in mind, its key requirements are 1) driving a switching PA, and 2) high sample rate ( $> 200$  MSPS). Phase modulator sample rate is especially important in outphasing applications because the phase signal is significantly bandwidth expanded due to the nonlinear transformation from an  $I/Q$  representation to amplitude/phase.

The role of the phase modulator is to take a digital phase command and produce a phase-shifted sinusoid at the carrier frequency. The two primary options for phase modulator design are phase-locked loops (PLL) and phase interpolation. A combination of these techniques is also possible [22]. A phase-locked loop (PLL) is a classic feedback system and has all of the advantages of a feedback-based architecture. This approach tends to have a bandwidth limitation, however, which makes it impractical for high-bandwidth communications. Phase-interpolation DRFPMS operate on the principle of vector summation, where a signal with arbitrary phase is generated by summing weighted components of sine and cosine of the carrier. This type of phase modulator can be implemented using two digital-to-analog converters (DACs) and

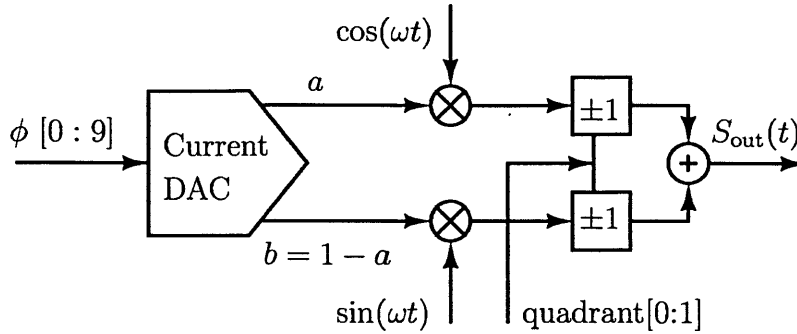


Figure 3-1: Phase modulator block diagram. The phase-modulated signal is  $S_{\text{out}} = \pm a \cos(\omega t) \pm (1 - a) \sin(\omega t)$ , where coefficient  $0 \leq a < 1$  is controlled by digital input  $\phi[0 : 9]$ .

upconverting mixers in a structure nearly identical to an  $I/Q$  modulator.

### 3.1 Phase Modulator Overview

The implemented DRFPM uses the phase interpolation architecture shown in Figure 3-1. Weighting coefficients  $a$  and  $b$  are established using a single current-steering DAC. To generate a phase in any quadrant, the polarities of the sine and cosine components can be reversed. In order to produce an arbitrary phase output, the coefficients should in theory be able to take on any arbitrary value. In that case, two DACs would be used to convert the digital input command to the analog signal that weights the sine and cosine to be summed. The coefficients in this single-DAC design are instead constrained such that  $b = 1 - a$ . With this constraint, each one of the current sources in the DAC is steered to contribute to either  $a$  or  $b$ . The result is a linear approximation to the ideal circle as shown in Figure 3-2. The digital input corresponds to the value of  $a$ , and the output phase is

$$\phi_1(a) = \tan^{-1} \left( \frac{1 - a}{a} \right)$$

This architecture has several advantages. With only one DAC used, the required area and power are essentially halved. The number of current sources which must

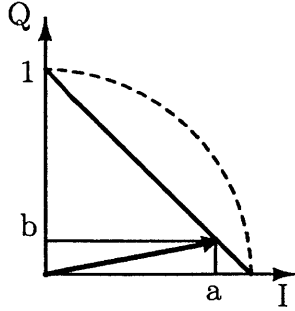


Figure 3-2: The constraint  $b = 1 - a$  results in a linear approximation to the ideal circle.

be matched is therefore also halved. Furthermore, since  $b$  is constrained to be a function of  $a$ , the digital input word length is also reduced. This approach is related to those used in [3] and [32] to reduce the number of required current cells over the more conventional approach of [22]. The relatively high phase resolution of this work as compared to [3, 32] enhances the area and power advantages of the single-DAC topology. The benefits come at the cost of linearity and accuracy; however, the loss of linearity can be corrected for by predistortion that is typically necessary for an RF transmitter. For instance, the AMO architecture relies on digital predistortion, making this strategic nonlinearity of the phase modulator acceptable within the larger system.

Figure 3-3 summarizes the three levels of vector decomposition that result when this phase modulator is used in an AMO system. At the highest level is the desired output vector with amplitude  $A$  and phase  $\phi$ . For AMO, this vector is decomposed into two outphased signals with independent amplitudes chosen from a discrete set of values:  $A_1 e^{j\phi_1}$  and  $A_2 e^{j\phi_2}$ . Then each of the two phases is generated by the DRFPMS as the sum of some  $a \sin(2\pi f_c t)$  and  $b \cos(2\pi f_c t)$ .

## 3.2 Core Circuit Design

The simplified DRFPM schematic is shown in Figure 3-4. The binary-weighted current sources are steered by latched differential switches to set up currents that will

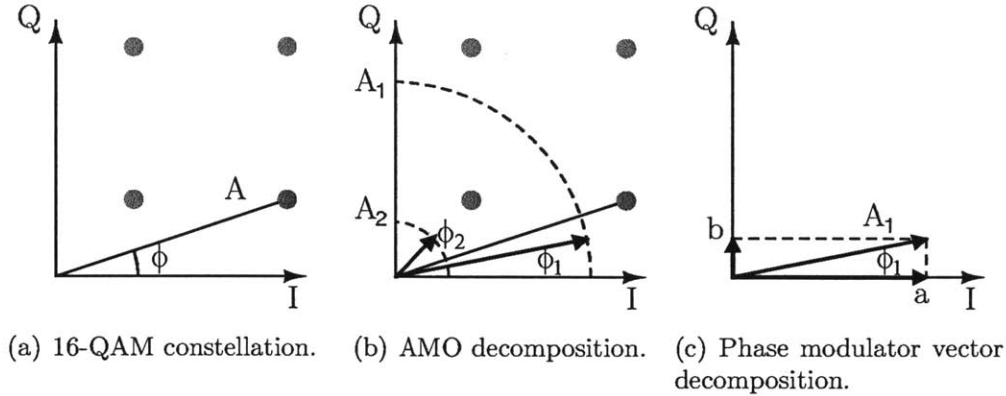


Figure 3-3: The multiple levels of vector decomposition in the AMO system with proposed phase modulator.

eventually correspond to coefficients  $a$  and  $b$ . Associated with each data switch output is a set of two differential switches that multiply by sine and cosine at the carrier frequency. The outputs of these mixers are combined, with the resulting currents  $I_{Ip}$  and  $I_{Qp}$  corresponding to the  $a \sin(2\pi f_c t)$  and  $b \cos(2\pi f_c t)$  from the theoretical discussion above. Note that these are now differential signals. The sign of the  $I$  and  $Q$  components is selected to determine the quadrant of the output using another set of latched differential switches. Finally, all the “positive” currents and all the “negative” currents are converted into voltages to produce a differential, phase modulated voltage. Because it is only the phase of this voltage that is relevant, not its amplitude, the signals are then put through a limiter, and ultimately used to drive the gate of the switching PA.

### 3.2.1 Current Source Array

The current sources are established as shown in Figure 3-5. They consist of identical unit transistors grouped in binary weighted numbers. The reference current is provided to a transistor with multiplicity eight, making  $I_{ref} = 8 \times I_0$  and allowing a relatively large  $I_{ref}$  to be provided by the off-chip source. A transistor of equal size generates  $I_{meas}$  for off-chip measurement. The phase modulator operates nominally with  $I_0 = 0.98 \mu A$  from the 1 V supply, resulting in a static power dissipation of 1mW

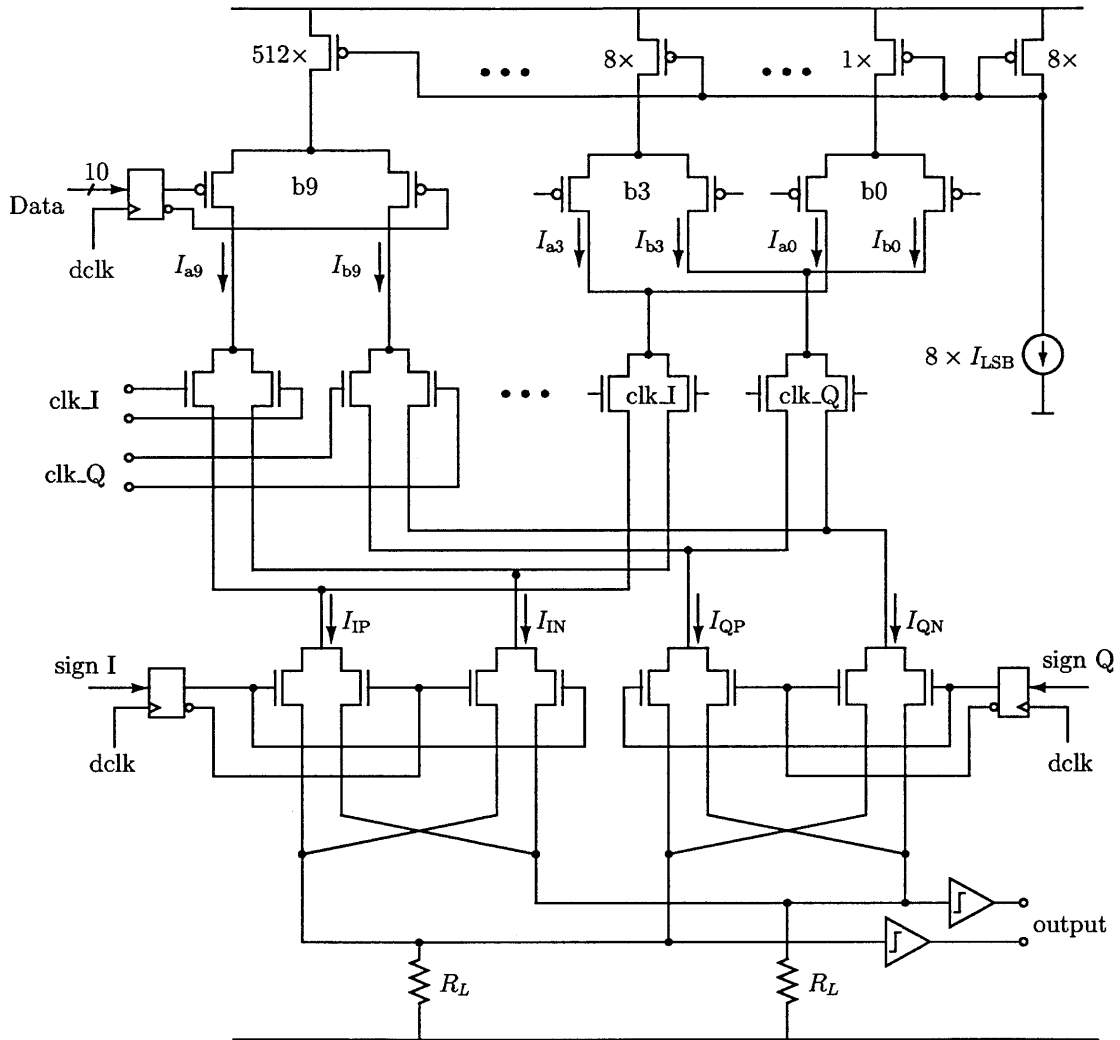


Figure 3-4: Simplified schematic of the fabricated phase modulator.

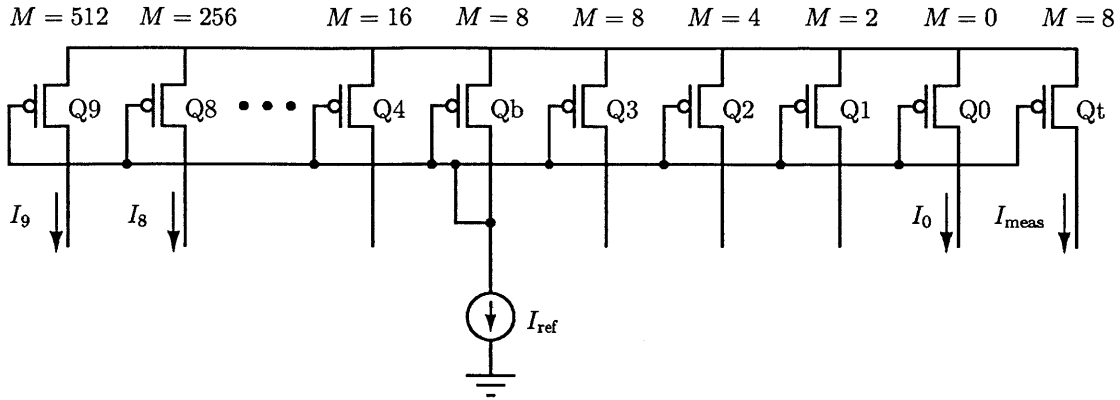


Figure 3-5: Current sources are generated by grouping unit transistors.

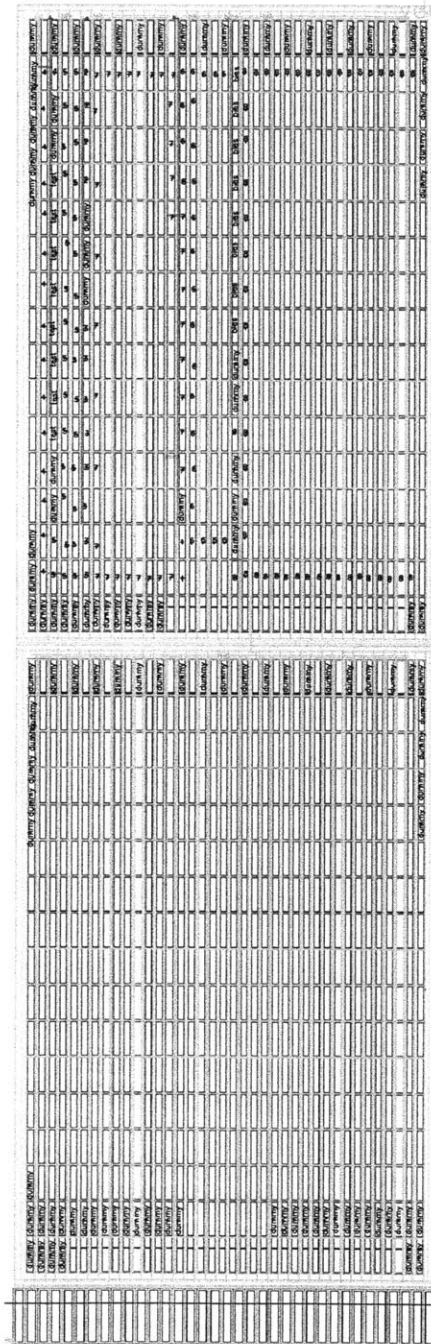
when other biasing circuitry is excluded.

The unit transistor is a low voltage threshold p-channel FET (device `pch_1vt`) with width  $20 \mu\text{m}$  and length  $4 \mu\text{m}$ . The largest possible device size given area limitations was used in order to maximize matching. The cell layout and approximate transistor distribution including dummy devices (indicated by grey areas) is shown in Figure 3-6. Interleaving the unit devices would produce better matching but would increase the routing complexity [10].

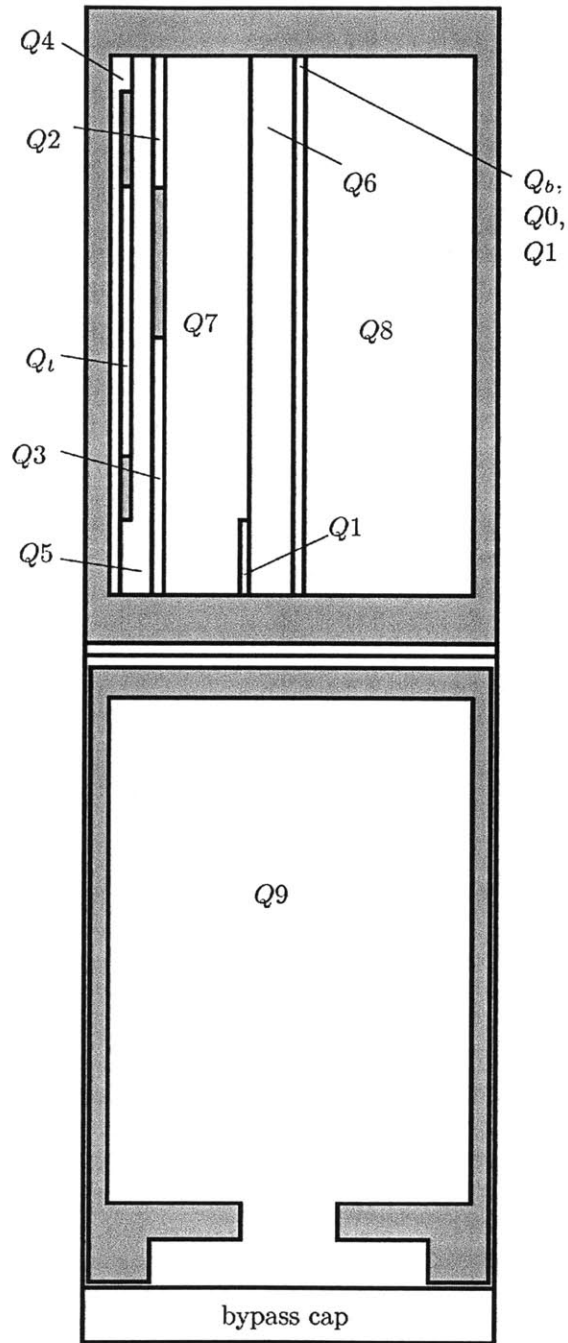
### 3.2.2 Data/Quadrant Switches and Latching

The data latching is implemented using the buffer-latch-switch topology from [10]. A schematic is shown in Figure 3-7. Weak inverters provide positive feedback to the latching structure. The quadrant selection latches have the same basic structure, but consist of two differential switches with outputs cross-coupled and inputs driven with signals of opposite sign. As indicated in Figure 3-4, this cross-coupling allows for the polarity of the input differential signal to be reversed.

When used as the DAC's current-steering switches, this differential switching topology provides a cascode-like effect for the current bias cell because the voltage at the source of the differential pair is nominally constant. In order for that voltage to be consistent across the current sources, the latches are scaled along with the current values. Scaling is accomplished by combining unit differential switches and



(a) Cell layout.



(b) Sketch of transistor grouping.

Figure 3-6: Current source array layout. The layout consists of 1292 unit transistors with width  $20 \mu\text{m}$  and length  $4 \mu\text{m}$ , grouped as indicated in (b).

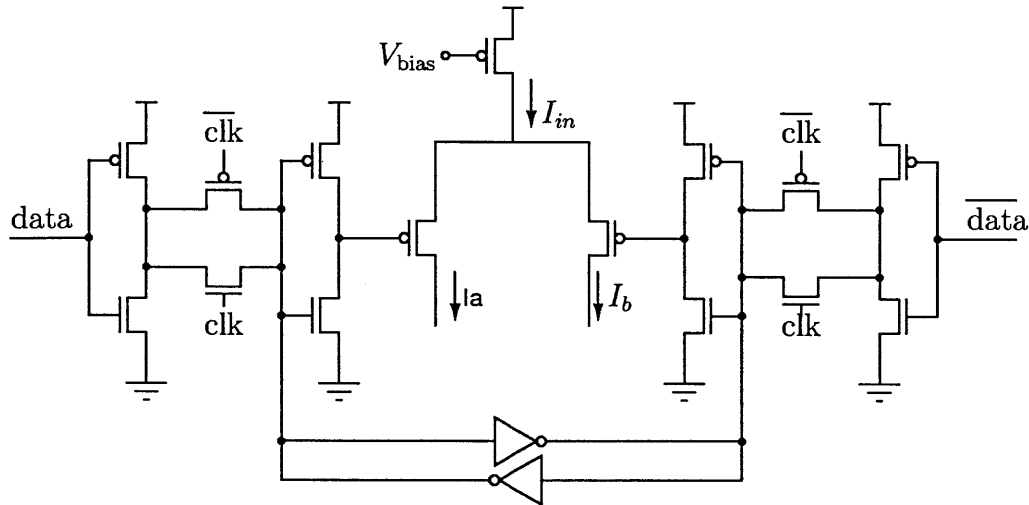


Figure 3-7: Latch structure used for data bits and quadrant selection

unit latches in binary weighted numbers. That is, the differential switch labeled b0 in Figure 3-4 is constructed of the unit cell shown in Figure 3-7, while switches b3 and b9 are constructed of 8 and 512 unit cells respectively. Figure 3-8 shows the layout image and organization sketch for these current-steering switches.

### 3.2.3 Multiplication by Carrier

The circuit that multiplies the DAC currents by the carrier is shown in Figure 3-9. As with the data switches and latches, the multiplicity of the differential switch pair is scaled with the current. For the carrier multiplication switches, however, the drain voltage does not need to be held constant to the same extent as for the data switches because the effect of this drain voltage on the value of the current source is limited. In order to reduce the area, one unit switching cell is used for the four least significant bit currents combined. For the higher-current bits, the unit cell is combined in binary-weighted values, with the MSB switches consisting of 32 parallel cells.

Square wave clocks are used for the multiplication since the small devices operate as switches rather than in the linear regime. Although the square wave approach introduces higher harmonics, they are attenuated by the inherent low-pass nature of



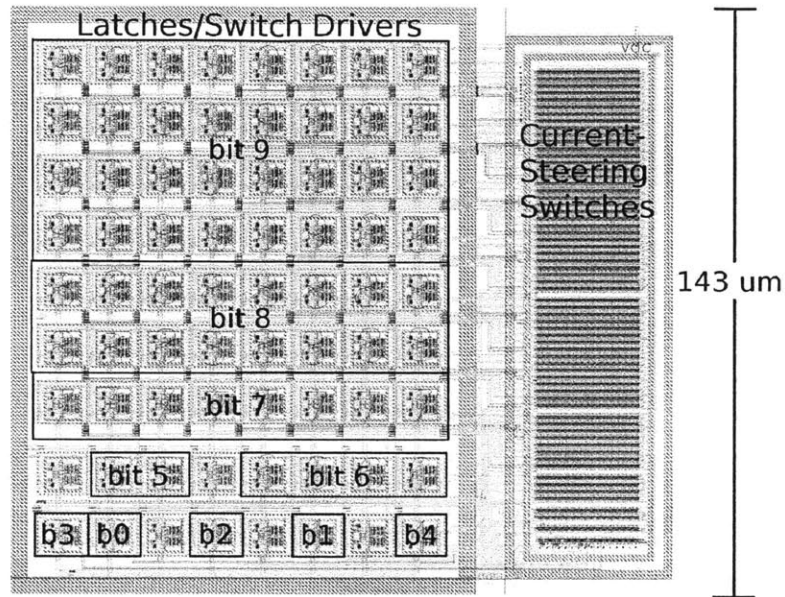


Figure 3-8: Current-steering switches and latches layout.

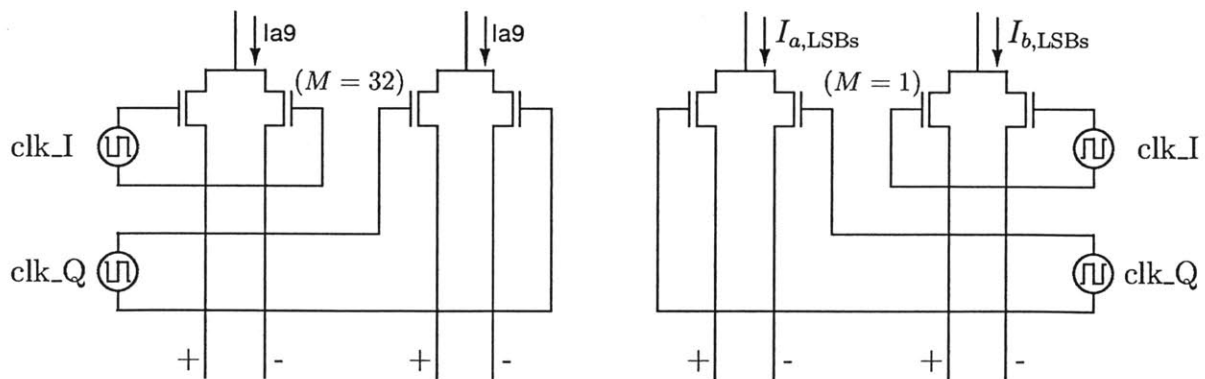


Figure 3-9: Carrier multiplication circuit detail for MSB and four LSB currents. The unit cell switches multiply the four LSB currents ( $I_{a,LSB} = I_{a0} + I_{a1} + I_{a2} + I_{a3}$ ). Higher bits use binary-scaled multiplicities, with a  $32\times$  multiplicity switch for the MSB.

the signal path.

The phase modulator topology can support a range of carrier frequencies around the nominal 2.5-GHz carrier frequency because it does not rely on tuned filters. In practice, the frequency range was constrained by external system elements, such as those used to convert the signal from the RF source to differential quadrature signals.

### 3.3 Clock Prerotation

One disadvantage of the phase-interpolation strategy used in this design is that it is difficult to produce output phases close to the quadrant boundaries ( $0^\circ$ ,  $90^\circ$ , etc.). In both single- and dual-DAC topologies, the smallest phase that can be produced is limited by the smallest weighting current  $I_A$  or  $I_B$ . Nonideal effects such as device leakage and carrier feedthrough can contribute an offset current to a weighting current even when its data input is set to zero. For example, simulation indicates that the total leakage current in this design is 0.10% of the combined current from the sources. That is, when the input bits are all value 1 and the clocks at the data switching frequency and the carrier frequency are omitted, the net current to the two load resistors are 0.983 mA and 1.012  $\mu$ A. This total leakage is nearly identical to an LSB of the current source DAC, and is therefore a non-negligible source of error. Carrier feedthrough, in which the drive signal for the carrier multiplication switches couples into the signal path, is another significant source of error in the output phase.

One solution to this output “dead zone” problem, used by Zhen Li in his 45-GHz DRFPM design, is to intentionally introduce negative carrier feedthrough by including dummy switches as shown in Figure 3-10 [30]. The devices can be sized to guarantee overlap at the quadrant boundaries, as indicated schematically in Figure 3-10, by increasing the phase range at quadrant boundaries by  $\Delta\theta$ . At the same time, the carrier injection should be limited so that the phase resolution over the quadrant is not excessively reduced.

For this work, a clock rotation technique was attempted as an alternate solution to the missing codes. Two sets of quadrature carrier signals are generated, one delayed

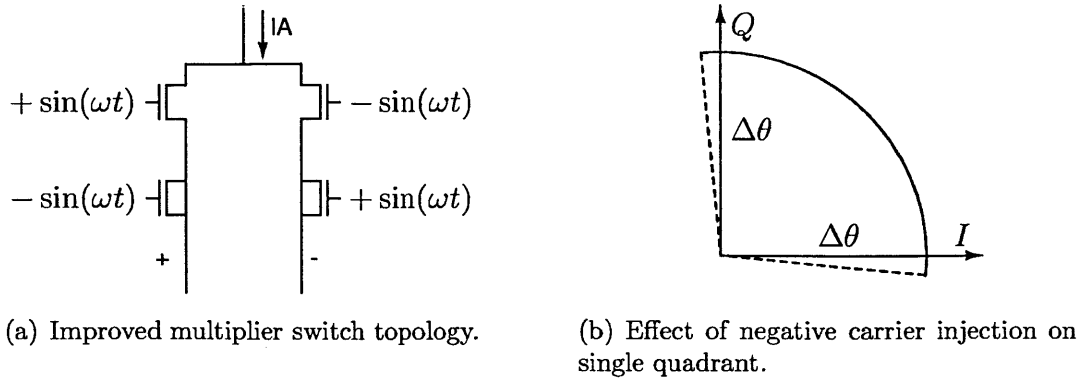


Figure 3-10: One solution to the dead zone problem inherent to high-accuracy phase-interpolation DRFPMs [30].

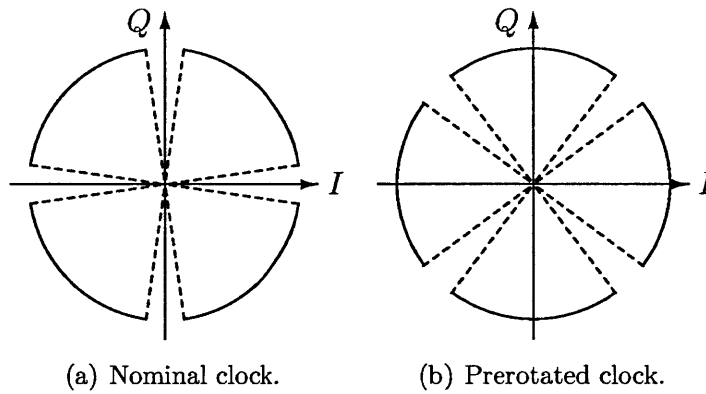


Figure 3-11: By providing two reference angles, the range of output phases is made continuous despite missing codes.

(“prerotated”) with respect to the other by approximately 45 degrees. Multiplexers are used to select between the two discrete phase rotations. By thus providing two reference phases, any output phase can be produced. The sketch in Figure 3-11 captures the effect of the clock prerotation.

Clock pre-rotation is implemented using the circuits shown in Figure 3-12. Pre-rotated versions of the carriers are generated using the same  $IQ$  modulation principle as in the phase modulator itself. The two circuits in Figure 3-12(a) and (b) perform vector addition and subtraction, respectively, of the input carriers. The clock for the phase modulator is then selected using a latched input to muxes for the  $I$  and  $Q$  carriers. The digital balun is a cross-coupled inverter structure that converts from a

single-ended to differential signal and enforces a 50% duty cycle. The clock treatment using single-ended signals in this way is more susceptible to phase noise than a fully differential circuit. This design was based on the availability of single-ended building blocks.

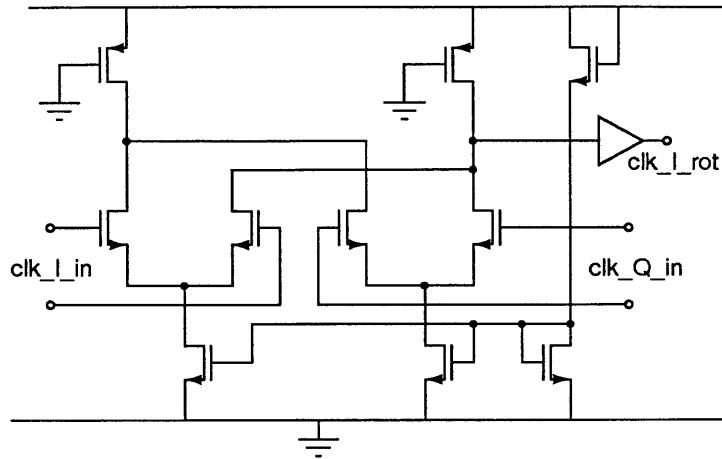
Although this pre-rotation scheme performed as expected in static tests, there was a timing mismatch between the pre-rotation switching and the other data bits that caused glitches in the output phase. Thus, prerotation was not used for dynamic measurements.

### 3.4 Additional Blocks

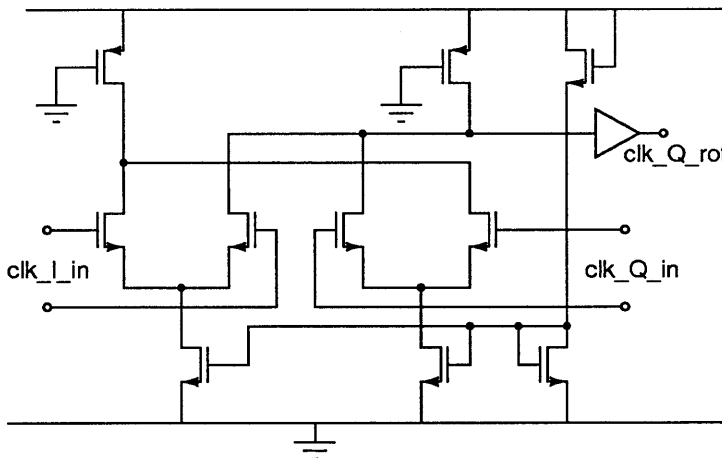
A number of additional blocks are included on-chip for configuration and data I/O. These blocks were designed in collaboration with Sungwon Chung and Philip Godoy.

Carrier clock input buffers receive differential in-phase and quadrature carrier signals generated using an RF source and off-chip 90° hybrid splitter. This off-chip signal generation approach allows for the two inputs to be tuned to adjust their relative phase. Data input buffers are designed for low-voltage differential switching (LVDS) and operation with a 200 MHz data clock. An on-chip shift register controls 8-bit DACs to set various bias voltages for the above I/O blocks.

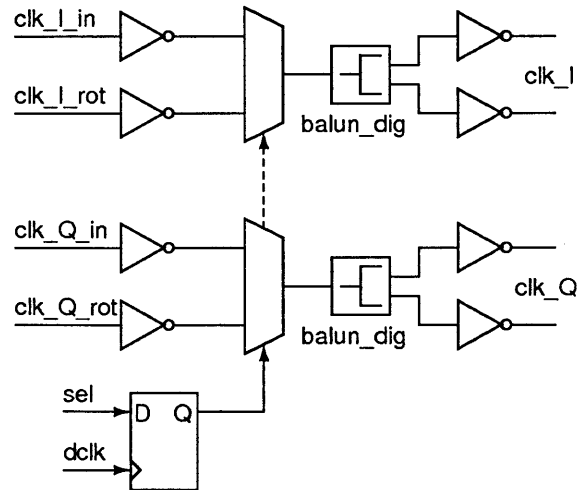
Also included is an output amplifier at the DRFPC output. A multiplexer selects whether the DRFPC output is connected to this output buffer or to an on-chip Class-E PA designed by Philip Godoy [13].



(a) Rotated  $I$  generation.



(b) Rotated  $Q$  generation.



(c) Clock selection.

Figure 3-12: Pre-rotation path, used to generate pre-rotated versions of  $I$  and  $Q$ .

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# Chapter 4

## DRFPM Experimental Results

This chapter describes the experimental setup and measured results for the DRFPM fabricated in 65-nm CMOS and occupying  $0.26 \text{ mm}^2$  on a  $2 \text{ mm} \times 2 \text{ mm}$  die. Also included on this chip is a Class-E PA designed as a part of the AMO outphasing system CMOS prototype, and used as an output amplifier for DRFPM testing. A die photo indicating the layout of the main blocks is shown in Figure 4-1. Unlabeled areas are occupied by circuits not relevant to the DRFPM testing.

### 4.1 Phase Modulator Measurement Setup

Figure 4-2 shows a block diagram of the experimental setup. An Opal Kelly 5010 development board with a Xilinx Virtex-5 FPGA provides the interface between the computer, where test signals and static predistortion are computed, and the DRFPM IC. Quadrature carrier signals are generated off-chip from an RF source and a  $90^\circ$  power splitter. The phase modulator output can be observed using either the on-chip PA or the output buffer. This measurement setup is used for both static and modulated tests. For outphasing measurements, a second chip is connected to the FPGA, and a connectorized Wilkinson combiner performs off-chip power combining.

For static measurements, the 13-bit input is swept and the output phase is compared to the reference signal from the RF source. The DRFPM output trace and a carrier reference signal are downloaded from the oscilloscope for computation in

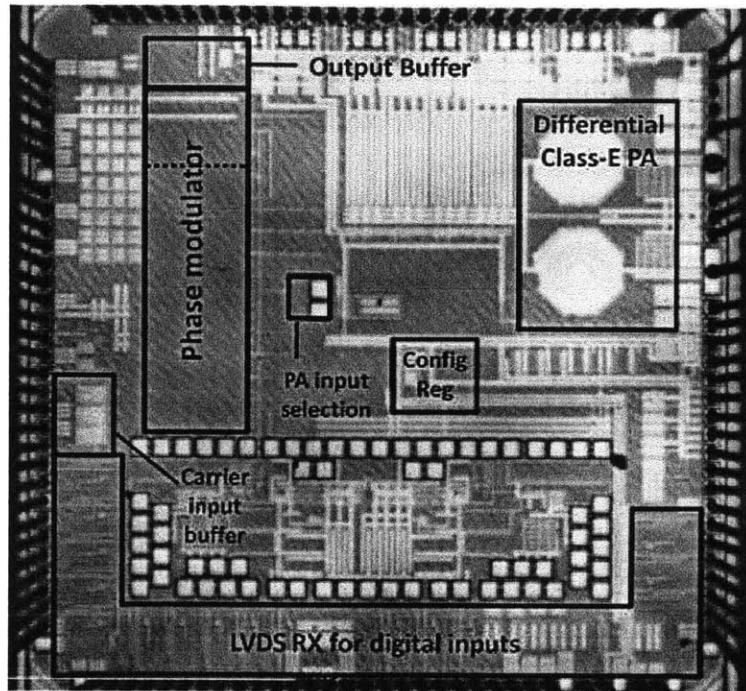


Figure 4-1: Die photo. The DRFPM consumes  $0.26 \text{ mm}^2$  on the  $2 \text{ mm} \times 2 \text{ mm}$  die. Unlabeled areas are occupied by circuits not relevant to the DRFPM testing.

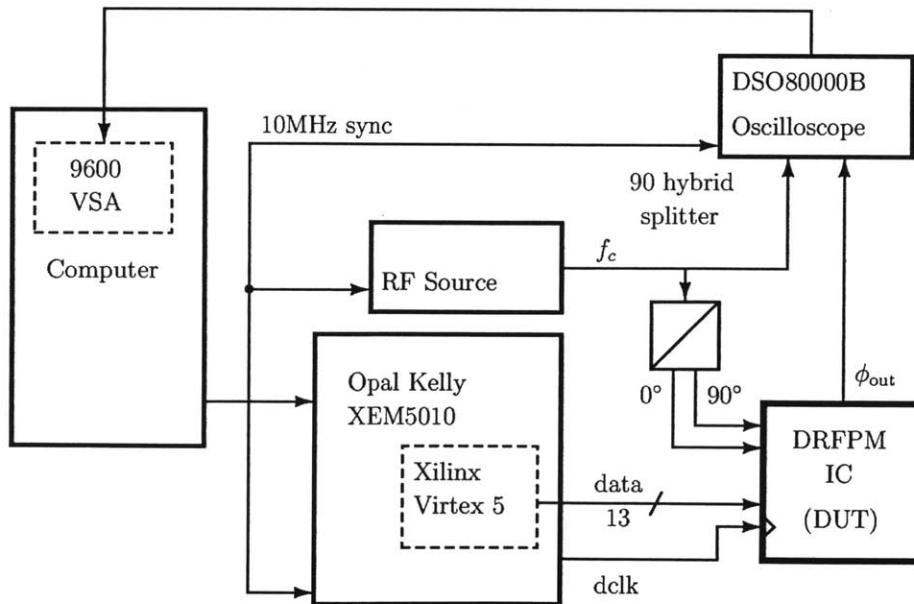


Figure 4-2: Block diagram of the experimental setup for the DRFPM chip.



MATLAB (see Section 4.3). For modulated tests, the oscilloscope is connected to the 9600 Vector Signal Analyzer (VSA) software on the computer through a GPIB interface. This software performs the demodulation and calculates spectrum and EVM for the output signal.

## 4.2 Carrier Frequency Operating Range

The DRFPM was designed to operate at a nominal carrier frequency of 2.5 GHz. As discussed in Section 3.2.3, however, the phase modulator core does not contain any inherently narrowband or frequency-specific circuits. The on-chip element limiting the upper limit carrier frequency range is the clock input buffer, including the parasitic effect of the bondwires and bondpads. A DC blocking capacitor in the clock input buffer sets the lower end of the frequency operating range. In practice, the range is further constrained by other elements in the measurement setup, namely the balun on the test PCB that converts carrier signals from single-ended to differential. With the nominally 2400-2500 MHz balun chosen for 2.5-GHz operation, the phase modulator operates over a measured range of 1.2-3.2 GHz. If a balun with nominal 3100-4900 MHz operating range is substituted in, the upper operating frequency (without pre-rotation) is 4.2 GHz. This limit is set by the 90 degree splitter whose frequency range is limited to 2000-4200 MHz. DRFPM characterization is performed for a 2.5-GHz carrier.

## 4.3 Static Measurement Results

Static measurements both characterize the linearity of the phase modulator and train the lookup table (LUT) used for the modulated tests. Measurements are made by sweeping the 13-bit data (12 bits phase data, 1 bit clock rotation) over all values, and recording the 1000× averaged, 40 GSPS oscilloscope traces of both the DRFPM output and reference signal from the RF source. For the 2.5 GHz carrier frequency, the sample rate of the oscilloscope is 16 samples per carrier period. A total of 128

datapoints per input command are recorded.

Once the dataset has been recorded, the phase for each input command is calculated in MATLAB. The DC offset is found from the DC component of the measured data FFT and is subtracted from the waveform. Both the DRFPM output and the reference signal are downconverted to  $I$  and  $Q$  baseband signals by multiplying by  $\sin(\omega_c t)$  and  $\cos(\omega_c t)$  respectively. Then, because the sample rate of the oscilloscope is a whole multiple of the carrier frequency, the average value of the downconverted  $I$  and  $Q$  signals can be used to calculate the phase of the DRFPM output with respect to the reference signal. A lookup table of input codes and phase outputs is recorded for static predistortion. This methodology relies on the agreement of the RF source and oscilloscope time bases, which are synchronized by a 10-MHz reference signal. Computing the phase of the reference carrier signal alleviates problems due to drift in phase over duration of this multiple-hour measurement.

An example DRFPM static phase measurement is shown in Figure 4-3. In Figure 4-3(a), the DRFPM output magnitude and phase are plotted over the entire range of inputs, including with clock prerotation. The outputs with the prerotated clock are scaled by 0.9 so that the phase gaps are visible. The most clearly visible gap in the unrotated output occurs near  $0^\circ$ . The prerotated output is continuous in this region but has a gap near  $45^\circ$ . The phase data is plotted in Figure 4-3(b) as a function of commanded input. Here, the nonlinear (tangent) behavior due to the single-DAC design is clearly visible. The different characteristics of quadrants one and three as compared to quadrants two and four and the locations of missing codes indicate that the carrier input signals are not exactly in quadrature.

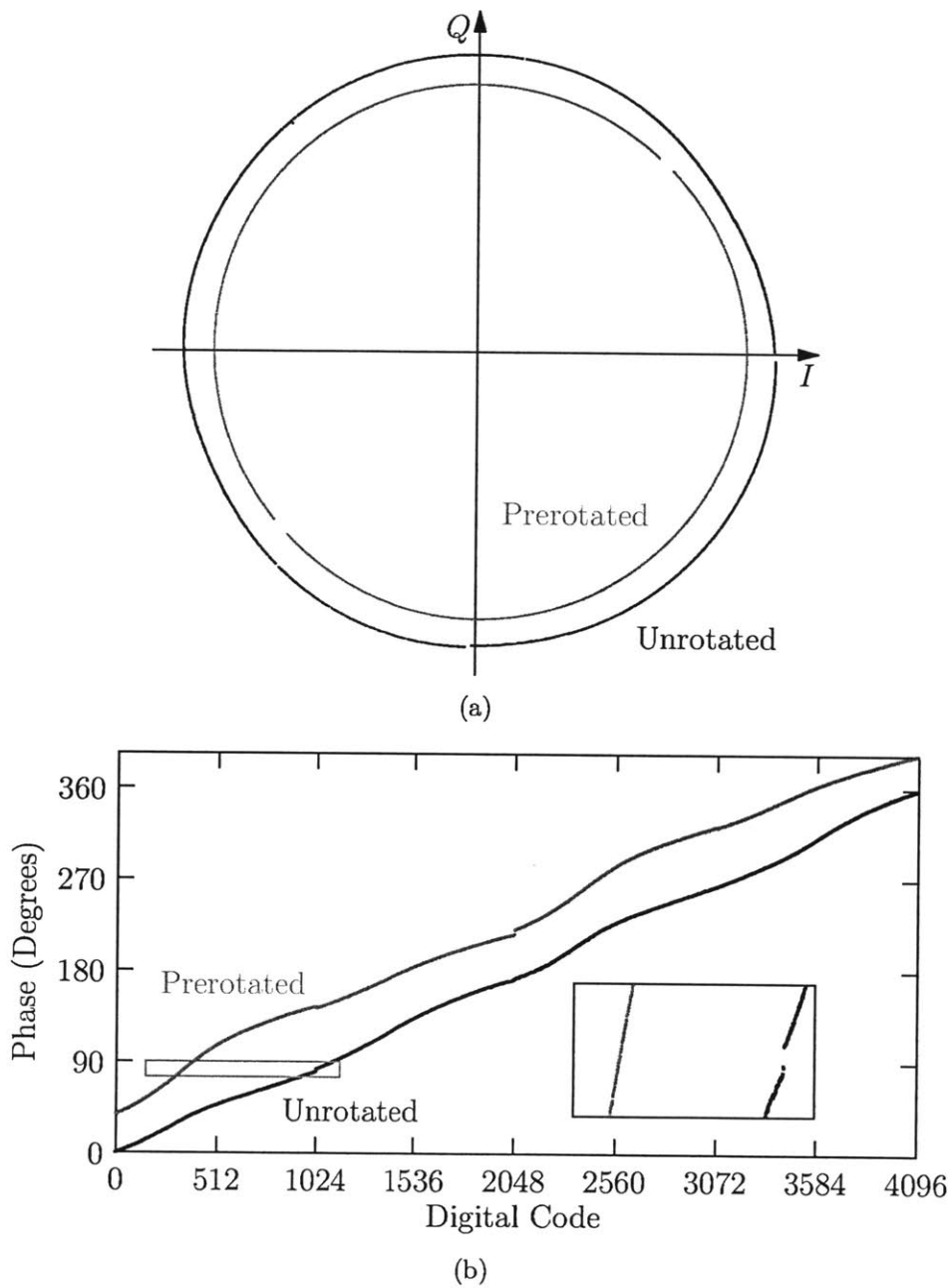


Figure 4-3: Phase modulator output over entire operating range. The pre-rotated data amplitude is scaled down in (a) so that phase gaps can be seen.

Table 4.1: Comparison of DRFPM performance with the state of the art.

<b>Parameter:</b>	<b>Carrier frequency</b>	<b>Measured sample rate</b>	<b>Phase resolution</b>	<b>Process</b>
<b>This work</b>	2.5 GHz	160 MSPS	12 bits	65 nm
<b>JSSC'09 [22]</b>	0.8-5GHz	50 MSPS	14 bits	90nm
<b>JSSC'09 [32]</b>	60 GHz	2.5 GSPS	6 bits	90 nm
<b>PRIME'09 [3]</b>	3.1-10.6 GHz	3.8 GSPS	4 bits	65 nm
<b>MTT'06 [42]</b>	1.75-3.5GHz	500 MSPS	4 bits	0.18 $\mu\text{m}$

Note: Power consumption figures are not available for refs. [22] and [32]. Power consumption is 2.78mW for ref [3], and 3.6mW for ref [42], compared with 1.9mW for this work.

## 4.4 Dynamic Performance

The dynamic performance of the DRFPM is characterized both through its step response and from its performance transmitting various modulated signals. Basic outphasing measurements are also demonstrated. The summary of results and comparison to other works in Table 4.1 indicates that this work represents performance on par with the state of the art in terms of its combination of sample rate and resolution. The 8-PSK measurement described in Section 4.4.2 is used to determine the DRFPM sample rate.

### 4.4.1 Transient Response

The transient plots in Figure 4-4 are calculated from measurements on the DSO80000B oscilloscope with a sample rate 40 GSPS. As with the static LUT measurements above, a 2.5-GHz carrier is used so that the signal is sampled 16 times per period of the carrier. The oscilloscope data is multiplied in MATLAB by sine and cosine of the carrier. Then, the magnitude and phase of the baseband signal are calculated on a cycle-by-cycle basis by averaging the resulting signals over each period of the carrier. Thus amplitude and phase information can be found at an effective sample rate of

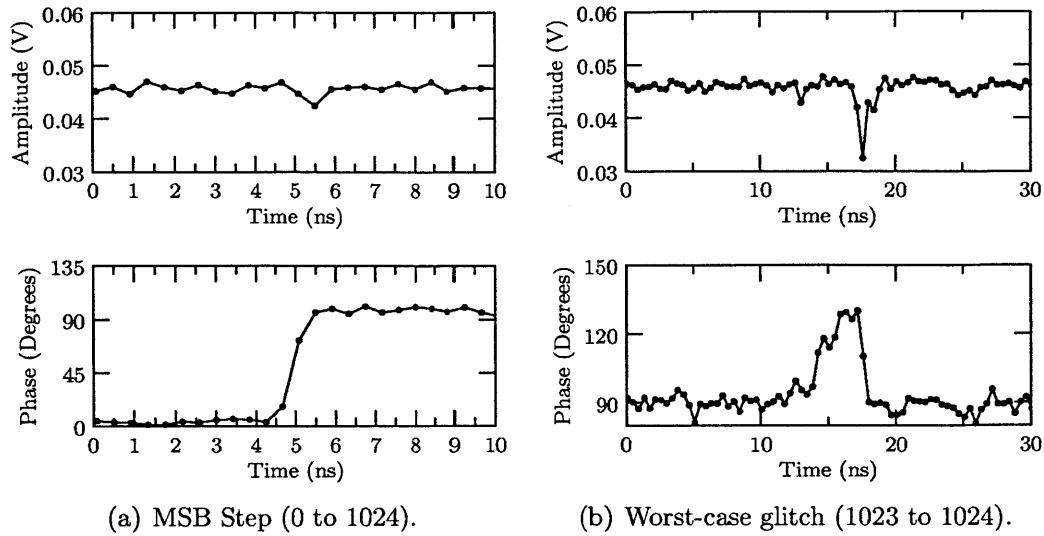


Figure 4-4: DRFPM step responses, computed by downloading oscilloscope trace data and demodulating to amplitude/phase data in MATLAB.

2.5 GSPS, i.e. sampled at 0.4 ns intervals.

The plots in Figure 4-4 show the best- and worst-case transient DRFPM outputs. In Figure 4-4(a), only the current DAC's MSB is switched with all other inputs remaining constant; i.e. the data input is switched from 0 to 1024. The settling time for this best-case transient is under 2 ns, with the phase exhibiting a first-order response and the amplitude remaining nearly constant. This settling time is typical of all bits when they are switched individually. Figure 4-4(b), on the other hand, shows the transient response to a step between inputs 1023 and 1024. This set of inputs requires all of the DAC bits to switch simultaneously and therefore represents the worst-case glitch situation. This transient response exhibits significant glitching, with a response time on the order of 10ns and dramatic variation in both amplitude and phase over this nominally sub-1° phase step. From this plot, it can be seen that there are problems with the timing of the digital interface to the DRFPM. In fact, the fast response of the analog portion of this design exacerbates the effect of this timing mismatch, in that the phase output has time to settle at a new value, here around 125°, before the other bit(s) are switched. As will be seen in subsequent sections, this digital timing problem severely limits the DRFPM performance in applications. The

clock pre-rotation bit has similar timing mismatch. Thus although the response in Figure 4-4(a) is indicative of a system that could operate at up to around 400 MSPS, further attention to the digital design would be necessary to reach that performance.

#### 4.4.2 Simplified 8-PSK

The phase modulator bandwidth can be demonstrated using an 8-PSK modulated test signal. Phase-shift keying is in theory appropriate for phase modulator testing because the signal initially has a constant envelope. Standards that employ 8-PSK modulation (eg. Bluetooth, WLAN), however, require filtering in the  $IQ$  domain to meet spectral masks. The filtered signal has a variable envelope and cannot be generated with the constant-envelope phase modulator alone. For this test, therefore, a simple 8-PSK signal was used in which adjacent symbols were transmitted sequentially. Baseband filtering was done in the phase domain.

The benefit of using a high oversampling ratio in the baseband digital front-end before upconversion as a way to reduce filtering requirements has been demonstrated in [21]. The DRFPM in this work has an advantage over lower resolution phase modulators in that it can similarly exploit oversampling to push zero-order hold replicas to higher frequency. Figure 4-5 shows the improvement of the spectrum of a 8x oversampled 2.5 MSymbol/second 8PSK signal compared to one without oversampling. Both measurements were performed without using the carrier pre-rotation mode of the phase modulator.

#### 4.4.3 GSM

The Global System for Mobile Communications (GSM) standard is one of few standards that employs a truly constant-envelope modulation scheme. Unlike PSK modulation schemes, where an initially constant-envelope baseband signal is digitally filtered into a variable-envelope signal, GSM uses Gaussian minimum-shift keying (GMSK) modulation which is inherently constant-envelope. The development of this modulation scheme is briefly discussed below, as it is not as straightforward as the

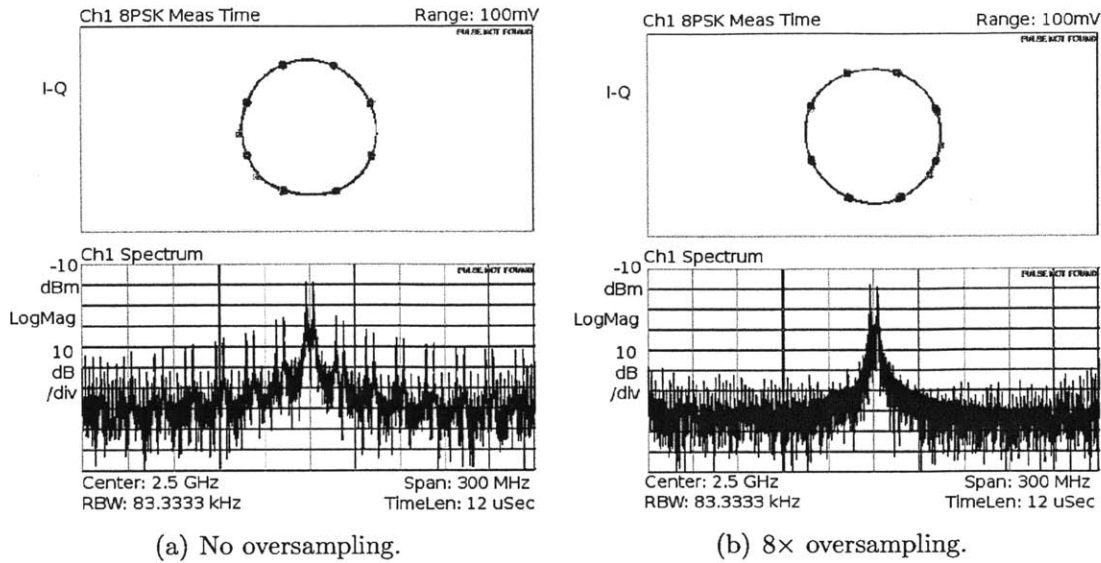


Figure 4-5: Spectrum and EVM measurement for sequential 8-PSK signal.

other modulation schemes (8-PSK, 16-QAM, etc.) used in this work.

## GMSK Modulation

GMSK is a variant of offset QPSK (OQPSK), which is itself related to QPSK modulation. The main difference between QPSK and OQPSK is that QPSK allows arbitrary transitions from any point in the constellation, whereas OQPSK limits phase changes between adjacent symbols to  $0^\circ$  or  $\pm 90^\circ$  [36]. The transmitted signal can be considered as a combination of in-phase and quadrature signals  $a_I(t)$  and  $a_Q(t)$  respectively, with a symbol period  $2T_S$ . In OQPSK these two signals are offset in time by  $T_S$  so that they cannot change sign simultaneously; as a result,  $180^\circ$  phase steps are impossible. When bandpass filtering is applied to the baseband signal, the QPSK signal with its transitions between diagonally opposed quadrants will require the signal envelope to go to zero. Sketches of the unfiltered QPSK and OQPSK, reproduced from [36], are shown in Figure 4-6(a).

If sinusoidal instead of rectangular pulses are used for the  $a_I(t)$  and  $a_Q(t)$  signals,

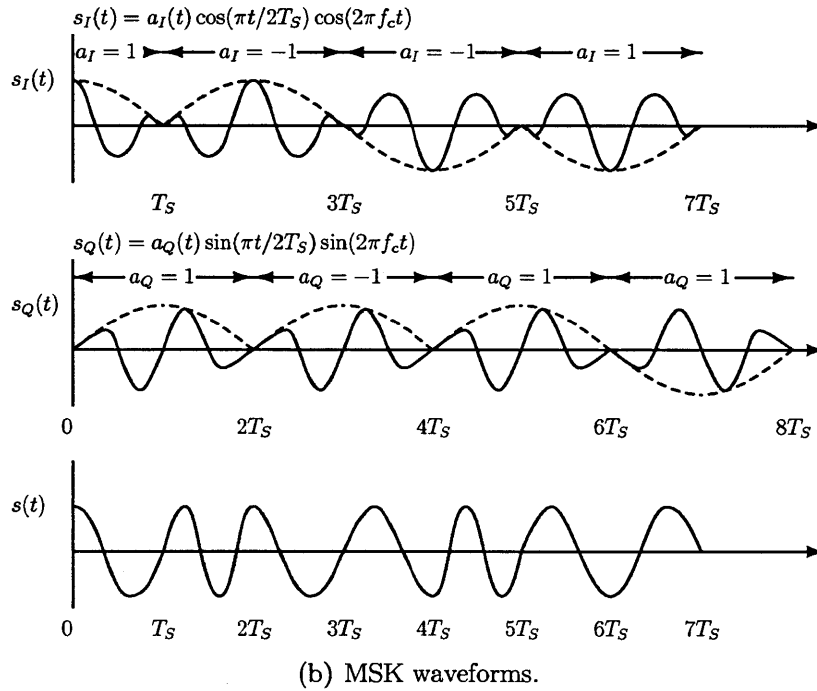
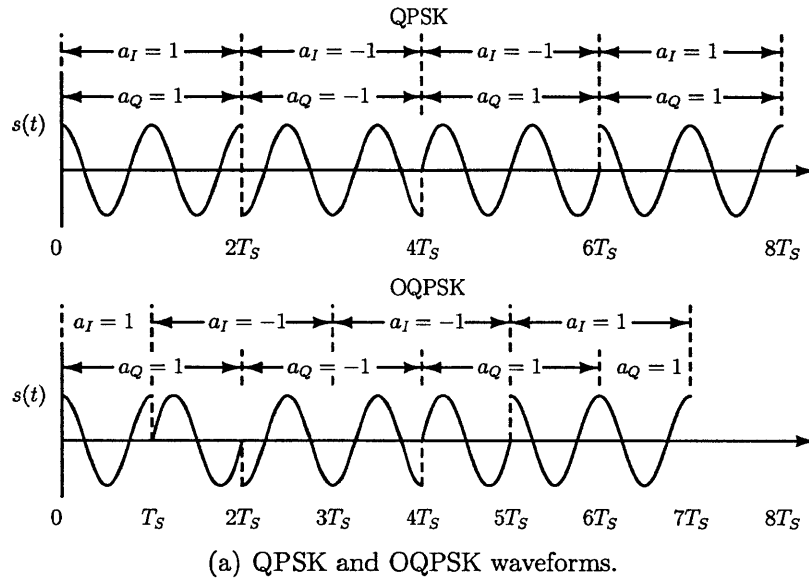


Figure 4-6: Example waveforms showing the evolution of MSK. [36]



an MSK signal is produced, with [36]:

$$s_{\text{MSK}}(t) = a_I(t) \cos\left(\frac{\pi t}{2T_S}\right) \cos(2\pi f_c t) + a_Q(t) \sin\left(\frac{\pi t}{2T_S}\right) \sin(2\pi f_c t)$$

The vector sum of the signal components now has a constant envelope, as sketched in Figure 4-6(b), and can be filtered without introducing amplitude variation. Gaussian pulse-shaping filters are applied to the MSK baseband signal to generate GMSK modulation.

## GSM Results

The phase modulator in this work is not very well-suited for demonstrating GSM because its optimal sample rate (200 MSPS) is over 1000 times the GSM symbol rate. A design intended for GSM would have different design choices from those in this work, including a lower sample clock rate that would reduce clock coupling issues that introduce phase noise in the output spectrum. Furthermore, it was shown in [43] that a phase modulator for MSK modulation requires only 4-bit phase resolution.

A further practical issue with demonstrating GSM with this system is the amount of RAM available on the FPGA, which limits tests to only 14 symbols. The spectrum of 14 repeating symbols clearly will have artifacts that are signal- rather than system-dependent. Six of these 14-symbol spectrum measurements were averaged to produce the spectrum in Figure 4-7, where GSM data is applied to a 2.5-GHz carrier signal. The system comes within 10 dB of meeting the very challenging requirements for GSM.

### 4.4.4 Outphasing Measurements

Outphasing measurements are performed using two of the DRFPM ICs with a connectorized Wilkinson combiner performing power combining of the two outputs from the Class-E PAs. The PA biasing configurations are adjusted so that the two chips have equal output amplitude. Setting the relative phase of the two DRFPMs controls the system output amplitude as described in Section 2.3.

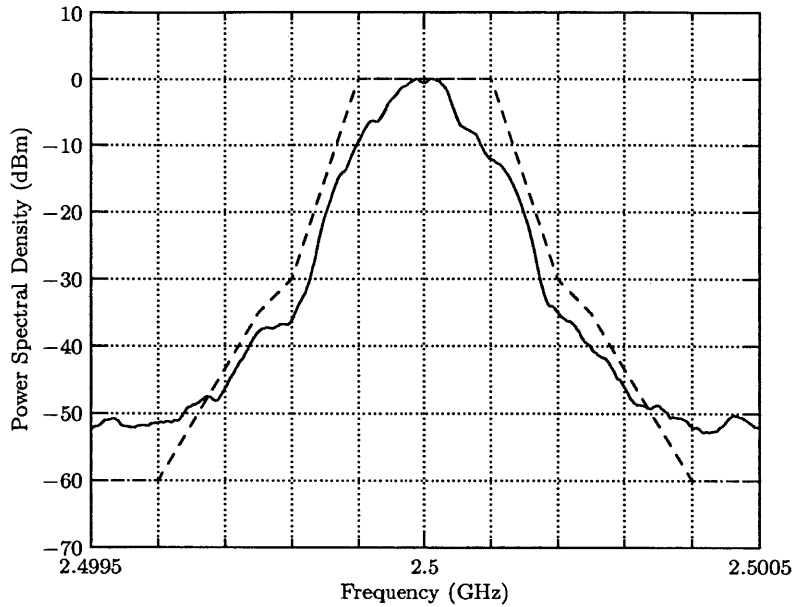


Figure 4-7: Measured spectrum for GMSK.

The step transient in Figure 4-8 shows the system response to a  $90^\circ$  step in the outphasing angle. Similarly to the transient measurement in Figure 4-4(a), the  $90^\circ$  step input was implemented by switching a single bit, here one of the quadrant selection bits. The output settles within 2.5 ns. The sinusoidal waveform in Figure 4-9 displays the same glitching behavior due to timing error in the digital interface to the DRFPM as are seen in 4-4(b). These amplitude spikes due to the nonmonotonic phase step response of the DRFPM limit its performance in an outphasing system. A modulated example demonstrating 16-QAM at 6.25 MSymbols/second with  $2\times$  oversampling (12 MSPS total) is shown in Figure 4-10. Despite the high out-of-band power due to the glitches and the limited baseband filtering, this system achieves an error vector magnitude (EVM) of 3.185 %<sub>rms</sub>.

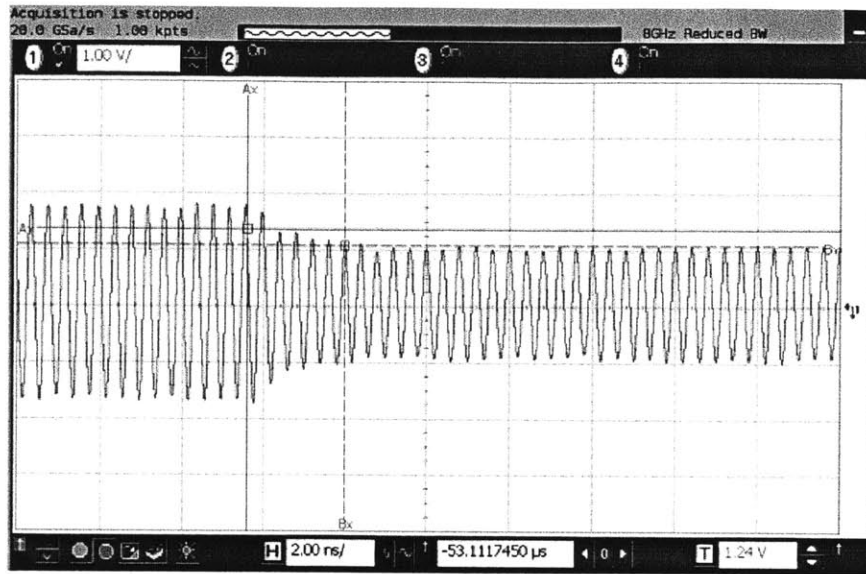


Figure 4-8: Outphasing system output for a 90-degree step in outphasing angle. The phase step is performed by switching a single quadrant bit so that no DAC glitches are present. The output settles within 2.5 ns.

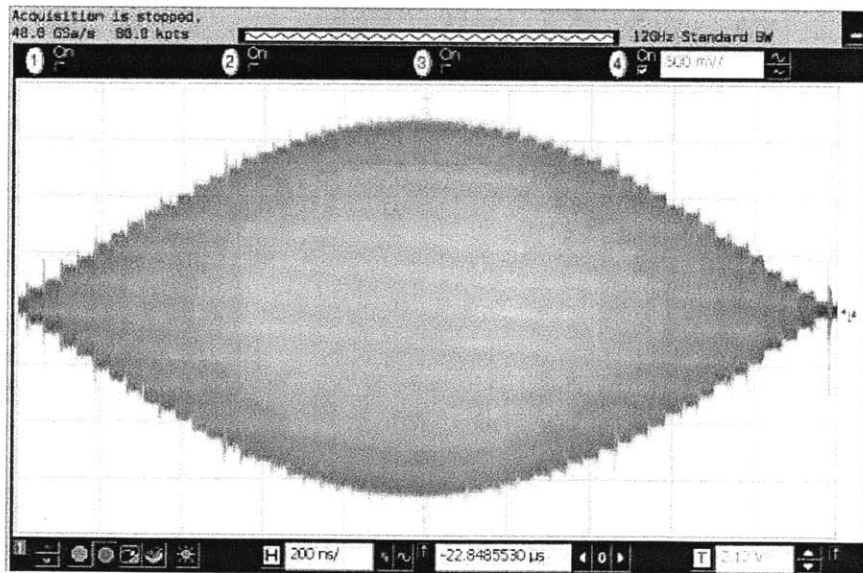


Figure 4-9: 250-kHz sinusoid generated by outphasing, 25 MSPS. The glitches visible at the step changes are a result of the timing errors in the digital portion of the DAC design.

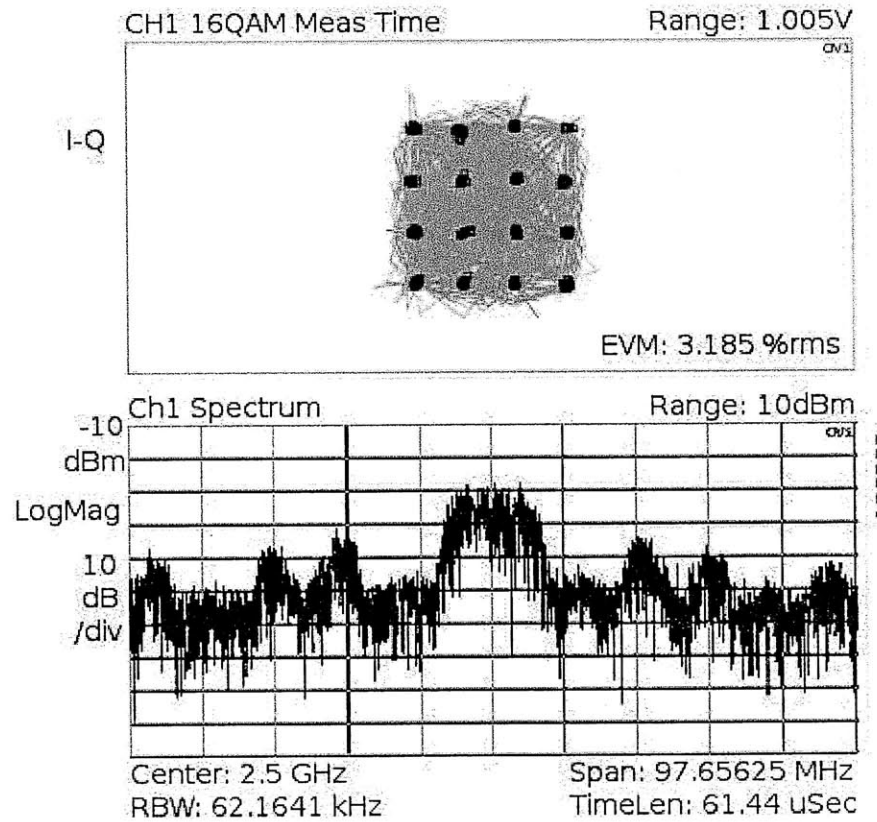


Figure 4-10: 16-QAM signal at 6.25 MSymbols/sec and with 2× oversampling (12 MSPS total). The poor spectral performance is due to a combination of the low oversampling rate and glitches.

# Chapter 5

## Four-Way Lossless Outphasing

### Combiner: Theoretical

### Development

The primary contribution of this work is the first-ever demonstration of the new four-way lossless outphasing and combining system at microwave frequencies. This new power combining and outphasing modulation system has been developed as a way to overcome the limitations of the outphasing systems described in Section 2.3 [37]. Similarly to Chireix and Doherty architectures, the combiner itself is non-isolating and constructed of ideally lossless components, and therefore avoids the efficiency degradation in outphasing architectures using isolating combiners. The combiner presents a nearly resistive load to the PAs over a significantly wider range of output power levels than those techniques. Because it can be implemented using discrete components, the combiner is also suitable for non-microwave frequency applications (medical imaging, power conversion, communications, etc.). The theory including control laws was demonstrated by Alex Jurkov in [24] for static measurements at a 27MHz carrier. For the 2.14-GHz carrier frequency used in this work, a discrete-component combiner is possible, and is used here to demonstrate the system. This chapter will follow the development in [23] but with a focus on microwave frequencies.

Appendix A contains a reference list of the variable definitions that will be used

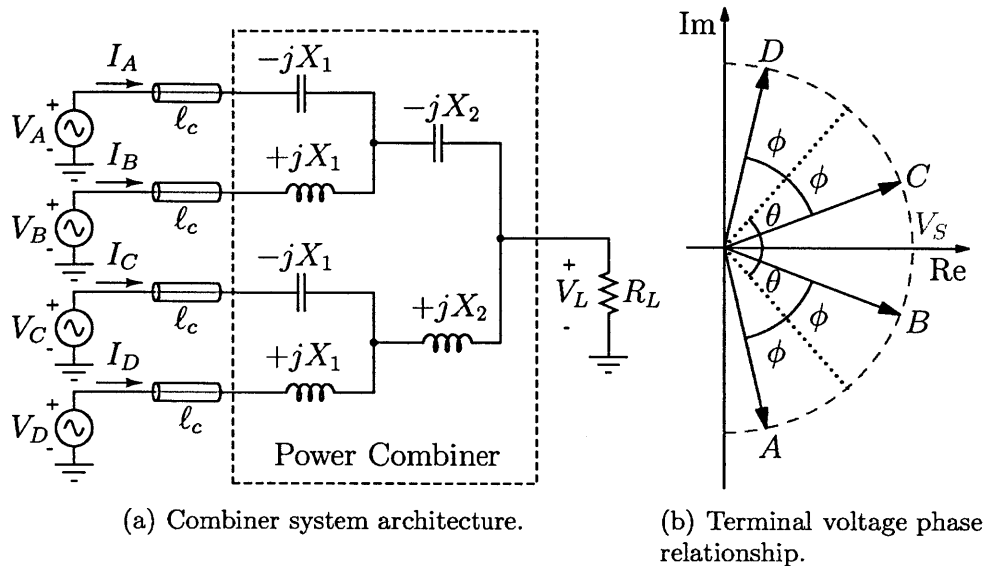


Figure 5-1: The four-way outphasing and combining architecture. The PAs are represented as ideal, constant-amplitude voltage sources with the phasor relationship shown. The transmission lines represent interconnects from the PA reference planes to the combiner input reference planes. All sources are operated at the same time and with equal amplitudes.

in the combiner discussion (Chapters 5, 6, and 7).

## 5.1 Theory of Operation

The power combining structure implementation is shown in Figure 5-1. It is related to the RCN of Section 2.5, and can be considered to be a RCN with the signs of all impedances changed, with the now negative resistors replaced with sources, and the independent source replaced with resistors. Although not identical, this conversion is related to time reverse duality [19]. The resulting power combiner has four ports connected to the PAs, and one connected to the (antenna) load. The four PAs are assumed to have the same amplitude  $V_s$  and a phase relationship as shown in Figure

5-1, that is

$$\begin{bmatrix} V_A \\ V_B \\ V_B \\ V_D \end{bmatrix} = V_S \begin{bmatrix} e^{-j\phi} e^{-j\theta} \\ e^{j\phi} e^{-j\theta} \\ e^{-j\phi} e^{j\theta} \\ e^{j\phi} e^{j\theta} \end{bmatrix} \quad (5.1)$$

Over all output power levels, all four PAs are continuously operated with equal amplitudes. With a zero-referenced output phase assumed for this analysis, the above phase relationship will result in a load voltage  $V_{L,\text{ref}}$  with zero phase. The phases may be adjusted by a common phase offset to control the absolute angle of the output.

This work follows the approach proposed in [37, 23] to select values for the combiner elements. This methodology originates from the one used to select reactance values for the RCN described in Section 2.5. In particular, the two reactances  $X_1$  and  $X_2$  are selected using RCN Equations 2.10 and 2.8, reproduced here:

$$X_1 = \frac{X_2}{k + \sqrt{k^2 - 1}} \quad (5.2)$$

$$X_2 = \frac{2R_L}{k + 1} \quad (5.3)$$

The parameter  $k$  becomes an important design parameter for the combiner and ultimately controls the system's overall performance. The best choice of  $k$  depends on a few factors, including the phase control strategy and characteristics of the signal to be transmitted. Phase control is described in Section 5.2, and the selection methodology of  $k$  in Section 5.3.

The input impedance to the power combiner is critical to the power amplifier operation. The impedance at each port depends on the phases of all four sources. In particular, a variable of interest is the effective admittance at *one* combiner input port when *all* sources are active. This admittance represents the power amplifier load when operating as part of the outphasing transmitter. It is shown in [37] that when the PAs are driven with the phase relationship as in Equation 5.1, the input

admittances of the four ports  $A - D$  can be written as:

$$Y_{\text{eff},A} = X_1^{-1}(\gamma - \gamma \cos(2\phi + 2\theta) - \gamma \cos(2\phi) + \gamma \cos(2\theta) - \beta \sin(2\phi)) \\ + jX_1^{-1}(1 - \beta - \gamma \sin(2\phi + 2\theta) - \gamma \sin(2\phi) + \gamma \sin(2\theta) + \beta \cos(2\phi)) \quad (5.4)$$

$$Y_{\text{eff},B} = X_1^{-1}(\gamma - \gamma \cos(2\theta - 2\phi) - \gamma \cos(2\phi) + \gamma \cos(2\theta) + \beta \sin(2\phi)) \\ + jX_1^{-1}(-1 - \beta - \gamma \sin(2\theta - 2\phi) + \gamma \sin(2\phi) + \gamma \sin(2\theta) + \beta \cos(2\phi)) \quad (5.5)$$

$$Y_{\text{eff},C} = X_1^{-1}(\gamma - \gamma \cos(2\theta - 2\phi) - \gamma \cos(2\phi) + \gamma \cos(2\theta) + \beta \sin(2\phi)) \\ - jX_1^{-1}(-1 - \beta - \gamma \sin(2\theta - 2\phi) + \gamma \sin(2\phi) + \gamma \sin(2\theta) + \beta \cos(2\phi)) \quad (5.6)$$

$$Y_{\text{eff},D} = X_1^{-1}(\gamma - \gamma \cos(2\phi + 2\theta) - \gamma \cos(2\phi) + \gamma \cos(2\theta) - \beta \sin(2\phi)) \\ - jX_1^{-1}(1 - \beta - \gamma \sin(2\phi + 2\theta) - \gamma \sin(2\phi) + \gamma \sin(2\theta) + \beta \cos(2\phi)) \quad (5.7)$$

where  $\gamma = R_L/X_1$  and  $\beta = X_2/X_1$ .

It can be shown [23] that for a given pair of outphasing angles  $(\theta, \phi)$  the load voltage is given by

$$V_L = j \frac{R_L}{X_1} (V_B + V_D - V_A - V_C). \quad (5.8)$$

When the phase relationship of Equation 5.1 is used, the above equation reduces to

$$V_L = -\frac{4R_L}{X_1} V_s \sin(\phi) \cos(\theta) \quad (5.9)$$

Thus the power delivered to the load is

$$P_{\text{out}} = \frac{V_L^2}{2R_L} = \frac{8R_L V_s^2}{X_1^2} \sin^2(\phi) \cos^2(\theta). \quad (5.10)$$

It can be seen from Equation 5.10 that the maximum output power to the load,  $P_{\text{max}}$ , occurs when  $\phi = 90^\circ$  and  $\theta = 0^\circ$  and is

$$P_{\text{out,max}} = \frac{8R_L V_s^2}{X_1^2} \quad (5.11)$$



In this case, the input admittances are given by Equations 5.12-5.15 below:

$$Y_{\text{eff,A,P}_{\text{max}}} = X_1^{-1} (4\gamma + j(1 - 2\beta)) \quad (5.12)$$

$$Y_{\text{eff,B,P}_{\text{max}}} = X_1^{-1} (4\gamma + j(-1 - 2\beta)) \quad (5.13)$$

$$Y_{\text{eff,C,P}_{\text{max}}} = X_1^{-1} (4\gamma + j(1 + 2\beta)) \quad (5.14)$$

$$Y_{\text{eff,D,P}_{\text{max}}} = X_1^{-1} (4\gamma + j(-1 + 2\beta)) \quad (5.15)$$

where  $\gamma = R_L/X_1$  and  $\beta = X_2/X_1$ . Evaluating these equations for an example system where  $k = 1.05$ ,  $R_L = 50 \Omega$ , and  $V_s = 1 \text{ V}$  gives a load impedance with real part  $6.34 \Omega$  and imaginary parts with magnitudes  $9.52 \Omega$  and  $20.48 \Omega$ .

The output power is zero when  $\theta = \phi = 0^\circ$ . All four PAs are in phase and see input admittances of

$$Y_{\text{eff,A}} = Y_{\text{eff,C}} = jX_1^{-1} \quad (5.16)$$

$$Y_{\text{eff,B}} = Y_{\text{eff,D}} = -jX_1^{-1} \quad (5.17)$$

This result can be confirmed by referring to the combiner structure in Figure 5-1. With each voltage source in phase, the sign-inverted symmetry of this structure means that the voltages at the intermediate nodes and the output will be zero. Thus each PA drives a load of impedance  $\pm jX_1$  to incremental ground. This result is true when  $P_{\text{out}} = 0$  regardless of the phase control strategy.

## 5.2 Phase Control Strategies

The phase relationship in Equation 5.1 only partially describes how the PA phases are determined. A variety of control laws for the two phases  $\phi$  and  $\theta$  can be devised that seek to optimize a particular aspect of the system such as PA load susceptance or input admittance phase. Summaries of three outphasing control strategies are included below, with a detailed development found in [23]. The advantage of the IRCN method is that the control equations can be computed analytically and are accurate

over the entire operating range. Compared to the optimal susceptance and optimal phase control methods, however, it results in less desirable loading conditions for the PAs. In practice, the optimal susceptance law is preferred. A slight improvement in overall system efficiency can be attained in practice by sweeping  $\phi$  and  $\theta$  around their nominal values and choosing the highest-efficiency plane in the resulting matrix. For the demonstrated system, however, the benefits of this lookup-table approach are minimal.

### 5.2.1 IRCN Control

The phases  $\phi$  and  $\theta$  can be chosen by analogy to the two-stage RCN in Section 2.5.1. That is, they can be chosen according to the terminal phase relationships that occur in the original RCN (see Equation 2.13)

$$\begin{aligned}\phi &= \arctan\left(\frac{X_1}{r_0}\right) \\ \theta &= \arctan\left(\frac{2r_0X_2}{r_0^2 + X_1^2}\right)\end{aligned}\tag{5.18}$$

In this case,  $r_0$  is an intermediate variable. Continuing the RCN analogy, it is reasonable to use

$$r_0 = \frac{2V_S^2}{P_{\text{cmd}}}\tag{5.19}$$

where  $P_{\text{cmd}} = (V_{L,\text{ref}}^2)/(2R_L)$  is the commanded output power, i.e. the input power that corresponds to the  $[\theta; \phi]$  pair of Equation 5.18 for the original RCN [37]. It has been shown, however, that the above choice of  $r_0$  does not result in a linear relationship between the commanded  $P_{\text{cmd}}$  and the actual  $P_{\text{out}}$  [23]. The RCN analysis is based on the assumption that the four terminal impedances (or voltage/current phase relationship) at the RCN load/combiner inputs are real. Thus the results are not exact for the case of the combiner where this impedance can be complex. An expression for  $r_0$  which yields an exact relationship between commanded power and

$P_{\text{out}}$  is given as

$$r_{0,\text{exact}} = \sqrt{\frac{4R_L V_s^2}{P_{\text{out}}} - X_1^2 - 2X_2^2 + 2\sqrt{\frac{4R_L^2 V_s^4}{P_{\text{out}}^2} - \frac{4R_L V_s^2 X_2^2}{P_{\text{out}}} + X_1^2 X_2^2 + X_2^4}} \quad (5.20)$$

It is convenient to rewrite the outphasing control law in terms of a commanded power relative to the output power when the load resistance to each PA is the nominal  $R_L = 50 \Omega$ . This power is  $P_L = (2V_s^2)/R_L$ . Substituting the expression  $P_N = P_{\text{out}}/P_L$  yields

$$r_O = \sqrt{\frac{2R_L^2}{P_N} - X_1^2 - 2X_2^2 + 2\sqrt{\frac{R_L^4}{P_N^2} - \frac{2R_L^2 X_2^2}{P_N} + X_1^2 X_2^2 + X_2^4}} \quad (5.21)$$

This  $r_0$  expression will be referred to as Inverse RCN (IRCN) control.

In Figure 5-2, the magnitude and phase of the four input port admittances are plotted for an example system as a function of the power command  $P_N$  for IRCN control. It can be seen that over a wide range of output powers, the phase is close to zero (equal to zero for exactly four output power levels), and the conductive components are closely matched and scale nearly linearly with output power. The corresponding values of  $\theta$  and  $\phi$  are shown as a function of  $P_N$  in Figure 5-3.

This load characteristic with primarily almost-real load impedances represents close to ideal loading conditions for many kinds of switching power amplifiers. These results indicate that this power combining scheme can provide desirable loading characteristics for the PAs over a wide range of output power levels. Furthermore, these results are accurate over the entire operating range  $0 \leq P_{\text{out}} \leq P_{\text{max}}$ .

## 5.2.2 Optimal Susceptance Outphasing Control

A phase control strategy that minimizes the effective input susceptance seen by the PAs is developed in [23] and summarized in this section. One advantage of this approach over IRCN is that the susceptive loading is evenly distributed across the

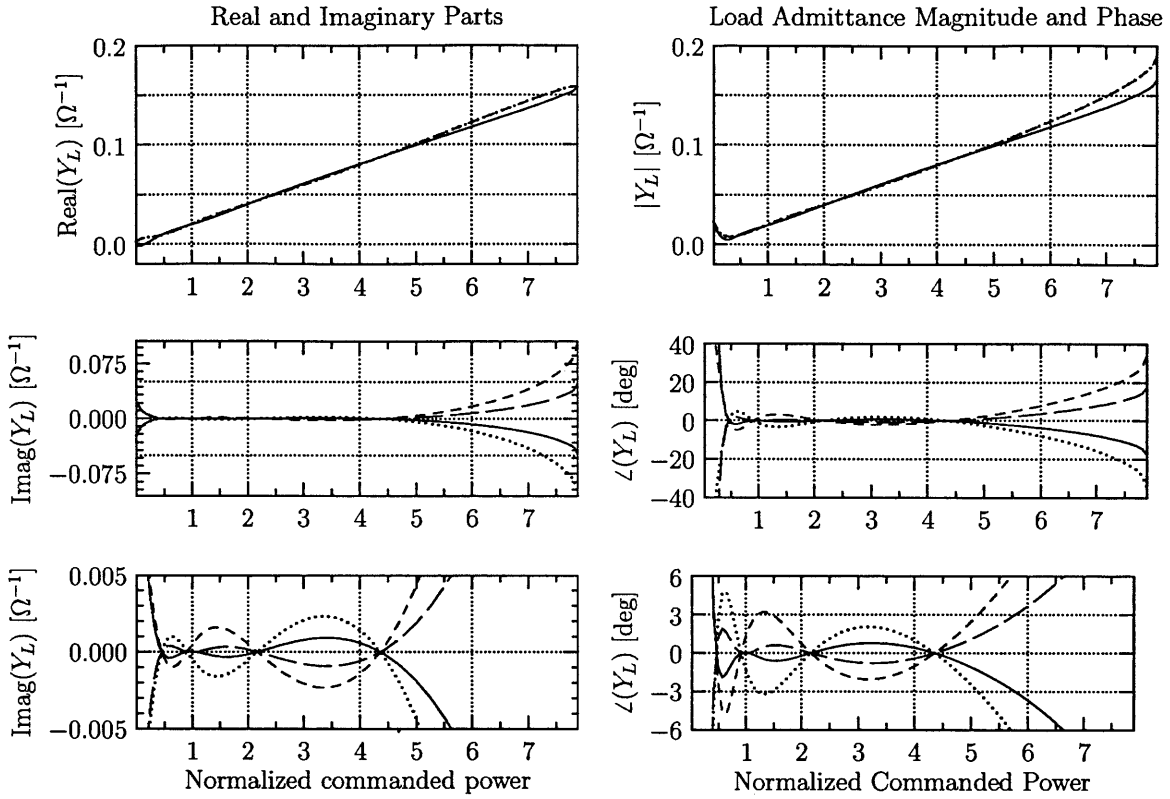


Figure 5-2: Effective input port admittances when IRCN control is used, with  $R_L = 50 \Omega$ ,  $V_s = 1V$ , and  $k = 1.05$ .

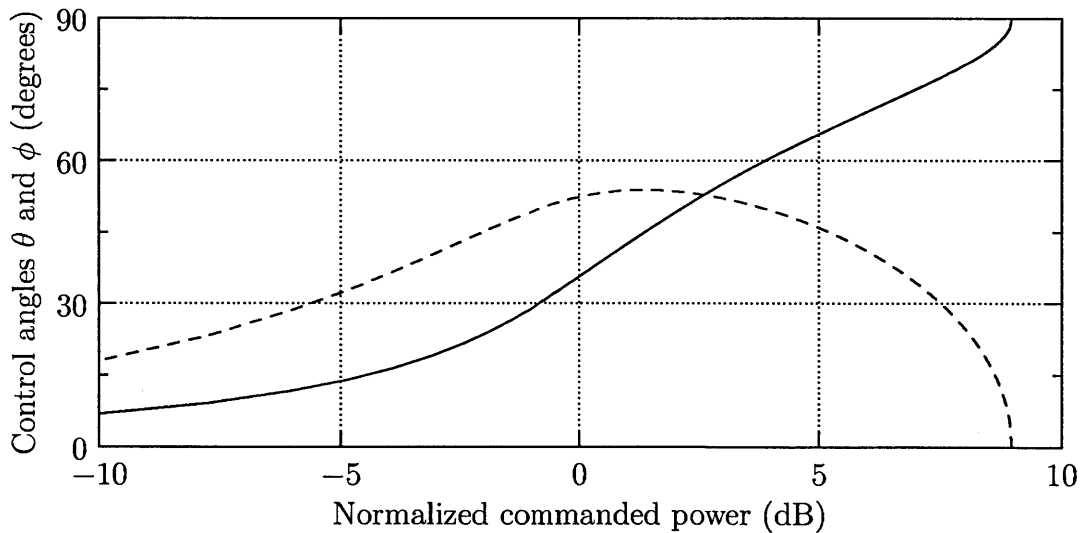


Figure 5-3: Phase commands over output power range when IRCN is used, with  $R_L = 50 \Omega$ ,  $V_s = 1 V$ , and  $k = 1.05$ .

four PAs. This optimal susceptance (OS) outphasing control law is given as

$$\begin{aligned}\phi &= \arctan\left(\frac{P_{\text{out}}X_1}{2V_s^2}\right) \\ \theta &= \arccos\left(\sqrt{\frac{4V_s^4 + P_{\text{out}}^2X_1}{8P_{\text{out}}R_LV_s^2}}\right)\end{aligned}\quad (5.22)$$

In terms of normalized commanded power  $P_N = (P_{\text{out}}R_L)/(2V_s^2)$ , the OS law becomes

$$\begin{aligned}\phi &= \arctan\left(\frac{X_1}{R_L}P_N\right) \\ \theta &= \arccos\left(\sqrt{\frac{1}{4P_N} + \frac{P_N}{4}\left(\frac{X_1}{R_L}\right)^2}\right)\end{aligned}\quad (5.23)$$

The OS control law is valid over the range

$$\frac{4R_L^2V_s^2 - 2V_s^2\sqrt{4R_L^4 - R_L^2X_1^2}}{X_1^2R_L} \leq P_{\text{out}} \leq \frac{4R_L^2V_s^2 + 2V_s^2\sqrt{4R_L^4 - R_L^2X_1^2}}{X_1^2R_L} \quad (5.24)$$

For values  $R_L = 50 \Omega$ ,  $V_s = 1 \text{ V}$ , and  $k = 1.05$ , Equation 5.24 evaluates to

$$0.010 \text{ W} \leq P_{\text{out}} \leq 0.305 \text{ W}. \quad (5.25)$$

The maximum output power for a combiner with these values is 0.316 W from Equation 5.11. Thus the OS control law is valid over a range of 3.3% to 96.7% of the maximum power, a variation of almost 30:1, or 14.8 dB. The OS control admittance and phase control plots are shown in Figures 5-4 and 5-5. The 14.8 dB maximum dynamic range indicates that some additional control scheme will be necessary to extend the dynamic range for communications applications. Although the OS law has a built-in dynamic range limit, however, in practice the limit is not more restrictive than for the RCN control case. For all three of the control schemes presented here, the practical limit on the dynamic range is due to the large susceptance at very low power levels. In order to generate the zero-crossings necessary for the majority of modern wireless standards, the power amplifier must be capable of generating significantly

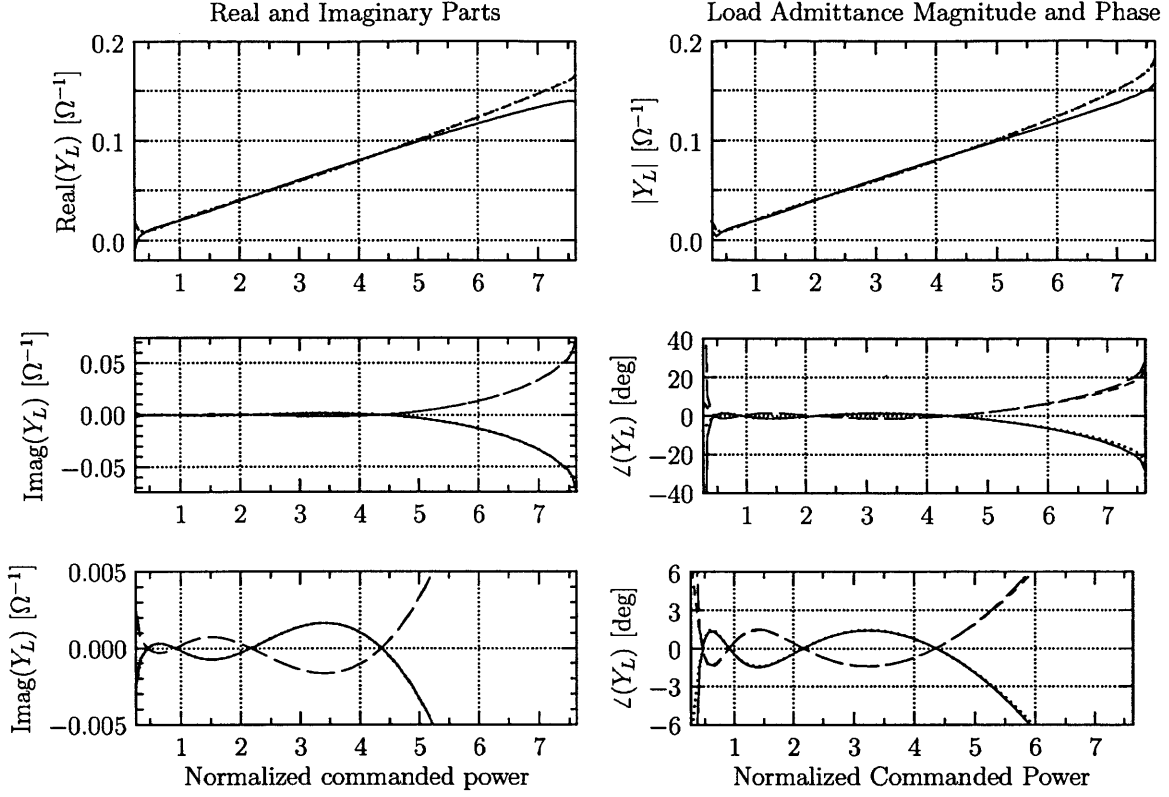


Figure 5-4: Effective input port admittances when OS control is used, with  $R_L = 50 \Omega$ ,  $V_s = 1 \text{ V}$ , and  $k = 1.05$ .

lower amplitude outputs than are possible with the combiner alone.

### 5.2.3 Optimal Phase Outphasing Control

The third control law presented in [23] is optimal phase (OP) control. This approach minimizes the admittance phase seen by the PAs at each power level. The phase commands  $\theta$  and  $\phi$  can be found by solving the nonlinear system of equations

$$\frac{P_{\text{out}} X_1^2}{8R_L V_s^2} = \sin^2(\phi) \cos^2(\theta) \quad (5.26)$$

$$\sin(2\phi) = \frac{2\gamma \cos^2(\theta)}{\beta^2 + 4\gamma^2 \cos^2(\theta) - 2\beta\gamma \sin(2\theta)}$$

The constraints on  $P_{\text{out}}$  are the same as those for the OS method given in Equation 5.24. This control strategy produces a result that is nearly indistinguishable to that

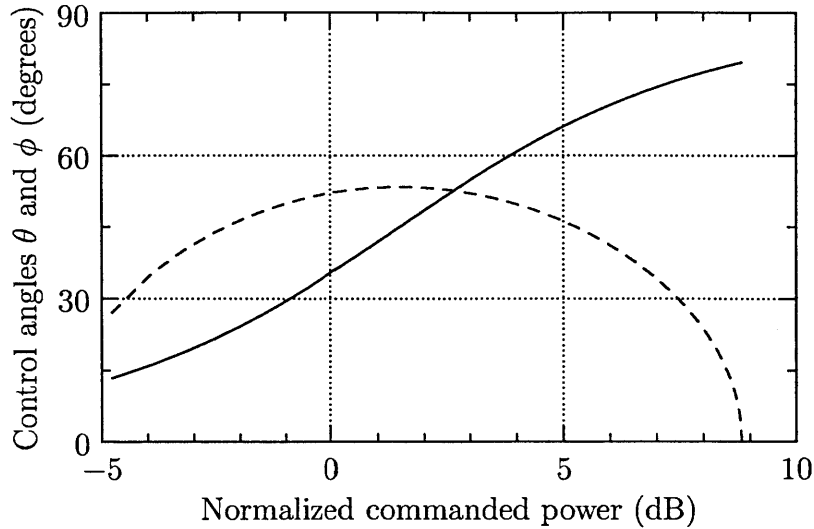


Figure 5-5: Phase commands over entire valid output power range when OS is used, with  $R_L = 50 \Omega$ ,  $V_s = 1 \text{ V}$ , and  $k = 1.05$ .

of the OS approach described above, but lacks an analytical expression for control variables  $\theta$  and  $\phi$ . The OP method is considered equivalent to the OS approach in this work and will not be considered separately.

### 5.3 Combiner Design with Parameter $k$

The choice of design variable  $k$  controls a tradeoff between output power dynamic range and the maximum variation in the phase of the load admittance seen by the four power amplifiers. This tradeoff is described in detail in [5]. Figure 5-6 illustrates the effect of  $k$  on dynamic range and load admittance phase for one of the PAs over a number of different values of  $k$ . In practice, the range of load impedances that the power amplifiers can drive efficiently much be considered in combination with the choice of  $k$ . As will be seen in Chapter 6, the system output power dynamic range is extended on the low-power end by modulating the amplitude of the PA drive. The experimental part of this work uses  $k = 1.05$ , corresponding to an output power range of approximately 10 dB for which an admittance phase of less than  $2^\circ$  is realized (assuming ideal-source PAs).

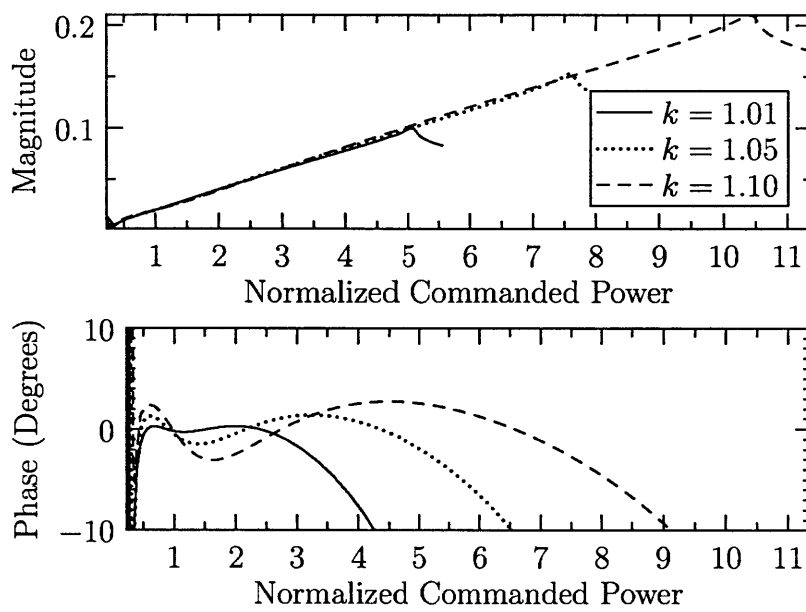


Figure 5-6: PA load magnitude and phase for a range of  $k$  values. A larger  $k$  gives an increased output power range but also increased deviation in the load phase.



# Chapter 6

## Four-Way Lossless Outphasing Combiner: Prototype Development

The combiner and outphasing system prototype consists of three major elements: the baseband signal generation and processing, the RF power amplifiers, and the combiner itself. This chapter describes the development of each element.

### 6.1 Baseband Signal Processing

The function of the baseband signal processing stage is to take test data, perform signal separation based on the outphasing control law, and generate the phase-modulated RF signals that are the inputs to the RF power stage. An Opal Kelly XEM5010 FPGA development board with a Xilinx Virtex-5 FPGA provides the interface between the phase modulators and the computer where test signals are generated. The four phase modulators are each implemented by a 16-bit dual-channel DAC evaluation board with upconverting mixers from Analog Devices (AD9779A). Power splitters, seen at the top of the baseband stage photograph in Figure 6-1, distribute the 2.14-GHz carrier signal to each phase modulator PCB. The data clocks are generated by the FPGA along with the data. This clock-forwarding scheme allows for adjustment in clock edge timing to correct for differences in total delay of the four predriver and PA paths. The clock edges can be adjusted with 72 ps resolution.

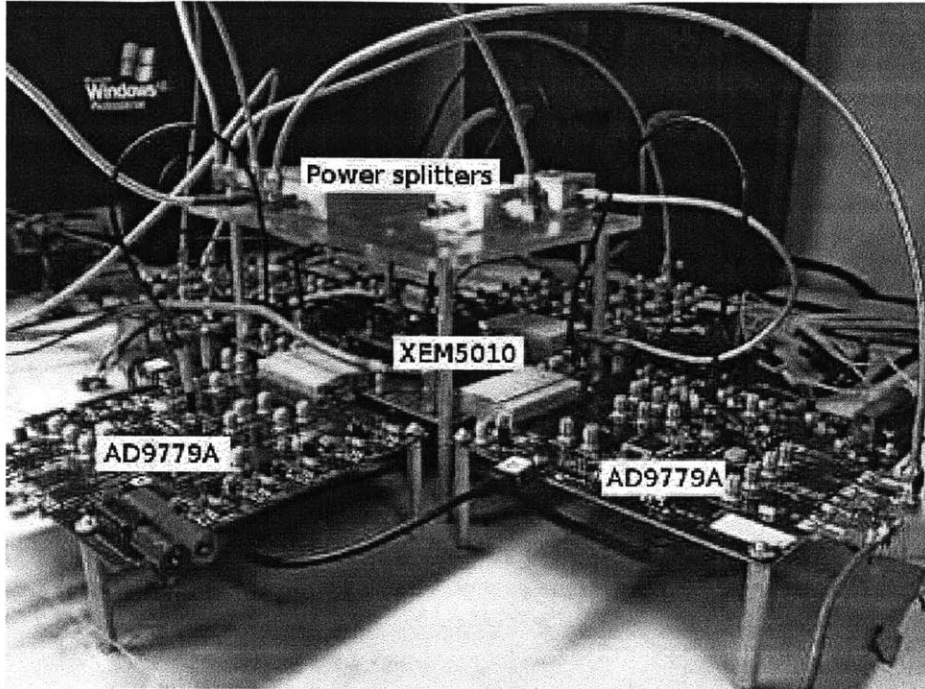


Figure 6-1: Photograph of the baseband stage prototype.

The phase modulators drive the switching PA inputs through a preamplifier chain with approximately 30 dB gain, not shown. This baseband processing block plus predriver chain can produce four phase-modulated signals at a maximum sample rate of 200 MSamples/second.

## 6.2 Class Inverse F Power Amplifier

The prototype outphasing system uses four class inverse F power amplifiers based on the design in [16]. The schematics are shown in Figures 6-2 and 6-3.

The PAs are fabricated on a 30-mil RO4350 substrate and operated at a supply voltage of 20V and gate bias -3.4V. The output power and drain efficiency of all four PAs are characterized under load modulation conditions similar to those they will see in the combiner system. The load modulation measurements in Figure 6-5 are made using the setup in Figure 6-4. First the Maury Microwave 1819B triple stub tuner is connected as in Figure 6-4(a), with the tuner terminated by the 50- $\Omega$  input

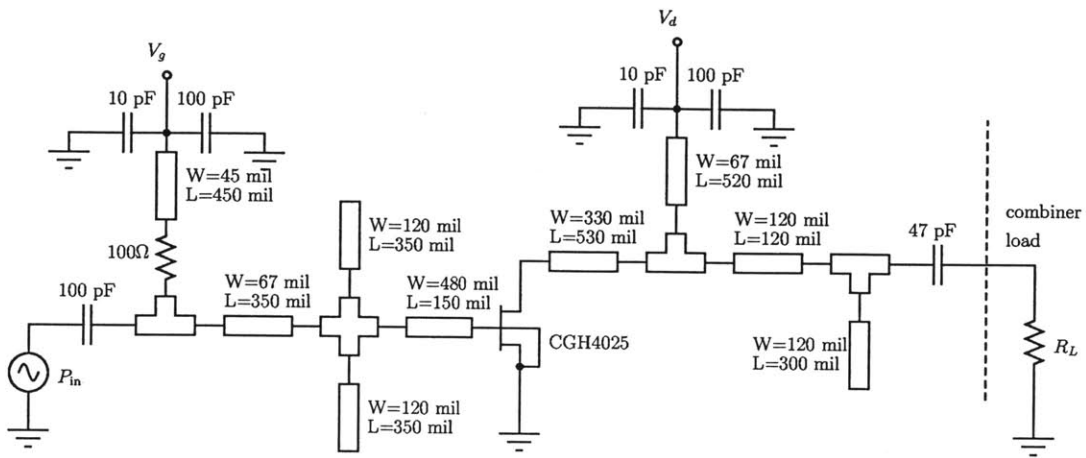


Figure 6-2: Class inverse F power amplifier schematic, reproduced from [16].

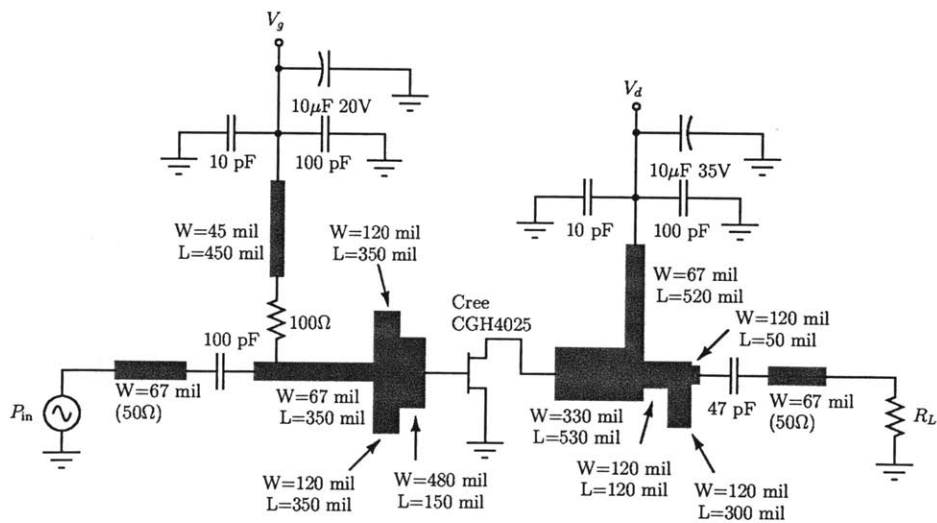


Figure 6-3: Class inverse F power amplifier, with layout reproduced from [16]. Not to scale.

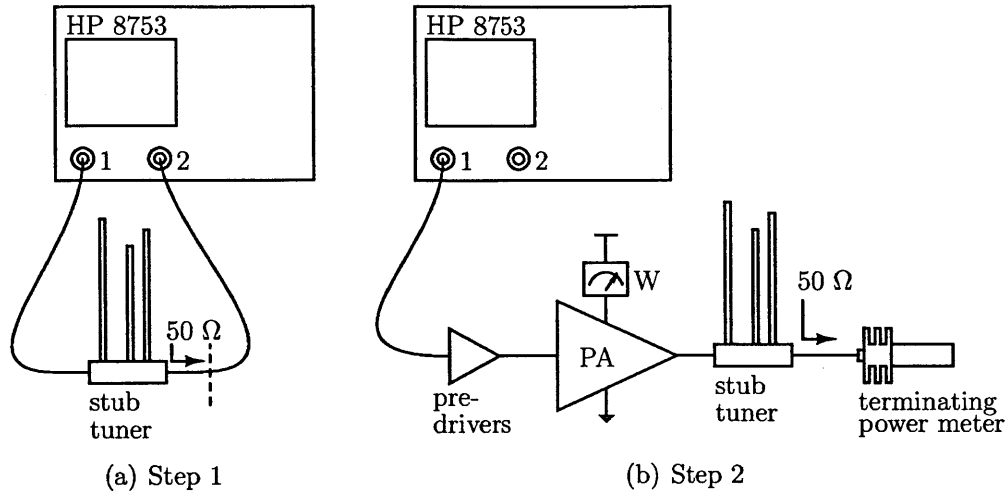


Figure 6-4: Measurement method. First, the stub tuner insertion loss and input impedance for a 50- $\Omega$  termination is measured, then the PA is loaded with that impedance and output power and drain efficiency are measured.

impedance to Port 2 of the VNA, and both  $S_{11}$  and  $S_{21}$  are measured. The input impedance is calculated from  $S_{11}$ , and the insertion loss is calculated as

$$L = \frac{|S_{21}|^2}{1 - |S_{11}|^2}$$

The stubs are tightened in place once their lengths are set to give the desired  $S_{11}$  and moved into place between the PA and terminating power meter as in Figure 6-4(b).

As part of the PA characterization, it is necessary to determine the net phase rotation between the reference plane at the SMA connector on the PA board and the transistor drain. This phase rotation must be compensated for in the connection between the PA and the combiner PCB (see Section 6.4) so that the mostly real input impedance at the input to the combiner shows up as a real impedance at the drain of the device.

To determine the correct phase rotation, one PA was loaded with a series of impedances having constant  $|S_{11}|$  and varying phase ( $\angle S_{11}$ ) by inserting the stub tuner between the PA output and a terminating power meter. The peak output power for a constant  $|S_{11}|$  is found when  $\angle S_{11} = -74^\circ$ . This peak power angle occurs when the drain of the device sees the *minimum* resistive load. In order for resistive

loading at the reference plane of the combiner input to correspond to peak output power, then, a total  $254^\circ$  rotation away from the load in the Smith chart must be added. In stub tuner tests, this rotation can be inserted by setting the VNA port extensions to rotate the peak power point around to the negative real axis. In the combiner system the correct rotation must be provided by the length of the connection between the PA and combiner PCBs.

After the necessary rotation correction has been made, the stub tuner lengths are set to produce resistive values. The results shown in Figure 6-5 show the PA performance over a range of real load impedances. The average efficiency for  $50\text{-}\Omega$  loading is 75.2%. The emphasis for PA tuning is on output power matching rather than efficiency optimization because the combiner should be driven with equal port amplitudes. The combined performance in Figure 6-5(b) is calculated from the measurements in Figure 6-5(a) by summing the output powers and averaging the efficiencies at each point. This calculation corresponds to truly lossless power combination and therefore represents the best possible performance for an ideal power-combining system using these PAs.

The amplifier PCB is mounted to a CPU cooler carrier as shown in Figure 6-6 to remove excess heat. Conductive thermal grease between the PCB and carrier and between the transistor and a milled slot in the carrier improves heat and electrical conductivity. A copper foil “liner” in the slot between the board and carrier is included to reduce stray inductance created when the slot width is inexact. It was found that PA efficiency using the “bolt and grease” method was comparable to soldering a copper carrier to the PA PCB, and that both methods were more efficient by about 2 percentage points than simply bolting to an aluminum heat sink. Including the copper foil liner improved efficiency for all PAs but by less than 1 percentage point.

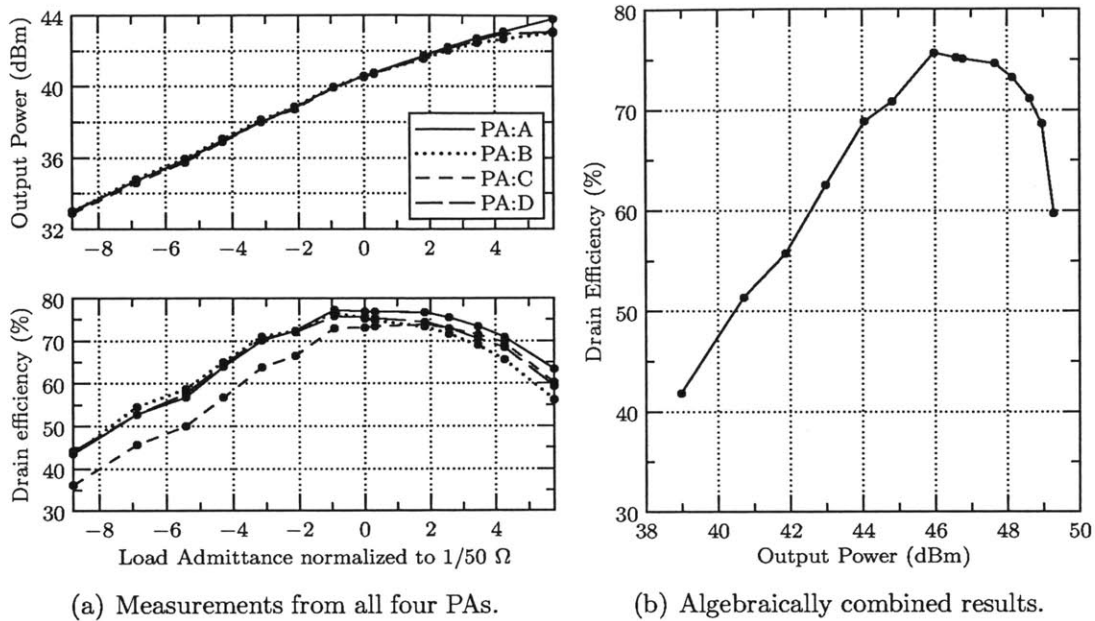
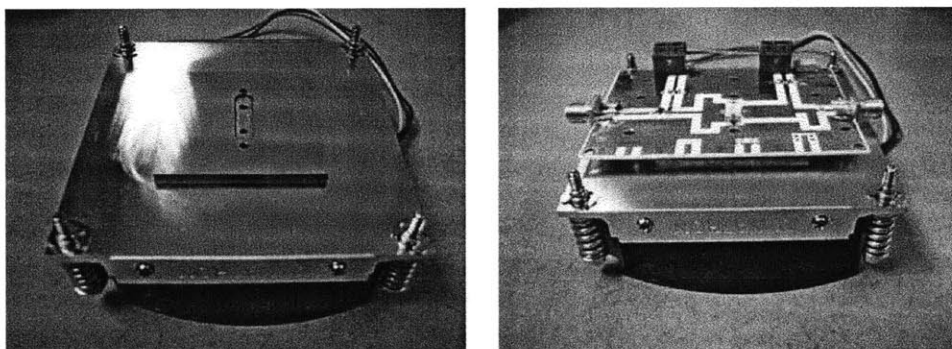


Figure 6-5: PA drain efficiency and output power under load modulation with  $V_g = -3.4 \text{ V}$  and  $V_{DD} = 20 \text{ V}$ .



(a) Carrier with milled slot for the transistor (b) PA mounted carrier for "bolt and grease" method.

Figure 6-6: Photograph of the class inverse F power amplifier.

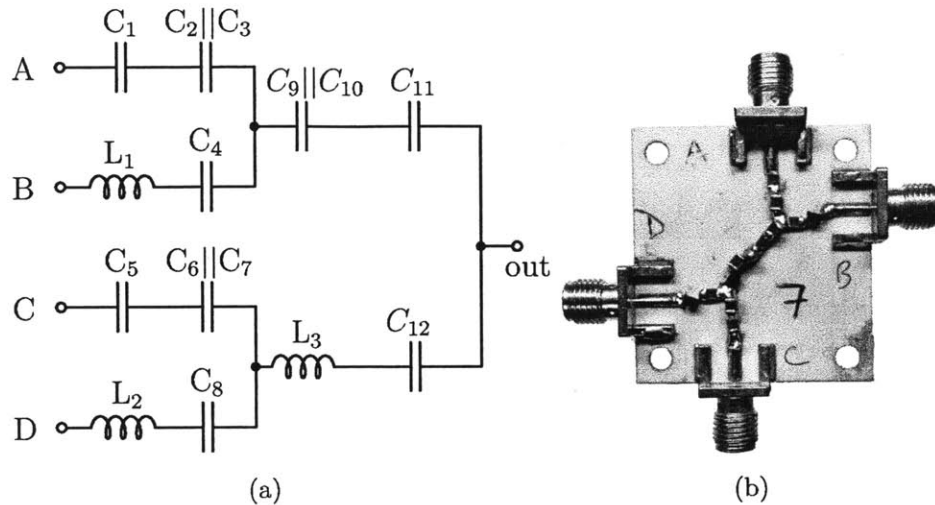


Figure 6-7: Discrete-component combiner implementation. The output (center) connector is on the reverse side.

Table 6.1: Component values for the implemented combiner.

Component	Value	Part #	Manufacturer
$C_{10}$	1pF	MC08CA010D-F	Cornell
$C_1$ - $C_8$ , $C_{11}$ , $C_{12}$	2pF	MC08CA020D-F	Dubilier
$C_9$	3pF	MC08CA030D-F	(ML-Series)
$L_1$ , $L_2$ , $L_3$	3.85 nH	0906-4GLB	CoilCraft

### 6.3 Discrete Combiner Design

The discrete-component combiner is constructed with CoilCraft Micro Spring inductors and Cornell Dubilier ML-series silver mica capacitors. Inductive branch impedances are synthesized from series L and C combinations in order to provide DC blocking. Capacitive branch impedances use both series and parallel capacitor combinations. All branches have approximately the same total physical length.

An important aspect of the combiner design is the tuning of the component values. The available CDE capacitors have values limited to 1pF, 2pF, 3pF, 5pF, and 10pF in a 100 V 0603 package. Consequently, the calculated capacitor values serve only as a starting point for a component trimming process. The combiner is characterized

Table 6.2: Measured and simulated ( $k = 1.05$ ) port amplitudes and phases when output is driven and input ports are terminated in  $50 \Omega$ .

Port	Measured		Simulated	
	Amplitude	Phase	Amplitude	Phase
A	1.02	+86°	1.00	+88°
B	0.97	+16°	1.00	+17°
C	1.01	-16°	1.00	-17°
D	1.01	-87°	1.00	-88°

by driving the center (output) terminal and comparing the measured amplitude and phase of the signals at the  $50\text{-}\Omega$  terminated input terminals to the theoretical values. Initially, the  $+jX_2$  and  $-jX_2$  branches are each shorted across in turn, and the phase and amplitude relationship between terminal pairs A,B and C,D are trimmed by selecting the branch capacitor values. Capacitors are stacked in parallel where necessary. Then, the phase relationship between the two port pairs is set by choosing the capacitor values that set  $\pm jX_2$ . This methodology addresses phase shifts and shunt capacitances occurring due to the physical size of the components. The combiner implemented with the values in Table 1 (see Figure 6-7) has amplitudes that match within  $\pm 3\%$  and phases that are within 2 degrees of the theoretical values for a combiner with  $k = 1.05$  and  $R_L = 50 \Omega$ . The measured combiner performance is summarized in Table 6.2.

The combiner efficiency is measured for  $50\text{-}\Omega$  terminations by driving the output port and measuring the total power transmission to each input port. The total efficiency of the combiner and connectors under this loading condition is 93.5%. Note that the efficiency is expected to vary with load impedances (or, outphasing angles). Furthermore, the measurement is made with a 20-dBm drive from the VNA, and the efficiency is not necessarily constant with power level.



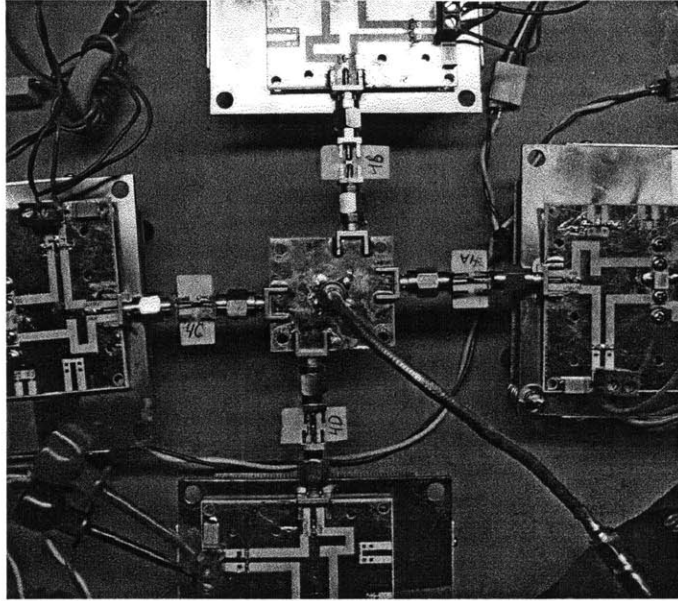


Figure 6-8: The complete RF power stage with connector lengths that provide a net  $\lambda/4$  between the PA and combiner boards.

## 6.4 Connector Lengths

For prototyping purposes, the combiner is built on a separate PCB from the power amplifiers, with the RF power stage connected as shown in Figure 6-8. The electrical length of the connectors between the boards, or equivalently the trace of the connection between the PAs and the reference plane of the combiner in a combined, single-PCB version, is critical. The length must be chosen so that the real impedance at the combiner reference plane appears as a real impedance to the amplifier. There are two options for connector length; it can provide a net half-wave rotation (no net rotation) or a quarter-wave rotation (impedance inversion). The half-wave connector results in behavior closest to that described in Chapter 5. The PAs operate as constant-amplitude voltage sources and the output power is modulated by controlling the load impedance  $R_L$  seen by each PA, so that the power into the combiner from each PA is  $P = V_S^2/R_L$ . The total system output power is inversely proportional to the load impedance seen by the PAs, which is in turn controlled by the outphasing control law.

A quarter-wave connector has the advantage of being physically shorter and therefore has a lower insertion loss. In this case, the input impedance to the combiner is transformed by the quarter-wave line so that the load impedance seen by the PAs increases. Thus, the load impedance seen by each PA *increases* with the commanded power set by the outphasing control law.

The choice of  $\lambda/4$  or  $\lambda/2$  length depends on the primary source of loss in the combiner. If the combiner efficiency is dominated by resistive losses, then a quarter-wave connector is preferred, because the branch current depends on output power rather than being constant. On the other hand, if the primary loss is due to charging and discharging the capacitance of the board substrate, then the constant current of the half-wave connector is preferred. An additional consideration is the effect of the connector on the PA harmonic loading. A  $\lambda/4$  connector will rotate the load impedance by 180 degrees in the Smith chart at all odd harmonics, which may affect PA efficiency.

The best connector length for this system is found experimentally by measuring the system performance for a variety of connectors. Each connector's rotation was found by measuring its  $\angle S_{11}$  when one end was terminated in an open. Then, the efficiency and output power are measured when that connector is used with the OS control law (see Section 5.2.2). The results are plotted in Figure 6-9. The angle of each dataset (groups of points along a constant angle) corresponds to  $\angle S_{11}$  of the connector when terminated by an open. The radius is normalized output power (dB), and the contours indicate lines of constant drain efficiency. The dataset at  $\angle S_{11} = 111^\circ$  has the highest drain efficiency over the range of output powers measured. This experimental methodology allows for the connectors to absorb to some extent the transmission line effects associated with the physical length of the combiner discrete components.

For this work, it was found that the  $\lambda/4$  line had the highest overall efficiency performance when  $V_{DD} = 20V$ . The 434-mil long PCB-based connectors that can be seen in Fig. 6-8 between the four individual amplifiers and the combiner board provide the phase rotation between the combiner and the amplifier.

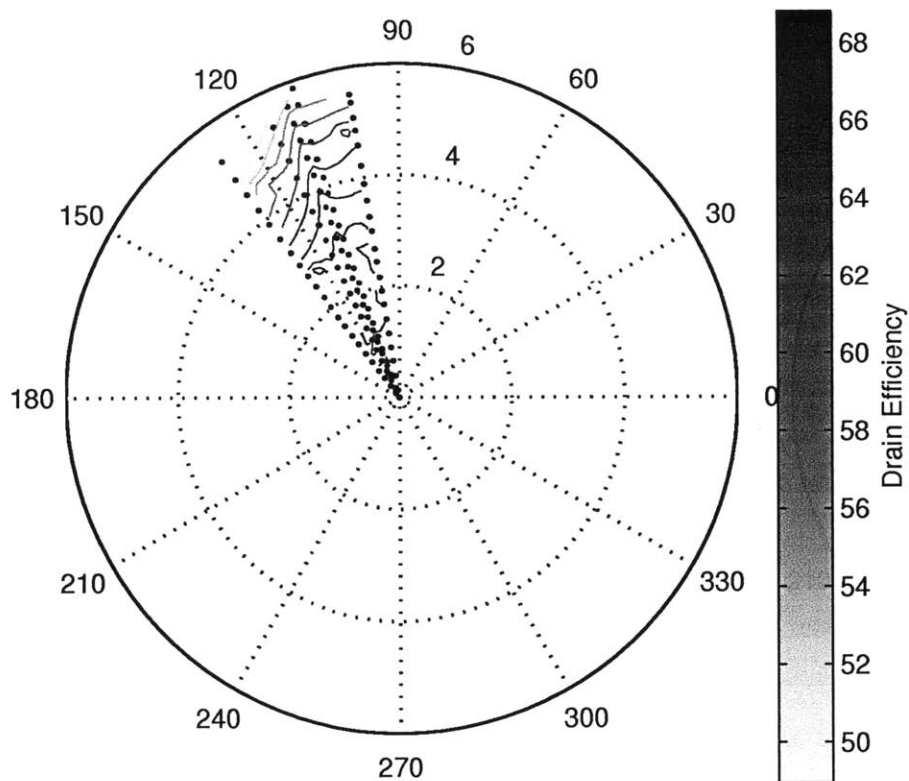


Figure 6-9: Contour plot of system performance with different connector lengths between the PA and combiner PCBs. The angle of each dataset corresponds to the connector rotation, the radius is the normalized output power, and the shaded contours indicate lines of constant drain efficiency.

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# Chapter 7

## Four-Way Lossless Outphasing Combiner: Measured Results

The building blocks in Chapter 6 are combined to demonstrate the first-ever prototype of the four-way lossless outphasing system at microwave frequencies. The experimental system block diagram is shown in Figure 7-1. Characterization is performed using an Agilent MXA N9020A Signal Analyzer and an Agilent DSO80000B oscilloscope. An HP 8482B terminating power sensor with an HP 436A power meter meter is used to calibrate the output power measurements made with the signal analyzer as it provides the most accurate power measurement of the available instrumentation. The oscilloscope is connected through a GPIB interface to a computer running 9600 Vector Signal Analyzer (VSA) software which demodulates the output signal in modulated tests.

A photograph of the complete test bench and a close-up of the RF power stage are shown in Figure 7-2. Also visible in Figure 7-2(b) is part of the Tide Water VGA Liquid Cooling system used to cool the combiner PCB. The cooling element is clamped to a free corner of the combiner PCB and heat exchanging is done remotely. Liquid cooling is used because of the space constraints due to the density of components and connectors on the combiner PCB that make a standard heatsink/fan impractical. In a production version of this system, the power amplifiers and combiner would be built on a single PCB with one cooling system.

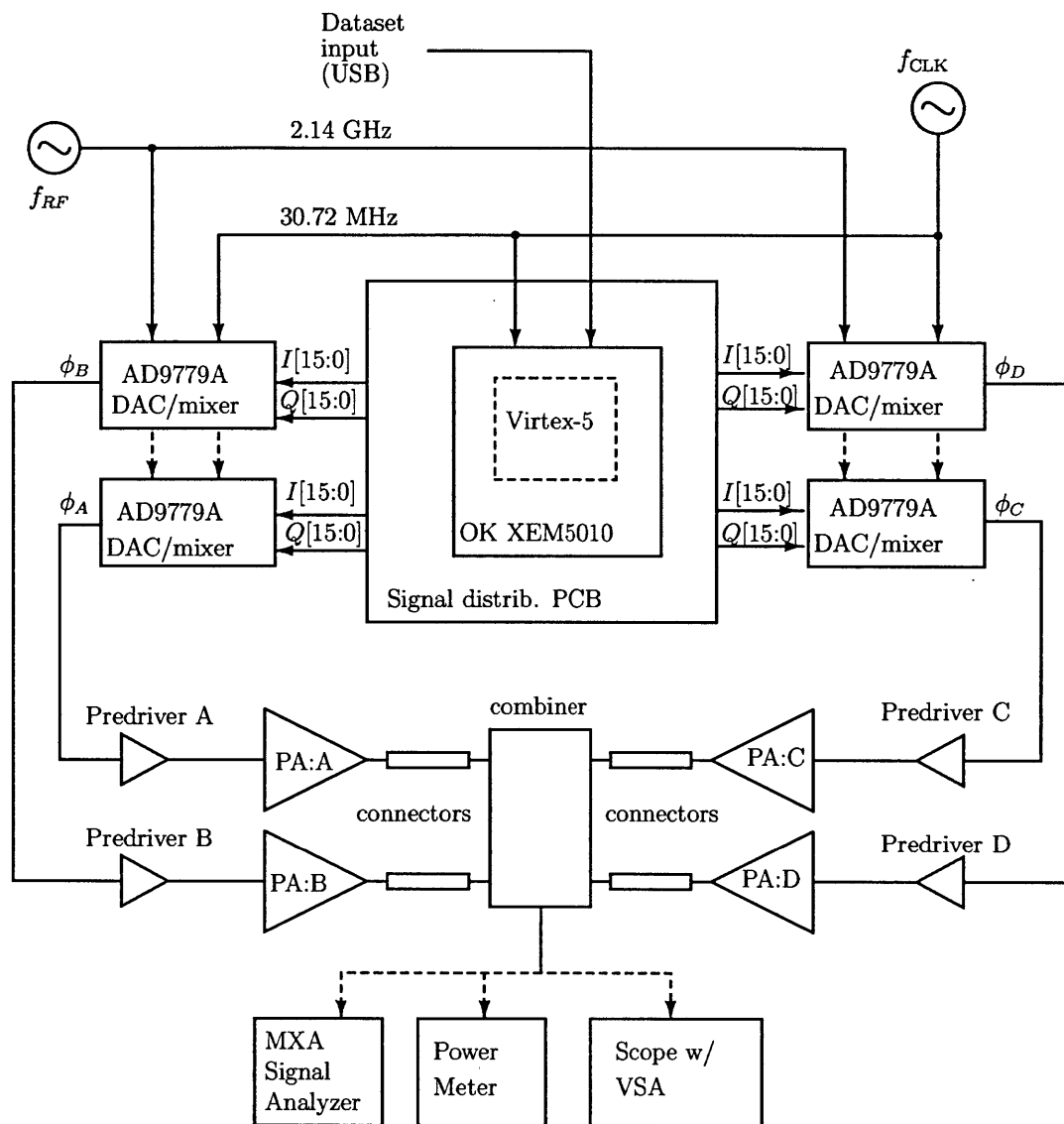
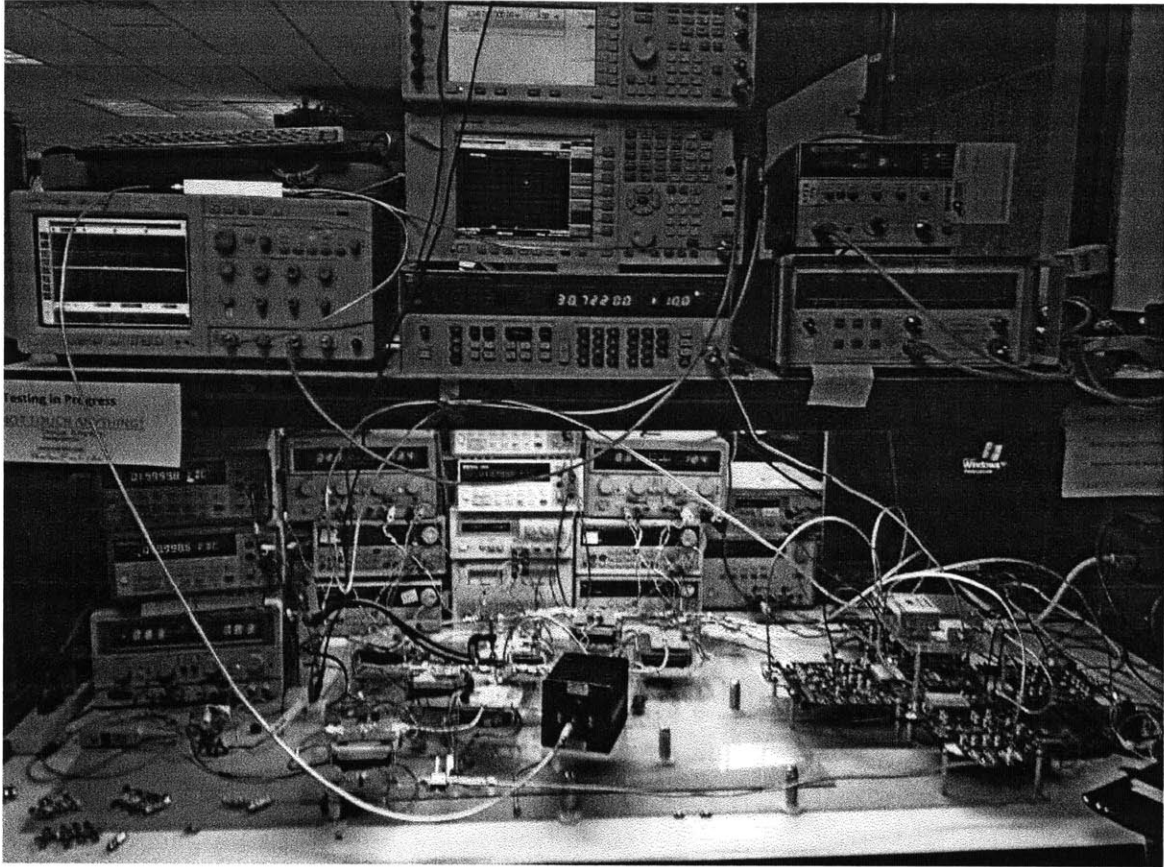
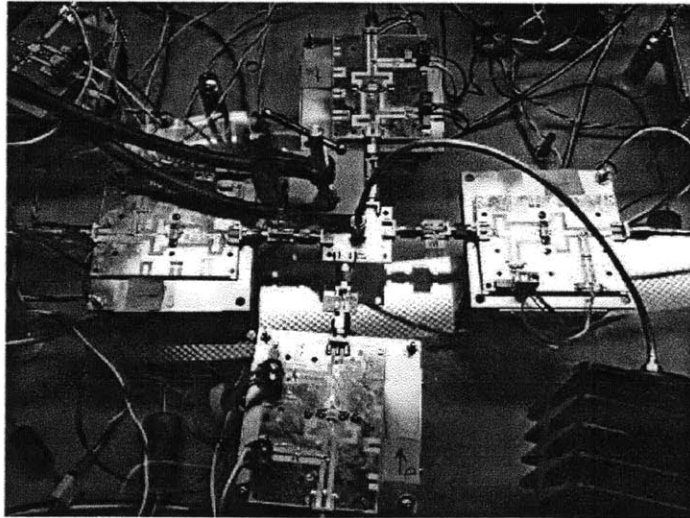


Figure 7-1: Measurement setup block diagram.



(a) Complete setup.



(b) RF power stage.

Figure 7-2: Four-way lossless outphasing and combining system measurement setup.

## 7.1 Static Performance

Static measurements are used to gain understanding of the outphasing control law performance. For these measurements, averaged system output power and drain efficiency measurements are made for each setting over a slow (sub-Hz) input sweep. Drain efficiency is shown in Figure 7-3 when the optimal susceptance outphasing control law is used to produce output powers over a 5.5-dB range. The PA drive power is held constant at maximum power for the outphasing curve (black). Also shown in Figure 7-3 are efficiency curves for drive backoff with various fixed outphasing angles (dashed curves). Below a 42-dBm output power, it becomes advantageous to use drive backoff rather than outphasing for power control. For outphasing alone, the system drain efficiency is greater than 55% over the entire output power range and has a peak value of 68.9%. The efficiency advantage of the four-way lossless power combining system over conventional backoff operation is evident.

The 46-dBm output power point in Figure 7-3 corresponds outphasing angles set for  $P_N = 1$ , i.e. 50- $\Omega$  PA loading. At this output power level, the outphasing system total drain efficiency is 9.5 percentage points lower than the total drain efficiency when all four PAs are independently driven into 50- $\Omega$  loads. The combiner efficiency with all ports terminated in 50  $\Omega$  is 93.5% (see Section 6.3). The close match between these efficiencies indicates that the combiner is working as expected to provide nearly-resistive loading to the power amplifiers. The 3 percentage point discrepancy in these values is most likely related to power-level-dependant losses in the power combiner.

The plot in Figure 7-4 is generated by calculating the percentage of total drain current that is provided by each of the four PAs at a given commanded power  $P_N$ . This drain current measurement is the best indicator available to observe the PA operation, as inserting any instrumentation between the PAs and combiner would alter the performance of the system. Note that the distribution of drain currents will not be equal when the PAs are loaded identically due to the mismatch in their efficiencies. Nonetheless, this plot shows the same characteristic shape, particularly noticeable where the current curves cross, as is expected from the plot of PA loading



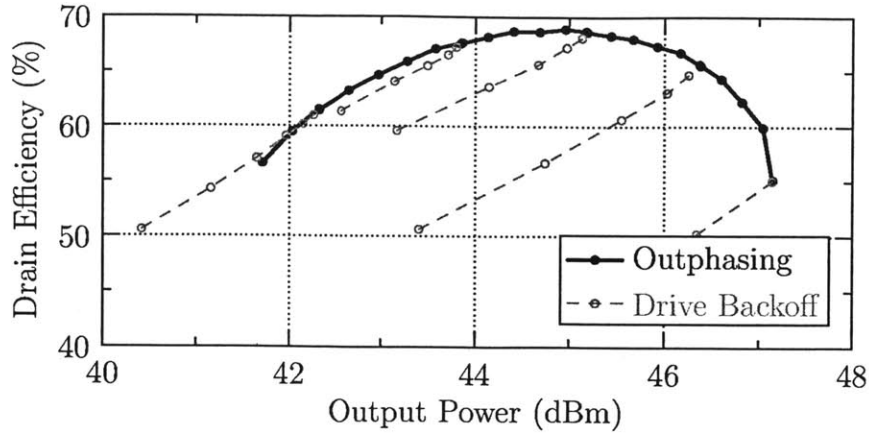


Figure 7-3: Measured drain efficiency and output power of the outphasing system (black) and single inverse class-F PA under load modulation (grey, dashed).

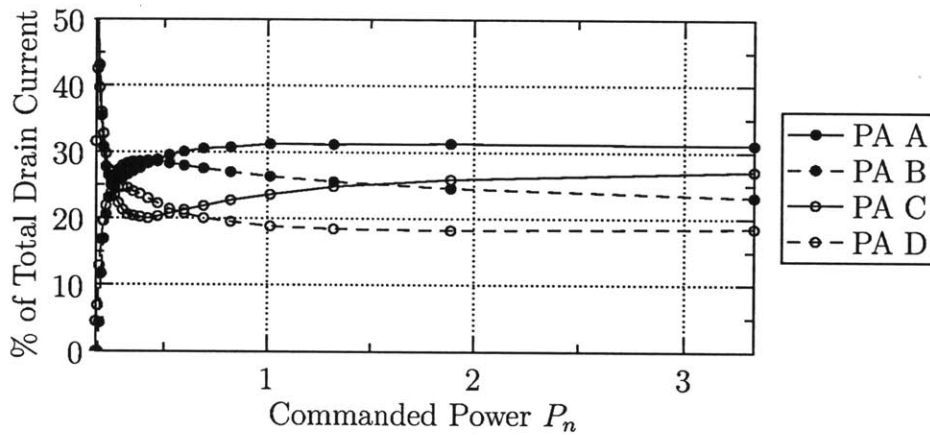


Figure 7-4: Percentage of total drain current provided by each PA over the range of measured outphasing commands.

in Figure 5-4.

The effect of nonidealities in the system including combiner branch impedance values and the behavior of the PAs under load modulation will potentially result in system behavior where the OS control law does not correspond to optimal efficiency performance. With this in mind, the outphasing control angles are swept with  $\phi$  varied around its the nominal values calculated from the OS law. The resulting output powers and drain efficiencies are plotted as a function of the two outphasing angles  $\phi$  and  $\theta$  in Figure 7-5. A new control law can be derived experimentally

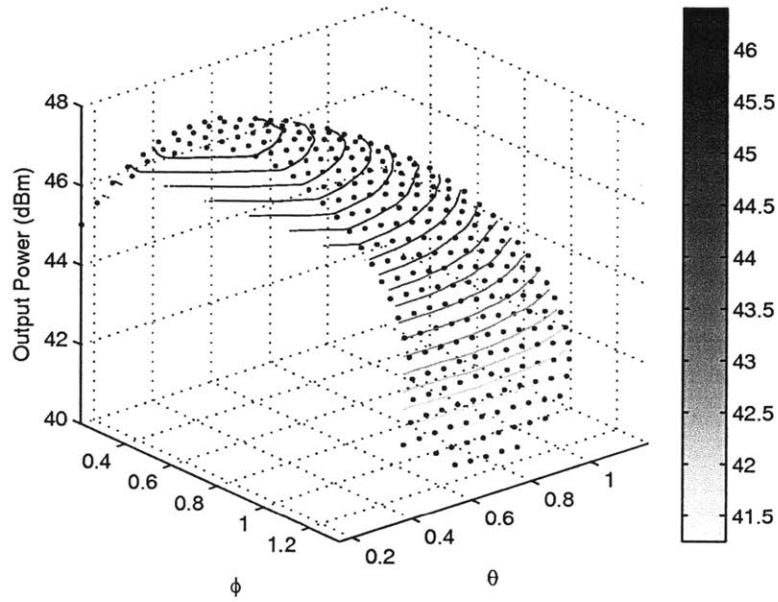
from these results by choosing the slice through this measured data that provides the highest overall drain efficiency for each output power. The peak efficiency point over all  $\theta$  and  $\phi$  values, however, occurs at a point on the OS control law curve, and the efficiency gains at other output powers are limited to approximately one percentage point. For modulated testing the straightforward OS control law was used in order to limit the complexity of the linearization lookup tables.

## 7.2 Dynamic Performance

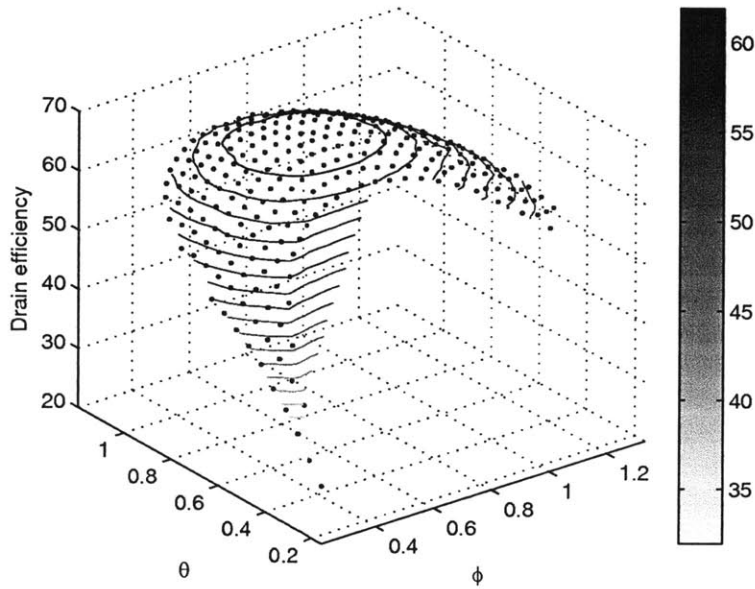
The dynamic performance of the four-way lossless power combining system is characterized both in terms of its transient response to a step and its performance in modulated tests for communication. For this work the intention is to demonstrate first that the system bandwidth is sufficient for communications systems, and second that it will be possible to control the inputs in a way that corrects for the system nonlinearities.

Like all modern communications systems, this one requires digital predistortion (DPD) for linear operation. Compared to the static DPD lookup table (LUT) used for the DRFPM and for AMO measurements in [14], the predistortion for this system is significantly more complicated due to thermal effects. The PAs have temperature dependant gain with a thermal time constant on the order of hundreds of microseconds. A “static” LUT characterized by measuring the output power and phase over many seconds of averaging is not useful for linearizing a modulated signal because the die temperature during LUT characterization does not match that during operation.

The four-way lossless power combining system is particularly sensitive to temperature dependant gains in the power amplifiers because it uses load modulation and drive backoff to modulate the output power. An outphasing system with an isolating combiner would not be affected to the same extent because the PA operating conditions are essentially constant regardless of system output power. The PAs are always loaded with  $50\text{-}\Omega$  terminations (by the isolating combiner), and are driven with a constant-amplitude phase-modulated signal. Thus the operating temperature of the



(a) Output Power (dBm).



(b) Drain Efficiency (%).

Figure 7-5: Output power and drain efficiency measurements and calculated contours when the outphasing angles are swept around the values calculated from the OS control law.

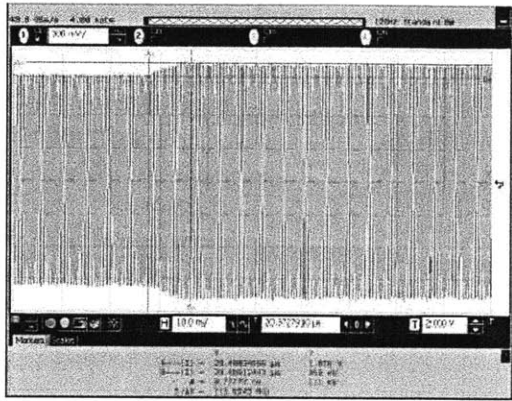
PAs should be constant, and any potential for memory effects would result from some aspect of the phase modulation scheme. Similarly, static predistortion only was used to demonstrate the AMO architecture. Although the PAs experience different operating conditions when the supply voltages are varied, static DPD provides a nearly -40 dBc noise floor [14].

### 7.2.1 Transient Response

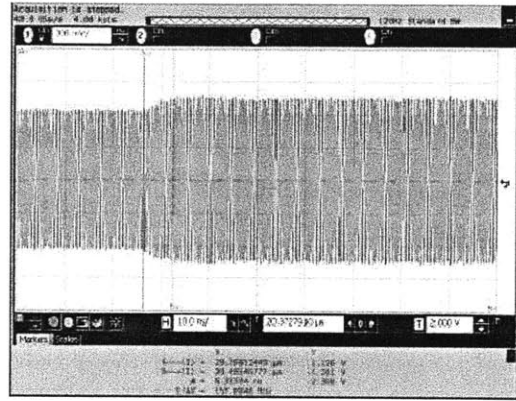
The system transient response depends on operating regime due to the variations in PA response under different loading and drive conditions. A selection of step responses at high, medium, and low amplitudes, with settling times ranging from 6.3 ns to 10.6 ns is shown in Figure 7-6. Also shown are the results of an envelope simulation of the system, performed with ideal voltage sources representing the PAs, and discrete combiner components with finite  $Q$ . The three simulated step responses are offset by their absolute output powers. All three simulated steps, full-scale outphasing, mid-scale outphasing, and drive amplitude step, settle in under 5 ns. The experimental system performance is clearly limited by the speed of the PAs (and/or predriver chains) and not the combiner.

### 7.2.2 Predistortion for Modulated Tests

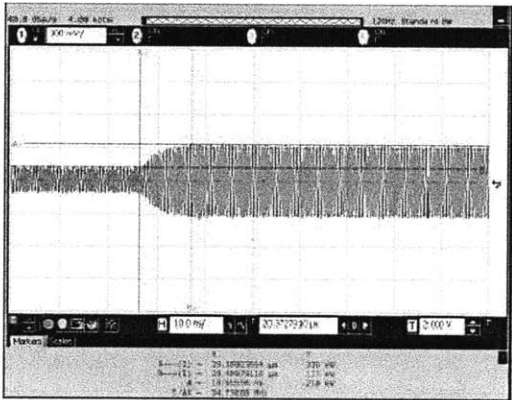
Digital predistortion is applied using a combination of a static LUT based on outphasing and backoff measurements, as well as sequence-based predistortion. The static predistortion provides a first-pass estimate of the output amplitude, but is based on measurements that do not account for the temperature dependant behavior of the power amplifiers. It also serves to define the outphasing and backoff control laws. For the measurements shown below, outphasing with constant (maximum) drive is used for  $0.42 < 1/P_N < 5.7$ , corresponding to a 5.5-dB output power range. Recall that the prototype system has quarter-wave connectors between the PAs and combiner so that  $1/P_N$  replaces  $P_N$  in the control law in Equation 5.23, i.e.  $1/P_N = 0.42$  corresponds to the maximum output power. This value is chosen experimentally as the



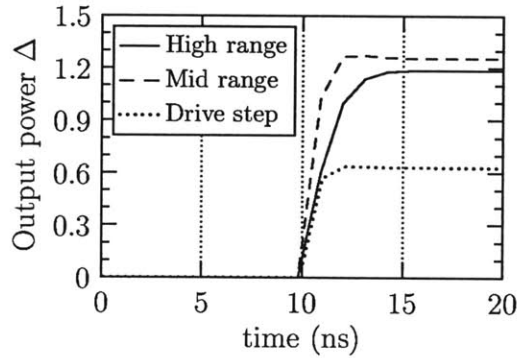
(a) Full scale outphasing step,  $t_s = 8.8$  ns



(b) Mid-scale outphasing step,  $t_s = 6.3$  ns



(c) Low amplitude drive amplitude step,  $t_s = 10.6$  ns



(d) Simulated versions of all steps  $t_s < 5$  ns

Figure 7-6: System step responses under a range of operating conditions, both measured and simulated using ideal voltage sources and a simulated finite-Q discrete-component combiner.

one corresponding to the lowest load impedance the combiner input that the PAs can drive while remaining saturated.

A combination of backoff and outphasing is used in the static LUT for output powers below  $P_{\text{out}} = P_{\text{max}} - 5.5$  dB. When  $1/P_N = 5.7$  and with maximum drive amplitude, the PAs see highly reactive loads, as can be inferred from the drain current plot in Figure 7-4. The PA characteristics are mismatched enough that when the drive power is reduced the relative output phases and amplitudes at the four combiner terminals will vary. This mismatch in behavior creates a potential for the outphasing angles to cause more highly reactive loading for the PAs, particularly problematic when the angles are already set for  $1/P_N = 5.7$ . Therefore as the drive backoff is reduced,  $1/P_N$  is also reduced to a minimum value of  $1/P_N = 2$ , where the system is robust to unequal drive amplitudes and/or phase offsets. For these measurements, a linear relationship between  $1/P_N$  and drive backoff was chosen, but a variety of strategies are possible.

Once the static performance has been characterized, the test signal is transmitted using the LUT for predistortion. The output is downconverted to baseband using the VSA software and recorded at a sample rate of 614.4 MSPS, 20× oversampling of the 30.72-MHz data clock. The output amplitude and phase are averaged over sample periods of the data clock and time-aligned with the input signal, and correction scale factors and phase offsets are calculated based on the mismatch. This process can be repeated for an arbitrary number of iterations; for the measurements below four iterations were used. Errors are particularly high for small amplitudes where the temperature during static LUT is much lower than during operation. An example is shown in Figure 7-7, where the results of four iterations of predistortion are shown for a portion of the transmitted curve with a particularly low amplitude. The linearity could be improved by increasing the number of iterations.

### 7.2.3 W-CDMA Modulation

The four-way lossless combiner is demonstrated using a W-CDMA (Wideband Code Division Multiple Access) signal with 3.47 peak to average ratio (PAPR). The output

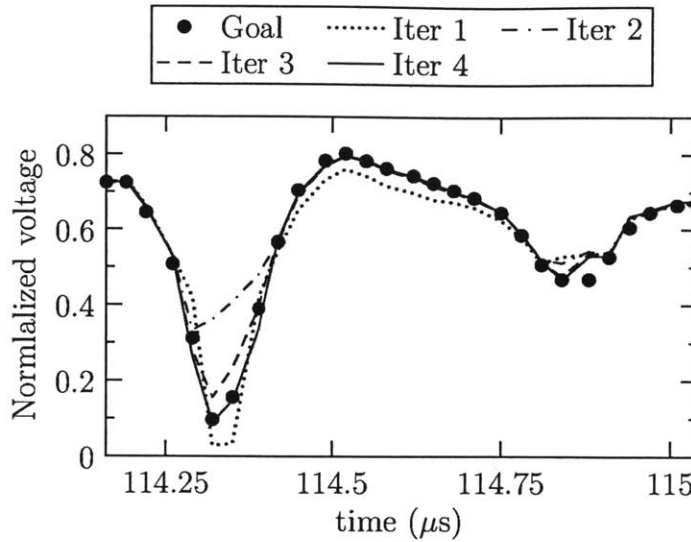


Figure 7-7: Example signal amplitude measurements over four iterations. The system is particularly nonlinear near low amplitudes, as can be seen during the portion of the curve where normalized amplitude is 0.1

spectrum is shown in Figure 7-8 with and without the sequence-based predistortion shown above. The channel output power is 42 dBm, and the average drain efficiency is 57%. This result matches the expected performances based on the static system measurements.

A comparison to other works demonstrating W-CDMA with comparable device technology is summarized in Table 7.1. It is clear that the new four-way lossless power combining and outphasing system is a competitor to other more established architectures such as Doherty. Furthermore, as the efficiency performance of the switching PAs improves due to better device technologies, the four-way lossless combining will only get better. By contrast, the Doherty architecture relies more strongly on drive backoff and therefore has a peak theoretical efficiency lower than that of the architecture in this work.

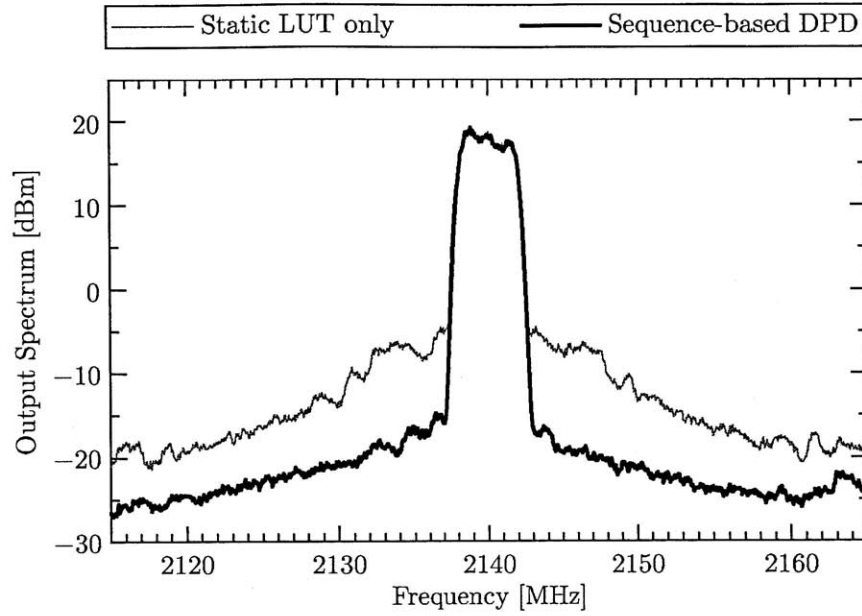


Figure 7-8: W-CDMA signal output spectrum, with and without sequence-based predistortion.

Table 7.1: Comparison of measured four-way combiner results to the state of the art.

System Arch.	Tech.	Carrier Freq.	PAPR	$P_{\text{out}}$	$\text{ACLR}_1$	Drain Eff.
<b>This Work</b>	GaN Cree 25 W	2140 MHz	3.47 dB	42 dBm 15.8 W	-36.6 dBc	57%
<b>Four-stage Doherty [16]</b>	GaN Cree 25 W	2140 MHz	6.5 dB	43 dBm 20 W	-31 dBc	61%
<b>Asymmetric Doherty [9]</b>	GaN In-house	2600 MHz	7 dB	57.3 dBm 537 W	-50.6 dBc	48%
<b>Harmonically Tuned Doherty [1]</b>	GaN Cree 35W	2110 MHz	7.3 dB	40.5 dBm 11.2 W	-44 dBc	41%
<b>Envelope-Tracking [12]</b>	GaN RFMD	800 MHz	-	49.0 dBm 80 W	-50 dBc	51%



# Chapter 8

## Conclusions and Future Work

### 8.1 Summary of Contributions

This work addresses the problem of the inherent linearity/efficiency tradeoff in RF power amplifiers with techniques for power amplification with high average efficiency. As modern communications systems move towards signals with increasingly high peak-to-average power ratios (PAPRs), outphasing architectures become appealing, particularly for high-power systems such as base stations where multiple PA outputs are combined to meet output power requirements. The two main elements in this work, the digital-to-RF phase modulator (DRFPM) and the new four-way lossless outphasing and power combining system, both advance the state of the art of outphasing techniques.

The DRFPM is based on a phase-interpolation approach using weighted sine and cosine vectors of the carrier to produce an arbitrary phase output. The design takes advantage of the requirements of an AMO system, namely that it will drive a switching PA that needs a constant-amplitude drive, and uses a single current-steering DAC to produce the weighting coefficients. The resulting DRFPM has reduced area and power requirements compared to a conventional  $IQ$  modulator approach to phase modulation. Although digital timing errors prevented a full AMO system demonstration, the 65-nm CMOS prototype achieves 2-ns settling times for individual bit transitions. The DRFPM has a 12-bit phase resolution and demonstrated sample rate

of 160 MSPS for a 2.5-GHz carrier, and has a static power consumption of 1 mW from a 1 V supply. A clock pre-distortion method was also demonstrated as a proposed solution to the missing codes resulting from offsets in the weighting coefficients due to device leakage and carrier feedthrough.

The other major contribution of this work is the first-ever demonstration of the four-way lossless outphasing and power combining system at microwave frequencies. This work focuses on the microwave-specific implementation details of that system, including transmission line effects. The experimental prototype demonstrates the basic system behavior including 5.5-dB output power control using outphasing. The drain efficiency over this entire 5.5-dB range is at least as high as the efficiency at peak output power. Although the system requires further effort in predistortion to meet spectral mask requirements, it has been demonstrated that digital predistortion will be effective. Furthermore, the system bandwidth is sufficient to support modern standards including W-CDMA.

## 8.2 Future Work

This work focuses on experimental prototypes of new techniques, which can naturally be extended beyond what is covered in this work. A clear improvement for the DRFPM is improved digital timing in the FPGA-DAC interface. Beyond this, the architecture can be extended for instance to higher frequencies, as is a current research topic being explored by Zhen Li in his work on a phase modulator for a 45-GHz carrier [31]. This 45-GHz DRFPM for a millimeter-wave AMO system has data rate requirements of 2 GSymbols/second and 12-bit phase resolution. The design uses two multiplexed versions of the single-DAC architecture developed in this work. In effect, instead of using the single-DAC idea to halve the required area, the design uses the idea to double the sample rate.

Similarly, the four-way lossless outphasing system represents only an initial effort in a rich research area. The combiner design alone has many topics of interest. The discrete-component design was chosen for this work because tuning of branch

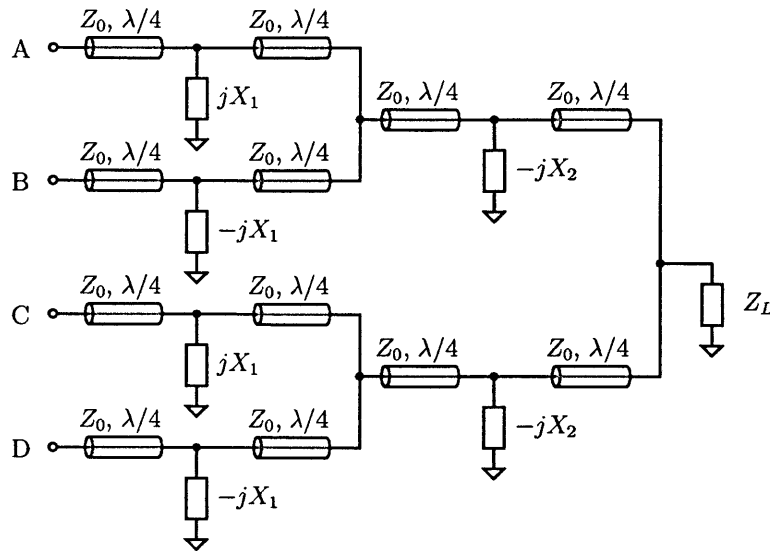


Figure 8-1: Versions of the combiner using microstrips are of interest for applications at microwave frequencies.

impedances is straightforward. In practice, however, tunability is far less desirable than repeatability. A microstrip version of the combiner would have the advantage, after initial design effort, of being easily reproduced. A variety of microstrip topologies can be developed based on the proposed combiner. For example, the topology in Figure 8-1 has the same characteristics as the topological dual (see [38]) of the combiner used in this work, but has no series discrete elements. The shunt elements can be synthesized using either open-circuited stubs or discrete components. Although transmission lines are often associated with narrowband operation, the combiner in Figure 8-1 with ideal discrete shunt components has a simulated envelope step transient of 12.2 ns, comparable with the experimental discrete version. Alternative combiner designs with different  $k$  values may also be of interest, particularly for signals with higher PAPR than the W-CDMA signal used in this work. A practical limitation to  $k$  arises from the PA performance under load modulation. If the PA is efficient even when loaded with high impedances and is not sensitive to e.g.  $\pm 5^\circ$  variation in load admittance, however, a higher  $k$  value may give higher overall efficiency.

Another research direction is combining the ML-LINC idea of switching the power

amplifier supplies between discrete levels with the four-way lossless outphasing system. This method could improve the system efficiency at low output powers, where the resulting efficiency as a function of output power would be made up of a number of curves with the shape of the outphasing measurement in Figure 7-3. Adding drain switching would complicate timing requirements by introducing amplitude paths. Nonetheless, the success of outphasing with drain switching architectures including ML-LINC and AMO indicates that such an architecture would be feasible, and the efficiency benefits may outweigh the cost of additional complexity.

Clearly temperature effects in the PAs must also be addressed for modulated operation. However, the Chireix and Doherty architectures also use load modulation for output power control, and the techniques for linearizing these amplifiers can be adapted to the new system. With some further development the four-way lossless power combining system demonstrated in this work has the potential to outperform more established methods such as Chireix and Doherty amplifiers.

# Bibliography

- [1] K. Bathich and G. Boeck. Wideband harmonically-tuned GaN Doherty power amplifier. In *Microwave Symposium Digest (MTT), 2012 IEEE MTT-S International*, pages 1–3, June 2012.
- [2] K. Bathich, A.Z. Markos, and G. Boeck. A wideband GaN Doherty amplifier with 35% fractional bandwidth. In *Microwave Conference (EuMC), 2010 European*, pages 1006–1009, Sept. 2010.
- [3] O. Casha, I. Greek, and F. Badets. CMOS phase-interpolation DDS for an UWB MB-OFDM alliance application. In *Proc. Conf. on Ph.D. Research in Microelectronics and Electronics*, pages 200–203, Dec. 2009.
- [4] Y. Chen, K. Jheng, A. Wu, H. Tsao, and B. Tzeng. Multilevel LINC system design for wireless transmitters. In *VLSI Design, Automation and Test, 2007. VLSI-DAT 2007. International Symposium on*, pages 1–4, 25-27 2007.
- [5] H. Chireix. High power outphasing modulation. *Proc. IRE*, 23(11):1370–1392, Nov. 1935.
- [6] J. Choi, J. Yim, J. Yang, J. Kim, J. Cha, D. Kang, D. Kim, and B. Kim. A  $\Delta\Sigma$ -digitized polar RF transmitter. *Microwave Theory and Techniques, IEEE Transactions on*, 55(12):2679–2690, Dec. 2007.
- [7] D. Chowdhury, S.V. Thyagarajan, Lu Ye, E. Alon, and A.M. Niknejad. A fully-integrated efficient CMOS inverse class-D power amplifier for digital polar transmitters. In *Radio Frequency Integrated Circuits Symposium (RFIC), 2011 IEEE*, pages 1–4, June 2011.
- [8] D.C. Cox. Linear amplification with nonlinear components. *IEEE Trans. on Communications*, December 1974.
- [9] H. Deguchi, N. Watanabe, A. Kawano, N. Yoshimura, N. Ui, and K. Ebihara. A 2.6GHz band 537W peak power GaN HEMT asymmetric Doherty amplifier with 48% drain efficiency at 7dB. In *Microwave Symposium Digest (MTT), 2012 IEEE MTT-S International*, pages 1–3, June 2012.
- [10] J. Deveugele and M.S.J. Steyaert. A 10-bit 250-MS/s binary-weighted current-steering DAC. 41(2):320–329, Feb. 2006.

- [11] W.H. Doherty. A new high efficiency power amplifier for modulated waves. *Proceedings of the Institute of Radio Engineers*, 24(9):1163 – 1182, sept. 1936.
- [12] N. Giovannelli, A. Cidronali, M. Mercanti, R. Hernaman, G. Wimpenny, and G. Manes. A 80 W broadband GaN HEMT envelope tracking PA harmonically tuned for WCDMA and LTE with 50% average efficiency. In *Microwave Symposium Digest (MTT), 2012 IEEE MTT-S International*, pages 1 –3, June 2012.
- [13] P.A. Godoy. *Techniques for High-Efficiency Outphasing Power Amplifiers*. PhD thesis, Massachusetts Institute of Technology, 2011.
- [14] P.A. Godoy, S. Chung, T.W. Barton, D.J. Perreault, and J.L. Dawson. A 2.4-GHz, 27-dBm asymmetric multilevel outphasing power amplifier in 65-nm CMOS. *IEEE Journal of Solid-State Circuits*, Accepted Feb. 2012.
- [15] P.A. Godoy, D.J. Perreault, and J.L. Dawson. Outphasing energy recovery amplifier with resistance compression for improved efficiency. *IEEE Transactions on Microwave Theory and Techniques*, Dec. 2009.
- [16] A. Grebennikov. A high-efficiency 100-W four-stage doherty GaN HEMT power amplifier module for WCDMA systems. In *IEEE 2011 Int. Microwave Symp.*, pages 1 –4, June 2011.
- [17] A. Grebennikov and N.O. Sokal. *Switchmode RF Power Amplifiers*. Communications Engineering Series. Elsevier/Newnes, 2007.
- [18] I. Hakala, D.K. Choi, L. Gharavi, N. Kajakine, J. Koskela, and R. Kaunisto. A 2.14-GHz Chireix outphasing transmitter. *Microwave Theory and Techniques, IEEE Transactions on*, 53(6):2129 – 2138, June 2005.
- [19] D.C. Hamill. Time reversal duality between linear networks. *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, 43(1):63 –65, Jan. 1996.
- [20] Y. Han, O. Leitermann, D. A. Jackson, J. M. Rivas, and D. J. Perreault. Resistance compression networks for radio-frequency power conversion. *Power Electronics, IEEE Transactions on*, 22(1):41 –53, Jan. 2007.
- [21] X. He, J. van Sinderen, and R. Rutten. A 45nm WCDMA transmitter using direct quadrature voltage modulator with high oversampling digital front-end. In *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International*, pages 62 –63, 2010.
- [22] M.E. Heidari, Minjae Lee, and A.A. Abidi. All-digital outphasing modulator for a software-defined transmitter. 44(4):1260 –1271, April 2009.

- [23] A.S. Jurkov and D.J. Perreault. Design and control of lossless multi-way power combining and outphasing systems. In *Midwest Symp. Circuits and Systems*, pages 1–4, Aug. 2011.
- [24] A.S. Jurkov, L. Roslaniec, and D.J. Perreault. Lossless multi-way power combining and outphasing for high-frequency resonant inverters. In *International Power Electronics and Motion Control Conference (IPEMC)*, June 2012.
- [25] L.R. Kahn. Single-sideband transmission by envelope elimination and restoration. *Proceedings of the IRE*, 40(7):803–806, July 1952.
- [26] J.H. Kim, J.H. Jung, and C.S. Park. 35 W bi-level supply modulated Doherty amplifier for 3G LTE base station. In *Power Amplifiers for Wireless and Radio Applications (PAWR), 2012 IEEE Topical Conference on*, pages 13–16, Jan. 2012.
- [27] H.L. Krauss, C.W. Bostian, and F.H. Raab. *Solid state radio engineering*. Wiley, 1980.
- [28] R. Langridge, T. Thornton, P.M. Asbeck, and L.E. Larson. A power re-use technique for improved efficiency of outphasing microwave power amplifiers. *Microwave Theory and Techniques, IEEE Transactions on*, 47(8):1467–1470, Aug. 1999.
- [29] T.H. Lee. *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press, 2004.
- [30] Z. Li. A sub-ns phase modulator for mm-wave AMO transmitters. unpublished.
- [31] Z. Li, D. Zhang, and J.L. Dawson G. Yahalom. Asymmetric multilevel outphasing for mm-wave transmitters. *MTL Annual Research Report*, 2011.
- [32] C. Marcu, D. Chowdhury, C. Thakkar, Jung-Dong Park, Ling-Kai Kong, M. Tabesh, Yanjie Wang, B. Afshar, A. Gupta, A. Arbabian, S. Gambini, R. Zamani, E. Alon, and A.M. Niknejad. A 90 nm CMOS low-power 60 GHz transceiver with integrated baseband circuitry. 44(12):3434–3447, Dec. 2009.
- [33] S. Moloudi, K. Takinami, M. Youssef, M. Mikhemar, and A. Abidi. An outphasing power amplifier for a software-defined radio transmitter. In *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, pages 568–636, Feb. 2008.
- [34] J. Moon, J. Kim, I. Kim, and B. Kim. Highly efficient three-way saturated Doherty amplifier with digital feedback predistortion. *Microwave and Wireless Components Letters, IEEE*, 18(8):539–541, Aug. 2008.
- [35] J. Moon, J. Lee, R.S. Pengelly, R. Baker, and B. Kim. Highly efficient saturated power amplifier. *Microwave Magazine, IEEE*, 13(1):125–131, Jan.-Feb. 2012.

- [36] S. Pasupathy. Minimum shift keying: A spectrally efficient modulation. *Communications Magazine, IEEE*, 17(4):14–22, July 1979.
- [37] D.J. Perreault. A new power combining and outphasing modulation system for high-efficiency power amplification. *IEEE Trans. Circuits Syst. I, Reg. Papers*, 58(8):1713–1726, Feb. 2011.
- [38] D.J. Perreault and A.S. Jurkov. Radio-frequency (RF) amplifier circuits and related techniques. US Patent Pub. No. US 2011/0187437 A1, Aug. 2011.
- [39] J.H. Qureshi, M.J. Pelk, M. Marchetti, W.C.E. Neo, J.R. Gajadharsing, M.P. van der Heijden, and L.C.N. de Vreede. A 90-W peak power GaN outphasing amplifier with optimum input signal conditioning. *Microwave Theory and Techniques, IEEE Transactions on*, 57(8):1925–1935, Aug. 2009.
- [40] F. Raab, P. Asbeck, S. Cripps, P. Kenington, Z. Popovic, N. Pothecary, J. Sevic, and N. Sokal. RF and microwave power amplifier and transmitter technologies – Part 3. *High Frequency Electronics*, pages 34–48, Sept. 2003.
- [41] F. Wang, D. Kimball, J. Popp, A. Yang, D.Y.C. Lie, P. Asbeck, and L. Larson. Wideband envelope elimination and restoration power amplifier with high efficiency wideband envelope amplifier for WLAN 802.11g applications. In *Microwave Symposium Digest, 2005 IEEE MTT-S International*, June 2005.
- [42] X. Yang and J. Lin. A digitally controlled constant envelope phase-shift modulator for low-power broad-band wireless applications. 54(1):96–105, Jan. 2006.
- [43] X. Yang, J. Lin, K.K. O, and J. Brewer. Design and analysis of a low-power constant envelope phase shift modulator. In *Radio and Wireless Conference, 2004 IEEE*, pages 363 – 366, 19-22 2004.



# Appendix A

## List of Variables Relating to Four-Way Lossless Combiner

$k$	Combiner design variable; represents a tradeoff between the dynamic range of the combiner output power and the average efficiency over that range.
$P_{\text{cmd}}$	The commanded output power for a control scheme analogous to inverse-RCN, i.e. the input power that corresponds to the $[\theta; \phi]$ pair of Equation 5.18 for the RCN.
$P_{\text{N}} = P_{\text{out}}/P_L$	Normalized commanded power used in the outphasing control laws; the system output power normalized by the output power when all PAs see the nominal load $R_L$ .
$P_L = (2V_s^2)/R_L$	System power delivered when each PA load impedance is the nominal load resistance $R_L$ .
$P_{\text{max}}$	Maximum system output power delivered to load.
$P_{\text{out}}$	System output power for a given set of outphasing commands.
$r_0$	An intermediate variable used in the inverse-RCN control law
$V_A, V_B, V_C, V_D$	Terminal voltages at the combiner terminals.