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AlGaN/GaN HEMT With 300-GHz $f_{\max}$

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***Abstract*—We report on a gate-recessed AlGaN/GaN high-electron mobility transistor (HEMT) on a SiC substrate with a record power-gain cutoff frequency ($f_{\max}$). To achieve this high $f_{\max}$, we combined a low-damage gate-recess technology, scaled device geometry, and recessed source/drain ohmic contacts to simultaneously enable minimum short-channel effects (i.e., high output resistance $R_{\rm ds}$) and very low parasitic resistances. A 60-nm-gate-length HEMT with recessed AlGaN barrier exhibited excellent $R_{\rm ds}$ of 95.7 $\Omega \cdot$ mm, $R_{\rm on}$ of 1.1 $\sim$ 1.2 $\Omega \cdot$ mm, and $f_{\max}$ of 300 GHz, with a breakdown voltage of $\sim$20 V. To the authors' knowledge, the obtained $f_{\max}$ is the highest reported to date for any nitride transistor. The accuracy of the $f_{\max}$ value is verified by small signal modeling based on carefully extracted S-parameters.**

***Index Terms*—AlGaN, GaN, gate recess, high-electron mobility transistor (HEMT), maximum oscillation frequency ($f_{\max}$), recessed ohmic, short-channel effects, SiC substrate.**

I. Introduction

GaN-BASED high-electron mobility transistors (HEMTs) have become one of the prime candidates for solid-state power amplifiers at frequencies above 30 GHz. With its unique combination of high electron velocity ($v_{\rm peak} \sim 2.5 \times 10^7$ cm/s) and high breakdown electric field ($\sim$3.3 MV/cm), these devices have already shown excellent performance, including output power densities in excess of 10 W/mm at 40 GHz [1] and more than 2 W/mm at 80.5 GHz [2], far surpassing other technologies (e.g., Si, GaAs, and InP).

In spite of the great progress in performance achieved during the last few years, there are still several important issues that need to be overcome to further increase the performance of GaN HEMTs at millimeter-wave frequencies (30–300 GHz). One of the key challenges to achieve high-gain millimeter-wave power amplification is to increase the maximum power-gain cutoff frequency ($f_{\max}$). $f_{\max}$ is the maximum frequency at which the transistor still provides a power gain and can be expressed as [3]

$$f_{\max} \approx \frac{f_T}{2\sqrt{(R_i + R_s + R_g)/R_{\rm ds} + (2\pi f_T) R_g C_{\rm gd}}} \quad (1)$$

where f_T is the current-gain cutoff frequency and $C_{\rm gd}$ is the gate–drain (depletion region) capacitance, while R_i, R_s, R_g, and $R_{\rm ds}$ represent the gate-charging, source, gate, and output resistance, respectively. To maximize $f_{\max}$, each parameter needs to be carefully optimized. f_T, for example, has been extensively studied and greatly improved by reducing the gate length to 30 nm [4]. However, despite its great importance, other parasitic components have been barely investigated. In this letter, we describe new design features to reduce both short-channel effects ($R_{\rm ds}$ and $C_{\rm gd}$) and parasitic resistances (R_i, R_s, and R_g) to achieve a very high $f_{\max}$.

In field-effect transistors, the short-channel effects play an important role in the high-frequency characteristics [5]. However, improvement of the short-channel effects has been seldom a path to improve the high-frequency performance in GaN HEMTs. In this letter, we applied a low-damage gate-recess technology to effectively suppress the short-channel effects. The resultant HEMT showed excellent output characteristics with a very high $R_{\rm ds}$ of 95.7 $\Omega \cdot$ mm, small $C_{\rm gd}$ of 42.6 fF/mm, and good pinchoff behavior. Also, the closer gate-to-channel distance helped reduce R_i, which is proportional to the charging time of the gate–source capacitance ($C_{\rm gs}$).

The parasitic resistances are also very important in that they can significantly degrade the frequency performance [6], [7]. To minimize them, we combined a short source-to-drain distance and recessed source/drain ohmic contacts [8]. Combination of 1.1-μm source-to-drain distance and optimized ohmic contact resistance (R_c) of 0.15 $\Omega \cdot$ mm resulted in extremely low $R_{\rm on}$ of 1.1 $\sim$ 1.2 $\Omega \cdot$ mm and a knee voltage of only 2 V. In addition, a T-shaped gate was fabricated to reduce R_g. Finally, our 60-nm-gate-length AlGaN/GaN HEMT exhibited a record $f_{\max}$ of 300 GHz, which, to the best of our knowledge, is the highest in any nitride transistor.

II. Device Fabrication

The AlGaN/GaN transistor structure was grown on a SiC substrate by molecular beam epitaxy at Raytheon IDS. This structure produced a 2DEG with a total charge density of $8 \times 10^{12}/\text{cm}^2$ and electron mobility of 2200 $\text{cm}^2/\text{V} \cdot \text{s}$ as measured on unpassivated samples using van der Pauw structures at room temperature. This mobility and charge density translate to a 2DEG sheet resistance of 356 Ω/sq.

Device fabrication began with mesa isolation using a Cl_2/BCl_3 plasma-based dry etch. Then, recessed ohmic technique was used to reduce the ohmic contact resistances. First, source and drain regions with a 1.1-μm separation [Fig. 1(a)] are defined by photolithography, and the AlGaN barrier is slowly etched using a low-power electron cyclotron resonance reactive ion etching (ECR-RIE) with Cl_2/BCl_3 gas mixture. To minimize the damage induced by ion bombardment, RF bias was kept low ($\sim$75 V), while ECR power was set to achieve an etch rate of 1 nm/min ($\sim$100 W). After the recess,

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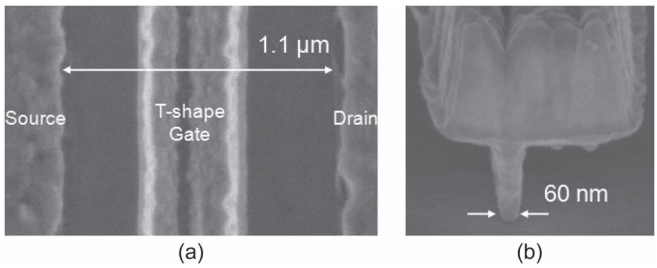


Fig. 1. (a) Plan-view SEM image of the fabricated HEMTs. The source-to-drain distance in this device is 1.1 μm. (b) A cross-sectional SEM image of the 60-nm T-shaped gate.

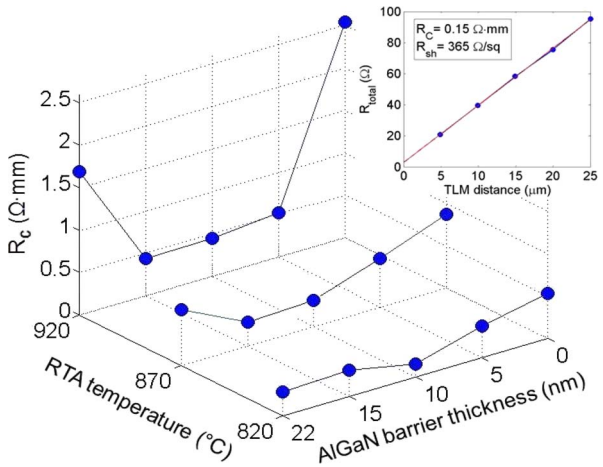


Fig. 2. Measured contact resistance (R_c) as function of RTA temperature and remaining AlGaN barrier thickness. The optimum R_c of 0.15 $\Omega \cdot$ mm was obtained at the 10-nm AlGaN barrier after annealing at 820 °C for 30 s in N_2 ambient. The sheet resistance $(R_{\rm sh})$ was kept almost constant $(\sim 360\ \Omega/{\rm sq})$ in all cases. In the devices with no remaining AlGaN barrier under the contacts, the ohmic contact is formed laterally between the annealed metals and the 2DEG in the unrecessed AlGaN/GaN access region [9].

a Ti/Al/Ni/Au metal stack was deposited, followed by rapid thermal annealing (RTA) for 30 s in the N_2 atmosphere. RTA temperature and remaining AlGaN barrier thickness were experimentally optimized to have the lowest contact resistance, as shown in Fig. 2. The best condition among the range that we explored was found at 820 °C with a 10-nm AlGaN barrier yielding an R_c of 0.15 $\Omega \cdot$ mm, which is one of the lowest contact resistances reported in the literature.

Electron-beam lithography was applied to define a T-shaped gate using a trilayer resist stack made of PMMA/Copolymer/PMMA. For the gate recess, we utilized the same technique as the recessed ohmic. We did not observe any degradation in the source-to-drain current after the recess [10]. Following the gate recess, a Ni/Au/Ni metal stack was deposited for the gate contact. The 60-nm physical gate length was confirmed by scanning electron microscope (SEM), as shown in Fig. 1(b). The devices were not passivated.

III. Results and Discussion

Fig. 3 shows the dc characteristics of the fabricated 60-nm gate-recessed AlGaN/GaN HEMT. The short source-to-drain distance in combination with the low ohmic contact resistance allowed a very low ON-resistance of 1.1 $\sim$ 1.2 $\Omega \cdot$ mm and a knee voltage of only 2 V. Also, the short-channel effects were

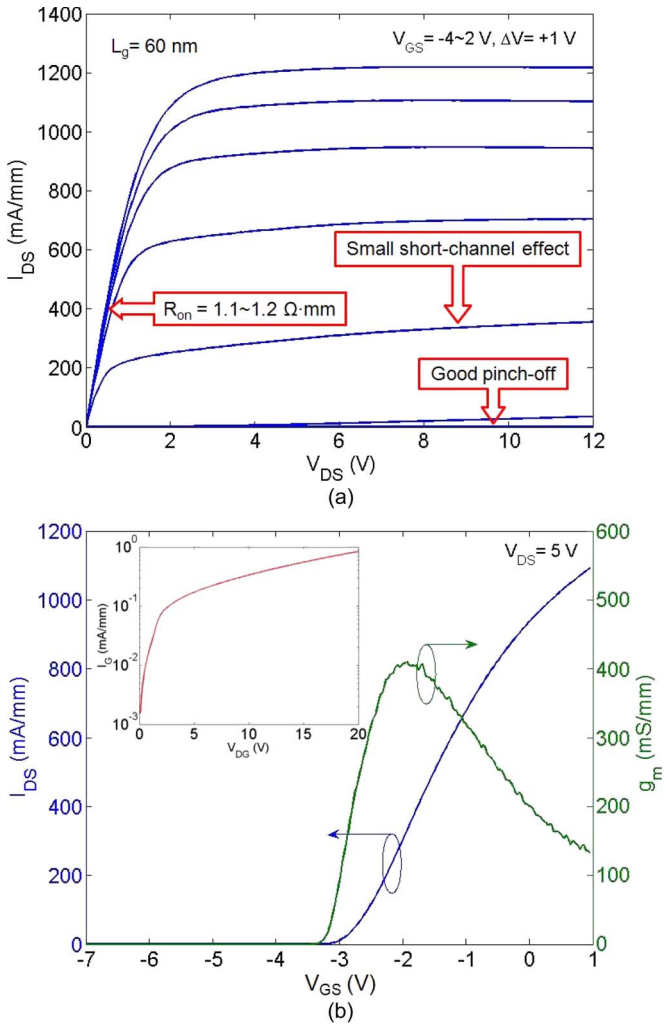


Fig. 3. (a) DC characteristics of the 60-nm gate-recessed AlGaN/GaN HEMT. (a) Output characteristics with a good pinchoff, low $R_{\rm on}$ of 1.1 $\sim$ 1.2 $\Omega \cdot$ mm, knee voltage of just 2 V, and high output resistance (small short-channel effect). (b) Transfer characteristics at $V_{\rm DS} = 5$ V and (inset) the two-terminal gate–drain breakdown voltage of $\sim$20 V defined at a 1-mA/mm reverse gate current.

effectively suppressed by the gate-recess technology as demonstrated by the high output resistance $(R_{\rm ds} = 95.7\ \Omega \cdot {\rm mm})$ and the good pinchoff $(I_{\rm on}/I_{\rm off} \sim 5 \times 10^3)$. This improvement is mainly attributed to better gate control over the channel by improved aspect ratio between the gate length and AlGaN barrier thickness. The maximum drain current at $V_{\rm GS} = 2$ V was 1.2 A/mm, and the peak extrinsic transconductance at $V_{\rm DS} =$ 5 V was 410 mS/mm. The two-terminal gate-drain breakdown voltage was $\sim$20 V. As part of our on-going work, we are currently developing high-k gate dielectric [11] to minimize the gate leakage as well as to allow even more aggressive gate recesses for improved gate modulation efficiency.

The RF performance of these devices was characterized from 0.45 to 50 GHz using an Agilent Technologies N5230A network analyzer. The system was calibrated with a short-open-load-through calibration standard. The calibration was verified by insuring that both S_{12} and S_{21} of the through standard are less than $\pm$ 0.01 dB and that both S_{11} and S_{22} are less than -45 dB within the measured frequency range after the calibration [5]. On-wafer open and short patterns were used to

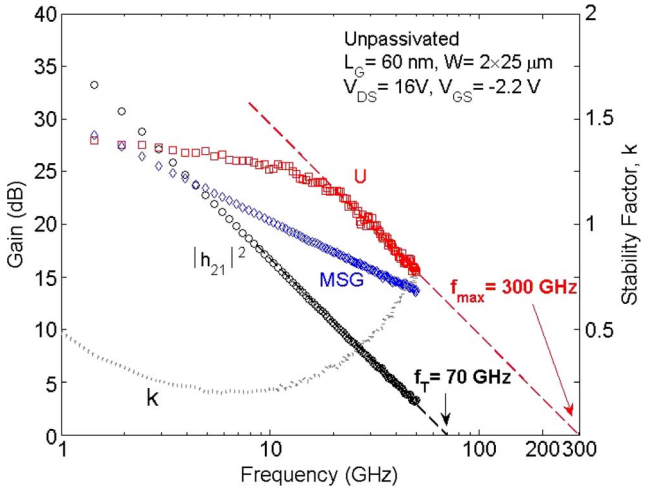
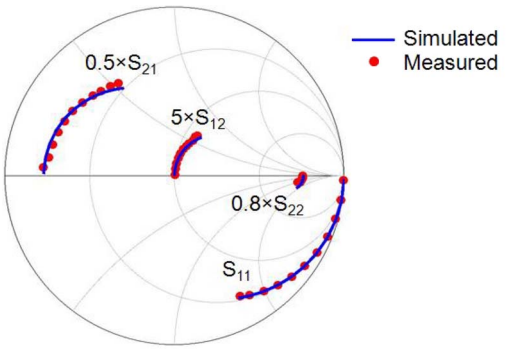


Fig. 4. RF performance of unpassivated 60-nm-gate-length HEMT showing $f_T = 70$ GHz and $f_{\max} = 300$ GHz. The f_T and $f_{\max}$ values are extrapolated following a -20 dB/dec ideal decrease with frequency.



Intrinsic Parameters	Calculated f_T	Measured f_T
$g_{m,i}$= 369.8 mS/mm C_{gs}= 740.8 fF/mm C_{gd}= 42.6 fF/mm R_i= 0.45 Ω·mm R_g= 0.23 Ω·mm R_s= 0.42 Ω·mm R_d = 0.57 Ω·mm R_{ds}= 95.7 Ω·mm	73 GHz	70 GHz
	Calculated f_{max}	**Measured f_{max}**
	288 GHz	300 GHz

Fig. 5. (Top) Comparison of simulated and measured S-parameters at $V_{\rm DS} = 16$ V and $V_{\rm GS} = -2.2$ V. (Bottom) Table shows the extracted intrinsic parameters and calculated $f_T/f_{\max}$.

subtract the effect of parasitic pad capacitances and inductances from the measured S-parameters [12]. Due to the effect of the pad capacitances, the f_T and $f_{\max}$ values calculated from the extrinsic S-parameters were 10% lower than the intrinsic values. The reproducibility error in our measurements due to the calibration was less than 5%. Fig. 4 shows $|h_{21}|^2$ and Mason's unilateral gain U against frequency for the 60-nm-gate-length device at $V_{\rm DS} = 16$ V and $V_{\rm GS} = -2.2$ V. An f_T of 70 GHz and a record $f_{\max}$ of 300 GHz were obtained by extrapolating measured data with a slope of -20 dB/dec using a least-square fit. For comparison, the highest $f_{\max}$ reported so far in nitride transistors was 251 GHz in 4-nm barrier AlGaN/GaN HEMTs with 60-nm gate length [13]. The $f_T/f_{\max}$ values are confirmed through S-parameter simulations in the 0.45–50 GHz range [14], as shown in Fig. 5. The small discrepancy between measurements and simulations (i.e., 300 GHz versus 288 GHz) could originate from incomplete small-signal model or (1) used in this letter. The relatively low f_T value is due to a combination of a lower than expected intrinsic RF transconductance $g_{m,i} \sim 370$ mS/mm (versus the calculated intrinsic dc transconductance of ~490 mS/mm) and the high gate-to-source capacitance ($C_{\rm gs}$) resulting from the extended effective gate length ($L_{\rm eff} = (C_{\rm gs} \cdot d_{\rm AlGaN})/\varepsilon \approx 100$ nm) at the large drain voltage used during the measurements ($V_{\rm DS} = 16$ V).

IV. Conclusion

We have reported $L_g = 60$ nm gate-recessed AlGaN/GaN HEMTs on SiC substrate having a record $f_{\max}$ of 300 GHz. Owing to the low-damage gate recess, short source-to-drain distance, and recessed ohmic contacts, the short-channel effects, as well as parasitic resistances, were effectively suppressed. The fabrication technology and the record $f_{\max}$ reported in this letter demonstrate the unsurpassed potential of GaN transistors for millimeter- and submillimeter-wave power amplifiers.

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