# Automated Wavelength Recovery for Silicon Photonics

by

Erman Timurdogan

Submitted to the Department of Electrical Engineering and Computer Science
in Partial Fulfillment of the Requirements for the Degree of

Master of Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

FEBRUARY 2013

Signature of Author:_____
Department of Electrical Engineering
February 1, 2013

Certified by:_____
Michael R. Watts
Professor of Electrical Engineering
Thesis Supervisor

Accepted by:_____
Leslie A. Kolodziejski
Professor of Electrical Engineering
Chair, Committee for Graduate Students

1

# Automated Wavelength Recovery for Silicon Photonics

by

Erman Timurdogan

Submitted to the Department of Electrical Engineering and Computer Science
on February 1, 2012 in Partial Fulfillment of the Requirements for the Degree of
Master of Science in Electrical Engineering and Computer Science

## ABSTRACT

In 2020, 1Tb/s on-/off-chip communication bandwidth and ~100fJ/bit total energy in a point to point link is predicted by Moore's law for high performance computing applications. These requirements are pushing the limits of on-chip silicon CMOS transistors and off-chip VCSELs technology. The major limitation of the current systems is the lack of ability to enable more than a single channel on a single wire/fiber. Silicon photonics, offering a solution on the same platform with CMOS technology, can enable Wavelength Division Multiplexed (WDM) systems. However, Silicon photonics has to overcome the wafer level, fabrication variations and dynamic temperature fluctuations, induced by processor cores with low-energy high-speed resonators.

In this work, we offer a solution, called as Automated Wavelength Recovery (AWR), to these limitations. In order to demonstrate AWR, we design and demonstrate high performance active silicon resonators. A microdisk modulator achieved open eye-diagrams at a data rate of 25Gb/s and error-free operation up to 20Gb/s. A thermo-optically tunable microdisk modulator with Low power modulation (11fJ/bit) at a data rate of 13-Gb/s, a 5.8-dB extinction ratio, a 1.22-dB insertion loss and a record-low thermal tuning (4.9-$\mu$W/GHz) of a high-speed modulator is achieved. We demonstrated a new L-shaped resonant microring (LRM) modulator that achieves 30 Gb/s error-free operation in a compact ($< 20\ \mu m^2$) structure while maintaining single-mode operation, enabling direct WDM across an uncorrupted 5.3 THz FSR. We have introduced heater elements inside a new single mode filter, a LRM filter, successfully. The LRM filter achieved high-efficiency (3.3$\mu$W/GHz) and high-speed ($\tau_f$ ~1.6 $\mu$s) thermal tuning and maintained signal integrity with record low thru to drop power penalty (<1.1 dB) over the 4 THz FSR and <0.5dB insertion loss. We have integrated a heater driver and adiabatic resonant microring (ARM) filter in a commercial bulk CMOS deep-trench process for the first time. The proposed AWR algorithm is implemented with an ARM multiplexer. An advanced method for AWR is also introduced and demonstrated with passive resonators.

Thesis Supervisor: Michael R. Watts
Title: Professor of Electrical Engineering

## ACKNOWLEDGMENTS

provided brilliant insights in 5 to 10 minutes meetings. His advices and ideas in general pushed me to become a better person in many ways. He is also a considerate person who has been valuable over the bad times. It will be a great pleasure to pursue my studies further in his group.

# Table of Contents

8

# 1. Introduction

Over the course of first chapter, on-/off-chip electrical and optical communications will be introduced with a focus on realization of Wavelength Division Multiplexed (WDM) Silicon Photonics. The roadmap of WDM Silicon Photonics will be summarized and an overview of ways to overcome the challenges of silicon photonics will be given. The need for automated wavelength recovery (AWR) will be justified and the architecture of AWR will be proposed.

## 1.1 Electrical on-/off-chip communications

Since the digital era started with Complementary Metal Oxide Semiconductor (CMOS) technology, the data storage, transmission bandwidth boomed up and the communication technologies scaled the clock frequency, power efficiency, on- and off-chip bandwidth and hard disk capacity. Gordon E. Moore predicted that the number of integrated components (especially transistors) will be doubled at every two year in 1965 [1]. His statement is true since 1965 and it is often called as Moore's Law. P-type and N-type metal oxide semiconductor field effect transistors (NMOS and PMOS) are the building blocks of on-chip communications. Off-chip communications utilized high speed electrical interconnects before the fiber optics and VCSEL technology. The off-chip short distance communication is still dominated with electrical interfaces. Definitions might vary for an electrical link but a simple electrical point to point link should have electrical modulator, switch, filter, amplifier and receiver (Fig. 1).
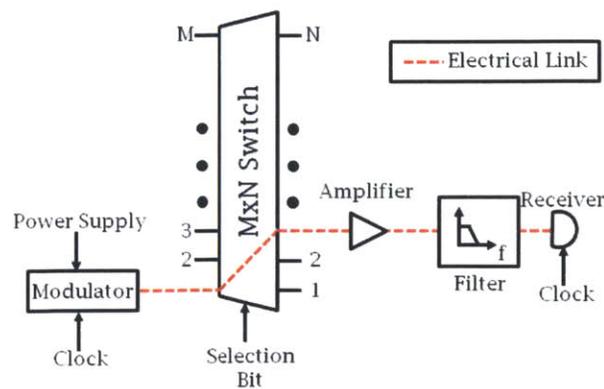


Figure 1. Point to point electrical Link with distributed clock

Digital modulators need to transmit two distinct logic levels; "1"s and "0"s at the local clock frequency. Data at the output of the modulator will be fed to a router or switch. The switch will pass the data to the desired node. The data will be amplified and filtered before it reaches the receiver. The data will be received and sampled using the clock at the end and signal integrity of this transmission will be determined with bit error rate (BER). BER of less than $1\times10^{-12}$, is considered error-free as a communication standard.

On-chip communications is dominated with electronics only due to cost effectiveness and scaling of transistor technology. Clock frequency scaled significantly from 66 MHz (1993, Pentium) to 3.9GHz (2012, Core i7 Extreme). Intel chipset x86 clock frequency is shown in Figure 2 and the clock frequency scaling trend is in good agreement with Moore's Law from 1993 to 2004.
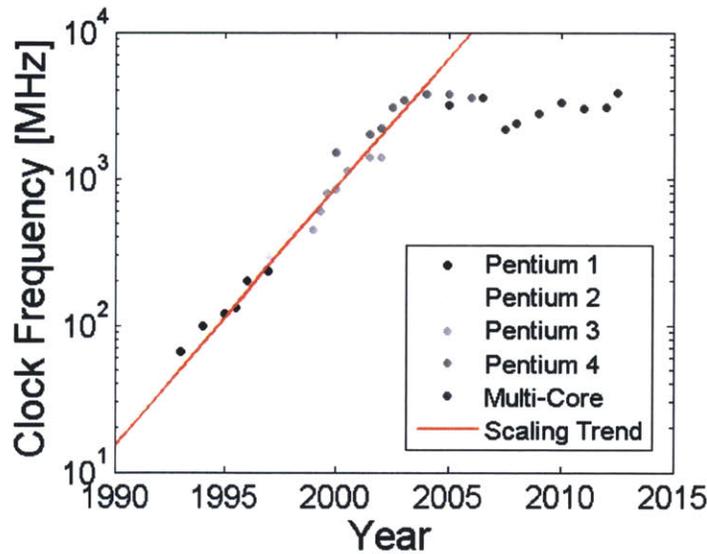


Figure 2. Clock frequency scaling for Intel chipset x86

After 2004, the clock frequency is kept similar to Pentium 4 and the number of cores is increased. Microprocessor area kept same to preserve high yield through the wafers. [2] Instead, the transistor density scaled to improve on-chip performance. This is enabled with research on advanced materials and Silicon fabrication [3-5], low voltage signaling (LVS) [6], memory architecture [7] and multicore design and performance validation [8,9]. These developments targeted to keep the scaling computer

performance. The number of floating-point operations per second (FLOPs) is widely used as a measure of computer performance. Theoretical maximum FLOPs can be calculated as follows [39];

$$FLOPs = N_{core} f_C \frac{Operations}{Core \times Clock\ Cycle}$$

Where, $N_{core}$ is the number of cores and $f_C$ is the clock frequency. Commodity microprocessors can currently at least perform 4 operations whereas supercomputers can perform more than 12 operations per core in single clock cycle. Since this assumes each core is fetching the maximum number of operations, it predicts a theoretical maximum FLOPS. Computer performance is plotted in Figure 3. Commodity computer performance is still increasing with a rate similar to Moore's Law after 2004. Even at this scaling rate, we expect to reach around ~1 TFLOPs by 2020. However, multicore processing does not
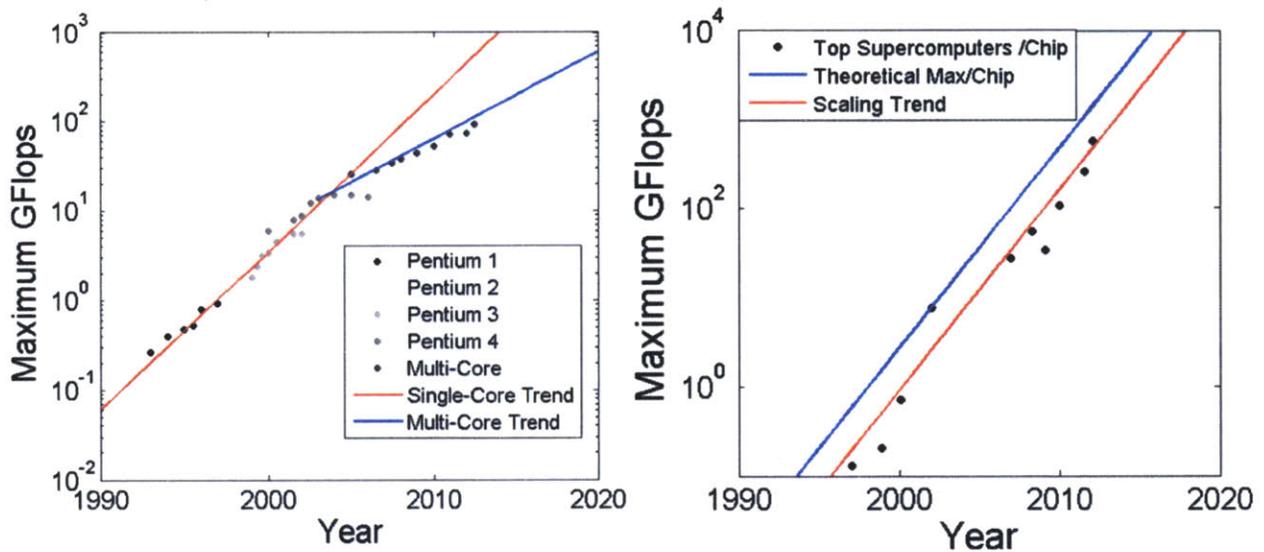


Figure 3. Maximum FLOPs for commodity (left) and supercomputer (right) microprocessor scaling as a measure of computer performance and memory bandwidth. Top Supercomputer FLOPs per chip (right) is calculated based on TOP500.org data. Theoretical maximum FLOPs per chip (right) is calculated using the FLOPs equation.

necessarily boost the performance linearly since some tasks cannot be handled in all cores at the same time. Amdahl has foreseen the future of computing in 1967 [23] and based on his predictions, Amdahl's Law of scaling has been formulated as follows [24];

$$Speedup_{parallel} = \cfrac{1}{r_{seq} + \cfrac{1 - r_{seq}}{N_{core}}}$$

Where, $r_{seq}$ is the ratio of the sequential part of the program, $1 - r_{seq}$ is the ratio of the parallel executable part of the program. Here the program is assumed to be a combination of sequential and parallel part.

If program execution is all parallel, then speedup is linear with number of cores. However, if the tasks are sequential, then there is no speedup due to parallel computing. Therefore, asymmetric multicore chips that combine one or more powerful core and standard cores inside a package and dynamic microprocessors which can arbitrarily interchange between sequential and parallel mode, have been proposed [24]. Both approaches have maximized the parallel computation Speedup than symmetric multicore chips that involve identical cores.

At this point, it is important to understand the trend for how to keep low power at higher clock frequency and having multiple cores. Power of a single transistor can be calculated as the following;

$$P_{tr} = N_{core}\, \alpha\, f_C\, C_{tr}\, V_{DD}^2$$

Where, $P_{tr}$ is the transistor power, $\alpha$ is the encoding scheme related multiplier, $C_{tr}$ is the transistor capacitance and $V_{DD}$ is the supply voltage. For non-return to zero on-off keying (NRZ-OOK) pseudo-random bit sequence (PRBS), there are equal number of 0-0, 0-1, 1-0, 1-1 transitions and the power is only consumed in 0-1 transition. Therefore, $\alpha$ is equal to 1/4. The $C_{tr}, V_{DD}, f_C$ is swept from 0 to 1 to show dependence of transistor power (Fig. 4).
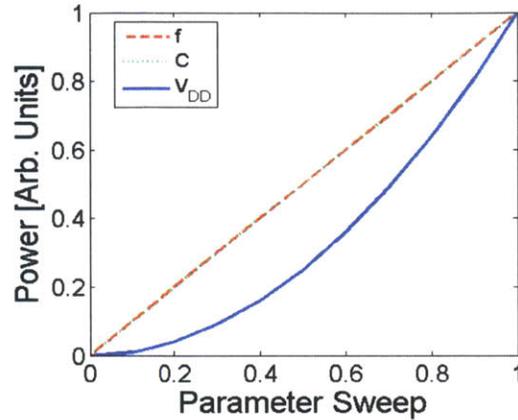
Figure 4. Normalized on-chip power scaling as a function of transistor capacitance, voltage supply and clock frequency

The power consumption will be constant if the transistor capacitance and voltage supply can be lowered while the clock frequency is rising. That is the reason the fabrication processor node is dwarfed from 0.8μm (1993) to 22nm (2012). While the transistor area is scaled down to achieve low power devices, the power density increased significantly. Power and heat density limited the scaling of transistor technology and the multi-core era has started in 2004. The methods for diminishing voltage supply ($V_{DD}$) up to a factor of 2 has been demonstrated recently [10, 11] and it might be an enabler for power and performance scaling.

Before moving from the on-chip to off-chip communications, one must discus about the memory access which is bridging the on- and off-chip communications. On-chip performance is measured by FLOPs and memory or data storage is indicated with bytes per second. The relation between byte (b) and FLOP are reported as 1 b/FLOP [12] for commodity and 0.5 b/FLOP [10] for supercomputers. 1 b/FLOP is regularly quoted for memory bandwidth. Therefore, we expect to reach around 1 Tb/s memory bandwidth in 2020 (Fig. 3). High bandwidth operation will be enabled by 3D CPU and it is predicted to be available by 2013 in 3D integration roadmap (Fig. 5) [33]. The on-/off-chip bandwidth will be bridged using an intermediate vertical connection between board to chip or chip to chip in 3D integration.
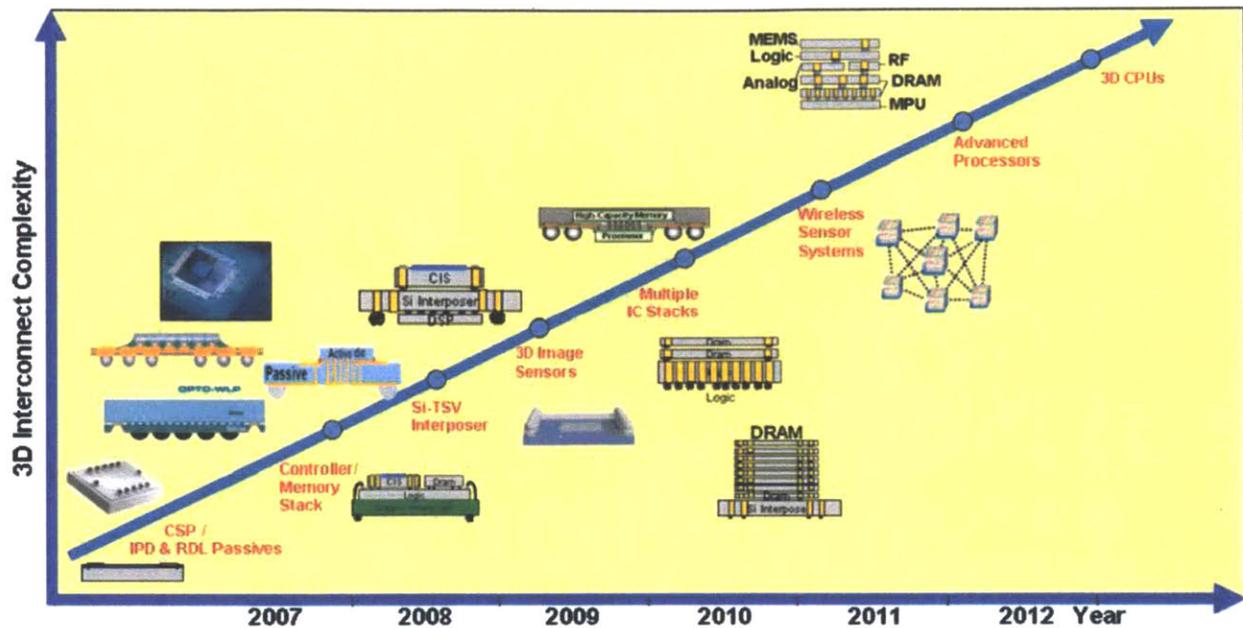
Figure 5. 3D integration complexity and roadmap predicted by Fraunhofer IZM

Ball grid array is being used to achieve high speed interconnects between CMOS chips [26]. Microballs are squeezed by the top and bottom chips to achieve microbump/solder structures (Fig. 6). It can be utilized for CMOS and photonic chip interconnects as well. However, standard pitch is ~50μm and allows
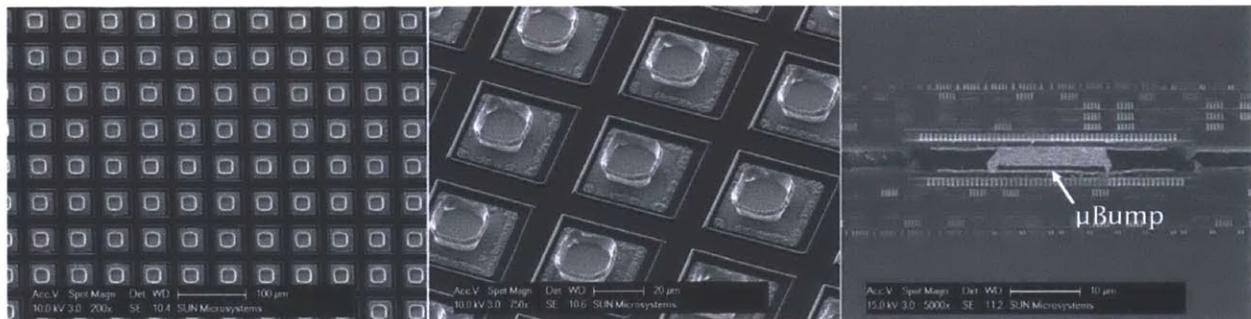


Figure 6. Micgrographs of high density microbump array (left), closeup on microbump array (middle), flip-chip bonding of two CMOS chips (right)

low density interconnects. Therefore, reaching high density interconnects and high off-chip bandwidth requires new methods of chip to chip interconnect.

On the other hand, Through Silicon Via (TSV) is a key alternative since it is an extension of convential via technology implemented in process design kits [22]. TSV is slightly taller than the existing

14

via on a microprocessor which can provide high speed and low latency off-chip interconnects and access to memory compared to existing technologies. TSV is currently formed by Cu, W and Poly-Si (Fig. 7).



Cu-TSV        W-TSV        PolySi-TSV
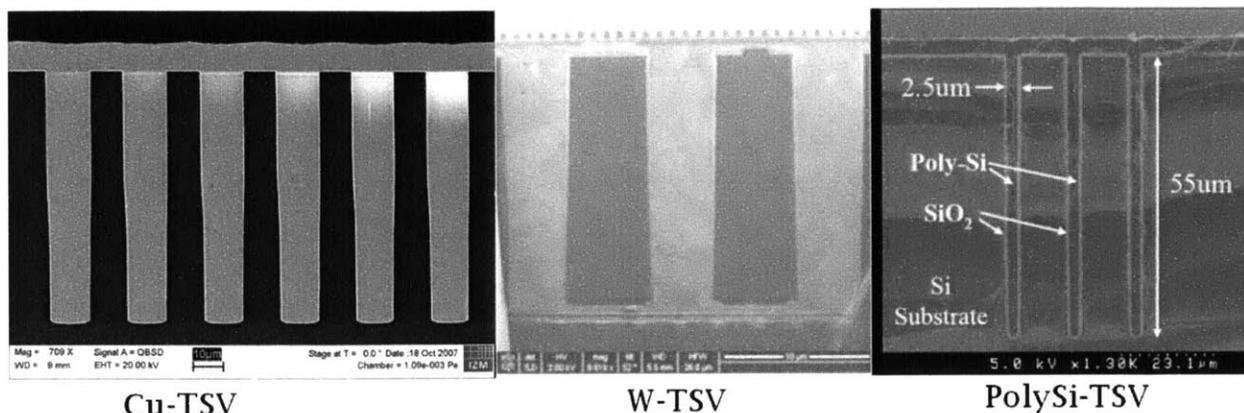
Figure 7. Cu-TSV (Fraunhofer IZM), W-TSV and Poly-si TSV

The common limitations of TSV are increased on-chip heat dissipation and density as well as threshold voltage shifts on transistors. The heat and power consumption problem might be alleviated by running at low clock frequencies [30]. RC time constant of the dense TSV interconnection will be dominated by high resistance due to thin cores or wires and via to via or wire to wire capacitance and inductance. TSVs are modeled into lumped electrical lines [28, 29] and estimated resistance and capacitance is agreeing with detailed simulation [31]. Due to the bandwidth limitation, TSV pitch is expected to be 16μm and pin density of TSVs is $\sim 4 \times 10^3/mm^2$ in 2011-2014 time frames [14]. Each pin is capable of supporting data rates up to 3 Gb/s [27]. Intel Nehalem and AMD Phenom Quad-core processors are shown in Figure 8 and 731 and 463 million of transistors arranged into a 263 and 283 mm$^2$ die area, respectively [32]. TSVs will most likely cover only 1-5% of the microprocessor chip [29]. Utilizing only 1% of the quad-core die area, cumulative off-chip bandwidth with these estimated numbers will be $\sim$ 32 Tb/s. For the same chip the cumulative off-chip bandwidth will be ~0.7 Tb/s with microbump array.
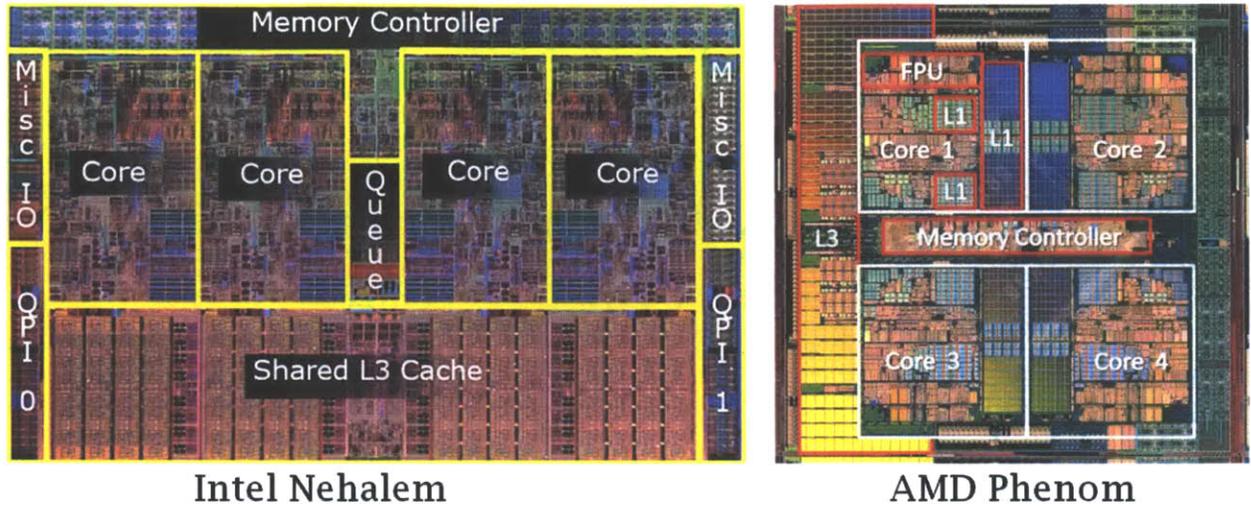
Figure 8. Intel Nehalem quad-core die (left) and AMD Phenom quad-core die (right) (images are not to scale)

On-chip to off-chip bandwidth is handled using low voltage signaling (LVS) which refers to wide range of differential signaling technologies with low voltage operation. Intel and AMD are using QuickPath Interface (QPI) and HyperTransport Interface (HPI) architecture, respectively. Intel's QPI improved the uni-directional front side bus and provides high speed, packetized, point to point links with differential signaling since 2008 [35]. This allowed high bandwidth up to 204.8 Gb/s and low latency utilizing 84 pins (data rates up to 2.5 Gb/s per pin). Although QPI or HPI is not designed for memory interconnects, it is the state of the art technology to estimate the current on-chip to off-chip electrical signaling capacity. Recently, a 1cm CMOS link with 356 and 463 fJ/link at 4 and 5.2 Gb/s has been demonstrated, respectively [36]. This Link is provided with 90nm process and integration to advanced CMOS process can double the bandwidth of QPI. Additionally, ball grid pitch scaling down to 35 μm will enable off-chip bandwidth of ~3.2 Tb/s.

For off-chip communications, the commodity computers and data centers, supercomputers have established different standards. The focus will be first in commodity interconnect technologies and later the rise of photonics in the supercomputers, data centers and long distance communications will be addressed. The coaxial cable, patented by O. Heaviside in 1880 [13], is revolutionary for electrical interconnects. It is really started to be widely used for transmission of many telephone carriers with a

16

single cable since 1930. Characteristic impedance of a coaxial line depends on the dielectric constant filling and the ratio of the inner and outer diameter.

$$Z_0 = \frac{1}{2\pi} \sqrt{\frac{\mu_R \mu_0}{\varepsilon_R \varepsilon_0}} \ln \frac{R_{in}}{R_{out}} \approx \frac{138\Omega}{\sqrt{\varepsilon_R}} \log_{10} \frac{R_{in}}{R_{out}}$$

Where, $Z_0$ is the characteristic impedance, $\mu_R$ is the relative magnetic permeability, $\mu_0$ is the vacuum magnetic permeability, $\varepsilon_R$ is the relative electric permittivity, $\varepsilon_0$ is the vacuum electric permittivity, $R_{out}$ is the outer radius of the coaxial cable and $R_{in}$ is the inner radius of the coaxial cable. Typical maximum power handling and attenuation is shown in Figure 9 [14]. Maximum power handling occurs for characteristic impedance of ~30Ω. Characteristic impedance of 52Ω is chosen as a compromise between minimum attenuation and maximum power by US Navy in World War 2. It is rounded to 50Ω later and widely accepted. Television broadcasts are matched to 75Ω to minimize attenuation through air.
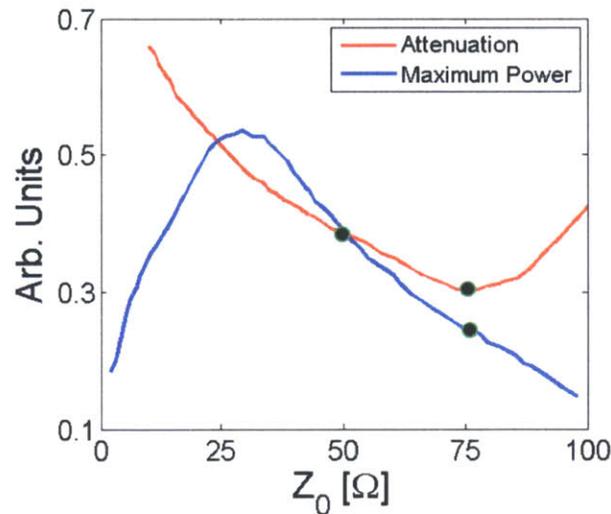


Figure 9. Maximum power and attenuation of a typical coaxial cable.

Widely used characteristic impedances are shown with black dots.

SubMiniature A, B, C and K (SMA, SMB, SMC and SMK) are widely used coaxial radio frequency (RF) connectors and cables from DC to 17, 4, 10 and 45 GHz bandwidth range, respectively (Fig. 10). At high frequencies even optimized rigid, semi-rigid or flexible coaxial cables tend to have high loss.

Figure 10. RF coaxial cable standards; SMA, SMB, SMC, SMK.

It is important to understand where the losses are originated at this point. For minimizing the propagation losses, the coaxial cable has to be designed as large as possible to minimize mode overlap with lossy media. However, if we consider high bandwidth cables on the market, the diameter of the cable is shrank from 3.5mm to 2.9mm, 2.4mm and down to 1mm as the bandwidth increases. The main reason for this decrease is that the coaxial cables support the fundamental transverse electric mode (TEM) as well as higher order modes if the cut off frequency is lower than the excitation frequency. Each perturbation on the cable including bend, twist or imperfections induced the coupling to the higher order modes which travel at different speed and lowers the voltage standing wave ratio (VSWR). Therefore, cables shrank down to 1mm diameter to support single mode at high frequencies. The cut off frequency of the RF coaxial cable can be modeled accurately using the finite difference modesolver. An approximation can be made to the cut off frequency using metallic boundary conditions;

$$f_c = \frac{c}{\pi \sqrt{\mu_R \varepsilon_R} \left( R_{out} + R_{in} \right)}$$

Where, $f_c$ is the cut off frequency, $c$ is the speed of light. Cut off frequency approximation is compared with commercially available cables in Figure 11.
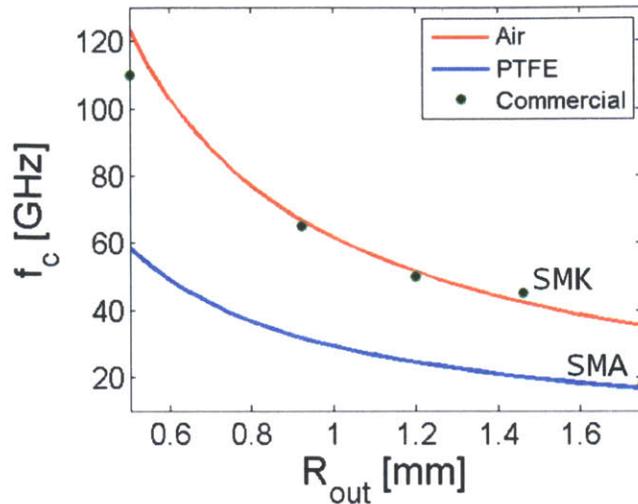
Figure 11. Comparison of the cut off frequency of commercially available cables and approximation

For local or short distance off-chip communications, PC interface standards; Universal Serial Bus (USB), Digital Visual Interface (DVI), High Definition Multimedia Interface (HDMI), Apple/Intel Thunderbolt and Displayport have been introduced (Fig. 12). There are mostly based on microstrip and stripline RF cables. Off-chip short distance communication bandwidth, shown in Figure 13, increased



| USB | DVI | HDMI | THUNDERBOLT | DISPLAYPORT |

Figure 12. High speed recent PC interface standards

from 12 Mb/s (1995) to ~18 Gb/s (2010). It is likely to have PC interfaces at 100 Gb/s or more in 2015 and 1 Tb/s or more in 2020. Display resolution standards; High Definition (HD) (1366x768), HD+ (1600x900), FullHD (1920x1080), WQXGA (2560x1600), QFHD (3480x2160), 4K×2K (4096x2160) will need high bandwidth interfaces in the near future. Video data rate can be calculated as follows;

*Video Data Rate = refresh rate × # of pixels × bits per pixel*

24 and 36 bits per pixel (bpp) is considered as low and high end color depth, respectively. Standard refresh rates are 60, 120 Hz. HDMI 1.4a cable supports 120Hz and 24bpp FullHD signal. However, Displayport 1.2 can support 4K×2K video at 60Hz and 30bpp. A 4K×2K video at 120Hz and 36bpp will

19

require 40 Gb/s interface. For a 3D display capability, two separate high quality images will be received by the user/s which doubles the bandwidth of transmission. This type of a 3D display technology does not provide motion parallax. In other words, user is observing the same 3D video independent of position with respect to screen which is different than real perception. Holographic displays or dynamic 3D
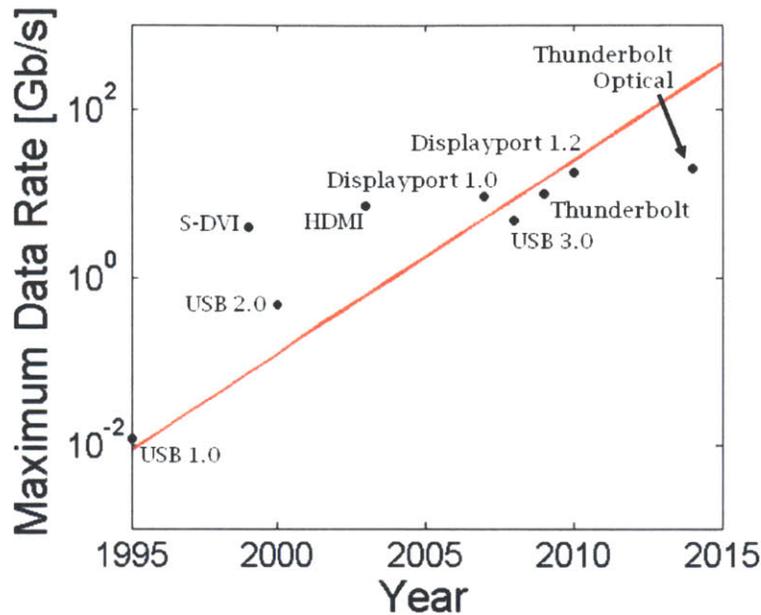


Figure 13. Short distance off-chip bandwidth scaling

content designed for each user can achieve 3D display with motion parallax. Such a display technology will require much more bandwidth than what have been discussed previously.

The most commonly used off-chip interface, Ethernet, for computer networking technology for local area networks (LANs) has introduced in 1980 with coaxial cables. Electrical cables induced high loss for off-chip long distance communications and the data needs to be amplified, filtered, received, and transmitted again using repeaters. The cables are replaced later with low loss twisted pair cables and fiber optic links. The Ethernet bandwidth is increased even at a rate faster than Moore's law (Fig. 14). It is expected to reach 1 Tb/s in 2015 by core network and 0.4 Tb/s in 2020 by server network.

20
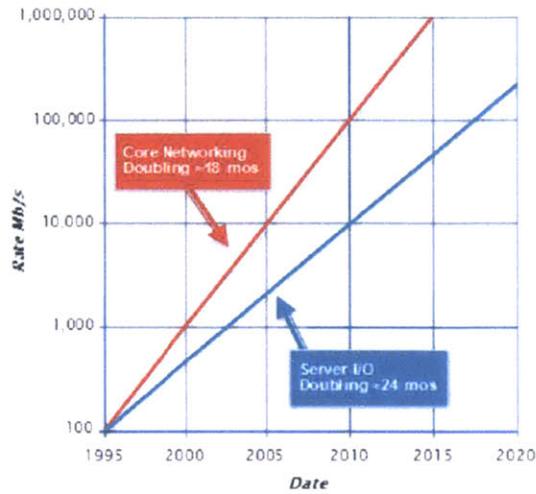
Figure 14. Ethernet bandwidth scaling according to IEEE 802.3 Ethernet Working Group Communication

## 1.2 Optical on-/off-chip communications

Since we summarized the on-/off-chip communications above, it is important to discuss where the optical interconnects (especially silicon photonics interconnects) are being used and will be used in the near future. Data centers or high performance computing machines (HPCs) are already utilizing the vertical cavity surface emitting lasers (VCSEL) as the optical interconnect since 2004 (Blue Gene L [10]). VCSELs handle communication between server cabinets in HPCs and gradually support communication between blades, boards and chips. VCSELs currently carry single channel per fiber similar to an electrical interconnect that carries single channel per wire. Recently, a 980nm VCSEL at 35 Gb/s data rate is demonstrated with as low as 268 fJ/bit [40]. At lower data rates, the 980nm VCSEL can achieve lower energy per bit. A 1060 nm VCEL at 10 Gb/s is also demonstrated with only 140 fJ/bit [41]. The 1060nm VCSEL showed reliable performance and the output power dimmed less than 10% of its original over 5000 hours of operation under thermal and humidity stress.

Today's top two fastest supercomputer, Sequoia (Blue Gene/Q) and the K have 1.572 million and 700 thousand cores and works at a peak performance of ~10 and ~16 PFLOPs, respectively. In order to achieve a EFLOPs machine with VCSELs we can start from the single chip with TSVs and we can determine the number of VCSELs and fibers for this system. We estimated the cumulative off-chip bandwidth of a single chip will be ~ 32 Tb/s or 20 TFLOPs above with TSVs. We can expect the VCSEL

21

technology will be advanced to 50 Gb/s in the same time frame. Even at this bandwidth, 640 VCSELs are needed to integrate on a single chip with 20 TFLOPs. Currently, IBM Blue Waters is using 40 VCSELs per 4 chip hub. Achieving 640 VCSELs on a chip is far beyond the current technology since VCSEL integration with CMOS on the optical chip has not been demonstrated. This also requires multiplexing and demultiplexing of many TSVs to achieve 50 Gb/s per VCSEL which increases the power consumption and complexity of the transmit and receive circuitry. If the 3D integration will be realized, VCSEL will limit the CMOS design since it is based on vertical cavity and can only integrated on top of the chip.

Even if the 20 TFLOPs on a single microprocessor is realized with 640 VCSELs, we will need 50,000 microprocessors for a super computer running at EFLOPs. With 640 optical fiber per chip at 50 Gb/s per fiber, we will need 32 million fibers and VCSELs in an EFLOPs machine. Although VCSEL was the current choice for optical interconnect, the scalability to exascale computing in dense 3D integration is technologically challenging and not cost effective. Therefore, wavelength division multiplexed (WDM) systems with large scalability and bandwidth will take place in off-chip communications. It is also addressed by International Technology Roadmap for Semiconductors (ITRS) in 2011 [14].

The WDM system proposed in this thesis will be silicon photonics. A silicon photonic WDM system that operates in C band (1530 - 1565nm) with a single channel carrying 50 Gb/s and 100 GHz channel spacing will provide 38 wavelength multiplexed channels and will be transmitted with a single mode fiber. This reduces the number of fibers 38 times compared to VCSELs. If the signal needs to be amplified, C and L band Erbium Doped Fiber Amplifier (EDFA) is available and widely used. Therefore, L band (1565 – 1625nm) can also be covered with additional WDM channels and double the number of channels to 75. All 75 channels can be still transmitted through a SM fiber. For a EFLOPs machine, the required number of fibers is 426 thousand with WDM system compared to 32 million fibers with VCSELs. The integration can be achieved on the same substrate utilizing monolithic integration with CMOS or on a 3D chip with flip chip bonding of CMOS and photonic chips.

Although integration of Silicon photonics with CMOS is encouraging and enabling technology, it is a major change for the process design kits. Based on ITRS roadmap [14], on-chip electronics have already determined ways to leverage the bandwidth and energy requirements until 2020. Simply, on-chip wire capacitance can be minimized with lower dielectric constant oxides. Process design kits are expensive to develop. Only minor changes are allowed to minimize the cost. Silicon photonics integration with current CMOS standards is a major change than lowering dielectric constant of conventional oxides. Moreover, ways to achieve Low-k dielectrics have been understood and demonstrated (Fig. 15). Dielectric constant <2.0 oxides becomes mechanically unstable and damaged from plasma etching. It is foreseen that dielectric constant will achieve around 2.15 in 2018. After 2018, a major change is expected in process design kit which can enable Air-Gap [15-17] or another technology such as on-chip silicon photonics. However, ITRS roadmap claimed the backend optically low loss materials such as Poly-Si that requires high temperatures [37] or SiN which is not a semiconductor or active material [38]. However, this is not completely true. Monolithic integration is realizable by tweaking the parameters of CMOS and photonic process. A monolithic integration of a microdisk modulator up to 2 Gb/s has demonstrated at Sandia National Laboratories [42]. Monolithic integrated 2nd order 4 channel thermally tunable microring filter bank has been demonstrated at MIT [43].
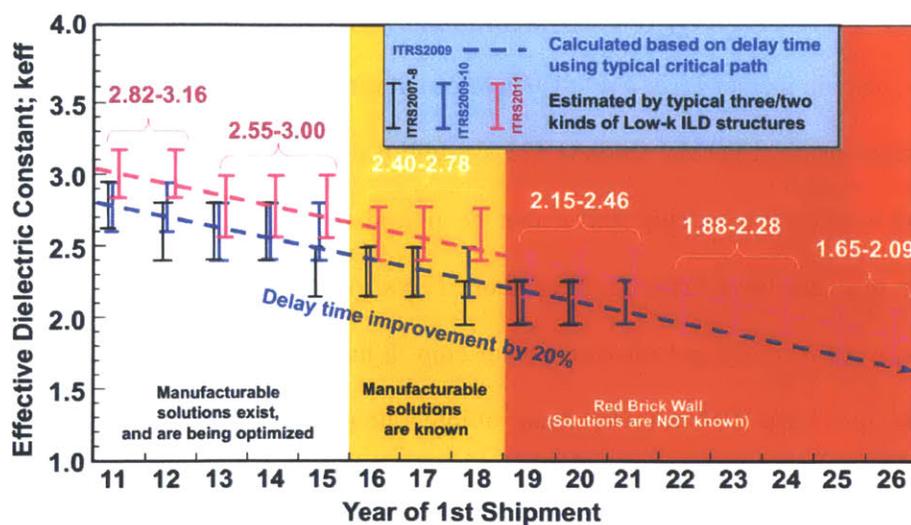


Figure 15. Low-k dielectric progression from ITRS roadmap. It is possible to achieve Low-k dielectrics until 2018.

Local memory communication, governed by electronics, is the next to discuss. Dynamic random access memory (DRAM) is currently limited by the bus between the memory and chip. Micron identifies this as the "memory wall" problem. 3D System-on-Chip (3D-SOC) that uses multiple stacked dies, 3D Wafer-Level-Packaging (3D-WLP) that is established by flip-chip bonding, and 3D-Stacked-Integrated-Circuit (3D-SIC) that utilizes direct interconnects between circuit blocks in different layers, are interconnect technologies that involve TSVs in ITRS roadmap. Chip to memory 3D integration (Hybrid Memory Cube), can be achieved vertically integrated by TSV technology instead of side by side or off-chip [18-21]. Conceptual drawing of Hybrid Memory Cube is shown in Figure 16.
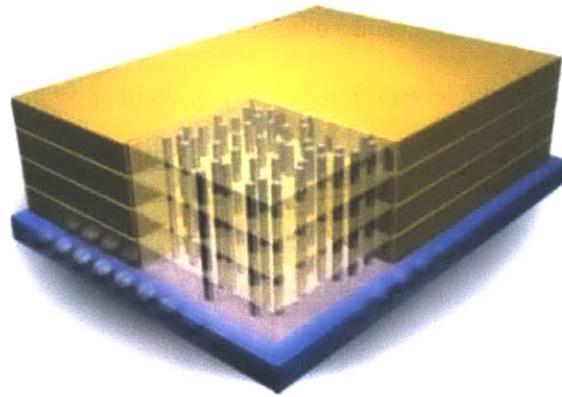


Figure 16. Hybrid Memory Cube proposed by Micron. Package, Logic and DRAM level is shown with pink, purple and gold colors, respectively. TSVs are shown in between DRAM and logic level.

On-chip cache is also occupying half of the chip size in order to save bandwidth of writing and reading from an off-chip memory (see Fig. 8). Therefore, it can leverage the access to DRAM and makes the current on-chip cache (SRAM) obsolete [25]. Additionally, the 3D memory cube will double the computation space since the on-chip cache can be placed on top of the microprocessor instead of occupying same physical layer. This requires short TSVs to be enabled on chip as well as accurate alignment between the memory and microprocessor chip. It has been demonstrated repeatable alignment tolerances within 3μm [26]. IBM has a roadmap to integrate photonics next to electronics for 2015 and includes vertical memory cube for 2020 [24]. Conceptual drawing of these integrations is shown in Figure 17. A recent study compared monolithically integrated 41 stage ring oscillators and identical ring

oscillators bounded between chips using TSVs. Results are surprising since there was no degradation in speed or increase in power consumption on the integrated chip with TSV connections. Moreover, data rates up to 3Gb/s per pin are already demonstrated using TSVs in 2008 [27]. However, these key developments still might not allow silicon photonics to take place in local memory communication for some time. Off-chip communications will stay optical (VCSELs) for HPCs and commodity PC interface standards with optical power supply and data transmission will likely to emerge.



2015 Roadmap    2020 Roadmap
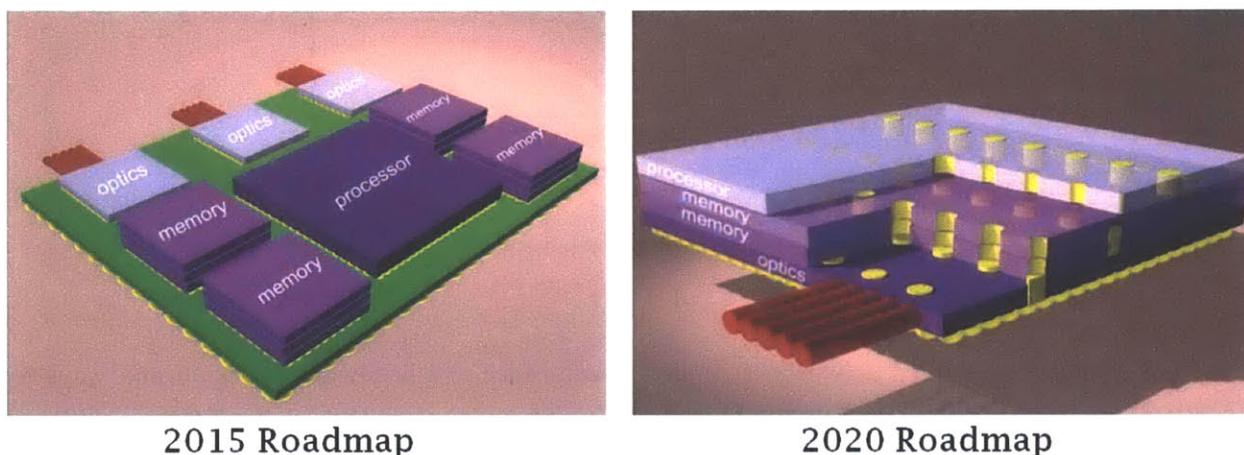
Figure 17. IBM 2015 and 2020 roadmap for photonics integration

## 1.3 Data Storage Scaling

High bandwidth off-chip communications such as Ethernet, computing and displays will require the data storage capacity to scale in parallel. Hard drive capacity, shown in Figure 18, scaled from 1 Gb (1995) to 4 Tb (2012) and it is even increasing at a rate higher than Moore's Law. The capacity scaling is referred as Kryder's Law [34]. It is predicted that a two-platter hard drive capacity will be 14 Tb on a 2.5" disk drive and cost ~40$ in 2020. However, speed of reading and writing the data is ~ 160 Mb/s for the state of the art hard disk drive with electromagnetic storage [45]. On the other hand, solid state drives are using flash access memory which is considerably faster up to ~ 390 Mb/s and 8 times more expensive per byte than the electromagnetic counterpart [46]. We can easily predict that data storage will be handled with a method different than photonics and it has other solutions for future [34].
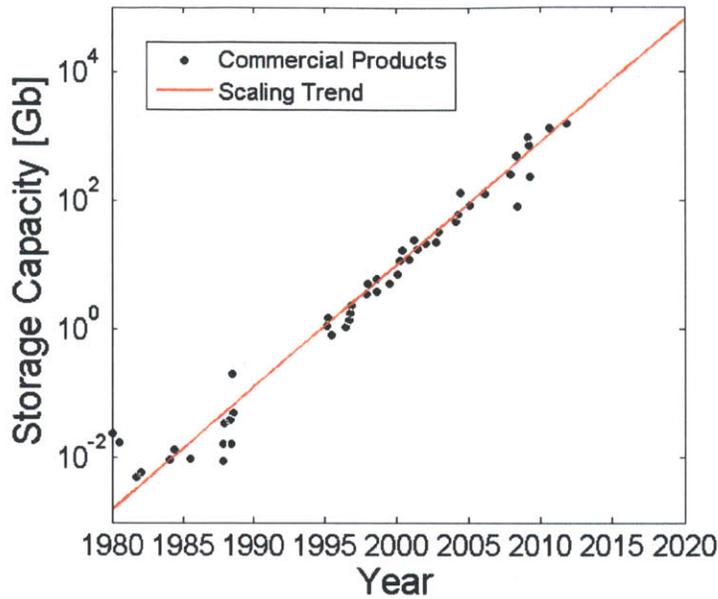
Figure 18. Storage capacity scaling

## 1.4 Energy per bit scaling on a chip

We have concentrated above on computer performance and bandwidth roadmap and ways to achieve those targets. Power handling on a microprocessor is also important because power density will increase in parallel with computing performance. Most chip architectures are limited to 1 $W/mm^2$. So, for a quad core chip with a die area of ~270 $mm^2$ (estimated based on Nehalem and Phenom chips) could handle maximum power consumption of 270 W and 20% of this power will be devoted to off-chip communications [44]. If the transmit and receive power is assumed to be equal, the maximum transmit or receive power will be 27 W. We can calculate the maximum bits per chip from the FLOPs per chip (Figure 3) by using 6 bits/FLOPs. 6 bits can be decomposed into 2 and 4 bits for off-chip and memory communication. Energy per bit, shown in Figure 19, is calculated by dividing the maximum transmit or receive power to number of bits. Top Supercomputers will reach the 100, 10 and 1 fJ/bit limit by 2020, 2025 and 2030, respectively. On the other hand, commodity computers will reach 100, 10 fJ/bit limit by 2025, 2030, respectively. This constraint is fundamental and derived basically the density of components in the chip area for high bandwidth operation. Transmit or receive energy per bit for 100 fJ/bit has not been demonstrated using VCSEL. However, silicon photonic resonant modulators with as low as 3 fJ/bit

26
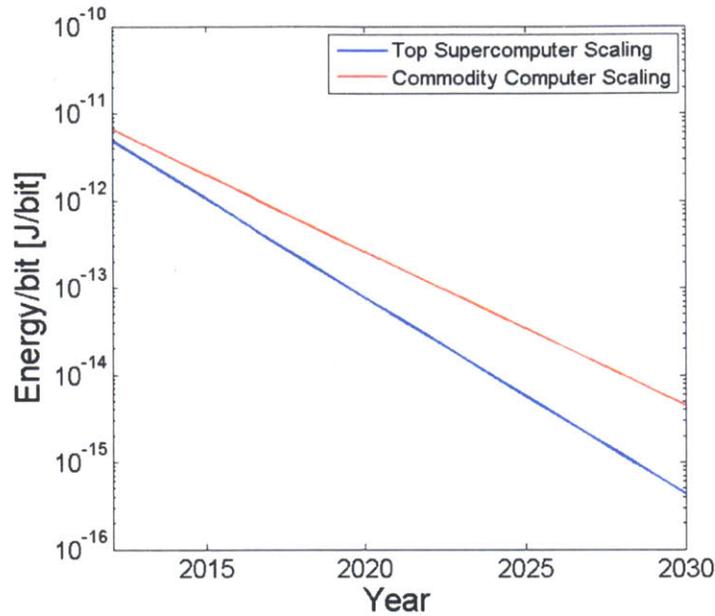
Figure 19. Energy per bit scaling

at 10 Gb/s and 13fJ/bit at 25Gb/s has been demonstrated [47,48]. This is only including an electro-optic modulator energy performance. With integrated circuitry and laser source, cumulative energy per bit will raise to ~100 fJ/bit. However, the resonant microdisk needs to be aligned in wavelength to an external or on-chip laser line. This is not necessarily true due to process/wafer variations and dynamic temperature fluctuations and this thesis is devoted to offer solutions and understand the reasons for this mismatch.

## 1.5 Silicon Photonics

Although photonics is commonly recognized by researchers, there are few commercially available devices utilizing the benefits of it. It may be partially due to challenging and sophisticated photonic system design requirements or challenges in integration of the photonics with electronics on the same platform. Silicon photonics is the effort of utilizing CMOS processes and CMOS compatible materials to form photonic components on the same platform. Silicon is an ideal platform for photonics since it is optically transparent or low loss above 1.1 μm and has a high refractive index around 3.48, allowing highly confined waveguides and tight bends (radius of curvature <1.75μm) as opposed to sophisticated fibers that allow bends in the order of millimeters.

Although older CMOS nodes match well with silicon photonic thickness requirements (~100-250nm), the current nodes are too thin for supporting highly confined optical modes. In order to increase the confinement factor central wavelength is shifted from 1550 to 1280nm for monolithic integration of electronics and photonics [43], which necessitates new design of each element on-chip and expensive amplifiers. It also requires the integration of Poly-Si or Amorphous-Si waveguides and extensive control of the process to lower the losses based on edge roughness and multi grain structure instead of C-si. A customized CMOS process have been demonstrated Photonics chip fabricated with an older node CMOS and state of the art electronics chip can be 3D integrated utilizing TSVs. Through my MIT studies, I was lucky to experience both monolithic integration at 1280nm with IBM and Micron processes and flip-chip bonding at 1550nm with CNSE Albany process. High performance devices can be achieved by bonding III-V materials on silicon layer. However, yield lowers significantly due to voids in the integration process.

WDM based silicon photonics with microdisk/ring resonators will be the main focus of this thesis. Silicon Mach-Zender modulators are not going to be discussed in this thesis but the transfer matrix of a Mach-Zender will resemble the solution in chapter 3. The most simple single channel point to point silicon photonic link is composed of a CW laser source, a resonant modulator, modulator driver and a detector and receiver circuit. For a multi channel WDM link, a single photonic bus waveguide can guide all channels and all external and/or on-chip laser sources need to be multiplexed to a single fiber or a waveguide. A multiplexer with microring filters is illustrated in Fig. 20. Each channel will require a CW laser source, a resonant modulator and a detector as well as a resonant filter prior to detection (Fig. 21, a).

Our team at MIT has measured the intrinsic loss of C-Si as low as 2.7dB/m and the ridge waveguide design is allowing a microring resonator with a quality factor of $2.2 \times 10^7$ [49]. Therefore, the on-chip transmission can be short enough that the signal will not require amplification. However, if the amplification is required, erbium doped gain medium or waveguide amplifier (EDWA) can be integrated on-chip [50] (Fig. 21, b). For off-chip communication, the amplification can be achieved by external erbium doped fiber amplifier (EDFA) for C and L bands (Fig. 21, c).

For receiving the signal, clock frequency and phase has to be determined. On-chip transmitter and receiver can share an additional electrical clock wire to receive data properly (Fig. 21, a-b). However, when the transmission is received data, clock has to be recovered with a clock recovery circuitry (Fig. 21, c) [51]. Electrical clock recovery will dissipate additional power and occupy additional chip area. However, it is a widely used control layer of an electrical link. In a WDM link, clock recovery can be eliminated by transmitting and receiving clock using an optical channel, as illustrated in Fig. 21, d.
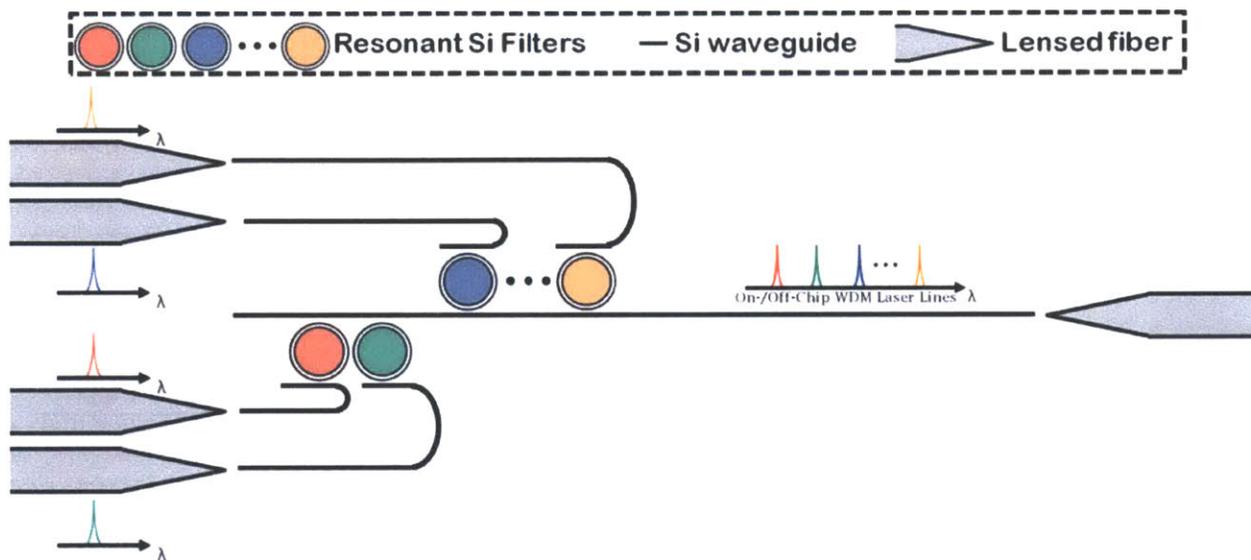


Figure 20. on-chip WDM multiplexer of laser sources, color coding is used to indicate the resonance of the filters. Each resonator resonance corresponds to the color coded laser lines.
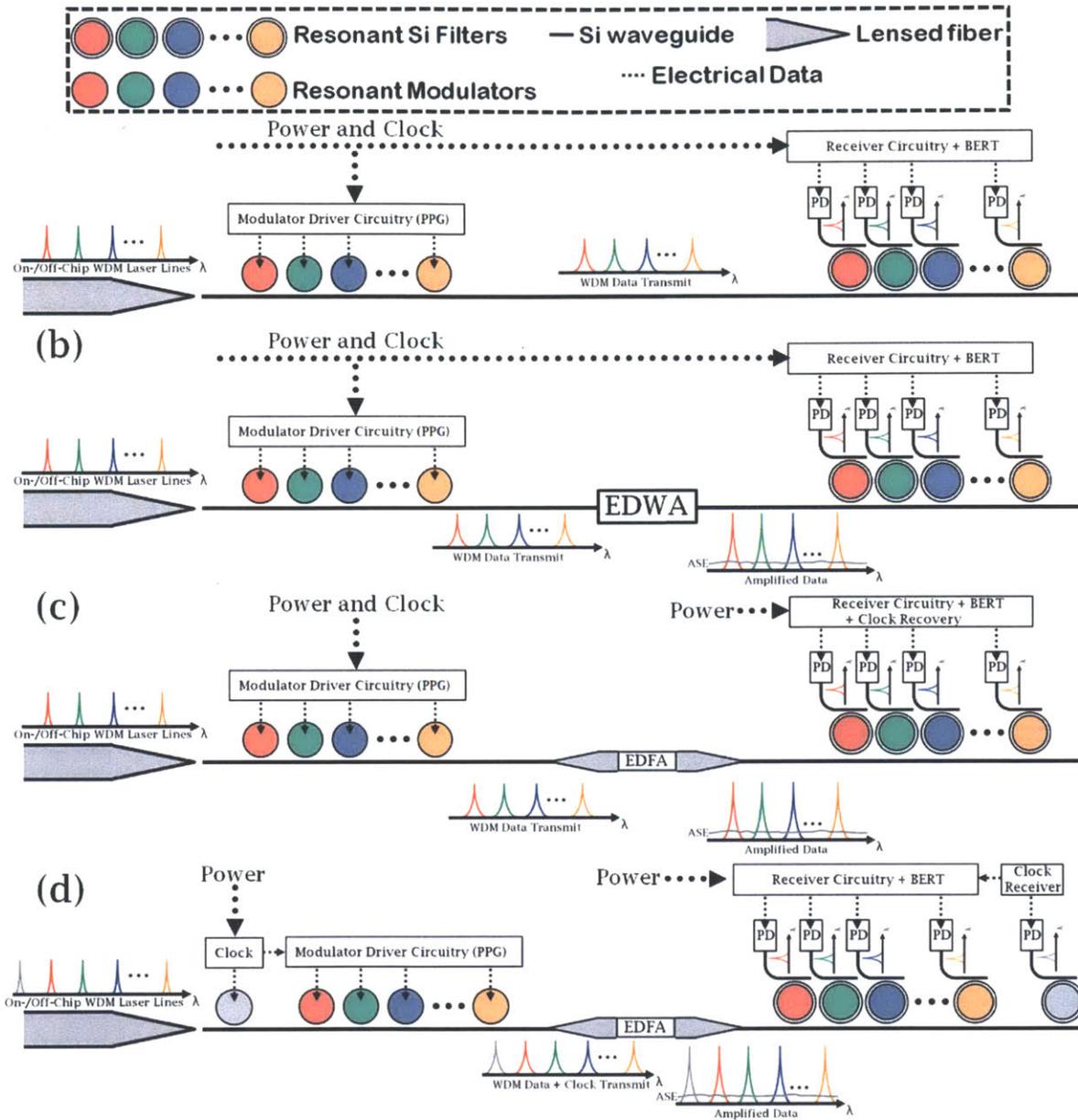
Figure 21. on-chip WDM link with no amplification (a) and integrated waveguide amplifier (b), off-chip WDM link with amplification between transmitter and receiver chips (c), off-chip WDM link with optical clock transmitter and receiver (d). Color coding is used to indicate the resonance of filters and modulators. Each resonator resonance corresponds to the color coded laser lines.

We have introduced a WDM link, which is composed of an optical multiplexer, a transmitter and a receiver (Fig. 20-21) which includes multiple silicon resonant filters and modulators. In such a WDM link, laser sources are required to be aligned in wavelength to the resonances of silicon resonant filters and modulators in the multiplexer and transmitter, respectively and transmitted data on each channel is

also assumed to be aligned with resonance of the filters in the receiver. The alignment is distorted by process and wafer imperfections and dynamic temperature fluctuations due to processor core activity which will be explained in detail in the following section.

## 1.6 Wafer Level and Process Variations

High confinement waveguides, which is enabled by high index contrast of Si, can be formed into compact (~3.5μm diameter) micro-ring/-disk resonators at the expense of susceptibility to the fabrication imperfections or wafer thickness variations. Fundamental TE and TM resonances of a micro-disk resonator experience frequency offsets to only thickness and diameter variations. The width and diameter imperfections can be extracted from the response of the two orthogonal polarizations [52]. Using a cylindrical modesolver, the microdisks with different diameters are designed around 1550nm in wavelength. Frequency offset due to thickness and diameter dependence is determined to be 140, 52 GHz/nm for fundamental TE radial mode, and 330 GHz/nm, 36 GHz/nm for fundamental TM radial mode, respectively. Microdisks at different location on a wafer have been fabricated on a thick SOI, respectively. A resonance frequency shift of ±400 GHz has been observed in a 6cm radius around the wafer center Fig. 22. A 4 channel second-order silicon microring filter bank have been demonstrated on a customized CMOS run with a post-fabrication undercut process (Fig. 23,a) [43]. Drop ports and thru port of the second-order microring filters have been measured at different positions on wafer to determine frequency mismatch between two resonators (Fig. 23,b-c). A frequency mismatch of ±45 GHz is achieved, which implies a tight process control compared to thick SOI process can be realized on a customized CMOS run. Therefore, a ±50 GHz frequency offset has to be compensated.
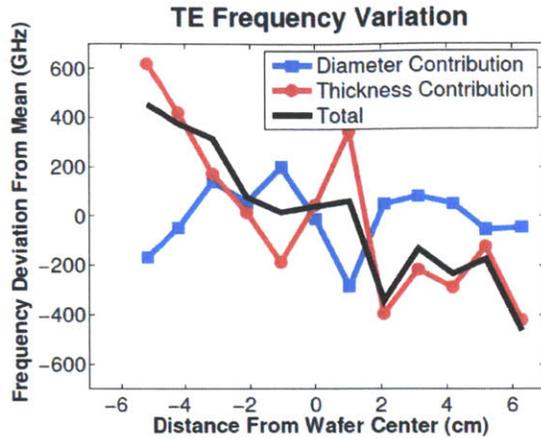
Figure 22. Fundamental TE resonance frequency deviation with respect to the distance from wafer center [52].
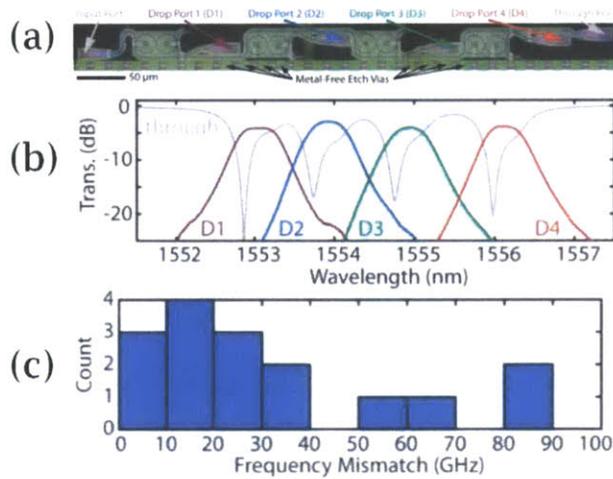


Figure 23. (a) Optical micrograph of a four-channel second-order filter bank, (b) Measured transmission normalized to off-resonance through port transmission for the four-channel second-order filter bank without thermal tuning or post-fabrication trimming, (c) histogram of resonant frequency mismatch between the two rings in the second-order filters from four die from different wafer locations [43].

## 1.7 Thermal Fluctuations

Silicon is a thermally and electrically active material. Electrical conductivity of Si can be controlled precisely with implantation and activation of $p$-/$n$-type doping species. This has been utilized to create transistors family and active photonic structures. On the other hand, thermal conductivity of Si is weakly dependent on doping concentration and can only be controlled by sophisticated rough nanostructures that engineer phonon scattering [53-57]. Although some of the offered solutions to control thermal conductance are CMOS compatible, they require complex processing and there is no silicon

32

resonator with specially engineered thermal conductance. Therefore, the Si waveguides and resonators are not thermally insulated and Si has a high thermo-optic coefficient that corresponds to ~10GHz/$^0$C resonance shifts [91]. It becomes a major problem in a processor core with dynamic temperature variations, as illustrated in Fig. 24 [58]. Furthermore, a 3D-integrated or a monolithically integrated photonic chip can have a dynamic temperature variation of $\pm 10^0$C, that corresponds to a $\pm 100$GHz frequency mismatch.
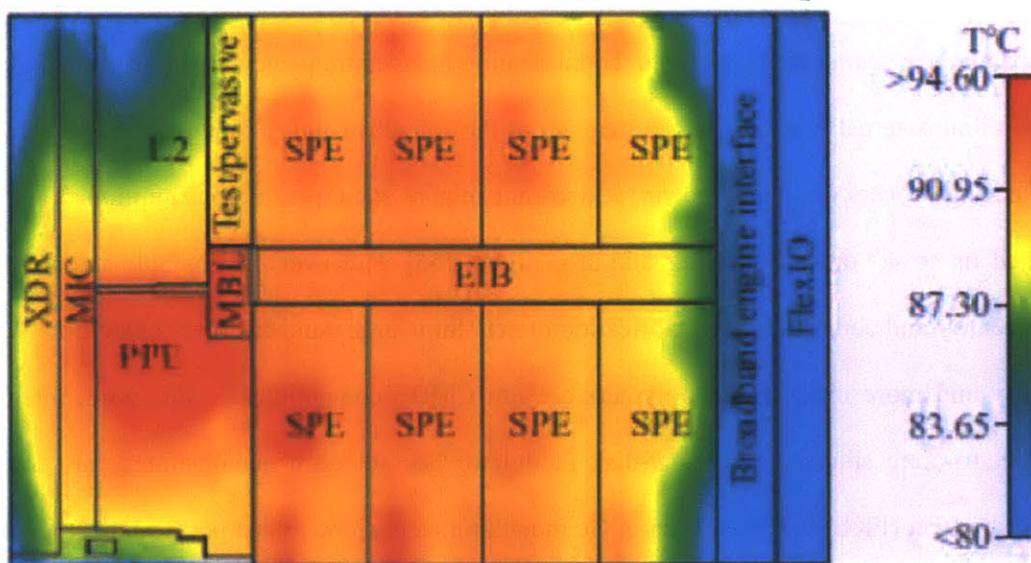


Figure 24. IBM microprocessor thermal map, showing a temperature variation of ~$\pm 7.3^0$C [58].

## 1.8 Available Solutions

In section 1.6 and 1.7, we have summarized the main factors that induce frequency mismatch. From these sections, we can predict that a total frequency mismatch of $\pm 150$GHz has to be compensated, including fabrication imperfections and dynamic temperature fluctuations. In this section, we will explain available solutions to resolve this problem. The passive methods include athermal, high-order box and SiN filters and active methods include electro-optic or thermo-optic tuning.

Athermal waveguides is formed with Si waveguides buried or covered with a polymer that has a negative thermo-optic coefficient [59-65]. Width of the Si waveguide can be scaled down to lower confinement factor and fundamental waveguide mode will overlap with the polymer to compensate the

33

thermo-optic coefficient. Additionally, the low confinement of silicon waveguide limits the radius of the current athermal microrings is >10µm. The confinement can be maximized with a large negative thermo-optic coefficient polymer, thus minimize bend radii. Compact devices lead to large free spectral range that allows large number of WDM channels and minimize the electrical power consumption of active devices. Therefore, the performance of athermal devices is limited to material engineering. We have explained how the athermal waveguides can be a solution for on-chip temperature fluctuations. However, the fabrication imperfections need post-trimming of the athermal resonators. The refractive index can be tuned by curing the polymer to compensate the fabrication induced frequency mismatch. The polymer can be cured with an external laser source and can store the refractive index change up to couple months. Although, curing process dissipates power, it does not require static power consumption. This has been demonstrated up to $4^{rd}$ order microring add-drop filters [65]. However, no scalable method has been offered to identify and compensate the fabrication offsets for a large number of resonators in a WDM link automatically and more importantly, polymers are not CMOS compatible. Furthermore, integration of athermal electro-optic silicon micro-ring/-disk modulator has not been demonstrated into this system. Franz-keldysh effect (FKE) has been used in Ge modulators that show robust performance in a thermally volatile environment [66]. However, FKE occurs at a small range of frequencies and limits the WDM capacity of the silicon photonic system.

Another passive solution will be using CMOS compatible thick SOI process to form high order microring filters. First order microring response has a lorentzian shape that distorts the signal significantly if there is a frequency mismatch between microring resonance and the data carrier center wavelength. High order microring exhibits a flat-top or box filter response with sharp cut-off, that allows the multiple WDM channels. A high order microring filter with a >300GHz 1-dB bandwidth will require no compensation with ±150GHz frequency drift [67]. The drawback is the electro-optic resonant silicon modulators are single micro-ring/-disk based devices. Therefore, modulators will require active control.

SiN can be used a material platform since the thermo-optic coefficient much smaller than Si and high order SiN has been demonstrated on thick SOI [68,69]. However, SiN is not likely to be a complete

solution due to three reasons. First, SiN is a low-index (~2) contrast material, thus increases size of the structures. The SiN thickness needs to be ~400nm to minimize substrate leakage on a SOI wafer, which requires tight process control to achieve low side-wall roughness. Second, the thickness of the Si is being decreased and density of transistors increased with the next generation of processor node. Therefore, even SiN microrings are fabricated with an older node; the pitch of the electrical wires will limit the performance of the hybrid photonic-electronic chip. Third, SiN is not electrically active (insulating) and fabrication imperfections need to be fixed with external control, which becomes a power hungry solution.

If any of the solutions offered above can be realized in a large-scale integration platform, it will definitely have an impact on the research and commercialization of Silicon photonic products. However, we should focus on a more general solution without limitations of passive methods. Active compensation methods; electro-optic and thermo-optic tuning have been optimized and energy per bit performance is dwarfed significantly in the last decade [71-74]. Active compensation methods will be explained in the following two sections.

## 1.9 Electro-optic tuning/modulation

This section will focus on PN junction resonant switches and modulators since the PN junction based devices have few demonstrations of electro-optic tuning [75]. The speed of the tuning will be limited by the bandwidth of electro-optic tuners, thus a faster device can be utilized for a reconfigurable network. Injection or depletion of the carriers from a PN diode formed inside a resonator exhibits the plasma-dispersion effect [70], which in turn changes the refractive index of the silicon waveguide. The electro-optic refractive index change alters the resonance frequency of the resonator. Using this principle, many variations of compact silicon modulators are formed and the first resonant modulator was an injection-based device [71].

Depletion based devices improve on this early injection-based device, enabling efficient high-speed operation of silicon microring and microdisk modulators. Recent work has yielded depletion-based modulators leveraging lateral-junction configurations capable of operating beyond 25 [76–78], and even 40 Gb/s [79-81]. Methods to interleave PN junctions have been utilized to increase the electro-optic

efficiency by enhancing the carrier-light overlap, which reduces the voltage-length product $V_\pi L_\pi$, achieving 25-Gb/s operation of a 30-μm-radius device with 4.5-dB extinction ratio at 2-V driving voltage [76], and 25-Gb/s operation of a 250-μm-circumference device with about 3.6-dB extinction ratio at 1.6-V driving voltage and 41-fJ/bit power consumption [77]. Another demonstration has achieved 25-Gb/s operation of a 7.5-μm-radius device with about 5-dB extinction ratio at 1-V driving voltage and about 7-fJ/bit power consumption [78]. By reducing the radius of the latter device to 5 μm, reducing the junction capacitance and the RC time constant, a similar device was demonstrated to operate at 40 (44) Gb/s, with 7- (2.3-) dB extinction ratios at 2-V driving voltages [79]. Leveraging PN-junction-interleaved cascaded microring resonators, 40-Gb/s operation was demonstrated with a 20-μm-radius device with 3.9-dB extinction ratio at 5-V driving voltage [80]. Lastly, a method to zigzag the PN junction has been employed to achieve 44-Gb/s operation with 3.01-dB extinction ratio at 3-V driving voltage [81]. Injection-based devices can be used as an electro-optic tuner, but the efficiency (~4.4μW/GHz [73]) will be quite low since it dissipates static power due to current.

Depletion-based devices leveraging vertical-junction configurations provide the added advantage to the drive voltage, power consumption, size, and speed [73]. The vertical junction maximizes the overlap of the depletion region with the radial TE mode, reducing the drive voltage and power consumption for modulation. It also enables direct electrical contacts to be made at the interior of the silicon microdisk or microring resonator, forming a hard outer wall that minimizes radiation, resulting in a significant size reduction of the device. This reduction in size also reduces the capacitance and increasing the speed. For example, depletion-based vertical-junction silicon microdisk modulators have enabled 12.5-Gb/s modulation of a 1.75-μm-radius device with 3.2-dB extinction ratio at 1-V driving voltage and 3-fJ/bit power consumption [73]. This device occupies less than one-tenth the area of traditional microring modulators, and maintains entirely-interior electrical contacts. Depletion based devices do not shift more than ~50GHz with CMOS compatible voltage range, thus it is not enough for an electro-optic tuner until today. However, if there will be a solution to the shift, depletion-based devices will have low static power, which is dominated by the leakage current.

However, one major limitation of microdisk resonators is that they support higher-order spatial modes that corrupt the free spectral range (FSR) by introducing undesired resonances. To combat this, several demonstrations have utilized adiabatic microring resonators, which leverage single-mode coupling regions and adiabatic tapering to enable contact regions and maintain single-mode operation [82–85]. These devices preserve most of the benefits of microdisk resonators, with the added advantage of enabling uncorrupted FSRs [82]. A single-mode adiabatic resonant microring (ARM) modulator has been demonstrated with comparable performance to the microdisk modulator [84,85].

## 1.10 Thermo-optic tuning

Refractive index of Si waveguides can be tuned by a heater. Optimized external heaters placed over the oxide cladding achieve 28-$\mu$W/GHz with a 6.4$\mu$s thermal time constant [72]. Recently, the heaters have been integrated within resonators which offer the best optimization of tuning efficiency and speed on thick SOI. One demonstration has directly integrated heaters within adiabatic microring resonators, achieving 4.4-$\mu$W/GHz tuning efficiency and 1-$\mu$s thermal tuning speed of a second-order filter [74]. The resonant modulators also require thermo-optic tuning to align with the WDM multiplexer and receiver. Unfortunately, heaters are usually integrated within resonant modulators at the expense of area and/or performance. A large ridge microring modulator (400$\mu$m$^2$) with ~42$\mu$W/GHz tuning efficiency and ~67% junction area coverage around the periphery [86] and a compact microdisk modulator (50$\mu$m$^2$) with 7$\mu$W/GHz tuning efficiency and 50% junction area coverage around the periphery [86] have been demonstrated in the literature. Junction area coverage limits the modulation efficiency and leads to an insertion loss of >5dB [5] and >3db [87]. For a normal distribution of ±10$^0$C temperature fluctuations and a ~100GHz resonance frequency offset due to fabrication/wafer variations, the total modulation and heater energy was >322fJ/bit [86] and >200fJ/bit [87]. Therefore, the total modulator efficiency is dominated by heater power.

## 1.11 Automated Wavelength Recovery Architecture

In section 1.5, we have shown the idealized WDM multiplexer, transmitter and receiver. Through section 1.6 to 1.10, we have stated the frequency mismatch due to fabrication/wafer imperfections and dynamic temperature fluctuations and between resonators and the on-/off-chip lasers. We also explained the available methods that can fix that frequency mismatch. Thermo-optic tuning is considered as the most realistic approach. We will offer a solution that we call as automated wavelength recovery (AWR), to fix a WDM silicon photonic link. This is a control layer that is required for a large scale WDM link that supports >1Tb/s bandwidth.

A realistic WDM link multiplexer before and after AWR is shown in Fig. 25, a-b. AWR loop is implemented to use the feedback from the integrated photodetector (PD) at thru port of each resonant filter and sending the control voltage to the integrated heaters. Minimizing the received signal at the detector will align the laser to the filter. The performance will be limited with the receiver sensitivity. The underlying algorithm and demonstration of such a loop will be explained in Chapter 3.
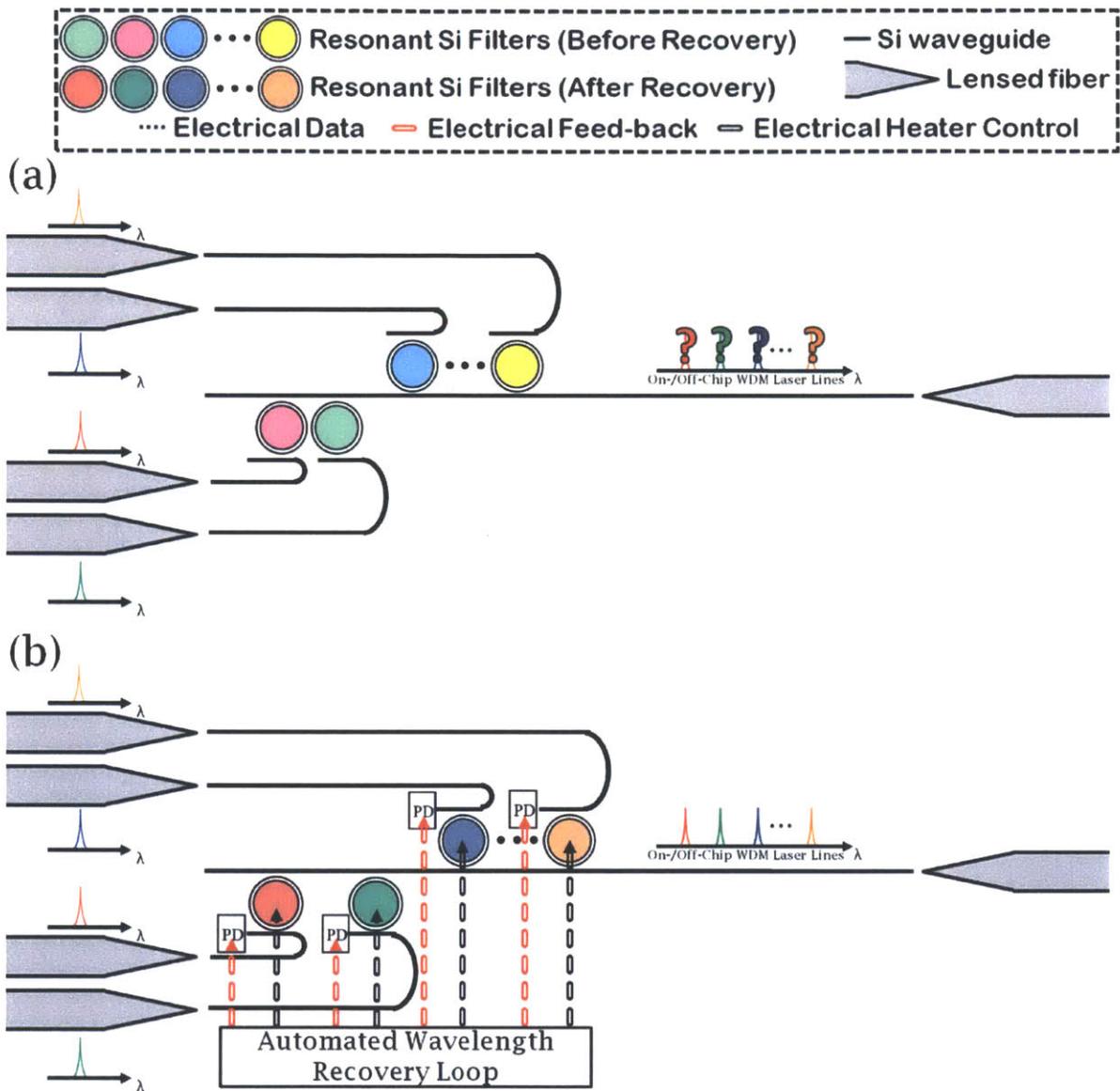
Figure 25. on-chip WDM multiplexer before(a) and after(b) wavelength recovery, color coding is used to indicate the resonance of the filters. Automated wavelength recovery loop is using the feedback from the integrated detector at thru port of each resonant filter and sending the control voltage to the integrated heaters. Each resonator resonance corresponds to the color coded laser lines after recovery.
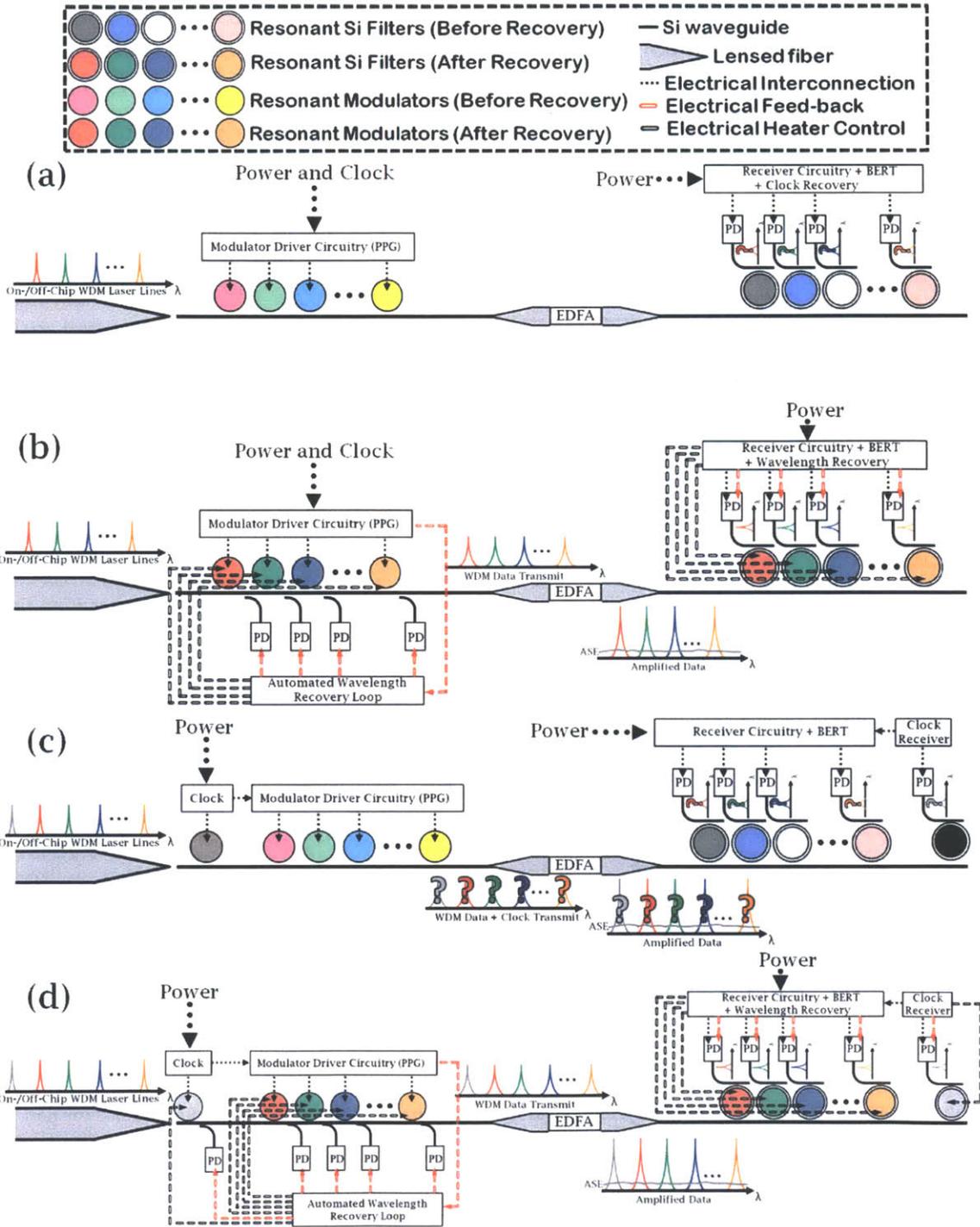
Figure 26. off-chip WDM link before(a) and after(b) automated wavelength recovery with amplification between transmitter and receiver chips, off-chip WDM link with optical clock transmitter and receiver (d). Color coding is used to indicate the resonance of filters and modulators.

A realistic WDM link transmitter and receiver with off-chip amplification, before and after AWR is shown in Fig. 26, a-b. This link requires clock recovery and a WDM channel can be used to transmit and receive the clock to eliminate clock recovery circuitry (Fig. 26,c-d). Thru port of the resonant modulators can be observed by adding an evanescently coupled PD after each modulator. The data received by each PD and the electrical data will be used as a feedback signal for the AWR loop and integrated heater within the modulator will be used to align the laser line (Fig. 26, c). For a 1-MHz thermal tuner bandwidth, and a data rate of 10-Gb/s, every $32^{th}$ bit from the electrical data can be compared to the data received by the PD at a loop with a bandwidth of ~312GHz. Another approach is to measure the average intensity in the PD and selecting a bias point based on the optical true one and zero. A loop bandwidth ~10-20MHz can be used for this approach which minimizes the power consumption of the driver circuitry. Power consumption of the heater driver have been measured on a monolithically integrated platform and at a clock frequency >20MHz a significant power is consumed by the driver head [87]. So far, all modulator recovery demonstrations [89,90] include a calibration data which is not a realistic solution considering optical performance fluctuations due to fabrication/wafer imperfections.

The transmitted data need to be demultiplexed before the receiver. A PD integrated to the drop port of each resonant filter is already being utilized for receiving the data. Therefore, the AWR loop can be implemented to use the feedback from this PD and sending the control voltage to the integrated heaters (Fig. 26, d). Maximizing the received signal at the detector will automatically align the data to the filter. The performance will be limited with the receiver saturation and/or sensitivity, depending on the input laser power and the insertion loss of the filter. The underlying algorithm of such a loop will be explained in Chapter 3.

The laser power fluctuations and frequency drifts are excluded up to this point since it is not directly related to silicon photonics except possible thermal crosstalk between the lasers and silicon photonic chip. However, laser is the key component of WDM link and AWR loop required to compensate laser power fluctuations and frequency drift. AWR algorithm offered in Chapter 3 is designed to handle this problem and minimizes the power required to stabilize the lasers.

## 1.12 Conclusions

In the first chapter, on-/off-chip electrical and optical communications introduced. The roadmap for bandwidth, clock frequency, energy, data storage and photonic integration discussed. The off-chip bandwidth (>1Tb/s in 2020) and energy scaling (<100fJ/bit in 2020 for HPC machines) obviously requires new technologies other than single channel per wire/fiber. WDM based Silicon Photonics is offered as an enabling technology that can reach those goals. However, there are challenges, wafer level and process variations and thermal fluctuations, ahead that silicon photonics need to overcome. The frequency drifts due to those challenges can be ~$\pm$150GHz (~ $\pm$50GHz from wafer/process imperfections and $\pm10^{0}$C from dynamic temperature fluctuations). The most of the available methods to compensate frequency drifts have limitations. Thermo-optic tuning can be used as a general solution at the expense of static power consumption. Integration of heaters to each resonator and using a feedback loop that constantly check for the frequency drifts is proposed which is called as automated wavelength recovery (AWR).

## 1.13 References

[1] Moore, G.E. , "Cramming More Components Onto Integrated Circuits," *Proceedings of the IEEE* , vol.86, no.1, pp.82-85, Jan. 1998.

[2] Ferris-Prabhu, A.V., "Introduction to Semiconductor Device Yield Modeling", 1992, New York: Artech House.

[3] Chen, F., et al. "Line edge roughness and spacing effect on low-k TDDB characteristics ," in Reliability Physics Symposium, 2008. IRPS 2008. IEEE Internati onal . 2008.

[4] Chen, X., et al. "A cost effective 32nm high -K/ metal gate CMOS technology for low power applications with single-metal/gate-first process" in VLSI Technology, 2008 Symposium on. 2008.

[5] Jan, C.H., et al. "A 32nm SoC platform technology with 2<sup>nd</sup> generation high -k/metal gate transistors optimized for ultra low power, high performance, and high density product applications" in Electron Devices Meeting (IEDM), 2009 IEEE International . 2009.

[6] Wang, X., L. Wu, and Y. Liu, "Low -power LVD S I/O interface for above 2Gb/s -per-pin operation" Journal of Electronics (China), 2009. 26(4): p. 525-531.

[7] Zhang, W., N.K. Jha, and L. Shang, "Design space exploration and data memory architecture design for a hybrid nano/CMOS dynamically reconfigurable architecture" J. Emerg. Technol. Comput. Syst., 2009. 5(4): p. 1-27.

[8] Sinharoy, B. "POWER7 multi-core processor design in Microarchitecture", 2009. MICRO-42. 42nd Annual IEEE/ACM International Symposium on. 2009.

[9] Howard, J., et al., "A 48-Core IA-32 Processor in 45 nm CMOS Using On -Die Message-Passing and DVFS for Performance and Power Scaling. Solid-State Circuits," IEEE Journal of, 2011. 46(1): p. 173-183.

[10] Kogge, P., The Tops in Flops (vol 48, pg 48, 2011). Ieee Spectrum, 2011. 48(3): p. 8-8.

[11] Kwong, J. and A.P. Chandrakasan, "Advances in Ultra -Low -Voltage Design. Solid-State Circuits Newsletter," IEEE, 2008. 13(4): p. 20 -27.

[12] Daniel E. Atkins, K.K.D., Stuart I. Feldman, Hector Gacia-Molina, Michael L. Klein, David G. Messerschmitt, Paul Messina, Jeremiah P. Ostriker, Margaret H. Wright, "Revolutionizing Science and Engineering Through Cyberinfrastructure. Report on the National Science Foundation Blue-Ribbon Advisory Panel on Cyberinfrastructure", 2003.

[13] Nahin, Paul J. (2002). "Oliver Heaviside: The Life, Work, and Times of an Electrical Genius of the Victorian Age".

[14] International Technology Roadmap for Semiconductors 2011 Edition - Interconnect.

[15] Watanabe, T., et al "Self-Formed Barrier Technology using CuMn Alloy Seed for Cu Dual-Damascene Interconnect with Porous-SiOC/ Porous-Par Hybrid Dielectric," IITC, 2007, p. 7

[16] Saito, T., et al., "A Reliability Study of Barrier-Metal-Clad Copper Interconnects With Self-Aligned Metallic Caps," IEEE Trans. Electron Devices, 48, p. 1340 .

[17] Hu, C.K., et al., "A Study of Electromigration Lifetime for Cu Interconnects Coated with CoWP, Ta/TaN, or SiCxNyHz," Proceedings of AMC, 2003, p. 253.

[18] http://www.xbitlabs.com/news/memory/display/20111102133147_Samsung_Plans_to_Manufacture_Hyper_Memory_Cube_Solutions_in_2013_2014.html.

[19] http://www.bit-tech.net/news/hardware/2012/05/09/microsoft-hmc-tech/1.

[20] http://www.electroiq.com/articles/ap/2011/12/ibm-fabs-micron-memory-cube-with-tsv-tech.html.

[21] http://www.i-micronews.com/news/Micron-reveals-%C3%A2%E2%82%AC%C5%93Hyper-Memory-Cube%C3%A2%E2%82%AC%20-3DIC-Technology,6472.html.

[22] Xie, Y., et al., "Design space exploration for 3D architectures" J. Emerg. Technol. Comput. Syst., 2006. 2(2): p. 65 -103.

[23] Amdahl, G.M., "Validity of the single processor approach to achieving large scale computing capabilities," AFIPS Joint Computer Conference, 1967.

[24] Coteus, P.W., Krickerbocker J.U. , Lam C.H., Vlasov Y. A., "Technologies for exascale systems," IBM Journal of Research and Development 55(5), 14-1, IBM, 2011

[25] Facchini, M., et al., An RDL -configurable 3D memory tier to replace on-chip SRAM, in Proceedings of the Conference on Design, Automation and Test in Europe 2010, European Design and Automation Association: Dresden, Germany. p. 291-294. 42

[26] Krishnamoorthy, A.V., et al., Computer Systems Based on Silicon Photonic. Interconnects. Proceedings of the IEEE, 2009. 97(7): p. 1337-1361.

[27] Kawano, M., et al. A 3D Packaging Technology for 4 Gbit Stacked DRAM with 3 Gbps Data Transfer. in Electron Devices Meeting, 2006. IEDM '06. International. 2006.

[28] Weldezion, A.a.W., Roshan and Pamunuwa, Danesh B. and Zheng, Li-Rong and Tenhunen, Hannu (2009) Bandwidth optimization for through silicon via (TSV) bundles in 3D integrated circuits. In: Workshop Notes, Design, Automation and Test in Europe

[29] Koyanagi, M., T. Fukushima, and T. Tanaka, High-Density Through Silicon Vias for 3 -D LSIs. Proceedings of the IEEE, 2009. 97(1): p. 49 -59

[30] Facchini, M., et al., An RDL -configurable 3D memory tier to replace on-chip SRAM, in Proceedings of the Conference on Design, Automation and Test in Europe 2010, European Design and Automation Association: Dresden, Germany. p. 291-294.

[31] Savidis, I . and E.G. Friedman, Closed -Form Expressions of 3-D Via Resistance, Inductance, and Capacitance. Electron Devices, IEEE Transactions on, 2009. 56(9): p. 1873 -1881.

[32] http://techreport.com/review/15818/intel-core-i7-processors

[33] Philip Garrou, Christopher Bower, Peter Ramm, "Handbook of 3D Integration," John Wiley & Sons, (2011)

[34] Kryder, Mark H. *et al.,*"After Hard Drives - What Comes Next?", *IEEE Transactions on Magnetics* **45** (10) October 2009.

[35] An Introduction to the Intel QuickPath Interconnect, 2009.

[36] Byungsub, K. and V. Stojanovic "A 4Gb/s/ch 356fJ/b 10mm equalized on-chip interconnect with nonlinear charge -injecting transmit filter and transimpedance receiver in 90nm CMOS". in Solid-State Circuits Conference - Digest of Technical Papers, 2009. ISSCC 2009. IEEE International . 2009.

[37] Preston, K., B. Schmidt, and M. Lipson, "Polysilicon photonic resonators for large-scale 3D integration of opti cal networks," Opt. Express, 2007. 15(25): p. 17283-17290.

[38] Young, I.A., et al. "Integration of nano -photonic devices for CMOS chip-to -chip optical I/O," in Lasers and Electro -Optics (CLEO) and Quantum Electronics and Laser Science Conference (QELS), 2010 Conference on . 2010.

[39] Samuel Williams, K.D., Jonathan Carter, Leonid Oliker, John Shalf, Katherine Yelick , David Bailey, "PERI - auto -tuning memory -intensive kernels for multicore," Journal of Physics, 2008. 125.

[40] Chang, Y.C., C.S. Wang, and L.A. Coldren, High-efficiency, high-speed VCSELs with 35 Gbit=s error-free operation. Electronics Letters, 2007. 43(19): p. 1022 -1023.

[41] Imai, S., et al. Recorded low power dissipation of 0.14 mW/Gbps in 1060 nm VCSELs for &#x201C;Green&#x201D; optical interconnection . in Semiconductor Laser Conference (ISLC), 2010 22nd IEEE International. 2010.

[42] Zortman, W.A., et al. "Monolithic integration of silicon electronics and photonics". in Winter Topicals (WTM), 2011 IEEE. 2011.

[43] J. S. Orcutt, A. Khilo, C. W. Holzwarth, M. A. Popovi, H. Li, J. Sun, T. Bonifield, R. Hollingsworth, F. X. Kärtner, H. I. Smith, V. Stojanovi, and R. J. Ram, "Nanophotonic integration in state-of-the-art CMOS foundries," Opt. Express, vol. 19, pp. 2335-2346, 2011.

[44] Miller, D.A.B., "Device Requirements for Optical Interconnects to Silicon Chips," Proceedings of the IEEE, 2009. 97(7): p. 1166 -1185.

[45] http://www.tomshardware.com/charts/hdd-charts-2012/-01-Read-Throughput-Average-h2benchw-3.16,2901.html

[46] http://www.tomshardware.com/charts/ssd-charts-2012/AS-SSD-4K-Q64-Random-Read,2786.html

[47] M. R. Watts *et al.*, "Vertical junction silicon microdisk modulators and switches", *Opt. Exp.* 19, 21989–22003 (2011).

[48] E. Timurdogan *et al.*, "Vertical Junction Silicon Microdisk Modulators at 25Gb/s," *OFC*, 2013.

[49] A. Biberman, M. Shaw, E. Timurdogan, J. Wright, and M. Watts, "Ultralow-loss silicon ring resonators," Opt. Lett. 37, 4236-4238 (2012).

[50] L. Agazzi, J. Bradley, M. Dijkstra, F. Ay, G. Roelkens, R. Baets, K. Wörhoff, and M. Pollnau, "Monolithic integration of erbium-doped amplifiers with silicon-on-insulator waveguides," Opt. Express 18, 27703-27711 (2010).

[51] Zerbe, J.; Werner, C.; Stojanovic, V.; Chen, F.; Wei, J.; Tsang, G.; Kim, D.; Stonecypher, W.; Ho, A.; Thrush, T.; Kollipara, R.; Yeh, G.-J.; Horowitz, M.; Donnelly, K.; , "Equalization and clock recovery for a 2.5-10Gb/s 2-PAM/4-PAM backplane transceiver cell," *Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC. 2003 IEEE International* , vol., no., pp. 80-479 vol.1, 2003

[52] W. Zortman, D. Trotter, and M. Watts, "Silicon photonics manufacturing," Opt. Express 18, 23598-23607 (2010).

[53] J.H. Kiely, D.V. Morgan, and D.M. Rowe, *Meas. Sci. Technol.* 5, 182 (1994)

[54] J. Xie, C. Lee, M. F. Wang, Y. H. Liu and H. H. Feng, Journal of Micromechanics and Microengineering 19, 125029 (2009).

[55] Jang M, Park Y, Jun M, Hyun Y, Choi S, Zyung T. The characteristics of Seebeck coefficient in silicon nanowires manufactured by CMOS compatible process. Nanoscale Res Lett. 2010;5:1654. doi: 10.1007/s11671-010-9690-2.

[56] Faiz Salleh, Kiyosumi Asai, Akihiro Ishida and Hiroya Ikeda.Appl. Phys. Express **2** (2009) 071203

[57] Hochbaum, A. I. *et al.* Enhanced thermoelectric performance of rough silicon nanowires. *Nature* **451**, 163–167 (2008)

[58] M. W. Riley, J. D. Warnock and D.F. Wendel, "Cell Broadband Engine Processor: Design and Implementation," *IBM J. Res. & Dev.* Vol. 51 No. 5 (2007).

[59] V. Raghunathan, J. Yagüe, J. Xu, J. Michel, K. Gleason, and L. Kimerling, "Co-polymer clad design for high performance athermal photonic circuits," Opt. Express 20, 20808-20813 (2012).

[60] B. J. Eggleton, B. Luther-Davies, and K. Richardson, "Chalcogenide photonics," *Nat. Photon.* **5**, 1–8 (2011).

[61] V. Raghunathan, T. Izuhara, J. Michel, and L. Kimerling, "Stability of polymer-dielectric bi-layers for athermal silicon photonics," Opt. Express 20, 16059-16066 (2012).

[62] A. Canciamilla, F. Morichetti, S. Grillanda, P. Velha, M. Sorel, V. Singh, A. Agarwal, L. Kimerling, and A. Melloni, "Photo-induced trimming of chalcogenide-assisted silicon waveguides," Opt. Express 20, 15807-15817 (2012).

[63] Andrea Melloni ; Stefano Grillanda ; Antonio Canciamilla ; Carlo Ferrari ; Francesco Morichetti ; Michael Strain ; Marc Sorel ; Vivek Singh ; Anu Agarwal ; Lionel C. Kimerling; Photo-induced trimming of chalcogenide-assisted silicon photonic circuits. Proc. SPIE 8266, Silicon Photonics VII, 82660A (February 9, 2012)

[64] V. Raghunathan, S. Grillanda, V. Singh, A. Canciamilla, F. Morichetti, A. Agarwal, J. Michel, A. Melloni, and L. Kimerling, "Trimming of Athermal Silicon Resonators," in Integrated Photonics Research, Silicon and Nanophotonics, OSA Technical Digest (online) (Optical Society of America, 2012), paper IW4C.5.

[65] A. Melloni, A. Canciamilla, C. Ferrari, S. Grillanda, F. Morichetti, P. Velha, M. Sorel, J. Hu, J. Musgraves, B. Zdyrko, I. Luzinov, K. Richardson, V. Singh, A. Agarwal, and L. Kimerling, "Exploiting photosensitivity in chalcogenide-assisted integrated optics," in Integrated Photonics Research, Silicon and Nanophotonics, OSA Technical Digest (CD) (Optical Society of America, 2011), paper IMB1.

[66] J. Liu, M. Beals, A. Pomerene, S. Bernardis, R. Sun, J. Cheng, L. C. Kimerling, and J. Michel, "Waveguide-integrated, ultralow-energy GeSi electroabsorption modulators," Nature Photonics 2, 433-437 (2008).

[67] Y. Vlasov, W. M. J. Green, and F. Xia, "High-throughput silicon nanophotonic wavelength-insensitive switch for on-chip optical networks," Nature Photonics 2, 242 - 246 (2008)

[68] M. Popovíc, T. Barwicz, M. Watts, P. Rakich, L. Socci, E. Ippen, F. Kärtner, and H. Smith, "Multistage high-order microring-resonator add-drop filters," Opt. Lett. 31, 2571-2573 (2006).

[69] T. Barwicz, H. Byun, F. Gan, C. Holzwarth, M. Popovic, P. Rakich, M. Watts, E. Ippen, F. Kärtner, H. Smith, J. Orcutt, R. Ram, V. Stojanovic, O. Olubuyide, J. Hoyt, S. Spector, M. Geis, M. Grein, T. Lyszczarz, and J. Yoon, "Silicon photonics for compact, energy-efficient interconnects [Invited]," J. Opt. Netw. 6, 63-73 (2007).

[70] Soref, R.; Bennett, B.; , "Electrooptical effects in silicon," *Quantum Electronics, IEEE Journal of*, vol.23, no.1, pp. 123- 129, Jan 1987 doi: 10.1109/JQE.1987.1073206.

[71] Q. Xu, B. Schmidt, S. Pradhan, and M. Lipson, "Micrometre-scale silicon.electro-optic modulator ", Nature, Vol. 435, pp. 325-327, 19 May 2005

[72] Gan, F.; Barwicz, T.; Popovic, M.A.; Dahlem, M.S.; Holzwarth, C.W.; Rakich, P.T.; Smith, H.I.; Ippen, E.P.; Kartner, F.X.; , "Maximizing the Thermo-Optic Tuning Range of Silicon Photonic Structures," *Photonics in Switching, 2007*, vol., no., pp.67-68, 19-22 Aug. 2007

[73] M. R. Watts et al., "Vertical junction silicon microdisk modulators and switches," *Opt. Express* 19, 21989–22003 (2011).

[74] M. R. Watts et al., "Adiabatic Resonant Microrings (ARMs) with directly integrated Thermal Microphotonics," *CLEO,* 2012.

[75] S. Manipatruni, C. B. Poitras, Q. Xu, and M. Lipson, Opt. Lett. 33, 1644.2008.

[76] X. Xiao, H. Xu, X. Li, Y. Hu, K. Xiong, Z. Li, T. Chu, Y. Yu, and J. Yu, "25 Gbit/s silicon microring modulator based on misalignment-tolerant interleaved PN junctions," *Opt. Express* **20,** 2507–2515 (2012).

[77] J. C. Rosenberg, W. M. J. Green, S. Assefa, D. M. Gill, T. Barwicz, M. Yang, S. M. Shank, and Y. A. Vlasov, "A 25 Gbps silicon microring modulator based on an interleaved junction," *Opt. Express* **20,** 26411–26423 (2012).

[78] G. Li, X. Zheng, J. Yao, H. Thacker, I. Shubin, Y. Luo, K. Raj, J. E. Cunningham, and A. V. Krishnamoorthy, "25Gb/s 1V-driving CMOS ring modulator with integrated thermal tuning," *Opt. Express* **19,** 20435–20443 (2011).

[79] G. Li, X. Zheng, H. Thacker, J. Yao, Y. Luo, I. Shubin, K. Raj, J. E. Cunningham, and A. V. Krishnamoorthy, "40 Gb/s thermally tunable CMOS ring modulator," Proc. International Conference on Group IV Photonics (GFP), 1–3 (2012).

[80] Y. Hu, X. Xiao, H. Xu, X. Li, K. Xiong, Z. Li, T. Chu, Y. Yu, and J. Yu, "High-speed silicon modulator based on cascaded microring resonators," *Opt. Express* **20,** 15079–15085 (2012).

[81] X. Xiao, X. Li, H. Xu, Y. Hu, K. Xiong, Z. Li, T. Chu, J. Yu, and Y. Yu, "44-Gb/s silicon microring modulators based on zigzag PN junctions," *IEEE Photon. Technol. Lett.* **24,** 1712–1714 (2012).

[82] M. R. Watts, "Adiabatic microring resonators," *Opt. Lett.* **35,** 3231–3233 (2010).

[83] M. R. Watts, W. A. Zortman, D. C. Trotter, G. N. Nielson, D. L. Luck, and R. W. Young, "Adiabatic resonant microrings (ARMs) with directly integrated thermal microphotonics," Proc. Conference on Lasers and Electro-Optics (CLEO), CPDB10 (2009).

[84] E. Timurdogan, M. Moresco, A. Biberman, J. Sun, W. A. Zortman, D. C. Trotter, and M. R. Watts, "Adiabatic resonant microring (ARM) modulator," Proc. Optical Interconnects Conference (OI Conference), TuC6 (2012).

[85] A. Biberman, E. Timurdogan, W. Zortman, D. Trotter, and M. Watts, "Adiabatic microring modulators," Opt. Express 20, 29223-29236 (2012).

[86] G. Li et al., "25Gb/s 1V-driving CMOS ring modulator with integrated thermal tuning," *Opt. Express* 19, 20435-20443 (2011).

[87] W. Zortman et al., "Integrated CMOS Comaptible Low Power 10Gbps Silicon Photonic Heater Modulator," *OFC,* 2012.

[88] C. Sun, E. Timurdogan, M. R. Watts, V. Stojanović "Integrated Microring Tuning in Deep-Trench Bulk CMOS," OIC 2013 (to be presented)

[89] Zortman, W.; Lentine, A.; Trotter, D.; Watts, M.; , "Bit error rate monitoring for active wavelength control of silicon microphotonic resonant modulators," *Micro, IEEE* , vol.PP, no.99, pp.1, 2013

[90] Padmaraju, K., Chan, J., Chen, L., Lipson, M. and Bergman, K., "Thermal stabilization of a microring modulator using feedback control", Opt. Express, Vol. 20, No. 27, 17 Dec. 2012

[91] A. McCaulley, V. M. Donnelly, M. Vernon, and I. Taha, "Temperature dependence of the near-infrared refractive index of silicon, gallium arsenide, and indium phosphide," *Physical Review B* 49, 7408 (1994).

# 2 Active Silicon Photonic Resonators

In Chapter 1, we focused on a WDM link that is composed photonic multiplexer, transmitter and receivers and proposed a general architecture for AWR. In order to perform AWR on chip, one needs the resonant filters and modulators. Therefore, this chapter will focus on resonators that I lead the effort of photonic design, layout and experimentally demonstration. Integrated electronic circuit for thermal tuner control is designed and implemented by Chen Sun. The vertical PN junction, utilized in section 2.1-2.3 for electro-optic modulation, is designed with Cheryl M. Sorace-Agaskar using Sentaurus process simulations. The devices in section 2.1-2.4 fabricated in CNSE, Albany. Micron Technology fabricated the photonic device and the electric circuit in section 2.5. The resonators, will be presented here, can be used to form a large scale low power high bandwidth WDM link with a focus on enabling AWR on chip.

## 2.1 Resonant Modulators

Silicon resonant modulators that utilize plasma dispersion effect [1], confine light in compact, high-Q devices and minimize device capacitance and modulation energy and enhance the bandwidth [2-16]. The first resonant modulators utilized carrier-injection in a P-I-N junction and ridge-waveguides for electrical contacts [4]. However, carrier injection based devices are bandwidth limited by the free-carrier lifetime in silicon ridge waveguides. Further, while ridge waveguide based modulators work well in injection configurations, in depletion-based modulators, the lateral PN junctions that have been employed exhibit a poor overlap with the optical mode, resulting in excess losses, higher drive voltages, and/or reduced extinction [4,9]. Additionally, lateral PN junction requires external electrical contacts and requires external ridge layer. The external ridge layer limits the confinement factor and bend-radii due to induced radiation. The most compact demonstrated ridge waveguide based modulator is 5 μm, minimizing the junction capacitance and the RC time constant, a similar device was demonstrated to operate at 40 (44) Gb/s, with 7- (2.3-) dB extinction ratios at 2-V driving voltages [13]. Moreover, vertical PN junctions enable centrally contacted microdisks [5-7] and microrings [8], and preserve hard outer wall of the resonator which minimizes the bent radii, capacitance and power consumption and substantially increase the overlap of the optical mode with the depletion region, thereby reducing the

drive voltage, improving the extinction ratio and reducing the excess losses. WDM link can support more channels with a compact device that results with a large free spectral range (FSR). In record-setting demonstrations, vertical PN junction devices have achieved error-free modulation up to 12.5Gb/s with only a 1V drive and while consuming only 3fJ/bit [6,7]. However, vertical junction modulators have been limited to 12.5Gb/s [5-8, 16]. Recently, we demonstrated the first vertical junction modulator to achieve open-eye diagrams up to 25Gb/s [17]. This work will be explained in section 2.2. Another demonstration is integrating a heater element to a high performance vertical junction microdisk modulator. This device can be directly used in a realistic WDM link with AWR loop. This work will be explained in section 2.3.

However, microdisks inherently support spurious modes that corrupt the free spectral range (FSR) by introducing unwanted resonance dips on the transmission. Therefore, only half of the FSR can be used for WDM channels in a silicon photonic link. Higher doping concentrations near the waveguide wall lower the quality factor (Q) of the fundamental mode and do not cut-off undesired higher-order modes. Microrings eliminate the undesired modes, but directly contacting the microring leads to scattering and loss. A 4-$\mu$m adiabatic resonant microring modulator, which enabled single-mode operation by adiabatic tapering of the single mode waveguide to allow interior contacts, was demonstrated but limited in data-rate to 12.5 Gb/s due to electrical resistance of the contacts [8,16]. Recently, we demonstrated L-shaped resonant microring modulator that can achieve error free operation up to 30Gb/s, which will be explained in section 2.4.

## 2.2 Vertical Junction Microdisk Modulator at 25 Gb/s

Previous demonstrations of vertical junction silicon modulators were limited by excess device resistance and capacitance caused both by electro-optic design and non-Ohmic electrical contacts [5-8, 16]. To reduce the resistance in the device we devised a circularly contacted silicon microdisk modulator (Fig. 1). The circular contact ensures that the electrical path out to the junction is effectively both short and wide, therein minimizing resistance.
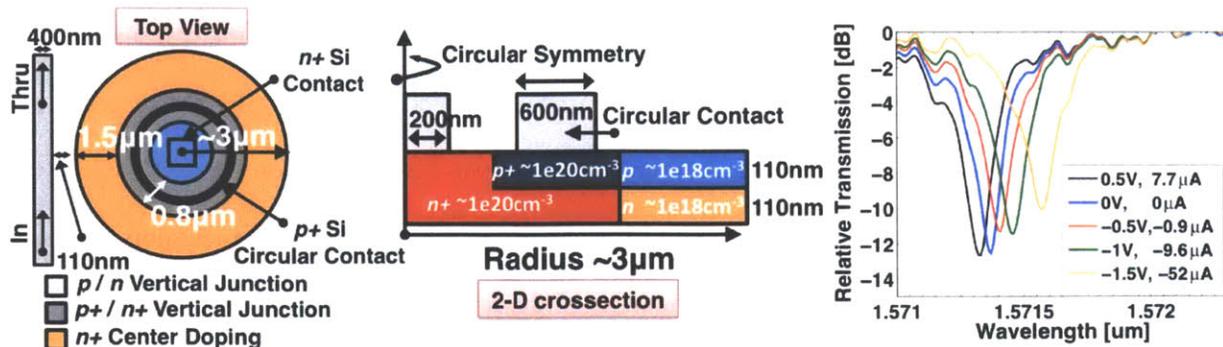
Figure 1. Top-view of the 6-μm-diameter microdisk modulator which utilizes circular inner contacts (left), 2D crossection showing the doping profile with PN vertical junction and P+ and N+ overlapping contacts (middle), spectral response of the microdisk modulator with respect to voltage dropped and current passing through the modulator (right).

The ~3μm radius microdisk modulator has a hard outer wall to maximize confinement and minimize optical bend loss. N+ and P+ doped regions with a carrier concentration ~$1 \times 10^{20}$ cm$^{-3}$ are used to circularly contact the device. PN vertical junction with a carrier concentration of ~$1 \times 10^{18}$ cm$^{-3}$ is formed around the edge. The PN vertical junction, centered ~110nm thickness, is chosen to maximize the mode overlap and formed around the edge (annulus of ~1.5μm). The N+ and P+ contacts are formed inside the microdisk where it is invisible to the fundamental radial mode, to allow a low resistance circular P+ contact and central N+ contact which will minimize the resistance of the overall device (Fig. 1, left-middle). The modulator was fabricated by using 193-nm immersion lithography on a 220-nm thick silicon-on-insulator (SOI) wafer with 2μm buried oxide (BOX) layer for optical isolation. The center contact is a 0.4μm×0.4μm square and the annulus of the circular contact is ~0.6μm wide. The microdisk is optically fed by a single mode, 400nm wide input waveguide with a 110nm coupling gap designed to ensure critical coupling.

### 2.2.1 Device characterization and demonstrated results

A GSG probe was landed to apply a voltage across the junction. Spectra were measured for a voltage sweep from +0.5V to -1.5V (Fig. 1, right). The voltage range was chosen to keep the diode off and in depletion mode. To maximize extinction ratio for an AC measurement, an AC coupled 1.2V$_{pp}$ was chosen as the device operating voltage when using a 50Ω terminated GSG probe. For a high impedance termination, only 0.6V$_{pp}$ is required.

In order to characterize the modulators and electro-optic test bench is used. An input tunable CW laser source was aligned with a polarization controller for TE excitation of the bus waveguide and the resonance of the microdisk modulator at ~1571.4 nm. The data generated by a pattern generator, is a non-return-to-zero (NRZ) on-off-keyed (OOK) signal, encoded with a $2^{31}-1$ pseudo-random bit sequence (PRBS). An electrical amplifier was used to achieve an AC coupled $1.2V_{pp}$ drive signal at the desired data rates. Drive voltage is applied to the modulator with a $50\Omega$-terminated GSG probe and the voltage dropped across the modulator is also ~$1.2V_{pp}$. The optical thru port is then received by an Erbium Doped Fiber Amplifier (EDFA) to overcome fiber-to-chip coupling losses and a tunable bandpass filter with a 1nm 3dB bandwidth, was used to filter out the Amplified Spontaneous Emission (ASE) of the EDFA. Eye diagrams were then taken with a sampling scope at data rates of 10Gb/s, 15Gb/s, 20Gb/s, and 25Gb/s (Fig. 2). The dynamic extinction ratio and insertion loss based on the optical eye diagrams are summarized in Table 1. With low insertion loss (~1dB) and high extinction ratio (>6.9dB), the measurements are comparable to commercial modulators and the optical eyes are wide-open all the way up to 25Gb/s.
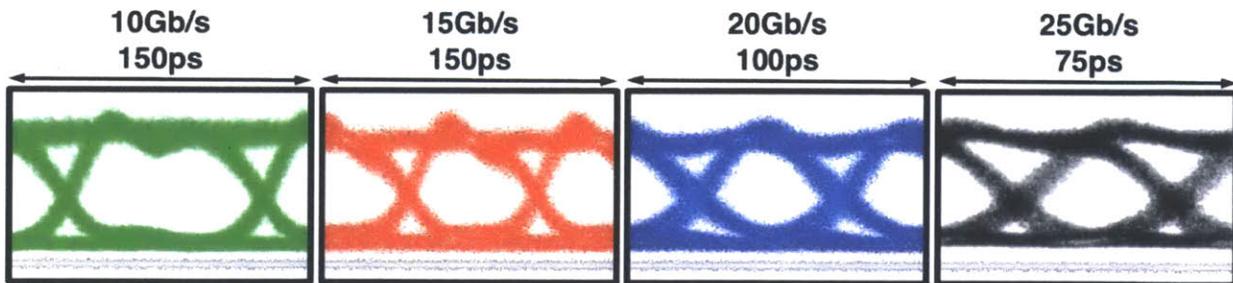


Figure 2. Measured optical eye diagrams from the on-chip silicon microdisk modulator at AC coupled device voltage of 1.2Vpp at 10-, 15-, 20-, 25-Gb/s data dates. The eye diagrams are shown with the true zero (gray line) at each data rate. The true one level is obtained by setting the laser off resonance by ~1nm and decreasing the EDFA to a non-satured level. The true one level can be calculated using the Table 1 insertion loss data.

For Bit-Error-Rate (BER) testing, a variable optical attenuator (VOA) was inserted before the receiver placed to adjust the received power level. The optical data was detected by a high-speed P-I-N photodiode and transimpedance amplifier (TIA) receiver and fed to the Bit-Error-Rate Tester (BERT) differentially for evaluation. No pre-emphasis or equalization was used throughout the experiments. The

total fiber-to-fiber insertion loss was ~16.5 dB. A commercial lithium niobate (LibNO$_3$) Mach-Zehnder modulator was substituted in for the on-chip microdisk modulator for comparison and power penalty. The commercial modulator is rated at 35GHz 3dB bandwidth, and driven with an AC coupled voltage 5.5V$_{pp}$ electrical signal.

In order to further quantify modulator performance, BER measurements and power penalty analysis is performed from 10Gb/s to 25Gb/s data rates (Fig. 3). For up to 20Gb/s, we have error free operation (BER <10$^{-12}$). At 25Gb/s even the commercial modulator cannot perform error free operation for the current setup parameters. Therefore, we believe the BER is limited by the experimental setup rather than the device itself. The power penalty is the relative received power difference at a BER of 10$^{-9}$ between the silicon microdisk modulator and the commercial modulator (Fig. 3). Data transferred by the silicon microdisk modulator have received with a positive power penalty of 0.29, 0.68, 1.17 and 2.06 dB, at data rates of 10Gb/s, 15Gb/s, 20Gb/s and 25Gb/s, respectively.

We can estimate the modulator energy-per-bit of the microdisk modulator (E$_M$) by calculating the average junction capacitance (C$_J$) and using the experimental voltage swing (Vpp); E$_M$=CV$_{pp}^2$/4 [5,6]. The junction capacitance is C$_J$=$\varepsilon_0$ $\varepsilon_{Si}$A/d where, $\varepsilon_0$ is vacuum permittivity, $\varepsilon_{Si}$ is relative permittivity of Si, $A$ is junction the area and $d$ is the depletion width. Sentaurus simulations are performed to estimate average depletion width and determined as ~65nm which leads to a junction capacitance of ~35fF. For a 1.2V$_{pp}$ drive voltage the modulator energy per bit is ~13fJ/bit.

| Data Rate | Extinction Ratio [dB] | Insertion Loss [dB] | Power Penalty [dB] |
|---|---|---|---|
| 10 Gb/s | 9.22 | 0.45 | 0.29 |
| 15 Gb/s | 8.57 | 0.65 | 0.68 |
| 20 Gb/s | 7.6 | 1.12 | 1.17 |
| 25 Gb/s | 6.9 | 1.59 | 2.06 |

Table. 1. Summary of the demonstrated results of the silicon microdisk modulator for data rates from 10Gb/s to 25Gb/s. Extinction ratio and insertion loss is based on the optical eye measurements. The measured power penalty of microdisk modulator is relative to the commercial lithium niobate modulator.
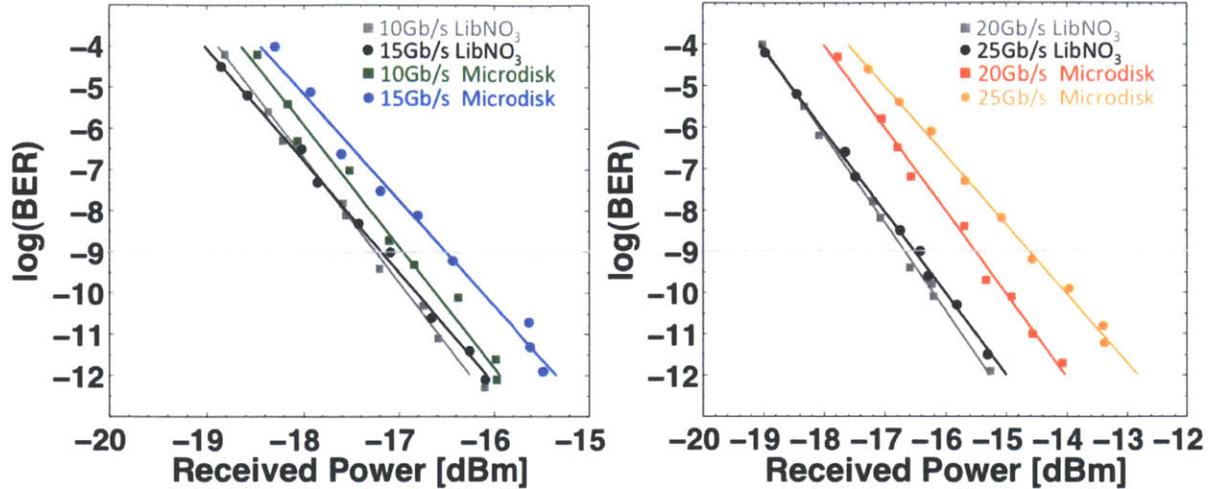
Fig. 3. Bit-error-rate (BER) curves measured for microdisk modulator. BERs are experimentally measured for data rates at 10Gb/s, 15Gb/s (left) and 20Gb/s, 25Gb/s (right). The results are compared to a lithium niobate Mach-Zender modulator and power penalty is obtained relative to this modulator.

## 2.3 Vertical Junction Microdisk Modulator with Integrated Heater

The modulator demonstrated in section offers high-performance modulation, however it can be only used in a WDM link if the resonance aligns with filters and lasers naturally. In a realistic WDM link, resonance drifts, induced by process/wafer variations and dynamic temperature fluctuations, distort the alignment. Therefore, resonant modulator required to integrate thermal tuners to be compatible with AWR arcitechture. The integration of heaters within microring filters and modulators achieves the best optimization of thermal tuning power (4.4 μW/GHz) and speed (1 μs) [18]. Unfortunately, heaters are usually integrated within resonant modulators at the expense of area and/or performance. A large ridge microring modulator (400μm$^2$) with ~42μW/GHz tuning efficiency and ~67% junction area coverage around the periphery [9] and a compact microdisk modulator (50μm$^2$) with 7μW/GHz tuning efficiency and 50% junction area coverage around the periphery [19] have been demonstrated in the literature. Junction area coverage limits the modulation efficiency and leads to an insertion loss of >5dB [9] and >3dB [19]. For a normal distribution of ±10$^0$C temperature fluctuations and a ~100GHz resonance frequency offset due to fabrication/wafer variations, the integrated heater needs to compensate ±75GHz on average. The total modulation and heater energy became >322fJ/bit [5] and >200fJ/bit [6] at a data rate

53

of 20Gb/s.

We proposed a ~6-µm diameter (footprint ~ 28 µm$^2$) microdisk modulator with a CMOS compatible integrated heater in the center that allows for high performance modulation and minimum thermal capacitance. The hard outer walls of the microdisk modulator enable minimum bend radii and high-Q operation [5-8,16-19]. High-speed modulation is enabled by a vertical *p-n* junction near to the edge of the microdisk modulator and low resistance interior contacts. The proposed microdisk modulator is measured to have a 4.9µW/GHz thermal tuning efficiency and ~11fJ/bit performance at a data rate of 13 Gb/s, a 5.8dB extinction ratio and a 1.22dB insertion loss. This is the most efficient heater integration in a modulator yet with total modulation and heater energy predicted to be less than <50fJ/bit which perfectly fits with 2020 energy roadmap.

### 2.3.1 Device characterization and demonstrated results

The microdisk modulator, coupled to a bus waveguide, has an integrated vertical *p-n* junction around the edge of the microdisk with same doping levels with the device explained in section 2.2. The integrated heater is formed in the center of the microdisk using the same *p* and *p+* type doping levels to minimize the number of necessary mask layers and fabrication cost (Fig. 4, left). This design allows, for
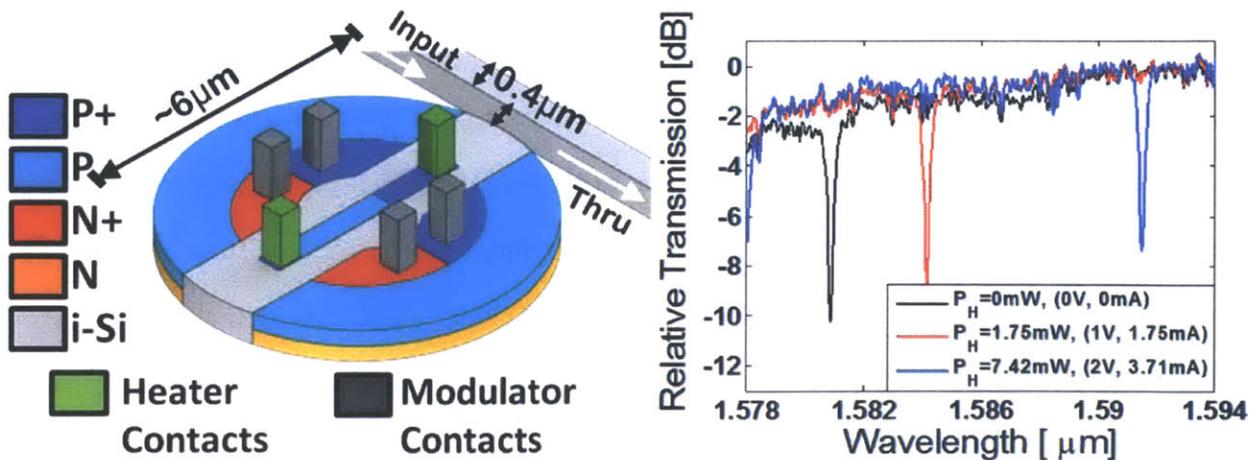


Figure 4. 3D sketch of the microdisk modulator showing size, doping and contacts (left), and measured DC spectral response of the integrated heater inside the microdisk modulator with an applied bias voltage to heater pins (right).

the first time, almost full peripheral junction area coverage (~90%) of the vertical junction around the edge of the microdisk without compromising high speed operation. The polarity of the heater bias is

chosen to minimize electrical crosstalk with the diode. The silicon waveguide thickness is 220nm and the bus waveguide width is 400nm.

Thermal tuning of the microdisk modulator is achieved by applying a DC bias voltage across the heater contacts. Spectral response is measured with a CW tunable laser for an applied heater DC voltage for 0V, 1V and 2V, as shown in Fig. 4, right. Wavelength shifts of 3 nm (~360 GHz) and 10 nm (~1.2 THz) are observed at heater power consumptions of 1.75 mW (1V) and 7.42 mW (2V). These values correspond to a heater efficiency of $4.9\mu W/GHz$ and $6.2\mu W/GHz$, respectively.

The microdisk modulator is characterized with a DC bias voltage applied across modulator pins from -3V to 0.5V as shown in Fig. 5, right. For a probe wavelength ~1581nm, a DC extinction ratio of 6dB is measured between -1V and 0.5V bias. The DC insertion loss is 1.2dB. In order to demonstrate high speed performance, the microdisk modulator is initially tuned to a frequency offset of 1.2 THz by applying 2V to the heater. The modulator contacts are driven electrically with a terminated probe and an AC coupled 1.5 $V_{pp}$ non-return-to-zero-on-off-keying (NRZ-OOK) signal encoded with a pseudo-random-bit-sequence (PRBS) at a pattern length of $2^{31}-1$. The optical eye diagram is obtained by a digital sampling oscilloscope at a data rate of 13-Gb/s, as illustrated in Fig. 5, left. The dynamic extinction ratio is 5.8dB and insertion loss of 1.22dB, in good agreement with the DC characterization (Fig. 5, right). Modulator capacitance is calculated (the same way described in section 2.2) to be 20fF and the energy of the modulator is estimated to be ~11fJ/bit for a voltage swing of 1.5Vpp. The modulator is PRBS source limited to 13Gb/s and experiments to achieve higher data rate operation are ongoing.

If the proposed microdisk modulator has a frequency offset of ~100GHz due to fabrication variation and is on a processor chip with $\pm10^0C$ temperature variation, the required heater power for compensation is ~1.5mW. Combined with an electro-optic modulation power of 0.22mW at a data rate of 20Gb/s, the microdisk modulator will have a realistic energy performance of 85 fJ/bit when one includes both heater and modulator energy. If the necessary tuning variations of the multiple microdisks in a WDM link obey a Gaussian distribution, then the required thermal compensation can be halved, and a more realistic performance estimate would be 48fJ/bits at a data rate of 20Gb/s as opposed to >322fJ/bit [5] and

>200fJ/bit [6].
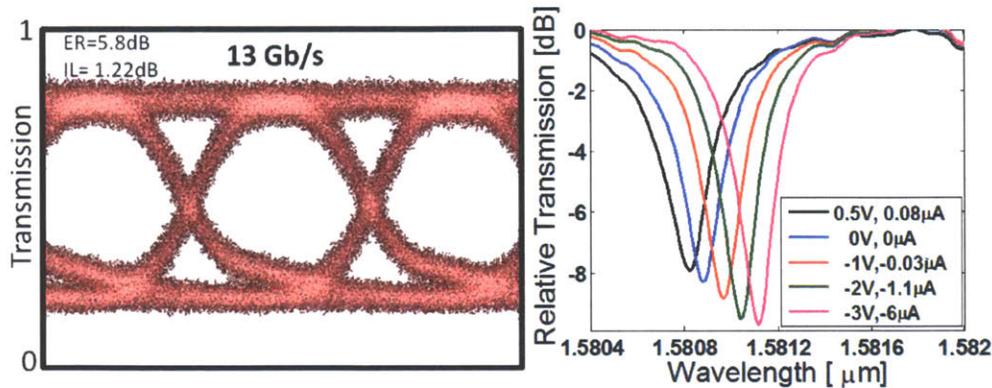


Figure 5. High-Speed Optical Eye Diagrams at a data rate of 13-Gb/s with an ac-coupled 1.5Vpp drive and 2V applied across heater contacts. The extinction ratio is 5.8dB and insertion loss is 1.22dB (left). Measured spectral response of the microdisk modulator with applied DC bias voltage to modulator pins from -3V to 0.5V (right).

## 2.4 L-Shaped Resonant Microring Modulator

Although the microdisk modulator demonstrated in section 2.3 is AWR compatible, it will limit the number of channels due to spurious or higher order modes. Spurious modes introduce unwanted resonance dips in transmission and thereby corrupting the FSR. The only half or less of the large FSR enabled by microdisk modulators, is useful in such a situation. Higher doping concentrations near the waveguide wall lower the quality factor (Q) of the fundamental mode and do not cut-off undesired higher-order modes. Microrings enable single mode operation, but directly contacting to the microring introduce excess scattering and radiation loss. Single mode external ridge based microrings enable electrical contacts at the expense of low confinement and bent radii (>5μm), thereby increasing the area and power consumption by nearly an order of magnitude [9-13]. A 4-μm adiabatic resonant microring modulator, which enabled single-mode operation by adiabatic tapering of the single mode waveguide to allow interior contacts, was demonstrated but limited in data-rate to 12.5 Gb/s due to electrical resistance of the contacts [8,16]. However, it allows contacts only in the adibatically widened regions which increases the contact resistance as opposed to microdisk modulators. Therefore, a new design is required.

We introduced a new class of modulators, L-shaped resonant microrings (LRM), which allow for both hard outer walls and single mode propagation while maintaining low resistance electrical contacts.

Thus, LRM modulators can have a compact size, high quality factor, and an uncorrupted FSR while maintaining high-speed operation. To allow for interior contacts, a hybrid junction consisting of a vertical and interdigitated PN junction (Fig. 6, left) is used. The L-shaped waveguide is formed by an internal ridge etch of a wide micro-ring/-disk, thus preserving the hard outer waveguide wall and enabling minimum bend radii and peripheral direct contact to full waveguide thickness. The thickness of the inner ridge is adjusted for single mode operation [20]. Since the L-shaped waveguide is inherently single mode, the coupling region does not require complicated waveguide geometry or phase matching. Here, we will demonstrate a hybrid PN junction based LRM modulator operating in depletion mode, with data rates up to 30 Gb/s, and occupying chip area of < 20 $\mu m^2$ and maintaining an uncorrupted 5.3 THz FSR.

### 2.4.1 Device characterization and demonstrated results

The LRM modulator, coupled to a bus waveguide, has an integrated hybrid PN junction formed by alternating doping of the ridge and full thickness silicon waveguide (Fig. 6, left). Doping concentrations are identical to the modulators in sections 2.2 and 2.3. The full and ridge silicon waveguide thicknesses are 220 and 110 nm, respectively. Spur-free FSR of 5.3 THz is demonstrated on a device with a diameter of ~5μm (Fig. 6, middle). Spectrum is measured at applied DC voltages from −2 to 0.5 V to characterize the modulator (Fig. 6, right).
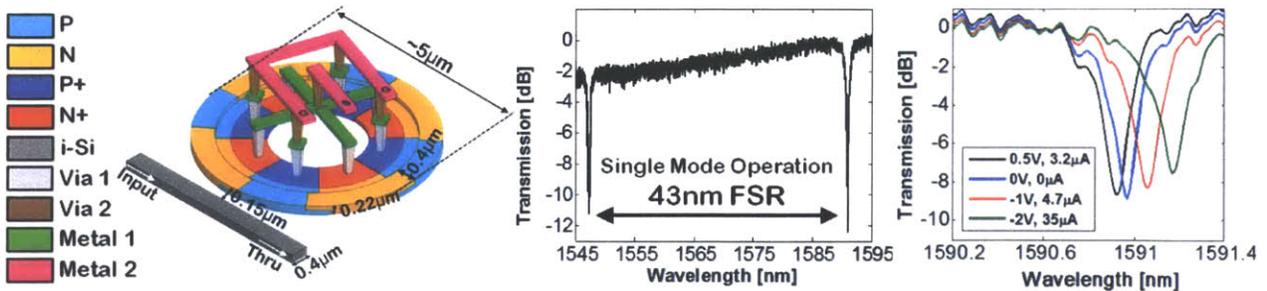


Figure 6. 3D sketch of the LRM modulator showing size, doping and metal connections (left), Spur-free single mode operation of the LRM modulator with a FSR of 5.3 THz (middle), and measured spectral response at applied DC voltages (right).
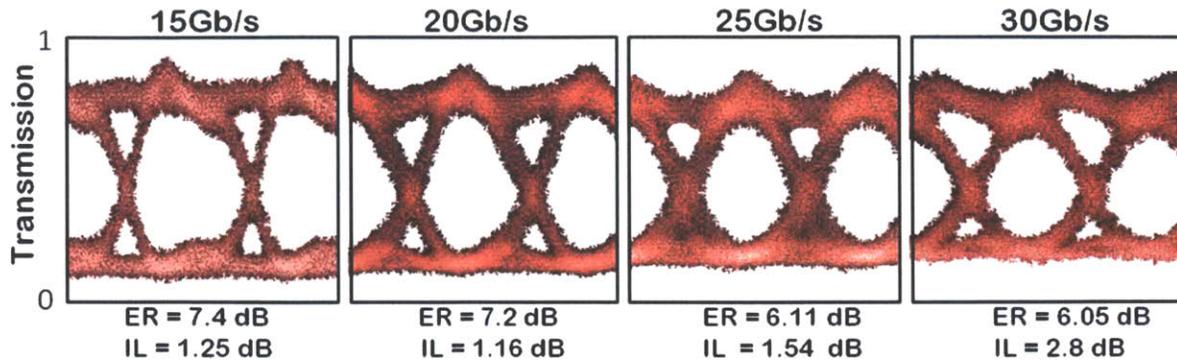
Figure 7. High-Speed Optical Eye Diagrams at 15-, 20-, 25- and 30-Gb/s data rates. Extinction ratio (ER) and insertion loss (IL) is denoted below the eye diagrams.

The modulator was driven electrically with a terminated probe using a non-return-to-zero-on-off-keying (NRZ-OOK) signal encoded with pseudo-random-bit-sequence (PRBS) data with a pattern length of $2^{31}-1$, at 2.2 $V_{pp}$ with a DC bias of –0.6 V. Optical eye diagrams at 15-, 20-, 25- and 30-Gb/s data rates are obtained using a digital sampling oscilloscope (Fig. 7). Extinction ratio and insertion loss is denoted below the eye diagrams. For further quantification of the modulator performance, BER measurements and power penalty analysis was performed from 15- to 30-Gb/s (Fig. 8). The procedure of BER testing is identical to section 2.2.1. A commercial $LiNbO_3$ Mach-Zehnder modulator with 4dB insertion loss and 35GHz bandwidth is used for comparison. Error-free operation (BER $<10^{-12}$) up to 30Gb/s and < 2.8 dB power penalty at a BER of $10^{-9}$ were demonstrated.
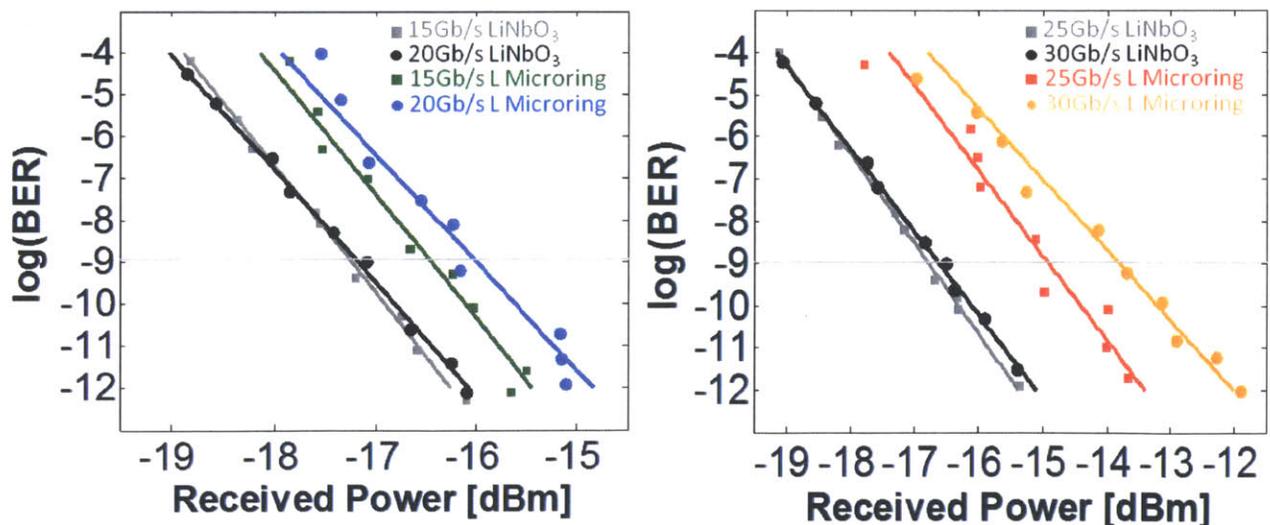


Figure 8. Bit Error Rate (BER) curves measured for the L shaped and $LiBNO_3$ modulator at 15-, 20- (left), 25- and 30-Gb/s (right) data rates.

## 2.6 Active Resonant Filters

The multiplexing and demultiplexing operations in an ideal WDM link are performed by microring-based filters which are tightly aligned between to laser lines and data carrier frequency. The resonance drifts by process/wafer variations and dynamic temperature fluctuations require high-speed thermo-optic control of those filters. The efficient active tunable filters can be realized in a realistic WDM link with AWR. The challenge is in implementing such control efficiently. Without using complex undercut etch processes [21], the most efficient thermo-optic tunable filter to date have been demonstrated with a 4.4 µW/GHz tuning efficiency, 1µs thermal time constant and a FSR of 5.6 THz [18]. For a WDM link with ± 10$^0$C variation due to processor activity, thermal tuning will consume ~0.6 mW [21] and ~0.9 mW [18] power as opposed to an integrated microdisk modulator with a 3 fJ/bit performance and a power consumption of 30 µW at a data rate of 10 Gb/s [5,6]. Therefore, it is essential to introduce new resonant microring filters. Additionally, high-speed thermal tuning can enable reconfigurable networks as well as track the dynamic processor activity. However, the buried oxide thickness around microring filter is favoring either thermal tuning efficiency or speed. Without using complex undercut etch processes, we demonstrated a better tuning efficiency than [18] with a L-shaped resonant microring filter. This work will be explained in section 2.7. We have also demonstrated the first heater driver and adiabatic microring filter integration in a CMOS (customized DRAM) platform which will be explained in section 2.8.

## 2.7 L-Shaped Resonant Microring Filter with Thermal Tuner

We introduced a new class of filters, L-shaped resonant microrings (LRM), which allow for both hard outer walls and single mode propagation while enabling interior electrical contacts without inducing radiation or scattering. Thus, LRM filters can directly integrate a heater within the resonator and minimize the thermal capacitance and maintain a compact size and an uncorrupted FSR. Here, we demonstrate a 6-um diameter LRM filter with high efficiency (3.3 µW/GHz), high-speed (1.6 µs) thermal tuning and record low thru-to-drop power penalty (<1.1 dB) over the 4 THz FSR.

## 2.7.1 Device characterization and demonstrated results
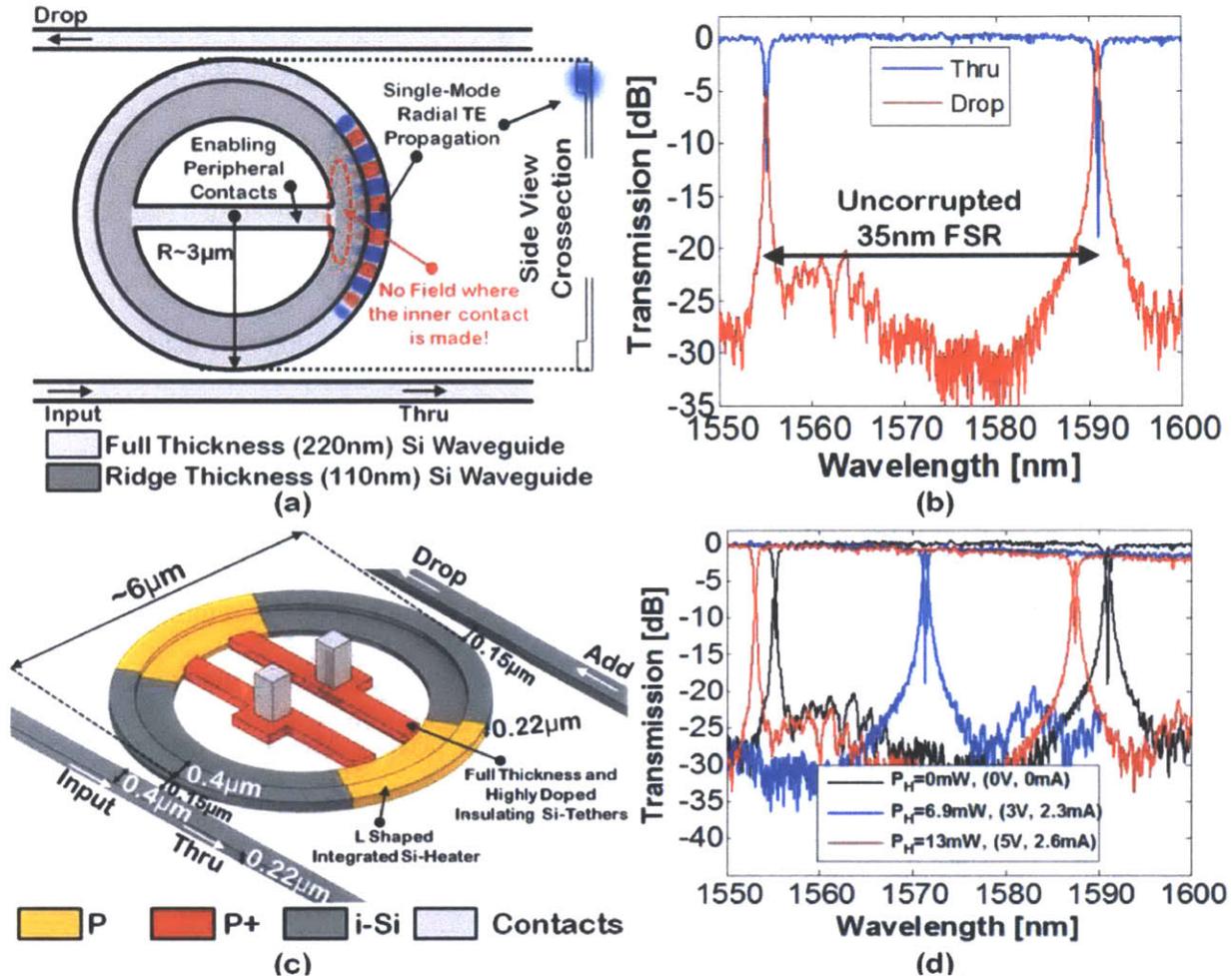


Figure 9. (a) FD-TD simulation of a LRM resonator, (b) Measured spectrum of a fabricated LRM filter, showing uncorrupted 4 THz FSR on thru and drop ports, (c) 3D sketch of the proposed LRM filter with integrated heater and insulating tethers, (d) Demonstration of thermal tuning of full FSR with a 13mW heater power and a 5V drive voltage.

The LRM filter has a L-shaped waveguide crossection, formed by an internal ridge etch of a wide micro-ring/-disk. The thickness of the inner ridge and width of the microring is optimized for single mode operation [20], thus the coupling region does not require a complicated waveguide geometry or phase matching. Since the radial TE mode is confined at the edge of the LRM, lossless contacts can be introduced to the periphery of the interior ridge without inducing scattering or radiation as shown by the Finite Difference Time Domain (FD-TD) simulation in Fig. 9(a). For a compact LRM resonator with a 220nm thick silicon waveguide and 110nm ridge waveguide, a cylindrical mode solver is predicting

single mode operation with a high quality factor ($Q>10^5$) and large spur-free FSR (>5 THz).

A LRM filter is designed and fabricated as illustrated in Fig. 9(c). Thru and drop spectrum of the fabricated LRM filter, showing single-mode operation and an uncorrupted FSR of 4 THz, is measured using tunable CW laser (Fig. 9(b)). Integrated heaters are introduced by P type doping concentration of $1\times10^{18}$ cm$^{-3}$ in the L-shaped waveguide. The thermally conductive vias/contacts are required to be insulated from the integrated heater for enabling low-power and rapid thermal tuning. This is achieved by contacting the integrated heater with narrow heavily doped ($p+$ type doping concentration of $1\times10^{20}$ cm$^{-3}$) silicon waveguide tethers (Fig. 9(c)). The resistance of the integrated heater is ~1.3k$\Omega$ and ~2k$\Omega$ for an applied voltage of below and above 3V, respectively.
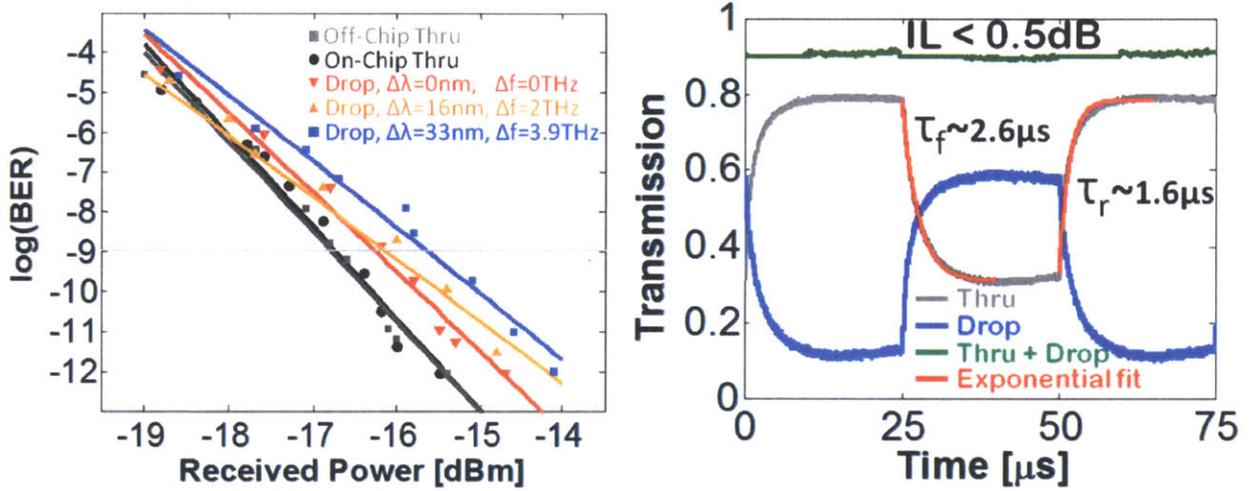


Figure 10. Bit Error Rate (BER) curves measured for the thru and drop ports of the LRM filter at different thermo-optic resonance shifts. to the BER curve of off-chip thru (bypassing the chip) is measured for comparison (left), temporal response of the thru and drop ports of the LRM filter, excited by 20kHz 0.15V square-wave drive, fit to a 2.6μs exponential decay and a 1.6μs rise thermal time constant (shown in red), the insertion loss of the LRM filter is <0.5dB.

The LRM filter is thermo-optically tuned by applying a voltage across the integrated heater and thru and drop spectrum of is measured using tunable CW laser (Fig. 9(d)). Wavelength shifts of 16 nm (~2 THz) and 33 nm (~3.9 THz) is observed for a heater power of 6.9 mW (3V) and 13 mW (5V), respectively. These values correspond to a heater efficiency of 3.45 μW/GHz and 3.33 μW/GHz, respectively and ~1.3 mW heater power for a temperature variation of $\pm~20^0$C. Power dissipation of the proposed LRM filter, fabricated on thick SOI process, is comparable to the undercut process [21].

An external LiNbO$_3$ Mach-Zehnder modulator, driven with a non-return-to-zero-on-off-keying (NRZ-OOK) signal encoded with pseudo-random-bit-sequence (PRBS) data with a pattern length of $2^{31}$–1, and a data rate of 13 Gb/s, was used to quantify data transmission and routing performance of the LRM filter. The procedure of BER testing is identical to section 2.2.1. Bit error rate (BER) was measured for off-chip (bypassing the chip), on-chip thru port (off-resonance) of the LRM filter, and drop port (on-resonance) at an applied voltage of 0V ($\Delta\lambda$=0nm), 3V ($\Delta\lambda$=16nm) and 5V ($\Delta\lambda$=33nm) across the LRM filter as shown in Fig. 10, left. The power penalty between on- and off-chip thru is recorded as <0.1dB and between on-chip thru and drop port is 0.5dB, 0.7dB, and 1.1dB for the applied voltage of 0V ($\Delta\lambda$=0nm), 3V ($\Delta\lambda$=16nm) and 5V ($\Delta\lambda$=33nm).

The temporal response of the LRM filter was measured by driving the LRM filter with a square-wave at a frequency of 20 KHz and 0.15 Vpp, and observing the thru and drop port intensity of a laser probe at $\lambda \sim 1555$nm (Fig. 10, right). The thru port intensity is in good agreement with an exponential decay ($\tau_f \sim 2.6\mu s$) and rise ($\tau_r \sim 1.6\mu s$) fit, shown with red lines in Fig. 10, right. Insertion loss of the LRM filter (<0.5 dB) is determined from the total intensity of the thru and drop ports with respect to transmission one.

## 2.8 Monolithically Integrated Adiabatic Resonant Microring Filter with Thermal Tuner

To date, thermal tuning of resonators have been demonstrated and characterized for devices built on thick SOI with and without localized substrate removal (undercut) [9,18,19,22], in thin SOI with silicon-carbide substrate transfer [23], and in bulk CMOS with localized substrate removal under shallow-trench isolation (STI) [21].

We demonstrated a heater driver system for microring resonators consisting of a fully-digital $\Delta\Sigma$-based heater driver circuit and an ARM filter (Fig. 11, left), both monolithically integrated in a commercial 0.25 $\mu$m-equivalent bulk CMOS process with deep-trench isolation capability. Integration of the heater driver alongside the integrated heater minimizes the parasitic resistance from driver to the heater, provides a digital heater control interface through which multiple rings can be controlled on-chip, and eliminates the dedicated pads for external heater control used in the majority of previous work. Using

a process-compatible supply voltage of 2.5V, the system is able to tune the resonance of an ARM filter by 350GHz, with an efficiency of 10-15μW/GHz.

2.8.1 System Overview and Experimental Results

The driver circuit, designed and implemented by Chen Sun, consists of a synthesized pipelined accumulator and a custom one-transistor driver head (Fig. 11, right). The circuit utilizes pulse density modulation (PDM) to output a heater drive waveform consisting of a digital pulse train, with a duty-cycle corresponding to an 8-bit digital input setting. The slow thermal response of the ring heater smoothens ripples in temperature and transmission introduced by the digital nature of the drive waveform, provided that the driver's clock frequency (and hence the PDM's oversampling ratio) is set significantly higher than the thermal time constant. Since power consumption of the circuit scales with the clock frequency, driver power can be optimized by fine-tuning the oversampling ratio of the PDM. The duty-cycled nature of the driver guarantees a monotonic and linear relationship between heater power and input setting, as well as constant step size. The implementation in this work is aggressively pipelined to hit frequency targets >400MHz and sized to drive >5mA of current. Design constraints can be relaxed to lower driver power and area.
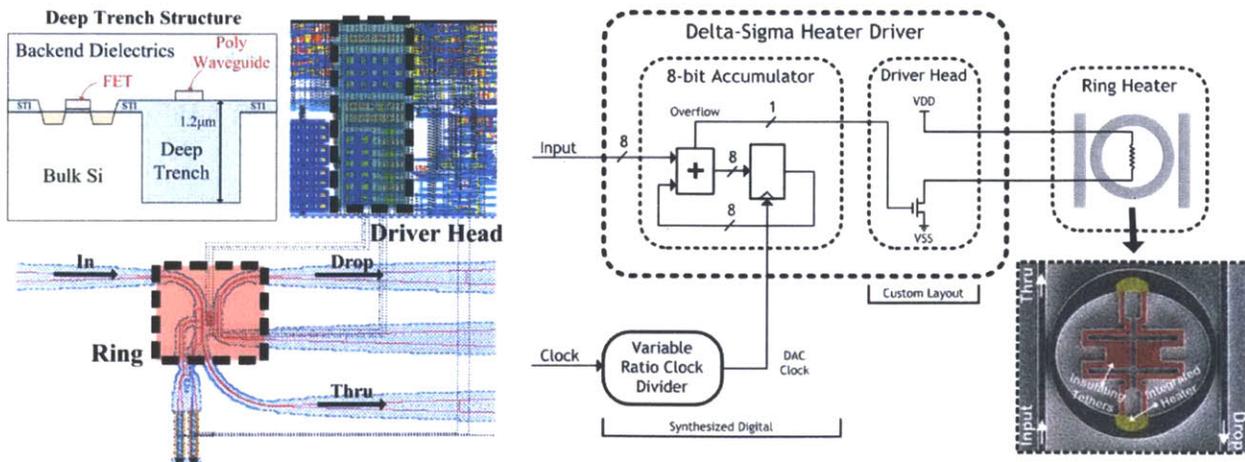


Figure 11. Layout of the integrated heater driver connected to the ARM filter, both integrated in a deep trench CMOS process (left). Block diagram of the $\Delta\Sigma$-based heater driver with SEM of the connected ARM filter (right). The ARM filter, 8-bit accumulator, and driver head occupy 28μm², 1500um², and 2500 um² of area, respectively, including area used for decoupling capacitances and fill cells
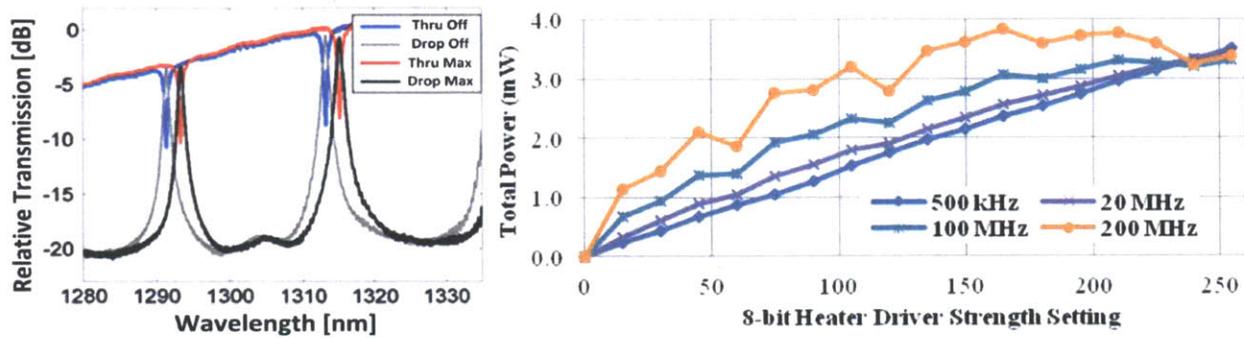
Figure 12. Optical spectrum when driver is *off* and at *max* power (left) and total power consumed at various driver power settings (right). For reference, *off* corresponds to a driver strength setting of 0, *max* corresponds to a strength setting of 255.

The ARM filter and circuit are integrated in a deep-trench bulk CMOS process (equivalent to a DRAM periphery process), with Poly-Si waveguides above deep oxide trenches (Fig. 11, left). The 6-μm diameter ARM filter is designed to work at a wavelength of λ~1290nm with a deep-trench. The single-mode waveguide width is 280nm in the coupling region and adiabatically tapered to 600nm to allow contacts to the adiabatic region. Single radial mode propagation is preserved through the adiabatic region, achieving an uncorrupted free spectral range (FSR) of 3.7THz (Fig. 12, left). The integrated heater with a resistance of ~1.7kΩ is formed by *n* type doping in the adiabatic region and the Si-tethers are doped *n*+ with silicide to minimize contact resistance and to insulate the tethers (Fig. 11, right-inset).
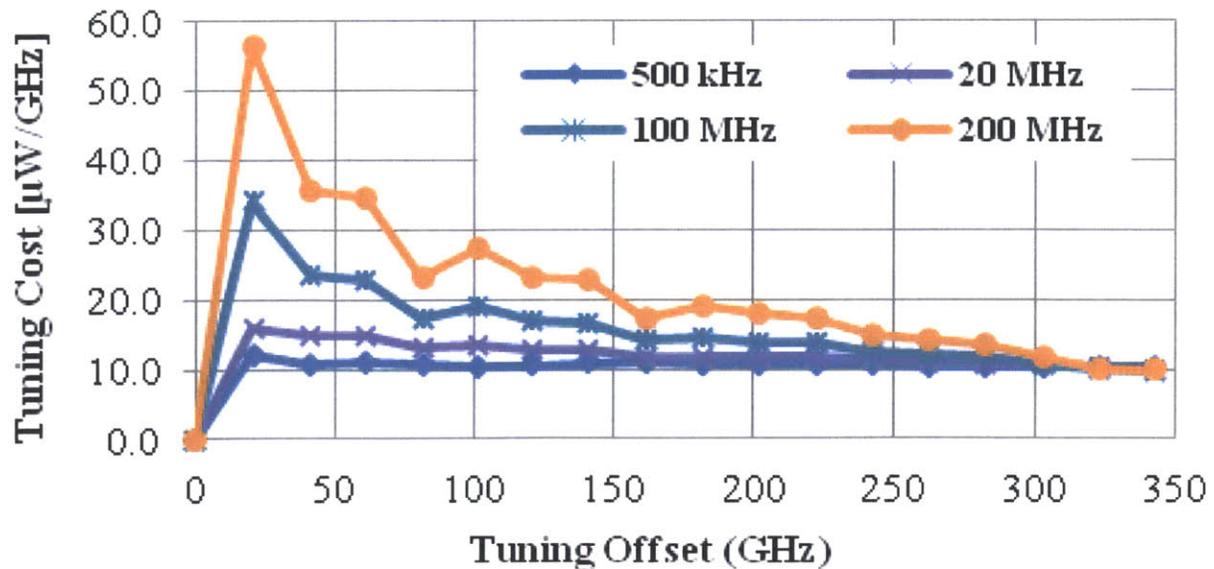


Figure 13. Tuning cost per gigahertz, with driver cost included, to reach a specific tuning offset

| Process | Raw Cost | FSR | Normalized |
|---|---|---|---|
| Bulk deep trench (this work) | 10 μW/GHz | 3.7 THz | 37.0 mW/2π |
| Thick SOI [9] | 42.2 μW/GHz | 1.6 THz | 67.4 mW/2π |
| Thick SOI with undercut [22] | 1.67 μW/GHz | 1.4 THz | 2.34 mW/2π |
| Thick SOI [18] | 4.4 μW/GHz | 5.6 THz | 24.6 mW/2π |
| Thin SOI with substrate transfer [23] | 14.3 μW/GHz | 2.04 THz | 29.2 mW/2π |
| Bulk shallow-trench with undercut [21] | 2.9 μW/GHz | 4.0 THz | 11.6 mW/2π |

Table 2. Comparison of the tuning costs between this work at 20 MHz in the high power regime and other works. The normalized cost is calculated as (Raw Cost) × (FSR/2π).

The heater output power is 3.5mW at the *max* power setting, limited by supply voltage (2.5V) and heater resistance (1.7kΩ). We achieved a maximum resonance shift of 350GHz (Fig. 12, left), corresponding to a step size of ~1.37GHz for an 8-bit input. Compared to the power delivered to the ARM's heater, the power overhead for the driver circuit is negligible at a clock frequency of 500kHz but substantial at 200MHz (Fig. 13, right). The tuning cost of the system improves with higher tuning offsets (Fig. 14), as the relative power overhead of the driver circuit shrinks compared to the power going to the heater. For the fabricated ARM filter, a clock frequency of 20MHz provided sufficient oversampling to minimize the transmission ripples, leading to a tuning cost between 10-15μW/GHz.

## 2.9 Conclusions

We have demonstrated the first vertical junction silicon microdisk modulator to achieve open eye-diagrams at a data rate of 25Gb/s and error-free operation up to 20Gb/s. These high-speed results were enabled by a unique doping profile which circularly contacts the modulators to reduce the device resistance while maintaining a hard outer wall for maximizing the optical confinement. The device represents the smallest silicon modulator to run at 25Gb/s and achieves the lowest reported power penalty,

important for the overall power budget in a microphotonic link.

We have integrated a silicon heater into a high performance vertical junction silicon microdisk modulator without affecting modulator performance or size. Low power modulation (11fJ/bit) at a data rate of 13-Gb/s, a 5.8-dB extinction ratio, a 1.22-dB insertion loss and a record-low thermal tuning (4.9-μW/GHz) of a high-speed modulator is achieved. A record low total energy of 48fJ/bit is predicted at a data rate of 20Gb/s for a frequency offset of ~100GHz and $\pm 10^{0}$C temperature variation.

Although a realistic AWR loop can be performed with the microdisk modulator with integrated thermal tuner, spurious mode in the FSR limit the WDM scalability or number of channels. In order to achieve a spur-free FSR, we demonstrated a new LRM modulator that achieves 30 Gb/s error-free operation in a compact (< 20 μm$^2$) structure while maintaining single-mode operation, enabling direct WDM across an uncorrupted 5.3 THz FSR. At a 70 GHz channel spacing, this modulator would allow 75 WDM channels along a single WDM link.

We have introduced high-efficiency heater elements inside a new single mode filter, a LRM filter, successfully. The LRM filter achieved high-efficiency (3.3μW/GHz) and high-speed ($\tau_f$~1.6 μs) thermal tuning and maintained signal integrity with record low thru to drop power penalty (<1.1 dB) over the 4 THz FSR and <0.5dB insertion loss. The efficiency is record-low for a thick SOI process. LRM resonators can be used to form suspended microrings and phase shifter elements.

Lastly, we demonstrated a monolithically-integrated heater driver system in a commercial bulk CMOS deep-trench process. We achieved a 350GHz thermal tuning range and 10-15μW/GHz tuning for an ARM filter integrated with CMOS driver. The power of the integrated driver is found to be negligible below ~1-2MHz. This is the first demonstration of microring thermal tuning and efficiency optimization in a deep-trench bulk process.

## 2.10 References

[1] R. A. Soref, and B. R. Bennett, "Electrooptical effects in silicon," IEEE J. Quantum Electron. **23**, 123-129 (1987)

[2] F. Gan and F. X. Kartner, "High-speed silicon electrooptic Modulator design," IEEE Photonics Technol. Lett. **17**, 1007-1009 (2005).

[3] Liu, L. Liao, D. Rubin, H. Nguyen, B. Ciftcioglu, Y. Chetrit, N. Izhaky, and M. Paniccia, "High-speed optical modulation based on carrier depletion in a silicon waveguide," Optics Express, Vol. 15, Issue 2, pp. 660-668 (2007).

[4] Q. Xu, B. Schmidt, S. Pradhan, and M. Lipson, "Micrometre-scale silicon electro-optic modulator," *Nature* **435**, 325–327 (2005).

[5] M. R. Watts, D. C. Trotter, R. W. Young, and A. L. Lentine, "Ultralow Power Silicon Microdisk Modulators and Switches," in *Proc. 5th Annual IEEE International Conference on Group IV Photonics*, Sorrento, Italy, WA2, pp. 4-6, September 2008.

[6] M. R. Watts, W. A. Zortman, D. C. Trotter, R. W. Young, and A. L. Lentine, "Vertical junction silicon microdisk modulators and switches," *Opt. Express* **19**, 21989–22003 (2011).

[7] William A. Zortman, Anthony L. Lentine, Douglas C. Trotter, and Michael R. Watts, "Low-voltage differentially-signaled modulators," Opt. Express **19**, 26017-26026 (2011)

[8] E. Timurdogan, M. Moresco, A. Biberman, J. Sun, W. A. Zortman, D. C. Trotter, and M. R. Watts, "Adiabatic resonant microring (ARM) modulator," Proc. Optical Interconnects Conference (OI Conference), TuC6 (2012).

[9] G. Li, X. Zheng, J. Yao, H. Thacker, I. Shubin, Y. Luo, K. Raj, J. E. Cunningham, and A. V. Krishnamoorthy, "25Gb/s 1V-driving CMOS ring modulator with integrated thermal tuning," *Opt. Express* **19**, 20435–20443 (2011).

[10] X. Xiao, H. Xu, X. Li, Y. Hu, K. Xiong, Z. Li, T. Chu, Y. Yu, and J. Yu, "25 Gbit/s silicon microring modulator based on misalignment-tolerant interleaved PN junctions," *Opt. Express* **20**, 2507–2515 (2012).

[11] J. C. Rosenberg, W. M. J. Green, S. Assefa, D. M. Gill, T. Barwicz, M. Yang, S. M. Shank, and Y. A. Vlasov, "A 25 Gbps silicon microring modulator based on an interleaved junction," *Opt. Express* **20**, 26411–26423 (2012).

[12] G. Li, X. Zheng, J. Yao, H. Thacker, I. Shubin, Y. Luo, K. Raj, J. E. Cunningham, and A. V. Krishnamoorthy, "25Gb/s 1V-driving CMOS ring modulator with integrated thermal tuning," *Opt. Express* **19**, 20435–20443 (2011).

[13] G. Li, X. Zheng, H. Thacker, J. Yao, Y. Luo, I. Shubin, K. Raj, J. E. Cunningham, and A. V. Krishnamoorthy, "40 Gb/s thermally tunable CMOS ring modulator," Proc. International Conference on Group IV Photonics (GFP), 1–3 (2012).

[14] Y. Hu, X. Xiao, H. Xu, X. Li, K. Xiong, Z. Li, T. Chu, Y. Yu, and J. Yu, "High-speed silicon modulator based on cascaded microring resonators," *Opt. Express* **20**, 15079–15085 (2012).

[15] X. Xiao, X. Li, H. Xu, Y. Hu, K. Xiong, Z. Li, T. Chu, J. Yu, and Y. Yu, "44-Gb/s silicon microring modulators based on zigzag PN junctions," *IEEE Photon. Technol. Lett.* **24**, 1712–1714 (2012).

[16] A. Biberman, E. Timurdogan, W. Zortman, D. Trotter, and M. Watts, "Adiabatic microring modulators," Opt. Express **20**, 29223-29236 (2012).

[17] E. Timurdogan *et al.*, "Vertical Junction Silicon Microdisk Modulators at 25Gb/s," *OFC*, 2013.

[18] M. R. Watts *et al.*, "Adiabatic Resonant Microrings (ARMs) with directly integrated Thermal Microphotonics," *CLEO,* 2012.

67

[19] W. Zortman *et al.*, "Integrated CMOS Comaptible Low Power 10Gbps Silicon Photonic Heater Modulator," *OFC*, 2012.

[20] J. Song *et al.*, "Thermo-optical tunable planar ridge microdisk resonator in silicon-on-insulator," *Opt. Exp.* 19, 11220-11227 (2011).

[21] J. S. Orcutt, *et al.*, "Nanophotonic integration in state-of-the-art CMOS foundries," *Optics Express*, Vol. 19, Issue 3, 2011

[22] P. Dong *et al.*, "Thermally tunable silicon racetrack resonators with ultralow tuning power," *Optics Express*, Vol. 18, Issue 19, 2010

[23] J. S. Orcutt *et al.*, "Open foundry platform for high-performance electronic-photonic integration," *Optics Express*, Vol. 20, Issue 11, 2012

# 3 Automated Wavelength Recovery Demonstration

For a realistic WDM link, the automated wavelength recovery (AWR) has to be performed for multiplexer, demultiplexer and transmitter resonators. This includes silicon microring/disk modulators and filters with integrated thermo-optic tuners. We have explained the architecture of the wavelength recovery in chapter 1 and the resonators designed and demonstrated to outperform the state of the art modulators and filters with thermal tuning in chapter 2. In this chapter, we will focus on a generic AWR algorithm and implementation to fix the wafer/process variations and dynamic temperature fluctuations. For a normal distribution of $\pm10^0$C temperature fluctuations and a ~100GHz resonance frequency offset due to fabrication/wafer variations, the integrated heater needs to compensate $\pm75$GHz on average out of a maximum of $\pm150$GHz [1-4]. The local temperature fluctuations, hot-spots, can be generated as fast as 100μs [3]. Therefore, AWR implementation required to be faster than ~10KHz.

Lasers are the key components of WDM link and AWR loop required to compensate laser power fluctuations and frequency drift. The laser power can fluctuate and the laser frequency can drift if the lasers are not in a controlled environment such as next or on the processors. If the AWR loop is robust against laser performance variations, then a laser with less control can be used which can increase the wall-plug efficiency. AWR algorithm offered in section 3.2 is designed assuming stable lasers but in section 3.5 we will update the AWR algorithm to handle the laser variations.

AWR compatible resonators from literature will be summarized here. I will only include resonators with integrated silicon heaters since they offer the best optimization between speed and efficiency. The adiabatic resonant microring (ARM) filters that have integrated heaters inside a single mode microring have demonstrated high efficieny (4μW/GHz) and high speed (1μs) thermal tuning [8,9]. A thermal sensor is integrated in such a ring and showed linear response with temperature [10]. A compact microdisk with integrated heater has demonstrated with 7μW/GHz tuning efficiency, 50% junction area coverage around the periphery, 1.14Vpp drive voltage, 3dB extinction ratio, >3dB insertion

loss at a data rate of 10Gb/s [7]. A large ridge microring modulator ($400\mu m^2$) with ~$42\mu W$/GHz tuning efficiency, ~67% junction area coverage around the periphery, 7fJ/bit modulation energy, 1Vpp drive voltage, ~5dB extinction ratio, >5dB insertion loss at a data rate of 25Gb/s have been demonstrated [5-6].The limitations of microdisk and ridge based modulators are explained in chapter 2.

Recently, different methods of wavelength tracking have been demonstrated. It is hard to call them AWR since the proposed methods does not offer a complete solution for temperature variations and process/wafer variations. C. Qui *et al.* [11] have leveraged scattering of the microring filters for wavelength locking. However, scattered light based techniques are not sufficiently reliable to enable scalable implementations and hard to integrate on-chip. K. Padmaraju *et al.* [12,13] have used a injection based modulator and a calibration set to achieve error free operation under thermal fluctuations to a certain point. The proposed method can only compensate $\pm 4^0C$ with a power penalty of >2.4dB. Therefore, it is not enough for either dynamic temperature fluctuations or fabrication/wafer variations. A modulator locking scheme is demonstrated using the microdisk modulator [7] with an integrated heater by active bit-error-rate (BER) testing loop [15,16].

In this chapter, we propose and demonstrate an AWR algorithm for a demultiplexer or a multiplexer ARM resonator [8,9]. While implementing the algorithm, we limit ourselves to have no *apriori* information about the quality factor or extinction ratio of resonator response, frequency drift between the resonance and the laser line and insertion loss of the resonators. The limitations will help us to provide a generic solution. The AWR algorithm required a simple implementation to achieve compact CMOS control circuitry, thereby minimizing the number of decisions making steps in the AWR algorithm and stored information in the registers. In the meantime, the AWR should maintain low-power and high-speed operation. An AWR compatible ARM resonator, shown in Fig. 1(b), will be used to implement the AWR algorithm [8,9]. Therefore, it is initially important to characterize the ARM in an open loop configuration to use as a reference. Later, the AWR algorithm will be introduced. The AWR will be implemented under thermo-optic stress and laser drifts. The speed of the AWR loop will be enhanced by simply changing

initial conditions. The stability of the loop in time will be monitored and quantified at different initial parameter settings. Lastly, the laser intensity will be actively adjusted and the AWR loop will be updated to recover in volatile environments.

## 3.1 Device fabrication and characterization
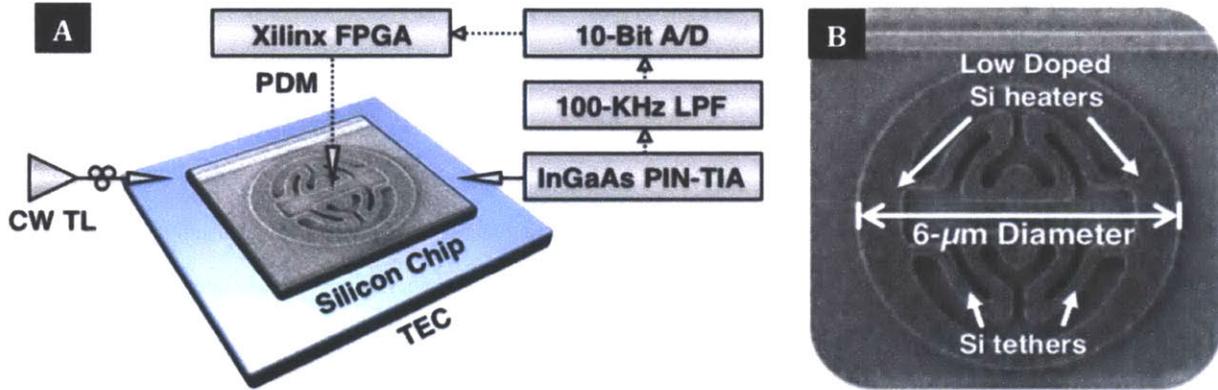


Figure 1. (a) Experimental setup for testing ARM resonator which is composed of a CW tunable laser, photonic chip, external TEC, FPGA and external photodetector, (b) micrograph of the ARM resonator, highlighting the integrated heater and insulating tethers.

The 6μm in diameter, single-mode ARM (Fig. 1(b)) is fabricated using a 350-nm process at Sandia National Laboratories on a six-inch 250-nm-thick silicon-on-insulator (SOI) wafer with a 3-μm buried oxide for optical isolation. The heater region and tethers have a N and a N+ doping concentration of $2 \times 10^{18}$/cm$^3$ and $10^{20}$/cm$^3$, respectively. Tungsten contacts, 500-nm in diameter, are directly contacted with insulating silicon tethers. The fabricated ARM resonator, coupled to a 320-nm wide and 250-nm thick silicon photonic bus, did not include a drop port. The gap between the edge of the microring and the bus waveguide is 360-nm.

Directly integrated heater inside the ARM minimize the thermal capacitance and enable high speed and low power thermal tuning. Silicon tethers act as low resistance contacts to the heater, thereby maximizing the voltage drop on the integrated heaters and increasing the tuning efficiency. The internal temperature, thus the resonance frequency can be thermo-optically tuned by applying a voltage bias across the integrated heaters. S shape and highly doped tethers are also achieving thermal isolation between contacts and the integrated heater within the resonator.

71
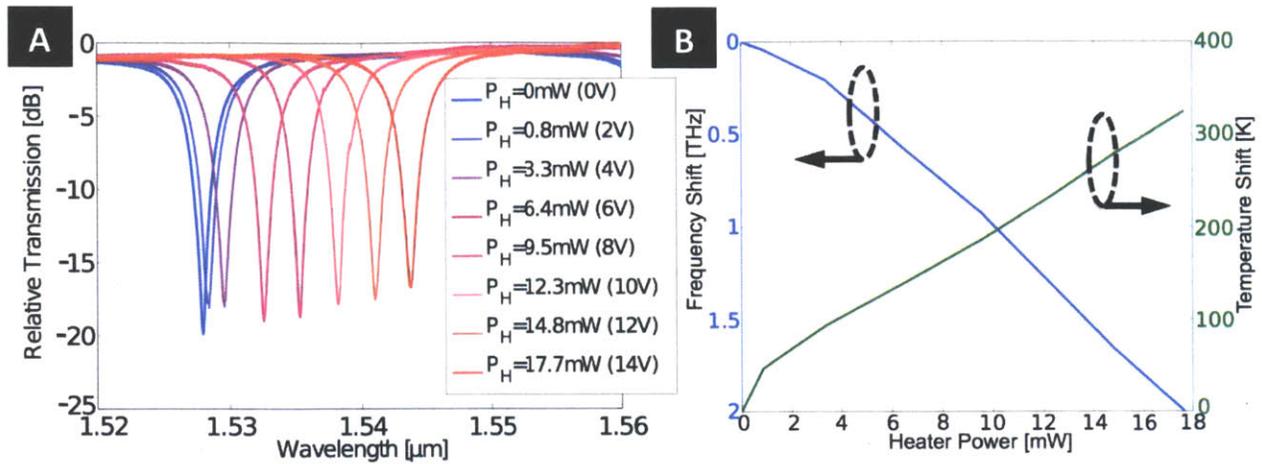
Figure 2. (a) Measured spectral response of a microring resonator as a function of heater power consumption (red shift is indicated by coloring from blue to red), (b) Correlation of heater power to frequency shift and calibrated temperature shift.

Experimental setup for full characterization of ARM is illustrated in Fig. 1a. The spectral scans for various voltage and power levels are measured using a CW tunable laser as shown in Fig. 2(a). TE radial fundamental mode is excited by the external laser. Resonance frequency shifts of 1 THz and 2 THz are achieved for 8.5mW and 17mW of heater power, respectively. The induced wavelength shift altered the coupling coefficient and the extinction ratio is dwarfed from 19.9dB to 16.5dB with ~17mW applied heater power. Heater power can be directly correlated with frequency shifts. However, relating the heater power to the internal temperature of the microring requires calibration with an external thermo-electro coupler (TEC). The TEC is placed under the chip and a thermistor is positioned next to the chip. Thermistor is used for readout and stabilization of the global chip temperature. The global chip temperature is assumed to be equal to internal temperature of the microring since the integrated heater is off during this measurement. Spectral scans are performed for various global chip temperatures. The spectral scans, obtained by applying voltage to the heater and the TEC, are used to correlate temperature shifts with integrated heater power (Fig. 2b). Temperature shifts of $150^0$K and $300^0$K correspond to 8.5mW and 17mW heater power, respectively. The ARM has a free spectral range (FSR) of 4THz and can be tuned more than 2THz. Therefore, it can be utilized for AWR applications and reconfigurable networks.

## 3.2 Automated Wavelength Recovery (AWR) Algorithm

While implementing the algorithm, we limit ourselves to have no *apriori* information about the quality factor or extinction ratio of resonator response, frequency drift between the resonance and the laser line and insertion loss of the resonators. The limitations will help us to provide a generic solution. The AWR algorithm required a simple implementation to achieve compact CMOS control circuitry, thereby minimizing the number of decisions making steps in the AWR algorithm and stored information in the registers. In the meantime, the AWR should maintain low-power and high-speed operation.

The AWR algorithm required to perform with no *apriori* information about the quality factor or extinction ratio of resonator response, frequency drift between the resonance and the laser line and insertion loss of the resonators. The algorithm should have minimum number of decisions and should not include data storage or calibration. This will simplify the algorithm and enable seamless integration with low-power CMOS electronics. The algorithm should locate the laser line around the resonance and achieve the global minimum for the through port or maximum for the drop port intensity for a first-order microring multiplexer filter. This will tightly align the laser line is with the filter resonance. The AWR algorithm is depicted with a state diagram in Fig. 3, which is composed of two loops; coarse and fine. The loops will be explained for an AWR implementation based on thru port intensity. Drop port based AWR can be implementing by simply reversing the conditional statements.

**Coarse Loop**                                   **Fine Loop**

Start 1: $P_H(t=0)=0, \Delta P_H(t=0)=\Delta P_C$   Start 2: $I_T(t=t_0) = I_0 , \Delta P_H(t=t_0) = \Delta P_F$
$P_H(t=t_0+1) = P_H(t=t_0) - \Delta P_H(t=t_0)$

State 1:  $P_H(t+1) = P_H(t)+\Delta P_H(t)$

State 2: $P_H(t+1) = P_H(t)+\Delta P_H(t)$
$e(t) = I(t) - I_T(t)$

If: $I(t) \leq I_0$  (T) $t_0=t$ go to: **Fine Loop**

(F)

$\Delta P_C=\Delta P_C/2$ return to: **Start 1**

While: $P_H(t) < P_{MAX}$

If: $[e(t) - e(t-1) \leq 0]$

(T)   (T)

(T)   (F)   (T)

$\Delta P_H(t) = +\Delta P_C$   If: $P_H(t) < P_{MIN}$   If: $e(t) \leq 0$ & $e(t-1) \leq 0$ ? → $I_T(t) = I(t)$

(F)   (F)

return to: **State 1**   $\Delta P_H(t) = -\Delta P_C$   $\Delta P_H(t+1) = -\Delta P_H(t)$ → return to: **State 2**
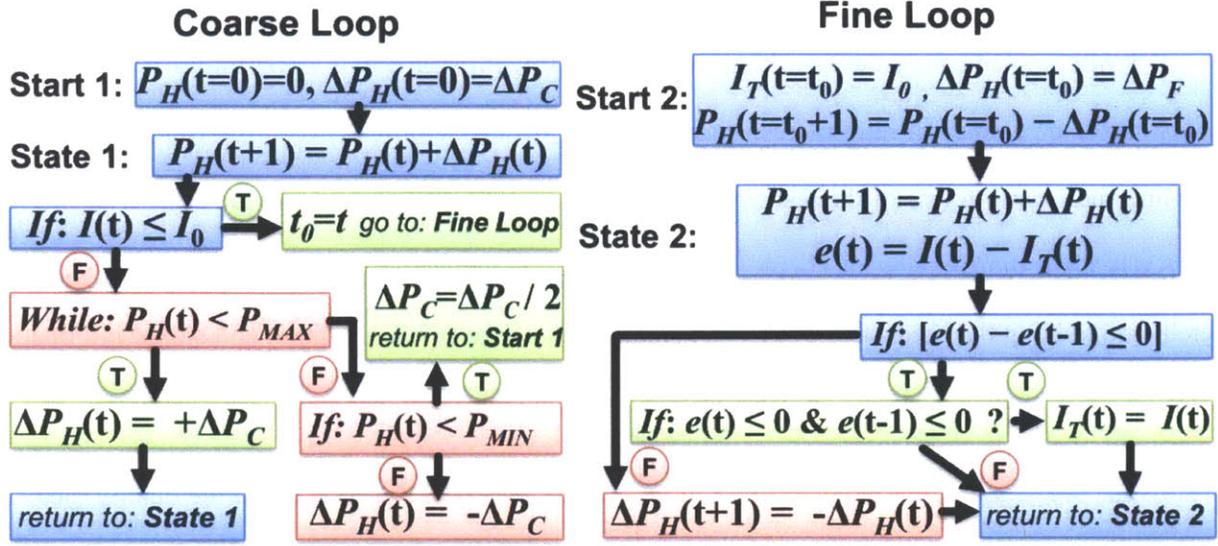
Figure 3. Coarse and fine loop AWR algortihm for thru port based AWR where $P_H(t)$ is real-time power dissipated in the heater, $\Delta P_H(t)$ is real-time power variation in the heater, $P_{MAX/MIN}$ is maximum/minimum heater power, $\Delta P_{C/F}$ is coarse/fine minimum power variation in the heater, $I(t)$ is real time output intensity, $I_0$ is the static threshold intensity (it can be converted into active threshold intensity (see section 6)), $e(t)$ is the error signal, $I_T(t)$ is the dynamic target intensity which is constantly updating for locking to the global minima. $T$ stands for true and $F$ for false for *if* statements. Drop port decision-making algorithm can be implemented by simply reversing the conditional statements.

Coarse loop is designed for rapid localization of the filter resonance around the laser frequency, by comparing with the threshold intensity. The threshold intensity can be set by measuring off-resonance intensity. If the laser power is fluctuating, then threshold intensity has to be varied dynamically in the algorithm which is implemented in section 3.5. Coarse loop sweeps the heater power and checks for the triggering threshold condition. Below and above the threshold intensity $(I_0)$ will be considered as around the resonance and off resonance, respectively. Fabry-Perot cavities due to reflections from the facets of the chip or internal reflections should be eliminated by appropriately selecting the threshold intensity. Microdisk resonators support higher order modes that corrupt the FSR with unwanted modes. Threshold intensity for a microdisk resonator required to be lower than the extinction ratio of high order modes. For practical purposes, minimum heater power, $P_{MIN}$, is set to 0mW. Maximum heater power, $P_{MAX}$, can be either set to maximum CMOS power level or the power level which the device breaks. Coarse loop algorithm is designed to sweep between these two extremes until the threshold is triggered by a

74

resonance. If the threshold intensity is not triggered between minimum and maximum heater power levels, then, heater power step will be divided by 2 to achieve finer tuning of the resonance. This allows the algorithm to locate the resonance around the laser line even with high-Q resonators. When the threshold triggered, a fine loop kicks in to achieve tight alignment.

Fine loop continuously searches for global minima below the threshold level and stabilizes at the resonance dip. Threshold intensity ($I_0$) is set as a target level intensity ($I_T$) for generating an initial error signal ($e(t)$). If the difference between two consecutive errors is below zero and both errors are not below zero, then, target intensity is updated and gets one step closer to the resonance. For other conditions, it searches until this condition is satisfied. The AWR loop automatically stabilizes when the target intensity reaches the actual resonance intensity. Since the actual resonance intensity is not known by the algorithm and can be dynamic, the integral based control loops such as proportional-integral-derivative (PID) or proportional-integral (PI) control loop will be unstable. If the device is calibrated, then PID or PI will give the best results. An adaptive proportional-derivative (PD) control is implemented to reach the target intensity. Every time the target intensity is surpassed with a lower intensity, it gets updated. Eventually the resonance dip will be equal to the target intensity which guarantees alignment between laser line and the resonance.

For a demultiplexer filter, AWR should be feedback with the average intensity at the photodetector instead of laser intensity and perform the same procedure as a multiplexer. Therefore, the same algorithm can be used for WDM multiplexer and demultiplexer. The demonstration in this chapter will focus on the multiplexer.

In a AWR implementation, the heater power change that corresponds to single bit accuracy at the receiver determines the stability. Minimum power step can be altered and the speed of the AWR can be enhanced at the expense of stability. Detailed analysis about this tradeoff is performed in Section 3.4.

75

## 3.3 Thermal and Laser Frequency Drifts

AWR algorithm is implemented using an external FPGA that controls the integrated heater voltage with 10-bit accuracy and collects feedback from an external DC-coupled detector with a 10MHz 3dB-bandwidth. AWR loop is initially stabilized in <5ms. Real-time photodetector data is stored for ~10 seconds at every ~30 seconds while heating the chip and cooling down. On-chip thermal drift is mimicked by heating or cooling the photonic chip with an external TEC under the chip. Real time global chip temperature of the chip is recorded using an external thermistor, attached to the chip. Chip is globally heated with the TEC from 25 to $75^0$C in 20 minutes with $5^0$C steps, stayed at $75^0$C for 5 minutes and cooled down from 75 to $25^0$C in 10 minutes with $5^0$C steps depicted in Fig. 4(a). TEC stabilizes using an optimized PID loop which oscillates within $\pm0.1^0$C from the target temperature at a low frequency of ~0.2Hz.

The experimental result under the thermal drift is shown in Fig. 4a. The internal temperature of microring is kept constant and transmission is stabilized when the AWR loop is on for more than 18 minutes and chip temperature raised from $25^0$C to $70^0$C (Fig. 4(a)). After 18 minutes, the global temperature rose above microring internal temperature (>$70^0$C) which requires shifting the microring resonance by more than one FSR. This was not possible with the given microring resonator. However, when the global chip temperature constantly cools down below $70^0$C, AWR loop can again align the resonance to the laser after $26^{th}$ minute (Fig. 4(a)). AWR loop compensated the dynamic temperature fluctuations for heating and cooling chip. Therefore, AWR loop performed with ARM resonator have demonstrated temperature fluctuation as much as $\pm17.5^0$C which corresponds to a AWR for a frequency mismatch of ~ $\pm175$GHz. The external CW laser used in the experiments is stable and drifts less than $\pm50$kHz over nominal frequency.

In another experiment, laser drift is mimicked by automatically tuning the external CW laser line in a linear fashion. An external TEC is used to stabilize the global chip temperature to a static $25^0$C within $\pm0.1^0$C error. The global chip temperature is stabilized to provide a controlled environment for the laser drift experiment. Laser is initially red shifted by 1.5THz in a second, waited for a second and then blue

76

shifted by 1.5THz in a second which is illustrated in Fig. 4(b) while AWR loop was on. While laser frequency is drifting, internal microring temperature is controlled by the AWR loop to align the drifting laser line on to microring resonance. From Fig. 2a, we know that the extinction ratio of the resonator is dependent on wavelength. When the local temperature is altered, the extinction ratio of the microring filter response is decreasing and increasing by red and blue shifting of the microring resonance, respectively. The extinction ratio of the reference measurements are 19.9 and 16.7 dB for zero and maximum heater power, respectively. The experimental results, shown in Fig. 4(b), are in good agreement with the reference measurements. This is the first demonstration of AWR over a frequency drift/offset of 1.5THz and in ~5ms (Fig. 4(b)-inset).
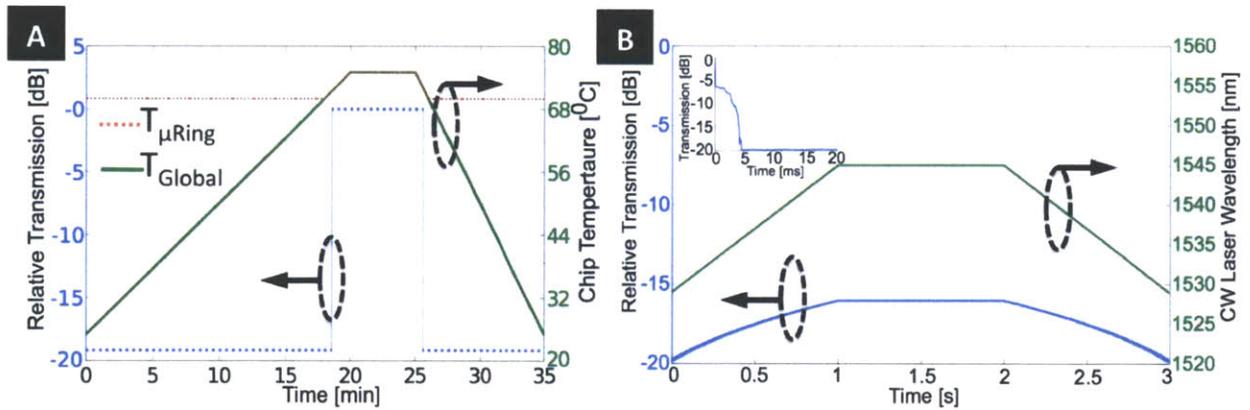


Figure 4. (a) AWR loop demonstration while thermally drifting the microring resonator by an external TEC. Internal microring temperature and global temperature of the chip is also shown, (b) Experimental measurement results of the AWR loop while the tunable CW laser line is red and blue shifting. Inset is showing the speed of the recovery which is around ~5ms.

## 3.4 AWR Speed and Stability Optimization

The proposed AWR technique in Section 3 is not cognizant of the actual on-resonance intensity or optimal target intensity. Therefore, optimizing the underlying control loop is device specific. In practical systems, the AWR control loop bandwidth is limited with integrated heater time constant or the analog to digital converter (ADC). System noise will be captured by the loop bandwidth after AWR is stabilized. Furthermore, minimum detectable noise by the loop will be limited by the minimum heater power step in the fine loop (Fig. 2). The AWR stability will be enhanced by diminishing heater power step. However,

alignment will take more time for smaller heater power step. AWR loop can be customized for different applications and given specifications of speed and stability.

To quantify the tradeoff between AWR speed and stability, CW laser line is set to ~1528.3nm and the microring resonance had a frequency offset of 30GHz to the laser line but this information is not used in the AWR loop. The offset is chosen to be particularly small to show the effect of speed and stability more clearly. The minimum heater power step is set to minimum detectable limit that is dictated by 10-bit ADC at sampling rate of 100KSa/s. The AWR loop performance is compared when the heater power step is set to 1, 2, 4, 8, 16 and 32 times of the minimum heater power step. Real-time heater power is recorded through the experiments. Thru port intensity of the ARM is measured with an external photodetector simultaneously. The characterization data shown in Fig. 2 (b) is used to correlate the frequency shift of the microring resonator to the real-time intensity and heater power. Correlated frequency shifts for different heater power step settings are shown in Fig. 5(a). By increasing the heater power step, the settling time of the AWR loop is diminished from ~4.3ms to ~200µs. The AWR has potential to speed up more with faster integrated heater and ADC.
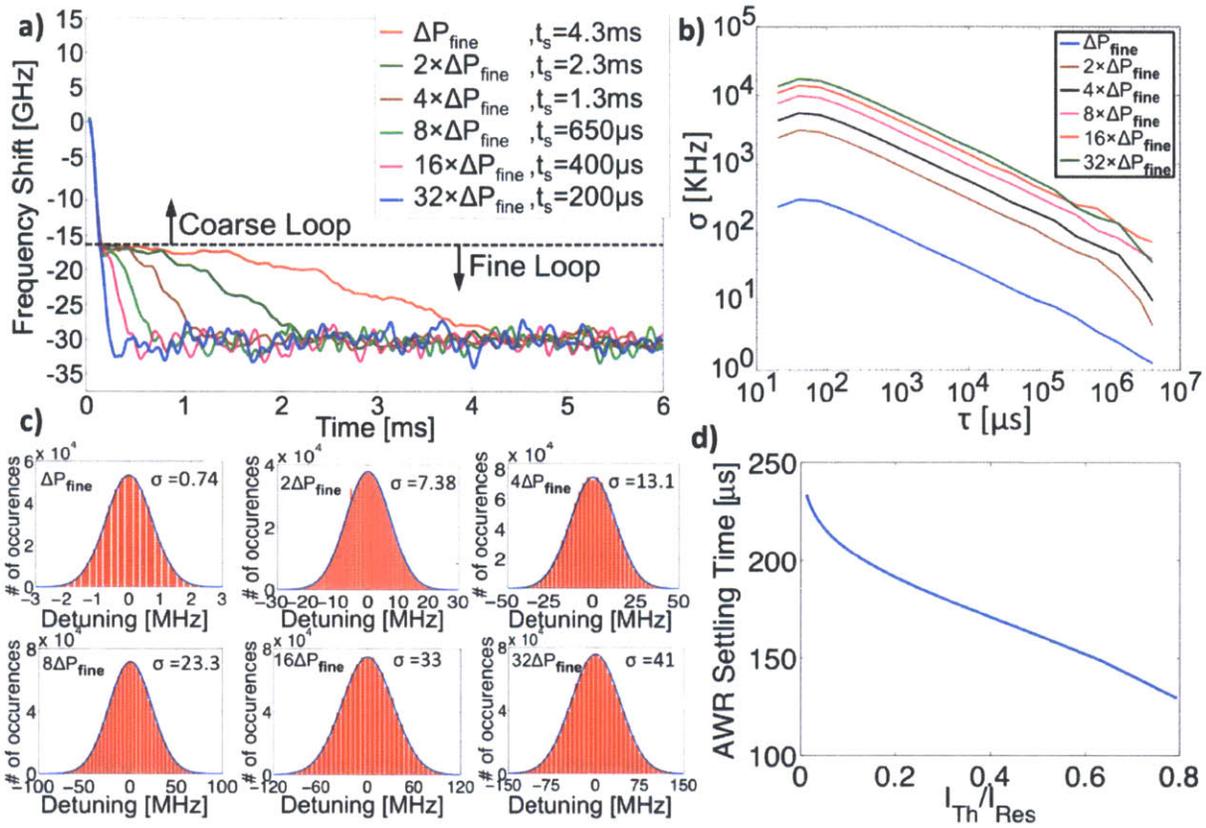
Figure 5. (a) AWR loop speed analysis with respect to heater power step settings. The loop is stabilized for each heater power setting. Settling time (t_S) of the each setting is diminished by increased heater power step. (b) Overlapping Allan variance analysis for each heater power step setting. 10s of real-time data after AWR is stabilized is used. (c) Histogram of the frequency stability for each heater power step setting. 10s of real-time data after AWR is stabilized is used. (d) AWR settling time dependence on the threshold intensity to the resonance intensity is depicted. Maximum heater power setting is chosen for the fine loop.

AWR control loop will expect to become less stable with increasing minimum heater power setting. To quantitatively understand the effects, histogram of the real-time data is fitted to the normal distribution and overlapping Allan variance, a well-known technique for noise and stability analysis, is performed [17-18]. The loop is observed after it settles to the on-resonance intensity for 10 seconds for each heater power step setting. Normal distribution and Allan variance sigma is calculated using a custom MATLAB program and the results are shown in Fig. 5 (b-c). Stability is raised with the smaller heater power steps as expected. From the most stable to least, a normal distribution sigma of 0.74, 7.38, 13.1, 23.3, 33, 41 MHz around the resonance is observed. If the ultra-high stability is not required, AWR speed can be increased

significantly.

AWR loop can further speed up if the threshold intensity in the coarse loop is placed closer to the on-resonance laser intensity. As the threshold gets closer to the on-resonance intensity the AWR loop will spend more time in coarse loop than fine loop which will speed up the recovery. In order to demonstrate the effect, the largest heater power step setting is chosen and AWR loop is performed for the different threshold intensity levels. Results are shown in Fig 5(d). Settling time is reduced from ~240us to ~130us. Long term-stability of the overall system did not change during the experiments. By adjusting the PD parameters of the loop and altering the threshold intensity the settling time is vanished by 33 times from ~4.3ms to ~130μs. Therefore, the loop offers any optimization between high stability (<1MHz) or high speed (~130μs) operation.

## 3.5 Laser intensity dependence

Insertion loss and intensity on each bus waveguide can be different on a real system. Additionally coupling efficiency of on-chip couplers is wavelength dependent and each wavelength channel will have different power on the bus waveguide. Therefore, AWR loop needs to be independent of the laser intensity. In order to perform this task, fine loop on Section 3 will stay same and coarse loop threshold intensity will be updated with dynamic control. Initial threshold intensity is set to upper bound of the laser intensity (+10dBm) for the drop port and minimum detectable intensity with the current detector (-45dBm) for thru port. When the threshold intensity is not triggered by the loop, threshold intensity is divided and multiplied by 2 for the drop and thru port, respectively. The advanced coarse-loop algorithm is shown in Fig. 6(a). Advanced AWR loop is demonstrated when the laser intensity on the waveguide is set to -2dBm, -9dBm and -16dBm which is not known by the loop. Real-time intensity data is shown in Fig. 6(b). The largest heater power step is used and the settling time is varied due to dynamic threshold intensity. Another way to control the threshold intensity dynamically is to record off-resonance intensity automatically and set the threshold intensity accordingly. However, any mechanical or thermal instability

in the experiments lead to misleading judgments about off-resonance intensity and it is not used in this experiment.
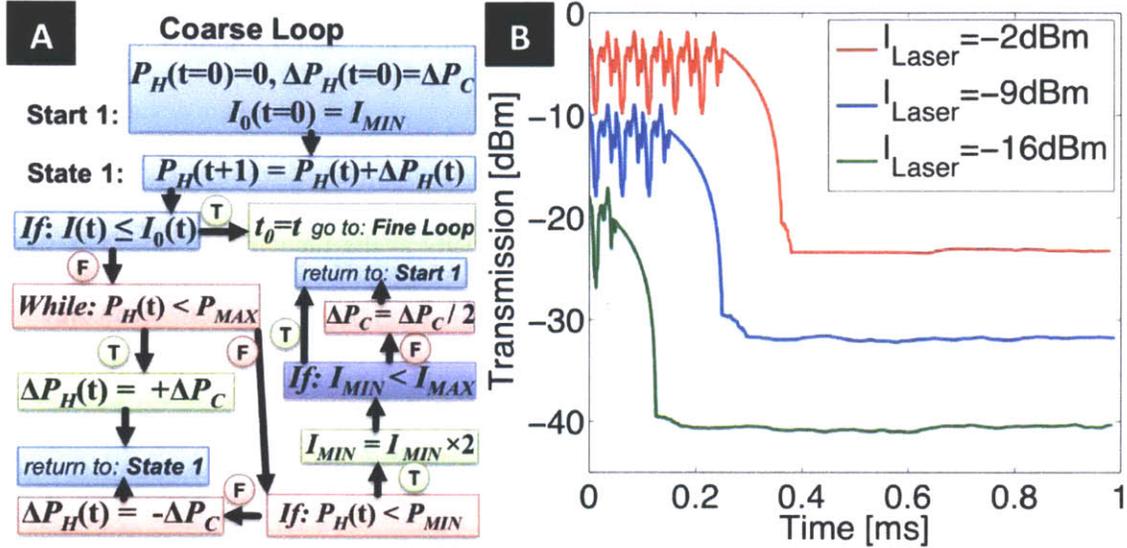


Figure 6. (a) Advanced coarse loop decision-making algortihm for thru port based AWR where $P_H(t)$ is real-time power dissipated in the heater, $\Delta P_H(t)$ is real-time power variation in the heater, $P_{MAX/MIN}$ is maximum/minimum heater power, $\Delta P_C$ is coarse minimum power variation in the heater, $I(t)$ is real time output intensity, $I_0(t)$ is the dynamic threshold intensity, $I_{MAX/MIN}$ is maximum/minimum laser intensity in the bus waveguide $T$ stands for true and $F$ for false for *if* statements. Drop port decision-making algorithm can be implemented by simply reversing the conditional statements. (b) AWR demonstration where the laser intensity is varied from -2 dBm to -16 dBm.

## 3.6 Conclusion

In this chapter, we implemented an AWR algorithm on a WDM multiplexer microring. The AWR is tested under thermal and laser drifts mimicking the possible extreme conditions. Thermal drift is emulated by an external TEC. Cooling and heating cycles are both recovered and stabilized over $\pm 17.5^0$K temperature differences and more than 18 minutes with settling time of ~5ms. Laser drifts are resembled by tuning the CW external laser. AWR is performed with a frequency offset of ~1.5THz with settling of time of only ~5ms. Red and blue shifting of the laser is perfectly captured and reacted real-time by the AWR.

81

The AWR speed is enhanced using parameter optimization in the algorithm. The PD control parameters are modified by heater power step settings and the threshold intensity is manually modified to observe the effect on speed of the recovery. The settling time is decreased from ~4.3ms to 130μs at a sampling rate of 100KSa/s. The histogram and overlapping Allan deviation of the frequency stability is investigated for each heater power step setting. Both the histogram and the Allan deviation results are correlated with speed.

The AWR loop has updated for variable laser intensity at the input waveguide. The threshold intensity is modified to be a dynamic parameter. This parameter is swept using an intelligent algorithm to align the laser line to the microring resonance. Laser intensity varied from -2 to -16 dBm and the settling time of the loop is reduced from ~380μs to ~180μs, respectively. In all experiments, the laser line is recovered by the updated loop with no *a priori* information.

The AWR technique is demonstrated with an ARM resonator under various extreme conditions with high speed and stability. Every development in the heater or the ADC speed will lead to faster and more accurate recovery with this technique. The AWR can be implemented using CMOS electronics and is readily scalable in a CMOS and photonics integrated platform for its simplicity and recovery speed.

## 3.7 References

[1] W. Zortman, D. Trotter, and M. Watts, "Silicon photonics manufacturing," Opt. Express 18, 23598-23607 (2010).

[2] J. S. Orcutt, A. Khilo, C. W. Holzwarth, M. A. Popović, H. Li, J. Sun, T. Bonifield, R. Hollingsworth, F. X. Kärtner, and H. I. Smith, "Nanophotonic integration in state-of-the-art CMOS foundries," *Opt. Express* **19**, 2335–2346 (2012).

[3] M. W. Riley, J. Warnock, and D. Wendel, "Cell broadband engine processor: Design and implementation," *IBM Journal of Research and Development* **51**, 545–557 (2007).

[4] J. A. McCaulley, V. M. Donnelly, M. Vernon, and I. Taha, "Temperature dependence of the near-infrared refractive index of silicon, gallium arsenide, and indium phosphide," *Physical Review B* **49**, 7408 (1994).

[5] G. Li, X. Zheng, J. Yao, H. Thacker, I. Shubin, Y. Luo, K. Raj, J. E. Cunningham, and A. V. Krishnamoorthy, "25Gb/s 1V-driving CMOS ring modulator with integrated thermal tuning," *Opt. Express* **19,** 20435–20443 (2011).

[6] G. Li, X. Zheng, H. Thacker, J. Yao, Y. Luo, I. Shubin, K. Raj, J. E. Cunningham, and A. V. Krishnamoorthy, "40 Gb/s thermally tunable CMOS ring modulator," Proc. International Conference on Group IV Photonics (GFP), 1–3 (2012).

[7] W. Zortman *et al.*, "Integrated CMOS Compatible Low Power 10Gbps Silicon Photonic Heater Modulator," *OFC*, 2012.

[8] M. R. Watts, "Adiabatic microring resonators," Opt. Lett. 35, 3231-3233 (2010).

[9] M. R. Watts, W. A. Zortman, D. C. Trotter, G. N. Nielson, D. L. Luck, and R. W. Young, "Adiabatic resonant microrings (ARMs) with directly integrated thermal microphotonics," Proc. Conference on Lasers and Electro-Optics (CLEO), CPDB10 (2009).

[10] C. T. DeRose, M. R. Watts, D. C. Trotter, D. L. Luck, G. N. Nielson, and R. W. Young, "Silicon microring modulator with integrated heater and temperature sensor for thermal control," Conference on Lasers and Electro-Optics (CLEO), (2010).

[11] C. Qiu, J. Shu, Z. Li, X. Zhang, and Q. Xu, "Wavelength tracking with thermally controlled silicon resonators," *Opt. Express* **19**, 5143–5148 (2011)

[12] K. Padmaraju, J. Chan, L. Chen, and M. Lipson, "Dynamic stabilization of a microring modulator under thermal perturbation," Optical Fiber Communication Conference (OFC), OW4F.2 (2012).

[13] Padmaraju, K., Chan, J., Chen, L., Lipson, M. and Bergman, K., "Thermal stabilization of a microring modulator using feedback control", Opt. Express, Vol. 20, No. 27, 17 Dec. 2012

[14] M. R. Watts, D. C. Trotter, and R. W. Young, "Maximally confined high-speed second-order silicon microdisk switches," National Fiber Optic Engineers Conference (NFOEC), PDP14 (2008).

[15] A. L. Lentine, W. A. Zortman, and D. C. Trotter, "Active wavelength control of silicon microphotonic resonant modulators," Optical Interconnects Conference (OI Conference), (2012).

[16] Zortman, W.; Lentine, A.; Trotter, D.; Watts, M.; , "Bit error rate monitoring for active wavelength control of silicon microphotonic resonant modulators," *Micro, IEEE* , vol.PP, no.99, pp.1, 2013

[17] Fabian Czerwinski, Andrew C. Richardson, and Lene B. Oddershede, "Quantifying Noise in Optical Tweezers by Allan Variance," *Opt. Express* **17**, 13255–13269 (2009).

[18] W. J. Riley, "Handbook of Frequency Stability Analysis", (2008).

# 4 Advanced Automated Wavelength Recovery

In chapter 1, we have introduced automated wavelength recovery (AWR) architecture. This architecture is designed to implement the AWR loop with minimum change to WDM link to offer the most general solution. However, the most general solution might not be the most efficient or stable one. Here, we will focus on a new architecture that is based on the phase response of the resonators instead of intensity information. In a resonator, the phase response is hidden in the thru and the drop port response. Therefore, in order to obtain phase response of a resonator, a Mach-Zender interferometer (MZI) [1-2] is required. The MZI interferometer should be passive, low-power to minimize electrical power consumption, compact to allow large scale integration, and broadband to enable C- and L-Band operation. The common MZI structures are occupying >500μm in length and formed with two 3-dB couplers that interferes two identical arms with 3-dB intensity. However, in this work we require a MZI in tens of micrometers length and use minimum optical intensity.

The phase response is less dependent to extinction ratio and quality factor of a resonator, thus it will provide high performance even with wafer/process variations. More importantly, the phase response of a resonator resembles the edge shape similar to the output of a Pound-Drever Hall (PDH) loop [3], which is widely used for stabilizing the frequency of high-Q lasers.

## 4.1 Integrated Amplitude to Phase Converter Theory

The proposed MZI is composed of two arbitrary couplers that interfere the response of resonator and the input signal. An exemplary design of such a MZI is illustrated in Fig. 1.
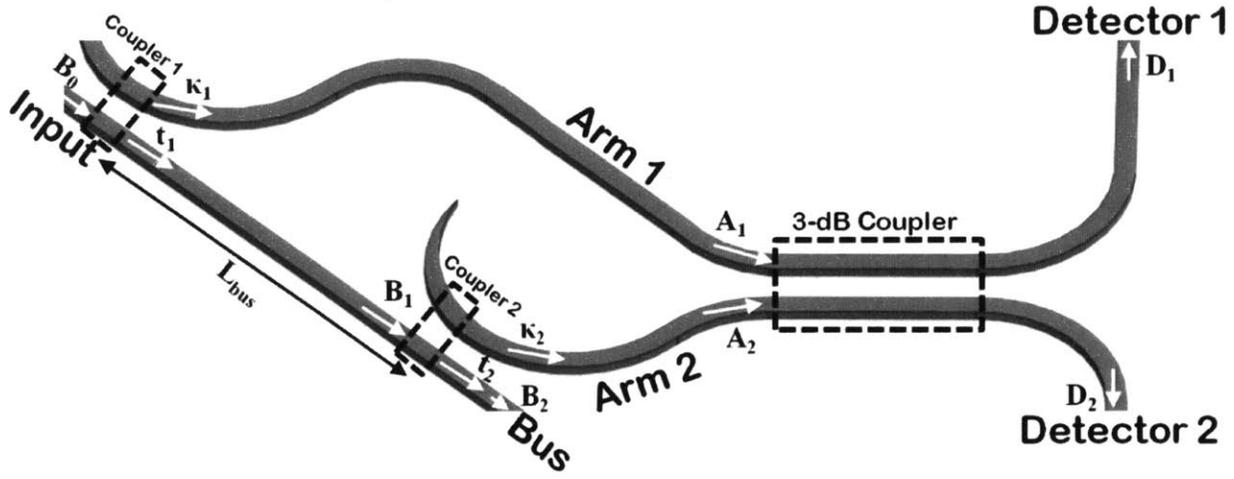
Figure 1. The MZI structure, composed of 2 directional couplers and a 3dB-coupler, is proposed to convert amplitude to phase response.

A directional coupler is envisioned to achieve arbitrary coupling to each arm of the MZI. To achieve low loss and compact coupler, a straight to bend coupler is placed. The bend radius of the bend can be as small as 1.5 to 3μm. If the space is not a constraint, the adiabatic couplers can achieve large bandwidth [4].Transfer matrix method is a widely used for modeling photonic resonators and devices [5, 6].

The amplitude coupling and transmission coefficient of the coupler # is denoted by $\kappa_\#$ and $t_\#$, respectively. For a lossless coupler, power conservation will be satisfied with;

$|t_\#|^2 + |\kappa_\#|^2 = 1$

The integrated Silicon directional couplers can achieve almost lossless operation. For a lossy coupler with an insertion loss of $s_\#$, then the power conservation will be satisfied with the following equation,

$|t_\#|^2 + |\kappa_\#|^2 + |s_\#|^2 = 1$

The amplitude at the 3dB-coupler input is denoted by $A_\#$. If the input amplitude is $B_0$, the amplitude in arm 1 is given by,

$A_1 = B_0 \times \kappa_1 \times e^{j\Theta_1}$

where, $\Theta_1$ is the phase accumulated due to optical path delay in arm 1 with respect to the input reference phase. Accumulated phase can be calculated in general as the following,

$\Theta_\# = 2\pi \times (n_g \times L_\#)/\lambda$

where, $\lambda$ is the operation wavelength and $n_g$ is the group index given by $n_g = n_{eff} - \lambda \times dn_{eff}/d\lambda$. The optical path delay in arm 1,

$\Theta_1 = 2\pi \times (n_g \times L_1)/\lambda + \Theta_{coupling} - \Theta_{reference}$

where, $\Theta_{coupling}$ and $\Theta_{reference}$ is the coupling induced phase shift and reference phase, respectively and $L_1$ is the path length in Arm 1. Coupling induced phase shift can result significant frequency shift for a resonator [7]. The amplitude before the second coupler is the following,

$B_1 = B_0 \times t_1 \times e^{j\Theta_{bus}}$

where, $\Theta_{bus}$ is the optical path delay in the bus waveguide and given by $\Theta_{bus} = 2\pi \times (n_g \times L_{bus})/\lambda$. Then, the amplitude in arm 2 is,

$A_2 = B_0 \times t_1 \times \kappa_2 \times e^{j\Theta_2}$

and the optical phase delay in arm 2 is given by,

$\Theta_2 = 2\pi \times (n_g \times (L_2 + L_{bus}))/\lambda + \Theta_{coupling} - \Theta_{reference}$

Then, the phase difference between the arms is,

$\Theta_{21} = \Theta_2 - \Theta_1 = 2\pi \times (n_g \times (L_1 - L_2 + L_{bus}))/\lambda$

A wavelength independent directional coupler has a transfer matrix as the following,

$$M = \begin{bmatrix} \cos(\theta) & j\sin(\theta) \\ j\sin(\theta) & \cos(\theta) \end{bmatrix}$$

For a special case at $\Theta = \pi/4$, it will represent a 3dB-coupler which is,

$$M_{3dB} = \begin{bmatrix} \cos(\pi/4) & j\sin(\pi/4) \\ j\sin(\pi/4) & \cos(\pi/4) \end{bmatrix}$$

The output arm 1 and 2 of the MZI, called as $D_1$ and $D_2$, used for detection the phase. The output of the MZI can be calculated as the following,

$$\begin{bmatrix} D_1 \\ D_2 \end{bmatrix} = \begin{bmatrix} \cos(\pi/4) & j\sin(\pi/4) \\ j\sin(\pi/4) & \cos(\pi/4) \end{bmatrix} \begin{bmatrix} A_1 \\ A_2 \end{bmatrix}$$

and the power at detector 1 and 2 is,

$$D_{1,2} = \left( \frac{A_{1,2}}{\sqrt{2}} + j\frac{A_{2,1}}{\sqrt{2}} \right)^2 = \frac{A_{1,2}^2 - A_{2,1}^2}{2} + jA_{2,1}A_{1,2}$$

We have explained the amplitude and phase relation between two output arms above. However, we still need to design it to satisfy a high contrast MZI output. The amplitude in both arms has to be equal, thereby satisfy the following,

$|A_2| = |A_1|$, => $t_1 \times \kappa_2 = \kappa_1$

A special case for $t_1 = 0.707$, $\kappa_1 = 0.707$, $\kappa_2 = 1$, the proposed MZI represents the conventional MZI response. Since we want to just observe the phase response with low intensity drop, we can consider the case with less than 5% coupled to each arm ($|\kappa_1|^2 < 0.05$). The table 1 shows the coefficients required to achieve high contrast MZI. If the first coupler power split is less than 1 percent ($|\kappa_1|^2 < 0.01$), then the second coupler can be identical with first coupler and minimize the complexity of the design.

| $|\kappa_1|^2$ | $\kappa_1$ | $\kappa_2$ | $t_1$ |
|---|---|---|---|
| 0.05 | 0.224 | 0.229 | 0.9747 |
| 0.04 | 0.200 | 0.204 | 0.9798 |
| 0.03 | 0.173 | 0.176 | 0.9849 |
| 0.02 | 0.141 | 0.143 | 0.9899 |
| 0.01 | 0.100 | 0.101 | 0.9950 |
| 0.005 | 0.071 | 0.071 | 0.9975 |
| 0.0025 | 0.050 | 0.050 | 0.9987 |
| 0.00125 | 0.035 | 0.035 | 0.9994 |
| 0.000625 | 0.025 | 0.025 | 0.9997 |

Table 1. The coupling coefficients for high contrast MZI design

The normalized detector 1 and 2 output as a function of phase difference between each arm is illustrated in Figure 2. The output is normalized to $2|\kappa_1|^2$.
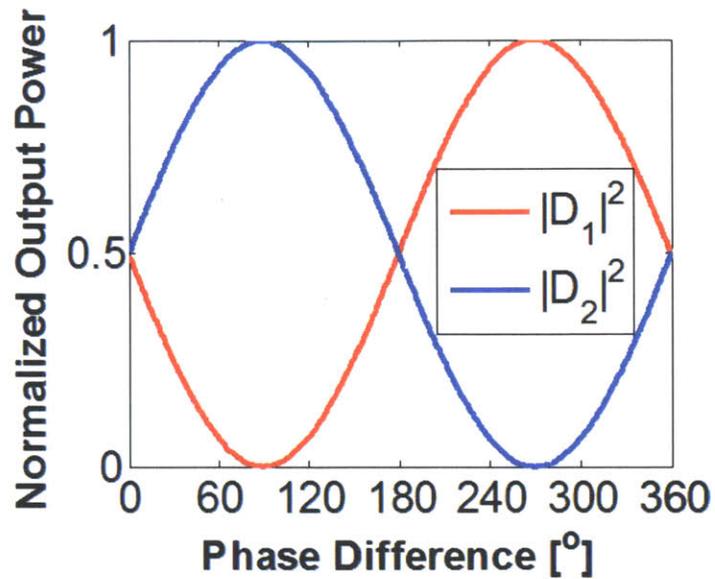
Figure 2. The proposed MZI structure normalized output as a function of phase difference between the MZI arms.

## 4.2 Integrated Amplitude to Phase Converter Design

In order to design the integrated Amplitude to Phase Converter MZI, we need to design the arbitrary directional couplers, the 3dB coupler and minimize the loss through the bends. The structure will be fully designed and simulated in 3D with custom Finite Difference Time Domain (FDTD) code (Fig. 3). The arbitrary directional couplers are designed for minimum bend radii. Therefore, the silicon waveguide is designed to maximize confinement and maintain single mode operation from 2-μm to 1.6-μm wavelength range.
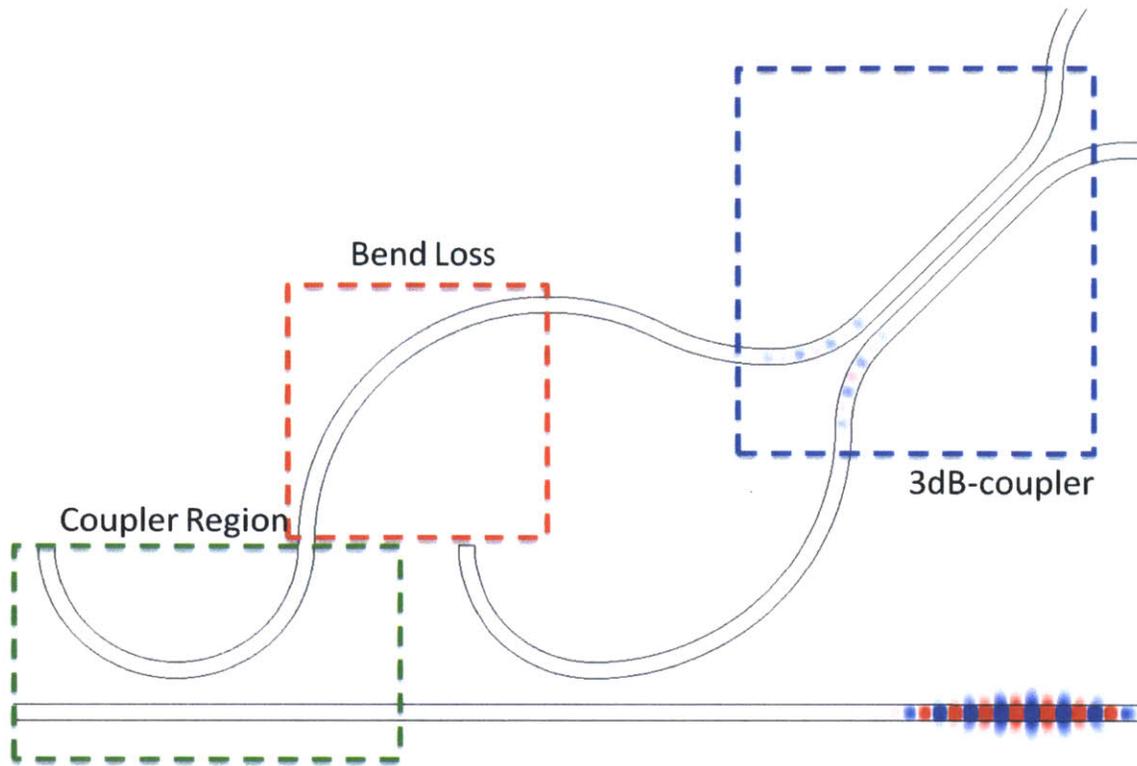
Figure 3. The initial MZI design with full-3D FDTD simulation.

### 4.2.1 Arbitary Coupler Design

The coupler region is designed as a straight to bend coupler to achieve the most compact design. The simulation is performed by exciting the TE mode of the input waveguide with a Gaussian amplitude distribution in time and placing flux monitors at the coupled port and thru port of the device, as illustrated in Fig. 4. The gap between the bend and straight waveguide is adjusted from 120 to 200nm for optimizing the coupling coefficient. The bend radius and width is kept at 3μm and 400nm, respectively. The thickness of the silicon waveguide is 220nm. The flux monitors are overlapped with the corresponding fundamental modes. The loss can be determined from the total overlap at the input, the drop and the coupled port (Fig. 5). The results are obtained in a broadband spectrum by appropriately adjusting the length of Gaussian excitation pulse.
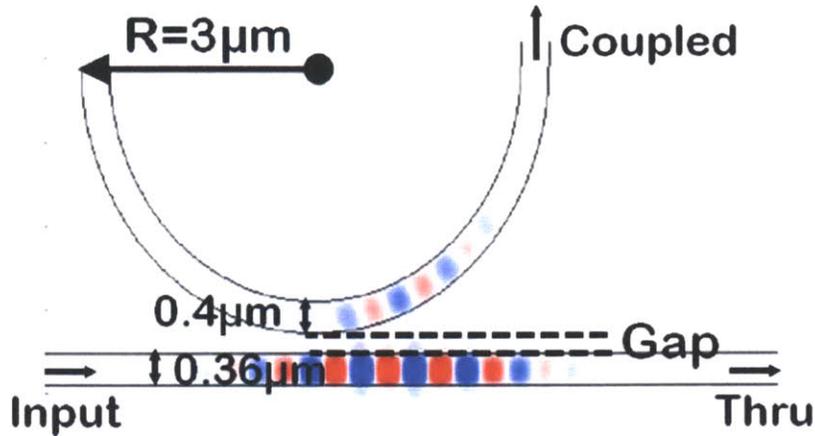
Figure 4. FDTD simulation of the straight to bend coupling. Size of each photonic part and photonic ports is shown on the figure.
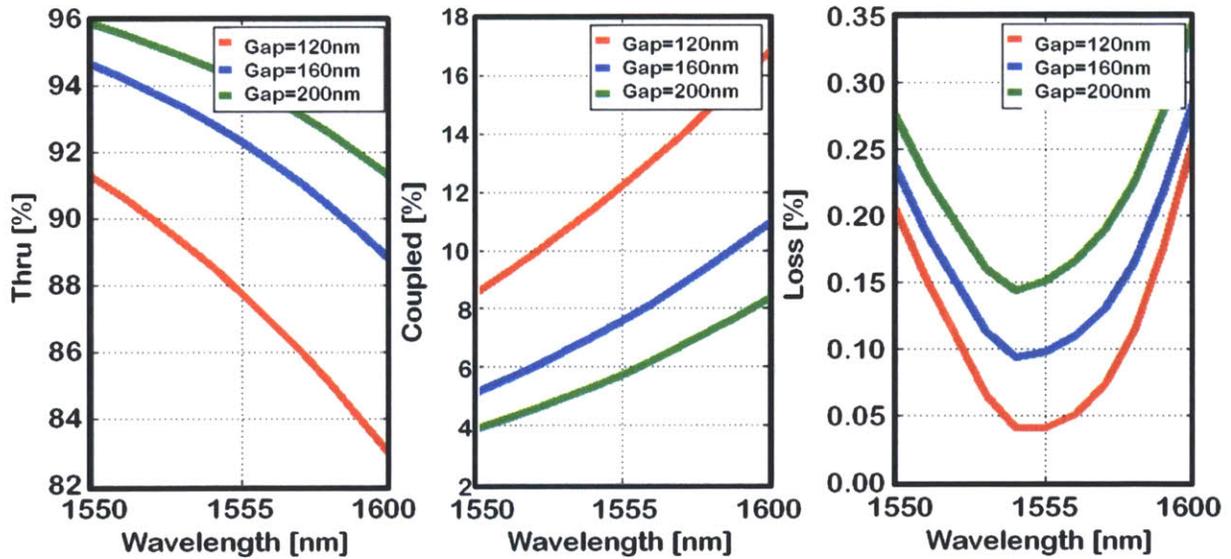


Figure 5. FDTD simulation results for Thru, Coupled and Loss power of the straight to bend coupling as a function of gap and wavelength.

The wavelength dependence of straight to bend coupler is ~0.03dB/nm, which is originating from confinement scaling of the bus and bend waveguide. If we consider a resonator, that has a free spectral range of 30nm, it will result with 0.9dB coupling dependence. This is acceptable for our application. The loss is optimized by varying the width of the bus waveguide and as well as varying the gap (Fig. 6). The width of the bus waveguide is varied from 360 to 440nm and the gap is varied from 120 to 200nm. The

bend radius and width is kept at 3µm and 400nm, respectively and the thickness of the silicon waveguide is 220nm. The coupled and loss power measured from corresponding flux monitors results at 1550nm (Fig. 7). The loss is minimized for the 360nm bus waveguide width.
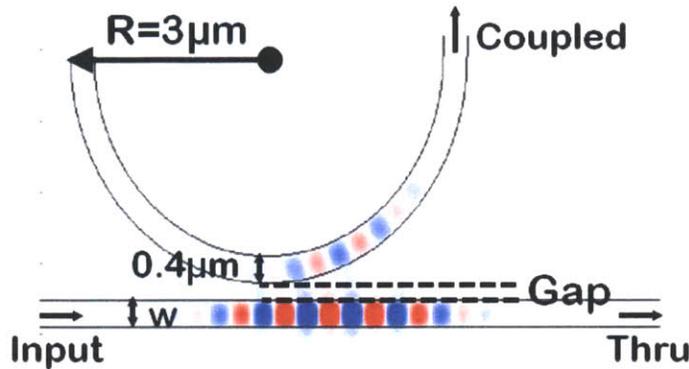


Figure 6. FDTD simulation of the straight to bend coupling for the loss optimization based on bus width and gap.
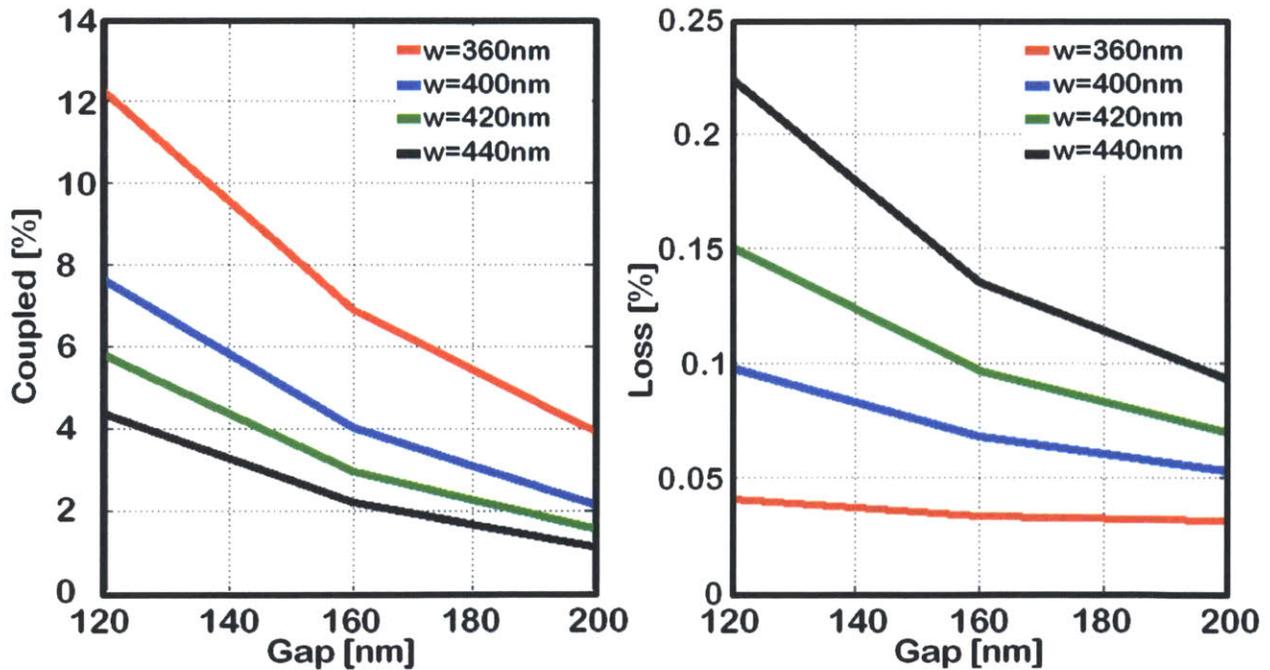


Figure 7. FDTD simulation results for Coupled and Loss power of the straight to bend coupling as a function of gap and bus width.

## 4.2.2 The 3dB Coupler Design

The 3dB Coupler is designed by utilizing mode beating between the symmetric and antisymmetric modes of two identical core waveguides placed next to each other (Fig. 8, left). This was an inherently wavelength dependent 3dB coupler and it will be updated in the demonstrated device with an adiabatically tapered 3dB coupler. The effective index of the TE fundamental antisymmetric and symmetric modes of the combined structure are calculated with a custom finite difference mode solver. Single arm excitation can be decomposed into asymmetric and symmetric modes of the structure. Therefore, single arm excites both modes with the same phase at the input of 3dB coupler. As the light

$$\begin{bmatrix} 1 \\ 0 \end{bmatrix} = \begin{bmatrix} 1/2 \\ 1/2 \end{bmatrix} + \begin{bmatrix} 1/2 \\ -1/2 \end{bmatrix}$$

Single Arm    Symmetric    Antisymmetric
Excitation     Mode       Mode

propagates the symmetric and antisymetric modes will have a wavelength and length dependent phase shift which is,

$$\Theta_{shift} = \Theta_{AS} - \Theta_S = 2\pi \times (n_{AS} - n_S) \times L/\lambda$$

where, subscript S and AS denotes symmetric and antisymmetric, respectively. When the phase shift between the antisymmetric and symmetric mode is equal to $\pm\pi/2 + 2\pi N$ (N is an integer), the power at each arm will be the following,

$$\left( \begin{bmatrix} 1/2 \\ 1/2 \end{bmatrix} + \begin{bmatrix} \pm j/2 \\ \mp j/2 \end{bmatrix} \right)^2 = \begin{bmatrix} \pm j/2 \\ \mp j/2 \end{bmatrix}$$

This is the 3dB point but the phase shift is wavelength dependent. If the phase shift between the arms is equal to $\pm\pi + 2\pi N$, then the input power is transferred to the secondary arm.

The 3dB coupler can be designed directly with a modesolver but the coupling region of the coupler will change the initial excitation conditions. Therefore, a proper FDTD-3D simulation is required (Fig. 8, right). The 3dB coupler length is determined to be ~5μm.

92
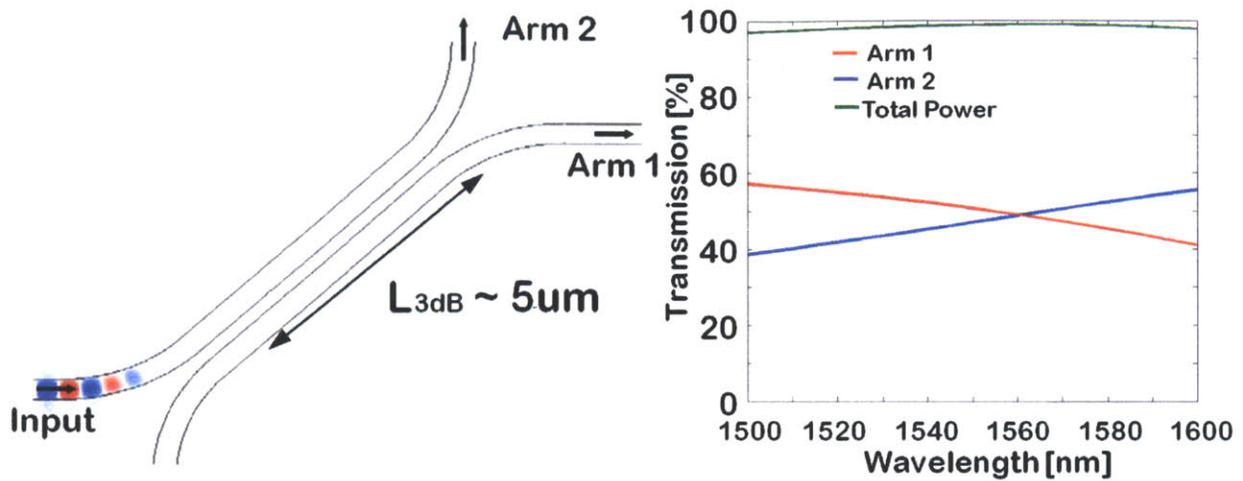
Figure 8. FDTD simulation of the 3dB-coupler, the 3dB length is initially guessed by the analytical calculation and then optimized in the simulation including the couplers (left), the arm power splitting and loss of the 3dB coupler for the simulated 3dB-coupler(right).

This design is wavelength dependent (~0.015dB/nm or 0.45dB for 30nm wavelength span) and it is prone to fabrication errors. The 3dB coupler is simulated against fabrication errors. The results for ±15nm thickness and ±10nm gap variation are shown in Fig. 9, left. Additionally, the results for ±15nm thickness and ±10nm asymmetric waveguide width variation are shown in Fig. 10, right. The FDTD-3D simulations are evaluated for the change in 3dB coupling point.
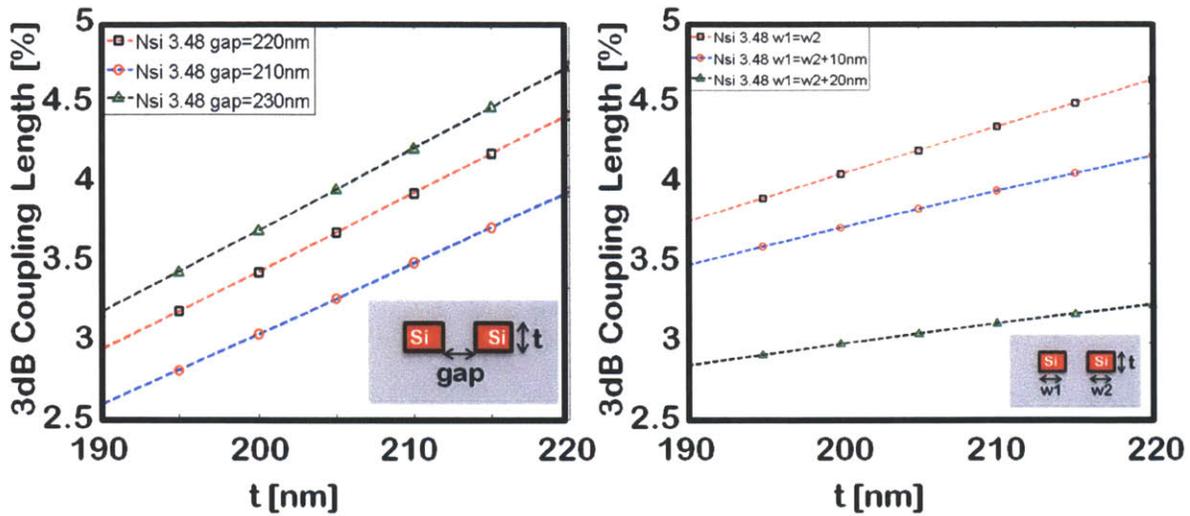
Figure 9. FDTD simulation of the 3dB-coupler with respect to thickness and gap variations (left), FDTD simulation of the 3dB-coupler with respect to thickness and asymmetric waveguide width variations (right). Each point represents a FDTD-3D simulation.

## 4.2.3 FDTD-3D Simulation of the Amplitude to Phase Converter

After optimization of each part of the proposed Amplitude to Phase Converter (MZI), the MZI is simulated as a whole (Fig.10, left). The arm outputs have achieved equal power splitting but wavelength dependence deteriorates the system performance (Fig. 10, right). Wavelength dependence can be eliminated if a broadband 3dB-coupler can be designed.
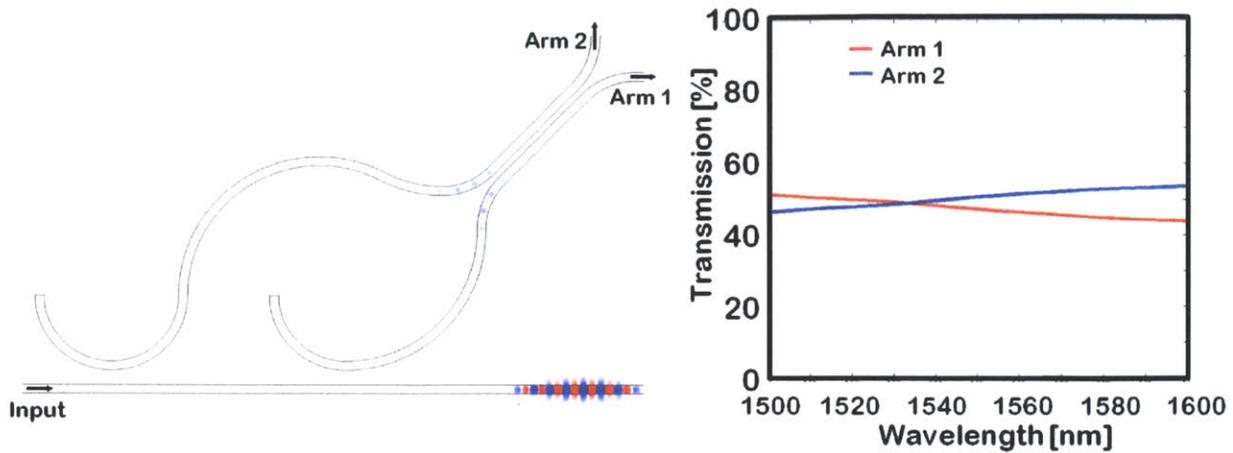
Figure 10. FDTD simulation of the proposed amplitude to phase converter (left), FDTD simulation results of the full structure normalized to total coupled power.

## 4.3 Advanced AWR with Amplitude to Phase Converter

The amplitude to phase converter is designed to convert the amplitude response of a resonator into phase response. In this section, we will discuss the implementation and a demonstration of such integration. The resonator will be placed between the coupler 1 and 2 to dynamically change the phase of arm 2, while maintaining the phase of arm 1. It is illustrated in Fig. 11. The resonator thru port will adjust the amplitude and phase of the second arm around the resonance. The same is thru is the drop port is used as the arm 2.
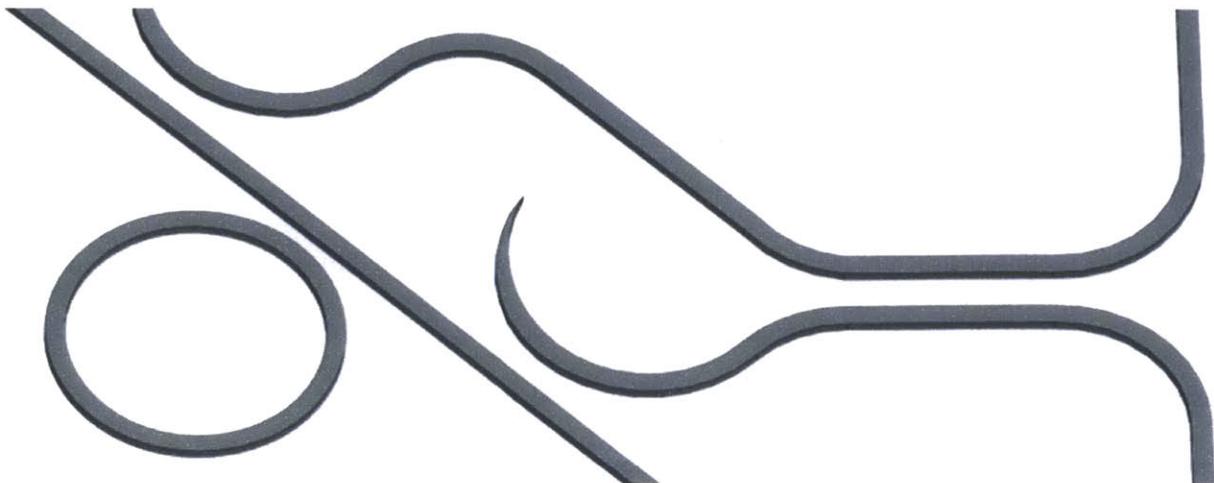


Figure 11. Integration of amplitude to phase converter with a resonator.
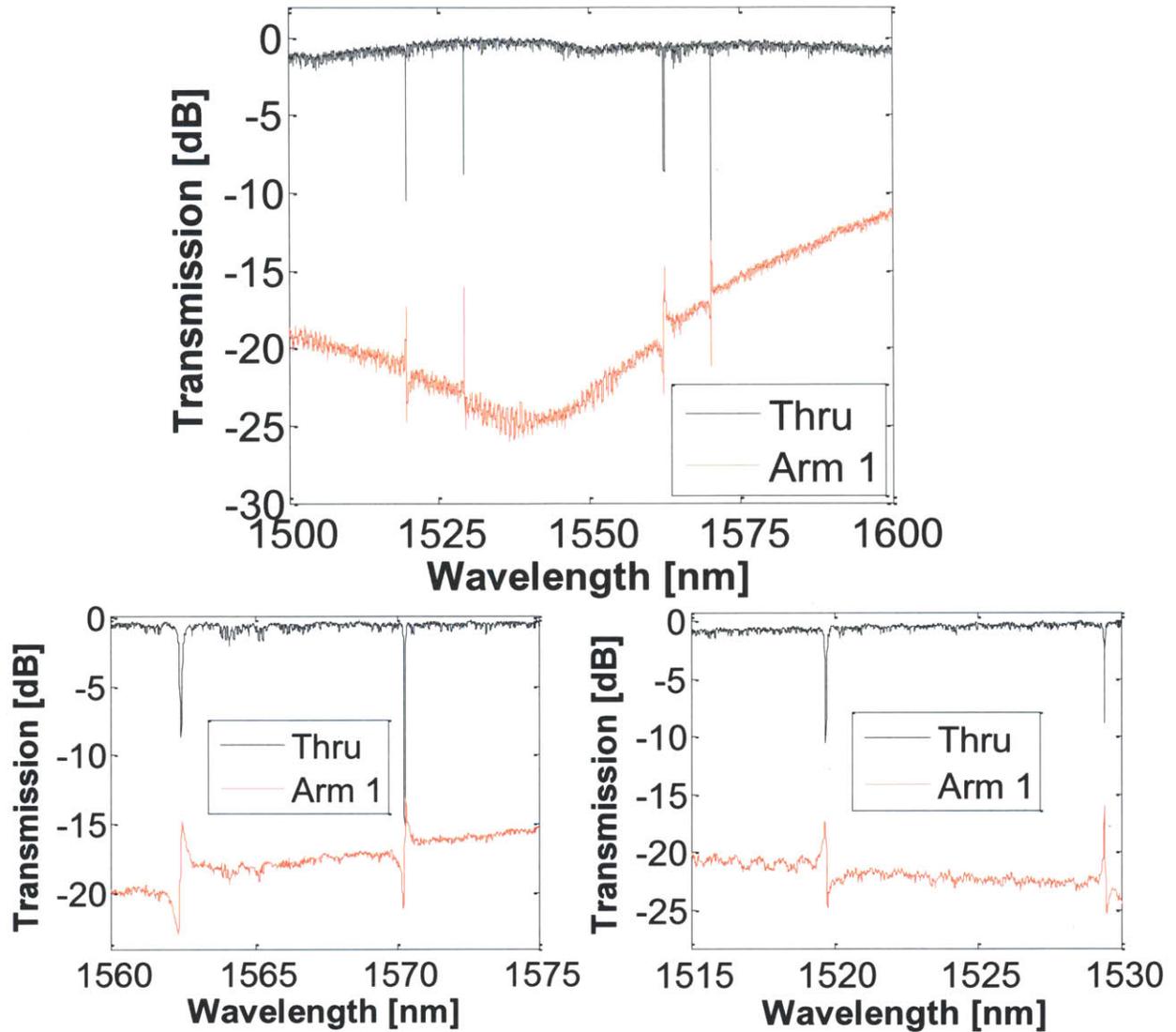
Figure 12. Demonstration of the proposed amplitude to phase converter integrated with a microdisk resonator. The top plot is showing the FSR of microdisk structure, the bottom plots are zoomed in captions to show the phase response over the whole FSR by the amplitude to phase converter

The proposed structure is fabricated at CNSE. Arm 1, arm 2 and thru spectrum is obtained by CW tunable laser coupled into the waveguide with taper fibers (Fig. 12). The output resembles the phase response of the resonator at the arm outputs. However, active demonstration of this structure did not work properly due to large variations in 3dB-coupler performance in wafer and the resonator became undercoupled after full process.

The phase response can be used directly to detect the resonance with an edge detection integrated circuit to achieve automated wavelength recovery. Since this method can be generalized for more than one ring at a time, it is a general solution for aligning multiplexer, demultiplexer or modulators. Modulator recovery with amplitude to phase converter will require the data to estimate the lock position or observing the average power at the detectors.

## 4.4 Conclusions and Future Work

In this chapter, we have introduced a new and advanced method of automated wavelength recovery. We have fully understood the theory and designed every component with FDTD-3D simulation. The first round fabrication demonstrated the passive response of the amplitude to phase response converter successfully. The work will follow with correcting the devices, achieving broadband response and demonstration more than one resonator with single converter. The possibility of high order ring recovery will be investigated.

## 4.5 References

[1]   Watts, M.R.; Zortman, W.A.; Trotter, D.C.; Young, R.W.; Lentine, A.L.; , "Low-Voltage, Compact, Depletion-Mode, Silicon Mach–Zehnder Modulator," *Selected Topics in Quantum Electronics, IEEE Journal of*, vol.16, no.1, pp.159-164, Jan.-feb. 2010

[2]   W. Green, M. Rooks, L. Sekaric, and Y. Vlasov, "Ultra-compact, low RF power, 10 Gb/s siliconMach-Zehnder modulator," Opt. Express 15, 17106-17113 (2007).

[3]   R. W. P. Drever et al., "Laser phase and frequency stabilization using an optical resonator," Appl. Phys. B: Photophys. Laser Chem. 31, 97–105 (1983).

[4]   Ramadan, T.A.; Scarmozzino, R.; Osgood, R.M., Jr.; , "Adiabatic couplers: design rules and optimization," *Lightwave Technology, Journal of*, vol.16, no.2, pp.277-283, Feb 1998

[5]   C. Katsidis and D. Siapkas, "General Transfer-Matrix Method for Optical Multilayer Systems with Coherent, Partially Coherent, and Incoherent Interference," Appl. Opt. 41, 3978-3987 (2002).

[6]   H. A. Haus, Waves and fields in optoelectronics. Englewood Cliffs, NJ: Prentice-Hall, 1984.

[7]   M. Popovic, C. Manolatou, and M. Watts, "Coupling-induced resonance frequency shifts in coupled dielectric multi-cavity filters," Opt. Express 14, 1208-1222 (2006).

# 5 Conclusions and Future Work

The thesis started with a review of electrical and optical on-/off-chip communications. The roadmap for realization of Wavelength Division Multiplexed (WDM) Silicon Photonics is summarized. The challenges that Silicon Photonics need to overcome introduced. The available ways to overcome those challenges are explained. The automated wavelength recovery (AWR) architecture is introduced.

The resonators that can enable AWR designed and demonstrated in Chapter 2 which includes a vertical junction circularly contacted microdisk modulator, a vertical junction microdisk modulator with thermo-optic tuner, a new L-shaped resonant microring (LRM) filter and modulator. The first integration of an adiabatic resonant microring (ARM) filter to heater driver is demonstrated on deep trench process. The demonstrated devices in this thesis can be used to realize a fully integrated WDM link with AWR, a high order switch or filter, suspended microring resonators and integrated phase shifters.

Using an ARM resonator, AWR is demonstrated under thermal stress, laser drifts and laser power fluctuations. AWR algorithm has shown the potential to be optimized in speed or accuracy. The future work will include recovery of large scale WDM networks as well as high order ring resonators.

We have envisioned an advanced way of automated wavelength recovery and fully understood the theory and designed every component with FDTD-3D simulation. The first round fabrication have demonstrated the passive response of the amplitude to phase response converter successfully. The work will follow with correcting the devices, achieving broadband response and demonstration more than one resonator with single converter. The possibility of high order ring recovery will be investigated.