Integration of Pentacene-Based Thin Film Transistors via Photolithography for Low and High Voltage Applications
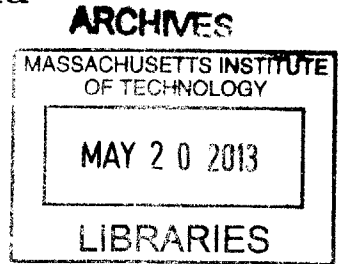
by

Melissa Alyson Smith

B.S., University of Illinois at Urbana-Champaign (2006)

Submitted to the Department of Materials Science and Engineering
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy in Materials Science and Engineering

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

September 2012

Author . . . .
Department of Materials Science and Engineering
July 31, 2012

Certified by. . . . .
Akintunde Ibitayo Akinwande
Professor of Electrical Engineering and Computer Science
Thesis Supervisor

Certified by. . . . .
Harry L. Tuller
Professor of Ceramics and Electronic Materials
Departmental Thesis Co-Supervisor

Accepted by . . . .
Gerbrand Ceder
Chair, Departmental Committee for Graduate Students

Integration of Pentacene-Based Thin Film Transistors via Photolithography for Low and High Voltage Applications

by

Melissa Alyson Smith

Submitted to the Department of Materials Science and Engineering
on July 31, 2012, in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy in Materials Science and Engineering

Abstract

An organic thin film transistor (OTFT) technology platform has been developed for flexible integrated circuits applications. OTFT performance is tuned by engineering the dielectric constant of the gate insulator and the insulator/semiconductor interface. Full integration is enabled by a low temperature photolithographic patterning process that is compatible with flexible substrates. Devices and circuits for low voltage ($|V_{DS}| \leq 5$ V) and high ($|V_{DD}| \geq 300$ V) voltage applications are demonstrated. Both the low and high voltage OTFTs are made from the same set of materials and processes.

Low voltage operation is achieved by the use of BZN ($Bi_{1.5}Zn_1Nb_{1.5}O_7$) which maintains a high dielectric constant (40) at low processing temperatures. With surface treatments and back channel encapsulation for patterning, OTFTs having two distinct threshold voltages ($V_T > 0$ V and $V_T < 0$ V) are integrated into logic inverters and ring oscillators based on logic inverters.

To assess how BZN can serve as a gate dielectric in OTFTs, dielectric breakdown studies of BZN deposited at room temperature by RF Sputtering are presented. The time dependent dielectric breakdown (TDDB) and the time-zero dielectric breakdown (TZDB) are studied as a function of the polarity constant DC current stress, dielectric thickness, temperature, and surface treatments. Results show that current flows through these films via Schottky emission with a barrier height of ~1 eV on Au. Further, initial breakdown was not fatal and is characterized as a change in conduction mechanisms. This suggests that a trap assisted conduction mechanism dominates beyond a critical trap density ($\rho = 1.5 \times 10^{17}$ cm^{-3}) which is generated due to electrical stressing.

High voltage thin film transistor (HVTFT) switches very large drain-to-source volt-

ages (V_{DD} >300 V) with a lower controlling voltage (V_G <20 V). An offset drain/source structure enables high voltage operation. A high voltage organic thin film transistor (HVOTFT) has been fabricated. As organic semiconductors and related devices are known for their compatibility with flexible media and/or large areas, the HVOTFT would be suitable for high voltage switching on such media. Gate insulator engineering is used to tune the threshold voltage and drain current in these devices. HVOTFTs of channel length 10 μm and offset length 20 μm suffer from non-saturating current behavior that is similar to the short channel effects reported in short channel OTFTs and Si-based MOSFETs, and a metastable charge injection similar to that reported in a-Si based HVTFTs.

Thesis Supervisor: Akintunde Ibitayo Akinwande
Title: Professor of Electrical Engineering and Computer Science

Departmental Thesis Co-Supervisor: Harry L. Tuller
Title: Professor of Ceramics and Electronic Materials

Acknowledgments

Microsystems Technology Laboratory
The staff at Microsystems Technology Laboratory at MIT is amazing. I can't imagine how I could have completed my work without their diligence, knowledge, insight, and experience. I am VERY fortunate to be able work in such an exciting environment created by the MTL staff. It is such a great community. At MIT, I wouldn't want to work any other place. Thank You MTL!!

Akinwande Research Group AKA the "A-Team"
There is never a bad day in the Akinwande Research Group (seriously). Being a part of the team has been the most rewarding experience I've had at MIT. From late evening in the cleanrooms to trips to the "library", all 100% fun. I owe my deepest gratitude to my esteemed thesis advisor Prof. Tayo Akinwande (AKA "The Man") for his guidance and continued unwavering support.

MIT
I am grateful to the following for support and advocacy on my behalf:
Prof. Sam Allen, Dean Christopher M. Jones, Monica Orta, Dean Christine Ortiz, Prof. Kristala Jones Prather, Dean Blanche Staton

UIUC
To those who made their support available beyond my undergraduate education. Thank you for being GREAT educators.
Prof. Les Allen, Dean N Jonné Brown, Prof. Trudy Kriven, Prof. Angus Rockett, Prof. John Weaver

Family and Friends
I am indebted to my many of my friends who supported me and gave me boost right when I needed. In no particular order: Laura Mulryan, Jacky Priego, Zenzile Brooks, Neha Patadia, Danielle Zurovcik (Yeah!! Yeah!!), Andrea Colaco, Alex Juarez, Cody Gilleland, Rizwan Dhanidina, Harlan Crystal, Annie Wang, Melinda Hale, Andrea Ridgeway, Victor Pollaci, Elizabeth Robinson, Namrata Kothari, Catarina Abreu, Diana Lewis, Tiara Brown, Stephen Guerrera, Stefan Mitropolitsky, Patti and Shaquille Florez, Jayne Collins
- *To Wayon Milton Smith Sr. (Pop Pop) (1931-2010)*: I wish you were here to watch me graduate. You were so proud that I was going to grad school. I know you were proud of me then I hope I continue to make you proud.
- *To Larisa Tyus (1984-2008)*: As long as I've known you, you've always wanted me to win. I wish I could share this one with you.
Super special thanks for those who have had to put up with me the longest, Faye Smith (mother dearest), Wayon Smith Jr. (Pops), and Kit Smith (brother, I AM smarter than you ☺). Words can't really articulate how critical your support is for me to finish. You were in my thoughts constantly and served as inspiration. Thank you and I love you. I'll be home for thanksgiving.

"Commit your works to the Lord, And your plans will be established." Proverbs 16:3

Thank You, -Melissa

Contents

List of Figures

List of Tables

Chapter 1

Introduction

Ages in time are defined by materials (Ice Age, Stone Age, Bronze Age, Iron Age, etc). So how does one define today? Some call it the Computer Age (semiconductors). Others call it the Age of Plastics (organic materials). The subject of this work, organic semiconductors, lies at the intersection of the two.

1.1 A BRIEF HISTORY of SOLID STATE DEVICES and INTEGRATED CIRCUITS

Consider the evolution of displays, telecommunication, and computation (Figure 1-1). Devices used for these applications have become so influential and ubiquitous that modern life is unimaginable without them. Further, these gadgets are so multifunctional it is difficult to determine for which application they are designed (smart phones, tablets). Beyond sharing mutually beneficial applications, the evolution of display, computation, and telecommunications technologies share a common similarity. In all three, multifunctionality is realized due to increasing design and fabrication complexity which is enabled by the integrated circuit (batch fabricated, interconnected electronic components). Following the wide scale adoption of the integrated circuit (IC), all three industries have shown dramatic advancement within the last 30 years.

The first beneficiary of the integrated circuit is computation. The demand for lower power consumption, faster microprocessors with more memory at lower costs spawned a prodigious industrial infrastructure for crystalline Si-based microelectronics. In 1965, Gordon Moore postulated that number of transistors that can be batch fabricated into an integrated circuit will double approximately every two years [1]. This trend has held since its inception. The need for cost reduction drives the miniaturiza-

FIGURE 1-1: Evolution of electronics

tion of integrated circuits. With this miniaturization, applications can be made more complex and multifunctional. As a result, this industry motivated the development of etching, deposition, and patterning techniques for the very large scale integration (VLSI) of circuits. [2].

The display and telecommunication industries progressed by adopting the fabrication techniques pioneered in Si-based microelectronics. For example, pressure sensors, accelerometers, gyroscopes and other micro-electro-mechanical systems (MEMS) based on silicon have used this infrastructure to miniaturize and integrate a significant amount of functionality onto MEMS chips while reducing size and hence cost through batch fabrication [3, 4, 5, 6, 7, 8, 9]. In the case of displays, this adaptation has motivated patterning technologies for large areas. Displays as large as 100" have been demonstrated. The achievement of displays on large areas conceived the notion of flexible displays or substrates for even large areas at lower costs, where active integrated devices could be embedded on any surface such as plastic or textiles [10].

1.2 DEMAND for LARGE AREA FLEXIBLE ELECTRONICS

Modern flat panel displays are not based on single crystal silicon (as with microprocessors) but on amorphous silicon (a-Si). Single crystal silicon cannot be grown or deposited at temperatures below 1000°C, whereas processing temperatures for glass substrates is limited to 400°C and below [11, 12, 13], limiting fabrication to rigid substrates. The extension of Si microfabrication technologies to mechanically compliant substrates suggest that new devices processed at temperatures close to ambient are necessary. This requirement has inspired and motivated research in organic (carbon-based) semiconductor electronics as they can be processed at room temperature making them compatible with flexible materials which have low melting points (plastics, fabric, gels, foams, etc.).

Large area, flexible electronics have the potential to make current technologies more pervasive and ubiquitous. Such ubiquity can take the form of roll-able displays, solar cells, microprocessors, portable medical diagnostics monitors, smart textiles, wearable antennas and sensors. While there are a number of semiconductor materials that are viable candidates for realizing such applications, the class of materials of interest in this dissertation is organic semiconductors.

1.3 ORGANIC THIN FILM TRANSISTORS

For over two decades, organic semiconductor based thin film transistors (OTFTs) have been of immense interest to solid state device physicists and engineers. This is because of the potential to build electronics with significant complexity and func-

tionality on any flexible, large area surface. The nature of the chemical bonding in organic semiconductors (Van der Waals or dispersive) allows them to be fabricated on mechanically compliant substrates. A number of devices with large areas show a modest level of complexity and have been demonstrated using OTFTs as components. These range from RFID tags [14, 15] and microcontrollers [16, 17] to tactile sensors [18], and actuators [19]. A comparison between the TFT and Metal Oxide Semiconductor FET (MOSFET) is shown in Figure 1-2.
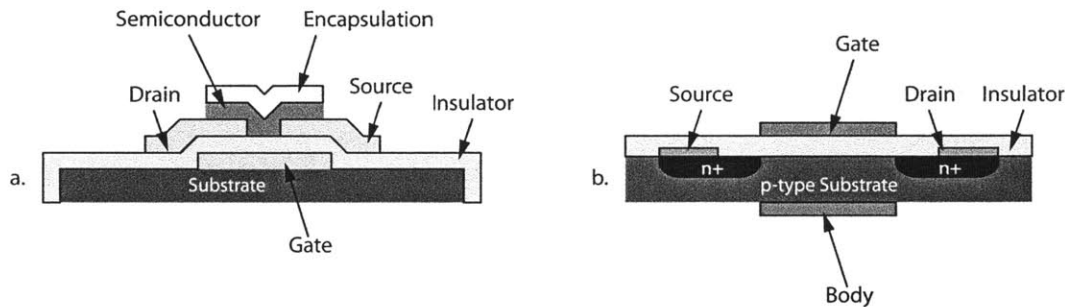
FIGURE 1-2: Cross section of the TFT explored in this work (a) and Cross section of typical monolithic MOSFET (b)

Initially, OTFTs were fabricated using highly doped Si as the unpatterned gate, with a thermally grown oxide, with metal contacts for the source/drain, and completed with the deposition of the semiconductor. A completed structure is shown in Figure 1-3. This structure is successful for giving quick feedback of materials and device exploration but was not suitable for building simple two transistor circuits such as the logic inverter. To demonstrate scalable devices and simple circuits, fabrication processes that use shadow masks were developed [20]. However, complex circuits (10,000 TFTs) with useful functions (voltage inverting) cannot be made with this patterning method as scaling and reproducibility are limited. This is a familiar problem as early Si-based devices had the same limitation. Photolithography was developed to surmount this issue in Si-based microelectronics and can be applied to OTFTs.

1.3.1 Patterning and Integration with Photolithography

By using low resolution patterning methods or lack of patterning altogether, the performance of organic thin film transistors (OTFTs) and related circuits can suffer from large overlap capacitances, cross talk, or source to drain current leakage [22, 23, 24, 25, 26]. For technologies based on organic semiconductors, photolithography is desirable as devices can be scaled to smaller feature sizes over large substrate areas enabling complex circuits on any flat surface [23, 26, 27]. Further, building OTFTs with photolithography allows for compatibility and easy integration with other system components that rely on photolithography, such as micro-electro-mechanical systems
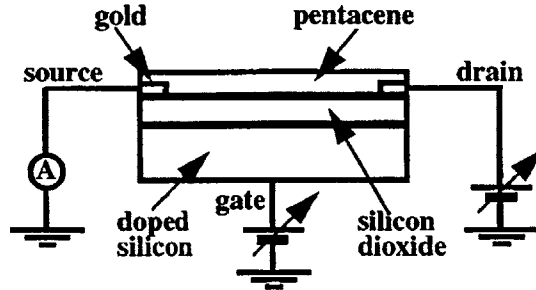
FIGURE 1-3: Schematic of early OTFT prototype structure [21]. This structure is not sufficient for making complex circuits.

(MEMS). Nausieda et al. showed how using photolithography can enable complex circuits (mixed-signal integrated circuits with dual threshold voltage technology by gate metal engineering) and applications like an organic active-matrix imager [28, 29]. As Nausieda et al. aptly demonstrated the benefits and added capabilities of photolithography, a key performance limitation which is high operating voltage, has yet to be addressed with devices and circuits built with photolithography.

1.3.2 High-κ Insulators for Low Operating Voltages

A number of different variables determine the drain current in an OTFT. One of which is the amount of charge that is accumulated in the channel by the applied gate voltage. This depends on the capacitance of the gate insulator. Equation 1.1 is the expression for gate insulator capacitance.

$$C = \frac{\epsilon_o \kappa A}{t_{ox}} \tag{1.1}$$

Where,

        C_i: gate insulator capacitance
        ϵ_o: permittivity of free space
        κ: dielectric constant of the insulator
        A: area of gate capacitor
        t_{OX}: thickness of gate insulator

Using this expression, there are two ways gate capacitance can be increased for more charge accumulation and higher drive currents. One way is to decrease the gate oxide thickness (t_{OX}). This is effective [30] but poses a reliability issue as the thinner dielectrics are worse insulators as they show large leakage currents. This too was an issue for Si-based devices and was successfully surmounted by using high-κ (dielectric constant) insulators or increasing κ in Equation 1.1. The wide scale use of high-κ insulators in Si-based devices was pioneered by Intel Corporation, a semiconductor chip maker, enabling multiple generations of advancement in chip performance [31].

High-κ dielectrics are of interest for OTFTs as a means of increasing drive currents and lowering operating voltages which improve energy efficiency in a circuit. Dimitrakopoulos et al. successfully demonstrated the use of high-κ dielectrics to lower the operating voltage of OTFTs in 1999 [32]. The high-κ dielectric not only lowered the operating voltage. To date, there are many reports of high-κ materials successfully reducing operating voltages in OTFTs [33].

1.3.3 Surface Treatments for Threshold Voltage Engineering

The threshold voltage (V_T) is the gate voltage necessary to accumulate enough charge in the semiconductor to form a conducting channel that will support a current. Equation 1.2 is a general expression (discussed in more detail in Chapter 3) for the threshold voltage in OTFTs.

$$V_T = (\phi_M - \phi_S) - \frac{t_{OX}}{\epsilon_o \kappa} (Q_{it} - Q_{OX})$$ (1.2)

Where,

ϕ_M and ϕ_S: work functions of the gate metal and the semiconductor

ϵ_o: permittivity of free space

κ: dielectric constant of the insulator

Q_{it}: surface charge density at the interface between insulator and the semiconductor.

$Q_{OX} = \int_0^{t_{OX}} \frac{t}{t_{OX}} \rho_{OX}(t) \cdot dt$

ρ_{OX}: charge density per unit volume in the insulator

t_{OX}: thickness of the insulator

From this expression (Equation 1.2), V_T can be controlled by engineering the interface state density (Q_{it}), among other device parameters (ϕ_M, κ, and t_{OX}). Circuits with two distinct threshold voltages will consume less power, are more area efficient, and show more defined "high" and "low" states (necessary for complex logic and computing). As most organic semiconductors cannot be reliably doped as with Si (dopant levels in Si determine threshold voltages), surface treatments that electronically modify the interface of the semiconductor/insulator are used to shift threshold voltage.

Using surface treatments to tune threshold voltages is common in OTFTs [34, 35, 36]. Wang et al. showed how to tune the threshold voltage by creating dangling bonds at the insulator/semiconductor interface via O_2 plasma treating an organic insulator. Of the reported high-κ insulators used to reduce operation voltages, the material deployed by Choi et al. BZN ($Bi_{1.5}Zn_1Nb_{1.5}O_7$), is of special interest. Choi et al. showed that the threshold voltage of OTFTs made from BZN can be shifted negative with a parylene-C based surface treatment creating a technology platform with both low operating voltages and two distinct V_Ts. The lack of a fully integrated, low voltage (V_{GS}), tunable V_T device technology platforms limit the traction of new applications based on organic thin film transistors.

28

1.4 SCOPE of the DISSERTATION

The realization of complex and advanced electronic systems with new functionality requires circuits to be built with materials (organic semiconductors) compatible with large areas and flexible substrates (low temperature processing). This will be addressed in this dissertation. Specifically, integrated circuits based on OTFTs featuring advanced materials (high-κ and threshold voltage shifting surface treatments) with be fabricated and demonstrated in both high and low voltage applications.

1.4.1 Low Voltage, Dual V_T, Thin Film Transistors and Integrated Circuits

Though pentacene has a comparable mobility to amorphous Si, there is still a need for devices to operate at lower voltages to realize the full potential of technologies based on organic semiconductors. Devices requiring high power supply voltages or several batteries limit the portability and usefulness of the applications that use these organic semiconductor technologies. At the very least, low voltage OTFTs will have a low threshold voltage (V_T), high drive currents (I_D), and distinct "on" and "off" states within a narrow voltage range or a small subthreshold swing (S). These design criteria can be met with a high-κ gate insulators [33].

As reported by Choi et al., the high dielectric constant (κ=40) gate insulator BZN, can lower operating voltages in OTFTs and circuits [37]. Further V_T can be shifted by using a surface treatment on this dielectric without sacrificing the low voltage operation. Nauseida et al., demonstrated the efficacy of building OTFT based integrated circuits featuring two distinct threshold voltages, which makes for more power and area efficient circuits [29].

This dissertation reports a technology which uses the materials reported by Choi et al. to lower operating voltage and realize two distinct threshold voltages which are deployed in similar integrated circuitry and fabrication techniques used by Nausieda et al. The technology is fully integrated via the low temperature processing methods.

1.4.2 A Study of Low Voltage Breakdown in $Bi_{1.5}Zn_1Nb_{1.5}O_7$

BZN is effective in lowering operating voltages in organic and metal oxide based TFTs [37, 38]. However, its wide accepted use is limited due to reliability issues emanating from high gate leakage and low breakdown fields in films deposited at room temperature [38, 39, 40]. Investigators have addressed this issue by fabricating composite dielectric stacks which feature larger bandgap insulators [38] and composition engineering to control parasitic trap assisted charge transport [40] in the dielectric. How-
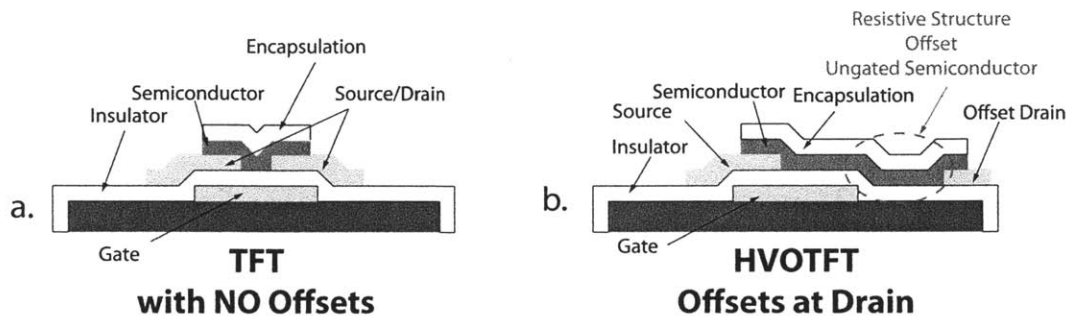
FIGURE 1-4: Cross sections OTFT and HVOTFT of comparing the structural differences.

ever, a rigorous statistical study of dielectric breakdown based on Time-Dependent Dielectric Breakdown and Time-Zero Dielectric Breakdown measurements in BZN films deposited at room temperature with minimal annealing (necessary for flexible substrates) is lacking. Such a study is conducted in this dissertation. Results support reported leakage mechanisms [40, 38] in BZN and provides more insight into how this material can be used practically in hundreds of devices on one substrate.

1.4.3 High Voltage Organic Thin Film Transistors

A High Voltage Thin Film Transistor (HVTFT) switches very large voltages ($|V_{DD}|$ >300V) with a small controlling voltage ($|V_{GS}| \leq 20V$). While field effect transistors are widely used for pixel addressing in large-area flat-panel displays, many applications require drive voltages much greater than 100V. Among these applications are ferroelectric liquid crystals, electrophoretic or PLZT electrooptic displays, and electrographic plotters [41, 42], digital x-ray imaging [43, 44], addressable poly-Si cold cathodes [45], and MEMS [4]. High voltage FETs are a necessity or enable substantial improvements for these applications.

Conceived in the late 1980's, the HVTFT is typically built with amorphous or poly-Si for the semiconductor [42, 41]. In this dissertation, the Si is replaced with an organic semiconductor and processed below $\sim 130°C$ realizing a HVTFT compatible with flexible substrates. This provides a technology platform for flexible MEMS drivers. To increase the drain-to-source driving voltage or electric field across an FET, a resistive structure can be placed between the drain or source electrode and the gated channel. In this work, high driving voltages are achieved by offsetting the drain or source electrode from the gate. This offset creates an resistive ungated semiconductor region in series with a gated semiconductor region. Martin et al. and Unagami et al. used this approach for amorphous Si and poly-Si-based HVTFTs [42, 41]. This structure is shown and compared to the typical OTFT in Figure 1-4.

30

1.5 DISSERTATION OVERVIEW

Advanced devices can be built by optimizing key materials and components. However to realize complete integrated systems, the materials and components must also be optimized within the constraints of the fabrication processes and device structures necessary for integration, not from materials properties alone. By considering both fabrication processes and device structures, in addition to material properties for materials selection, integrated circuits are built for two widely different applications using the same materials.

This dissertation will report the following.

1. A scalable, low temperature ($<130°C$), fully photolithographic, fabrication process is developed for OTFTs. It features high-κ (40) gate dielectrics for low voltage operation ($|V_{GS}|$ and $|V_{DS}| \leq 5$ V) and surface treatments for threshold voltage engineering.

2. For low voltage integrated circuits, OTFTs with two distinct threshold voltages, depletion-mode ($V_T > 0$ V) and enhancement-mode ($V_T < 0$ V) will be integrated into circuits. Using two distinct threshold voltages enables area and power efficient complex integrated circuits which are demonstrated with logic inverters and an 11-stage ring oscillator.

3. For high voltage integrated circuits, high voltage OTFTs (HVOTFT) capable of switching high voltages ($|V_{DD}| > 300$ V) using low controlling voltages ($|V_G| \leq 20$ V) are demonstrated.

Chapter 2 provides a justification of the materials selected for these investigations. Chapter 3 present the relevant field effect transistor models and methods parameter extraction. Chapter 4 describes the processing techniques and devices structures used to fabricate these TFTs. The demands of this fabrication process are discussed in detail by relating final material structure and morphology to the electrical performance of the resulting devices. In Chapters 5, 6, 7, and 8, the limitations of this technology are discussed as a consequence of the fabrication process and materials selection. Chapter 7 will study the reliability of BZN specifically and propose how this dielectric can be used practically for large scale integration. Low voltage and high voltage devices and circuits are discussed in Chapter 6, and Chapter 8 respectively. Finally, future investigations are proposed in Chapter 9 based on results and discussions in Chapters 5, 6, 7, and 8.
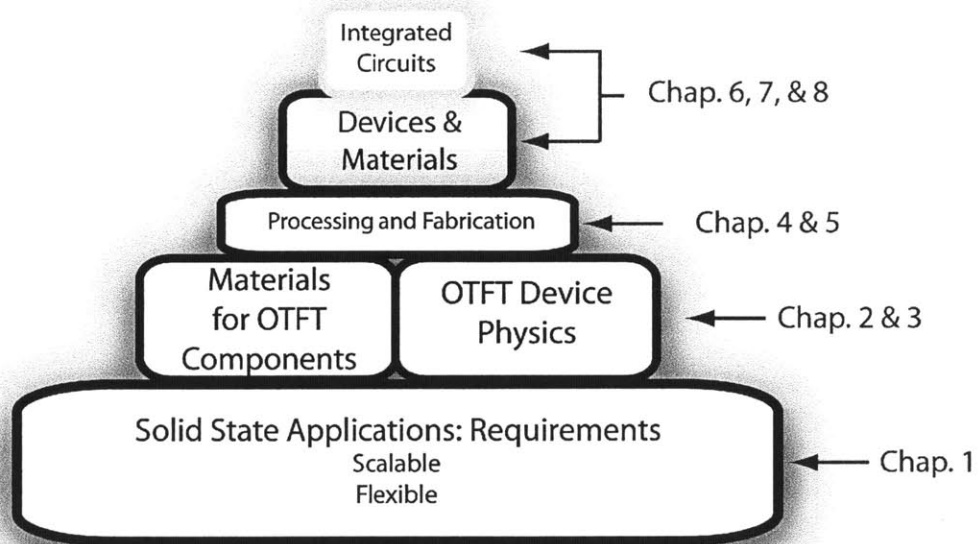
FIGURE 1-5: Thesis Overview

1.6 REFERENCES

[1] G. E. Moore, "Cramming more components onto integrated circuits," *Electonics Magazine*, vol. 38, no. 8, 1965.

[2] "International technology roadmap for semiconductors: Lithography," 2011.

[3] S. Chalasani, Y. Xie, and C. Mastrangelo, "Microfabricated pressure sensing particles with integrated retroreflectors," in *Micro Electro Mechanical Systems (MEMS), 2011 IEEE 24th International Conference on*, pp. 1158 –1161, jan. 2011.

[4] E. A. Chow, J. P. Lu, J. Ho, C. W. Shih, D. De Bruyker, M. Rosa, and E. Peeters, "High voltage thin film transistors integrated with MEMS," *Sensors and Actuators a-Physical*, vol. 130, pp. 297–301, 2006.

[5] H. K. Rockstad, T. W. Kenny, P. J. Kelly, and T. B. Gabrielson, "A microfabricated electron-tunneling accelerometer as a directional underwater acoustic sensor," *AIP Conference Proceedings*, vol. 368, no. 1, pp. 57–68, 1996.

[6] M. Mehregany, K. Gabriel, and W. Trimmer, "Integrated fabrication of polysilicon mechanisms," *Electron Devices, IEEE Transactions on*, vol. 35, pp. 719 –723, jun 1988.

[7] L.-S. Fan, Y.-C. Tai, and R. Muller, "Integrated movable micromechanical structures for sensors and actuators," *Electron Devices, IEEE Transactions on*, vol. 35, pp. 724 –730, jun 1988.

[8] D. DeVoe and A. Pisano, "Surface micromachined piezoelectric accelerometers (pixls)," *Microelectromechanical Systems, Journal of*, vol. 10, pp. 180 –186, jun 2001.

[9] M. Lemkin and B. Boser, "A three-axis micromachined accelerometer with a CMOS position-sense interface and digital offset-trim electronics," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 456 –468, apr 1999.

[10] D. Marculescu, R. Marculescu, N. Zamora, P. Stanley-Marbell, P. Khosla, S. Park, S. Jayaraman, S. Jung, C. Lauterbach, W. Weber, T. Kirstein, D. Cottet,

J. Grzyb, G. Troster, M. Jones, T. Martin, and Z. Nakad, "Electronic textiles: A platform for pervasive computing," *Proceedings of the IEEE*, vol. 91, pp. 1995 – 2018, dec 2003.

[11] S.-J. Lee, S.-W. Lee, K.-M. Oh, S.-J. Park, K.-E. Lee, Y.-S. Yoo, K.-M. Lim, M.-S. Yang, Y.-S. Yang, and Y.-K. Hwang, "A Novel Five-Photomask Low-Temperature Polycrystalline Silicon CMOS Structure for AMLCD Application," *IEEE Transactions on Electron Devices*, vol. 57, pp. 2324 –2329, sept. 2010.

[12] C.-W. Chen, T.-C. Chang, P.-T. Liu, H.-Y. Lu, K.-C. Wang, C.-S. Huang, C.-C. Ling, and T.-Y. Tseng, "High-performance hydrogenated amorphous-Si TFT for AMLCD and AMOLED applications," *IEEE Electron Device Letters*, vol. 26, pp. 731 – 733, oct. 2005.

[13] M. Lee, K.-Y. Ho, P.-C. Chen, C.-C. Cheng, S. Chang, M. Tang, M. Liao, and Y.-H. Yeh, "Promising a-Si:H TFTs with High Mechanical Reliability for Flexible Display," in *Electron Devices Meeting, 2006. IEDM '06. International*, pp. 1 –4, dec. 2006.

[14] P. F. Baude, D. A. Ender, M. A. Haase, T. W. Kelley, D. V. Muyres, and S. D. Theiss, "Pentacene-based radio-frequency identification circuitry," *Applied Physics Letters*, vol. 82, no. 22, pp. 3964–3966, 2003.

[15] E. Cantatore, T. C. T. Geuns, G. H. Gelinck, E. van Veenendaal, A. F. A. Gruijthuijsen, L. Schrijnemakers, S. Drews, and D. M. de Leeuw, "A 13.56-MHz RFID system based on organic transponders," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 1, pp. 84–92, 2007.

[16] K. Myny, E. van Veenendaal, G. Gelinck, J. Genoe, W. Dehaene, and P. Heremans, "An 8b organic microprocessor on plastic foil," in *2011 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pp. 322 – 324, feb. 2011.

[17] A. Daami, C. Bory, M. Benwadih, S. Jacob, R. Gwoziecki, I. Chartier, R. Coppard, C. Serbutoviez, L. Maddiona, E. Fontana, and A. Scuderi, "Fully printed organic CMOS technology on plastic substrates for digital and analog applications," in *2011 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pp. 328 –330, feb. 2011.

[18] T. Someya, T. Sakurai, and T. Sekitani, "Flexible, large-area sensors and actuators with organic transistor integrated circuits," in *IEEE International Electron Devices Meeting, IEDM Technical Digest*, pp. 4 pp. –445, dec. 2005.

[19] Y. J. Hsu, Z. Jia, and I. Kymissis, "A Locally Amplified Strain Sensor Based on a Piezoelectric Polymer and Organic Field-Effect Transistors," *IEEE Transactions on Electron Devices*, vol. 58, 2011 2011.

[20] C. D. Dimitrakopoulos and D. J. Mascaro, "Organic thin-film transistors: A review of recent advances," *IBM Journal of Research and Development*, vol. 45, pp. 11 –27, jan. 2001.

[21] A. R. Brown, A. Pomp, D. M. de Leeuw, D. B. M. Klaassen, E. E. Havinga, P. Herwig, and K. Müllen, "Precursor route pentacene metal-insulator-semiconductor field-effect transistors," *Journal of Applied Physics*, vol. 79, no. 4, pp. 2136–2138, 1996.

[22] J.-W. Lee, B.-K. Ju, J. Jang, Y.-S. Yoon, and J.-K. Kim, "High mobility organic transistor patterned by the shadow-mask with all structure on a plastic substrate," *Journal of Materials Science*, vol. 42, no. 3, pp. 1026–1030, 2007.

[23] I. Kymissis, A. I. Akinwande, and V. Bulovic, "A lithographic process for integrated organic field-effect transistors," *Journal of Display Technology*, vol. 1, no. 2, pp. 289–294, 2005.

[24] I. Kymissis, C. D. Dimitrakopoulos, and S. Purushothaman, "Patterning pentacene organic thin film transistors," *Journal of Vacuum Science and Technology B: Microelectronics and Nanometer Structures*, vol. 20, no. 3, pp. 956–959, 2002.

[25] S. Steudel, K. Kris, Myny, S. De Vusser, J. Genoe, and P. Heremans, "Patterning of organic thin film transistors by oxygen plasma etch," *Applied Physics Letters*, vol. 89, no. 18, p. 183503, 2006.

[26] H. Wang, Z.-Y. Ji, L.-W. Shang, X.-H. Liu, Y.-Q. Peng, and M. Liu, "Top contact organic field effect transistors fabricated using a photographic process," *Chinese Physics B*, vol. 20, no. 8, p. 087306.

[27] H. Jia, E. K. Gross, R. M. Wallace, and B. E. Gnade, "Patterning effects on poly (3-hexylthiophene) organic thin film transistors using photolithographic processes," *Organic Electronics*, vol. 8, no. 1, pp. 44 – 50, 2007.

[28] I. Nausieda, K. Ryu, I. Kymissis, A. I. Akinwande, V. Bulovic, and C. G. Sodini, "An organic active-matrix imager," *IEEE Transactions on Electron Devices*, vol. 55, no. 2, pp. 527–532.

[29] I. Nausieda, K. K. Ryu, D. Da He, A. I. Akinwande, V. Bulovic, and C. G. Sodini, "Mixed-signal organic integrated circuits in a fully photolithographic dual threshold voltage technology," *IEEE Transactions on Electron Devices*, vol. 58, no. 3, pp. 865–873, 2011.

[30] H. Klauk, U. Zschieschang, J. Pflaum, and M. Halik, "Ultralow-power organic complementary circuits," *Nature*, vol. 445, no. 7129, pp. 745–748, 2007.

[31] R. Chau, "Intels Breakthrough in High-K Gate Dielectric Drives Moores Law Well into the Future ," *Technology@Intel Magazine*, 2004.

[32] C. D. Dimitrakopoulos, S. Purushothaman, J. Kymissis, A. Callegari, and J. M. Shaw, "Low-voltage organic transistors on plastic comprising high-dielectric constant gate insulators," *Science*, vol. 283, no. 5403, pp. 822–824, 1999.

[33] R. P. Ortiz, A. Facchetti, and T. J. Marks, "High-κ organic, inorganic, and hybrid dielectrics for low-voltage organic field-effect transistors," *Chemical Reviews*, vol. 110, no. 1, pp. 205–239, 2010,.

[34] A. Wang, I. Kymissis, V. Bulovic, and A. Akinwande, "Tunable threshold voltage and flatband voltage in pentacene field effect transistors," *Applied Physics Letters*, vol. 89, no. 11, p. 112109, 2006.

[35] F. D. Fleischli, S. Suarez, M. Schaer, and L. Zuppiroli, "Organic thin-film transistors: The passivation of the dielectric-pentacene interface by dipolar self-assembled monolayers," *Langmuir*, vol. 26, no. 18, pp. 15044–15049.

[36] C. Kim, S. Jo, S. Lee, W. Kim, H. Baik, and S. Lee, "Surface-Modified High-κ Oxide Gate Dielectrics for Low-Voltage High-Performance Pentacene Thin-Film Transistors," *Advanced Functional Materials*, vol. 17, no. 6, pp. 958–962, 2007.

[37] Y. Choi, I. D. Kim, H. L. Tuller, and A. I. Akinwande, "Low-voltage organic transistors and depletion-load inverters with high-κ pyrochlore BZN gate dielectric on polymer substrate," *IEEE Transactions on Electron Devices*, vol. 52, no. 12, pp. 2819–2824, 2005.

[38] M.-H. Lim, K. Kang, H.-G. Kim, I.-D. Kim, Y. Choi, and H. L. Tuller, "Low leakage current-stacked $MgO/Bi_{1.5}Zn_{1.0}Nb_{1.5}O_{7.0}$ gate insulator— for low voltage ZnO thin film transistors," *Applied Physics Letters*, vol. 89, no. 20, pp. 202908–3, 2006.

[39] I. D. Kim, M. H. Lim, K. Kang, H. G. Kim, and S. Y. Choi, "Room temperature fabricated ZnO thin film transistor using high-κ $Bi_{1.5}Zn_{1.0}Nb_{1.5}Oi_{7.0}$ gate insulator prepared by sputtering," *Applied Physics Letters*, vol. 89, no. 2, p. 3, 2006.

[40] N. G. Cho, H. Seo, D. H. Kim, H.-G. Kim, J. Kim, and I.-D. Kim, "Characterization on bandedge electronic structure of MgO added $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_{7.0}$ gate dielectrics for ZnO-thin film transistors," *Electrochemical and Solid-State Letters*, vol. 14, no. 1, pp. G4–G7.

[41] T. Unagami and O. Kogure, "High-voltage TFT fabricated in recrystallized polycrystalline silicon," *IEEE Transactions on Electron Devices*, vol. 35, pp. 314 –319, March 1988.

[42] R. A. Martin, V. M. Da Costa, M. Hack, and J. G. Shaw, "High-voltage amorphous silicon thin-film transistors," *IEEE Transactions on Electron Devices*, vol. 40, no. 3, pp. 634–644, 1993.

[43] K. S. Karim, P. Servati, and A. Nathan, "High voltage amorphous silicon TFT for use in large area applications," *Microelectronics Journal*, vol. 35, no. 3, pp. 311–315, 2004.

[44] W. Zhao, J. Law, D. Waechter, Z. S. Huang, and J. A. Rowlands, "Digital radiology using active matrix readout of amorphous selenium: Detectors with high voltage protection," *Medical Physics*, vol. 25, no. 4, pp. 539–549, 1998.

[45] N. Kim, "Fabrication of silicon field emitter arrays combined with HVTFT at low temperature," *SMDL Annual Report, School of Engineering, Seoul National University*, 1999.

Chapter 2

Materials Selection

This chapter will discuss the electronic and physical properties of the insulators, semi-conductor, and metals used to build OTFTs in this work. A justification will be given for the selection of each material. The criterion for selection is compatibility with flexible substrates or low temperature processability.

2.1 SEMICONDUCTOR: PENTACENE

Pentacene is widely studied organic semiconductor which has a relatively high mobility compared to other known organic semiconductors. The molecule is shown in Figure 2-1. Figure 2-2, compares pentacene to other organic semiconductors on the basis of mobility (μ) and shows pentacene to have mobilities comparable to amorphous Si. It is suitable for large area and flexible device applications due to low temperature process compatibility.
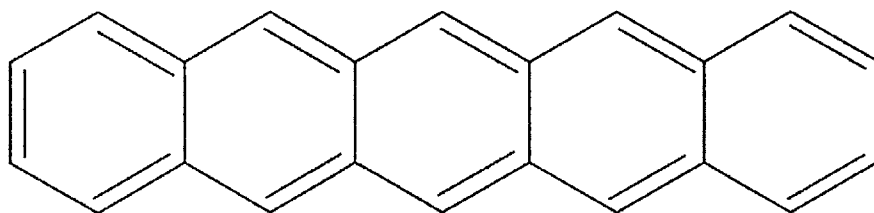
FIGURE 2-1: A molecule of pentacene

2.1.1 Chemical Structure and Bonding

Pentacene ($C_{22}H_{14}$) is a linear polycyclic carbon-based molecule consisting of 5(pent) benzene rings (acene) from which is derives its name. Conjugation is the delocalization of electrons in the π-orbitals of sp^2 hybridized carbons and is key to conducting
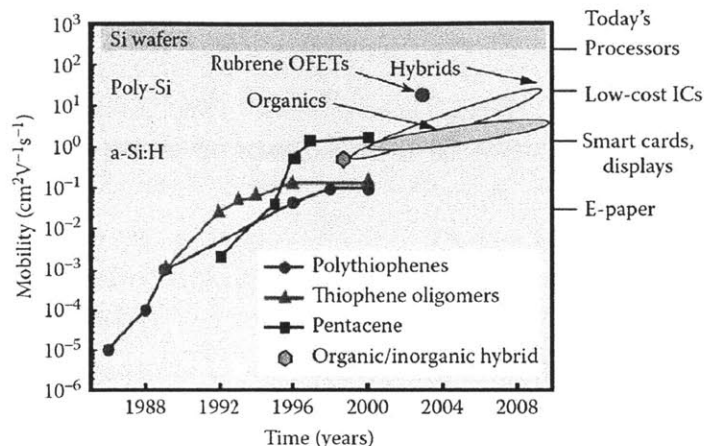
FIGURE 2-2: Evolution of carrier mobility for various organic semiconductors [1]. As most commercial TFT are made with a-Si, an organic semiconducting material should have a mobility that is comparable or better than a-Si, such as pentacene.

or semiconducting properties organic molecules. According to Hückels Rule [2], for each ring (n) in the aromatic molecule, there are 4n+2 π-bonding electrons where each carbon contributes one π-orbital for electron delocalization. In the case of the pentacene, the molecular orbitals are 1/2 full as there are 22 π-bonding electrons and 22 π-orbitals. Casting the network of delocalized π-orbitals as quantum potential well, quantized energy levels appear as a function of the number of carbons in the electron confining molecule. This is analogous to a "particle-in-a-box" where the energy of the electrons are given by Equation 2.1.

$$E_n = \frac{n^2 h^2}{8mL^2} \tag{2.1}$$

Where,

> E_n: energy of a particle
> n: principal quantum number, this is related to the wavelength of the particle in the box
> h: planks constant
> L: length of the box or number of carbons in the molecule
> m: mass of the particle

As with such quantized systems, more nodes (a region of zero probability of finding an electron) in the electron wave function means higher energy electrons. As seen in Figure 2-3 [3], the HOMO (highest occupied molecular orbital or highest bonding state) has fewer nodes than the LUMO (lowest unoccupied molecular orbital or lowest antibonding state). As one half of the orbitals are filled in pentacene, the HOMO level can be thought of as a valence band and the LUMO as a conduction band. Figure 2-4

LUMO+1

LUMO

HOMO

HOMO−1

Energy (eV)

"Conduction Band"

LUMO

E_{GAP}=~2eV

HOMO

"Valence Band"
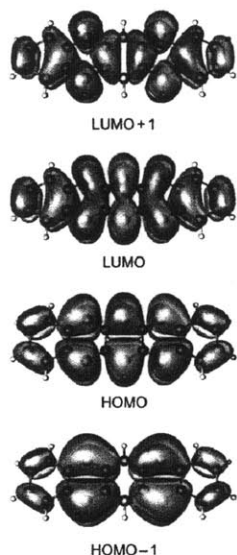
FIGURE 2-3: Molecular orbitals of the LUMO+1, LUMO, HOMO, HOMO-1 for pentacene [3] where the different colors of the orbitals represent ($\pm$) spin quantum numbers of the π orbital.
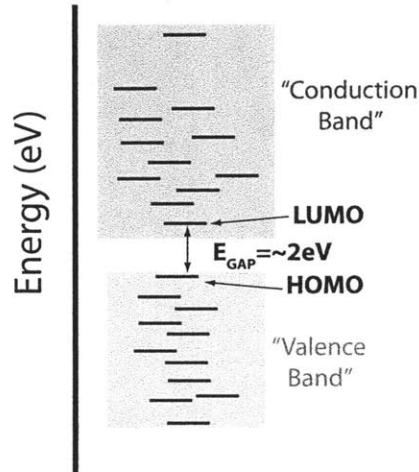
FIGURE 2-4: Molecular orbital energy levels for pentacene. Each distinct energy level corresponds to a specific molecular orbital.

qualitatively, shows how the "valence" and "conduction" bands arise from discreet energy levels of bonding and antibonding π-orbitals in pentacene. The entire solid thin film does not show wide π-electron delocalization as in single pentacene molecule, Therefore the spatial orientation of individual molecules can effect π-orbital overlap. As a result the bandgap and energy bandwidth are sensitive to the molecular stacking or existing phases. Consequently, there is difficulty in developing all encompassing theory for carrier transport in pentacene [4].

2.1.2 Carrier Transport and Mobility

The carrier mobility (μ_0) is a measure of how easily charge carriers move through a solid. It is the constant of proportionality between average charge carrier velocity and applied electric field ($\nu=\mu_0 E$), dictated by phonon scattering and degree of molecular orbital interaction or overlap. In the case of pentacene, there is no complete delocalization of molecular orbitals throughout the solid. Therefore, the degree of molecular orbital interaction has pronounced impact on carrier mobility.

Pentacene is polymorphic with a triclinic crystal structure where the range of lattice parameters are shown in Table 2.1. Thin films of pentacene are reported to exist in two distinct phases; the "thin film" phase (d_{001}=15.4$\mathring{A}$ [5]) and the "bulk" phase (d_{001}=14.0$\mathring{A}$ [5]) as shown in Figure 2-6. There have been reports of interplanar spacing within the 14.0$\mathring{A}$ -15.4$\mathring{A}$ range.

41
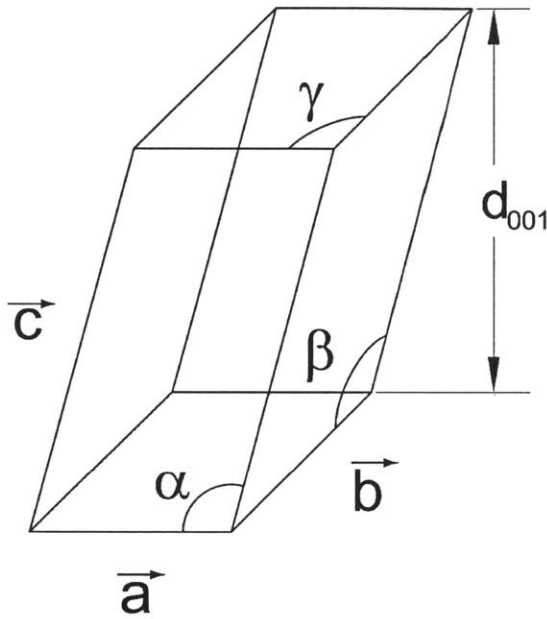
FIGURE 2-5: Triclinic Crystal Lattice
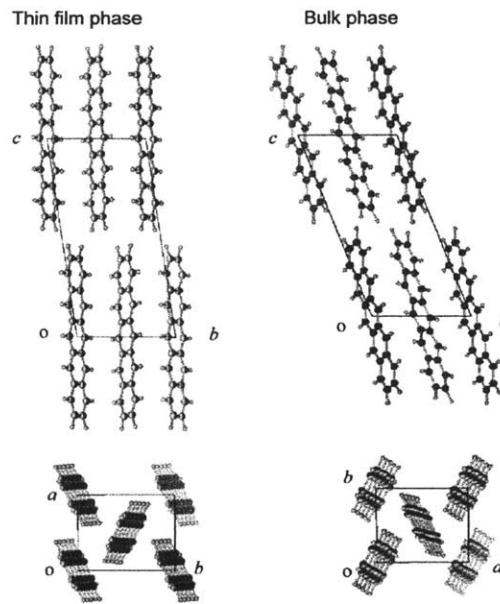
FIGURE 2-6: [001], [010], and [100] planes showing the pentacene thin and bulk phases [6]

Conduction in pentacene occurs inplane on the $\vec{a}\vec{b}$ plane as depicted in Figure 2-7 [6, 7]. From this, it is clear how the orientation and spacing of the molecules on this plane can have a substantial impact on carrier transport. Parisee et. al, reports the bulk phase to be more thermodynamically stable and to have a higher HOMO-LUMO gap, smaller bandwidth (both the HOMO and the LUMO) than the thin film phase (ΔHOMO$_{TOT}$=0.36 for the bulk phase and ΔHOMO$_{TOT}$=0.69 for the thin phase). A smaller bandwidth indicates a larger curvature of radius ($(\partial^2\varepsilon/\partial\vec{k}^2)^{-1}$) and therefore larger effective mass giving rise to lower mobility[4, 7]. The bandwidth of the conduction or valence band can be related to effective mass and therefore carrier

TABLE 2.1: Lattice parameters for a unit cell of pentacene [5]

Lattice Parameter	Distance (Å and °)
$\vec{a}$	6.1 - 7.9
$\vec{b}$	5.9 -7.1
$\vec{c}$	14.4 - 16.1
α	76.8° -101.9°
β	85.0° - 112.7°
γ	84.5° - 91.0°
d_{001}	14.0Å - 15.4Å
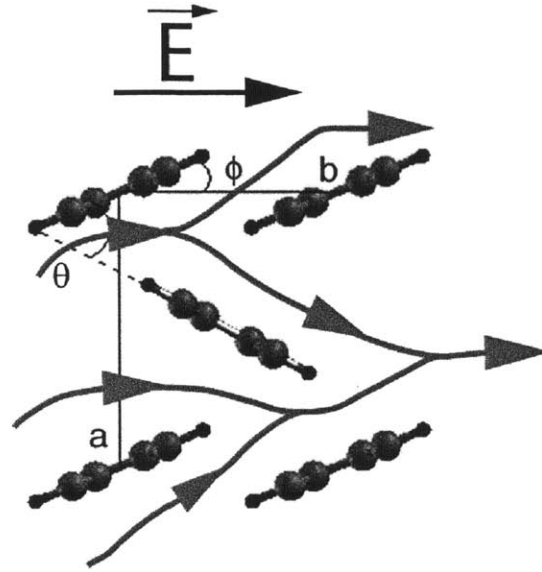
FIGURE 2-7: Conduction in Pentacene. Figure adapted from Parisse et al.[7]

mobility through Equations 2.2, 2.3 and 2.4.

$$bandwidth \propto \left(\frac{\partial^2 \varepsilon}{\partial \vec{k}^2} \right)^{-1} \qquad (2.2)$$

$$\frac{1}{m^*} = \frac{1}{\hbar} \frac{\partial^2 \varepsilon}{\partial \vec{k}^2} \qquad (2.3)$$

$$\mu_0 = \frac{q}{m^*} \tau \qquad (2.4)$$

Where,

    μ_0: carrier mobility

    q: elementary charge

    m^*: effective mass

    τ: relaxation time related to carrier scattering

    $\vec{k}$: is the wave vector

    $\hbar$: h/π

    $\varepsilon(\vec{k})$: energy as a function of the wave vector

Conduction in pentacene is a thermally activated process and there is a pronounced electric field dependence on mobility. For reference in this chapter, the mobility (μ) accounts for defects and tail band states in the solid in addition to carrier mobility (μ_0). Further, thermally evaporated pentacene thin films are typically polycrystalline. Therefore, intergrain as well as intragrain (single grain) charge transport must be considered when evaluating mobility in pentacene.

43

Mobility Within a Crystal: (Intragrain or Field Effect Mobility)

Mobility depends on the applied gate-to-source (V_{GS}) and drain-to-source (V_{DS}) voltages. Charge transport occurs via hopping (variable-range hopping) or the thermally activated tunneling of carriers between localized states (tail band states), as opposed to the promotion of carriers to a transport level (conduction or valence band) as is the case in crystalline semiconductors. Vissenberg et al. reports the applied gate-to-source voltage accumulates charge at the semiconductor/insulator interface. Initially, charges fill the low energy states, such that additional accumulated charges occupy higher energy states. As these charges then have higher energies, there is less additional energy needed for the carrier to hop to the next site. Therefore, the mobility depends on the electric fields in the material [8].
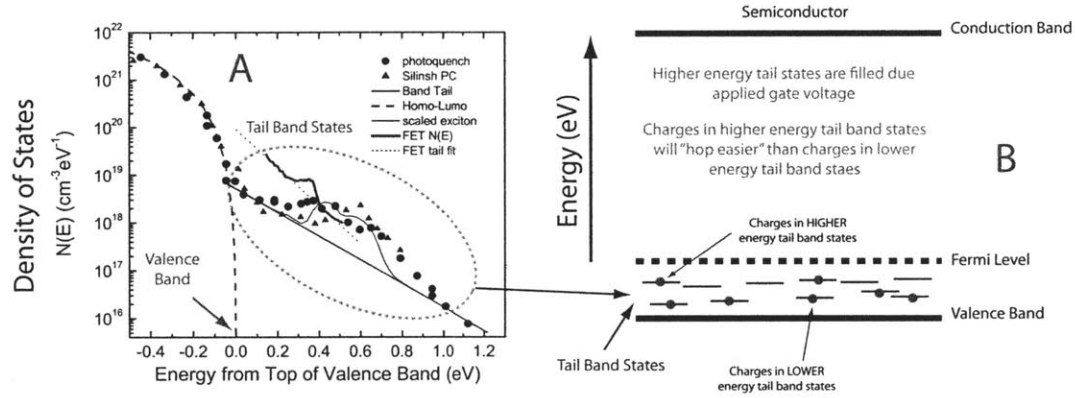
FIGURE 2-8: A) The tail bands as a function of energy measured from the top of the valence band from Lang et al. [9] B) Representation of how tail bands modify the band structure therefore charge transport.

As a result, field effect mobility follows Equation 2.5 [10] where $V_{GS} - V_T$ is a measure of the vertical field applied to the semiconductor/insulator interface.

$$\mu_{FE} = \mu_0 \left[\frac{V_{GS} - V_T}{V_{AA}} \right]^{\xi} \tag{2.5}$$

Where,

μ_{FE}: field effect mobility

μ_0: carrier mobility

V_{GS}: gate voltage

V_T: threshold voltage

V_{AA}: normalizing parameter

ξ: parameter that depends on the energy distribution of localized states ~ 0.5

Mobility and Microstructure: (Intergrain)

If the length, of the semiconductor channel (L) is larger than the average grain size in material, carrier conduct across grain boundaries. Carlo et al. report an expression for μ_I, the intergrain mobility in Equation 2.6 [11], which accounts for conduction across grain boundaries.

$$\mu_I = \mu_{FE} \frac{1}{1 + n_B \beta_G exp(E_B/kT)} \tag{2.6}$$

Where,

μ_{FE}: field effect mobility

E_B: energy barrier height at the grain boundary

β_G: l_G/L (L: channel length, l_G: effective grain boundary size)

n_G: number of grain boundaries in the channel

μ_I: intergrain mobility

Equation 2.6 illustrates how μ_I is a function of grain boundaries by modeling intergrain electron motion as a thermally activated process. E_B is the energy barrier at the grain boundary the carrier must surmount for conduction and it depends on the electric field in the semiconductor and the number of carriers trapped in the boundary. In Equation 2.6, β_G captures the actual size of the grain boundary [12, 13].

There is no simple well accepted expression for mobility in pentacene. The dependence of intragrain transport is debated to be either variable range hopping with lattice polarons (distortions of the lattice enabling conduction) [8, 14, 15, 16, 17] or Frenkel-Poole conduction [18, 19, 20, 21] (distortions of the electric potential field of a trap center enabling conduction). Regarding intergrain transport, thermally activated transport is generally agreed upon [11, 22, 12]; however, interface states and source/drain contact effects may obscure these observations [23]. Regardless, the carrier transport is still susceptible to thin film microstructure and morphology, and electric fields in the solid. As it will be discussed in Chapter 4, surface energy, roughness, and deposition conditions will determine grain size and distribution.

Figure 2-9 shows the evolution of mobility for pentacene based FETs (μ), over the past two decades. A technology review by Kitamura et al. suggests the mobility for single crystal pentacene may be as high as 150 cm^{2}V^{-1} s^{-1}, based on reports from first principle calculations [5], where values for mobility for polycrystalline pentacene films have been reported to be as high as 5.5 cm^{2}V $^{-1}$ s^{-1} [24].

2.2 INSULATOR, SURFACE TREATMENT, ENCAPSULATION: PARYLENE-C

For this dissertation, parylene-C will be used as a gate insulator for high voltage circuit applications (low-κ=3.15 [25]), a surface treatment for shifting threshold voltage in OTFTs based on BZN [26], and a protective encapsulation for patterning pen-
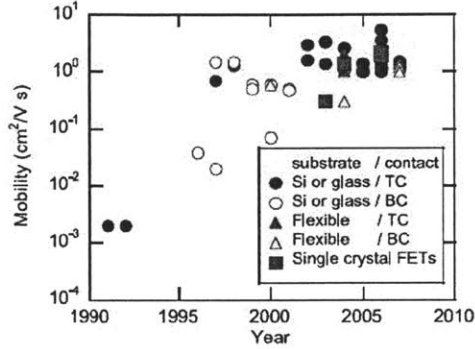
FIGURE 2-9: The increase of field effect mobility of pentacene FETs from 1990 to 2010 [5].

tacene. Parylene-C has the lowest gas permeability and water transmission rate of the available parylene materials from supplier Specialty Coating Systems. Parylene-C is stable in high vacuum, insoluble in organic solvents, and most acids and bases at room temperature making it compatible with photolithography and metal etchants.

2.2.1 Chemical Structure

Parylene is the generic name for members of a specific polymer system typically used as a moisture barrier and insulation for printed circuit boards. The basic member of the system is parylene-N, poly(para-xylylene) which has a high dielectric strength and a low dielectric constant variance with frequency. A derivative of parylene-N used in this work parylene-C, differs from parylene-N by the substitution of the Cl atom for one of the aromatic hydrogens [25]. This is shown in Figure 2-10.

2.2.2 Electronic Structure

Suppliers of parylene-C report UV (ultraviolet) light absorption at ~280 nm [25], which corresponds to a bandgap of 4.42 eV using Equation 2.7. The electron affinity is estimated to be 4.08 eV. According to NIST, the ionization potential for p-Xylene shown in Figure 2-10 is ~8.5 eV[1] [27]. Estimating that this ionization potential is close to that of the parylene-C and the E_{GAP} to be 4.42 eV from photospectrosopy, electron affinity is determined via Equation 2.8. This bandgap and corresponding band offsets show parylene-C to be a viable insulator for pentacene based TFTs.

$$\lambda_{ph} = \frac{hc}{E_{GAP}} \tag{2.7}$$

$$\chi_A = I_P - E_{GAP} \tag{2.8}$$

---

[1] The ionization potential of p-Xylene is not necessarily the same as parylene-C. They have similar structures and therefore may have similar ionization processes.
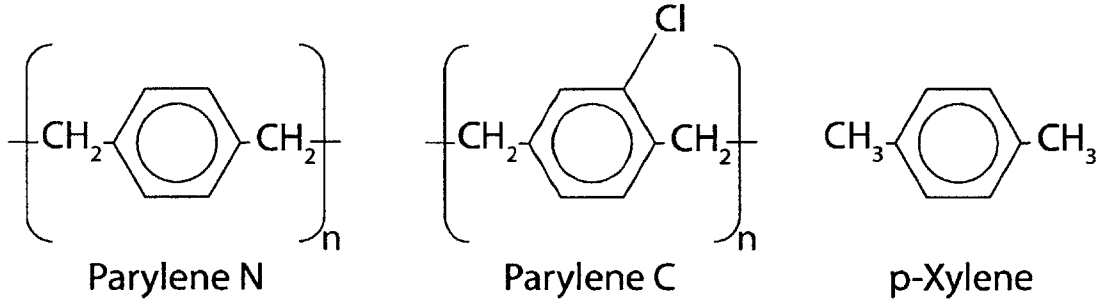
FIGURE 2-10: Molecules of parylene. Parylene-C is used in this work.

Where,

λ_{ph}: wavelength of incident light

h: Planks' Constant

c: speed of light

E_{GAP} : Bandgap

I_P: Ionization Potential

χ_A : Electron Affinity

For large scale integration, the probability of a device being operational is critical to the success of a technology in addition to device design. Gowrisanker et al. evaluated parylene as the gate dielectric for pentacene based TFTs by studying reliability and lifetime using common electrical stress techniques in for Si-based microelectronics [28]. Such studies and reports of integrated circuits based on pentacene based OTFT [29, 30] suggest that parylene is suitable for large scale integration.

2.3 INSULATOR: $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_{7.0}$ (BZN)

BZN is a material of interest as it has a high dielectric constant (κ) with low temperature processing. This makes BZN suitable as a gate insulator in pentacene-based TFTs as the high dielectric constant will enable lower operating voltages and its low temperature processability is compatible with flexible substrates. Choi et. al demonstrated that this material can lower operating voltages in pentacene-based TFTs and the threshold voltage can be shifted with surface treatments [26]. This work adopts this approach to lower the operating voltage in pentacene based TFT device for integrated circuits.

2.3.1 Chemical Structure and Polarization

BZN is a paraelectric cubic pyrochlore which typically serves as an insulator. It is a promising candidate for printed circuit board embedded capacitors [31]. Materials capable of being polarized under an applied electric field are said to be paraelectric. Paraelectricity is typically found in crystalline ceramics. This behavior arises as a result of the physical displacement of the electron cloud from the center of the ionic

nucleus leading to polarization.
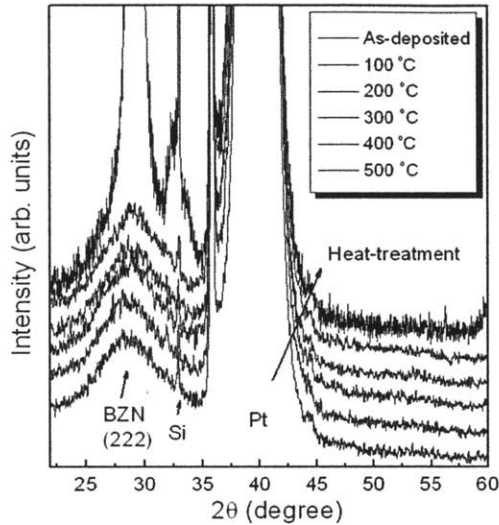
FIGURE 2-11: X-ray diffraction pattern of BZN as a function of annealing temperature [32]
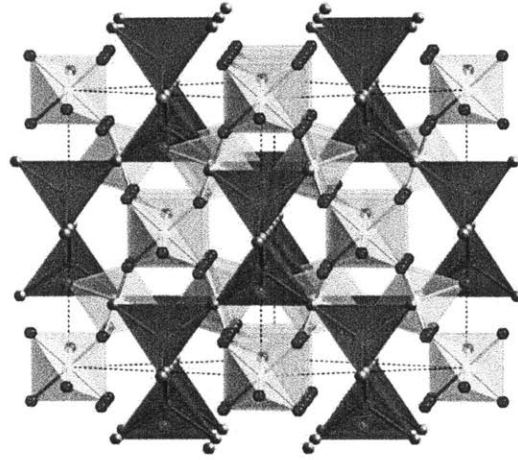
FIGURE 2-12: Ideal $A_2B_2O_6O'$ pyrochlore structure showing two interpenetrating subnetworks: A_2O' tetrahedral in red and the B_2O_6 octahedra in blue [33].

$Bi_{1.5}Zn_1Nb_{1.5}O_7$ is ionic with a cubic pyrochlore ($A_2B_2O_6O'$) crystal structure. Ideal stoichiometric pyrochlores $A_2B_2O_7$ are cubic with space group $Fd\bar{3}m$ and often described as two interpenetrating networks of B_2O_6 octahedra and A_2O' tetrahedral as shown in Figure 2-12 [33, 34]. At low processing temperatures, BZN shows short range order giving rise to a high dielectric constant [32]. Lu et al. reports, nanocrystals of size $\sim$5 nm for as-deposited sputtered films suggesting the extent of this short range order [35]. In the case of non-stoichiometry, different compounds with different phases ($Bi_2Zn_{2/3}Nb_{4/3}O_7$ with a monoclinic zirconolite or orthorhombic pyrochlore structure, $ZnNb_2O_6$ and $Zn_3Nb_2O_8$ compounds) may deteriorate electrical properties of BZN [36, 37, 35]. The cubic phase shows better dielectric properties however this phase tends to appear at annealing temperatures above 400°C [32, 35] as shown in Figure 2-11. Diffraction from the [222] plane is of interest in BZN. Its presence and width suggest degree of crystallinity, composition, and size of crystals [31, 32, 35, 38, 37].

Three different polarization mechanisms (electronic, ionic, and dipolar) can be present in this structure and can contribute to its permittivity as reported by Sudheendran et al. [38]. It is well agreed that the high dielectric constant in these films can be attributed to displacement disorder at the A and O' positions [31, 38, 39]. Park et al. reports that in films deposited at low temperatures, Zn-O provides a significant contribution to the dielectric constant as the Bi-O or Nb-O form at higher temperatures [31].

2.3.2 Current Leakage in BZN

Current leakage in BZN has been attributed two sources, phase inhomogeneity and a low optical band gap. Park et al. report that there is a metallic Bi-rich phase in annealed films deposited at room temperature as the ions lack enough energy to form the stoichiometric film. Fewer Bi atoms are available to bond with O. This reduces the effective dielectric constant and creates a path for current conduction through the dielectric [31]. Deposited BZN films show E_{GAP} values on the order of 3.30 eV to 3.60 eV. The calculated E_{GAP} increases with increasing oxygen pressure during deposition as reported by Sudheendran et al. [38]. The optical band gap increases with annealing, indicating onset of crystallization [38, 40].

Investigators have addressed current leakage issues by fabricating composite stacks which incorporate larger bandgap insulators [41] and composition engineering to control parasitic trap assisted transport [40]. As was shown with parylene, BZN must be evaluated as the gate dielectric for pentacene based TFTs by studying its reliability and lifetime under electrical stress to confirm it's suitability for large scale integration. In Chapter 7, dielectric breakdown in BZN is studied using electrical stress techniques developed that are common in Si-based microelectronics to further support and clarify leakage mechanisms in BZN, and assess the material for large scale integration.

2.4 SOURCE, DRAIN, AND GATE CONTACTS: GOLD (Au)

A conductive material is needed to wire devices to each other and to connect to instrumentation. Gold is used for the devices built in this work for 3 reasons; high conductivity, low reactivity, and efficient carrier injection.

2.4.1 Bulk Properties

High Conductivity

Highly conductive interconnects and wires result in better signal transmission and lower power dissipation is circuits. Common highly conductive metals used in microelectronics are Al (aluminum), Cu (copper), Ag (silver), Au (gold), and W (tungsten). The resistivity of these metals are summarized in Table 2.2.

Low Reactivity

The fabrication process used to build integrated OTFTs prioritizes the electrical performance of the pentacene and the gate insulators, not the contacts. By using a noble metal such as gold, additional processing is not necessary to minimize corrosion and oxidation.

TABLE 2.2: Resistivity of pure metals at room temperature. This table is from Mayer and Lau. [42]

Metal	Atomic Symbol	ρ $10^{-6}\Omega \cdot cm$
aluminum	Al	2.5
copper	Cu	1.6
gold	**Au**	**2.0**
silver	Ag	1.5
tungsten	W	5.6

2.4.2   Efficient Carrier Injection into Pentacene

Injecting carriers from metal contact into the pentacene demands that the work function of the metal (ϕ_M) be close to that of the semiconductor (ϕ_S). An energy band diagram for pentacene on a metal is shown in Figure 2-13. When a metal and an organic material are brought into contact, charge transfers across the interface which creates an electronic interface dipole (E_Δ) and an electric field in the semiconductor [43]. As a result, a charge injection barrier is created. According to Kitamura et al., the expression for this barrier height (E_{BH}) for this injection is given by Equation 2.9 and for the electronic interface dipole (E_Δ) is given by Equation 2.10. From these expressions, increasing ϕ_M will decrease E_{BH}, implying metals with a larger work function such as gold (ϕ_M=5.1eV) will improve charge injection.

$$E_{BH} = (E_{HOMO} - E_\Delta) - \phi_M \qquad (2.9)$$

$$E_{HOMO} = -\frac{(\phi_M - 3.5)}{1.8} \qquad (2.10)$$

Where,

E_{BH}: barrier height for charge injection
E_Δ: electronic interface dipole
E_{HOMO}: energy level of the HOMO level
ϕ_M and ϕ_S: work functions of the metal and the semiconductor

2.5   SUMMARY

SEMICONDUCTOR

Pentacene ($C_{22}H_{14}$) is a linear polycyclic carbon-based molecule consisting of 5(pent) benzene rings (acene).

- Pentacene is a semiconductor because of delocalized π-orbitals. One half of the orbitals are filled with electrons giving rise to distinct energy states that surface as a "conduction band" and "valence band".
- Charge carriers do not conduct through pentacene via band transport.
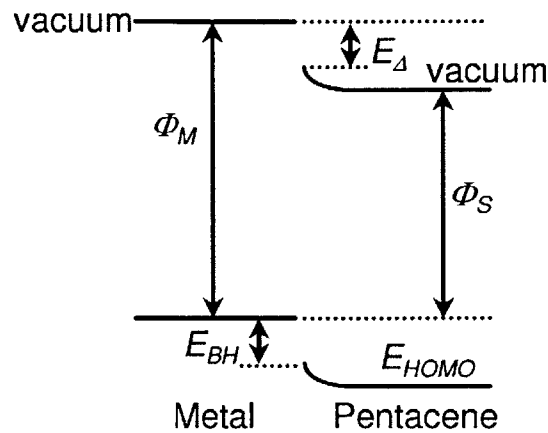
FIGURE 2-13: Energy diagram for pentacene/metal interface [5].

Carries move through the solid by a thermal activated hopping transport suspected to be either Frenkel-Poole or Polaronic.

- Microstructure and morphology dictate electrical performance. This includes crystal structure and grain structure.
  - The "thin film" phase shows higher mobility that the "bulk" phase.
  - Pentacene film with larger grains with small boundaries show higher mobilities. [44, 11].

INSULATORS

Parylene-C deposited at room temperature will serve as a gate insulator, surface treatment and encapsulation.

- These films are pinhole free, conformal, transparent, and stable.
- This insulator is suitable for large scale integration.

BZN will be deposited at room temperature by RF magnetron sputtering with annealing $<150°C$.

- The κ ~40^2 will lower operating voltage (V_{GS}).
- Current leakage is an issue with this material and will be investigated more deeply in Chapter 7.

GATE, SOURCE, AND DRAIN CONTACTS: GOLD

Gold is used as it has a high conductivity, efficiently injects charge carriers into pentacene, and is resistant to corrosion.

---

^{2} Extracted in Chapter 7

VACUUM
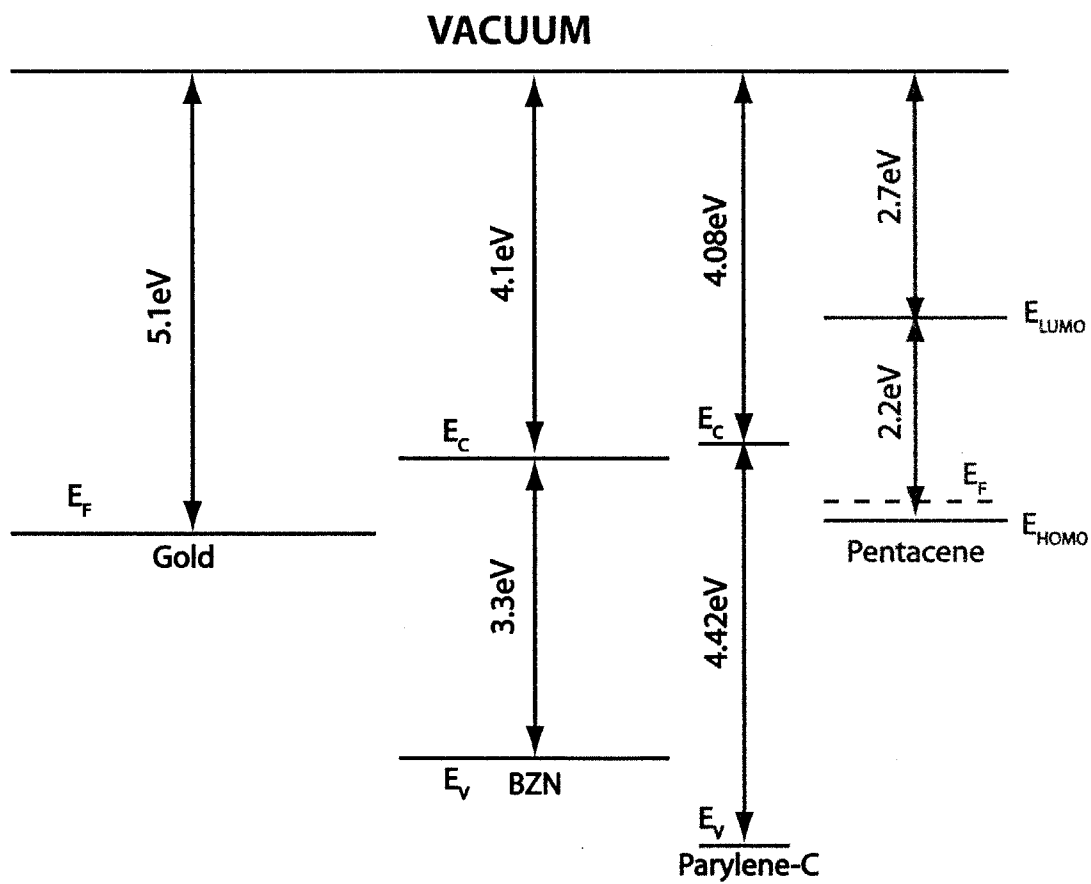
FIGURE 2-14: Energy Band Diagram of Relevant Materials.

TABLE 2.3: Summary of relevant materials properties

Material	BZN	Parylene-C	Pentacene	Au
Purpose	Gate Insulator	Gate Insulator, Passivation, Encapsulation,	Semiconductor	Gate, Source, Drain Contacts
Chemical Formula	$Bi_{1.5}Zn_1Nb_{1.5}O_7$	C_8H_7Cl	$C_{22}H_{14}$	Au
Crystal Structure	Cubic[45]	Amorphous	triclinic [46, 47]	FCC
Band Gap (eV)	3.3 [38, 40]	4.42 [25]	2.2[20]	-
Dielectric Constant	40^3	3.15[20, 25]	3[20]	-
Electron Affinity (eV)	4.1^3	4.08[27]	2.7[20]	-
Work Function (eV)	-	-	-	5.1[5, 20]

---

[2] Determined in Chapter 7

2.6 REFERENCES

[1] P. Vitaly, "Charge carrier transport in single-crystal organic field-effect transistors," in *Organic Field-Effect Transistors*, Optical Science and Engineering, pp. 27–72, CRC Press, 2007.

[2] P. Y. Bruice, *Organic Chemistry*. Prentice Hall, 2002.

[3] P. M. Zimmerman, Z. Zhang, and C. B. Musgrave, "Singlet fission in pentacene through multi-exciton quantum states," *Nat Chem*, vol. 2, no. 8, pp. 648–652. 10.1038/nchem.694.

[4] P. Parisse, L. Ottaviano, B. Delley, and S. Picozzi, "First-principles approach to the electronic structure in the pentacene thin film polymorph," *Journal of Physics: Condensed Matter*, vol. 19, no. 10, p. 106209, 2007.

[5] M. Kitamura and Y. Arakawa, "Pentacene-based organic field-effect transistors," *Journal of Physics-Condensed Matter*, vol. 20, no. 18, 2008.

[6] H. Yoshida, K. Inaba, and N. Sato, "X-ray diffraction reciprocal space mapping study of the thin film phase of pentacene," *Applied Physics Letters*, vol. 90, no. 18, pp. 181930–3, 2007.

[7] P. Parisse, S. Picozzi, M. Passacantando, and L. Ottaviano, "Experiments and theory on pentacene in the thin film phase: structural, electronic, transport properties, and gas response to oxygen, nitrogen, and ambient air," *Thin Solid Films*, vol. 515, no. 23, pp. 8316–8321, 2007.

[8] M. C. J. M. Vissenberg and M. Matters, "Theory of the field-effect mobility in amorphous organic transistors," *Phys. Rev. B*, vol. 57, pp. 12964–12967, May 1998.

[9] D. V. Lang, X. Chi, T. Siegrist, A. M. Sergent, and A. P. Ramirez, "Amorphous-like density of gap states in single-crystal pentacene," *Phys. Rev. Lett.*, vol. 93, p. 086802, Aug 2004.

[10] M. G. Kane, "Organic and Polymeric TFTs for Flexible Displays and Circuits," in *Flexible Electronics* (W. S. Wong and A. Salleo, eds.), vol. 11 of *Electronic Materials: Science and Technology*, pp. 215–260, Springer US, 2009.

[11] A. Di Carlo, F. Piacenza, A. Bolognesi, B. Stadlober, and H. Maresch, "Influence of grain sizes on the mobility of organic thin-film transistors," *Applied Physics Letters*, vol. 86, no. 26, p. 263501, 2005.

[12] G. Horowitz, "Tunnel current in organic field-effect transistors," *Synthetic Metals*, vol. 138, no. 12, pp. 101 – 105, 2003. Organic Materials for Device Applications. Proceedings of Symposium F, E-MRS Spring Meeting 2002, June 18-21, 2002, Strasbourg, France.

[13] J. W. Orton and M. J. Powell, "The hall effect in polycrystalline and powdered semiconductors," *Reports on Progress in Physics*, vol. 43, no. 11, p. 1263, 1980.

[14] M. Hultell and S. Stafstrm, "Polaron dynamics in highly ordered molecular crystals," *Chemical Physics Letters*, vol. 428, no. 46, pp. 446 – 450, 2006.

[15] D. Emin, "Formation and hopping motion of molecular polarons," *Phys. Rev. B*, vol. 61, pp. 14543–14553, Jun 2000.

[16] K. Hannewald and P. A. Bobbert, "Anisotropy effects in phonon-assisted charge-carrier transport in organic molecular crystals," *Phys. Rev. B*, vol. 69, p. 075212, Feb 2004.

[17] P. J. Freud, "Electric-field-dependent conductivity for hopping-type charge transport," *Physical Review Letters*, vol. 29.

[18] J. Frenkel, "On pre-breakdown phenomena in insulators and electronic semiconductors," *Physical Review*, vol. 54, no. 8, pp. 647–648, 1938.

[19] L. Wang, D. Fine, D. Basu, and A. Dodabalapur, "Electric-field-dependent charge transport in organic thin-film transistors," *Journal of Applied Physics*, vol. 101, no. 5, pp. 054515-8, 2007.

[20] W. T. Wondmagegn, N. T. Satyala, I. Mejia-Silva, D. Mao, S. Gowrisanker, H. N. Alshareef, H. J. Stiegler, M. A. Quevedo-Lopez, R. J. Pieper, and B. E. Gnade, "Experimental and modeling study of the capacitance voltage characteristics of metal insulator semiconductor capacitor based on pentacene/parylene," *Thin Solid Films*, vol. 519, no. 13, pp. 4313–4318.

[21] W. Wondmagegn and R. Pieper, "Simulation of top-contact pentacene thin film transistor," *Journal of Computational Electronics*, vol. 8, no. 1, pp. 19–24, 2009.

[22] G. Horowitz and M. Hajlaoui, "Grain size dependent mobility in polycrystalline organic field-effect transistors," *Synthetic Metals*, vol. 122, no. 1, pp. 185 – 189, 2001. Proceedings of the E-MRS 2000 Spring Meeting, Symposium I.

[23] S. F. Nelson, Y.-Y. Lin, D. J. Gundlach, and T. N. Jackson, "Temperature-independent transport in high-mobility pentacene transistors," *Applied Physics Letters*, vol. 72, no. 15, pp. 1854–1856, 1998.

[24] S. Lee, B. Koo, J. Shin, E. Lee, H. Park, and H. Kim, "Effects of hydroxyl groups in polymeric dielectrics on organic transistor performance," *Applied Physics Letters*, vol. 88, no. 16, p. 162109, 2006.

[25] Specialty Coating Systems, "SCS Parylene Properties." Promotional brochure, 2010.

[26] Y. Choi, I. D. Kim, H. L. Tuller, and A. I. Akinwande, "Low-voltage organic transistors and depletion-load inverters with high-κ pyrochlore BZN gate dielectric on polymer substrate," *IEEE Transactions on Electron Devices*, vol. 52, no. 12, pp. 2819–2824, 2005.

[27] S. Lias, *p-Xylene*. NIST Standard Reference Database 69: NIST Chemistry WebBook, NIST: Materials Measurement Laboratory, 2011.

[28] S. Gowrisanker, M. A. Quevedo-Lopez, H. N. Alshareef, and B. E. Gnade, "Time dependent breakdown characteristics of parylene dielectric in metal insulator metal capacitors," *Organic Electronics*, vol. 10, no. 5, pp. 1024–1027, 2009.

[29] I. Kymissis, A. I. Akinwande, and V. Bulovic, "A lithographic process for integrated organic field-effect transistors," *Journal of Display Technology*, vol. 1, no. 2, pp. 289–294, 2005.

[30] I. Nausieda, K. K. Ryu, D. Da He, A. I. Akinwande, V. Bulovic, and C. G. Sodini, "Mixed-signal organic integrated circuits in a fully photolithographic dual threshold voltage technology," *IEEE Transactions on Electron Devices*, vol. 58, no. 3, pp. 865–873, 2011.

[31] J. H. Park, W. S. Lee, N. J. Seong, S. G. Yoon, S. H. Son, H. M. Chung, J. S. Moon, H. J. Jin, S. E. Lee, J. W. Lee, H. D. Kang, Y. K. Chung, and Y. S. Oh, "Bismuth-zinc-niobate embedded capacitors grown at room temperature for printed circuit board applications," *Applied Physics Letters*, vol. 88, no. 19, 2006.

[32] I. D. Kim, M. H. Lim, K. Kang, H. G. Kim, and S. Y. Choi, "Room temperature fabricated ZnO thin film transistor using high-κ $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_{7.0}$ gate insulator prepared by sputtering," *Applied Physics Letters*, vol. 89, no. 2, p. 3, 2006.

[33] B. B. Hinojosa, J. C. Nino, and A. Asthagiri, "First-principles study of cubic Bi pyrochlores," *Physical Review B*, vol. 77, no. 10, p. 104123, 2008.

[34] I. Levin, T. G. Amos, J. C. Nino, T. A. Vanderah, C. A. Randall, and M. T. Lanagan, "Structural study of an unusual cubic pyrochlore $Bi_{1.5}Zn_{0.92}Nb_{1.5}O_{6.92}$," *Journal of Solid State Chemistry*, vol. 168, no. 1, pp. 69–75, 2002.

[35] J. W. Lu, Z. Q. Chen, T. R. Taylor, and S. Stemmer, "Composition control and dielectric properties of bismuth zinc niobate thin films synthesized by radio-frequency magnetron sputtering," *Journal of Vacuum Science and Technology A*, vol. 21, no. 5, pp. 1745–1751, 2003.

[36] D. Shihua, Y. Xi, and Y. Li, "Study of structure and dielectrc properties of non-stoichiometric Bi_2O_3-ZnO-Nb_2O_5 ceramics," *Journal of Electroceramics*, vol. 21, no. 1, pp. 435–438, 2008.

[37] X. L. Wang, H. Wang, and X. Yao, "Structures, phase transformations, and dielectric properties of pyrochlores containing bismuth," *Journal of the American Ceramic Society*, vol. 80, no. 10, pp. 2745–2748, 1997.

[38] K. Sudheendran, M. Ghanashyam Krishna, and K. Raju, "Effect of process parameters and post-deposition annealing on the microwave dielectric and optical properties of pulsed laser deposited $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ thin films," *Applied Physics A: Materials Science and Processing*, vol. 95, no. 2, pp. 485–492, 2009.

[39] Nino, C. Juan, Youn, J. Hyuk, Lanagan, T. Michael, Randall, and A. Clive, *Bi_2O_3 solubility of Bi-based pyrochlores and related phases*, vol. 17. Cambridge, ROYAUME-UNI: Cambridge University Press.

[40] N. G. Cho, H. Seo, D. H. Kim, H.-G. Kim, J. Kim, and I.-D. Kim, "Characterization on bandedge electronic structure of MgO added $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_{7.0}$ gate dielectrics for ZnO-thin film transistors," *Electrochemical and Solid-State Letters*, vol. 14, no. 1, pp. G4–G7.

[41] M.-H. Lim, K. Kang, H.-G. Kim, I.-D. Kim, Y. Choi, and H. L. Tuller, "Low leakage current-stacked MgO/$Bi_{1.5}Zn_{1.0}Nb_{1.5}O_{7.0}$ gate insulator— for low voltage ZnO thin film transistors," *Applied Physics Letters*, vol. 89, no. 20, pp. 202908–3, 2006.

[42] J. Mayer and S. Lau, *Electronic materials science: for integrated circuits in Si and GaAs*. Macmillan, 1990.

[43] H. Peisert, M. Knupfer, and J. Fink, "Energy level alignment at organic/metal interfaces: Dipole and ionization potential," *Applied Physics Letters*, vol. 81, no. 13, pp. 2400–2402, 2002.

[44] S. Y. Yang, K. Shin, and C. E. Park, "The Effect of Gate-Dielectric Surface Energy on Pentacene Morphology and Organic Field-Effect Transistor Characteristics," *Advanced Functional Materials*, vol. 15, no. 11, pp. 1806–1814, 2005.

[45] D. H. Back, Y. S. Lee, Y. P. Hong, J. H. M. Moon, and K. H. Ko, "Tunability of Bi-rich bzn cubic pyrochlore thin films by reactive sputtering," in *MATERIALS RESEARCH SOCIETY SYMPOSIUM*, vol. 783, 2004.

[46] R. Ruiz, D. Choudhary, B. Nickel, T. Toccoli, K. C. Chang, A. C. Mayer, P. Clancy, J. M. Blakely, R. L. Headrick, S. Iannotta, and G. G. Malliaras, "Pentacene thin film growth," *Chem. Mater.*, vol. 16, no. 23, pp. 4497–4508, 2004.

[47] F. Y. S. T. Sadowski J. T., Al-Mahboob A., "Nucleation and growth of thin pentacene films studied by LEEM and STM," Wednesday, July 02, 2008 2008.

Chapter 3

Device Physics and Parameter Extraction

A field effect transistor (FET) is a three-terminal device (source, gate, and drain) where the current between the source and drain of the device is controlled by a voltage applied between the gate and source as shown in Figure 3-1. The FET performs two basic functions in electronic circuits, switching and amplification. This dissertation concentrates on the use of FETs as switches in digital systems. The circuit schematic the OTFT is shown in Figure 3-1.
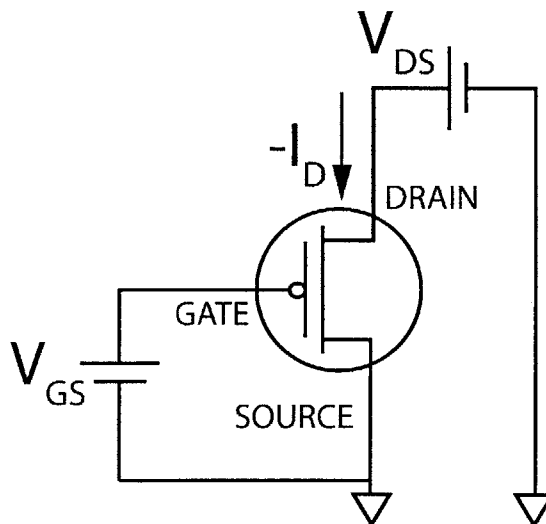
FIGURE 3-1: Circuits schematic of a p-channel field effect transistor

In this chapter, the relevant physics that dictate FET operation will be discussed. For the purpose of this dissertation, key device performance targets will be large drain currents at low operating voltages, tunable threshold voltages for efficiently integrating OTFTs for logic circuits. This is achieved through the engineering of the gate insulator. The relevant figures of merit for the devices in this dissertation are (1) threshold voltage (V_T), (2) mobility (μ), (3) subthreshold swing (S). These figures of merit and their extraction will also be discussed in detail in this chapter.

1. Threshold voltage (V_T) can be defined as the gate-to-source voltage (V_{GS}) necessary to accumulate a channel of charge carriers in the semiconductor. Beyond the threshold voltage, the devices is said to be "on".

2. Mobility (μ) is a measure of the ease in which charge carriers move through the semiconductor channel in the device, in response to an applied electric field between the source and drain.

3. Subthreshold Slope (S) quantifies the efficiency by which the device turns on and off. A "subthreshold" regime exists between the distinct "on" and "off" regimes where the device is neither distinct"on" nor "off". It is the transition between the distinct "on" and "off" regimes.

3.1 DEVICE PHYSICS

3.1.1 Metal-Insulator-Semiconductor Capacitor

A Metal-Insulator-Semiconductor (MIS) capacitor is made by defining the gate electrode (metal) followed by stacking the insulator and the semiconductor as shown in Figure 3-2. By placing source/drain electrodes on both sides of the semiconductor, a field effect transistor structure is created that can support a current (I_D). This current, I_D is controlled by the gate-to-source voltage (V_{GS}) and the drain-to-source voltage (V_{DS}). How the charge accumulates (V_{GS}) in the channel determines how the current (I_D) will flow through the OTFT in response to the drain-to-source voltage (V_{DS}).

Flatband Voltage (V_{FB}) and Threshold Voltage (V_T)
In the absence of traps due to interface states and grain boundaries, when applying a gate-to-source voltage (V_{GS}), a portion of the voltage is dropped across the gate insulator, the rest is dropped in the semiconductor. To turn on an FET, charge carriers must be accumulated at the semiconductor/insulator interface, by applying the appropriate gate-to-source voltage. Accumulation or "on" is shown in a MIS capacitor in Figure 3-2 (A).

To turn the device off, the channel must be depleted of conducting charges, by reducing the gate-to-source voltage. Depletion or "off" is shown in Figure 3-2 (B).
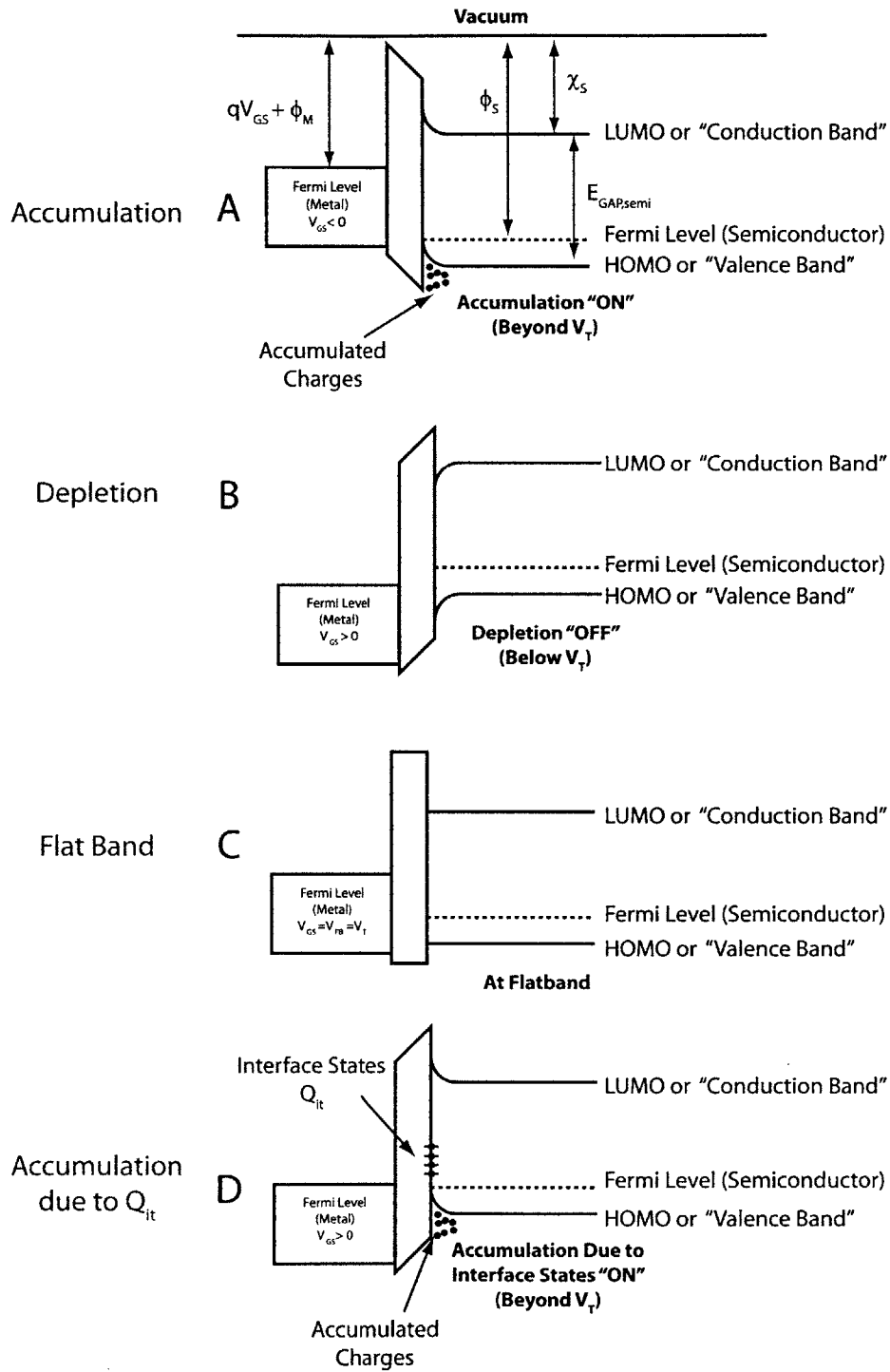
FIGURE 3-2: Band diagrams for MOS structure comparing (A) Accumulation due to V_{GS}, (B) Depletion due to V_{GS}, (C) Flatband due to V_{GS} and (D) Accumulation as a result of interface states (V_{GS} here is the same as V_{GS} in B). For this illustration, I_D is flowing into or out of the page.

The minimum gate-to-source voltage necessary to turn the device on or the maximum gate-to-source voltage that can be applied while the device remains off is the flatband voltage (V_{FB}). Flatband is defined as the condition where there is no electric field in the semiconductor, or the conduction and valence bands are flat. The electric field in the material is proportional to the slope of the conduction or valence bands of that material. Flatband is shown in Figure 3-2 (C).

For thin film transistors and other field effect transistors that operate in accumulation the flatband voltage is the gate-to-source voltage where the semiconductor at the insulators/semiconductor interface changes from depletion to accumulation where a conducting channel is formed. Therefore in the absence of traps due to interface states and grain boundaries, the flatband voltage is numerically equal to the threshold voltage, where all accumulated charge in the channel contributes to drain current (I_D). The presence of interface states (Q_{it}), alters how charge is accumulated in the channel at a given gate-to-source voltage. These interface states can be charged and therefore change the way the electric field and therefore the gate-to-source voltage is distributed in the insulator and semiconductor. The interface states or traps have to be filled before an accumulation layer of mobile carriers can form. This is shown in Figure 3-2 (D).

Equation 3.1 [1] gives a generally accepted expression for the V_{FB} in a field effect transistor. It is simply the summation of the potential difference between the work functions of the semiconductor (ϕ_S) and the gate metal (ϕ_M), and the voltage dropped in the gate insulator (t_{OX}, Q_{OX}) with the influence of interface states (Q_{it}).

$$V_{FB} = (\phi_M - \phi_S) - \frac{t_{OX}}{\epsilon_o \kappa}(Q_{it} - Q_{OX}) = V_T \qquad (3.1)$$

Where,

ϕ_M and ϕ_S: work functions of the gate metal and the semiconductor

ϵ_o: permittivity of Free Space (8.85×10^{14})

κ: dielectric constant of the insulator

Q_{it} : surface charge density at the interface between insulator and the semiconductor

Q_{OX}: $= \int_0^{t_{OX}} \frac{t}{t_{OX}}\rho_{OX}(t) \cdot dt$

ρ_{OX}: charge density per unit volume in the insulator

t_{OX} : thickness of the insulator

Q_{OX}, is not a sheet charge. However, by integrating the charge volume density ($\rho_{OX}(t)$) over the thickness (t_{OX}) of the oxide, and evaluating the integral at interfaces, Q_{OX} can be treated as a sheet charge mathematically.

It is clear from Equation 3.1 that many variables can modify V_T. In this dissertation, threshold voltage is controlled by two methods; altering the dielectric constant (κ) and modifying the interface states at the insulator/semiconductor interface (Q_{it}).

Using a high-κ dielectric reduces the voltage dropped in the gate insulator, so more is dropped in the semiconductor causing accumulation at lower gate-to-source voltages (V_{GS}) . For the second method, the interface states pin the potential at the insulator/semiconductor interface as seen in Figure 3-2 (D). The exact quantitative amount of voltage that must be dropped in the semiconductor for charges to be accumulated depends on how the applied voltage (or electric field in the semiconductor) modifies the equilibrium charge concentration (ϕ_S) in the semiconductor. The details of this are beyond the scope of this work. However, threshold voltage can still be engineered qualitatively using Equation 3.1 without an aggressive analysis of the nonequilibrium behavior of the semiconductor.

Accumulation vs. Inversion
Pentacene behaves like a p-type semiconductor without any sort of intentional doping. Pentacene cannot be inverted, due to the excessive deep traps created by interface states, tail band states that exist due to general disorder, and bulk defects such as grain boundaries. The Shockley-Hall-Read recombination rate is extremely high and a minority carrier population is unable to form in pentacene. This is similar to a-Si. As OTFTs based on pentacene operate in accumulation, a negative voltage must be applied to the gate to create a conducting channel of positive charges ($V_{GS} <$ 0). The vast majority of field effect transistors operate in inversion where minority charge carriers collect at the insulator/semiconductor interface (i. e. positive charge carriers in n-type Si). Despite this difference, pentacene OTFTs have similar electrical characteristics to MOSFETs that run in inversion. The difference between inversion and accumulation is shown in Figure 3-3.
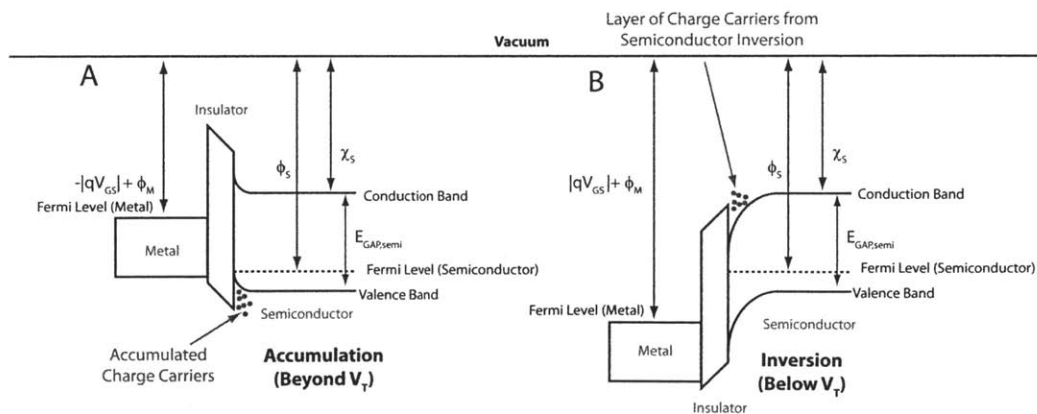
FIGURE 3-3: (A) Charges are "accumulated" at the semiconductor/insulator interface to create a conducting channel. In a MOSFET (B), charges are "inverted". For this illustration, I_D is flowing into or out of the page.

3.1.2 Field Effect Transistor

Placing source and drain electrodes on both sides of the semiconductor channel of the MIS capacitor as shown in Figure 3-5 and Figure 3-4 creates the field effect transistor. The relevant geometrical parameters and superimposed circuit diagram are shown in Top View and in Cross section in Figure 3-4 and Figure 3-5, respectively. The size of the semiconductor channel is geometrically defined by width (W) and channel length (L) in Figure 3-5. The electrical behavior of all transistors is characterized using two current-voltage characteristics that are of fundamental significance. They are the Output Characteristic and the Transfer Characteristic.
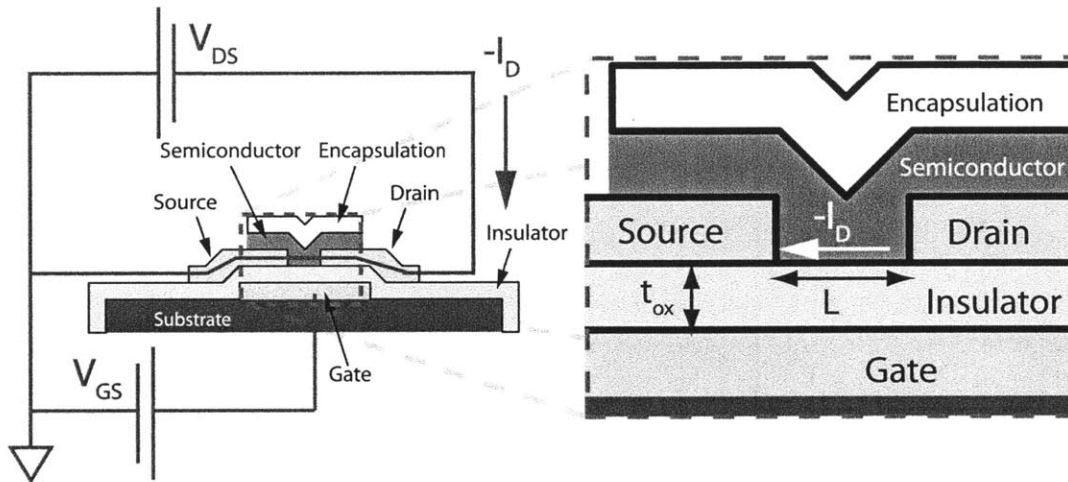
FIGURE 3-4: Cross Section of OTFT

3.1.3 Current-Voltage Behavior

Output Characteristic

For the Output Characteristic (See Figure 3-6) (Plot I_D vs. V_{DS}), V_{DS} is swept while V_{GS} is stepped and I_D is measured. This characteristic verifies gate control, effective switching, and adequate isolation of the gate from the source and drain electrodes. The Output Characteristics display two definitive operating regimes, the linear regime and saturation regime which are delineated in Figure 3-6. In an ideal device, in the linear regime I_D will increase with increasing V_{DS}. Beyond a certain V_{DS} ($>V_{DS,sat}$) the device is said to be in saturation, where I_D is independent of V_{DS} and is constant or saturate at a value of $I_{D,sat}$. This saturation occurs when $V_{DS} \geq V_{GS} - V_T$. When, $V_{DS} = V_{GS} - V_T$, the region of the channel close to the drain is depleted of charges. Additional drain-to-source voltage, depletes more of the channel as opposed to increasing the drain current (I_D).
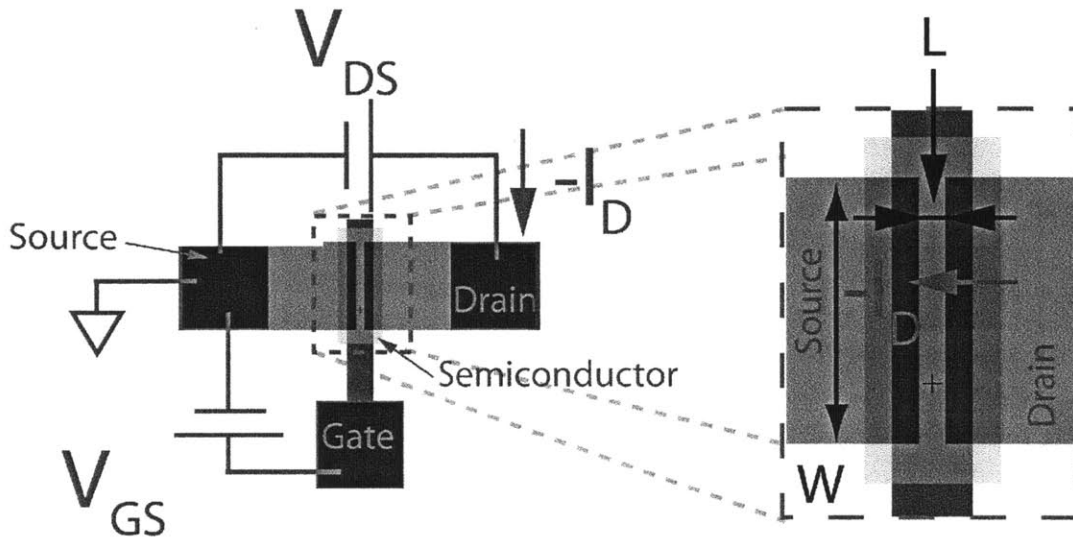
FIGURE 3-5: Top View of OTFT
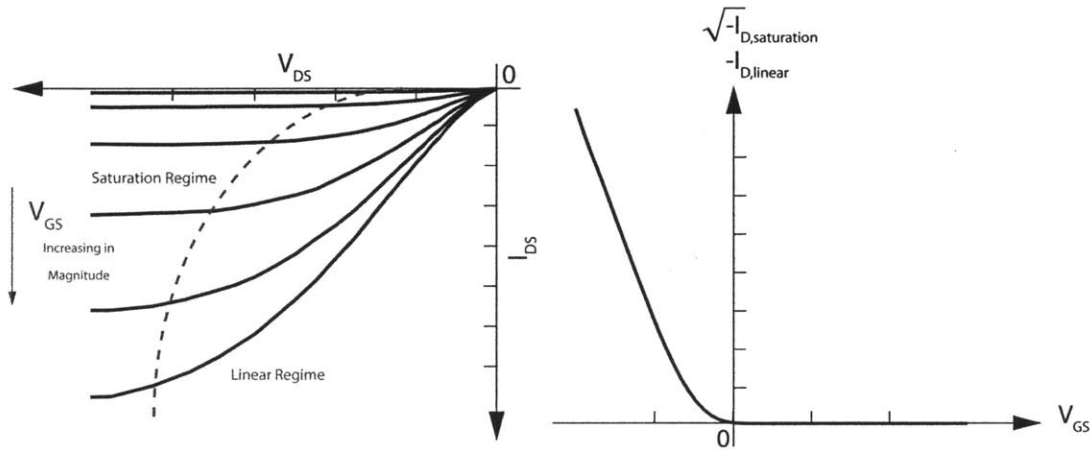
FIGURE 3-6: Output Characteristic of an OTFT. V_{DS} is swept while V_{GS} is stepped and I_D is measured. This characteristic verifies gate control, effective switching, and adequate isolation of the gate from the source and drain electrodes.

FIGURE 3-7: Transfer Characteristics of an OTFT. V_{GS} is swept while measuring I_D and V_{DS} is stepped. The Transfer Characteristic provides insight into how the gate (V_{GS}) controls the current (I_D) in the device and is used to extract device parameters.

Transfer Characteristic

The second current-voltage characteristic is the Transfer Characteristic (See Figure 3-7) (Plot I_D vs. V_{GS}) where V_{GS} is swept while measuring I_D and V_{DS} is stepped. The Transfer Characteristic provides insight into how the gate (V_{GS}) controls the current (I_D) in the device and is used to extract device parameters.

3.2 FIGURES of MERIT: PARAMETER EXTRACTION

3.2.1 Threshold Voltage: V_T

Classically, the drain current has a linear dependence or a square law dependence on gate-to-source voltage and the change in the capacitance of the MIS structure from the "on" state to "off" state follows the current (high current, high capacitance to low current, low capacitance). This can be referred to as the Si Long Channel MOSFET Model. Interface states (Q_{it}) can disrupt charge transport in the channel of the semiconductor, by trapping charge carriers and as was mentioned earlier, the tail band states cause the mobility in the channel and therefore drain current to be field dependent. As a result, the accumulated charge in the channel does not translate proportionally to the density of mobile carriers and hence the drain current. This complicates the extraction of a well defined threshold voltage using the Si Long Channel MOSFET Model, as it relies on measuring current through the accumulated channel or capacitance of the MIS structure. Thus, the definition of V_T itself deviates from what is predicted by the flatband condition shown in Figure 3-2 (C).

The creation of a conducting channel is a continuous event, hence the existence of a "subthreshold" regime. This regime occurs over a range of gate-to-source voltages (V_{GS}). A practical way of defining the threshold voltage is when I_D/W reaches a value high enough to perform switching functions in a circuit. In this approach, the focus is on identifying when the current - voltage behavior deviates from "off" characteristics. For this dissertation, V_T will be defined and extracted in two different ways; a device physics approach based on the change of the drain current dependence on gate-to-source voltage (I_D (V_{GS})) and a classical model based approach where extraction will be taken at likely circuit operating conditions. These two extraction methods are illustrated in Figure 3-8.

1. SI LONG CHANNEL MOSFET MODEL This method of extracting V_T is widely used and accepted. The threshold voltage is extracted by extrapolating a fitting line to $I_D = 0$, for the linear regime and $\sqrt{I_D}=0$ for the saturation regime, as shown in Figure 3-8. This method for extracting V_T depends heavily on the V_{GS} and V_{DS} values from which it was extracted, which is shown in Figure 3-9 [2, 3] as mobility is field dependent. However, if extracted at the likely device operating voltages, it can provide an accurate prediction of circuit performance.

2. SUBTHRESHOLD LINEAR REGRESSION Ryu et al. suggests a method of extracting threshold voltage to that is not subject to inaccuracies and discrepancies caused by the field effect mobility and interface states as illustrated in Figure 3-9 [3]. Threshold voltage can be defined as the change in the functionality of $I_D(V_{GS})$ or at the V_{GS} where the OTFT transitions from "subthreshold" to "on". In Figure 3-8, the change in slope from "subthreshold" to "on" is used
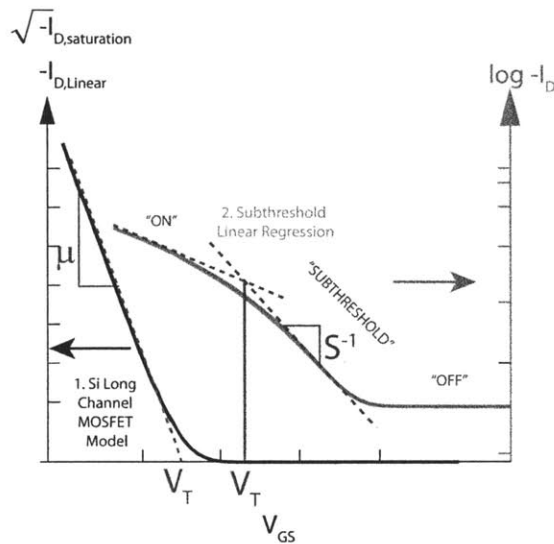
FIGURE 3-8: Illustration of subthreshold linear regression and Si Long Channel MOSFET Model for extraction of threshold voltage.
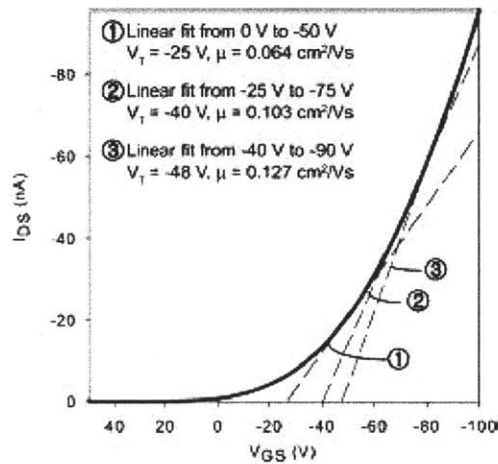
FIGURE 3-9: Extracting mobility and threshold voltage using the Si Long Channel MOSFET Model for three different V_{GS} ranges. Extracted mobility and the threshold voltage vary significantly depending on location of linear fit [2].

to determine V_T. An exact value for V_T is extracted by performing a linear regression in the "on" regime and the "subthreshold" regime and finding point of intersection of the two. This method removes the complexities from field dependencies, tail band states, and interface states; however, it is not representative of device operating conditions, leading to a less accurate prediction of circuit performance.

From Figures 3-8 and 3-9 extracting V_T may seem subjective. However, V_T can be still be engineered using Equation 3.1. For completeness, both methods of extracting V_T are used in this work.

3.2.2 Mobility: μ

Expressions for current through the TFT in the linear and saturated regimes or the Si Long Channel MOSFET Model are shown below. Mobility is extracted by taking the slope of the I_D vs. V_{GS} in the linear regime or the slope of $\sqrt{I_D}$ vs. V_{GS} in the saturation regime.

Equations governing I_D behavior in these regimes are,

$$-I_D = \frac{\mu W \kappa \epsilon_o}{L t_{ox}} \left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{3.2}$$

In the linear regime, $V_{DS} \ll V_{GS} - V_T$

$$I_{D,linear} = \frac{\mu W \kappa \epsilon_o}{L t_{ox}} \left[(V_{GS} - V_T)V_{DS} \right] \tag{3.3}$$

In the saturation regime, $V_{DS} > V_{GS} - V_T$

$$I_{D,saturation} = \frac{\mu W \kappa \epsilon_o}{2 L t_{ox}} \left[(V_{GS} - V_T)^2 \right] \tag{3.4}$$

Where,

    I_D: drain current
    μ: mobility
    W: channel width
    L: channel length
    C_i: Capacitance per unit area for the gate insulator
    V_T: threshold voltage
    V_{GS}:gate-to-source voltage
    V_{DS}: drain-to-source voltage

There is no all inclusive expression for mobility in pentacene which can be inserted into Equations 3.3 and 3.4. Mobility also depends on V_{DS}, though this dependence is not well understood [4]. Beyond the intricacies of mobility and its dependence on microstructure and morphology, carrier scattering caused the gate dielectric surface roughness and coulombic interaction with fixed charges in the insulator [1] can be also an complicate matching extracted values to those predicted by Equations 2.6 and 2.5 discussed in Chapter 2.

3.2.3 Subthreshold Swing: S

In the transition from the "on" state to the "off" state, the TFT enters the "subthreshold" regime where current evolves exponentially with gate-to-source voltage as shown in Equation 3.5. The slope of this transition region (or subthreshold swing),

quantifies how effectively the semiconductor can be depleted of charges or how efficiently the device turns off (smallest current value the devices will support). More technically, it is a measure of how much gate-to-source voltage is needed to change the current by an order of magnitude, which is expressed in Equation 3.6. This value will be extracted at the maximum (note that the subthreshold swing is the inverse the subthreshold slope) slope in the "subthreshold" regime as shown in Figure 3-10. For a device design, a small subthreshold swing is desirable.

Drain currents in the subthreshold regime follows [4],

$$I_{D,sub} = \frac{W}{L} K \mu C_i (1 - e^{-qV_{DS}/kT}) e^{qV_{GS}/nkT} \tag{3.5}$$

$$S = \frac{\partial V_{GS}}{\partial log(I_{D,sub})} = ln10 \frac{\partial V_{GS}}{\partial ln(I_{D,sub})} \tag{3.6}$$

$$S = nkTln(10) \tag{3.7}$$

Where,

$I_{D,sub}$: subthreshold current
μ: mobility
W: channel width
L: channel length
C_i: Capacitance per unit area of the gate insulator
V_T: threshold voltage
V_{GS}: the source-gate voltage
V_{DS}: source-drain voltage
q: elementary charge
k: Boltzmann's constant
T: temperature
n: ideality factor, this is effected by interface states (Q_{it})
K: materials and device structure dependent constant
S: subthreshold swing

The effect of interface states (Q_{it}) on subthreshold swing is reflected in the ideality factor(n) in Equation 3.5, where more charges imply a larger slope and larger ideality factor as shown in Figure 3-10. Subthreshold swing is related to ideality factor through Equation 3.7.

Interface states (Q_{it}) at the insulator/semiconductor interface serve as traps for charge carriers in the semiconductor. These are NOT tail band states and are located deeper in the bandgap. Excess gate voltage is needed to release the charge carriers from these traps. In a device with a small subthreshold swing, the channel is completely depleted at a small gate-to-source voltage below the V_T and is said to be "off". Excess trapped charges at the insulator/semiconductor interface will require a larger gate-to-source voltage below V_T to completely deplete the channel of charges. These interface states or traps can be the same defects (Q_{it}) used to shift the threshold voltage.
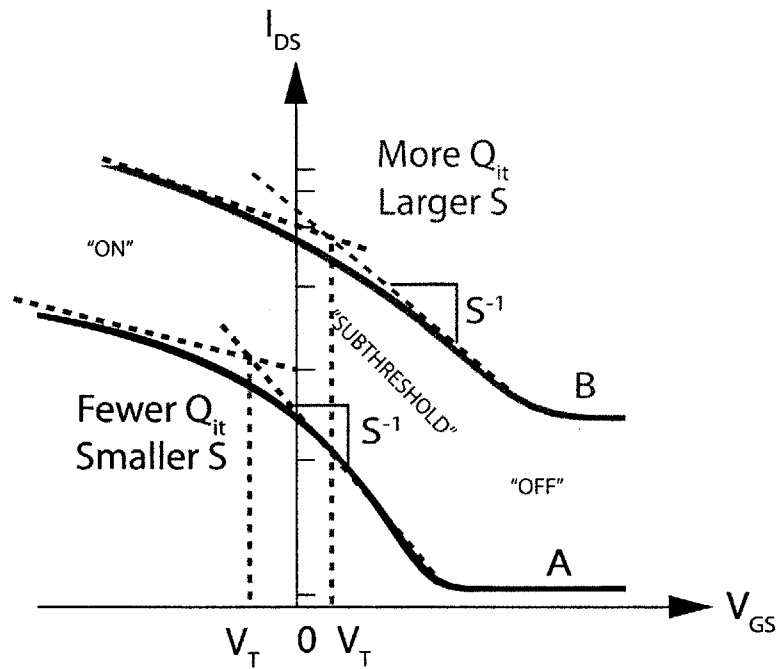
FIGURE 3-10: Variation in subthreshold swing with interface states (Q_{it})

Therefore, one can expect a change in the subthreshold swing as a result of surface modifications. The density of interface states Q_{it} is proportional to the subthreshold swing via Equations 3.8 [1], 3.10, 3.11, and 3.12. Q_{it} cannot be extracted directly from the subthreshold swing. Interface states are manifested as states within the semiconductor bandgap as shown in Figure 3-11.
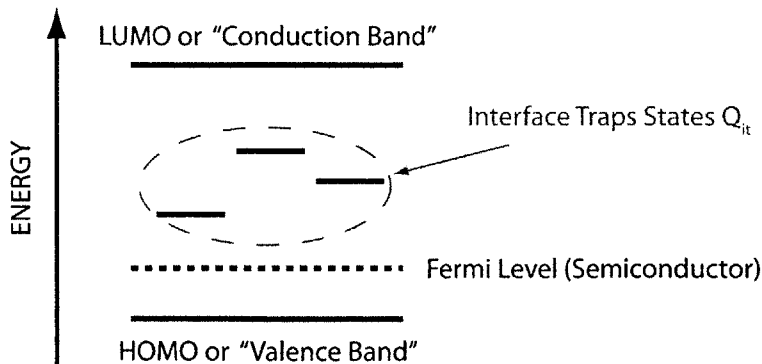
FIGURE 3-11: Interface states (Q_{it}) in bandgap. These are not tail band states and are located deeper in the bandgap. Excess gate voltage is needed to release the charge carriers from these traps.

$$S = ln(10)\frac{kT}{q}\left(1 + \frac{C_d + C_{it}}{C_i}\right) \tag{3.8}$$

In the case that there are no interface states, $C_{it} = 0$ and ideally S with be,

$$S_{ID} = ln(10)\frac{kT}{q}\left(1 + \frac{C_d}{C_i}\right) \tag{3.9}$$

Where n can be related to C_{it} with Equations 3.7 and 3.8 by,

$$n = \frac{1}{q}\left(1 + \frac{C_d + C_{it}}{C_i}\right) \tag{3.10}$$

$$D_{it} = \frac{C_{it}}{q} = (S - S_{ID})\frac{q}{kT}\frac{1}{ln10} \tag{3.11}$$

$$C_{it} = \frac{{}^*\partial Q_{it}}{\partial \phi_S} \tag{3.12}$$

Where it follows that:

$$n \propto Q_{it} \tag{3.13}$$

Where,

C_d : Capacitance per unit area of the semiconductor in depletion

C_{it} : Capacitance per unit area due to interface charges

D_{it} : interface state density distribution, at a particular energy level in the HOMO-LUMO gap.

${}^*Q_{it}$: interface state density, when solving for Q_{it} the probability of a trap being filled must be considered

q : elementary charge

k : Boltzmann's constant

T : temperature

To directly relate Q_{it} and D_{it}, exact state levels must be known as well as the band structure for the semiconductor [5, 6]. This is beyond the scope of this dissertation however, extracting D_{it} by taking the minimum subthreshold swing for each device will give a qualitative indication of the interface state density (Q_{it}) for comparison between other interfaces and devices.

3.3 DEVICE INTEGRATION into CIRCUITS

The details of integrated circuits for specific high and low voltage applications will be discussed Chapter 6 and Chapter 8 respectively. Low voltage circuits in this work focus on the basic logic component found in digital systems, the logic inverter. It is desirable to have two threshold voltages (specifically, $V_T{>}0$ and $V_T{<}0$) for these circuits as distinct "on" and "off" transistor states translate to "1" and "0" resolution in logic circuits. Having two distinct threshold voltages also lowers power consumption.

Transistors can have large resistances when "off" resulting in minimal idle currents. For these devices, κ and Q_{it} will be engineered to lower the operating voltage and establish two distinct threshold voltages.

The high voltage circuits in this work are suited for driving MEMS and actuators. For these applications it is desirable to control large source-to-drain (V_{DS}) voltages with small gate-to-source voltages (V_{GS}) using device sizes (channel length and width) that are comparable to the MEMS themselves. For these devices, κ and Q_{it} will be engineered to lower the threshold voltage without sacrificing gate insulator reliability for minimal gate leakage at high supply voltages (V_{DD}).

3.4 SUMMARY
MIS CAPACITOR

This chapter discussed approaches for extracting and comparing device parameters.

- OTFTs based on pentacene operate in accumulation as opposed to inversion as in MOSFETs

- In the absence of interface states, grain boundaries, and tail band states $V_{FB}=V_T$. Their presence complicates establishing a well defined V_T which may not match that which is predicted by in the ideal, defect free case. However, Equation 3.1 can still be used to engineer V_T.

FIELD EFFECT TRANSISTOR

Adding source and drain electrodes the MIS capacitors completes the FET structure. There are two IV characteristics used to characterize FETs.

- Output Characteristics: Sweep V_{DS} while Stepping V_{GS} and measure I_D.

- Transfer Characteristics: Sweep V_{GS} while Stepping V_{DS} and measure I_D.

FIGURES OF MERIT

- threshold voltage (V_T)

- mobility (μ), this term includes contributions from carrier mobility (μ_0), field effect mobility, (μ_{FE}), and the intergrain mobility μ_I.

- subthreshold swing (S)

PARAMETER EXTRACTION

- Both the Si Long Channel MOSFET Model [1] and Subthreshold Linear Regression [3] are used to extract V_T. The Si Long Channel MOSFET Model is good for predicting device behavior at likely operating conditions,

but direct comparison to other OTFT technologies can be misleading due to field dependence of mobility. Subthreshold Linear Regression addresses issues regarding field effect mobility and interface states however, may not offer the best predictions for actual device performance.

- The Si Long Channel MOSFET Model [1] will be used to extract μ.

- Given the disordered nature of pentacene and it sensitivity on morphology and microstructure, extracted values from the Si Long Channel MOSFET Model cannot be well correlated those predicted by Equations 2.6, 2.5, and 3.1. However, theses expressions can be used to qualitatively engineer device performance.

3.5 REFERENCES

[1] B. G. Streetman and S. K. Banerjee, *Solid state electronic devices.* Pearson Prentice-Hall, 2009.

[2] K. Ryu, I. Kymissis, V. Bulovic, and C. G. Sodini, "Direct extraction of mobility in pentacene OFETs using C-V and I-V measurements," *IEEE Electron Device Letters*, vol. 26, no. 10, pp. 716–718, 2005.

[3] K. Ryu, I. Nausieda, I. Kymissis, V. Bulovi, and C. G. Sodini, "Standard test methods for the characterization of thin film transistors for display applications: MIT February Protocol," 2006.

[4] M. G. Kane, "Organic and Polymeric TFTs for Flexible Displays and Circuits," in *Flexible Electronics* (W. S. Wong and A. Salleo, eds.), vol. 11 of *Electronic Materials: Science and Technology*, pp. 215–260, Springer US, 2009.

[5] M. Kim, I. Nam, H. Kim, H. Shin, T. Kim, H. Park, K. Kim, K. Kim, J. Choi, K. Min, D. Kim, D. Kang, and D. Kim, "Optical subthreshold current method for extracting the interface states in MOS systems," *IEEE Electron Device Letters*, vol. 25, pp. 101 – 103, feb. 2004.

[6] S. J. Song, H. T. Kim, S. S. Chi, M. S. Kim, W. S. Chang, S. D. Cho, H. T. Shin, T. E. Kim, H. J. Kang, D. J. Kim, and D. M. Kim, "Characterization of interface states in MOS systems by using photonic high-frequency capacitance-voltage responses," *Journal of the Korean Physical Society*, vol. 41, no. 6, pp. 892–895, 2002.

Chapter 4

Processing Methods for Device Integration

This chapter with provide a brief discussion of the deposition, etching, and patterning processes used to build integrated OTFT and related circuits in this work. The processes that will be reviewed in this section are common in Si-based microelectronics. All processing methods are selected such that devices can be integrated on a 100mm glass wafer. There are other processing methods (inkjet printing [1], microcontact printing [2]) capable of building integrated OTFTs and circuits. However these processes have not seen the decades of development, refinement, and advancement as is the case with the fabrication processes currently used in integrated Si-based microelectronics. Further, it is valuable to show that this technology does not require the development of new processes and fabrication systems by developing the technology within the existing microelectronics manufacturing infrastructure.

4.1 MATERIALS DEPOSITION

The goal of a deposition process is to transfer material from a target or source crucible to a supporting substrate. Ideally, the material deposited on the substrate will be a thin film with thicknesses ranging from nanometers to microns. This section will discuss the methods necessary to deposit pentacene, parylene-C, and BZN on a supporting substrate to fabricate OTFTs.

4.1.1 Pentacene: Thermal Evaporation

As discussed in Chapter 2, the mobility in thin films of pentacene are highly sensitive to the final microstructure of the film and grain distribution. The evolution of grains as a function of deposition parameters, insulator/semiconductor interface roughness and surface energy will be discussed in this section.

Pentacene was deposited by thermal evaporation in vacuum (system shown in Figure 4-1) as this method allows for precise control of film microstructure, therefore electrical performance. With this thermal evaporation, a crucible holding the purified pentacene crystal is heated under vacuum ($<10^{-7}$ torr) with a resistive heater to $\sim 200°C$. The pentacene will condense on the substrate that is held at a room temperature. The microstructure and morphology of pentacene thin films evolve via the theory set forth by Venables et al. [3]. The five relevant atomistic processes active in thin film pentacene growth are (A) adsorption, (B) diffusion, (C) nucleation, (D) coalescence, and (E) desorption as shown in Figure 4-2. There are three crucial elements that determine thin film microstructure and morphology; number of nuclei, surface roughness, and surface energy.
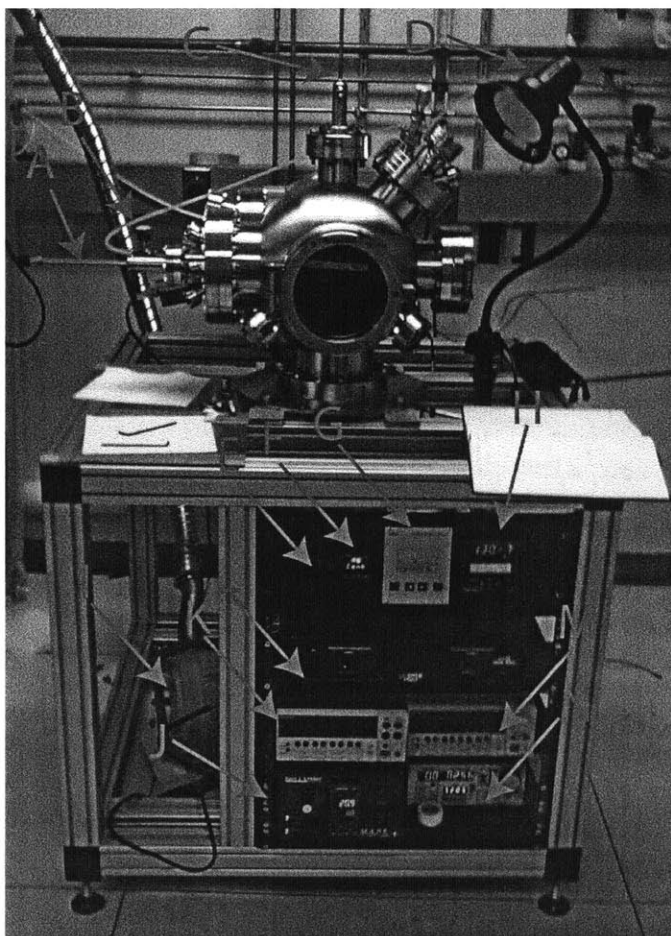
System Components
A: Stage Shutter Feedthrough
B: Vent Valve
C: Stage Feedthrough
D: Lamp
E: Evaporator Shutter
F: Stage Temperature Controller
G: Turbo Controller
H: Pressure Gauge
I: Roughing Scroll Pump
J: Kurt J Lesker M.A.P.S Power Supply
K: 2410 SourceMeter
L: Amplifier
M: 2661 AC/DC Current Source
N: Thickness Monitor
O: Chamber

FIGURE 4-1: Thermal evaporative deposition system used to deposit pentacene
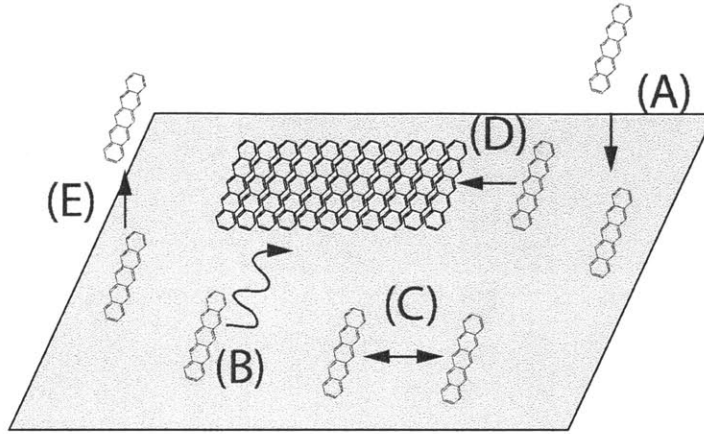
FIGURE 4-2: Atomistic processes active during the thermal evaporative deposition of pentacene. (A) adsorption, (B) diffusion, (C) nucleation, (D) coalescence, (E) desorption

Grain Size: Nuclei Density, Surface Roughness, Surface Energy

NUCLEI DENSITY In regards to the influence of processing, the number of nuclei that form on the substrate during deposition is determined by substrate temperature and evaporant flux. Controlling the nucleation process is critical to growing a film with specific electrical properties. The quantitative nucleation theory articulated by Venables et al. derived from simple kinetic theory is used to model the nucleation of thin films during deposition. Equation 4.1 is the expression for nuclei density.

$$\text{nuclei density} \rightarrow \frac{n_x}{N_0} \sim \left(\frac{F}{N_0 \nu}\right)^p exp\left(\frac{E}{kT}\right) \tag{4.1}$$

TABLE 4.1: Model parameters for relevant growth regimes [3]

	Extreme Incomplete Condensation	Initially Incomplete Condensation	Complete Condensation
p	i	$\frac{i}{2}$	$\frac{i}{i+2}$
E	$E_i + (i+1)E_{des} - E_{diff}$	$\frac{1}{2}(E_i + iE_{des})$	$\frac{(E_i + iE_{diff})}{i+2}$

77
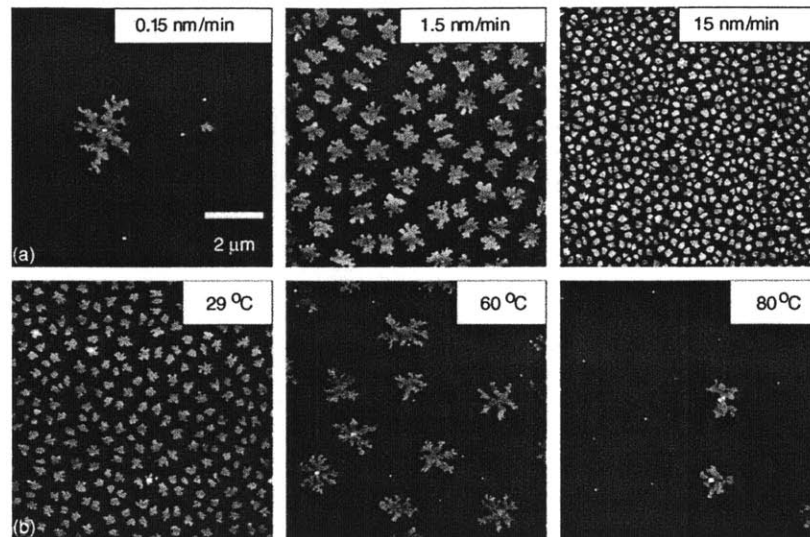
FIGURE 4-3: Grain evolution of pentacene thin films on SiO$_2$ with varying flux and temperature. At larger fluxes there more nuclei and therefore smaller grain sizes. At higher temperatures are fewer nuclei and therefore larger grain sizes [6].

Where,

ν: (effective) surface vibration frequency ($\sim 10^{11}$-10^{13})

E$_i$: binding energy

E$_{diff}$: diffusion energy

E$_{des}$: desorption energy

F: rate of arrival or flux

n$_x$: number of stable clusters

N$_0$: sites per unit area

k: Boltzmann's constant

T: substrate temperature

i: critical cluster size $\sim$3-16 [4, 5]

Extreme Incomplete Condensation: grains only grow by direct impingement

Incomplete Condensation: reevaporation of molecules is significant

Complete Condensation: reevaporation of molecules is not significant

From this model, depositions at high substrate temperatures and low fluxes lead to fewer nuclei and larger grains. Figure 4-3 [6] shows this quantitative nucleation theory is able to explain experimentally observed grain evolution of pentacene deposited on silicon dioxide. Increasing the flux increases the nucleation density. Increasing the substrate temperature, decreases the nucleation density.

SURFACE ROUGHNESS Surface roughness is inherently related to grain size. The reported trend is that the increase in surface roughness increases nuclei density and reduces grain size, which is shown in Figure 4-4 [7]. The reduction in grain size is said to be a result of limited pentacene surface adatom diffusion and reduced activation

energy for nucleation [8]. The physical reason for the decrease in adatom mobility is could be one of several things, a decrease in activation energy for adatom mobility [9], charges trapped in valleys, or adatom scattering [10].
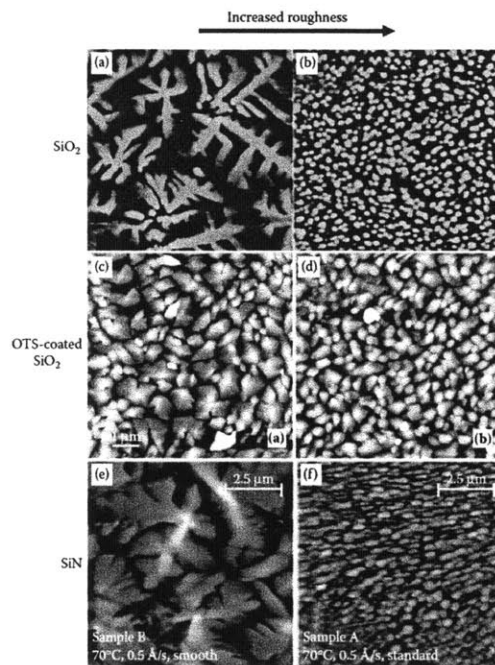
FIGURE 4-4: Effects of substrate surface roughness on pentacene film morphology. Rougher surfaces are the micrographs in the right column [7] which show smaller grains.

SURFACE ENERGY: GROWTH MODES It has generally been concluded that depositing pentacene on insulators with a surface energy within the range of 30 to 50 mN/m results in the best electrical performance, irrespective of grain size as shown in Figure 4-5 [11, 12, 13]. On high energy surfaces, the pentacene passivates (2D Growth) the surface while sacrificing the formation of ordered, full, and stable grains. On low energy surfaces, the pentacene will form full and stable smaller grains [12]. Typically, organic surfaces have a lower surface energy than inorganic surfaces. Thus, literature reports larger dendritic, ramified grains on inorganic surfaces indicating minimal surface diffusion as the pentacene has a stronger interaction with the substrate. Organic surfaces show smaller, rounder grains indicative of more surface diffusion as pentacene will have a stronger interaction with itself as opposed to the substrate [14].

79
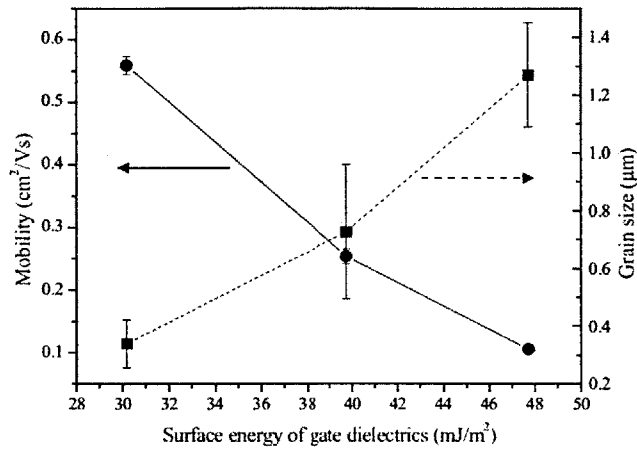
FIGURE 4-5: Relationship between the mobility and grain size for pentacene on insulators with different surface energies [12]

TABLE 4.2: Summary of growth kinetics and its dependence on surface energy

	High Energy	Low Energy
Surface Diffusion	Less	More
Growth	2D, Stranski-Krastanov	3D, Volmer-Weber
Grain Shape	Larger, Dendritic	Small, Rounder

4.1.2 Parylene-C: Chemical Vapor Deposition

Parylene-C films in this work are formed via vacuum vapor deposition polymerization (Gorham Process [15]). The vacuum based pressure is ~0.1 torr where the mean free path is 0.1cm. The deposition is not line of sight as with physical vapor deposition processes therefore the entire substrate surface is coated uniformly creating a pinhole free film. The process for forming this coating is shown in Figure 4-6. In step 1, the loaded dimer is vaporized or heated. In step 2, the dimer vapor is pyrolyzed and cracked into its respective monomer. In step 3, the monomers adsorb and polymerizes onto at substrate that is held at room temperature. [16].
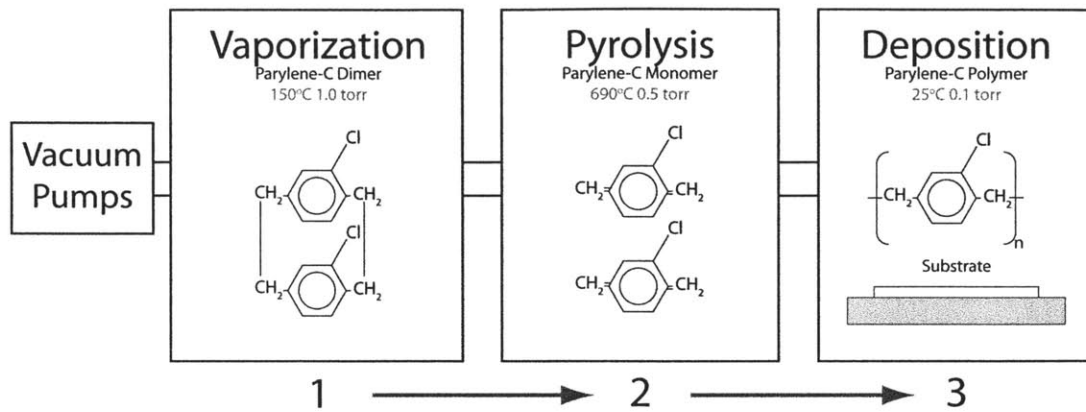
FIGURE 4-6: Schematic of the Chemical Vapor Deposition process for parylene-C

4.1.3 $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_{7.0}$ (BZN): RF Magnetron Sputtering

Exploiting the versatility of physical vapor deposition techniques over larger areas, BZN is deposited by Radio Frequency Magnetron Sputtering. It can be difficult to deposit stoichiometric films from multicomponent targets. The different constituents may have different evaporation rates and therefore deposition rates. RF Sputtering is typically used when the composition of the film is key to its application and must be precisely controlled as is the case with BZN.
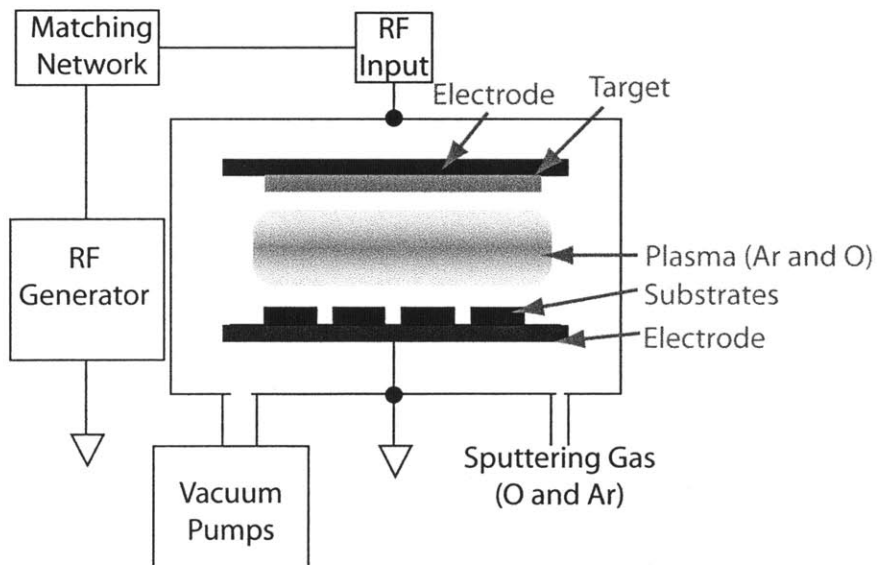
FIGURE 4-7: Schematic of RF Magnetron Sputter Deposition for BZN [17]

In this method, vapor is created using energetic gaseous ions or plasma accelerated by an applied voltage to sputter atoms from a target. The sputtered atoms condense

on the surface of the substrate. For the gases to respond to the applied accelerating voltage, it must first be ionized. As ionizing inert (chemically stable) gasses can be difficult, magnets are often used to concentrate ionizing electrons at the surface of the target to increase gas ionization and therefore sputtering efficiencies. This is shown in Figure 4-7. To control chemical reactions between the target and plasma, either inert gases (i.e. Ar) or gases that can serve as a component in the film such as oxygen. Insulating materials will charge upon direct current plasma (DC Sputtering) exposure as they cannot dissipate charge. This charging of the insulator will discharge the plasma stopping deposition. Therefore, a high frequency alternating voltage is used to maintain the plasma and stop the insulating target from charging. 13.56MHz is a commonly used frequency [17].

4.1.4 Gold (Au): e-Beam Evaporative Deposition

A source of heat is needed with all evaporative deposition methods. In modern microelectronics, a high-energy electron beam (e-Beam) can be used as this heat source. An e-Beam heater can reach higher temperatures allowing a variety of materials to be deposited, including some refractory materials. Further, the e-Beam only melts the top portion of the target which minimizes contamination from the crucible [17].

With the system under vacuum, the e-Beam is focused on the target (material to be deposited) with magnetic optics to evaporate the target material. The vapor will then condense on a substrate held in line of sight the target material. An illustration of e-Beam deposition is shown in Figure 4-8.
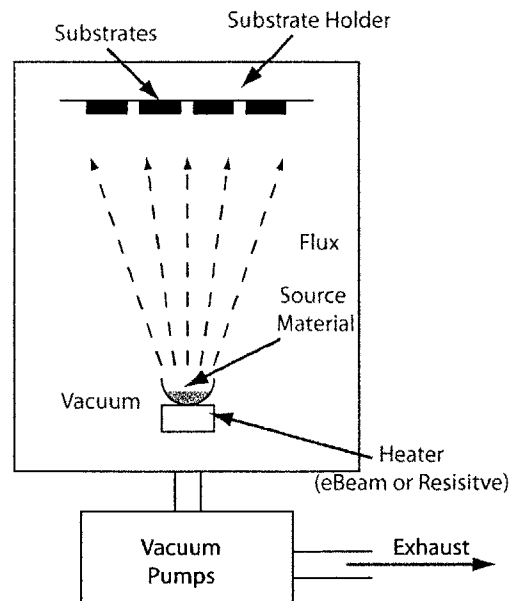
FIGURE 4-8: Schematic of Vacuum Evaporative Deposition System [17]

4.2 ETCHING

After films are deposited, areas of the target film must be selectivity removed to define a device. This process is referred to as etching. Ideally, no other thin films in the device will dissolve or be removed other than the materials targeted during specific etching steps.

4.2.1 Wet Etching

Wet etching is the simplest form of material removal. Substrates holding the thin films are immersed in liquid chemicals which are designed to dissolve the target film. These liquids are typically acids designed to etch metals (Au) and oxides (BZN), and not organic materials also on the wafer (parylene-C, pentacene) [17]. The most common organic materials found in VLSI, photoresists, are used for patterning and will be discussed Section 4.3. Au etches in Gold Etch (KI based etchant) and BZN etches in hydrogen fluoride (HF).

4.2.2 Dry Etching

Dry etching typically uses gaseous etchant ions and is often called plasma etching. Plasma etching has gained popularity as the use of reactive plasma enabled faster etching rates and the ions are capable of being collimated for more anisotropic etches. For plasma etching there can be both a physical component (ion or plasma energy) and a chemical component (gas species). By selecting the proper gas and ion energies, fast etch rates with appropriate material etch selectivity can be achieved. For this work, plasma etching will be used to etch and pattern pentacene and parylene-C. O_2 Plasma is commonly used to ash or strip photoresist from a patterned wafer as the reactive oxygen burns away the susceptible organic material [17]. Using the same principle, parylene-C and pentacene will be etched in an O_2 Plasma.

Etching is used to transfer a pattern into the target materials. In this work, the patterns are made with photolithography and is discussed in the next section.

4.3 PATTERNING: PHOTOLITHOGRAPHY

As mentioned in Chapter 1, currently photolithography is the best patterning method for very large scale integration. Photolithography is a pattern transfer process where ultra violet (UV) light is used to selectively expose a photosensitive material (photoresist) though a photomask which carries the pattern to be transferred. Figure 4-9 illustrates how pattern transfer occurs through photolithography, specific to the work in this dissertation.

In step 0, the target material is deposited. In step 1, photoresist is spin coated onto

the target material and baked at $\sim$95°C to evaporate the photoresist solvent. Photoresist is a typically soluble polymer (PMMA for example) that is reactive upon exposure to light. In this work, a positive photoresist used. This type of photoresist will become more soluble upon exposure to light (light breaks chemical bonds) which is illustrated in step 2. The photomasks holds the pattern to be transferred and is held in contact with or close proximity to the photoresist coated substrate. On the photomask, the pattern is opaque such that light cannot pass through leaving the photoresist below these areas unexposed and insoluble. In the next step, (step 3) the photoresist is submerged in a resist developer (weak organic hydroxide) which is designed to dissolve the exposed areas leaving unexposed areas intact. At this point, the pattern has been transferred to the photoresist, which will be used to transfer the pattern into the target material. In the etching step (Step 4), a liquid ("wet") or plasma ("dry") chemical removes the target material in the areas not protected by the photoresist. With the target material now patterned, the photoresist is removed or stripped (Step 5) with an organic solvent.

When using photolithography, the materials must physically withstand heat ($\sim$95°C) and organic solvents with the minimal degradation of electrical performance. As mentioned previously in Chapter 2, the mobility in pentacene degrades dramatically when exposed to heat above $\sim$55°C [18] because of a phase transition from the thin film (higher mobility) to the bulk phase (lower mobility). In addition, exposing pentacene to solvents (water, acetone, and photoresist developer) will severely degrade mobility. Gundlach et al. attributed this to the formation of the low mobility bulk film phase of pentacene and film "buckling" resulting in poor grain structure [19]. From this, it is clear how a simple photolithographic process can degrade pentacene performance. In an effort to minimize degradation due to photolithography two preemptive approaches are used.

1. Commonly, an insoluble encapsulation layer (parylene-C [20], polyvinyl alcohol [21, 22], Al_2O_3 [23]) is used to protect the pentacene during photolithography. For this work, pentacene will be encapsulated with parylene-C which is impervious to organic solvents and most acids and bases. Parylene-C will protect the pentacene from the solvents used in photolithography.

2. Pentacene will be deposited after the gate contact, insulator, and source/drain contacts. These layers will be patterned with photolithography as well demanding heat and solvents. Depositing the pentacene as late as possible in the process will minimize the heat exposed to the pentacene.

For more information regarding materials processing and patterning for very large scale integration, refer to Plummer, Deal, and Griffin [17].

84
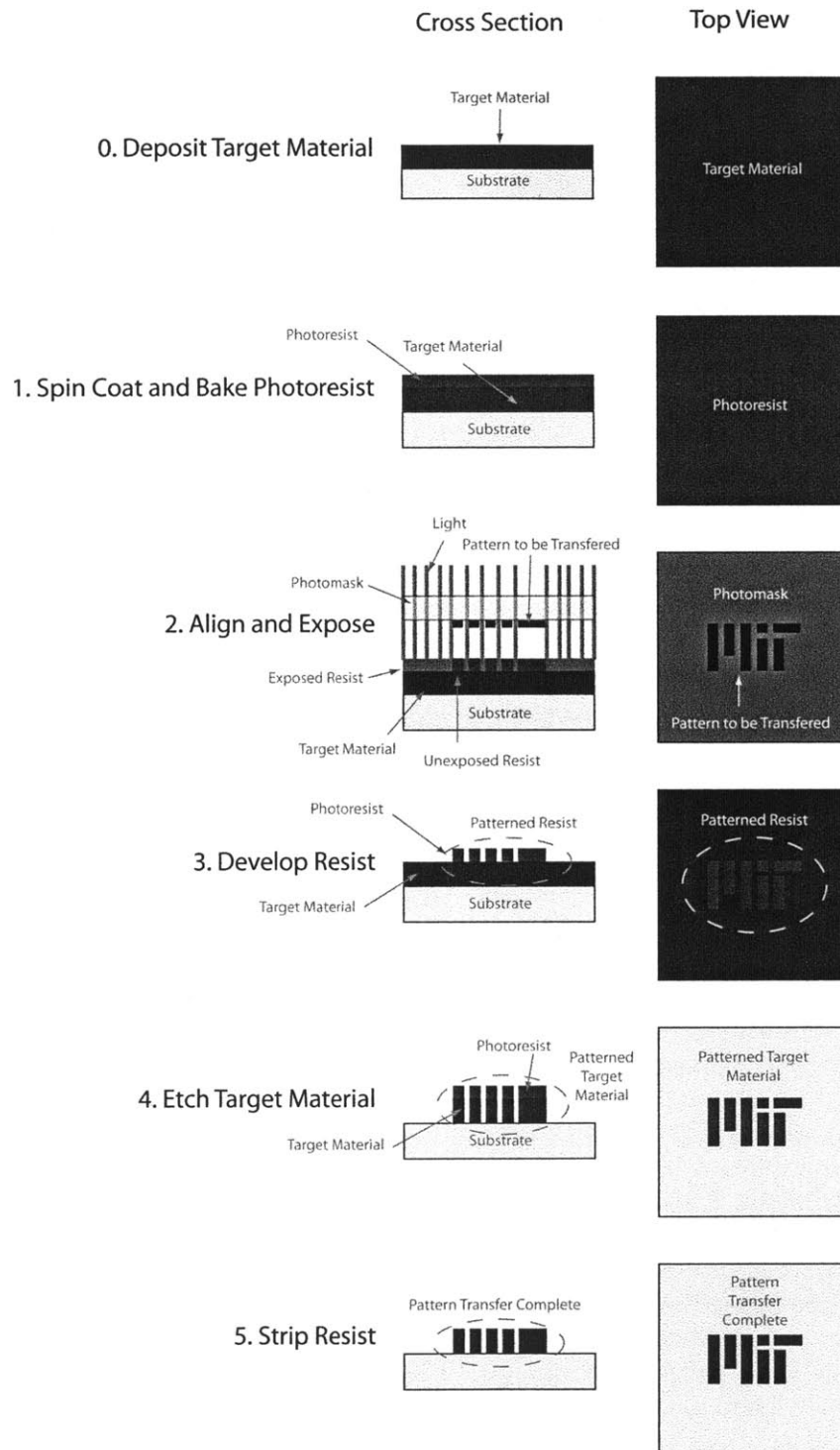
FIGURE 4-9: Illustration of Steps in Photolithography
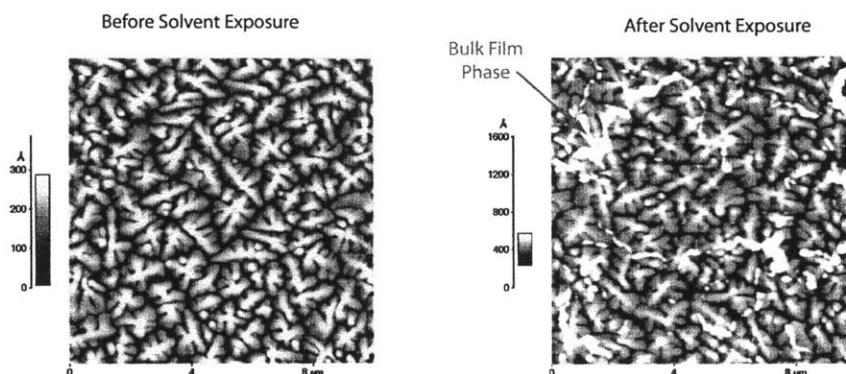
FIGURE 4-10: AFMs of pentacene before and after solvent exposure [19]. After exposure to solvents, more bulk phase pentacene appears which is deleterious to carrier transport.

4.4 DEVICE STRUCTURE CONSIDERATIONS

To fabricate a TFT, the gate must be electrically insulated from the semiconductor and source/drain contacts which are in electrical contact. This gives rises to four possible device structures for TFTs. A specific structure is chosen to maintain performance and facilitate easy fabrication, which is dictated by the stability of the semiconductor and gate insulator through the fabrication process.

4.4.1 Bottom Gate vs. Top Gate

Mobility in the device depends on the roughness of the insulator/semiconductor interface where charge is accumulated [9]. The bottom gate offers a smoother insulator/semiconductor surface for charge transport as the gate metal and insulator deposition techniques create flatter surfaces compared to the top of the semiconductor surface. In the case of the top gate structure, the semiconductor layer is first deposited followed by the insulator layer and then gate layer. The top of the semiconductor layer is rough after deposition leading to a semiconductor/insulator interface that is rougher than in the case with bottom gate structure. Thus, the bottom gate TFT structure typically shows higher mobilities than the top gate structures [9, 24].

4.4.2 Bottom Contact vs. Top Contact

Contact selection is critical to minimize contact resistance in the TFT. As pentacene does not grow well on metals, (pentacene/metal interaction is too strong and disordered grains are formed) a top contact structure is preferred for optimal performance [25]. Bottom contact devices were used in the initial conception of the photolithographically patterned OTFT to minimize pentacene heat exposure and for simpler fabrication [26]. Only recently have top contact photolithographically patterned devices been reported [27]. However, the fabrication for this structure was more complex and the fabrication process subjects the semiconductor to more heat. For this work,

86
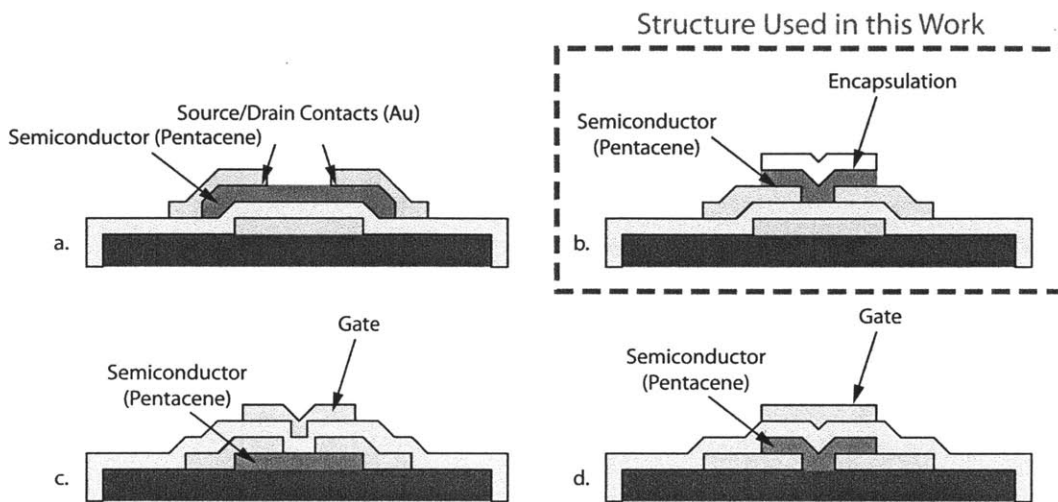
FIGURE 4-11: Illustration of possible TFT structures. Bottom Gate Top Contact(a) Bottom Gate Bottom Contact(b) Top Gate Top Contact(c) Top Gate Bottom Contact(d) A structure is selected to faciliate fabracation with minimal degradation to device performance.

the bottom gate bottom contact structure is used as there is more general knowledge and experience with this device structure with photolithography, despite that devices with top contact show fewer issues injecting charge carriers into the semiconductor.

4.5 SUMMARY

This chapter is an overview of the deposition, etching and patterning processes and device structures needed to fabricate fully integrated OTFTs.

DEPOSITION

PENTACENE

- Pentacene will be deposited by thermal evaporation and dry etched in O_2 Plasma.
- The processing conditions used during deposition affect the microstructure of the film and therefore electrical performance, in addition to surface roughness and surface energy.
- Mobility can be linked to insulator/semiconductor roughness where flatter interface show better performance.
- Pentacene grown on insulators with surface energies in the range of 30-50mN/m show higher mobilities.

INSULATORS

- Parylene-C is deposited at room temperature by chemical vapor deposition and dry etched in O_2 Plasma
- BZN will be deposited at room temperature by RF magnetron sputtering with annealing due to photolithography back out and O_2 Plasma etching $<130°C$ for ~ 80 minutes and wet etched in dilute HF.

Gate, Source, and Drain Contacts: Gold

- Gold will be deposited by e-Beam Evaporation and wet etched in KI based Gold Etch.

PATTERNING: PHOTOLITHGRAPHY
All layers will be patterned with photolithography

- This processes used heat and organic solvents which are not compatible with pentacene. A parylene-C encapsulation is used to protect the pentacene from solvents and the pentacene is deposited as late as possible in the process to minimize the heat seen in subsequent processing steps.

DEVICE STRUCTURE CONSIDERATIONS
This chapter justified the use of the bottom gate, bottom contact device structure.

- For ease of fabrication and integration bottom gate bottom contact structure is used.
- Using this structure will minimize heating of the pentacene after its deposition and definition.

4.6 REFERENCES

[1] H. Sirringhaus, T. Kawase, R. H. Friend, T. Shimoda, M. Inbasekaran, W. Wu, and E. P. Woo, "High-Resolution Inkjet Printing of All-Polymer Transistor Circuits," *Science*, vol. 290, no. 5499, pp. 2123–2126, 2000.

[2] J. A. Rogers, Z. Bao, A. Makhija, and P. Braun, "Printing Process Suitable for Reel-to-Reel Production of High-Performance Organic Transistors and Circuits," *Advanced Materials*, vol. 11, no. 9, pp. 741–745, 1999.

[3] J. A. Venables, G. D. T. Spiller, and M. Hanbucken, "Nucleation and growth of thin-films," *Reports on Progress in Physics*, vol. 47, no. 4, pp. 399–459, 1984.

[4] R. Ruiz, D. Choudhary, B. Nickel, T. Toccoli, K. C. Chang, A. C. Mayer, P. Clancy, J. M. Blakely, R. L. Headrick, S. Iannotta, and G. G. Malliaras, "Pentacene thin film growth," *Chem. Mater.*, vol. 16, no. 23, pp. 4497–4508, 2004.

[5] D. Choudhary, P. Clancy, R. Shetty, and F. Escobedo, "A computational study of the sub-monolayer growth of pentacene," *Advanced Functional Materials*, vol. 16, no. 13, pp. 1768–1775, 2006.

[6] S. Pratontep, M. Brinkmann, F. Nesch, and L. Zuppiroli, "Nucleation and growth of ultrathin pentacene films on silicon dioxide: effect of deposition rate and substrate temperature," *Synthetic Metals*, vol. 146, no. 3, pp. 387–391, 2004.

[7] Z. Bao and J. J. Locklin, *Organic Field-Effect Transistors*. CRC Press, 2007.

[8] S. Steudel, S. De Vusser, S. De Jonge, D. Janssen, S. Verlaak, J. Genoe, and P. Heremans, "Influence of the dielectric roughness on the performance of pentacene transistors," *Applied Physics Letters*, vol. 85, no. 19, pp. 4400–4402, 2004.

[9] S. E. Fritz, T. W. Kelley, and C. D. Frisbie, "Effect of dielectric roughness on performance of pentacene TFTs and restoration of performance with a polymeric smoothing layer," *The Journal of Physical Chemistry B*, vol. 109, no. 21, pp. 10574–10577, 2005.

[10] D. Knipp, R. A. Street, and A. R. Volkel, "Morphology and electronic transport of polycrystalline pentacene thin-film transistors," *Applied Physics Letters*, vol. 82, no. 22, pp. 3907–3909, 2003.

[11] C. Wei-Yang, K. Chia-Wei, C. Horng-Long, C. Yi-Ren, T. Fu-Ching, Y. Feng-Yu, S. Dun-Yin, and L. Chi-Chang, "Effect of surface free energy in gate dielectric in pentacene thin-film transistors," *Applied Physics Letters*, vol. 89, no. 11, p. 112126, 2006.

[12] S. Y. Yang, K. Shin, and C. E. Park, "The Effect of Gate-Dielectric Surface Energy on Pentacene Morphology and Organic Field-Effect Transistor Characteristics," *Advanced Functional Materials*, vol. 15, no. 11, pp. 1806–1814, 2005.

[13] M. Yoshida, S. Uemura, T. Kodzasa, T. Kamata, M. Matsuzawa, and T. Kawai, "Surface potential control of an insulator layer for the high performance organic FET," *Synthetic Metals*, vol. 137, no. 1-3, pp. 967–968, 2003.

[14] B. Stadlober, U. Haas, H. Maresch, and A. Haase, "Growth model of pentacene on inorganic and organic dielectrics based on scaling and rate-equation theory," *Physical Review B (Condensed Matter and Materials Physics)*, vol. 74, no. 16, p. 165302, 2006.

[15] M. Szwarc, "Poly-para-xylelene: It's chemistry and application in coating technology," *Polymer Engineering and Science*, vol. 16, no. 7, pp. 473–479, 1976.

[16] Specialty Coating Systems, "SCS Parylene Properties." Promotional brochure, 2010.

[17] J. Plummer, M. Deal, and P. Griffin, *Silicon VLSI Technology: Fundamentals, Practice and Modeling*. Prentice Hall Electronics and VLSI Series, Prentice Hall, 2000.

[18] C. D. Dimitrakopoulos and D. J. Mascaro, "Organic thin-film transistors: A review of recent advances," *IBM Journal of Research and Development*, vol. 45, pp. 11 –27, jan. 2001.

[19] D. J. Gundlach, T. N. Jackson, D. G. Schlom, and S. F. Nelson, "Solvent-induced phase transition in thermally evaporated pentacene films," *Applied Physics Letters*, vol. 74, no. 22, pp. 3302–3304, 1999.

[20] I. Kymissis, A. I. Akinwande, and V. Bulovic, "A lithographic process for integrated organic field-effect transistors," *Journal of Display Technology*, vol. 1, no. 2, pp. 289–294, 2005.

[21] L. Zhou, A. Wanga, S.-C. Wu, J. Sun, S. Park, and T. N. Jackson, "All-organic active matrix flexible display," *Applied Physics Letters*, vol. 88, no. 8, p. 083502, 2006.

[22] M. G. Kane, J. Campi, M. S. Hammond, F. P. Cuomo, B. Greening, C. D. Sheraw, J. A. Nichols, D. J. Gundlach, J. R. Huang, C. C. Kuo, L. Jia, H. Klauk, and T. N. Jackson, "Analog and digital circuits using organic thin-film transistors on polyester substrates," *IEEE Electron Device Letters*, vol. 21, no. 11, pp. 534–536, 2000.

[23] H. Jia, E. K. Gross, R. M. Wallace, and B. E. Gnade, "Patterning effects on poly (3-hexylthiophene) organic thin film transistors using photolithographic processes," *Organic Electronics*, vol. 8, no. 1, pp. 44 – 50, 2007.

[24] C. R. Newman, R. J. Chesterfield, M. J. Panzer, and C. D. Frisbie, "High mobility top-gated pentacene thin-film transistors," *Journal of Applied Physics*, vol. 98, no. 8, pp. 084506–6, 2005.

[25] I. Kymissis, "Morphology and performance in pentacene," Master's thesis, Massachusetts Institute of Technology, 1999.

[26] I. Kymissis, C. D. Dimitrakopoulos, and S. Purushothaman, "High-performance bottom electrode organic thin-film transistors," *IEEE Transactions on Electron Devices*, vol. 48, no. 6, pp. 1060–1064, 2001.

[27] H. Wang, Z.-Y. Ji, L.-W. Shang, X.-H. Liu, Y.-Q. Peng, and M. Liu, "Top contact organic field effect transistors fabricated using a photographic process," *Chinese Physics B*, vol. 20, no. 8, p. 087306.

Chapter 5

Device Fabrication and Resulting Materials Properties

5.1 MOTIVATION

Building integrated circuits that are suitable for VLSI requires precise and controllable deposition, etching, and patterning processes. The Si-based microelectronics industry has developed an infrastructure to fabricate integrated circuits with such deposition, etching, and patterning processes. Similar processes will be used to fabricate OTFT based integrated circuits for low and high voltage applications. The gate insulators for OTFTs operating at low voltages (10 V $\leq V_{DS}$) have a different selection criteria than the gate insulators for OTFTs operating at high voltages (300 V $> V_{DD}$).

For the low voltage devices, a high-κ insulator, BZN is used for the gate insulator. To shift the threshold voltage a thin parylene-C based surface treatment is used to modify the interface states on the surface of BZN (pBZN) following the approach used by Choi et al.[1]. Choi et al. showed that simple two transistor inverters can be made. However, those devices were not integrated. The key development with the technology reported in this dissertation is the complete integration of BZN and pBZN gate insulators into OTFTs and circuits. This approach offers scalability, reproducibility and leads to the realization of more complex circuits that use more than two OTFTs.

Typically, as the dielectric constant of a material increases the energy band gap decreases [2]. This leads to a small barrier height for typical conduction mechanisms in these materials. As a result, high-κ insulators tend to suffer from large leakage currents. Materials with a low-κ typically do not have this issue as they tend to have

larger band gaps, and therefore a larger barrier height for conduction. As the high voltage devices will see a large voltage difference between the source/drain electrodes and gate electrode, BZN itself cannot serve as the gate insulator in these devices. However, it is still important to maintain low threshold voltages such that small gate-to-source voltages can switch large source-to-drain voltages.

To serve as a standard, reliable low-κ insulator parylene-C (PAR) will be evaluated as a dielectric for high voltage devices. The parylene-C will be modified in two ways to obtain a reduction in threshold voltage. For the first method, parylene-C will be treated with O_2 plasma (O_2 PAR) to create interface states that will modify the threshold voltage. This was first shown by Wang et al. [3]. The second method will combine the large breakdown resistance of parylene-C and with the high-κ of BZN (PAR/BZN) to create a composite insulator stack with high voltage reliability and a lower threshold voltage.

Though these insulators are optimized for completely different types of integrated circuits (PAR, O_2 PAR, PAR/BZN for high voltage circuits; BZN and pBZN for low voltage circuits) the fabrication of OTFTs based on each insulator is similar to and is derived from that reported by Kymissis et al. [4]. Illustrations of these insulators are shown in Figure 5-1.
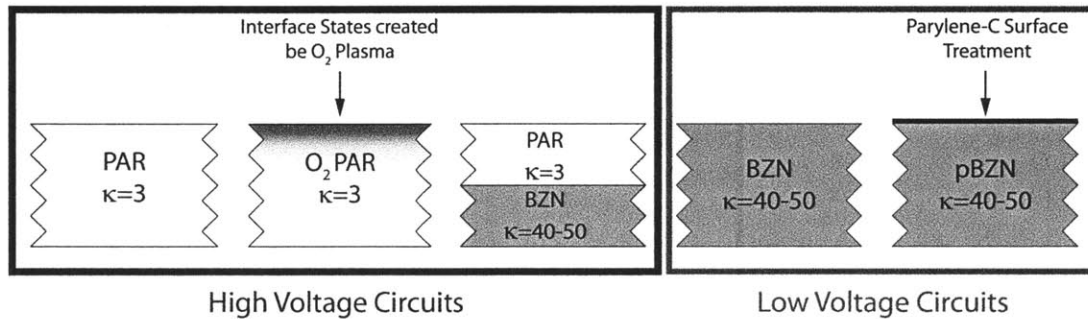
FIGURE 5-1: Insulators Stacks explored in this work. The PAR, O_2 PAR, PAR/BZN insulators will be used in high voltage applications. The BZN and pBZN insulators will be used in low voltage applications.

There is a considerable amount of literature regarding the properties of parylene-C, pentacene, and BZN. To understand how effectively they will serve in their respective components in an OTFT fabricated towards full integration, an evaluation of the properties of these materials is conducted with regards to the processing needed to build integrated devices and circuits. This will provide an awareness of how the demands of these processes will affect material properties and device performance.

5.2 BUILDING OTFTS

1 ACQUIRE SUBSTRATE: For the devices in this work, the substrate is a 100mm glass wafer, though the process is not limited to a rigid substrate as all processes are run at or near room temperature.

2 GATE DEFINITION: For the gate layer, 10 nm of a Cr adhesion layer followed by 80-100 nm of Au to serve as a gate metal are deposited both by e-Beam evaporation and patterned by standard photolithography and a wet etch.

3 INSULATOR DEFINITION: The parylene-C and BZN insulators are used selectively to achieve a particular device performance. Regardless of how they are distributed in the insulator, they are processed as described below.

- **Parylene-C:** With a SCS Parylene-C Coater, chemical vapor deposition is used to deposit parylene-C, while the substrate remains at room temperature. The parylene-C films are transparent and colorless. It is patterned by photolithography and a dry O_2 plasma etch.

- **BZN:** RF magnetron sputtering is used to deposit BZN with the substrate at room temperature with 95 W at 9:3 argon to oxygen gas ratio at a pressure of 3mtorr. The stoichiometry of the target is $Bi_{1.5}Zn_1Nb_{1.5}O_7$ which is the intended composition of the film. The resulting BZN films are transparent with a yellowish tint. The BZN is then patterned by photolithography and very dilute BOE wet etch. BZN is then treated with O_2 plasma at 1000 W in a barrel asher to normalize and stabilize the surface. As BZN is not a common cleanroom material, its stability in standard solvents and etch undercutting needed to be assessed as shown in Figure 5-2, Figure 5-3, Figure 5-4, and Figure 5-5. These assessments revealed that the BZN was not adversely affected by cleanroom processes/conditions.
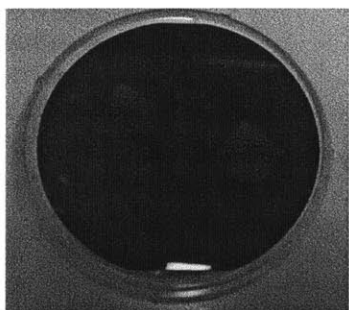
FIGURE 5-2: BZN on 100mm Si Wafer
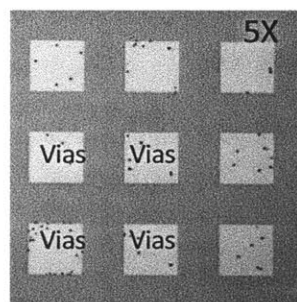
FIGURE 5-3: Open vias after BZN wet etch in BOE
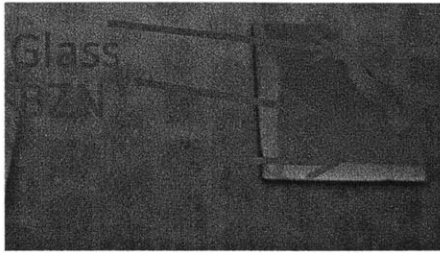
FIGURE 5-4: BZN on Au
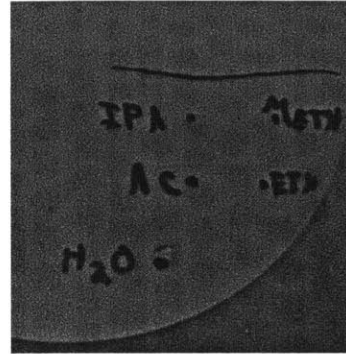
FIGURE 5-5: BZN is stable in standard solvents found in a typical microfabrication environment.

4 SOURCE/DRAIN DEFINITION: For the source/drain electrodes, 80-100 nm of Au is deposited by e-Beam evaporation and patterned by photolithography and a wet etch.

4b SURFACE TREATMENT DEFINITION: For the devices that require a surface treatment definition, it is performed after the source/drain electrodes have been defined. The rest of processing necessary to complete the device is the same for all insulators.

- **Low Voltage Devices:** A thin parylene-C layer is deposited immediately after patterning the BZN and before the deposition of the source/drain electrodes. To pattern this surface treatment, an O_2 plasma is used to etch the parylene-C. This is shown in Figure 5-7 at step 4b. From this step, two different surfaces are created. One surface is inorganic bare BZN and the other is an organic surface of parylene-C. These two different surfaces give rise to OTFTs with different threshold voltages on one wafer.

- **High Voltage Devices:** For the O_2 PAR insulator, selectively exposing the parylene-C to O_2 plasma will create two different surfaces on one wafer. The parylene-C surface is stable and has fewer interface states than the surface exposed to O_2 plasma. This gives rise to OTFTs with two different threshold voltages on one wafer.

5 SEMICONDUCTOR DEFINITION: The pentacene semiconductor layer is deposited by thermal evaporation to a thickness of 10-40 nm at a rate $\sim$2 nm/min at a pressure of 2×10^{-7} torr. The pentacene films are transparent with a blue-ish tint. An encapsulation layer of parylene-C is deposited to protect the pentacene from the solvents in the following photolithographic patterning step. The definition of the device is completed by dry etching the semiconductor and encapsulation layer in O_2 plasma.

Tables 5.1 - 5.4 and Figure 5-7 summarize and illustrate this process flow. There is no intentional heating in any process steps, excluding each photolithographic step in which the baking occurs at 95° C for 20 min and the O_2 plasma dry etch which is believed to be less than 130° C based on the electrical properties of the BZN [5] and a preliminary evaluation for this work. The PAR devices and O_2 PAR devices can be integrated on the same wafer using O_2 plasma as a surface treatment. The BZN and pBZN devices can easily be integrated on the same wafer, using parylene-C as a surface treatment.
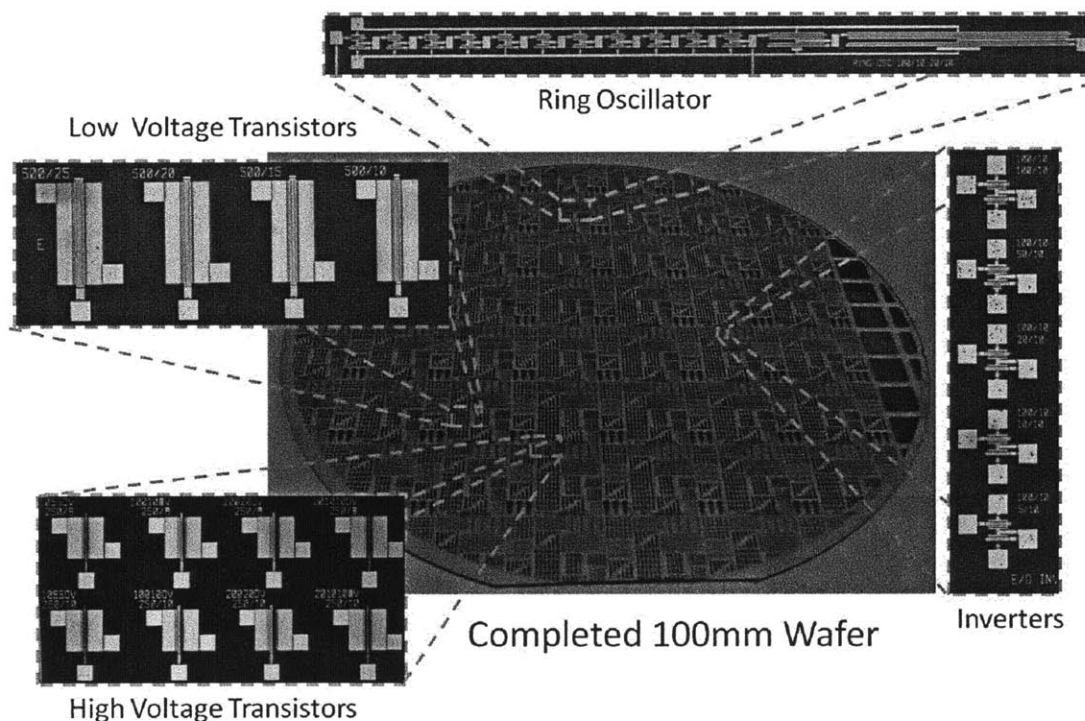
FIGURE 5-6: Completed 100 mm Wafer with OTFTs devices and circuits. OTFTs include low voltage transistors and high voltage transistors. Integrated circuitry includes arrays of inverters based on two transistors with two distinct threshold voltages and ring oscillators based on inverter chains.
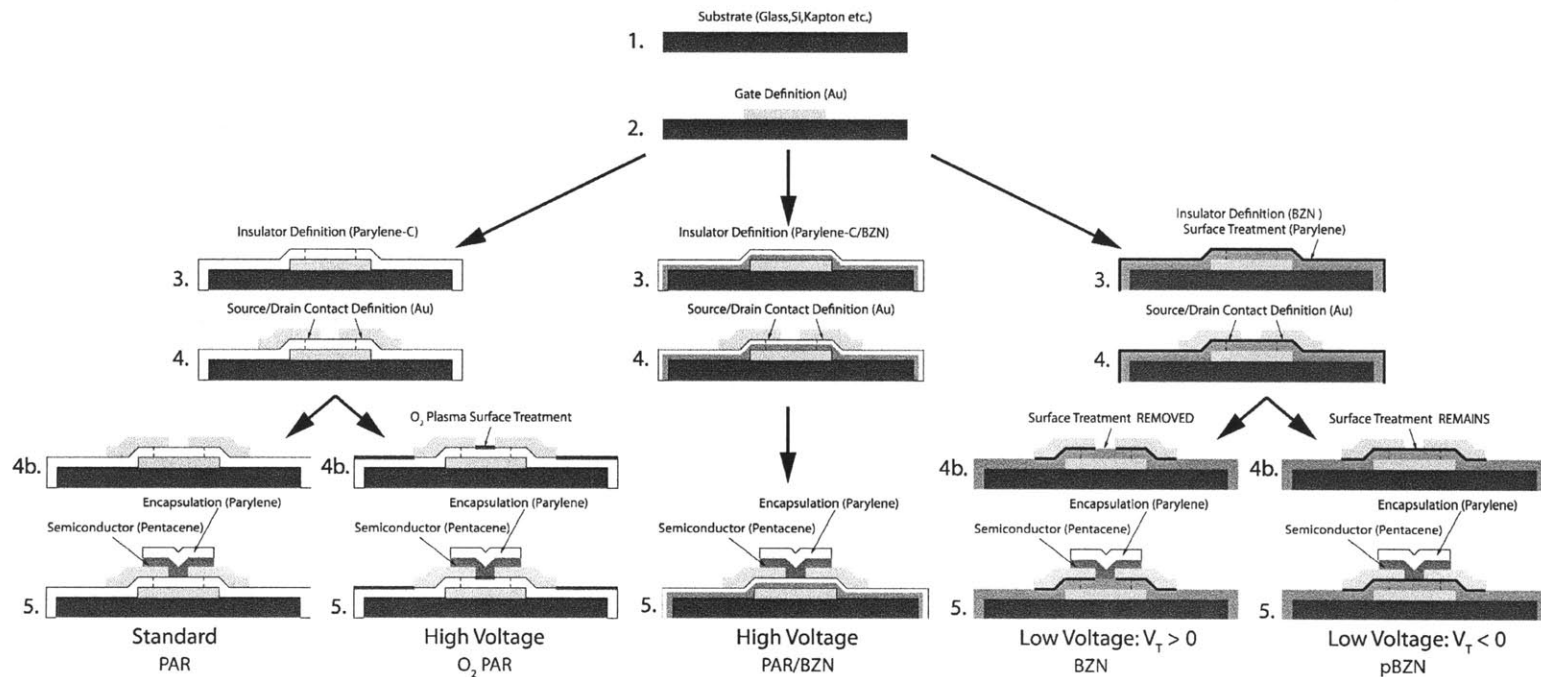
FIGURE 5-7: Process flow for fabricating OTFTs. The processing for all five insulators is shown and differ only by how the insulator is processed.

TABLE 5.1: Process steps for fabricating High Voltage OTFTs.

Step	Layer	Action	PAR	O$_2$ PAR	PAR/BZN
1	Acquire Vacuum Compatible Substrate				
2	Gate Definition	Dep. Etch	e-Beam Evaporation (Cr and Au) Gold Etch and Chrome Etch)		
3	Insulator Definition	Dep. Etch	CVD O$_2$ Plasma	CVD O$_2$ Plasma	RF Spt.(BZN) CVD (PAR) Dilute HF (BZN) O$_2$ plasma (PAR)
4	Source/Drain Definition	Dep. Etch	e-Beam Evaporation (Au) Gold Etch		
4b	Surface Treatment	Etch	-	O$_2$ Plasma	-
5	Semiconductor Encapsulation Definition	Dep. Dep. Etch	Thermal Evaporation (Pentacene) CVD (Parylene-C) O$_2$ Plasma		

TABLE 5.2: Thickness of respective layers in High Voltage OTFTs

Step	PAR	O$_2$ PAR	PAR/BZN
Encapsulation	Parylene-C 200 nm		
Semiconductor	Pentacene 20 nm	Pentacene 40 nm	Pentacene 20 nm
Source/Drain	Au 80-100 nm		
Insulator	Parylene-C 500 nm	Parylene-C 350 nm	Parylene-C 200 nm BZN 200 nm
Gate	Au 80-100 nm		

TABLE 5.3: Process steps for fabricating Low Voltage OTFTs

Step	Layer	Action	BZN	pBZN
1	Acquire Vacuum Compatible Substrate			
2	Gate Definition	Dep. Etch	e-Beam Evaporation (Cr and Au) Gold Etch and Chrome Etch)	
3	Insulator Definition	Dep. Etch	RF Spt.(BZN) CVD (PAR) Dilute HF	RF Spt.(BZN) CVD (PAR) Dilute HF
4	Source/Drain Definition	Dep. Etch	e-Beam Evaporation (Au) Gold Etch	
4b	Surface Treatment	Etch	O$_2$ Plasma	-
2	Semiconductor Encapsulation Definition	Dep. Dep. Etch	Thermal Evaporation (Pentacene) CVD (Parylene-C) O$_2$ Plasma	

99

TABLE 5.4: Thickness of respective layers in Low Voltage OTFTs

Step	BZN	pBZN
Encapsulation	Parylene-C 200 nm	
Semiconductor	Pentacene 20 nm	
Source/Drain	Au 80-100 nm	
Insulator	BZN 400 nm	Parylene-C ~1-3 nm BZN 400 nm
Gate	Au 80-100 nm	

5.3 TECHNIQUES for MATERIALS CHARACTERIZATION

As device integration is the ultimate goal of this process flow, fabrication methods are selected to facilitate this, not to optimize materials performance. Therefore, materials characterization is performed to understand how the materials respond to their deposition, patterning, and etching processes and subsequent processes of other components. Criteria for materials selection was compatibility with other materials and the low temperature processes that are necessary to make complete devices and circuits that are suitable for flexible and large area systems. Characterization is done to confirm and/or assess this compatibility. The final morphology and atomic structure of BZN, pentacene, and parylene-C were assessed by X-ray Photospectroscopy (XPS), X-ray Diffraction (XRD), the Static Sessile Drop Technique for extraction of surface energy, Atomic Force Microscopy (AFM), and Scanning Electron Microscopy (SEM).

X-RAY PHOTOSPECTROSCOPY (XPS): XPS is a quantitative spectroscopic technique used to determine composition, chemical formula, and the electronic states of elements < 10 nm from the surface of a sample. As discussed in Chapter 2, the electrical properties of BZN depend on its composition. Analysis was performed on BZN to determine the actual composition of the deposited films and how the composition changes throughout processing. Characterization and analysis was conducted by Analytical Answers Inc. by Dr. Kaj G. Stolt. Data was collected with an Al target with a pass energy of 187.85 eV and with a work function of 3.67 eV. Six sweeps were performed on each sample. For more information regarding XPS, refer to the ASM Handbook, Volume 10 - Materials Characterization [6].

X-RAY DIFFRACTION (XRD): XRD is an x-ray scattering technique that can be used to reveal structural information about a material. As discussed in Chapter 2, the electrical properties of both BZN and pentacene are sensitive to their structure (crystalline vs. amorphous for BZN, thin film phase vs. bulk phase for pentacene). Further, processing conditions may affect the resulting structure of the film. Therefore, analysis was performed on BZN and pentacene to determine the crystallinity and existing phases, and to compliment XPS results regarding the composition of

BZN. Analysis was conducted by Evans Analytical Group by Wes Nieveen and Dr. Stephen B. Robie. Data was collected by Grazing Incidence XRD (GIXRD) (incident angle at 0.2°) with the standard θ-2θ geometry. A PANalytical XPert Pro MRD diffractometer was used with a Cu X-ray tube and parallel-beam optics. For more information regarding XRD, refer to Hammond [7].

Sessile Drop Technique for Extraction of Surface Energy

The microstructure of a pentacene thin film can affect its electrical performance. The resulting microstructure is sensitive to the energy of the surface that it is deposited on. Analysis was performed on parylene-C, O_2 plasma treated parylene-C, BZN, and parylene-C surface treated BZN, as they represent the gate insulators used in the pentacene based OTFTs in this work. Contact angles were measured using Model 250 Standard Contact Angle Goniometer/Tensiometer and DROPimage Advanced software by ramé-hart. Surface energy was extracted using Owens/Wendt Theory [8, 9] with DI water and ethylene glycol as test liquids. For more information regarding surface energy extraction via the sessile drop technique, refer to Owens et al.[9] and Carre et al. [8].

$$\frac{\gamma_L}{\sqrt{\gamma_L^D}} = 2\sqrt{\gamma_S^D} + 2\sqrt{\gamma_S^P}\frac{\sqrt{\gamma_L^P}}{\sqrt{\gamma_L^D}} \tag{5.1}$$

$$\gamma_S = \gamma_S^D + \gamma_S^P \tag{5.2}$$

Where,

γ: Surface Energy
Subscript L: liquid
Subscript S: solid;
Superscript D: dispersive
Superscript P: polar

Scanning Electron Microscopy (SEM):

SEM is a very high resolution imaging technique that generates images of a surface from secondary electrons and other kind of electrons and x-rays. Analysis was performed on RF sputtered BZN and Pulsed Laser Deposited BZN and pentacene deposited on parylene-C, O_2 plasma treated parylene-C, BZN, and pBZN surfaces to visually confirm microstructure and identify additional smaller scale composition or structure features. Micrographs were taken with the Zeiss Supra-40 in a Class 10 CMOS-compatible cleanroom. For more information regarding SEM, refer to Yao and Wang [10].

Atomic Force Microscopy (AFM):

AFM is image/measurement technique that uses mechanical and electrical forces to map the nature and topography of a surface. As the electrical performance of pentacene is sensitive to its microstructure, analysis was performed on BZN, pBZN, parylene-C, O_2 plasma treated parylene-C, and pentacene on each respective surface. The purpose is to reveal the microstructure

of pentacene films on various surfaces with different surface energies and roughness. Micrographs were taken with a Veeco D3100 Atomic Force Microscope in a Class 10 CMOS-compatible cleanroom and analyzed with software. For more information regarding AFM, refer to Yao and Wang [10].

5.4 CHARACTERIZATION of BZN

5.4.1 X-Ray Diffraction for Structure Determination

X-ray diffraction (XRD) analysis shows these BZN films to have composition of $Bi_{1.5}Zn_1Nb_{1.5}O_7$ and to be nanocrystalline. The analyzed films were fabricated by depositing 150 nm of BZN by RF Sputtering, annealing for one hour at 95° C and exposing the surface to O_2 plasma. This simulates the processing that BZN undergoes during device fabrication.

Crystalline BZN shows diffraction peaks at 29.3° for [222] and 48.8° for [440] [11, 12]. As shown in Figure 5-8, these films show broad peaks at $2\theta \sim 29°$ and $\sim 50°$. The location of these peak indicate some degree of order as they coincide with those of crystalline BZN [12, 13]. The breadth of these peaks is indicative of a nanocrystalline structure. Results from the Evans Analytical Group and hand calculations summarized in Table 5.5 estimate the crystal size to be smaller than the lattice constant of BZN (a=10.552Å [12]). As was discussed in Chapter 2, the high dielectric constant in BZN is a consequence of its cubic pyrochlore structure [13] and films sputtered and processed under similar conditions can have $\sim$5 nm nanocrystals [14]. Thus, it likely that similar crystal sizes exist in the BZN films in this work. More rigorous extraction methods are needed to confirm the actual crystal sizes in these films.

TABLE 5.5: Summary of XRD interplanar spacing (d_{222}) and crystal size (Å) for BZN.

Source	2θ	d_{222} (Å)	FWHM (2θ)	Crystal Size (Å)
ICDD/ICSD Database	29.292°	3.06	-	-
Evans Analytical Group	28.849°	3.0922	6.493°	100% Amorphous
Hand Calculations[1]	29.25°	3.05[7]	6.1°	0.3 [7]

[1]Hand calculations from data provided by Evans Analytical Group

BZN is projected to crystallize above 400°C [15] and to have a higher dielectric constant if it is heat treated above 150°C [5]. When bakeout during the photolithography occurred at 95°C, the dielectric constant was $\sim$40. When bakeout occurred at 130°C, the dielectric constant was $\sim$73. The O_2 plasma step generates heat but the wafer temperature during processing cannot be measured with the available tooling. Using the BZN film as a thermometer, the highest possible temperature this process is predicted to be is $\sim$130°C, as the BZN is still nanocrystalline after all processes have been run and there was not a dramatic change in the dielectric constant. Last, anal-
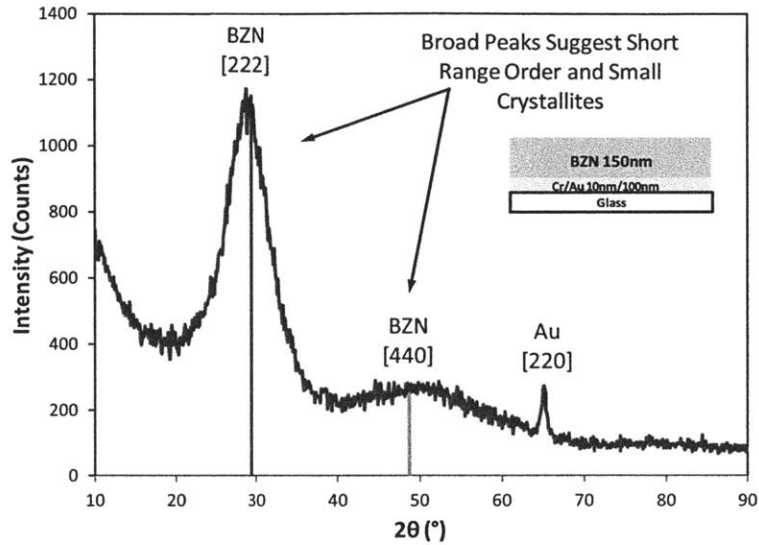
FIGURE 5-8: X-ray Diffraction pattern for BZN films on Au.

ysis shows that the composition of BZN does not change in the subsequent processes necessary to fabricate complete devices.

5.4.2 X-Ray Photospectroscopy for Determination of Composition

XPS analysis shows that the composition of the top surface of the films to be Bi-rich. Analysis also shows that the composition of the surface is O-rich after exposure to O_2 plasma, which is unavoidable when patterning the parylene-C surface treatment for the low voltage OTFTs. This is reported in Table 5.6 and is shown in Figure 5-9. This suggests there may be more Bi-O bonds on the surface, compared to the bulk. As there are more Bi-O bonds on the surface, the surface may have different dielectric properties than the bulk as the Bi-O interactions contribute most to the dielectric constant [16].

TABLE 5.6: Summary of the composition of BZN after different processes. The arrows indicate how the composition of the element changes with the process from the as-deposited film. There was a substantial amount of carbon detected and was assumed to be inert surface contamination. Therefore it is neglected.

Process	Bi (%)	Zn (%)	Nb (%)	O (%)	Compound
Sputtered As Dep.	18.45	2.55 =	8.9	43.6	$Bi_{7.23}Zn_1Nb_{3.24}O_{17.1}$
Sputtered O_2 Plasma	16.55 ↓	2.5 =	7.85 ↓	46.55 ↑	$Bi_{6.62}Zn_1Nb_{3.14}O_{18.62}$
Sputtered Anneal	15.45 ↓	1.45 ↓	6.3 ↓	35.2 ↓	$Bi_{10.66}Zn_1Nb_{4.34}O_{24.28}$
Sputtered O_2 Plasma and Anneal	12.5 ↓	2.45 =	5.3 ↓	51.4 ↑	$Bi_{5.10}Zn_1Nb_{2.16}O_{21}$
PLD	13.67	8.79	13.61	63.93	$Bi_{1.5}Zn_1Nb_{1.5}O_7$
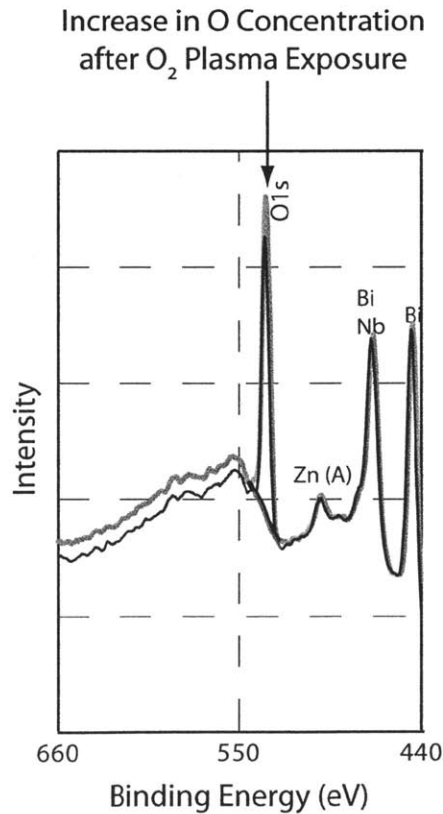
FIGURE 5-9: XPS Spectra of room temperature RF Sputtered BZN films before and after O_2 plasma exposure

104

5.4.3 Atomic Force Microscopy for Determination of Surface Roughness

An O_2 plasma is used to pattern the parylene-C surface treatment in the low voltage OTFTs. As a result, the bare BZN surface is exposed to O_2 plasma which oxidizes this surface and reduces roughness. It is not clear if the surface roughness affects the electrical properties of BZN. The surface smoothing is most likely a thermodynamically driven process as it occurs during the O_2 plasma treatment with heating and oxidation. Regarding the actual patterning of BZN, there is heat in the patterning processes due to photoresist baking but the BZN is covered during the actual etch and does not see the BOE. Figure 5-10 shows that applying the wet etch after the O_2 plasma treatment results in minimal smoothing. This leads to a conclusion that the oxidation with the O_2 plasma etch has the greater impact on surface smoothing than heat itself. Lastly, one can conclude that the surface smoothing achieved by the O_2 plasma etch will leave the smoothest surface possible for this material with the process flow used to build OTFTs in this dissertation. It should be noted that the BZN surface is slightly smoother than the pBZN surface as shown in Figure 5-11 as roughness may impact the electrical properties of pentacene as its microstructure is sensitive to the roughness of the surface it is deposited on.

105

After Deposition
RMS Roughness: 1.45nm

O$_2$ Plasma Etch
RMS Roughness: 0.39nm

Wet Etch
RMS Roughness: 0.66nm

O$_2$ Plasma Etch and Wet Etch
RMS Roughness: 0.38nm
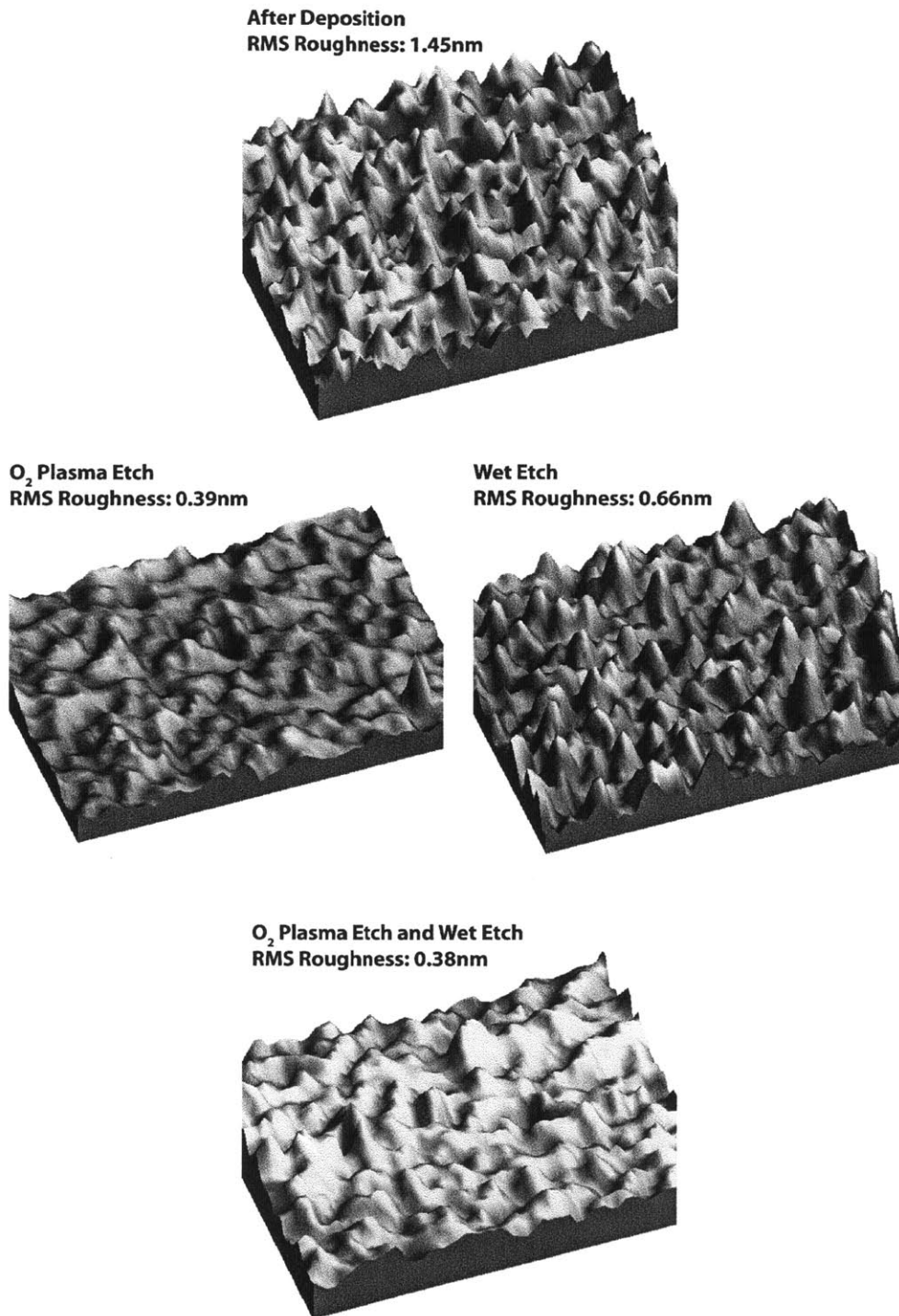
FIGURE 5-10: The AFM micrographs illustrate how surface roughness evolves throughout processing. The O$_2$ plasma has a more notable effect on reducing surface roughness that heat.

106

BZN Before Semiconductor Deposition
RMS Roughness: 1.09nm

pBZN Before Semiconductor Deposition
RMS Roughness: 1.57nm
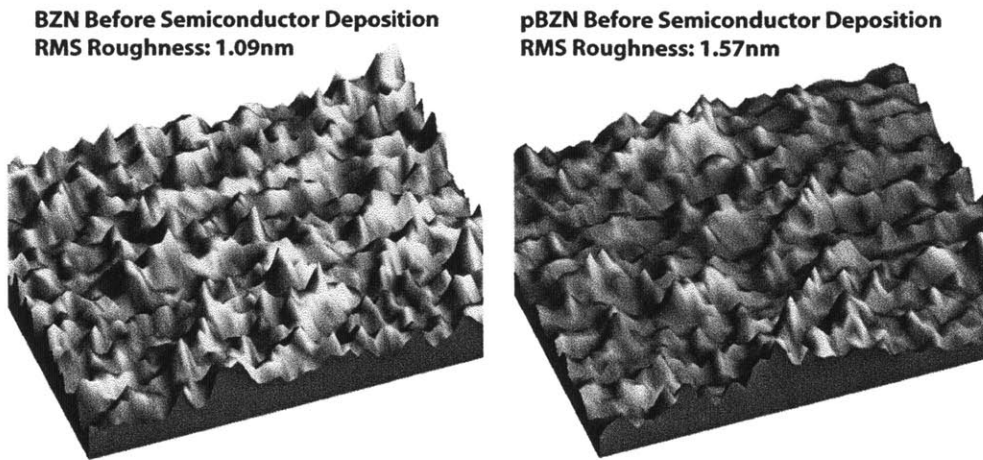
FIGURE 5-11: AFM micrographs of the insulator surface before and after parylene surface treatment. The roughness varies by Å

5.4.4 Scanning Electron Microscopy for Microstructural Analysis

SEM images show the sputtered BZN film surface to be inhomogeneous while the more porous BZN film deposited by PLD (pulsed laser deposition) is homogeneous. The inhomogeneities are likely to be Bi-rich clusters indicated by XPS. The light streaks in the micrograph are assumed to be more metallic as metals appear brighter in SEM images. These metallic inclusions indicate parasitic conductions paths which may prove detrimental to the insulator breakdown strength. PLD is a better technique for growing these films, however available tooling for processing on a 100mm wafer is currently limited [17].
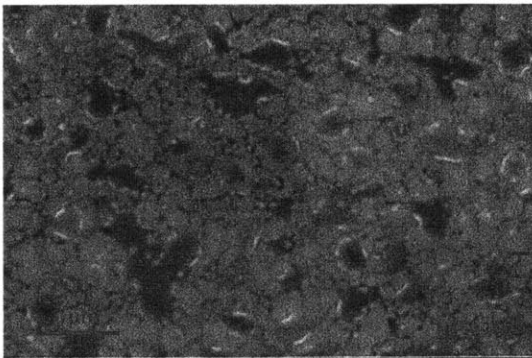
FIGURE 5-12: A 30 nm thick layer of BZN that was deposited by RF Sputtering Magnification ×45k
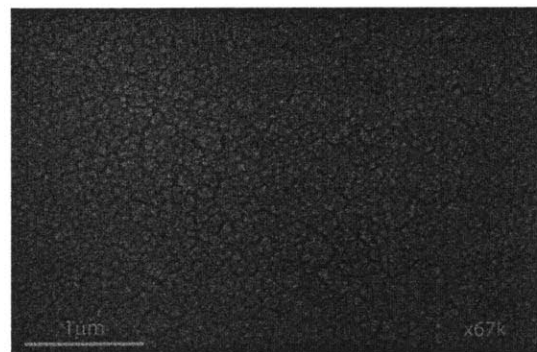
FIGURE 5-13: A ~200 nm thick layer of BZN that was deposited by Pulsed Laser Deposition Magnification ×67k

107

5.4.5 Static Sessile Drop Technique for Extraction of Surface Energy

As discussed in Chapter 5, the surface energy provides an indication of how pentacene will grow on a surface (2D growth or 3D growth). BZN has a higher surface energy than pBZN due to the polar contribution (γ_P), as shown in Table 5.7. The drop profiles of DI water on BZN after various processes are shown in Figure 5-14.

It can be concluded that the metal-oxygen bonds (Bi-O, Nb-O) in BZN are responsible for this polar contribution as they are polar. As parylene-C is less polar than BZN, it is apparent how the surface treatment reduces this polar contribution. It is

TABLE 5.7: Summary of surface energy for BZN and pBZN surfaces prior to semiconductor deposition. γ=Total Surface Energy, γ_D = Dispersive Surface Energy, γ_P = Polar Surface Energy

Surface	BZN	pBZN
Contact Angle (DI Water)	58°	78°-92°
γ (mN/m)	43	28
γ_D (mN/m)	15	14
γ_P (mN/m)	28	14
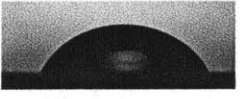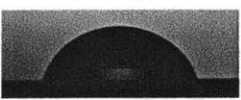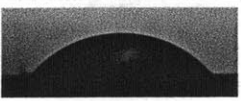
Surface	Contact Angle (θ)	Image
Glass (No BZN)	26	
As Deposited BZN	62	
Annealed BZN	80	
BZN Plasma O$_2$	56	
pBZN	92	

FIGURE 5-14: Contact angles with DI water on BZN throughout processing.

108

speculated that the parylene-C surface treatment is also passivating charge traps or interface states (Q_{it}) on the BZN surface. It is expected that such passivation will impact breakdown behavior of the insulator and the electrical properties of pentacene. As was discussed in Chapter 2, the electrical properties of pentacene are sensitive to its microstructure which is sensitive to the energy and roughness of the surface that it is deposited on. Figure 5-14 suggests the O_2 plasma increases the surface energy of BZN and may be a result of the increased O concentration and therefore polar contribution (γ_P) on the surface.

Yoshida et al. report a surface energy ranging from 40-50 mN/m results in optimal charge transport (high mobility μ) [18] in pentacene. However in the case reported by Yoshida et al., the dispersive component (γ_D) likely contributed more to the surface energy as all organic surfaces were studied, though the dispersive component (γ_D) is not reported. In our case, the polar component (γ_P) contributes significantly to its surface energy, as BZN is inorganic with polar bonds. Chou et al. reported 38 mN/m [19] to be optimal while Yang et al., reported lower surface energies around 30 mN/m [20] show better charge transport in pentacene. Both report that the surface with the larger polar contribution (γ_P) has worse charge transport. From this, it is expected that pentacene on BZN will show worse charge transport (lower μ) compared to pentacene on pBZN.

5.5 CHARACTERIZATION of PARYLENE-C

5.5.1 Atomic Force Microscopy for Determination of Surface Roughness

Generally, the parylene-C surface shows nanometer scale roughness independent of the surface it is deposited on. The exception is where the roughness of the underlying surface exceeds that of the parylene-C as in the case of the parylene-C on the Au in Figure 5-15. The parylene-C insulator surfaces are generally rougher than the BZN-based insulator surfaces. The O_2 plasma surface treatment appears to roughen the surface while quenching in an organic solvent (acetone or isopropanol) appears to remove this roughness. It is not apparent why this smoothing happens, but may be related to surface reconstruction and the passivation of the dangling bonds created by the O_2 plasma treatment.

Parylene-C on Glass
RMS Roughness = 4nm

(B)
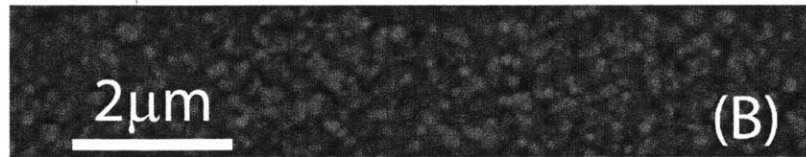
Parylene-C on BZN
RMS Roughness = 4nm

(C)

Parylene-C on Au
RMS Roughness = 6nm

(D)
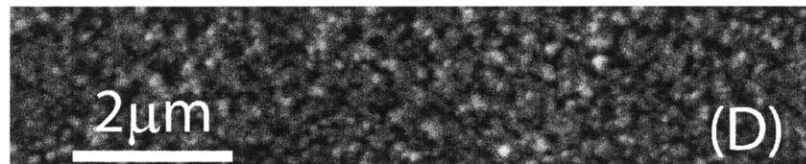
O_2 Plasma Treated Parylene-C (Quenched)
RMS Roughness = 4nm

(E)
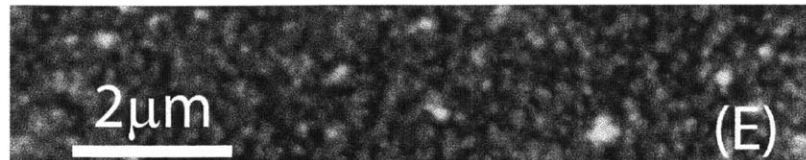
O_2 Plasma Treated Parylene-C (Fresh)
RMS Roughness = 5nm

FIGURE 5-15: AFM micrographs of 200 nm parylene-C on various surfaces

5.5.2 Static Sessile Drop Technique for Extraction of Surface Energy

O_2 plasma etches parylene-C. Briefly treating the parylene-C with O_2 plasma, will "damage" this surface and create dangling bonds or interface states (Q_{it}) that serve as charge traps, which affects the electrical properties of pentacene [3]. The evidence of "damage" from O_2 plasma is the increased surface energy (specifically the polar contribution), extracted from contact angle measurements. This is summarized in Table 5.8 and Figure 5-16.

Table 5.8 shows the variability in surface energy as a result of O_2 plasma treatments. The surface energy of the O_2 plasma treated surfaces depends on time spent at am-

TABLE 5.8: Summary of surface energy for parylene-C and O_2 plasma treated parylene-C surfaces prior to semiconductor deposition. Exposure time is 6 seconds at 100 W in an AutoGlow Plasma System by Glow Research.

Surface	PAR	O_2 PAR	
		(Stale)	(Fresh)
Contact Angle (DI Water)	94°	56°	20°
γ (mN/m)	38	45	79
γ_D (mN/m)	38	9	4
γ_P (mN/m)	0.4	36	75
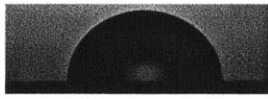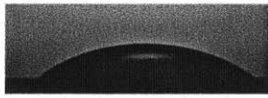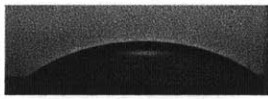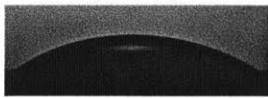
Surface	Contact Angle (θ)	Image
As Deposited	94	
O_2 Plasma 6 sec	38	
O_2 Plasma 30sec	38	
O_2 Plasma 60 sec	34	

FIGURE 5-16: Contact angles with DI water on parylene-C with different O_2 plasma exposure times.

bient after O_2 plasma exposure and indicated with the stale and fresh samples. The stale samples were stored in an ambient environment for $\sim$3 weeks before analysis while the fresh samples were measured immediately after treatment. This poses a reproducibility issue as time from treatment to pentacene deposition can be difficult to control. This issue may be addressed by applying a "solvent quench" to stabilize the surface. The O_2 plasma treated surface is most reactive immediately after processing and the ambient atmosphere slowly passtivates the surface. The "solvent quench" is designed to normalize and stabilize the reactive surface to reestablish reproducibility and predictability in the process. Further, such a "quench" is unavoidable if the surface treatment is patterned, as solvents are used to strip the photoresist after patterning.

5.6 CHARACTERIZATION of PENTACENE
5.6.1 X-Ray Diffraction for Structure Determination
As crystal structure is related to mobility, XRD was performed on pentacene thin films to determine the structure and how it is affected by heating during photolithography on the BZN and pBZN surfaces. Analysis shows that crystals grow on both organic and inorganic surfaces. The d_{001} peak locations shown in Table 5.11 match to those of the thin film phase as reported [21, 22]. Figure 5-17 [7, 21] shows that pentacene on pBZN shows more distinct and defined peaks on higher order diffractions planes compared to pentacene on BZN. This is indicative of 3D crystal growth and better ordering for the pentacene grown on pBZN compared to BZN. This is as expected as pentacene grows better on organic interfaces [20, 19, 23]. Table 5.11 summarize the sizes of crystallites determined from the XRD spectra.

Figure 5-18 [22] shows that pentacene on pBZN after heat treatment has more distinct and defined peaks than before heating. This implies larger crystallites for the pBZN and/or grain ripening for pentacene after heating. This is expected as the increased temperature leads to greater diffusion or grain ripening. At the [002] diffraction peak, there appears to be a doublet forming. This may correspond to formation of the bulk phase with the lower mobility. The coexistence of the bulk phase and thin film phase can degrade carrier mobility [24, 25].

TABLE 5.9: Interplanar spacing (d_{001}) and crystallite sizes extracted from XRD for pentacene on BZN and pBZN

Surface	d_{001} (nm)	Crystallite Size (nm)
BZN After Heat	1.52	17
pBZN Before Heat	1.50	20
pBZN After Heat	1.49	33

FIGURE 5-17: GIXRD pattern comparing pentacene deposited on BZN to pentacene deposited on pBZN after heating
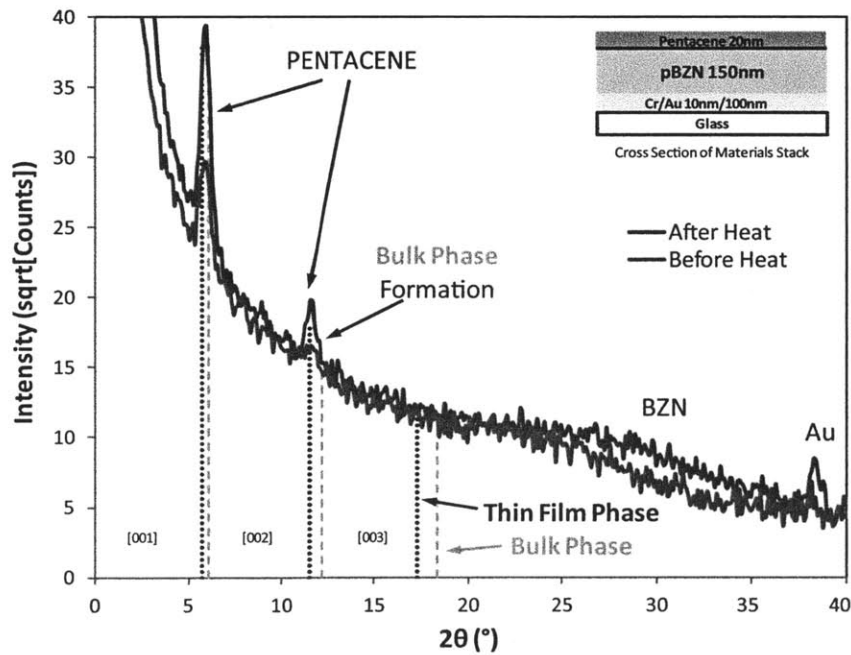
FIGURE 5-18: GIXRD pattern comparing pentacene deposited on pBZN before and after heating.

113

5.6.2 Atomic Force Microscopy for Microstructural Analysis

AFM images for 20 nm pentacene deposited on PAR, O_2 PAR, BZN and pBZN surfaces can be seen in Figure 5-19 and summarized in Table 5.10. These micrographs show the evolution of the pentacene microstructure as a result of heat treatment. Literature reports growth of pentacene on similar surfaces (oxides and polymer surfaces) at room temperature are likely to be completely condensed [23, 26]. This means that the final microstructure will depend heavily on surface diffusion. Pentacene has the largest grains on the BZN surface as it has the highest surface energy and is the most flat. It should also be noted that the pentacene grains on this surface show poor coalescence which has been attributed to poor electrical performance [20]. This is well supported by literature [24, 27]. The pBZN surface has the same surface energy as the PAR surface but shows larger grains. Clearly, pentacene on pBZN diffuses faster as the surface is flatter [28]. This implies the surface roughness is limiting grain growth in these systems.
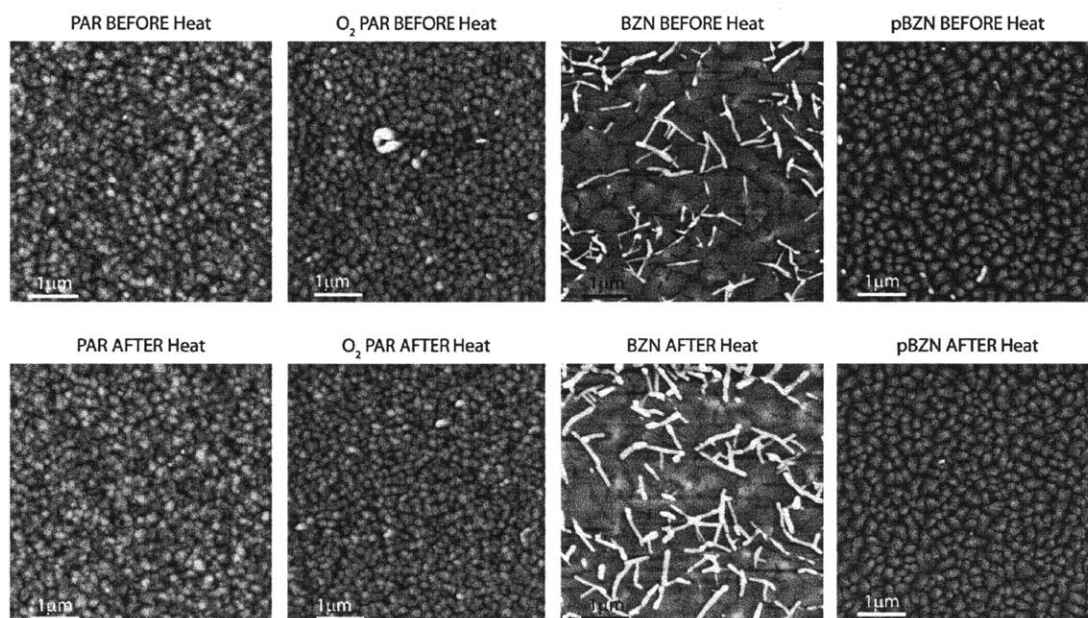
FIGURE 5-19: AFM images for pentacene on PAR, O_2 PAR, BZN, and pBZN surfaces before and after heating

Of the four surfaces, pentacene on the BZN surface shows more prominent changes in microstructure due to heat. In addition to the ramified grains that are growing laterally, there appears to be elongated ribbon-like structures resting on top of the dendritic grains. The ribbon-like structures coarsen upon heating. These elongated structures have been identified as the bulk phase [24, 29], though not always detectable by XRD [20]. This morphology appears as a consequence of "buckling" of the pentacene thin films transforming into the bulk phase in response to stress. This

TABLE 5.10: Grain sizes and other features extracted from AFM micrographs for pentacene on PAR, O_2 PAR, BZN and pBZN

Surface Treatment and Heat	Grain Size (nm)		Ribbon Size (nm)	
Heat	Before	After	Before	After
Parylene-C	200	200	-	-
O₂ PAR	200	200	-	-
BZN	620	620-700	30-40	60-80
pBZN	115-430	210-350	90	-

inherently implies that both the thin film and bulk phase are present in these films [24].

The crystallite size extracted from XRD is smaller than the grain size revealed in AFM which is summarized in Table 5.10. This may suggest that the coarser grains seen in the AFM images are composed of smaller crystallites detected by XRD or that both the bulk phase and the thin film phase are present at crystal sizes that cause peak broadening. The peaks are broad such that the respective XRD peak for each phase is not distinct.

5.6.3 Scanning Electron Microscopy for Microstructural Analysis

The microstructure of pentacene deposited on Au forms what appear to be interlaced ribbons. It well accepted that pentacene deposited on metals has poor electrical characteristics. SEMs show ribbons of similar size grow on all insulator surfaces however less densely. AFM and SEM show that the BZN surface has the highest density of ribbons compared to the other three surfaces. The ribbons seen here are slightly smaller than those seen in AFM; however that may be a result of tip dilation and further supports the existence of two separate phases. SEMs of pentacene on these surfaces show grain sizes comparable to those seen in AFM.

The grain sizes observed with AFM and SEM do not match those determined from XRD. In regards to the BZN and pBZN surfaces, to explain that mobility is larger for pentacene on the pBZN surface, one can attribute this to a well formed grain structure that is seen with AFM, the interplanar spacing of the pentacene crystals extracted with XRD, or a minimal existence of bulk phase pentacene. Better transport in pentacene on the BZN surface can be attributed to the courser grains seen in the AFM images. However Yang et al. indicate that such ramified grains show worse transport due to poor grain connectivity [20]. One can attribute a degraded mobility upon heating to the appearance of the bulk phase and an improvement of mobility to an increase in grain size. The result from actual OTFTs in are discussed

115
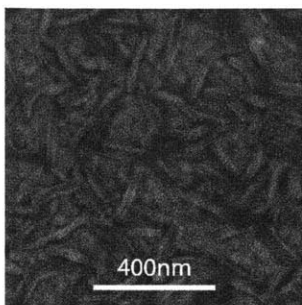
FIGURE 5-20: SEM micrographs for pentacene on Au. The ribbon-like crystallites are shown.

PAR   O$_2$ Plasma   BZN   pBZN
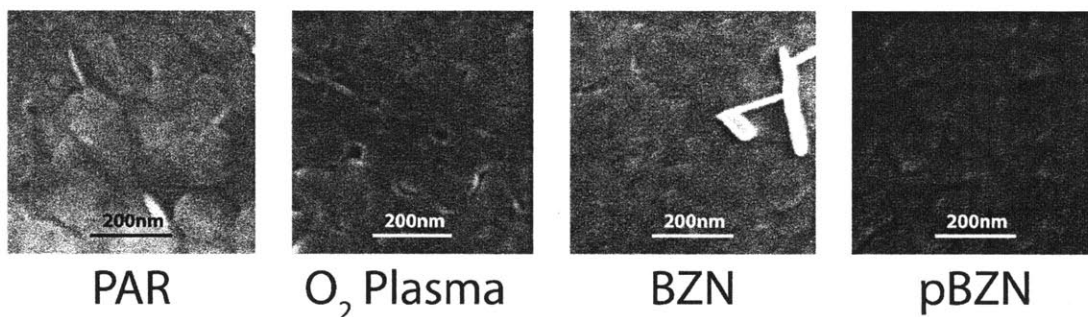
FIGURE 5-21: SEM micrographs for pentacene on PAR, O$_2$ PAR, BZN, and pBZN surfaces.

TABLE 5.11: Grain sizes and other features extracted from SEM for pentacene on Au, PAR, O$_2$ plasma, BZN and pBZN

Surface	Grain Size (nm)	Ribbon Size (nm)
Au	–	24
Parylene-C	150-180	20
O$_2$ PAR	120-180	23
BZN	420	29-35
pBZN	183	93

in Chapter 6 and Chapter 8, will ultimately reveal how the pentacene performs with the microstructures revealed by AFM, SEM, and XRD.

5.7 CONCLUSION

While the process presented in this chapter is effective in creating reliable and reproducible OTFTs, there are a number of issues that lead to less than optimal performance. The following issues have an impact on performance and should be addressed in future investigations.

PENTACENE AND HEAT

The heating of the pentacene during photolithography leads to the ripening of pentacene crystallites and grains (better mobility) but encourages the development of the bulk phase (worse mobility). Electrical data will reveal which has the most effect on performance.

SURFACE OF BZN

The stoichiometry of the surface of the sputter deposited BZN does not match that of the bulk. The surface is Bi-rich which indicates parasitic metallic conductive paths and therefore reduced reliability and breakdown resistance. Further, the BZN surface is exposed to O_2 plasma during surface treatment patterning, before the semiconductor deposition. This increases oxygen concentration in the surface of the film. Therefore, the surface composition of the BZN, will not match that of the bulk, though this may not be detrimental to performance.

PARYLENE-C SURFACE TREATMENT ON BZN: THICKNESS

The SCS Parylene-C Coater is optimized for depositing films thicker than 100 nm. Depositing 1-3 nm of parylene-C consistently is a problem. Methods should be explored to make the process more consistent for depositing precise 1 nm films.

O_2 PAR PROCESS CONTROL

This process creates a very reactive surface, which is difficult to control. The reactivity of this surface, or the density of dangling bonds or interface states directly relates to electrical characteristics of pentacene. Exposing the surface to a solvent can reduce the density of these dangling bonds are restore some process control.

5.8 SUMMARY

This is a brief, listed summary of the most relevant findings in this chapter.

PROCESS FLOW

- The fully photolithographic process used to build OTFT allows for the integration of devices with two distinct threshold voltages by applying and patterning surface treatments on the gate insulator.

- The maximum temperature predicted for the entire process is estimated to be 130° C.

- BZN and pBZN gate insulators can be integrated on one wafer. This will enable the full integration of devices with two threshold voltages on the same wafer.

- PAR and O_2 PAR gate insulators can be integrated on one wafer. This

117

will enable the full integration of devices with two threshold voltages on the same wafer.

MATERIALS CHARACTERIZATION

BZN is deposited by RF magnetron sputtering at room temperature at 95 W with an argon : oxygen ratio of 9:3.

- XRD shows BZN to be have very small crystalline domains and the bulk composition to be $Bi_{1.5}Zn_1Nb_{1.5}O_7$.

- The as-deposited surface composition is Bi-rich and oxygen concentration increases with the O_2 plasma etch used for defining the surface treatments in the low voltage OTFTs.

- O_2 plasma smoothes the BZN surface and increases surface energy.

- The oxidation of BZN in O_2 plasma has a greater impact on surface smoothing in BZN than the heat alone.

PARYLENE-C is deposited by CVD with the substrate at room temperature.

- O_2 plasma roughens this surface but can be smoothened with an organic solvent quench.

- All parylene-C surfaces are rougher than BZN surfaces.

PENTACENE is deposited with the substrate at room temperature by thermal evaporation in vacuum at $\sim$2 nm/min at a pressure of 2×10^{-7} torr.

- The thin film phase exists in these pentacene films under the specified deposition conditions. The bulk phase begins to form with the heat used during photolithography which has a max temperature of 95°C.

- Grain structure is most influenced by surface roughness followed by surface energy. Of the surfaces that show comparable roughness (BZN and pBZN), the surface with the lower energy, pBZN showed better formed grains. This implies that the films are completely condensed and the microstructure is determined by surface diffusion, in reference to the kinetics of thin film evolution.

- The pentacene on all surfaces is suspected to form the bulk phase after heating or annealing. Pentacene on the BZN surface has largest grain growth and shows two phases most prominently, one which is suspected to be the low mobility bulk phase.

118

5.9 REFERENCES

[1] Y. Choi, I. D. Kim, H. L. Tuller, and A. I. Akinwande, "Low-voltage organic transistors and depletion-load inverters with high-κ pyrochlore BZN gate dielectric on polymer substrate," *IEEE Transactions on Electron Devices*, vol. 52, no. 12, pp. 2819–2824, 2005.

[2] P. W. Peacock and J. Robertson, "Band offsets and schottky barrier heights of high dielectric constant oxides," *Journal of Applied Physics*, vol. 92, no. 8, pp. 4712–4721, 2002.

[3] A. Wang, I. Kymissis, V. Bulovic, and A. Akinwande, "Tunable threshold voltage and flatband voltage in pentacene field effect transistors," *Applied Physics Letters*, vol. 89, no. 11, p. 112109, 2006.

[4] I. Kymissis, A. I. Akinwande, and V. Bulovic, "A lithographic process for integrated organic field-effect transistors," *Journal of Display Technology*, vol. 1, no. 2, pp. 289–294, 2005.

[5] J. H. Park, W. S. Lee, N. J. Seong, S. G. Yoon, S. H. Son, H. M. Chung, J. S. Moon, H. J. Jin, S. E. Lee, J. W. Lee, H. D. Kang, Y. K. Chung, and Y. S. Oh, "Bismuth-zinc-niobate embedded capacitors grown at room temperature for printed circuit board applications," *Applied Physics Letters*, vol. 88, no. 19, 2006.

[6] J. Lumsden, "ASM Handbook, Volume 10 - Materials Characterization."

[7] C. Hammond, *The basics of crystallography and diffraction*. Oxford University Press, 2001.

[8] Carr and Alain, "Polar interactions at liquid/polymer interfaces," *Journal of Adhesion Science and Technology*, vol. 21, no. 10, pp. 961–981, 2007.

[9] D. K. Owens and R. C. Wendt, "Estimation of the surface free energy of polymers," *Journal of Applied Polymer Science*, vol. 13, no. 8, pp. 1741–1747, 1969.

[10] N. Yao and Z. Wang, *Handbook Of Microscopy For Nanotechnology*. Kluwer Academic Publishers, 2005.

[11] X. L. Wang, H. Wang, and X. Yao, "Structures, phase transformations, and dielectric properties of pyrochlores containing bismuth," *Journal of the American Ceramic Society*, vol. 80, no. 10, pp. 2745–2748, 1997.

[12] I. Levin, T. G. Amos, J. C. Nino, T. A. Vanderah, C. A. Randall, and M. T. Lanagan, "Structural study of an unusual cubic pyrochlore $Bi_{1.5}Zn_{0.92}Nb_{1.5}O_{6.92}$," *Journal of Solid State Chemistry*, vol. 168, no. 1, pp. 69–75, 2002.

[13] I. D. Kim, M. H. Lim, K. Kang, H. G. Kim, and S. Y. Choi, "Room temperature fabricated ZnO thin film transistor using high-κ $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_{7.0}$ gate insulator prepared by sputtering," *Applied Physics Letters*, vol. 89, no. 2, p. 3, 2006.

[14] J. W. Lu, Z. Q. Chen, T. R. Taylor, and S. Stemmer, "Composition control and dielectric properties of bismuth zinc niobate thin films synthesized by radio-frequency magnetron sputtering," *Journal of Vacuum Science and Technology A*, vol. 21, no. 5, pp. 1745–1751, 2003.

[15] M.-H. Lim, K. Kang, H.-G. Kim, I.-D. Kim, Y. Choi, and H. L. Tuller, "Low leakage current-stacked $MgO/Bi_{1.5}Zn_{1.0}Nb_{1.5}O_{7.0}$ gate insulator— for low voltage ZnO thin film transistors," *Applied Physics Letters*, vol. 89, no. 20, pp. 202908–3, 2006.

[16] D. Shihua, Y. Xi, and Y. Li, "Study of structure and dielectrc properties of non-stoichiometric Bi_2O_3-ZnO-Nb_2O_5 ceramics," *Journal of Electroceramics*, vol. 21, no. 1, pp. 435–438, 2008.

[17] T. Venkatesan and S. M. Green, "Pulsed Laser Deposition: Thin Films in a Flash," *The Industrial Physicist*, vol. 2, pp. 22–24, September 1996.

[18] M. Yoshida, S. Uemura, T. Kodzasa, T. Kamata, M. Matsuzawa, and T. Kawai, "Surface potential control of an insulator layer for the high performance organic FET," *Synthetic Metals*, vol. 137, no. 1-3, pp. 967–968, 2003.

[19] C. Wei-Yang, K. Chia-Wei, C. Horng-Long, C. Yi-Ren, T. Fu-Ching, Y. Feng-Yu, S. Dun-Yin, and L. Chi-Chang, "Effect of surface free energy in gate dielectric in pentacene thin-film transistors," *Applied Physics Letters*, vol. 89, no. 11, p. 112126, 2006.

[20] S. Y. Yang, K. Shin, and C. E. Park, "The Effect of Gate-Dielectric Surface Energy on Pentacene Morphology and Organic Field-Effect Transistor Characteristics," *Advanced Functional Materials*, vol. 15, no. 11, pp. 1806–1814, 2005.

[21] M. Kitamura and Y. Arakawa, "Pentacene-based organic field-effect transistors," *Journal of Physics-Condensed Matter*, vol. 20, no. 18, 2008.

[22] C. C. Mattheus, A. B. Dros, J. Baas, G. T. Oostergetel, A. Meetsma, J. L. de Boer, and T. T. M. Palstra, "Identification of polymorphs of pentacene," *Synthetic Metals*, vol. 138, no. 3, pp. 475–481, 2003.

[23] B. Stadlober, U. Haas, H. Maresch, and A. Haase, "Growth model of pentacene on inorganic and organic dielectrics based on scaling and rate-equation theory," *Physical Review B (Condensed Matter and Materials Physics)*, vol. 74, no. 16, p. 165302, 2006.

[24] D. J. Gundlach, T. N. Jackson, D. G. Schlom, and S. F. Nelson, "Solvent-induced phase transition in thermally evaporated pentacene films," *Applied Physics Letters*, vol. 74, no. 22, pp. 3302–3304, 1999.

[25] C. D. Dimitrakopoulos and P. R. L. Malenfant, "Organic thin film transistors for large area electronics," *Advanced Materials*, vol. 14, no. 2, pp. 99–117, 2002.

[26] P. c. v. R. Ribič, V. Kalihari, C. D. Frisbie, and G. Bratina, "Growth of ultrathin pentacene films on polymeric substrates," *Phys. Rev. B*, vol. 80, p. 115307, Sep 2009.

[27] S. Verlaak, S. Steudel, P. Heremans, D. Janssen, and M. S. Deleuze, "Nucleation of organic semiconductors on inert substrates," *Physical Review B*, vol. 68, no. 19, p. 195409, 2003.

[28] S. E. Fritz, T. W. Kelley, and C. D. Frisbie, "Effect of dielectric roughness on performance of pentacene TFTs and restoration of performance with a polymeric smoothing layer," *The Journal of Physical Chemistry B*, vol. 109, no. 21, pp. 10574–10577, 2005.

[29] G. Dong, I. Susumu, and S. Koichiro, "Modified bimodal growth mechanism of pentacene thin films at elevated substrate temperatures," *Journal of Physics: Condensed Matter*, vol. 22, no. 26, p. 262001.

Chapter 6

Low Voltage, Dual V_T, Thin Film Transistors and Integrated Circuits

6.1 MOTIVATION and STATE of the ART

A key advantage of using pentacene for the semiconductor in OTFTs is that its mobility is comparable to amorphous Si. However, there is still a fundamental need for pentacene based OTFTs to operate at lower voltages. For this investigation, low operating voltages are obtained by using a high-κ gate insulator.

Table 6.1 is a summary of organic transistors that have been reported in recent literature. The table lists the semiconductor, the insulator and the patterning approach. It also indicates if the devices have two distinct threshold voltages on the same substrate, if circuits were reported and if the devices are integrated were reported. Most OTFTs that use high-κ dielectrics do not use photolithography as a means to pattern the semiconductor. There are many reports of integrated circuits based on OTFTs, however they use low-κ materials (higher operating voltages) or one threshold voltage (less energy efficient).

Notable Reports from Literature
Shang et al. and Koo et al. reported an integrated circuit using a high-κ material (Al_2O_3 κ=9) for the gate dielectric [1, 2]. These circuits however did not feature two distinct threshold voltages. Klauk et. al reported a very low power integrated circuit technology based on AlO_x (κ=9 with self-assembled monolayers (SAMs) for improved dielectric reliability) [3]. Two threshold voltages and therefore low power consumption, were achieved by using n-type (hexadecafluorocopperphthalocyanine) and p-type (pentacene) organic semiconductors. This report shows that low power

123

organic CMOS circuits are possible, however large scale integration is currently impossible with the unstable n-type semiconductors and the shadow masking patterning techniques used. Nausieda et al. reported mixed-signal integrated circuits with two threshold voltages by using gate metal engineering and a fully photolithographic technology[4, 5]. This showed that photolithography can be used to build complex integrated circuits. However, the higher operating voltages were not addressed. As shown in Table 6.1, no reports were found of integrated circuits using high-κ gate insulators, and the integration of two distinct threshold voltages with a photolithographically patterned semiconductor layer in one technology, except for this work.

LEGEND FOR FOLLOWING TABLE

Semi.= semiconductor material

Patt.=Method used to pattern semiconductor. In the case of "Photo." the material in parenthesis following is used for encapsulation

(I)? $\#V_T$ = Number of distinct threshold voltages reported, where "(I)" indicates of the integration of multiple was reported.

(I)(C)? indicates of circuits were reported (C) and if they were integrated (I)

TABLE 6.1: **State of the Art for Low Voltage OTFT and Circuits**

Source	Dielectric	Semi.	Patt.	(I)? $\#V_T$	(I)(C)?
Gay et al. [6]	PVP[1] κ=3.6	Pentacene	NS[2]	1	(Y)(Y[3])
Cantatore et al. [7]	PVP κ=3.6	Pentacene	Y	(N)2	(Y) (Y)
Sirringhaus et al. [8]	PVP κ=3.6	F8T2[4]	None	1	(Y)(Y)
Shi et al [9]	PVP κ=3.6	Pentacene	NS	1	N[5]
Lee et al. [10]	PVP κ=3 P(VDTrFE)[6] κ=6-9	Pentacene	Shadow Mask	(N)2	N
Klauk et al. [3]	PVP κ=3.6	Pentacene	NS	1	(Y)(Y)
Nausieda et al. [5]	Parylene-C κ=3	Pentacene	Photo. (Parylene)	2	(Y)(Y)
Zhou et al. [11]	SiO$_2$ κ=3.6 SiN κ=7	Pentacene	Photo. (PVA[7], Parylene)	1	N
Kane et al. [12]	SiO$_2$ κ=3.6	Pentacene	Photo. (PVA)	1	(Y)(Y)
Wang et a.l [13]	SiO$_2$ κ=3.6	CuPc	Photo. (PVP)	1	N
Sung et al. [14]	SiO$_2$ κ=3.6	TIPS-Pentacene	None	1	(Y)(Y)

---

[1] poly-4-vinyphenol   [2] Not Specified   [3] Yes   [4] poly(9,9-dioctylfluoreneco-bithiophene)   [5] No

[6] poly(vinylidene fluoride/trifluoroethylene)   [7] polyvinyl alcohol

TABLE 6.1: State of the Art for Low Voltage OTFT and Circuits (cont.)

Source	Dielectric	Semi.	Patt.	(I)? $\#V_T$	(I)(C)?
Jia et al. [15]	SiO_2 κ=3.6	P3HT[8]	Photo. (Parylene, Al_2O_3)	1	N
Fukuda et al. [16]	AlO_x SAM[9]	DNTT [10]	NS	1	(Y)(Y)
Koo et al. [17]	Al_2 O_3 κ=8 ZrO_2 κ=24	Pentacene	NS	2	(?)(Y)
Koo et al. [2]	Al_2 O_3 κ=8 HMDS	Pentacene	NS	1	(?)(Y)
Klauk et al. [18]	AlO_x κ=9 SAM[11] κ=2.5	Pentacene, F16CuPc[12]	Shadow Mask	2	(Y)(Y)
Shang et al. [1]	Al_2O_3 κ=8	Pentacene	NS	1	(Y)(Y)
Zhang et al. [19]	HfO_2 κ=14.9 ODPA[13]	Pentacene	NS	(N)2	N
Shang et al. [20]	ZrO_2 κ=22 PMMA[14] κ=2.6	CuPc[15]	NS	(N)2	N
Choi et al. [21]	BZN[16] κ=50	Pentacene	Shadow Mask	2	(?)(Y)
Chia-Yu et al. [22]	BST[17] κ=15.57	Pentacene	NS	1	N
Han et al. [23]	SBT[18] κ=50	P-3HT	NS	1	(N)(Y)
Liang et al. [24]	Ta_2O_5 κ=17	Pentacene	NS	(N)Many	N
Majewski et al. [25]	TiO_2 κ=21 PAMS[19]	Pentacene	NS	1	N
This Work	**BZN κ=40**	**Pentacene**	**Photo. (Parylene)**	**2**	**(Y)(Y)**

Technical Approach

As reported by Choi et al., BZN ($Bi_{1.5}Zn_1Nb_{1.5}O_7$) based OTFTs not only operate at low voltages but the threshold voltage can be shifted from depletion-mode (V_T >0V) to enhancement-mode (V_T <0V) with the application of a parylene-C surface treatment [21]. While single stage inverters were demonstrated, the fabrication methods were not suitable for realizing circuits with higher complexity and more than one logic gate, such as a ring oscillator. This dissertation builds on the work of Choi et al. [21], by using photolithography as opposed to shadow masking, thereby allowing scalability, precision, and reproducibility via a photolithographic patterning process inspired by devices and circuits reported by Nausieda et al. [5] and Kymissis et al. [26]. The reported circuits serve as a proof of concept that fully functioning integrated circuits

[8] poly (3-hexylthiophene)   [9] n-tetradecylphosphonic acid   [10] dinaphtho[2,3-b:2,3-f]thieno[3,2-b] thiophene   [11] n-octadecylphosphonic acid)   [12] hexadecafluorophthalocyaninatocopper   [13] octadecylphosphonic acid   [14] poly(methyl methacrylate)   [15] copper phthalocyanine   [16] $Bi_{1.5}Zn_1Nb_{1.5}O_7$ [17] $Ba_{1.2}Ti_{0.8}O_3$ [18] $SrBi_2Ta_2O_9$ [19] poly(α-methlystyrene)

can be built with the high-κ BZN gate insulator and V_T shifting surface treatments. Improvements are proposed to realize the full potential of the technology regarding low voltage operation.

6.2 ELECTRICAL CHARACTERIZATION of TFTS

In this section, the parameters low voltage OTFTs fabricated with the previously mentioned processes (Chapters 4 and 5) and materials (Chapter 2) will be discussed.

6.2.1 Raw Data, Extracted Parameters, and Observations

Output and Transfer Characteristics

Electrical characterization was done in a dark, ambient atmosphere with an Agilent 4156C Semiconductor Parameter Analyzer at room temperature. Examples of completed OTFTs are shown in Figure 6-2. The Si Long Channel MOSFET model suggests that I_D should scale linearly with the channel width (Figure 6-3) and linearly with the inverse of the channel length (L) (Figure 6-4), which is the case for this
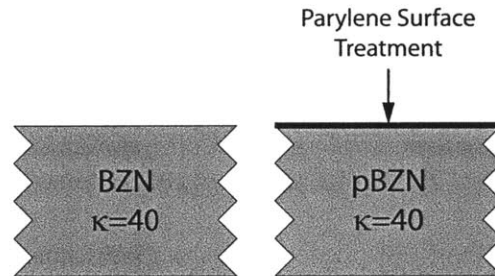
FIGURE 6-1: Insulators stacks explored low voltage OTFTs
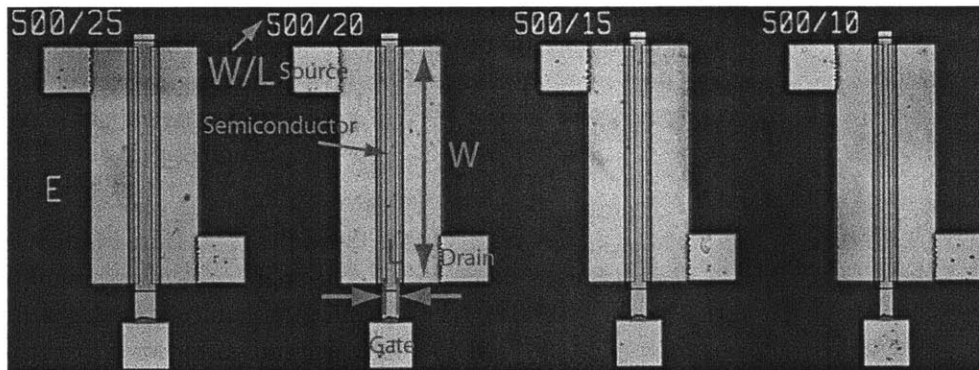
FIGURE 6-2: Top View of Real OTFTs. Channel Length (L), Channel Width (W), Gate, Source, Drain, and Semiconductor are defined. Channel Lengths (L) 25 μm, 20 μm, 15 μm, 10 μm all having a Channel Width (W) of 500 μm.

technology. Functional TFTs where fabricated from both BZN and pBZN insulators.
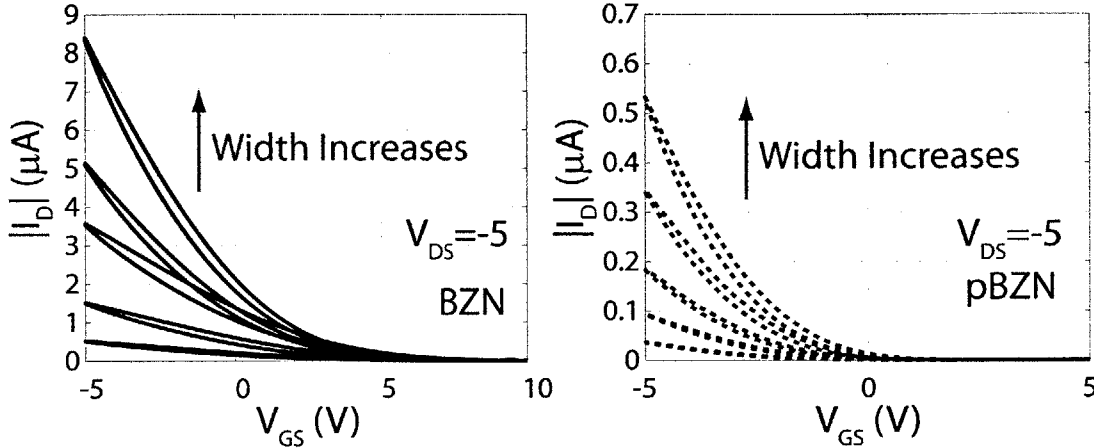
FIGURE 6-3: Transfer Characteristics for OTFTs with BZN and pBZN insulators at different channel widths (W)=100, 250, 500, 1000, 1500 μm, channel length (L)=10 μm. I_D increases as the channel width increases.

For the Output Characteristics, V_{GS} is stepped from 0 to -5V in -1V increments while V_{DS} is swept from 0 to -5 V in -0.25 V increments. Figure 6-5 shows the Transfer Characteristics for these devices where V_{DS} is stepped from -1 to -5V in -1V increments while V_{GS} is swept forwards and backwards, starting positive, in -0.25 V increments. Extracted device parameters are summarized in Table 6.2. Parameters are extracted via methods and equations discussed in Chapter 3. Transfer Characteristics were completed by sweeping V_{GS} forward and backward starting at positive V_{GS} values. Parameters were extracted on the reverse sweep.

TABLE 6.2: Summary of extracted device parameters for BZN and pBZN based OTFTs. Parameters are extracted at $V_{GS} = -4.5V$V and $V_{DS} = -5$v from the reverse sweep.

PARAMETERS	BZN	pBZN
Ox Thick (nm)	400	400
[20]V_T^{SLCMM} (V)	0.704	-0.71
[21]V_T^{SLR} (V)	3.9	0.18
μ (cm ^{2}/Vs)	0.021	0.0047
S (V/dec)	2.4	0.78
S_{ID} (V/dec)	0.095	0.095
D_{it} (cm^2/eV)	2.21E+13	6.32E+12

[20]SLCMM=Si Long Channel MOSFET Model
[21]SLR=Subthreshold Linear Regression
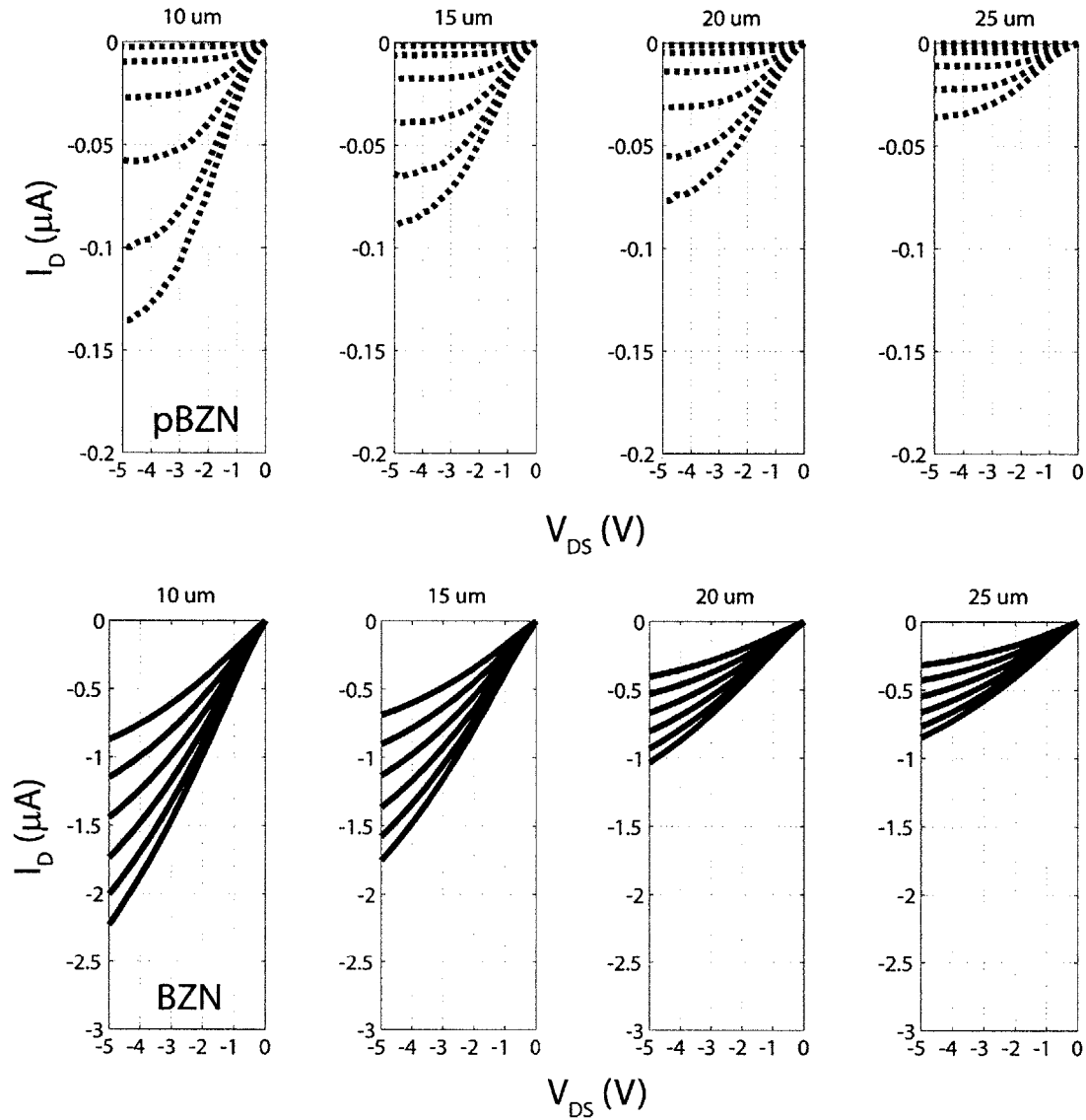
FIGURE 6-4: Output Characteristics for OTFTs with BZN and pBZN insulators at channel lengths (L)=10, 15, 20 and 25 μm, channel width (W)=500 μm. I_D decreases as the channel length increases.

For the BZN based OTFTs, $V_T > 0$ V and for the pBZN based OTFTs and $V_T < 0$ V. The pBZN based OTFTs turn off and saturate within the voltage ranges tested. The BZN devices do not appear to turn off at the most positive V_{GS} values nor saturate at the most negative V_{GS} values tested. The dielectric breaks down before the device completely turns off. The BZN devices show a considerable amount of hysteresis. Hysteresis is a result of mobile charges in the insulator responding to applied electric fields or being trapped either in the semiconductor or the insulator, such that trans-
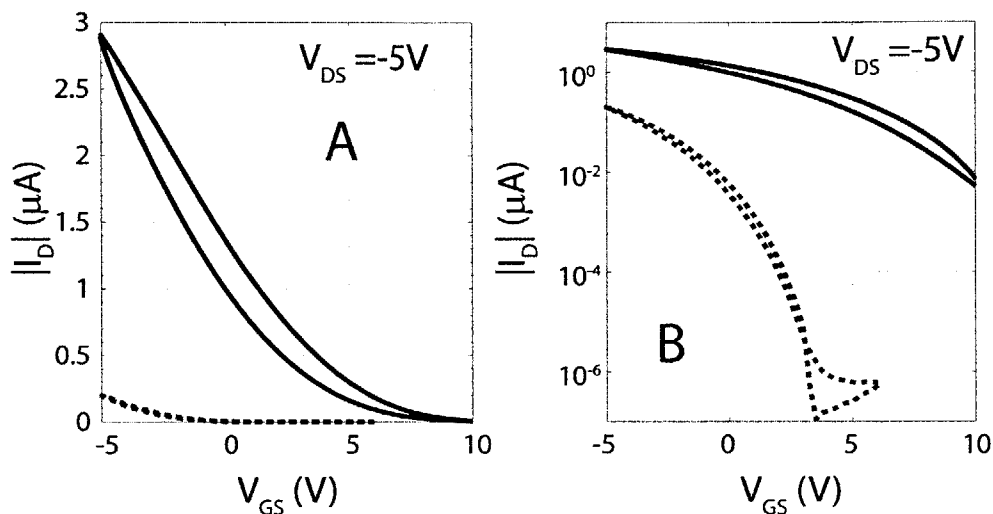
FIGURE 6-5: Transfer Characteristics for BZN (solid line) and pBZN (dashed line) insulators. (A) (linear) I_D vs. V_{GS} (B) (semilog) I_D vs. V_{GS}. The channel length (L) $= 10$ μm and the channel width (W) $= 500$ μm.

port properties (V_T and μ) are affected. This trapping is temporary and depends how the devices are measured. From Figure 6-5, the pBZN based OTFTs have very little hysteresis which compared to the BZN devices. This suggests, the mobile charges causing the hysteresis are on the insulator surface and that the parylene-C surface treatment immobilizes the mobile charges and/or passivates the traps associated with these charges.

Band Diagrams

To construct a equilibrium band diagram for the BZN and pBZN based OTFTs, the states of the channel (accumulated or depleted) must be known at $V_{GS}=0$ V. The Output and Transfer Characteristics from the last section reveal the BZN based OTFTs to be accumulated at $V_{GS}=0$ V while the pBZN based OTFTs are depleted at $V_{GS}=0$ V. For both insulators, there are interface states at the insulators/semiconductor interfaces. This will create a discontinuity in the electric field at this interface. The discontinuity will be determined by the magnitude and sign on the charges at the interface. More specifically, slope of the conduction or valence band in the insulators will not match the slope of the HOMO or LUMO level in the pentacene adjacent to the semiconductor/insulator interface. The Time-Zero Dielectric Breakdown measurements in Chapter 7 revealed the band offset between BZN and Au to be $\sim$1 eV. Last, literature reports the electronic properties (electron affinity, band gap, work function) of Au, BZN, parylene-C and pentacene as discussed in Chapter 2 and are illustrated in Figure 8-7. Knowing the state of the channel, band offsets, and fundamental electronic material properties, band diagrams for BZN and pBZN based

129

OTFTs are qualitatively proposed in Figures 6-7, and 6-8.
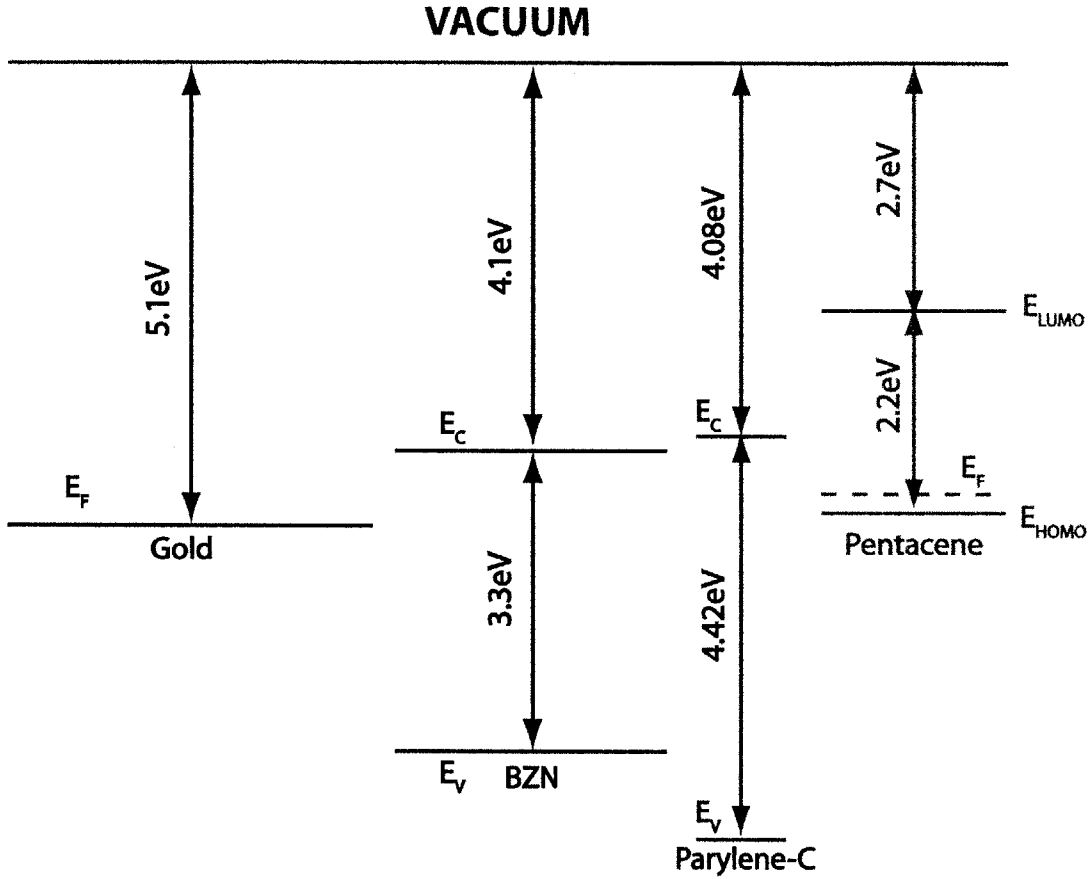
FIGURE 6-6: Energyband levels for the materials used to build devices in this work.

BZN MIS Structure
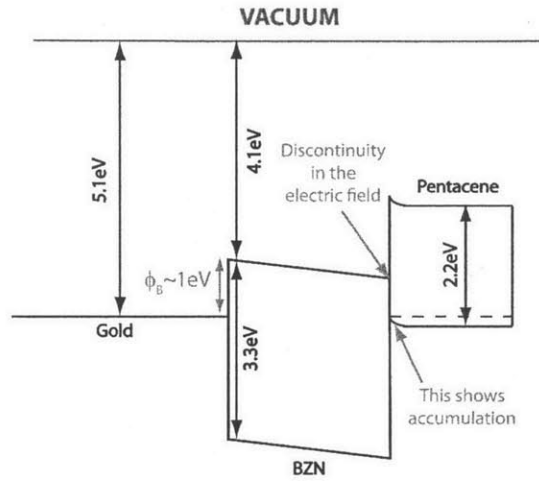
FIGURE 6-7: Band diagram of the BZN MIS capacitor

pBZN MIS Structure
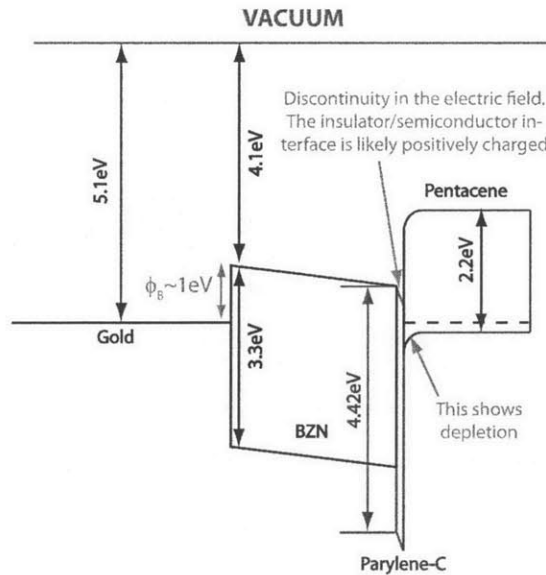
FIGURE 6-8: Band diagram of the pBZN MIS capacitor

131

Effect of Parylene-C Encapsulation

As the encapsulation is only used for patterning the semiconductor, devices were made without encapsulation and patterning for comparison. The cross sections of these device are illustrated in Figure 6-9 and the Output and Transfer Characteristics are shown in Figures 6-10 and 6-11. The parameters are summarized in Table 6.3 and compared to encapsulated and patterned devices.
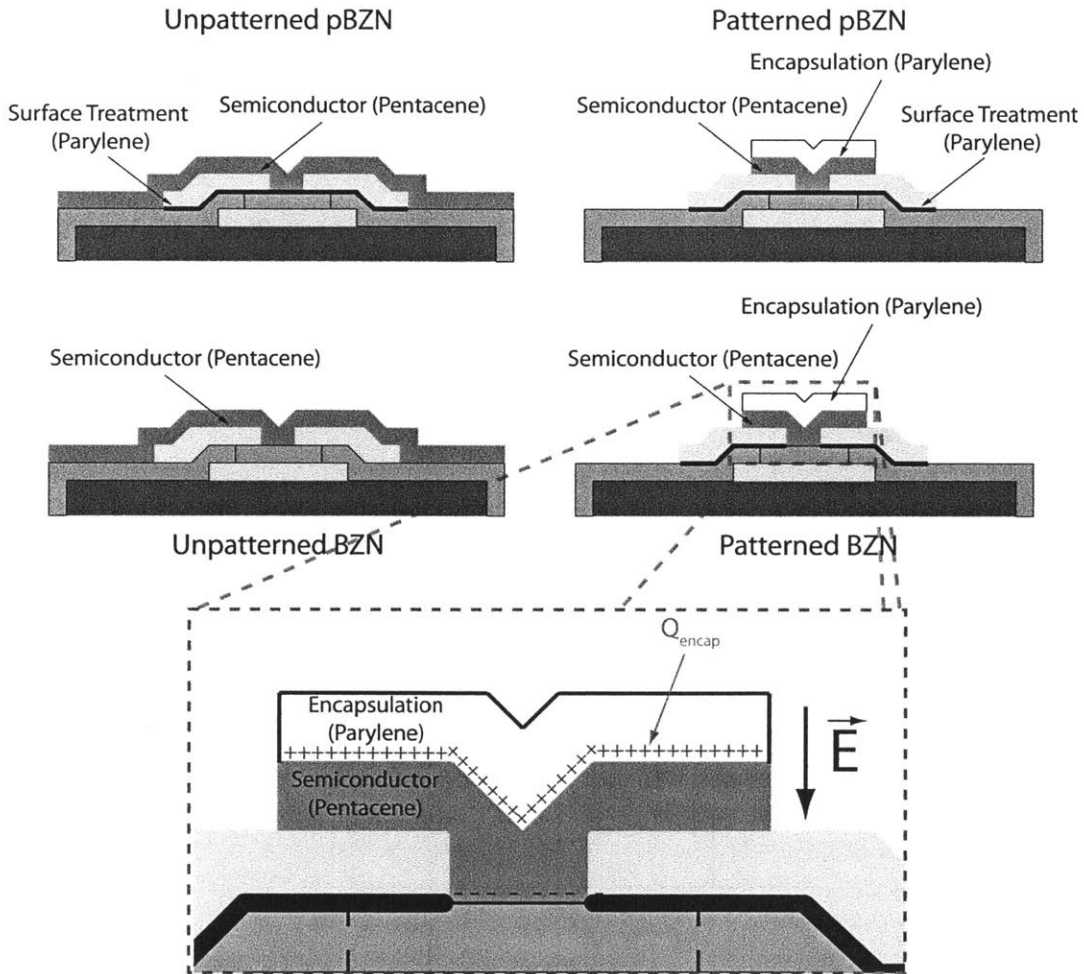
FIGURE 6-9: Cross sections for devices in Figure 6-11
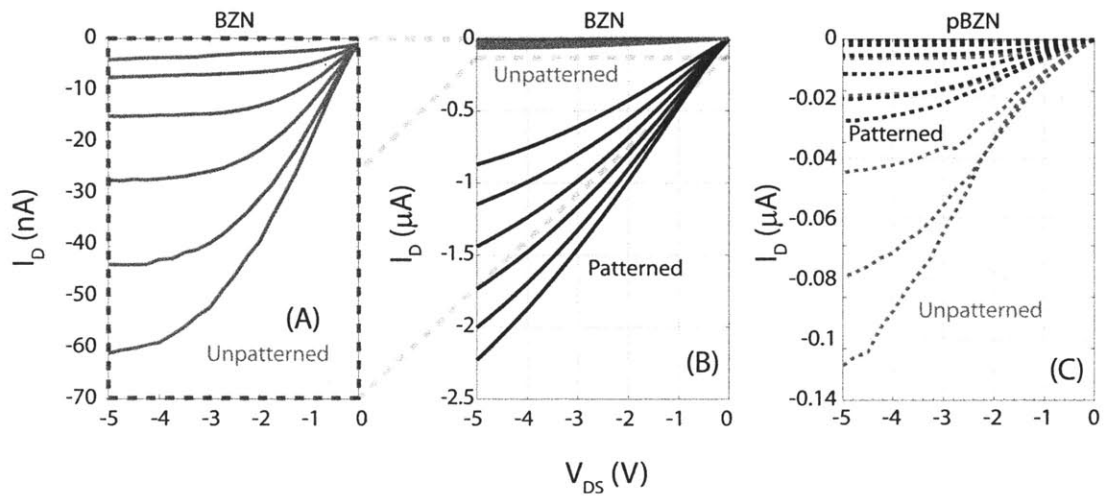
FIGURE 6-10: Output Characteristics of the BZN and pBZN based devices comparing patterned and unpatterned devices (A) Unpatterned BZN (B) Unpatterned and Patterned BZN (C) Unpatterned and Patterned pBZN
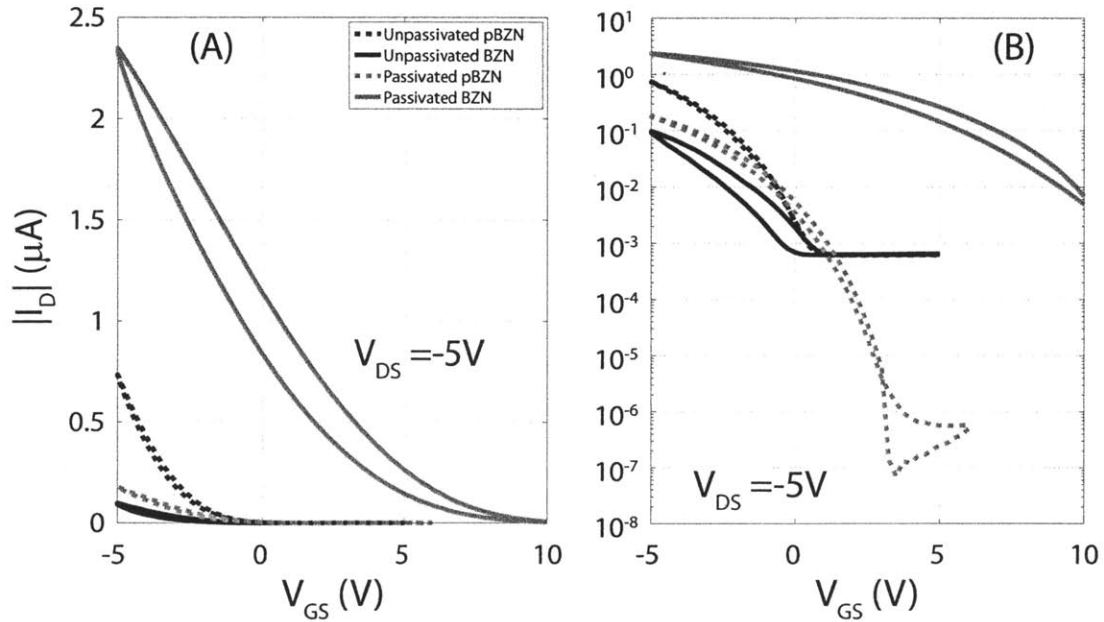
FIGURE 6-11: Transfer Characteristics for BZN (solid line) and pBZN (dashed line) based OTFTs comparing patterned and unpatterned devices (A) (linear) I_D vs. V_{GS} (B) (semilog) I_D vs. V_{GS}

133

TABLE 6.3: Summary of extracted device parameters of patterned and unpatterned devices with a channel length (L)=10 μm and a channel width (W)=500 μm. The parameters are extracted at $V_{GS} = -4.5V$ and $V_{DS} = -5V$

PARAMETERS	BZN	BZN	pBZN	pBZN
Encapsulated?	YES	NO	YES	NO
Ox Thick (nm)	400	400	400	400
[22]V_T^{SLCMM} (V)	0.72	-1.25	-0.67	-1.31
[23]V_T^{SLR} (V)	6.32	-1.9	-0.27	-1.71
μ (cm^2/Vs)	0.022	0.0042	0.0047	0.017
S (V/dec)	2.3	2.55	1.06	1.5

[22]SLCMM=Si Long Channel MOSFET Model
[23]SLR=Subthreshold Linear Regression

6.2.2 Discussion: Figures of Merit and Effects of Integration

There are several approaches to building TFTs with two distinct threshold voltages. A similar technology developed by Nausieda et al., showed that threshold voltage can be controlled selecting gate metals with different work functions (ϕ_M) [5]. Wang et al. showed that V_T can be controlled by charges in the back channel of low temperature lithographically processes ZnO TFT by modulating the semiconductor channel thicknesses [27]. With the technology reported in this dissertation, different transport and device properties are achieved in the BZN and pBZN based OTFTs by surface treatment of the insulator, which effectively modifies the interface states at the insulator/semiconductor interface (Q_{it}), charge trap densities semiconductor bulk (Q_{semi}), and the semiconductor/encapsulation interface ($Q_{encap,it}$), as will be discussed in the next section. As the surface treatment is organic and the bare BZN insulator is inorganic, there are different the electronic interactions with pentacene on an organic surface (pBZN) than pentacene an inorganic surface (BZN). This technology serves as a pragmatic example of how different electronic interactions (organic-inorganic vs. organic-organic) can have a definitive impact on critical OTFT device parameters.

Threshold Voltage

The fabrication and expected device parameters are based on results from Choi et al. [21] and preliminary studies conducted with devices fabricated using shadow masks for the patterning. The parylene-C encapsulation implemented for photolithographic patterning in the last step is necessary for integration. For BZN and parylene-C treated BZN, Choi et al. reported the respective threshold voltages to be 0.1V (BZN) and -2.2 V (pBZN) with 200 nm of BZN and ~2 nm for the parylene-C surface treatment. The devices in this work which are better suited for large scale integration, required 400-425 nm of BZN and 1-3 nm for the parylene-C surface treatment, with a V_T=0.7 V for the BZN devices and V_T=-0.7 V for the pBZN patterned devices.

TABLE 6.4: Comparing the V_T extracted from OTFTs in this work to Choi et al.

Device	Insulator Thickness (nm)	BZN V_T	pBZN V_T	Source of V_T Shift
Choi el al.	200	0.1 V	-2.2 V	Semiconductor/Insulator Interface
Unpatterned	400-425 nm	-1.25 V	-1.31 V	No Shift
Patterned	400-425 nm	0.7 V	-0.7 V	Semiconductor/Insulator Interface and parylene-C encapsulation

For the unpatterned devices, V_T=-1.25 V for BZN and V_T=-1.31 V for pBZN. For the unpatterned devices, the threshold voltage is insensitive to the surface treatment. The devices reported by Choi et al. and the patterned devices in this work have threshold voltages with the same sign; however, the magnitudes are different. This is summarized in Table 6.4.

Based on these differences, it is apparent that the parylene-C encapsulation layer used for patterning, and the thicker insulator leads to a more positive threshold voltage compared to that reported by Choi et al. Therefore, the encapsulation in addition to the different insulator/semiconductor interfaces (pentacene on BZN compared to pentacene on pBZN) give rise to the different threshold voltages in the technology reported in this chapter. Whereas Choi et al. demonstrated two distinct threshold voltages based solely on a single insulator/semiconductor interface.

EFFECT OF PARYLENE-C ENCAPSULATION ON THRESHOLD VOLTAGE
The OTFTs reported in this chapter and similar devices reported in literature show that the encapsulation will change V_T. Others have reported a V_T shift based on exposing the back channel to different enviro nments and processing. Specifically, Jia et al. reported a ~10 V shift in threshold voltage when poly (3-hexylthiophene) (P3HT) based organic thin film transistors are encapsulated in parylene and Al_2O_3 [15]. Kymissis et al. reported a threshold voltage shift from -3.0 V to +2.5 V upon encapsulation and patterning [26]. In both cases, the shift is attributed to unintentional doping. Further, Wang et al. reports that unintentional doping can shift V_T [28]. Moreover, a shift in threshold voltage as a result of the deposition or adsorption of a material or chemical on the exposed semiconductor back channel is the operating principle behind OTFT based chemical sensors of which there are many reports [29, 30, 31, 32, 33, 34].

For these devices, a shift in V_T is seen most prominently in the BZN devices. From Figure 6-11, the parylene-C encapsulation pushes the V_T for the BZN devices so positive that the devices do not turn off before breaking down. Accounting for the additional bulk charges and interface charges created by the encapsulation process, the expression for threshold voltage is modified as shown in Equation 6.1. This expression is derived in Appendix A. Figures 6-9 and 6-12, qualitatively illustrate

the existence and location of the additional charges in the BZN MIS structure due to encapsulation.
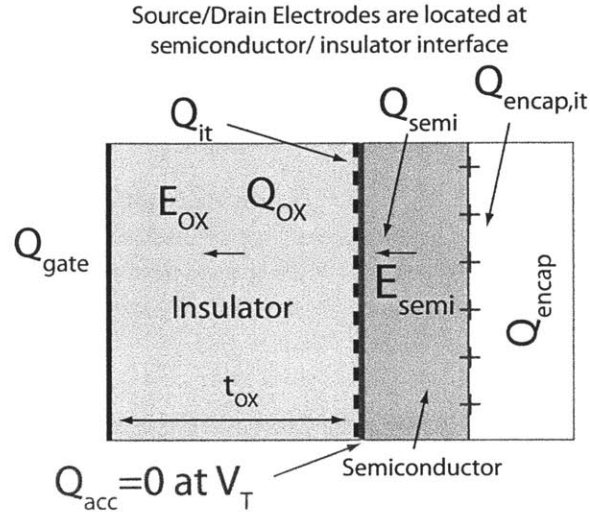
FIGURE 6-12: Location and identification of charges in the MIS capacitor.

$$V_T = (\phi_m - \phi_S) - \left(\frac{Q_{OX} + Q_{it} + Q_{semi} + Q_{encap,it} + Q_{encap}}{\kappa \epsilon_o} \right) t_{ox} \qquad (6.1)$$

Where,

ϕ_M and ϕ_S: work functions of the gate metal and the semiconductor

ϵ_o: permittivity of free space

κ: dielectric constant of the insulator

Q_{it}: surface charge density at the interface between insulator and the semiconductor.

Q_{OX}: charge density per unit volume in the insulator integrated over the thickness of the insulator. See the Note below.

Q_{semi}: charge density per unit volume in the semiconductors integrated over the thickness of the insulator. See the Note below.

$Q_{encap,it}$: surface charge density at the interface between semiconductor and the encapsulation.

Q_{encap}: charge density per unit volume in the encapsulation integrated over the thickness of the encapsulation. See the Note below.

t_{OX}: thickness of the insulator

****NOTE: Q_{OX}, Q_{semi}, and Q_{encap} are not sheet charges. They are the results to integrating charge volume density (ρ) over the thickness (t) of each respective region. By considering locations at interfaces, Q_{OX}, Q_{semi}, and Q_{encap} can be treated as sheet charges mathematically as indicated. See Appendix A for more detail.*

Mobility

The extracted mobility of the BZN and pBZN OTFTs reported in this work is comparable to values reported by other researchers with devices using a high-κ insulators. These values range from $10^{-1} - 10^{-2} cm^2/Vs$ [35]. The mobility for this technology is sensitive to the patterning process; specifically both the temperature generated from the bakeout step and O_2 plasma etch and from the parylene-C encapsulation.

BAKING AND O_2 PLASMA ETCH FOR SEMICONDUCTOR PATTERNING

Figure 6-13 shows that the heat generated from the bakeout during photolithography is detrimental to device performance, specifically lowering mobility. This decrease in mobility is attributed to the increase in the amount of bulk phase in pentacene. There are other reports indicating that the heat treatment of pentacene degrades mobility. It has been suggested that a shorter bake time at a higher temperature or a longer time at a lower temperature may minimize this degradation [36, 37, 38]. Using a photoresist that does not require a bake may minimize this degradation, however the heat generated in the O_2 plasma etch process is unavoidable. Last, though not investigated in this work, the O_2 plasma etch itself may detrimental to device performance [39].
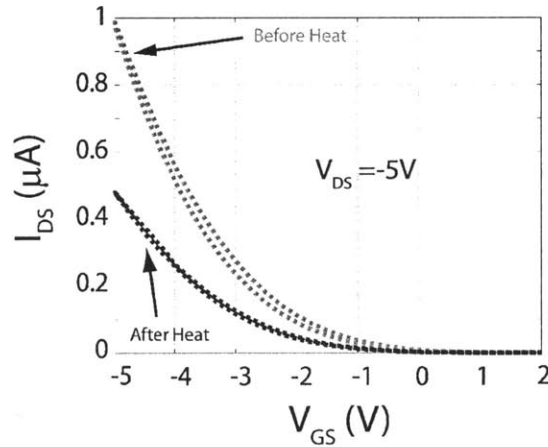
FIGURE 6-13: Mobility degrades as a result of the heating during photolithography for pBZN surface. Channel Length (L)=5μm Channel Width (W)=500μm

EFFECT OF PARYLENE-C ENCAPSULATION ON MOBILITY

Figure 6-11 shows that before encapsulation and patterning the pBZN based OTFTs have a higher mobility than the BZN based OTFTs, which agrees with literature [40]. Comparing these to devices that have been encapsulated and patterned, the mobility of the BZN based OTFTs increase by an order of magnitude while the mobility of the pBZN based OTFTs decreases as predicted with the processing demands (heat from bakeout and etching) of this step. Again, Jia et al. [15] and Kymissis et al. [26] attribute the threshold voltage shift to unintentional doping of the semiconductor;

however they did not report dramatic changes in mobility. As discussed in Chapter 2, pentacene grain structure effects mobility, and the encapsulation may be altering the occupancy of charge traps at the grain boundaries (Q_{semi}). Wang et al. report that traps in grain boundaries degrade charge transport. [41] while Yogev et al. reports that the effect of traps in grain boundaries on charge transport is not clear [42]. Further, investigations should be conducted to determine if charge traps in the grain boundaries are contributing to the change in mobility in devices.

Subthreshold Swing (S)
Quasi-static Capacitance-Voltage measurements suggest that the channel of the BZN based OTFTs do not deplete despite the fact that the OTFT is not "on". This is shown in Figure 6-14. As expected, the extracted subthreshold swing for the BZN based OTFTs is larger than the pBZN based OTFTs suggesting more interface states and charge trapping. Note that the patterned BZN devices cannot be turned off completely, therefore the extraction of S is limited and may not be completely indicative of the actual subthreshold slope. However it is still likely that S for BZN is larger than S for pBZN as is the case for the unpatterned devices.
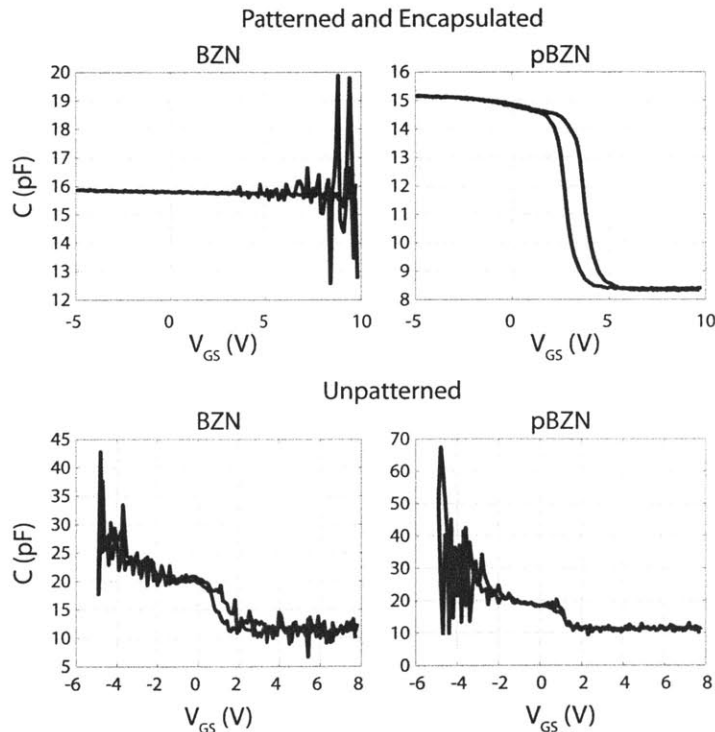
FIGURE 6-14: Quasi-static Capacitance-Voltage measurements for patterned and unpatterned BZN and pBZN based OTFTs. The channel length (L)=15μm and channel width (W)=500μm

<u>EFFECT OF PARYLENE-C ENCAPSULATION ON SUBSTHRESHOLD SWING</u>
Though it is not clear how the encapsulation is changing charge transport in the devices, the larger hysteresis in the patterned BZN based OTFTs and the change in V_T with encapsulation indicates more charge traps in the semiconductor or at the semiconductor/insulator interface. Such a hysteresis has been seen with similar pentacene-based OTFT systems featuring organic surface treatments on high-κ dielectrics [43] and is linked to trapping at the semiconductor/insulator interface. As a result, S should increase as a result of the encapsulation as a larger V_{GS} is needed to release the trapped charges and deplete the channel. For the unpatterned devices, S appears to be larger compared to the patterned devices. This is likely due to the lack of semiconductor patterning. In Figure 6-14, the CV curves are the same for both the unpatterned BZN and pBZN based OTFTs despite clear differences in transport behavior shown in Figure 6-11. As there is current leakage path from the source and drain electrodes to the gate electrode, this calls into question the validity of the quasi-static CV measurement from these unpatterned devices. Further investigations should be performed to evaluate if and how the encapsulation affects the subthreshold swing.

Summary of Effects of Encapsulation

In reference to Equation 6.1, Q_{it}, Q_{semi}, $Q_{encap,it}$, and Q_{encap} give rise to the difference in V_T between OTFTs based on the BZN and pBZN. These charge densities can be related to the grain structure of pentacene on BZN compared to pBZN as shown in Figure 6-15 and which is mediated by the difference in the chemical nature of the insulator surface (organic vs. inorganic) and its interaction with pentacene (organic/organic vs. inorganic/organic).

Pentacene BZN AFTER Heat   Pentacene on pBZN AFTER Heat
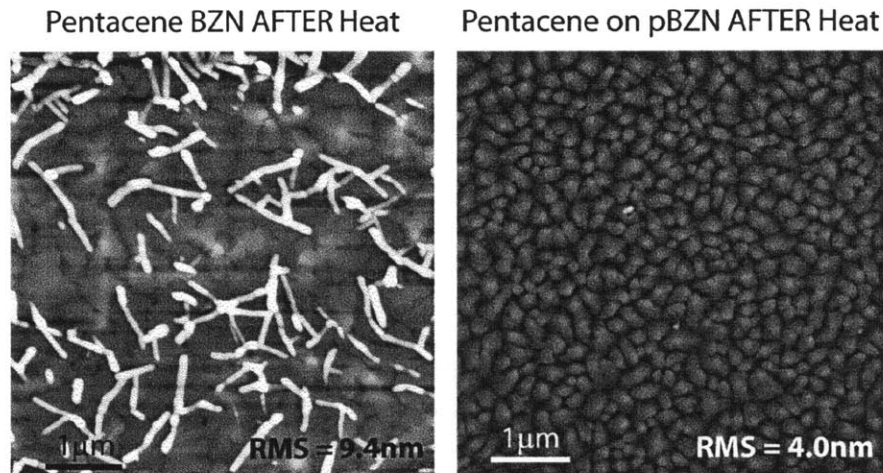
FIGURE 6-15: AFM images for Pentacene on BZN (rms roughness 9.4 nm) and pBZN (rms roughness 4.0 nm). Pentacene on BZN has a larger roughness (rms) due to the elevated, elongated needlelike structures resting on the larger grains on pentacene. The different grain structure of pentacene on the two different surfaces suggest a different Q_{semi} for each.

139

- Q_{it}: It is clear from surface energy and subthreshold slope extraction from both patterned and unpatterned devices that Q_{it} is different for these two insulators. Extracted D_{it} values from Table 6.2 suggest that there is a least four times as many interface states in the BZN based devices compared to the pBZN.

- Q_{semi}: Pentacene on BZN and pentacene on pBZN have different grain structures. AFMs (Figure 6-15 reveal that pentacene grown on BZN to be more ramified and show poor grain connectivity compared to pBZN. As grain boundaries can trap charge [42], Q_{semi}, cannot be expected to be the same for pentacene on BZN and pBZN. Further, this may relate to or confirm the unintentional doping reported by Kymissis et al. and [26] and Jia et al. [15].

- $Q_{encap,it}$: With the different grain structures and likely growth modes (2D for pentacene on BZN and 3D for pentacene on pBZN), the roughness of the back channel is different for pentacene on BZN compared to pentacene on pBZN as indicated in Figure 6-15. Therefore, the area of the semiconductors/encapsulation interface will most likely be different for pentacene on BZN compared to pentacene on pBZN. This implies that $Q_{encap,it}$ is different for pentacene on BZN compared to pBZN.

- Q_{encap}: The surface kinetics for thin film growth may or may not impact how parylene-C grows on different grain structures of pentacene. Beyond this, little evidence suggests that Q_{encap} is different for BZN and pBZN based OTFTs.

Reliability of BZN-Based Devices

Despite the relativley large value of 400-425 nm of BZN for the insulator thickness (t_{ox}), it was observed that both the BZN and the pBZN based OTFTs were susceptible to dielectric breakdown at low voltages. This is shown in Figure 6-16 (A).

This breakdown is evident as the gate current (I_G) equals the drain current (I_D) shown in Figure 6-16 (A). When $V_{GS} > 0$, this pBZN based OTFT is off. The sustained drain current indicates a short in the gate insulator. The frequency of failures was not large enough to render this device technology unsuitable for integrated circuitry which is discussed in the next section.

Next, the threshold voltage for the BZN based devices is unstable due to trap generation when a bias is applied between the gate and the source. Figure 6-16 (B) shows how the V_T shift can occur without intentionally stressing. In this case, the shift in the threshold voltage of the BZN devices depends on the range of gate voltage applied during the sweep. Starting the sweep at a more positive gate voltage, shifts the threshold voltage positive by ~4V using the Subthreshold Linear Regression method to extracting threshold voltage. Figure 6-16 (B) clearly shows that the V_T of the BZN devices shifts quite substantially however the pBZN device show little to no shift.

140
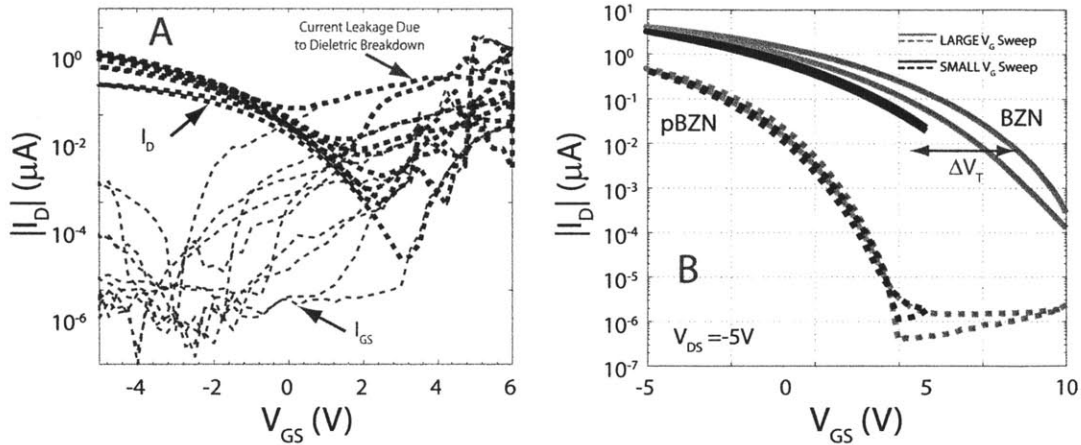
FIGURE 6-16: The reliability of BZN and pBZN based OTFTs. (A) The gate insulator breaks down creating a short from the gate to the drain electrode. (B) V_T shift depends on range of V_{GS} swept. The shift is due to substantial charge trap generation in the insulator as a part of the break down process.

Results from Time-Zero Dielectric Breakdown (TZDB) and Time-Dependent Dielectric Breakdown (TDDB) studies show significant trap generation at device operating voltages (-5 V to 10 V (V_{DS}) and -5 V to 0 V (V_{GS})) and breakdown at low (<15V) voltages. These results will be discussed in Chapter 7. Despite these reliability issues, these devices can still be successfully integrated into circuits.

6.3 INTEGRATED CIRCUITS

A depletion-load inverter and an 11-stage ring oscillator are used to illustrate the efficacy of building integrated circuits with this high-κ, dual V_T OTFT technology. These circuits require two or more fully operating OTFTs. This is the first report of a fully integrated circuits based on OTFTs with a high-κ gate insulator and two distinct threshold voltages in one technology.

6.3.1 Logic Inverters

Principles of Operation

The most basic building block for all digital circuits is the inverter, which inverts voltage level at the output relative to the input. More specifically, the logical function of the inverter is to have a high voltage state at the output (V_{OUT}) when the voltage at the input is (V_{IN}) is low or have a low voltage state at V_{OUT} when V_{IN} is high. As pentacene currently cannot be doped with long term stability, CMOS logic (inverter based on one p-type FET and another n-type FET) with pentacene is currently impossible. Integrating an enhancement mode (driver) TFTs (V_T <0

141
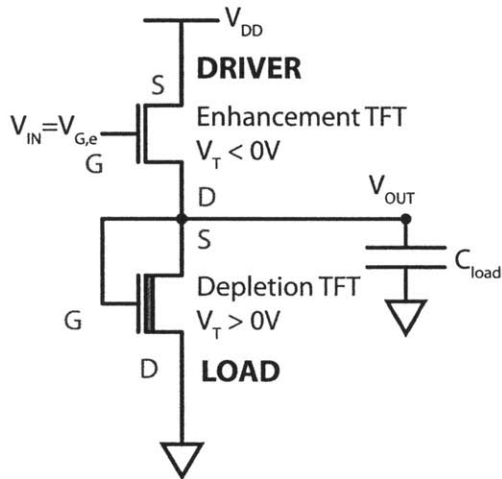
FIGURE 6-17: Circuit diagram of depletion-load inverters
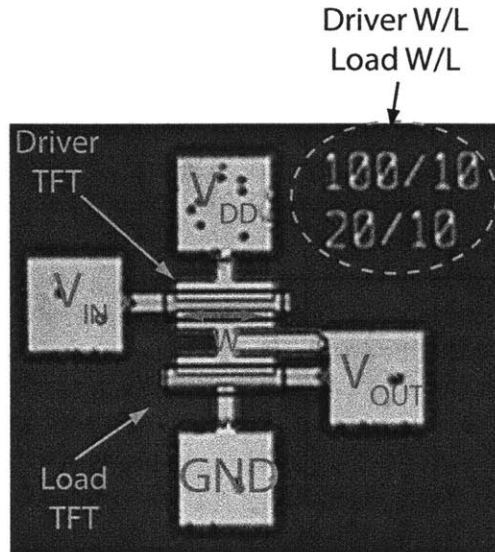
FIGURE 6-18: Top view of E/D inverters

V) and a depletion mode (load) TFTs ($V_T > 0$ V) wired as shown in Figure 6-17 and Figure 6-18 is commonly used to build E/D (enhancement/depletion) logic gates when CMOS is not possible. This approach preceded CMOS as the first set of microprocessors were built with E/D technology. From Figure 6-17, C_{LOAD} represents the capacitance at V_{OUT} imposed by instrumentation (Agilent 4156C Semiconductor Parameter Analyzer) or subsequent logic gates and associated wiring. For the BZN and pBZN technology, the pBZN based OTFT is the driver and BZN based OTFT is the load, hence depletion-load.

Low to High

The voltage at V_{IN} is connected to the gate of the driver OTFT and V_{OUT} is connected to the gate and source of the load OTFT as shown in Figure 6-17. The voltage at V_{OUT}, is set by the charge delivered to the C_{LOAD} (Q=CV), through the current supplied by the driver (enhancement TFT). For the driver, $V_{GS}=V_{IN}-V_{DD}$. Therefore, when $V_{IN}=0$, $V_{GS}=-V_{DD}$. If this is beyond threshold, the driver is "on" and a current is delivered to ground where C_{LOAD} is charged in parallel. The voltage on C_{LOAD} or V_{OUT} equals the voltage dropped (V_{DS}) across the load (in depletion) TFT where $V_{GS}=0$. As $V_T > 0$, this device is always conducting. Ideally, when $V_{IN}=0$V the load has a larger resistance than the driver, such that the voltage dropped is large (V=IR) or V_{OUT} is high. This is illustrated at point I in Figure 6-20.

142
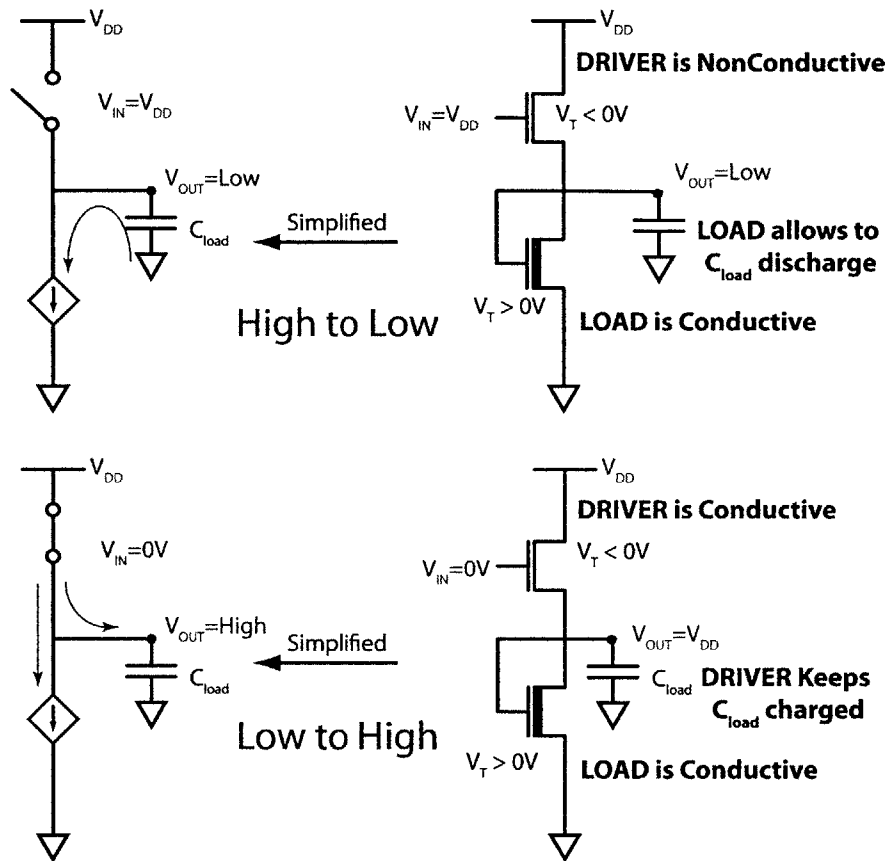
FIGURE 6-19: Summary of voltage states of the logic inverter circuit

High to Low

When $V_{IN}=V_{DD}$, $V_{GS}=0V$ for the driver. As $V_T <0$, the driver OTFT will turn "off". With the driver OTFT "off", and the load OTFT "on", C_{LOAD} discharges, and $V_{OUT}=0V$. This is illustrated at point V in Figure 6-20. The different voltage conditions are summarized in Figure 6-19 and typical voltage transfer characteristics are shown in Figure 6-20. The trip point (point III in Figure 6-20) for the circuit is when $V_{IN}=V_{OUT}$.

Expressions for relevant logic inverter parameters can be found in Equations 6.2 through 6.5 [44] and are illustrated in Figure 6-20. The parameter $k_{load,driver}$, essentially represents the conductivity of the load OTFT or driver OTFT. Gain (A_v) is a measure of how effectively the inverter to changes the signal from the input to the output. It is desirable to maximize this parameter at the voltage trip point and minimize it at the stable output voltages i.e. V_H and V_L. The noise margin low (NM_L) is the amount by which V_{IN} can be above is lowest voltage (V_L) and still be interpreted as a low condition. Accordingly, the noise margin high NM_H is the amount by which

V_{IN} can be below the maximum voltage (V_{MAX}) and still be interpreted as a high condition. It is desirable to maximize both noise margins. Ideally, the voltage at which the circuit inverts is the V_M and is located at the midpoint between high voltage condition and low voltage condition ($V_{IN} = V_{DD}/2$ and $V_{OUT} = V_{DD}/2$). With a wide load OTFT, C_{LOAD} will charge slow as more current will flow to ground as opposed to supplying charge to C_{LOAD}. This will lower the gain, which is undesirable. However, with $V_{GS}=0$ for the depletion-load, increasing the width will reduce the low voltage condition at V_{OUT} making it closer to ground. This will increase noise margins, which is desirable. With such design tradeoffs, it is most optimal to change the width of the driver (k_{driver}) as opposed to the width of the load (k_{load}) to optimize circuit performance. For more details regarding digital circuits, refer to Howe and Sodini [44].

Voltage Transfer Characteristic

Graphical Representation of Logic States in Voltage Inverter
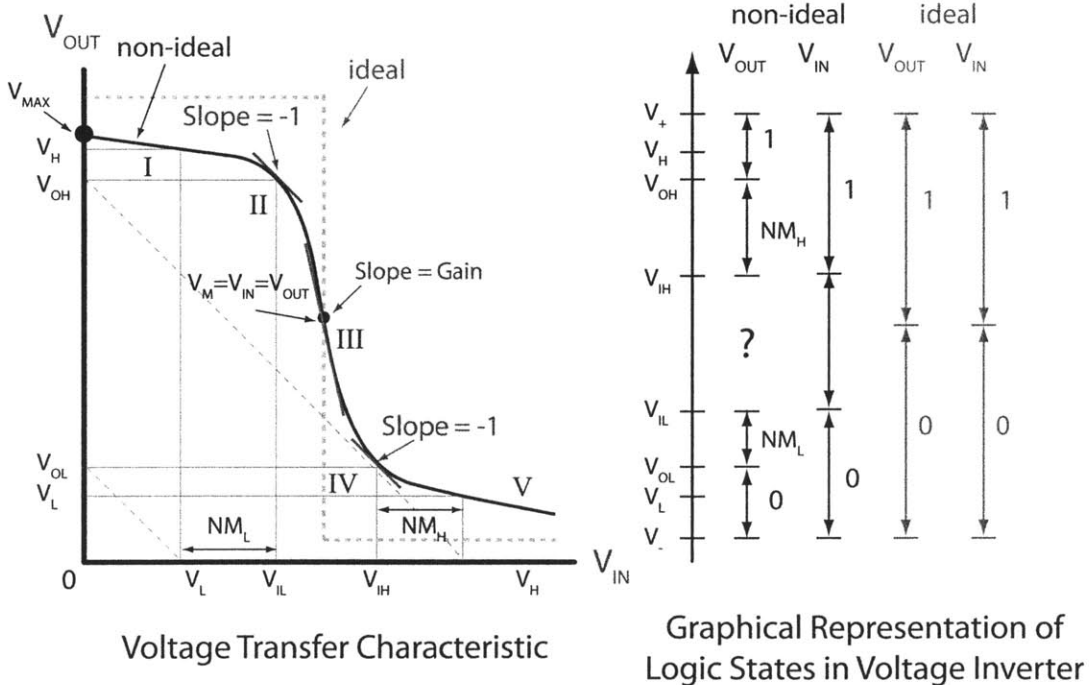
FIGURE 6-20: Defining performance parameters for logic inverter [45].

$$k_{\substack{load,\\driver}} = \frac{W}{L}_{\substack{load,\\driver}} \mu_{\substack{load,\\driver}} C_{ox,\substack{load,\\driver}} \tag{6.2}$$

$$V_M = \frac{V_{T,load} + \sqrt{\dfrac{k_{driver}}{k_{load}}}(V_{DD} + V_{T,driver})}{\sqrt{\dfrac{k_{driver}}{k_{load}}}} \tag{6.3}$$

$$NM_L = V_{IL} - V_{OL} \tag{6.4}$$

$$NM_H = V_{OH} - V_{IH} \tag{6.5}$$

$$gain = -(g_{m,load} + g_{m,driver})\left(\frac{1}{r_{o,load}} + \frac{1}{r_{o,driver}}\right)^{-1} \tag{6.6}$$

Where,

$$g_{m,\substack{load,\\driver}} = \frac{\partial I_D}{\partial V_{GS}} \tag{6.7}$$

$$r_{o,\substack{load,\\driver}} = \frac{\partial V_{DS}}{\partial I_{D,sat,\substack{load,\\driver}}} \tag{6.8}$$

Where,

V_{IL}: maximum input voltage for low input logic state where V_{OH} is the matching output voltage

V_{IH}: minimum input voltage for high input logic state where V_{OL} is the matching output voltage

A_v(gain): the efficiency that the inverter to changes the signal from the input to the output

V_{MAX}: V_{OUT} at V_{IN}=0V

V_L: V_{OUT} at $V_{IN} \geq V_{DD}$

V_M: location on the voltage transfer characteristics where $V_{IN} = V_{OUT}$, or trip point

V_{DD}: supply voltage

NM_L: the amount by which V_{IN} can be above V_L and still be interpreted as a low condition

NM_H: the amount by which V_{IN} can be below V_{MAX} and still be interpreted as a high condition

Figure 6-21 illustrates a graphical method of choosing size for the load OTFT and driver OTFT. Mapping the load line (where V_{GS}=0 V for the load OTFT) onto the output characteristics of the driver OTFT and noting where they intersect reveals the value of V_{OUT} at a given V_{IN} or the inverter voltage transfer characteristic. By selecting the width (W) and length (L) of the driver (k_{driver}) and load (k_{load}) , V_M, noise margins, and gain of the inverter can be optimized. It should be noted that the depletion-load gives a lower low voltage condition, compared to a resistive load,
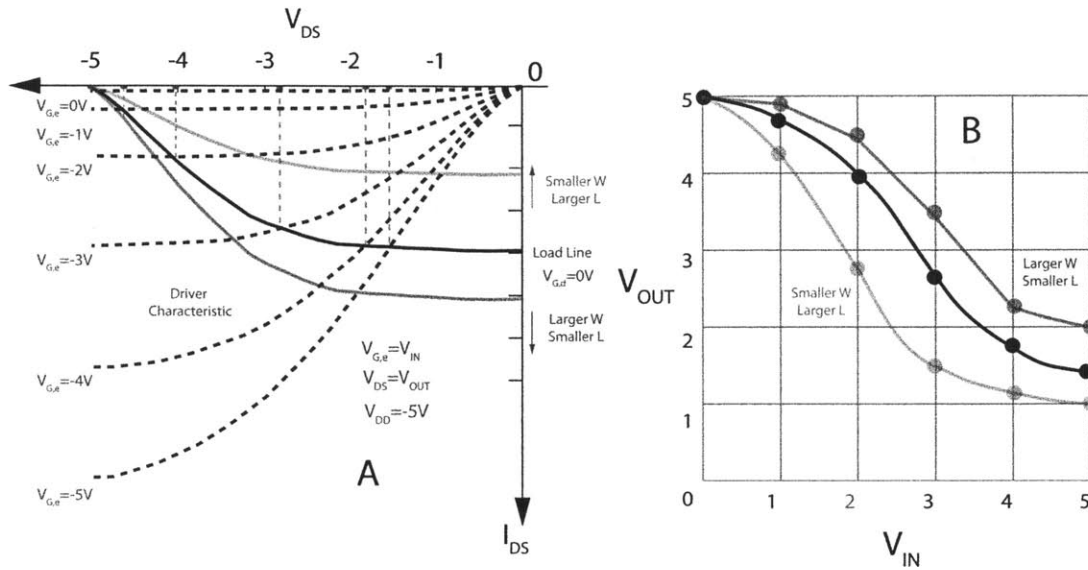
FIGURE 6-21: Determining driver and load sizes (W/L) (A) Output Characteristic for enhancement-mode OTFT and load line for a depletion-mode OTFT and (B) Voltage transfer characteristics for a depletion-load inverter

therefore larger noise margins.

Electrical Characterization

Actual voltage transfer characteristics for logic inverters fabricated from OTFT with the BZN and pBZN insulators are shown in Figures 6-22 and 6-23. As discussed in the last section, the BZN devices do not saturate within the operable voltage ranges tested and have relatively large mobility due to the encapsulation. As these counterintuitive device properties are not completely understood, W and L were selected from conventional values (W=100 μm) with the addition of circuits with larger driver widths (1000 μm) to assess the counterintuitive carrier transport in the BZN devices. Therefore, the sizes of the driver and load OTFTs for these inverters are not optimized, though the logic inverter still inverts voltage.

Observing the difference in performance between Figure 6-22 and Figure 6-23, it can be appreciated how having a precise and reproducible patterning method available (photolithography) can improve performance. By simply using a wider driver, (1000 μm in Figure 6-23 opposed to 100 μm in Figure 6-22) we obtain better gain and larger noise margins at a lower supply voltage. Fundamentally, the wider driver is able to charge C_{LOAD} faster than the load will allow C_{LOAD} to discharge.

Beyond the V_{DD} reported in Figures 6-22 and 6-23, there was not good agreement

146

V_{DD}	6		8	
V_{MAX}	4.1		5.9	
	Pred.[44]	Exp.	Pred.[44]	Exp.
Gain MAX	1.8	1.2	1.8	1.8
Gain V_M	1.8	1.1	1.8	1.8
NM_L	1.2	1.0	1.7	0.7
NM_H	0.7	-0.9	-1.0	0.3
V_M	2.2	2.6	3.2	3.2
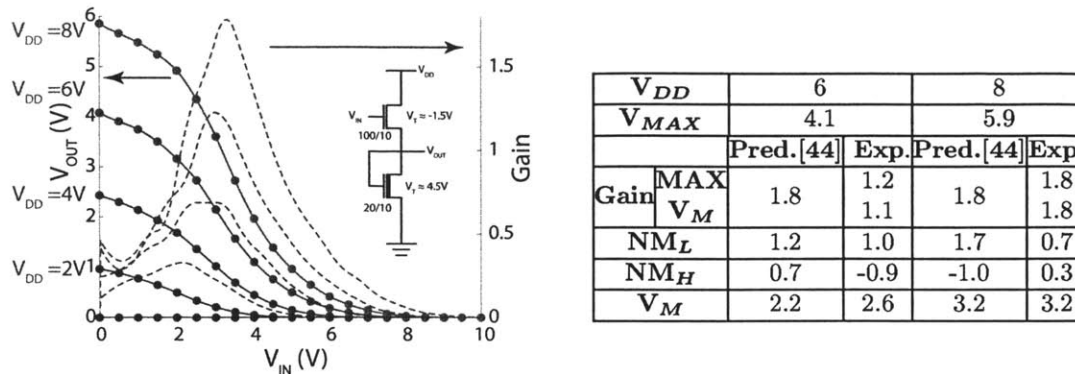
FIGURE 6-22: Transfer Characteristic for depletion-load inverter for E/D logic. The driver is sized 100 μm wide with a 10 μm channel length. The load is sized 20 μm wide with and 10 μm channel.

V_{DD}	4		6	
V_{MAX}	3.8		5.8	
	Pred.[44]	Exp.	Pred.[44]	Exp.
Gain MAX	1.2	2.1	1.4	3.2
Gain V_M	1.2	1.2	1.4	3.2
NMv_L	1.7	2.02	3.0	2.5
NM_H	-1.0	-1.2	-1.4	-0.3
V_M	2.6	2.8	4.2	3.7
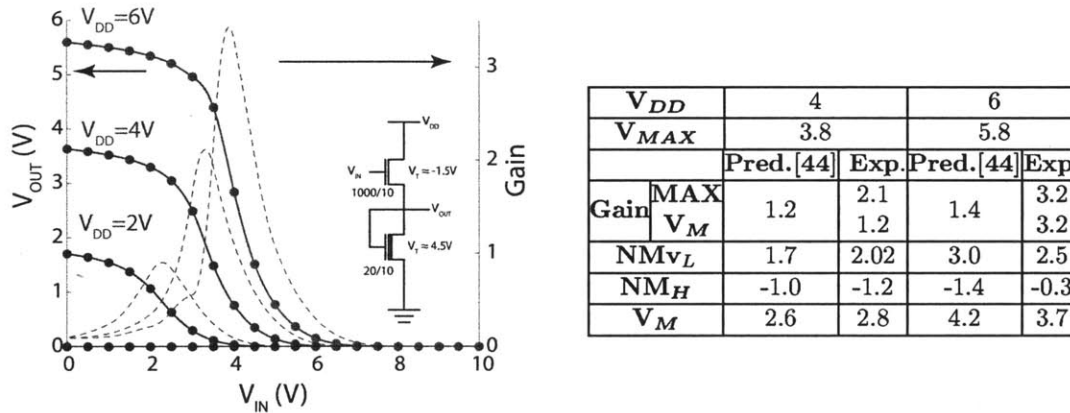
FIGURE 6-23: Transfer Characteristic for depletion-load inverter for E/D logic. The driver is sized 1000 μm wide with a 10 μm channel length. The load is sized 20 μm wide with and 10 μm channel.

with predicted values. This is believed to be a result of the shift in V_T caused by trap generation in the dielectric, specifically in the BZN devices discussed in the previous section. At a larger V_{DD}, the threshold voltage shifts positive in the BZN based OTFTs, the load is more conductive. As a result, V_{OH} will be lower when V_{IN} is at its low voltage state than if V_T had not shifted. Redesigning the circuit to operate at a lower voltage ($V_{DD} \leq 5V$) by using a larger driver width will fix this issue. Further the negative noise margins (NM_H) reported at the supply voltage (V_{DD}) suggests that such operating conditions are not ideal for more complex circuits containing more logic gates. A larger V_{DD} must be used to obtain positive noise margins which creates more unpredictability in OTFT performance due to the shifting V_T.

A key innovation and advantage with this technology is that two distinct threshold voltages can be integrated on the same wafer. Cantatore et al. report that using a

147

negative threshold voltage for the driver (pBZN in this dissertation) will improve both symmetry and noise margins [7]. Figure 6-24 compares the transfer characteristics of an inverter consisting of two TFTs with the same threshold voltage (Enhancement/Enhancement (E/E) Inverter) to an inverter consisting of two OTFTs with two different threshold voltages threshold voltages (Enhancement/Depletion (E/D) Inverter). Using two distinct threshold voltages results in better noise margins, a more symmetric V_M [7], a smaller V_L without sacrificing gain in agreement with Cantatore et al. These parameters are summarized in Table 6.5.
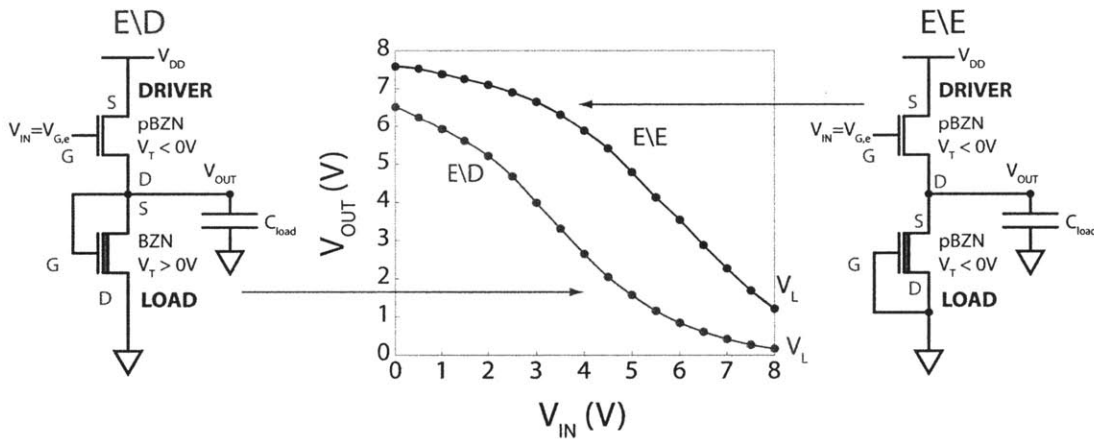
FIGURE 6-24: Transfer Characteristics comparing an Enhancement/Enhancement (E/E) Inverter to a Enhancement/Depletion (E/D) Inverter with V_{DD}=10 V. For both circuits, the channel width of the driver is 100 μm and the width of the load is 5 μm. For all TFTs the channel length is 10 μm. The E/D inverter shows better noise margins, a lower V_M, a smaller V_L without sacrificing gain. This is summarized in Table 6.5.

TABLE 6.5: Comparing parameters of an E/E inverter to an E/D inverter of equal size. The V_{DD} = 10 V and channel length = 10 μm

Inverter	E/D	E/E
Driver Width (μm)	100	100
Load Width (μm)	5	5
V_M (V)	3.4	4.9
Gain	1.4	1.4
NM_L (V)	0.2	2.9
NM_H (V)	0.5	-2.2
V_L (V)	0.2	1.2

148

6.3.2 Ring Oscillator

Principles of Operation

A ring oscillator is a simple circuit consisting of an odd number of inverters in a chain where the input (B) of one inverter (V_{IN}) is connected to the output (A) (V_{OUT}) of the inverter preceding it as shown in Figure 6-25. The output of the last inverter (D) in the chain is fed back (E) to the input of the first inverter (C) forming ring. The ring oscillator provides a simple way of examining the speed and energy consumption of this low voltage OTFT technology.

As was mentioned in the previous section, a voltage at V_{OUT}, is set by the charge delivered to C_{LOAD}. The charging of this capacitor is not instantaneous which causes a signal delay at each stage of inverters in the ring. Therefore, a low V_{IN} at the beginning of the chain will not register a high V_{OUT} at the end of the chain immediately. Exploiting this delay, connecting V_{IN} at beginning of the chain to V_{OUT} at the end of the chain will create an oscillation in the signal at V_{OUT}, where the frequency of the oscillation is determined by the delay of each stage as can be shown with Equation 6.14. The delay of each stage (t_P) is related to $k_{load,driver}$ and C_{ox} and is in equations Equations 6.10, 6.11, and 6.12.

$$C_{LOAD} = C_G + C_P + C_{wire} \tag{6.9}$$

$$t_{PHL} = \frac{(C_G + C_P)\dfrac{V_{OH}}{2}}{\dfrac{k_{load}}{2}(V_{DD} - V_{T,load})^2} \tag{6.10}$$

$$t_{PLH} = \frac{(C_G + C_P)\dfrac{V_{OH}}{2}}{\dfrac{k_{driver}}{2}(V_{DD} - V_{T,driver})^2} \tag{6.11}$$

$$t_P = \frac{t_{PHL} + t_{PLH}}{2} \tag{6.12}$$

$$\text{Period} = 2 \times \text{Number of stages} \times t_P \tag{6.13}$$

$$f_{osc} = \frac{1}{\text{Period}} = \frac{1}{(2 \times \text{Number of stages} \times t_P)} \tag{6.14}$$

$$P_{Diss.} = (C_G + C_P)V_{DD}^2 f_{osc} \tag{6.15}$$

Where,

C_{LOAD}: capacitance at the output node of the inverter

C_G: capacitance of gate insulator (C_{ox}) excluding overlap capacitance C_P

C_P: the source/drain electrode gate electrode overlap capacitance

C_{wire}: capacitance of interconnects

t_{PHL}: time it takes for V_{OUT} to discharge from V_{MAX} to $V_{MAX}/2$

t_{PLH} time it takes for V_{OUT} to charge from $V_{MAX}/2$ to V_{MAX}

f_{osc}: frequency of oscillation a ring oscillator

$P_{Diss.}$: Power dissipation of the ring oscillator

Electrical Characterization

The ring oscillators fabricated consists of 11 inverters with an integrated buffer, totaling 26 OTFTs. The output for this ring oscillator is shown in Figure 6-26. As the delay time for the ring oscillator is inherently dependent on the transient behavior of the logic inverters and the OTFTs it consists of, a fully functional ring oscillator would match the oscillation frequency predicted from discreet OTFT parameters. As shown in Figure 6-16 B, the threshold voltage shifts to more positive values when the sweep is started at a more positive values, which are comparable to the supply voltage for the ring oscillator. By accounting for this shift in threshold voltage (~4 V), the experimental values match better to predicted values. The parameters reported in Table 6.6 show reasonable agreement with predicted values and confirms that all OTFTs in the ring oscillator shown in Figure 6-26 and 6-25 are working as designed.

TABLE 6.6: Performance of 11-stage Ring Oscillator

Amplitude(V)	8.8		
Stages	11		
Buffer	Integrated		
V_{DD}(V)	12		
C_{LOAD} (pF)	4.8		
	Pred. [44]	Pred. with V_T adjusted	Exp.
V_{MAX}(V)	9.7	9.7	9.1
t_P(μsec)	92	154	132
f_{osc}(Hz)	496	296	345
$P_{Diss.}$(μW)	0.34	0.20	0.24

Several functional ring oscillators were found on a wafer. However, they tended to breakdown if tested for long times (10-20 sec) at the higher supply voltages (V_{DD}) needed achieve oscillation due to the load/driver size mismatch. As will be reported in the next chapter, this technology is unstable beyond -10 V (V_{GS}).
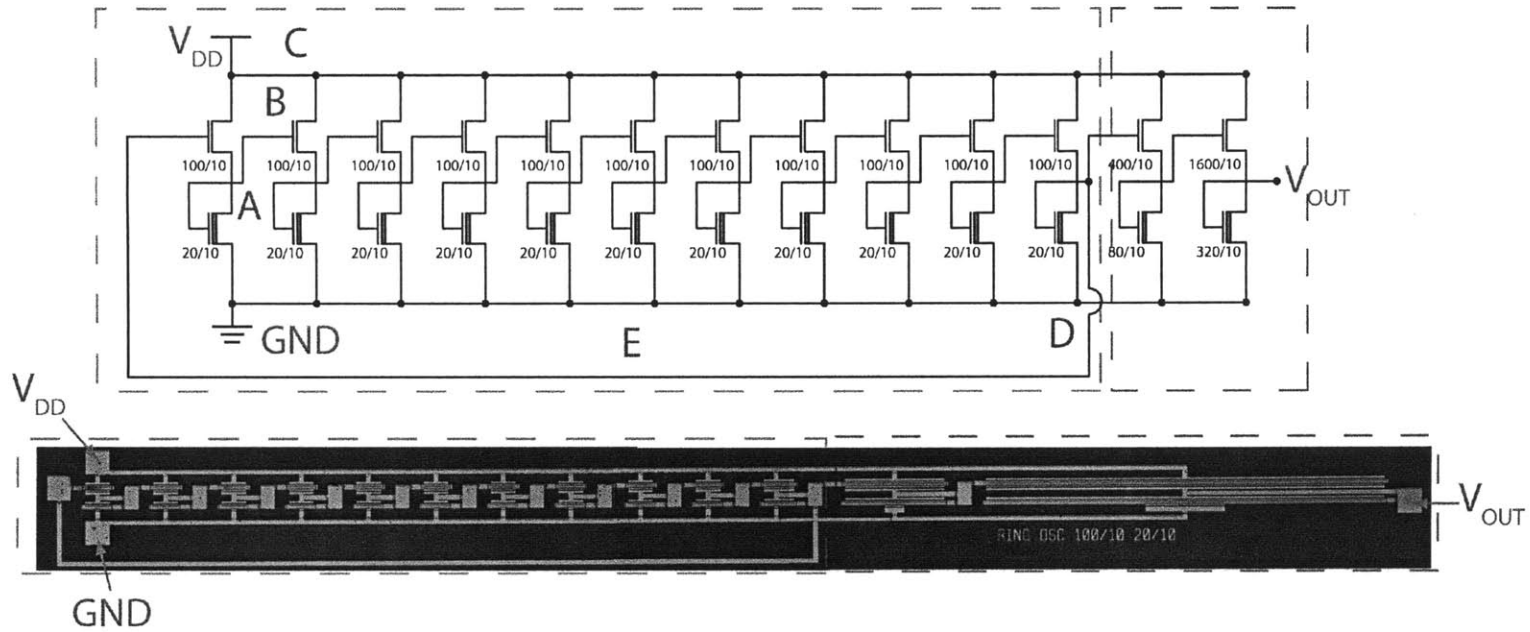
FIGURE 6-25: Circuit schematic and image of an actual 11-stage ring oscillator. The stages consist of the inverters that are illustrated in Figure 6-22
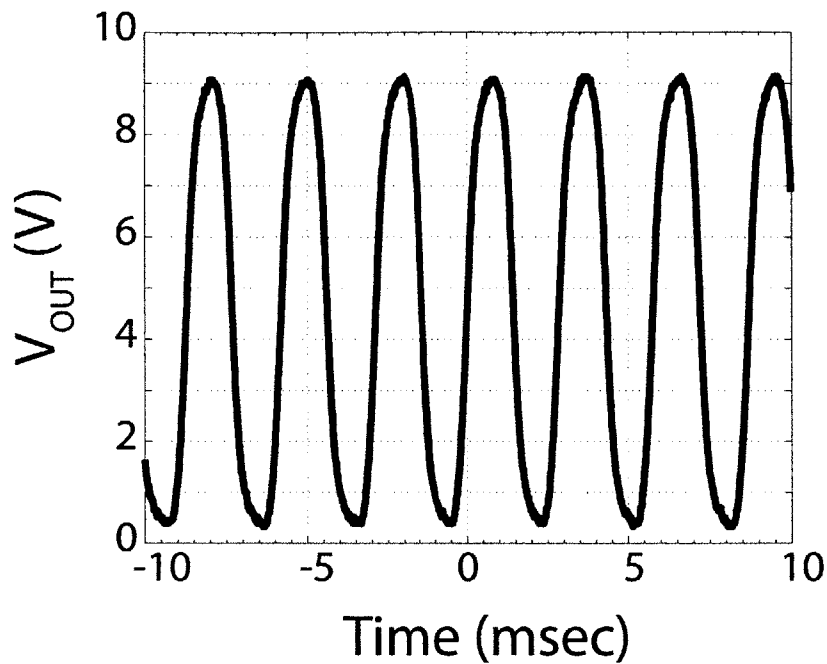
FIGURE 6-26: Ring Oscillator Output Response

6.4 CONCLUSION

The technology reported in this chapter combines multiple innovations demonstrated to improve OTFT performance separately into one complete technology. This system features a high-κ gate insulator and the full integration of two distinct threshold voltages with a low temperature process and patterned semiconductor layer. The logic inverters and ring oscillators serve to prove that this technology is feasible for VLSI. When compared to similar technologies as in Table 6.7, this technology shows comparable performance in propagation delay time. Again as this is a demonstration to illustrate the feasibility of this technology, the circuit sizes (W and L) are not optimized for competitive performance with other performance parameters. Specifically, it is likely that V_{DD} can be decreased without sacrificing propagation delay and increasing gain and noise margins by increasing the size of the driver width, as was shown with Figure 6-22 and Figure 6-23. Further, these results suggest that this technology would be better suited for applications where large amounts of charge must be delivered quickly at low voltages, such as a portable LED display.

TABLE 6.7: Comparison of the performance of OTFT based digital circuits.

Source	This Work	Shang et al. [1]	Nausieda et al. [5]	Cantatore et al. [7]
Inverter Load	Depletion	Enhancement	Depletion	Zero V_{GS}
DriverV_T (V) Load V_T (V)	-0.7 0.7	0.3	-0.5 0.1	2.5
Driver μ (cm^2/Vs) Load μ (cm^2/Vs)	0.0047 0.021	0.16	0.02	0.0125
Driver S (V/dec) Load S (V/dec)	0.78 2.4	NS[24]	NS	Small
V_{DD} (V)	12	5	3	30
Gain	4(estimated)	12	7	NS
Patterning	Photo.	NS	Photo.	Photo.
Insulator	BZN	Al$_2$O$_3$	parylene-C	PVP
κ	40	8	3.15	3.6
# of Stages	11	5	11	NS
t_P (ms)	0.132	0.125	27	NS
f_{osc} (Hz)	345	800	1.5	NS
Static Current	53nA V_{DD}=10 V	10nA V_{DD}=5 V	480fA V_{DD}=3 V	NS
Static Power (nW)	530	500	1	NS

[24]Not Specified

6.5 SUMMARY

The relevant findings if in this chapter are summarized below.

DISCREET TRANSISTORS

- Functional and reproducible OTFTs have been made.

- BZN and pBZN based OTFTs are completely integrated and energy band diagrams are proposed

- The encapsulation in addition to surface treatments gives rise to the difference in V_T as opposed to solely surface treatments as demonstrated by Choi et al. Three additional terms (Q_{semi}, $Q_{encap,it}$, and Q_{encap}) are added to the expression for V_T as a result of the encapsulations process. This sort of encapsulation has been linked in unintentional doping of the pentacene films shifting the V_T and altering the mobility in similar devices reported in literature.

- Heat associated with the patterning process degrades pentacene performance due to the appearance more bulk phase pentacene, which has lower carrier mobility.

- Devices show signs of substantial trap generation with occasional failure at low operating voltages.

153

INTEGRATED CIRCUITS

- Functional and reproducible integrated circuits are demonstrated (logic inverter and ring oscillator) and shows that this technology is feasible for VLSI.

- The circuits showed reasonable agreement with predictions.

- The deviations from predictions are mostly likely due trap generation leading to breakdown in the dielectric.

6.6 REFERENCES

[1] L. Shang, Z. Ji, Y. Chen, H. Wang, X. Liu, M. Han, and M. Liu, "Low voltage organic devices and circuits with aluminum oxide thin film dielectric layer," *SCIENCE CHINA Technological Sciences*, vol. 54, no. 1, pp. 95–98.

[2] J. B. Koo, J. W. Lim, S. H. Kim, S. J. Yun, C. H. Ku, S. C. Lim, and J. H. Lee, "Pentacene thin-film transistors and inverters with plasma-enhanced atomic-layer-deposited Al_2O_3 gate dielectric," *Thin Solid Films*, vol. 515, no. 5, pp. 3132 – 3137, 2007.

[3] H. Klauk, M. Halik, U. Zschieschang, F. Eder, G. Schmid, and C. Dehm, "Pentacene organic transistors and ring oscillators on glass and on flexible polymeric substrates," *Applied Physics Letters*, vol. 82, no. 23, pp. 4175–4177, 2003.

[4] I. Nausieda, K. Ryu, I. Kymissis, A. I. Akinwande, V. Bulovic, and C. G. Sodini, "An organic active-matrix imager," *IEEE Transactions on Electron Devices*, vol. 55, no. 2, pp. 527–532.

[5] I. Nausieda, K. K. Ryu, D. Da He, A. I. Akinwande, V. Bulovic, and C. G. Sodini, "Mixed-signal organic integrated circuits in a fully photolithographic dual threshold voltage technology," *IEEE Transactions on Electron Devices*, vol. 58, no. 3, pp. 865–873, 2011.

[6] N. Gay and W. J. Fischer, "OFET-based analog circuits for microsystems and RFID-sensor transponders," in *Polymers and Adhesives in Microelectronics and Photonics, 2007. Polytronic 2007. 6th International Conference on*, pp. 143–148, 2007.

[7] E. Cantatore, T. C. T. Geuns, G. H. Gelinck, E. van Veenendaal, A. F. A. Gruijthuijsen, L. Schrijnemakers, S. Drews, and D. M. de Leeuw, "A 13.56-MHz RFID system based on organic transponders," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 1, pp. 84–92, 2007.

[8] H. Sirringhaus, T. Kawase, R. H. Friend, T. Shimoda, M. Inbasekaran, W. Wu, and E. P. Woo, "High-resolution inkjet printing of all-polymer transistor circuits," *Science*, vol. 290, no. 5499, pp. 2123–2126, 2000.

[9] J. Shi, M. B. Chan-Park, Y. Wang, H. Yang, and C. M. Li, "A micropatterning technique to fabricate organic thin-film transistors on various substrates," *Journal of Materials Chemistry*, vol. 21, no. 40, pp. 16184–16189.

[10] K. H. Lee, K. Lee, M. S. Oh, J. M. Choi, S. Im, S. Jang, and E. Kim, "Flexible high mobility pentacene transistor with high-κ/low-κ double polymer dielectric layer operating at-5V," *Organic Electronics*, vol. 10, no. 1, pp. 194–198.

[11] L. Zhou, A. Wanga, S.-C. Wu, J. Sun, S. Park, and T. N. Jackson, "All-organic active matrix flexible display," *Applied Physics Letters*, vol. 88, no. 8, p. 083502, 2006.

[12] M. G. Kane, J. Campi, M. S. Hammond, F. P. Cuomo, B. Greening, C. D. Sheraw, J. A. Nichols, D. J. Gundlach, J. R. Huang, C. C. Kuo, L. Jia, H. Klauk, and T. N. Jackson, "Analog and digital circuits using organic thin-film transistors on polyester substrates," *IEEE Electron Device Letters*, vol. 21, no. 11, pp. 534–536, 2000.

[13] H. Wang, Z.-Y. Ji, L.-W. Shang, X.-H. Liu, Y.-Q. Peng, and M. Liu, "Top contact organic field effect transistors fabricated using a photographic process," *Chinese Physics B*, vol. 20, no. 8, p. 087306.

[14] P. Sung Kyu, J. E. Anthony, and T. N. Jackson, "Solution-processed TIPS-pentacene organic thin-film-transistor circuits," *IEEE Electron Device Letters*, vol. 28, no. 10, pp. 877–879, 2007.

[15] H. Jia, E. K. Gross, R. M. Wallace, and B. E. Gnade, "Patterning effects on poly (3-hexylthiophene) organic thin film transistors using photolithographic processes," *Organic Electronics*, vol. 8, no. 1, pp. 44 – 50, 2007.

[16] K. Fukuda, T. Sekitani, T. Yokota, K. Kuribara, T. Huang, T. Sakurai, U. Zschieschang, H. Klauk, M. Ikeda, H. Kuwabara, T. Yamamoto, K. Takimiya, K.-T. Cheng, and T. Someya, "Organic pseudo-CMOS circuits for low-voltage large-gain high-speed operation," *IEEE Electron Device Letters*, vol. 32, pp. 1448 –1450, oct. 2011.

[17] J. B. Koo, S. J. Yun, J. W. Lim, S. H. Kim, C. H. Ku, S. C. Lim, J. H. Lee, and T. Zyung, "Low-voltage and high-gain pentacene inverters with plasma-enhanced atomic-layer-deposited gate dielectrics," *Applied Physics Letters*, vol. 89, no. 3, pp. 033511–3, 2006.

[18] H. Klauk, U. Zschieschang, J. Pflaum, and M. Halik, "Ultralow-power organic complementary circuits," *Nature*, vol. 445, no. 7129, pp. 745–748, 2007.

[19] X.-H. Zhang, S. P. Tiwari, S.-J. Kim, and B. Kippelen, "Low-voltage pentacene organic field-effect transistors with high-κ HfO$_2$ gate dielectrics and high stability under bias stress," *Applied Physics Letters*, vol. 95, no. 22, pp. 223302–3, 2009.

[20] L. Shang, L. Ming, T. Deyu, L. Ge, L. Xinghua, and J. Zhuoyu, "Low-voltage organic field-effect transistor with PMMA/ZrO$_2$ bilayer dielectric," *IEEE Transactions on Electron Devices*, vol. 56, no. 3, pp. 370–376, 2009.

[21] Y. Choi, I. D. Kim, H. L. Tuller, and A. I. Akinwande, "Low-voltage organic transistors and depletion-load inverters with high-κ pyrochlore BZN gate dielectric on polymer substrate," *IEEE Transactions on Electron Devices*, vol. 52, no. 12, pp. 2819–2824, 2005.

[22] W. Chia-Yu, K. Shu-Hao, H. Yu-Ming, H. Wen-Chieh, F. Adriyanto, and W. Yeong-Her, "High-Mobility Pentacene-Based Thin-Film Transistors With a Solution-Processed Barium Titanate Insulator," *IEEE Electron Device Letters*, vol. 32, no. 1, pp. 90–92.

[23] S. Han, X. Liu, J. P. Han, and C. Zhou, "Polymer thin-film transistors with high dielectric constant gate insulators," *Applied Physics A: Materials Science and Processing*, vol. 77, no. 7, pp. 873–875, 2003.

[24] Y. Liang, G. Dong, Y. Hu, L. Wang, and Y. Qiu, "Low-voltage pentacene thin-film transistors with Ta$_2$O$_5$ gate insulators and their reversible light-induced threshold voltage shift," *Applied Physics Letters*, vol. 86, no. 13, pp. 132101–3, 2005.

[25] L. A. Majewski, R. Schroeder, and M. Grell, "One volt organic transistor," *Advanced Materials*, vol. 17, no. 2, pp. 192–196, 2005.

[26] I. Kymissis, A. I. Akinwande, and V. Bulovic, "A lithographic process for integrated organic field-effect transistors," *Journal of Display Technology*, vol. 1, no. 2, pp. 289–294, 2005.

[27] A. I. Wang, *Low Temperature Lithographically Patterned Metal Oxide Transistors for Large Area Electronics*. PhD thesis, Massachusetts Institute of Technology, 2011.

[28] S. D. Wang, T. Miyadera, T. Minari, Y. Aoyagi, and K. Tsukagoshi, "Correlation between grain size and device parameters in pentacene thin film transistors," *Applied Physics Letters*, vol. 93, no. 4, 2008.

[29] J.-M. Kim, S. K. Jha, R. Chand, D.-H. Lee, and Y.-S. Kim, "DNA hybridization sensor based on pentacene thin film transistor," *Biosensors and Bioelectronics*, vol. 26, no. 5, pp. 2264–2269.

[30] J. Mabeck and G. Malliaras, "Chemical and biological sensors based on organic thin-film transistors," *Analytical and Bioanalytical Chemistry*, vol. 384, no. 2, pp. 343–353, 2006.

[31] K. Lee, P. R. Nair, A. Scott, M. A. Alam, and D. B. Janes, "Device considerations for development of conductance-based biosensors," *Journal of Applied Physics*, vol. 105, no. 10, pp. 102046–13, 2009.

[32] M. C. Tanese, L. Torsi, G. M. Farinola, L. Valli, O. H. Omar, G. Giancane, E. Ieva, F. Babudri, F. Palmisano, F. Naso, and P. G. Zambonin, "Enhanced chemical sensing organic thin-film transistors," in *Organic-based Chemical and Biological Sensors*, vol. 6659, (San Diego, CA, USA), pp. 66590A–8, SPIE, 2007.

[33] M. E. Roberts, A. N. Sokolov, and Z. Bao, "Material and device considerations for organic thin-film transistor sensors," *Journal of Materials Chemistry*, vol. 19, no. 21, pp. 3351–3363, 2009.

[34] L. Torsi, "Novel applications of organic based thin film transistors," *Microelectronics Reliability*, vol. 40, no. 45, pp. 779–782, 2000.

[35] R. P. Ortiz, A. Facchetti, and T. J. Marks, "High-κ organic, inorganic, and hybrid dielectrics for low-voltage organic field-effect transistors," *Chemical Reviews*, vol. 110, no. 1, pp. 205–239, 2010,.

[36] D. Guo, S. Ikeda, K. Saiki, H. Miyazoe, and K. Terashima, "Effect of annealing on the mobility and morphology of thermally activated pentacene thin film transistors," *Journal of Applied Physics*, vol. 99, no. 9, pp. 094502–7, 2006.

[37] W. Y. Chou, Y. S. Mai, H. L. Cheng, C. Y. Yeh, C. W. Kuo, F. C. Tang, D. Y. Shu, T. R. Yew, and T. C. Wen, "Correlation of growth of pentacene films at various gas ambience conditions to organic field-effect transistor characteristics," *Organic Electronics*, vol. 7, no. 6, pp. 445–451, 2006.

[38] T. Ji, S. Jung, and V. K. Varadan, "On the correlation of postannealing induced phase transition in pentacene with carrier transport," *Organic Electronics*, vol. 9, no. 5, pp. 895 – 898, 2008.

[39] S. Steudel, K. Kris, Myny, S. De Vusser, J. Genoe, and P. Heremans, "Patterning of organic thin film transistors by oxygen plasma etch," *Applied Physics Letters*, vol. 89, no. 18, p. 183503, 2006.

[40] S. Y. Yang, K. Shin, and C. E. Park, "The Effect of Gate-Dielectric Surface Energy on Pentacene Morphology and Organic Field-Effect Transistor Characteristics," *Advanced Functional Materials*, vol. 15, no. 11, pp. 1806–1814, 2005.

[41] Y.-W. Wang, H.-L. Cheng, Y.-K. Wang, T.-H. Hu, J.-C. Ho, C.-C. Lee, T.-F. Lei, and C.-F. Yeh, "Influence of measuring environment on the electrical characteristics of pentacene-based thin film transistors," *Thin Solid Films*, vol. 467, no. 12, pp. 215 – 219, 2004.

[42] S. Yogev, R. Matsubara, M. Nakamura, and Y. Rosenwaks, "Local charge accumulation and trapping in grain boundaries of pentacene thin film transistors," *Organic Electronics*, vol. 11, no. 11, pp. 1729 – 1735, 2010.

[43] C. Kim, S. Jo, S. Lee, W. Kim, H. Baik, and S. Lee, "Surface-Modified High-κ Oxide Gate Dielectrics for Low-Voltage High-Performance Pentacene Thin-Film Transistors," *Advanced Functional Materials*, vol. 17, no. 6, pp. 958–962, 2007.

[44] R. T. Howe and C. G. Sodini, *Microelectronics: an integrated approach.* Prentice Hall, 1997.

[45] R. Jaeger and T. Blalock, *Microelectronic Circuit Design.* McGraw-Hill, 2010.

159

Chapter 7

A Study of Breakdown in

$(Bi_{1.5}Zn_{1.0}Nb_{1.5}O_{7.0})$

7.1 MOTIVATION

Beyond a proof of concept, gate insulators must prove to be reliable to be suitable for large scale integration. Chapter 6 showed BZN is effective in lowering the operating voltage in OTFTs because of its high dielectric constant. However it's acceptance in OTFTs is limited due reliability issues emanating from high gate leakage and low breakdown fields in films deposited at room temperature [1, 2, 3].

Investigators have addressed current leakage issues by fabricating composite insulators which incorporate larger bandgap insulators [1] and to control parasitic trap assisted transport [3] in BZN. In Chapter 6, large gate currents were minimized by simply using a thicker gate insulator.

However, an assessment of how reliable BZN is as a gate insulator is lacking. Dielectric breakdown has a statistical nature. Breakdown resistance is determined by weaknesses that are randomly distributed in at material; not by the average of a property distributed through a material. Hori writes in regards to dielectric breakdown, "This may require researchers to have a statistical way of thinking" [4]. Thus, dielectric breakdown in BZN is studied by widely accepted stress measurements that determine breakdown conditions with statistical significance. The results from these investigattion will support and elucidate leakage mechanisms in BZN, and to determine how the material can be used for large scale integration. Dielectric constant, time dependent dielectric breakdown (TDDB) and time-zero dielectric breakdown (TZDB) measurements of BZN-based MIM capacitors were conducted to study breakdown as

161

a function of constant DC current stress polarity, dielectric thickness, temperature, and surface treatments.

This chapter reveals that breakdown in BZN occurs by trap generation where breakdown is likely beyond a trap density of 1.5×10^{17} cm^{-3}. This trap generation is recoverable and gives rise to another conduction mechanism which renders the dielectric non-insulating, which was also found by Cho et al. [3]. Prior to breakdown, current flows through the dielectric via Schottky emission. Barrier heights for Schottky emission are extracted from current-voltage behavior prior to breakdown such that complete energy band diagrams can be proposed. Further, the conclusions regarding how breakdown is affected by stress polarity, dielectric thickness, and surface treatments can be made with statistical certainty.

7.2 FABRICATION OF CAPACITORS

Rectangular MIM capacitors of length 500 μm and width 10 μm were used for these investigations. This geometry mimics that of source/drain to gate overlap in the OTFTs described in Chapters 6 and 8. The process mimics that of the OTFTs built in this dissertation which demands minimal annealing, surface treatments and exposure to O_2 plasma to pattern the surface treatments. An organic surface treatment is often used to improve charge transport in OTFTs [5]. In the case of BZN, parylene-C surface treatments are known to shift the threshold voltage in OTFTs [6] and is fully compatible with patterning and fabrication processes needed to build fully integrated OTFTs, as was shown in Chapter 5 and 6. This study explored two thicknesses of BZN (400 nm and 280 nm) and two different top surfaces (bare BZN and ~1-3 nm of parylene on BZN (pBZN)).

Au was deposited by e-Beam evaporation with a Cr adhesion layer and photolithographically patterned for the bottom electrode on a 100 mm glass wafer. 280 nm of BZN was next deposited at room temperature by RF sputtering. One half of the wafer was masked and an additional 120 nm of BZN was then deposited on the unmasked portion of the wafer bringing the total thickness to 400 nm. Approximately, 1-3 nm of parylene-C was deposited on the whole wafer and 1/2 of the wafer was exposed to O_2 plasma to etch away the parylene-C surface treatment. Au was deposited by eBeam evaporation and photolithographically patterned for the top electrode. The dielectric saw two photolithographic steps subjecting the BZN to 40 minutes of heating at 95°C, in air. OTFTs were fabricated in a small area of the wafer to verify that the dielectric was suitable to make devices. Electrical characterization was done in the dark, in air with an Agilent 4156 Semiconductor Parameter Analyzer and a Hewlett Packard 4192A Impedance Analyzer. Figure 7-1 summarizes the thicknesses and parylene-C surface treatments implemented for the MIM capacitors tested. Figure 7-2 illustrates where each type of capacitor was fabricated on the wafer. Figure
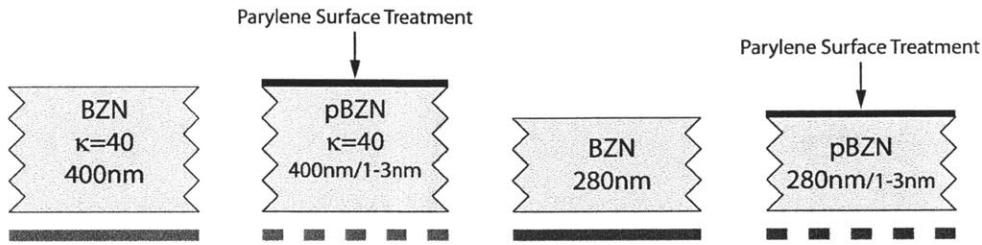
FIGURE 7-1: Insulators stacks tested for quasistatic capacitance, TZDB, TDDB measurements
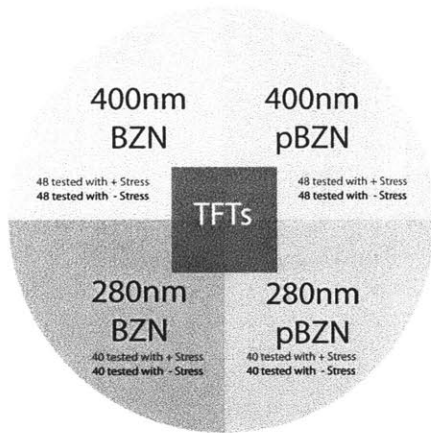
FIGURE 7-2: Map of 100 mm wafer used for reliability studies. 352 capacitors were measured in total.
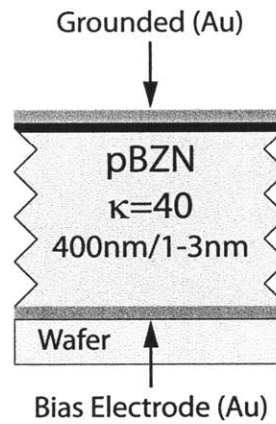
FIGURE 7-3: Example of MIM (400 nm thick pBZN surface) capacitor used to in these studies.

7-3 illustrates a cross section of the MIM structures that were tested and shows the locations of the grounded and biasing electrode.

7.3 DIELECTRIC CONSTANT

Quasistatic Capacitance Voltage measurements were used to extract the dielectric constants (Equation 7.1) from the MIM capacitors. These values are in good agreement with values extracted from the same capacitors at 1 MHz. Figure 7-4 shows the parylene-C surface treatment changes dielectric constant of the stack less than variation seen between capacitors with the same insulator. The standard deviation for all insulators suggests about a 5% variability in the dielectric constant. The thinner insulators appear to have a slightly larger dielectric constant, which may be an artifact of the larger current leakage through these films.

Equation 7.2 used to determine $\kappa_{eff,ideal}$ with surface treatment thickness assumed to be ~2 nm. Table 7.1 summarizes the properties of BZN and pBZN from MIM capacitors.

163
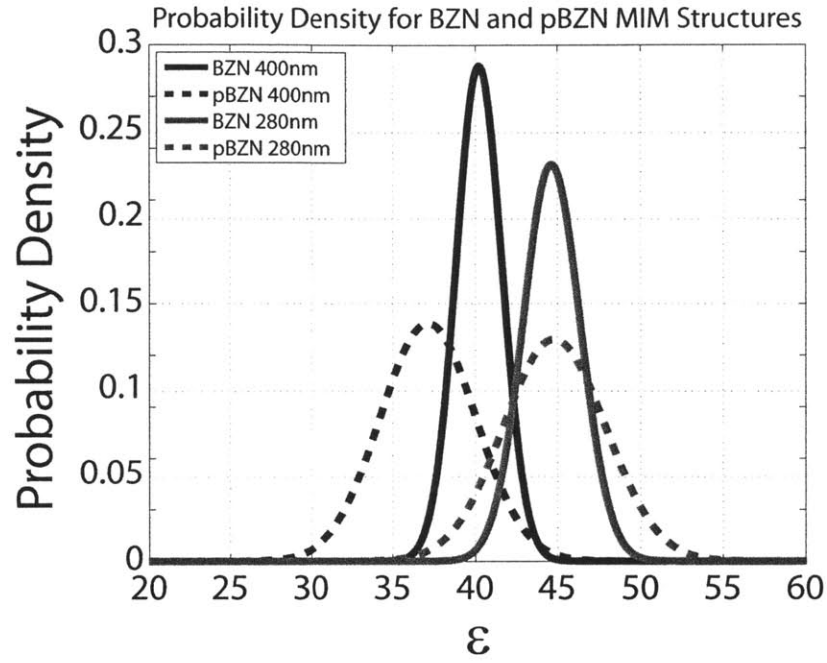
FIGURE 7-4: Probability distribution for dielectric constants extracted from 288 MIM capacitors with Area= 5×10^{-5} cm^2. The dielectric constants of BZN and pBZN are essentially the same, with a variation of about 5%

$$C = \frac{Area \times \epsilon_o \times \kappa}{t_{OX}} \tag{7.1}$$

$$\frac{1}{C} = \frac{1}{C_{BZN}} + \frac{1}{C_{par}}$$

$$\frac{t_{BZN} + t_{par}}{\dfrac{t_{BZN}}{\kappa_{BZN}} + \dfrac{t_{par}}{\kappa_{par}}} = \kappa_{eff,idl} \tag{7.2}$$

Where,

      C (F/cm^2): total capacitance per unit area

      C_{BZN}(F/cm^2): capacitance per unit area of BZN

      C_{par}(F/cm^2): capacitance per unit area of parylene-C

      t_{BZN}(nm): thickness of BZN

      t_{par}(nm): thickness of parylene-C

      κ_{BZN}: dielectric constant of BZN

      κ_{par}: dielectric constant of parylene-C

TABLE 7.1: Extracted dielectric constants and leakage current from 288 MIM capacitors total. 72 MIM capacitors were measured for each dielectric surface and thickness. 5 capacitors were measured for each dielectric surface and thickness at 1MHz.

Thickness	Surface	Cap F/cm^2	$\kappa_{eff}(\pm\sigma)$	$\kappa_{eff,idl}$	FWHM[1]	J at -0.5V nA/cm^2	κ @1MHz
400 nm	BZN	8.89E-8	40 ($\pm$1)	-	2.4	2.2	39
400 nm	pBZN	8.21E-8	37 ($\pm$3)	38	7.1	1.7	33
280 nm	BZN	1.41E-7	45 ($\pm$1)	-	2.4	14	44
280 nm	pBZN	1.42E-7	45 ($\pm$3)	41	7.1	9.4	39

[1]Full Width Half Max $= 2\sqrt{2ln2}\sigma$

7.4 ELECTRICAL STRESS TESTING and RESULTS

When an external electric field or current is applied to a solid, electrons will flow through the solid. The flowing electrons will transfer energy into the solid by colliding with the atoms and/or ions that make up the solid. These collisions create defects and are referred to as electrical stressing. Breakdown in an insulator occurs when enough defects are generated to disrupt the atomic arrangement of the atoms and/or ions holding the solid together. A large rearrangement of the atomic structure will lead to drastic changes in the electric properties of the material. For the following experiments, a constant current electrical stress in one study and a ramped voltage electrical stress in another will be used to induce dielectric breakdown in BZN and pBZN. From these studies, conditions and mechanisms for dielectric breakdown will be revealed.

7.4.1 Time-Dependent Dielectric Breakdown (TDDB): Constant Current Electrical Stress

For this measurement, a constant current is forced through the dielectric while the voltage necessary to maintain the constant current (VG) is measured as a function of time. According to Suñé et al., charge traps are created as a result of this stress. To keep the stress current constant, the forcing voltage must increase to compensate for the influence of the increasing number of trapped electrons. With constant current stressing, there are two notable regions as shown in Figure 7-5. In Region 1, pre-existing traps are filled with electrons and the forcing voltage evolves exponentially. As the preexisting traps are filled, the material enters Region 2 where traps are both generated and filled and the forcing voltage can be approximated to be linear [7]. Extracted parameters from TDDB measurements are shown in Figure 7-6 and Equation 7.3 through 7.5.

165
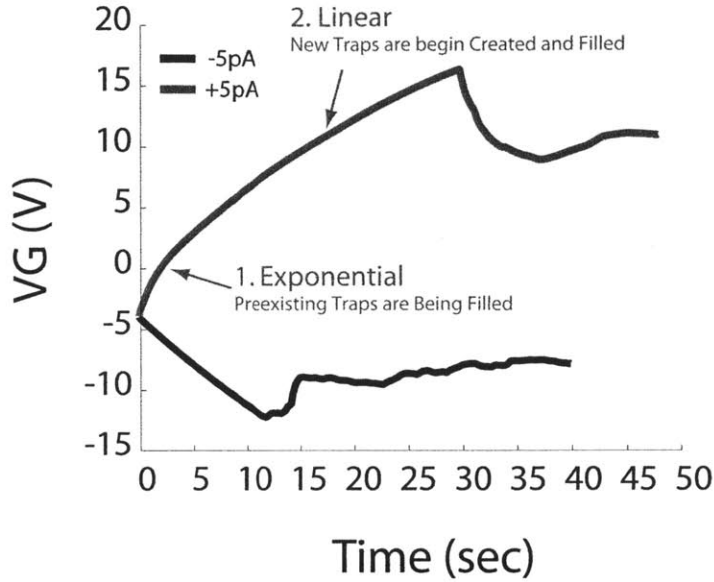
FIGURE 7-5: Results from TDDB measurements showing two regions of different VG(I) dependence. Two different capacitors with 400 nm of BZN are stressed, one positive and one negative. Region 1 shows an exponential dependence where preexisting or initial charge traps are filled. Region 2 shows a linear dependence where new traps are generated and filled.
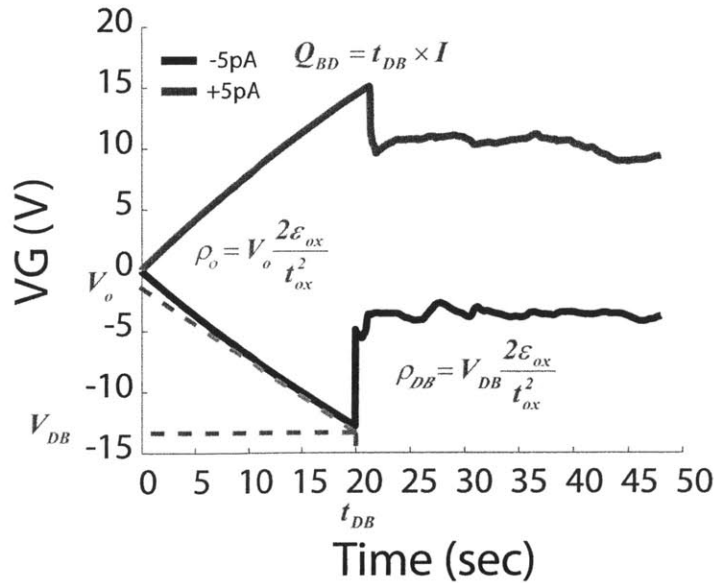
FIGURE 7-6: Typical results from TDDB constant current measurements and definition of extracted properties [8].

166

$$VG(t) = V_o exp\left(\frac{t}{\tau}\right) + tW_t \tag{7.3}$$

$$V = \rho\frac{t_{OX}^2}{2\kappa\epsilon_O} \tag{7.4}$$

$$Q_{BD} = t_{BD} \times J \tag{7.5}$$

Where,

VG (V): forcing voltage required to maintain a constant current (Equation 7.3)

V_o(V): exponential prefactor

τ(s): characteristic exponential voltage decay time

$W_t(Vs^{-1})$: linear rate of rise in the forcing voltage

V_{BD}(V): the voltage where the dielectric breaks down

$\rho_o(cm^{-3})$: initial trap density (Equation 7.4)

$\rho_{BD}(cm^{-3})$: trap density at breakdown (Equation 7.4)

$Q_{BD}(Ccm^{-2})$: charge delivered until breakdown (Equation 7.5)

To minimize microstructural changes due to joule heating, stress conditions were chosen such that breakdown occurred within 48 seconds. A current stress of $\pm$5pA was applied to bottom contacts while the top contact was grounded with one measurement taken every 40 ms. 160 capacitors were measured, 40 for each thickness and surface with 20 for each polarity. Table 7.2 summarizes the results from TDDB constant current measurements.

From Figures 7-6 and 7-5, V_o, W_t, and ρ_o, are very sensitive to how the linear fit is made in Region 2. Further Region 2 can only be approximated as a line if $t_{DB}<\tau$ [7]. As studying the breakdown behavior of these insulators is the priority and short stress times are used, the extraction of V_o, W_t, and ρ_o may not be optimized as τ is unknown for this system. Parameters V_{BD}, t_{BD}, and ρ_{BD} can be extracted from the Figure 7-6 with less ambiguity and will be used to reveal breakdown mechanism and trends.

It was observed that insulators under positive stress broke down at higher field than under negative stress. Comparing at the same polarity, the pBZN broke down at higher fields than the BZN. There is no E_{BD} dependence on thickness excluding the 400 nm thick pBZN insulator which indicates a larger E_{BD}.

TABLE 7.2: Summary of parameters extracted from TDDB constant current measurements.

BZN 400	Stress (-)	Stress (+)	pBZN 400	Stress (-)	Stress (+)
$Q_{BD}(\mu C/cm^2)$	1.4 (±0.7)	2.0 (±0.5)	$Q_{BD}(\mu C/cm^2)$	2.1 (±0.5)	2.3 (±0.5)
$\rho_{BD}(cm^{-3})$	2.0×10^{17} (±5.7×10^{16})	-2.8×10^{17} (±7.0×10^{16})	$\rho_{BD}(cm^{-3})$	3.8×10^{17} (±8.8×10^{16})	-3.9×10^{17} (±6.1×10^{16})
$V_{BD}(V)$	-7.2 (±2.1)	10 (±2.6)	$V_{BD}(V)$	-14 (±3.2)	14 (±2.2)
$E_{BD}(MV/cm)$	-0.18(±0.05)	0.25(±0.07)	$E_{BD}(MV/cm)$	-0.35(±0.08)	0.35(±0.06)
$t_{DB}(sec)$	13.7 (±7.1)	19.7 (±5.1)	$t_{DB}(sec)$	21.5 (±5.3)	22.7 (±4.6)
BZN 280	**Stress (-)**	**Stress (+)**	**pBZN 280**	**Stress (-)**	**Stress (+)**
$Q_{BD}(\mu C/cm^2)$	1.7(±0.8)	1.8(±0.6)	$Q_{BD}(\mu C/cm^2)$	2.0 (±0.9)	2.5 (±0.9)
$\rho_{BD}(cm^{-3})$	2.3×10^{17} (±3.6×10^{16})	-2.8×10^{17} (±5.5×10^{16})	$\rho_{BD}(cm^{-3})$	2.8×10^{17} (±5.2×10^{16})	-3.5×10^{17} (±5.1×10^{16})
$V_{BD}(V)$	-4.2 (±0.6)	4.9(± 1.0)	$V_{BD}(V)$	-5.1 (±0.9)	6.2(±0.9)
$E_{BD}(MV/cm)$	-0.15(±0.02)	0.18(±0.04)	$E_{BD}(MV/cm)$	-0.18(±0.09)	0.22(±0.09)
$t_{DB}(sec)$	16.6 (±7.7)	18.5 (±6.2)	$t_{DB}(sec)$	20.1 (±9.1)	24.9 (±8.5)

7.4.2 Time-Zero Dielectric Breakdown (TZDB) and Temperature

For these measurements, voltage is ramped at fast step rates to prevent time dependent effects. In addition, this measurement offers rapid evaluation of breakdown behavior [4, 9] hence "Time-Zero". Further, it allows for the extraction of intrinsic and extrinsic breakdown in the insulator with good resolution [10]. Specific to the films and tests in this study, the ramp rates for the TZDB and VG rise rates from TDDB are comparable. Thus, it is likely the two stressing techniques (TDDB and TZDB) will measure the same breakdown phenomena.

Quasistatic CV measurements were taken before and after stressing. Both positive and negative biases were applied to bottom contacts while the top contact was grounded for stressing. The stress voltage was ramped from 0 to ±50 V. The test conditions are a [2]step size of 0.5 V, a [3]Hold time of 1 sec., and a [4]delay time of 0.1 sec. The capacitors were not functional after stressing. Current-Voltage (I V) characteristics show that the current increases with voltage. Generally, the pBZN insulator broke down at a higher voltages compared to the BZN insulator. Results from the TDDB measurements agree with the TZDB measurements results regarding the dependence of breakdown voltage on surface treatments, polarity, and thickness. 160 capacitors were measured, 40 for each thickness and surface with 20 for each polarity.

---

[2] voltage change increment   [3] time allowed for the system to settle after starting sweep   [4] time allowed for the system to settle after incrementing voltage
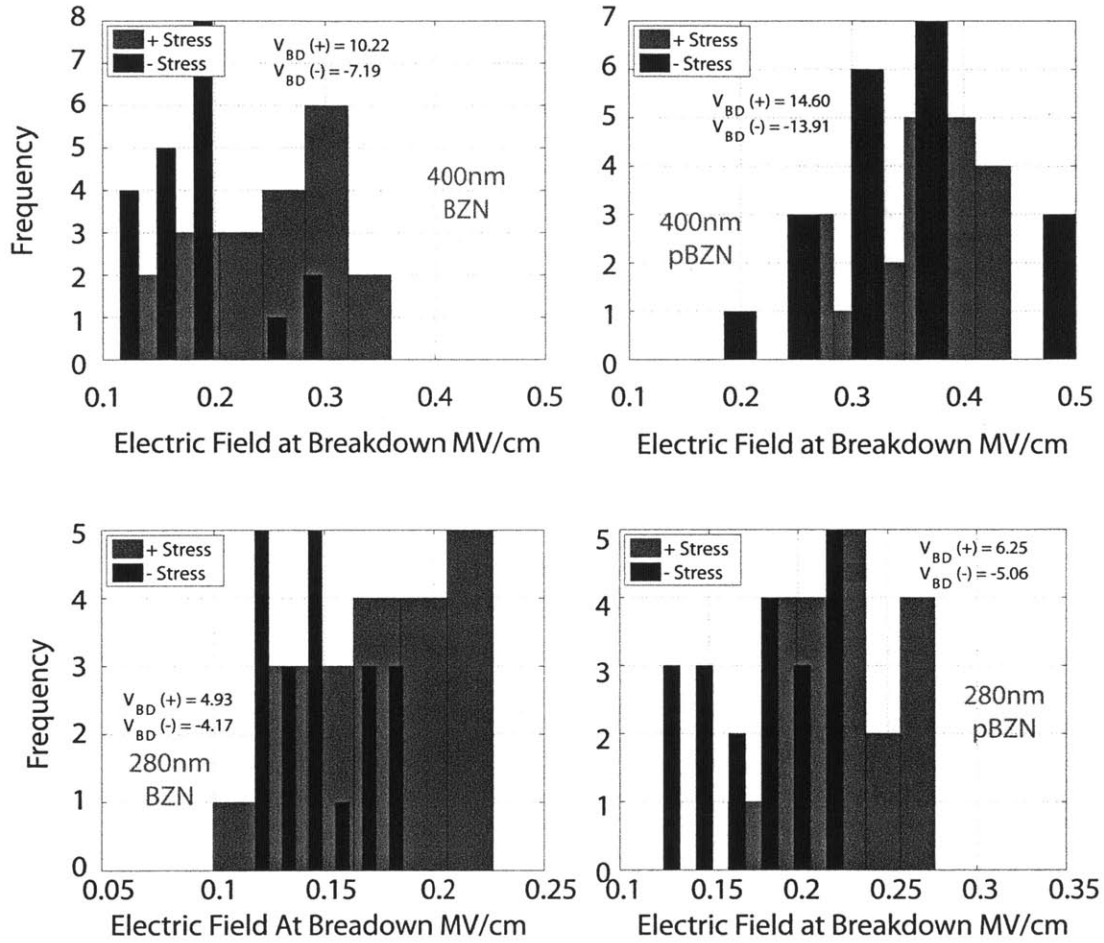
FIGURE 7-7: Histograms generated from TDDB stress measurements

TABLE 7.3: Breakdown results from TZDB measurements at room temperature

Dielectric Thickness	Surface	Positive Bias (V)	Negative Bias (V)	Positive Bias ($^{MV}/_{cm}$)	Negative Bias ($^{MV}/_{cm}$)
400 nm	BZN	7.5($\pm$2.7)	-6.1($\pm$1.8)	0.19($\pm$0.07)	-0.15($\pm$0.05)
400 nm	pBZN	12.2($\pm$3.3)	-12.0($\pm$3.0)	0.30($\pm$0.08)	-0.30($\pm$0.08)
280 nm	BZN	5.6($\pm$1.1)	-4.5($\pm$0.8)	0.20($\pm$0.04)	-0.16($\pm$0.03)
280 nm	pBZN	7.3($\pm$1.7)	-5.6($\pm$1.0)	0.26($\pm$0.06)	-0.20($\pm$0.04)

TZDB measurements were selected for experiments that explore conduction as a function of temperature as the fast ramp rates allow data to be extracted quickly at elevated temperatures to minimize microstructural changes in the dielectric. Quasistatic Capacitance Voltage measurements were taken before and after stressing.

169
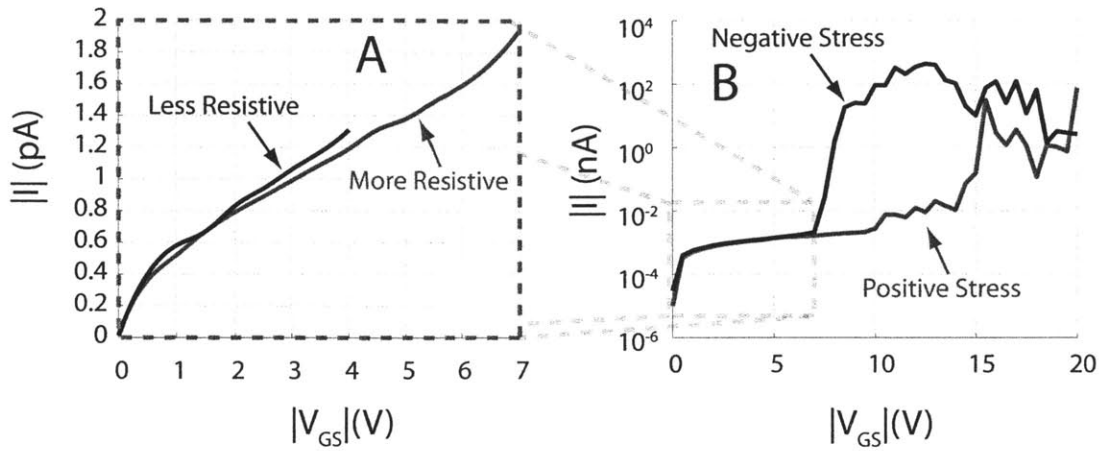
FIGURE 7-8: TZDB Typical current-voltage characteristics for MIM capacitors. The capacitors tested has a 400 nm BZN insulator with Area= $5 \times 10^{-5} cm^2$

Positive and negative biases were applied to bottom contacts while the top contact was grounded. The stress voltage was ramped from 0 to -10 V with a step size of -0.25 V, a Hold time of 1 sec., and a delay time of 0.1 sec. Tests were done at room temperature, 55°C, 75°C, and at 90°C. Capacitors were functional after stressing. Increasing the temperature resulted in higher currents. Evaluating the current-voltage behavior upon returning the capacitors to room temperature indicated that structural changes due to heating were either minimal or temporary. These results are shown in Figures 7-10 and 7-11. 32 capacitors were measured, 4 at each temperature and for each surface of the 400 nm thick insulators.
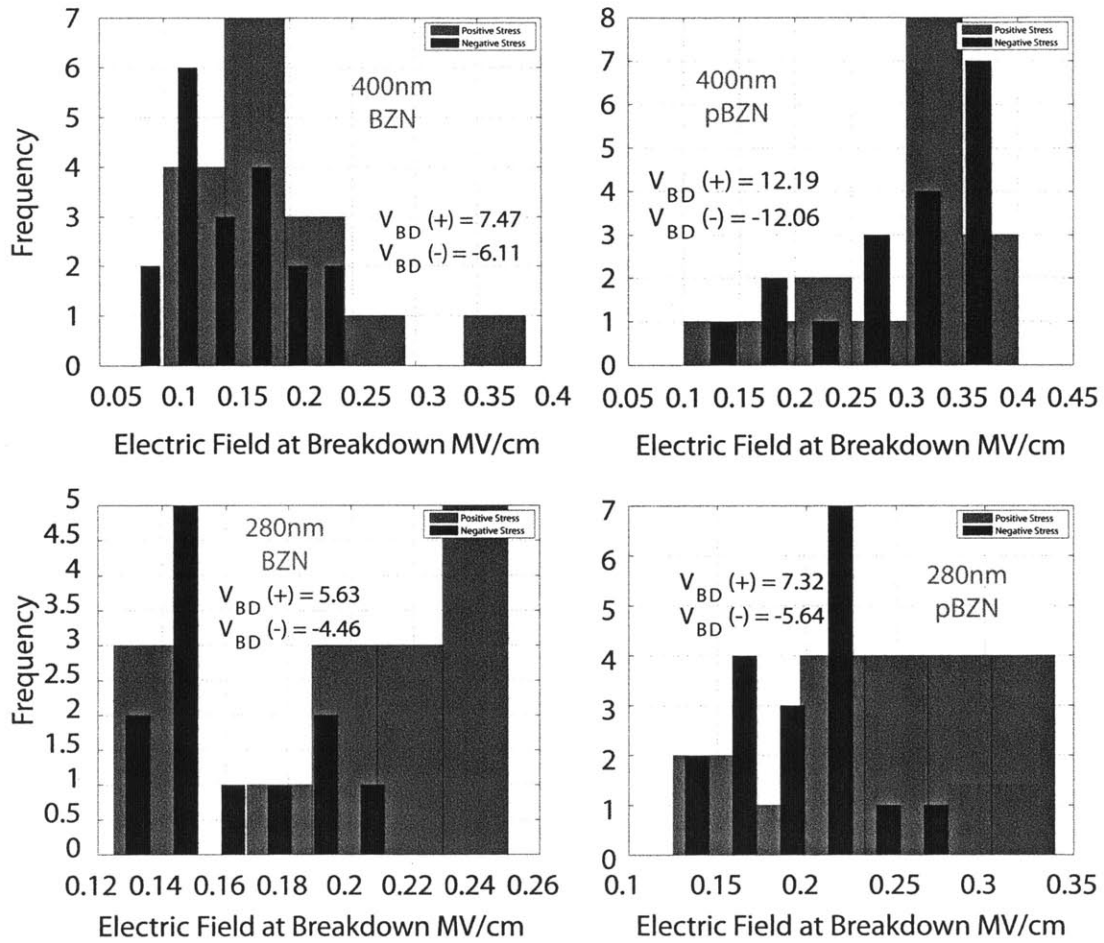
FIGURE 7-9: Histograms generated from TZDB stress measurements
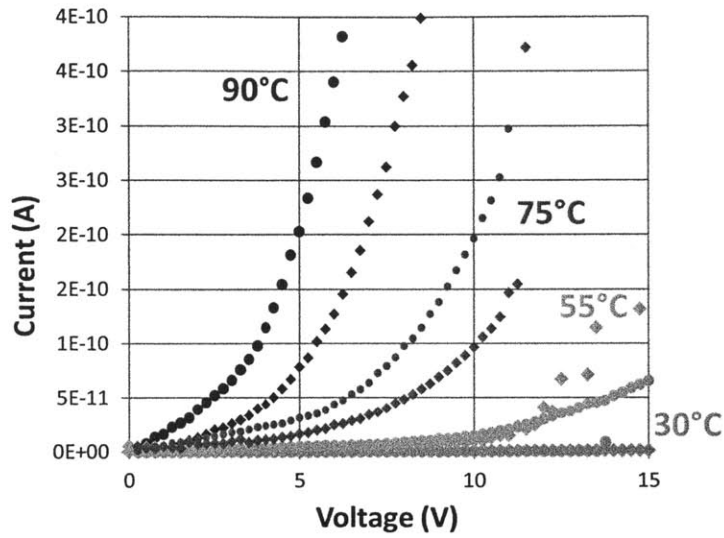
FIGURE 7-10: Current-voltage characteristics taken at 30°C, 55°C, 75°C, 90°C.
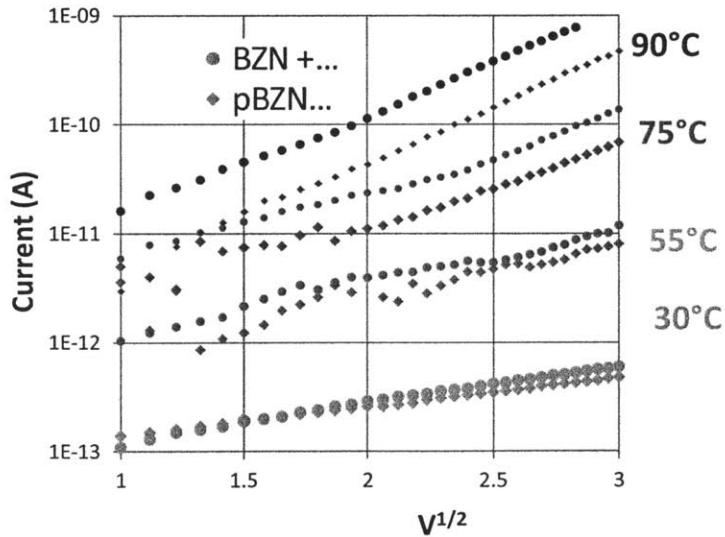
FIGURE 7-11: Semilog I $V^{1/2}$ Characteristics taken at 30°C, 55 °C, 75°C. 90°C ambient temperatures.

7.5 DISCUSSION

Polarity of Stress

For all capacitors, positive stress showed a larger average breakdown voltage or breakdown electric field (V_{BD} and E_{BD}). Q_{BD} and ρ_{BD} follow V_{BD} as they are extracted/calculated from this value. However, the variability suggests that the stress polarity has a very minimal effect on breakdown behavior. In the case of high-κ insulators, it is useful to treat them as wide bandgap semiconductors [11]. As is the case with most semiconductors, hole and electron transport are not the same, normally showing different mobilities for each carrier. Okada et al. report reliability studies on high-κ insulators (HfO_2) and propose a model which suggests that different stress polarity can result in different breakdown (V_{BD}) depending on which carrier (electron or hole) is dominant [12]. Stress tests should be done with p-channel and n-channel MOSFETs to determine the dominant charge carrier in BZN, which then can be correlated to the breakdown sensitivity to polarity.

Parylene-C: Surface Treatment and Thickness of Dielectric

When comparing BZN to pBZN (same polarity) at a thickness of 400 nm, pBZN showed a larger average breakdown voltage or electric field (V_{BD} and E_{BD}). The variability shows this is statistically significant. However, Q_{BD} does not vary significantly comparing of BZN and pBZN. Comparing BZN to pBZN (same polarity) at a thickness of 280 nm, pBZN showed a larger average breakdown voltage or electric field (V_{BD} and E_{BD}), though the variability suggests these are about the same. Again, Q_{BD} does not vary significantly and is the same for BZN and pBZN. Q_{BD} is the same for all insulators stacks measured and the current passed through the film can fundamentally be related to the density of traps at breakdown (ρ_{BD}).

However, Table 7.2 shows the 400 nm pBZN insulator to have a larger ρ_{BD}. Accounting for ~5% reduction in dielectric constant due to the parylene-C surface treatment from Equation 7.2, ρ_{BD} is also reduced by ~5%, which places the values within the range of variability suggesting the same ρ_{BD} for all insulator stacks. Assuming the surface treatment only effects the surface of the insulators, the same ρ_{BD} for all insulators suggests that the majority of trap generation occurs in the bulk of the insulators. Though not insulating and possibly obscured by material variations across the wafer, the surface treatment reduces the voltage dropped across the BZN enabling better breakdown resistance. The parylene-C may be suppressing trap generation at the interface with the grounded electrode. However this cannot be readily extracted from these types of measurements [8]. Further and more notably this confirms that breakdown occurs via trap generation and suggests that the generated trap density in these insulators is a better predictor of the impending breakdown than electric field in this system.

173

7.5.1 Time-Dependent Dielectric Breakdown (TDDB): Constant Current and Reversible Soft Breakdown

TDDB results also show that breakdown is not fatal. Figure 7-12 shows the MIM structures to be functional after 5 stressing cycles, where the material was insulating and then broke down. Once the bias was removed, the structures became insulating again. This has two implications; the first is that another conduction mechanism becomes activated beyond a certain trap density. The first implication being true, the second implication is that the generated traps recover upon removal of the bias. Such observations are in agreement with Cho et al., who reports two types of conduction mechanism in similar BZN films, Schottky emission at low electric fields and Frenkel-Poole at larger electric fields [3].
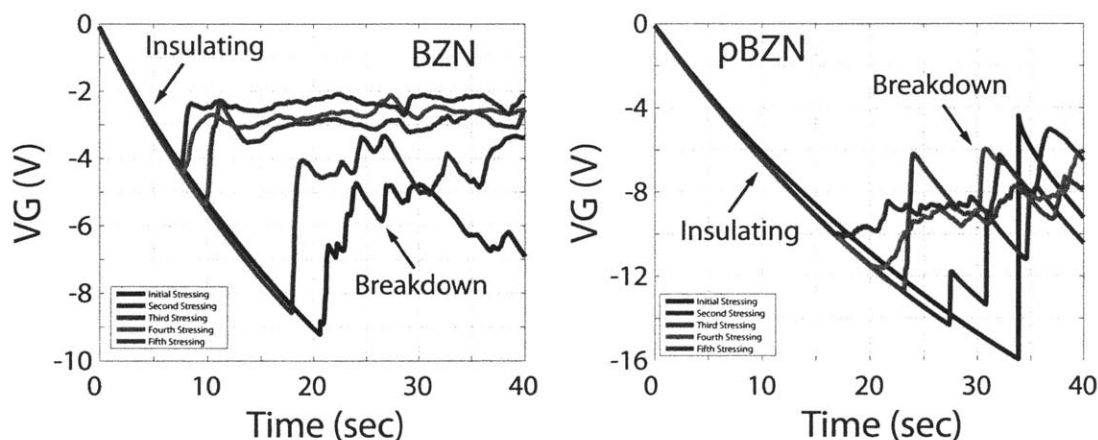
FIGURE 7-12: TDDB showing non-fatal breakdown in BZN and pBZN MIM capacitors, 5 stressing cycles were run on the same capacitor consecutively.

The breakdown detected in these studies can be thought of as a soft breakdown, which has been observed in HfO_2, another high κ gate insulators that is used in Si-based VLSI and in ultra-thin SiO_2 films [13, 14, 15, 16]. Reports attribute soft breakdown to the creation of a weak localized percolation path between the electrodes as a result of a critical number of traps generated ρ_{BD} in the insulator bulk and interface. An example of soft breakdown in shown in Figure 7-14.

This soft breakdown is permanent in most cases however, a reversible soft breakdown is realizable with low voltage stressing [17] and with materials that have a low defect formation energy [18]. Further, investigations are needed to determine what kinds of generated defects lead to breakdown in these BZN films and their associated energies. From these results, the energy for trap generation in BZN is likely to be small as a substantial amount of traps are generated at low voltages.
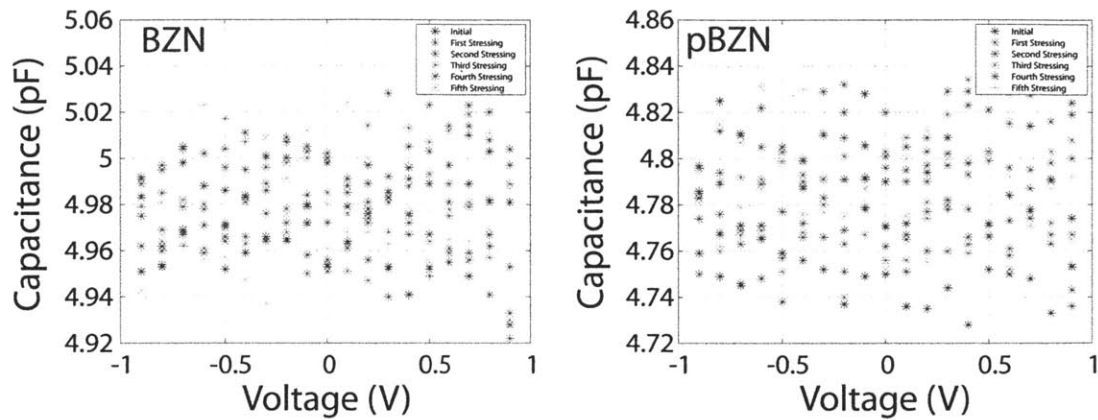
FIGURE 7-13: Capacitance of BZN and pBZN MIM structures before and after 5 TDDB stressing cycles were run on the same capacitor consecutively. The capacitance of the respective MIM structures is not affected by the recoverable breakdown.
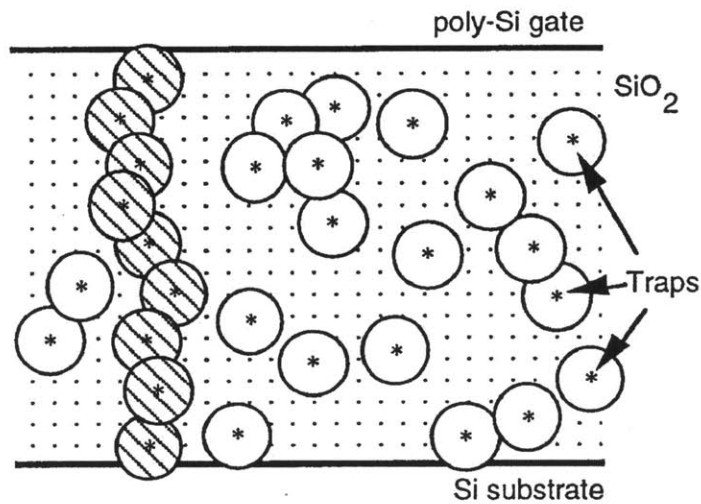
FIGURE 7-14: Illustration intrinsic oxide reversible soft breakdown based on trap generation and conduction via traps. A percolative path is indicated by the hatched circles [16]. If permanent damage is not sustained, the material can recover its insulator properties (reversible soft breakdown).

7.5.2 Time-Zero Dielectric Breakdown (TZDB) and Temperature

Results from TZDB measurements agree with those from TDDB measurements. For tests run at room temperature, the insulators showed better breakdown resistance with positive stressing compared to negative stressing on average, where variability suggested the difference is not statistically significant. The parylene-C surface treatment improved the average breakdown field with statistical significance.

The ramp rates for these measurements are comparable to the rate of rise of the forcing voltage (VG) for the TDDB measurements discussed in the last section. Further, as these measurements showed the same trends in regards to surface treatments, thickness and polarity, TZDB and TDDB measurements are capturing the same soft breakdown phenomena. This suggests that the total amount of charge delivered through the bulk at breakdown (Q_{BD}) or trapped density at breakdown (ρ_{BD}) is a measure of breakdown as concluded by TDDB measurements. This supports that breakdown occurs via trap generation and a weak localized percolative path as concluded in the last section.

Electrical Behavior Before Breakdown:
Conduction in BZN via Schottky emission
Electrical conduction in these sputtered deposited BZN films showed two types of conduction. The first dominates before the reversible soft breakdown and is suspected to be Schottky emission. This is an electronic transport mechanism characterized by thermionic emission of over a potential barrier. The potential barrier (ϕ_B) is the difference between the work function of the metal electrode and valence or conduction band energy level depending on the carrier transport the film [19, 20, 21]. This type of emission has a field dependence because the conduction band energy level in the insulator, and therefore the potential barrier (ϕ_B), is lowered by the image forces between the electrons in the insulator and the metal. The image force is proportional to the electric field through the insulator. A diagram illustrating this type of conduction in shown in Figure 7-15. Equation 7.6 is the current-voltage behavior for Schottky emission and is said to be active if plotting $ln[J/A**T^2]vs.V^{1/2}$ shows a linear dependence as in Equation 7.7 [19, 20, 21]. This is seen for both BZN and pBZN in Figure 7-16. Using Equation 7.7, barrier heights are extracted and reported in Table 7.4.

$$J = A^{**}T^2 exp\left[\frac{-q\left(\phi_B - \sqrt{qV/4\pi\kappa\epsilon_o t_{OX}}\right)}{kT}\right] \tag{7.6}$$

$$ln\frac{J}{A^{**}T^2} = \frac{-q\phi_B}{kT} + \frac{\sqrt{q/4\pi\kappa\epsilon_o t_{OX}}}{kT}\sqrt{V} \tag{7.7}$$
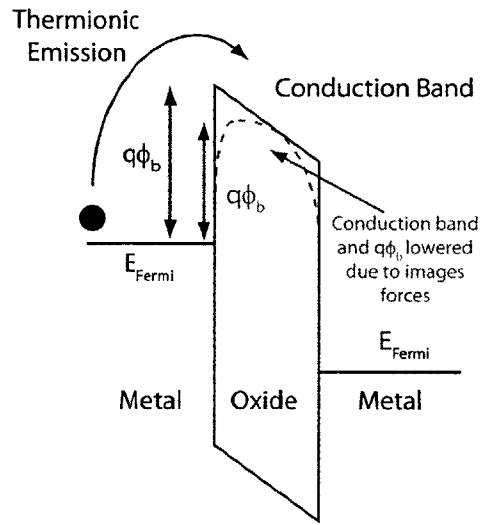
FIGURE 7-15: Energy band diagram showing Schottky emission [21]

Where,

 J (A/cm^2): current density

 T (K): Temperature

 k (eV/K): Boltzmans' Constant

 A** $(A/cm^2 K^2)$:effective Richardson constant (120)

 q (C): elementary charge

 ϕ_B (eV): Schottky Barrier Height

 V (V): applied voltage or bias

 κ : dielectric constant of insulator

 t_{OX} (nm): thickness of insulators

 ϵ_o (F/cm): permittivity of Free Space (8.85×10^{14})

TABLE 7.4: Extracted Schottky barrier heights (ϕ_B) from MIM capacitors

Temperature	30°C	55 °C	75°C	90°C
Surface/Bias	Barrier Height ϕ_B ($\pm$0.04)			
BZN/Positive (eV)	0.96	0.99	1.03	1.04
BZN/Negative (eV)	0.95	0.99	0.99	1.00
pBZN/Positive (eV)	0.95	1.00	1.06	1.10
pBZN/Negative (eV)	0.92	0.99	1.02	1.03

177
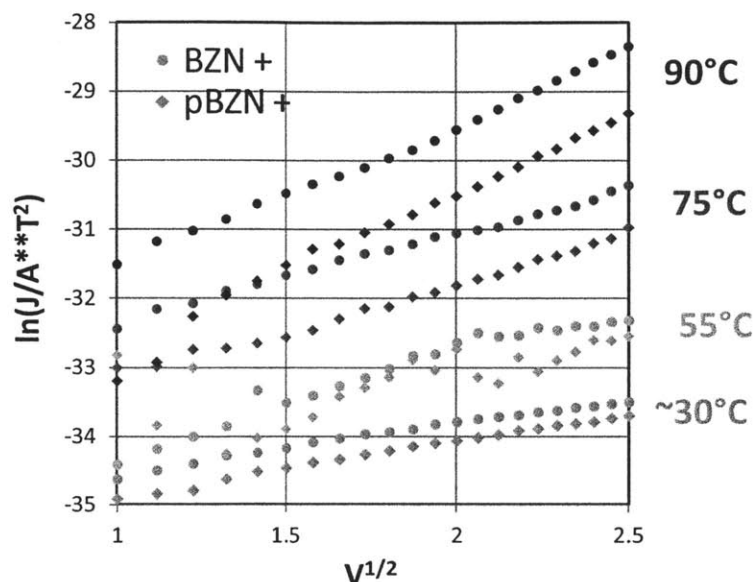
FIGURE 7-16: Confirmation of Schottky emission

Barrier Height Extraction and Band Diagrams

From Table 7.4, the barrier height appears to be insensitive to the direction of stressing, and therefore the conditions of the interfaces at the electrodes. A higher resolution extraction method may reveal how the barrier height depends on interfaces at the electrodes. From Table 7.4, barrier height also appears to depend on temperature which may be an artifact of the testing setup. Roberston et al. reports that at a barrier height of at least 1 eV is necessary for oxides to serve as insulators in electronic devices[11]. The work function of Au (5.1 eV) is close to HOMO level of pentacene (4.9 eV below the vacuum level). Therefore, the barrier heights extracted for BZN and pBZN on Au are barely tolerable for BZN and pBZN to function as an insulator for pentacene based OTFTs.

For a simple determination of the band structure, the electron affinity model is used [22, 23]. In this model, the barrier height for Schottky emission is the difference in the absolute energy of the conduction or valence band energy level of BZN and the work function of the metal electrode. Assuming the Schottky barrier is between Au and the valence band of BZN, Figure 7-17 shows this band alignment with BZN**. Assuming the Schottky barrier is between Au and the conduction band of BZN, Figure 7-17 shows this band alignment with BZN. The work function of Au is 5.1 eV and the work function of Pt is 6.35 eV. If the valence band energy level is for BZN is at 6.1 eV or 1 eV below Au, Pt cannot serve as a metal electrode for MIM capacitors as no Schottky barrier ($\phi_B = -0.25 eV$) would exist. This is indicated in Figure 7-17.
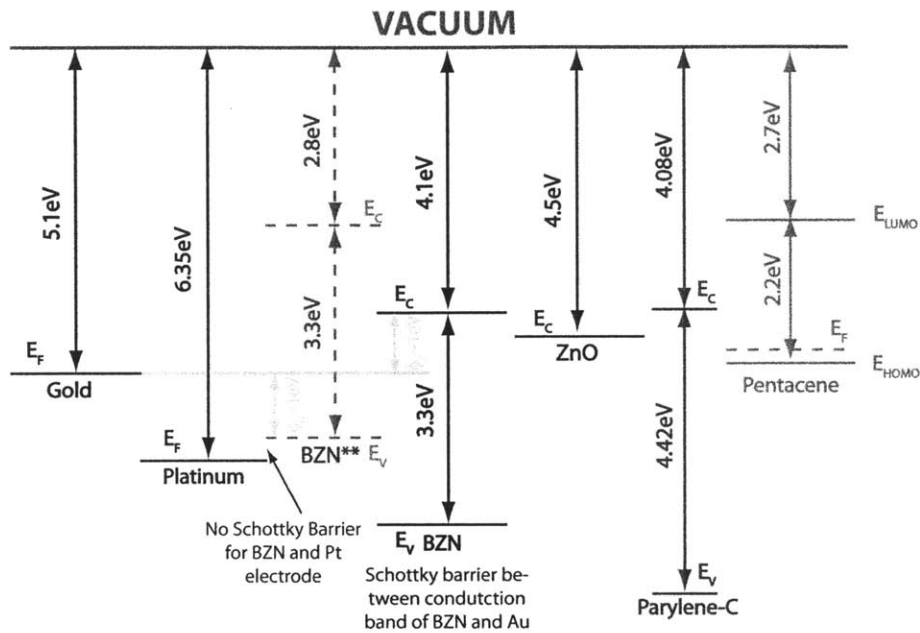
FIGURE 7-17: Energy band levels for Au, Pt, ZnO, BZN, pentacene, and parylene-C. The Schottky barrier for the MIM structures studied in this work is likely between the conduction band of BZN and the work function of Au.

As Cho et al. report functioning MIM capacitors with Pt electrodes, the extracted barrier height is likely between the conduction band energy level of BZN and work function for Au for the MIM capacitors in this work. This should be confirmed with more materials characterization to determine the existence of interface dipoles due to charge transfer and Schottky barrier pinning [24, 11] and more tests to determine the dominant and subordinate carriers in BZN [12]. If the barrier height for Schottky emission is between the conduction band energy level of BZN and the work function of Au, the conduction band energy level for BZN must be at 4.1 eV below vacuum. In this case, BZN will serve as a very leaky gate insulator for ZnO based TFTs as a barrier height of 0.4 eV for Schottky emission from ZnO to BZN is small. There are many reports of fully functional ZnO based TFTs using BZN as a gate insulator and gate leakage is cited as limiting issue [1, 2, 25, 26]. Energy band diagrams from this analysis and reasoning are shown in Figure 7-18.

179

BZN MIM Capacitors

pBZN MIM Capacitors
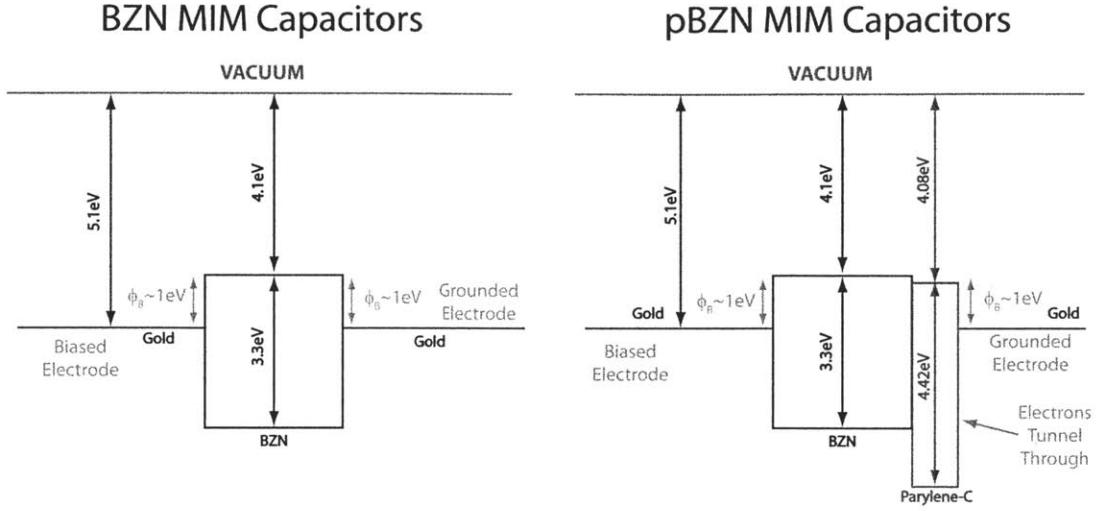
FIGURE 7-18: Energy band diagrams for BZN and pBZN MIM capacitors based on extracted barrier heights and the electron affinity model [22, 23]. Drawing NOT TO SCALE

Electrical Behavior After Breakdown

The measurements from TDDB from Figure 7-12 suggest that the insulator can recover from breakdown. This implies that there is another conduction mechanism that is activated beyond a certain trap density and that the generated traps recover upon removal of the bias. TZDB and TDDB measurements show breakdown to occur at the approximately the same electric fields as summarized in Table 7.2. Therefore, the two stress tests are capturing the same breakdown mechanism or a change in conduction mechanisms.

TABLE 7.5: A summary of the breakdown results E_{BD} from TZDB and TDDB measurements

Dielectric Thickness	Surface	TZDB E_{BD} ($^{MV}/_{cm}$)		TDDB E_{BD} ($^{MV}/_{cm}$)	
400 nm	BZN	0.19($\pm$0.07)	-0.15($\pm$0.05)	0.25($\pm$0.07)	-0.18($\pm$0.05)
400 nm	pBZN	0.30($\pm$0.08)	-0.30($\pm$0.08)	0.35($\pm$0.06)	-0.35($\pm$0.08)
280 nm	BZN	0.20($\pm$0.04)	-0.16($\pm$0.03)	0.18($\pm$0.04)	-0.15($\pm$0.02)
280 nm	pBZN	0.26($\pm$0.06)	-0.20($\pm$0.04)	0.22($\pm$0.09)	-0.18($\pm$0.09)

Cho et al. attributed leakage in BZN to a trap assisted conduction in BZN of which was reduced using a multiple-phase composite oxide, MgO-BZN. The trap assisted conduction at higher fields was reported to be Frenkel-Poole conduction[3]. This supports the conclusion that the nondestructive conduction mechanism that dominates at higher fields may be related to a critical trap density generated in the insulator. Beyond the initial breakdown, it is difficult to extract the exact current-voltage dependence with these TZDB measurements. As BZN is known to have metallic Bi-rich phases when deposited at room temperature [27, 28], it is conceivable how these

phases can also contribute to a percolative trap assisted conduction mechanism, which is not destructive. Chapter 5 reported what appeared to be metallic inclusions on the surface of the BZN after deposition. Attributing breakdown to the activation of a trap assisted charge transport mechanism facilitated by ohmic conduction implies reversibility. Thus, one can describe breakdown in room temperature sputtered BZN as a change in dominant conduction mechanisms from Schottky at low electric fields and small trap densities to a percolative mechanism enabled by trap generation beyond a critical value. From a device design perspective, neither type of breakdown (destructive or non-destructive) is tolerable.

7.6 CONCLUSION

From these stress studies it has been shown how BZN can serve as an effective insulator for pentacene-based TFTs. Results showed the current-voltage behavior of all insulators to depend slightly on stress polarity, though not significant when compared with the variation across similar capacitors. Traps are generated with a low applied voltage which ultimately leads to a reversible soft breakdown. TDDB and TZDB stress tests show the BZN insulator to breakdown at electric fields larger than 0.1 MV/cm which agrees with that reported for similar films by Cho et al [3]. The pBZN (surface modified BZN) films showed better breakdown strength at 0.3 MV/cm. For a 400 nm film, the breakdown voltage is >7 V for the BZN insulator while for the pBZN insulator the breakdown voltage is >12 V. This indicates that OTFTs made from similar films are unstable beyond a drain-to-source voltage of 10V which confirms the instabilities and leakage reported in the devices and circuits based on these insulators in Chapter 6. More compelling, TZDB and TDDB breakdown studies suggest that the trap densities generated as a result of an applied voltage or current are a better indicator of breakdown as opposed to electric field. The trap density created enables and mediates a temporary percolative conduction mechanism. This is similar to reports from ultra-thin SiO_2 and HfO_2 insulators. A conservative estimate for a threshold trap density generated for such breakdown is 1.5×10^{17} cm^{-3}. From temperature dependent measurements the barrier heights for Schottky emission are extracted to be 1 eV for BZN and pBZN on Au. From this value and energy band level for BZN, pentacene, ZnO, and Au reported in the literature [3, 29, 30, 31, 32], quantitative band diagrams are proposed for this system.

7.7 SUMMARY

This is a brief summary of the findings in this chapter.

Dielectric Constant

- 352 capacitors were evaluated for this investigation.
- Dielectric constant for this system is 40 with a variation of about 5%.

- For the capacitors used in these investigations, the parylene-C modified the dielectric constant within the variability seen in capacitors with one type of insulator. From a practical perspective, parylene-C does not modify the dielectric constant.

Stress Testing: General Observations

In regards to the OTFTs built and discussed in Chapter 6, electric integrity of the BZN must not be compromised at -5 V.

- Devices under positive bias broke down at larger stressing voltages compared to a negative bias.

- pBZN devices broke down at larger stressing voltages compared to BZN devices.

- The 280 nm dielectric broke down just below 5 V while the 400 nm dielectric broke down beyond 5 V.

- For this technology, the key to robustness is using a thicker (400 nm) dielectric and using the parylene-C surface treatment where possible in integrated MIM structures.

Time-Dependent Dielectric Breakdown

- The forcing voltage evolves with constant current stressing via the theory set for by Suñé et al. This suggests TDDB stress measurements are valid for evaluating reliability in BZN.

- Breakdown occurs via trap generation which may be a better predictor of dielectric failure than electric field.

- Initial breakdown is not fatal and another conduction mechanism is suspected to dominate beyond a critical trap density that has been generated during stressing.

- The conduction mechanism beyond the initial breakdown is suspected to be trap assisted, perhaps Frenkel-Poole, according to Cho et al.

Time-Zero Dielectric Breakdown

- Results from these test agreed with results from TDDB measurements

- Conduction through films occurs via Schottky emission before breakdown.

- The extracted barrier height for BZN on Au is ~ 1 eV.

7.8 REFERENCES

[1] M.-H. Lim, K. Kang, H.-G. Kim, I.-D. Kim, Y. Choi, and H. L. Tuller, "Low leakage current-stacked $MgO/Bi_{1.5}Zn_{1.0}Nb_{1.5}O_{7.0}$ gate insulator— for low voltage ZnO thin film transistors," *Applied Physics Letters*, vol. 89, no. 20, pp. 202908–3, 2006.

[2] I. D. Kim, M. H. Lim, K. Kang, H. G. Kim, and S. Y. Choi, "Room temperature fabricated ZnO thin film transistor using high-κ $Bi_{1.5}Zn_{1.0}Nb_{1.5}Oi_{7.0}$ gate insulator prepared by sputtering," *Applied Physics Letters*, vol. 89, no. 2, p. 3, 2006.

[3] N. G. Cho, H. Seo, D. H. Kim, H.-G. Kim, J. Kim, and I.-D. Kim, "Characterization on bandedge electronic structure of MgO added $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_{7.0}$ gate dielectrics for ZnO-thin film transistors," *Electrochemical and Solid-State Letters*, vol. 14, no. 1, pp. G4–G7.

[4] H. Takashi, *Gate dielectrics and MOS ULSIs: principles, technologies, and applications.*

[5] C. Kim, S. Jo, S. Lee, W. Kim, H. Baik, and S. Lee, "Surface-Modified High-κ Oxide Gate Dielectrics for Low-Voltage High-Performance Pentacene Thin-Film Transistors," *Advanced Functional Materials*, vol. 17, no. 6, pp. 958–962, 2007.

[6] Y. Choi, I. D. Kim, H. L. Tuller, and A. I. Akinwande, "Low-voltage organic transistors and depletion-load inverters with high-κ pyrochlore BZN gate dielectric on polymer substrate," *IEEE Transactions on Electron Devices*, vol. 52, no. 12, pp. 2819–2824, 2005.

[7] J. Suñé, I. Placencia, N. Barniol, E. Farrs, and X. Aymerich, "Degradation and Breakdown of Gate Oxides in VLSI Devices," *physica status solidi (a)*, vol. 111, no. 2, pp. 675–685, 1989.

[8] C. Silvestre and J. R. Hauser, "Time dependent dielectric breakdown measurements on RPECVD and thermal oxides," *Journal of The Electrochemical Society*, vol. 142, no. 11, pp. 3881–3889, 1995.

[9] A. Berman, "Time-Zero Dielectric Reliability Test by a Ramp Method," in *Reliability Physics Symposium, 1981. 19th Annual*, pp. 204 –209, april 1981.

[10] A. Martin, P. O'Sullivan, and A. Mathewson, "Dielectric Reliability Measurement Methods: A Review," *Microelectronics Reliability*, vol. 38, no. 1, pp. 37 – 72, 1998.

[11] J. Robertson, "Band offsets of wide-band-gap oxides and implications for future electronic devices," *Journal of Vacuum Science Technology B: Microelectronics and Nanometer Structures*, vol. 18, pp. 1785 –1791, may 2000.

[12] K. Okada, H. Ota, T. Nabatame, and A. Toriumi, "Dielectric Breakdown in High-κ Gate Dielectrics - Mechanism and Lifetime Assessment," in *45th annual. IEEE International Reliability physics symposium*, pp. 36 –43, april 2007.

[13] Y. H. Kim, K. Onishi, C. S. Kang, H.-J. Cho, R. Nieh, S. Gopalan, R. Choi, J. Han, S. Krishnan, and J. Lee, "Area dependence of TDDB characteristics for HfO_2 gate dielectrics," *IEEE Electron Device Letters*, vol. 23, pp. 594 –596, oct. 2002.

[14] J. Suñé, E. Wu, D. Jimenez, R. Vollertsen, and E. Miranda, "Understanding soft and hard breakdown statistics, prevalence ratios and energy dissipation during breakdown runaway," in *Electron Devices Meeting, 2001. IEDM Technical Digest. International*, pp. 6.1.1 –6.1.4, 2001.

[15] M. Houssa, T. Nigam, P. W. Mertens, and M. M. Heyns, "Model for the current voltage characteristics of ultrathin gate oxides after soft breakdown," *Journal of Applied Physics*, vol. 84, pp. 4351 –4355, oct 1998.

[16] R. Degraeve, G. Groeseneken, R. Bellens, M. Depas, and H. Maes, "A consistent model for the thickness dependence of intrinsic breakdown in ultra-thin oxides," in *Electron Devices Meeting, 1995., International*, pp. 863 –866, dec 1995.

[17] K. Cheung, "Ultrathin gate-oxide breakdown-reversibility at low voltage," *IEEE Transactions on Device and Materials Reliability*, vol. 6, pp. 67 – 74, march 2006.

[18] X. Wu, K. L. Pey, G. Zhang, P. Bai, X. Li, W. H. Liu, and N. Raghavan, "Electrode material dependent breakdown and recovery in advanced high-κ gate stacks," *Applied Physics Letters*, vol. 96, pp. 202903 –202903-3, may 2010.

[19] M. Dawber, K. M. Rabe, and J. F. Scott, "Physics of thin-film ferroelectric oxides," *Reviews of Modern Physics*, vol. 77, no. 4, pp. 1083–1130, 2005.

[20] P. R. Emtage and W. Tantraporn, "Schottky emission through thin insulating films," *Physical Review Letters*, vol. 8, no. 7, pp. 267–268, 1962.

[21] S. M. Sze and K. K. Ng, "Metal-insulator-semiconductor capacitors," in *Physics of Semiconductor Devices*, pp. 197–240, John Wiley and Sons, Inc., 2006.

[22] R. Anderson, "Experiments on Ge-GaAs heterojunctions," *Solid-State Electronics*, vol. 5, no. 5, pp. 341 – 351, 1962.

[23] W. A. Harrison, "Elementary theory of heterojunctions," *Journal of Vacuum Science and Technology*, vol. 14, pp. 1016 –1021, jul 1977.

[24] P. W. Peacock and J. Robertson, "Band offsets and schottky barrier heights of high dielectric constant oxides," *Journal of Applied Physics*, vol. 92, no. 8, pp. 4712–4721, 2002.

[25] I.-D. Kim, Y. Choi, and H. L. Tuller, "Low-voltage ZnO thin-film transistors with high-κ $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ gate insulator for transparent and flexible electronics," *Applied Physics Letters*, vol. 87, no. 4, p. 043509, 2005.

[26] N. G. Cho, D. H. Kim, H.-G. Kim, J.-M. Hong, and I.-D. Kim, "Zinc oxide thin film transistors using MgO-$Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ composite gate insulator on glass substrate," *Thin Solid Films*, vol. 518, no. 10, pp. 2843 – 2846, 2010.

[27] J. H. Park, W. S. Lee, N. J. Seong, S. G. Yoon, S. H. Son, H. M. Chung, J. S. Moon, H. J. Jin, S. E. Lee, J. W. Lee, H. D. Kang, Y. K. Chung, and Y. S. Oh, "Bismuth-zinc-niobate embedded capacitors grown at room temperature for printed circuit board applications," *Applied Physics Letters*, vol. 88, no. 19, 2006.

[28] H. Qiao, X. Yao, and S. Ding, "Studies on dielectric relaxation and high temperature conductivity of $Bi_{1.5}Zn_{1-x}Nb_{1.5}O_{7-x}$ ceramics," *Journal of Electroceramics*, vol. 21, no. 1, pp. 444–447, 2008.

[29] K. Sudheendran, M. Ghanashyam Krishna, and K. Raju, "Effect of process parameters and post-deposition annealing on the microwave dielectric and optical properties of pulsed laser deposited $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ thin films," *Applied Physics A: Materials Science and Processing*, vol. 95, no. 2, pp. 485–492, 2009.

[30] M. Kitamura and Y. Arakawa, "Pentacene-based organic field-effect transistors," *Journal of Physics-Condensed Matter*, vol. 20, no. 18, 2008.

[31] S. Gowrisanker, M. A. Quevedo-Lopez, H. N. Alshareef, and B. E. Gnade, "Time dependent breakdown characteristics of parylene dielectric in metal insulator metal capacitors," *Organic Electronics*, vol. 10, no. 5, pp. 1024–1027, 2009.

[32] S. Hasegawa, S. Nishida, T. Yamashita, and H. Asahi, "Field electron emission from polycrystalline GaN nanorods," *Journal Of Ceramic Processing Research*, vol. 6, no. 3, pp. 245–249, 2005.

Chapter 8

High Voltage Organic Thin Film Transistors

8.1 MOTIVATION and STATE of the ART

A transistor is a switch. Though the most common design goals of a TFT are to minimize power consumption while switching at very high speeds, the fundamental purpose of the transistor is to switch current on or off. TFTs are widely used for pixel addressing in large-area flat-panel displays. However, many applications require drive voltages (V_{DD}) larger than 100 V, which is beyond the typical operating range of conventional TFTs. Among these applications are ferroelectric liquid crystals, electrophoretic or PLZT electrooptic displays electrographic plotters [1, 2], digital x-ray imaging [3, 4], poly-Si cold cathodes [5], and MEMS [6].

A typical TFT is not suitable for high voltage applications. The gate insulator will fail or breakdown when integrity of the dielectric is compromised by large electric fields. Gate breakdown can be attributed to a number of different physical phenomena that become active at high fields. These include by are not limited to basic dielectric breakdown similar to Time-Zero Dielectric Breakdown that was discussed in Chapter 7 and the impingement of energetic carriers on the gate insulator or hot carrier injection. To minimize these deleterious physical phenomena and still achieve high voltage switching, the TFT structure must be modified to allow the switching of very large drain-to-source voltages ($V_{DD} \geq 300V$) while maintaining a low controlling voltage ($V_G \leq 20V$).

PRINCIPLE OF OPERATION One way to increase the drain-to-source driving voltage and/or electric field across the channel in an FET is to place a resistive structure
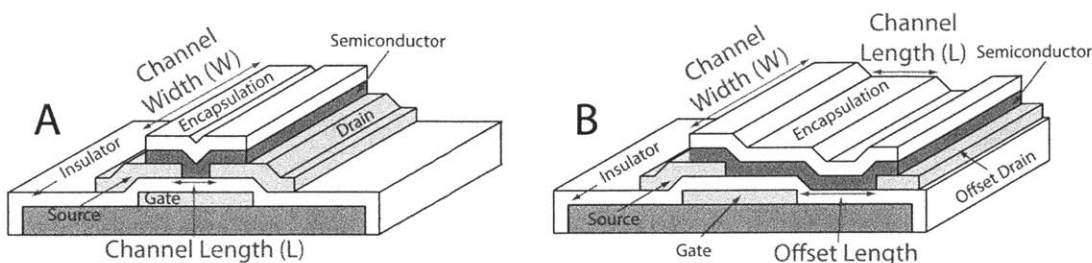
FIGURE 8-1: Comparing the structures of a TFT(A) and an HVTFT (B) with the offset by the drain.

between the drain or source electrode and the gated channel. For this work, high driving voltages are achieved by offsetting the drain or source electrode from the gate. This creates an ungated semiconductor region (resistive structure) in series with a gated semiconductor region. The saturation current ($I_{D,sat}$) through the devices is controlled by the gated semiconductor region which limits the voltage dropped across (and electric field) the gated region. The excess voltage is dropped across the ungated semiconductor enabling high voltage operation. Therefore, the offset or ungated semiconductor region is necessary for high voltage operation. Without the offset, the gate dielectric will fail at high voltages which restricts the maximum attainable switchable voltage. Figures 8-1 compares the cross sections of a standard TFT structure to that of an HVTFT with an offset at the drain.

In this dissertation, high voltage organic thin film transistors (HVOTFT) based on pentacene are demonstrated, giving rise to MEMS devices that are compatible with flexible substrates. Such an innovation widens the applicability for traditional MEMS and related applications. As MEMS devices span a large range of applications, it is necessary to show how the electrical parameters of the HVOTFT can be engineered to meet the demands of different applications requiring high voltage switching.

The aim of this work is to demonstrate that organic semiconductors are viable in HVTFTs, they operate similarly to a-Si HVTFTs, and they can be described with the FET models developed for Si-based short channel devices. For high voltage applications, it is necessary to control large drain-to-source voltages (V_{DD}) with small gate-to-source voltages (V_G) and/or create large currents to quickly charge and discharge capacitive MEMS. The goal is to show that the threshold voltage (V_T) and drive current (I_D) can be engineered through surface treatments [7] and high-κ insulators [8] and explore the issues that arise as a consequence of the high voltage operation. Three different gate insulators will be evaluated for HVOTFTs in this work, parylene-C (PAR), O_2 plasma treated parylene-C (O_2 PAR), and a composite stack consisting of parylene-C and BZN (PAR/BZN). PAR is room temperature deposited parylene-C and will serve as a standard insulator for OTFTs. Reducing V_T is achieved
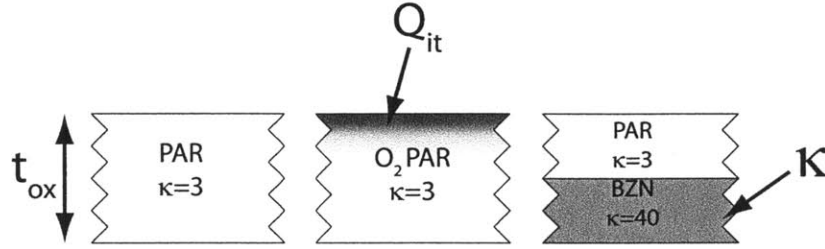
188

FIGURE 8-2: Illustration of the three insulators studied for High Voltage Organic Thin Film Transistors

by treating parylene-C with O_2 plasma (O_2 PAR) which changes Q_{it} in Equation 8.1 and was shown to be affective by Wang et al [7]. To increase drive currents (I_D) and reduce V_T, a composite insulator stack of parylene-C and BZN ($Bi_{1.5}Zn_{1.0}Nb_{1.5}O_{7.0}$) (PAR/BZN) is used to combine the high dielectric constant (κ in Equation 8.1) of BZN with the high breakdown resistance of parylene-C (2-4 MV/cm).

$$V_T = (\phi_M - \phi_S) \ - \frac{t_{OX}}{\epsilon_o \kappa}(Q_{it} - Q_{OX}) \tag{8.1}$$

Where,

ϕ_M and ϕ_S: work functions of the gate metal and the semiconductor

ϵ_o: permittivity of free space

κ: dielectric constant of the insulator

Q_{it}: surface charge density at the interface between insulator and the semiconductor.

$Q_{OX} := \int_0^{t_{OX}} \frac{t}{t_{ox}}\rho_{OX}(t) \cdot \mathrm{d}t$

ρ_{OX}: charge density per unit volume in the insulator

t_{OX}: thickness of the insulator

8.2 ELECTRICAL CHARACTERIZATION of TFTS

Before characterizing HVOTFTs, conventional TFTs are made to assess the suitability of each insulator for switching and high voltage stability. In this section, the parameters of discreet OTFTs that are fabricated using the materials presented in Chapter 2 and fabrication processes presented in Chapters 4 and 5. Electrical characteristics were taken with an Agilent 4156C Semiconductor Parameter Analyzer in the dark at room temperature. Functional OTFTs where fabricated from the insulators described above.

8.2.1 Raw Data, Extracted Parameters, and Observations

Output Characteristics

Output characteristics for OTFTs based on these three insulators are shown in Figure 8-3. V_{GS} is stepped from 0 to -20 V in -5 V increments while V_{DS} is swept from 0 to

FIGURE 8-3: Output Characteristics for OTFTs with PAR, O_2 PAR and, PAR/BZN insulators. The channel width (W)=500 μm and the channel length (L)=10 μm. V_{GS} is stepped from 0 to -20 V in -5 V increments while V_{DS} is swept from 0 V to -20 V in -0.5 V increments

-20 V in -0.5 V increments.

Transfer Characteristics

Transfer Characteristics for OTFTs based on these three insulators are shown in Figure 8-4. Table 8.1 is a summary of extracted device parameters. The V_{DS} is stepped from -5 V to -20 V in -5 V increments while V_{GS} is swept from 20 V to -20 V in -0.25 V increments.
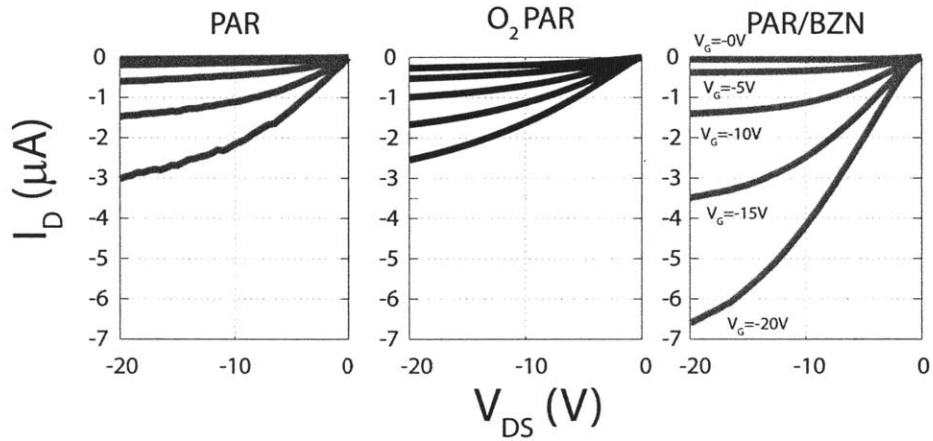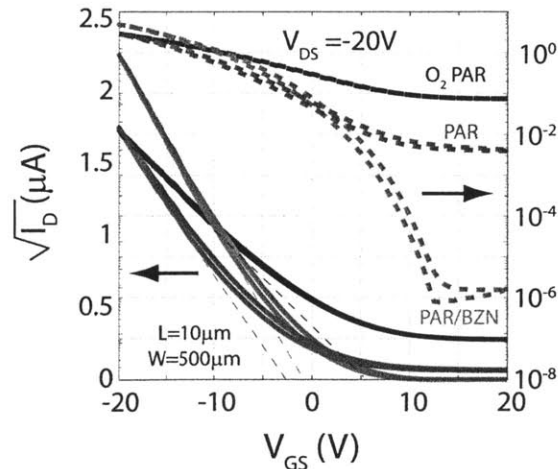

FIGURE 8-4: Transfer Characteristics for OTFT with PAR, O_2 PAR and, PAR/BZN insulators. The channel width (W)=500 μm and the channel length (L)=10 μm. V_{DS} is stepped from -5 V to -20 V in -5 V increments while V_{GS} is swept from 20 V to -20 V in -0.25 V increments.

TABLE 8.1: Summary of device parameters for PAR, O_2 PAR, and PAR/BZN based OTFTs. Parameters are extracted at $V_{GS} = -17.5V$ and $V_{DS} = -20V$. I_D is extracted at V_{GS} and V_{DS} =-20 V

PARAMETERS	PAR	O_2 PAR	PAR/BZN
Ox Thick (nm)	500	350	200/200
κ	3	3	[1]6
Semi. Thick (nm)	20	40	20
[2]V_T^{SLCMM} (V)	-1.7	5.4	-0.24
[3]V_T^{SLR} (V)	-10.6	-14.4	1.0
μ (cm^2/Vs)	0.068	0.023	0.014
S (V/dec)	9.8	18.3	2.3
S_{ID} (V/dec)	0.117	0.116	0.106
D_{it} (cm^2/eV)	5.38E+12	1.51E+13	8.62E+12
I_D (μA)	3	2.5	6.5

[1]Dielectric constant is calculated using:

$$\frac{t_{BZN} + t_{par}}{\dfrac{t_{BZN}}{\kappa_{BZN}} + \dfrac{t_{par}}{\kappa_{par}}} = \kappa_{eff,idl}$$

[2]Si Long Channel MOSFET Model
[3]Subthreshold Linear Regression

8.2.2 Discussion: Figures of Merit and Effects of Integration

Threshold Voltage

The PAR and O_2 PAR based OTFTs have a high "off" current. This leakage may be in the result of a back channel in the semiconductor or incomplete patterning of the semiconductor layer. Such leakage appears minimally disruptive to transistor operation and appears to only impact the "off" behavior. The V_T^{SLR} is affected by this leakage showing large a value. Thus, V_T^{SLCMM} is likely a more accurate value for a practical threshold voltage. Compared to the PAR device, the threshold voltage (V_T^{SLCMM}) shifts positive for the O_2 PAR and PAR/BZN based OTFTs. As the O_2 plasma is a surface treatment it is assumed that dielectric constant is not affected. Therefore the shift in V_T for the O_2 PAR based OTFT is due to negative charges trapped on the surface as a result of the treatment [7]. As the semiconductor/insulator surface is the same for the PAR/BZN and PAR based OTFTs, the decrease in V_T is due to the increased dielectric constant of the PAR/BZN insulator. The dielectric constant for PAR/BZN is twice as large as parylene-C. Accordingly, the current (I_D) is twice as large for the PAR/BZN based OTFTs compared to the PAR based OTFTs. This can be seen in Table 8.1.
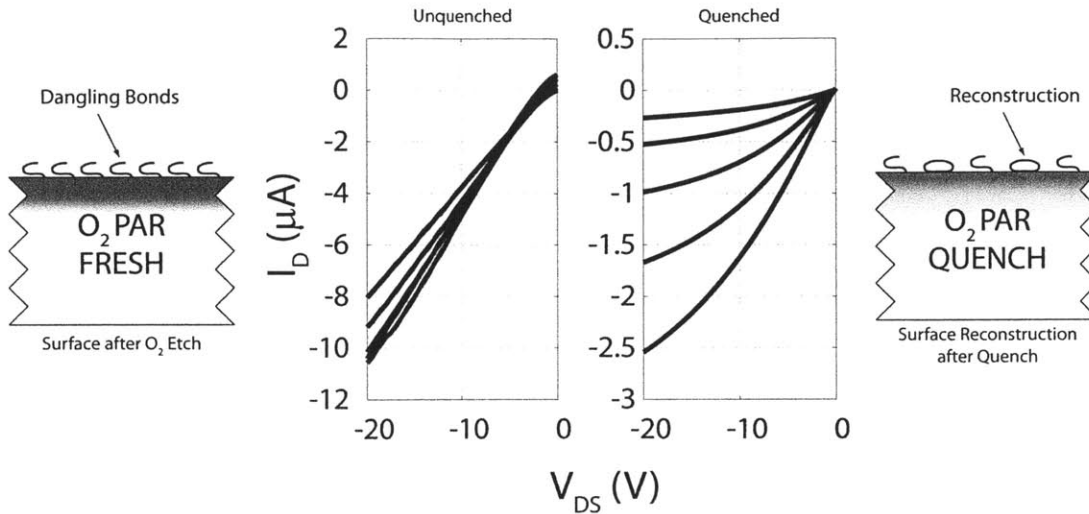
191

FIGURE 8-5: Output characteristics comparing unquenched O_2 plasma and acetone quenched O_2 plasma. The channel width (W)=500 μm and the channel length (L)=10 μm. Reconstruction of dangling bonds comparing unquenched O_2 plasma and acetone quenched O_2 plasma.

O_2 PAR DEVICES AND QUENCHING For the O_2 PAR based OTFTs, the surface is exposed to acetone during the resist strip after the O_2 plasma surface treatment patterning. This exposure to acetone or any other resist stripping solvents is unavoidable. The acetone in this case "quenches" the reactive surface before semiconductor deposition effectively reconstructing dangling bonds created by the O_2 plasma. Figure 8-5 shows the differences in device Output Characteristics between quenched and unquenched devices. The unquenched devices behave more like resistors suggesting that an overwhelming amount of interface charges are dictating transport properties. This is supported by the high surface energy of the unquenched surface (79 mN/m) relative to the quenched surface (45 mN/m), as reported in Chapter 5. In this case, the solvent quenching is beneficial and necessary for functional OTFTs.

Mobility
The mobility for the OTFTs fabricated from these three insulators are comparable and within the same order of magnitude. Differences can be attributed to varying processing conditions for each wafer.

TEMPERATURE AND O_2 PLASMA Figure 8-6 shows that the heat generated from the bakeout during photolithography is detrimental to device performance, specifically lowering mobility. This decrease in mobility is attributed to the increase in the amount of bulk phase pentacene present as revealed in Chapter 5. There are other reports that heat treating or annealing pentacene degrades carrier mobility. Using a shorter baking time at high temperatures or a longer baking time at a lower temperature may
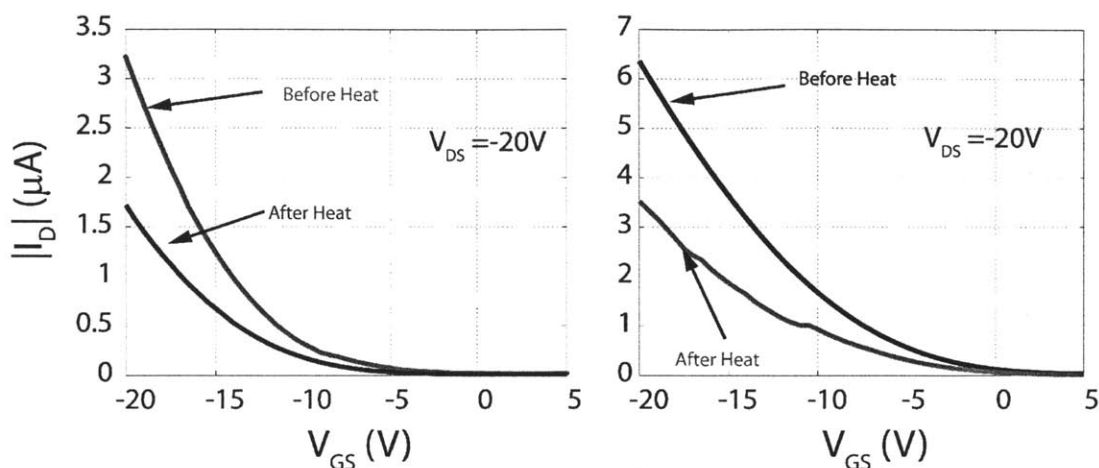
FIGURE 8-6: Mobility degrades as a result of the heating during photolithography on the PAR and O$_2$ PAR surfaces. Channel Width (W)=500 μm Channel Length (L)=5 μm.

be a solution [9, 10, 11]. Further, using a photoresist that does not require baking may also minimize this degradation, however the heat generated in the O$_2$ plasma etch is unavoidable. Last, though not investigated in this work, the O$_2$ plasma etch itself may detrimental to device performance [12].

Subthreshold Swing (S)

The PAR and O$_2$ PAR based OTFTs have a large subthreshold swing indicating less than optimal gate control or parasitic leakage. In the case of the PAR based OTFTs, the relatively thick insulator (t_{OX}=500 nm) used for the gate insulator in order to obtain high voltage operation and reliability is a likely source. In essence, V_{GS} and V_{DS} are competing for control of the charge in the channel. When V_{DS} begins to dominate charge transport in the channel (less gate control), the device looks more resistor-like as in the case with the PAR based OTFTs.

The O$_2$ PAR based OTFTs have a large subthreshold swing even with t_{OX}=350 nm. This implies that is a parasitic leakage path somewhere in the device. As 40 nm of pentacene was used for these devices, the leakage may be in the back channel or due to a residual layer of pentacene as a result of incomplete patterning. Such leakage appears to be minimally disruptive to transistor operation and appears to only impacts the "off" behavior.

Transfer Characteristics show a small hysteresis in the PAR/BZN based OTFTs. This has been observed in other OTFTs employing both organic and inorganic gate materials [13, 14]. This is attributed to mobile charges at the insulator/semiconductor interface or bulk charges in the insulator. This suggests there is some trapping in the insulator but it does not lead to the breakdown of the gate insulators in these voltage

ranges. Specifically, Hwang et al. describes this trapping as "electrons which can be injected from gate electrode to a vulnerable dielectric and then trapped inside the dielectric." [14]. Similar organic/inorganic insulators stacks show charge trapping at the organic/inorganic interfaces [15, 14, 16].

Band Diagrams

To construct a equilibrium band diagram for the PAR and O_2 PAR and PAR/BZN based OTFTs, the states of the channel (accumulated or depleted) must be known at V_{GS}=0 V. The Output and Transfer Characteristics from the last section reveal the O_2 PAR based OTFTs to be accumulated at V_{GS}=0 V while the PAR and PAR/BZN based OTFTs are depleted at V_{GS}=0 V. For PAR and O_2 PAR and PAR/BZN insulators, there are interface states at the insulators/semiconductor interfaces. This will create a discontinuity in the electric field at this interface. The discontinuity will be determined by the magnitude and sign on the charges at the interface. More specifically, slope of the conduction or valence band in the insulators will not match the slope of the HOMO or LUMO level in the pentacene adjacent to the semiconductor/insulator interface. The Time-Zero Dielectric Breakdown measurements in Chapter 7 revealed the band offset between BZN and Au to be $\sim$1 eV. Last, literature reports the electronic properties (electron affinity, band gap, work function) of Au, BZN, parylene-C and pentacene as discussed in Chapter 2 and are illustrated in Figure 8-7. Knowing the state of the channel, band offsets, and fundamental electronic material properties, band diagrams for PAR, O_2 PAR, and PAR/BZN based OTFTs are qualitatively proposed in Figures 8-8, 8-9, and 8-10. With confirmation that the dielectrics are suitable for conventional OTFTs, HVOTFTs can be fabricated. Again, high voltage operation in enabled by offsetting the source and/or drain from the gate as shown in Figure 8-11.

VACUUM
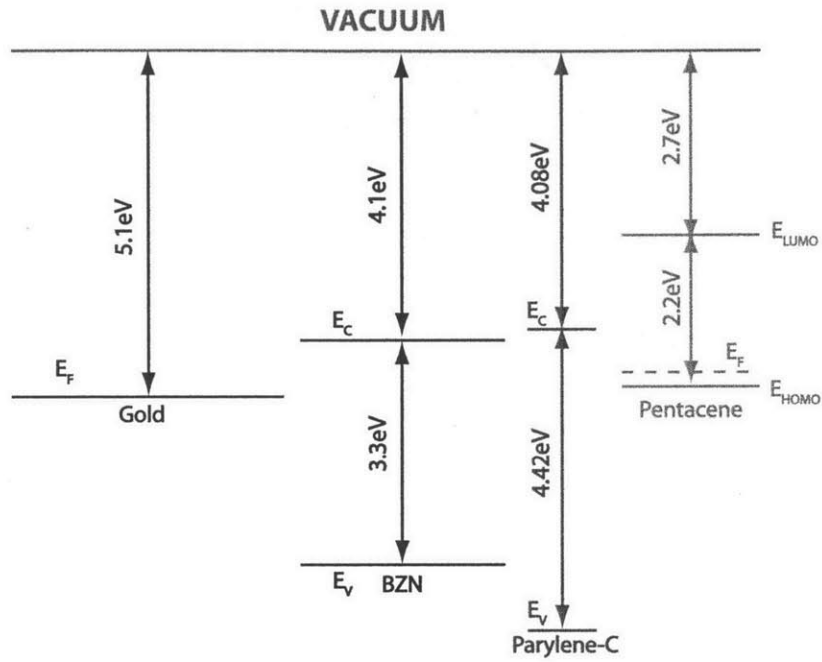
FIGURE 8-7: Energy band levels for Au, BZN, parylene-C, and pentacene

PAR MIS Structure

VACUUM
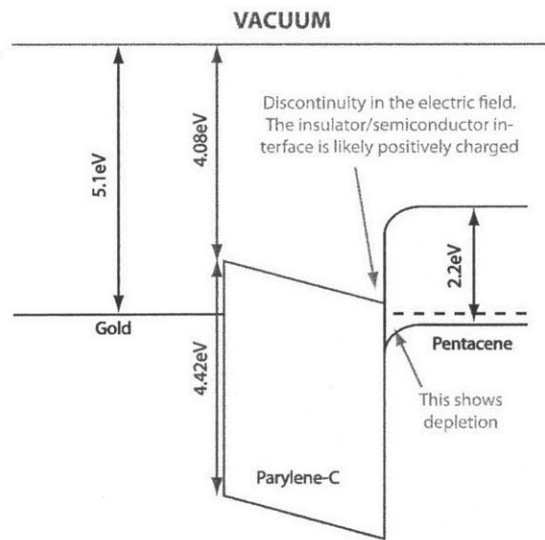

FIGURE 8-8: Band diagram of the PAR based MIS capacitors
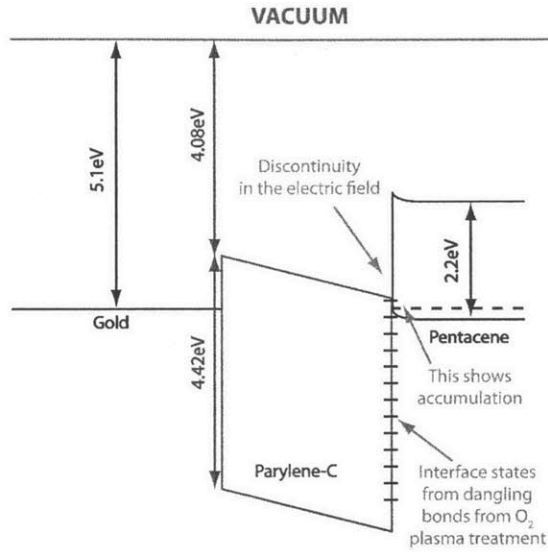
O$_2$ PAR MIS Structure

FIGURE 8-9: Band diagram of the O$_2$ PAR based MIS capacitors
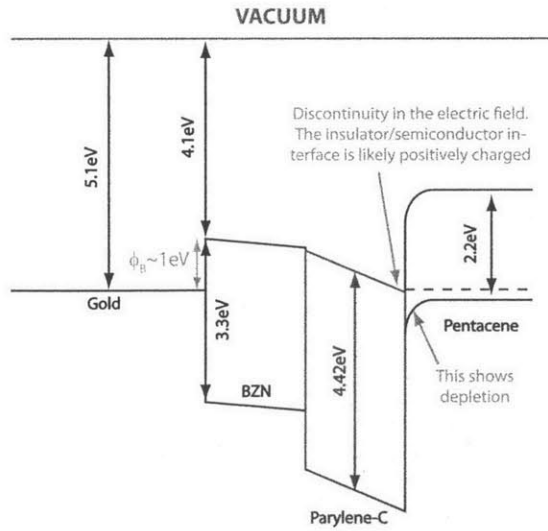
PAR/BZN MIS Structure

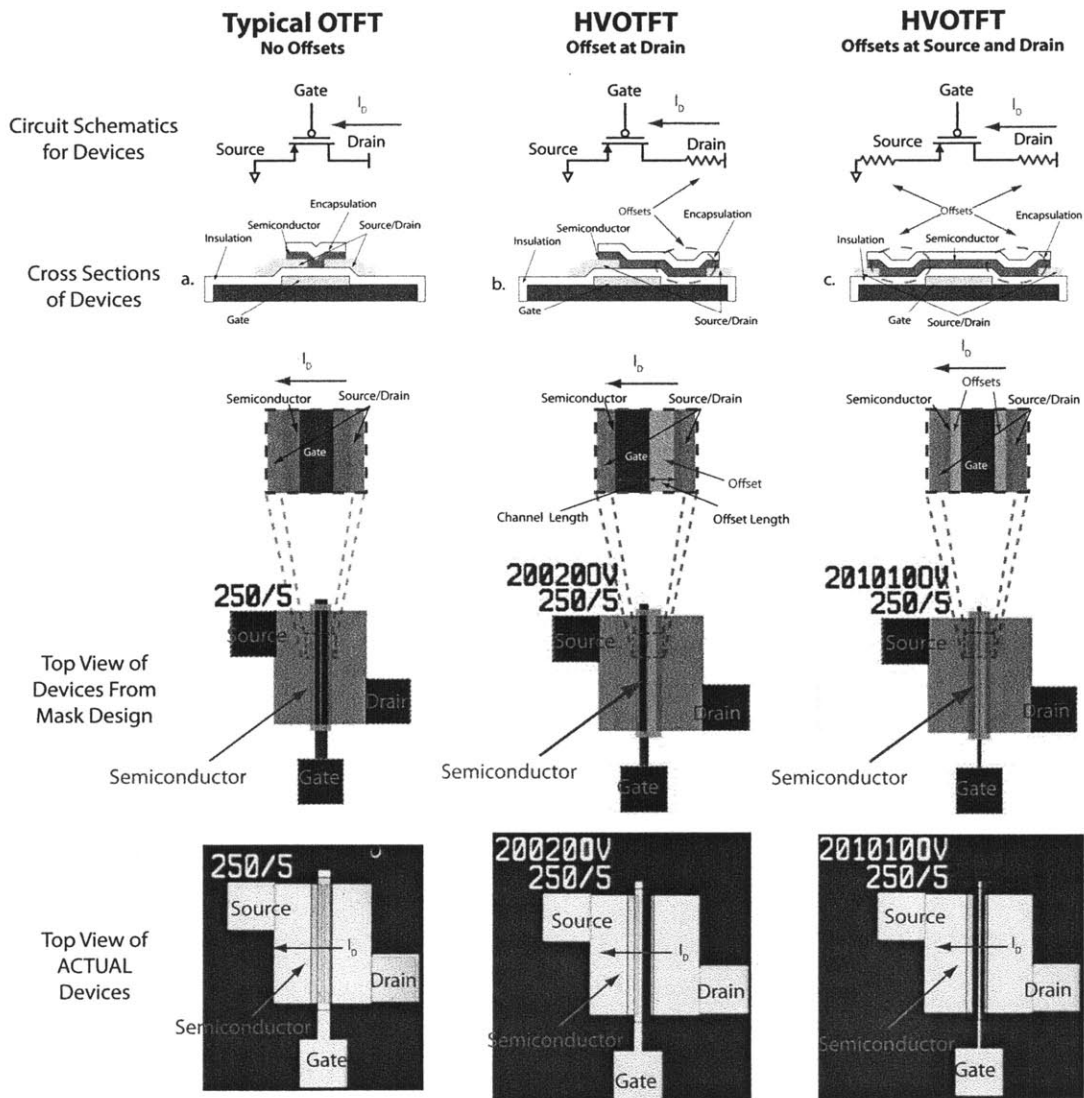FIGURE 8-10: Band diagram of the PAR/BZN based MIS capacitors

196

FIGURE 8-11: Circuit Schematics, Cross Sections and Top Views of devices illustrating the offset structure and locations in HVOTFTs

8.3 INTEGRATED CIRCUITS: HVOTFT

Though an HVOTFT appears to be a discreet device physically, it must be evaluated as a circuit where an OTFT is in series with resistors which represent the offsets (ungated semiconductor) at the source and/or drain as shown in Figure 8-11 and 8-12. The effective gate-to-source and drain-to-source voltages that are switching and driving the OTFT or gated semiconductor and the resulting drain current (I_D) must be modified to account the voltage dropped across the offsets. The expressions for these relations can be seen in Equations 8.2, 8.3, 8.4, and 8.5 which are modifications to the Si Long Channel MOSFET Model. The modifications account for the voltage that is dropped across the offsets taking the current through the offset and the resistance of the offset.
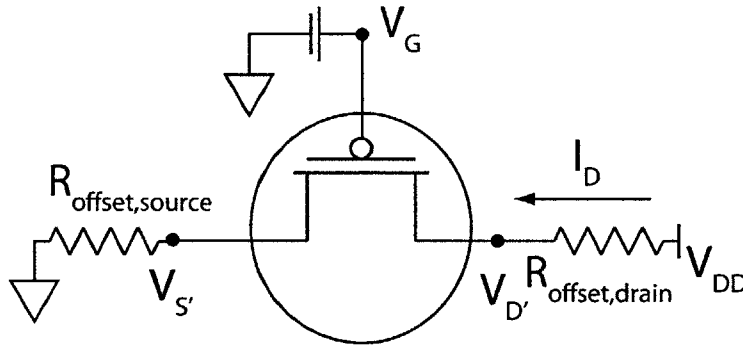
FIGURE 8-12: Effective circuit schematic for HVOTFT

$$V_{DS'} = V_{DD} - I_D R_{offset,drain} - I_D R_{offset,source} \qquad (8.2)$$

$$V_{GD'} = V_G - (V_{DD} - I_D R_{offset,drain}) \qquad (8.3)$$

$$V_{GS'} = V_G - I_D R_{offset,source} \qquad (8.4)$$

$$I_{D,sat,HV} = \frac{\mu C W}{2L} [V_G - V_T - (I_{D,sat,HV} R_{offset,source})]^2 \qquad (8.5)$$

Where,

V_{DD}: driving or supply voltage

$V_{DS'}$: effective drain-to-source voltage of the OTFT in the HVOTFT circuit

$V_{GD'}$: effective gate-to-drain voltage of the OTFT in the HVOTFT circuit

$V_{GS'}$: effective gate-to-source voltage of the OTFT in the HVOTFT circuit

V_G: voltage applied at the gate of the OTFT in the HVOTFT circuit. This is reference from ground.

$I_{D,sat,HV}$: Modified $I_{D,sat}$ accounting for offsets.

$R_{offset,source}$: Resistance of the offset that is located between the source of the OTFT and ground

$R_{offset,drain}$: Resistance of the offset that is located between the drain of the OTFT and V_{DD}

198
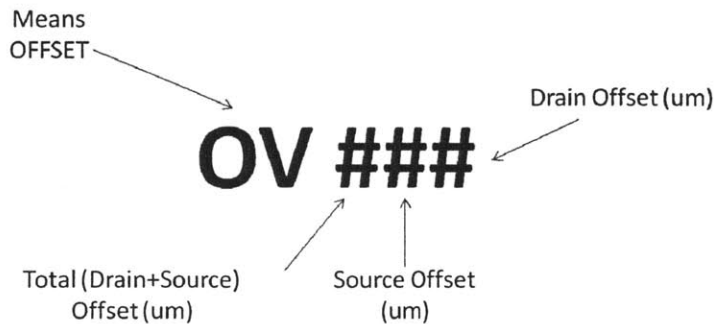
FIGURE 8-13: Naming convention for HVOTFTs
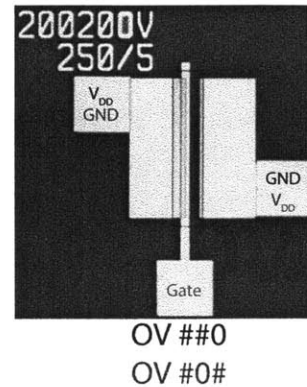
FIGURE 8-14: An illustration of how switching the source and drain probes to change the orientation of the offset

Clearly, there is an infinite number of possible source and drain offset size and location combinations. A naming convention has been adopted to clarify references to specific HVOTFT device structures. Devices are identified with a "OV###" format. "OV" implies offset. The offset is defined from the edge of the gate to the source or drain electrode as shown in Figures 8-1 and 8-11. The first number is the total offset. The second number is the size offset at the source; the third number is the size offset at the drain. Thus, the second number added to the third number equals the first number. All units are in microns (μm). Figure 8-13 describes this naming convention. Thus, for Figure 8-14, "20020OV" indicates a total of 20 μm of offset in the device, 0 μm at the source electrode and 20 μm at the drain electrode. For the asymmetric devices, the OV##0 structure is physically the same as the OV#0# structure. By switching the ground (GND) and supply voltage contacts, measurements for both the OV#0# structure and the OV##0 structure are obtained from one device.

8.3.1 Electrical Characterization and Discussion

LOW VOLTAGE SWEEPS: $V_{DD} \leq 100V$ Figures 8-15 through 8-20 show that these devices generally behave like conventional OTFTs at low voltages and show that the device follows the expected trends with the addition of the offsets. The standard device (no offsets, OV000) has the largest I_D and the devices with longest offsets have the smallest I_D in the reported voltage range. Placing and offset at the source has a more pronounced effect on I_D than placing an offset at the drain as predicted Equation 8.5. An offset at the source reduces the gate-to-source voltage ($V_{GS'}$) that drives the gated semiconductor region. A voltage V_G is applied to the gate however the actual voltage ($V_{GS'}$) that drives the gated region is less than V_G. This is a result of the offset at the source. This is expressed in Equation 8.4.
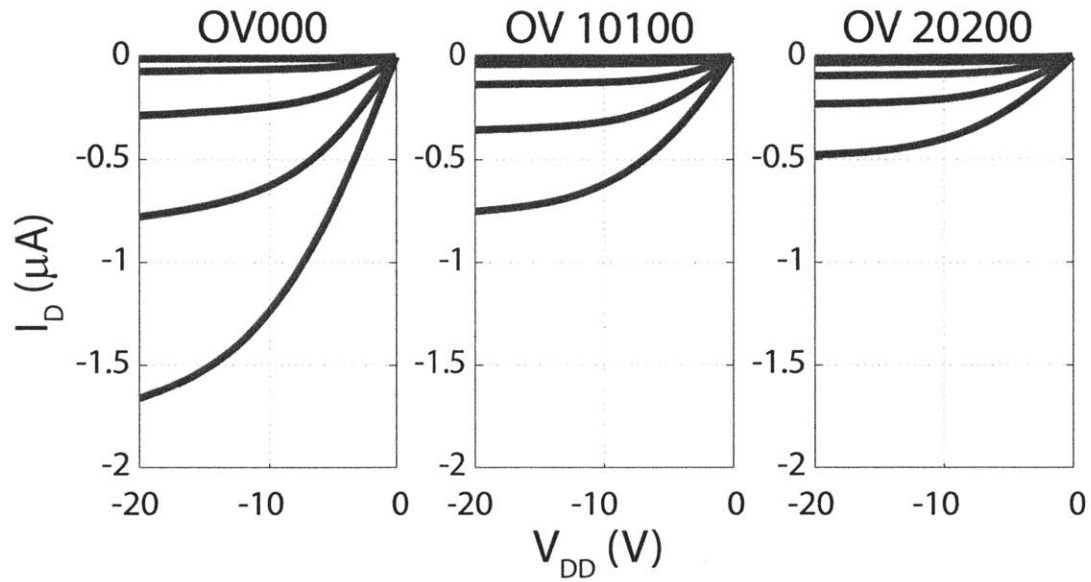
FIGURE 8-15: Output Characteristics of PAR based OTFTs with offsets at the source. The channel length (L)=5 μm and the channel width (W)=250 μm
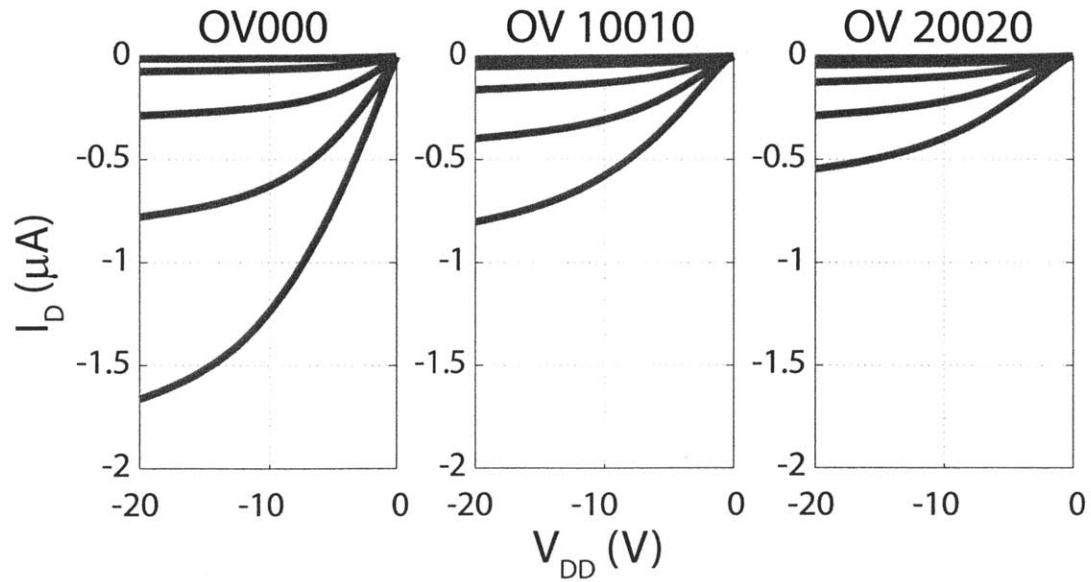
FIGURE 8-16: Output Characteristics of PAR based OTFTs with offsets at the drain. The channel length (L)=5 μm and the channel width (W)=250 μm
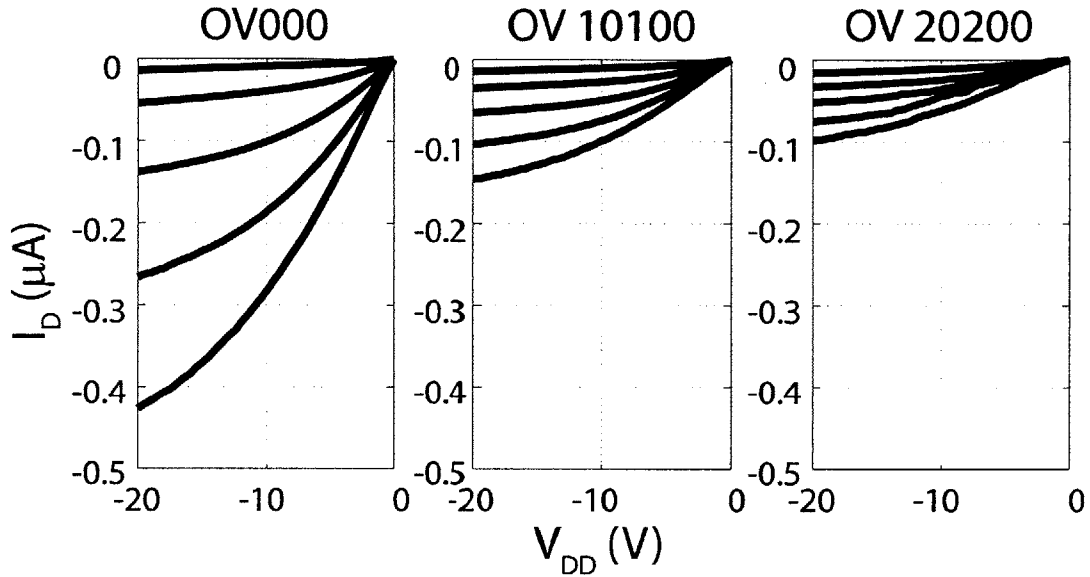
FIGURE 8-17: Output Characteristics of O_2 PAR based OTFTs with offsets at the source. The channel length (L)=5 μm and the channel width (W)=250 μm
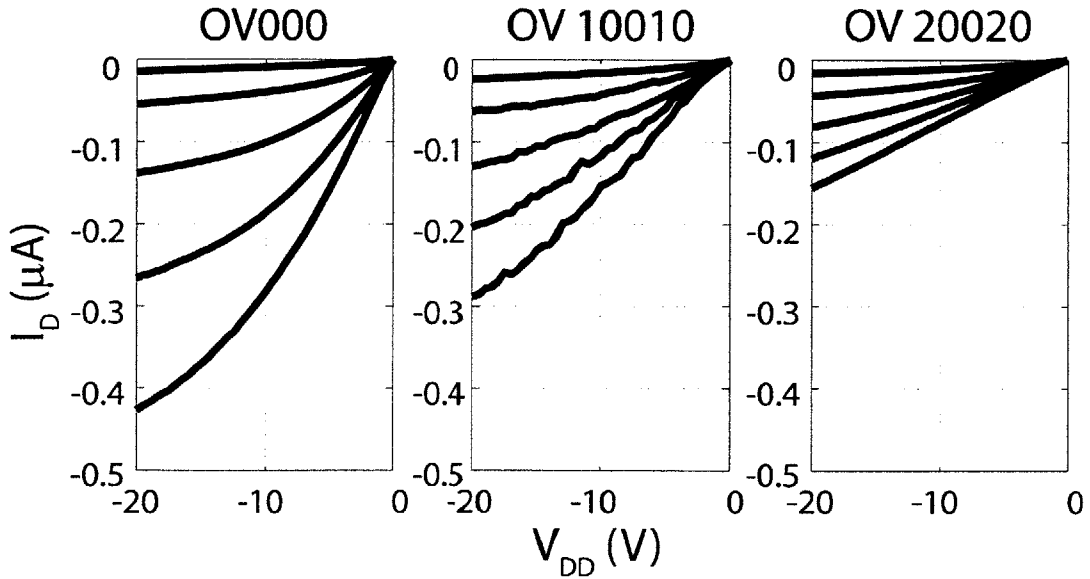
FIGURE 8-18: Output Characteristics of O_2 PAR based OTFTs with offsets at the drain. The channel length (L)=5 μm and the channel width (W)=250 μm

201
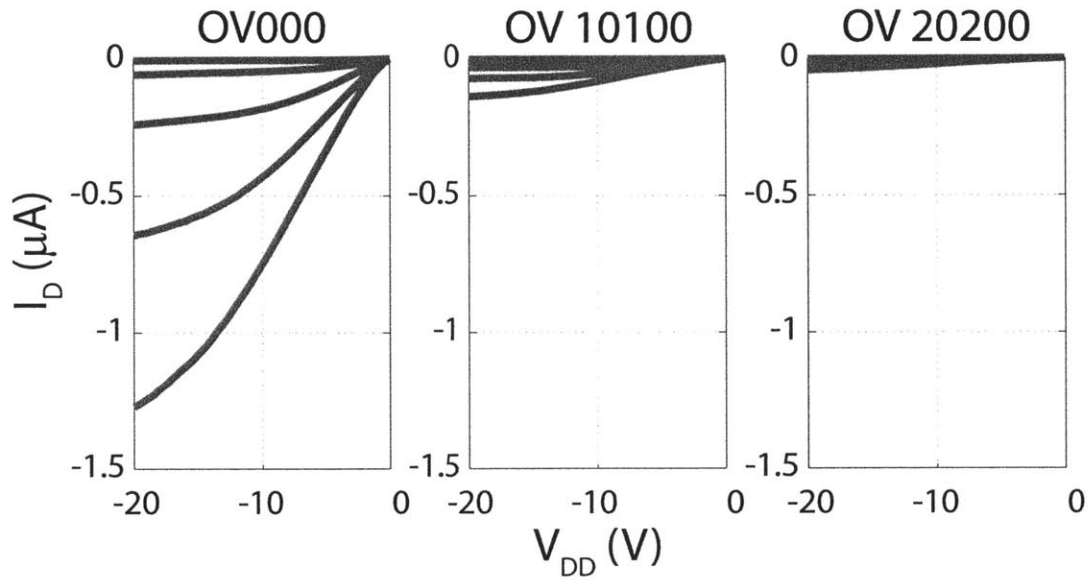
FIGURE 8-19: Output Characteristics of PAR/BZN based OTFTs with offsets at the source. The channel length (L)=5 μm and the channel width (W)=250 μm
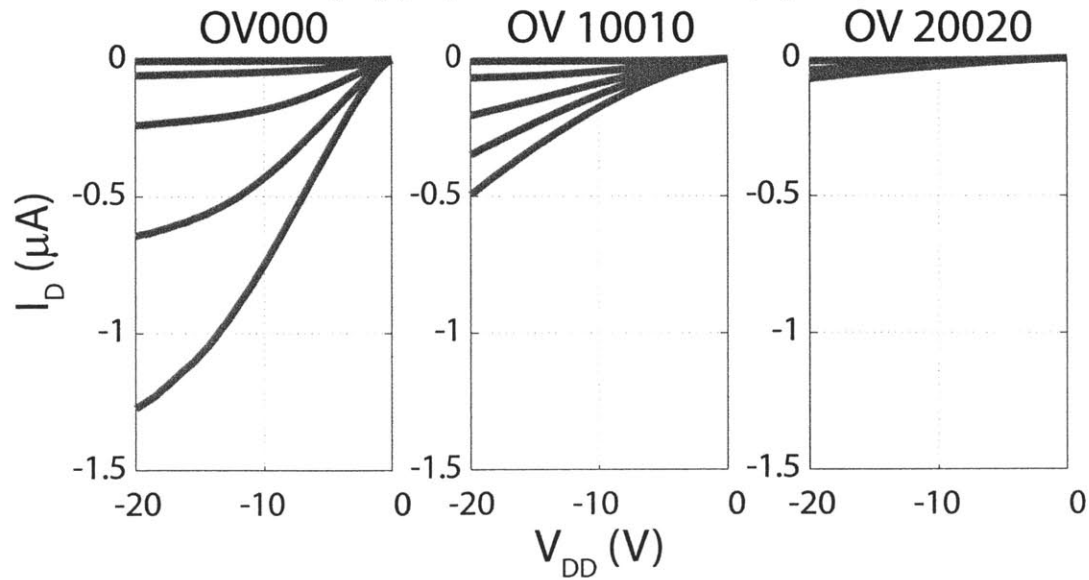
FIGURE 8-20: Output Characteristics of PAR/BZN based OTFTs with offsets at the drain. The channel length (L)=5 μm and the channel width (W)=250 μm
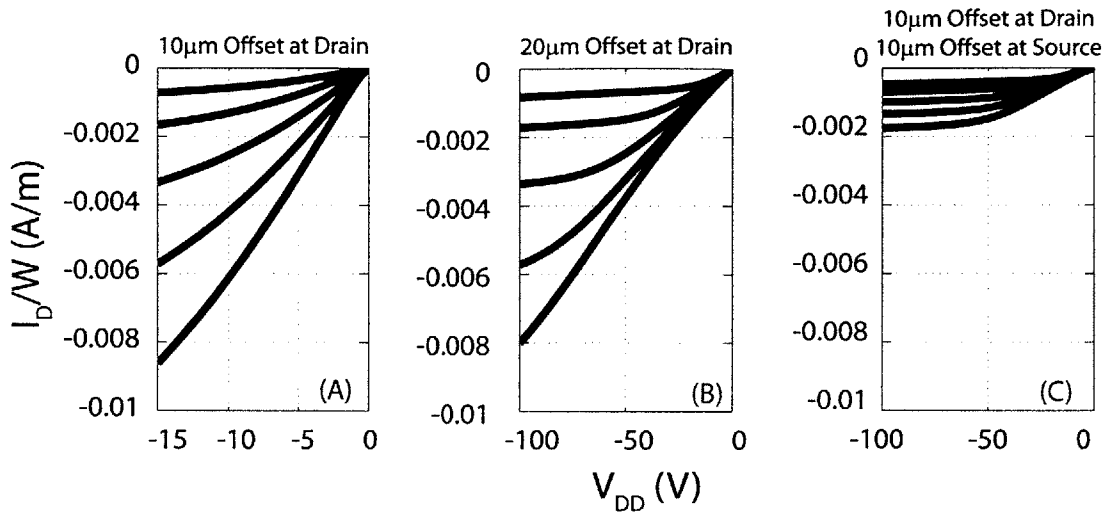
FIGURE 8-21: Output characteristics comparing $I_{D,sat}$ for different offset structures. The channel length (L)= 5μm for these O_2 PAR based OTFT and HVOTFTs.

When evaluating the impact of the location of the offset (at the source vs. the drain), Figure 8-21 shows how $I_{D,sat}$ is essentially the same for the device with no offset (A) compared to a device with an offset at the drain (B). It should be noted that a larger V_{DD} is required to reach $I_{D,sat}$ as shown in Figure 8-21(B). The device with the offset at the source and drain (C) has a lower $I_{D,sat}$, which again follows from Equation 8.5.

In regards to Transfer Characteristics, as the gate voltage increases the gated region becomes more conductive. Beyond a point, the offset will begin to dominate the IV behavior of the circuit as the gated regions become less resistive with the applied V_G. This shown in Figure 8-22. Therefore, the HVOTFT should not be used to extract threshold voltage (V_T), mobility (μ), or subthreshold swing (S).

203
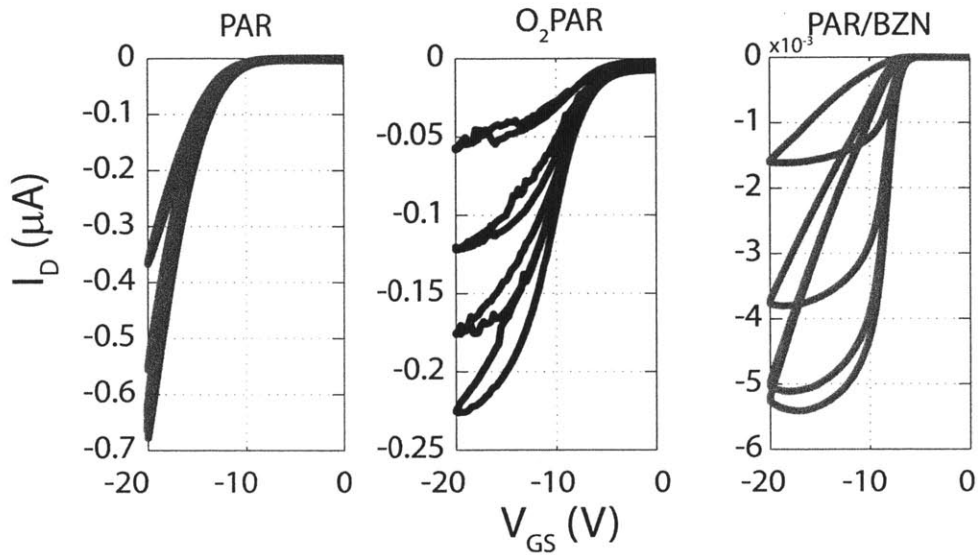
FIGURE 8-22: Comparing the Transfer Characteristics of HVOTFTs with the PAR, O_2 PAR, and PAR/BZN insulators. The channel length (L)=5 μm and the channel width (W)=250 μm with a 20 μm offset at the drain (OV20020). HVOTFT reveals a deflection in the transfer characteristic as a result of the offset. V_T, μ, and S cannot be accurately extracted due to this deflection.

HIGH VOLTAGE SWEEPS: $V_{DD} \geq 300V$ Electrical characteristics at high voltages were taken with two Keithley 236 Source Measure Units operating in parallel in a dark at room temperature. Output characteristics at high voltages were taken to assess the behavior of these devices at high operating voltages and with different insulators. Ideally, all HVOTFTs regardless of offset size should not pass current larger than that predicted by a conventional OTFT as shown Figure 8-23 as proposed by the modifications in Equation 8.5.
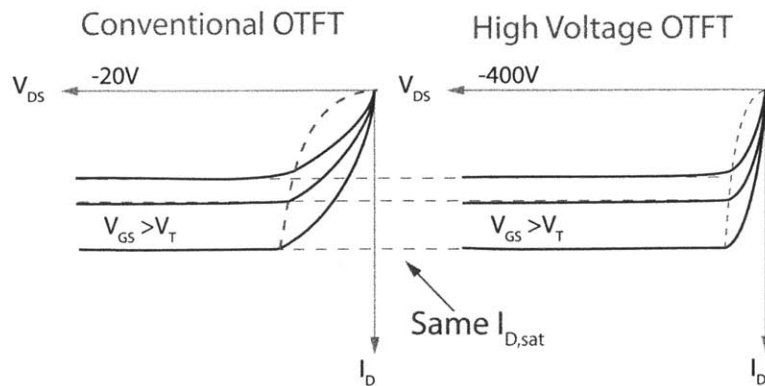
FIGURE 8-23: Output Characteristics of an ideal HVOTFT as compared to a Conventional OTFT.

204

Actual, current voltage characteristics for each insulator are shown in Figure 8-24. For reference, output characteristics for conventional OTFT are shown in plots A through C for the PAR, O_2 PAR, and PAR/BZN based OTFTs respectively. HVOTFTs with a 20 μm offset on the drain side for the PAR, O_2 PAR, and PAR/BZN based devices are shown in plots E-F, respectively. The devices still show clear gate control at high voltages but do not saturate well. This is not in agreement with Equation 8.5 which implies that $I_{D,sat}$ should not change when there is no offset at the source.

The PAR based OTFTs have an insulator thickness of 500 nm. The HVOTFT passes a current larger than what is predicted by its corresponding conventional OTFT in Figure 8-24 (A). The square law dependence appears to be lost as I_D (V_G) appears linear as shown in Figure 8-24(D), or the spacing between each sweep appears linear. The I_D vs. V_{DD} plot for this device shows a quadratic behavior as shown in Figure 8-24(D), and is substantially larger than what is predicted by the Si Long Channel MOSFET Model. A parasitic space charge limited current brought about by high fields is likely responsible for this non-saturation behavior [17].

For the O_2 PAR based OTFTs, the insulator thickness is 350 nm and the current follows the square law dependence (spacing between sweeps increase at a power higher than 1 more precisely though they do not saturate well either as shown in Figure 8-24(E). The I_D vs. V_{DD} plot for this device shows linear behavior and better matches the $I_{D,sat}$ predicted by the conventional OTFT which is shown in Figure 8-24 (B). This also may be due to the high fields.

For the PAR/BZN based OTFTs the dielectric thickness is 400 nm (200 nm of parylene-C on top of 200 nm of BZN) The current follows the square law dependence as well, but it also does not saturate as shown in Figure 8-24(F). The I_D vs. V_{DD} behavior for this device shows quadratic behavior and better matches the $I_{D,sat}$ predicted by the conventional OTFT as shown in Figure 8-24(C), but not as well as the O_2 PAR device. As with the PAR device, parasitic space charge current brought about by high fields is likely responsible for this non-saturation behavior [17, 18].

Placing the offset at the source has some utility, though often dismissed as simply reducing the device transconductance ($\partial I_D/\partial V_G$). Consider the HVOTFT to be a voltage divider consisting of a OTFT and a resistor. The element with the most resistance will dominate IV behavior. By placing the offset at the source, the OTFT is much more resistive (the gate is unbiased[4] by the offset at the source) and can dominate IV behavior as in Equation 8.5. Therefore the PAR based OTFT which has the worst saturation and gate control; one can reestablish FET IV behavior by placing an offset at the source, at the expense of reducing the transconductance. Figure 8-25

---

[4] the offset reduces the gate-to-source voltage that drives the gated semiconductor regions and indicted in Equation 8.4.
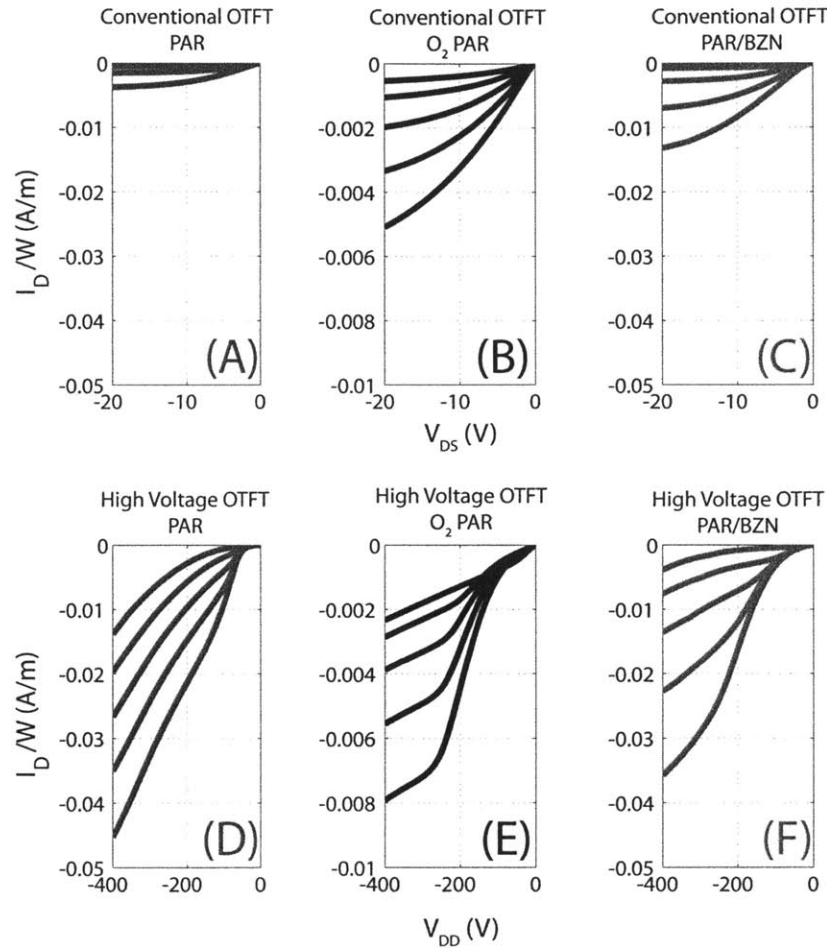
FIGURE 8-24: A-C are standard OTFTs with no offsets at lower operating voltages. They are plotted for comparisons with HVOTFTs which should saturate at the same I_D/W. D-E are HVTFTs with OV20020 (corresponding to a 20 μm offset at the drain) at high operating voltages. The channel length (L) is 10 μm. Gate Voltage (V_G) stepped from 0 V to -20 V in -5 V increments. Drain Voltage (V_{DD}) stepped from 0 V to -400 V in -5 V increments.

shows better saturation with an offset at the source.

From Figure 8-25, the I_D at V_{DD}=-400 V and V_G=-5 V and of the OV20020 device in (B) is $\sim -5~\mu A$ and is equal to the I_D at V_{DD}=-400 V and V_G=-20 V of the OV201010 device in (C). This suggests a drop of $\sim$ 15 V across the offset at the source. If $\sim$15 V drop across the offset at the source, $\sim$15 V must drop across the offset at the drain as both pass the same current. This leaves a voltage drop greater than 300 V across the gated regions. This implies the potential at the edge of the gates is more negative than -300 V. With a breakdown field of 2-4 MV/cm [19], the gate insulator parylene-C will breakdown on at a voltage difference of 200 V. With this analysis,

206
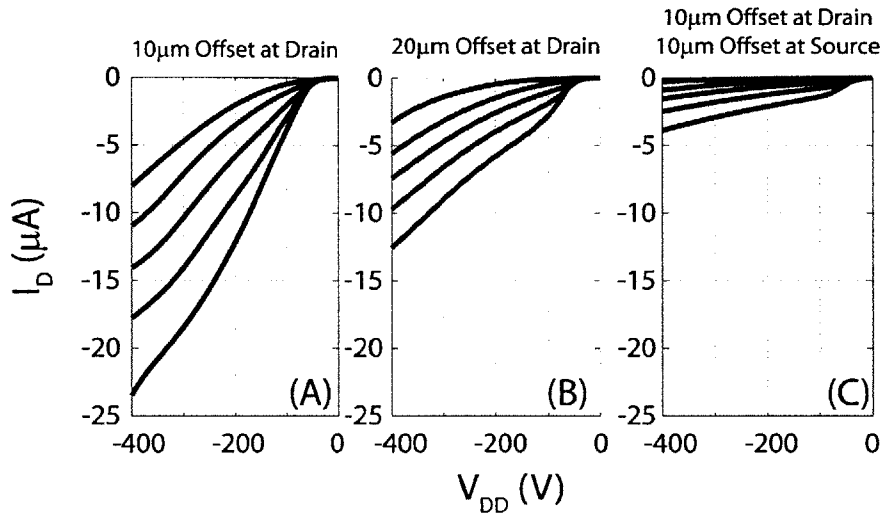
FIGURE 8-25: Output Characteristics for HVOTFT comparing different offset locations. The channel length (L)=8μm and the channel width (W)=250 μm, PAR based OTFT. V_G is stepped from 0 to -20 V in -5 V increments while V_{DS} is swept from 0 to -400 V in -5 V increments.

the devices in Figure 8-25(C), should fail at a much smaller V_{DD}. As the device is operable at $V_{DD} = -400V$, the voltage dropped across the offset at the drain must be >100 V. However, as the device still turns on and shows gate control the voltage drop across the source cannot be >100 V, even though the offsets at the source and drain pass the same current. Therefore it can be concluded that the resistivity of the offset at the source has dropped substantially. At this time, it is unclear what would cause such a reduction in resistivity.

8.3.2 High Field Effects

For MOSFETs and TFTs, the model for $I_D(V_{DS}, V_{GS})$ is based on the gradual channel approximation i.e. the vertical field (due to V_{GS}) is much larger than the horizontal field (due to V_{DS}). As articulated in Section 8.2.2 the gate and the drain are competing for control of the charge in the channel. The gate will accumulate charge at the insulator/semiconductor interface. The drain will deplete the channel of charges. In the ideal case, the gate maintains control of the charge in the channel and the drain will not modify this charge beyond saturation. When the gate begins to lose control in the channel or the horizontal field becomes large, IV deviates significantly from what is predicted by the Si Long Channel MOSFET Model. A large electric field from the source-to-drain can occur by the application of a large V_{DS} (or V_{DD} in the case of a HVOTFT) but is typically the result of short channel lengths. Depending on what physical mechanism are active, I_D will increase or decrease with V_{DS} (or V_{DD}) when the I_D should be constant and independent of V_{DS} (or V_{DD}). Such effects in Si-based MOSFET motivated the development of the Si Short Channel MOSFET Model. The HVOTFTs made with the insulators in this work, all show a larger drain current than

207

TABLE 8.2: Summary of short channel effects in literature

Source	E (MV/cm)	Current Saturation?	t_{ox} (nm)	Semiconductor	Year
Collet et al. [20]	0.5	N	2	sexithiophene	2000
Austin et al. [21]	0.4	N	5	P3HT[5]	2002
Zhang et al. [22]	0.7	Y	30	pentacene	2003
Wang et al. [23]	6	N	100	pentacene	2004
Lee et al. [24]	0.3	Y	3	pentacene	2005
Haddock et al. [25]	0.6	Y	200	material[6]	2006
Tukagoshi et al. [18]	0.25	Y	4	pentacene	2007
Chen et al. [26]	0.17 0.13	N Y	70	P3HT	2009
Hirose et al. [27]	7	Y	200	F8T2[7]	2010
This Work	0.1	N	350-500	pentacene	2012

[5] poly-3-hexylthiophene

[6] E,E-2,5-bis-40-bis-(400-methoxy-phenyl)amino-styryl-3,4-ethylenedioxy-thiophene

[7] poly9,9-dioctylfluorene-co-bithiophene

predicted than their conventional OTFT counterparts. Therefore, high field effects that similar to the traditional short channel effects are active in these devices.

The HVOTFT with the offset and channel lengths (10 μm-20 μm) used in this work operate voltages larger than 300 V. The electric fields across the channel of the device are the same as a submicron device operating at lower voltage ranges that are typical in Si-based microelectronics. Therefore, it is expected that the HVOTFT will suffer from similar non-ideal current-voltage characteristics at high drain-to-source voltages. From the output characteristics, there appears to be two mechanisms that contribute to non-ideal output characteristics in these HVOTFTs. They are space charge limited current (SCLC) and channel length modulation (CLM) and have been reported by other investigators with similar drain-to-source electric fields in OTFTs as shown in Table 8.2. It should be noted that this work shows non-ideal output characteristics operative at long channel lengths as opposed to the short channel lengths reported in other organic semiconductors.

High Field Effects: Parasitic Space Charge Limited Current

Mott-Gurney Space charge limited current (SCLC) is a conduction mechanism where charge flow is treated as a continuum of charges drifting through a solid that can support a distribution of charges, such as a dielectric or depleted semiconductor. In addition, space charge limited current typically occurs in the absence of defects or charge traps in the solid [28, 29]. Thin films of pentacene are disordered systems, in where charge traps exists. However, there are numerous reports of space charge limited currents in pentacene thin films. Lee et al. reported space charge limited current conduction become active in pentacene thin films at voltages > 100 V with

structures sizes of $\sim 10\mu m$ [17]. This is comparable to the voltages and sizes of the devices in this work. Below a critical voltage or electric field, conduction is ohmic. The transition from ohmic conduction to space-charge-limited conduction corresponds to the filling of charge traps created by microstructural disorder in the pentacene thin film [17]. Tukagoshi et al. attributed non-saturation in submicron pentacene based TFTs to SCLC [18] enhanced by the Frenkel Effect [18, 28, 30]. The Frenkel Effect occurs when large electric fields make the charge carriers more energetic. There is less additional energy needed for the carrier to hop to the next site. This is believed to be the same mechanism that gives rise to the field effect mobility in pentacene that was discussed in Chapter 2. This reduces the effectiveness of the charge traps and makes space charge limited currents more significant. The expression for this is Equation 8.6 [28].

$$J_{SCLC} = \frac{9}{8}\mu_0 \kappa \epsilon_o \frac{V^2}{L^3}\theta_o \tag{8.6}$$

$$\theta_o = \frac{\rho_f}{\rho_f + \rho_t} = \frac{N_v}{N_T}exp\left(-\frac{A}{kT}\right) \tag{8.7}$$

Where,

J_{SCLC}: Space Charge Limited Current Density
μ_0: carrier mobility
ϵ_o: permittivity of free space
L: channel length
V: applied voltage
ρ_f and ρ_t: the free and trapped charge densities
N_T: density of traps
N_V: density of states
A: Activation energy

Consider the output characteristic for a 10 μm channel length HVOTFT with a 20 μm offset at the drain at $V_G=0$ for all three insulators as shown in Figure 8-26. Following Equation 8.8, the slope of the IV behavior ($log(I_D)$ vs. $log(V_{DD})$) for each insulator will indicate the type of conduction (~ 2 for SCLC and ~ 1 for ohmic) flowing through the devices.

$$I_D \propto V_{DD}^m \Rightarrow log(I_D) \propto m \times log(V_{DD}) \tag{8.8}$$

Where,

V_{DD}: voltage applied at drain electrode or supply voltage
I_D: Drain Current
m: slope of $log(I_D)$ vs. $log(V_{DD})$

The current voltage behavior is quadratic ($m \sim 2$) at high voltages for the PAR and PAR/BZN based devices ($V_{DD} > 100$ V) and indicative of space charge limited

209
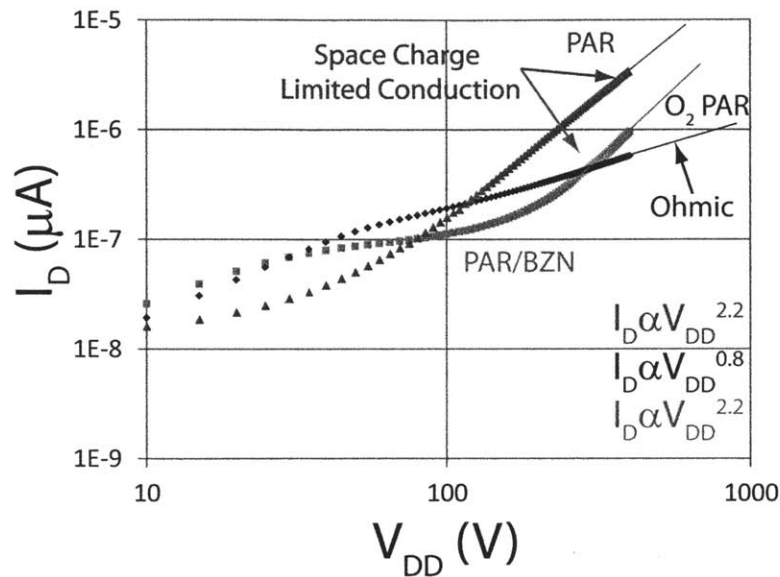
FIGURE 8-26: I_D vs. V_{DD} at $V_G = 0$ V shows a quadratic relationship for PAR and PAR/BZN and a linear relationship for O_2 PAR. The channel length (L) is 10 μm with a 20 μm offset at the drain (OV20020).

current similar to the that reported be Lee et al [17, 18]. In an attempt to remove this parasitic SCLC, subtracting the $V_G=0$ sweep from the rest of the output characteristics, as shown in Figure 8-27 (B), generates curves that look similar to the O_2 PAR based OTFTs as shown in Figure 8-27(C) (linear non-saturation, square law dependence). As there is still no saturation after accounting the parasitic space charge limited current, there is likely another mechanism that is operative that inhibits current saturation.

To minimize the SCLC, Tukagoshi et al. reduced the thickness of the insulator (increased the gate capacitance) and reduced the semiconductor layer thickness as the SCLC is suspected to be in the bulk of the film. [18]. Reducing t_{ox} for the PAR based devices will help the gate maintain control (smaller subthreshold swing) of the channel but at the sacrifice of high voltage reliability (max V_{DD}). This is summarized in Table 8.3. Accordingly, as the PAR/BZN based OTFT have a larger gate capacitance due to the larger dielectric constant, they show less SCLC compared to the PAR based devices as Tukagoshi et al. suggests.

This explanation for non-saturation is sufficient for the PAR and PAR/BZN based OTFTs, however not for the O_2 PAR based OTFTs that have non-ideal saturation behavior that is linear and not quadratic, even with a thicker semiconductor layer. The surface treatment used to shift the threshold voltage in the O_2 PAR based OTFTs

210
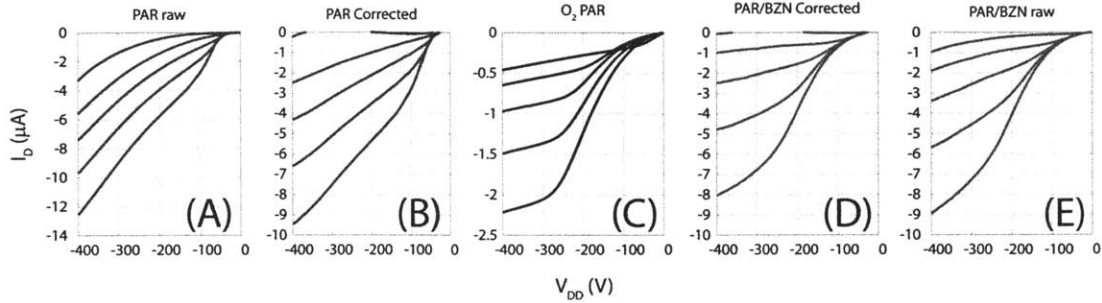
FIGURE 8-27: (A) Raw Output Characteristics of a 8 μm channel length HVOTFT with a 20 μm offset at the drain (OV20020). By subtracting the quadratic component (V_G=0 V) from the sweeps taken at higher V_G values, the PAR device (B) shows similar behavior to that of the O$_2$ PAR device (C) (linear non-saturation, square law dependence). This case holds for the PAR/BZN based OTFTs where the raw data is at (E) and the corrected sweep is at (D).

TABLE 8.3: Summary of extracted device parameters for PAR based OTFTs with different insulator thicknesses. The thickness of the pentacene is ~20 nm, the channel length (L) =10 μm, with a 20 μm offset at the drain (OV20020) for the corresponding HVOTFT.

PARAMETERS	500 nm	350 nm
I_{OFF}/W (A/m)	8E-8	2E-10
S (V/dec)	8.8	3.1
S_{ID} (V/dec)	0.117	0.116
D_{it} (cm^2/eV)	4.82E+12	2.74E+12
Max V_{DD}	-500 V	-300 V

may be the source of this. With the surface treatment interface traps were created at the insulator/semiconductor interface. Recalling from Table 8.1, the O$_2$ PAR based OTFTs had the larger D_{it} than the PAR and PAR/BZN based OTFTs, which indicates more interface states and therefore charge traps. Further, extracted surface energy is large for the O$_2$ PAR surface which suggests the presence of interface states. Intuitively, more interface states implies more trapped charges or a larger N_T (See Equation 8.7). in the pentacene layer of the O$_2$ PAR based OTFTs. From Equations 8.6 and 8.7, more trapped charges (N_T is large), leads to an smaller SCLC, which is what is seen for the O$_2$ PAR based OTFTs at high voltages. Therefore, it is concluded that the interface states created to shift the threshold voltage in the O$_2$ PAR based OTFTs, trap free carriers (N_T is large) to the extent that SCLC is suppressed. Therefore, another mechanism must be responsible for non-saturation in the O$_2$ PAR based OTFTs.

211

High Field Effects: Channel Length Modulation

Consider how the charge is distributed in the channel when V_{GS} is below V_T and V_{DS}=0 V (or V_{DD}=0 V) as shown in Figure 8-28 (b). As V_{DS} (or V_{DD}) increases, the region of the channel that is close to the drain becomes less accumulated or more depleted. Logically, when $V_{DS} = V_{GS} - V_T$ (or $V_{DS'} = V_{GS'} - V_T$), the region of the channel close to the drain electrode is fully depleted of charges based on the depletion approximation. The depleted region is highly resistive where charges are quickly swept through this region and the current saturates. Additional V_{DS} (or V_{DD}) depletes more of the channel. The electrostatic field at the drain increases and the carriers move faster through the depleted region (increasing I_D). This depleted region close to the drain is small however, if the size of the channel is comparable to the size of this depleted region, the effective length of the channel decreases with increasing V_{DS} (or V_{DD}). As a result, I_D will depend on V_{DS} (or V_{DD}). This is referred to as channel length modulation and shown in Figure 8-28(d). Again, as there are large lateral voltages across the channel, HVOTFTs can be susceptible channel length modulation. The Si Long Channel MOSFET model is modified by the addition of the channel-length modulation parameter (λ) [31]. When channel length modulation is active, I_D will increase linearly with V_{DS} (or V_{DD}) as shown in Equation 8.9. Figure 8-29 shows a typical MOSFET that suffers from channel length modulation and how the channel-length modulation parameter (λ) is extracted. Channel length modulation is reported in a-Si based HVTFTs by Karim et al.[3] and in organic based TFTs by Haddock et al. [25].

$$I_{D,sat} = \frac{\mu C W}{2L}(V_G - V_T)^2(1 + \lambda V_{DS}) \qquad (8.9)$$

There numerous reports of submicron OTFTs that suggest that high field effects in OTFTs can be treated similarly to those found in Si-based submicron MOSFETs [24, 18]. There are number of additional mechanisms that lead to short channel effects in MOSFETs, including but not limited to drain-induced barrier lowering, punchthrough, surface scattering, velocity saturation, impact ionization and hot electrons [31]. (For more details on short channel effects in FETs, refer to Streetman [31].) It is difficult to extract how these affect current voltage behavior in MOSFETs. These same difficulties with the additional complication a hopping based transport (Frenkel-Poole or polaronic as discussed in Chapter 2) as opposed to band transport seen in pentacene, make the identification of the active high field effects in OTFTs more difficult. Accounting for the channel-length modulation parameter (λ), the saturation current for a HVOTFT is modified as shown in Equation 8.10. Figure 8-31 shows the output characteristics for the O_2 PAR based OTFT at V_G=-20 V for various V_{DD}. The extracted λ is summarized in Table 8.4.

$$I_{D,sat,HV} = \frac{\mu C W}{2L}[(V_G - V_T - (I_{D,sat,HV}R_{offset,source})]^2(1 + \lambda V_{DS'}) \qquad (8.10)$$

212
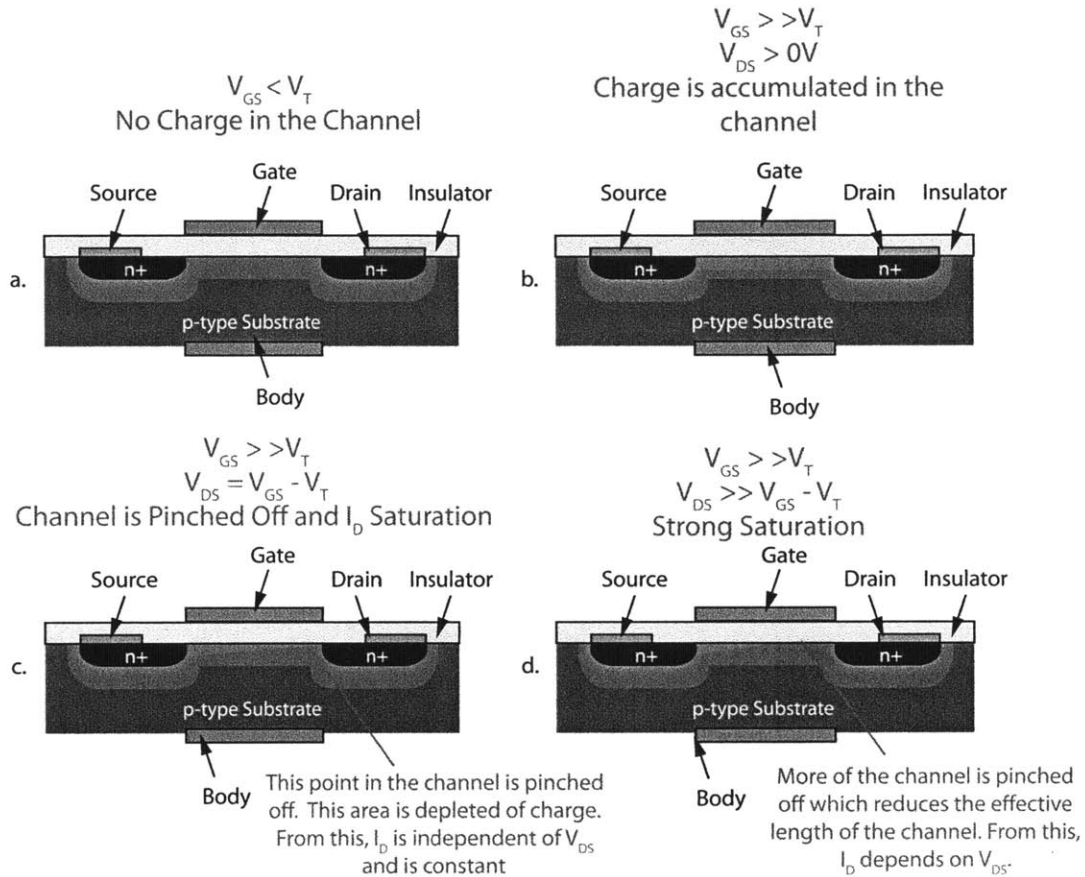
FIGURE 8-28: MOSFET cross sections under different operating conditions.

The modification of the Si Long Channel MOSFET model appears to describe the linear non-ideal saturation current behavior in the O_2 PAR based OTFTs well as the extracted λ is the same for $V_{DD} = $ -300 V, -400 V, and -500 V. Equation 8.10 suggests that $I_{D,sat,HV}$ should increase linearly with V_{DS} (or V_{DD}). From Figure 8-27(C), the O_2 PAR based OTFTs shown a linear non-saturating behavior consistent with channel length modulation as well as the PAR (Figure 8-27(B)) and PAR/BZN (Figure 8-27(D)) based OTFTs also showing linear non-saturating behavior after correcting for the SCLC. The channel length modulation parameters for all insulators after correcting for leakage and SCLC are tabulated in Table 8.5.

From Equations 8.10, the $I_{D,sat,HV}$ depends on the sizes of the offsets at both the source and drain. The likely IV behavior of the offsets is shown in Figure 8-30. This is a non linear dependence, likely to be Frenkel-Poole conduction or polaronic hopping as discussed in Chapter 2. This implies that the resistance of the offset decreases with

213
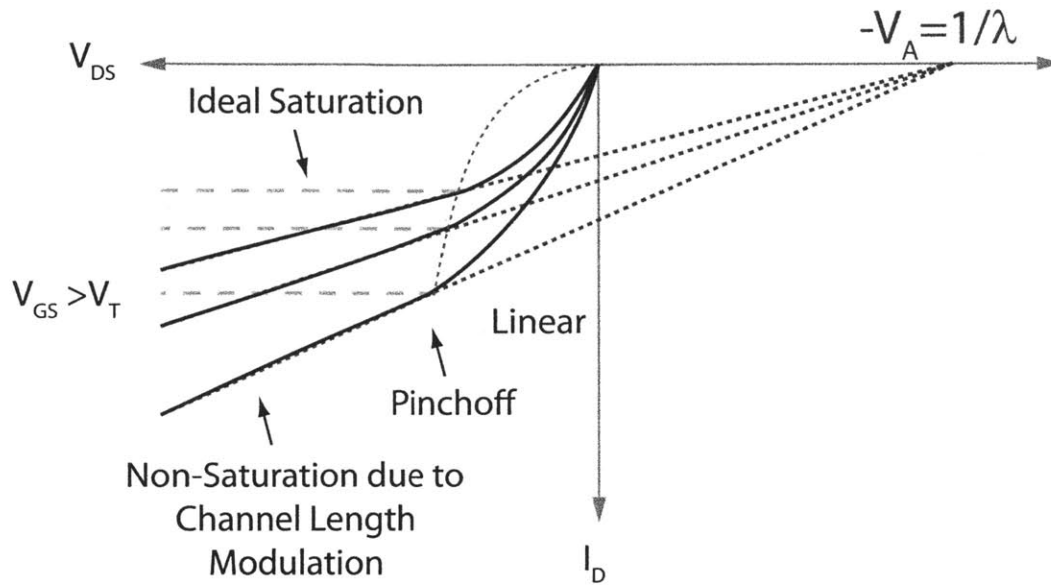
FIGURE 8-29: Output Characteristics of MOSFET affect by Channel Length Modulation. This figure shows how the channel length modulation parameter ($\lambda 4$) is extracted.

TABLE 8.4: Extracted V_A and λ from various V_{DD} values from the O_2 PAR based HVOTFTs. These values take into account leakage that showed and "OFF" conductance of 1E-9 S

V_{DD}	$\mathbf{V_G = 0V}$	$\mathbf{V_G = -5V}$	$\mathbf{V_G = -10V}$	$\mathbf{V_G = -15V}$	$\mathbf{V_G = -20V}$
(V)	V_A (V) [λ (V^{-1})]				
300	200[0.0050]	400[0.0025]	800[0.0013]	1600[0.0006]	1430[0.0007]
400	170[0.0059]	500[0.0020]	1000[0.0010]	1300[0.0008]	1250[0.0008]
500	130[0.0077]	670[0.0015]	1000[0.0010]	1140[0.0009]	1000[0.0010]
600	125[0.0080]	400[0.0025]	710[0.0014]	1000[0.0010]	1000[0.0010]
700	500[0.0020]	830[0.0012]	1110[0.0009]	2000[0.0005]	1000[0.0010]

increasing electric fields or V_{DD}. In reference to Equation 8.10, the reduction in the resistance of the offset will increase $V_{DS'}$. This will result in a more pronounced channel length modulation. This is evident in Figure 8-31 as at $V_{DD}=$ -600 V and -700 V as the extracted λ changes and the non-ideal saturation behavrior appears to be non-linear. Further, the device broke down just beyond $V_{DD}=$-700 V. Though not apparent from Equation 8.10, a large gate capacitance can reduce channel length modulation by better accumulating charges in the semiconductor.

TABLE 8.5: Extracted V_A and λ from various V_G values from PAR, O_2 PAR, and PAR/BZN based HVOTFTs, $V_{DD} = -400$ V.

V_G (V)	PAR	O_2 PAR	PAR/BZN
	$V_A(V)[\lambda(V^{-1}]$		
0	-	170[0.0059]	-
-5	25[0.0400]	500[0.0020]	500[0.0020]
-10	6[0.1667]	1000[0.0010]	333[0.0030]
-15	40[0.0250]	1300[0.0008]	285[0.0035]
-20	50[0.0200]	1250[0.0008]	300[0.0033]
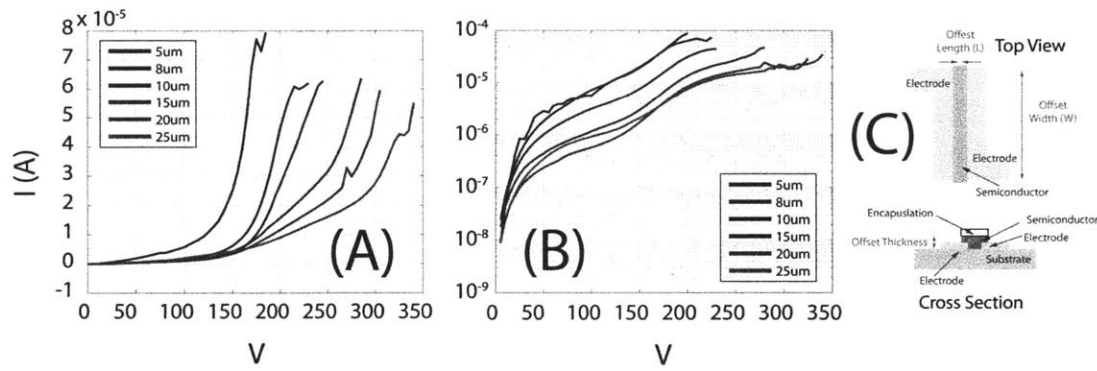
FIGURE 8-30: (A) Linear IV Behavior of offset length of size 5, 8, 10, 15, 20, and 25 μm. (B) Log IV Behavior of Offset Sized 5,8,10,15,20, and 25 μm. The offsets have nonlinear IV behavior. The thickness of pentacene used in these resistors are 10 nm, which is between 1/2-1/4 of what is used in the HVOTFT. (C) Cross Section and Top View of the structure measured to represent the offset. They mimic the device structure of OTFTs
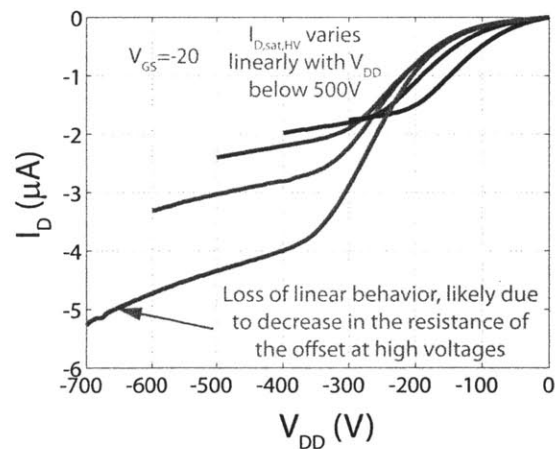
FIGURE 8-31: I_D vs. V_{DS} at V_G=-20 V and various V_{DD} for O_2 PAR HVOTFTs. The channel length (L)=10 μm and the channel width (W)=250 μm with a 20 μm offset at the drain (OV20020) for O_2 PAR based HVOTFTs

215

High Field Effects: Threshold Voltage Roll-Off

Threshold voltage roll-off is similar to drain induced barrier lowering or DIBL in Si-based microelectronics. DIBL occurs when the threshold voltage decreases at high drain voltages, due to the extension of the depletion region into the back of the channel [31, 32]. It is typically expressed and the change in V_T with V_{DS} as expressed in Equation 8.11.

$$DIBL = \frac{\Delta V_T}{\Delta V_{DS}} \tag{8.11}$$

The Transfer Characteristics of the OTFT clearly show the effect of the offset (Figure 8-22). As a result of the offsets in the HVOTFT, threshold voltage cannot be extracted without a firm understanding of the mechanism operative in the offsets. Evaluating the conventional OTFT at higher drain-to-source voltages ($V_{DS} \leq 100$ V) in Figure 8-32, there is clearly a shift in threshold voltage induced by large drain-to-source voltages. Haddock et al. report a similar threshold voltage roll-off in short channel OTFTs [25]. Therefore, threshold voltage roll-off is likely operative the HVOTFTs, however, extracting an exact dependence is not possible with these structures. In some cases, this high field effect is taken into account with the channel length modulation parameter (λ) [31].
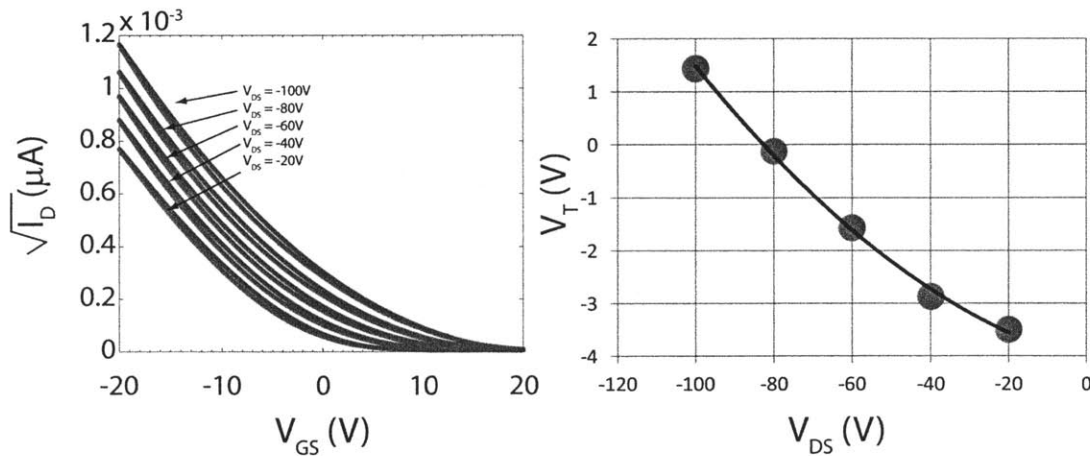
FIGURE 8-32: Threshold Voltage Roll-Off in a PAR based OTFT with a channel length (L)=10 μm and channel width (W)=250 μm. Threshold voltage shifts more positive with increasing V_{DS}. This is similar to DIBL.

8.3.3   Metastable Charge Injection

In Figure 8-33, there appears to be a significant contact resistance ("Birds' beak") that appears after high voltages have be applied across the HVOTFT. This suggests that a large V_{DD} creates substantial injection barrier in the device, which impacts charge transport. From Martin et al. regarding a-Si based HVTFTs, "If improperly
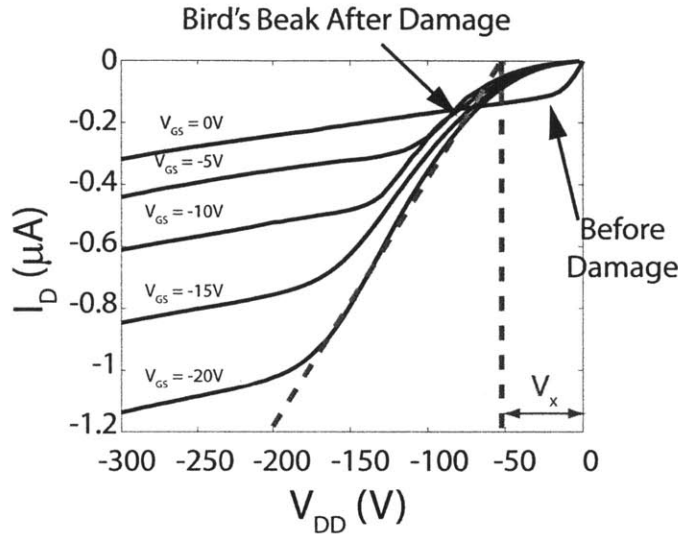
FIGURE 8-33: Output Characteristic of HVOTFT device illustration how damage appears with high voltage operation. The channel length (L)=10 μm and channel width (W)=250 μm, with a 10 μm offset at the drain and a 10 μm offset at the source (OV201010).

designed, a-Si HVTFT's show an unusual instability. The drain voltage for the onset of the increase in drain current with V_{DD} can shift to higher voltages. This arises from the creation of metastable states in the a-Si in the offset region near the gate edge." [2]. For a-Si, the offset region is completely depleted of charges. When voltage is applied to the gate, no free charges exist in the offset. The material responds by generating trap states or changing the density of states such that the band structure is modified. As a result, a barrier for injection is created consisting of charged filled modified trap states that were created by the large fringing fields at the corner of the gate electrode. A similar instability in pentacene based HVOTFTs are likely the cause of the "Birds' beak" seen in Figure 8-33 which may have similar origins to the a-Si case. Figure 8-34 shows the location of the generated traps that resulted in the instability in the HVOTFTs in this work. This instability is quantified by V_x which is the shift in the onset of current rise as defined in Figure 8-33. Figure 8-31 shows that the size of this instability changes with the V_{DD} or the lateral electric field applied across the device, which is reported by Martin et al [33, 2]. Table 8.6 summarizes how V_x increases with V_{DD}. As with the extracted channel length modulation parameter λ, the trend is lost beyond $V_{DD} = $ -600 V, which coincides with the suspected dramatic decrease in the resistance of the offset.

This instability in charge injection can also modify charge transport in the device.
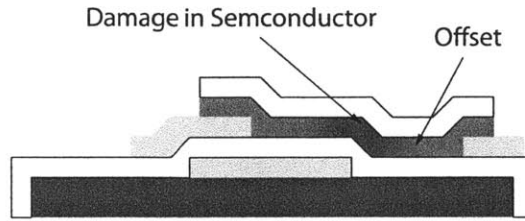
FIGURE 8-34: Cross-section of HVOTFT illustrating the location of the generated traps in the semiconductor at the edge of the gated region.

TABLE 8.6: Trends in how V_x changes with V_{DD}. Extraction was taken at V_G=-20 V. The channel length (L)=10 μm and the channel width (W)=250 μm with a 20 μm offset at the drain (OV20020). I_D has not been corrected for this extraction.

V_{DD} (V)	$E_{lateral}$ (MV/cm)	PAR V_x(V)	O$_2$ PAR V_x(V)	PAR/BZN V_x(V)
200	0.07	-	-	25
300	0.10	20	60	50
400	0.13	50	100	100
500	0.17	66	150	-
600	0.20	-	200	-
700	0.23	-	150	-

TABLE 8.7: Trends in how V_x changes with V_G. Extraction was taken at V_{DD}=-400 V. The channel length (L)=10 μm and the channel width (W)=250 μm with a 20 μm offset at the drain (OV20020). I_D has not been corrected for this extraction.

V_G (V)	PAR	O$_2$ PAR	PAR/BZN
0	-	-	-
-5	50	90	25
-10	50	100	50
-15	50	100	80
-20	50	105	105

In the asymmetric devices (where OV0##0 and OV#0#), it was observed that I_D depended on which orientation was measured first. Figure 8-35 shows that measuring the OV#0# orientation first reduces the I_D of the OV##0 orientation compared to what it would have been if the OV##0 orientation had been measured first.
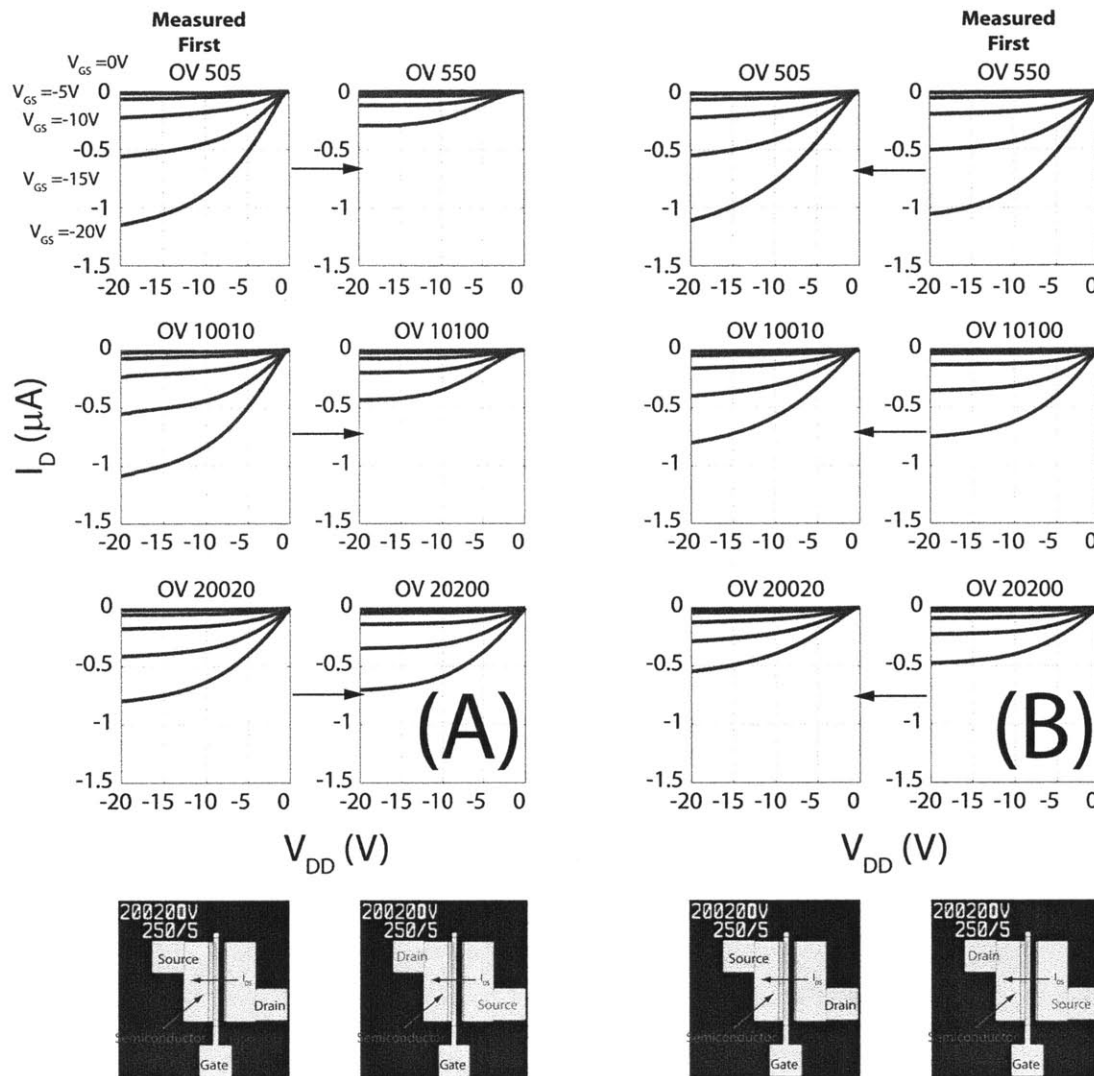
FIGURE 8-35: Output Characteristics and the dependence on which orientation is measured first. The channel length (L)=5 μm and the channel width (W)=250 μm. On the left (A), OV#0# is measured first followed by OV##0. On the right (B), OV##0 is measured first followed by OV#0#. Based on the difference in I_D base on the orientation measured, charges being trapped in the device.

Figure 8-36 shows the evolution of the output characteristics based on testing history and orientation. Starting with the OV##0 orientation, the ground and supply voltage probes are switched back and forth consecutively. The IV characteristics shown in Figure 8-36(F) were taken three hours after the IV characteristics shown in Figure 8-36(E). This comparison suggests an improvement in transport properties in the channel. This implies the instability created is reversible as reported with a-Si case
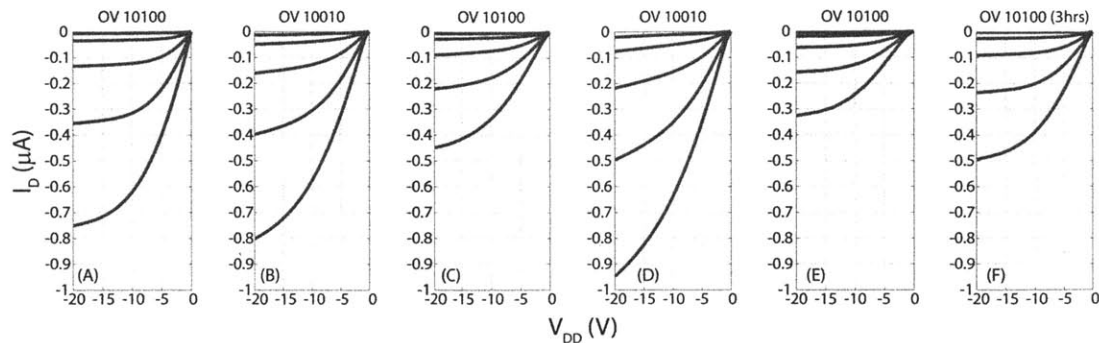
FIGURE 8-36: Evolution of Output Characteristics for devices tested in order (A)-(F).

by Martin et al.[2, 33] and Shaw et al.[34].

Martin et al. reported an injection barrier of 0.1 MV/cm in an a-Si based HVTFT with an offset length of 15 μm and a channel length of 5 μm and channel width 240 μm [33, 2] which is comparable to the sizes of devices in this work. From Figure 8-30, the offsets fail at fields ranging from 0.1 MV/cm to 3 MV/cm. Assuming that the fringing fields in the a-Si based HVTFT structure from Martin et al. are comparable to fringing fields in the HVOTFTs in this work, these fields are large enough to create traps in the pentacene at the edge of the gate.

Shaw et al. [34] and Martin et al. [33, 2] report that using a field plate improved the performance of their HVTFT. The field plate improved devices performance by weakly accumulating charge at the transition of the gate and offset. First, this provides more free charge that can respond to the fringing fields as opposed to creating defects. Second, the offset is less resistive such that current can rise faster with the applied V_{DD} which leads results is a smaller or negligible V_x. This is shown in Figure 8-37.

The physics behind how this instability is manifested in pentacene is beyond the scope of this dissertation. For more information regarding the origins in V_x, refer to Martin et al. 1993 [33, 2] and Shaw et al. 1991 [34]. Moreover, using an alternative patterning method may that creates a smoother corners may mitigate large fringing fields.

220
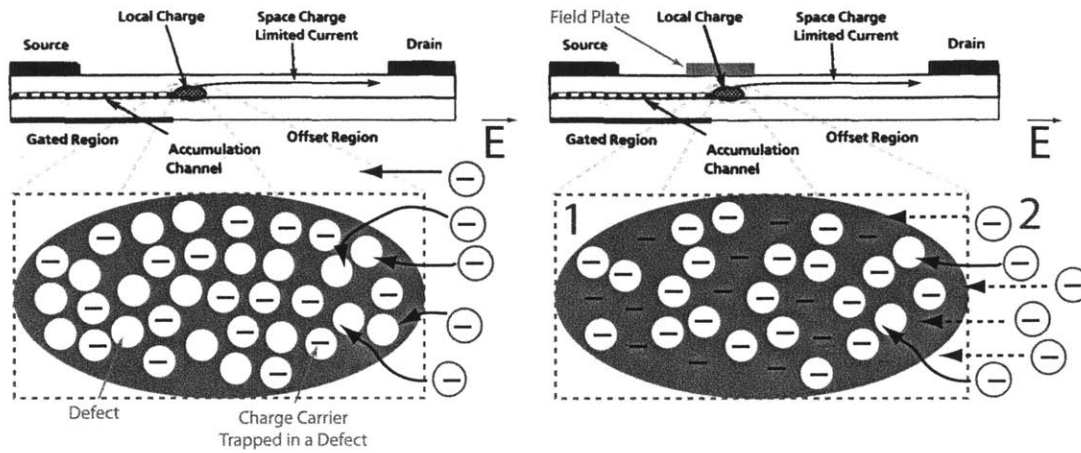
FIGURE 8-37: Illustration of how defects are created due to fringing fields. A field plate weakly accumulated charge in at the edge of the gate region. As result, more free charge can respond to the fringing field and fewer traps are created and the offset is less resistive such that current can rise faster with the applied V_{DD} which reduces V_x.

8.3.4 Correcting for High Field Effects

Figures 8-38 through 8-40 show how the output characteristics of the HVOTFTs built with each gate insulators with corrections for leakage, space charge limited current, and channel length modification. Equation 8.12 shows how the measured I_D values are corrected to account for high field effects. With these modifications, the HVOTFTs behave more ideally in that the gated region is controlling $I_{D,sat}$ such that it matches that of an conventional OTFT. A correction for V_x should be proposed after high field effects are mitigated or when relevant parameters quantifying these effects can be established for a technology.

$$I_{D,corrected} = \frac{I_{D,measured} - I_{SCLC,leakage}}{(1 + \lambda V_{DD})} \tag{8.12}$$

$$\lambda^{-1} = V_A + |V_x| \tag{8.13}$$

FIGURE 8-38: PAR based HVOTFTs corrected for SCLC and channel length modulation. The channel length (L)=10 μm and channel width (W)=250 μm with a 20 μm offset at the drain (OV20020), $\lambda^{-1} = V_A + |V_x|$=90 V

FIGURE 8-39: O_2 PAR based HVOTFTs corrected for SCLC and channel length modulation. The channel length (L)=10 μm and channel width (W)=250 μm with a 20 μm offset at the drain (OV20020), $\lambda^{-1} = V_A + |V_x|$ =1130 V

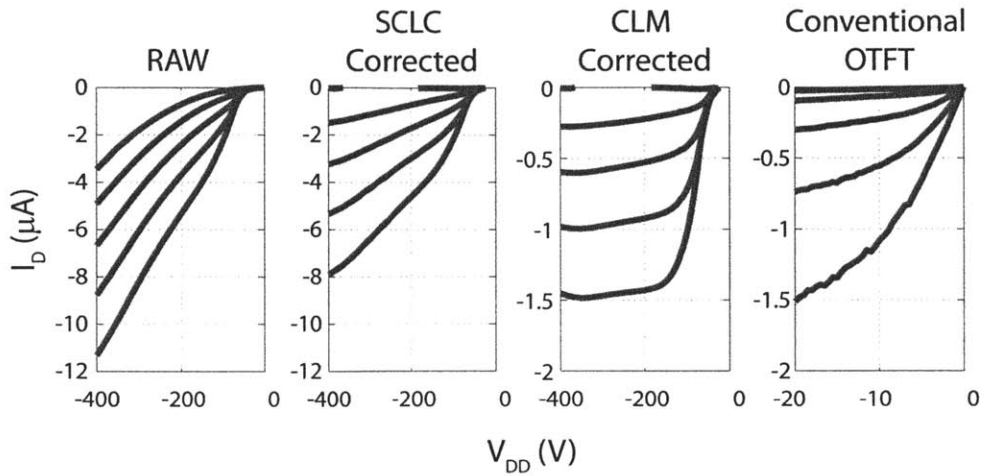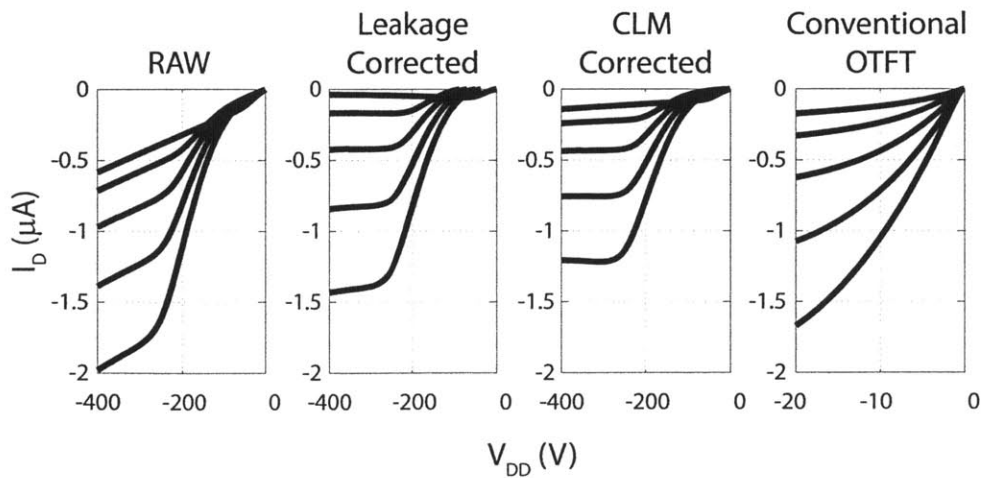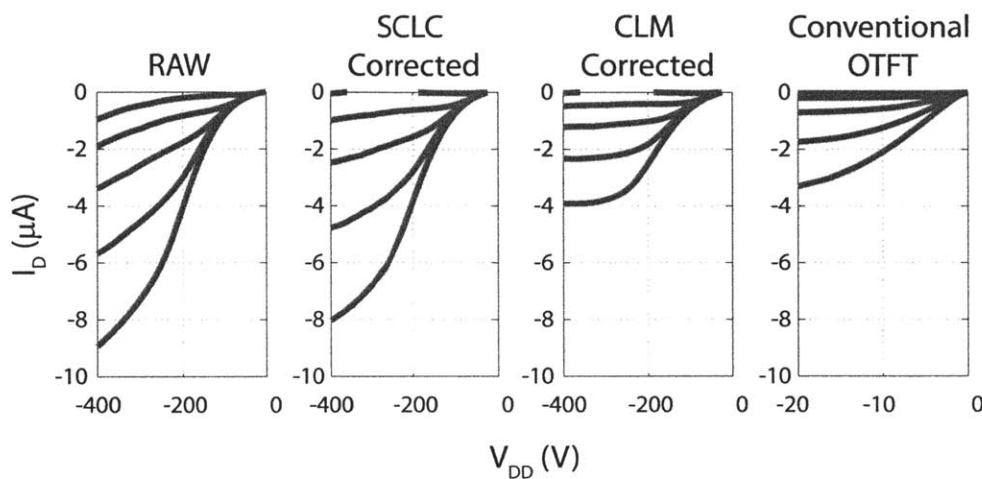FIGURE 8-40: PAR/BZN based HVOTFTs corrected for SCLC and channel length modulation. The channel length (L)=10 μm and channel width (W)=250 μm with a 20 μm offset at the drain (OV20020), $\lambda^{-1} = V_A + |V_x| = 380$ V

8.4 STABILITY

The electrical parameters of OTFTs are known to change with time and exposure to ambient environments. The degradation is attributed to creation of charge traps at the grain boundaries of the pentacene and the insulator/semiconductor interface [35, 36]. The parylene-C encapsulation can help with this issue however, the encapsulation is still insufficient beyond protection from the solvents used in photolithography [37]. Figures 8-41 through 8-43 show how fresh conventional OTFTs and HVOTFTs compare with those measured over 6 months later. The PAR and PAR/BZN based OTFTs show mobility degradation and less SCLC. The stale O_2 PAR based OTFTs also show mobility degradation and begin to show a substantial SCLC not present in the fresh devices. Attempting to explain these changes, consider the ratio of free charge density (ρ_f) and trapped charge density (ρ_t) in Equation 8.7. By reducing the free charge density (ρ_f), SCLC is reduced which may be the case for the PAR and PAR/BZN based OTFTs. For the O_2 PAR based OTFTs, a faster reduction in the trapped charge density (ρ_t) relative to the free charge density (ρ_f) will increase SCLC. Such a decrease in the trapped charge density (ρ_t) implies that the threshold voltage of the O_2 PAR based OTFTs should change with degradation and the surface treatment used to shift the threshold voltage is unstable. As the threshold voltage for the O_2 PAR based OTFT shifted negative by ~5 V, it is likely that the interface states or traps created by the O_2 plasma are being passivated as the OTFTs age, and the effective number of trapped charge decreases. With a smaller trap density (ρ_t), this SCLC will increase as Equation 8.6 predicts. With the O_2 PAR based OTFTs showing substantial instability, efforts should be spent developing the HVOTFT technology with the PAR/BZN or an insulator with a similar κ and stable surface, that shows

223

FIGURE 8-41: A comparison between the Output Characteristics of a fresh conventional OTFT and HVOTFT to a stale OTFT and HVOTFT. The insulator is PAR. The channel length (L)=10 μm and channel width (W)=250 μm with a 20 μm offset at the drain (OV20020).

FIGURE 8-42: A comparison between the Output Characteristics of a fresh conventional OTFT and HVOTFT to a stale OTFT and HVOTFT. The insulator is O_2 PAR. The channel length (L)=10 μm and channel width (W)=250 μm with a 20 μm offset at the drain (OV20020).

reasonable stability, less susceptible to high field effects due to the high-κ insulator and with a smaller threshold voltage compared to the PAR based OTFTs.
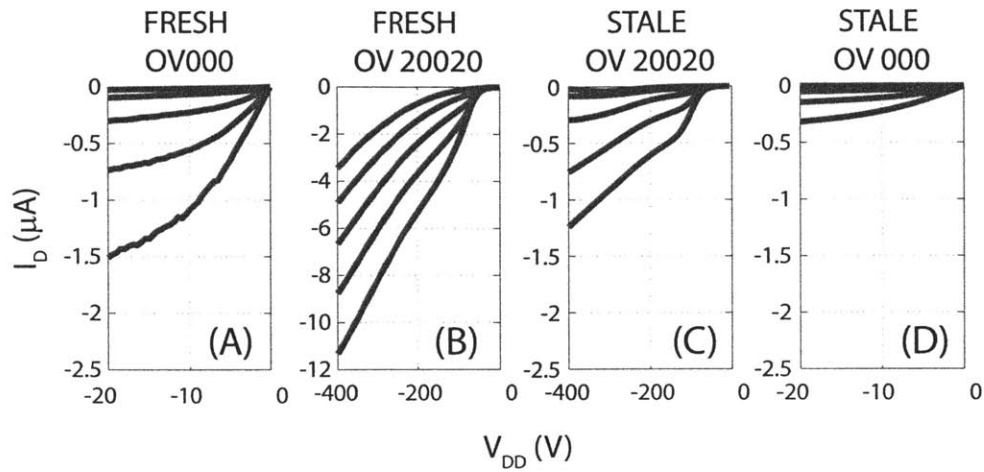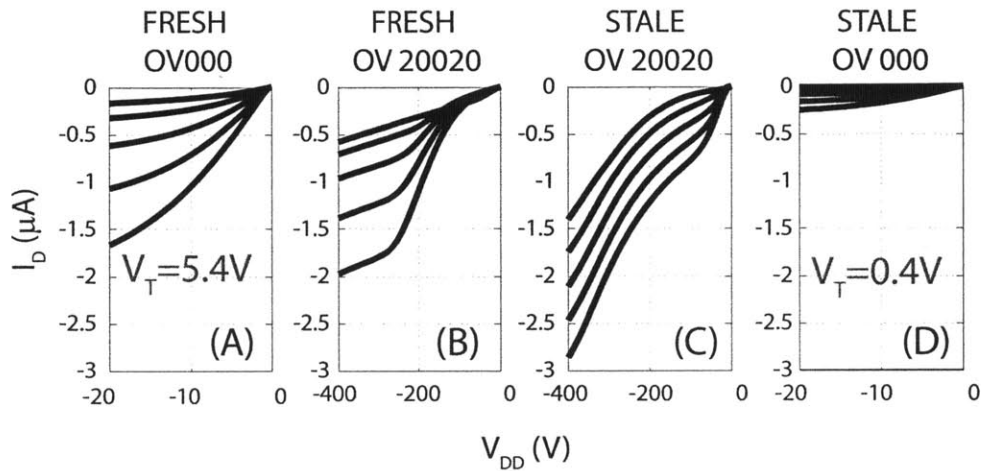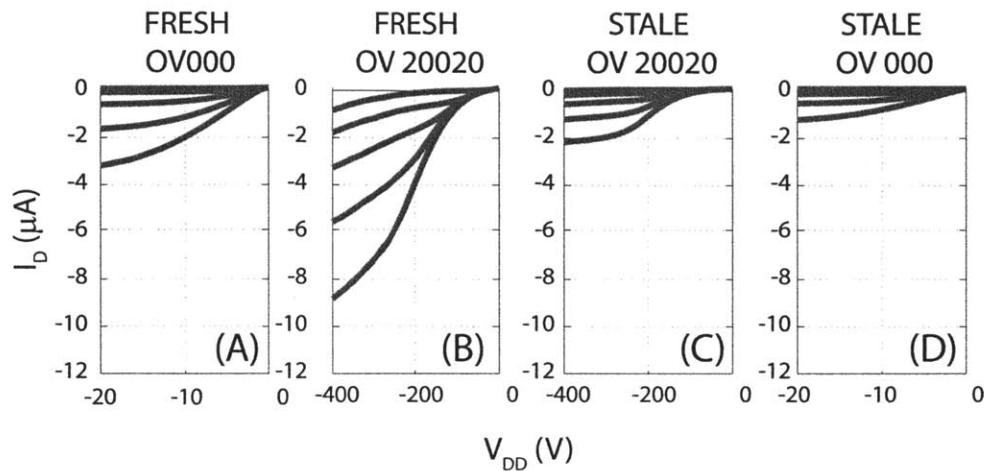
FIGURE 8-43: A comparison between the Output Characteristics of a fresh conventional OTFT and HVOTFT to a stale OTFT and HVOTFT. The insulator is PAR/BZN. The channel length (L)=10 μm and channel width (W)=250 μm with a 20 μm offset at the drain (OV20020).

8.5   CONCLUSION

Qualitatively, the HVOTFT current voltage behavior follows the simple modifications to the Si Long Channel MOSFET Model. The HVOTFTs in this work show non-saturation behavior due to SCLC, V_T rolloff and channel length modulation, an instability created by large fringing fields at the transition of the gate and ungated semiconductor region, and a non linear resistance in the offsets. The fundamental physical carrier transport in pentacene which is not completely understood makes it is difficult to develop a comprehensive analytical model for these HVOTFTs at this time. Different device geometry, gate insulator materials, and different sized offsets, and a field plate should be used to further assess these complications to determine how effectively they can be mitigated and controlled. Of the three insulators evaluated, the PAR performed the worst showing both SCLC and channel length modulation. Fresh O_2 PAR based OTFTs showed little SCLC but this was not long standing as stale devices showed substantial SCLC and non-saturation. The PAR/BZN device showed less SCLC compared to the PAR based device and channel length modulation. The instability created by large fringing fields at the transition of the gate and ungated semiconductor region could be mitigated by a field plate as shown by Martin et al. and Shaw et al [33, 34]. Further, efforts should be made to develop a model to predict maximum operating voltages for these devices.

The most substantial contribution of this work is the demonstration that organic semiconductors are viable in HVTFTs on flexible media. The HVOTFTs can be described with FET models developed for Si-based short channel devices, operate similarly to a-Si HVTFTs, and can be integrated with MEMS just as easily.

TABLE 8.8: Comparison of the performance of various High Voltage TFTs. All other HVTFTs are Si-based except for those demonstrated in this work.

Source	Unagami et al. [1]	Martin et al. [2]	Karim et al. [3]	Chow et al. [6]	This Work
Structure	Offset Drain and Source	Offset Drain	Offset Drain Soft Contact	Offset Drain	Offset Drain and Source
Max. Temp. °C	1100	NS[8]	260	<350	130
Semiconductor	poly-Si	a-Si	a-Si	a-Si	pentacene
Insulator t_{ox} (nm)	SiO$_2$ 150	SiN 300	SiN 250	SiN 300	Various 350-500
V_T (V)	2.7	1-2	4.5	<5	-1.5-+5.4
Max V_{DD} (V)	400	500	NS	300-800	500
L (μm)	10	5	23	9	5-10
Offset Length (μm)	5-20	15	NS	6-100	10-20
Saturation	N	Y	Y	Y	N
Year	1988	1993	2004	2005	2012

[8]Not Specified

8.6 SUMMARY

CONVENTIONAL TRANSISTORS

- Functional and reproducible TFTs have been demonstrated.

- Energy band diagrams are proposed for OTFT built from PAR, O$_2$ PAR, and PAR/BZN based OTFTs.

- The PAR and O$_2$ PAR device have high "off" currents and a large sub-threshold swing. Poor gate control is the suspected cause for this in the PAR device and parasitic conduction in the back channel of the O$_2$ PAR device or dues to incomplete patterning.

- Heat associated with the patterning process degrades pentacene performance due to the appearance more bulk phase pentacene, which has lower carrier mobility.

- The O$_2$ plasma surface treatment is sensitive to the solvents used to strip the resist after patterning.

HIGH VOLTAGE ORGANIC THIN FILM TRANSISTOR

- High Voltage Organic Thin Film Transistors are demonstrated. The devices did not show ideal current saturation. The non saturating output characteristic is attributed to high field effects; specifically space-charge-limited current, V_T rolloff, and channel length modulation.

- Fresh PAR and the PAR/BZN based devices showed space charge limited current and channel length modulation, while the O$_2$ PAR based OTFTs

showed only channel length modulation. It is believed that space-charge-limited current in the O_2 PAR based OTFTS is suppressed by the excessive traps at the insulator/semiconductor interface used to shift the threshold voltage.

- There is an instability brought about by the high electric field at transition from the gated to ungated region that is similar to that reported in a-Si HVTFTs. This instability impacts device transport behavior, is quantifiable (V_x), and is reversible.

- Upon accounting for space charge limited current and channel length modulation HVOTFTs showed more ideal output and current saturation behavior.

- Regarding stability with the time spent in ambient from device completion, the O_2 PAR based devices are the most unstable. Specifically, these devices begin to suffer from SCLC similar to the fresh PAR based OTFTs. The PAR and PAR/BZN based OTFTs showed decrease carrier mobility however, better saturation behavior with a decrease in SCLC.

8.7 REFERENCES

[1] T. Unagami and O. Kogure, "High-voltage TFT fabricated in recrystallized poly-crystalline silicon," *IEEE Transactions on Electron Devices*, vol. 35, pp. 314–319, March 1988.

[2] R. A. Martin, V. M. Da Costa, M. Hack, and J. G. Shaw, "High-voltage amor-phous silicon thin-film transistors," *IEEE Transactions on Electron Devices*, vol. 40, no. 3, pp. 634–644, 1993.

[3] K. S. Karim, P. Servati, and A. Nathan, "High voltage amorphous silicon TFT for use in large area applications," *Microelectronics Journal*, vol. 35, no. 3, pp. 311–315, 2004.

[4] W. Zhao, J. Law, D. Waechter, Z. S. Huang, and J. A. Rowlands, "Digital radiology using active matrix readout of amorphous selenium: Detectors with high voltage protection," *Medical Physics*, vol. 25, no. 4, pp. 539–549, 1998.

[5] N. Kim, "Fabrication of silicon field emitter arrays combined with HVTFT at low temperature," *SMDL Annual Report, School of Engineering, Seoul National University*, 1999.

[6] E. A. Chow, J. P. Lu, J. Ho, C. W. Shih, D. De Bruyker, M. Rosa, and E. Peeters, "High voltage thin film transistors integrated with MEMS," *Sensors and Actuators a-Physical*, vol. 130, pp. 297–301, 2006.

[7] A. Wang, I. Kymissis, V. Bulovic, and A. Akinwande, "Tunable threshold volt-age and flatband voltage in pentacene field effect transistors," *Applied Physics Letters*, vol. 89, no. 11, p. 112109, 2006.

[8] Y. Choi, I. D. Kim, H. L. Tuller, and A. I. Akinwande, "Low-voltage organic tran-sistors and depletion-load inverters with high-κ pyrochlore BZN gate dielectric on polymer substrate," *IEEE Transactions on Electron Devices*, vol. 52, no. 12, pp. 2819–2824, 2005.

[9] D. Guo, S. Ikeda, K. Saiki, H. Miyazoe, and K. Terashima, "Effect of anneal-ing on the mobility and morphology of thermally activated pentacene thin film transistors," *Journal of Applied Physics*, vol. 99, no. 9, pp. 094502–7, 2006.

[10] W. Y. Chou, Y. S. Mai, H. L. Cheng, C. Y. Yeh, C. W. Kuo, F. C. Tang, D. Y. Shu, T. R. Yew, and T. C. Wen, "Correlation of growth of pentacene films at various gas ambience conditions to organic field-effect transistor characteristics," *Organic Electronics*, vol. 7, no. 6, pp. 445–451, 2006.

[11] T. Ji, S. Jung, and V. K. Varadan, "On the correlation of postannealing induced phase transition in pentacene with carrier transport," *Organic Electronics*, vol. 9, no. 5, pp. 895 – 898, 2008.

[12] S. Steudel, K. Kris, Myny, S. De Vusser, J. Genoe, and P. Heremans, "Patterning of organic thin film transistors by oxygen plasma etch," *Applied Physics Letters*, vol. 89, no. 18, p. 183503, 2006.

[13] L. Shang, L. Ming, T. Deyu, L. Ge, L. Xinghua, and J. Zhuoyu, "Low-voltage organic field-effect transistor with PMMA/ZrO_2 bilayer dielectric," *IEEE Transactions on Electron Devices*, vol. 56, no. 3, pp. 370–376, 2009.

[14] D. K. Hwang, M. S. Oh, J. M. Hwang, J. H. Kim, and S. Im, "Hysteresis mechanisms of pentacene thin-film transistors with polymer/oxide bilayer gate dielectrics," *Applied Physics Letters*, vol. 92, no. 1, pp. 013304–3, 2008.

[15] A. L. Deman and J. Tardy, "Stability of pentacene organic field effect transistors with a low-κ polymer/high-κ oxide two-layer gate dielectric," *Materials Science and Engineering: C*, vol. 26, no. 23, pp. 421–426, 2006.

[16] N. Wrachien, A. Cester, A. Pinato, M. Meneghini, A. Tazzoli, G. Meneghesso, J. Kovac, J. Jakabovic, and D. Donoval, "Threshold voltage instability in organic TFT with SiO_2 and SiO_2/parylene-stack dielectrics," in *2009 IEEE International Reliability Physics Symposium*, pp. 109–116, 2009.

[17] K. O. Lee and T. T. Gan, "Space-charge-limited currents in evaporated-films of pentacene," *Physica Status Solidi a-Applied Research*, vol. 43, no. 2, pp. 565–571, 1977.

[18] K. Tsukagoshi, F. Fujimori, T. Minari, T. Miyadera, T. Hamano, and Y. Aoyagi, "Suppression of short channel effect in organic thin film transistors," *Applied Physics Letters*, vol. 91, no. 11, p. 113508, 2007.

[19] Specialty Coating Systems, "SCS Parylene Properties." Promotional brochure, 2010.

[20] J. Collet, O. Tharaud, A. Chapoton, and D. Vuillaume, "Low-voltage, 30 nm channel length, organic transistors with a self-assembled monolayer as gate insulating films," *Applied Physics Letters*, vol. 76, no. 14, pp. 1941–1943, 2000.

[21] M. D. Austin and S. Y. Chou, "Fabrication of 70 nm channel length polymer organic thin-film transistors using nanoimprint lithography," *Applied Physics Letters*, vol. 81, no. 23, pp. 4431–4433, 2002.

[22] Y. Zhang, J. Petta, S. Ambily, Y. Shen, D. Ralph, and G. Malliaras, "30 nm channel length pentacene transistors," *Advanced Materials*, vol. 15, no. 19, pp. 1632–1635, 2003.

[23] L. Wang, D. Fine, T. Jung, D. Basu, H. von Seggern, and A. Dodabalapur, "Pentacene field-effect transistors with sub-10-nm channel lengths," *Applied Physics Letters*, vol. 85, no. 10, pp. 1772–1774, 2004.

[24] J. Lee, P. Chang, J. Liddle, and V. Subramanian, "10-nm channel length pentacene transistors," *IEEE Transactions on Electron Devices*, vol. 52, pp. 1874 – 1879, Aug. 2005.

[25] J. N. Haddock, X. Zhang, S. Zheng, Q. Zhang, S. R. Marder, and B. Kippelen, "A comprehensive study of short channel effects in organic field-effect transistors," *Organic Electronics*, vol. 7, no. 1, pp. 45–54, 2006.

[26] Y. Chen and I. Shih, "Scaling down of organic thin film transistors: short channel effects and channel length-dependent field effect mobility," *Journal of Materials Science*, vol. 44, pp. 280–284, 2009.

[27] T. Hirose, T. Nagase, T. Kobayashi, R. Ueda, A. Otomo, and H. Naito, "Device characteristics of short-channel polymer field-effect transistors," *Applied Physics Letters*, vol. 97, no. 8, p. 083301, 2010.

[28] P. N. Murgatroyd, "Theory of space-charge-limited current enhanced by Frenkel effect," *Journal of Physics D: Applied Physics*, vol. 3, no. 2, p. 151, 1970.

[29] N. Mott and R. Gurney, *Electronic processes in ionic crystals*. Dover books on chemistry and physical chemistry, Dover Publications, 1964.

[30] W. D. Gill, "Drift mobilities in amorphous charge-transfer complexes of trinitrofluorenone and poly-n-vinylcarbazole," *Journal of Applied Physics*, vol. 43, no. 12, pp. 5033–5040, 1972.

[31] B. G. Streetman and S. K. Banerjee, *Solid state electronic devices*. Pearson Prentice-Hall, 2009.

[32] L. Yau, "A simple theory to predict the threshold voltage of short-channel IGFET's," *Solid-State Electronics*, vol. 17, no. 10, pp. 1059 – 1063, 1974.

[33] R. Martin, P. K. Yap, M. Hack, and H. Tuan, "Device design considerations of a novel high voltage amorphous silicon thin film transistor," in *1987 International Electron Devices Meeting*, vol. 33, pp. 440 – 443, 1987.

[34] J. G. Shaw, M. G. Hack, and R. A. Martin, "Metastable effects in high-voltage amorphous silicon thin-film transistors," *Journal of Applied Physics*, vol. 69, no. 4, pp. 2667–2672, 1991.

[35] C.-L. Fan, T.-H. Yang, and C.-Y. Chiang, "Performance degradation of pentacene-based organic thin-film transistors under positive drain bias stress in the atmosphere," *IEEE Electron Device Letters*, vol. 31, pp. 887 –889, aug. 2010.

[36] C. Pannemann, T. Diekmann, and U. Hilleringmann, "Degradation of organic field-effect transistors made of pentacene," *Journal of Materials Research*, vol. 19, no. 7, pp. 1999–2002, 2004.

[37] M. Rapisarda, D. Simeone, G. Fortunato, A. Valletta, and L. Mariucci, "Pentacene thin film transistors with (polytetrafluoroethylene) PTFE-like encapsulation layer," *Organic Electronics*, vol. 12, no. 1, pp. 119 – 124, 2011.

Chapter 9

Conclusions and Future Work

9.1 MAJOR FINDINGS

In this work, a device technology platform has been developed and evaluated for integrated circuits based on OTFTs and optimized to operate at low and high voltages. Limits imposed by integration were identified; some of which are not technically insurmountable. Two insulators for low voltage (Chapter 6) applications and three insulators for high voltage (Chapter 8) applications were evaluated for their efficacy as gate insulators. These investigations illustrate both the importance and necessity of full device integration. This dissertation reports the following.

1. A scalable, low temperature ($<130°C$), fully photolithographic, fabrication process has been developed. This process integrates OTFTs that feature the high-κ (40) gate insulator BZN ($Bi_{1.5}Zn_1Nb_{1.5}O_7$), and two distinct threshold voltages (V_T) on the same substrate. Materials characterization reveals conditions necessary for integration in this fashion. Surface treatments applied to the surface of the insulator are used to establish two distinct threshold voltages. In the case of the low voltage BZN-based insulators, a thin parylene-C film serves as the threshold voltage shifting surface treatment and it is patterned by O_2 plasma. For the high voltage insulators, O_2 plasma is used to create dangling bonds on the surface of a parylene-C insulator before the deposition of the semiconductor layer. These dangling bonds serve as interface states that shift the threshold voltage [1]. A composite PAR/BZN insulator stack is also used to shift the threshold voltage and increase drive currents for the high voltage OTFT. Key observations regarding the integration of OTFT in this dissertation are listed below.

   (a) O_2 plasma was used to either define or create a surface treatment. O_2 plasma alters the composition on the surface of BZN ($Bi_{1.5}Zn_1Nb_{1.5}O_7$ by

233

making it O-rich. Exposure to O_2 plasma resulted in a decrease in surface roughness for BZN and an increase in surface roughness for parylene-C. Last, O_2 plasma increased the surface energy for both BZN and parylene-C surfaces.

(b) For this fabrication process, surface roughness has more impact on the microstructure of the pentacene followed by surface energy.

(c) The carrier transport properties of pentacene degrades as a result of photolithography. X-Ray Diffraction and Atomic Force Microscopy revealed the formation of the low mobility bulk phase of pentacene as a result of the heat generated during bakeout. The formation of bulk phase pentacene may be limited by optimizing the bakeout process.

(d) Solvents are unavoidable when patterning with photolithography. Solvents used to strip the resist decreased the surface energy of the O_2 plasma treated parylene-C. This indicates a modification of the interface states or dangling bonds that shift the threshold voltage.

2. An existing technology developed by Choi et al. [2]. for low voltage applications was enhanced to allow the fabrication of simple integrated circuits using photolithography. This allowed OTFTs with two distinct threshold voltages, depletion-mode (V_T >0 V) and enhancement-mode (V_T <0 V) to be integrated into circuits. These operating voltages for these OTFTs are below $|5V|$. Using this technology platform, simple integrated circuits were demonstrated. The resulting logic inverters operate at power supply voltages that are less than 8V and 11-stage ring oscillator operate at a power supply voltage that is less than 12 V.

3. High-κ insulator BZN ($Bi_{1.5}Zn_1Nb_{1.5}O_7$) used as the gate insulator suffers from low breakdown fields. As dielectric breakdown has a statistical nature, the reliability of BZN was evaluated with time dependent dielectric breakdown (TDDB) and time zero dielectric breakdown (TZDB) stress measurements which are commonly used to evaluate dielectric breakdown in Si-based microelectronics. The stress tests revealed an initial non-fatal breakdown occurred at critical charge fluence ($Q_{BD} \approx 2 \times 10^{-6} \ C/cm^2$) which can be related to the trap density ($\rho_{BD} \approx 1.5 \times 10^{16} \ C/cm^3$). Prior to breakdown, conduction occurs via Schottky Emission with a barrier height (ϕ_B)$\approx$1 eV for BZN on Au. Initial breakdown is characterized by a change in dominant conduction mechanisms beyond a critical trap density (ρ_{BD}), from Schottky Emission to a trap assisted transport.

4. High voltage organic thin film transistors (HVOTFTs) capable of switching high voltages ($|V_{DD}|$ >300 V) using low controlling voltages ($|V_G| \leq 20$ V) were demonstrated. High voltage operation is enabled by offsetting the source and/or drain electrodes from the gate to reduce the electrostatic field (voltage drop)

across the channel. Three different gate insulators were evaluated (1) parylene-C, (2) O_2 plasma treated parylene-C and (3) a composite insulator stack consisting of high-κ (BZN $(Bi_{1.5}Zn_1Nb_{1.5}O_7)$, low-$\kappa$ (parylene-C) dielectrics. At lower supply voltages ($|V_{DD}|$ <100 V), the device current scales as expected with the location and size of the source and/or drain electrode offset. At high operating voltages, ($|V_{DD}|$ >300 V), the HVTOFT showed clear gate control.

However as a result of the offset source and drain structure and high fields, two distinct non-idealities were noted. HVOTFT showed non-saturating current behavior that can be analogized to "short channel effects" seen in both short channel FETs and a metastable charge injection barrier also seen with a-Si based HVTFTs. Literature suggests that both the high field effects and metastable charge injection can be modeled to predict current voltage behavior and facilitate device design.

The work presented in this dissertation built on prior work on organic TFT device integration. The key developments that enabled this work are listed below.

- The use of BZN and parylene-C surface treatment in OTFTs was first reported by Choi et al. in 2005 [2].

- An account of O_2 plasma being used to shift V_T in OTFTs was reported by Wang et al. in 2006 [1].

- The processes used to build devices are developed and modified from the reports of similar processes and devices from Kymissis et al. in 2005 [3] and Nausieda et al [4] in 2011.

- The offset drain structure used in Si-based TFTs for HVTFTs were first reported for poly-Si in 1988 by Unagami et al. [5] and for a-Si in 1986 by Tuan [6] and further developed by researchers at the Palo Alto Research Center [7, 8, 9].

9.2 FUTURE WORK

The ultimate goal of this dissertation is to demonstrate the integration of OTFT devices into simple functional circuits. This successful demonstration also points to how device performance and reliability can be improved in OTFTs and HVOTFTs. Three areas are identified for the continued improvement of this technology.

9.2.1 Advancements in Device Integration

BZN/PAR Insulator for More Reliable Low Voltage Dual V_T OTFTs

PAR/BZN and pBZN show similar device performance as shown in Figure 9-1. The breakdown resistance of parylene-C is 2-4 MV/cm while the breakdown resistance for BZN is ~0.1 MVcm. The PAR/BZN composite insulator was pursued as means to

FIGURE 9-2: Proposed insulators for a reliable dual V_T integrated OTFT technology
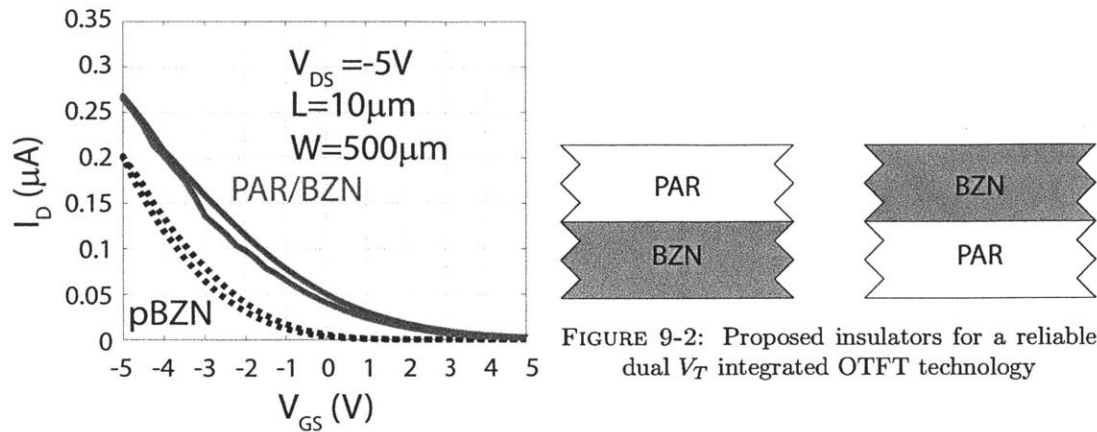
FIGURE 9-1: Transfer Characteristics comparing PAR/BZN and pBZN insulators.

increase the dielectric constant of the gate insulator without sacrificing breakdown resistance. The deposition of BZN on top of parylene-C to create a composite insulator, BZN/PAR (the opposite or PAR/BZN) should be explored. The likely result would be a positive shift in threshold voltage as devices with patterned pentacene on BZN had a positive threshold voltage. If a PAR/BZN and a BZN/PAR could be integrated on the same wafer, this may lead to another approach for accomplishing a dual V_T technology with low operating voltages. The benefit of using such a composite insulator for a low voltage dual V_T technology is the added gate reliability as PAR/BZN did not show substantial leakage or breakdown at higher operating voltages (V_{GS}=-20 V).

Field Plate for HVOTFT

The HVOTFTs showed a metastable charge injection barrier which is indicated by V_x in Figure 9-3. A similar instability was reported in a-Si based HVTFT and was attributed to trap generation in response to large fringing fields at the transition from the gated region to the ungated region in the semiconductor [7, 10]. Martin et al. and Shaw et al. used a field plate to the minimize size of this instability [7, 10].

Essentially, the field plate is allowing more charge to accumulate in the transition region. The excess charge effectively shortens the offset without increasing the electric field, such that the applied V_{DD} allows I_D to rise faster (smaller V_x). Secondly, the excess charge responds to the fringing fields such that fewer traps are generated and therefore, a smaller injection barrier is created [10].

The cause of the metastable charge injection in pentacene is unconfirmed. As was the case with the a-Si HVTFTs, device simulations can be used to verify if the source of the instability in HVOTFTs has the same origin as the instability in a-Si HVTFTs
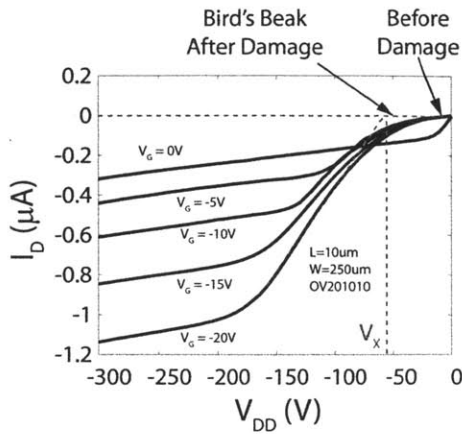
236

FIGURE 9-3: HVOTFT showing injection barrier or Birds' Beak which is quantified by V_x
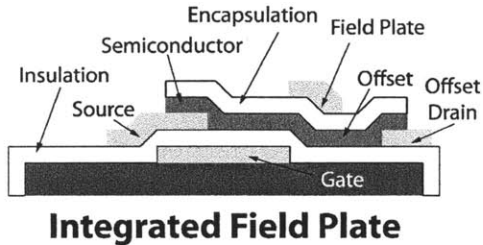
Integrated Field Plate

FIGURE 9-4: HVOTFT with Field Plate

(i.e. trap generated due to large fringing fields) [7, 10]. If this is the case, integrating a field plate should solve this instability as was demonstrated in the a-Si HVTFTs. Adding a field plate requires another deposition and patterning process. The HVOTFTs and the current fabrication process are compatible with the proposed field plate addition.

Flexible Substrates

The devices reported in this work are fabricated on rigid glass substrates but this is not a requirement as the materials and fabrication process used to build the devices are compatible with flexible substrates. Further, all of the processes used to build these devices occur at low temperature which maintains a compatibility with flexible substrates. There are vacuum compatible flexible substrates such as Kapton as shown in Figure 9-5, which are compatible with the processes used to build these devices. Therefore, this fabrication process could be immediately implemented on flexible substrates, such as Kapton. This is would be a key demonstration required to make these technologies more ready for tangible applications requiring low voltage and/or high voltage integrated devices and circuits on a flexible media.
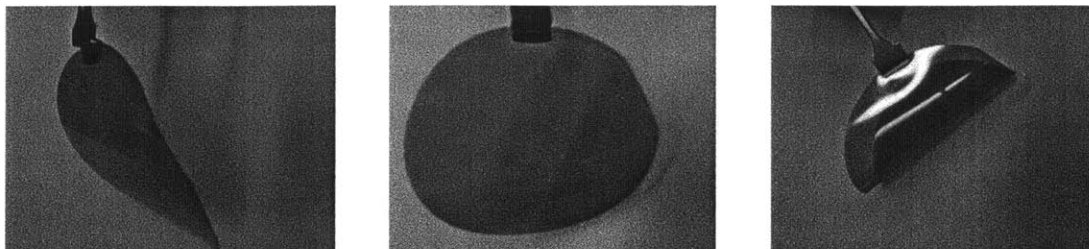
FIGURE 9-5: Flexible Kapton 100 mm Wafer Shaped Substrate

237

9.2.2 OTFT Device Model Development

Modeling V_T Shift due to Encapsulation

In Chapter 6, it was concluded that the encapsulation in addition to the semiconductor/insulator surface treatment is responsible the difference in threshold voltage in the BZN and pBZN based OTFTs. A shift in threshold voltage with encapsulation is in agreement with Jia et al. and Kymissis et al. who attribute the shift to unintentional doping [3, 11]. A modification to V_T was proposed to account for additional charges due to the parylene-C encapsulation needed for patterning (Equation 9.1). The additional terms that appear as a result of the encapsulation are Q_{semi}, $Q_{encap,it}$, and Q_{encap}.

$$V_T = (\phi_m - \phi_S) - \left(\frac{Q_{OX} + Q_{it} + Q_{semi} + Q_{encap,it} + Q_{encap}}{\kappa \epsilon_o} \right) t_{ox} \qquad (9.1)$$

Where,

ϕ_M and ϕ_S: work functions of the gate metal and the semiconductor

ϵ_o: permittivity of free space

κ: dielectric constant of the insulator

Q_{it}: surface charge density at the interface between insulator and the semiconductor.

Q_{OX}: charge density per unit volume in the insulator integrated over the thickness of the insulator. See the Note below.

Q_{semi}: charge density per unit volume in the semiconductors integrated over the thickness of the insulator. See the Note below.

$Q_{encap,it}$: surface charge density at the interface between semiconductor and the encapsulation.

Q_{encap}: charge density per unit volume in the encapsulation integrated over the thickness of the encapsulation. See the Note below.

t_{OX}: thickness of the insulator

****NOTE:* Q_{OX}, Q_{semi}, and Q_{encap} *are not sheet charges. They are the results to integrating charge volume density (ρ) over the thickness (t) of each respective region. By considering locations at interfaces, Q_{OX}, Q_{semi}, and Q_{encap} can be treated as sheet charges mathematically as indicated. See Appendix A for more detail.*

- $\underline{Q_{semi}}$ Suppose most of the traps in the bulk of the semiconductor are located in the grain boundaries as shown in Figure 9-6. As the microstructural evolution of thermally evaporated pentacene thin films follows the theory set forth by Venables et al., grain sizes and grain boundaries can be controlled by the substrate temperature and/or flux during deposition. Therefore, Q_{semi} is likely to be modified by varying deposition conditions that change grain sizes and distributions. By studying if and how the threshold voltage changes with grain structure in this system, it could be concluded if the charge in the semiconductor at the grain boundaries contribute to the shift in V_T as a result of encapsulation.
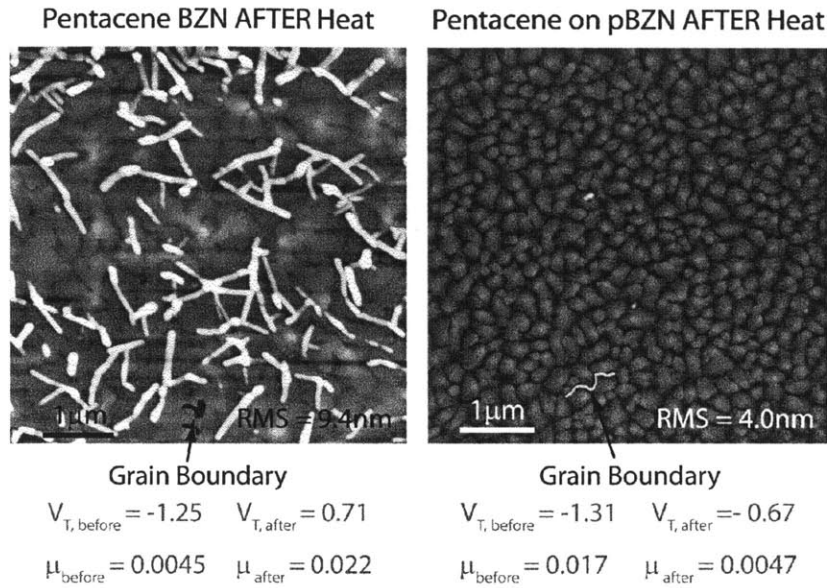
Pentacene BZN AFTER Heat

Pentacene on pBZN AFTER Heat

Grain Boundary

Grain Boundary

$V_{T, before} = -1.25$ $V_{T, after} = 0.71$

$V_{T, before} = -1.31$ $V_{T, after} = -0.67$

$\mu_{before} = 0.0045$ $\mu_{after} = 0.022$

$\mu_{before} = 0.017$ $\mu_{after} = 0.0047$

FIGURE 9-6: $V_{T,before}$ and μ_{before} refers to the threshold voltage and mobility before encapsulation and patterning. $V_{T,after}$ and μ_{after} refers to the threshold voltage after encapsulation and patterning. The OTFT with pentacene on BZN showed larger shift in V_T compred to the pBZN based devices. This cab be attributed the difference in grain structure and therefore Q_{semi} (i.e. $Q_{semi,BZN} \neq Q_{semi,pBZN}$) in addition to $Q_{encap,it}$ and Q_{encap}.

- $\underline{Q_{encap,}}$ The impact of Q_{encap} can be studied by using different encapsulations as shown in Figure 9-7 assuming the encapsulations have different bulk change densities and/or properties.

- $\underline{Q_{encap,it}}$ The impact of $Q_{encap,it}$ depends on both the grain structure the pentacene and the encapsulation. The grain structure of the pentacene will determine the area that the interface charges ($Q_{encap,it}$) are distributed over. As was shown in Chapter 6, the 3D and 2D growth modes have different rms roughnesses. Comparing the 3D and 2D growth modes, this implies a different effective area for which back channel interface charges are distributed over. Therefore, the magnitude of $Q_{encap,it}$ is likely related to the growth mode (3D vs. 2D) of the pentacene thin films. Given the divergent nature of organic/inorganic interfaces, using organic vs. inorganic encapsulation will likely give rise to dif-
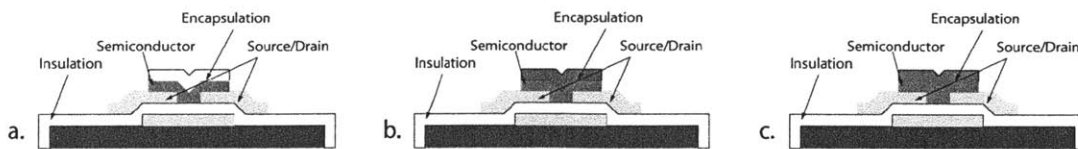

FIGURE 9-7: Different encapsulation materials for semiconductor layer patterning

239

ferent values of $Q_{encap,it}$ also and should be investigated in detail.

Developing an Analytical Model for HVOTFTs

Martin et al. offer an analytical model to determine the voltage drops across the ungated and gated semiconductor regions in the a-Si based HVTFT [7]. This relies heavily on knowing the density of states of the semiconductor as well as equilibrium charge densities, the distribution of deep localized states, and saturation current in the device. Upon building HVOTFTs that saturate well, a similar model should be developed for pentacene, beyond the modifications to the Si MOSFET Models proposed in Chapter 8.

9.2.3 Charge Trapping and Memory

Charge transport (I_D) can be altered in an OTFT by trapped charges. That is fundamental concept behind memory modules based on transistor and capacitive structures.

Floating Gate Organic Thin Film Transistor

In a floating gate structure (Kahng and Sze in 1967), a metal or conductive electrode is embedded and electrically isolated from or capacitively connected to all other components (gate, source, drain, channel) in the OTFT as shown in Figure 9-8. Charge can be collected on floating gate by applying a large voltage applied at the gate electrode. Current flows through a dielectric which surrounds the floating gate via Fowler-Nordheim tunneling, Schottky Emission, and Frenkel-Poole conduction [12, 13]. As the floating gate is embedded in a resistive material, charge can be stored on the floating gate for extended periods of time.
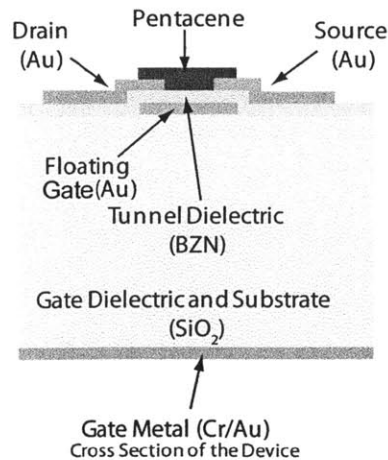

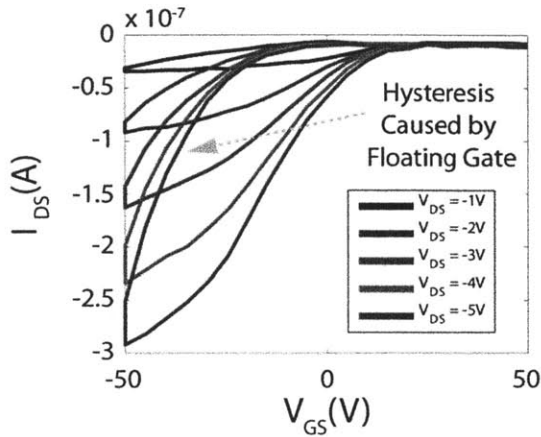FIGURE 9-8: Cross section of floating gate structure

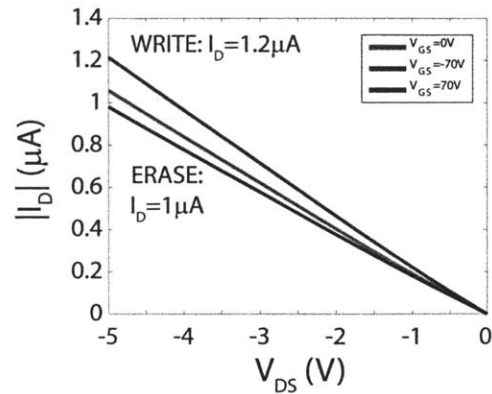FIGURE 9-9: Transfer Characteristic of floating gate structure. The channel length (L)=15 μm and the channel width (W)=500 μm

FIGURE 9-10: Output characteristics for floating gate structures based on BZN after write (-70 V) and erase (+70 V) $V_{GS} = $ - 5V

As BZN shows non-fatal breakdown at low electric fields, it may be a viable candidate as a tunneling dielectric for low voltage floating gate organic thin film transistors. Figure 9-9 shows the transfer characteristics of the floating gate structures depicted in Figure 9-8. The observed hysteresis in the transfer characteristics are indication of charges stored on the floating gate. In the case of a TFT, the presence of charge on the floating gate will change the threshold voltage of TFT, which will modify the drain current. This is shown in Figures 9-9 and 9-10.

Figure 9-11 shows how the charge on the floating gate evolves with time. The solid lines are the current measured at the source and drain. The dotted lines represent the current through the gate electrode. The various sweeps represent the writing voltage applied at the gate. The writing voltage is applied at ~10 seconds and removed at ~22 seconds. Upon removal of the writing voltage, the current through the gate (dotted line) drops to zero while the currents through the source and drain decay exponentially similar to a discharging capacitor. Integrating this current over time is a measure of the charge that was stored on the floating gate during writing.
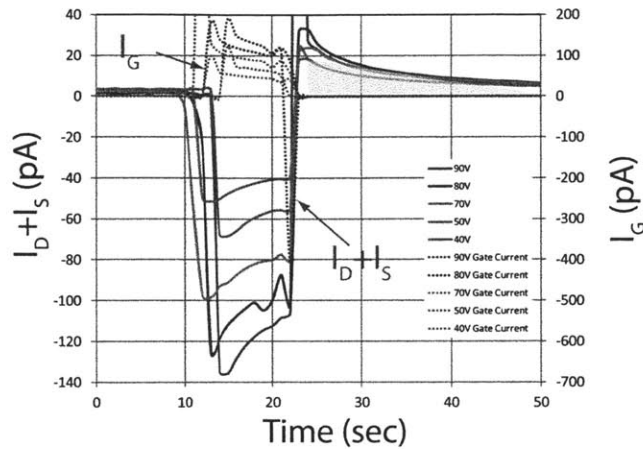
241

FIGURE 9-11: Transient behavior of floating gate structure. The floating gate stays charged for ~10 seconds after writing

Offset Drain Structures

Two components are necessary for a functional HVTFT, an offset source or drain electrode and a reliable gate insulator. As suspected in Chapter 8 for the HVOTFTs, traps are generated at the transition region between the gated and the ungated semiconductor regions. By using a less reliable high-κ insulator, high voltage operation is lost but traps are still generated in the transition region between the gated and ungated semiconductor as shown in Figure 9-12 even at low operating voltages. The effect of the trapped charge at low voltages is shown in Figure 9-13 with the hysteresis. Figure 9-14 shows the length of time charge remains trapped in the structure, such that I_D is modified.

Charge can be stored in these two different device structures, to the extent that current is affected. The charge in the floating gate discharges faster as shown in Figure 9-11 than the charge stored in the offset (Figure 9-14). However, the reversibility of the charge storage in the offset is not yet well understood. Success in understanding
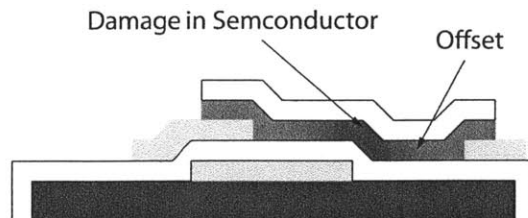

FIGURE 9-12: Cross-section of HVOTFT illustrating damage in the semiconductor at the edge of the gated region.
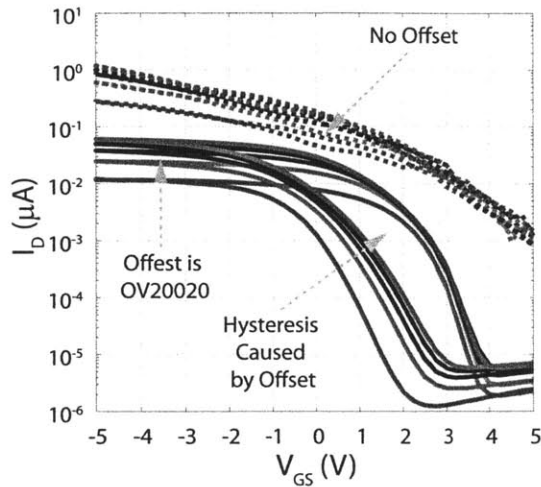
242

FIGURE 9-13: Transfer Characteristics comparing a conventional device and a device with the offset source and drain the channel length (L)=8μm and the channel width (W)=250μm V_{DD}= -1,-2,-3,-4, and -5 V
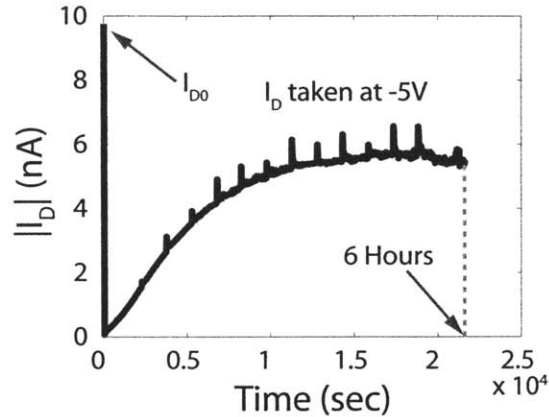
FIGURE 9-14: Evolution of I_D as function time as damage in semiconductor "heals" OV201010 the channel length (L)=8 μm and the channel width (W)=250 μm, V_G=-10V V_{DD}=30 V stress

the storage of charges would be a key development for low voltage non-volatile memory cells built with a fully integrated process. It would also be a key advancement for organic semiconductor based systems.

9.3 SUMMARY

To address the demand for more ubiquitous and multifunctional electronic systems a technology platform for integrated systems that can be built on a flexible media has been presented. A compatibility with a flexible media has been met by using an organic semiconductors pentacene and low temperature processing. To address the high operating voltages of pentacene-based TFTs, a high-κ gate insulator BZN is used in increase gate capacitance for more charge accumulation at lower voltages. As pentacene cannot reliably doped, devices with two distinct threshold voltages were integrated into circuits. Different and distinct threshold voltages are achieved by interface engineering with surface treatments at the semiconductor/insulators interface. Full integration is enabled by photolithographic patterning. Integrated circuits are demonstrated for two applications that differ by required driving voltages that spans two orders of magnitude (i.e. 5V for low voltage applications and >300 V for high voltage applications). The same materials are used for devices for each application which is enabled by full integration. This dissertation emphasizes the importance of considering fabrication processes and techniques used to build devices towards integration in addition to materials properties and performance.

9.4 REFERENCES

[1] A. Wang, I. Kymissis, V. Bulovic, and A. Akinwande, "Tunable threshold voltage and flatband voltage in pentacene field effect transistors," *Applied Physics Letters*, vol. 89, no. 11, p. 112109, 2006.

[2] Y. Choi, I. D. Kim, H. L. Tuller, and A. I. Akinwande, "Low-voltage organic transistors and depletion-load inverters with high-κ pyrochlore BZN gate dielectric on polymer substrate," *IEEE Transactions on Electron Devices*, vol. 52, no. 12, pp. 2819–2824, 2005.

[3] I. Kymissis, A. I. Akinwande, and V. Bulovic, "A lithographic process for integrated organic field-effect transistors," *Journal of Display Technology*, vol. 1, no. 2, pp. 289–294, 2005.

[4] I. Nausieda, K. K. Ryu, D. Da He, A. I. Akinwande, V. Bulovic, and C. G. Sodini, "Mixed-signal organic integrated circuits in a fully photolithographic dual threshold voltage technology," *IEEE Transactions on Electron Devices*, vol. 58, no. 3, pp. 865–873, 2011.

[5] T. Unagami and O. Kogure, "High-voltage TFT fabricated in recrystallized polycrystalline silicon," *IEEE Transactions on Electron Devices*, vol. 35, pp. 314–319, March 1988.

[6] H. C. Tuan, "Novel a-Si:H Thin Film High Voltage Transistor," in *MRS Proceedings*, vol. 70, p. 651, 1986.

[7] R. A. Martin, V. M. Da Costa, M. Hack, and J. G. Shaw, "High-voltage amorphous silicon thin-film transistors," *IEEE Transactions on Electron Devices*, vol. 40, no. 3, pp. 634–644, 1993.

[8] R. Martin, P. K. Yap, M. Hack, and H. Tuan, "Device design considerations of a novel high voltage amorphous silicon thin film transistor," in *1987 International Electron Devices Meeting*, vol. 33, pp. 440–443, 1987.

[9] M. Hack, A. Chiang, T. Huang, A. Lewis, R. Martin, H. Tuan, I. Wu, and P. Yap, "High-voltage thin film transistors for large area microelectronics," in *Electron*

Devices Meeting, 1988. IEDM '88. Technical Digest., International, pp. 252 –255, 1988.

[10] J. G. Shaw, M. G. Hack, and R. A. Martin, "Metastable effects in high-voltage amorphous silicon thin-film transistors," *Journal of Applied Physics*, vol. 69, no. 4, pp. 2667–2672, 1991.

[11] H. Jia, E. K. Gross, R. M. Wallace, and B. E. Gnade, "Patterning effects on poly (3-hexylthiophene) organic thin film transistors using photolithographic processes," *Organic Electronics*, vol. 8, no. 1, pp. 44 – 50, 2007.

[12] K. Kahng and S. Sze, "A floating gate and its application to memory devices," *Bell System Technical Journal*, vol. 46, no. 4, pp. 1288–1295, 1967.

[13] S. Lai, "Flash memories: where we were and where we are going," in *Electron Devices Meeting, 1998. IEDM '98 Technical Digest., International*, pp. 971 –973, dec 1998.

Appendix A

Derivation of Threshold Voltage
Accounting for Encapsulation

Consider the MIS stack to be a system of simple sheets of charge shown Figure A-1. This is representative of the MIS structure for OTFT containing the BZN insulator. For this section, Q will be in units of C/cm^2. The total charge in the entire system must be 0 ($Q_{TOT}=0$) and the source electrode is connected to ground. The total charge in the system is the addition of all charges density in all materials.
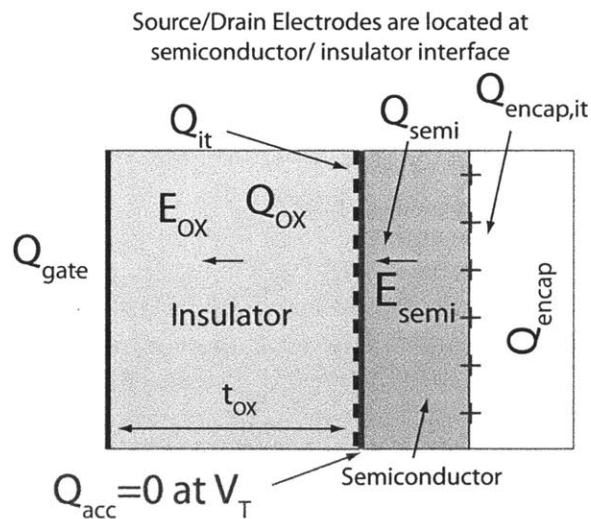

FIGURE A-1: Location and indentification of charges in the MIS capacitor.

$$Q_{TOT} = 0 \qquad \text{(A.1)}$$

$$Q_{gate} + Q_{OX} + Q_{it} + Q_{acc} + Q_{semi} + Q_{encap,it} + Q_{encap} = Q_{TOT} = 0 \qquad \text{(A.2)}$$

Where,

ϕ_M and ϕ_S: work functions of the gate metal and the semiconductor

ϵ_o: permittivity of free space

κ: dielectric constant of the insulator

ϵ_{OX}: $\kappa \times \epsilon_o$

Q_{it}: surface charge density at the interface between insulator and the semiconductor

Q_{OX}: charge density per unit volume in the insulator integrated over the thickness of the insulator.

Q_{semi}: charge density per unit volume in the semiconductors integrated over the thickness of the insulator.

$Q_{encap,it}$: surface charge density at the interface between insulator and the semiconductor.

Q_{encap}: charge density per unit volume in the encapsulation integrated over the thickness of the encapsulation.

t_{OX}: thickness of the insulator

Q_{OX}, Q_{semi}, and Q_{encap} are not sheet charges. However, by integrating (See Equation A.3) the charge volume density (ρ) over the thickness (t) of each region, and considering locations at interfaces, they can be treated as sheet charges mathematically.

$$Q = \int_0^t \rho \cdot dt \qquad \text{(A.3)}$$

The system at threshold is described by:

$$Q_{acc} = 0 \qquad \text{(A.4)}$$

Therefore, the solution for Gauss's Law for a sheet of charge is:

$$E = \frac{Q}{2\epsilon} \qquad \text{(A.5)}$$

Electric field at the gate electrode or through the oxide is:

$$\frac{Q_{gate}}{2\epsilon_{OX}} - \frac{Q_{OX}}{2\epsilon_{OX}} - \frac{Q_{it}}{2\epsilon_{OX}} - \frac{Q_{acc}}{2\epsilon_{OX}} - \frac{Q_{semi}}{2\epsilon_{OX}} - \frac{Q_{encap,it}}{2\epsilon_{OX}} - \frac{Q_{encap}}{2\epsilon_{OX}} = E_{OX} \qquad \text{(A.6)}$$

From Equation A.2 it follows that:

$$Q_{gate} = -Q_{OX} - Q_{it} - Q_{acc} - Q_{semi} - Q_{encap} - Q_{encap,it} \qquad \text{(A.7)}$$

Therefore the electric field in the oxide at the gate electrode is:

$$\frac{-Q_{OX} - Q_{it} - Q_{acc} - Q_{semi} - Q_{encap,t} - Q_{encap}}{2\epsilon_{OX}} - \frac{Q_{OX}}{2\epsilon_{OX}} - \frac{Q_{it}}{2\epsilon_{OX}}$$
$$- \frac{Q_{acc}}{2\epsilon_{OX}} - \frac{Q_{semi}}{2\epsilon_{OX}} - \frac{Q_{encap,it}}{2\epsilon_{OX}} - \frac{Q_{encap}}{2\epsilon_{OX}} = E_{OX} \qquad \text{(A.8)}$$

$$-\frac{Q_{OX}}{\epsilon_{OX}} - \frac{Q_{it}}{\epsilon_{OX}} - \frac{Q_{acc}}{\epsilon_{OX}} - \frac{Q_{semi}}{\epsilon_{OX}} - \frac{Q_{encap,it}}{\epsilon_{OX}} - \frac{Q_{encap}}{\epsilon_{OX}} = E_{OX}$$
$$\left(\frac{Q_{OX} + Q_{it} + Q_{acc} + Q_{semi} + Q_{encap,it} + Q_{encap}}{\epsilon_{OX}} \right) = -E_{OX} \qquad \text{(A.9)}$$

The definition of voltage is a potential difference:

$$V_A - V_B = \int_B^A \vec{E} \cdot \vec{dl} \qquad \text{(A.10)}$$

Integrating from source/drain electrodes (where accumulation charge enter the semi-conductor channel) to the gate electrode, through the gate oxide, V_{GS} is defined.

$$V_G - V_S = (\phi_m - \phi_S) + \int_S^G \vec{E_{OX}} \cdot \vec{dl} \qquad \text{(A.11)}$$

$$V_{GS} =$$
$$(\phi_m - \phi_S) - \int_S^G \left(\frac{Q_{OX} + Q_{it} + Q_{acc} + Q_{semi} + Q_{encap,it} + Q_{encap}}{\epsilon_{OX}} \right) \cdot \vec{dl} \qquad \text{(A.12)}$$

$$V_{GS} =$$
$$(\phi_m - \phi_S) - \left(\frac{Q_{OX} + Q_{it} + Q_{acc} + Q_{semi} + Q_{encap,it} + Q_{encap}}{\epsilon_{OX}} \right) t_{ox} \qquad \text{(A.13)}$$

By definition, at threshold, $Q_{acc} = 0$, where $V_{GS} = V_T$. The expression for threshold voltage has be modified to account for the extra interface and encapsulation charges, where Q_{semi}, $Q_{encap,it}$, are additional terms Q_{encap}.

$$V_T = (\phi_m - \phi_S) - \left(\frac{Q_{OX} + Q_{it} + Q_{semi} + Q_{encap,it} + Q_{encap}}{\epsilon_{OX}} \right) t_{ox} \qquad \text{(A.14)}$$