

MIT Open Access Articles

Light up the Future of Silicon Microprocessors

The MIT Faculty has made this article openly available. **Please share** how this access benefits you. Your story matters.

Citation: Liu, Jifeng, Mark Beals, Jurgen Michel, and Lionel Kimerling. "Light up the Future of Silicon Microprocessors." In ECS Transactions, 17-28. © 2009 ECS - The Electrochemical Society

As Published: <http://dx.doi.org/10.1149/1.3118927>

Publisher: The Electrochemical Society

Persistent URL: <http://hdl.handle.net/1721.1/79693>

Version: Final published version: final published article, as it appeared in a journal, conference proceedings, or other formally published context

Terms of Use: Article is made available in accordance with the publisher's policy and may be subject to US copyright law. Please refer to the publisher's site for terms of use.



Light up the Future of Silicon Microprocessors

Jifeng Liu, Mark Beals, Jurgen Michel and Lionel C. Kimerling

Microphotonics Center and Department of Materials Science and Engineering,
Massachusetts Institute of Technology, Cambridge, MA 02139

For decades, the performance of Si microprocessors has increased exponentially following "Moore's Law" by shrinking the dimensions of transistors. However, the progress in microchip performance has become stagnant since 2004 despite the continued device dimension shrinkage mainly due to power consumption and latency issues in traditional electronic interconnects that ended clock frequency scaling. It has become increasingly clear that parallelism is replacing traditional clock frequency scaling, and electronic-photonic synergy that takes the advantage of high bandwidth and energy-efficient photonic interconnects, is the key to high functionality extension of Moore's Law. We present an overview on the recent progress in Si photonic devices and their integration with CMOS fabrication process, including high performance waveguides, couplers, filters, modulators and photodetectors on a Si platform. Photonic data links based on these integrated photonic devices provide large bandwidth and low energy consumption for future generations of microprocessors.

The Quest for Electronic-Photonic Synergy

The performance of silicon integrated circuits (ICs) had been growing exponentially for nearly half a century by continuously shrinking the sizes of electronic devices for higher and higher levels of integration. However, power consumption and latency issues in traditional electronic interconnects have ended the clock frequency scaling of microprocessors since 2004 and induced a large gap between performance enhancement and transistor scaling (1). Simply increasing the number of transistors per chip will no longer significantly improve the overall functionality of the microprocessors since the major bottleneck limiting the system performance is the interconnection instead of the transistors themselves (2). In fact, as the cross-sectional area of metal wires decreases and the density of wires increases with the shrinkage of transistor dimensions, the electronic interconnection issue becomes more and more severe because both the resistance and the capacitance further increase, resulting in more RC delay, power consumption, and heat dissipation. Although low resistivity copper wires and low-k dielectric materials have been applied to alleviate the problem, they are unable to provide the ultimate solution. Therefore, interconnection technology with high bandwidth and low energy consumption is the key to further enhancement in the functionality of microchips. In order to keep the exponential growth in the performance of Si microprocessors, on the other hand, the scaling of clock frequency has to be replaced by scaling in parallelism. In fact, parallelism is already delivering an aggregate system performance enhancement of $2\times$ per year that outpaces the $2\times$ every eighteen months "Moore's Law" rate (3). Again, an energy-efficient and high bandwidth interconnection approach is critical for core-to-core

communications in future generations of multicore parallel processors with Tb/s capability.

Considering that optical interconnects have replaced electrical interconnects at a distance-bandwidth product of >10 Mb/s km, which is equal to 1 Tb/s cm, on-chip interconnects with cm distance and Tb/s data rate will naturally adopt a photonic approach (2). Different from electrons transporting through metallic wires, photons propagating in transparent optical waveguides dissipates no heat and involves no RC delay. In this sense, photons are the real “superconductors” for data transmission. Furthermore, wavelength division multiplexing (WDM) in photonic domain can provide multiple communication channels for different cores without any interference, which greatly improves the interconnection capacity and simplifies the programming in multicore processors (4). Due to these significant advantages over traditional electronic interconnection, silicon-based integrated photonics for electronic-photonic integrated circuits (EPICs) has been progressing rapidly in recent years. The synergy of electronic and photonic devices on a single Si chip combines the merits of electrons in data processing and the merits of photons in data transmission, which leads the path to a bright future for the microprocessors in the 21st century.

Integrated Photonic Circuits on Si

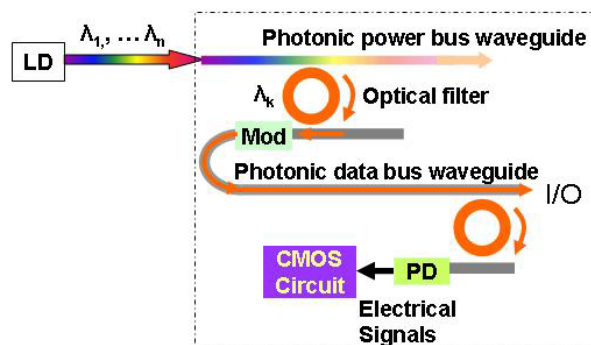


Figure 1. Schematics of an integrated photonic circuit for on-chip optical interconnect.

Traditionally, most photonic interconnection systems are composed of discrete optical devices, which is very similar to the status of electronics technology before the age of ICs. Analogous to the advantages of electronic ICs vs. discrete devices, integrated photonics is able to achieve orders of magnitude improvement in system performance at the same cost compared to conventional discrete optical devices (5). Figure 1 schematically shows the major components of integrated photonic circuits for data transmission. A laser source provides optical power to the microprocessor through the photonic power bus, similar to the way the electrical source powers the electronic circuits. A wavelength multiplexed laser source can be adopted for on-chip WDM which multiplies the capability of photonic interconnection. A particular wavelength is selected by an optical filter as a specific channel, and it is encoded with photonic signals by a modulator (Mod) before being delivered though the optical data bus. Multiple wavelength channels can share the same data bus without interference. At each receiving port, signals from a specific wavelength channel are filtered out and input to a photodetector (PD) so that the photonic signals is converted into the electrical domain and passed on to CMOS logic circuitry for data processing. As we can see in Figure 1, waveguides, couplers and filters are the major

passive devices while photodetectors, modulators and lasers are the key active devices for integrated photonic circuits. Next we will discuss the recent advances and achievements in these devices in detail.

Passive Photonic Devices

Waveguides. Photonic waveguides are equivalent to the electric wires on-chip. To achieve a large scale of photonic integration with $>10^6$ photonic devices/chip, it is crucial that the waveguides allow a small bending radius of a few μm without losing the optical confinement. High refractive index contrast between the core and cladding of the waveguides is necessary to satisfy this requirement. Low loss SiON/SiO_2 , $\text{Si}_3\text{N}_4/\text{SiO}_2$ and Si/SiO_2 waveguides with a core-cladding index difference of $\Delta n=0.3-2$ and a small bending radius of several μm have been demonstrated. Among them, Si/SiO_2 waveguides are the most suitable one for large scale integration because of the largest core/cladding index contrast that allows $\sim 1 \mu\text{m}$ bending radii. However, the large index contrast also makes Si/SiO_2 waveguides vulnerable to the scattering losses due to the roughness on the surfaces and sidewalls. Surface oxidation and etching has been developed to smooth the surfaces and sidewalls of Si waveguides and significantly reduce the scattering loss (6, 7). In particular, low temperature chemical oxidation and etching methods has been developed recently, which allows a significant reduction in the scattering loss of Si waveguides with negligible thermal budget (7). The propagation loss has been reduced to 0.35 dB/cm for crystalline Si waveguides.

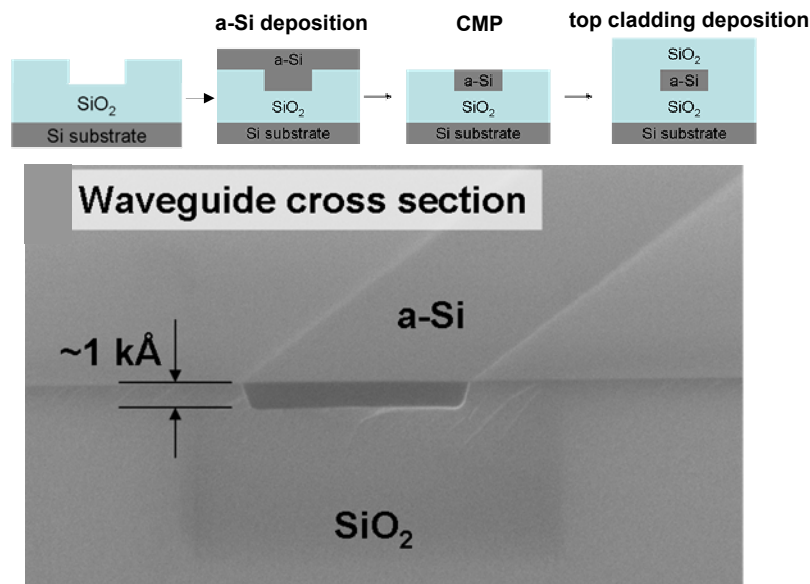


Figure 2. Process flow (upper part) and cross-sectional SEM picture (lower part) of a low loss a-Si channel waveguide fabricated by damascene process.

Although most of the low loss Si waveguides have been based on single crystalline Si (c-Si) so far to take the advantage of its zero material absorption loss at around 1550 nm, research on amorphous Si (a-Si) waveguides deposited by plasma enhanced chemical vapor deposition (PECVD) has also made significant progress in recent years (8,9). The material absorption due to the dangling bonds in a-Si has been reduced to nearly 0 by optimizing the PECVD recipe to incorporate atomic H for defect passivation. Thin SiN

cladding layers have been applied to prevent the outdiffusion of H from a-Si during processing and preserve the H passivation. Since the refractive index of SiN is between those of Si and SiO₂, these SiN cladding layers also help to reduce the electric field at the core/cladding interface and subsequently, the sensitivity of the scattering loss to the interface roughness. Very recently, a damascene process for single mode a-Si channel waveguides has been developed and a record-low propagation loss of 2.5 dB/cm has been achieved. In this process, a trench is etched into the SiO₂ cladding layer by reactive ion etching followed by dilute HF chemical etching for sidewall smoothing. An a-Si layer is deposited by PECVD to fill the trenches and then planarized by chemical mechanical polishing (CMP) to form the core of the waveguide (see Figure 2). Another SiO₂ is then deposited to form the upper cladding of the waveguide. Compared to the sidewall smoothing of Si, experimental results indicated that this approach is more effective in reducing the sidewall and surface roughness to decrease the scattering loss. These significant achievements in low loss a-Si waveguides make it possible to fabricate high index contrast waveguides in the upper interconnection level of microchips using back end of line (BEOL) processing and will eventually lead to 3D photonic-electronic integration.

Couplers. Coupling between fibers and waveguides is essential to launch external optical power source onto the microchip and to enable chip-to-chip optical interconnects. The major challenge here is the large difference in mode size ($\sim 100\times$) and effective index ($\Delta n_{\text{eff}} \sim 1$) between the optical fiber mode and the high index contrast waveguide mode on-chip. Different fiber-waveguide couplers have been designed, including inverse taper couplers (11), holographic lens couplers (10), and graded index lens couplers (12, 13). All these designs aim at an efficient mode conversion between the fiber mode and the waveguide mode. A very low fiber-to-waveguide coupling loss of <0.5 dB has been experimentally demonstrated with the optimized graded index lens coupler schematically illustrated in Figure 3a (13). In this structure, the parabolically graded index in the vertical direction guides the light to the waveguide layer at the bottom, while the lens and the taper focus the light in the horizontal direction to match the waveguide mode. An important advantage of this graded index lens coupler is that it allows a very low coupling loss of 0.4 ± 0.05 dB in a broad wavelength range of 1520-1630 nm with a short coupling length of 20 μm .

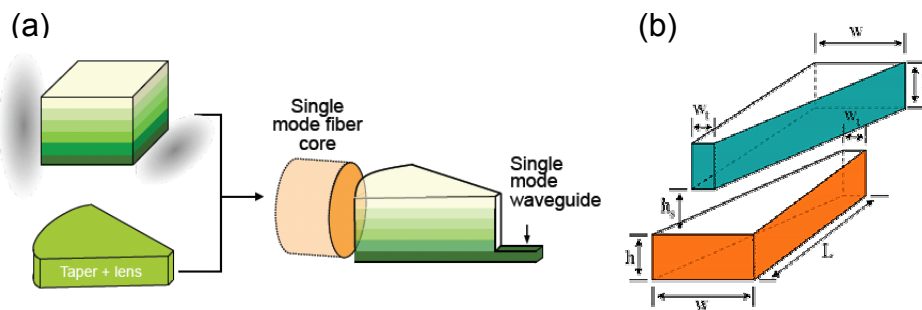


Figure 3. Schematic drawing of (a) a graded index lens coupler for fiber-to-waveguide coupling, and (b) an impedance matching vertical waveguide coupler using overlapping inverse tapers for 3D photonic integration on-chip.

Couplers between on-chip waveguides that are robust to fabrication errors and refractive index variation are also very important for steering light freely across the chip, particularly layer-to-layer optical coupling in the vertical direction for 3D photonic circuits. We have recently achieved an impedance matching vertical waveguide coupler with overlapping inverse tapers (Figure 3b) that exhibited a very low coupling loss of <0.3 dB in a broad wavelength range of 1460-1570 nm and robust to both refractive index variation and fabrication error (14). The effectiveness of these vertical waveguide couplers has already been demonstrated in waveguide-integrated Ge photodetectors.

Optical Filters. Ring resonator filters are the most widely used optical filters for integrated silicon photonics due to the small footprint and high quality factor (Q). The low waveguide propagation loss has enabled multi-stage microring filters to deliver sharp, flat top channel definition with $Q > 10^5$ for add/drop and switching functions. Figure 4 shows a single mode a-Si channel waveguide with a cross-sectional dimension of $0.5 \times 0.2 \mu\text{m}^2$ coupled to a micro-ring optical filter constructed with the same waveguide dimensions. A major disadvantage of ring resonator filters, though, is that the resonance frequency is sensitive to fabrication errors and temperature variations since they both affect the effective index of the resonator. To compensate the fabrication errors, we have developed a trimming process for ring resonators by photo-oxidizing the cladding material (15). To enhance the thermal stability of the ring resonators, cladding material with an opposite sign of thermo-optic coefficient to the core material has been applied to compensate the thermally induced effective index change of the waveguide and stabilize the resonant frequency (16, 17). Experimental results have demonstrated an order of magnitude improvement in the robustness of the resonant wavelength to temperature variations using this athermal approach (17).

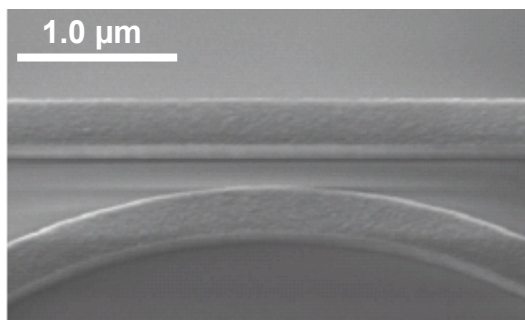


Figure 4. SEM picture of a single mode a-Si channel waveguide with a cross-sectional dimension of $0.5 \times 0.2 \mu\text{m}^2$ coupled to a micro-ring optical filter constructed with the same waveguide dimensions.

Active Photonic Devices

Photodetectors In an EPIC circuit, photodetectors are required to efficiently convert optical signals into electrical ones at a high speed. Ge is the ideal material for monolithically integrated photodetectors on Si due to its CMOS compatibility and efficient direct gap absorption in the telecom wavelength regime around 1550 nm that is transparent to Si waveguides. Thermally induced tensile strain has been successfully incorporated into epitaxial Ge films on Si (18-20) to reduce the direct band gap of Ge and further extend the absorption spectrum to the L band (1561-1620 nm). Furthermore, the

carrier mobility in Ge is about 4 times higher than in silicon, which enables high bandwidth photodetectors at a low reverse bias.

Traditionally, there is a fundamental trade-off between the bandwidth and the efficiency of free-space coupled photodetectors because both the optical absorption path and the carrier collection path are determined by the thickness of the absorption layer. Increasing the absorption layer thickness elongates the optical absorption path and increases the efficiency of the detector, yet it also decreases the bandwidth due to the increased carrier transit time. By separating the optical absorption path in the longitudinal direction from the carrier collection path in the transverse direction, waveguide-integrated Ge photodetectors on Si relieve this bandwidth-efficiency product constraint. The length of the photodetector can be increased beyond 100 μm to absorb all the light, while the cross-sectional dimensions can be made as small as a single mode waveguide ($\sim 0.5 \mu\text{m}$) to collect the photogenerated carriers in less than 10 ps. Waveguide-photodetector coupling has been achieved by butt-coupling or evanescent coupling with $>90\%$ coupling efficiency (21-24). As an example, Figure 5 shows the cross-sectional SEM picture of an evanescently coupled Ge photodetector with the input Si waveguide at the bottom. In both coupling schemes, vertical Si/Ge/Si heterojunction p-i-n diodes structures are adopted to obtain a uniform electric field in the intrinsic Ge layer at a low reverse bias. The performance has reached >30 GHz bandwidth (24) with 90% quantum efficiency in a broad wavelength range of 1480-1580 nm (21-24). A very low dark current of 0.2 nA at -1 V reverse bias with full bandwidth and responsivity has been achieved for butt-coupled Ge photodetectors on Si with the active Ge region selectively grown in a 0.6 μm trench (21,22).

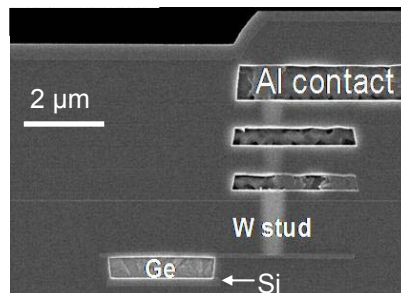


Figure 5. Cross-sectional SEM picture of an evanescently coupled Ge photodetector with the input Si waveguide at the bottom.

Modulators Integrated photonic modulators on Si are crucial devices to encode optical signals for this application. Silicon photonic modulators based on free carrier plasma dispersion effect (25) have achieved significant progress in recent years (26-32). In these devices, the refractive index of Si is controlled by carrier injection or depletion, and electro-optical modulators based on interference effects has been achieved using Mach-Zehnder interferometer (MZI) or microring resonator structures. Some remaining issues include the large size and relatively high energy consumption of Si MZIs, and the susceptibility to fabrication errors as well as limited operation wavelength range of Si microring modulators. Another mechanism for optical modulation is the electro-absorption (EA) effect, where the optical absorption coefficients of a semiconductor material are modified by an applied electric field. Compared to modulators based on free carrier dispersion effect, electro-absorption modulators (EAMs) offer unique benefits for

electronic-photonic integration with small footprint, low energy consumption, and the ability to operate in a relatively broad spectrum range for on-chip WDM. The EA effect is an ultra-fast process that takes place in sub-ps time scale (33), intrinsically suitable for 100 GHz high speed photonic modulation. However, the EA effect of Si is too weak to be applied to the near infrared regime where Si waveguides are transparent. Recently, strong electro-absorption effect from the direct gap transition of Ge has been demonstrated in tensile strained, epitaxial Ge-on-Si (34) and Ge quantum wells (35, 36). The optimal EA contrast is in the L-band (1610-1640 nm) for 0.2% tensile strained Ge-on-Si, compared to 1440-1460 nm for Ge quantum wells (QWs). In order to achieve optimal performance in C-band (1528-1560 nm), we have designed the material composition and device structure of a waveguide-integrated, tensile strained GeSi EAM on SOI for C-band applications (37). Based on this design, a butt-coupled GeSi EAM alloyed with 0.8% Si for optimal performance at 1550 nm has been experimentally demonstrated using 180 nm CMOS fabrication technology (38). The device structure is shown in Figure 6. To take advantage of the low transmission loss in c-Si waveguides, light is propagating in the c-Si waveguide for most of its optical path and it is coupled to a short segment of a-Si waveguide when approaching the GeSi EAM through the tapered vertical waveguide coupler mentioned earlier. The modulated light is then coupled back into the c-Si waveguide in a similar way. The active device area of the GeSi EAM is only $30 \mu\text{m}^2$, and the capacitance is only 11 fF. An 8 dB extinction ratio at 1550 nm was achieved with 3 V peak-to-peak voltage swing. Due to the ultralow capacitance and the relatively small voltage swing, the energy consumption is only 50 fJ/bit even for the worst case scenario where the device is switching between “0” and “1” all the time. In digital communications the average energy consumption of the GeSi EAM is as low as 25 fJ/bit. The device demonstrated a relatively broad operational spectrum range of 1539-1553 nm that covers half of the C-band for on-chip WDM applications. The bandwidth of this prototype device is 1.2 GHz, which can be readily improved to >10 GHz by reducing the series resistance at the contact region with improved fabrication process. With a small footprint, an ultra-low energy consumption, a broad operation spectrum range and CMOS compatibility, the device offers unique benefits for large scale electronic-photonic integration on Si.

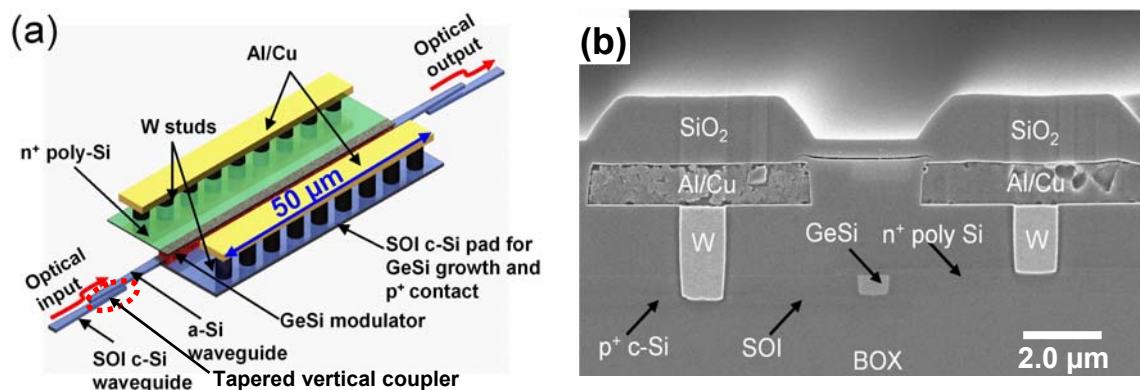


Figure 6. (a) Schematic diagram of a waveguide-integrated GeSi EA modulator with c-Si to a-Si waveguide coupling, and (b) cross-sectional SEM photo of the device.

Laser Sources The Si-compatible laser has long been one of the “holy grails” for electronic and photonic integration on Si. Although electrically pumped III-V

semiconductor lasers at wavelengths transparent to Si waveguides have been successfully bonded to Si substrates at a low thermal budget (39), yet such process cannot be performed at a wafer scale due to the wafer size difference between III-V semiconductors and Si. Due to this reason, the fabrication cost would be approximately an order of magnitude higher than a monolithically integrated laser source on Si. Germanium is a particularly interesting candidate for monolithic lasers on Si due to its pseudo-direct band gap behavior and its CMOS compatibility. The energy difference between the direct and indirect band gaps of Ge is only 136 meV, which can be further reduced by introducing tensile strain to achieve more direct gap semiconductor behavior (18-20). Theoretically, Ge becomes a direct gap material at 2% tensile strain according to the deformation potential theory (40). However, the band gap shrinks to ~ 0.5 eV in that case, corresponding to a wavelength of 2500 nm instead of 1550 nm. To achieve efficient light emission while still keeping the emitted wavelength around 1550 nm, we have proposed a combination of two approaches: (1) introducing 0.25% tensile strain to decrease the difference between the direct and indirect gaps of Ge to ~ 100 meV; (2) compensating the remaining energy difference between the direct Γ valley and the indirect L valley by n-type doping such that the Fermi level reaches the Γ valley (41). Our theoretical modeling has shown that a net optical gain of 400 cm^{-1} can be achieved with this band-engineered Ge-on-Si material (41). Experimental results have indeed demonstrated nearly two orders of magnitude enhancement of the *direct gap* photoluminescence (PL) intensity from tensile-strained, n^+ epitaxial Ge-on-Si at room temperature (42, 43), as shown in Figure 7. Optical bleaching (42) and the onset of optical gain (44) upon steady-state optical pumping have also been observed very recently, and a gain coefficient of $50/\text{cm}$ (~ 200 dB/cm) has been achieved around 1605 nm. In addition, electroluminescence from the direct gap transition of tensile strained Ge-on-Si has also been achieved (45). Considering that the PL, EL and optical gain from the direct gap transition of the band-engineered Ge-on-Si materials are all demonstrated at room temperature, these results point to a promising practical solution for monolithic lasers on Si.

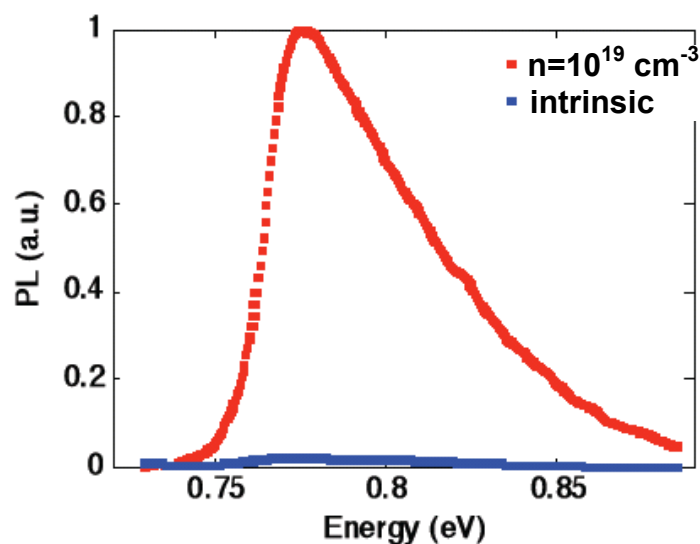


Figure 7. Room temperature photoluminescence of epitaxial Ge-on-Si. The PL intensity of the sample with $n=10^{19} \text{ cm}^{-3}$ in situ phosphorous doping is nearly two orders of magnitude higher than the intrinsic Ge sample due to the increased Fermi level which results in higher injected carrier population in the direct Γ valley.

Process Integration and System Performance

Integration of Si-based photonic devices with CMOS process is an important step for EPICs. The process integration of photonic devices with CMOS transistors on a silicon-on-insulator (SOI) platform is schematically illustrated in Figure 8 (21). Currently the photonic devices have been integrated into the front end of line (FEOL) of CMOS process. Low loss Si waveguides and high Q filters were fabricated by photolithography and reactive ion etching of the single crystalline Si layer on the SOI substrate, while the Ge-based active devices were fabricated after polysilicon gate and silicide formation but before tungsten deposition to accommodate the thermal budget of the epitaxial Ge material. While this approach has achieved a significant success in demonstrating electronic-photonic integration, a disadvantage is that the photonic devices occupy a notable area on the single crystalline Si device level which trades off some of the CMOS transistor region. Considering that metallic interconnects are on the upper levels above the c-Si layer in Si ICs, it is preferred to move the photonic components to the upper interconnect levels using the back end of line (BEOL) process to avoid occupying the CMOS transistor area on the c-Si layer as well as to reduce the thermal budget and the fabrication cost. Investigations on fabricating photonic devices with BEOL process is still an on-going research effort. So far low loss a-Si waveguides on the upper dielectric layers and efficient vertical waveguide couplers for layer-to-layer optical coupling have already been demonstrated. The major challenge is to fabricate high performance active photonic devices such as photodetectors and modulators at temperatures <450 C in the BEOL process without using the single crystalline templates for epitaxial growth. Large grain size and effective defect passivation are critical to achieve this goal.

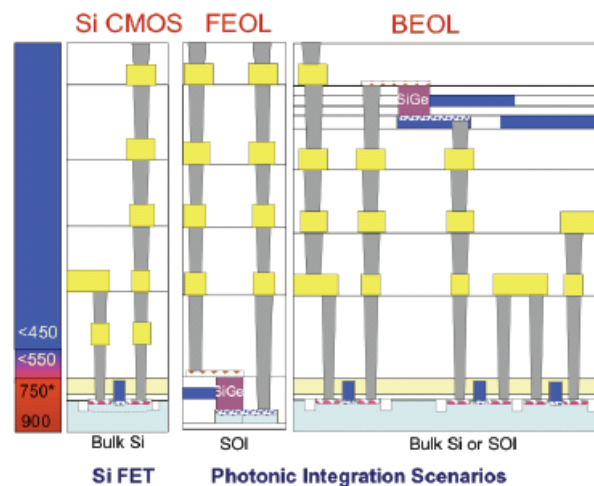


Figure 8. Process integration of photonic devices with CMOS transistors. Currently the integrated photonic devices have been integrated into the front end of line (FEOL) of CMOS process, and it will be moved to the back end of line (BEOL) process in the future to save the area on the single crystalline Si layer for CMOS transistors and reduce the overall thermal budget and fabrication cost.

With the integrated photonic devices available on a Si platform, electronic-photonic integration can be applied to maximize the capability of microprocessors. TABLE I. shows the performance of the state-of-the-art photonic data link and the projected performance in 10 years. The energy consumption in photonic links is dominated by the photonic modulator which has been reduced to 25 fJ/bit based on the GeSi EAM

performance mentioned earlier, about 100 times smaller than typical electrical interconnects (several pJ/bit). The bandwidth of the best photodetectors and modulators on Si is already beyond 30 GHz, which is larger than any existing electrical interconnects on-chip. Using the WDM photonic interconnection shown in Figure 1, the bandwidth of the microchip can be multiplied by the number of wavelength channels and reach above Tb/s for parallel data processing in multicore microprocessors. Future development in Si-based photonic materials and devices can further reduce the power consumption and increase the bandwidth of photonic links for large-scale electronic-photonic integration.

Today's State of the Art		Achievable within ~10 years	
Waveguide-Coupled Ge Photodetectors		Waveguide-Coupled Ge Photodetectors	
Footprint	5 μm^2	Footprint	<2 μm^2
Responsivity	>1.0 A/W	Responsivity	>1.0 A/W
Bandwidth	>30 GHz	Bandwidth	>80 GHz
Spectrum range	1200-1650 nm	Spectrum range	1200-1700 nm
Energy/bit	$\sim 10^{-2}$ fJ/bit		< 10^{-3} fJ/bit
Waveguide-Coupled Modulators		Waveguide-Coupled Modulators	
Footprint	$\sim 20\text{-}30 \mu\text{m}^2$	Footprint	<5 μm^2
Extinction Ratio	>10 dB	Extinction Ratio	>20 dB
Insertion Loss	<4 dB	Insertion Loss	<2 dB
Bandwidth	>30 GHz	Bandwidth	>100 GHz
Energy/bit	25 fJ/bit	Energy/bit	< 5 fJ/bit (with Ge EAMs)
Waveguides and Resonators		Waveguides and Resonators	
Waveguide Loss	0.35 dB/cm	Waveguide Loss	<0.1 dB/cm
Resonator Diameter	$\sim 2 \mu\text{m}$	Resonator Diameter	$\sim 2 \mu\text{m}$
Resonator Q	$\sim 10^6$	Resonator Q	> 5×10^6
Lasers on Si		Lasers on Si	
III-V lasers bonded to Si		Monolithic Si laser using Ge or Er as active media	

TABLE I. Performance of the state-of-the-art photonic data link and the projected performance in 10 years

Conclusions

We have reviewed the recent progress in integrated Si photonic devices for electronic-photonic integrated circuits in future generations of microprocessors. Photonic interconnects can greatly reduce the power consumption and increase the bandwidth for Tb/s data rate on-chip. The synergy of photonics in data links and electronics in data processing provides an excellent solution to system performance scaling beyond the Moore's Law to light up the future of microprocessors in the 21st century.

Acknowledgments

This research was sponsored by the Defense Advanced Research Projects Agency's (DARPA) EPIC program supervised by Dr. Jagdeep Shah, and the Si-based Laser Initiative of the Multidisciplinary University Research Initiative (MURI) sponsored by the Air Force Office of Scientific Research (AFOSR) and supervised by Dr. Gernot Pomrenke.

References

1. A. Agarwal, Workshop on Edge Computing Using New Commodity Architectures (EDGE), May 2006, North Carolina. (<http://gamma.cs.unc.edu/EDGE/SLIDES/agarwal.pdf>)
2. Randolph Kirchain and Lionel C. Kimerling, *Nature Photonics* **1**, 303 (2007).
3. A. Benner, A. Ignatowski, J. Kash, K. Kuchta, D. Ritter, *IBM Journal of R&D*, Vol. 49, number 4/5, 2005.
4. J. Psota, J. Eastep, J. Miller, T. Konstantakopoulos, M. Watts, M. Beals, J. Michel, L.C. Kimerling, and A. Agarwal, Proceedings of the Fifth Annual Boston Area Architecture Workshop, p 107, January 2007 (http://www.bu.edu/barc2007/barc_proceedings.pdf)
5. L. C. Kimerling, D. Ahn, A. B. Apsel, M. Beals, D. Carothers, Y-K. Chen, T. Conway, D. M. Gill, M. Grove, C-Y Hong, M. Lipson, J. Liu, J. Michel, D. Pan, S. S. Patel, A. T. Pomerene, M. Rasras, D. K. Sparacin, K-Y. Tu, A. E. White, and C. W. Wong, *Proc. SPIE* **6125**, 612502 (2006).
6. K. K. Lee, D. R. Lim, L. C. Kimerling, J. Shin and F. Cerrina, *Opt. Lett.* **26**, 1888 (2001)
7. D. K. Sparacin, S.J. Spector, L.C. Kimerling, *IEEE Journal of Lightwave Technology*, **23**, 2455 (2005).
8. D. K. Sparacin, R. Sun, A.M. Agarwal, M.A. Beals, J. Michel, L.C. Kimerling, T. J. Conway, A.T. Pomerene, D.N. Carothers, M.J. Grove, D.M. Gill, M.S. Rasras, S.S. Patel, and A.E. White, 3rd IEEE International conference on Group IV Photonics, p 255, IEEE Catalog Number: 06EX1276C (Toronto, Canada 2006)
9. Rong Sun, Mark Beals, Kevin McComber, Jing Cheng, Daniel K. Sparacin, Jurgen Michel and Lionel C. Kimerling, submitted to *Opt. Lett.* (2009).
10. V. Almeida, R. Panepucci, and M. Lipson, *Opt. Lett.* **28**, 1302 (2003)
11. C. Gunn, *IEEE. Micro.* **26**, 58 (2006)
12. V. Nguyen, T. Montalbo, C. Manolatou, A. Agarwal, C.-Y. Hong, J. Yasaitis, L. C. Kimerling, and J. Michel, *Appl. Phys. Lett.* **88**, 081112 (2006).
13. R. Sun, V. Nguyen, A. Agarwal, C.-Y. Hong, Yasaitis, L. C. Kimerling, and J. Michel, *Appl. Phys. Lett.* **90**, 201116 (2007).
14. R. Sun, M. Beals, A. Pomerene, J. Cheng, C. Y. Hong, L. C. Kimerling, and J. Michel, *Opt. Express.* **16**, 11682 (2008)
15. D. K. Sparacin, C. Y. Hong, L. C. Kimerling, J. Michel, J. P. Lock and K. K. Gleason, *Opt. Lett.* **30**, 2251 (2005)
16. W. N. Ye, J. Michel, and L. C. Kimerling, *IEEE. Photon. Technol. Lett.* **20**, 885 (2008)
17. W. N. Ye, R. Sun, J. Michel, L. Eldada, D. Pant, and L. C. Kimerling, 5th IEEE International Conference on Group IV Photonics, IEEE Catalog Number: CFP08GFP-CDR, p 401 (Sorrento, Italy, 2008)
18. Y. Ishikawa, K. Wada, D. D. Cannon, J. F. Liu, H. C. Luan, and L. C. Kimerling, *Appl. Phys. Lett.* **82**, 2044 (2003)
19. J. F. Liu, D. D. Cannon, K. Wada, Y. Ishikawa, D. T. Danielson, S. Jongthammanurak, J. Michel, and L. C. Kimerling, *Phys. Rev. B* **70**, 155309 (2004)
20. J. F. Liu, D. D. Cannon, K. Wada, Y. Ishikawa, S. Jongthammanurak, D. T. Danielson, J. Michel, and L. C. Kimerling, *Appl. Phys. Lett.* **87**, 011110 (2005)

21. Mark Beals, J. Michel, J.F. Liu, D.H. Ahn, D. Sparacin, R. Sun, C.Y. Hong, L. C. Kimerling, A. Pomerene, D. Carothers, J. Beatti, A. Kopa, A. Apsel, M. S. Rasras, D. M. Gill, S. S. Patel, K.Y. Tu, Y. K. Chen, and A. E. White, *Proc. SPIE* **6898**, 689804 (2008)
22. J. F. Liu and J. Michel, ECS transactions **16**, 575 (2008)
23. D. Ahn, C. Y. Hong, J. F. Liu, W. Giziewicz, M. Beals, L. C. Kimerling, and J. Michel, *Opt. Express* **15**, 3916 (2007).
24. T. Yin, R. Cohen, M. Morse, G. Sarid, Y. Chetrit, D. Rubin, and M. J. Paniccia, *Opt. Express*. **15**, 13965 (2007)
25. R. A. Soref and B. R. Bennett, *IEEE J. Quantum Electron.* **23**, 123 (1987).
26. A. Liu, R. Jones, L. Liao, D. Samara-Rubio, D. Rubin, O. Cohen, R. Nicolaescu and M. Paniccia, *Nature* **427**, 615 (2004).
27. Q. Xu, B. Schmidt, S. Pradhan and M. Lipson, *Nature* **435**, 325 (2005).
28. A. Liu, L. Lin, R. Doron, H. Nguyen, B. Ciftcioglu, Y. Chetrit, N. Izhaky, and M. Paniccia, *Opt. Express*. **15**, 660 (2007)
29. B. Analui, D. Guckenberge, D. Kucharski, and A. Narasimha, *IEEE. J. Solid-State. Circ.* **41**, 2945 (2006)
30. W. M. J. Green, M. J. Rooks, L. Sekaric and Y. A. Vlasov, *Opt. Express*. **15**, 17106 (2007)
31. Q. Xu, S. Manipatruni, B. Schmidt, J. Shakya, and M. Lipson, *Opt. Express* **15**, 430 (2007)
32. S. Manipatruni, Q. Xu, and M. Lipson, *Opt. Express* **15**, 13035 (2007)
33. J. F. Lampin, L. Desplanque and F. Molloy, *Appl. Phys. Lett.* **78**, 4103 (2001).
34. S. Jongthanmmanurak, J. F. Liu, K. Wada, D. D. Cannon, D. T. Danielson, D. Pan, L. C. Kimerling and J. Michel, *Appl. Phys. Lett.* **89**, 161115 (2006).
35. Y.-H. Kuo, Y. K. Lee, Y. Ge, S. Ren, J. E. Roth, T. I. Kamins, D. A. B. Miller, and J. S. Harris, *Nature* **437**, 1334 (2005).
36. J. E. Roth, O. Fidaner, R. K. Schaevitz1, Y. H. Kuo, T. I. Kamins, J. S. Harris, Jr., and D. A. B. Miller. *Opt. Express*. **15**, 5851 (2007)
37. J. F. Liu, D. Pan, S. Jongthanmmanurak, K. Wada, L. C. Kimerling and J. Michel, "Design of monolithically integrated GeSi electro-absorption modulators and photodetectors on an SOI platform", *Optics Express* **15**, 623 (2007)
38. J. F. Liu, M. Beals, A. Pomerene, S. Bernardis, R. Sun, J. Cheng, L. C. Kimerling and J. Michel, *Nature Photonics* **2**, 433 (2008)
39. A.W. Fang, H. Park, O. Cohen, R. Jones, M. J. Paniccia, and J. E. Bowers, *Opt. Express* **14**, 9203-9210 (2006).
40. C. G. Van de Walle, *Phys. Rev.* **B 39**, 1871-1883 (1989).
41. J. F. Liu, X. C. Sun, D. Pan, X. X. Wang, L. C. Kimerling, J. Michel and T. L. Koch, *Optics Express* **15**, 11272-11277 (2007)
42. J. F. Liu, X. C. Sun, P. Becla, L. C. Kimerling and J. Michel, 5th IEEE International Conference on Group IV PhotonicS, IEEE Catalog Number: CFP08GFP-CDR, p16 (Sept. 2008, Sorrento, Italy)
43. X. C. Sun, J. F. Liu, L. C. Kimerling, and J. Michel, 2008 OSA Conference on Integrated Photonics and Nanophotonics research and Application (Jul. 2008, Boston, MA, USA), paper # IMC5
44. X. C. Sun, J. F. Liu, L. C. Kimerling and J. Michel, submitted to *Nature Photonics* (2009)
45. X. C. Sun, J. F. Liu, L. C. Kimerling and J. Michel, submitted to *Opt. Lett.* (2009)