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# Stability of polymer-dielectric bi-layers for athermal silicon photonics

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**Abstract:** Temperature sensitivity of Si based rings can be nullified by the use of polymer over-cladding. Integration of athermal passive rings in an electronic-photonic architecture requires the possibility of multi-layer depositions with patterned structures. This requires establishing UV, thermal and plasma stability of the polymer during multi-layer stacking. UV stability is enhanced by UV curing to saturation levels. However, thermal stability is limited by the decomposition temperature of the polymer. Further, robust performance in oxidizing atmosphere and plasma exposure requires a SiO<sub>2</sub>/SiN<sub>x</sub> based dielectric coatings on the polymer. This communication uses a low temperature (130°C) High Density Plasma Chemical Vapor Deposition (HDPCVD) for dielectric encapsulation of polymer cladded Si rings to make them suitable for device layer deposition. UV induced cross-linking and annealing under vacuum make polymer robust and stable for Electron Cyclotron Resonance (ECR)-PECVD deposition of 500nm SiO<sub>2</sub>/SiN<sub>x</sub>. The thermo-optic (TO) properties of the polymer cladded athermal rings do not change after dielectric cap deposition opening up possibilities of device deposition on top of the passive athermal rings. Back-end CMOS compatibility requires polymer materials with high decomposition temperature (> 400°C) that have low TO coefficients. This encourages the use of SiN<sub>x</sub> core waveguides in the back-end architecture for athermal applications.

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**OCIS codes:** (130.2790) Guided waves; (130.3130) Integrated optics materials; (160.5470) Polymers; (160.6840) Thermo-optical materials; (220.4000) Microstructure fabrication; (230.5750) Resonators; (230.7380) Waveguides, channeled; (310.1860) Deposition and fabrication.

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## 1. Introduction

Si based ring resonators form an integral part of back-end photonic interconnect stack of an electronic-photonic integrated chip. Sensitivity to fabrication variations and temperature fluctuations necessitates tuning the filter response of the resonators. Active tuning involving heaters and thermo-electric coolers prove power inefficient apart from limiting the number of I/O lines for high density integration [1]. Stojanovic et al. [2] have shown that thermal tuning energy forms a significant portion of non-data dependent power (NDD) in an all-to-all computing (ATAC) environment. Thermal tuning of back-end resonators accounts for 75% of the energy-cost at a data rate of around 1 GB/s per link. Though this cost goes down with higher data rate per link, it still constitutes to roughly 50% of the energy cost at an optimized bandwidth of around 4GB/s per link. With energy and bandwidth density driving the Moore's law for the next generation microprocessors, there is an increasing demand for passive design solution for athermal ring resonators.

Passive thermal compensation using polymer over-cladding to compensate for the positive TO effects from the core has been demonstrated [3–7]. In our earlier paper [3], we had demonstrated the lowest TO peak shift of 0.5 pm/K in polymer cladded a-Si rings. Further, the role of waveguide dispersion that necessitates the use of different athermal waveguide dimensions based on the resonance wavelength filtered was established. Also, residual second order effects at low TO peak shifts were observed. This communication extends the previous work [3] and explores the possibility of hermetic sealing of the polymer cladded devices that enables deposition of patterned structures on top of the athermal rings.

Polymers have not been the first choice for CMOS integration owing to the reliability concerns arising from photo-oxidation of polymers. Hyperlinked fluoropolymer cladding, used in this study, is made stable for high levels of UV dose (~8000 mJ/cm<sup>2</sup>) by curing to saturation levels using a short arc mercury lamp ( $\lambda$ :365-405nm, UV dose: 6000mJ/cm<sup>2</sup>) and baked in vacuum at 150°C for 4 hours. Back-end compatibility might require deposition of patterned structures on top of the polymer cladded athermal rings thereby requiring robust performance to plasma exposure and oxidation. This communication explores the possibility of multi-layer stacking on these polymer cladded devices. This involves encapsulating them with a thin layer of dielectric layer that acts as a diffusion barrier for oxygen and as a etch stop during plasma exposure of patterned structures on top. However, the decomposition temperature of polymerlayer limits the deposition temperature to less than 300°C in non-oxidizing atmosphere. Though conventional PECVD of dielectrics can be carried out between 250 and 350°C, hydrogen incorporation in the film at low temperatures (<300°C) discourages their application. We use High Density Plasma Chemical Vapor Deposition (HDPCVD) using

Electron Cyclotron Resonance (ECR) source to deposit 500nm of 2 choices of dielectric: SiO<sub>2</sub> and SiN<sub>x</sub> at a low temperature (130°C) after stabilizing the polymer for UV exposure. The thermo-optic (TO) response of the encapsulated rings does not change after the dielectric deposition with a robust performance over an operating temperature range of 25°C-125°C. Back-end-of-line (BEOL) compatibility requires polymers that have a high decomposition temperature (> 400°C) to ensure stability during the metal contact deposition. However, such polymers have a low TO coefficient that might not negate the positive TO response of Si core. SiN<sub>x</sub> cores with a lower TO coefficient might be a better choice for athermal performance of CMOS compatible BEOL interconnects.

## 2. Prototype fabrication

205nm thick a-Si films ( $n: 3.48$ ,  $TO: 2.3 \times 10^{-4}$ ) are deposited on a 3 $\mu\text{m}$  SiO<sub>2</sub> ( $n: 1.46$ ,  $TO: 1 \times 10^{-5}$ ) wafer using PECVD of SiH<sub>4</sub> (50sccm) at 200°C with Ar (600sccm) as the inert gas in the plasma. The pressure inside the chamber is around 1000mTorr and the RF power input to the plasma is 52W. The deposition rate of the film is measured to be around 55.5nm/min. The films have a 5MPa tensile stress and have 3% uniformity across a 6 inch wafer. Ring resonators with racetrack pattern (Fig. 1(a)) are transferred to a-Si via photolithography using an i-line stepper. The cross-section (Fig. 1(b)) of the waveguides (550nm x 205nm) has been designed for single TM mode operation. The devices are then spin coated with 3-4 $\mu\text{m}$  hyperlinked fluoropolymer, EP, at Enablence Inc. ( $n: 1.38$ ,  $TO: -2.65 \times 10^{-4}$ )

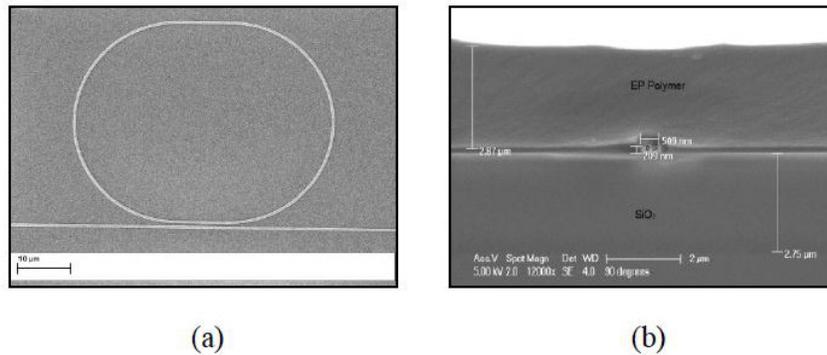


Fig. 1. (a) Top view of the unclad a-Si resonator shows the racetrack configuration that is used for TO measurements. (b) Cross-sectional SEM of the device shows 509nm x 209nm a-Si core with 2.75 $\mu\text{m}$  SiO<sub>2</sub> under-cladding and 2.87 $\mu\text{m}$  EP polymer over-clad. The design rule involves expanding the TM mode into the polymer cladding, thereby, negating the positive TO effects from the core.

## 3. Prototype performance

### 3.1. UV Stability

Polymer clad is UV cured by exposing it for 20 minutes to 5mW/cm<sup>2</sup> (6000 mJ/cm<sup>2</sup>) from a short arc mercury lamp. The samples are further baked at 150°C under vacuum for 4 hours to enhance the cross-linking in the cured polymer. This process stabilizes the polymer for further UV exposure during lithography and plasma deposition steps. FTIR spectra of the cured polymer film exposed to a 254 nm UV handheld lamp with a power flux of 2.2 mW/cm<sup>2</sup> showed no significant changes in the bond chemistry of the polymer, thereby establishing its chemical stability (upto 7920 mJ/cm<sup>2</sup> of UV dose). The amorphous network-property correlation supports the stable optical performance of the polymer cladding that shows bond chemistry invariance on UV exposure. In other words, TO performance of an athermal ring (Fig. 1) remains the same even after UV exposure. This is verified by exposing the athermal devices to 9.5 mJ/cm<sup>2</sup> of UV radiation (365-405nm). TO performance is

measured by noting the transmission spectrum for every 5°C of an athermal ring that is heated from 25°C-70°C. Temperature dependent wavelength shift (TDWS) of the devices is found for various resonances. The TO performance of various devices reveals a decrease in TDWS with wavelength. This decrease is attributed to the waveguide dispersion of the device resulting in decreased optical confinement with increasing wavelength [3]. The observed scatter in TO experimental values (around 1pm/K) of an athermal ring exposed to UV radiation is within expected limits ( $\pm 5$  pm/K) due to thickness variations ( $\pm 6$ nm) associated with a-Si deposition (Fig. 2).

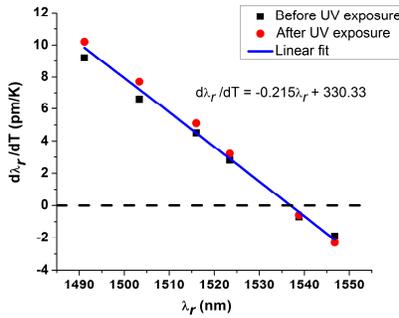


Fig. 2. Experimental data suggests that UV exposure has minimal effect on the TO response of an athermal ring. Curing of spun-on polymer by exposing it to a 5mW/cm<sup>2</sup> UV radiation for 20 minutes creates enough cross-linking and structural reorganization within polymer thereby making it stable to any further UV exposure ( $\lambda$ : 365-405nm, Dose: 9.5mJ/cm<sup>2</sup>). Variation of experimental TO values around the linear fit is within the expected limits ( $\pm 5$ pm/K) arising from thickness non-uniformity ( $\pm 6$ nm) during a-Si deposition.

### 3.2 Thermal Stability

A stable performance over the working temperature range, 25°C – 125°C, is ensured by baking the polymer cladded device in vacuum at 150°C for 4 hours. However, back-end CMOS compatibility of these athermal rings might require it to withstand temperatures as high as 400°C associated with the copper metallization and final forming gas annealing steps [8].

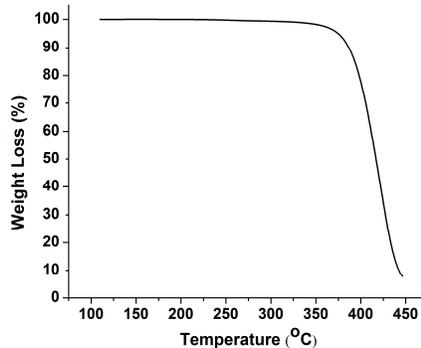
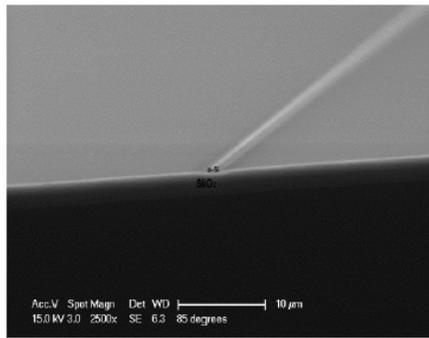


Fig. 3. TGA measurement of the polymer sample in N<sub>2</sub> atmosphere reveals weight loss above 350°C at a heating rate of 10°C/min. Multi-layer depositions on polymer film needs to be carried out at temperatures less than 300°C to prevent any weight loss resulting in polymer degradation.

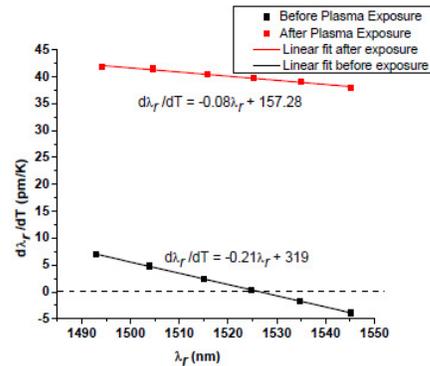
Thermogravimetric analysis (TGA) of the polymer in N<sub>2</sub> atmosphere shows weight loss around 375°C at a heating rate of 10°C/min (Fig. 3). However, the onset of decomposition may change with heating rate. It is important to note that cooling to operating temperature after the onset of decomposition can result in the loss of polymer functionalities for athermal application. Further, there are no structural transitions in the polymer upto 300°C. Hence, multi-layer deposition processes on athermal rings that are carried out at less than 300°C in non-oxidizing atmosphere would ensure a safe processing condition that prevents any property changes of the polymer as long as equilibrium cooling of the polymer layer is ensured.

### 3.3 Plasma Stability

Deposition of patterned structures on athermal rings demands stability to plasma exposure. However, the SEM and TO performance of rings (Fig. 4) exposed to Argon plasma at 130°C suggests the etching of polymer over-clad. The change in the absolute TDWS values indicates the increase in effective TO of the system after plasma exposure (Fig. 4(b)). The change in the slope value is indicative of the change in TO contrast between the core and the cladding. In addition, different waveguide dispersion also reflects the fact that the confinement factor of the waveguide has changed after plasma exposure thereby changing its effective index. This motivates the need for a dielectric hermetic layer that prevents polymer degradation in the presence of plasma.



(a)

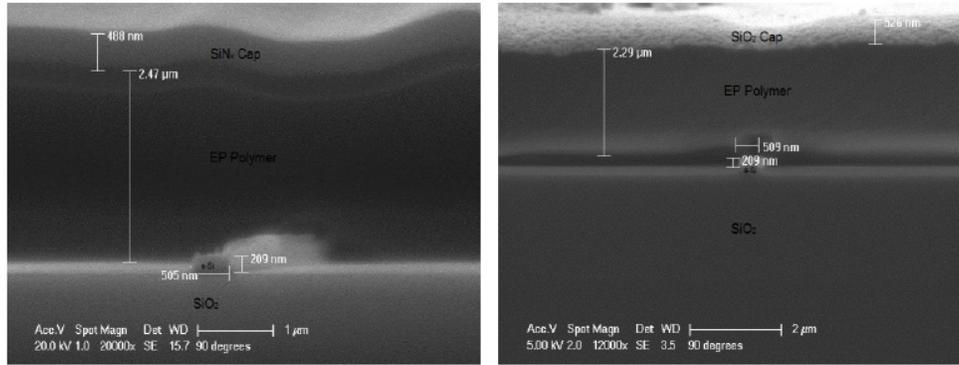


(b)

Fig. 4. (a) SEM image of the plasma exposed athermal device confirms the etching of polymer top cladding. (b) TO performance of the ring exposed to Argon plasma reveals increased TDWS values (around 40 pm/K) due to the absence of polymer.

## 4. HDPCVD of Dielectric Encapsulation

The incentive for encapsulating the polymer clad athermal rings with a thin layer of dielectric is two pronged: robust performance in oxidizing atmosphere and plasma exposure. Dielectrics act as oxygen diffusion barrier thereby preventing unwanted oxidation of underlying polymer. In addition they could act as possible etch stops during new device patterning on top of the athermal rings. However, the polymer decomposition constrains the dielectric deposition to temperatures less than 300°C in non-oxidizing atmosphere. Conventional PECVD results in hydrogen incorporation at temperatures less than 300°C, thereby motivating the need for a low temperature deposition that might result in lesser hydrogen incorporation.



(a)

(b)

Fig. 5. (a) SEM confirms the successful deposition of dielectrics on the polymer cladding. Cross-sectional SEM of 505nm  $\times$  209nm a-Si with 3 $\mu$ m SiO<sub>2</sub> under-clad, 2.47 $\mu$ m EP polymer over-clad encapsulated with a 488nm SiN<sub>x</sub>. (b) Cross-sectional SEM of 509nm  $\times$  209nm a-Si with 3 $\mu$ m SiO<sub>2</sub> under-clad, 2.29 $\mu$ m EP polymer over-clad encapsulated with a 526nm SiO<sub>2</sub> cap.

High density plasma chemical vapor deposition, using electron cyclotron resonance (ECR) as the high density plasma source, of high quality SiN<sub>x</sub> and SiO<sub>2</sub> films with low hydrogen content has been demonstrated at low temperatures [9–11]. Two choices of dielectrics, namely SiN<sub>x</sub> and SiO<sub>2</sub>, are considered as possible encapsulates. 500 nm of both the dielectrics are successfully deposited on the polymer layer using HDPCVD (Fig. 5) using the conditions listed in Table 1.

**Table 1. HDPCVD Conditions for SiO<sub>2</sub> and SiN<sub>x</sub> on the Polymer Cladded Devices**

Deposition Conditions	SiO <sub>2</sub>	SiN <sub>x</sub>
Substrate Temperature(°C)	130	130
Ar flow rate(sccm)	10	20
O <sub>2</sub> flow rate (sccm)	20	-
N <sub>2</sub> flow rate (sccm)	-	11.6
3% SiH <sub>4</sub> / Ar flow rate (sccm)	100	110
Pressure (mTorr)	20	20
Microwave Power (W)	300	265
Deposition rate (nm/min)	20.1	16.6
Refractive index	1.47	1.95
Stress (MPa)	-2.3	37
Uniformity (4 inch wafer, 1 sigma)	5%	4.5%

## 5. Performance of dielectric caps

It is important to ensure that the presence of dielectric caps doesn't affect the TO performance of the athermal rings. The optical mode is fully confined within the polymer cladding as far its thickness is greater than 2  $\mu$ m (Fig. 5). The invariance of polymer optical properties and the athermal performance is easily verified through the TDWS performance of the capped devices (Fig. 6). The deposited a-Si films have a thickness uniformity around 3% which results in uncertainty in its thickness values to around 6nm. FIMMWAVE simulations indicate that 1nm change in thickness of these rings could shift its TDWS by 1pm/K, given the sensitivity of TM mode response to the thickness variation. This results in a possible variation of 5pm/K in the TDWS value of a resonator for a given wavelength. TO response of the encapsulated rings falls within this variable limit thereby making them suitable for multi-layer stacking.

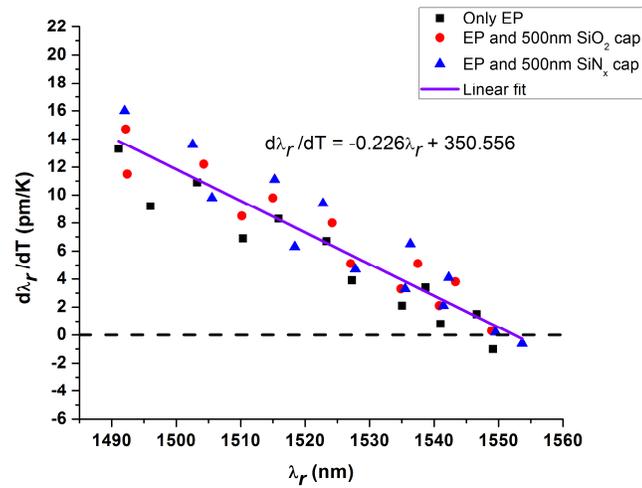


Fig. 6. The TDWS response doesn't change significantly after the dielectric ( $\text{SiO}_2/\text{SiN}_x$ ) deposition on the polymer. The scatter in experimental TDWS values are within the expected variation ( $\pm 5\text{pm/K}$ ) due to 3% thickness non-uniformity during the deposition of 205nm thick a-Si film.

## 6. Material Selection for CMOS BEOL compatibility: core-cladding combination

CMOS BEOL process flow involves metallization and annealing steps at temperatures between  $400^\circ\text{C}$  -  $450^\circ\text{C}$ . Further, the high metal levels use 248 nm lithography with dose levels between  $20 - 50 \text{ mJ/cm}^2$  [8]. Though, the hyperlinked fluoropolymer polymer under study can handle the expected UV dose levels without any significant degradation, the thermal decomposition might make it incompatible with the metallization and annealing steps. This encourages the use of polymers with high decomposition temperatures ( $>450^\circ\text{C}$ ) for back-end compatibility. BCB and Polyimides belong to polymer classes with high thermal stability [12–14]. However, such polymer choices have low TO coefficient [15] that might be insufficient to compensate for the high TO coefficient of the Si cores (Table 2). Hence,  $\text{SiN}_x$  with a lower TO coefficient (Table 2) might prove to be a better core choice for BEOL interconnects. Further, it is important to note that BCB and polyimides have glass transitions occurring beyond  $350^\circ\text{C}$  and  $310^\circ\text{C}$  respectively [14]. Hence, the cooling rate might have to be optimized after the metallization step to ensure the desired optical functionality in these polymers. For a given polymer cladding choice, it is shown that the athermal constraint results in comparable  $n_{\text{eff}}$  of the device for both Si and  $\text{SiN}_x$  cores [3]. So, the choice between Si and  $\text{SiN}_x$  core is not clear under athermal constraint and the polymer cladding choice for CMOS compatibility could prove to be a crucial parameter in the figure-of-merit.

**Table 2. Polymer Cladding Choices for a Given core for Athermal Application  $\text{SiN}_x$  core having a low TO coefficient can be compensated with a low TO coefficient polymer. Such polymers have a high decomposition temperature and hence are compatible with back-end CMOS processes.**

Core material	Core TO coefficient ( $\times 10^{-4}$ )	Possible Cladding choice	Cladding TO coefficient ( $\times 10^{-4}$ )	Cladding Decomposition Temperature ( $^\circ\text{C}$ )
a-Si	2.3	EP (Hyperlinked fluoropolymer)	-2.65	$\sim 375$
Si	1.86	EP (Hyperlinked fluoropolymer)	-2.65	$\sim 375$
$\text{SiN}_x$	0.4	BCB	-0.25 to -1.15 [15]	$\sim 400-450$ [13]
		Fluorinated Polyimides	-0.46 to -1.04 [15]	$\sim 400-450$ [14,15]

## 7. Summary and Conclusions

This communication explores the possibility of multi-layer stacking on passive athermal a-Si rings. UV stability of the polymer is established by UV curing and annealing cycle. The polymer decomposition around 375°C requires dielectric deposition at a lower temperature. Hence, HDPCVD is utilized to deposit 500 nm of SiN<sub>x</sub>/SiO<sub>2</sub>, at 130°C, on polymer over-clad to prevent the etching of polymer layer during subsequent plasma exposure steps. The TO performance of dielectric encapsulated rings are not altered due to the dielectric deposition. Hence, this communication opens up new range of possibilities involving device stacking on top of the athermal a-Si rings as long as the temperature of deposition is kept under 300°C. However, back-end interconnect architecture on a CMOS platform involves metallization and annealing steps around 400°C. This demands the use of a polymer clad with a high decomposition temperature. This involves a trade-off with the magnitude of the polymer's TO coefficient, which is lower than that of a-Si/Si. Back-end CMOS compatibility encourages the use of SiN<sub>x</sub> core waveguides with a polymer of high decomposition temperature to achieve athermal operation.

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