A Process Technology for Realizing Integrated Inertial Sensors Using Deep Reactive Ion Etching (DRIE) and Aligned Wafer Bonding

by

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B.Eng., Electrical Energy Systems Engineering
University of Hong Kong, 1996

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of
Master of Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 1999

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ABSTRACT

The demand for silicon micromachined inertial sensors is expected to grow tremendously in the next few years. Potential benefits such as improved performance, enhanced reliability and lower cost can be gained by integrating these sensors with on-chip electronics. Using deep reactive ion etching (DRIE) and aligned wafer bonding, a process technology for realizing integrated inertial sensors is developed. DRIE allows the formation of high-aspect-ratio structures especially crucial for lateral inertial sensors. Compatibility with standard IC processes is achieved by the sealed-cavity approach as enabled by wafer bonding. This process also realizes a new interconnection scheme which permits signal crossovers.

During process development, DRIE gap-widening and footing effects are observed. These effects are characterized and ways to minimize them found. The process technology is successfully demonstrated by the fabrication of functional accelerometers and gyroscopes. The characteristics of the accelerometers are measured by shaker tests and Computer Microvision. Some deviation from the design values is observed, however, its cause is not completely understood.

Thesis Supervisor: Martin A. Schmidt
Title: Professor of Electrical Engineering

ACKNOWLEDGMENTS

The nice thing about completing one stage and awaiting the next is that it provides a convenient point to stop and retrace everything that has happened, and ponder what has been achieved and who have made all these possible.

I can still vividly remember the excitement I had when I learnt of the opportunity to join the MEMS research group at MIT two years ago. I would like to express my heartfelt gratitude to Prof. Martin Schmidt for giving me the opportunity to work in his group. Marty is surely a respectable scholar with enormous breadth and depth of knowledge. I admire the way he leads and communicates as well as his caring for the students. I owe much thanks to Prof. Charles Sodini who literally brought me to MIT after we met only once in Hong Kong. His belief in my potential is greatly appreciated. I have to thank Prof. Felix Wu, Prof. Ping Ko, and Prof. Man Wong for opening up opportunities for me to pursue my goal.

I would like to thank Kei Ishihara from whom I have learnt a great deal during our one year and a half of collaborative work. I am inspired by his goal- and result-oriented attitude, his efficiency, and his equal emphasis on both work and play. Special thanks go to Dr. Arturo Ayón for his expert advice on DRIE and for pointing out the difference between a cleanroom and a McDonald.

I am very glad to have Joel Voldman and Dye-Zone Chen as my officemates who are always there to help and advise. Thanks to Joel for all the group lab training, and for decorating the terminal with his entertaining MATLAB plots. Thanks to Zony for sharing his thoughts on many technical matters, as well as on study and career. Thanks to both for introducing me to the fascinating world of Palm™. Every member of the group has given me advice or assistance at one point or another. I benefit a lot from their collective knowledge. To them I owe much thanks. Specifically, I would like to thank Dr. Xin Zhang, Dr. Reza Ghodssi, Jo-Ey Wong, Robert Bayt, C.-C. Lin, Samara Firebaugh, Christine Tsau, and Rebecca Braff. I would like to thank the MTL staff for training me in the use of various machines and for their valuable processing advice. I would also like to thank Skip Hoyt at Lincoln Laboratory for providing the wafer polishing services, usually on short notice, and to Dr. Vicky Diadiuk for her "express" services.

My sincere thanks go to Gary Yau for his help over the years, especially for his advice during the graduate school application process and for helping me settle down in a new environment. I would also like to say thanks to Dr. K. C. Chan (Chu Gor) for flooding my inbox with innumerable (3000+) emails in the past two years to make my late night work a bit less solitary, and for that matter, thanks go to Ma Sin (Ging) Ging (To).

I would like to express my deepest thanks to Cindy for her encouragement during those despondent moments and all the experiences and memories we share.

Finally I am very grateful to my parents and family who always support whatever decision I have made. They provide me with the best possible environment so that I can devote myself wholeheartedly to whatever I choose to pursue, free from any financial worries and household chores. To them I cannot but say thanks. I must also thank my uncle's family for their support over the years.

This work is supported by SRC (SC309) and DARPA (N66001-97-C-8643). The SOI wafers used in this work are provided by Motorola.

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1. INTRODUCTION

This work aims to develop a process technology for realizing integrated high-aspect-ratio inertial sensors, and is done in collaboration with Kei Ishihara. A brief review of micromachined inertial sensors is given in Section 1.1. Section 1.2 describes the general integrated sensor approach adopted in this work. The two enabling technologies essential to the process technology, namely aligned wafer bonding and deep reactive ion etching (DRIE), are described in Sections 1.3 and 1.4 respectively. Section 1.5 gives the thesis outline.

1.1 MICROMACHINED INERTIAL SENSORS

Inertial sensors are sensors that measure acceleration (accelerometers) and rotation (gyroscopes). The last decade or so has seen the rapid development of silicon micromachined inertial sensors based on MEMS technologies. Microaccelerometers alone have the second largest sales volume in the silicon microsensor market after pressure sensors, and it is believed that microgyroscopes will soon be mass-produced at similar volumes. There is a rapidly growing market especially for automotive (e.g. air-bag deployment, suspension control and navigation) and consumer (e.g. camcorder stabilization, 3-D mouse, virtual reality games/toys and sports equipment) applications. Compared with their conventional counterparts, silicon inertial sensors promise to be smaller, lighter, potentially lower in cost, and more amenable to mass production. Another advantage silicon inertial sensors possess is the potential of integrating signal processing and control circuitry onto the same chip as the sensor to produce integrated or smart sensors. The drive towards higher performance, lower cost, greater functionality, higher levels of integration, and higher volume is expected to continue in the next decade as new fabrication, circuit and packaging techniques are developed to meet the ever increasing demand for inertial sensors.

1.2 INTEGRATED SENSOR APPROACH

The fact that MEMS technology originated from the IC technology leads naturally to the concept of integrating MEMS and microelectronics onto the same chip. Potential benefits of integration include smaller form factor, lower packaging and assembly costs, enhanced reliability due to less bond wires and improved system performance (e.g. by significantly reducing parasitics in capacitive sensors). The major challenges in developing an integrated sensor process are process incompatibility, thermal budget incompatibility and material incompatibility.

The process described in this thesis is based upon the sealed-cavity process previously reported by our group [1,2,3,4]. Figure 1.1 illustrates this generic approach to integrated sensor fabrication. The front-end micromachining process involves the bonding of a device wafer to a handle wafer to create a two-wafer stack containing embedded cavities. The resulting stack resembles a standard unprocessed wafer and therefore can go through standard IC processes at a foundry without special handling or processing. After circuit fabrication, back-end micromachining processing is performed to functionalize and package the device. This sealed-cavity process has been demonstrated to be compatible with a full CMOS process flow [3,4].

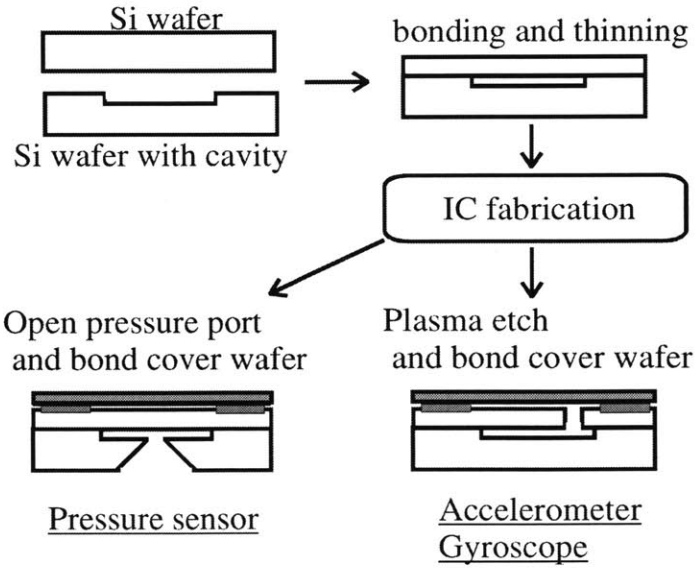


Figure 1.1 Generic sealed-cavity approach to integrated sensor fabrication

The present work couples the above generic sealed-cavity process with deep reactive ion etching (DRIE) to result in a process technology for realizing integrated inertial sensors. Apart from being compatible with standard IC processes, this process technology has several other advantages. First, the use of single-crystal silicon as mechanical structures eliminates the reproducibility and long-term stability issues of polysilicon in surface micromachining. Second, thicker, high-aspect-ratio structures made possible by this technology lead to increased sense capacitance, enhanced mode separation, reduced cross-axis sensitivity, and reduced susceptibility to Brownian noise, all crucial for the realization of lateral inertial sensors. Finally, unlike conventional bulk micromachining, etching by DRIE is not limited by crystal plane orientations. Corner compensation issues are absent, and higher device density can be attained.

Several groups have previously combined wafer bonding with DRIE to fabricate high-aspect-ratio inertial sensors [5,6]. In these previous works, however, an interconnection scheme is either not reported, or only possible at the perimeter of the mechanical structures. An interconnection scheme is especially important for capacitive sensors or comb drive structures which have sense/drive electrodes that need to be electrically interconnected in high density. This work realizes a new interconnection scheme for electrical signal routing with signal crossovers. This versatile routing scheme can connect any part of the device without the restriction of peripheral connection.

1.3 Aligned Wafer Bonding

Wafer bonding is an enabling technology for the integrated sensor process described in this thesis because it achieves IC compatibility through the sealed cavity process. It also provides a powerful additive technology for adding a thick layer of material to a substrate, both of which can be patterned, to form complicated structures which are hard to achieve with conventional deposition methods.

The general process of direct wafer bonding can be summarized as a three-step sequence: surface preparation, contacting, and annealing [7]. The starting wafers must be smooth and flat, as characterized by surface roughness and bow. The surface preparation step involves

cleaning the two wafers to form hydrated surfaces. The contacting step involves pressing the two surfaces together at one central point where a contact wave is initiated and sweeps across the entire surface, thus bringing the two wafers into intimate contact. The final step is an anneal of the contacted pair at elevated temperatures (typically 800°C-1200°C) to increase the bond strength.

In this work, alignment between the two wafers is necessary during the contacting step since features are present on both surfaces. This is accomplished using an Electronic Vision EV 450 Aligner and AB1-PV Bonder [8]. One wafer is first fed into the bond aligner where it is aligned to a set of cross-hairs. The second wafer is then brought in and aligned to the same set of cross-hairs and hence to the first wafer. After alignment, the two wafers are clamped together in a bond fixture with an appropriate separation gap between them. The bond fixture is next loaded into the bond chamber where the wafers are pushed into contact with each other under controlled ambient.

1.4 Deep Reactive Ion Etching (DRIE)

Deep reactive ion etching (DRIE) is another enabling technology for the integrated sensor process described in this thesis. It enables the fabrication of high-aspect-ratio structures crucial for the realization of high performance lateral inertial sensors that displace in the plane of the wafer.

The deep reactive ion etcher used in this work is a Surface Technology Systems multiplex ICP [9]. High etch rate is made possible by the ionization efficiency of inductively coupled plasmas (ICP). Anisotropy is made possible by the time multiplexed deep etching (TMDE) technique which utilizes alternate etch and passivation cycles to preferentially etch the bottom of a trench while inhibiting sidewall etch. The major variables are: gas flow rate, etch/passivation cycle time, electrode power and pressure. Together, they form a large parameter space that determines the etch rate, uniformity, aspect ratio dependent etching and anisotropy [10].

Several phenomena are associated with DRIE, including RIE lag, footing and gap-widening. All of these have a direct bearing on the process development as will be explained later in this thesis.

1.5 THESIS OUTLINE

Chapter 1 has given an overview of the present work by reviewing the micromachined inertial sensors, the integrated sensor approach and the two enabling technologies, namely aligned wafer bonding and DRIE. Chapter 2 describes in detail the design of a process flow for fabricating integrated inertial sensors. The process results are contained in Chapter 3. Chapter 4 delineates the design of the accelerometers and gyroscopes which are used as vehicles for demonstrating the process technology. Characterization of these devices is given in Chapter 5. Chapter 6 concludes by summarizing the contributions of this work and suggesting possible future work.

2. PROCESS DESIGN

The preceding chapter has introduced the sealed-cavity process as a generic approach to fabricating integrated sensors. This chapter describes an actual implementation of such an approach for fabricating high-aspect-ratio inertial sensors. The IC and cover wafer as depicted in Figure 1.1 are not implemented in this work. The process flow is shown in Figure 2.1 and will be explained in the following sections. Sections 2.1 and 2.2 describe the process steps prior to bonding for the handle wafer and the device wafer respectively. Section 2.3 describes all subsequent process steps for the handle-device wafer pair. The process traveler is included in Appendix A. Step numbers therein will be referenced in what follows.

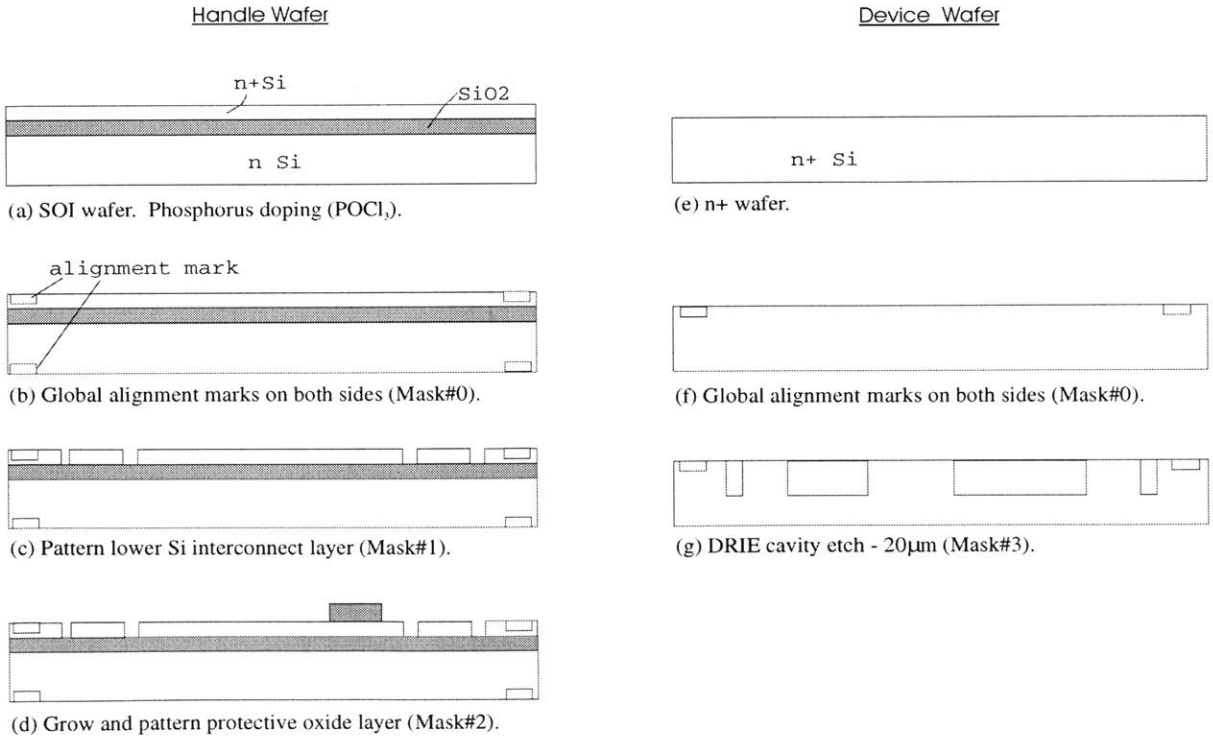


Figure 2.1 Integrated inertial sensor process flow

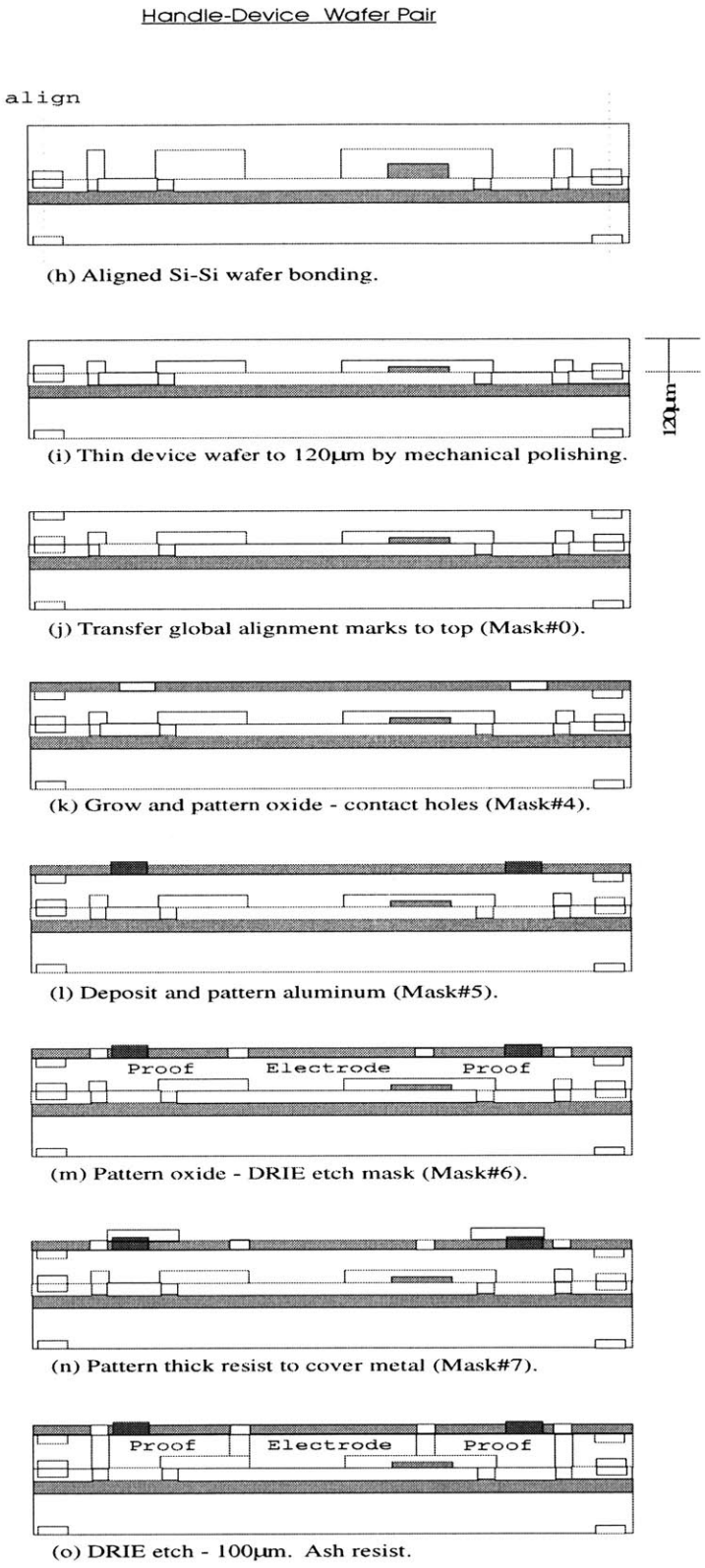


Figure 2.1 Integrated inertial sensor process flow (continued)

2.1 HANDLE WAFER PROCESS

Starting material (Figure 2.1(a); steps 1-3)

The starting material for the handle wafer is a double-sided polished 4-inch n-type SOI wafer. The SOI layer (4-6 Ωcm) is about 2μm thick, on top of 1μm SiO_2. Apart from providing a handle for the device wafer to attach to, the SOI layer also serves as a lower interconnect layer to connect otherwise isolated regions on the device wafer. Because of this latter function, the handle wafer is heavily doped by phosphorous diffusion with a $POCl_3$ source in order to reduce the interconnect resistance.

Global alignment marks (Figure 2.1(b); steps 4-11)

To provide a reference for all subsequent photolithography and bonding alignment, global alignment marks are needed on both the front and back sides of the wafer. The patterning is done with 1μm standard resist using Mask#0 plus a matching dark field jig[※]. The alignment marks are first patterned and etched on the back side, during which the front side is coated with resist to avoid scratch. The alignment marks are then "transferred" to the front side using IR alignment. The etch is about 0.5μm deep and is done using a Lam 480 Plasma Etcher.

Lower interconnect (Figure 2.1(c); steps 12-15)

The SOI layer is then patterned with 1μm standard resist using Mask#1 and clear field jig. A Lam 480 Plasma Etcher is used for the etch. The purpose of this step is to define the interconnect layer used for electrically connecting otherwise isolated regions on the device wafer. This interconnect layer can be regarded as an extra plane for interconnecting the device layer in addition to the device layer itself (and possibly the upper bond wire or capping wafer). It provides a capability for signal crossovers which is otherwise unattainable, and is one peculiarity that sets this process technology apart from other similar processes.

[※] Jigs are used in most of the exposure steps. There are two jigs: one covering the whole wafer except the alignment marks, the other covering only the alignment marks and the edge of the wafer. They will be referred to as dark field jig and clear field jig respectively.

Protective oxide (Figure 2.1(d); steps 16-21)

Next, a 0.5μm thick oxide is thermally grown with wet oxidation at 1000°C for about 50 minutes. The oxide layer is then patterned with image reversal resist using Mask#2 plus clear field jig[※]. Double coating of resist can be done if necessary to ensure good step coverage of the ~2μm topography. The image reversal process (hot plate post-bake plus flood exposure) then follows to essentially reverse the polarity of the resist. A clear mask is not recommended for the flood exposure, as any opaque spots on the mask, however small, will ultimately translate into oxide remains on the wafer which may potentially prevent bonding. The oxide is etched using BOE. The oxide pattern defined in this step serves to protect the underlying Si interconnect from being etched during the final DRIE release step. The Si interconnect needs to be covered with oxide only at regions that will be exposed to DRIE and only when such exposure is detrimental to device operation.

2.2 DEVICE WAFER PROCESS

Starting material (Figure 2.1(e))

The starting material for the device wafer is a double-sided polished 4-inch n-type wafer. Although n-type wafers (0.2-6 Ωcm) are used in this work, n+ wafers are recommended since the capacitors and/or comb fingers in the capacitive inertial sensors are supposed to be good electrical conductors.

Global alignment marks (Figure 2.1(f); steps 22-25)

Global alignment marks are patterned on one side of the wafer (the side to be bonded with the handle wafer) with 1μm standard resist using Mask#0 with dark field jig. The etch is about 0.5μm deep and is done using a Lam 480 Plasma Etcher.

[※] The reason for using a dark field Mask#2 in combination with image reversal is to save some processing steps. If Mask#2 is made clear field, some oxide will remain around the alignment mark regions after BOE. In that case, a few extra steps are required to remove these oxide remains in order to avoid problems during bonding.

Cavity (Figure 2.1(g); steps 26-29)

The device wafer is then patterned with 1μm standard resist using Mask#3 with clear field jig. Cavities are formed by a 20μm DRIE etch with the resist as etch mask. The etch depth defines the distance between the proof mass of the devices and the handle wafer and hence the parasitic capacitance between them. A 20μm etch depth is chosen to minimize such parasitic capacitance. This step essentially defines the anchors that support the devices on the handle wafer.

2.3 HANDLE-DEVICE WAFER PAIR PROCESS

Wafer bonding (Figure 2.1(h); steps 30-32)

The handle wafer and the device wafer are now ready for bonding. The two wafers are first subjected to a RCA clean to form hydrated surfaces. They are then aligned with each other in the Electronic Vision EV 450 Aligner. The device (top) wafer should be loaded first followed by the handle (bottom) wafer. After alignment, they are clamped together in the bond fixture with a separation gap defined by three flags. The whole bond fixture is transferred from the aligner to the Electronic Vision AB1-PV Bonder where the flags are removed and the two wafers are pressed against each other at 3000mbar in 100% N_2 under computer control. Finally the contacted pair is annealed at 1100°C for one hour to increase the bond strength.

Thinning (Figure 2.1(i); steps 33-35)

Next, the device wafer (now part of the handle-device bonded pair) is thinned down to 120μm by mechanical polishing. This results in 100μm thick mechanical elements supported by 20μm tall anchors defined earlier by a 20μm DRIE cavity etch. The polishing service is provided by Lincoln Laboratory. After polishing, the wafers should undergo a post-polishing cleaning procedure before they are brought back into the cleanrooms.

Global alignment marks (Figure 2.1(j); steps 36-39)

Global alignment marks are patterned on top of the bonded pair with 1μm standard resist using Mask#0 with the dark field jig. During alignment at the contact aligner, three sets of alignment marks on the bonded pair can be successively seen under infrared as the focus is being adjusted. The mask should be aligned with respect to the alignment marks which are defined at steps 22-25 (Figure 2.2) because all subsequent features should be aligned to the cavities or anchors defined at steps 26-29 rather than the lower Si interconnect. This is not an issue if the bonding misalignment is small because the three sets of alignment marks should coincide well then. The alignment marks are etched using a Lam 480 Plasma Etcher with an etch depth of about 0.5μm.

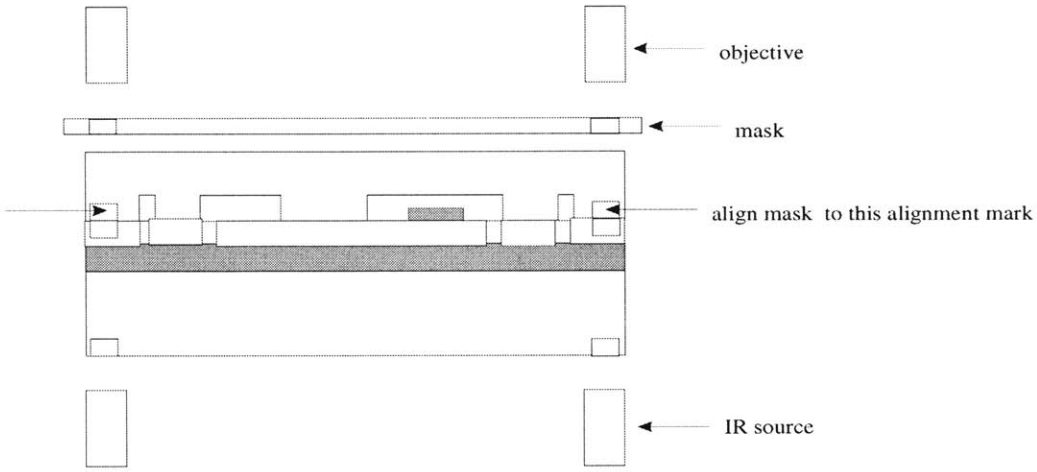


Figure 2.2 Mask alignment at step 37

IC fabrication

At this point, the bonded pair is ready to be sent to an IC foundry for circuit fabrication. The circuit can be fabricated either on the top surface of the device wafer as is, or on an epi layer grown on top of the device wafer, depending on the starting material requirements of the foundry. This IC fabrication step is not done in this work.

Oxidation (Figure 2.1(k); steps 40-41)

Next, a 1.5μm thick oxide is thermally grown with wet oxidation at 1100°C for about 290 minutes. This oxide layer will serve as the DRIE etch mask at the final release step. Regular resist is not a feasible etch mask in this case. Its relatively low selectivity (compared with oxide) necessitates a relatively thick layer to survive the etch (e.g. >6μm). Small gaps (e.g. 3-5μm) cannot be defined accurately with such a thick resist because wet development of thick resist results in poor patterning resolution and also the resist gap tends to blow out as the etch proceeds. The use of thermal oxide as a DRIE etch mask is actually not IC compatible because thermal oxidation is a high temperature process. If the wafer has run through the IC fabrication, a high-aspect-ratio polymer mask such as SU-8 should be used which is both IC compatible and able to faithfully transfer small features.

Contact hole (Figure 2.1(k); steps 42-45)

The oxide is then patterned with 1μm standard resist using Mask#4 with the clear field jig. This is followed by a BOE etch to define the contact holes through which the metal makes contact with the Si. This step is needed only if thermal oxide is used as the DRIE etch mask, and can be omitted otherwise.

Metallization (Figure 2.1(l); steps 46-53)

A 1 μm thick aluminum is deposited by electron beam evaporation. The aluminum is then patterned with image reversal resist using Mask#5 plus the clear field jig. The image reversal process (hot plate post-bake plus flood exposure) then follows to essentially reverse the polarity of the resist. A clear mask is not recommended for the flood exposure, as any stains or residues on the mask tend to transfer and get stuck to the wafer. A PAN (Phosphoric-Acetic-Nitric) etch is then done at around 40°C to define the bond pads, followed by a sintering step at around 400°C to ensure good contact formation. The metallization is actually part of the IC process, and therefore this step can be omitted if the wafer has gone through the IC fabrication at a foundry.

DRIE mask (Figure 2.1(m); steps 54-57)

The oxide is now patterned with standard resist using Mask#6 to define the DRIE pattern. No jig should be used during exposure so that the dicing lanes that separate the dies can run all the way to the edge of the wafer, thereby facilitating manual dicing using a scribe. Double coating is necessary to achieve a resist thickness of about 2.5μm. Such a thickness is required to survive the etch given the low selectivity associated with the dry plasma etch which is done using the Applied Materials Precision 5000 Etcher.

Resist cover (Figure 2.1(n); steps 58-59)

Before the final DRIE etch, the metal has to be covered by resist to avoid contaminating the DRIE machine. This is done by patterning the wafer with thick resist using Mask#7 which will be a clear field mask covering the metal regions only and leaving the rest of the wafer exposed. An alternative, which is adopted in this work, is to use Mask#6 and rely on overdeveloping the resist. In general, this is not recommended since the thick resist may clog gaps in the oxide layer in case of significant misalignment. Either way, a jig should not be used for the same reason mentioned above.

DRIE release (Figure 2.1(o); steps 60-61)

This step serves the dual purposes of first defining and subsequently releasing the sensor structure. It involves a three-step DRIE sequence. First, DRIE is done without the passivation step to yield an isotropic etch of a few microns depth. This is to minimize the undesirable DRIE gap-widening effect. A regular anisotropic DRIE recipe is then used to etch almost all the way down the 100μm thick mechanical elements until the etch is close to completion, at which point the recipe is shifted to one which has less DRIE footing effect. The end point is detected by placing test structures that will fall off when released at several locations on the wafer. DRIE footing and gap-widening effects will be discussed in the next chapter.

Capping wafer

After DRIE release, a capping wafer can be bonded on top of the device wafer by thermocompression gold-to-gold bonding at the wafer level. This provides a powerful

wafer-level packaging technique to protect the sensor from the environment and/or to achieve vacuum sealing essential for resonating types of devices such as the gyroscope, allowing a significant reduction in packaging cost in a manufacturing environment. The thermocompression gold bonding also realizes an upper level interconnect (as opposed to the lower Si interconnect) which serves to interconnect different parts of the sensor (e.g. connecting the mechanical structures to the electrical circuits). This step is not implemented in this work. If it is, gold deposition and patterning on the device wafer should be done prior to DRIE release.

Dicing

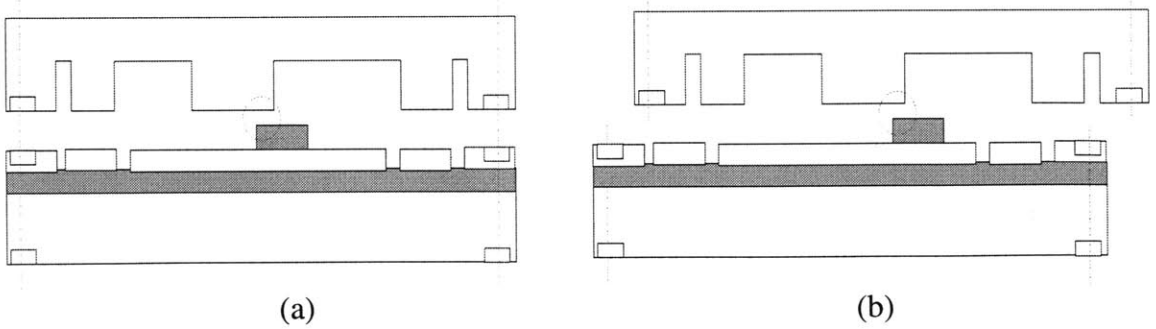
Currently, dicing is done manually. The wafer will break along the dicing lanes (200μm wide; etched during the final DRIE step) when scribed with a diamond scribe. The diesaw is not used because there is a potential danger of the fragile mechanical structures being damaged by excessive vibration, and also because the device narrow gaps will be fouled up by the water during the diesaw operation. The use of a capping wafer will eliminate these problems.

3. PROCESS RESULTS

In the course of developing the process described in the preceding chapter, a number of problems are encountered. Section 3.1 describes a problem associated with wafer bonding, while Sections 3.2 and 3.3 discuss DRIE gap-widening and footing respectively. Some other miscellaneous processing problems are described in Section 3.4. Based on the processing and equipment constraints as well as the problems identified, a set of design rules for this process technology is formulated and is given in Section 3.5. Finally a modified process is proposed in Section 3.6 to avoid some of the problems encountered.

3.1 WAFER BONDING PROBLEM

Any protrusion from the wafer surface can produce problems in the bonding. Figure 3.1 depicts a potential scenario in the context of this process in which the overlapping of an anchor with the protective oxide prevents bonding from occurring. Such overlapping can result from a flaw in mask design (Figure 3.1 (a)) or simply from a bonding misalignment (Figure 3.1(b)); the latter can be allowed for by adhering to proper design rules during the mask layout stage. Figure 3.2 shows the IR image of a bonded pair whose left part is not properly bonded due to a design error in the protective oxide mask (Mask#2).



(a) (b)

Figure 3.1 Bonding problem due to (a) an error in mask design (b) bonding misalignment

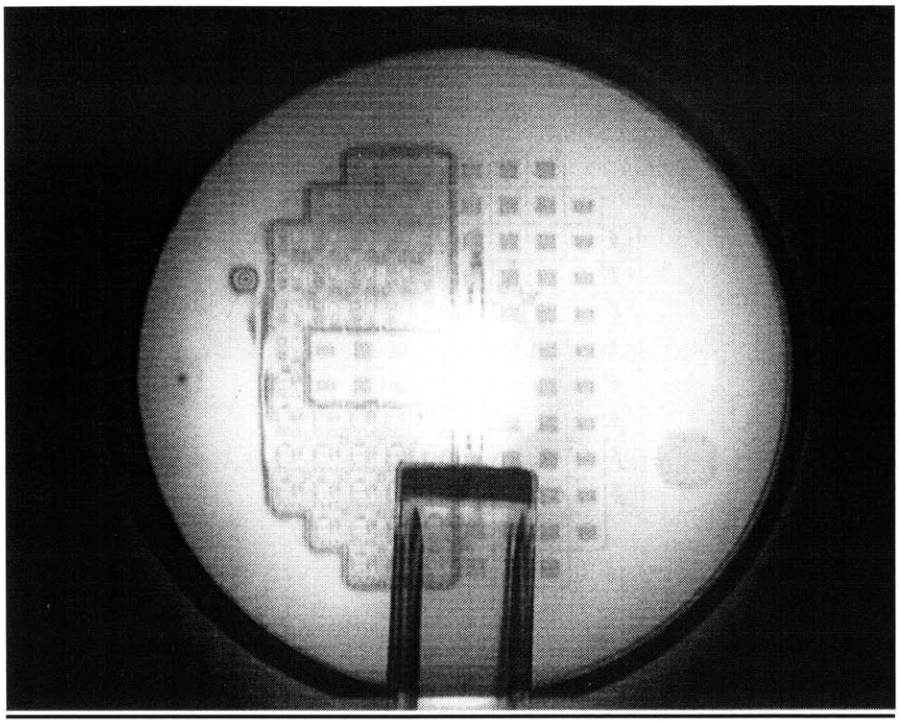
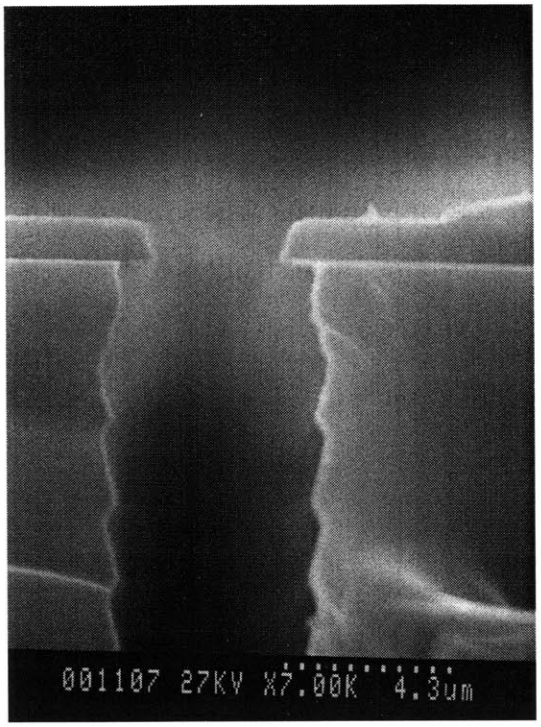
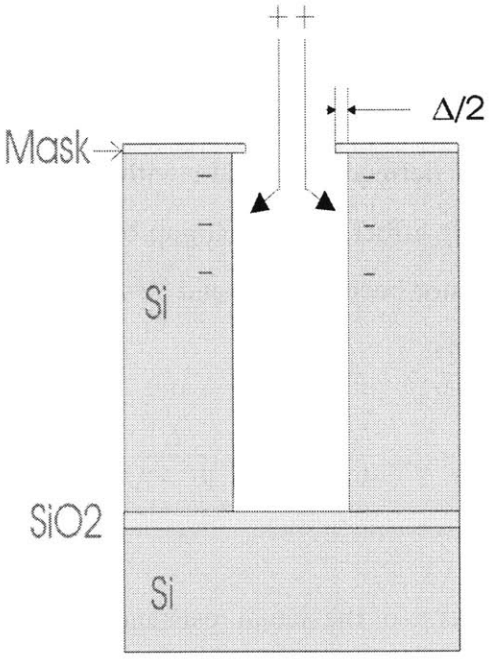


Figure 3.2 An IR image of a bonded pair whose left part is not bonded well due to a design error in the protective oxide mask (Mask#2)

3.2 DRIE GAP-WIDENING

During process development, it is observed that for SOI wafers, the actual gap etched by DRIE becomes wider than that defined by the oxide etch mask (Figure 3.3(a)). This phenomenon is not observed in regular non-SOI wafers. It is believed that the sidewall tends to be charged up negatively by the electrons in the plasma [11,12] and therefore deflects the downward positive ion flux sideways (Figure 3.3(b)). The resulting lateral component of the etch tends to widen the gap. For regular non-SOI wafers, this negative sidewall charging is less of a problem because charges can flow to ground via the wafer chuck. Such a path to ground is blocked by the buried oxide in the case of SOI wafers.





(a) (b)

Figure 3.3 DRIE gap-widening (a) A SEM photo showing the actual gap being conspicuously wider than the opening in the oxide etch mask (b) Conjectured mechanism

For inertial sensors, device characteristics depend strongly on the tether width (w) and the gap associated with the capacitive sense/drive electrodes (g) (Table 3.1). The gap-widening effect implies an inability to control w and g accurately and therefore is undesirable in general.

Characteristics of a typical lateral accelerometer	Dependence on w, g
tether stiffness	w^{3}
mechanical sensitivity (displacement per unit acceleration)	w^{-3}
mechanical resonant frequency	$w^{1.5}$
sense capacitance	g^{-1}
electrical sensitivity (capacitance change per unit acceleration)	$w^{-3} g^{-2}$

Table 3.1 Dependence of device characteristics on tether width (w) and capacitor gap (g) for a typical lateral accelerometer

To characterize this gap-widening effect, test structures are placed on the wafer from which the difference between the actual gap and the oxide mask opening (Δ in Figure 3.3(b)) can be extracted. The test structures are a set of 7 resistors with the same nominal length (L) 1000μm and different nominal width (W) varying from 10μm to 40μm in steps of 5μm defined by a halo with nominal gap size g (Figure 3.4(a)). Due to the gap-widening effect, the actual gap becomes g+Δ and therefore the actual length and width of the resistor become L+Δ and W-Δ respectively. Consequently, the actual resistance of the resistor is:

$$R = R_S \frac{L+\Delta}{W-\Delta} \approx R_S \frac{L}{W-\Delta} \qquad (L >> W >> \Delta) \qquad (3.1)$$

The inverse of the actual resistance is:

$$\frac{1}{R} \approx \left(\frac{1}{R_S L}\right) W - \frac{\Delta}{R_S L} \qquad (3.2)$$

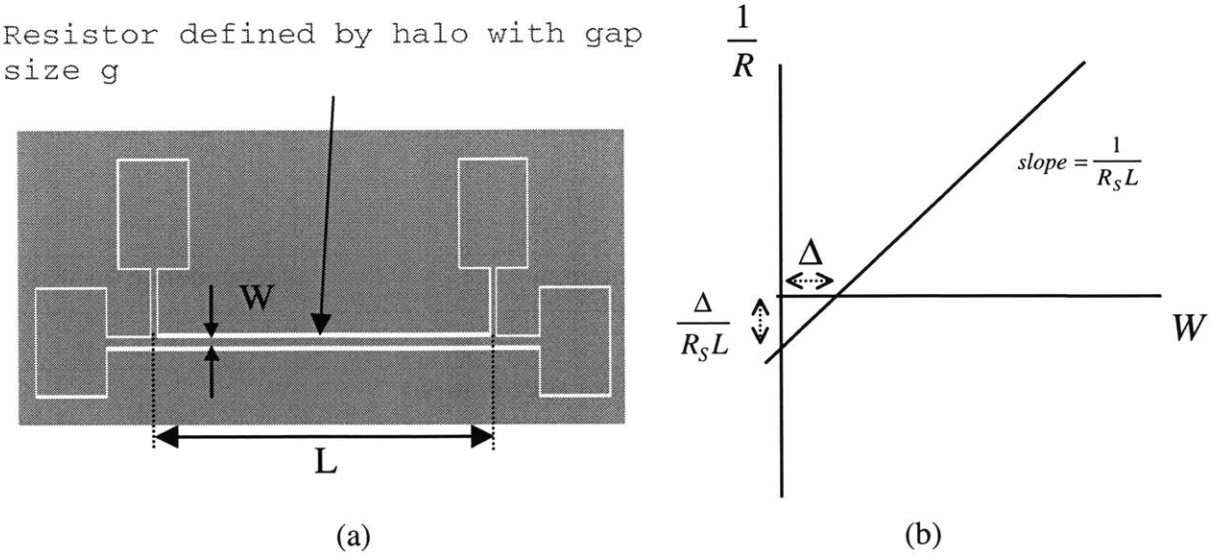


Figure 3.4 (a) Test structure for extracting Δ (b) A plot of 1/R versus W

A plot of the inverse of actual resistance versus nominal width thus gives a straight line with slope $1/R_SL$ and x-intercept Δ (Figure 3.4(b)). The actual resistance is extracted from the V-I characteristics using a HP4145B semiconductor analyzer. Figure 3.5 shows such a plot for a set of test resistors located on the lower left of the wafer for a nominal halo gap size of 3μm. Δ is read from the x-intercept to be about 1.8μm, meaning that the nominal 3μm gap is widened to about 4.8μm because of the DRIE gap-widening effect.

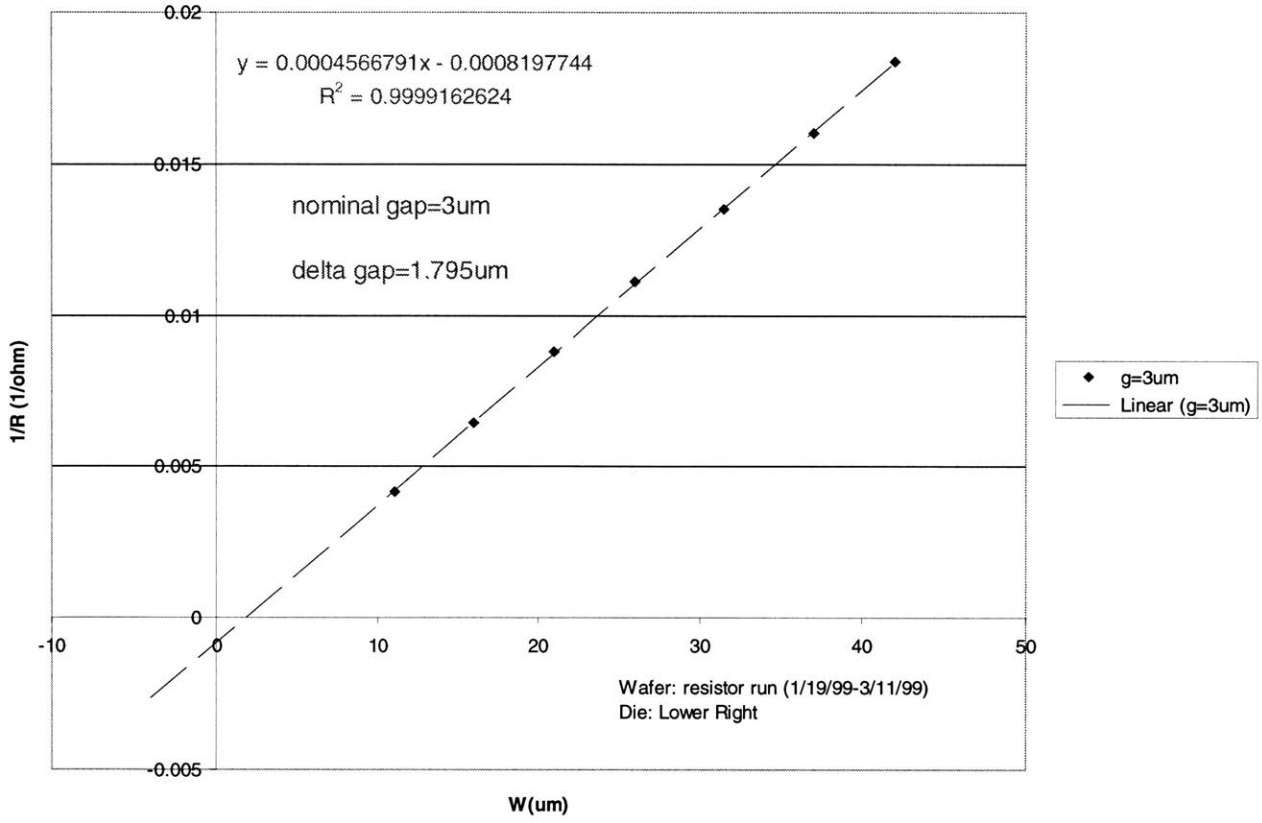


Figure 3.5 A plot of 1/R versus W for a set of test resistors with a nominal halo gap g=3μm

Using this method, the difference between the actual gap and the oxide mask opening (Δ) is determined for 3 different nominal halo gap size g=3,5,10μm at four locations (lower-left, lower-right, upper-left, upper-right) on the wafer. The result is shown in Figure 3.6 and agrees with values obtained from SEM. There are two observations. First, Δ is larger for a larger nominal gap. Second, Δ depends on where the gap is located on the wafer.

The dependence of Δ on location is found to correlate with the dependence of etch rate on location which, in turn, is related to the geometric arrangement of the coil power coupling and the gas feed schemes used in the DRIE equipment.

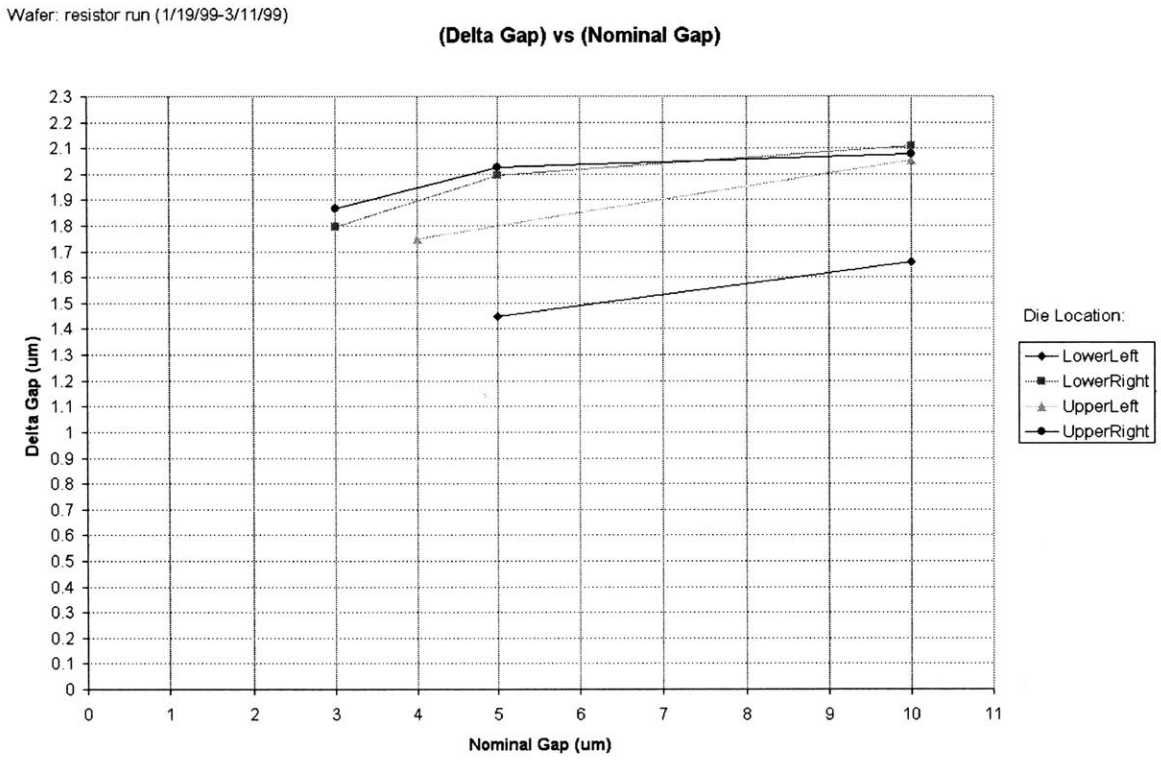


Figure 3.6 A plot of Δ (as determined from the test resistors) versus nominal gap size g for different locations on the wafer

Because of its dependence on gap size and location, allowing for Δ at the mask design stage is not a practical solution to the gap-widening effect. Since this effect originates from the interaction between the negative sidewall and the positive ion flux, it can be supposedly suppressed by minimizing such interaction. Thinking along this line leads to a two-step etching process that solves the problem (Figure 3.7(a)). The first step involves a shallow etch of the feature isotropically in a SF_6 plasma which can be done with DRIE with the passivation cycle removed. The next step is an anisotropic DRIE etch. Because the first step removes the silicon around the mask opening, the negative charging is far enough from the ion flux so as not to affect the flux direction significantly. Figure 3.7(b)

shows the result of this two-step process. The relationship between Δ (as determined from SEM) and the amount of initial isotropic etching for a nominal gap g=3μm is shown in Figure 3.8. While the gap-widening effect can be suppressed, the initial side-etching inherent in this solution implies that a narrow beam cannot be fabricated.

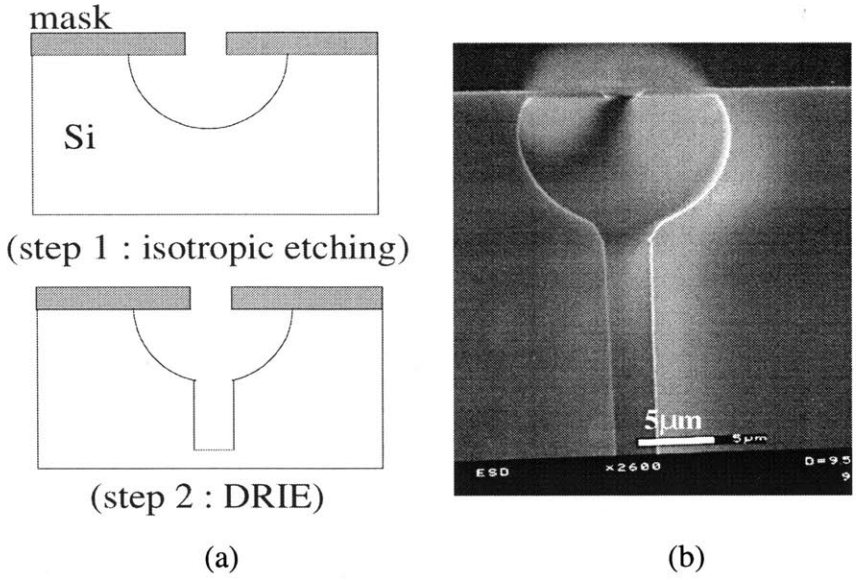


Figure 3.7 Solution to gap-widening (a) Two-step etching process (b) A SEM photo showing the etch profile obtained by this process (Courtesy of Kei Ishihara)

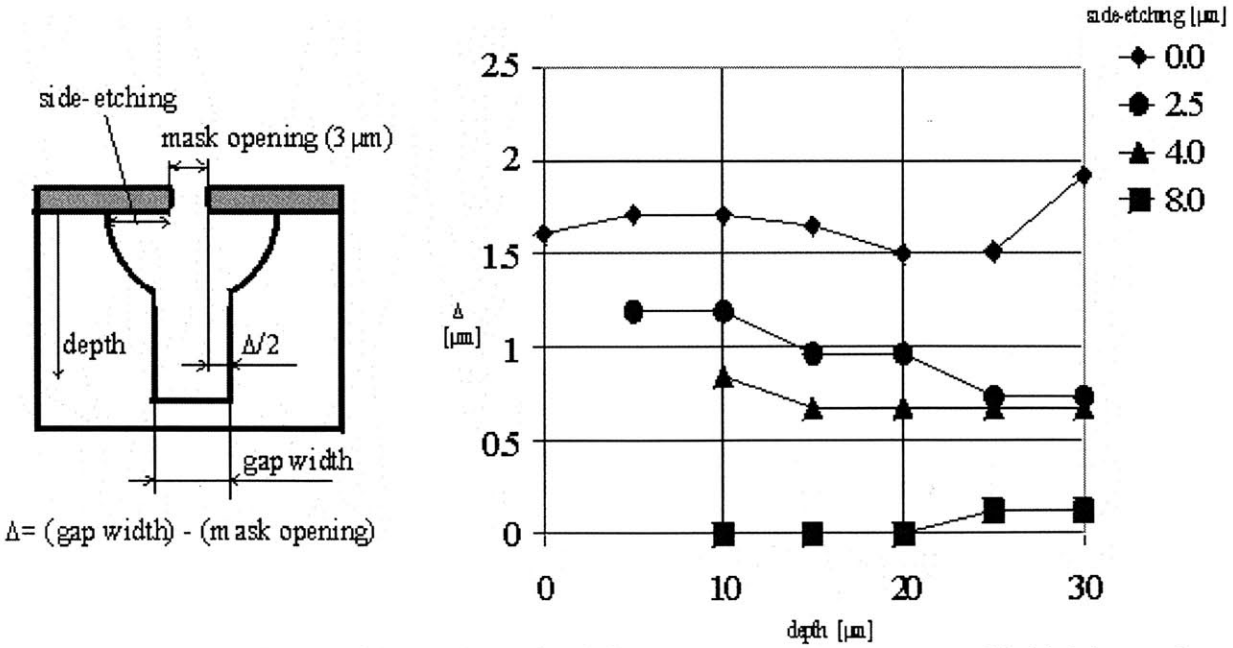
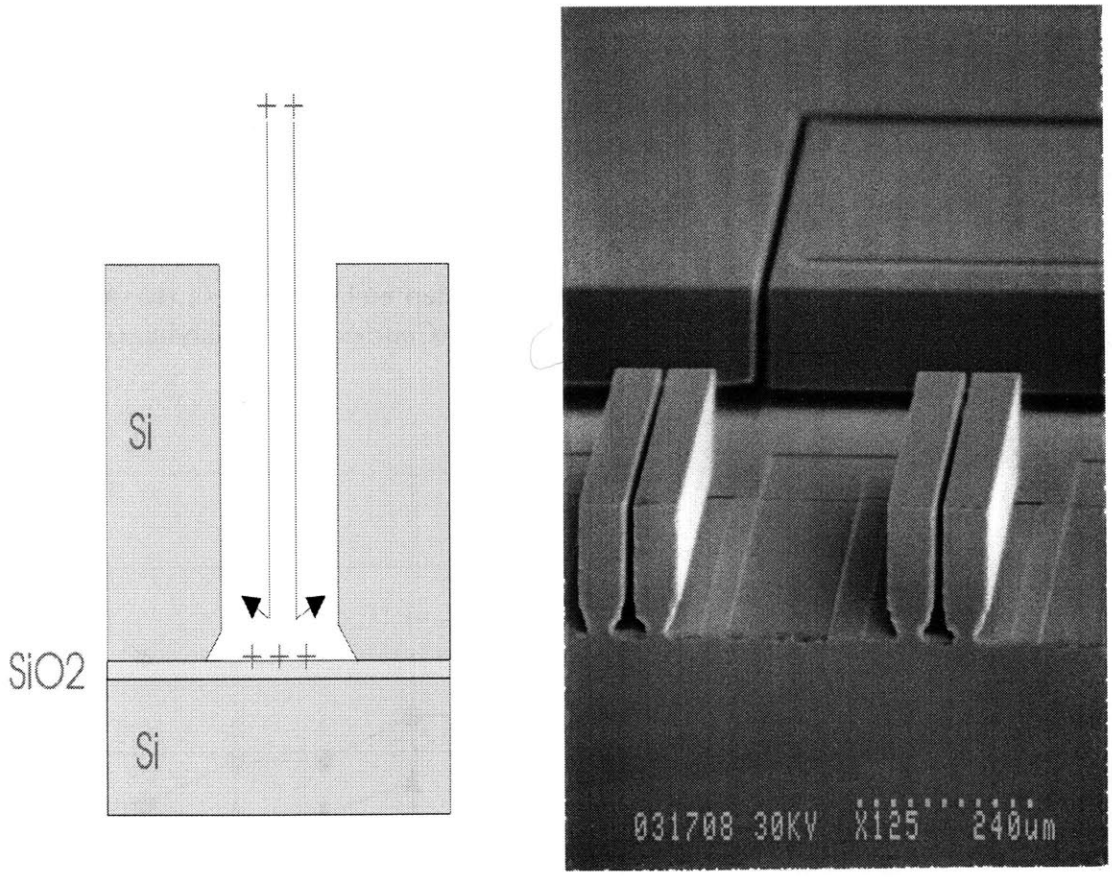


Figure 3.8 Dependence of Δ (as determined from SEM) on the amount of initial isotropic etching for a nominal gap g=3μm (Courtesy of Kei Ishihara)

3.3 DRIE FOOTING

In plasma etching, it has been reported that there is a notching or footing effect, which is a rapid lateral etching at the silicon/oxide or polysilicon/oxide interface [11,13,14,15]. This is negligible in most etching systems, but becomes more evident in DRIE because of their high density plasma. The oxide layer tends to be charged positively and deflects the ion flux sideways, leading to a noticeable lateral etch (Figure 3.9(a)). Because of this footing effect, the lower part of the device structures are etched unexpectedly during process development. Figure 3.9(b) shows part of an accelerometer (without the proof-mass). The footing at the bottom of the electrodes can be clearly seen.

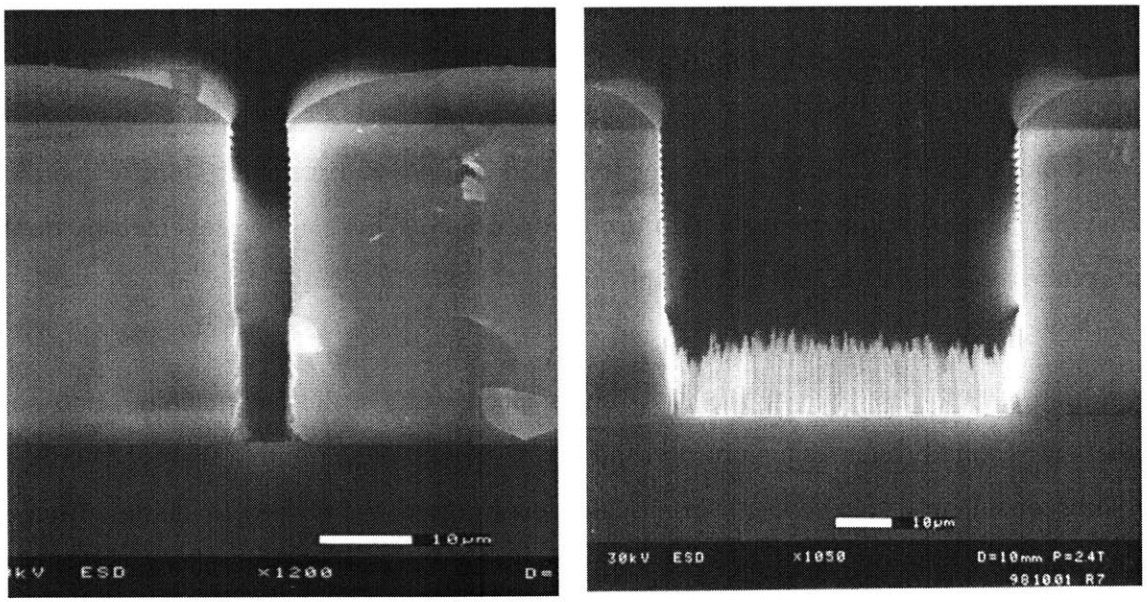


(a) (b)

Figure 3.9 DRIE footing (a) Conjectured mechanism (b) A SEM photo showing DRIE footing at the bottom part of the electrode structures of an accelerometer

The footing effect is aggravated by the fact that DRIE etch rate has a strong dependence on trench width [10]. In general, wide trenches are etched faster than narrow trenches and therefore will be over-etched for a long time while waiting for narrow trenches to clear. Eventually, structures with small anchors will be completely undercut if the over-etch is allowed to prolong.

The attempt to reduce footing by increasing passivation is unsuccessful because it reduces footing in narrow trenches at the expense of grass formation in wider trenches [12] (Figure 3.10). Increased passivation also reduces etch rate and anisotropy. As a result, it is concluded that the only robust solution to the footing problem is to **(1)** require uniform pattern width in the DRIE mask to reduce potential over-etch; **(2)** design large anchors that are tolerant of footing and **(3)** change the etching parameters in the recipe to increase passivation just before the etch is complete.



(a) (b)

Figure 3.10 SEM photos showing the effect of increased passivation (a) Footing is reduced in a 8μm trench. (b) Grass is formed in a 70μm trench. (Courtesy of Kei Ishihara)

3.4 MISCELLANEOUS PROBLEMS

It is found that after the thinning process, some chipping occurs at the edges of the device wafers. This is undesirable because wafers which are not intact will be refused by IC foundries.

Currently the metal patterning is done with a dark field mask (Mask#5) in combination with image reversal. This is to avoid leaving some metal around the alignment mark regions after the PAN etch, as will be the case for a clear field mask. However it is found that the image reversal resist does not adhere very well on the aluminum layer. As a result, some metal under the resist is attacked by the PAN etch. Sometimes some resist patterns even come off just after the development step. To minimize the problem, development time and PAN etch time are kept to the minimum necessary. Experimentation on process parameters such as pre-bake and post-bake time can be carried out to see if adhesion can be improved or not. If the problem is deemed unacceptable, it is suggested that the metal mask (Mask#5) be reverted to clear field so that standard resist can be used. In that case, metal left around the alignment marks after the PAN etch has to be subsequently removed.

It is found that the metal and Si do not form good ohmic contact and exhibit some diode behavior. This is a problem especially for dc operation. This can be prevented by doping the contact regions before the metal deposition.

The first completed wafer in the first run is diced using a diesaw machine, and some tethers are found broken. This prompts the use of manual dicing with a diamond scribe for all subsequent runs. However, in some later test run with the diesaw machine, all tethers remain intact. It is suggested more experimentation with the diesaw process be carried out to characterize the survivability of tethers upon diesawing. The water used during the diesaw operation is another concern, but it will become a non-issue if a capping wafer is implemented.

3.5 DESIGN RULES

This section summarizes the information needed by individuals interested in designing devices using this process technology.

Masks

Table 3.2 lists the masks used in this process.

Mask#	Field	Purpose	
0.1-0.4 **(GLOBAL)**	-	These are the same mask physically and are used for putting alignment marks on the front and back sides of both wafers. These global alignment marks are used for all photolithography and wafer bonding alignment.	
		0.1	bottom of handle wafer
		0.2	top of handle wafer
		0.3	bottom of device wafer (i.e. contact surface with 0.2)
		0.4	top of bonded pair (after polishing)
1 **(SILICON)**	Dark	This mask defines the lower Si interconnect pattern on the SOI starting material. This layer is about 2μm thick, on top of 1μm SiO_2, and is heavily doped.	
2 **(OXIDE)**	Dark	This mask defines the protective SiO_2 pattern. This thermal oxide layer protects the lower Si interconnect region from etch during the DRIE.	
3 **(CAVITY)**	Dark	This mask defines the anchors of the structures and corresponds to the cavity of the sealed cavity process. A 20μm DRIE etch is used for reduced parasitics, but this can be adjusted. This mask has to be mirror-imaged, since it is a 'backside' mask.	

4 **(CONTACT)**	Dark	This mask opens contact holes on the oxide layer which is used as the DRIE etch mask. The metal makes contact with Si through these contact holes.
5 **(METAL)**	Dark	This mask defines the metal layer. Currently ~1μm thick Al or AlSi is used.
6 **(DRIE)**	Dark	This mask patterns the oxide etch mask for the DRIE, which is a 100μm deep etch through the device wafer.
7 **(COVER)**	Clear	This mask patterns a thick resist layer to cover the metal, so that the metal will not be exposed to the DRIE.

Table 3.2 Masks used in this process technology

Currently, mask exposure is done with a Karl Suss MA-6 Mask Aligner capable of backside alignment using IR illumination. The tolerance for alignment on the same plane (front-side alignment) is about 3μm. The tolerance for alignment on different planes (backside alignment using IR) is about 5μm. Wafer bonding is done using Electronic Vision EV 450 Aligner and AB1-PV Bonder. The bonding misalignment should be less than 3μm according to the manufacturer's specification. However, a misalignment of more than 10μm is quite often observed in practice. To allow for this, a tolerance of 20μm for the aligned bonding is assumed for design purposes. Table 3.3 gives the alignment map for the masks and the tolerances involved.

Mask#		Mask#	Tolerance (±μm)
0.2		0.1	5
1		0.2	3
2		0.2	3
3		0.3	3
0.3	is aligned to	0.1	20
0.4		0.3	5
4		0.4	3
5		0.4	3
6		0.4	3
7		0.4	3

Table 3.3 Alignment map and associated tolerances

Die size and dicing

A 'scribe and break' technique is used for dicing. By adding dicing lanes in the **DRIE** mask (Mask#6), DRIE can be used as the 'scribe'. Since some buffer region on each side of a die is needed to ease the hand-breaking process, all device features including the bonding pads should be confined to a $0.5l$ x $0.5l$ square centered at an actual die size of l x l. Diesaw machine can be used in place of hand-breaking if capping wafer is implemented in the future.

Bond pad

Currently, the upper interconnect is realized by wire bonding. If initial testing is to be done at MIT, huge bond pads (~300μm x 300μm) are preferred to allow easier placement of test probes.

Geometrical design rules

Based on the process constraints identified, a set of design rules for this process technology is formulated and is described in Table 3.4. Figure 3.11 explains the nomenclature used. A pictorial description of these rules is given in Figure 3.12.

Rule	Description
A	Minimum lower Si interconnect linewidth in the **SILICON** layer is 15μm.
B	Minimum separation between two isolated lower Si interconnect regions in the **SILICON** layer is 10μm.
C	Minimum anchor size in the **CAVITY** layer is 60μm x 60μm. If the gaps (in the **DRIE** layer) around the anchor are 3 to 5μm wide, the minimum anchor size can be relaxed to 50μm x 50μm. Too small an anchor will be destroyed by the DRIE footing effect.
D	**SILICON** encloses **CAVITY**, with a minimum enclosure boundary of 10μm. This rule, together with rule B, ensure that a bonding misalignment of 20μm or

	less will not cause the anchors to short two supposedly isolated lower Si interconnect regions.
E	Minimum spacing between **OXIDE** and **CAVITY** is 20μm. This allows for the possible bonding misalignment. Violation of this rule may lead to bonding problem.
F	Minimum contact opening in the **CONTACT** layer is 5μm x 5μm.
G	If initial testing is to be done at MIT, then bond pads in the **METAL** layer should have a minimum size of 200μm x 200μm. This allows enough area for the wire bond and/or test probe.
H	**METAL** encloses **CONTACT**, with a minimum enclosure boundary of 5μm. This allows for possible mask misalignment.
I	**COVER** encloses **METAL**, with a minimum enclosure boundary of 15μm. This accounts for the reduced resolution of thick resist.
J	**DRIE** encloses **COVER**, with a minimum enclosure boundary of 15μm. This accounts for the reduced resolution of thick resist.
K	**DRIE** encloses **CAVITY**, with a minimum enclosure boundary of 10μm.
L	**OXIDE** must extend over **DRIE** with a minimum cut-inside of 20μm. This protects the lower Si interconnect from the DRIE.
M	Minimum tether width in the **DRIE** layer is 15μm. The initial isotropic etch used to reduce the DRIE gap-widening effect implies that too narrow a tether cannot be fabricated. Also, tether width cannot be controlled very precisely due to process tolerances.
N	All gaps in the **DRIE** layer should be in the range of 3 to 10μm to keep the gap width variation small across the wafer. This reduces DRIE footing effect.

Table 3.4 Geometrical design rules for this process technology

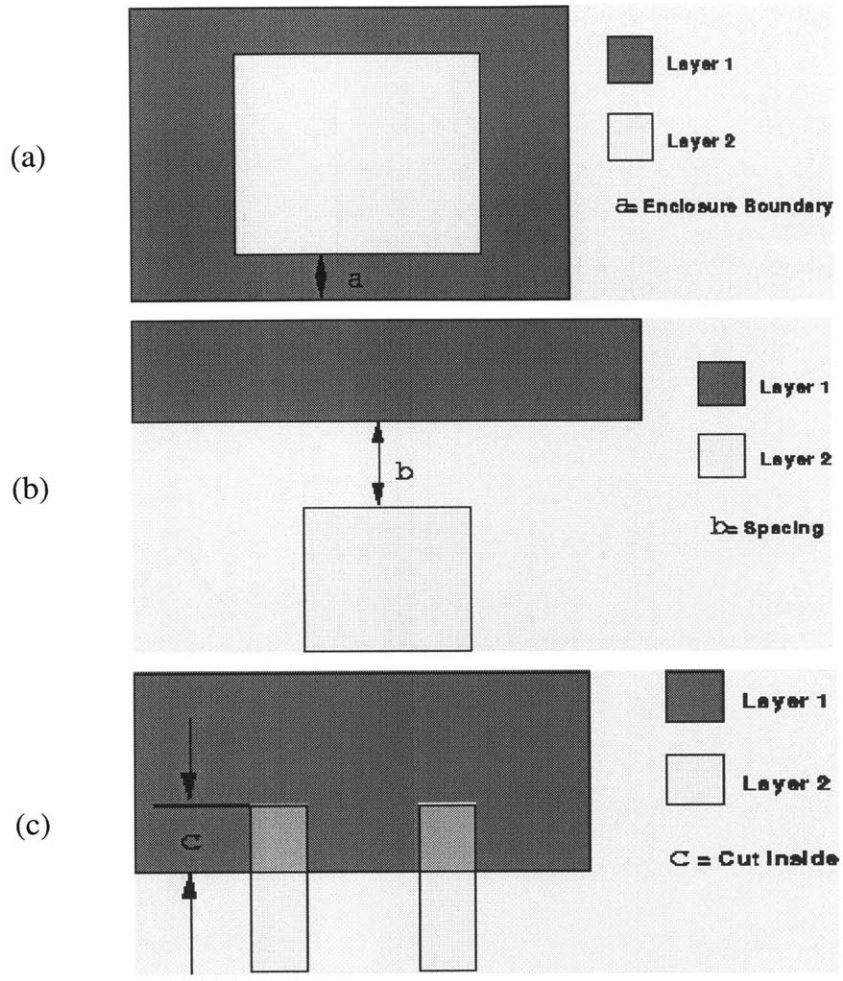


Figure 3.11 Explanation of nomenclature used in the design rules (a) Enclosure boundary (b) Spacing (c) Cut-inside

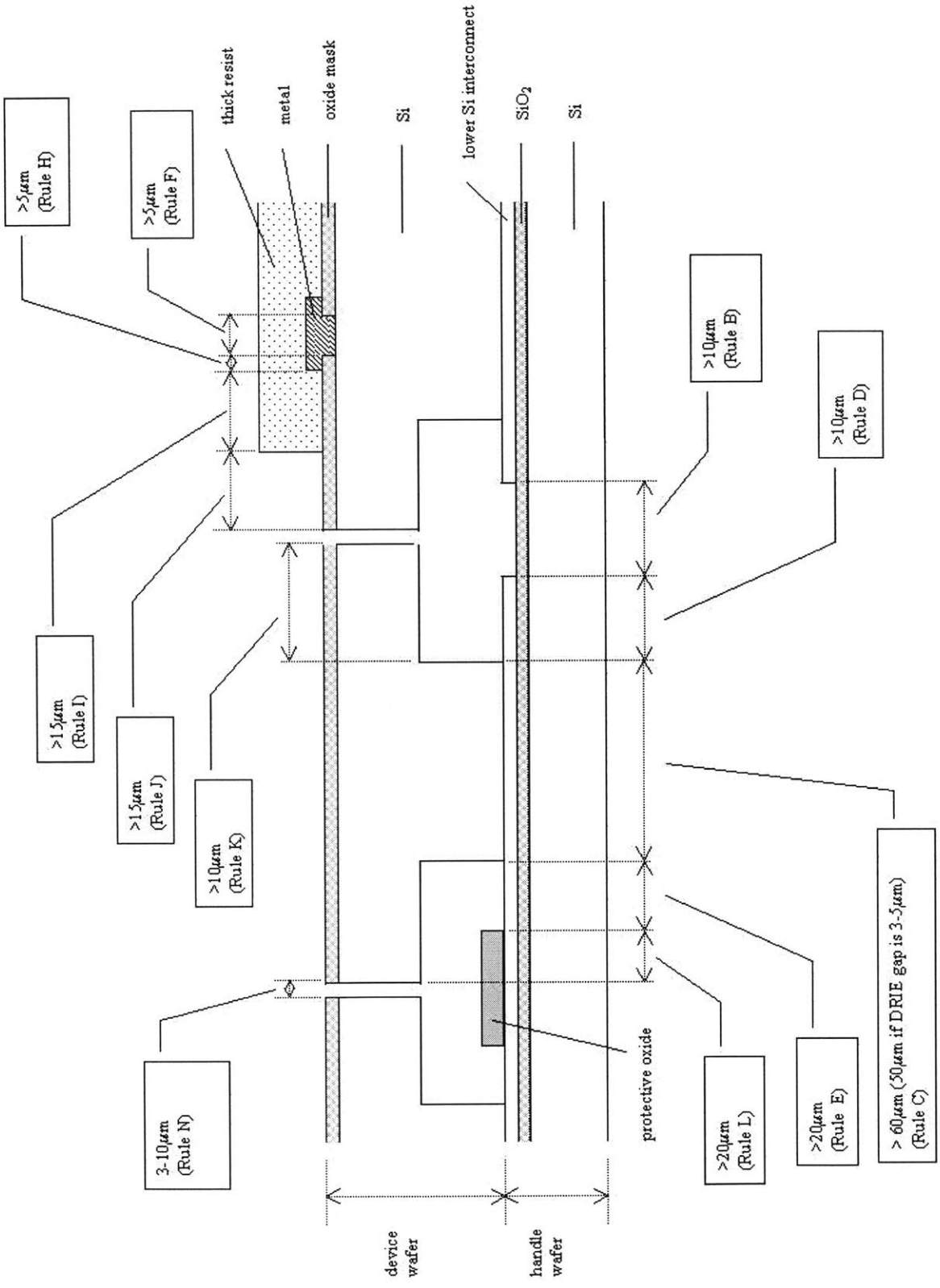


Figure 3.12 A pictorial description of the design rules (cross-sectional view)

3.6 PROPOSED MODIFIED PROCESS

Although solutions have been developed for both DRIE gap-widening and footing, they are not very robust. For example, the isotropic etch used to reduce gap-widening actually widens the gap at its top. This renders the fabrication of thin tethers impossible, and therefore prevents the further shrinking of device size and places a limit on the sensitivity that can be achieved. The isotropic etch also alters the tether stiffness and potentially introduces geometrical non-uniformities which are particularly detrimental to gyroscope operation. Consequently, it will be desirable to develop a process which is not plagued by DRIE gap-widening and footing effects.

Both the DRIE gap-widening and footing effects can be attributed to the buried oxide in the SOI wafer. For DRIE gap-widening, the buried oxide prevents the negatively charged sidewall from discharging to ground, resulting in a lateral etch of the sidewall. For DRIE footing, the reactive ions stop etching further upon hitting the buried oxide layer and begin to etch sideways because they are deflected by the positively charged oxide layer and also because of their sheer accumulation. In either case, the problems should not occur if the DRIE is done on a regular non-SOI wafer. Thinking along this line leads to some proposed modifications to the process. Figure 3.13 shows the proposed modified process side by side with the original process. The idea is to shift the DRIE step which defines the critical sensor features (tethers, electrodes, proof mass etc.) to a regular non-SOI wafer. This critical DRIE step defines features that are most important in determining the device characteristics and hence require precise dimensional control most. Other DRIE steps, such as the DRIE cavity etch which defines the anchors, are less critical in a sense.

In the proposed modified process, the top Si layer of the handle wafer is used as an interconnect as well as anchors (Figure 3.13(b2,3)) while in the original process it serves as an interconnect only (Figure 3.13(a2)). The critical DRIE step which defines the sensor features is now done on the regular non-SOI device wafer before bonding (Figure 3.13(b5)) and is therefore free from the gap-widening and footing effects. The final DRIE step now becomes a rather shallow large-area etch for releasing the structure (Figure

3.13(b8)), while in the original process the final DRIE step serves the dual purposes of first defining the sensor structure and subsequently releasing it (Figure 3.13(a7)).

Several points are worth noting regarding the proposed process: **(1)** some photolithographic steps for the handle wafer now need to be done in rather deep trenches (Figure 3.13(b3,4)). This should not be a big concern since the features on the handle wafer (interconnect, anchors, protective oxide) are not very critical and can be made large to allow for the reduced patterning resolution; **(2)** the protective oxide now resides in recessed trenches (Figure 3.13(b4)) and therefore will not potentially prevent bonding, resulting in less restrictions on design; **(3)** both gap-widening and footing are eliminated from the critical DRIE etch step because the etch is now done on a regular non-SOI wafer (Figure 3.13(b5)); **(4)** since the critical DRIE step is now done before IC fabrication (Figure 3.13(b5)), thermal oxide can still be used as DRIE etch mask even for a truly integrated run, eliminating the need to develop a high-aspect-ratio polymer mask process; **(5)** since the final DRIE release step is a rather shallow large-area etch involving no fine features (Figure 3.13(b8)), standard resist can be used as etch mask, eliminating the need to use high-aspect-ratio polymer as a post-IC etch mask; **(6)** since the final DRIE release step is a rather shallow large-area etch (Figure 3.13(b8)), RIE lag will not be significant, thus minimizing the potential damage by footing; **(7)** however, if RIE lag is significant in the critical DRIE etch (Figure 3.13(b5)), then different parts of a sensor will take different amount of time to release in the final DRIE release step (Figure 3.13(b8)). Essentially, any RIE lag in the critical DRIE step will still reappear in the final DRIE release step, and the potential footing effect will resurface. For this reason, a common gap width mask is still recommended for the critical DRIE etch step (Figure 3.13(b5)). In a sense, DRIE footing is impossible to eliminate completely; **(8)** the sidewalls of the mechanical structures can now be doped by diffusion right after the critical DRIE step (Figure 3.13(b5)). Highly conductive electrodes can thus be formed; **(9)** the end point in the final DRIE release step can now be easily detected by visual check of each and every die on the wafer. Previously, end point detection relies on test structures that fall off when released, which is less direct and less reliable. A surer way to detect end point allows better control of etch time and

eliminates any unnecessary over-etch that causes footing; **(10)** the contact hole mask (Mask#4) and resist cover mask (Mask#7) are no longer needed.

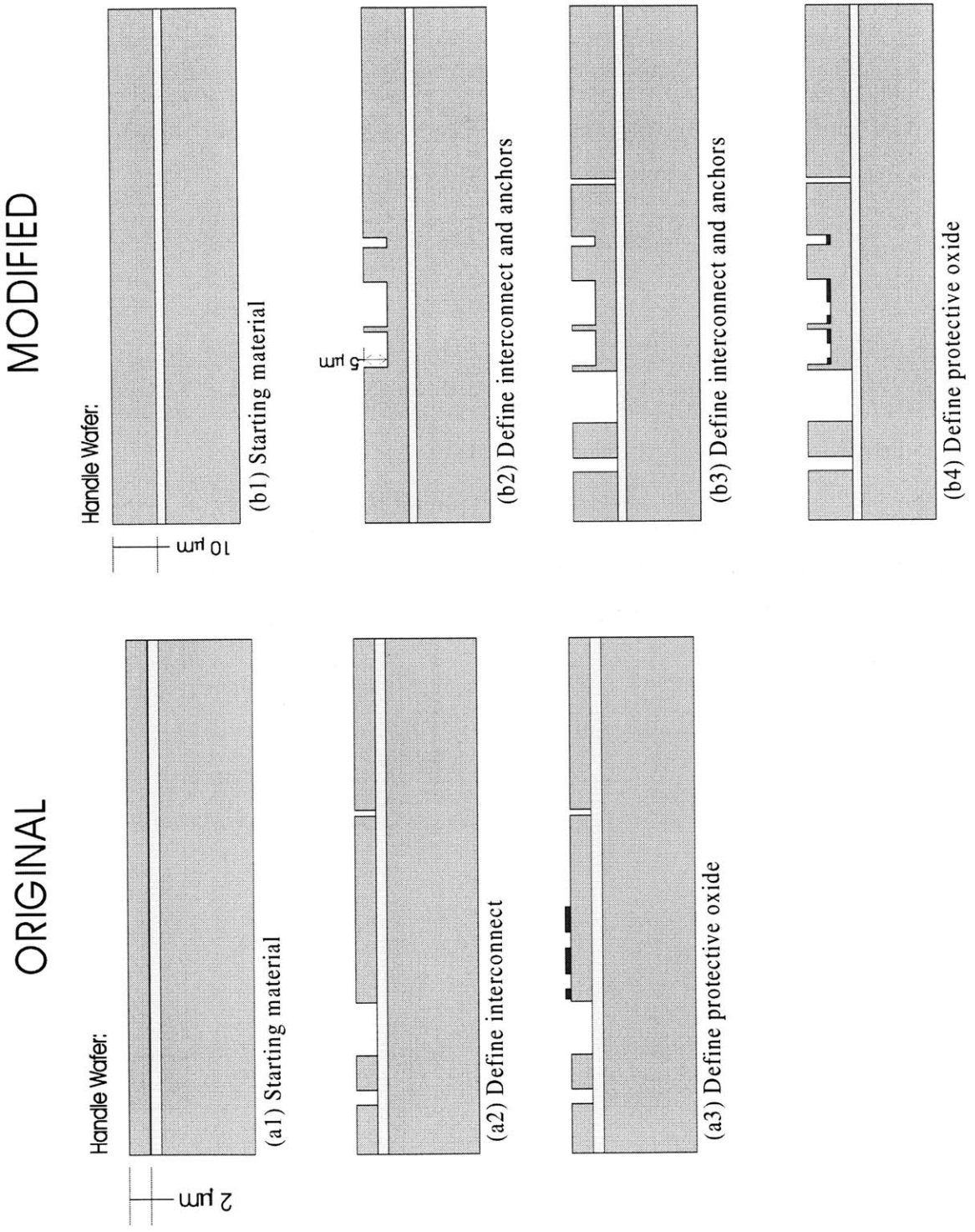


Figure 3.13 (a) Original process (b) Proposed modified process

Figure 3.13 (a) Original process (b) Proposed modified process (continued)

4. DEVICE DESIGN

Accelerometers and gyroscopes have been designed as a vehicle to demonstrate this process technology. The accelerometers are designed by Kei Ishihara. Design of the gyroscopes is provided by Ashwin Seshia of UC Berkeley and is subsequently modified by Kei Ishihara and the author to meet the requirements imposed by the process constraints. Sections 4.1 and 4.2 discuss the accelerometer design and the gyroscope design respectively.

4.1 ACCELEROMETER

Principle of Operation

A typical deflection-type accelerometer generally consists of a proof mass suspended by compliant beams anchored to a fixed frame and can usually be modeled as a second-order mass-spring-damper lumped-element model (Figure 4.1). The proof mass has a mass M, the suspension beams have an effective spring constant K, and there is a damping term B accounting for energy dissipation in the system typically associated with squeeze film damping in micromachined accelerometers. An external acceleration a_{in} displaces the proof mass relative to the support frame. This relative displacement can be used as a measure of the external acceleration and can be sensed, for instance, capacitively.

By Newton's second law, the relative displacement x and the external acceleration a_{in} are related by:

$$M\ddot{x} + B\dot{x} + Kx = Ma_{in} \qquad (4.1)$$

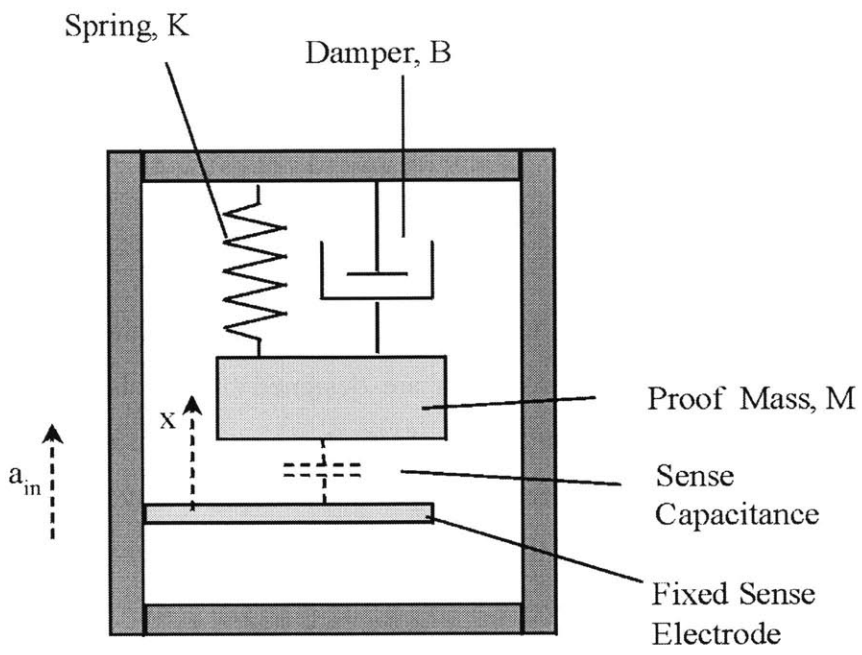


Figure 4.1 Lumped parameter model of an accelerometer

In the s-domain:

$$\frac{x(s)}{a_{in}(s)} = \frac{M}{Ms^2 + Bs + K} = \frac{1}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{4.2}$$

where

$$\omega_n = \sqrt{\frac{K}{M}} \tag{4.3}$$

$$\xi = \frac{B}{2\sqrt{KM}} \tag{4.4}$$

ω_n is the natural frequency and ξ is the damping ratio. For open loop designs, critical damping is usually preferred, for which $\xi \approx 0.7$.

The static sensitivity of the accelerometer can be defined as displacement per unit constant acceleration, and is easily seen from Equation 4.1 or 4.2 to be:

$$S = \frac{M}{K} \tag{4.5}$$

From (4.3) and (4.5):

$$S\omega_n^2 = 1 \tag{4.6}$$

Therefore the sensitivity and bandwidth of an accelerometer cannot be independently optimized. There is always a tradeoff between the two.

Device Structure

The 1-axis accelerometer design is shown in Figure 4.2(a) with the interconnection scheme highlighted. The thick silicon elements (device wafer) formed by DRIE are bonded to a patterned thin film silicon interconnect layer sitting on the insulating SiO_2 layer (handle wafer). These silicon islands not only serve as anchoring points for the thick silicon elements, but also provide a means for routing electrical signals between electrically distinct thick silicon elements. The interconnection scheme also enables the sensing electrodes to be placed inside the proof mass. Appendix B contains the mask layout of this 1-axis accelerometer.

The proof mass movement (and hence the external acceleration) is inferred by measuring the capacitance change between the proof mass and the sensing electrodes. Two complementary sets of electrodes are used to implement a differential sensing scheme. When the proof mass displaces in response to an acceleration, the capacitance between one set of electrodes and the proof mass goes up (C_1), while the capacitance between the other set of electrodes and the proof mass goes down (C_2). Their difference (C_{diff}) is to first order proportional to the input acceleration (a_{in}) for small proof mass displacements (Equation 4.7). The reason for putting two complementary electrodes in one slot instead of two separate slots is to fulfill the common gap width requirement as a way to reduce DRIE footing.

$$C_{diff} \equiv C_1 - C_2 = \frac{2C_s}{g}\frac{M}{K}a_{in} \tag{4.7}$$

where C_s is the nominal capacitance associated with one set of electrodes and g is the gap between the electrode and the proof mass, assuming a parallel plate capacitor configuration.

The 2-axis accelerometer design is shown in Figure 4.2(b). Two-axis sensing is realized by two sets of sensing electrodes which are orthogonal to each other. The possibility of placing electrodes inside the proof mass as enabled by the interconnect layer is particularly beneficial in this case, as it allows greater freedom in the design of tethers which are compliant in two directions.

The presence of small gaps typically associated with a parallel plate capacitor configuration results in squeeze-film damping. It is assumed that squeeze-film damping is the dominant dissipative mechanism in the present design. For the case where a compressible fluid with viscosity μ is squeezed between two parallel rectangle plates with length 2b and width 2a, separated by a gap g, the damping coefficient is given by [16]:

$$B = \frac{96(2a)^3(2b)\mu}{\pi^4 g^3}\sum_{n=1,3,5,\ldots}^{\infty}\frac{1}{n^4}\left\{1 - \frac{2a}{n\pi b}\tanh\left(\frac{n\pi b}{2a}\right)\right\} \tag{4.8}$$

For design purposes, the overall spring constant is calculated as various series and parallel combinations of single straight tether segments. The spring constant of a single straight tether segment with length l, width w and thickness t is given by:

$$K = \frac{Etw^3}{l^3} \tag{4.9}$$

where E is the modulus of elasticity. The thickness t is about 100μm in this case.

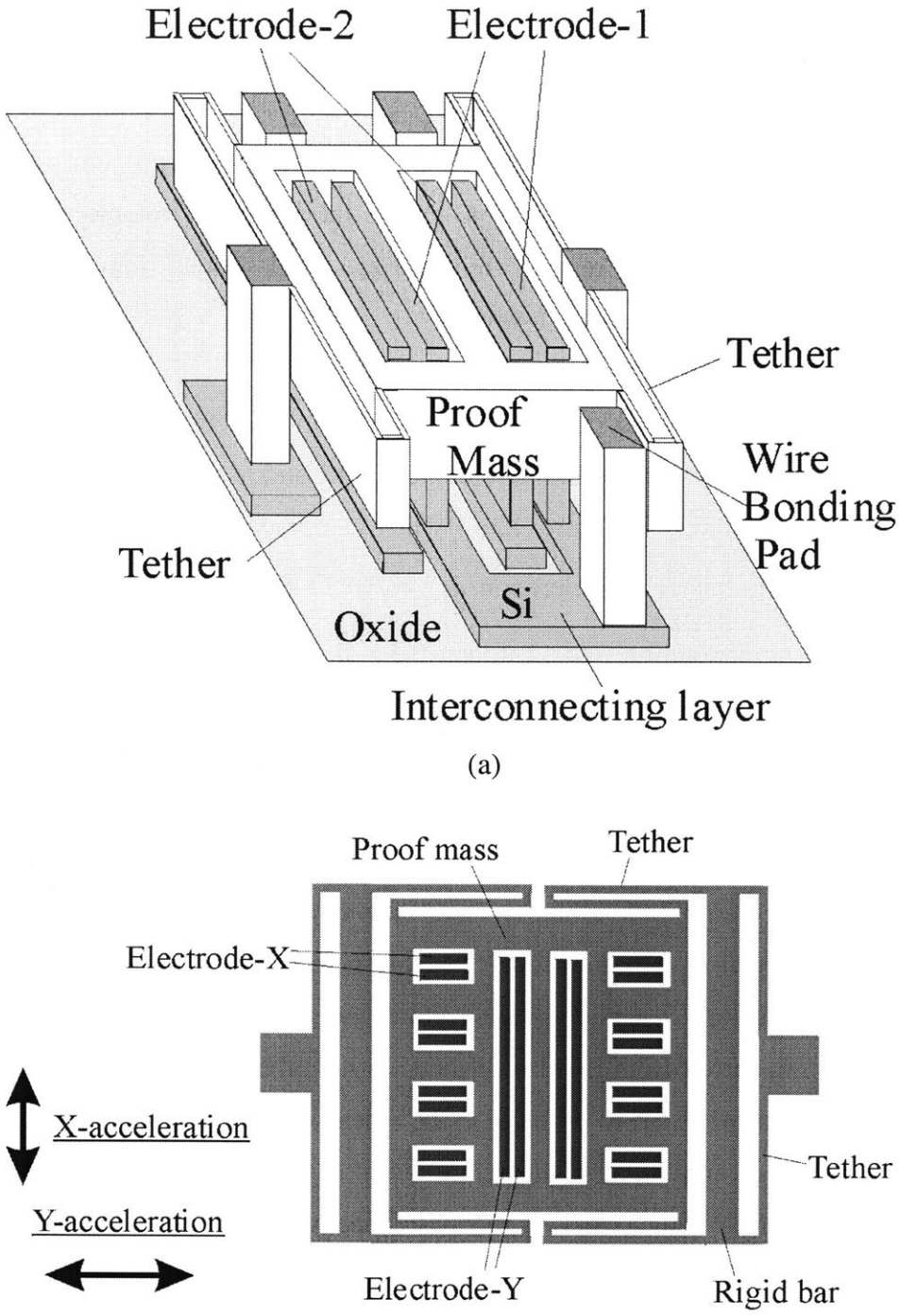


Figure 4.2 Device structure (a) 1-axis accelerometer (b) 2-axis accelerometer (Courtesy of Kei Ishihara)

4.2 GYROSCOPE

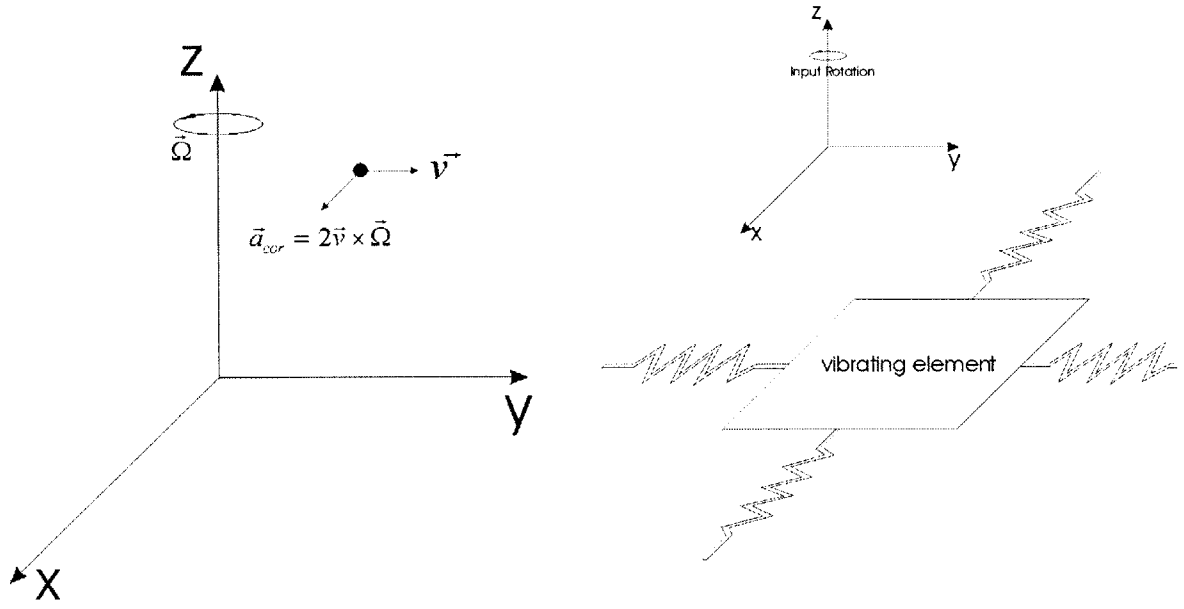
Theory of operation

Almost all reported micromachined gyroscopes are of the vibratory type, and use some vibrating mechanical element to sense rotation. Since they have no rotating parts that require bearings, they can be readily miniaturized and batch fabricated with micromachining techniques at potentially low cost.

All vibratory gyroscopes are based on the concept of Coriolis acceleration which is an apparent acceleration that arises in a rotating reference frame and is proportional to the rate of rotation. This is illustrated in Figure 4.3(a) where a particle moving in space with velocity $\vec{v}$ is perceived to have an acceleration $\vec{a}_{cor} = 2\vec{v} \times \vec{\Omega}$ by an observer attached to a reference frame rotating at rotation rate $\vec{\Omega}$ around the z-axis. The vibrating element in a vibratory gyroscope can be modeled as two harmonic oscillators (normal modes) coupled by Coriolis acceleration, as represented by the spring-mass system in Figure 4.3(b). All vibratory gyroscopes are based on the transfer of energy between the two vibration modes caused by Coriolis acceleration. To measure rotation rate, the vibrating element is driven into oscillation at a fixed amplitude along one axis (the driven mode). In the absence of rotation, the oscillation will remain aligned to this axis and all the energy of vibration will be stored in this driven mode. Under rotation, however, the Coriolis acceleration will cause energy to be transferred from the driven mode to the other mode (the sense mode) and the vibrating element will start to oscillate in the other axis. In the open-loop mode of operation, the sense mode amplitude is allowed to build up to steady state and provides a measure of rotation rate. This effect is the basic operating principle underlying all vibratory gyroscopes.

Device Structure

Figures 4.4 and 4.5 show the two gyroscope designs which are included in the process run. For both the single-mass and dual-mass designs, a suspended element is supported by tethers compliant in two orthogonal directions in the plane of the wafer, but stiff out of the plane because the device is relatively thick (~100μm). It is driven electrostatically into



(a) (b)

Figure 4.3 The Coriolis effect (a) Coriolis acceleration in a rotating frame (b) Normal mode model

resonance along the x-axis using comb drives (Equation 4.10). Any deflections in the y-axis that result from Coriolis acceleration are detected differentially in the sense mode using interdigitated comb fingers (Equation 4.11).

$$x(t) = X_o \sin \omega_x t \tag{4.10}$$

$$\ddot{y}_{cor} = 2 \cdot \Omega_Z(t) \cdot \dot{x}(t) = 2 \cdot \Omega_Z(t) \cdot X_o \cdot \omega_x \cdot \cos \omega_x t \tag{4.11}$$

The major difference between the two designs is that in the dual-mass gyroscope, the vibrating element consists of two masses coupled by a spring driven to oscillate in anti-phase. Differential measurement between the two masses results in the cancellation of common mode acceleration, and a doubling of Coriolis signal.

Two additional features can be seen in the gyroscope structures in Figures 4.4 and 4.5. They are for quadrature error nulling and sense-mode resonant frequency tuning [17].

Due to process variations or flaws, the vibrating element will not oscillate exactly parallel to the x-axis. This implies that some small fraction, ε, of the oscillation lies along the y-axis (Equation 4.12), leading to an acceleration term in the same axis as the Coriolis acceleration. This acceleration term due to off-axis oscillation is referred to as quadrature error and can be quite large (Equation 4.13). Since the quadrature error varies linearly with position, it can be cancelled by applying a balancing force proportional to position using electrodes designed for quadrature error nulling.

$$y_{quad} = -\varepsilon \cdot x(t) \tag{4.12}$$

$$\ddot{y}_{quad} = \varepsilon \cdot X_o \cdot \omega_x^2 \cdot \sin \omega_x t \tag{4.13}$$

Ideally, the sense mode resonant frequency should match the drive mode oscillating frequency to obtain a gain of Q in sensitivity, where Q is the quality factor of resonance. However, the open-loop bandwidth of the sensor is then limited to $\omega_x/2Q$ which may become too small for practical applications. Consequently, some gyroscopes are operated with a slight mismatch in resonant frequency. Tuning of the sense mode resonant frequency to the desired value is accomplished by applying a voltage between the vibrating element and the frequency tuning electrodes. The resulting attractive force can be captured as a negative electrostatic spring constant (k_e) which reduces the sense-mode resonant frequency (Equation 4.14).

$$\omega_y = \sqrt{\frac{k_y + k_e}{M}} \qquad (k_e < 0) \tag{4.14}$$

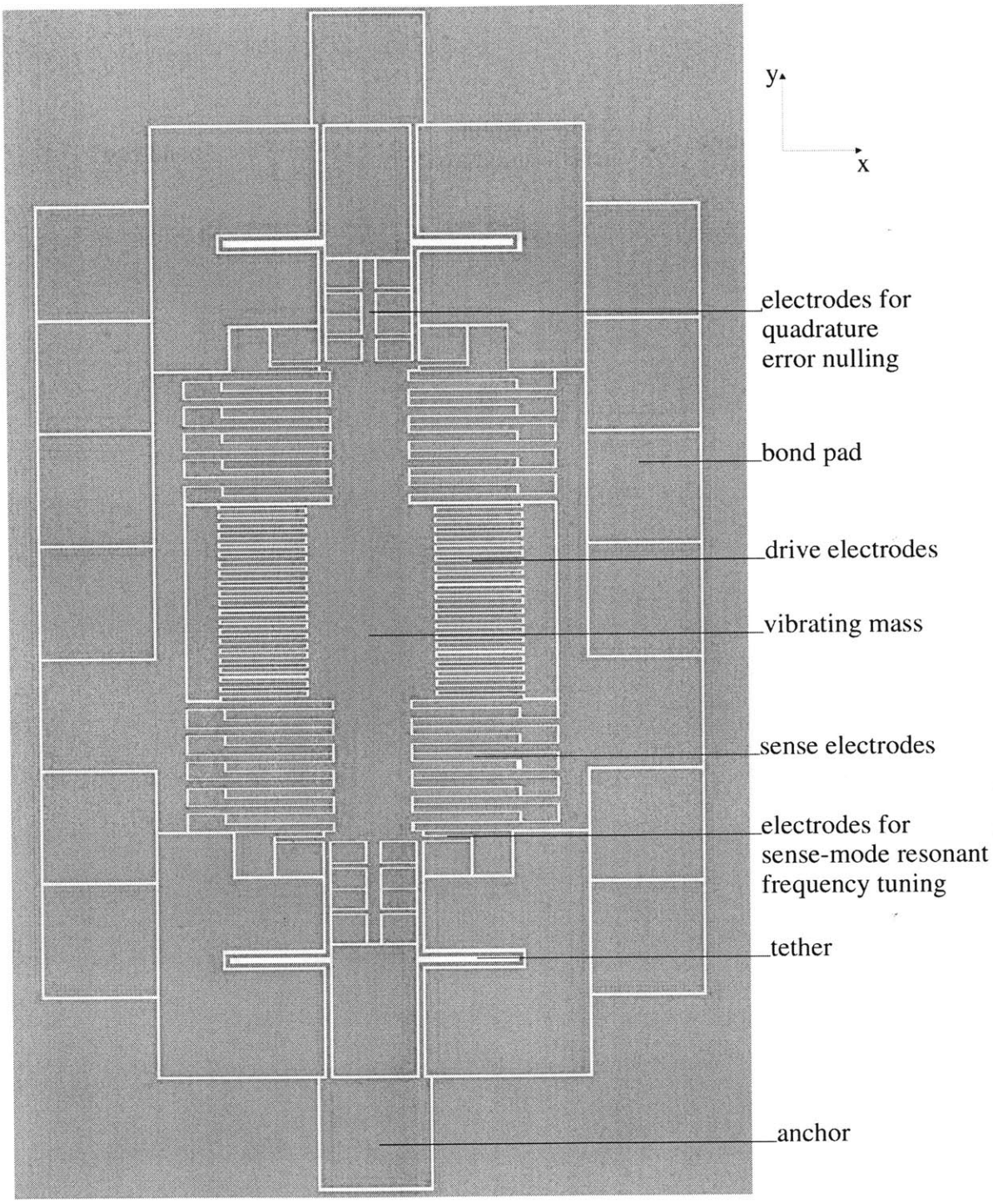


Figure 4.4 Device structure of single-mass gyroscope

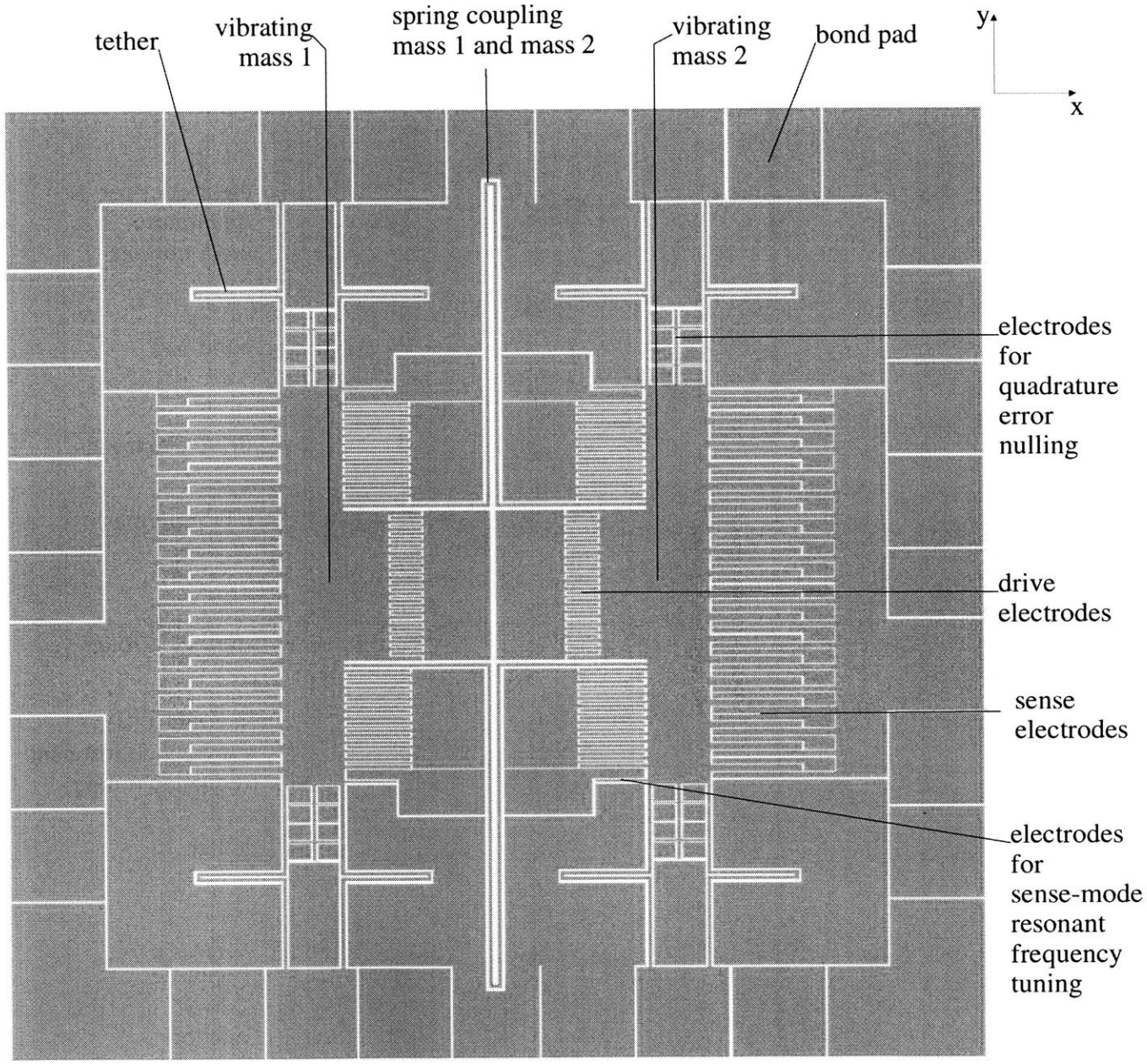


Figure 4.5 Device structure of dual-mass gyroscope

5. DEVICE CHARACTERIZATION

The accelerometers and gyroscopes described in the preceding chapter have been successfully fabricated (Figure 5.1), thus validating this process technology. This chapter gives the device characterization results. Only results for the accelerometers are given. The gyroscopes have been sent back to UC Berkeley for testing and will not be discussed here. Sections 5.1 and 5.2 give the characterization results for the accelerometers as obtained by the shaker test and the Computer Microvision [18,19] respectively. Section 5.3 discusses the results obtained by the two methods.

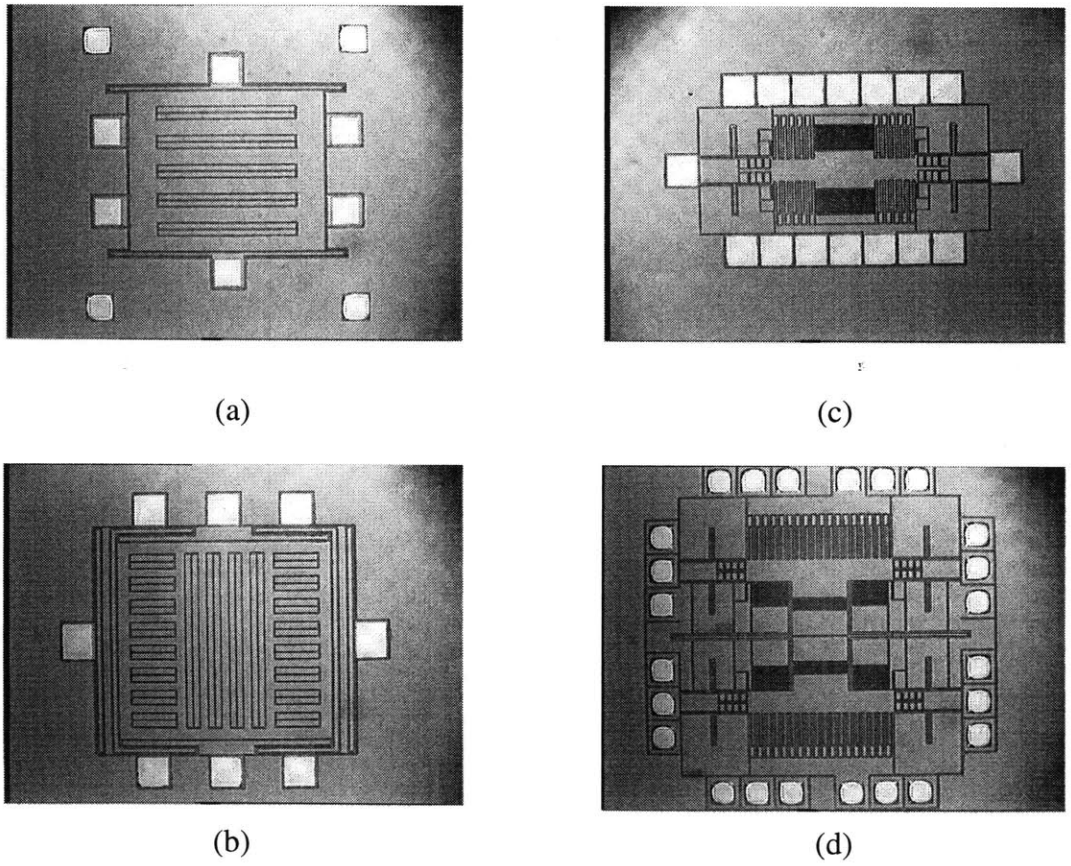


Figure 5.1 Fabricated devices (a) 1-axis accelerometer (b) 2-axis accelerometer (c) Single-mass gyroscope (d) Dual-mass gyroscope

5.1 SHAKER TEST

The dynamic response of the accelerometers is studied by measuring their differential capacitance change when subjected to known accelerations in a range of frequencies. The acceleration input is provided by an electrodynamic shaker which is designed to give a sinusoidal motion with variable amplitude and frequency. The test setup is shown in Figure 5.2. The shaker used is a Ling Dynamic Systems V456 driven by a Ling Dynamic Systems PA1000 power amplifier. The amplitude and frequency of the shaker motion is varied by modulating the input to the power amplifier using a function generator. The accelerometer under test and a reference accelerometer are attached to the shaker side by side. The capacitance change of the accelerometer under test is measured differentially by an off-chip capacitance detection circuit. The reference accelerometer is a B&K 4379 Delta Shear piezoelectric accelerometer and its output is amplified by a B&K 2651 charge amplifier. Finally the outputs of the capacitance detection circuit and the charge amplifier go to an oscilloscope.

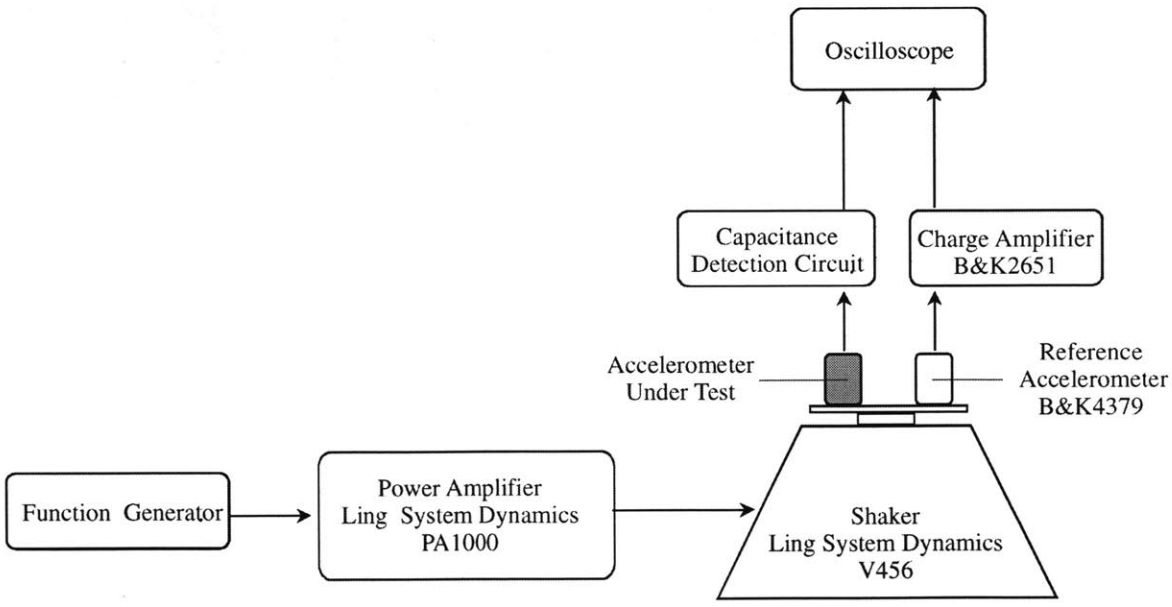


Figure 5.2 Shaker test setup

The capacitance detection circuit is shown in Figure 5.3. It converts the differential capacitance between two complementary capacitors in the accelerometer, which is proportional to the input acceleration, to a voltage output. A 1V 50kHz voltage (V_{in}) is applied to each of the two complementary capacitors, producing in each a current (I_1, I_2) proportional to the instantaneous capacitance (C_1, C_2). The two currents are then converted to voltages (V_1, V_2) by the current-to-voltage converters. Finally, the difference between the two voltages (V_2-V_1) is amplified by a difference amplifier to produce an ac output voltage (V_{out}) whose amplitude is modulated by the differential capacitance (C_2-C_1) (Equation 5.1).

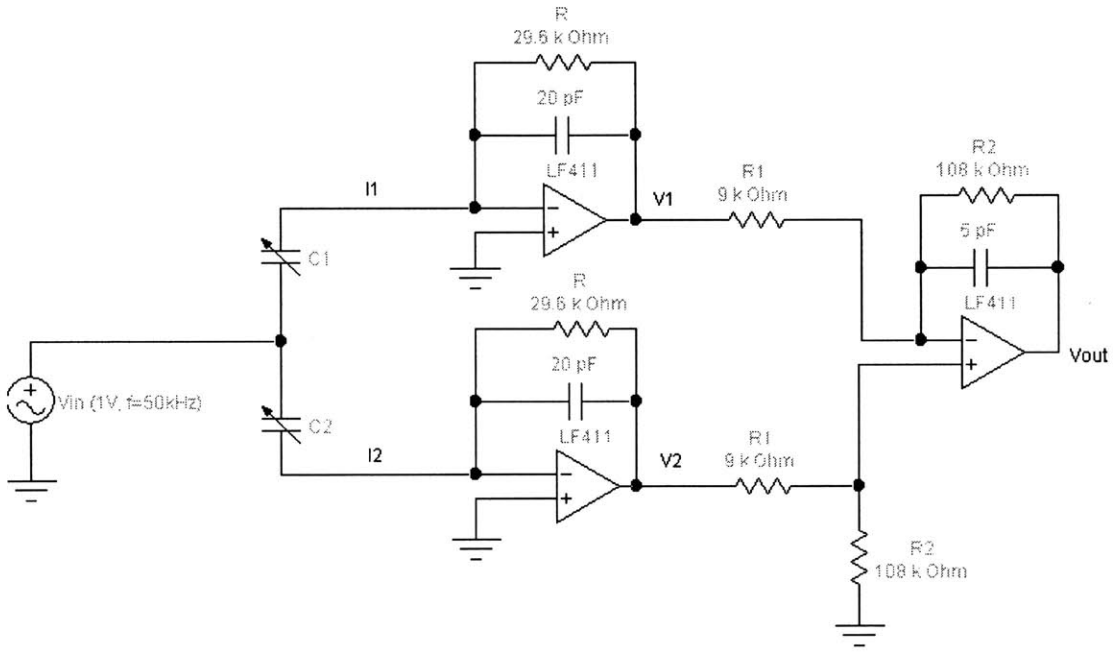
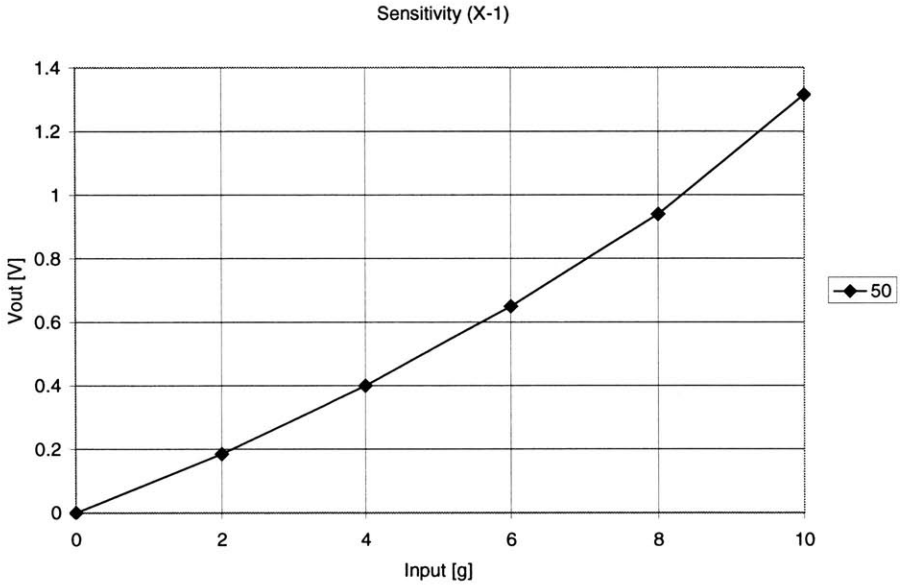


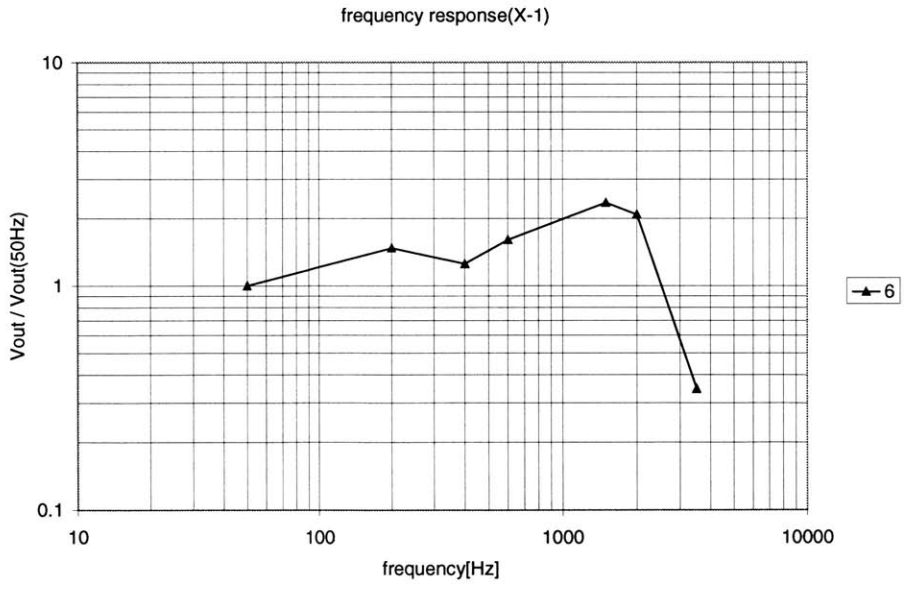
Figure 5.3 Capacitance detection circuit

$$\left|V_{out}\right| = 2\pi f R \left|V_{in}\right| \frac{R_2}{R_1}\left(C_2 - C_1\right) \qquad (5.1)$$

Using the above-mentioned setup, the sensitivity and frequency response of the accelerometers can be obtained. Figure 5.4 shows the results of the 1-axis accelerometer. Figures 5.5 and 5.6 show the results of the 2-axis accelerometer when driven in the x- and y-axis respectively.

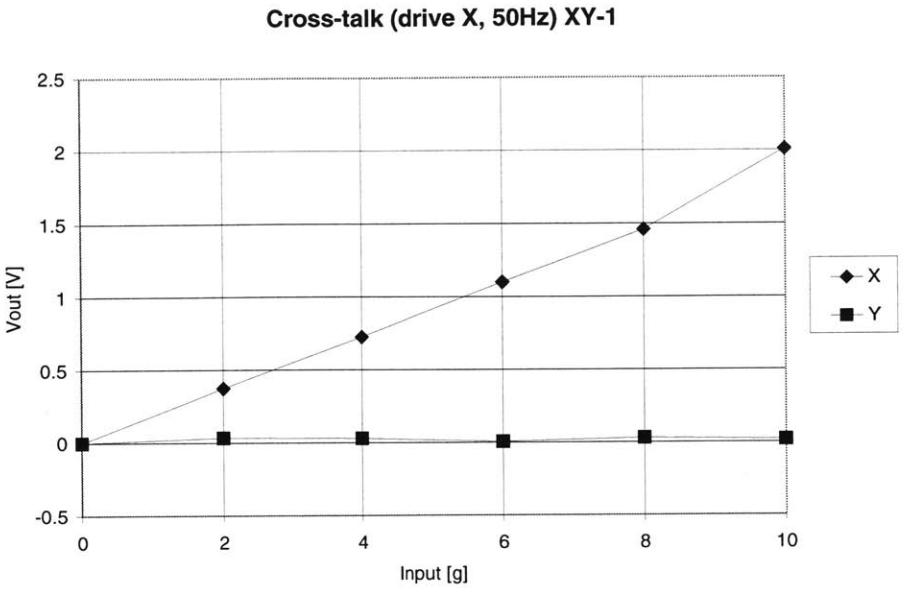


(a)

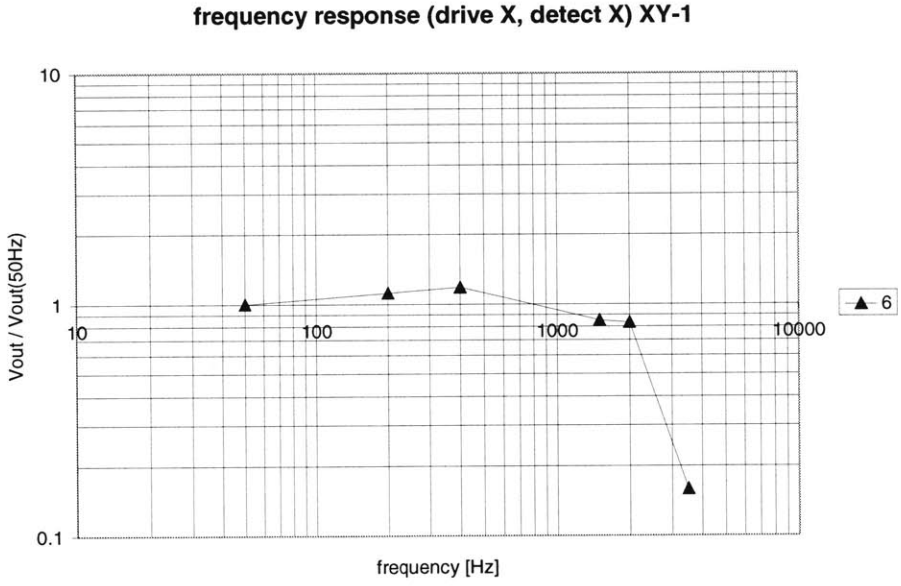


(b)

Figure 5.4 Shaker test results of 1-axis accelerometer (a) sensitivity (at 50 Hz) (b) frequency response (normalized with respect to 50 Hz)

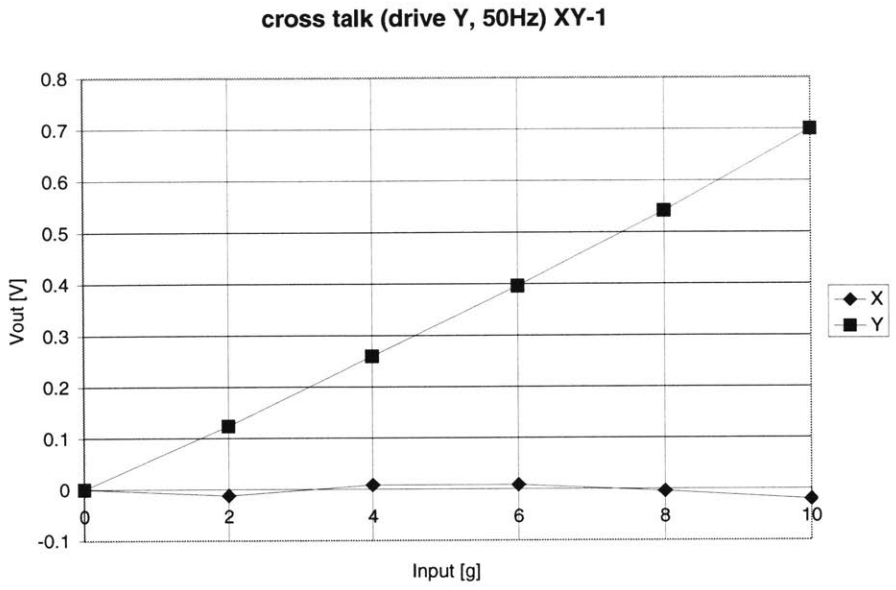


(a)

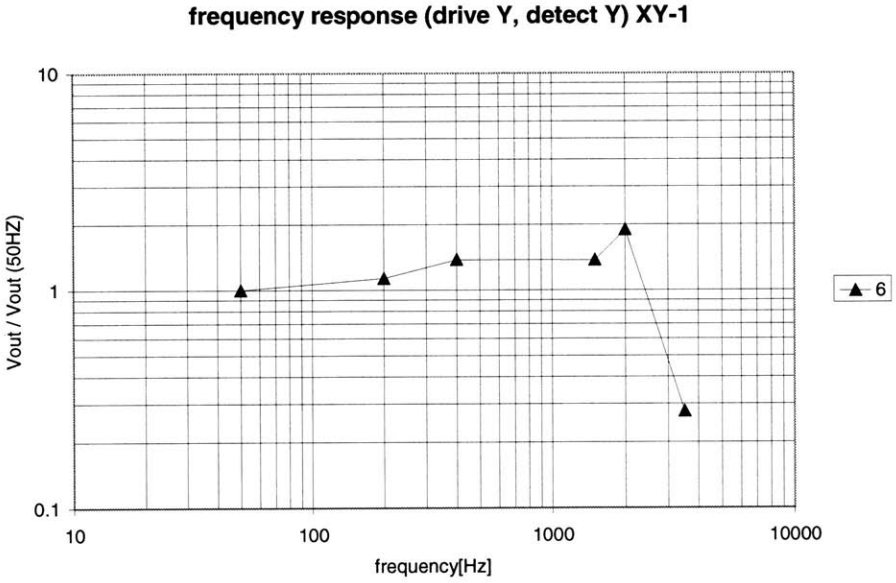


(b)

Figure 5.5 Shaker test results of 2-axis accelerometer with input acceleration along x-axis (a) sensitivity (at 50 Hz) (b) frequency response (normalized with respect to 50 Hz)



(a)



(b)

Figure 5.6 Shaker test results of 2-axis accelerometer with input acceleration along y-axis (a) sensitivity (at 50 Hz) (b) frequency response (normalized with respect to 50 Hz)

5.2 COMPUTER MICROVISION TEST

In addition to the shaker test, the dynamic response of the accelerometers is obtained by another technique called Computer Microvision developed by Prof. Dennis Freeman's group at MIT [18,19]. It is a tool for in situ measurement of micromechanical motions based on the combination of light microscopy, video imaging, and machine vision (Figure 5.7). The device is viewed with a microscope and imaged with a CCD camera while being driven by a sinusoidal voltage. A LED is strobed once per stimulus period at a chosen phase to yield a snapshot of the device position at the specified phase. The strobe is repeated at several stimulus phases to determine the periodic motion of the device using computer vision algorithms. The whole process is then repeated at other stimulus frequencies to yield frequency response of the device.

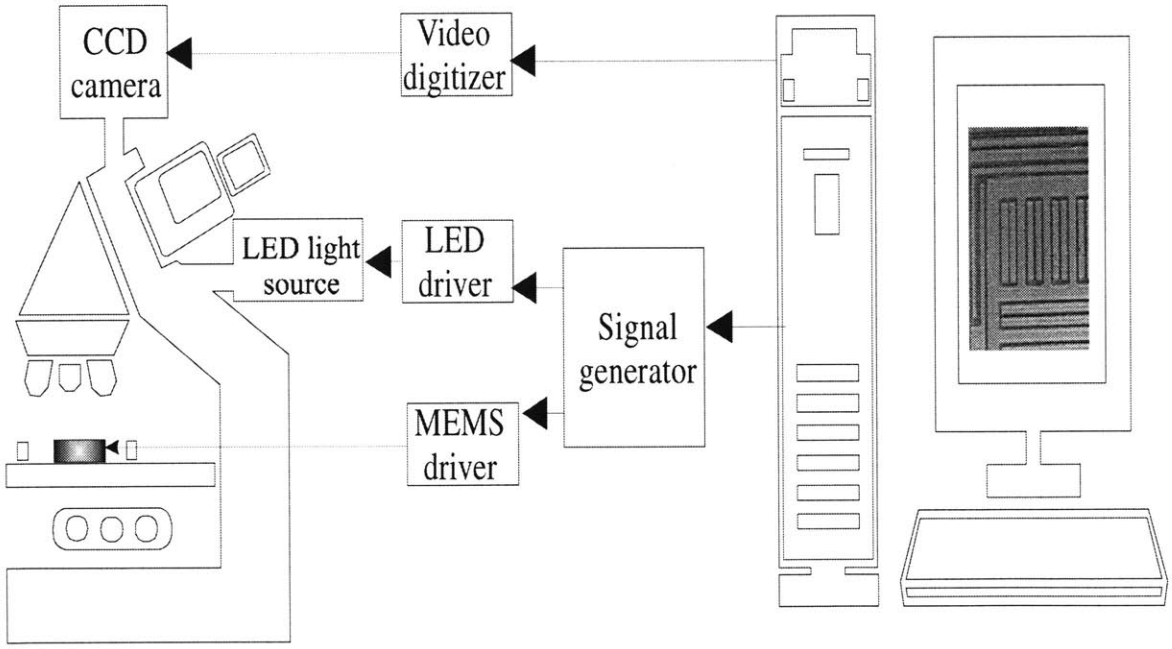
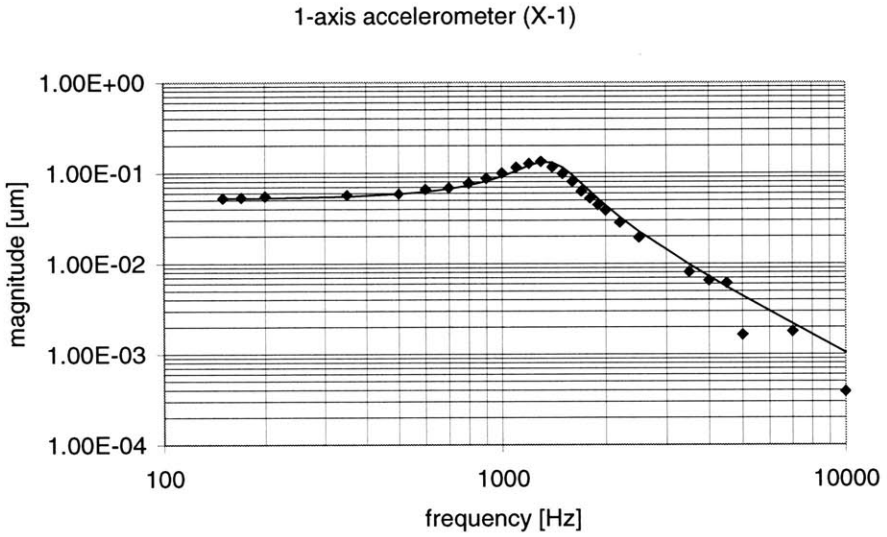
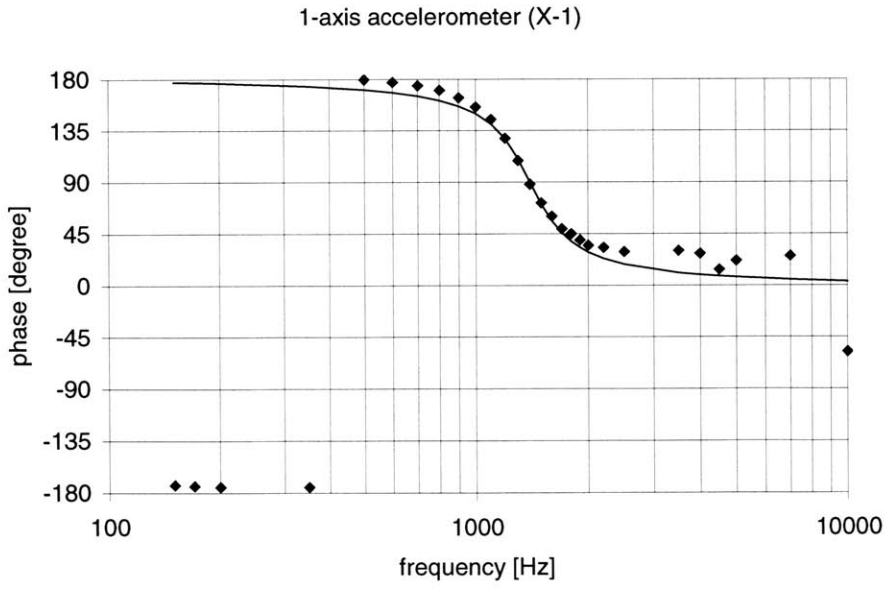


Figure 5.7 Computer Microvision system

Both magnitude and phase responses of the accelerometers are obtained using Computer Microvision with a driving signal of 4V peak-to-peak superimposed on a 4V dc bias. Figure 5.8 shows the results of the 1-axis accelerometer. Figures 5.9 and 5.10 show the results of the 2-axis accelerometer when driven in the x- and y-axis respectively.

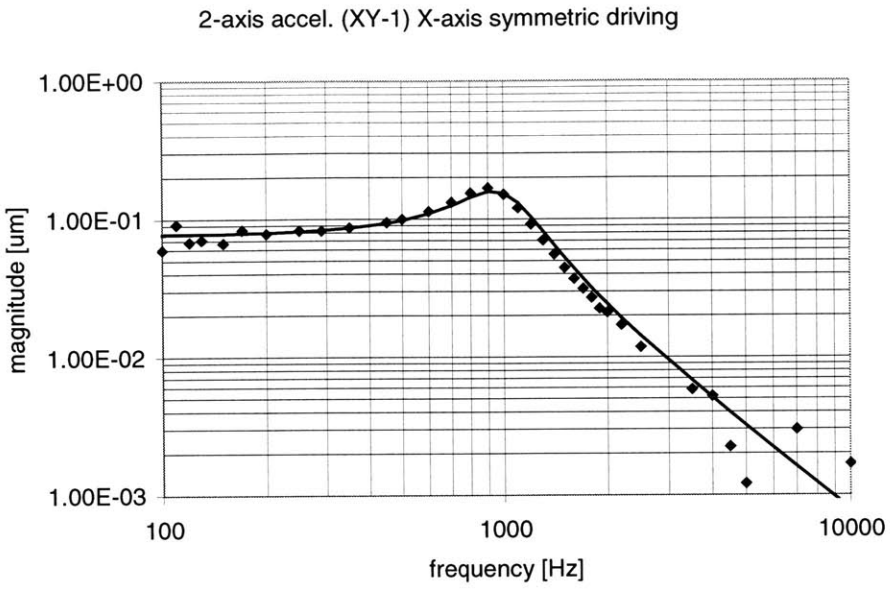


(a)

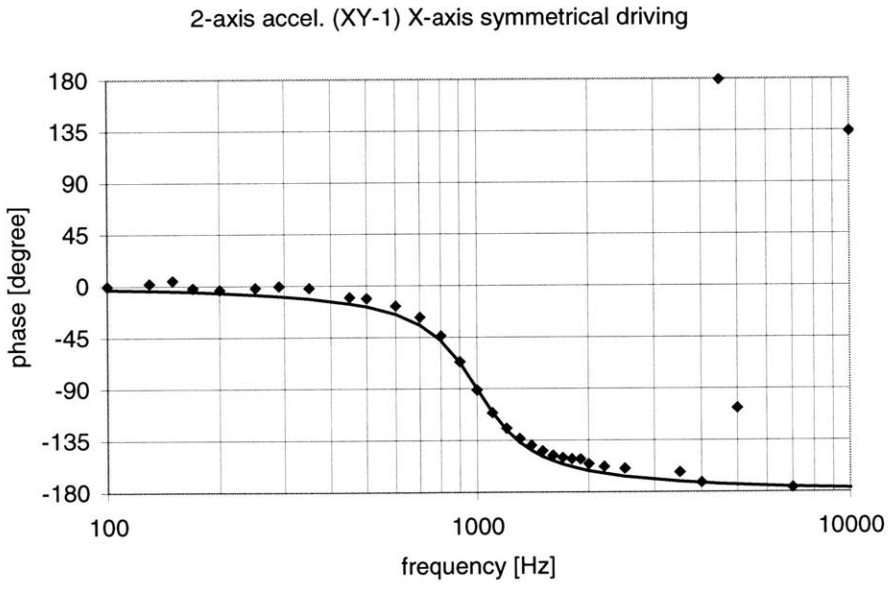


(b)

Figure 5.8 Microvision results of 1-axis accelerometer (a) magnitude plot (b) phase plot (data fitted to a second order system)

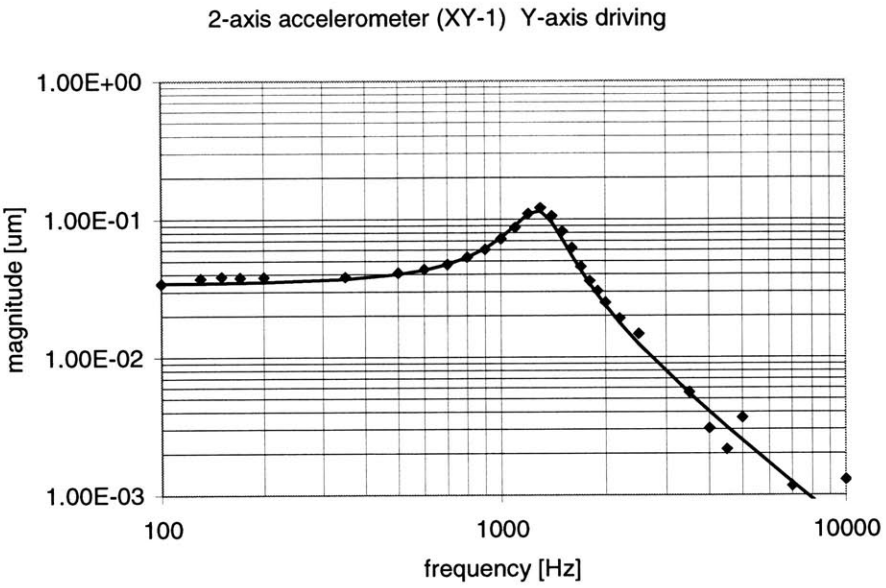


(a)

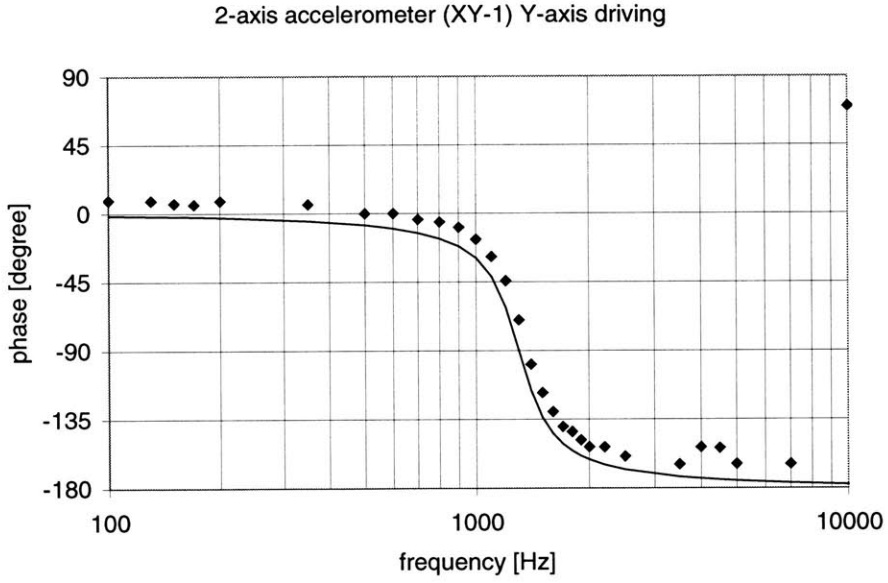


(b)

Figure 5.9 Microvision results of 2-axis accelerometer when driven electrostatically in the x-direction (a) magnitude plot (b) phase plot (data fitted to a second order system)



(a)



(b)

Figure 5.10 Microvision results of 2-axis accelerometer when driven electrostatically in the y-direction (a) magnitude plot (b) phase plot (data fitted to a second order system)

5.3 Discussion of Results

Table 5.1 lists the results obtained from the shaker and Microvision tests alongside the design values. Two observations can be immediately made. First, for the shaker test, the measured x- and y-axis sensitivities of the 2-axis accelerometer differ considerably from each other, despite the fact that they are designed to be the same. Second, for the Microvision test, the measured resonant frequencies deviate substantially from the design values. The measured x- and y-axis displacements of the 2-axis accelerometer also differ considerably from each other, even though they are supposed to be the same by design.

			Shaker	Design	Microvision
1-axis accelerometer		resonant frequency	~2 kHz	2 kHz	1.4 kHz
		sensitivity	53 fF/g	106 fF/g	-
		displacement amplitude at given drive	-	0.13 μm	0.058 μm
		damping ratio	~0.3	0.5	0.2
2-axis accelerometer	x-axis	resonant frequency	~2 kHz	2 kHz	1 kHz
		sensitivity	82 fF/g	99 fF/g	-
		displacement amplitude at given drive	-	0.13 μm	0.078 μm
		damping ratio	~0.6	0.5	0.25
	y-axis	resonant frequency	~2 kHz	2 kHz	1.3 kHz
		sensitivity	32 fF/g	99 fF/g	-
		displacement amplitude at given drive	-	0.13 μm	0.034 μm
		damping ratio	~0.3	0.5	0.15

Table 5.1 Measured accelerometer characteristics versus the design values

The results shown in Sections 5.1 and 5.2 suggest that the Microvision measures the frequency response more reliably than the shaker test. The shaker test results are not very reliable in general because the output signal from the capacitance detection circuit is quite noisy. Furthermore, the possibility of exciting vibration modes associated with the fixtures and the shaker system compromises the accuracy of the measured frequency response, and there is also some difficulty in locating the resonant frequency in the frequency response curve due to the limited number of data points collected. By comparison, the Microvision results are more reliable because Microvision measures the displacement in a more direct way with nanometer resolution instead of inferring the displacement from off-chip capacitance measurement which is prone to interference and parasitic effects. Since the device is driven electrostatically, it is free from errors introduced by the fixture and shaker dynamics. Also, more data points are taken in the frequency range of interest. As can be seen from Figures 5.8-5.10, the data fit quite well with the frequency response of a second order system. The resonant frequency extracted from the measured frequency response should be reliable since the shape (as opposed to the values) of the frequency response is to first order unaffected by the various uncertainties in the measurement process.

Now, based on the premise that the resonant frequency inferred from the Microvision test is reliable, it can be concluded that the resonant frequencies of the fabricated devices are significantly lower than the design values. Assuming the actual mass is not substantially different from the design value, this translates into a lowering of the actual tether stiffness from the design for both the 1-axis and 2-axis accelerometers. In particular, for the 2-axis accelerometer, the x-axis tether as fabricated is less stiff than the y-axis tether, which is consistent with, and can potentially explain, the observation that both the measured sensitivity and displacement in the x-axis is larger than in the y-axis. There are two things to be explained: why the fabricated tether is less stiff than the design for both types of accelerometers, and why the fabricated tether in the x-axis is less stiff than that in the y-axis for the 2-axis accelerometer. The DRIE gap-widening effect is expected to reduce the tether width and hence the stiffness. The isotropic etch used to reduce gap-widening removes materials at the top of the tether and therefore also reduces the tether stiffness. Figure 5.11 is a SEM picture of a tether cross section, from which it is observed that the

bottom of the tether is significantly thinner than the top. This can also account for the reduced tether stiffness. However, it is uncertain at this point as to whether this tapering phenomenon is general or particular to that one die chosen for SEM. Further probing is needed.

Alternatively, it is possible that the expression used for tether stiffness (Equation 4.9) is inappropriate in the present situation. Assuming all those effects which reduce tether stiffness such as gap-widening, isotropic etch and tapering apply equally to both the x-axis and y-axis tethers, it is expected that the x-axis and y-axis tether stiffness should be lowered by a similar amount. The fact that they are not suggest that the expression may not capture the situation well in the first place. That expression assumes zero-slope boundary conditions at both ends of a tether segment. The validity of this assumption is not immediately obvious, and should be checked by finite element analysis.

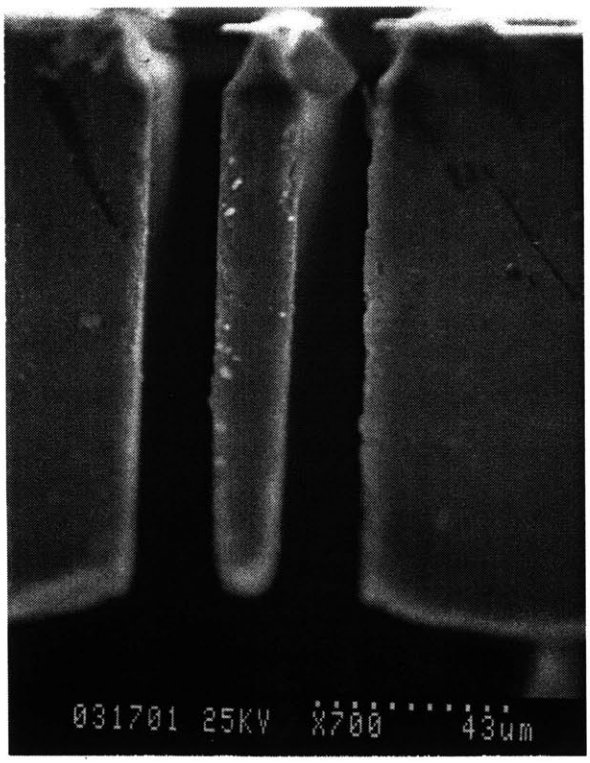


Figure 5.11 A SEM photo showing the tapered profile of a tether cross section

To make meaningful comparison, the design values have to be recalculated based on the resonant frequencies obtained from the Microvision test which, as discussed above, are believed to be reliable. Table 5.2 lists the measurement results against the recalculated design values. It is found that the gap size g has to be 6-8μm to give a good fit to the measured sensitivities and displacements, while the design nominal gap size is 3μm. A widening of this extent is unsupported by SEM taken of some test structures. This is actually quite implausible given that the two-step process described in Section 3.2 has already been used to minimize gap-widening. Therefore, it is believed that in addition to the actual gap being wider than design, other factors may be responsible for the reduced sensitivities and displacements. For example, the device wafer is not heavily doped for capacitive readout, and some deleterious effects may result. Furthermore, the Al-Si interface does not form good ohmic contact and actually shows some diode behavior due to the fact that the contact area is not doped. Some deleterious effects may arise accordingly. In particular, the actual voltage across the proof mass and the electrodes may be considerably smaller than the applied voltage if the voltage drop across the bad contacts is significant. To sum up, there is no conclusive explanation for the observed discrepancies at this point. Further analysis is needed.

			Shaker	Design		Microvision
1-axis accelerometer		resonant frequency	~2 kHz	g=6μm	1.4 kHz	1.4 kHz
		sensitivity	53 fF/g		52.3 fF/g	-
		displacement amplitude at given drive	-		0.056 μm	0.058 μm
2-axis accelerometer	x-axis	resonant frequency	~2 kHz	g=7μm	1 kHz	1 kHz
		sensitivity	82 fF/g		75.3 fF/g	-
		displacement amplitude at given drive	-		0.082 μm	0.078 μm
	y-axis	resonant frequency	~2 kHz	g=8μm	1.3 kHz	1.3 kHz
		sensitivity	32 fF/g		34.1 fF/g	-
		displacement amplitude at given drive	-		0.032 μm	0.034 μm

Table 5.2 Measured accelerometer characteristics versus the design values recalculated based on the Microvision resonant frequencies (with the gap size g chosen to give a good fit to the measured sensitivities and displacements)

6. CONCLUSION

6.1 CONTRIBUTION

The major contribution of this work is the development of a process technology for realizing integrated high-aspect-ratio inertial sensors utilizing aligned wafer bonding and DRIE. In particular, a new interconnection scheme using a lower interconnect layer is developed for electrical signal routing, which greatly augments the design space by providing an extra plane of freedom. DRIE gap-widening and footing effects are observed during process development. These effects are characterized and ways to minimize them found. The process technology is successfully demonstrated by the fabrication of working accelerometers and gyroscopes.

6.2 FUTURE WORK

For a real integrated run, thermal oxide cannot be used as the etch mask for the final DRIE etch because the high temperature thermal oxidation step is not IC compatible. An alternative mask material which is IC compatible and can survive the relatively long DRIE etch while giving high patterning resolution is needed. SU-8, being a high-aspect-ratio polymer mask material, is a potential candidate.

The chipping that is occasionally observed at the edge of the device wafers after thinning will potentially disturb the existing IC processing line at the foundry. Ways to eliminate chipping are to be examined.

Dicing is currently done manually. This reduces yield and is not suitable in a manufacturing process. A capping wafer, apart from serving its wafer-level packaging functions, will make diesawing a feasible dicing solution by keeping the water or slurry

during diesawing away from the sensor. Thermocompression gold bonding for realizing the capping wafer is currently under study. Also, more study on tether survivability upon diesawing is needed.

Inconsistencies found in the accelerometer characterization results remain to be resolved. More in-depth study of these inconsistencies will lead to a better understanding of the process technology itself.

Finally the proposed modified process can be tried out to test its feasibility and to see if any real advantages over the original process can be gained.

APPENDIX A

PROCESS TRAVELER

```
Process Traveler

Micromechanical Accelerometer and Gyroscope Process


Handle Wafer:
Starting Material: SOI-Wafer (backside polished) n type {1 0 0}

[ICL]
1  RCA

2  Phosphorus Doping
   tube A4
   recipe#310

3  Strip PSG

[TRL]
4  HMDS, Resist-coat, Pre-bake
   standard resist (OCG 825)
   (first coat front side for protection, then coat backside)

5  Pattern Si
   ksaligner2
   Mask#0, dark field jig

[ICL]
6  Dry Etch Si (0.5um etch)
   etcher-1
   recipe#10
   (etch alignment marks on the backside)

[TRL]
7  Ash Resist
   asher

8  HMDS, Resist-coat, Pre-bake
   standard resist (OCG 825)
   (coat front side)

9  Pattern Si
   ksaligner2
   Mask#0, dark field jig
   (transfer alignment marks from backside to front side using IR)
```

```
[ICL]
10 Dry Etch Si (0.5um etch)
   etcher-1
   recipe#10
   (etch alignment marks on the front-side)

11 Ash Resist
   asher

[TRL]
12 HMDS, Resist-coat, Pre-bake
   standard resist (OCG 825)

13 Pattern Si
   ksaligner2
   Mask#1, clear field jig

[ICL]
14 Dry Etch Si (2.2um etch)
   etcher-1
   recipe#19

15 Ash Resist
   asher

16 RCA

17 Oxidation (0.5um)
   tubeB1
   recipe#G122
   (1000C Wet H20: 50min)

18 HMDS, Resist-coat, Pre-bake
   image reversal resist (AZ 5214E-IR)

[TRL]
19 Pattern Oxide
   ksaligner2
   Mask#2, clear field jig

[ICL]
20 Wet Etch Oxide (0.5um)
   BOE

21 Ash Resist
   asher


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

Device Wafer:
Starting Material: Double-side polished n type {1 0 0}

[TRL]
22 HMDS, Resist-coat, Pre-bake
   standard resist (OCG 825)
```

```
23 Pattern Si
   ksaligner2
   Mask#0, dark field jig

[ICL]
24 Dry Etch Si (0.5um etch)
   etcher-1
   recipe#10

25 Ash Resist
   asher

[TRL]
26 HMDS, Resist-coat, Pre-bake
   standard resist (OCG 825)

27 Pattern Si
   ksaligner2
   Mask#3, clear field jig

28 DRIE Etch Si (20um etch)
   recipe MIT37

[ICL]
29 Ash Resist
   asher


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

Device Wafer and Handle Wafer:

[TRL]
30 RCA

31 Wafer Bonding
   evaligner, evbonder
   program #fusion.abe
   electrode down 3000mbar in N2

[ICL]
32 Bonding Anneal (in N2)
   tube A3 in ICL
   recipe#225
   (1100C, 1 hour)

[outside] Lincoln Lab
33 Polishing
   Device wafer thinned to 120um thick

[5th floor group lab]
34 Wafer Cleanup

[TRL]
35 Post KOH Clean
   acid-hood
```

```
36 HMDS, Resist-coat, Pre-bake
   standard resist (OCG 825)

37 Pattern Si
   ksaligner2
   Mask#0, dark field jig
   (transfer alignment marks to top surface using IR)

[ICL]
38 Dry Etch Si (0.5um etch)
   etcher-1
   recipe #10

[TRL]
39 Ash Resist
   asher

40 Piranha, HF(50:1) Dip 20s
   acid-hood

41 Oxidation (1.5um)
   tubeA1
   (1100C, ~290 min Wet H2O)

42 HMDS, Resist-coat, Pre-bake
   standard resist (OCG 825)

43 Pattern Oxide (contact hole)
   ksaligner2
   Mask#6, clear field jig

44 BOE etch
   acid-hood

45 Ash Resist
   asher

46 Piranha Clean
   acid-hood

[ICL]
47 E-beam Al (1um)
   10A/s

[TRL]
48 HMDS, Resist-coat, Pre-bake
   image reversal resist (AZ 5214E-IR)

49 Pattern Al
   ksaligner2
   Mask#4, clear field jig

50 PAN Wet Etch
   acid-hood

51 Ash Resist
   asher
```

52 Nano-strip
   acid-hood

53 Al Sintering
   tube A3
   400C
   (1)N2(#1)   (60%) 50min
   (2)forming(N2/H2)#7   (40%) 30min
   (3)N2(#1)   (60%) 0min

54 HMDS, Resist-coat, Pre-bake
   standard resist (OCG 825)
   (double coating)

55 Pattern Oxide
   ksaligner2
   Mask#5, no jig

[ICL]
56 Oxide Etch
   AME5000
   recipe Isabels LTO

[TRL]
57 Ash Resist
   asher

58 HMDS, resist-coat, pre-bake
   thick resist(AZ4620)
   1750rpm 9S
   3000rpm 60s
   7000rpm 10s

59 Pattern Resist (for Al cover)
   STS mask
   exposure: 400s (Ksaligner2)
   develop AZ440 MIF 4min

60 DRIE Etch Si (100um etch)
   SF6_3: 2min
   MIT59: 70min
   37_SOI_4

61 Ash Resist
   asher

APPENDIX B

MASK LAYOUT OF 1-AXIS ACCELEROMETER

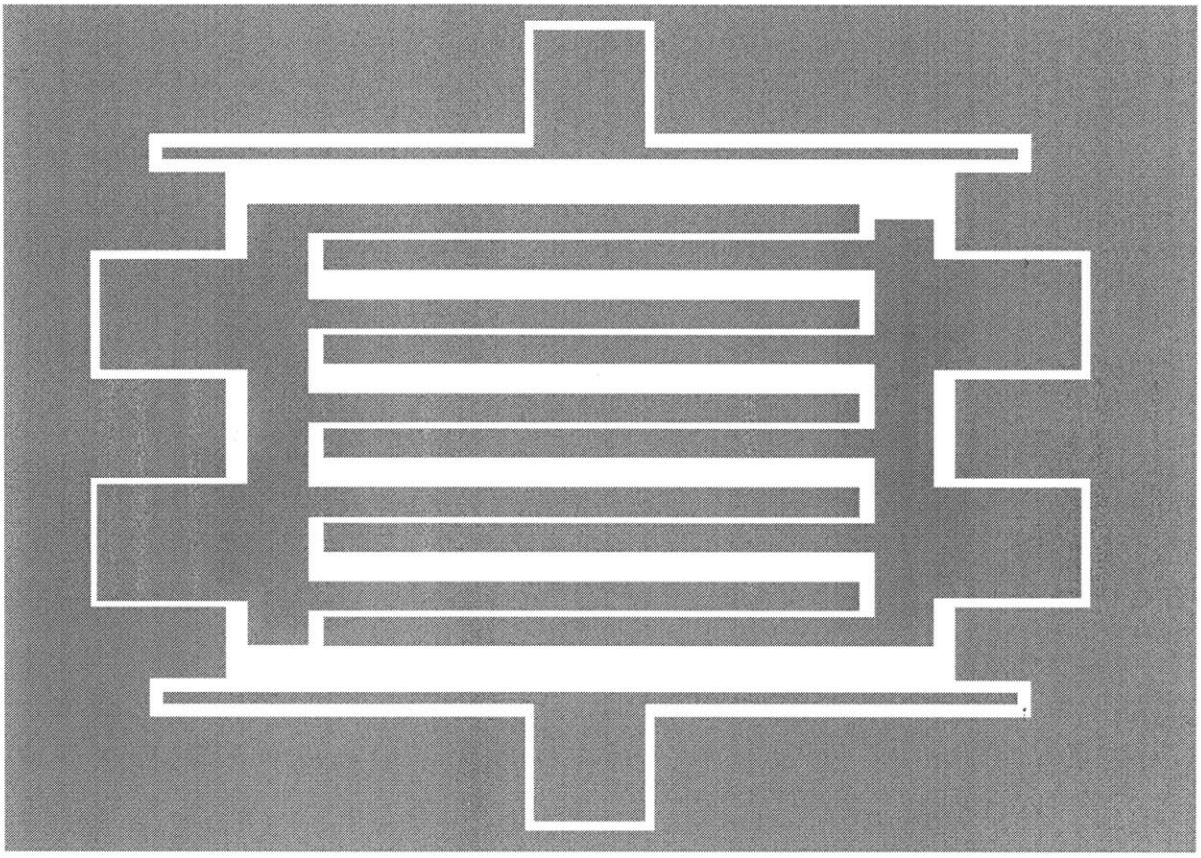


Figure B.1 Mask#1 SILICON

Figure B.2 Mask#2 OXIDE

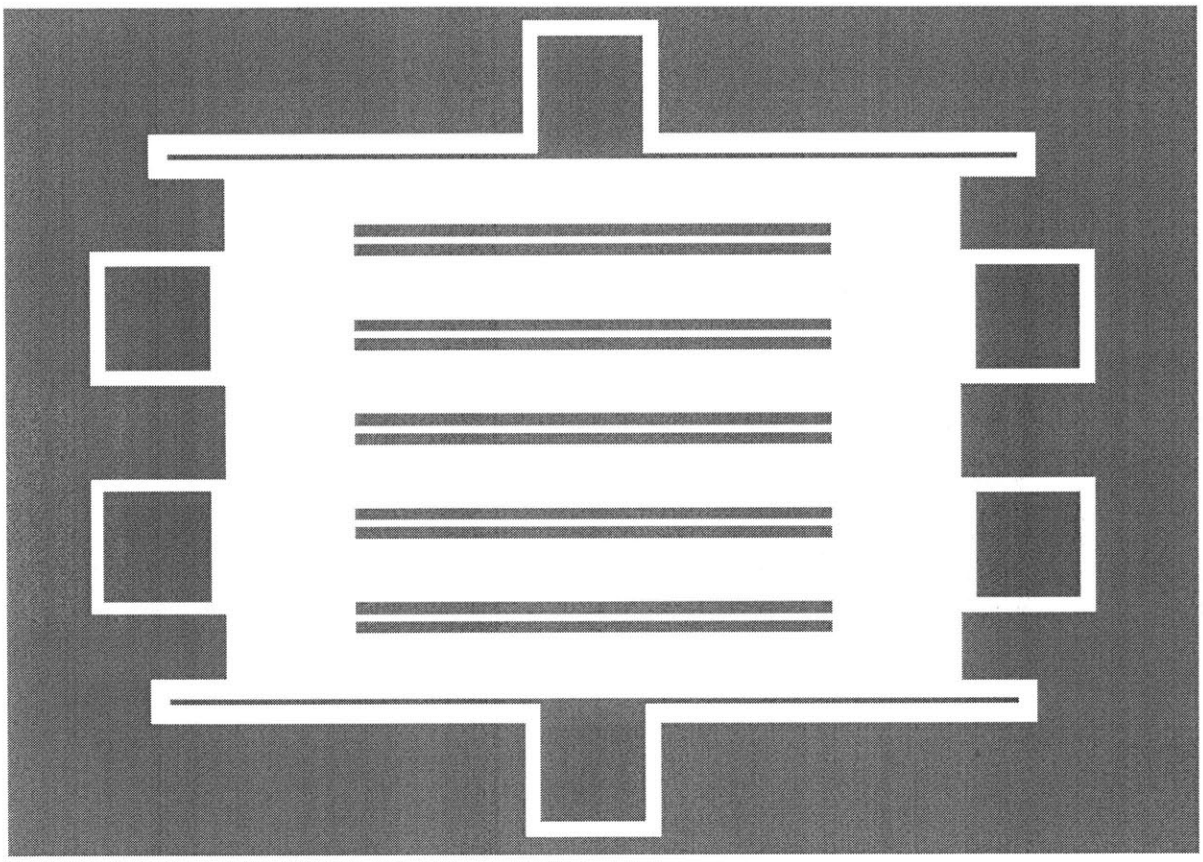


Figure B.3 Mask#3 CAVITY

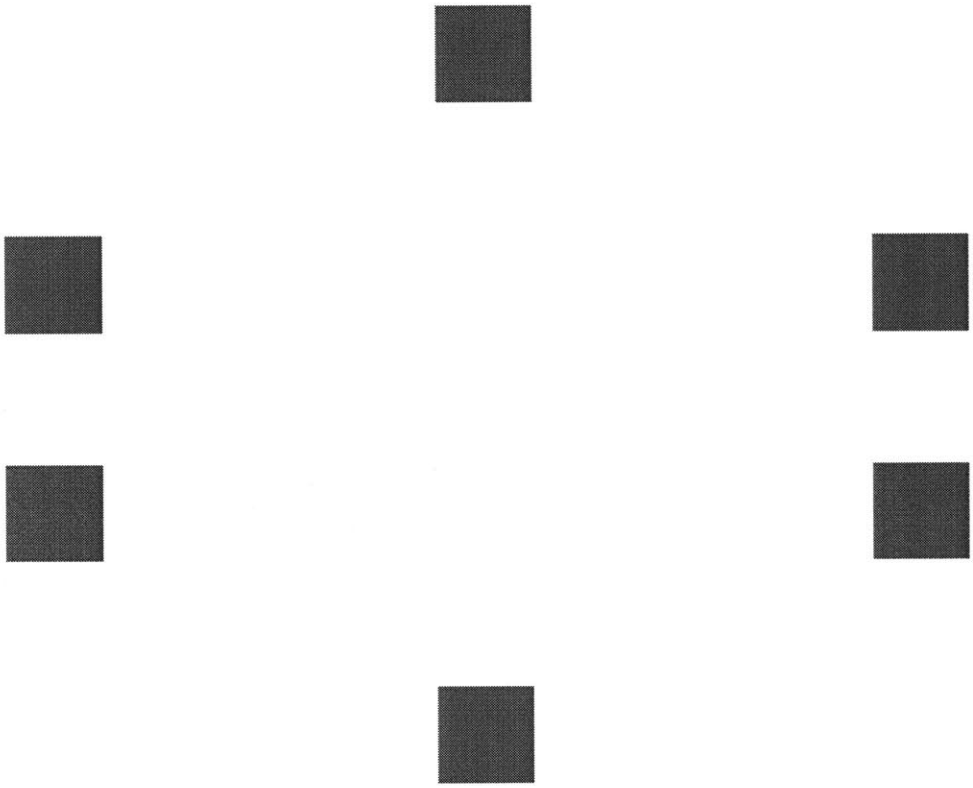


Figure B.4 Mask#4 CONTACT

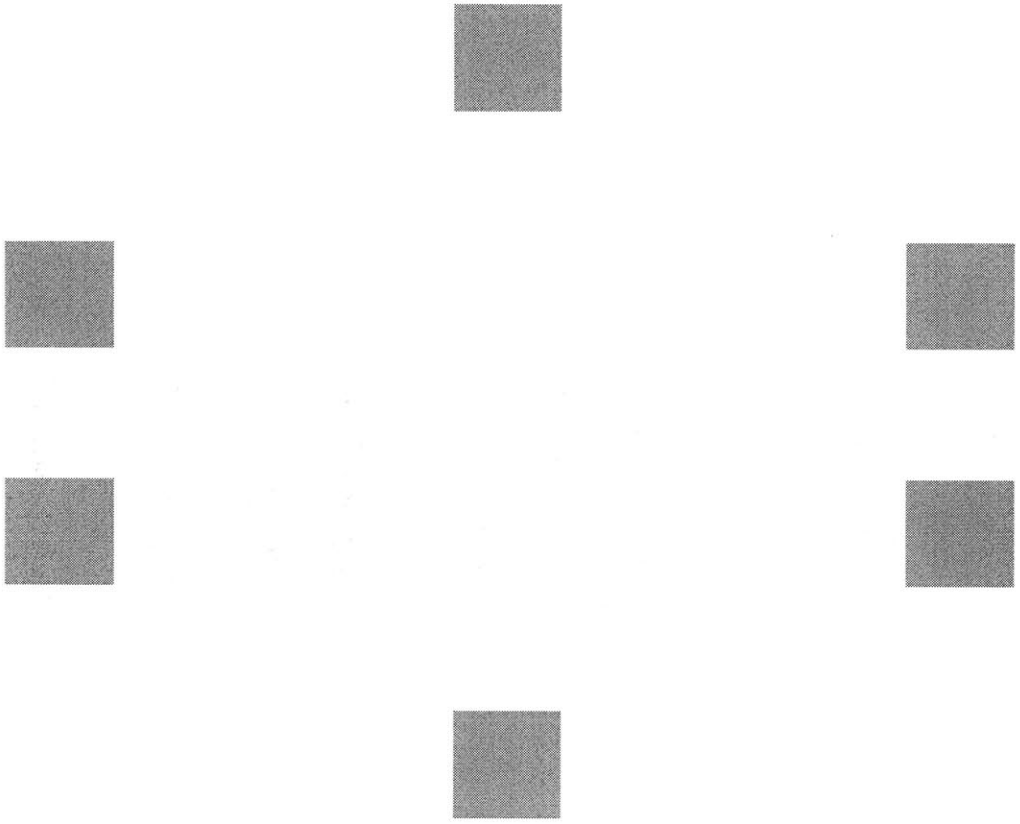


Figure B.5 Mask#5 METAL

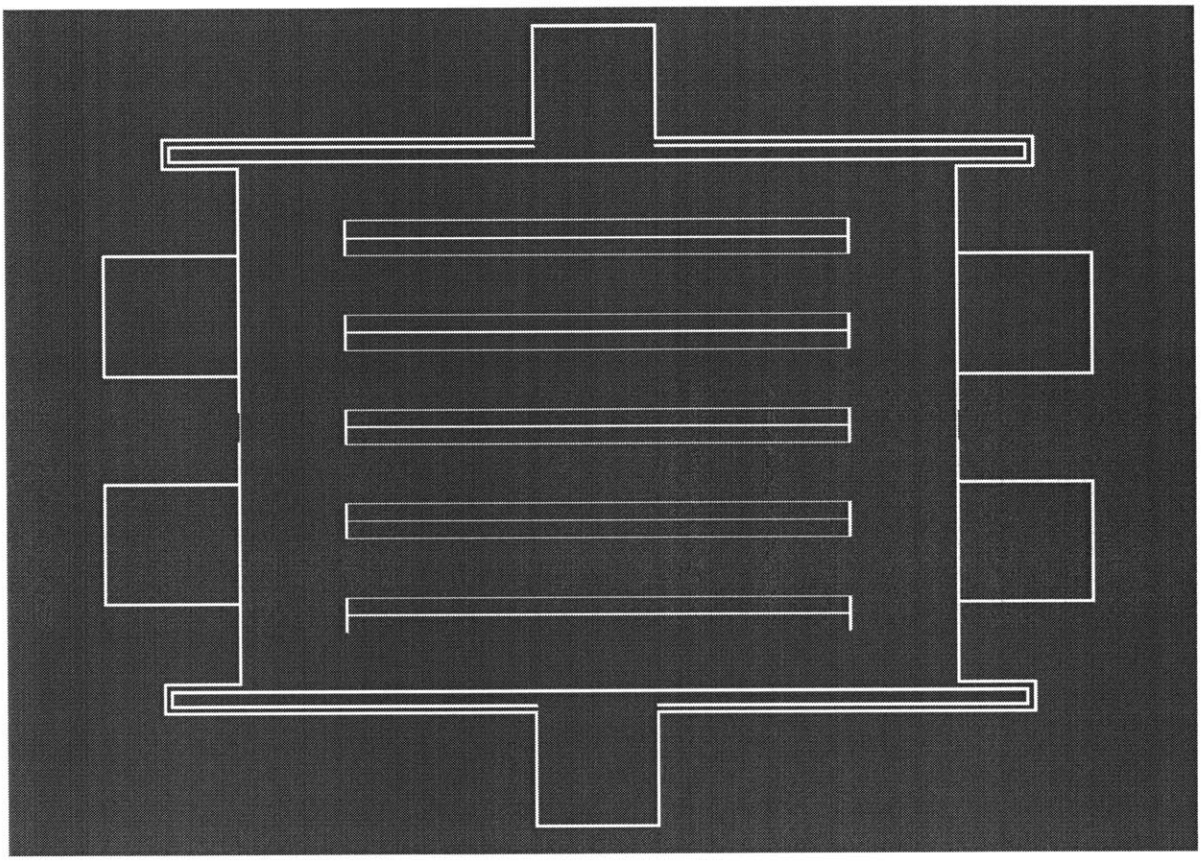


Figure B.6 Mask#6 DRIE

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