Study of Substrate Noise and Techniques for Minimization

by

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Abstract

This thesis presents a study of the effects of substrate noise on analog circuits in mixed-signal chips and techniques for minimizing these harmful effects on sensitive analog circuits. A microchip built in a 0.25um CMOS epitaxial process was designed, fabricated, and tested for this research.

Through the use of an on-chip sampling scope, the effect of substrate noise generated by digital inverters with coupling capacitors to the substrate on analog circuits was characterized. Substrate noise coupled into a representative analog circuit, a switched capacitor delta-sigma modulator primarily through the asymmetrical parasitics of the input sampling circuit. Furthermore, since some of the parasitics are nonlinear with input voltage, substrate noise couples into the analog circuits producing an input signal dependent component and an input signal independent component. The substrate noise, with decay time constants of a few nanoseconds and ringing frequencies of few hundred megahertz, can decrease analog circuit performance. In the case of a delta-sigma modulator, substrate noise caused the signal to noise power ratio to decrease by more than 18dB, 3 bits in terms of analog-to-digital converter metrics.

In addition, two techniques of minimizing the substrate noise and its effects were explored. The first used a replica delta-sigma modulator on the same chip to subtract the effects of substrate noise from the original delta-sigma modulator. This method proved useful for removing input signal independent substrate noise, but not input signal dependent substrate noise which dominates in-band noise for large input signal magnitudes.

The second technique involved an active substrate noise cancellation system. A discrete time feedback loop senses the substrate noise, processes it through a filter, and uses an array of digital inverters to cancel the substrate noise. The principal advantages of this technique are the shaping of substrate noise through a designed filter without a significant power penalty and design independence from the analog and digital components. Measured data shows that this technique is capable of over 20dB reduction in substrate noise on the substrate voltage itself. Measured data also shows over 10dB improvement in SNDR of the delta-sigma modulator in certain cases.

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Acknowledgments

For me, the Ph.D. at MIT has been more than just a research endeavor. It has been a *life* experience. Only through the unrelenting support of many people during these years have I been able to successfully get through this experience and I would like to acknowledge them.

First and foremost, I would like to thank my advisor, Professor Hae-Seung Lee, with utmost gratitude. Under his enduring guidance and continued encouragement, I have had the chance to learn about analog circuit design and to apply my creativity and skills to an important topic. It has been an honor and my good fortune to work under him.

My thesis committee readers, Professor Charles Sodini and Dr. Joseph Lutsky also deserve special thanks for taking the time to read my scribblings. They genuinely helped me in providing insightful and constructive comments on my research. Kush Gulati and Ayman Shabra have been exceptional as senior colleagues. Not only are they experts in the field, but they are great mentors as well. Jim Goodman has also been most gracious by providing technical assistance and a real digital circuit design for use in my project. In addition, I would like to thank all my officemates, young and old, for giving me a dynamic and exciting atmosphere to live and learn in. You can really learn a lot by just being around smart people. Todd Sepke, Mark Spaeth, and Andrew Chen deserve special mentions for answering my LaTeX questions, providing video games, and giving me miscellaneous help, respectively.

Undying gratitude also goes to the MTL and MIT staff who have helped me navigate my way through the labyrinth of MIT policies and regulations. Super special thanks to Carolyn Collins for being an extraordinary administrator of my concerns and needs at MIT.

National Semiconductor also helped me immensely in my completing the research for this dissertation. Not only did they provide chip fabrication, but also computing resources, tools, and technical assistance at their East Coast Labs branch. I sincerely appreciated the time and effort they took for me.

On a different note, I want to give special recognition to Ashdown House as my *home sweet home* during the past five years. Ashdown House is truly the best place to live while at MIT because of the people and community that exists for students to be a part of. It has been one exhilarating and enriching experience. My roommate of four years, Ron Dror, deserves a medal of honor for putting up with me and my frequent guests.

During this time, I think the person most burdened has been my beloved wife and editor, Diana. She has been a special and great influence in my life and has supported me unconditionally. She makes my days brighter and more vibrant. Furthermore, under her tutelage, I have had a rigorous course in fashion and etiquette. As a result, I have become a more refined being.

Lastly, I want to thank my mother and family. They have made everything in my life possible. In particular, my mother and Don have fed me steaks and served me wine so that I could grow to be a big man. *At times, I feel like nothing but Matsuzaka beef.* Marlo, Garvin, Cade, and XiaoMei have taken me to Disneyland so that I could become a kid again. In all, it has been a long, long, and long road.

As a final word, I would like to acknowledge MIT, the institution as a whole. MIT is a wonderful place where I have not only explored a fascinating problem, but I have also been

able to grow as a person. The dynamic environment and motivating people foster education in the truest and purest sense. Despite my frequent grumbling and moaning, it still is a world-class institution for learning just about everything. I will forever miss the life as a student here at MIT.

I dedicate this thesis to my father, Chu-Chin Peng.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

The basic demands of power, speed, and cost have driven systems to ever higher levels of circuit integration. The goal is to integrate as much functionality on as few microchips as possible for a single system. With fewer chips, decreased power comes with driving less data lines between separate chips. Increased speed comes with the elimination of relatively slow off-chip traces. Reduced cost, perhaps the most important factor, comes with fewer chip packages and simpler circuit boards.

The ultimate manifestation in this integration quest is a single chip or the so-called System on a Chip (SoC). One example of SoC is the PicoRadio project at the University of California at Berkeley [1]. This project aims to create "transceivers for ubiquitous wireless data acquisition that minimize power/energy dissipation." It will do this by integrating on a single piece of semiconductor as much as possible including, but not limited to: field programmable gate array (FPGA), digital signal processor (DSP), memory, power control, filtering, radio-frequency (RF) circuits, analog to digital converters (ADC), and digital to analog converters (DAC). A graphical representation of this system integration is shown in Figure 1-1.

In general, the realization of mixed-signal systems for SoC requires the integration of analog circuits and digital circuits onto the same substrate. Traditionally separated, these two parts, placed together on a single chip, can interact in unintended and harmful ways. One way is through the power supply. If the analog and digital power supplies are not properly designed (*e.g.* separating analog and digital supplies), then any voltage fluctuation on the power rail due to large digital current spikes flowing through the bondwire/pad inductance, will affect the analog circuits. Another and perhaps more insidious way in which digital and analog circuits can interact harmfully is substrate noise coupling. The digital circuits create unwanted signals in the shared substrate–from herein referred to as substrate noise–which then couples into and affects sensitive analog circuits. This effect, illustrated in Figure 1-2, can severely degrade performance, even rendering the analog circuits useless if the substrate noise is severe enough.

Substrate noise coupling has received increased attention as integration for SoC and mixed-signal chips has become practical through aggressive technology scaling and necessary for satisfying the demand of new consumer applications. In the future, the problem of

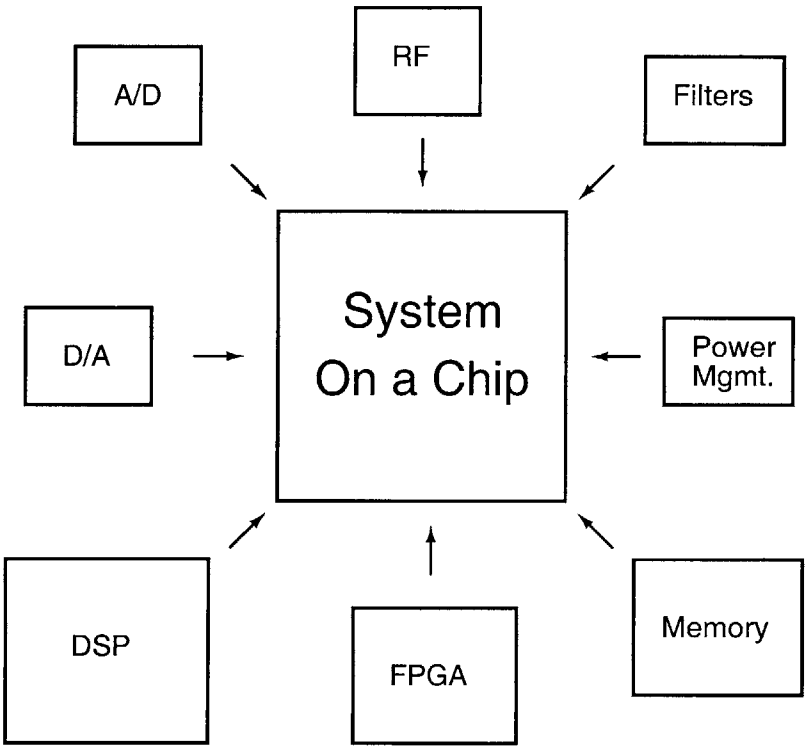


Figure 1-1: Integration of all system components on to a single chip.

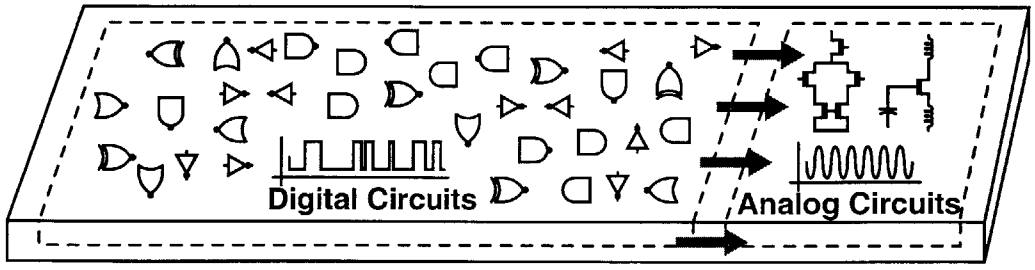


Figure 1-2: Digital circuits generate substrate noise that affects analog circuits fabricated on the same substrate.

substrate noise coupling will only worsen for many reasons:

1. **Increased Digital Circuit Content** – As feature sizes shrink, more and more digital circuits can be placed on a chip. Tens of millions of digital gates on a chip is commonplace. Systems, in general, try to push as many functions as possible into the digital domain because of ease of implementation and noise immunity. This can only increase the amount of substrate noise generated by the digital circuits.

2. **Reduced Voltages** – The supply voltage continues to scale down because of smaller feature sizes. While many benefits are reaped from smaller features, signal swing becomes squeezed and any noise in analog circuits becomes less tolerable.

3. **Increased Digital Clock Speeds** – With smaller feature sizes, transistors can run faster and thus digital clock speeds can be increased. If digital transients do not settle quickly, the substrate may be constantly fluctuating so that analog operations must be performed in a noisy environment. As an example, many of the most advanced digital circuits are now clocked at over 2GHz, giving transients less than half a nanosecond to settle.

4. **Large Numbers of I/O** – In order to offer increased functionality on a single chip, systems will need to have more channels of communication, specifically inputs and outputs (I/O). More I/O requires more pad drivers which can dominate substrate noise [2].

Thus, the study of substrate noise coupling as well as methods to mitigate its effects have come to the forefront of IC research. In the last decade, a modest body of research on substrate noise coupling has been performed, but more needs to be done, especially since the problem will only worsen. Additionally, more research needs to focus on understanding the ultimate effects on sensitive analog circuits and ways of combating them. This knowledge will allow development of techniques to combat the substrate noise effectively. This research was an attempt in that direction.

This research had two focuses. One of the focuses of this research was on the ways substrate noise from digital circuits affects analog circuits, specifically sampled data systems. These types of analog circuits are now widely used and identifying the mechanisms of performance degradation inflicted by substrate noise coupling is useful. Understanding these mechanisms will allow design of more robust circuits. In addition, the work done for sampled data circuits can also be generalized to other analog circuits as well.

The second focus of this research was to propose and develop techniques for minimizing the harmful substrate noise coupling. In particular, this research examined the effectiveness of using replica analog circuits to subtract substrate noise effects from the primary analog circuits. Also, the effectiveness of an active substrate noise cancellation system, essentially a feedback loop, was proposed and evaluated. The proposed active cancellation circuit aims to shape the substrate noise in specific bands of interest and uses a bank of digital inverters as the feedback element. The chief advantages of this technique were simplicity, practicality, and low power.

In order to conduct this research, a chip that facilitated substrate noise study and implemented the minimization techniques was designed and fabricated in National Semiconductor's 0.25um CMOS on an epitaxial wafer.

1.1 Thesis Organization

Chapter 2 summarizes past work in the field of substrate noise coupling. This includes mechanisms of coupling, modeling, and techniques for minimization.

Chapter 3 presents the study of substrate noise coupling and effects on analog circuits, specifically, switched capacitor delta-sigma modulators. Circuit designs and testing methodologies for the experimental chip are described. Testing results and analysis of the measured data are also presented. The chapter concludes with prescriptions for minimizing substrate noise and its effects.

Chapter 4 presents substrate noise minimization techniques. System design and circuits used in these techniques are described. The effectiveness of the techniques are then discussed in light of measured data.

Chapter 5, the final chapter, draws conclusions from the research and suggests future directions for this work.

For convenience and reference, Table 1-1 provides the definitions of the abbreviations and acronyms used in this thesis. These abbreviations and acronyms will also be defined the first time they are used in the text.

Abbreviation or Acronym	Shorthand for	Comments
SoC	System on a Chip	
FPGA	field programmable gate array	
DSP	digital signal processor	
RF	radio frequency	
ADC	analog to digital converter	
DAC	digital to analog converter	
IC	integrated circuit	
PCB	printed circuit board	
LNA	low noise amplifier	
SCL	source coupled logic	
ECL	emitter coupled logic	
DRIE	deep reactive-ion etching	
DS	delta-sigma modulator	
SC	switched capacitor	
DS1	delta-sigma modulator 1	converts an external off-chip analog signal
DS2	delta-sigma modulator 2	converts the substrate voltage
InvArrA	Inverter Array A	simulates substrate noise generated by I/O pad drivers and clock buffers
DelayA	delay A	the delay between the rising edge of the clock that controls InvArrA and the analog sampling edge
CIFB	Cascade of Integrators with Feedback	
STF	signal transfer function of the delta-sigma modulator	
NTF	noise transfer function of the delta-sigma modulator	

Table 1-1: Abbreviations/acronyms used in this thesis.

Abbreviation or Acronym	Shorthand for	Comments
SNR	signal power to noise power ratio	
SNDR	signal power to noise plus distortion power ratio	
THD	total harmonic distortion	in dB below full scale
CMFB	common-mode feedback	
FFT	fast fourier transform	
TINP	total in-band noise power	in dB below full scale
DSA	delta-sigma modulator A	converts an external off-chip analog signal
DSB	delta-sigma modulator B	converts an external off-chip analog signal
D2Inv	digital to inverter array	generates substrate noise for use in the SNSL
SNSL	substrate noise shaping loop	
DSRCP	Domain Specific Reconfigurable Processor	designed by Goodman [3]
DelayB	delay B	the delay between the rising edge of the clock that controls DSRCP and the analog sampling edge
DelayX	delay X	the delay between the rising edge of the clock that controls D2Inv and the analog sampling edge

Table 1-2: More abbreviations/acronyms used in this thesis.

Chapter 2

Substrate Noise Background

Substrate noise, transient signals on the substrate caused by circuits, occurs because the substrate does not have zero impedance. Ideally, the substrate is a uniform, perfectly conducting medium that acts like a voltage source. However, parasitics such as bond wire inductance, interconnect capacitance/resistance, printed circuit board (PCB) trace capacitance/resistance and substrate resistivity create finite source impedance as shown in Figure 2-1. This makes the substrate voltage fluctuate in response to any changing voltages or currents caused by circuits that are fabricated on the substrate. Furthermore, the impedance at each and every point on the substrate to the power supply differs and thus, the substrate voltage can vary across the substrate.

2.1 Mechanisms

Three mechanisms of circuits creating substrate noise have been identified [4] [5]. They are:

1. **Capacitive Coupling** – Switching signals create displacement currents in the substrate through transistor gate capacitance as well as parasitic junction capacitance and interconnect to substrate capacitance.

2. **Impact Ionization** – In the high electric field region under the gate of an NMOS, accelerated electrons create electron-hole pairs. The holes then flow to the substrate contacts and appear as a current fluctuation on the lower power rail.

3. **Power Supply Transient** – Inductance, capacitance, and resistance allow the voltage to fluctuate on the power supply rails as seen by the circuits on the chip. Since the substrate is ultimately connected to the lowest power rail through a non-zero impedance source, it will also fluctuate if there is any disturbing event such as a sudden current draw from a transitioning inverter.

In past studies [4] [5] [6, pp. 11-13] [7], the mechanisms of capacitive coupling and power supply transient have been identified as major sources of substrate noise in current technologies. However, impact ionization, while much smaller in magnitude, can still add substrate noise, especially in short channel MOS technologies.

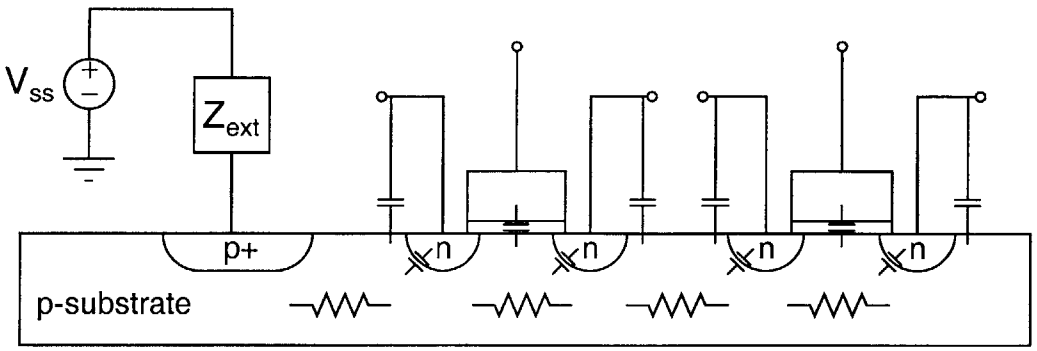


Figure 2-1: Parasitics, on and off the chip die, make the substrate look like a non-zero impedance voltage source. The voltage across the substrate will also be non-uniform due to the finite resistivity of the substrate. Z_{ext} denotes all off-chip impedances such as bondwire and pin inductance.

The identified mechanisms contribute different types of substrate noise. Substrate noise generated via capacitive coupling is correlated with the digital signal transition that created it. A capacitor tends to keep a constant voltage across itself and any voltage change on one side of the capacitor will be accompanied by a voltage change on the other side. For example, digital high-to-low transitions will create high-to-low noise signals in the substrate and digital low-to-high transitions will create low-to-high noise signals in the substrate. On the other hand, power supply transient and impact ionization create substrate noise that is less correlated with the digital signal transition that created it. This is because the substrate noise is created by transient currents such as direct path currents (shown in Figure 2-2) which tend to be independent of digital transition direction. For example, digital high-to-low transitions and digital low-to-high transitions will create similar types of substrate noise [6, p.126]. The resulting substrate noise is the sum of the substrate noise components generated by each mechanism.

The relative strength of substrate noise generated through the aforementioned mechanisms depends on many factors related to the physical layout, fabrication technology, and packaging of a circuit. For example, physically large transistors result in large parasitic capacitances from signal nodes to the substrate and will result in large capacitive coupling. In terms of fabrication technology, more heavily doped substrates result in increased junction capacitance. In terms of chip packaging, long bondwires result in larger inductance which will worsen the power supply transient. In general, the effect of these factors can be minimized through careful design which will result in less substrate noise.

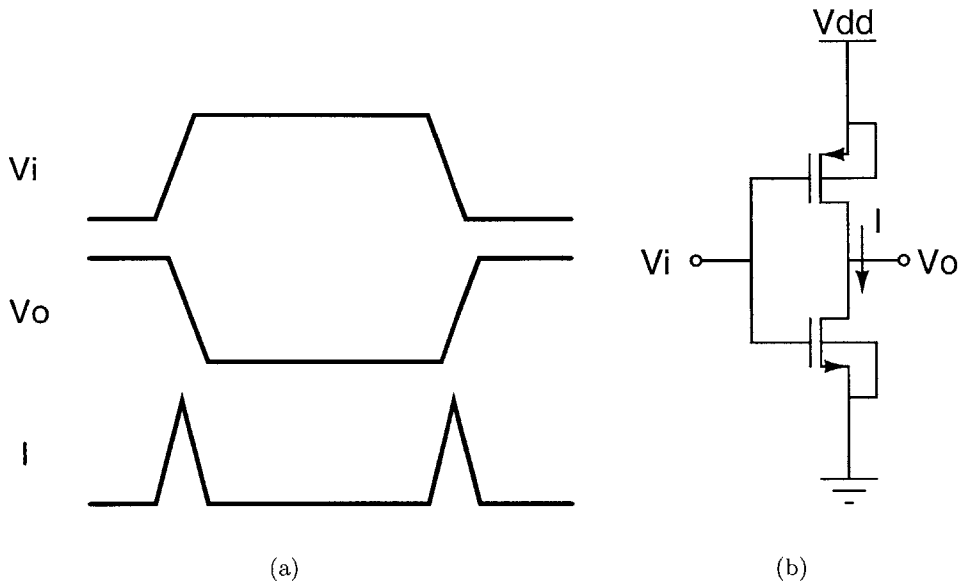


Figure 2-2: Typical voltage and current waveforms for a conventional static CMOS inverter. (a) waveforms and (b) conventional CMOS inverter schematic.

2.2 Substrate Noise Measurements

Substrate noise generated by digital circuits has been measured and characterized in many different ways for many different fabrication technologies and circuit applications [4] [6] [8] [9] [10] [11] [12] [13] [14]. In general, the data shows that substrate noise waveforms tend to ring in response to events such as switching digital gates. This is reasonable since the substrate is connected to parasitic capacitance and inductance that form a resonant circuit. In addition, the data shows that the frequency content of the substrate voltage is dominated by resonant frequencies based on parasitics (e.g. bond wire, decoupling capacitance, etc.) as well as by digital circuit repetition and clock frequencies. One study also showed that low frequency substrate noise is mainly caused by random digital logic activity [14]. The conclusion from this is that substrate noise can be strong in certain frequency bands and weaker in others.

In all the studies cited above, the substrate noise source was always some type of simple digital circuit, usually inverters switched in a deterministic way. These may simulate substrate noise due to digital I/O pad drivers and clock buffers, but they do not exactly mimic a real digital circuit such as a DSP, which has random digital logic as well.

In general, the major components of a digital chip are random digital logic, pad drivers, and clock buffers. Any one of these components can dominate substrate noise in a mixed-signal chip. Thus, analog circuits must be tested against each type of digital circuit to

ascertain a complete picture of analog circuit performance in the presence of substrate noise.

It should be noted that analog circuits can create substrate noise since they are actively changing states and are coupled to the substrates in the same ways as digital circuits. However, the substrate noise generated by analog circuits is usually ignored because it is much smaller in comparison to that generated by digital circuits. The main reason for this is that digital signals (*i.e.* voltage and current) swing quickly from one extreme to another, maximizing substrate noise creation through capacitive coupling, power supply transient, and impact ionization. In comparison, analog circuits, except for comparators, usually swing much less and relatively slowly, resulting in much less substrate noise.

2.3 Modeling

Modeling of the entire chip allows simulation of substrate noise and the discovery of any problems it may cause in a circuit design. Any problems discovered before fabrication can be corrected (or at least made tolerable) so that costly errors are not cast in silicon.

Modeling of the chip die itself is conceptually straightforward. The substrate and material above it is divided into an mesh of unit elements as shown in Figure 2-3. The fineness of meshing will depend on the accuracy desired. From these unit elements, a circuit schematic of transistors, capacitors, inductors, and resistors can be extracted which can then be used for simulation. This will include all explicitly designed devices, such as decoupling capacitors, as well as parasitic ones such as *pn* junctions and interconnect above the substrate. To get the complete chip model, the devices of the chip package must also be added since they significantly impact the substrate noise behavior. Additionally, all these parasitics mentioned must be modeled well because they are, in fact, the determinants of substrate noise.

Generating, let alone simulating, this complete chip model is particularly difficult because chips today are large and extremely complex in geometry, resulting in prohibitive amounts of computation. Much research in substrate noise modeling has focused on reducing computation [6, pp. 51–70] [15] [16] [17] [18, pp. 77–116] [19]. They use certain simplifications, macromodels, and efficient solvers, which shorten computation, but usually not enough to be practical for large designs.

One particular simplification of note for modeling is the case of low-resistivity substrates such as an epitaxial substrate. An epitaxial substrate usually has a lightly doped, highly resistive layer fabricated on top of a highly doped, highly conductive layer as shown in Figure 2-4. In this case, previous studies have showed through experimental data and extensive simulations that the substrate voltage varies weakly with the x and y dimension shown in Figure 2-3 [8] [15]. As a consequence, the entire substrate can be approximated as a single node. This single node has an impedance, Z_{sub}, to the power supply that includes bondwire/pin inductance, interconnect resistance, etc. The digital circuits interacting with the substrate through different mechanisms can be modeled as a Thevenin equivalent: an equivalent voltage source, V_{digth}, and a equivalent source impedance, Z_{digth}. This Thevenin equivalent circuit coupled with the Z_{sub} results in Figure 2-5. This simple model shows

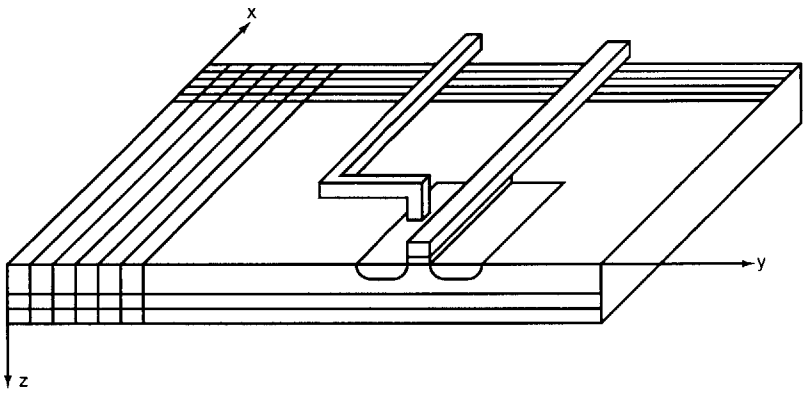


Figure 2-3: Meshing of the chip die. Even with just a few devices, the chip die must be meshed finely to attain useful results which makes chip simulation difficult and computation of substrate model components long.

that substrate noise, fluctuations on V_{sub}, depend on the digital circuits connected to the substrate as well as the parasitic impedances from the substrate to ground.

2.4 Substrate Noise Effects on Analog Circuits

Past studies measured the performance degradation of analog circuits due to substrate noise. Blalack *et al.* showed that signal power to noise plus distortion power ratio (SNDR) was severely decreased in a CMOS cascaded third-order sampled data delta-sigma modulator in the presence of substrate noise [20]. Using inverters to drive noise into the substrate via multiple 5pF capacitances, a decrease of over 30dB in SNDR was observed when the rising edge of the digital clock (*i.e.* when the inverters transitioned) was coincident with the sampling clock. This is attributed to the transients associated with the digital noise sources which are at a maximum during the rising edge of the digital clock. Furthermore, most of the decrease in SNDR was due to distortion of the input signal. Larger input signals resulted in a disproportionately larger decrease in SNDR suggesting that the mechanisms of distortion were being enhanced by the substrate noise.

In a study of the effects of substrate noise on low noise amplifiers (LNA), Xu *et al.* concluded that the substrate noise can directly couple to the differential output through differential mismatch [13]. Furthermore, the substrate noise, as a common mode source, enhances intermodulation effects. The amount of substrate noise coupling is influenced by the amount of capacitive coupling from digital circuits to the substrate and the rise/fall time of the digital circuitry.

For operational amplifiers, a study by Catrysse showed that substrate noise can cause distortion and phase shifts in operational amplifier output [21]. Since operational amplifiers are basic building blocks for other analog circuits, this effect is very important in determining

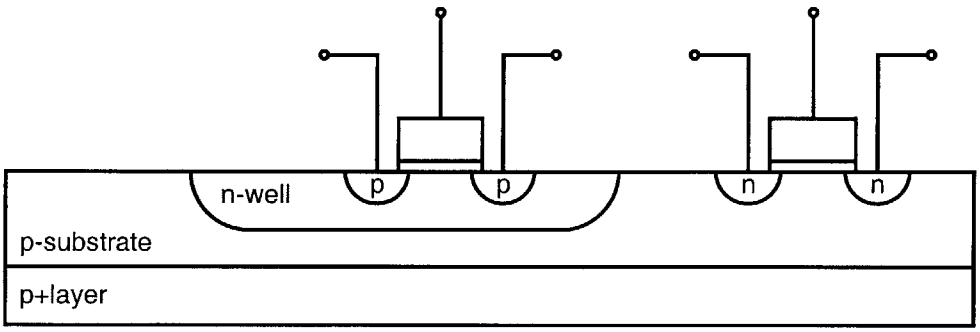


Figure 2-4: Cross-section of a p-type epitaxial substrate. Transistors are fabricated on a lightly doped, highly resistive p-type substrate which is on top of a highly doped, highly conductive p-type buried layer.

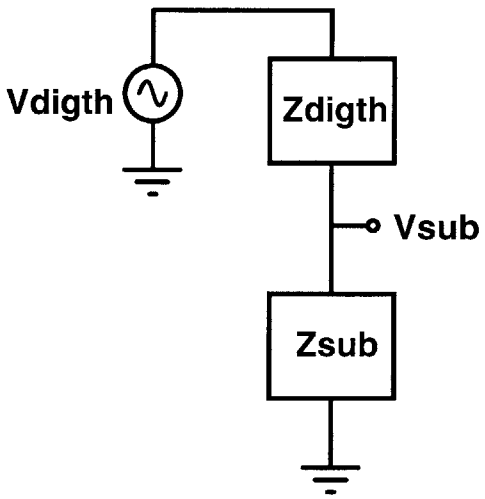


Figure 2-5: Simple model of the substrate noise for a low-resistivity substrate which can be approximated as one node [8] [15]. Digital circuits and their interactions with the substrate through substrate noise generation mechanisms are modeled by a Thevenin equivalent circuit composed of V_{digth} and Z_{digth}. Impedance from the substrate node, V_{sub}, to the power supply, is represented by Z_{sub}. Substrate noise, fluctuations on V_{sub} due to digital circuits, thus depends on the digital circuits on the substrate as well as the impedance from the substrate to the power supply.

overall system performance degradation.

In general, the substrate noise, as expected, always degrades performance. This problem is especially acute in RF circuits where even the slightest substrate noise coupling can be problematic because signal levels are low [22].

2.5 Techniques for Coping with Substrate Noise

Many techniques have been proposed and implemented to combat harmful substrate noise and its concomitant effects. The following is a non-exhaustive list of approaches to tackling the problems of substrate noise. Additionally, advantages and disadvantages are briefly discussed. More detail and discussion can be found in the references.

2.5.1 Reduced Noise Digital Design

One method to reduce the amount of substrate noise generated by the digital circuits is to design digital circuits that generate less substrate noise.

The most widely used digital circuit family is static CMOS. This digital circuit family is usually noisy because many gates/circuits simultaneously draw large spikes of current and quickly swing from rail-to-rail voltages as shown in Figure 2-2 on Page 27. The substrate noise peak magnitudes can be lessened by manipulating the times at which different digital gates/circuits transition. By manipulating skews and delays, the substrate noise associated with digital transitions can be spread out over a period of time which minimizes the peak magnitude of substrate noise. Figure 2-6 illustrates the general concept of this scheme. Badaroglu *et al.* used this scheme to reduce peak magnitudes of substrate noise by a factor of 3 with only 3% area penalty and 4% power penalty [23]. The main advantage of this technique is that static CMOS can still be used and no fabrication technology modification is needed. The main disadvantage of this technique is that implementing this type of skew management combined with other digital time constraints (*e.g.* race conditions, flip-flop hold time, etc.) of complex digital circuits may be very difficult and time consuming.

Digital families other than static CMOS may be used for lower substrate noise. Certain digital families inherently generate less substrate noise because they do not have the undesirable characteristics of static CMOS. Examples are Source Coupled Logic (SCL) [24] and Emitter Coupled Logic (ECL) [6, p.201] which have relatively small voltage swings and as a consequence have very small dynamic power, both of which minimize substrate noise. The drawback of these families, despite the extremely low propagation delays, is the large static power consumption which allows fast switching.

Another technique to minimize the impact of substrate noise on analog circuits is to perform crucial analog operations out of phase with digital operations [25]. If digital transients settle quickly, analog operations can be performed when the substrate returns to the quiescent voltage as shown in Figure 2-7. The limitation of this method is that digital clocking speeds must be low enough to allow for substrate transient settling and relatively slow analog operations. Increasing digital clock speeds may, however, make the substrate voltage constantly fluctuate and thus not allow any "quiet" time for analog operations to be performed.

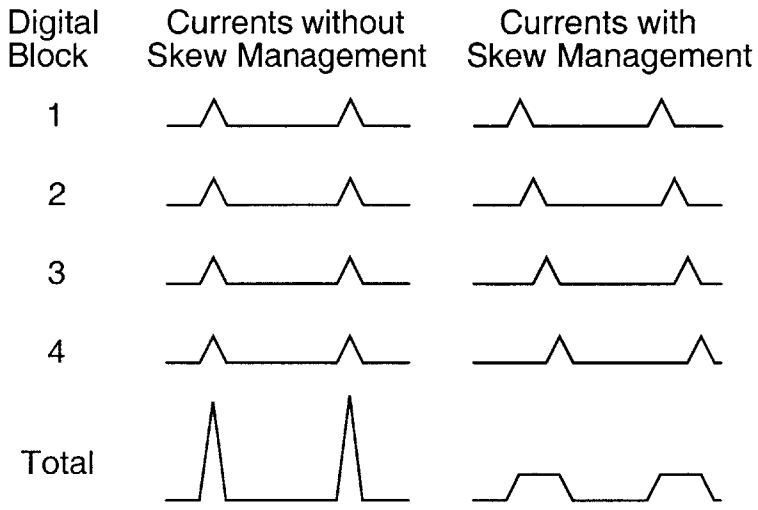


Figure 2-6: By managing the skew between different digital blocks, the peaks of current spiking, which create substrate noise, can be minimized.

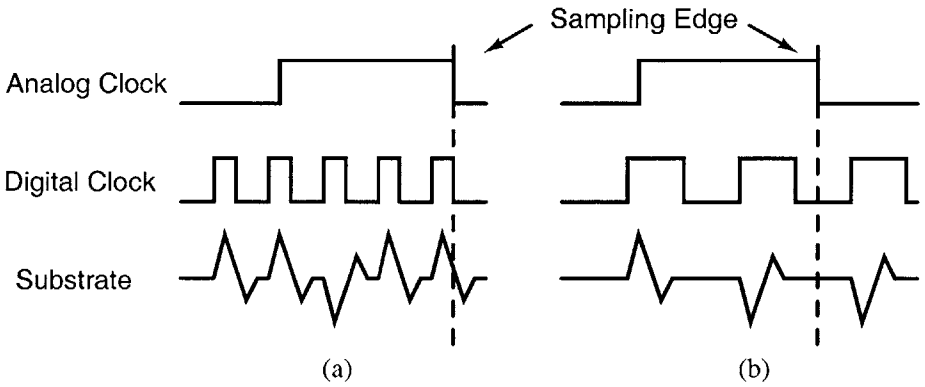


Figure 2-7: By managing delays between digital and analog clocks, transients on the substrate can be avoided when performing analog operations such as sampling. (a) the substrate voltage has not settled when analog operations are performed and (b) the substrate voltage has settled before analog operations are performed.

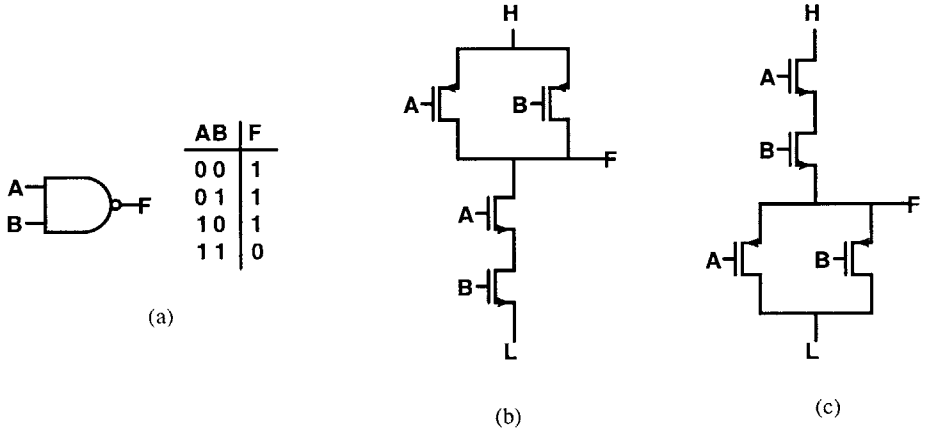


Figure 2-8: Dual digital circuit implementations of a NAND. (a) NAND Gate Symbol and Truth Table (b) Positive Logic Implementation (c) Negative Logic Implementation.

Another approach for reducing substrate noise created by digital circuits is to build dual digital circuits [26]. Digital circuits are implemented in both positive digital logic–a low voltage corresponds to a binary zero and a high voltage corresponds to a binary one– and in negative digital logic–a low voltage corresponds to a binary one and a high voltage corresponds to a binary zero. These two implementations, which perform the exact same function, placed together on the same chip minimize the amount of capacitively coupled substrate noise by matching every positive transition (a low voltage to a high voltage) to a negative transition (a high voltage to a low voltage)[1]. Thus, no net displacement current from capacitive coupling is injected into the substrate. As an example, the case for a NAND gate is examined. Table 2-1 and Table 2-2 shows the transitions for a NAND gate implemented in positive and negative logic. Figure 2-8 shows the circuit implementations. Although this scheme may reduce capacitively coupled substrate noise, it does not reduce and in fact worsens the substrate noise due to the power supply transient and impact ionization because of a doubling of direct path currents. Furthermore, this scheme is very power inefficient since two implementations of the same function increase the power consumption of digital circuits by two.

2.5.2 Packaging

Substrate noise can also be reduced by minimizing the pin/bondwire impedances associated with chip packaging. These impedances are responsible for the power supply transients when digital circuits switch.

An example of a specialized package that minimizes the pin impedances associated with substrate biasing is a "paddle package." This package has a "paddle," a solid metal

[1]These facts are closely related to De Morgen's Theorem [27].

Inputs	Outputs	Volt. Transitions	
$A_0B_0 \longrightarrow A_1B_1$	$F_0 \longrightarrow F_1$	L→H	H→L
00(LL) $\longrightarrow$ 01(LH)	1(H) $\longrightarrow$ 1(H)	1	0
01(LH) $\longrightarrow$ 11(HH)	1(H) $\longrightarrow$ 0(L)	1	1
11(HH) $\longrightarrow$ 00(LL)	0(L) $\longrightarrow$ 1(H)	1	2
00(LL) $\longrightarrow$ 11(HH)	1(H) $\longrightarrow$ 0(L)	2	1

Table 2-1: NAND–Transitions in Positive Logic. Parentheses represent the corresponding voltage level–H is high voltage and L is low voltage.

Inputs	Outputs	Volt. Transitions	
$A_0B_0 \longrightarrow A_1B_1$	$F_0 \longrightarrow F_1$	L→H	H→L
00(HH) $\longrightarrow$ 01(HL)	1(L) $\longrightarrow$ 1(L)	0	1
01(HL) $\longrightarrow$ 11(LL)	1(L) $\longrightarrow$ 0(H)	1	1
11(LL) $\longrightarrow$ 00(HH)	0(H) $\longrightarrow$ 1(L)	2	1
00(HH) $\longrightarrow$ 11(LL)	1(L) $\longrightarrow$ 0(H)	1	2

Table 2-2: NAND–Transitions in Negative Logic. Letters in the parentheses represent the corresponding voltage level–H is high voltage and L is low voltage.

piece, as the backside of the package. Chip die are mounted on this paddle, creating a low-impedance backside contact. Furthermore, "downbonds" connect ground pads to the paddle, further decreasing the parasitic impedances. The package is then soldered to a printed circuit board so that the backside paddle is in contact with a ground pad or plane. This reduces the parasitic impedances of the substrate connection greatly. The drawback of this approach is the cost of the package and the extra downbonding process. However, for certain applications such as RF ones, the cost may be justified. In fact, this package was originally developed for RF applications which need low impedance substrate to ground connections [22].

2.5.3 Power Grid Design

Since much of the substrate noise generated is due to switching currents in the digital circuits, much effort has focused on designing power supply networks that inherently reduce power supply fluctuations.

The first way to reduce substrate noise due to power supply fluctuations is to use the so-called Kelvin grounding technique [5] where the substrate, digital circuits, and analog circuits all have their own dedicated power supplies as shown in Figure 2-9. Using this scheme, short circuit current spikes caused by either the analog circuits or digital circuits will not affect the substrate through the power rails. Substrate noise, however, can still couple in capacitively to the substrate through the parasitic capacitances associated with every node. Also, the substrate connections between the analog and digital circuits may not be easily isolated since the substrate itself is conductive. For example, in Figure 2-9, if the chip is fabricated on a conventional p-substrate, then V_{subana} and V_{subdig}, the dedicated supplies for the substrate in the analog and digital sections, respectively, will be "soft" connected through the substrate. This technique has the drawbacks of extra interconnect and more pins for separate supplies which may not be acceptable. Compromises can be made by selectively combining supplies thereby reducing the drawbacks. For example, in Figure 2-9, the analog supply, V_{ssana}, may not be so noisy and may be combined with the dedicated supply connected to the substrate, V_{subana}.

Another way to reduce the substrate noise is to design power supply filters as shown in Figure 2-10 [5] [9] [28]. Given that bond wiring and package pins will always cause non-zero impedance on the supplies, appropriate networks of decoupling capacitors and resistances can be added to minimize transients and settling time. 80% reduction of peak-to-peak transients on the power supply have been reported [9]. Although promising, it must be realized that these techniques depend heavily on known parasitic values as well as realizable filter components. Care must also be taken not to affect circuit operation which can happen if extra resistances create large IR drops. Also note that capacitively coupled substrate noise is not reduced in these techniques.

2.5.4 Physical Separation and Barriers

One of the most commonly used techniques to combat substrate noise is physical separation and barriers. These techniques diminish the substrate noise transmission path and diminish

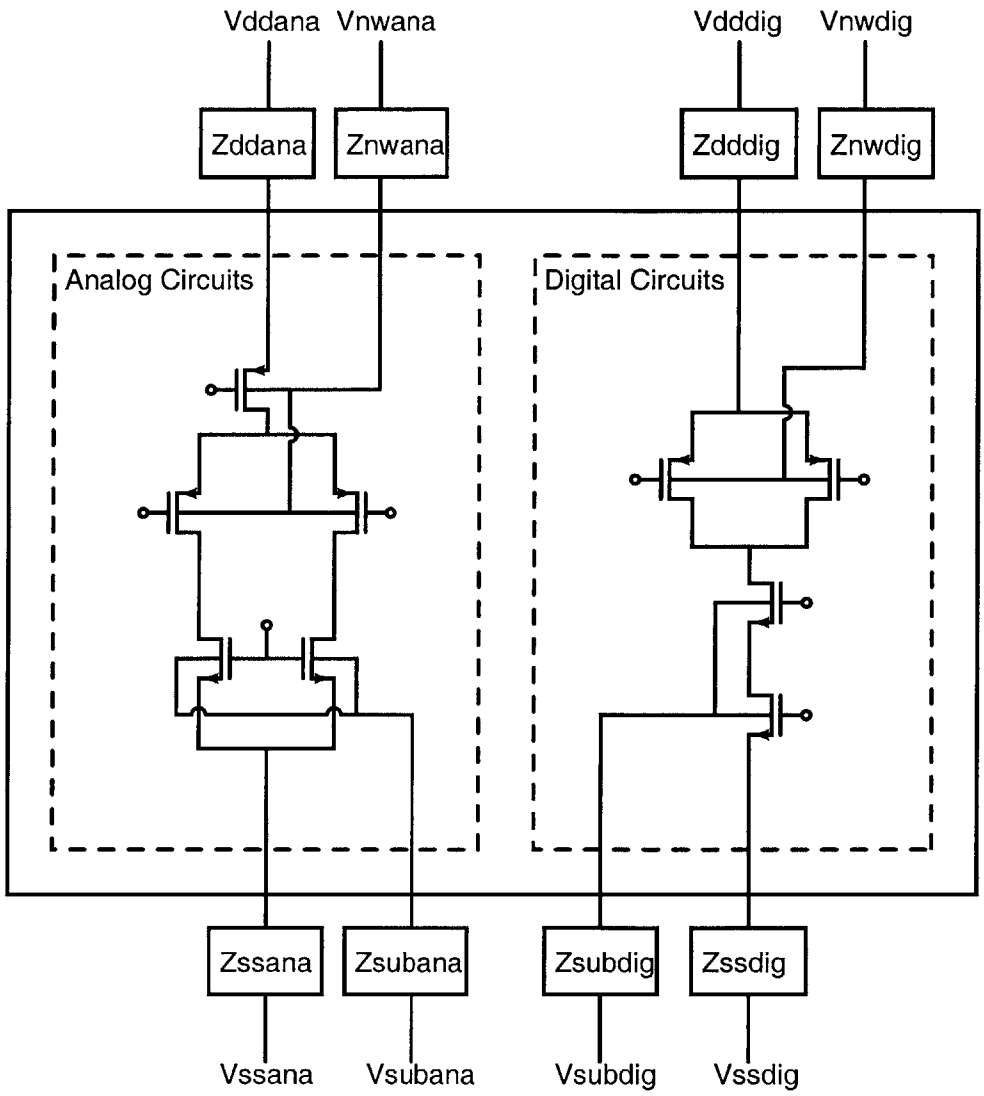


Figure 2-9: Kelvin grounding uses dedicated power supplies to the analog and digital circuit n-wells, substrate, analog circuits, and digital circuits. The V_{ddana} and V_{dddig} voltage supplies provide currents for circuit operation in the analog and digital circuits, respectively. V_{nwana} and V_{nwdig} bias the n-wells in the analog and digital sections of the chip, respectively. Similarly, V_{ssana} and V_{ssdig} supply currents to the analog and digital circuits while V_{subana} and V_{subdig} bias the substrates in the analog and digital sections. Z_{ddana}, Z_{nwana}, Z_{dddig}, Z_{nwdig}, Z_{ssana}, Z_{subana}, Z_{ssdig}, and Z_{ssana} are the associated impedances (*e.g.* pin/bondwire inductance, PCB trace resistance) with each voltage supply. These impedance values may be different because of physical differences such as bondwire length and PCB routing.

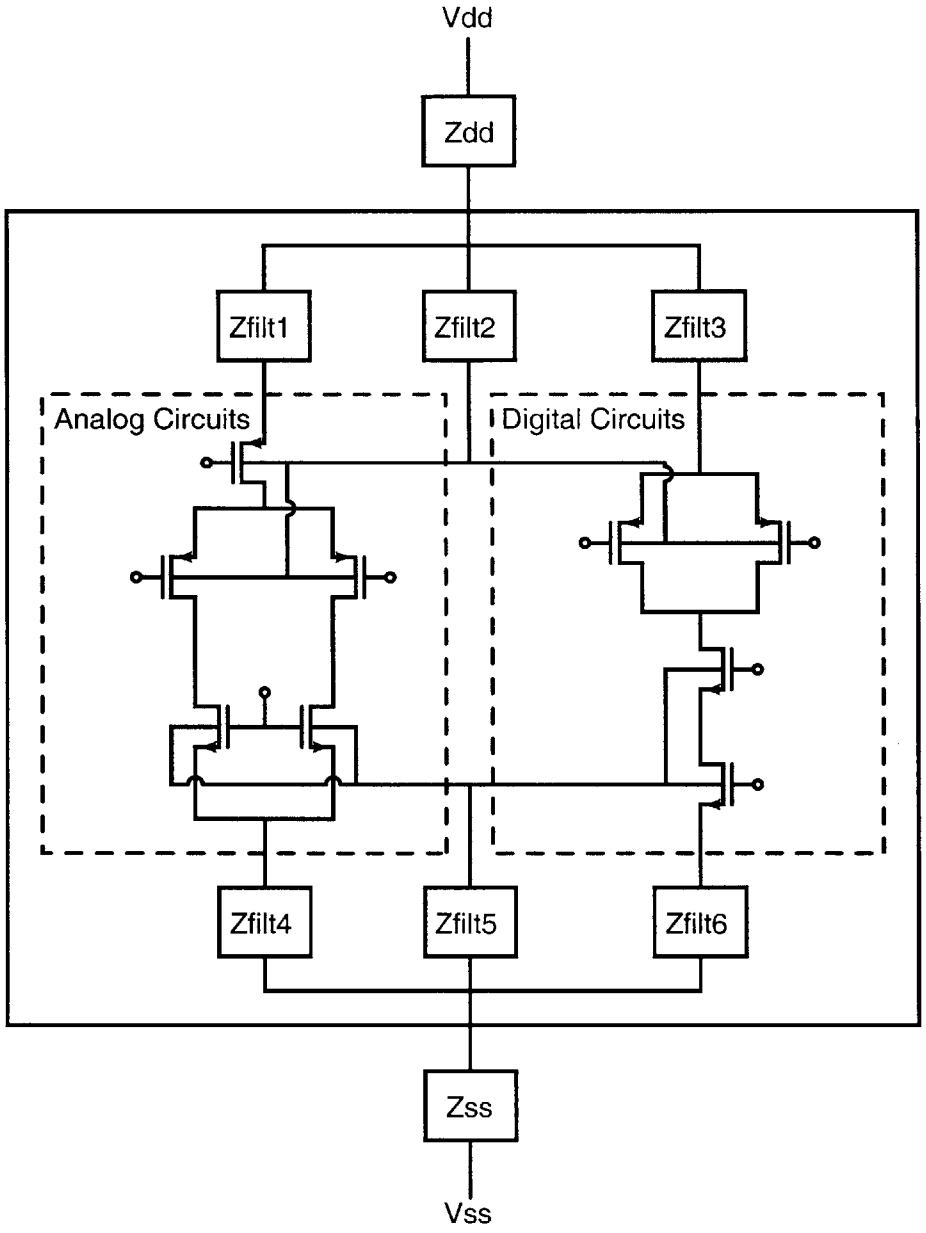


Figure 2-10: Adding filtering, Z_{filtn}, to the power supplies with parasitic impedances Z_{dd} and Z_{ss} can help reduce power supply fluctuations due to current transients by the analog or digital circuits. Z_{filtn} is designed so that when it is combined with Z_{dd} or Z_{ss}, substrate noise is attenuated at selective frequencies. An example of a simple filter is a resistor which dampens transients and reduces peak substrate noise magnitudes. Multiple Z_{filtn} can be used for different sections of the chip to provide some power supply isolation between different sections of the chip.

the magnitude of substrate noise seen at the analog circuits. To date, these techniques are the most common solutions to combating substrate noise for analog circuits and digital circuits fabricated on the same chip.

In physical separation, analog circuits are grouped together and then placed as far from the noisy digital circuits as possible. The expectation is that the distance between these two types of circuits will attenuate the substrate noise as it travels through the substrate. The amount of attenuation is dependent on the substrate material and distance of separation. This means that physical separation is not very effective for low-resistivity substrates where the substrate essentially looks like one node. Also, it may not be possible to place the digital and analog sections far from each other if chip area is a constraint.

Physical barriers include guard rings and guard trenches that are placed in between digital and analog circuits as shown in Figure 2-11. These guard rings when biased with a voltage source provide a low-impedance path for the substrate noise to be absorbed, thereby preventing further transmission. A study by Su *et al.* showed that biased guard rings can reduce substrate noise by a more than a factor of five [8].

The effectiveness of this technique, just as in physical separation, relies on the substrate material. This technique is not effective for commonly used epitaxial processes. Chips manufactured in this process have a low-resistivity buried substrate which transmits the substrate noise and thus guard rings will not absorb substrate noise as shown in Figure 2-12 [8].

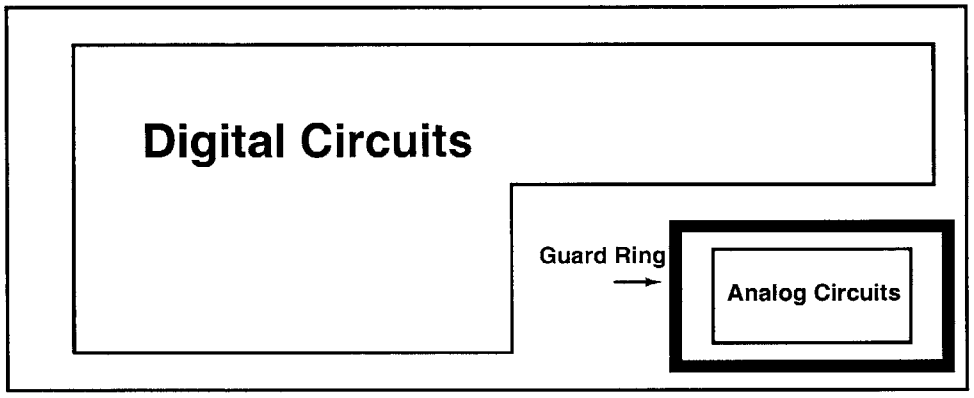
Another form of physical barrier is the"Faraday Cage" [29]. Through-wafer vias, created by deep reactive ion-etching (DRIE), are filled with metal and patterned around sensitive circuits so that a "Faraday Cage" is built. This Faraday cage has shown 20dB of isolation between two pads at 1GHz. The main disadvantage of this technique is the complexity of fabrication process integration.

A last form of physical barrier is the etching of a trench in the substrate to separate the digital and analog sections of a chip with air [30]. This lack of material essentially creates a capacitor which attenuates low frequency noise, but not high frequency noise. This method, like the Faraday Cage idea, suffers from processing integration issues.

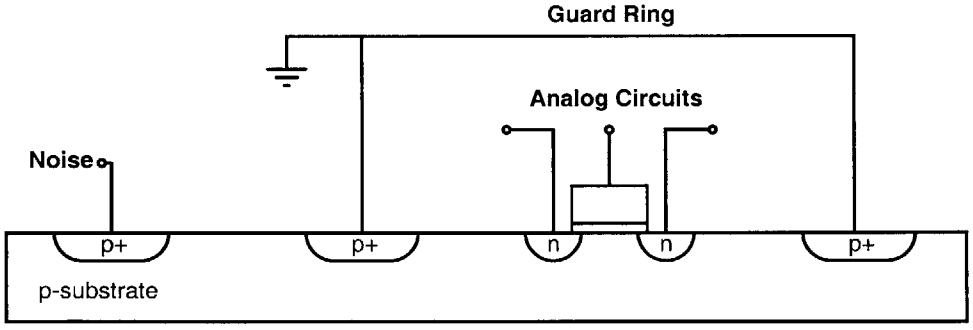
The use of physical separation barriers requires an appropriate power supply scheme. While focus has been on the substrate noise transmission through the substrate, it is possible that substrate noise may travel through the metal interconnect that connects to the substrate. Interconnect has low resistance and may be the medium of substrate noise transmission if the substrate is highly resistive. For example, if the digital and analog sections share the same power supply to connect to the substrate on a high-resistivity substrate, placing the digital and analog sections far from each other will have no effect because the noise in the digital section will be picked up and transmitted by the interconnect to the analog section.

2.5.5 Materials

Materials engineering, which designs the substrate noise transmission medium, is also an effective method of reducing substrate noise. High resistivity substrates such as non-epitaxial processes attenuate substrate noise as it propagates through the substrate from the point



(a)



(b)

Figure 2-11: Guard rings and trenches can absorb substrate noise and prevent further propagation to sensitive analog circuits. (a) top view (b) cross-section view

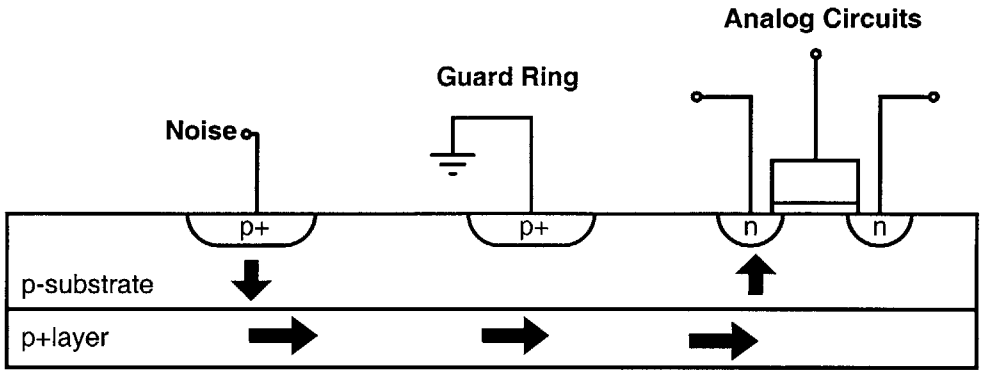


Figure 2-12: Substrate noise in epitaxial wafers travels through the low resistivity buried layer.

of substrate noise creation to the analog circuits. In this case, physical separation between analog circuits and digital circuits as well as use of physical barriers, explained above, is effective. On the other hand, low-resistivity substrates, such as epitaxial substrates, insignificantly attenuate substrate noise as it travels from one end of a chip to the other end. The low resistivity makes the substrate effectively appear as one-node so that physical separation is not effective. Furthermore, the use of physical barriers in epitaxial processes will not be effective because the substrate noise is transmitted through the buried low-resistivity layer as shown in Figure 2-12. On the other hand, since the substrate has lower resistivity it has lower impedance and thus substrate noise peak magnitudes are lower than that of high-resistivity substrates. Studies of the substrate noise in high and low-resistivity substrates confirm these conclusions [8] [15].

Of the two types, low-resistivity substrates are more commonly used because they minimize latch-up hazards, and thus are preferred by digital designers. This makes it likely that mixed-signal chips will also use low-resistivity substrates.

Another way to diminish the amount of substrate noise propagation through materials engineering is using multiple-well processes. The most conventional process, bulk CMOS, only has n-wells in which PMOS transistors are fabricated. This provides some isolation for the PMOS transistors since the substrate noise is conducted through the p-type substrate. NMOS transistors, on the other hand, all lie together in the p-substrate and cannot be isolated from one another. This can be changed with a deep n-well or "triple well" process which electrically isolates NMOS transistors from each other and the bulk substrate. A cross section of a chip fabricated in a deep n-well process is shown in Figure 2-13. The figure shows that all transistors are isolated from each other and the common substrate through reverse-biased junctions. In addition to extra fabrication costs, the use of deep n-wells incurs an area penalty for putting down two extra wells (a p-well and an n-well) for the NMOS transistors. A study by Joardar reported 66dB isolation (at 100MHz) between two areas in their own deep n-wells [31].

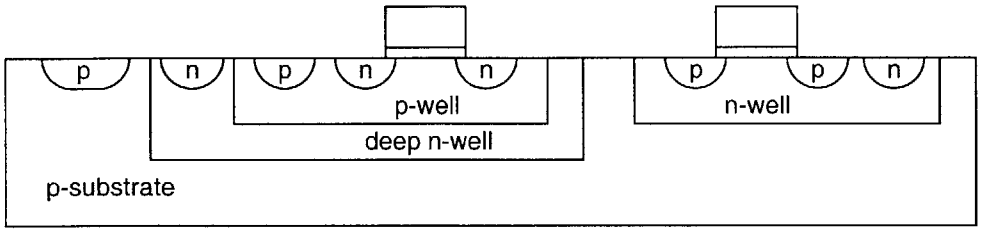


Figure 2-13: A cross section of a chip fabricated in a triple-well process. Transistors of any type can be isolated from each other and from the common substrate.

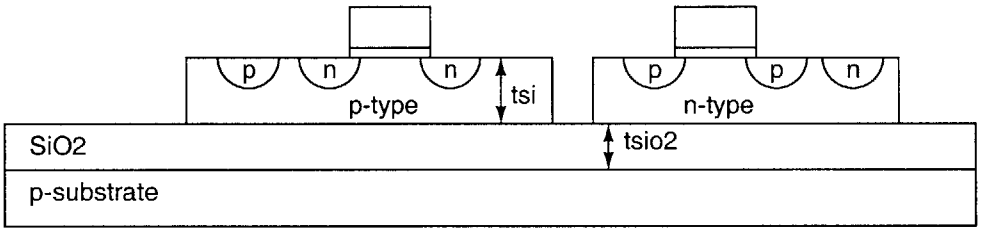


Figure 2-14: Typical cross section of a chip fabricated in a SOI technology. Transistors of any type can be isolated from each other and from the common substrate. t_{si} is typically 50nm-200nm and t_{si} is typically 400nm in common SOI technologies.

A special manifestation of the multiple well process is Silicon-on-Insulator (SOI). In SOI, selective "islands" of transistors, similar to wells, are fabricated on an electrically insulating substance, usually silicon dioxide. This is akin to having many disconnected substrates on the same chip, which thereby isolates circuits from each other. A typical cross section of the transistors fabricated in SOI technology is shown in Figure 2-14. This technology has been shown to be effective in isolating digital circuits from analog circuits [32], but not ideal since there is still appreciable capacitive coupling between the islands and the substrate because the t_{sio_2} dimension indicated in Figure 2-14 is typically only about 400nm. Furthermore, this capacitive coupling reduces the isolation at high frequencies. A study by Joardar reported 55dB isolation (at 100MHz) between two islands in SOI technology [31]. The main drawback of this technology is the fabrication cost.

Note that in all these different materials, separate power rails are needed or else the power rails themselves become the conduits of the noise, thereby destroying the benefits of using the special materials.

2.5.6 Analog Circuit Architectures

One of the most effective and most commonly used techniques to diminish the harmful effects of substrate noise is fully differential analog circuit architectures [33, pp. 335–336]. Differential circuits rely on the relative levels of signals, not on absolute levels. Under ideal conditions, common mode perturbations such as substrate noise, are perfectly rejected (*i.e.* do not create a differential signal). However, due to layout variations, random mismatch, non-linearities and other sources of asymmetry, differential circuits can still be adversely affected by common mode noise. Differential circuits add complexity because of the need for more circuitry than a single-ended implementation. However, the advantages of using differential circuits greatly outweigh the disadvantages.

2.5.7 Active Continuous Time Substrate Noise Cancellation

All methods listed so far have been passive techniques. They are passive in the sense that after chip fabrication, the substrate noise is determined and can not be reduced without physical modification of the chip.

Active techniques, on the other hand, make use of circuits to directly reduce the substrate noise when the chip is in operation. A system senses the substrate noise and then creates "anti-noise" in the substrate so that the net result is a reduction in substrate noise.

To date, the active noise cancellation systems conceived have all been continuous time implementations [34] [35] [36] [37] [38]. They all use a differencing amplifier to sense the substrate noise, compare it to a reference, and then drive an opposite signal back into the substrate as shown in Figure 2-15. The coupling of the amplifier to the substrate is usually done with a capacitor since the DC voltage level of the substrate, usually the lowest voltage in the system, is usually not in the acceptable range of amplifier input. This problem can be avoided by tailoring the input of the operational amplifier for the substrate DC voltage level [35].

Active noise cancellation systems have the advantages of:

1. **Standard Digital and Analog Circuit Design** – The approach makes no demands on the digital or analog circuit designs. The active substrate noise cancellation system can be designed independently and simply added to the mixed-signal chip.

2. **Complementary to Other Techniques** – Using an active substrate noise cancellation system does not preclude use of other techniques for minimizing substrate noise and its effects. Popular techniques such as differential circuit architectures and guard rings can be used in conjunction.

Past implementations of active substrate noise cancellation systems report up to 40dB noise suppression in low frequency bands. However, noise suppression diminishes at higher frequencies because of the amplifier's bandwidth limitations. Figure 2-16 shows the typical shape of substrate noise suppression versus frequency. At low frequencies, substrate noise suppression is limited by circuit noise of the sensing circuit in the active feedback circuit. At higher frequencies, substrate noise suppression degrades as the amplifier's frequency response degrades.

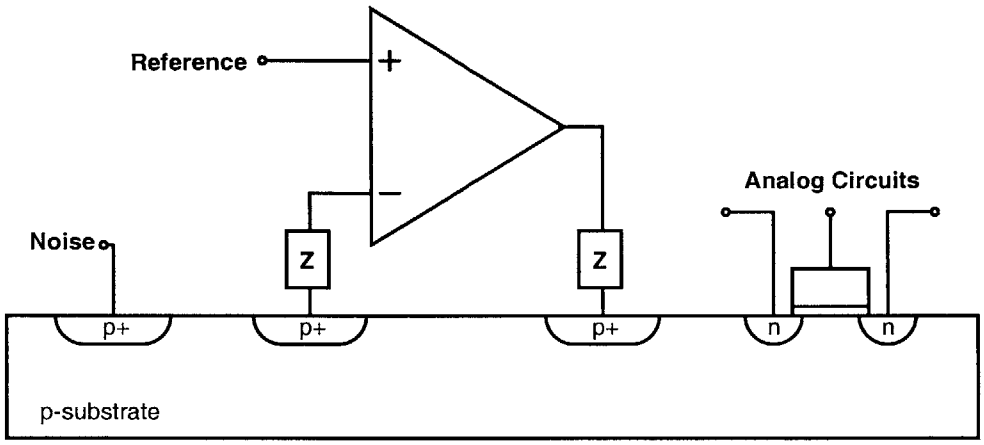


Figure 2-15: Implementation of a continuous time substrate noise cancellation circuit.

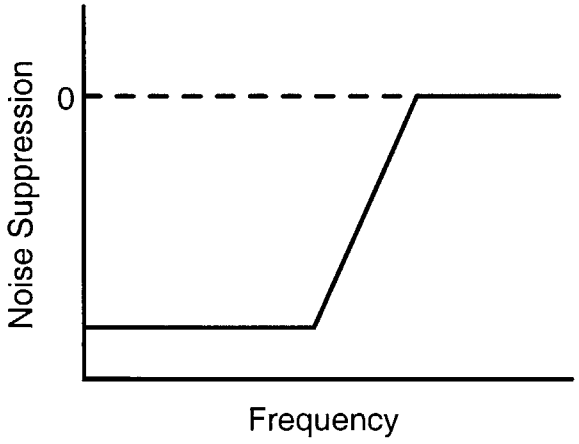


Figure 2-16: Typical noise suppression of continuous time active substrate noise cancellation systems versus frequency.

The main drawbacks of these active substrate noise cancellation systems is that they require a power hungry feedback amplifier. Since the substrate tends to be low impedance, the amplifier must consume much power to drive it. Moreover, the amplifier will consume power even if there is no substrate noise to cancel. This technique may be especially wasteful if the analog circuits such as switched capacitor filters, do not need continuous time substrate noise cancellation.

Furthermore, the limited bandwidth of the continuous time active substrate noise cancellation system is problematic for sampled data circuits. High frequencies unattenuated by the continuous time active substrate noise shaping system alias down and can appear as low frequency signals in the sampled data system. Since the sampled data system is intrinsically not a continuous time system, a mismatch exists between what the continuous time active substrate noise shaping system sees as substrate noise and what the sampled data system sees as substrate noise.

A last problem with active substrate noise cancellation systems is the associated resistivity of the substrate. The problem of driving the substrate becomes worse for low-resistivity substrates which are preferred by digital designers. Low-resistivity substrates such as that in an epitaxial process, have lower impedance from the substrate to the power supply than high-resistivity substrates, making it difficult to drive a signal into the substrate. The advantage of using low-resistivity substrates from an active substrate noise canceling perspective, however, is that spatial dependence of the substrate noise can be ignored because of the one-node approximation mentioned above. In contrast, spatial dependence of substrate noise cannot be ignored for high-resistivity substrates and must be accounted for when implementing active substrate noise cancellation.

2.6 Summary

This chapter has summarized the basic aspects of substrate noise and substrate noise coupling and past research: mechanisms, modeling, and past techniques for minimization.

Chapter 3

Study of Substrate Noise

One of the main thrusts of this research was to study the effect of substrate noise on analog circuits. A representative analog circuit, a switched capacitor delta-sigma modulator was chosen for the study of substrate noise. For a delta-sigma modulator, analysis of substrate noise effects could be confined to the first stage because noise entering later stages was shaped by the loop filter of the delta-sigma modulator. However, any conclusions about the nature of substrate noise coupling can be extended to switched capacitor circuits in general and even analog circuits in general because modes of substrate noise coupling are not delta-sigma modulator specific.

Analysis of substrate noise on the delta-sigma modulator as a representative analog circuit was based on the measured data from the output of the delta-sigma modulator in different configurations. The case with substrate noise was compared to the case without substrate noise so that an accurate picture of the effects could be made. Furthermore, the data from the delta-sigma modulator in different configurations with substrate noise present allowed conclusions to be made about the ways substrate noise affects delta-sigma modulators and analog circuits in general. This allowed prescriptions to be made for designing analog circuits that are less susceptible to substrate noise.

3.1 Substrate Noise Testing System

The substrate noise testing system was composed of two identical delta-sigma modulators (DS1 and DS2) and an array of 31 equally sized inverters with coupling capacitors (InvArrA) to the substrate. The components of the system, fabricated on a test chip in National Semiconductor's 0.25um CMOS process on an epitaxial wafer[1], are shown in Figure 3-1.

Each delta-sigma modulator can convert either an external off-chip analog signal or the substrate voltage, selectable through an analog multiplexer. When converting an external off-chip signal, an external differential signal is accepted and passed directly to the differential inputs of the delta-sigma modulator. When converting the substrate voltage, the

[1]The use of an epitaxial wafer means that the buried substrate layer is heavily doped and causes the entire to substrate to appear as one node as discussed in Section 2.5.5.

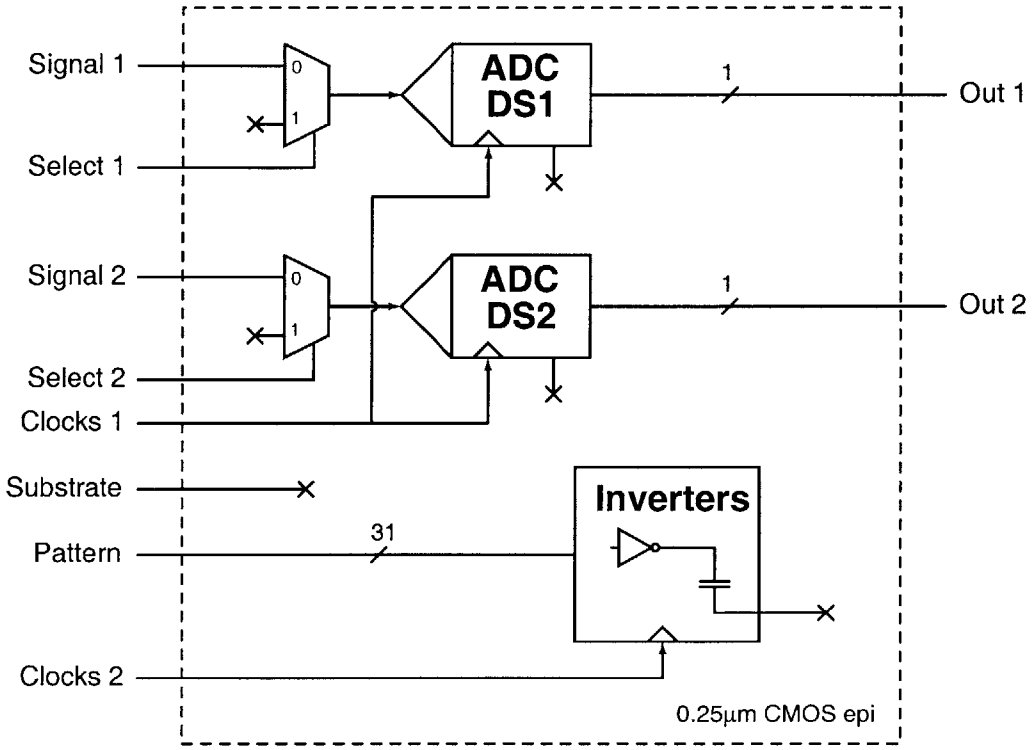


Figure 3-1: System components for studying the substrate noise and its effects on analog circuits.

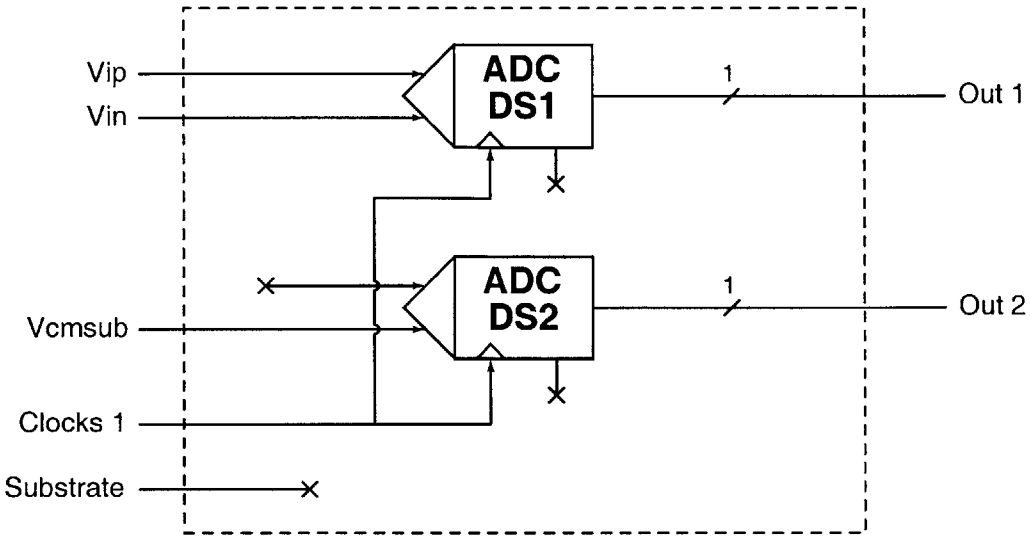


Figure 3-2: Configuration of delta-sigma modulators for studying substrate noise.

delta-sigma modulator's positive differential input is connected to the substrate, and the negative differential input is connected to an off-chip voltage reference.

For testing, one delta-sigma modulator (DS1) converted an external differential analog signal and the other delta-sigma modulator (DS2) converted the substrate voltage as shown in Figure 3-2. This configuration allowed the substrate noise, voltage fluctuations on the substrate voltage, and coupled substrate noise, voltage fluctuations appearing as an input signal to the delta-sigma modulator due to substrate noise coupling, to be characterized in DS2 and DS1, respectively. Although DS2 converts the substrate noise, it is also susceptible to coupled substrate noise like DS1. Therefore, the output of DS2 also has the effect of coupled substrate noise. However, since coupled substrate noise is much smaller than the magnitude of substrate noise itself, the DS2 output is dominated by substrate noise.

3.1.1 Clock Timing

Since substrate noise is a transient effect, the clock timing in the system is of paramount importance as shown in Figure 2-7. More specifically, the time between the rising edge of the digital clock, which triggers the digital circuits, and the sampling edge of the analog clock, needs to be carefully controlled to vary the amount of substrate noise and coupled substrate noise sampled by DS1 and DS2. Therefore, this design includes many independent and adjustable clocks which can be set at the board level as shown in Figure 3-3. This setup allows clock delay adjustments from zero to about 8ns. For convenience, the clock delay from the rising edge of the clock that controls InvArrA to the analog sampling edge of the delta-sigma modulators will be called DelayA from here on in. In addition, all clock phases and variants are generated and adjusted off-chip. This includes non-overlapping clocks,

Specification	Value
Voltage Supply	2.5V
Output	1-bit
Order	4
Resolution	96dB (16b)
Oversampling Ratio	128
Differential Full Scale Voltage	4V
Analog Sampling Frequency	5MHz
Band of Interest	0-20kHz

Table 3-1: Specifications for the delta-sigma modulator.

delayed non-overlapping clocks, and comparator clocks.

3.1.2 Sampling Scope

The substrate noise and coupled substrate noise time domain waveforms were characterized using the "sampling scope" technique [39] with the delta-sigma modulators [40].

The sampling scope concept is to manipulate the delay, T_d, between the analog sampling clock and the digital clock while taking successive data sets generated by delta-sigma modulators. This process is depicted in Figure 3-4.

For a fixed T_d, the delta-sigma modulator always samples the substrate noise or coupled substrate noise waveform at a fixed delay since the substrate noise and coupled substrate noise is triggered by the digital clock. If the substrate noise or coupled substrate noise waveform is periodic, then the average value of the delta-sigma modulator output will be the value of the substrate noise or coupled substrate noise waveform at T_d. The accuracy of the values depends on the number of averaged output samples. In other words, the filter used on the output will determine accuracy. Then, repeating this process of data gathering for different values of T_d, the substrate noise and coupled substrate noise waveform can be reconstructed. Since this technique uses a delta-sigma modulator, it has the advantages of the delta-sigma architecture including inherent signal averaging and linear performance. Note that this technique only works with periodic waveform inputs to the sampling scope.

With small enough time steps of T_d, the substrate noise and coupled substrate noise time domain waveform can be faithfully reconstructed and analyzed.

3.1.3 Delta-Sigma Modulator

The delta-sigma modulator for this research was chosen to be a low-pass one-bit oversampling delta-sigma modulator because it was simple to design, making implementation straightforward. Since the goal of this research is not breakthrough performance nor power optimization, conservative and achievable specifications, listed in Table 3-1, were chosen.

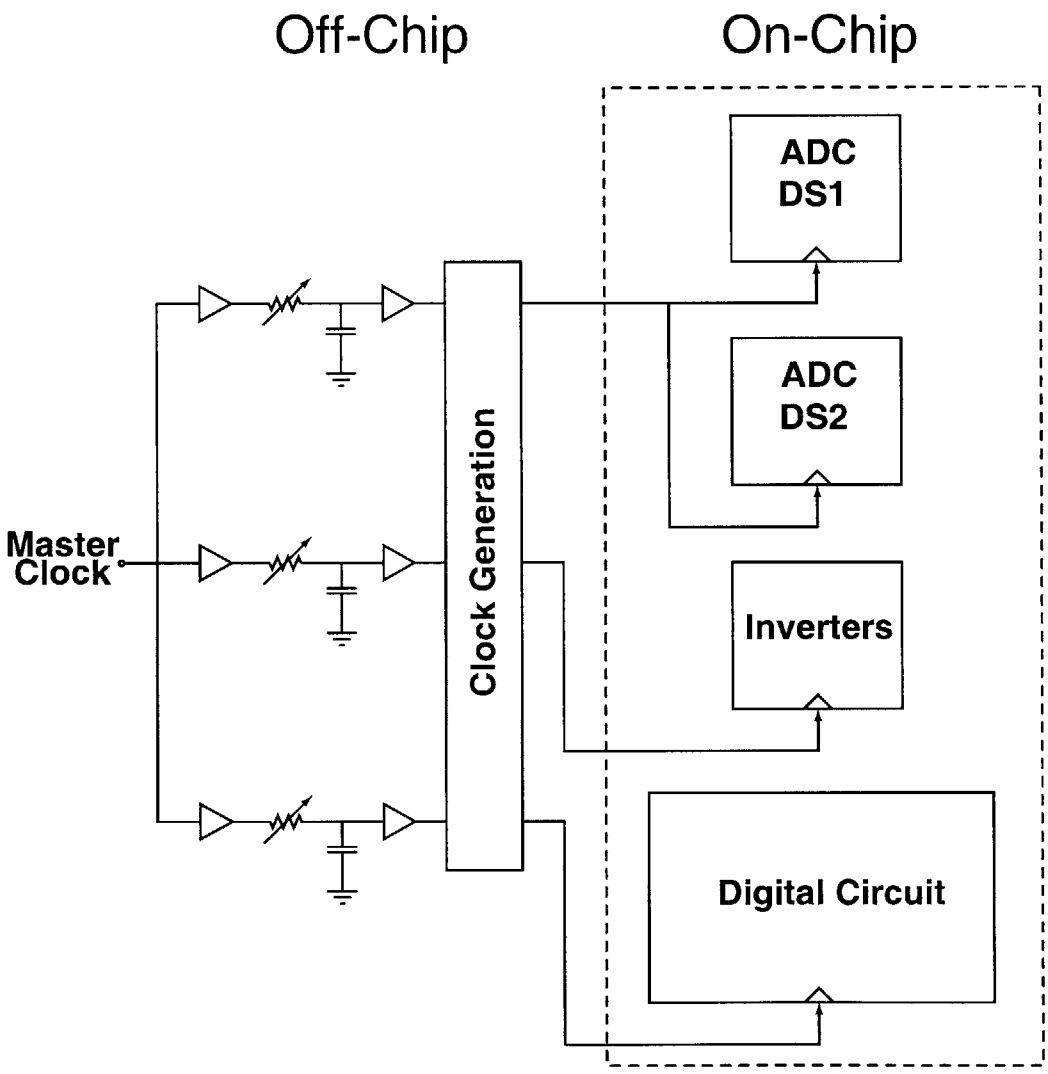


Figure 3-3: Clocks to each block in the system are generated and independently set off-chip.

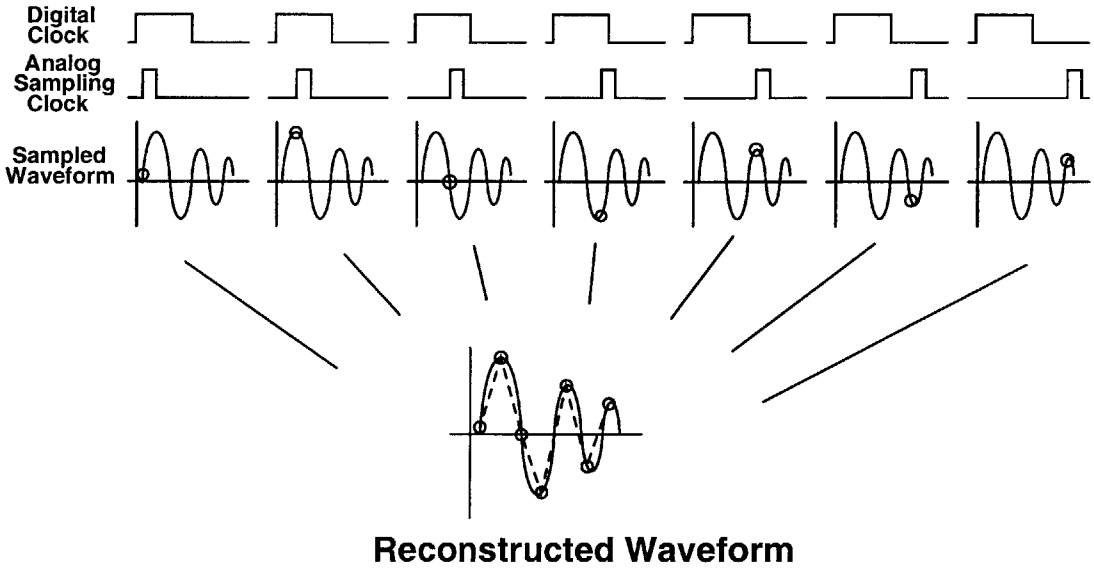


Figure 3-4: Illustration of the "sampling scope." The circles on the sampled waveform represent the value sampled by the analog circuits.

For this research, a delta-sigma modulator synthesis tool [41], utilizing the Delta-Sigma Toolbox for Matlab [42], was used to generate a basic design. Refinements to the synthesized design were then made (*e.g.* larger input sampling capacitors) and additional circuitry (*e.g.* chopping) was added to improve and complete the modulator design. The complete delta-sigma modulator design is discussed in the following sections.

The theory of delta-sigma modulators is not discussed here, but detailed explanations can be found in the following references [33] [43].

3.1.3.1 Architecture

The architecture chosen for the low pass delta-sigma modulator was the Cascade of Integrators with Feedback (CIFB) shown in Figure 3-5 [33, pp. 179-180]. This structure has input feedforward, as well as feedback, to every stage. This allowed the signal transfer function (STF) to be set independently of the noise transfer function (NTF) [33, p.179]. In addition, the signal transfer function had unity gain across the entire spectrum.

Based on behavioral simulations, it was determined a fourth order version of the CIFB was necessary to achieve the specified signal-to-noise-ratio (SNR). A fourth order noise transfer function and signal transfer function were generated by the Delta-Sigma Toolbox [42].

Figure 3-6 shows the magnitude bode plots for the generated STF and NTF for this delta-sigma modulator. In normalized frequency where unity maps to the sampling frequency, the band of interest is 0 to 0.0039. The figure shows that the input signal is unattenuated

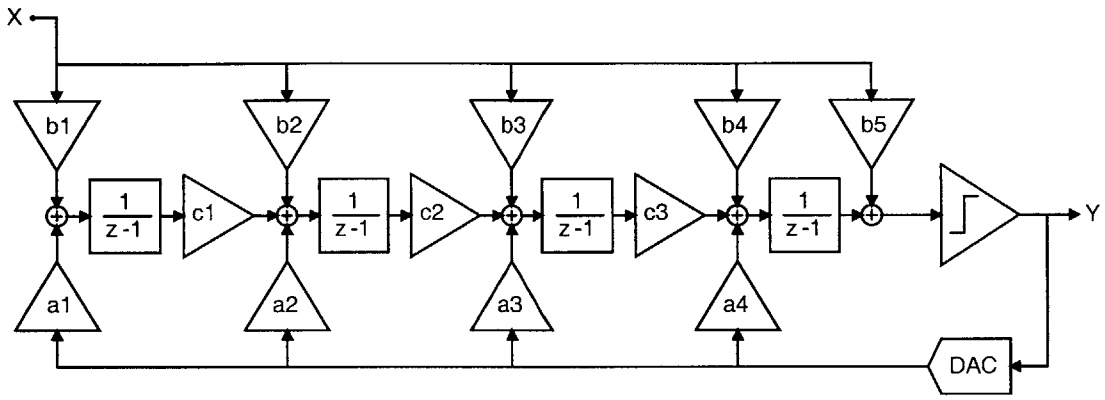


Figure 3-5: Block diagram of the CIFB structure for delta-sigma modulators.

by the STF in the band of interest and quantization noise will be greatly attenuated at low frequencies by the NTF. According to the bode plot shown in Figure 3-6(b), the NTF will provide at least 85dB of quantization noise attenuation across the band of interest. Combined with 1 bit quantization noise which is more than 30dB below full scale[2], an SNR of at least 105dB for a full scale input[3] (more than 16 bits) is possible.

Figure 3-7 shows the pole-zero diagram for the NTF in the z-plane. Four zeros are coincident on the point $(0, 1)$ of the unit circle which gives rise to the large amount of quantization noise attenuation at low frequencies. More noise attenuation could have been achieved if the four zeros were spread across the band of interest instead of being coincident at the origin. However, implementing this would have required resonators instead of simple integrators. For simplicity, the four NTF zeros were placed on the point $(0, 1)$ since delta-sigma modulator performance is not the main goal.

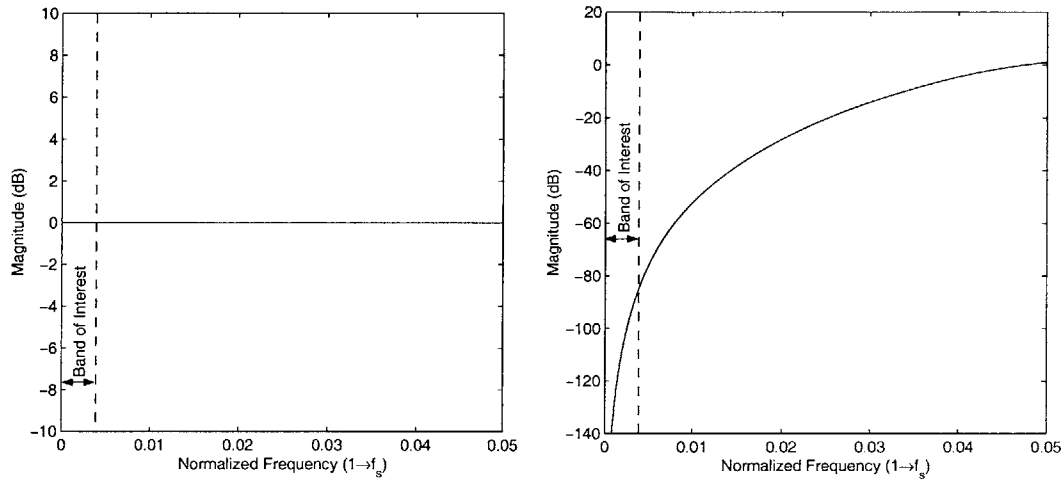
A behavioral model of the delta-sigma modulator was built in Matlab's Simulink [44]. The basic block diagram with discrete time blocks is shown in Figure 3-8. The coefficients and values shown are the ones produced by the Delta-Sigma Toolbox [42].

The Simulink simulations with this model yielded a maximum SNR–quantization noise only–of over 119dB for a half of full scale sine wave input. Larger input amplitudes created instability in the modulator and thus caused SNR to decline. The relationship between SNR and input amplitude for this modulator, determined with data from behavioral simulations, is shown in Figure 3-9.

The delta-sigma modulator is very robust and very tolerant of non-idealities such as finite operational amplifier gain, mismatch, etc. In behavioral simulations with coefficient rounding of 0.1%, a DC operational amplifier gain of 5000 and operational amplifier output

[2] $V_{Q(rms)} = \frac{V_{LSB}}{(\sqrt{12})(\sqrt{OSR})} = \frac{1}{(\sqrt{12})(\sqrt{128})} = -31.9dB$

[3] "Full scale input" means an input sine with a peak-to-peak magnitude equal to the reference voltage. For example, if the reference is 4V differential, then a full scale input would be a sine wave that has a 4V differential peak-to-peak amplitude.



(a) (b)

Figure 3-6: Bode plots of the (a) STF and (b) NTF.

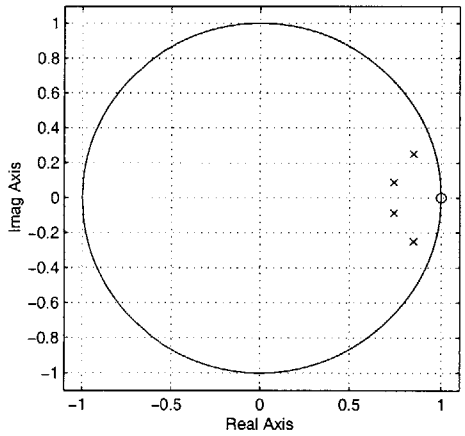


Figure 3-7: z-plane pole-zero diagram of the delta-sigma modulator's NTF. The 4 zeros in the NTF are coincident.

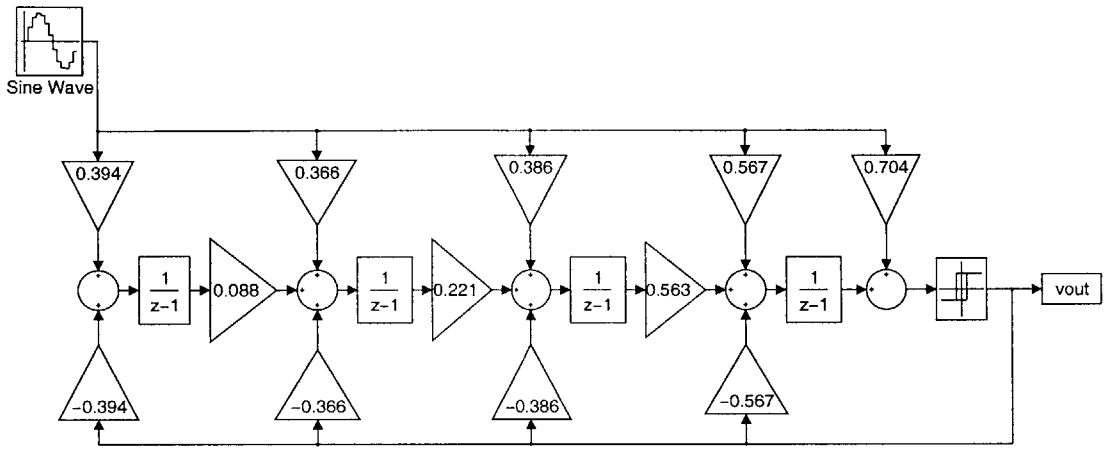


Figure 3-8: Simulink basic model of the delta-sigma modulator. The coefficients shown are scaled for maximum dynamic range.

limiting, the SNR curve shown in Figure 3-9 was hardly affected. A peak SNR of over 118 dB was still achieved.

3.1.3.2 Circuit Implementation

The circuit implementation of this delta-sigma modulator was chosen to be differential to maximize robustness of the circuit [33, p. 335].

A full circuit schematic of the delta-sigma modulator is shown in Figure 3-10 with clocking in one differential path labeled. The other differential path has the same clocking unless otherwise noted.

As shown in the block diagram of Figure 3-5, the input to the comparator is the addition of the output of the fourth stage integrator and the input signal attenuated by b_5. Although there are many ways to realize this, the most straightforward implementation of using the fourth stage operational amplifier also as a gain stage was chosen. In Figure 3-10, the last stage operational amplifier, $OA4$, is used in a discrete time integration configuration with the charge sampled on capacitors C_{41}, C_{42}, and C_{44} integrated onto feedback capacitor C_{43}. In addition, capacitor C_{45}, is connected directly to the summing input of $OA4$, thereby implementing an amplifier with the gain determined by the ratio C_{45}/C_{43}. By superposition, the resulting outputs of these two functions sum, thereby achieving the necessary continuous time addition.

The comparator in the delta-sigma modulator evaluates its input during the non-overlap period between $\Phi 1$ and $\Phi 2$ so that a stable value can be ensured during $\Phi 1$.

The capacitor sizes in the circuit were determined by a minimum capacitor size in each stage and the capacitor ratios needed to implement the scaled coefficients shown in Figure 3-8. The minimum capacitor size for the second, third, and fourth stages is 100fF to ensure

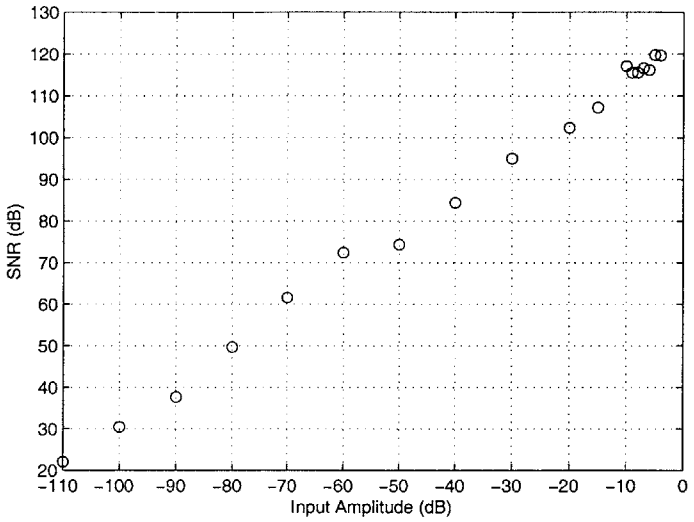


Figure 3-9: Simulated SNR vs. input amplitude curve.

reasonable differential matching. The minimum capacitor size for the first stage, 6pF, is much larger because of noise requirements as explained in Section 3.1.3.9. The values of all the capacitors used in the delta-sigma modulator are shown in Table 3-2. They correspond to the capacitors shown in the circuit schematic of Figure 3-10.

The capacitors were realized with poly-to-poly capacitors. Since the capacitor ratios called for by the coefficients are non-integers, both unit size and non-unit size capacitors are used. The unit size capacitors are square and the non-unit size capacitors are rectangular. The dimensions of the rectangles were determined by the constraint that all capacitors preserve perimeter to area ratios which ensures that processing variations such as etching undercut minimally affect capacitor ratios. This technique is explained in Johns and Martin [43, pp. 108-111]. Additionally, the capacitors were physically shielded on top with grounded metal sheets in the highest metal level to prevent any stray coupling from above the chip that could adversely impact signals on the capacitors. However, the capacitors were not shielded from the substrate which was directly below the capacitors. This was done to allow substrate noise a path to couple into the analog circuit so that it could be observed.

The delta-sigma modulator requires four operational amplifiers to implement the four integrators. For simplicity in design and layout, only two operational amplifier sizes are used. Both are scaled up versions of a base operational amplifier design discussed in Section 3.1.3.3. The scaling methodology of the operational amplifiers preserves current densities and increases capacitor sizes so that important characteristics of the operational amplifier do not change with scaling factor [41].

The larger operational amplifier design is used in only the first stage of the delta-sigma modulator. It was designed to be 100 times larger than the base operational amplifier design

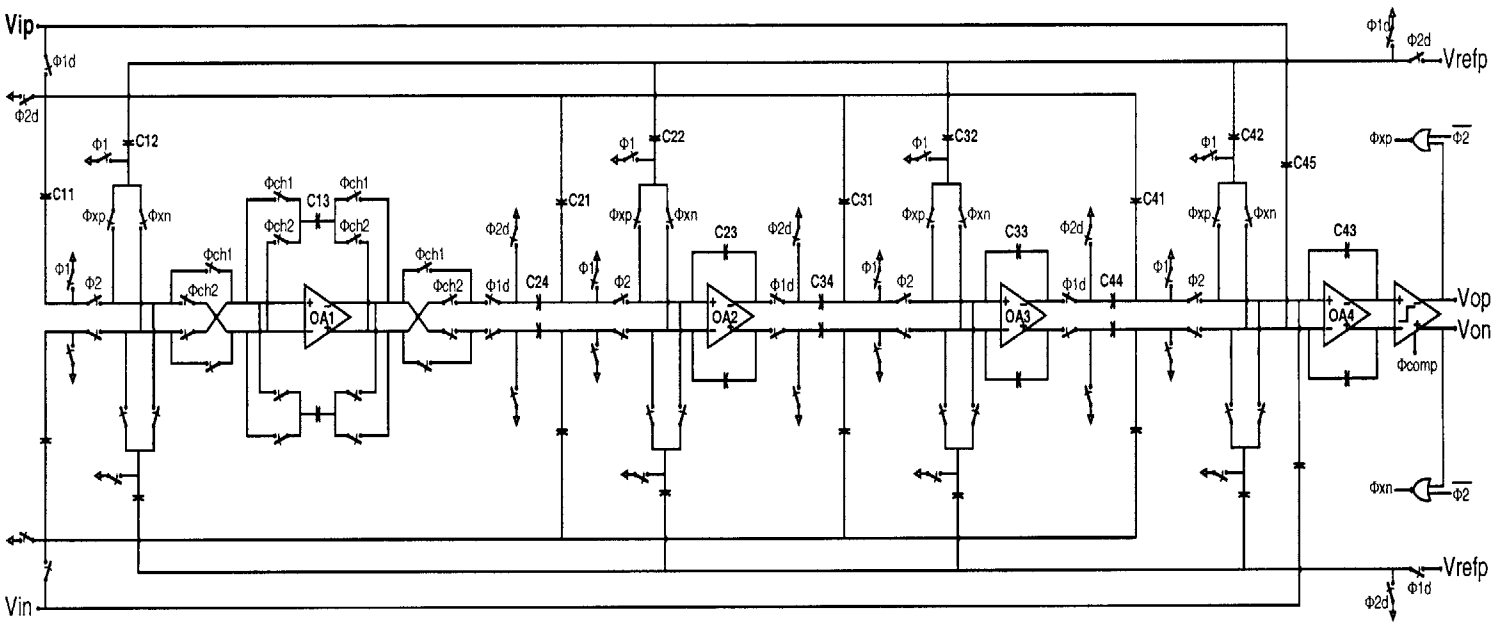


Figure 3-10: Circuit schematic of the delta-sigma modulator. Clocks and component names are differentially symmetric unless otherwise indicated.

Stage	C_{n1}	C_{n2}	C_{n3}	C_{n4}	C_{n5}
$n = 1$	6000	6000	15227	–	–
$n = 2$	415	415	1140	100	–
$n = 3$	174	174	452	100	–
$n = 4$	101	101	178	100	125

Table 3-2: Delta-sigma modulator capacitor sizes in fF. Capacitor names correspond to the ones in Figure 3-10.

so that it could meet the delta-sigma modulator noise requirements and settling constraints since it is driving the large capacitors of the first stage of the delta-sigma modulator.

The smaller operational amplifier design, ten times larger than the base operational amplifier design, was used in the second, third and fourth stages. This design satisfied settling requirements of these stages by a large margin as verified by simulation.

3.1.3.3 Operational Amplifier Design

The fully differential operational amplifiers used in this design are based on the traditional 2-stage operational amplifier with Miller Compensation. They are all scaled versions of a base operational amplifier design with a load capacitance of 100fF. Scaling is based on the load capacitance. Currents, transistor widths, and capacitor sizes were each scaled by the ratio between the load capacitance to be driven and the load capacitance of the base operational amplifier design. This scaling results in preservation of all key operational amplifier characteristics since the ratio of current densities and capacitor values remains constant [41]. As a result, only the base operational amplifier design is discussed here since it generalizes to scaled versions. The schematic of the base operational amplifier is shown in Figure 3-11.

The base operational amplifier was designed to have low noise, high slew rate, and low power. The active load (NMOS) in the first stage was found to have large $1/f$ noise and was thus designed to have a large area which reduced $1/f$ noise. In addition, the input stage uses PMOS transistors which have relatively low $1/f$ noise. The currents in each stage are large enough so that they can drive the capacitors (compensation and load) and settle within the allotted time in the worst case (*i.e.* a 4V differential step). Slew rate was designed to be high so that nonlinear settling would be minimized.

3.1.3.3.1 Base Operational Amplifier Performance The performance of the base operational amplifier, based on simulations, is summarized in Table 3-3. The simulations were done with the slow corner models of the process to ensure acceptable performance under worst case scenarios.

3.1.3.3.2 Common Mode Feedback Circuit Since the operational amplifier is fully differential, a common mode feedback circuit (CMFB) is needed to center the differential

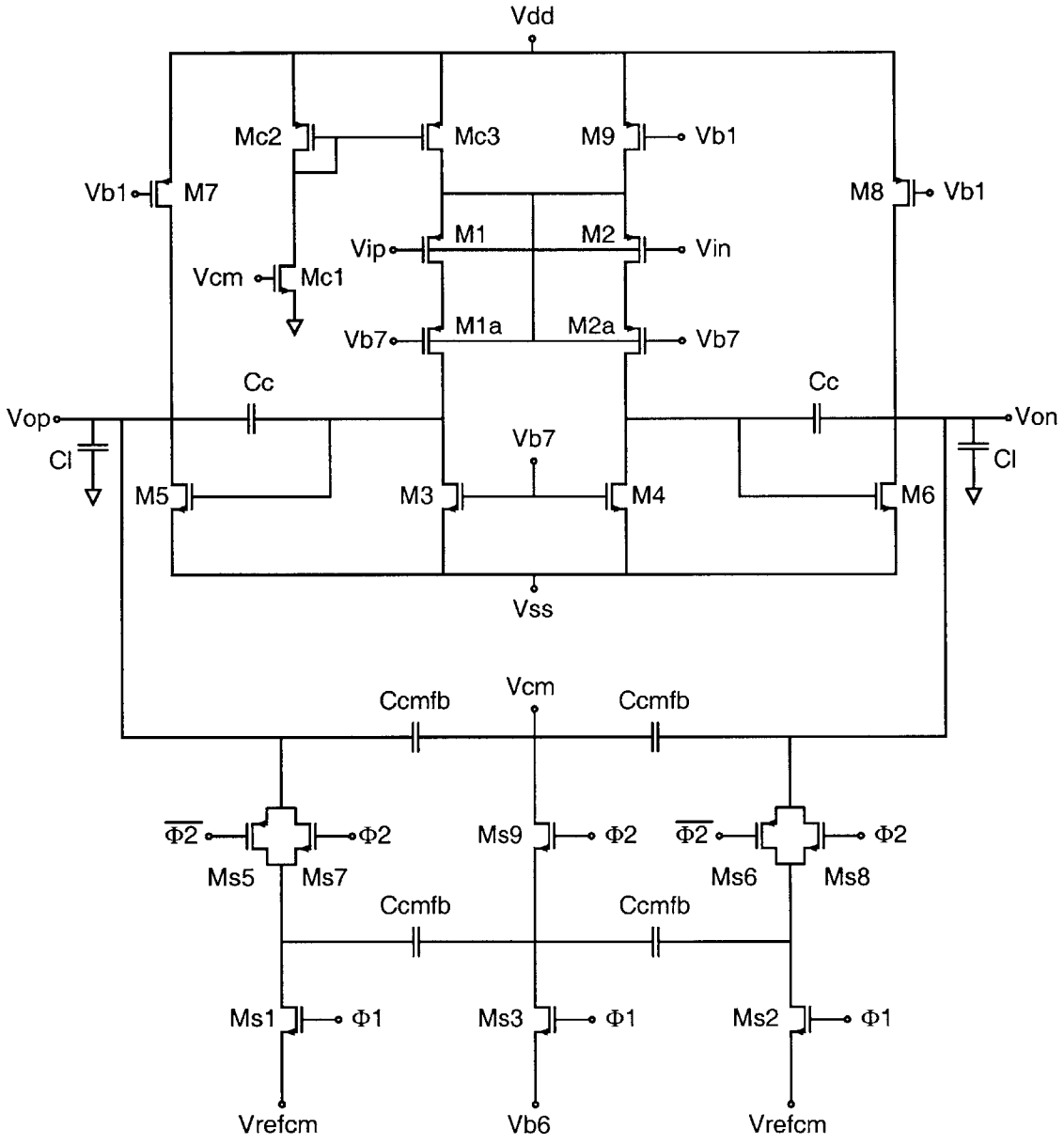


Figure 3-11: Circuit schematic of the base size operational amplifier.

Characteristic	Value	Units
DC Gain (Vout=0)	14,000	
Output Range (Gain > 10,000)	0.25-2.25	V
Unity-Gain Frequency	85	MHz
Phase Margin	49	Degrees
Slew Rate (calculated)	125	V/μs
0.1 % Settling (4V diff step)	42	ns
0.01 % Settling (4V diff step)	57	ns
Power (standby)	156	μW

Table 3-3: Simulated base operational amplifier design performance summary for the slow process corner.

output for maximum dynamic range. The circuit is based on a switched capacitor implementation [45], as shown at the bottom of Figure 3-11. The clocks indicated in Figure 3-11 correspond to the clocks used in the delta-sigma modulator shown in Figure 3-10.

The CMFB compares the common mode output of the operational amplifier to an adjustable reference, V_{refcm}, and adjusts the amount of current in the first stage of the operational amplifier. It controls about 20% of the operational amplifier first stage current. In steady state, the common mode output deviates by less than 10mV due to charge injection effects on the switched capacitors of this CMFB.

The CMFB, unlike the rest of the operational amplifier, was not scaled for larger designs. In other words, an operational amplifier scaled up by a factor of 100 had the same CMFB circuit with the same switch and capacitor sizes. This has the effect of slowing down common mode settling because the same amount of charge from the CMFB must charge a larger transistor input capacitance (*i.e.* the input capacitance of M_{c1}). However, since common mode response does not need to be fast, this was not a problem and the CMFB circuit was not scaled up in order to save chip area and power.

3.1.3.3.3 Base Operational Amplifier Spectral Noise Power Density The operational amplifier noise, a contributor to the overall noise of the delta-sigma modulator, for the base operational amplifier design was calculated. This section shows calculations of spectral noise power density based on standard noise models [43] and nominal operational amplifier performance. Only the main sources of operational amplifier noise, thermal noise and $1/f$ noise, were considered [43, p. 200]. These calculations can easily be used for scaled designs because spectral noise power scales inversely with the scaling used for the operational amplifiers (*i.e.* increasing current, transistor widths, and capacitor sizes by the same factor). All calculations are for noise seen differentially.

The input-referred spectral thermal noise power density of the first stage of the base operational amplifier in which the first stage input transistors and active load transistors contribute noise is (the cascode transistors contribute a negligible amount of noise when

input-referred because the cascode transistors do not affect the currents in the first stage much):

$$\begin{aligned} S_{i,oab1,th}(f) &= \left(2\left(\frac{8}{3}kT\right)\left[\frac{1}{g_{m1}} + \left(\frac{g_{m3}}{g_{m1}}\right)^2\left(\frac{1}{g_{m3}}\right)\right]\right) \\ &= \left(25.7\frac{nV}{\sqrt{Hz}}\right)^2 \end{aligned} \tag{3.1}$$

where the subscripts of the parameters correspond to the transistors in Figure 3-11. Note that the extra factor of 2 for the spectral noise power density of the thermal noise in the first stage comes from the fact that a differential implementation is used. The two sides of the differential circuit are assumed to have uncorrelated thermal noise.

The input referred spectral $1/f$ noise power density of the first stage of this operational amplifier is[4]:

$$S_{i,oab1,1/f}(f) = 2\left[\frac{K_p}{f} + \left(\frac{g_{m3}}{g_{m1}}\right)^2\left(\frac{K_n}{f}\right)\right] \tag{3.2}$$

The input referred spectral thermal noise power density of the second stage of the operational amplifier is shown in Figure 3-12. The spectral noise power density of the second stage is divided by the square of the first stage gain when referred to the input of the operational amplifier. The first stage gain is frequency dependent. At low frequencies, the first stage gain is:

$$A_{v,1,low} = g_{m1}R_{o1} \tag{3.3}$$

where g_{m1} is the transconductance of M_1 in Figure 3-11 and R_{o1} is the output resistance of the first stage. At high frequencies, the Miller capacitor, C_c, acts like a short circuit, reducing the output resistance of the first stage. Thus the first stage gain at high frequencies is:

$$A_{v,1,high} = \frac{g_{m1}}{g_{m5}} \tag{3.4}$$

where g_{m5} is the transconductance of M_5. The first stage gain starts to decrease from the low frequency gain, $A_{v,1,low}$, at the dominant pole:

$$p_1 = \frac{1}{g_{m5}R_{o2}R_{o1}C_c} \tag{3.5}$$

where R_{02} is the output resistance of the second stage. The spectral thermal noise power density at the input of the second stage of the operational amplifier (a similar calculation

[4]The form for the $1/f$ noise in a MOSFET is $S_{1/f}(f) = \frac{K}{WLC_{ox}f}$ [43, p. 199]. The K's for NMOS and PMOS transistors were extracted from measured data of devices with the closest geometries and bias levels to those used in the design.

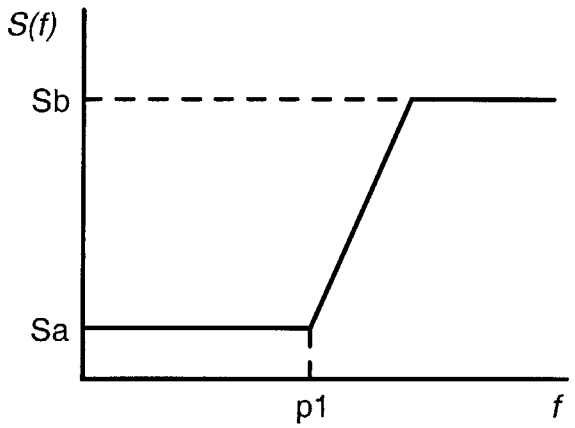


Figure 3-12: Spectral power density of the input-referred thermal noise from the second stage of the operational amplifier. The quantities, S_a, S_b and p_1 are defined in the text.

to the first stage) is:

$$S_{oab2,th}(f) = 2\left(\frac{8}{3}kT\right)\left[\frac{1}{g_{m5}} + \left(\frac{g_{m7}}{g_{m5}}\right)^2\left(\frac{1}{g_{m7}}\right)\right] \tag{3.6}$$

The result of referring the second stage spectral thermal noise power density to the input of the operational amplifier is shown in Figure 3-12, where $S_a = S_{oab2,th}(0)/(A_{v,1,low})^2$ and $S_b = S_{oab2,th}(0)/(A_{v,1,high})^2$. The spectral power thermal noise power density shown in Figure 3-12 is $S_{i,oab2,th}(f)$.

The spectral $1/f$ noise power density of the second stage of the operational amplifier is:

$$S_{oab2,1/f}(f) = 2\left[\frac{K_p}{f} + \left(\frac{g_{m7}}{g_{m5}}\right)^2\left(\frac{K_n}{f}\right)\right] \tag{3.7}$$

This power density is also divided by the first stage gain when referring it to the input of the operational amplifier. Since most of this power density is at low frequencies where it is divided by the low frequency gain of the first stage, its noise contribution is small and ignored.

Thus, the total input referred spectral noise power density in the base operational amplifier is:

$$S_{i,oab}(f) = S_{i,oab1,th}(f) + S_{i,oab2,th}(f) + S_{i,oab1,1/f}(f) \tag{3.8}$$

3.1.3.4 Bias Circuits

All the bias voltages for the operational amplifiers are derived from a current that is fed into the chip from an off-chip, adjustable current source. Figure 3-13 shows the simple bias

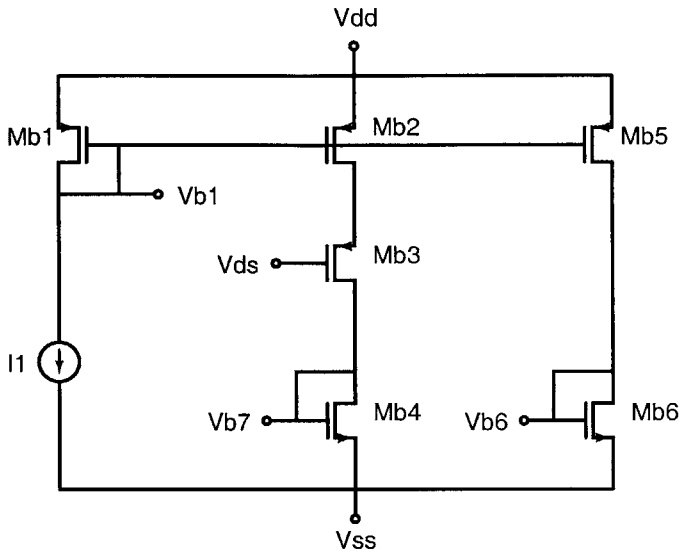


Figure 3-13: Bias circuit for operational amplifier. V_{ds} is the voltage halfway between V_{dd} and V_{ss}.

circuits used. The created bias voltages are referenced to the supply rails so that voltage supplies could be varied without affecting the biases. In addition, all transistors that share the same bias voltage (*e.g.* M_{b1} and M_{b2}) had the same transistor geometries to ensure good current matching. If currents, derived from the same bias voltage, needed to be scaled (*e.g.* M_{b1} and M_7 in Figure 3-11), then the number of transistor fingers was adjusted to ensure current scaling by the desired amount.

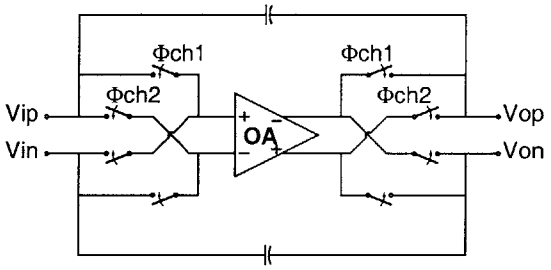
Since all the operational amplifiers are derived from a base operational amplifier design, they, in theory could have shared the same biases. However, for isolation and better matching, 2 bias circuits are used. One, with larger currents, is used exclusively to bias the large operational amplifier of the first stage of the delta-sigma modulator where noise performance is critical. Another bias circuit, with smaller currents, is shared among the three smaller operational amplifiers of the second, third, and fourth stage.

All other bias voltages for the delta-sigma itself, are generated off-chip. These include input common mode voltages, reference voltages, etc.

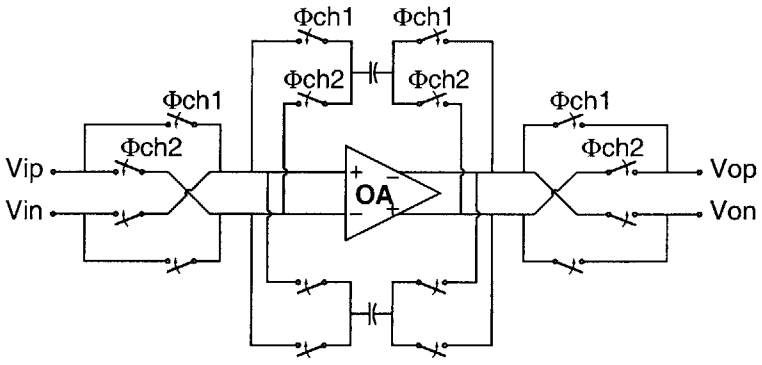
3.1.3.5 Chopping

Chopping, shown in Figure 3-14, was designed into the system to minimize $1/f$ noise of the operational amplifier in case it was a problem. It is only used in the first stage since its noise contribution is large in the delta-sigma modulator.

By chopping (swapping the nominally symmetric differential paths) the operational amplifier of the first stage at a certain frequency, f_{chop}, low frequency noise components



(a)



(b)

Figure 3-14: Chopping schemes. (a) conventional chopping (b) variant chopping [46].

(*e.g.* $1/f$ noise, DC offset, etc.) of the operational amplifier are modulated up to f_{chop} and removed from the band of interest.

The conventional chopping scheme is shown in Figure 3-14(a). However, a variant, shown in Figure 3-14(b) is used because it has advantages over the conventional scheme [46, pp. 65–67]: faster settling response and lower noise. Both these advantages come from the fact that the chopping switches are not in series with the operational amplifier inputs. On the other hand, this scheme has more complexity because four extra switches are needed for implementation in comparison to the conventional scheme.

Functionally, the variant chopping scheme is the same as the conventional. Instead of swapping the differential paths of the operational amplifier at the chopping frequency, the differential paths of the network around the operational amplifier are swapped at the chopping frequency.

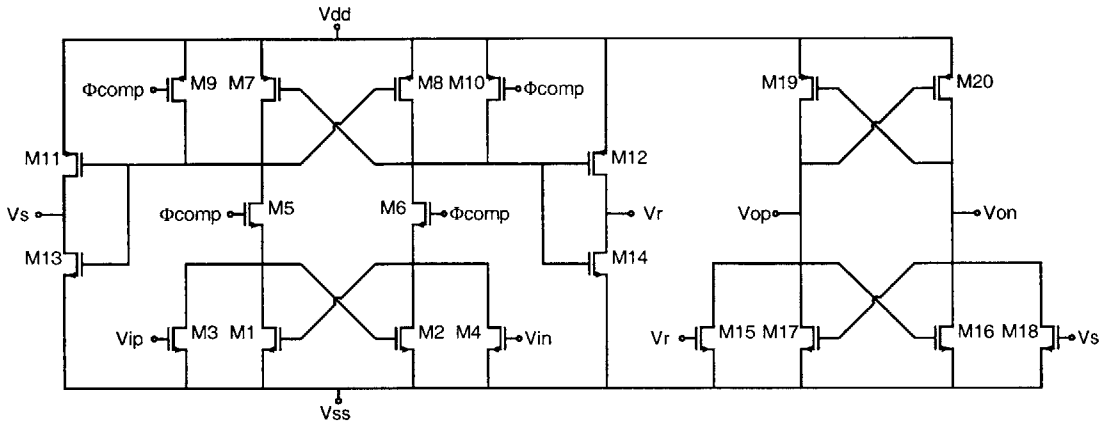


Figure 3-15: Schematic of the comparator used in the delta-sigma modulator.

3.1.3.6 Comparator Design

The comparator used for this delta-sigma modulator is based on a cross-coupled, clocked latch [47]. The schematic of the comparator is shown in Figure 3-15.

The comparator operates by forcing its cross-coupled latch into a metastable state when Φ_{comp} is low and then switching its output based on the comparator inputs when Φ_{comp} goes high. The outputs of the latch are buffered by inverters and then fed into an SR latch. The SR latch, a memory element, holds the output value while the comparator is reset for the next comparison.

Simulations under worst case conditions (capacitive load equal to the switches it must drive as shown in Figure 3-10 and slow corner of process), the comparator differential output fully latches within two nanoseconds for differential input overdrive of 10mV.

The comparator is laid out as symmetrically as possible to minimize mismatch effects. However, any non-idealities such as input voltage offset and hysteresis are not significant because they are shaped by the fourth order loop filter of the delta-sigma modulator.

3.1.3.7 Digital-to-Analog Converter (DAC) Design

The one bit DAC, shown in Figure 3-16, is based on a previous design by Ferguson *et al.* [33, p. 359]. This DAC avoids charge delivery non-idealities which can lead to distortion in the delta-sigma modulator.

The conventional, simple DAC implementation, shown in Figure 3-16(a), selects the positive or negative reference voltage, V_{refp} or V_{refn}, to charge the sampling capacitors, C_{a2p} and C_{a2n} based on the comparator output. In the presence of capacitor mismatch between C_{a2p} and C_{a2n} in Figure 3-16, the charge delivered to the positive summing node by C_{a2p} when charged by V_{refp} is different from the amount of charge delivered to the negative summing node by C_{a2n} charged by V_{refp}. The same is true when the capacitors are charged by V_{refn}. This effect results in distortion as the charge delivered is data-

dependent. A better implementation, shown in Figure 3-16(b), avoids this problem. The sampling capacitors, C_{b2p} and C_{b2n} are always charged by the same reference voltage and thus the positive and reference charge amounts are always the same. The comparator then decides which summing junctions get the positive and negative reference charge packets. Thus, a positive reference charge packet will always deliver the same amount of charge to either the positive or negative summing junction. Although this DAC is more complicated, it results in more linear performance which is needed for high resolution. In addition, only a single reference voltage is needed.

3.1.3.8 Switches

The switches used in the delta-sigma modulator are implemented with transmission gates: an NMOS and PMOS connected in parallel. This allows for full scale operation and relatively constant on-resistance without using special techniques such as bootstrapping [27, pp. 213–214]. The PMOS and NMOS have the same widths and lengths to ease layout.

For all switch sizes, the minimum transistor length is used to minimize charge injection and on-resistance. For the smallest switch, the minimum transistor width is not used because of narrow width effects. The width of the transistor determines switch on-resistance and thus a minimum width transistor that is most affected by narrow width effects will have on-resistances that can vary greatly. This on-resistance variation leads to mismatches in the differential paths and deviations from designed bandwidths.

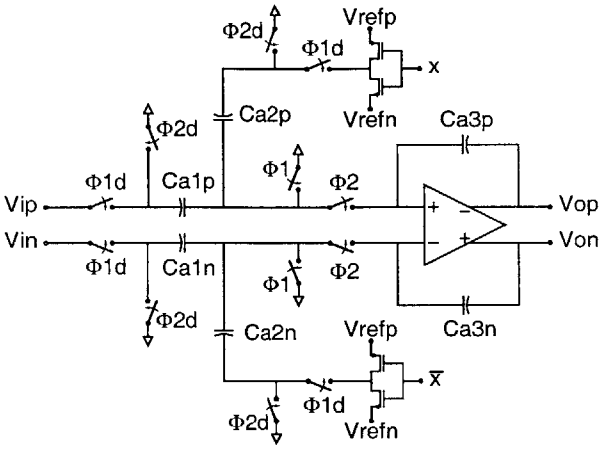
A conservative methodology was used to choose the appropriate switch sizes for each switch shown in the schematic of Figure 3-10. To be certain that settling would not affect the delta-sigma modulator resolution, switch sizes were calculated by computing the on-resistance needed to settle each respective capacitor to 100dB accuracy in half a clock cycle, in response to a full-scale step input. On-resistances of the switches were extracted from extensive simulations in SPICE.

In retrospect, this methodology may have been too conservative, especially for the input sampling switches of the first stage. The inputs never receive a full-scale step input because the input signal is bandlimited to audio frequencies by specification. However, having such a high bandwidth for the input sampling switch ensures gain flatness from the input signal from to the output signal over the band of interest.

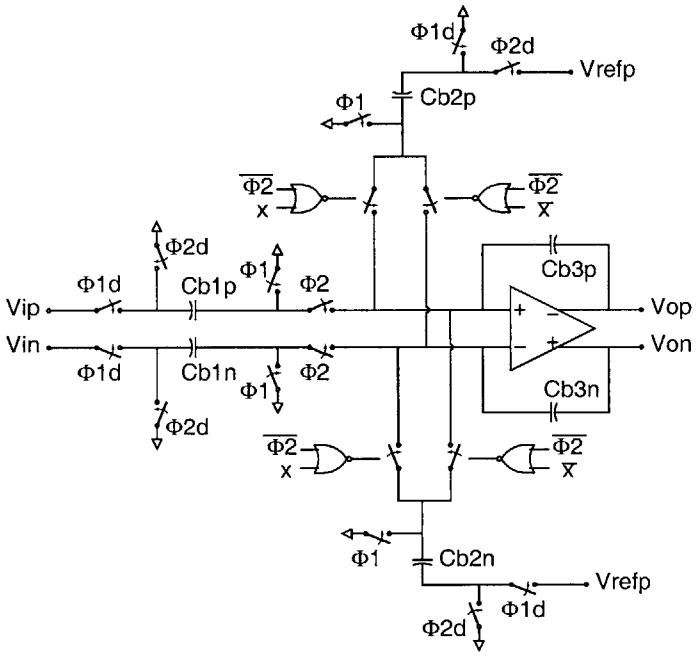
3.1.3.9 Delta-Sigma Modulator Noise Analysis

Noise calculations for the delta-sigma modulator were performed to help in design (*e.g.* sizing of input sampling capacitors) and to verify the 16-bit SNR goal. Since the delta-sigma modulator is a low pass design, only noise contributions for the first stage were considered. Noise from later stages are attenuated by the loop filter and are not significant. The first stage of the delta-sigma modulator is shown in Figure 3-17. All calculations are for noise seen differentially. Hence, many equations include an extra factor of 2.

The input sampling capacitors, $C11p$ and $C12p$ in Figure 3-17, both contribute kT/C noise directly to the delta-sigma modulator input. They are both sized at 6000fF to make



(a)



(b)

Figure 3-16: DACs for a delta-sigma modulator. The signal x represents the output of the comparator of the delta-sigma modulator. (a) simple implementation (b) better implementation.

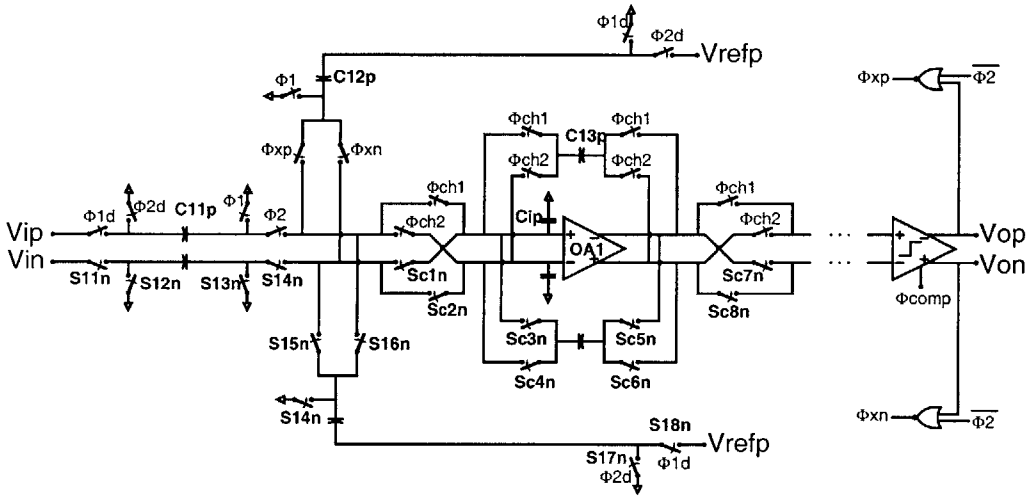


Figure 3-17: Circuit schematic of the first stage of the delta-sigma modulator for noise calculations. Clocking is differentially symmetric unless otherwise noted. Naming of components is also differentially symmetric except with the last character an n for components in the lower differential circuit and p for components in the upper differential circuit. C_{ip} and its differential counterpart are the parasitic input capacitances of the operational amplifier.

their noise contributions low. The amount of noise power they contribute is:

$$\begin{aligned} N_{i,ds,sampcap} &= 2 * 2 \left[\left(\frac{kT}{C_{11p}} \right) + \left(\frac{kT}{C_{12p}} \right) \right] \\ &= (74\mu V)^2 \end{aligned} \tag{3.9}$$

The two factors of 2 come from the fact that the circuit is differential and the fact that there are two phases in each clock period. In other words, both sides of the differential path sample uncorrelated thermal noise twice a clock cycle [33, p. 354].

The operational amplifier of the first stage also contributes noise to the delta-sigma modulator. Since the operational amplifier, $OA1$, is 100 times the base operational amplifier design, its spectral noise power density is divided by 100. Using Equation 3.8, the input referred spectral noise power density of $OA1$ is:

$$S_{i,oa100}(f) = S_{i,oab}(f)/100 \tag{3.10}$$

Both thermal and $1/f$ noise power density scale by the same factor because both the thermal and $1/f$ noise power density of the operational amplifier decrease linearly with transistor width increase.

To get the total noise power at the output of the operational amplifier, $S_{i,oa100}(f)$, must be multiplied by the closed loop frequency response of the operational amplifier, $A_{cl}(f)$, in

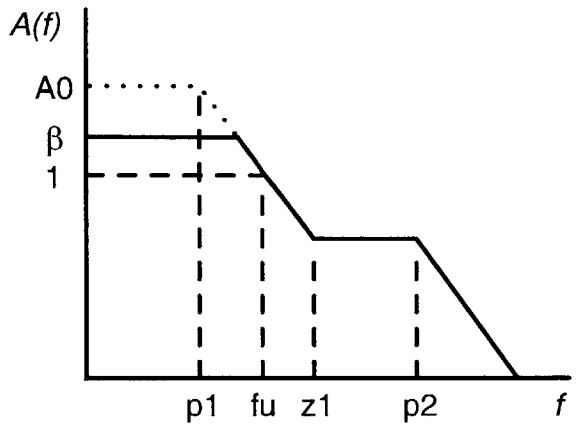


Figure 3-18: Open loop frequency response (dotted line) and closed loop frequency response, $A_{cl}(f)$ (solid line) of the operational amplifier, $OA1$. The quantities, p_1, z_1, p_2, f_u, A_0, and β are defined in the text.

the configuration shown in Figure 3-17. The open loop frequency response, (dotted line), and closed loop frequency response (solid line), $A_{cl}(f)$, is shown in Figure 3-18. A_0 is the open loop DC gain of the operational amplifier. p_1 is the dominant pole as calculated in Equation 3.5, $z_1 = g_{m5}/C_c$ is the zero and $p_2 = g_{m5}/C_l$ is the non-dominant pole. $f_u = g_{m1}/C_c$ is the unity gain frequency. β is the low frequency gain of the operational amplifier from its input to the output in the given configuration and is given by:

$$\begin{aligned} \beta &= 1 + \frac{C_{11p} + C_{12p} + C_{13p} + Cip}{C_{13p}} \\ &= 2.91 \end{aligned} \tag{3.11}$$

The total noise power appearing at the output of the operational amplifier is then:

$$\begin{aligned} N_{o,oa100} &= \int_0^\infty S_{i,oa100}(f) A_{cl}^2(f) df \\ &= \int_0^\infty \left(\frac{S_{i,oab1,th}(f)}{100} + \frac{S_{i,oab2,th}(f)}{100} + \frac{S_{i,oab1,1/f}(f)}{100} \right) A_{cl}^2(f) df \\ &= (51\mu V)^2 + (0.31\mu V)^2 + (2.7\mu V)^2 \\ &= (51\mu V)^2 + (2.7\mu V)^2 \end{aligned} \tag{3.12}$$

where the thermal and $1/f$ noise components have been kept separate.

The total noise power at the output of the operational amplifier can be referred to the

input of the delta-sigma modulator to get:

$$\begin{aligned} N_{i,ds,oa100} &= \frac{N_{o,oa100}}{\left(\frac{C_{11p}}{C_{13p}}\right)^2} \\ &= (129\mu V)^2 + (6.8\mu V)^2 \end{aligned} \tag{3.13}$$

Only the thermal noise power of this delta-sigma modulator is divided by the oversampling ratio. $1/f$ noise is not divided by the oversampling ratio because it is concentrated at low frequencies. Therefore, dividing thermal noise sources by the oversampling ratio and adding up the noise components, the total calculated noise power of the delta-sigma modulator is:

$$\begin{aligned} N_{i,ds} &= \frac{N_{i,ds,sampcap}}{OSR} + \frac{N_{i,ds,oa100,th}}{OSR} + N_{i,ds,oa100,1/f} \\ &= \frac{(74\mu V)^2}{128} + \frac{(129\mu V)^2}{128} + (6.8\mu V)^2 \\ &= V_{noiserms}^2 \\ &= (15\mu V)^2 \end{aligned} \tag{3.14}$$

For this delta-sigma modulator, the maximum SNR achievable based on the above calculated noise and assuming a maximum sine wave input with a differential peak-to-peak amplitude of 2V for a 4V full-scale[5] is:

$$\begin{aligned} SNR &= 20\log\left(\frac{V_{inrms}}{V_{noiserms}}\right) \\ &= 93.5dB \end{aligned} \tag{3.15}$$

where quantization noise (which has been attenuated by over 119dB as simulated in Section 3.1.3.1) has been ignored. For comparison, a true 16-bit converter that can accept a 50% of full-scale peak-to-peak amplitude sine wave has an SNR of 92.1dB. A true 16-bit converter that can accept a full-scale peak-to-peak amplitude sine wave has an SNR of 98.1 dB.

3.1.4 Array of Digital Inverters (InvArrA)

An array of 31 buffered inverters with capacitive coupling to the substrate (InvArrA) was used to create substrate noise as shown in Figure 3-19. InvArrA had two states: (1) *Reset*–half the inverters are in the high state and half are in the low state. (2) *Trigger*–the number of inverters in the low to high states are determined by the input pattern. In effect, these states imply that the input pattern, fed from an off-chip source, controls the amount of substrate noise generated during each clock period because it decides how

[5]Large inputs (near full-scale) to delta-sigma modulators usually result in instability which decreases the maximum achievable SNR.

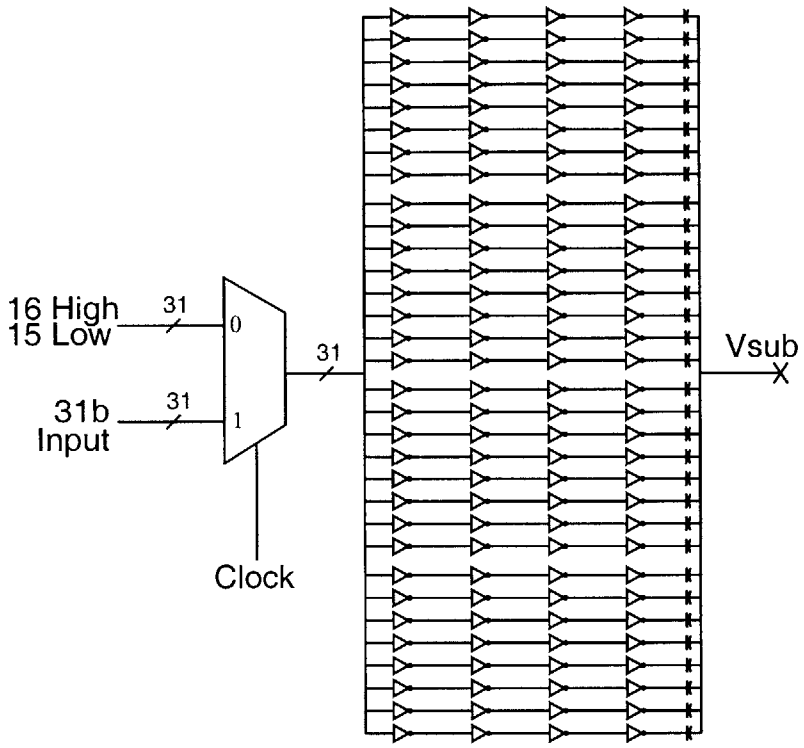


Figure 3-19: Array of digital inverters (InvArrA) for creating substrate noise.

many inverters transition from low-to-high and high-to-low when InvArrA changes from the *Reset* state to *Trigger* state. InvArrA transitions between states when the clock that controls the multiplexer changes. The transition from the *Reset* to *Trigger* state happens on the rising edge of the clock controlling InvArrA, which can be delayed by DelayA in relation to the analog sampling clock edge. The transition from the *Trigger* to *Reset* state happens on the falling edge of the clock. This transition was designed to happen during non-critical times (*i.e.* well away from the analog sampling clock edge) to prevent the substrate noise generated by this transition from interfering with the substrate noise generated near the analog sampling edge. This *Reset* state is necessary in order to center the InvArrA for maximum dynamic range. For example, if InvArrA needs to generate 8 low-to-high transitions for 10 consecutive periods, it does not have 80 inverters already in the low state so that each period, a new set of eight inverters will transition from low-to-high. Thus, inverters need to be reset so that InvArrA can generate the requisite amount of high-to-low and low-to-high transitions.

Each large inverter that creates substrate noise is buffered with a series of three inverters so that four scaled inverters were connected in series, as shown in Figure 3-20. These inverters are standard static CMOS digital inverters with an interstage scaling of 5. The

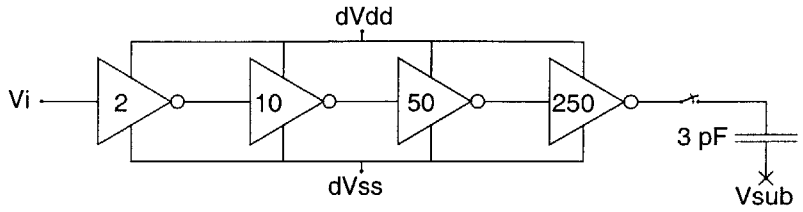


Figure 3-20: A single unit of InvArrA.

last and largest inverter, responsible for most of the substrate noise, drives a 3pF capacitor connected to the substrate to increase generated substrate noise. This capacitor can be disconnected from the inverter output if necessary. In addition, InvArrA has dedicated power supplies so that it does not affect other circuitry.

Each inverter was designed so that rise and fall times were roughly equal which is common in digital design.

3.1.5 Power Grid

All the analog circuits (*i.e.* bias circuits, SC filters, etc.) share a set of power supplies. InvArrA has its own dedicated power supplies. N-wells of the digital circuits are connected to the digital high power rail and the n-wells of the analog circuits are connected to the analog high power rail. The substrate was also connected to the digital and analog low power rail in the digital and analog sections of the chip, respectively. However, unlike the n-wells, the substrate in which the NMOS of digital and analog circuits lie cannot be separated. As a consequence, the digital and analog low power rails are "soft" connected through the substrate while the digital and analog high power rails are not.

3.2 Chip Micrograph

The chip micrograph with the parts used for the study of substrate noise is shown in Figure 3-21.

3.3 Experimental Results and Discussion

3.3.1 Delta-Sigma Modulator Performance

The delta-sigma modulator, operating alone on the mixed-signal chip, performs roughly as expected. Current levels were lowered from design values because they did not affect performance. This is because the delta-sigma modulator was over-designed with large safety margins as explained above in the previous sections.

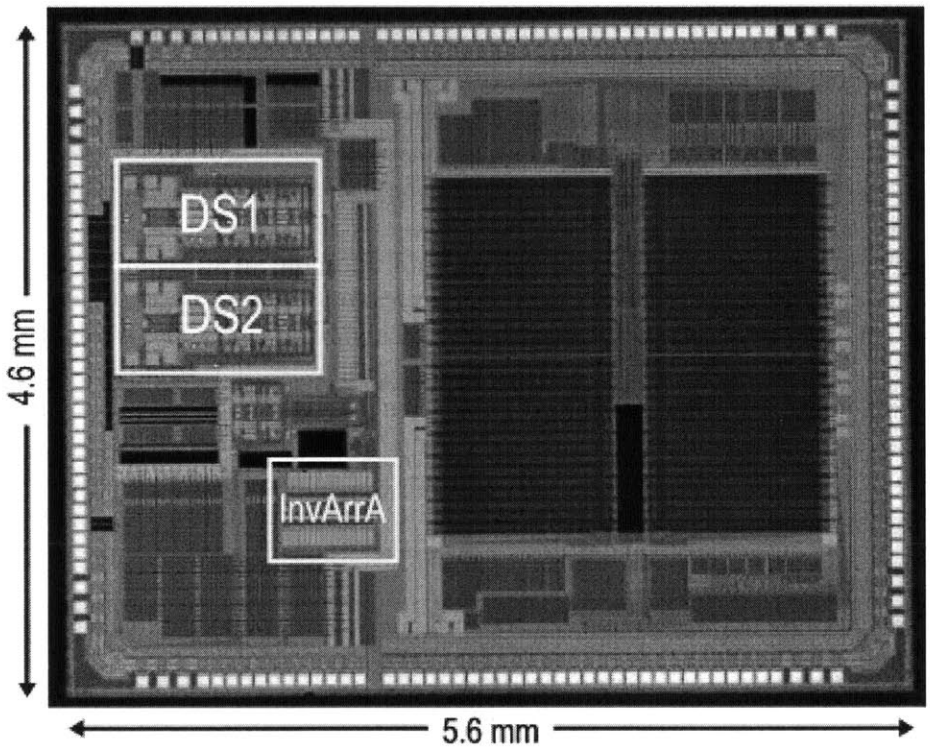


Figure 3-21: Chip micrograph and components used for study of substrate noise.

Figure 3-22 shows the Hann-windowed[6] spectrum of the delta-sigma modulator output with a 353mVrms 1kHz input tone. The input tone has a skirt because the clock generator and input tone generator were not phase locked. For subsequent calculations the input tone power encompasses the tone and this skirt. The fast fourier transform (FFT) shown used 262,144 points. All subsequent FFT will also use 262,144 points unless otherwise noted.

In Figure 3-22, the third and second harmonics of the input tone are visible. Theoretically, the second harmonic should not appear because the implementation was differential, but in reality no converter is perfectly symmetric and hence the appearance of the second harmonic. The harmonics are mainly caused by mismatch in input impedances between the differential inputs of the delta-sigma modulator which leads to signal dependent charge injection [48]. The effect worsens with larger input amplitudes, because larger input voltages increases the input impedance mismatch of the differential inputs, and thus increases the magnitude of the harmonics.

The spectrum shown is without use of chopping. The effect of $1/f$ noise was determined to be small and negligible. Thus, chopping, although designed into the delta-sigma modulator, was not used at all data gathered and presented here. This is true of all data presented subsequently.

The metrics of signal to noise ratio (SNR), total harmonic distortion (THD), and signal to noise plus distortion ratio (SNDR)[7] versus input amplitude of a 1kHz sine wave for the delta-sigma modulator are shown in Figure 3-23. The band of interest, as mentioned before is 0 to 20kHz. From the figure, the SNDR of the performance at low input levels is dominated by the circuit noise (*i.e.* thermal and $1/f$) since the THD is very low. This is reflected in the tight correspondence of SNR and SNDR. At larger input levels, the distortion, mainly the third harmonic, rises because of signal dependent charge injection in the input stage as explained above. As a result, THD grows and begins to dominate the SNDR. The SNR exceeds 96 dB for large input magnitudes, roughly in line with expectations from the noise analysis of Section 3.1.3.9.

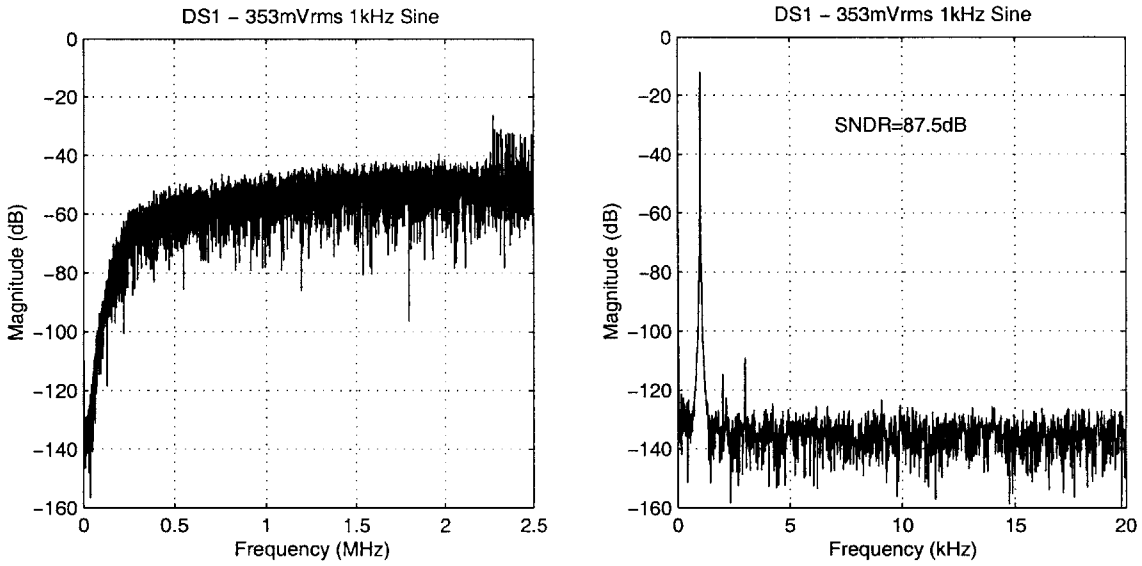
In summary, the delta-sigma modulator functioned as designed. Including bias circuits, the delta-sigma modulator consumed about 18mW of power.

3.3.2 Substrate Noise Waveforms

Using InvArrA to generate substrate noise and the sampling scope concept mentioned above, waveforms digitized by DS1, a delta-sigma modulator converting an external off-chip analog signal, and DS2, a delta-sigma modulator converting the substrate voltage, are shown in Figure 3-24. The waveform associated with DS1 is coupled substrate noise, apparent input signal in DS1 due to substrate noise coupling, and the waveform associated with DS2 is substrate noise, the substrate voltage fluctuation due to digital circuits. The differential input to DS1 is 0V DC. The x-axis represents DelayA, the time between the rising edge of

[6]This window, which preserves power ratios, is also known as the raised cosine window.

[7]SNR is the input tone power divided by the noise power in the band of interest. The noise does not include harmonics of the input tone. THD is the sum power of the harmonics falling in the band of interest. SNDR is the input tone power divided by the rest of the energy in the band of interest.



(a) (b)

Figure 3-22: Measured delta-sigma modulator output spectrum in response to a 353mVrms 1kHz input tone. (a) Spectrum from 0 to 2.5MHz. (b) Spectrum from 0 to 20kHz.

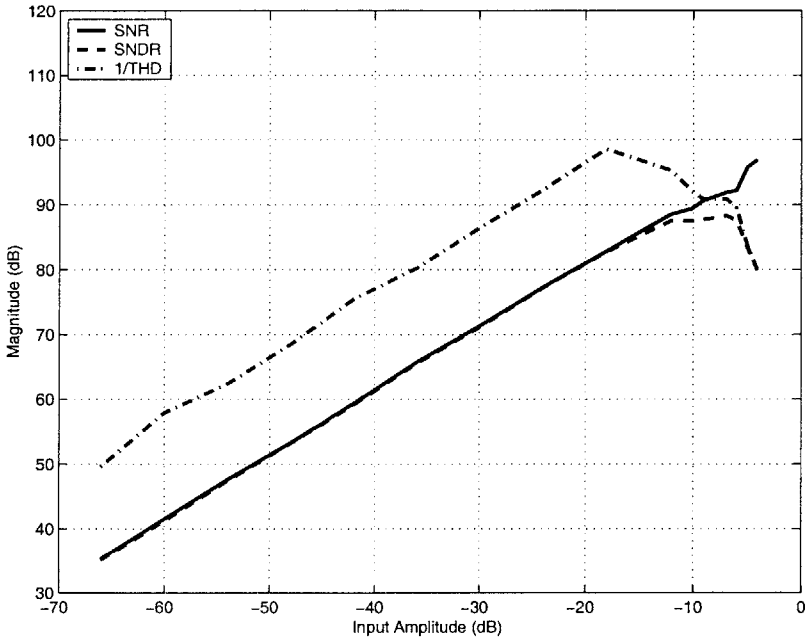


Figure 3-23: Measured performance of delta-sigma modulator. Input amplitude is normalized to the full-scale voltage.

the clock that controls InvArrA and the analog sampling edge. The time resolution used for reconstruction was 0.4ns. 100,000 samples from each delta-sigma modulator were averaged to obtain one point in the waveforms. Figure 3-24 only shows DelayA up to 8ns because of the limited adjustment range of DelayA. Waveforms were also reconstructed with InvArrA off which resulted in no signal in DS1 and DS2.

The waveforms shown were in Figure 3-24 are in response to InvArrA switching 16 inverters high-to-low and 15 inverters low-to-high with coupling capacitors connected to the substrate. The maximum difference between the high-to-low and low-to-high transient waveforms is approximately 400uV for coupled substrate noise in DS1 at 3.0ns and approximately 10mV for substrate noise in DS2 at 3.0ns. These measured values were much smaller than anticipated[8].

In Figure 3-24, the waveforms caused by high-to-low and low-to-high transitions in DS1 and DS2 are not symmetric. The peaks of each waveform do not coincide in time and the peak values are not equal in magnitude. These differences can be explained by considering the substrate noise generation mechanisms as discussed in the following section. Furthermore, the waveforms digitized by DS1 and DS2 are not similar. The waveforms seen by DS1 ring about the zero voltage level while their counterparts seen by DS2 ring about the initial overshoot peak. Since DS1 and DS2 are configured differently, the differences between the two are reasonable and can be explained upon closer examination of the input sampling circuit as done below.

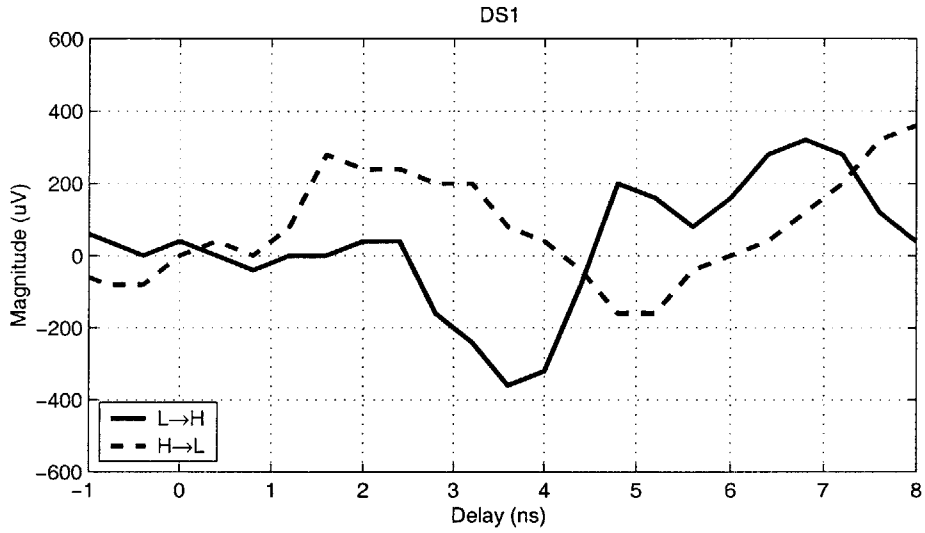
Based on the measured waveforms, the coupled substrate noise and substrate noise waveforms have decay time constants of at least a few nanoseconds. The period of ringing, or natural frequency of the coupled substrate noise and substrate noise, is roughly 300MHz. These values imply that if the digital parts in this chip run above a few hundred Megahertz, the substrate will never have a chance to settle in response to a digital transition and will constantly fluctuate while the digital circuits are in operation.

3.3.2.1 Substrate Noise Generation Mechanisms

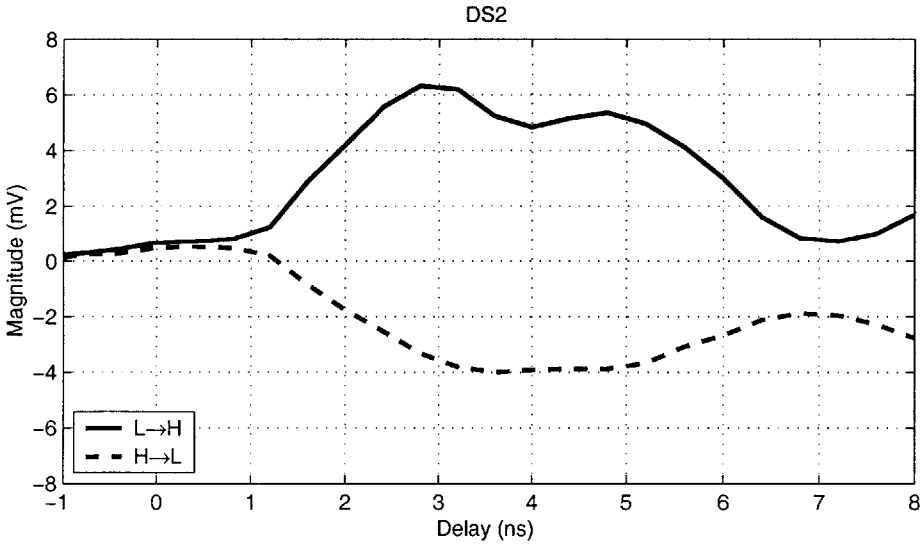
The coupled substrate noise and substrate noise waveforms seen in DS1 and DS2 were the result of substrate noise generated by the mechanisms discussed in Section 2.1: (1) power supply transient, (2) impact ionization, and (3) capacitive coupling. Figure 3-25 illustrates the result of the mechanisms creating substrate noise. The mechanisms of power supply transient and impact ionization create substrate noise because of short circuit current spikes in the inverter during switching[9]. The current spikes are roughly the same for high-to-low and low-to-high transitions, resulting in a *direction independent* voltage transient waveform on the substrate due to the finite substrate impedance. This is indicated as V_{subind} in Figure 3-25. The mechanism of capacitive coupling creates substrate noise because of the voltage transition of the inverter output node, which couples to the substrate through

[8]Past literature and communications with mixed-signal chip experts led to the expectation of about a hundred millivolts of substrate noise.

[9]A current spike occurs when the output of the inverter is as fast as the input to the inverter [27, pp.242–244]. This was the case for InvArrA on this chip because of the inverter scaling used.



(a)



(b)

Figure 3-24: Substrate noise and coupled substrate noise waveforms generated by InvArrA with coupling capacitors to the substrate connected. Waveforms are reconstructed from measured data using the sampling scope technique. Note that the scales in each subfigure are different. (a) coupled substrate noise in DS1 and (b) substrate noise in DS2.

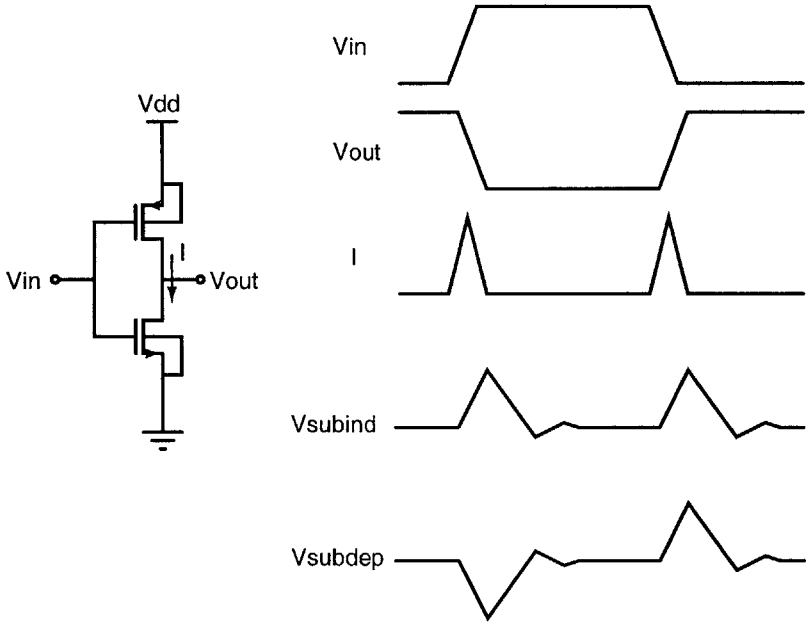
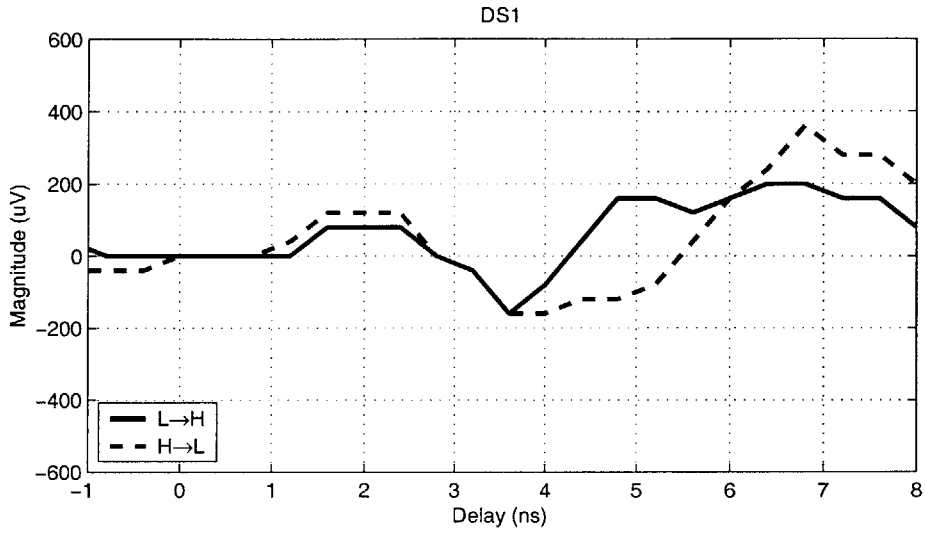


Figure 3-25: An inverter has a direction dependent and direction independent substrate noise component for every transition.

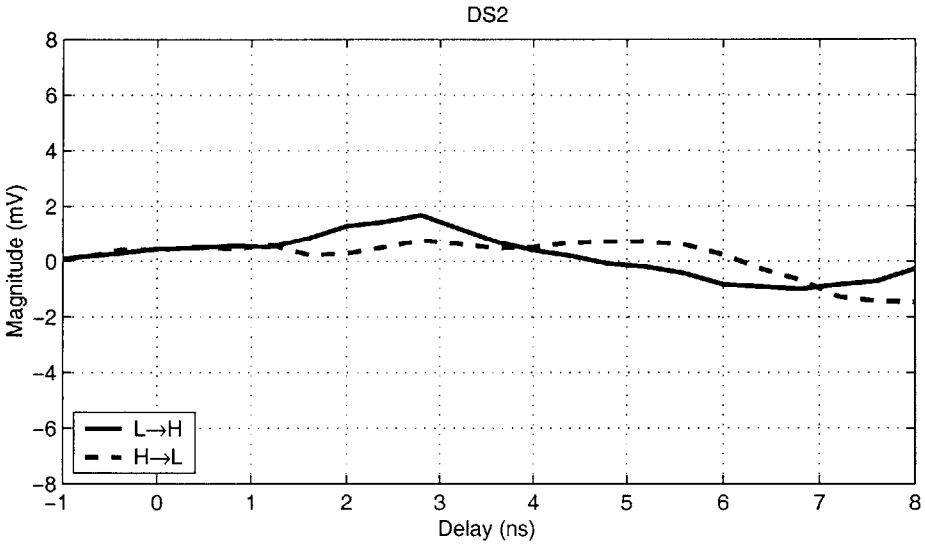
capacitance, including parasitic junction capacitance and the explicit coupling capacitors. This results in a *direction dependent* voltage transient waveform on the substrate, indicated in Figure 3-25 by V_{subdep}.

These effects are also seen in the coupled substrate noise and substrate noise waveforms in Figure 3-26 in which InvArrA had its coupling capacitors to the substrate disconnected. In this case, both the high-to-low and low-to-high waveforms in the substrate noise and coupled substrate noise are much more similar because the capacitive coupling had been substantially decreased; the direction independent transient was dominant. The waveforms still differ, however, because there is still capacitive coupling through the parasitic capacitance from digital signals to the substrate.

The effects of capacitive coupling can be clearly seen if the effect of the direction independent transient is subtracted. By averaging the high-to-low and low-to-high transitions for coupled substrate noise and substrate noise waveforms in Figure 3-26 and then subtracting from the coupled substrate noise and substrate noise waveforms in Figure 3-24, Figure 3-27 is obtained. Figure 3-27 shows symmetric waveforms for high-to-low and low-to-high transitions that are characteristic of capacitive coupling or direction dependent transients.

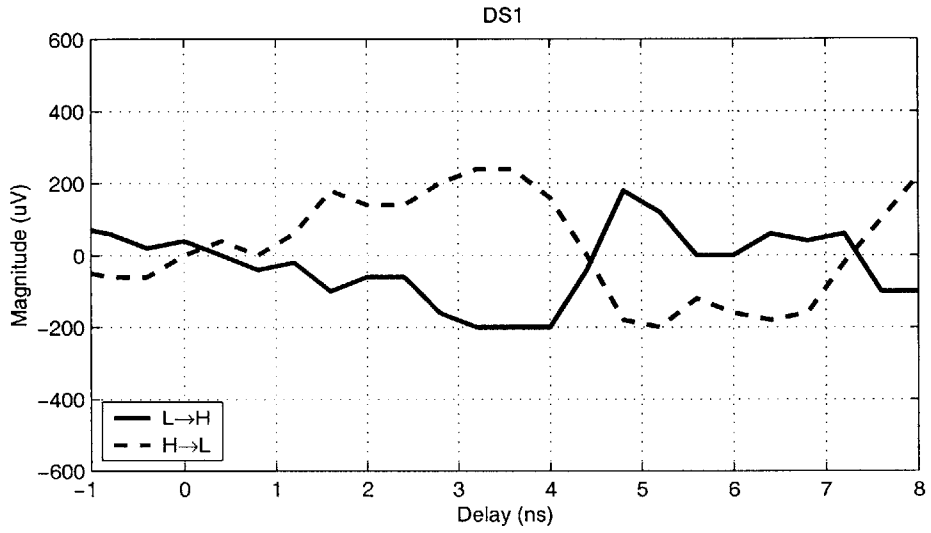


(a)

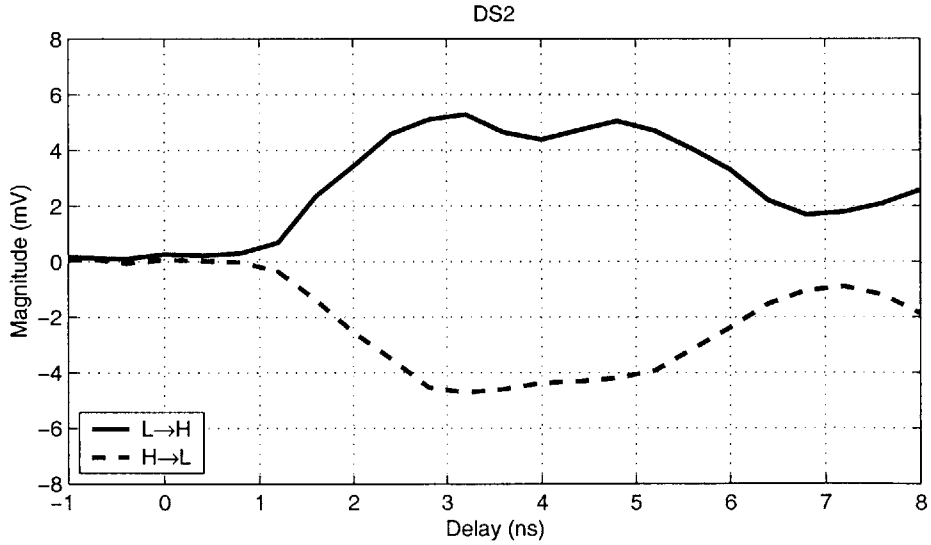


(b)

Figure 3-26: Coupled substrate noise and substrate noise waveforms generated by InvArrA with coupling capacitors disconnected. Waveforms are reconstructed from measured data. Note that the scales are different in each subfigure. (a) coupled substrate noise in DS1 and (b) substrate noise in DS2.



(a)



(b)

Figure 3-27: Coupled substrate noise and substrate noise waveforms generated by InvArrA with the direction dependent components subtracted. Waveforms are reconstructed from measured data. Note that the scales are different in each subfigure. (a) coupled substrate noise in DS1 (b) substrate noise in DS2.

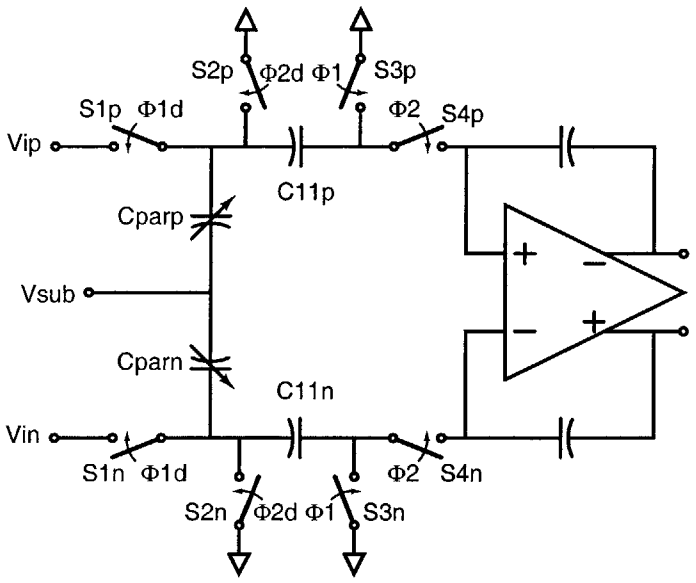


Figure 3-28: Input sampling circuit of the first stage of the delta-sigma modulator.

3.3.3 Input Signal Independent and Input Signal Dependent Components of Coupled Substrate Noise

In all the coupled substrate noise waveforms shown so far, the differential input to DS1 was 0V DC. Since the delta-sigma modulator is implemented differentially, substrate noise, a common mode signal, should be rejected perfectly such that coupled substrate noise, an apparent input signal in DS1, is zero. However, because of device and parasitic differential mismatches caused by process variations and physical layout, the differential paths are asymmetric allowing common mode signals to create differential signals. This is the case for the substrate noise generation mechanisms which created common mode signals (*i.e.* substrate noise) and then caused the differential signals (*i.e.* coupled substrate noise) seen in the figures. This coupled substrate noise was additive or *input signal independent* in the sense that even without an input signal to the delta-sigma modulator, coupled substrate noise will still appear in the DS output. Furthermore, only asymmetry in the first stage of the delta-sigma modulator is important because any noise contributions in later stages of the delta-sigma modulator are shaped by the loop filter.

Differential asymmetry is also caused by the input signal itself because of device non-linearities. Specifically, the input sampling circuit is differentially biased by the input signal as shown in Figure 3-28. This means the switch resistance and parasitic junction capacitance to the input nodes, both functions of input voltage, are mismatched between the two sides of the differential circuit. Thus, the amount of coupled substrate noise in DS1 depends on the exact input voltage. This effect is shown in Figure 3-29 where the coupled substrate noise waveform magnitude changes with the DS1 input voltage. An implication of this analysis

is that coupled substrate noise also has a mixing, or *input signal dependent* component (*i.e.* coupled substrate noise is modulated by the input signal) in addition to the additive component described above.

Further evidence that substrate noise couples into DS1 significantly through the parasitic junction capacitances of the input sampling circuit is seen in the coupled substrate noise waveform itself. Substrate noise coupling capacitively into DS1 implies that the coupled substrate noise is a high-pass version of the substrate noise on the substrate voltage. This can be seen through the analysis of the sampling circuit shown in Figure 3-28. An equivalent model for analysis is shown in Figure 3-30. In the figure, R_{1p} and R_{1n} represent the equivalent resistances looking out from the bottom plates (towards the inputs V_{ip} and V_{in}) of C_{11p} and C_{11n}, respectively. R_{2p} and R_{2n} represent the equivalent resistances looking out from the top plates of C_{11p} and C_{11n}, respectively.

If the circuit is differentially symmetric except in the parasitic capacitances:

$$\begin{aligned} C_{parp} = C_p = C_{parn} - C_\epsilon \\ R_{1p} = R_1 = R_{1n} \\ R_{2p} = R_2 = R_{2n} \\ C_{11p} = C_{11} = C_{11n} \end{aligned}$$

The transfer function from V_{sub} to the voltages, V_{1p} and V_{1n}, on capacitors C_{11p} and C_{11n}, respectively, is:

$$\frac{V_{1p}}{V_{sub}}(s) = \frac{C_p\left(1 + sC_{11}\left(R_1 + R_2\right)\right)}{C_{11}\left(sC_p\left(R_1 + R_2\right) + 1 + \frac{C_p}{C_{11}}\right)\left(sC_{11}R_2 + 1\right)} \tag{3.16}$$

$$\frac{V_{1n}}{V_{sub}}(s) = \frac{\left(C_p + C_\epsilon\right)\left(1 + sC_{11}\left(R_1 + R_2\right)\right)}{C_{11}\left(s\left(C_p + C_\epsilon\right)\left(R_1 + R_2\right) + 1 + \frac{C_p + C_\epsilon}{C_{11}}\right)\left(sC_{11}R_2 + 1\right)} \tag{3.17}$$

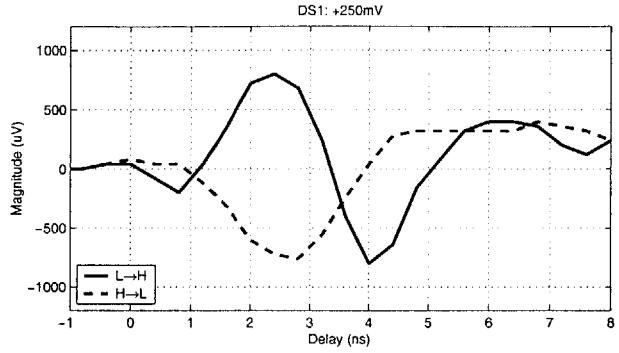
At relatively lower frequencies where the pole due to C_p can be ignored, the transfer function from the substrate voltage to the differential input of the delta-sigma modulator is:

$$\frac{V_{1p} - V_{1n}}{V_{sub}}(s) \approx \frac{C_\epsilon\left(1 + sC_{11}\left(R_1 + R_2\right)\right)}{C_{11}\left(sC_{11}R_2 + 1\right)} \tag{3.18}$$

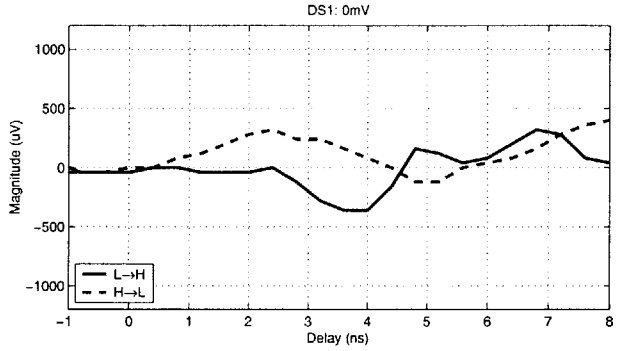
Equation 3.18 shows that the transfer function from substrate noise to the input of the delta-sigma modulator has a high-pass characteristic due to mismatch in the parasitic capacitances. Furthermore, the amount of substrate noise coupling depends on the amount of mismatch, C_ϵ, of the junction capacitances as well.

The amount of substrate noise coupling will also increase due to mismatches in the differential circuit from process variations and physical layout as they affect the values in Equation 3.16 and Equation 3.17. These mismatches increase the amount of substrate noise coupling.

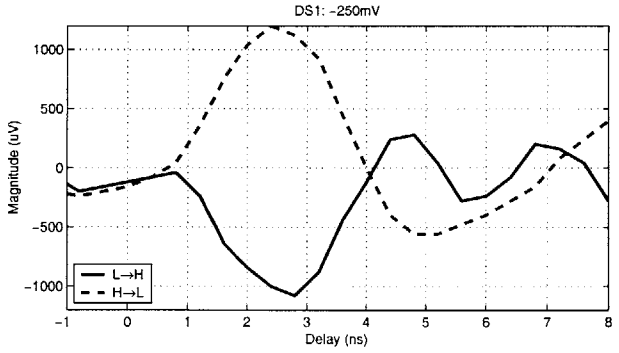
This analysis is consistent with the behavior seen in Figure 3-27 where the coupled substrate noise seen in DS1 is roughly a high-pass version of the substrate noise seen in



(a)



(b)



(c)

Figure 3-29: Coupled substrate noise waveforms in DS1 with differential DC input voltages. (a) +250mV (b) 0V (c) -250mV.

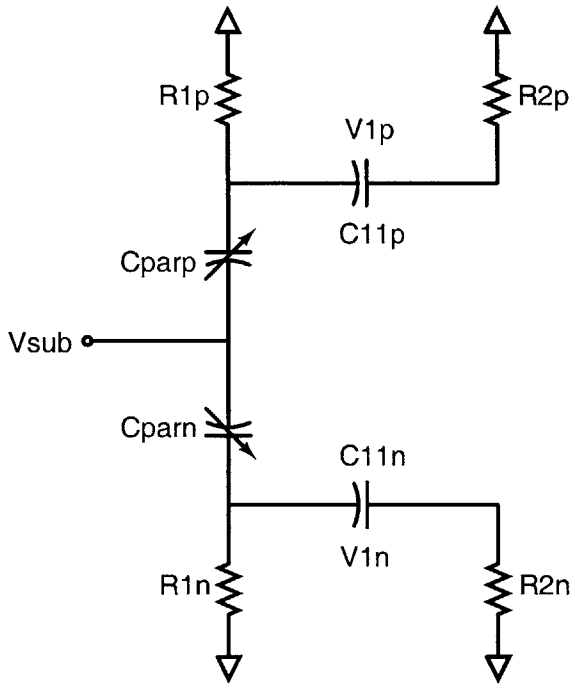


Figure 3-30: Equivalent input sampling circuit of the first stage of the delta-sigma modulator (Figure 3-28) for analyzing coupled substrate noise seen in DS1. R_{1p} and R_{1n} represent the equivalent resistances looking out from the bottom plates (towards the inputs V_{ip} and V_{in}) of C_{11p} and C_{11n}, respectively. R_{2p} and R_{2n} represent the equivalent resistances looking out from the top plates of C_{11p} and C_{11n}, respectively.

DS2.

3.3.3.1 Coupled Substrate Noise from Voltage Reference Sampling Circuit

In addition to the input sampling circuit discussed above, the first stage of DS1 had another sampling circuit: one that samples the reference voltage. This reference voltage sampling circuit also couples substrate noise into the delta-sigma modulator the same way as the input voltage sampling circuit. A behavioral model in Simulink was constructed and is shown in Figure 3-31.

The model shows a single coupled substrate noise source introducing coupled substrate noise into both the input voltage and the reference voltage through a mixing (input signal dependent) and additive (input signal independent) gain in each case. Since the DAC structure removes mismatches due to process variations and physical layout (Section 3.1.3.7, the substrate noise cannot couple through those mismatches and thus the additive path has been removed by setting "Ref additive gain" in Figure 3-31 to zero. Also, "Ref mixing gain" has been set to -1 instead of 1 which means the coupled substrate noise from the input sampling circuit and reference sampling circuit will add together instead of subtract from each other as explained below.

Simulations of the model are shown in Figure 3-32. The input signal tone was a -27dB of full scale 10kHz sine wave. The coupled substrate noise tone was a -60dB of full scale 1.1kHz sine wave. The delta-sigma modulator was modeled with a differential DC offset of -80dB. The simulations show the effect of substrate noise coupling into the delta-sigma modulator through the input and reference sampling circuits. In Figure 3-32(a), the output spectrum has a single tone at 10kHz, no coupled substrate noise and a DC offset of -80dB. Figure 3-32(b) shows the effect of substrate noise coupling through the input sampling circuit only. The coupled substrate noise appears at 1.1kHz, the additive part, and at both 8.9kHz and 9.9kHz, the mixing part. Figure 3-32(c) shows the effect of substrate noise coupling through the reference sampling circuit only. In this case, the output, *vout*, modulates the coupled substrate noise (*i.e.* in Figure 3-17, the output of the delta-sigma modulator decides if the charge sampled on the capacitors, C_{12p} and C_{12n}, which contain the contributions from the coupled substrate noise as well as the reference voltage, is delivered to the capacitors, C_{13p} and C_{13n}, respectively, or C_{13n} and C_{13p}, respectively.). However, *vout*, is output of the delta-sigma modulator meaning its spectrum contains the input signal of the delta-sigma modulator plus quantization noise. Thus, the coupled substrate noise, modulated by the output of the delta-sigma modulator, appears at both 8.9kHz and 9.9kHz due to the input tone present in the delta-sigma modulator output and at 1.1kHz due to the DC offset. Since these coupled substrate tones now appear in the output, these tones also modulate the coupled substrate noise so that tones appear at 2.2kHz, 7.8kHz, and 12.2kHz. These tones, in turn, again modulate the coupled substrate noise making this a data-dependent process. If the substrate noise coupling is small, then the modulated tones will disappear under the quantization noise because of the attenuation through modulation. In Figure 3-32(d), the combination of the effect of coupled substrate noise on the input sampling circuit and the reference sampling is shown. Since a negated version of the delta-sigma modulator output is fed back to the first stage of the delta-sigma modulator, the mixing part of the

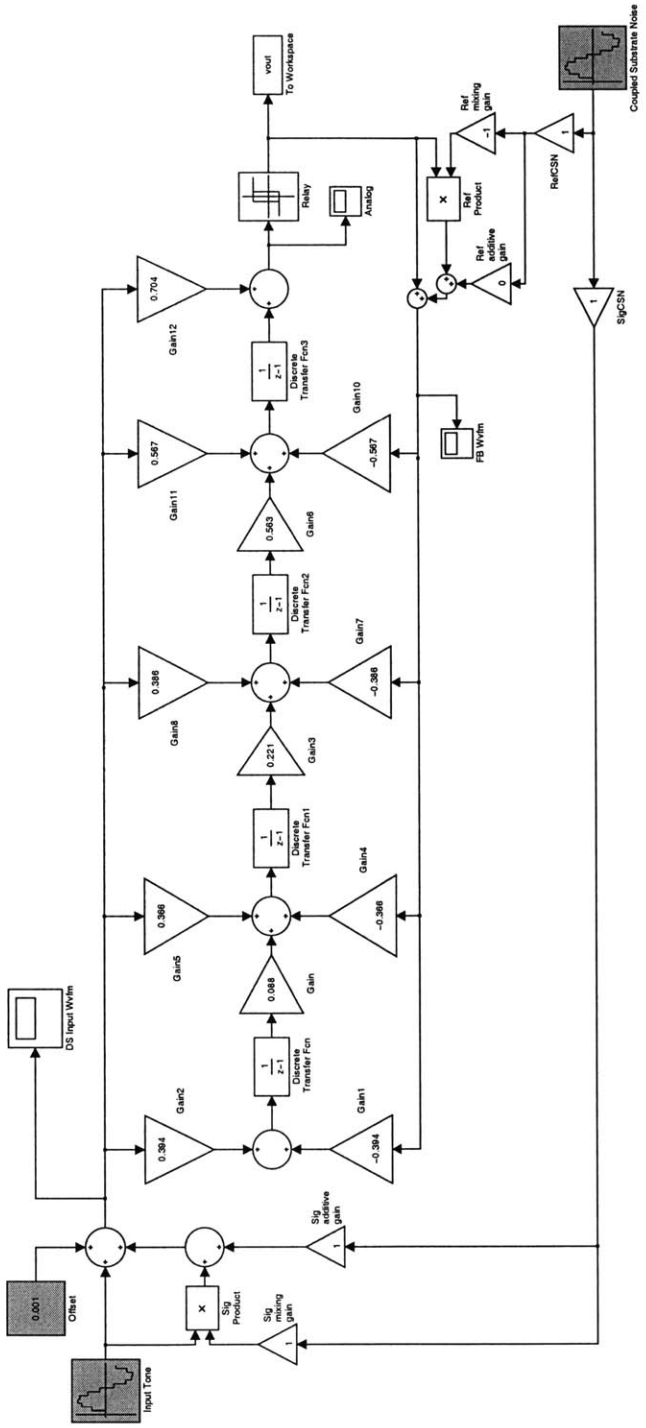


Figure 3-31: Simulink model of substrate noise coupling into a delta-sigma modulator. The substrate noise couples in through the sampling circuits of the first stage, one that samples the input, and one that samples the reference. The substrate noise coupling is modeled with an additive gain and a mixing gain in each case. No substrate noise couples in additively through the reference sampling circuit because process variation and physical layout mismatches have been removed with the DAC structure (Section 3.1.3.7).

coupled substrate noise from the input sampling circuit and the reference sampling circuit will subtract if "Ref mixing gain" is 1. However, since the "Ref mixing gain" has been set to -1, the mixing part of the coupled substrate noise from the input and reference sampling circuit actually add in the simulation. In an actual circuit, the mixing part due to the input sampling circuit may add to or may partially cancel the mixing part due to the reference sampling circuit, but because of mismatch and non-linearities, it is unlikely to fully cancel the effect as seen in the measured data.

The conclusion of these simulations is that substrate noise couples in to a delta-sigma modulator through the input sampling circuit as well as the reference sampling circuit. Both the coupled substrate noise from the input sampling circuit and the reference sampling circuit contribute to the overall noise in the delta-sigma modulator and thus affect the performance of the delta-sigma modulator.

3.3.4 SNDR Decrease Due to Coupled Substrate Noise

Figure 3-34(a) and 3-35(a,c) show the SNDR decrease of DS1 due to coupled substrate noise. The input pattern to InvArrA, the substrate noise generator, was a 300Hz 50% duty cycle square wave alternating between the digital values, 7 and 15. Since InvArrA in the *Reset* state has 16 inverters high and 15 inverters low, each analog period has either 9 or 1 high-to-low digital transitions. To be more specific, in a 1.66ms time duration, 9 high-to-low digital transitions in InvArrA occur DelayA before each and every analog sampling operation. During the next 1.66ms, 1 high-to-low digital transition in InvArrA occurs DelayA before each and every analog sampling operation. This cycle then repeats for subsequent 3.33ms periods, thus giving the 300Hz activity rate for substrate noise even though InvArrA is clocked at the analog sampling rate, 5MHz. The inverter array, moreover, can be clocked faster, but it should be noted that faster digital clock speeds may not worsen analog circuit performance since it is DelayA, the relative delay between when substrate noise is created and when analog signals are sampled in the circuits, that is crucial. As long as DelayA is less than a few decay time constants of the coupled substrate noise and substrate noise waveforms, the analog circuits will be affected by substrate noise. In terms of waveforms, the coupled substrate noise and substrate noise waveforms over many cycles has been constructed with measured data and are shown in Figure 3-33. This figure shows that although the continuous time waveform is not a square wave, the values, indicated by the triangles in Figure 3-33, sampled at 5MHz by DS1 and DS2 form a 300Hz 50% duty cycle discrete time square wave.

The input to DS1 was a 125mVrms 7.6kHz sine wave for the data shown in Figure 3-34 and Figure 3-35. The figures show the SNDR for DS1, which converts an external signal, and the total in-band noise power (TINP) in terms of decibels below full scale for DS2, which converts the substrate voltage.

The decrease in SNDR for DS1 was about 19dB and the increase in TINP for DS2 was about 30dB for a DelayA of 3.0ns. Other DelayA values resulted in different SNDR decreases and TINP increases because DelayA determined what point the coupled substrate noise and substrate noise waveforms were sampled by DS1 and DS2, respectively. For a DelayA of 2.0ns, the SNDR decrease in DS1 was about 16dB, half a bit better performance

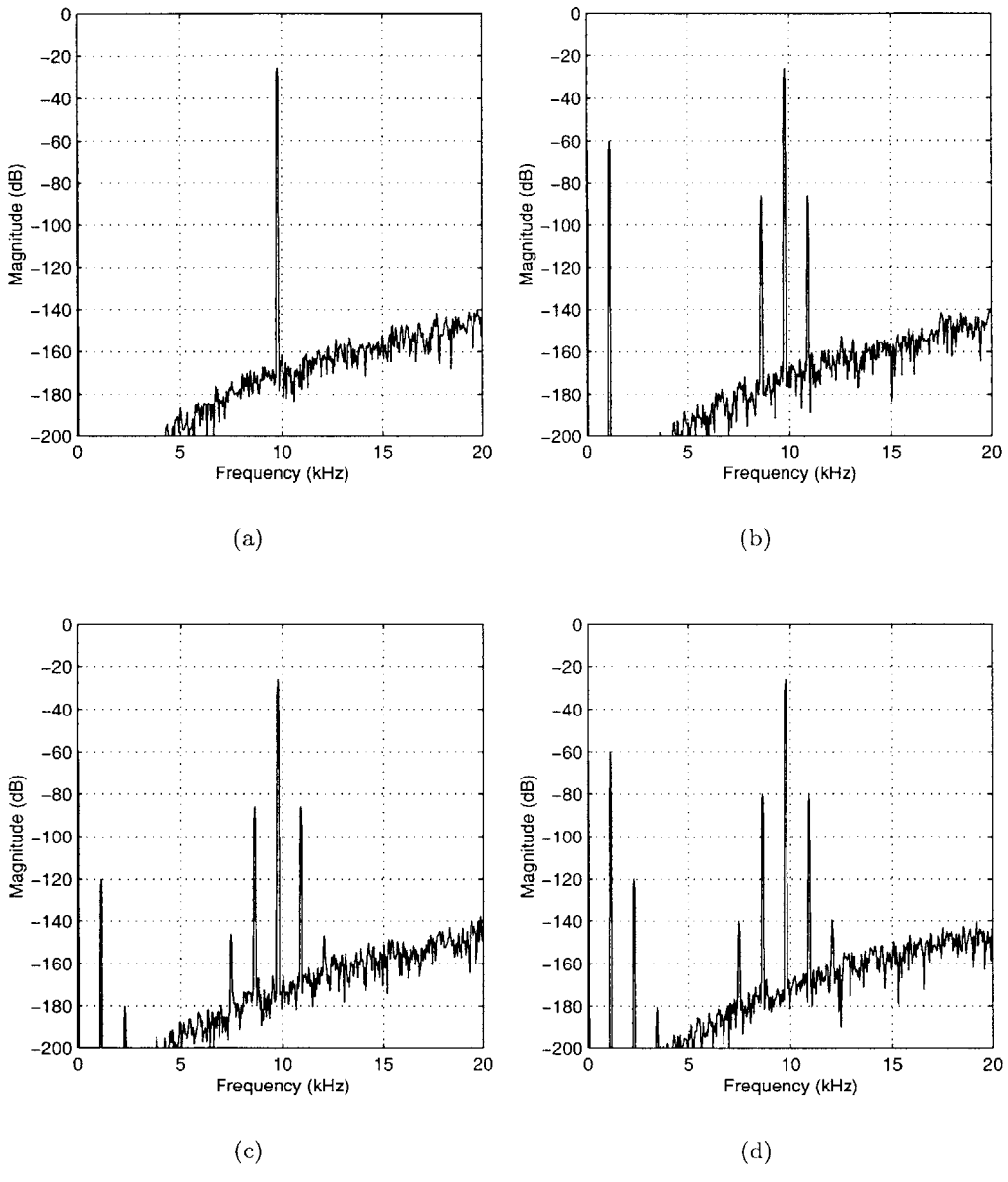
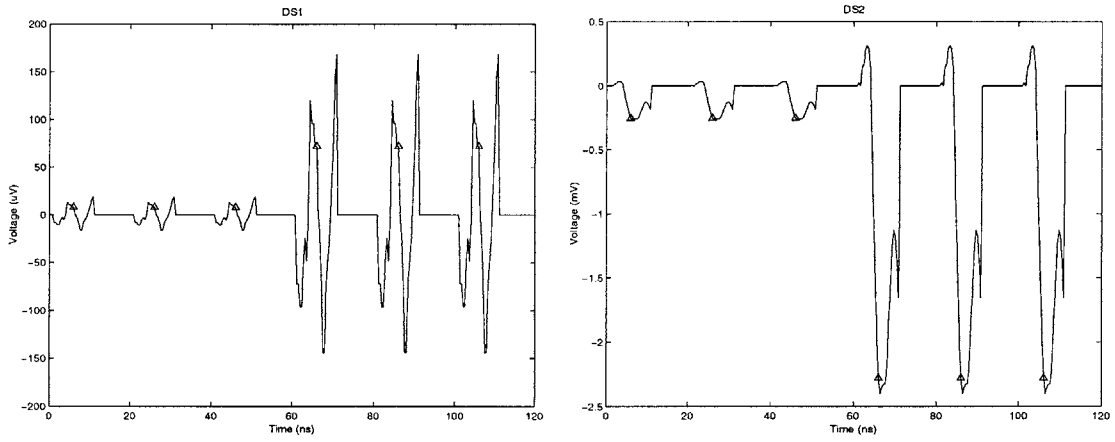
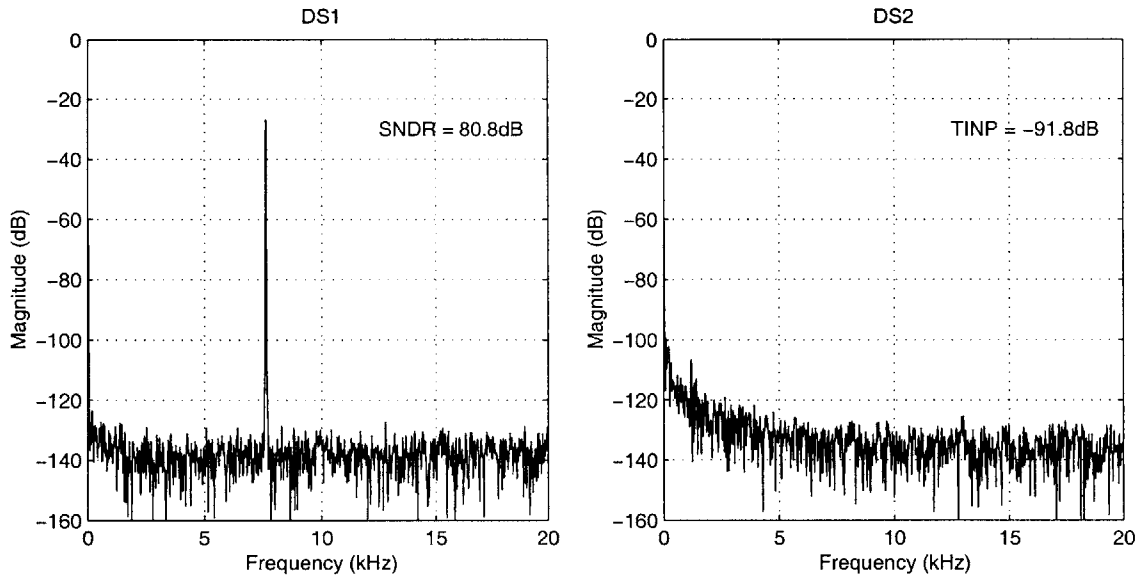


Figure 3-32: Results of behavioral simulations using the Simulink model shown in Figure 3-31. The input signal tone was a -27dB of full scale 10kHz sine wave. The coupled substrate noise tone was a -60dB of full scale 1.1kHz sine wave. The delta-sigma modulator was modeled with a differential DC offset of -80dB. (a) No substrate noise coupling through the input nor reference sampling circuit. (b) Substrate noise coupling through the input sampling circuit only. (c) Substrate noise coupling through the reference sampling circuit only. (d) Substrate noise coupling through both the input and reference sampling circuit.



(a) (b)

Figure 3-33: Simulated coupled substrate noise and substrate noise waveforms generated by InvArrA over time. InvArrA causes 1 high-to-low transition every analog clock period or 9 high-to-low transitions every analog clock period depending on its input pattern. The triangles indicate the sampled values in DS1 and DS2. Although in continuous time the waveform is constantly changing, the discrete time values form a square wave. The frequency of the clock that controls when InvArrA transitions has been set at about 50MHz for this illustration to more fully illustrate the continuous time transient waveforms because they have ringing frequencies of about 300MHz. In the actual test setup, the frequency of the clock that controls InvArrA is 5 MHz. Furthermore, transients due to reset of the InvArrA have been omitted. The waveforms have been constructed from measured data with some zero padding after the waveforms to allow clear distinction of a clock cycle. (a) coupled substrate noise in DS1 (b) substrate noise in DS2.



(a) (b)

Figure 3-34: Measured delta-sigma modulator output spectra from 0-20kHz with no substrate noise. The input to DS1 is a 125mVrms 7.6kHz input tone. (a) DS1 (b) DS2.

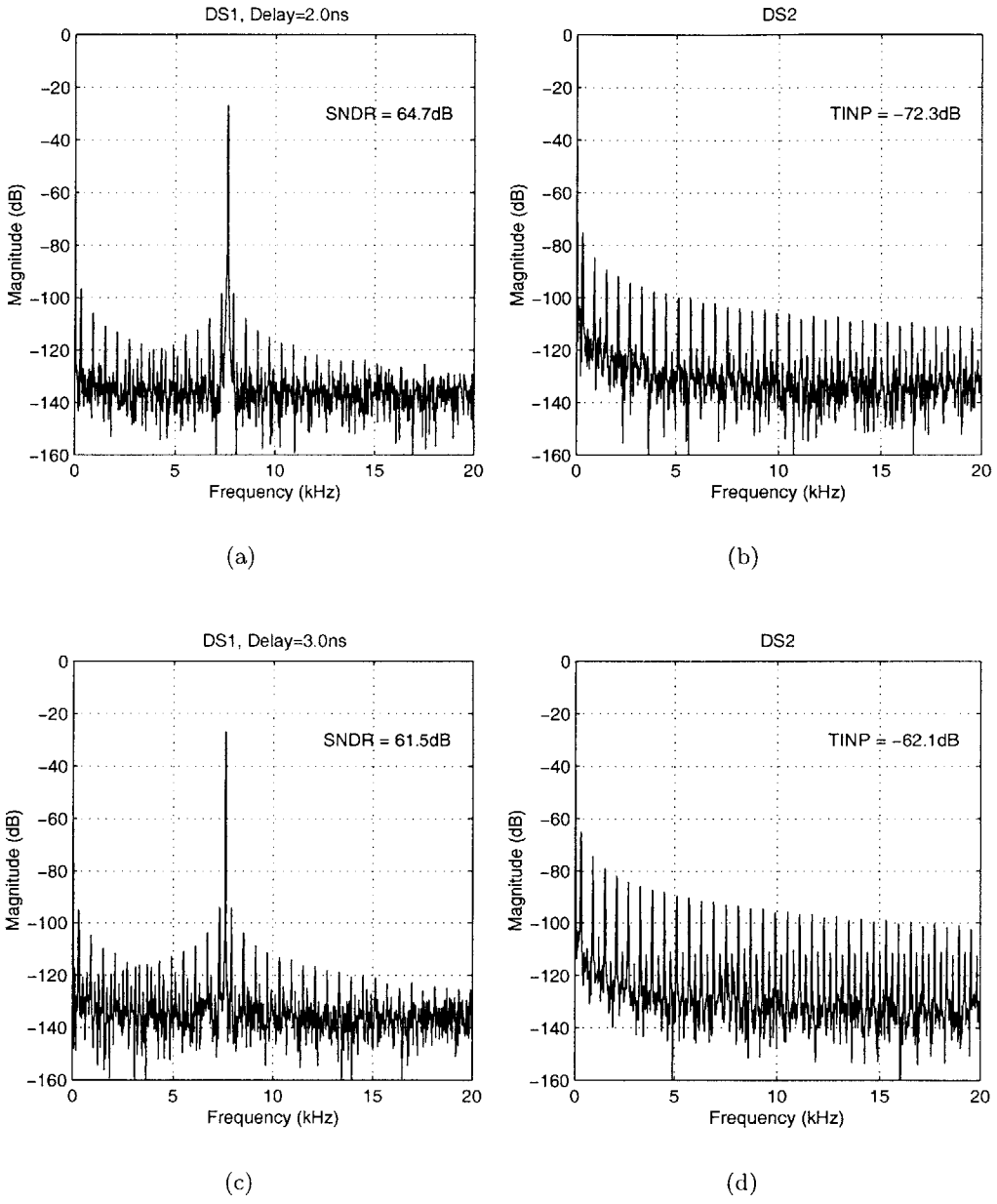
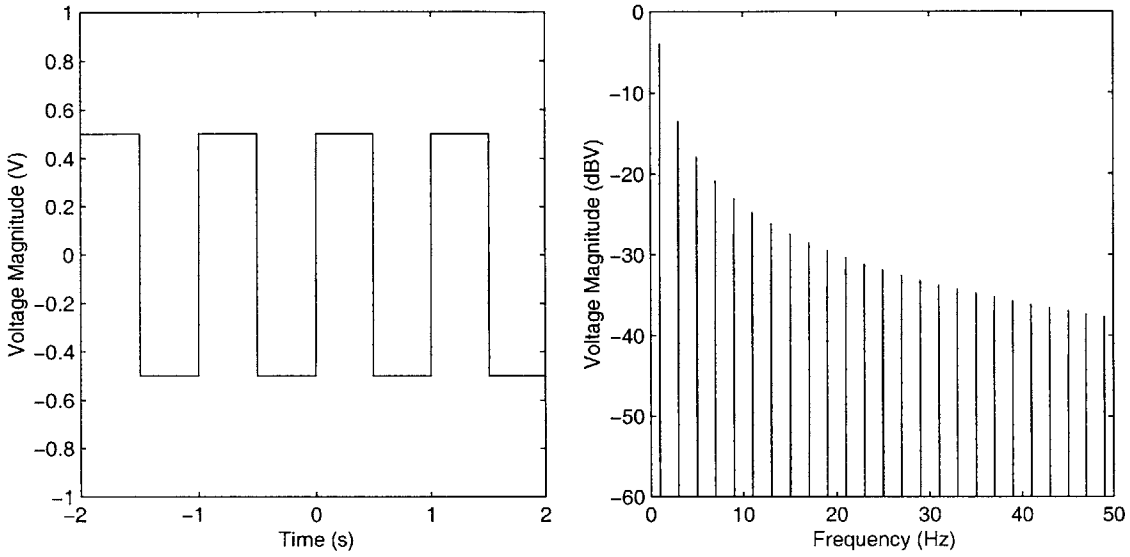


Figure 3-35: Measured delta-sigma modulator output spectra from 0-20kHz with substrate noise. The input to DS1 was a 125mVrms 7.6kHz input tone. Substrate noise was generated by a 300Hz square wave input to InvArrA described in the text. The coupled substrate noise and substrate noise waveforms are shown in Figure 4-22. The delay indicated is DelayA. (a) DelayA=2.0ns, DS1 (b) DelayA=2.0ns, DS2 (c) DelayA=3.0ns, DS1 (d) DelayA=3.0ns, DS2



(a) (b)

Figure 3-36: A 1Hz, 1V peak-to-peak magnitude simulated square wave. (a) Time domain (b) Frequency domain.

than when DelayA was 3.0ns and the TINP increase in DS2 was 20dB, a 10dB improvement than when DelayA was 3.0ns.

As expected from the previous analysis, an additive and mixing copy of the substrate noise spectrum, a square wave with a spectrum shown in Figure 3-36, are seen in the spectrum of DS1. These copies came from the fact that differential asymmetries are caused by input signal independent and input signal dependent factors in the input sampling circuit as well as the reference sampling circuit.

From the spectra of the measured data, the magnitude of the coupled substrate noise and substrate noise square waves sampled in DS1 and DS2 can be inferred. Based on the fourier coefficients of an ideal square wave and using the data in Figure 3-35(c) and (d) (DelayA=3.0ns), the magnitude of the coupled substrate noise square wave seen in DS1 was calculated to be 55uV peak-to-peak and the substrate noise square wave seen in DS2, 2.0mV peak-to-peak. Since the substrate noise was generated with only a quarter of the inverters transitioning, these numbers are in line with the previously stated maximum peak-to-peak magnitudes gleaned from the coupled substrate noise and substrate noise waveforms shown in Figure 3-24.

3.3.5 Differences Between Digital Inverter High-to-Low and Low-to-High Transitions

The amount of coupled substrate noise and substrate noise generated and sampled in DS1 and DS2 respectively, with different numbers of high-to-low transitions and low-to-high transitions in InvArrA at certain DelayA values is shown in Figure 3-37. The x-axis represents the number of high-to-low transitions. A negative number of high-to-low transitions represents a positive number of low-to-high transitions.

From the figure, the first point to notice is that the amount of substrate noise generated with the number of inverters transitioning, the gain, is roughly linear in both the high-to-low and low-to-high transition regions. The second point to notice is that these gains in the high-to-low and low-to-high regions are not the same and depend on DelayA, the difference between the analog sampling clock and the clock that controls InvArrA. This is because of the interaction of the direction independent and direction dependent components of the substrate noise. For example, in Figure 3-37(a), the direction independent component added to the direction dependent component in the low-to-high region, enhancing the gain. On the other hand, the direction independent component subtracted from the direction dependent component in the high-to-low region, diminishing the gain. Furthermore, since the direction dependent and direction independent components are transients that are not necessarily in phase, DelayA affected the gain. In Figure 3-37(c), the direction independent component almost cancels out the direction dependent component in the low-to-high transition region resulting in a very small gain. The final point to notice is that the gain curve of the high-to-low and low-to-high transitions meet at one point implying monotonicity. These points are important for the use of an inverter array like InvArrA for use in an active substrate noise shaping loop discussed in the next chapter. Its monotonicity is important for making a stable loop.

3.3.6 Interchange of DS1 and DS2

As shown in Figure 3-1, DS1 and DS2 can be reconfigured so that they swap roles; DS1 can convert the substrate voltage and DS2 can convert an external signal. Swapping the roles of DS1 and DS2 yielded similar results. This also helps to validate assumption that the low-resistivity substrate is behaving as one node.

In addition to swapping the roles of DS1 and DS2, an off-chip digital noise source connected to the chip through a substrate ground pin was also used. Similar conclusions were made as the substrate noise generated in this fashion affected the analog circuits in the same manner as that presented above.

Figure 3-38 gives a graphical summary of the analyses in this section.

3.3.7 Recommendations

Based on the analysis of data from the coupled substrate noise and substrate noise waveform measurements, recommendations to lessen the effects of substrate noise on analog circuits can be made as follows:

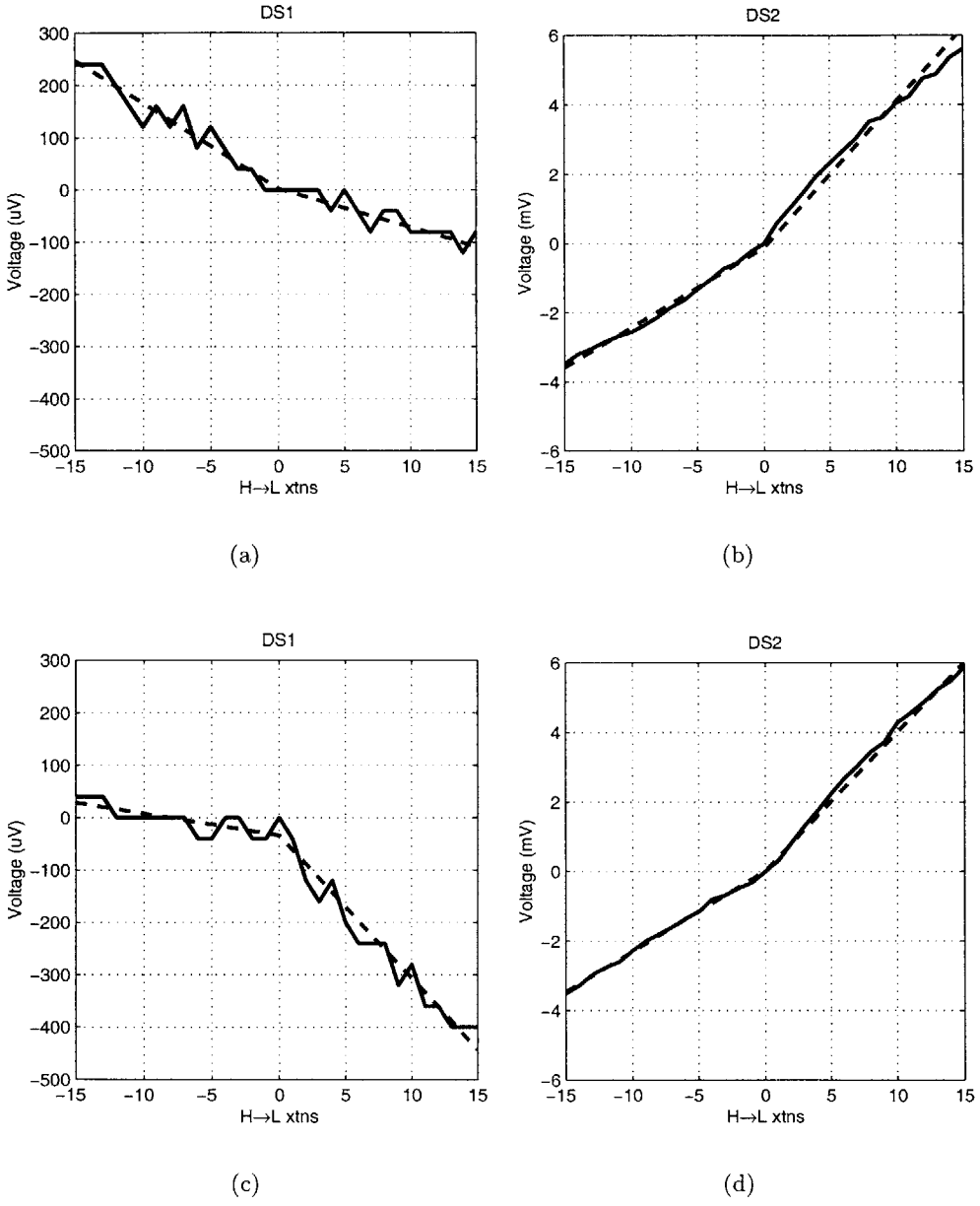


Figure 3-37: Amount of coupled substrate noise and substrate noise sampled versus number of inverters switching. The x-axis represents the amount of high-to-low transitions in InvArrA. Negative numbers represent the number of low-to-high transitions. The dashed lines in each plot represents regression analysis. The delay represents DelayA, the difference between the analog sampling clock and the clock that controls InvArrA. (a) DelayA=2.6ns, DS1 (b) DelayA=2.6ns, DS2 (c) DelayA=4.1ns, DS1 (d) DelayA=4.1ns, DS2.

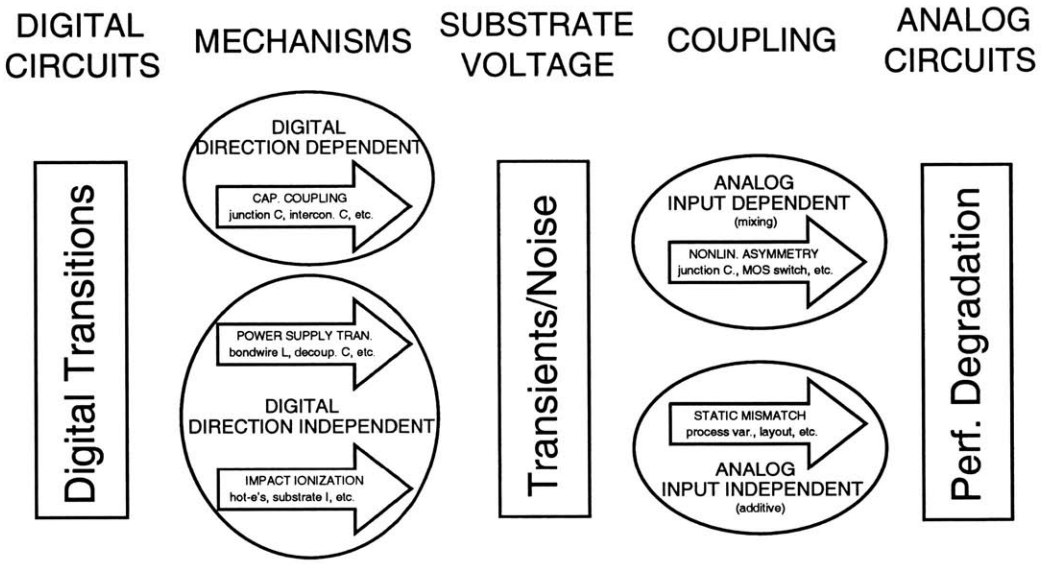


Figure 3-38: Graphical summary of the substrate noise analysis.

1. **Reduce Substrate Noise** – As seen in the data, substrate noise couples into analog circuits with an input signal dependent component and an input signal independent component through the input and reference sampling circuit. Thus any attempt to ameliorate the effects of substrate noise must reduce the substrate noise itself. It cannot be measured and subtracted out unless the input signal, the mismatch between the input and reference sampling circuit, and the substrate noise mixing gain is known.

2. **PMOS switches** – The use of PMOS only switches instead of fully complementary transmission gates (NMOS and PMOS) in bulk CMOS processes provides some isolation for sensitive analog nodes from the substrate because PMOS transistors are usually fabricated in biased n-wells. The n-wells add an extra layer between the PMOS transistor and the p-type substrate that the NMOS transistor doesn't have. Furthermore, separate n-wells can isolate noise from PMOS transistors to PMOS transistors as well.

3. **Minimize Input Sampling Bandwidth** – Besides minimizing for power, input sampling bandwidths should be minimized to reduce the amount of substrate noise that couples into an analog circuit. Equation 3.16 and Equation 3.17 showed that coupled substrate noise can be limited by a low pass characteristic of which the on-resistances of the switches are a factor. Specifically, transistors used as switches should be made as small as possible to decrease the poles so as to attenuate high frequency substrate noise as much as possible. Reducing the input sampling bandwidth may be in conflict with design goals such as distortion due to gain droop of the low pass input sampling transfer function.

4. **Digital/Analog Clock Delay Adjustment** – As seen from the measured data of the coupled substrate noise waveform created by the inverter array, there are time instances at which the coupled substrate noise is at a minimum. Therefore, the delay between digital clock edges that create substrate noise and analog clock edges when vital analog operations are performed should be adjusted so that the amount of coupled substrate noise seen in the analog circuits during these operations is at a minimum. This strategy can be used even if the substrate voltage is not constant because it only requires that the substrate noise or coupled substrate noise is at a minimum. For example, if the digital I/O pad drivers are the major source of substrate noise, then their timing can be adjusted with respect to analog sampling operations. However, this strategy may not work well if the delay at which coupled substrate noise is minimum changes from cycle to cycle because of the pseudo-random nature of digital logic.

3.4 Summary

In this chapter, a system for studying substrate noise affecting analog circuits was explained. It used delta-sigma modulators and sampling scope concepts to reconstruct substrate noise waveforms. This system yielded coupled substrate noise and substrate noise waveforms in a representative analog circuit. These waveforms had decay time constants of a few nanoseconds and ringing frequencies of about 300MHz which implied future mixed-signal chips, with modest digital clocking speeds of a few hundred megahertz will no longer have quiet substrates. Furthermore, the coupled substrate noise sampled in the delta-sigma modulator converting an external signal were the result of input signal dependent and input signal independent asymmetries in the first stage of the delta-sigma modulator. Most importantly, the coupling through the mismatches in the nonlinear junction capacitances of the input sampling stage resulted in a high-pass version of the substrate noise appearing in the delta-sigma modulator input. Having understood substrate noise and substrate noise coupling into analog circuits, some ways of reducing its pernicious effects were prescribed.

Chapter 4

Techniques for Substrate Noise Minimization

The second main thrust of this research was proposing and evaluating techniques for substrate noise minimization. Specifically, this thesis proposed and evaluated two techniques for reducing substrate noise and its effects in analog circuits. The first uses a second delta-sigma modulator, a replica of the first delta-sigma modulator, to correct for substrate noise effects in the first delta-sigma modulator. The second involves an active substrate noise shaping system, which utilizes a feedback loop with an array of digital inverters to cancel out the substrate noise in a certain band of interest. Both techniques were implemented on a National Semiconductor 0.25um CMOS test chip and tested for effectiveness in reducing the harmful effects of substrate noise.

4.1 Correction for Substrate Noise with a Replica Converter

One straightforward method of coping with substrate noise is to use a second delta-sigma modulator, DSB, to correct for substrate noise in the first delta-sigma modulator, DSA[1]. If X_A is the input signal to the first delta-sigma modulator, then the output of the delta-sigma modulator, Y_A is:

$$Y_A = X_A + N_{q,ckt,A} + N_{sub,A} \tag{4.1}$$

where $N_{q,ckt}$ is the sum of quantization and circuit noise (*i.e.* thermal and flicker noise) and N_{sub} is the coupled substrate noise. Similarly, for DSB:

$$Y_B = X_B + N_{q,ckt,B} + N_{sub,B} \tag{4.2}$$

[1]These delta-sigma modulators are the same modulators as that used in the first part of this research, but the second delta-sigma (DS2) has been configured to convert an external analog signal like the first delta-sigma modulator (DS1). Different names have been used to make this distinction clear.

If X_B is zero and Equation 4.2 is subtracted from Equation 4.1 then the result is:

$$Y_A - Y_B = X_A + N_{q,ckt,A} + N_{sub,A} - N_{q,ckt,B} - N_{sub,B} \tag{4.3}$$

If the substrate noise couples into DSA in the same way as substrate noise couples into DSB, then the substrate noise terms, $N_{sub,A}$ and $N_{sub,B}$ will cancel. This results in:

$$Y_A - Y_B = X_A + N_{q,ckt,A} + N_{q,ckt,B} \tag{4.4}$$

Thus, substrate noise can nominally be removed from the first delta-sigma modulator. Note that since circuit noise is uncorrelated noise[2], the noise power of $N_{q,ckt,A}$ and $N_{q,ckt,B}$ sum. This signifies that the circuit noise power of the delta-sigma modulator will double or rise by 3dB, which must be accounted for when designing the delta-sigma modulator in this type of scheme.

For evaluation, output spectra and signal power to noise plus distortion power ratio (SNDR) were compared for the cases of the output of DSA without any correction and the output of DSA with the output of DSB subtracted from it.

4.1.1 System Design

This method requires two copies of a single delta-sigma modulator design as well as digital circuits for substrate noise generation. The system components are shown in Figure 4-1.

As seen in Figure 4-1, DSA accepts and converts an external analog signal. DSB accepts and converts a zero DC voltage. The output of DSB is then subtracted from DSA to correct for the effects of substrate noise[3].

The input DC voltage to DSB was adjusted to account for differences in layout and process variations. From work in the first part of this thesis, it was shown that the DC input voltage of the delta-sigma modulator affects the magnitude of coupled substrate noise appearing at the delta-sigma modulator input.

4.1.1.1 Delta-Sigma Modulators

The delta-sigma modulators used are the same as that used in the first part of this thesis. The design is described and elaborated on in Section 3.1.3.

The two delta-sigma modulators, DSA and DSB are physical replicas of each other to ensure similar substrate noise coupling. Furthermore, they are clocked with the same set of clocks.

4.1.1.2 Digital Circuit for Substrate Noise Generation

The digital circuit used for substrate noise generation is the inverter array, InvArrA, described in Section 3.1.4.

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[2]Noise processes in each transistor is generally assumed to be uncorrelated with other transistors.

[3]The outputs of DSB and DSA were subtracted in software.

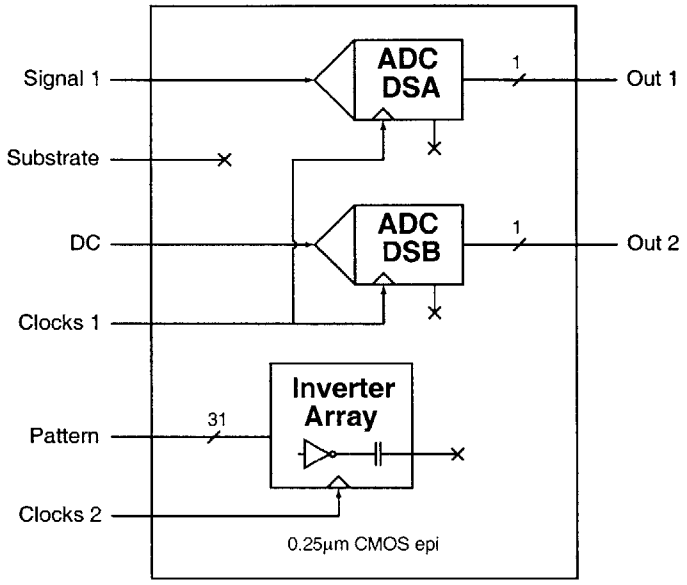
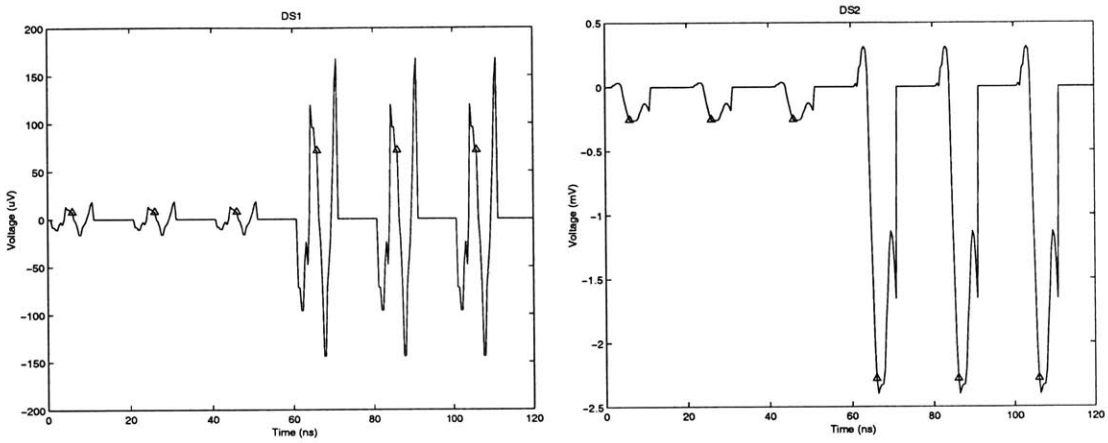


Figure 4-1: System to correct for substrate noise effects in a delta-sigma modulator, DSA, with data from a replica delta-sigma modulator, DSB.

4.1.2 Experimental Results and Discussion

Figure 4-3 shows the spectra of DSA, DSB and DSA-DSB, the corrected spectrum. The input to DSA was a 50mVrms 7.6kHz sine wave. The substrate noise, generated using InvArrA, was a sampled square wave. The input pattern to InvArrA and the resulting substrate noise and coupled substrate noise waveforms are the same as that in the first part of this thesis, described in Section 3.3.4 and shown in Figure 3-33. However, for clarity, the relevant section and figure is repeated here. The input pattern to InvArrA, the substrate noise generator, was a 300Hz 50% duty cycle square wave alternating between the digital values, 7 and 15. Since InvArrA in the *Reset* state has 16 inverters high and 15 inverters low, each analog period has either 9 or 1 high-to-low digital transitions. To be more specific, in a 1.66ms time duration, 9 high-to-low digital transitions in InvArrA occur DelayA before each and every analog sampling operation. During the next 1.66ms, 1 high-to-low digital transition in InvArrA occurs DelayA before each and every analog sampling operation. This cycle then repeats for subsequent 3.33ms periods, thus giving the 300Hz activity rate for substrate noise even though InvArrA is clocked at the analog sampling rate, 5MHz. The inverter array, moreover, can be clocked faster, but it should be noted that faster digital clock speeds may not worsen analog circuit performance since it is DelayA, the relative delay between when substrate noise is created and when analog signals are sampled in the circuits, that is crucial. As long as DelayA is less than a few decay time constants of the coupled substrate noise and substrate noise waveforms, the analog circuits will be affected



(a) (b)

Figure 4-2: Simulated coupled substrate noise and substrate noise waveforms generated by InvArrA over time. InvArrA causes 1 high-to-low transition every analog clock period or 9 high-to-low transitions every analog clock period depending on its input pattern. The triangles indicate the sampled values in DS1 and DS2. Although in continuous time the waveform is constantly changing, the discrete time values form a square wave. The frequency of the clock that controls when InvArrA transitions has been set at about 50MHz for this illustration to more fully illustrate the continuous time transient waveforms because they have ringing frequencies of about 300MHz. In the actual test setup, the frequency of the clock that controls InvArrA is 5 MHz. Furthermore, transients due to reset of the InvArrA have been omitted. The waveforms have been constructed from measured data with some zero padding after the waveforms to allow clear distinction of a clock cycle. (a) coupled substrate noise in DS1 (b) substrate noise in DS2.

by substrate noise. In terms of waveforms, the coupled substrate noise and substrate noise waveforms over many cycles has been constructed with measured data and are shown here again in Figure 4-2. This figure shows that although the continuous time waveform is not a square wave, the values, indicated by the triangles in Figure 4-2, sampled at 5MHz by DS1 and DS2 form a 300Hz 50% duty cycle discrete time square wave.

Also for the data taken, DelayA was equal to 3.0ns. The differential input to DSB was 0V DC.

From Figure 4-3, it is seen that the coupled substrate noise due to input signal independent asymmetries are similar in both DSA and DSB thereby allowing effective cancellation of them. However, input signal dependent components of the coupled substrate noise are not subtracted out because DSB has no input signal. Input signal dependent components dominate the SNDR when the input signal independent components are subtracted out.

In fact, the input signal dependent components can dominate the SNDR even when the input voltage independent components are not subtracted out. This happens when the input signal is large enough to cause the input signal dependent components to have greater magnitudes than the input signal independent components. This is shown in Figure 4-4.

Figure 4-5 shows the effectiveness of using the replica delta-sigma to subtract out effects of substrate noise in terms of the SNDR of DSA. As expected, this technique worked well for small input amplitudes where the input signal independent components dominated the SNDR of DSA. However, it did not work effectively for larger input amplitudes as the input signal dependent components dominate the SNDR of DSA. Notice that at low input amplitudes, even though the coupled substrate noise was mostly canceled out, the SNDR of DSA with corrected output is still about 3dB below the case without substrate noise. This reflects the doubling of circuit noise power when the output of DSB is subtracted from DSA discussed above.

In summary, this technique works well for small input amplitudes and is especially well-suited for applications that have less stringent noise requirements at larger input amplitudes. An example is audio applications where at low input signal amplitudes, a certain amount of noise is unacceptable, but at high input signal amplitudes, the same amount of noise is acceptable.

4.2 Active Substrate Noise Shaping

An interesting technique to reduce substrate noise and its impact on analog circuits is active substrate noise cancellation as mentioned in Section 2.5.7. Since it actually reduces the magnitude of substrate noise, it can reduce input signal dependent and input signal independent components in contrast to the replica technique, which only reduces input signal independent components. This technique can be understood with a simple model of substrate noise.

4.2.1 Simple Model of Substrate Noise

Digital circuits, the major source of substrate noise, create substrate noise because of finite impedances between the circuits and the substrate as well as between the substrate and the power supply, as explained in Chapter 2. For an epitaxial substrate, the substrate can be approximated as one node [8], V_{sub}, and a simple model of digital circuits generating substrate noise, a Thevenin equivalent, is shown in Figure 4-6, which was also shown and discussed in Section 2.3.

One way of keeping the substrate node, V_{sub}, a constant voltage is to add another element that will affect the substrate such as a large capacitively coupled operational amplifier or another set of digital circuits. This element can be controlled with an amplifier that senses the substrate node and compares it to a reference, essentially creating a feedback loop. With proper design of the amplifier's transfer function, the feedback loop can be made to cancel substrate noise generated by the digital circuits. In terms of the circuit model, this scheme adds another digital noise source with a Thevenin equivalent impedance, Z_{digfb}, controlled by an amplifier with transfer function $A(s)$. This is shown in Figure 4-7.

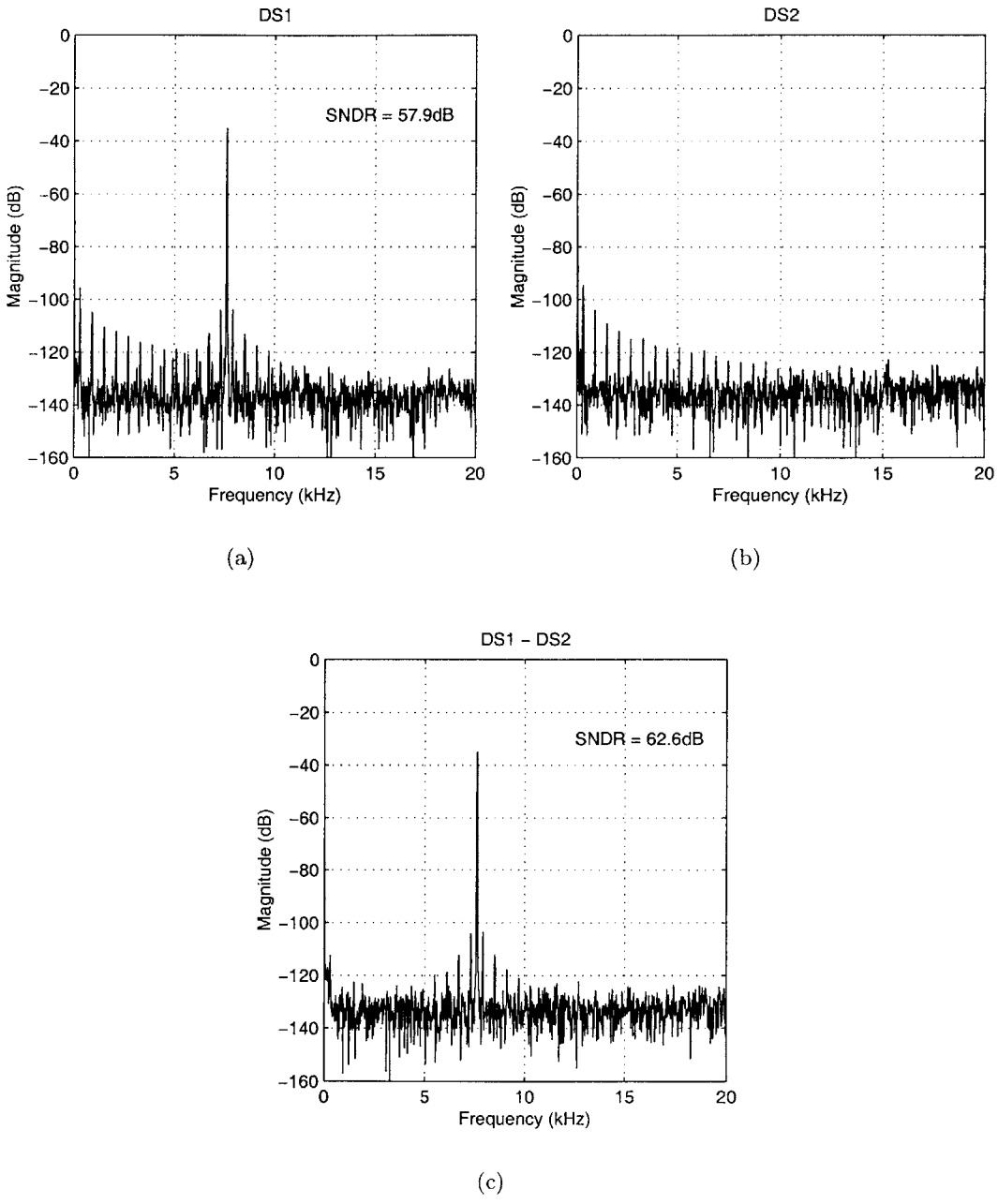


Figure 4-3: Measured data from using a replica delta-sigma modulator to subtract out effects of substrate noise. Differential input to DSA is a 50mVrms 7.6kHz sine wave and the differential input to DSB is 0V. DelayA, the delay between substrate noise generating InvArrA and analog sampling clock is 3.0ns. (a) DSA (b) DSB (c) DSA - DSB.

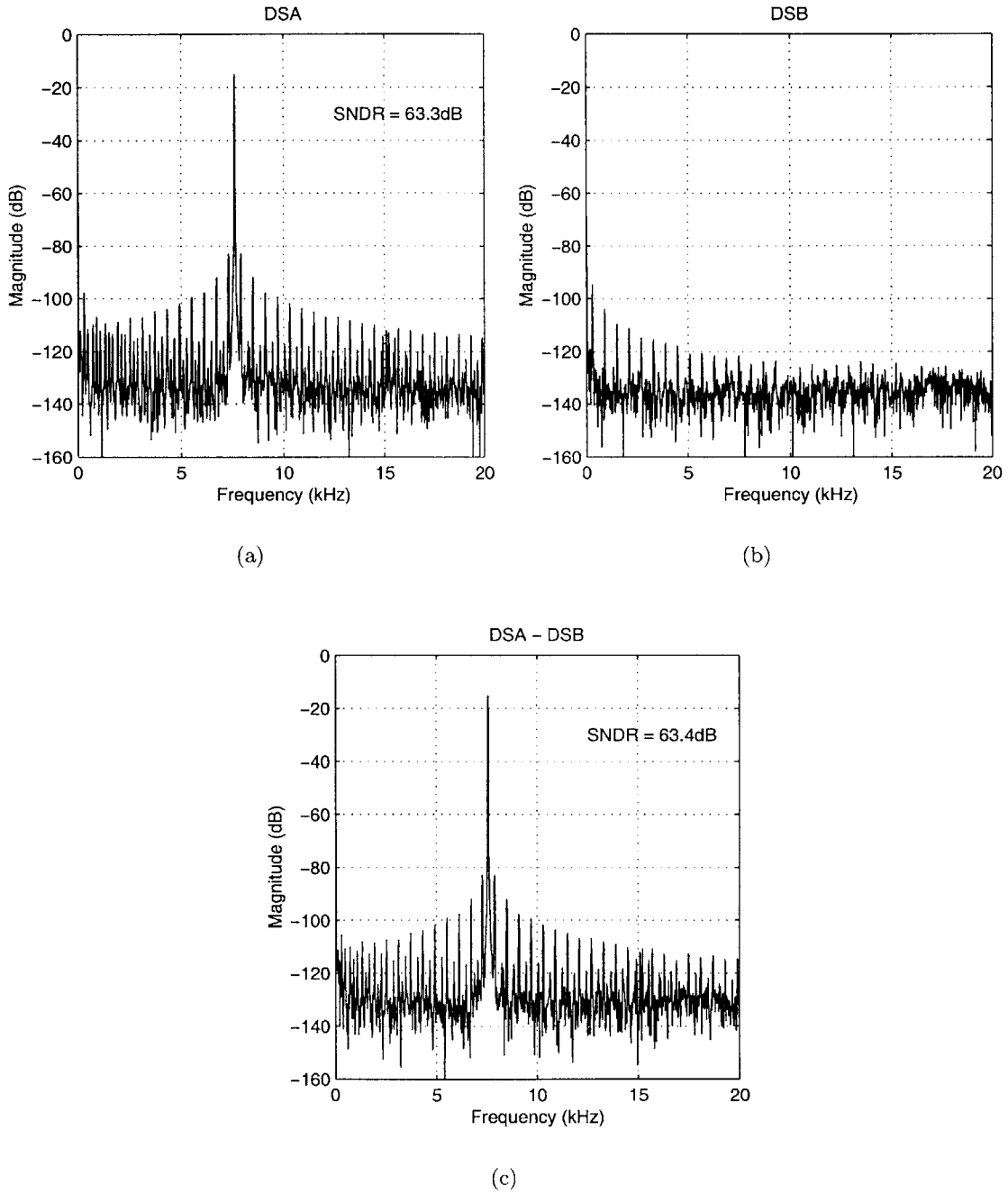


Figure 4-4: Measured data from using a replica delta-sigma modulator to subtract out effects of substrate noise. Differential input to DSA is a 500mVrms 7.6kHz sine wave and the differential input to DSB is 0V DC. DelayA is 3.0ns. (a) DSA (b) DSB (c) DSA - DSB.

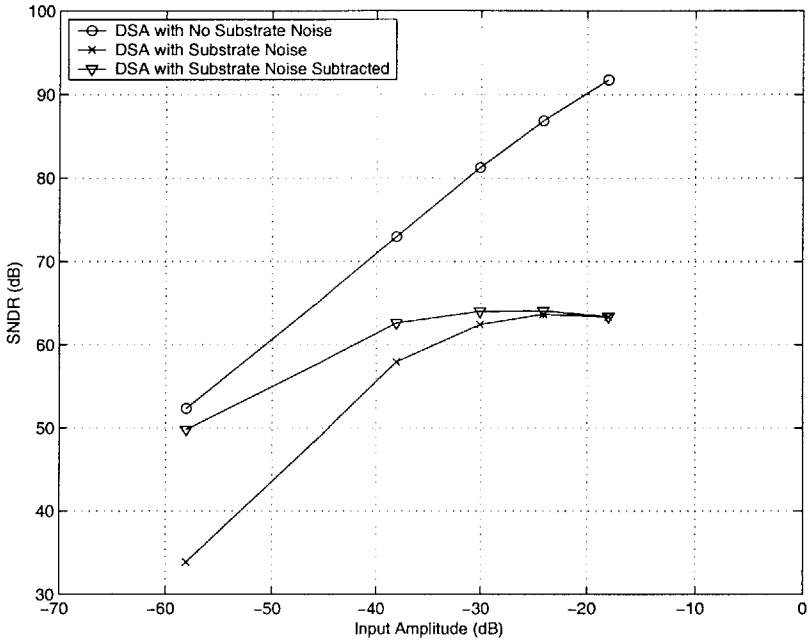


Figure 4-5: Improvement in SNDR of DSA using a replica delta-sigma modulator to subtract coupled substrate noise. Input signal to DSA is a 7.6kHz sine wave.

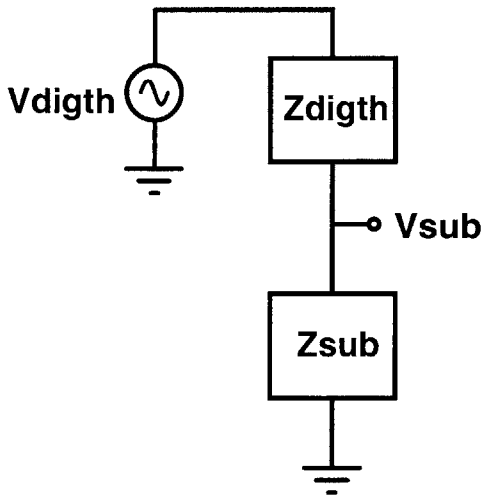


Figure 4-6: Simple circuit model of substrate noise. Digital noise sources have been modeled with a Thevenin equivalent, V_{digth} and Z_{digth}, and impedances from the substrate to the power supply have been modeled by Z_{sub}.

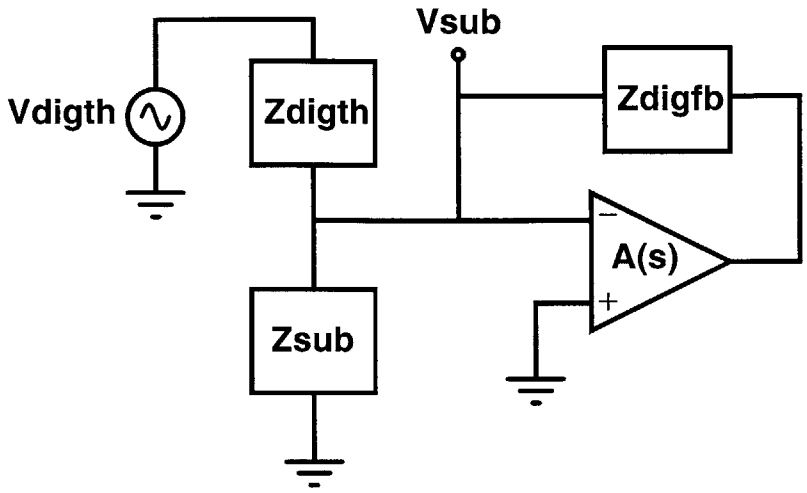


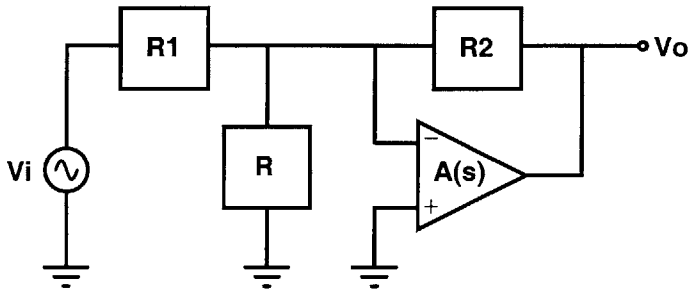
Figure 4-7: Circuit model of substrate with feedback loop added for substrate noise cancellation.

This feedback system can be analyzed by comparing it to an operational amplifier in an inverting configuration shown in Figure 4-8. Using previous analysis [49, pp. 166-167], the block diagram of the inverting operational amplifier can be derived from the circuit as shown in Figure 4-8.

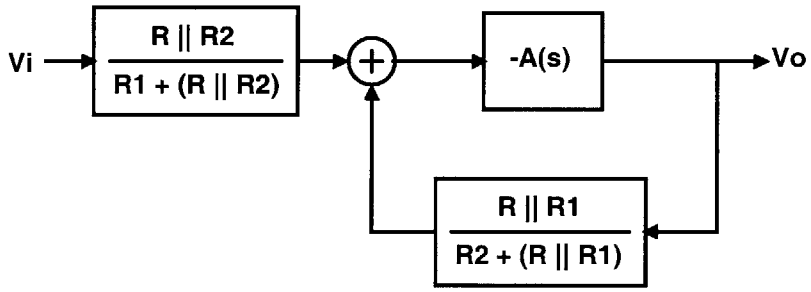
With appropriate substitutions of the model parameters and taking the output at the appropriate point, the circuit model and block diagram of the inverting operational amplifier can be used for the substrate noise feedback system. The circuit model and block diagram for the substrate noise feedback system is shown in Figure 4-9.

In Figure 4-9, the feedback path which includes the amplifier, tries to suppress the substrate noise with "anti-noise". The amount of suppression depends on the gain of the feedback path and the loop dynamics as described in control theory. Although the impedances, Z_{digth}, Z_{sub}, and Z_{digfb} are not easily calculated and thus not well-known, the system can still suppress noise if the amplifier gain is large enough. Furthermore, since the amplifier gain is frequency dependent, the amount of noise suppression will also be frequency dependent. Most amplifiers have low gain at high frequencies and thus substrate noise suppression at high frequencies can be difficult.

An active feedback loop to suppress substrate noise can also be implemented for non-epitaxial substrates. Analysis is similar, however, the substrate can no longer be approximated as one single node and substrate voltage becomes dependent on the geometry of the chip. To use an active substrate noise cancellation system in this case, attention must be paid to the location of substrate noise sensing and the location of anti-noise creation. Most likely an array of feedback loops will be needed to properly suppress substrate noise and its effects in sensitive areas.



(a)



(b)

Figure 4-8: Inverting operational amplifier configuration in Roberge [49, pp. 166-167]. (a) circuit schematic and (b) block diagram.

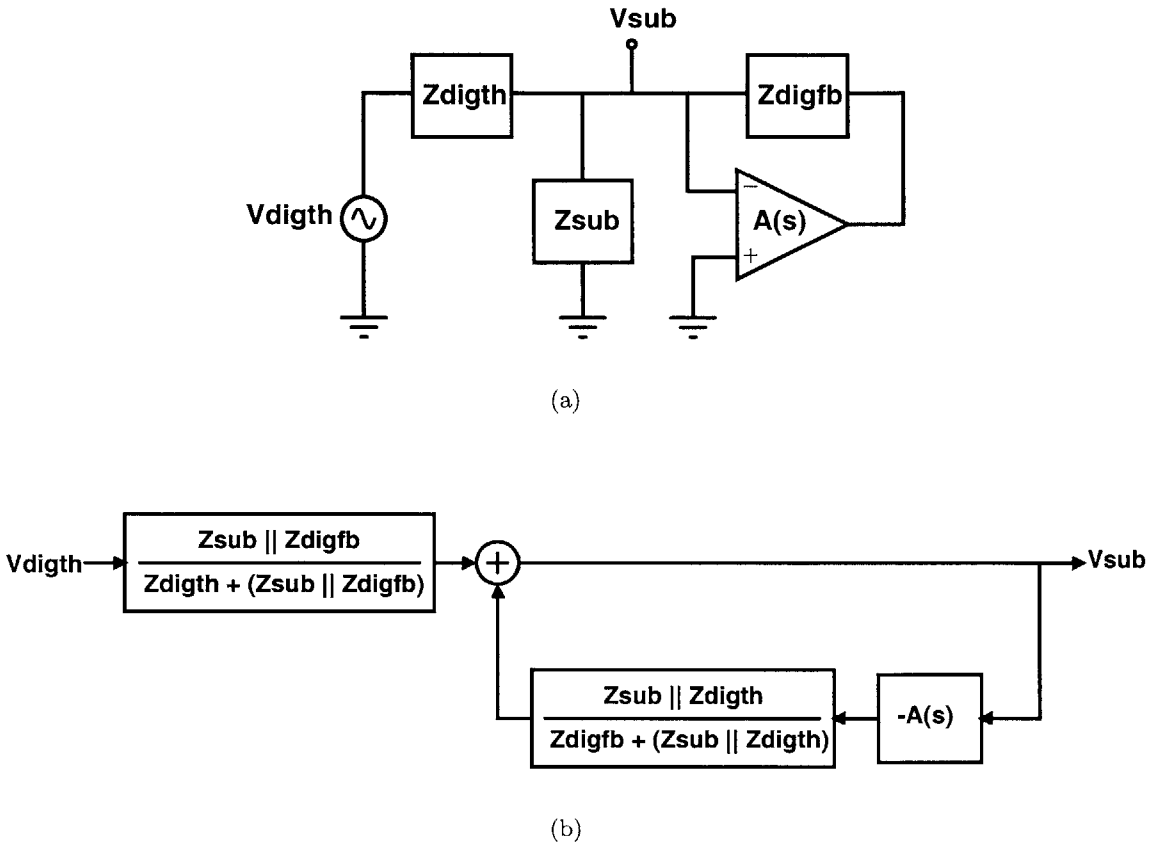


Figure 4-9: Active substrate noise feedback loop. (a) circuit schematic and (b) block diagram.

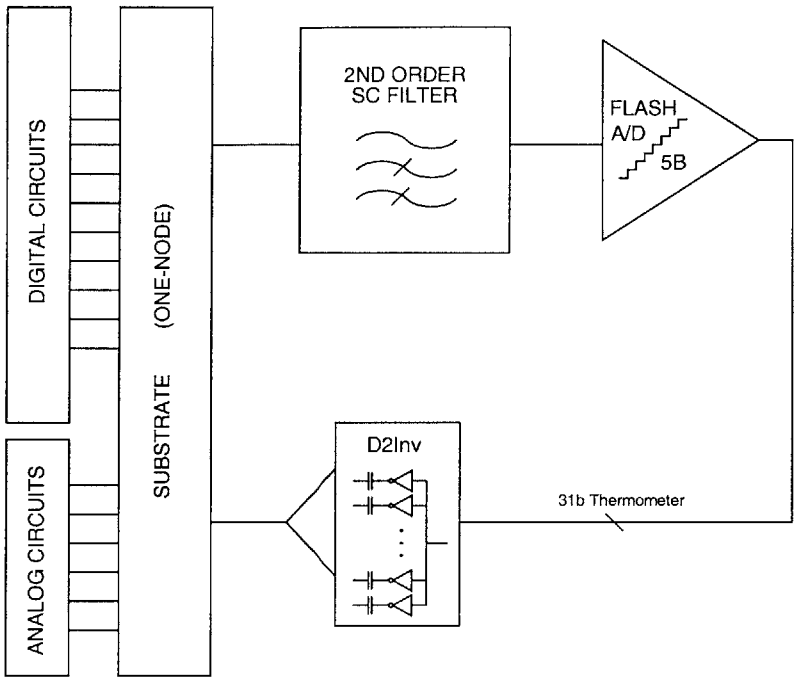


Figure 4-10: Diagram of alternative active substrate noise cancellation system.

4.2.2 Alternative Active Substrate Noise Cancellation System

Past effort has focused on continuous time, wide-band implementations of the active substrate noise cancellation system with large and power hungry amplifiers as feedback elements [34] [35] [36] [37] [38]. This research, in contrast, proposed a discrete-time implementation canceling substrate noise in a small band with an array of digital static CMOS inverters called the "D2Inv" as the feedback element. A diagram of this active substrate noise cancellation system is shown in Figure 4-10.

This approach has many advantages over past ones:

1. **Noise Shaping** – Instead of trying to suppress substrate noise indiscriminately over a large frequency band, only substrate noise in bands of interest are suppressed. This selective noise reduction, known as noise shaping, is achieved by tailoring the loop filter of the feedback loop. This technique is especially useful for applications that have a certain band of interest such as oversampled delta-sigma converters.

2. **Lower Power** – There are three reasons why this technique was lower power than past approaches: (1) By using conventional static CMOS inverters, D2Inv, as the feedback element instead of an analog amplifier, power was consumed only when the inverters switch with the exception of a small amount of static power in the loop filter.

If the substrate noise is large, then many inverters switch to cancel it. On the other hand, if the substrate noise is small, then only a few inverters switch, burning little power. (2) The requirements for the analog circuits in the feedback loop depend on the amount of substrate suppression desired. Since substrate noise suppression targets are not very high (over 20dB reduction is significant), analog circuit performance in the feedback loop can be modest, resulting in lower power designs. (3) Since only substrate noise in certain bands of interest are targeted for suppression, power needs to be spent only in those bands for substrate noise cancellation.

To illustrate the usefulness of this system, a prototype was designed, implemented and fabricated. The prototype consisted of oversampling delta-sigma modulators as analog circuits, large inverters and a complex encryption engine as digital circuits, and the proposed active substrate noise cancellation circuit, herein called the substrate noise shaping loop (SNSL). The SNSL has the same band of interest as the delta-sigma modulators and was designed with a target of 40dB substrate noise suppression over the 0-20kHz band of interest–reducing the substrate noise from hundreds of millivolts to millivolts.

The goal of the prototype is to demonstrate feasibility, not system performance breakthroughs. Therefore, many of the specifications of the system and circuits were chosen conservatively to minimize risks.

4.2.3 System Design

The system to demonstrate the utility of SNSL consists of (1) analog circuits–two low pass delta-sigma modulators, (2) digital circuits–a programmable inverter array simulating pad driver/clock driver circuits and a complex encryption processor simulating arbitrary digital logic, and (3) substrate noise shaping loop circuit. The system with all these components is shown in Figure 4-11.

Many of the components used in this section are the same as ones used in previous sections and information about those designs are referred to in the following sections.

4.2.3.1 Delta-Sigma Modulators

The conservatively designed delta-sigma modulators used were the same as those described in first part of this work, Section 3.1.3 on Page 48. Furthermore, their configurations are the same and they will also be referred to as DS1 and DS2. DS1 converts an external off-chip analog signal so its output shows coupled substrate noise. DS2 converts the substrate voltage through a substrate contact and its output shows substrate noise.

4.2.3.2 Digital Circuits

Digital circuits representative of the two major sources of substrate noise are included on this test chip: (1) array of digital inverters used in the first part of this thesis, InvArrA, which is similar to digital pad drivers and clock buffers and (2) complex encryption engine which is a circuit that implements digital logic functions. The effectiveness of the SNSL in

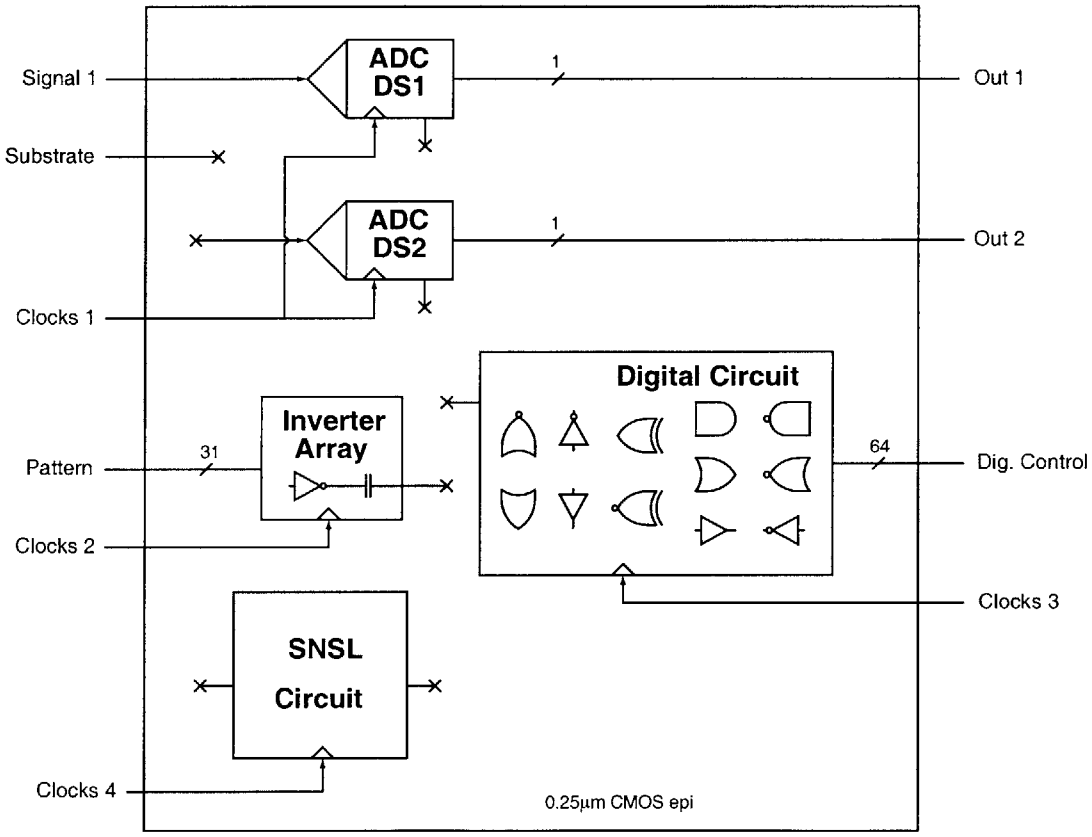


Figure 4-11: System for demonstrating substrate noise shaping.

response to substrate noise generated by both these types of digital circuits was evaluated and analyzed.

The InvArrA with large buffered inverters driving large capacitances simulates substrate noise generated by pad drivers and clock buffers. The InvArrA, used in the first part of this work, is described in Section 3.1.4.

The digital encryption engine, the Domain Specific Reconfigurable Cryptographic Processor (DSRCP), simulates the substrate noise generated by arbitrary digital logic. The circuit was designed by Goodman [3]. It optimizes the tradeoff of encryption level and power consumption. The encryption engine is a stand-alone component in that it only shares the substrate with the delta-sigma modulators and SNSL. Everything else such as power supplies has been separated. This digital design contains approximately 880,000 devices and consumes about 10mW in the most power intensive configuration (*i.e.* highest level of encryption).

This encryption engine is a synchronous circuit in that the digital circuits are all triggered on the rising edge of the digital clock. However, the number of cycles for completion of a particular instruction is not fixed and depends on the instruction as well as the encryption level.

This digital circuit was run at 20MHz, four times the analog clock frequency. The digital circuit is instructed to perform an arithmetic function called exponential modulation repeatedly. One of the operands of the function is the result of the previous execution so that the number of digital circuits switching is pseudo-random. This instruction does not drive any output pads. Data is stored internally and only output to the pads when explicitly instructed to do so.

For convenience, the delay between the analog sampling edge and the rising edge of the clock that controls InvArrA will be referred to as DelayA and the delay between the rising edge of the clock that controls the DSRCP and analog sampling edge will be referred to as DelayB. Note that DelayB only represents the delay between the rising edge of the master clock of DSRCP and analog sampling edge. Clocks to digital circuits in DSRCP are internally buffered and triggered at a later time.

4.2.3.3 Substrate Noise Shaping Loop (SNSL)

The design of the SNSL was, for the most part, straightforward. The target amount of substrate noise suppression on the substrate voltage, 40dB (substrate noise suppression from hundreds of millivolts to millivolts), coupled with the analog clocking frequency, 5MHz, determined the performance requirements of the individual components of the SNSL. Unfortunately, the amount of substrate noise created by the D2Inv was not well-described and not known in advance. Therefore, extra flexibility was designed into the chip to manage this unknown quantity as described in later sections.

4.2.3.3.1 Architecture The schematic diagram of the SNSL is shown in Figure 4-10. A linearized model for analytical purposes is shown in Figure 4-12. The loop filter, a switched capacitor filter, is represented by standard gain blocks such as adders, gains, and

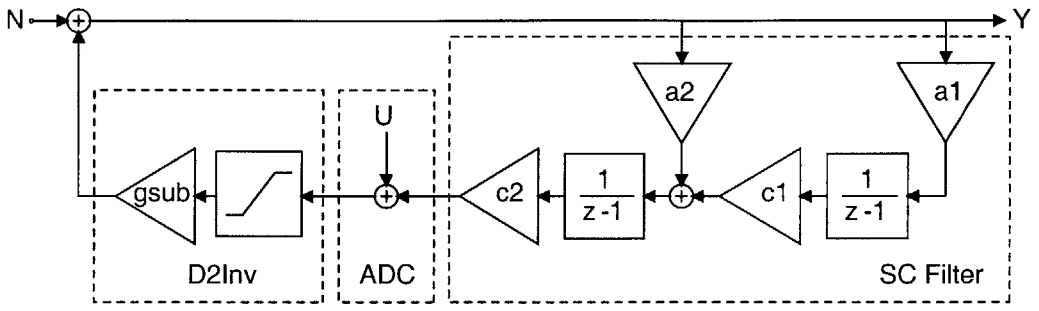


Figure 4-12: Linearized block diagram of substrate noise shaping loop (SNSL).

integrators. The 5 bit ADC is represented as adding a quantization noise[4], U. Since the ADC is a 5 bit converter, U is relatively small when referred to the input of the loop and compared to the substrate noise magnitude. Therefore it is ignored in further analysis. The D2Inv is represented as a gain, *gsub* and a limiter. This combination implies that the D2Inv will not produce a full rail to rail substrate voltage waveform, but rather a waveform with a much smaller magnitude. The exact magnitude depends on *gsub*, which in turn depends on the fabrication process, physical layout, packaging, etc. as well as the time at which analog values are sampled by the SNSL. This gain may also be nonlinear since it is based on parasitics such as junction capacitance. However, since the substrate noise magnitude is small, a linear approximation was useful for analyzing and designing the system[5]. The limiter was also included to represent the limited dynamic range of the D2Inv in producing substrate noise.

The SNSL was designed as a second order loop. The choice of order was based on the desire for maximum stability while still ideally achieving at least 40dB of substrate noise rejection in the band of interest.

The structure of the loop filter for the SNSL was chosen to be a cascade of integrators and is shown in Figure 4-12. The coefficients for the filter were generated by the Delta-Sigma Matlab Toolbox [42][6]. *gsub* was assumed to be 0.25 in the model for subsequent analysis[7].

The loop filter was designed so that the two closed loop zeros are coincident on the point $(0, 1)$ in the z-plane as shown in Figure 4-13. This was done for simplicity. More noise suppression could have been achieved by distributing the zeros throughout the band of interest, but the cost would have been extra circuitry and a higher possibility of instability.

[4]Quantization noise is usually modeled as a white noise source [33, pp. 4–5].

[5]As determined measured data presented in Section 3.3.5, the gain of the inverters was fairly linear. Only a discontinuity in slope was observed at the center point where there is a changeover from high-to-low transitions to low-to-high transitions.

[6]The Delta-Sigma Matlab Toolbox is essentially a filter design tool with extra functions for delta-sigma behavioral simulations.

[7]A *gsub* of 0.25 meant that the D2Inv could produce up to 1V of substrate noise for a full-scale of 4V.

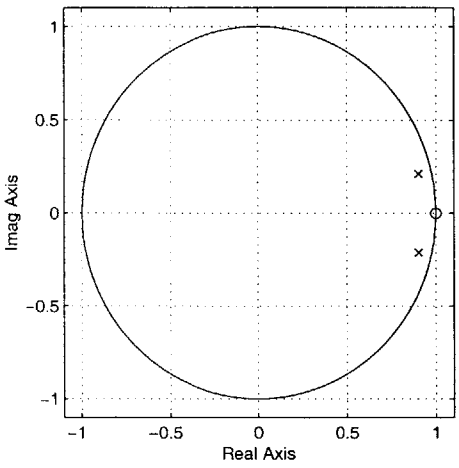


Figure 4-13: z-plane pole-zero diagram of the closed loop SNSL. Two zeros are coincident at the point $(0, 1)$.

The bode magnitude plot of the closed loop is shown in Figure 4-14. As seen in the figure, the closed loop transfer function has a high pass characteristic. For the band of interest, the substrate noise suppression is at least 40dB.

The SNSL was also behaviorally simulated in Matlab's Simulink. The Simulink model is shown in Figure 4-15. Different input sources with different magnitudes were used as substrate noise sources (*i.e.* Gaussian noise, uniform random noise, sine waves). In every case, over 40dB suppression of substrate noise was observed. The input magnitudes used in these cases never saturated the SNSL.

4.2.3.3.2 Effect of *gsub* on Stability and Substrate Noise Suppression As stated before, the amount of substrate noise created by the D2Inv, represented by *gsub*, was not well known during design of the SNSL. This was because it depended on processing, physical layout, and chip packaging which are all very difficult to calculate separately, let alone together. Since *gsub* may not be exactly what it was assumed to be, the effect of any deviation must be understood in terms of feedback loop behavior.

In terms of stability, *gsub* affects the open loop gain without modifying the open loop phase characteristics. The open loop magnitude and phase of this discrete time system, with *gsub* set to 0.25, are plotted in Figure 4-16.

The frequency response plots show that at the current crossover frequency, the frequency at which the open loop gain is unity, the phase is about -150 degrees, which means the loop is stable. In fact, at a large range of frequencies near the crossover frequency, the phase is much greater than -180 degrees. This means any small deviations in *gsub* from the design value will most likely result in a functional system. However, if a deviation in *gsub* results in a phase just greater than -180 degrees, the system may not be usable because the system

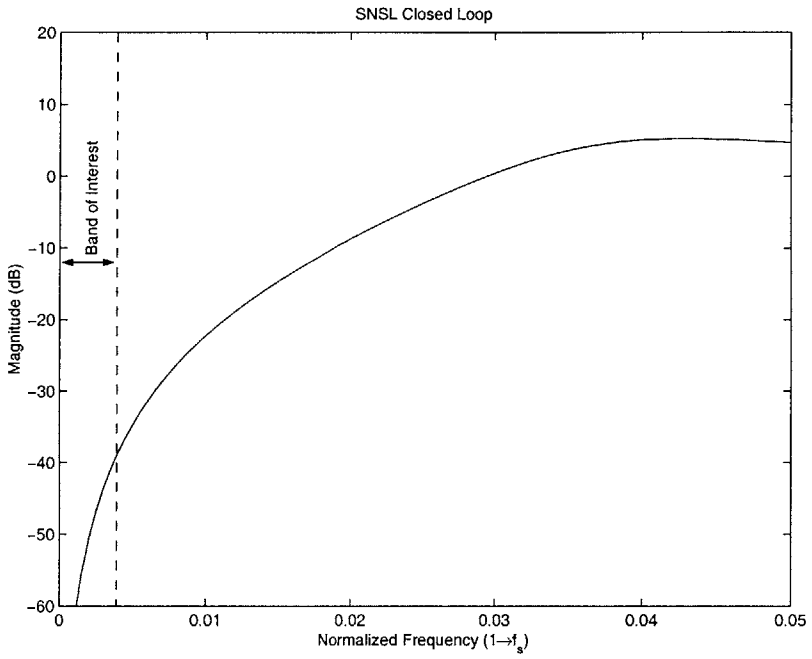


Figure 4-14: Bode magnitude plot of the closed loop transfer function of SNSL.

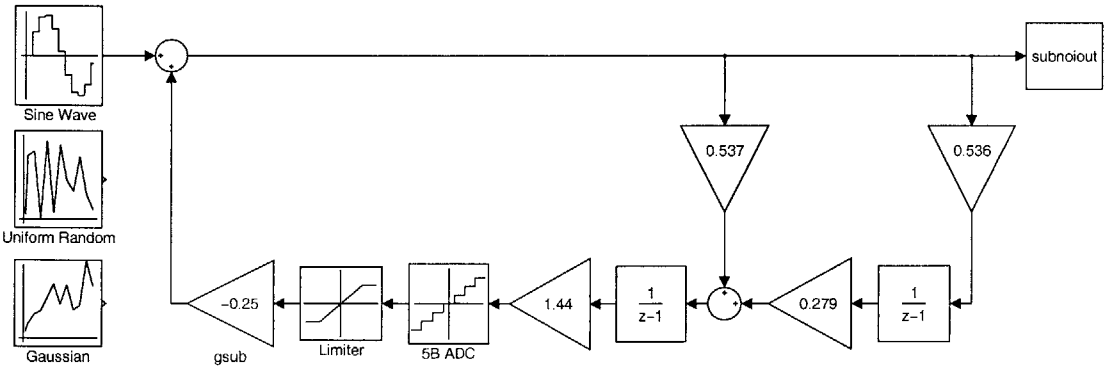


Figure 4-15: Matlab Simulink model of the SNSL.

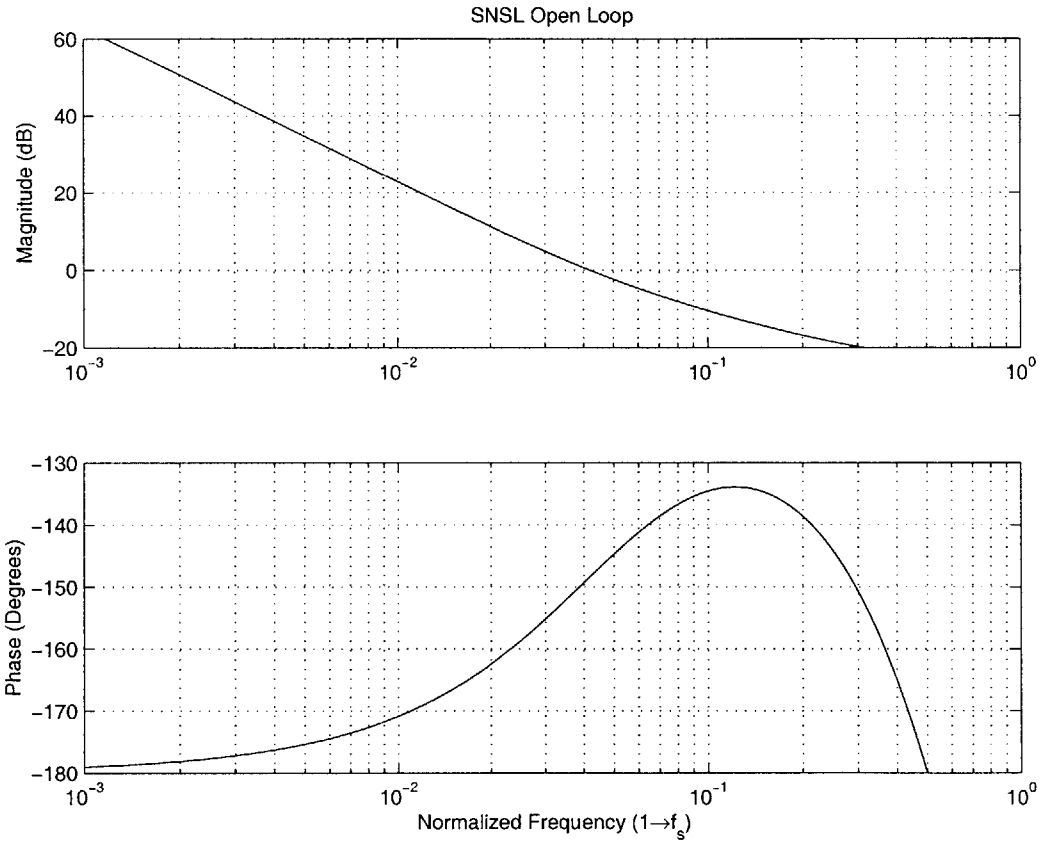


Figure 4-16: Frequency response of the open loop discrete time transfer function of the SNSL.

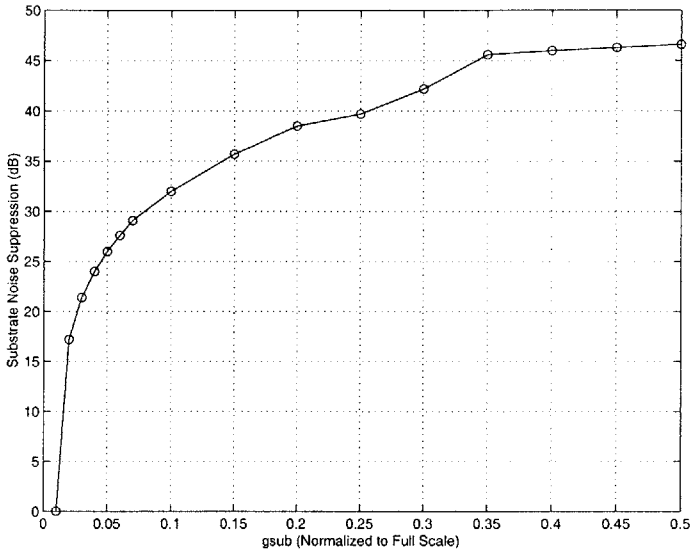


Figure 4-17: Effect of different *gsub* (gain/dynamic range) on substrate noise shaping effectiveness. The substrate noise source is a 0.02 of full scale sine wave at the upper edge of the band of interest.

will have large oscillations which will saturate the system. Setting the phase at -170 degrees for a functional system, the *gsub* needs to be in the range from 0.025 to 2.5 for the system to be functional.

Since the open loop gain affects the closed loop characteristics, *gsub* will also affect the amount of substrate noise suppression in the band of interest. In addition, *gsub* will affect the dynamic range of the SNSL. If the substrate noise is too large, then the SNSL will saturate. Since the loop is only second order, the SNSL can recover after saturation. This results in some substrate noise suppression, even if the SNSL saturates. These effects are shown in Figure 4-17, which plots substrate noise suppression in the normalized band of interest based on data from behavioral simulations. The substrate noise was a sine wave with a frequency close to the upper edge of the band of interest and a magnitude of 0.02 of full scale. The graph can be divided into 2 regions. The first is *gsub* above 0.02. In this region, the SNSL does not saturate because its dynamic range is large enough. The substrate noise suppression decreases for smaller *gsub* because the open loop gain decreases. The second region is *gsub* less than 0.02. This is when the SNSL saturates because it cannot produce a feedback signal large enough to match the input signal. Substrate noise suppression drops dramatically, but partial cancellation of the substrate noise is still seen.

4.2.3.3.3 Circuit Implementation The circuit schematic of the SNSL is shown in Figure 4-18. Translation into circuits from the block diagram was straightforward. The substrate, as illustrated, was treated as one node.

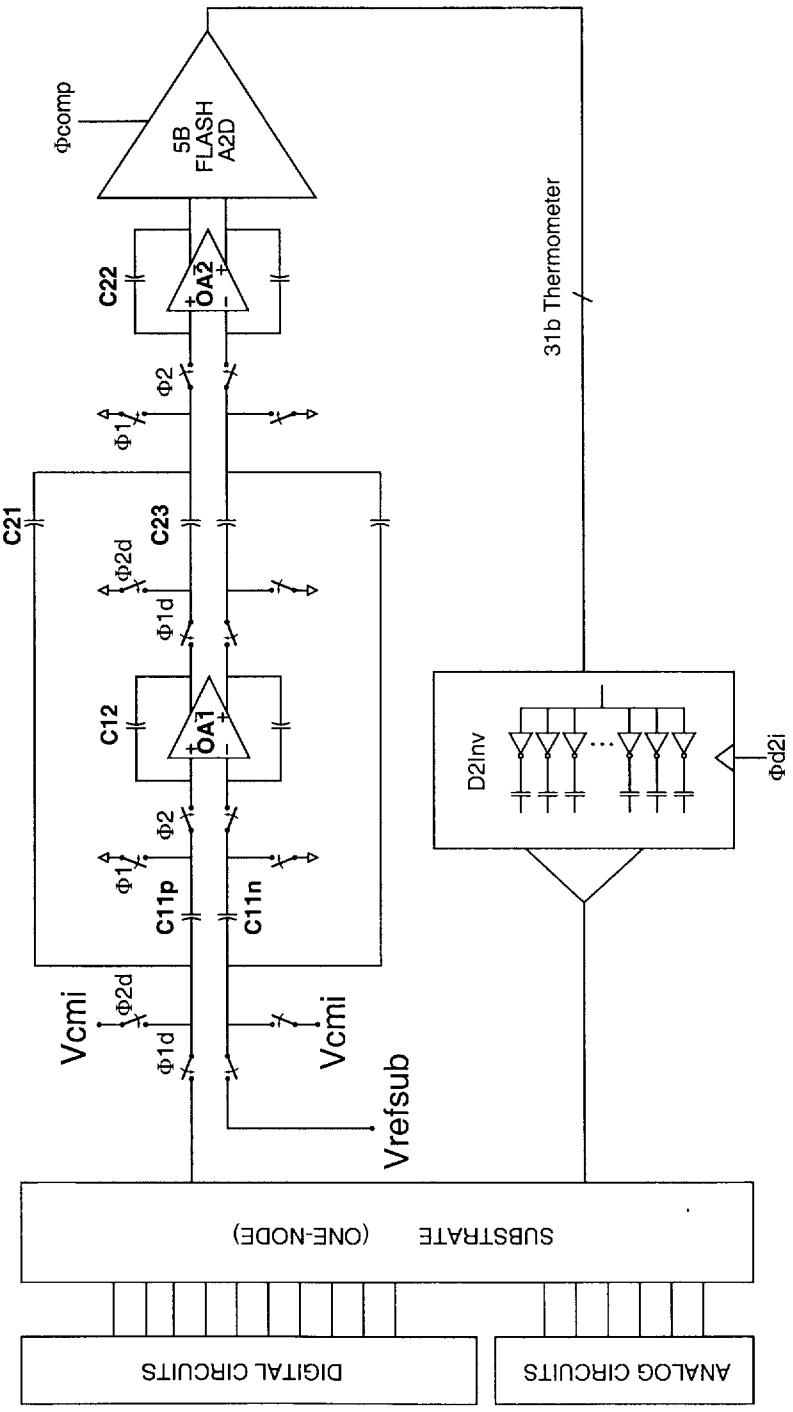


Figure 4-18: Circuit schematic of the substrate noise shaping loop. Clocking is the same for both sides of the differential circuit.

Stage	$Cn1$	$Cn2$	$Cn3$
1	500	932.92	–
2	192.45	358.34	100

Table 4-1: SNSL capacitor sizes (in fF).

4.2.3.3.4 Substrate Noise Sensing For sensing, the substrate voltage, through a substrate contact, is connected to the positive differential input of the SNSL while the negative differential input is connected to an adjustable reference voltage, V_{refsub}. This configuration is the same as that of DS2. V_{refsub} is used to cancel any DC offsets of the substrate noise. For example, a periodic current spike will create substrate noise. However, if the current spike does not change in shape, then it will create the same amount of substrate noise every analog sampling period resulting in a DC signal for the sampled substrate noise. This DC substrate noise is not be a problem for many systems and was ignored in any performance metrics.

Since the nominal substrate voltage is the lower power rail voltage, then V_{refsub} in Figure 4-18 is set to the lower power rail voltage to minimize the differential input DC voltage. V_{cmi} is also set to V_{ref} so that the common mode voltage of the top plates of C_{11p} and C_{11n} is roughly the same during Φ_1 and Φ_2.

4.2.3.3.5 Switched Capacitor Filter The switched capacitor filter was implemented differentially, with coefficients generated by the delta-sigma toolbox, essentially a filter design tool. The coefficients were scaled for maximum dynamic range with SWITCAP [50] before being used to determine capacitor ratios. The capacitor ratios coupled with minimum capacitor sizes in each stage determined capacitor sizes. The minimum capacitor size in the first stage is 500fF for keeping kT/C noise small[8] and providing some low pass filtering for the input of the switched capacitor filter. 100fF, a reasonable size for good matching, is the minimum capacitor size for the second stage. These poly-to-poly capacitors, which have non-integer ratios, were realized with the same technique used for the delta-sigma modulator capacitors described in Section 3.1.3.2.

The switched capacitor filter is clocked by the same clocks used for the loop filter of the delta-sigma modulator to maintain similarity between the SNSL and delta-sigma modulators.

4.2.3.3.6 Operational Amplifiers The operational amplifiers used for the SNSL are of the same design as the ones used in the second, third, and fourth stages of the delta-sigma modulator. This operational amplifier is a scaled-by-ten version of the base operational amplifier discussed in Section 3.1.3.3. This was done for simplicity and design reuse. Based

[8] 100fF was actually enough for the substrate noise levels anticipated (millivolts), but a larger capacitor was chosen for overdesign.

on worst case simulations, the operational amplifiers satisfy the settling requirements and noise requirements of the SNSL for their given configurations in the switched capacitor filter.

4.2.3.3.7 D2Inv The D2Inv, an array of inverters with coupling capacitors serves as a DAC in the SNSL and creates the anti-noise in the substrate to cancel out the substrate noise generated by the digital circuits. It is exactly the same as InvArrA, which is used to generate substrate noise. InvArrA is discussed in the first part of this research in Section 3.1.4.

This array of inverters using equal size elements and thermometer encoding as opposed to binary weighted elements, ensures monotonicity and linearity of the anti-noise substrate feedback signal.

The clocking to the D2Inv is independent of all other clocks on the chip. It can be adjusted with respect to the analog sampling clock so that the D2Inv generates the greatest amount of substrate signal sampled in the SNSL for maximum dynamic range. The amount of substrate signal sampled in the delta-sigma modulator versus the delay is shown in the first part of this work in Figure 3-24. For convenience, the delay between the analog sampling edge and the rising edge of the clock that controls D2Inv will be referred to as DelayX, which may be different in value from DelayA or DelayB.

4.2.3.3.8 5 Bit FLASH ADC The performance requirements on this ADC in the SNSL are not stringent. The SNSL runs at the same clock frequency as the delta-sigma modulator, 5MHz.

A flash architecture was chosen for the ADC because of its straightforward implementation and thermometer code output which is used without conversion by the D2Inv. In total, 31 clocked differential comparators are used to generate the output word. The circuit schematic of this flash ADC is shown in Figure 4-19. It is based on a previous implementation [33, p. 238].

Each clocked differential comparator makes a decision based on the difference between the differential reference ladder voltage and differential input voltage. For example, in the seventeenth differential comparator, when Φ_1 falls, the appropriate reference ladder voltages, V_{r17} and V_{r15}, are sampled onto the input sampling capacitors, C_{17p} and C_{17n}, respectively. Φ_{1d} falls slightly later to minimize the effect of signal dependent charge injection. During Φ_{2d}, the differential input voltages, V_{ip} and V_{in}, are connected to the capacitors, C_{17p} and C_{17n}, respectively. As a result, the comparator inputs, $V_{comp17p}$ and $V_{comp17n}$ get the voltages, $V_{ip} - V_{r17}$ and $V_{in} - V_{r15}$, respectively, since the capacitors do not change in charge and thus voltage during Φ_{2d}. Next, Φ_{comp} goes high triggering the comparator evaluation before Φ_{2d} falls. Thus, the comparator decision is based on the differences between the comparator inputs when Φ_{comp} goes high:

$$\begin{aligned} V_{comp17diff} &= V_{comp17p} - V_{comp17n} \\ &= (V_{ip} - V_{r17}) - (V_{in} - V_{r15}) \\ &= (V_{ip} - V_{in}) - (V_{r17} - V_{r15}) \end{aligned} \tag{4.5}$$

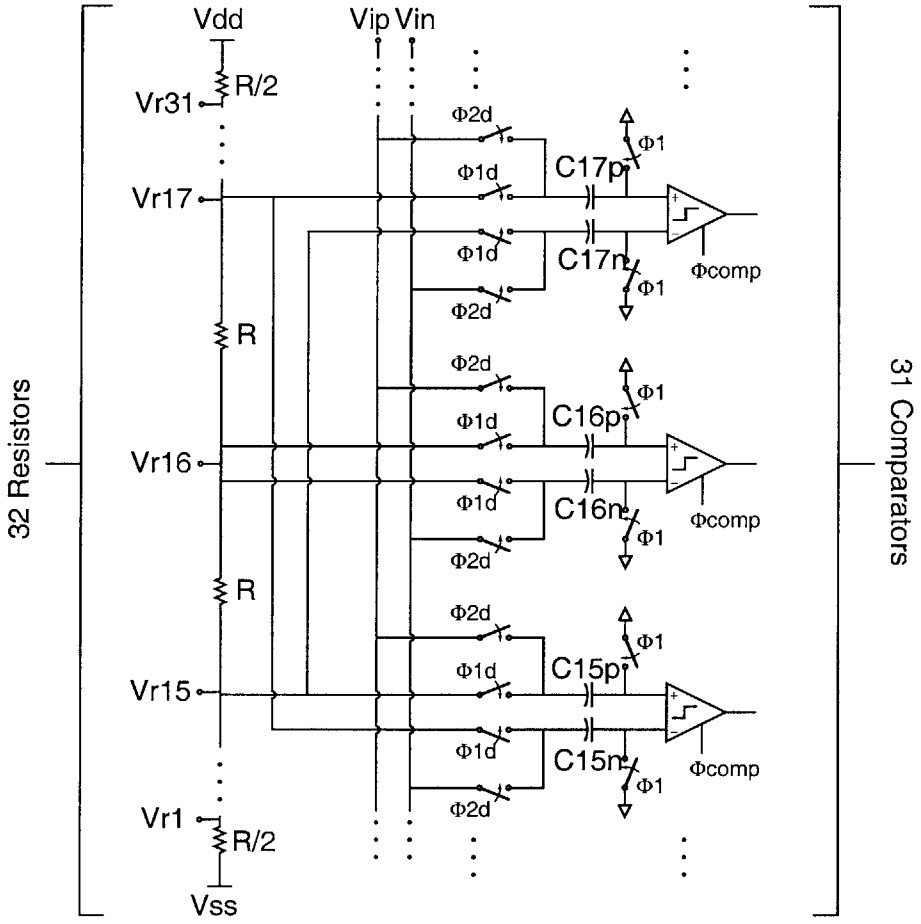


Figure 4-19: Circuit schematic of the 5 bit differential FLASH ADC used in the SNSL.

The other comparators operate in a similar manner except with different reference ladder voltages.

The comparator core used is the same as the one used for the one bit ADC in the delta-sigma modulator loop discussed in Section 3.1.3.6. A chain of resistors provides the necessary reference ladder voltages as indicated in the Figure 4-19.

No special techniques are used to increase performance of this 5 bit ADC because of the low resolution and the low performance requirements of the SNSL. High linearity is not necessary because the input signal, the substrate noise, does not need to be preserved. Moreover, the ADC non-idealities are second order shaped when referred to the input of the SNSL.

4.2.3.3.9 Flexibility Many different controls and signal outputs were designed into the chip to provide maximum flexibility for testing.

One of the chief problems of designing the SNSL was estimating the magnitude of substrate noise and the substrate signal the D2Inv could generate . As mentioned before, substrate noise depends on processing, physical layout, and chip packaging, all of which were hard to predict. As a consequence, estimates of substrate noise generated by the digital circuits were made during design based on past research and personal communications. Controls allowed flexibility for increasing or decreasing the magnitude of substrate noise sampled by the SNSL in the event that it was not the same as the estimates made:

- Sampling Clock Adjustment – As seen in the first part of the work, the time at which analog circuits sample the input signal determine the sampled magnitude of substrate noise. By adjusting the analog sampling clock, the magnitude of substrate noise sampled by the SNSL can be increased or decreased. For example, to obtain smaller SNSL sampled magnitudes of substrate noise, the analog sampling edge could be set far away from the digital clock that triggered the substrate noise generating digital circuits (*i.e.* increase DelayA or DelayB).

- Number of Ground Pins – The substrate impedance, and thus the substrate noise peak magnitude can easily be increased by decreasing the amount of parallel pins connecting the substrate to ground. This increases impedance from the substrate to ground.

- DSRCP Encryption Level – The DSRCP trades off encryption level for power consumption. Higher encryption levels (*i.e.* longer word lengths) use more digital circuits and thus, generate more substrate noise.

- Supply Voltage – The supply voltage can be lowered to slow down transitions and decrease current draws to generate less substrate noise. Vice versa, the supply voltage can be raised to speed up transitions and increase current draws to generate more substrate noise.

Many other adjustments and diagnostic outputs were designed in at the circuit level. A more detailed circuit schematic of the SNSL including these diagnostic outputs and control inputs is shown in Figure 4-20. They are described as the following:

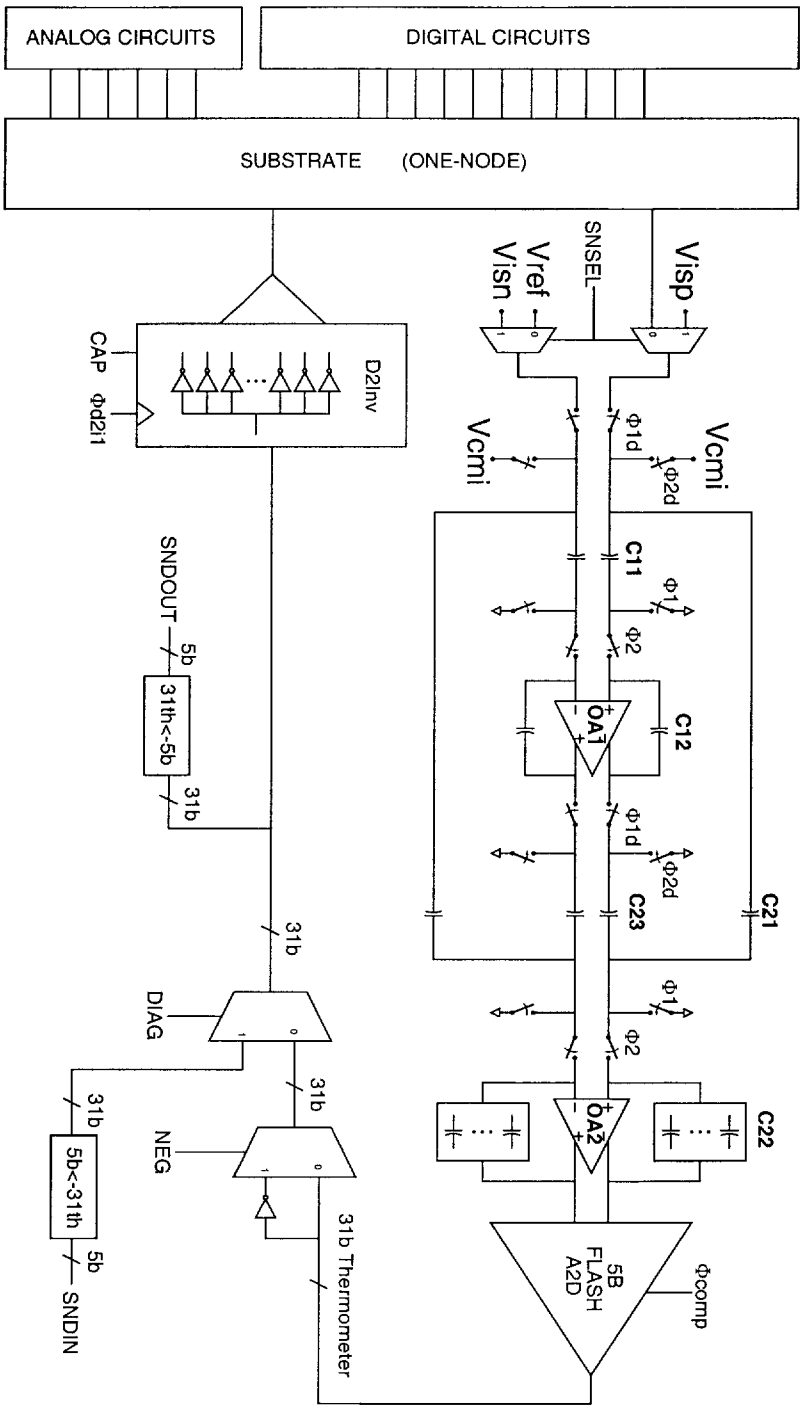


Figure 4-20: Circuit schematic of the SNSL with extra circuits for flexibility/diagnostics.

- Programmable Loop Gain – The open loop gain of the substrate noise shaping loop can be adjusted through the feedback capacitor array of the last stage of the switched capacitor filter. Four values in the capacitor array allow the open loop gain to range from one to 10 times the original value, effectively increasing the substrate noise magnitude sampled by the SNSL.

- Polarity in Feedback Loop – Because substrate noise is a transient with overshoot and undershoot, the sign of the SNSL sampled substrate signal created by the D2Inv could be either positive or negative. Therefore, an optional inversion of the input word to the D2Inv is included to ensure that negative feedback is possible in the SNSL.

- D2Inv Input – The operation of the SNSL can be verified by analyzing the input of the D2Inv. If the SNSL is actually suppressing substrate noise, the output of the D2Inv should be the inverse of the substrate noise generated by the digital circuits. To reduce pin count, the 31 bit thermometer code input word generated by the ADC is converted to a 5 bit binary code by a simple decoder.

4.2.4 Chip Micrograph

The chip micrograph is shown in Figure 4-21. The components used for the SNSL are labeled and outlined.

4.2.5 Experimental Results and Discussion

4.2.5.1 Actual *gsub*

To frame the discussion of substrate noise reduction, *gsub*, a determinant of SNSL performance as explained above, was inferred from measured data. Based on the substrate noise waveforms in the first part of this work, Section 3.3.2, the maximum amount of dynamic range of the D2Inv (*i.e.* the maximum difference between the DS2 sampled values of substrate noise due to 16 high-to-low and 15 low-to-high transitions) was about 10mV with DelayX equal to 3.0ns. This amount of dynamic range plus a rather linear characteristic implied a *gsub* of 0.0025[9]. This was much lower than anticipated, but could be effectively increased by the changing the programmable loop gain which had a maximum extra gain of 10. This resulted in a maximum *gsub* of 0.025. With this gain, the SNSL can still reduce substrate noise by over 20dB in the band of interest as shown in Figure 4-17 as long as the SNSL does not saturate (*i.e.* the substrate noise sampled by the SNSL does not have a magnitude larger than the D2Inv can generate).

4.2.5.2 SNSL with InvArrA as Substrate Noise Generator

The SNSL was first used to shape substrate noise generated by InvArrA, which generates substrate noise typical of pad drivers and clock buffers in a digital chip.

[9] $gsub = \frac{MaximumPeak-to-Peak}{FullScaleVoltage} = \frac{10mV}{4} = 0.0025.$

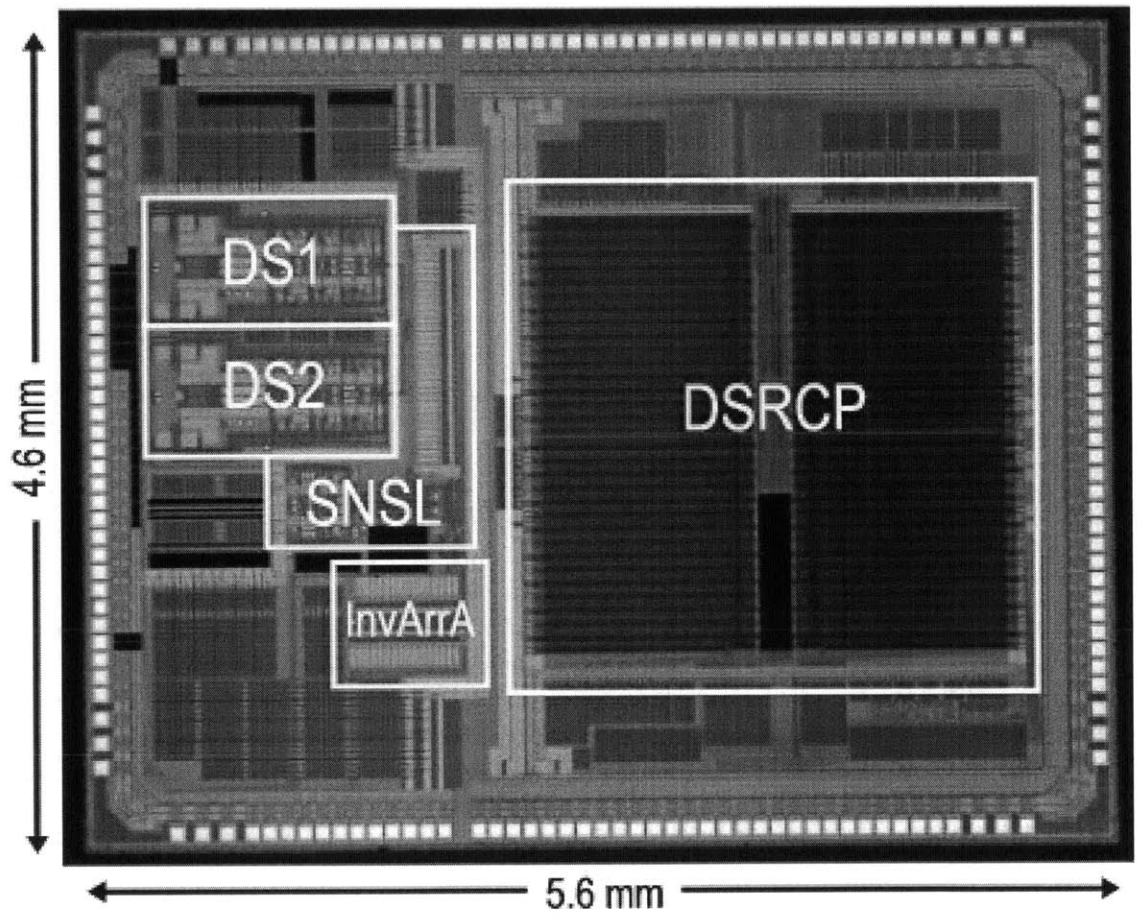


Figure 4-21: Chip micrograph and components used for evaluating the SNSL.

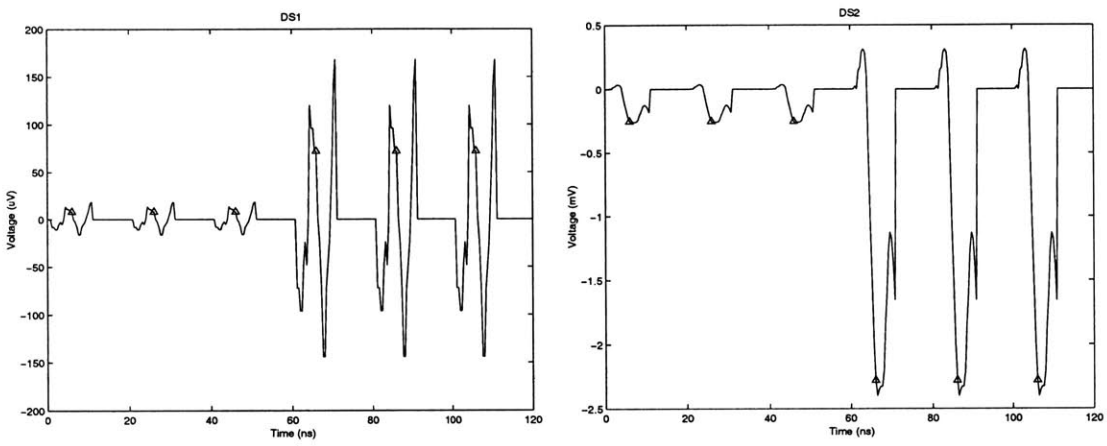
Figure 4-24 shows the outputs of DS1, a delta-sigma modulator converting an external signal and DS2, a delta-sigma modulator converting the substrate voltage with the SNSL on and off in the presence of substrate noise generated by InvArrA. The input to DS1 was a 7.6kHz sine wave with a 125mVrms or -27dB of full scale amplitude. The substrate noise generated by InvArrA and sampled by the SNSL (or DS2 since their input sampling circuits are configured the same) was a discrete time square wave. The input pattern to InvArrA and resulting substrate noise waveforms and SNSL/DS2 sampled values are the same as that used in the first part of this thesis, described in Section 3.3.4 and shown in Figure 3-33. For clarity, the description of the substrate noise and appropriate figure is repeated here. The input pattern to InvArrA, the substrate noise generator, was a 300Hz 50% duty cycle square wave alternating between the digital values, 7 and 15. Since InvArrA in the *Reset* state has 16 inverters high and 15 inverters low, each analog period has either 9 or 1 high-to-low digital transitions. To be more specific, in a 1.66ms time duration, 9 high-to-low digital transitions in InvArrA occur DelayA before each and every analog sampling operation. During the next 1.66ms, 1 high-to-low digital transition in InvArrA occurs DelayA before each and every analog sampling operation. This cycle then repeats for subsequent 3.33ms periods, thus giving the 300Hz activity rate for substrate noise even though InvArrA is clocked at the analog sampling rate, 5MHz. The inverter array, moreover, can be clocked faster, but it should be noted that faster digital clock speeds may not worsen analog circuit performance since it is DelayA, the relative delay between when substrate noise is created and when analog signals are sampled in the circuits, that is crucial. As long as DelayA is less than a few decay time constants of the coupled substrate noise and substrate noise waveforms, the analog circuits will be affected by substrate noise. In terms of waveforms, the coupled substrate noise and substrate noise waveforms over many cycles has been constructed with measured data and are shown in Figure 4-22. This figure shows that although the continuous time waveform is not a square wave, the values, indicated by the triangles in Figure 4-22, sampled at 5MHz by DS1 and DS2 form a 300Hz 50% duty cycle discrete time square wave.

For the following measurements, DelayA, the delay between the clock that controls InvArrA and the analog sampling edge, and DelayX, the delay between the clock that controls the D2Inv and the analog sampling edge, were both 3.0ns.

For comparison, Figure 4-23 shows the output of DS1 and DS2 with no substrate noise and the SNSL off. It shows the raw performance of the delta-sigma modulator as if it was used as a stand-alone converter.

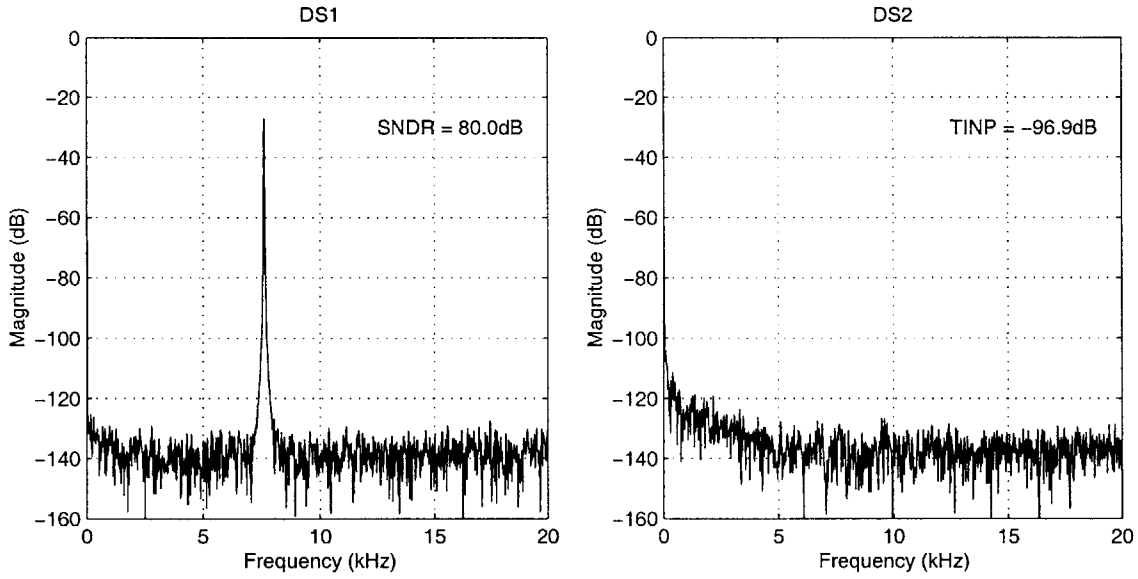
As shown in the Figure 4-23 and Figure 4-24, the SNSL reduces coupled substrate noise and substrate noise sampled in DS1 and DS2, respectively, by over 10dB and over 20dB, respectively. The over 20dB reduction of substrate noise in DS2, which converts the substrate voltage directly, roughly matches the behavioral simulations for the inferred *gsub* discussed above (Figure 4-17).

Unlike the replica technique, the SNSL reduces both the input signal independent and input signal dependent components. This indicates that the SNSL actually reduces the substrate noise itself in the band of interest as demonstrated by the DS2 output. In other words, the low frequency voltage fluctuations on the substrate have been reduced.



(a) (b)

Figure 4-22: Coupled substrate noise and substrate noise waveforms generated by InvArrA over time as seen by DS1 and DS2/SNSL. The waveforms have been constructed from measured data gathered from Chapter 3 of this thesis. Some zero padding after the waveforms has been added to denote the end of a clock cycle. InvArrA causes 1 high-to-low transition every analog clock period or 9 high-to-low transitions every analog clock period depending on its input pattern. The triangles indicate the sampled values in DS1 and DS2. Although the continuous time waveform is constantly changing, the discrete time values form a square wave. The frequency of the clock that controls when InvArrA transitions has been set at 50MHz for this illustration to more fully illustrate the continuous time transient waveforms because they have ringing frequencies of about 300MHz. In the actual test setup, the frequency of the clock that controls InvArrA is 5 MHz. Also, transients due to the InvArrA resetting have been omitted. (a) coupled substrate noise seen in DS1 (b) substrate noise seen in DS2.



(a) (b)

Figure 4-23: Measured delta-sigma modulator output spectra from 0-20kHz with no substrate noise. The input to DS1 was a -27dB of full scale 7.6kHz input tone. (a) DS1 (b) DS2.

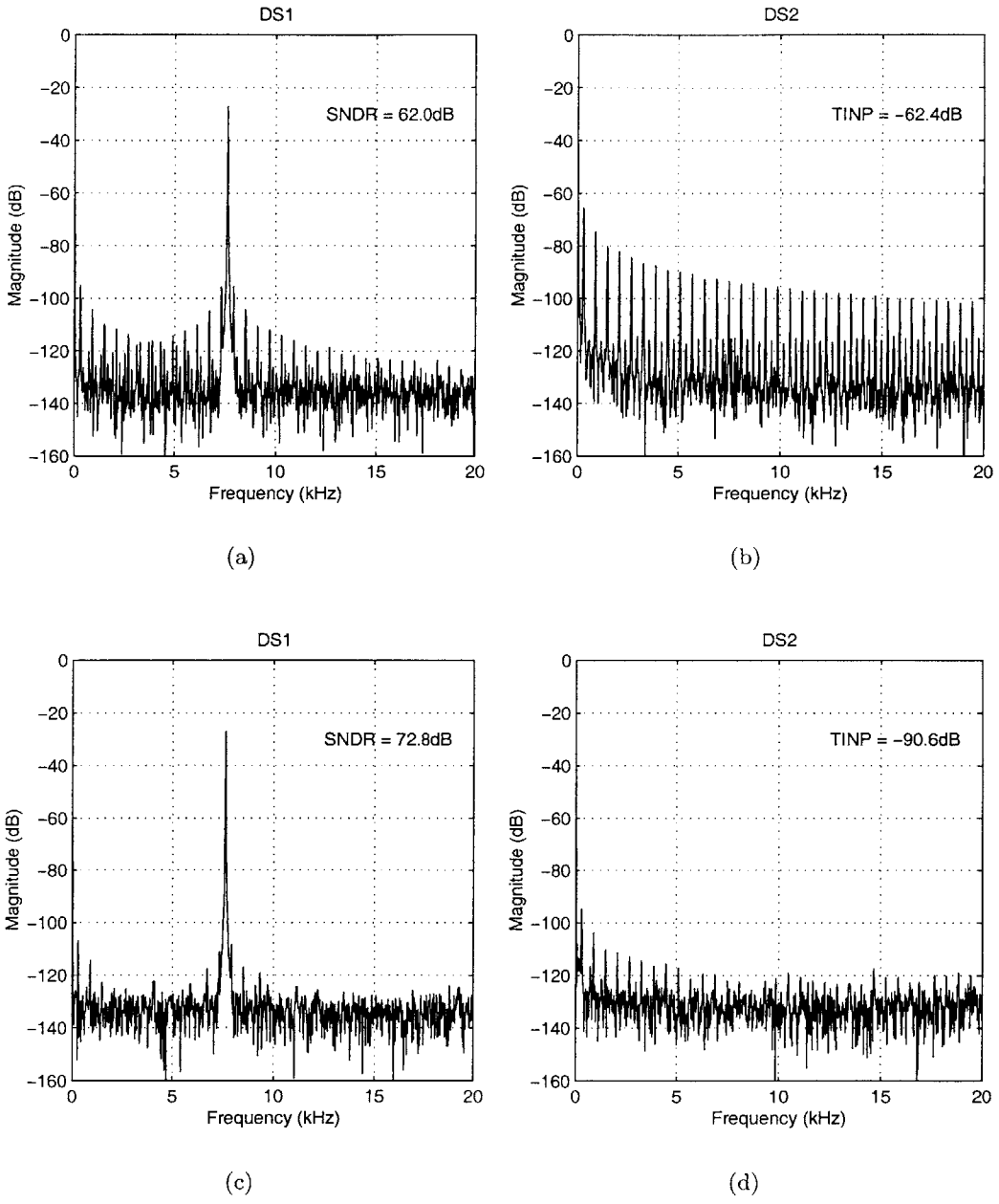
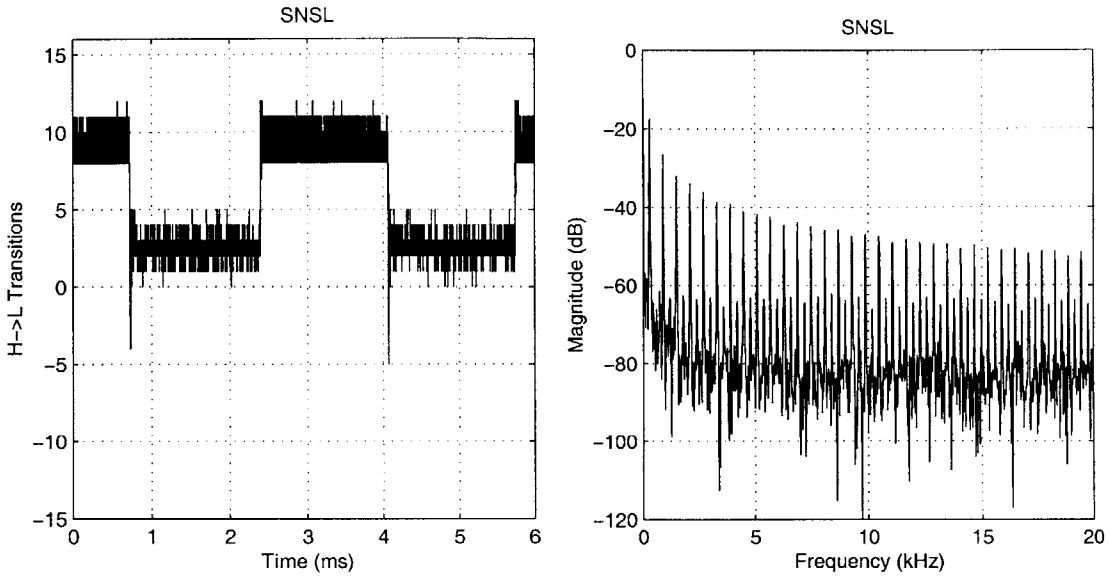


Figure 4-24: Measured data showing the effect of SNSL on coupled substrate noise and substrate noise generated by InvArrA. Spectra of the delta-sigma modulators are shown with the SNSL on and off. (a) DS1, SNSL off (b) DS2, SNSL off (c) DS1, SNSL on (d) DS2, SNSL on.



(a) (b)

Figure 4-25: Measured data of the input word to the D2Inv while the SNSL cancels the discrete time square wave substrate noise. The 31 bit thermometer code has been changed to a decimal representation. A negative number of high-to-low transitions is a positive number of low-to-high transitions. (a) time domain (b) frequency domain.

Figure 4-25 shows the time waveform and frequency spectrum of the input to the D2Inv. The 31 bit thermometer code has been converted to a decimal representation. As seen in the figure, the SNSL followed a 300Hz square wave in the time domain. In the frequency domain, the SNSL spectrum is predictably a 300Hz square wave which is similar in shape to the original substrate noise spectrum seen in DS2 (Figure 4-24(b)). This indicates that the SNSL tracks and cancels the substrate noise as designed.

A close up of the time domain waveform, shown in Figure 4-26, reveals the system dynamics of the SNSL. In response to the substrate noise square wave transitioning–transitioning in the discrete time sense (*i.e.* sampled values in DS1 and DS2 go from the low value to the high value)–the SNSL overshoots and rings like a second order system before settling. The same behavior can be obtained from the behavioral model of the SNSL with some non-idealities such as finite operational amplifier gain included[10]. The final value of settling is not constant and fluctuates in a small range. This range of values is the result

[10]Finite operational amplifier gain moves the closed loop poles off the point (0,1) in the z-plane resulting in higher phase margin and slower settling response. This also reduces and flattens the substrate noise reduction in the pass band.

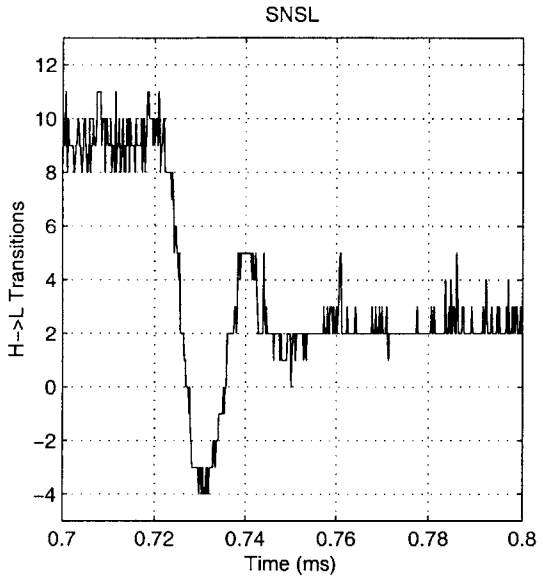


Figure 4-26: Measured data of the input word to the D2Inv of the SNSL with substrate noise generated by InvArrA. The 31-bit thermometer code has been changed to a decimal representation. A negative number of high-to-low transitions is a positive number of low-to-high transitions.

of the SNSL shaping the quantization noise of the discrete feedback element, the D2Inv.

Figure 4-27 shows the reduction of the 300Hz square wave harmonics in DS2 when the SNSL is used. As expected, substrate noise is generally reduced more at low frequencies and less at higher frequencies. This level of performance is consistent with the inferred *gsub* in the behavioral models.

Figure 4-28 shows the effectiveness of using the SNSL to improve analog circuit performance. The SNSL does not completely remove coupled substrate noise and substrate noise, but reduces it considerably in both the SNDR of DS1 and the TINP of DS2. The curve that depicts the SNDR with the substrate noise on and the SNSL off plateaus at about 65dB because at that point the input signal dependent components of coupled substrate noise dominate the SNDR since input signal dependent components rise with larger input signal magnitudes.

In short, the SNSL is effective in reducing coupled substrate noise and substrate noise for substrate noise generated by InvArrA, which is similar to digital pad drivers and clock buffers.

4.2.5.3 SNSL with DSRCP as Substrate Noise Generator

The SNSL was next used to shape substrate noise generated by the DSRCP, which generates noise typical of arbitrary digital logic implementing functions in a digital chip.

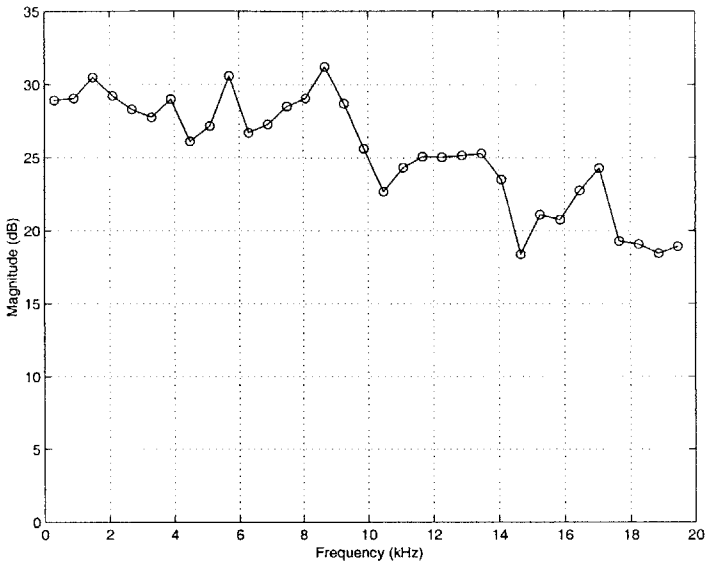


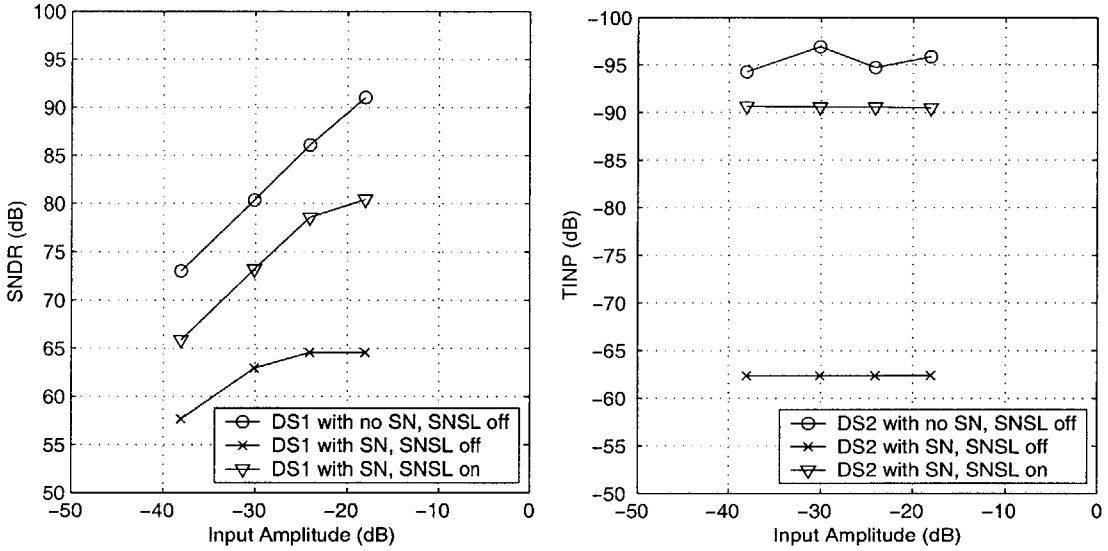
Figure 4-27: Measured reduction in substrate noise (DS2) tones of the 300Hz discrete time square wave substrate noise by the SNSL.

Figure 4-29 shows the outputs of DS1 and DS2 with the SNSL on and off in the presence of substrate noise generated by the DSRCP. The input to DS1 was again a 7.6kHz sine wave with a -27dB of full scale amplitude. The DSRCP was used in the highest power mode possible so that it would generate the maximum amount of substrate noise possible. The delay of the digital clock with respect to the analog sampling clock, DelayB, was 1.0ns[11]. Again, for comparison, Figure 4-23 shows the output of DS1 and DS2 with no substrate noise and the SNSL off.

As shown in Figure 4-23, Figure 4-29(b) and (d), the SNSL reduces the substrate noise as seen in DS2 by about 20dB in terms of TINP. The substrate noise generated by the DSRCP was periodic with a fundamental of about 192Hz and harmonic content that dropped off quickly. Closer study revealed that the associated period of 1/192Hz = 4.8ms was the time needed for the DSRCP to complete one exponential modulation instruction in the infinite loop used for generating the substrate noise.

Figure 4-30 shows the time waveform and frequency spectrum of the input word to the D2Inv when the SNSL cancels substrate noise generated by the DSRCP. As before, its frequency spectrum is very similar to that sensed in DS2, which indicates that it was tracking the substrate noise.

[11]This delay is between the clock that feeds the digital circuits and the analog sampling clocks. The digital circuits may actually switch later than this delay because the digital clock is buffered internally and fed to the entire digital chip leading to extra delay.



(a) (b)

Figure 4-28: Measured SNDR of DS1 and TINP of DS2 when using SNSL. Note the inverted scale for subfigure (b). (a) SNDR of DS1 (b) TINP of DS2.

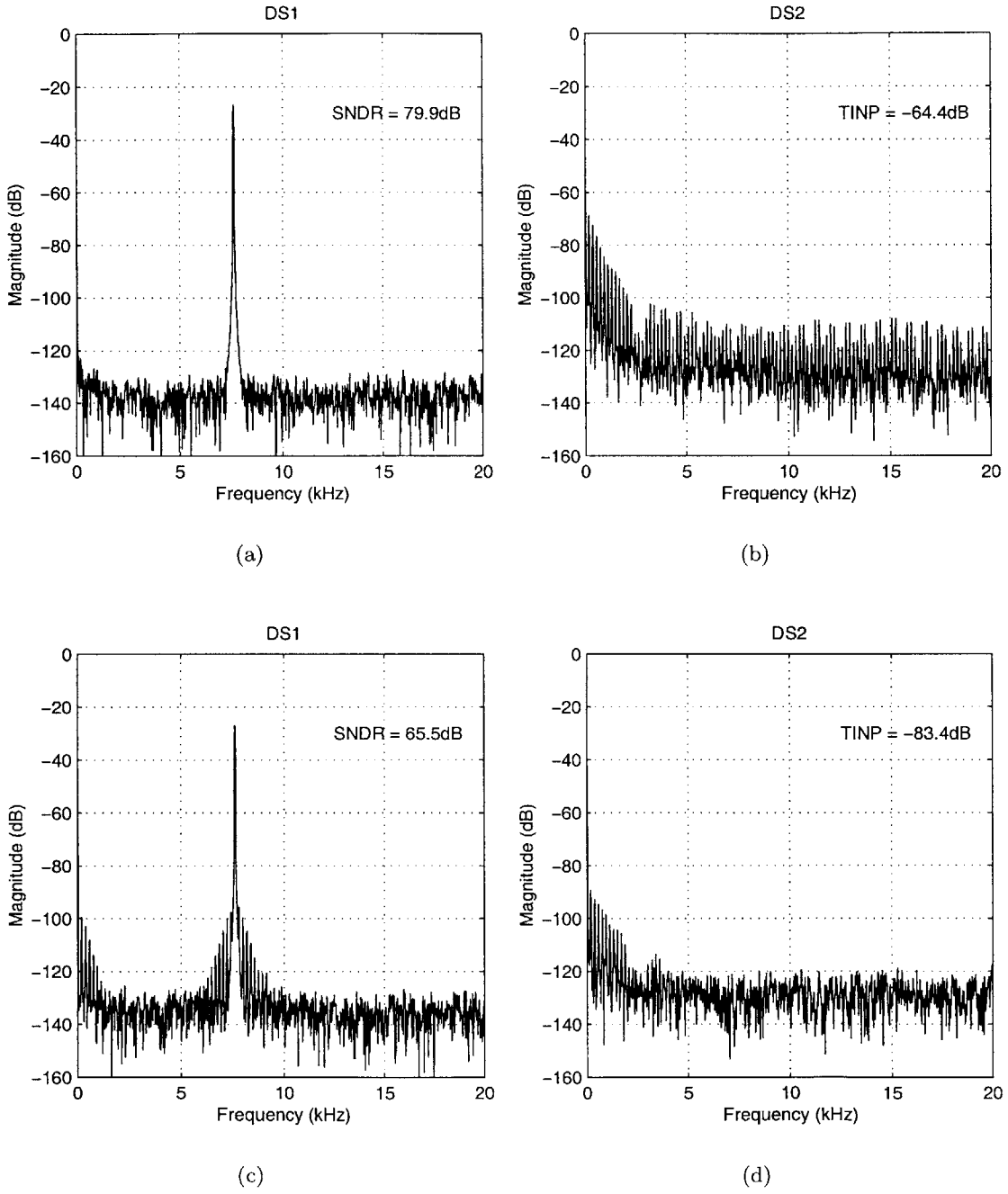
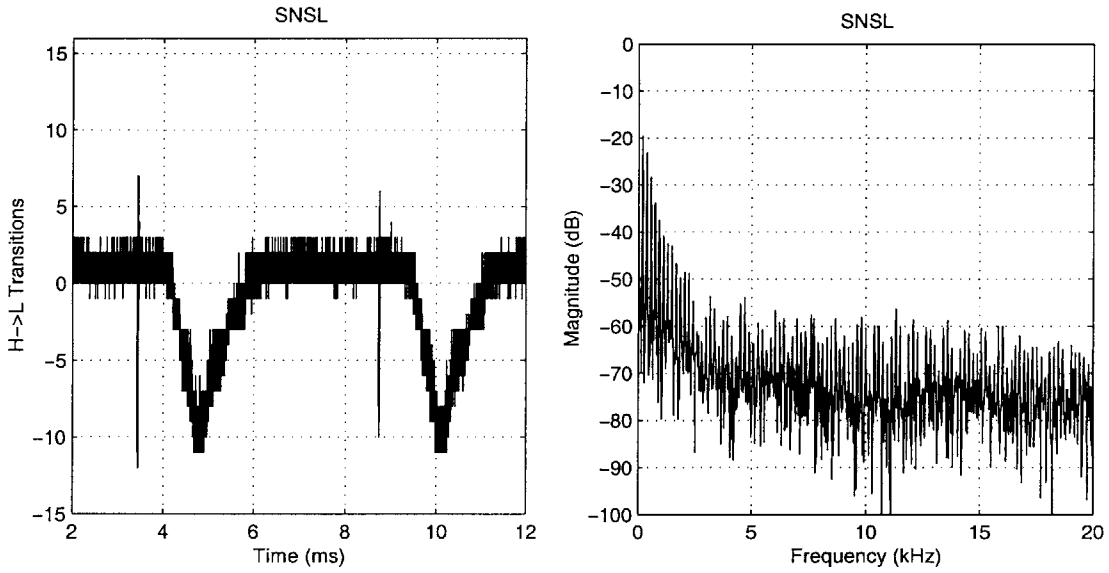


Figure 4-29: Measured data showing the effect of SNSL on coupled substrate noise and substrate noise generated by the DSRCP seen in DS1 and DS2, respectively. (a) DS1, SNSL off (b) DS2, SNSL off (c) DS1, SNSL on (d) DS2, SNSL on.



(a) (b)

Figure 4-30: Measured data of the input word to the D2Inv while the SNSL canceled the substrate noise generated by the DSRCP. The 31-bit thermometer code has been changed to a decimal representation. A negative number of high-to-low transitions is a positive number of low-to-high transitions. (a) time domain (b) frequency domain.

Although the SNSL reduces the substrate noise seen in DS2, the salient feature of SNSL with the DSRCP generating the substrate noise is the creation of a significant amount of coupled substrate noise seen in DS1. When the SNSL is off and the DSRCP is on, the spectrum of DS1 is hardly affected and it performs almost the same as when the DSRCP is off, going from an SNDR of 80.5dB to 79.9dB. However, when the SNSL is turned on, significant coupled substrate noise appears in DS1, adding both input signal dependent and input signal independent components to the spectrum, reducing the SNDR of DS1 from 79.9dB to 65.5dB. This phenomena can be explained by the nature of the substrate noise generator and the SNSL sensing of the substrate noise.

4.2.5.3.1 Nature of Coupled Substrate Noise and Substrate Noise Generated by DSRCP The DSRCP does not generate much coupled substrate noise for two reasons. The first reason is that the DSRCP was designed to be a low power circuit [3] which means that transistor sizes were made small and digital transitions were minimized with efficient logic. These attributes translate into less coupled substrate noise as current spikes and parasitic coupling values, which help determine the derivative of substrate noise, are reduced.

The second reason that the DSRCP does not generate much coupled substrate noise is because of the time distribution of transitions in digital circuits that implement digital logic. Digital circuits that implement digital logic tend to be composed of many small digital gates rather than a few large gates. This means that the substrate noise waveform generated by these digital circuits each clock cycle is relatively slow because it is a composite waveform of many digital gates switching at slightly different times due to clock skew and gate delay. This composite transient is relatively low frequency and thus the coupled substrate noise seen in DS1, a high pass version of the substrate noise waveform in DS2, is correspondingly low [7]. In contrast, digital pad drivers and clock buffers like InvArrA, have large inverters switching simultaneously producing relatively fast and large substrate noise waveforms, high frequency content which couples into DS1 easily. This is a key difference which must be considered when analyzing how much coupled substrate noise is generated by digital circuits.

The differences between the coupled substrate noise and substrate noise generated by InvArrA (D2Inv as well) and the DSRCP are illustrated in Figure 4-31 and Figure 4-32. Figure 4-31 shows hypothetical coupled substrate noise and substrate noise waveforms generated by a simulated digital circuit, DigCktA, with behavior similar to the DSRCP. As explained in the previous chapter, coupled substrate noise is a high-pass version of the substrate noise and thus a derivative multiplied by 1/3 was used to generate the coupled substrate noise waveform (DS1) from the substrate noise waveform (DS2) shown in Figure 4-31. As seen in Figure 4-31, the sampled coupled substrate noise as seen in DS1 is relatively small even though the sampled substrate noise magnitude in DS2 is relatively large. For comparison, Figure 4-32 shows measured coupled substrate noise and substrate noise waveforms seen in DS1 and DS2, respectively, for a single inverter in InvArrA or D2Inv. Zero values have been inserted for times at which data was not gathered. If more than one inverter in InvArrA or D2Inv switches, then the waveforms in Figure 4-32 are

scaled by the number of inverters switching to determine the total coupled substrate noise and substrate noise. This captures the fact that the inverters switch at the same time and thus the coupled substrate noise and substrate noise waveforms they create add, resulting in an overall coupled substrate noise and substrate noise waveform that is larger in magnitude than a single inverter, but not different in shape. Note that the DS1 sampled coupled substrate noise value for a single inverter denoted by the circle in Figure 4-32(a) is larger than the DS1 sampled coupled substrate noise value for the DigCktA in Figure 4-31(a) and (c) even though DigCktA's DS2 sampled substrate noise value in Figure 4-31(b) and (c) is much larger than the single inverter's in Figure 4-31.

The end result of the DSRCP generating substrate noise is that the coupled substrate noise seen in DS1 is small[12] even though there are relatively large amounts of substrate noise as seen in DS2. The substrate noise waveform generated by the DSRCP is relatively slow so coupled substrate noise, a high-pass version of substrate noise, is small.

4.2.5.3.2 SNSL Sensing The primary reason coupled substrate noise in DS1 is enhanced when using the SNSL is the quantity sensed in the SNSL. The SNSL senses the substrate voltage and thus it cancels substrate noise. The original thought at system conception was that the reduction of substrate noise would be accompanied by a reduction of all harmful effects due to substrate noise. This, however, is not necessarily true because coupled substrate noise seen in DS1 is a high-pass version of substrate noise seen in DS2. Thus, sensing the substrate noise and canceling it will not necessarily cancel the coupled substrate noise seen in DS1. In addition, the DSRCP was not a suitable digital circuit as a substrate noise generator since it generated so little coupled substrate noise compared to an inverter array. Thus, when the SNSL is turned on, coupled substrate noise appears to be enhanced. The anti-noise created by D2Inv has sharp transitions and couples to DS1 much more than the original substrate noise created by DSRCP. Hence the D2Inv dominates the coupled substrate noise seen in DS1.

A simulation of the SNSL in the presence of substrate noise illustrates the problem of SNSL sensing. A script written in Matlab simulated the SNSL. DS1 and DS2 were assumed to be ideal converters with no circuit nor quantization noise. Substrate noise coupling into DS1 is modeled with an input signal independent and input signal dependent component consistent with findings in the first part of this research. The waveforms of DigCktA, described above, were used as the coupled substrate noise and substrate noise transients. DigCktA alternates at a 300Hz activity rate with a 50% duty cycle between the two instructions (each take one digital clock cycle to finish), Instruction A and Instruction B, shown in Figure 4-31. The D2Inv of the SNSL generated coupled substrate noise and substrate noise waveforms shown in Figure 4-32 scaled by the appropriate number of inverters that switch. The digital clock and analog clock were both set at 50MHz in the simulation for illustration purposes. The delay between the digital clock rising edge and analog sampling edge was 3.0ns. The values sampled by DS1 and DS2/SNSL are indicated by the circles on each waveform.

[12]The coupled substrate noise may not be visible in measured data because it is below the circuit/quantization noise of the delta-sigma modulator.

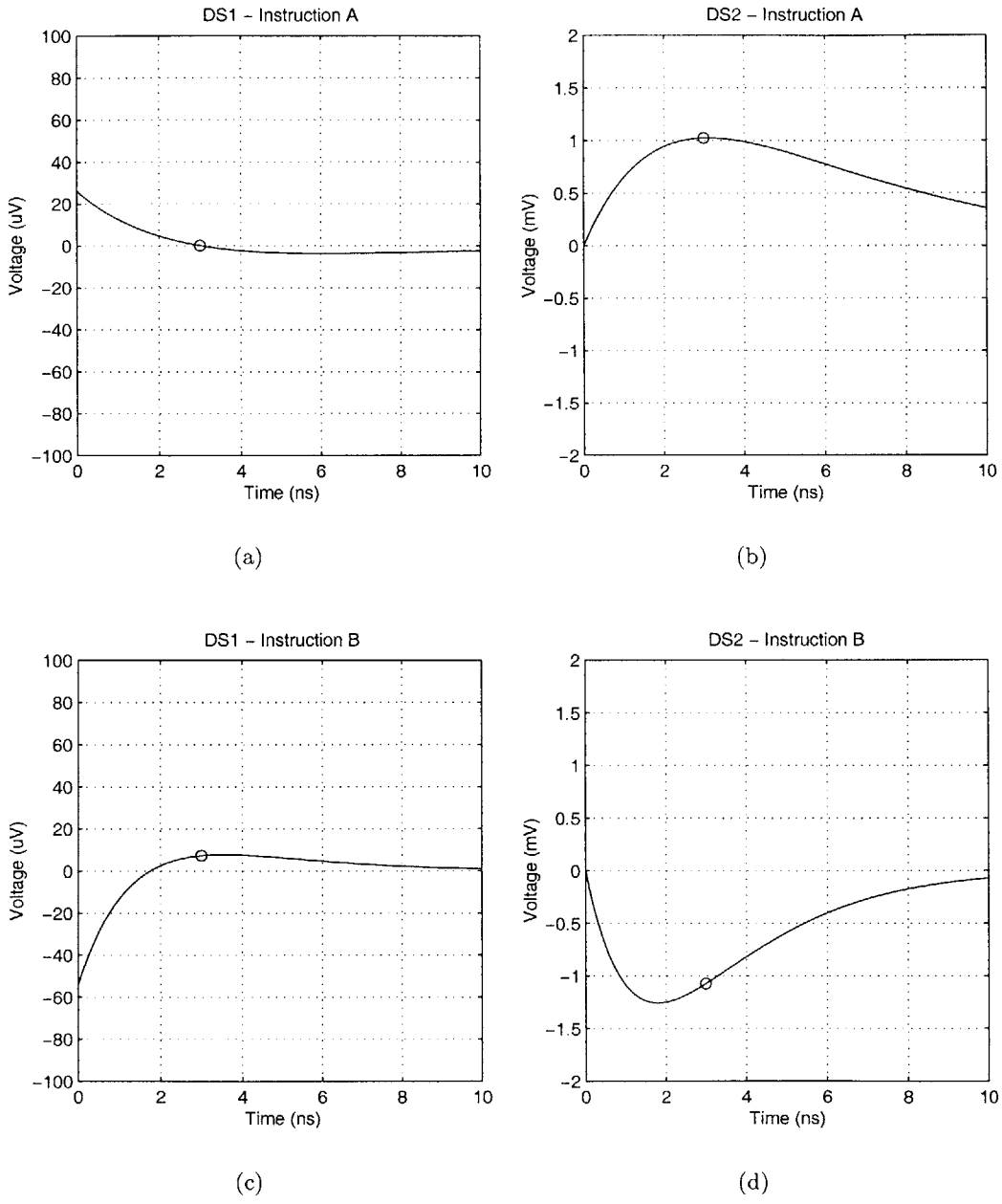


Figure 4-31: Hypothetical coupled substrate noise and substrate noise waveforms generated by DigCktA, a digital circuit similar to the DSRCP performing different instructions each clock cycle. Circles indicate the values sampled in each case. (a) DS1 - DigCktA Instruction A (b) DS2 - DigCktA Instruction A (c) DS1 - DigCktA Instruction B (d) DS2 - DigCktA Instruction B

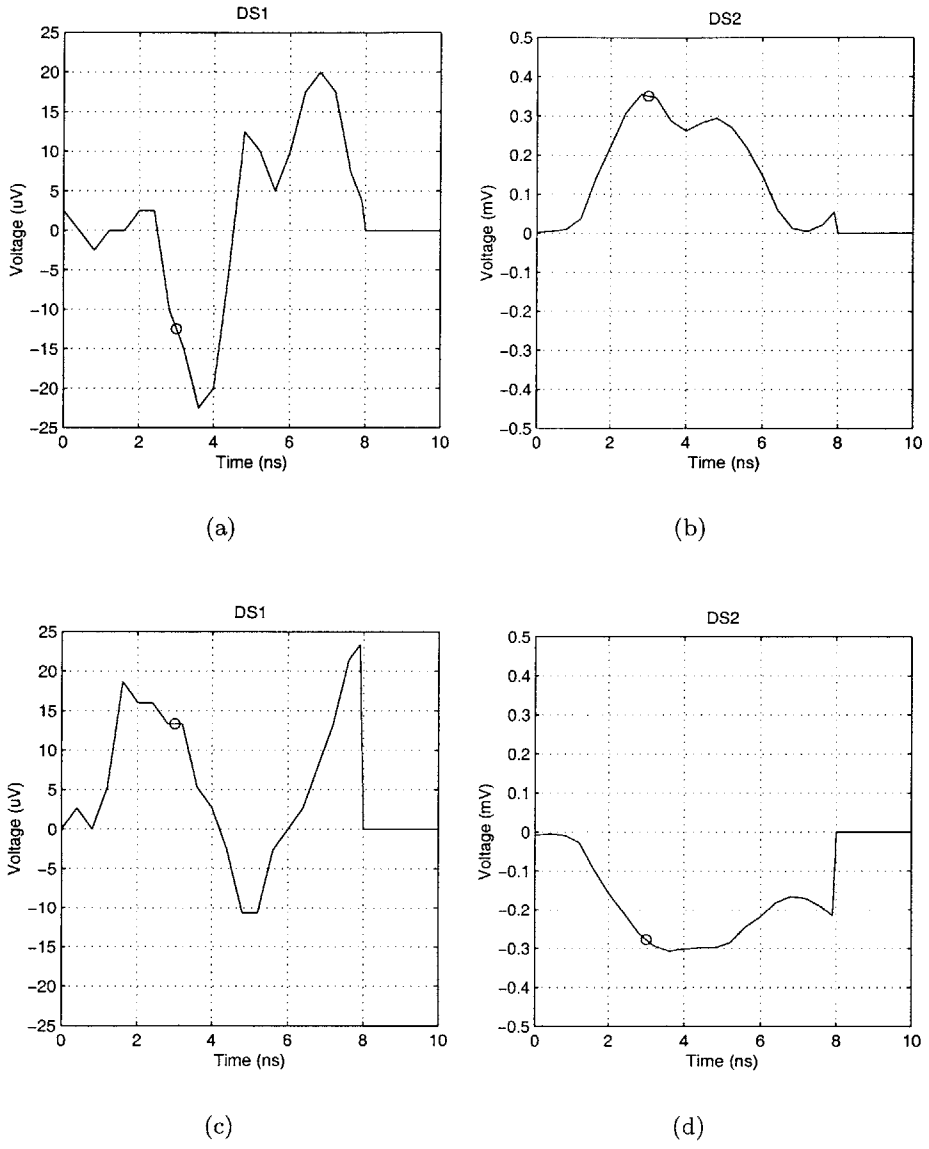


Figure 4-32: Coupled substrate noise and substrate noise waveforms generated by a single inverter in the InvArrA or D2Inv, reconstructed from measured data. This figure has been reformatted version of Figure 3-24. The high-to-low and low-to-high coupled substrate noise and substrate noise waveforms have been separated into different plots and scaled for a single high-to-low or low-to-high transition. Also, the waveforms have been padded with zeros for values not gathered before. DelayA and DelayX both equal 3.0ns and thus the circles indicate the values sampled by the SNSL in each case. (a) DS1, H→L (b) DS2, H→L (c) DS1, L→H (d) DS2, L→H.

Figure 4-33 shows simultaneous continuous time waveforms seen at the input of DS1 and DS2. As can be seen, DigCktA and the SNSL both cause a certain coupled substrate noise and substrate noise transient every clock period. These transients add and become the total waveform, DigCktA+SNSL as indicated in the figure, seen in DS1 and DS2. The actual values sampled by DS1 and DS2 are indicated by circles. Note that at the sampling instant, while the values of the DigCktA and SNSL component waveforms in DS2 cancel, they do not in DS1.

Figure 4-34 shows the values sampled by DS1 and DS2 over a longer period of time. As the figure shows, the SNSL cancels the substrate noise seen in DS2 by keeping the resultant sampled values, DigCktA+SNSL, to roughly zero in Figure 4-34(b). The substrate voltage is the quantity sensed and hence substrate noise, fluctuations on the substrate voltage, was canceled. However, in doing so, the SNSL added coupled substrate noise seen in DS1 that dominated the resultant sampled values, DigCktA+SNSL, seen in DS1. Originally, the coupled substrate noise was small because DigCktA generated relatively little coupled substrate noise at the sampling instances as indicated by the pointing-up triangles.

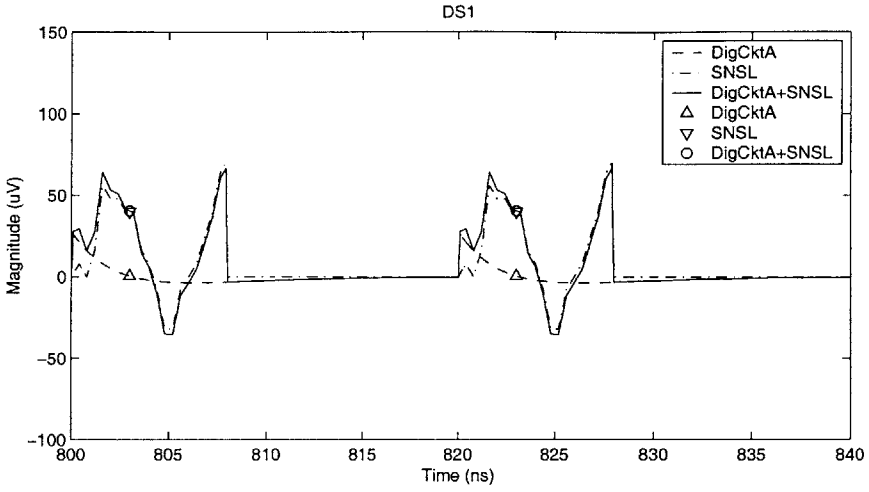
This time domain behavior translates into the frequency domain as seen in Figure 4-35. For the spectra in Figure 4-35, the input to DS1 was a 7.6kHz sine wave with a -27dB of full scale amplitude.

In Figure 4-35, when the SNSL is off, coupled substrate noise seen in DS1 is small, while substrate noise seen in DS2 is relatively large. In many circuits, the coupled substrate noise in DS1 may not be observable because it is below the circuit and quantization noise of the delta-sigma modulator. When the SNSL was on, the coupled substrate noise seen in DS1, dominated by the coupled substrate noise contribution from the D2Inv of the SNSL, was larger and the substrate noise in DS2 was smaller. These results are consistent with the observed behavior of DS1 and DS2 when substrate noise was generated by the DSRCP.

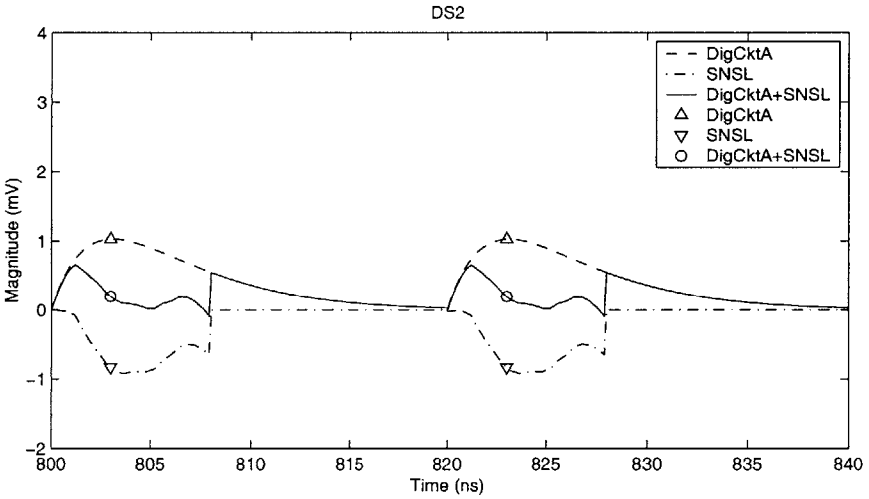
This explanation is also consistent with the results seen for coupled substrate noise and substrate noise generated by InvArrA. In this case, the SNSL uses waveforms of the coupled substrate noise and substrate noise that have roughly inverse values at the sampling instant. Although the component waveforms, SNSL and InvArrA, do not cancel each other out in continuous time as seen by DS1 and DS2 in Figure 4-36, the component's sampled values in DS1 and DS2 do cancel out. In other words, the sampled substrate noise in DS2/SNSL is a proxy for the sampled coupled substrate noise in DS1, and thus the sensing of the substrate voltage is appropriate for canceling coupled substrate noise generated by InvArrA.

Figure 4-37 shows just the DS1 and DS2 sampled values over a longer period of time than Figure 4-36. As can be seen, not only is the substrate noise seen in DS2 canceled, but the coupled substrate noise seen in DS1 is attenuated as well with use of the SNSL. This simulation was consistent with measured data when InvArrA generates the substrate noise. Note that since the coupled substrate noise generated by InvArrA and seen by DS1 does not have exact inverse values in the inverter high-to-low and low-to-high waveforms at 3.0ns, the delay between the digital clock rising edge and the analog sampling edge. Hence, the coupled substrate noise reduction is less than the substrate noise reduction.

From the simulations, it is seen that SNSL sensing the substrate voltage is effective for substrate noise generated by InvArrA. However, it is not effective for substrate noise

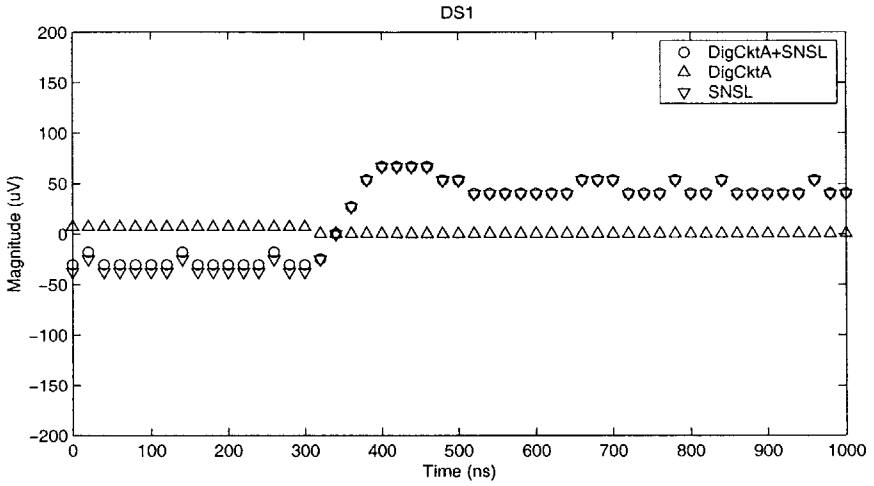


(a)

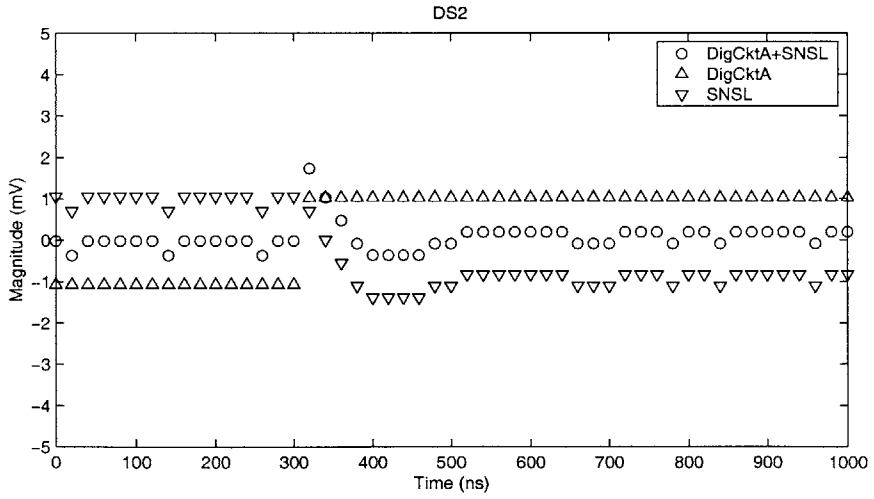


(b)

Figure 4-33: Simulated continuous time domain waveforms of SNSL canceling substrate noise generated by DigCktA, which is similar to the DSRCP. The clock frequency to DigCktA and the analog circuits, DS1 and DS2, have been set to 50MHz (test setup was 5MHz) to show more detail in the waveforms. Coupled substrate noise and substrate noise components generated by DigCktA, the SNSL, and the total are shown. DigCktA, performs the same operations in the two clock cycles shown above. Ultimately the DigCktA+SNSL waveform is sampled by DS1 and DS2 as indicated by the circles. (a) DS1 (b) DS2.



(a)



(b)

Figure 4-34: Simulated discrete time domain waveforms of SNSL canceling substrate noise generated by DigCktA. Component and resultant waveforms are shown. The simulation used a clock frequency of 50MHz instead of 5MHz as in the test setup. Times correspond to those in Figure 4-36 for closer examination of the continuous time waveforms involved. (a) DS1 (b) DS2.

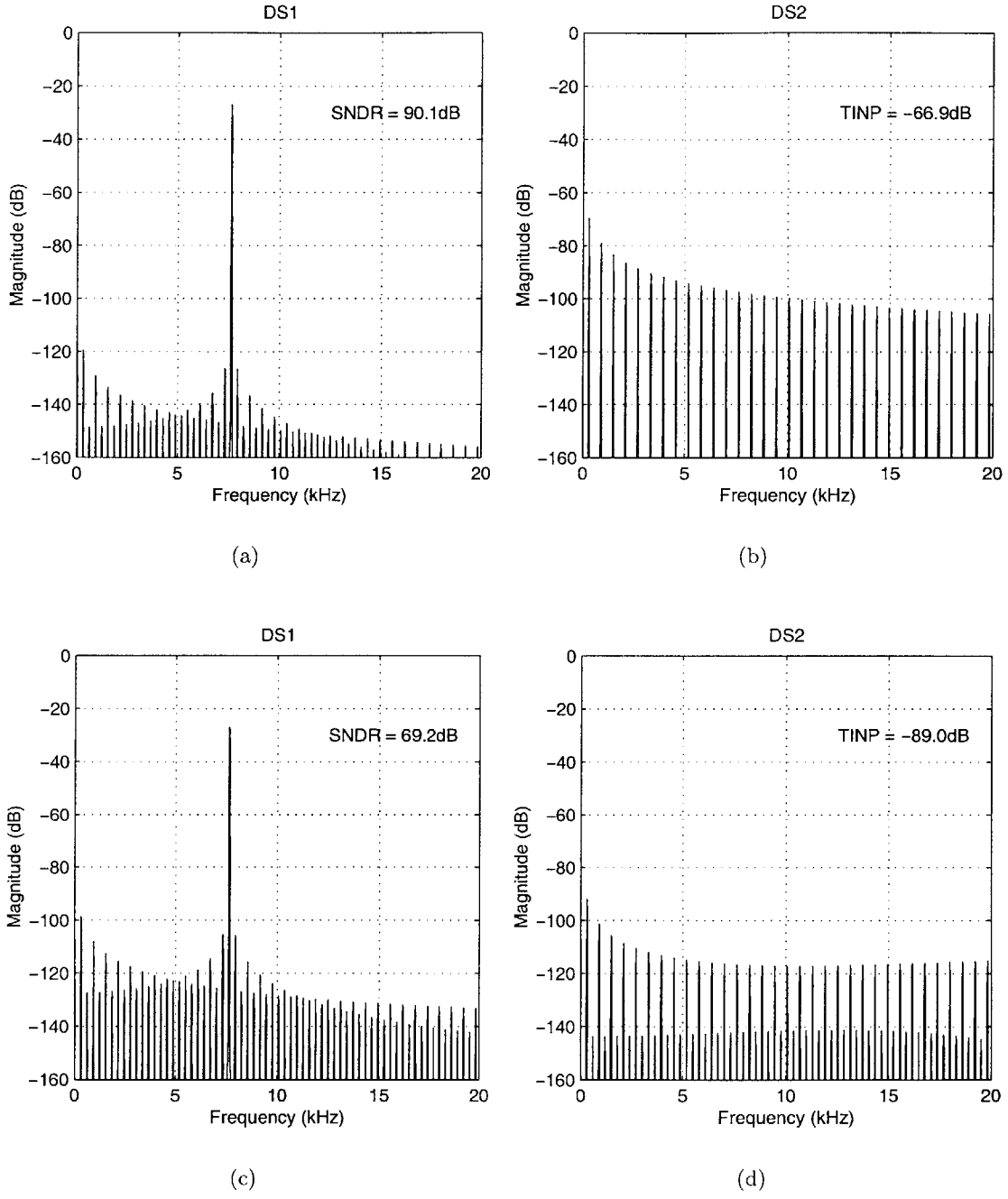
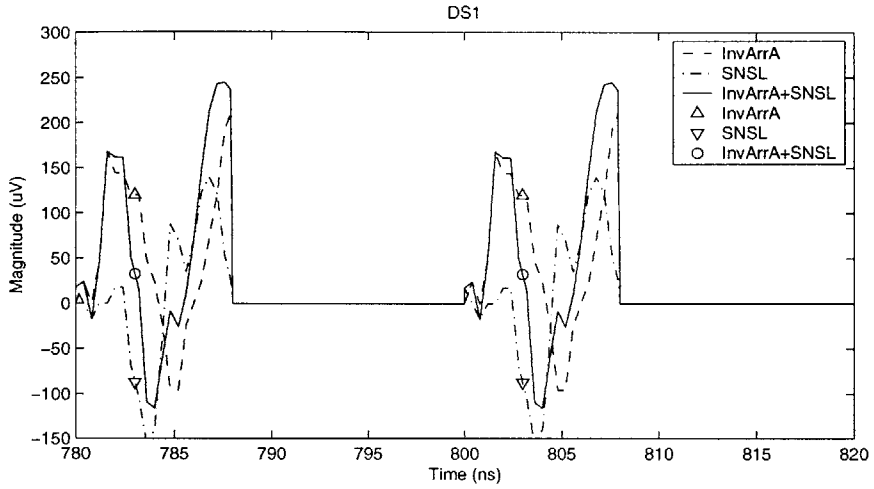
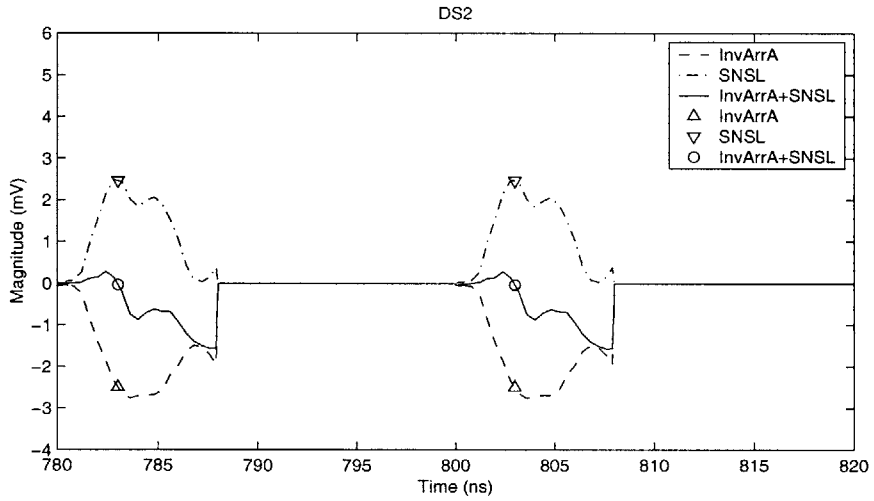


Figure 4-35: Frequency spectra of SNSL simulations with coupled substrate noise and substrate noise generated by DigCktA. (a) DS1, SNSL off (b) DS2, SNSL off (c) DS1, SNSL on (d) DS2, SNSL on.

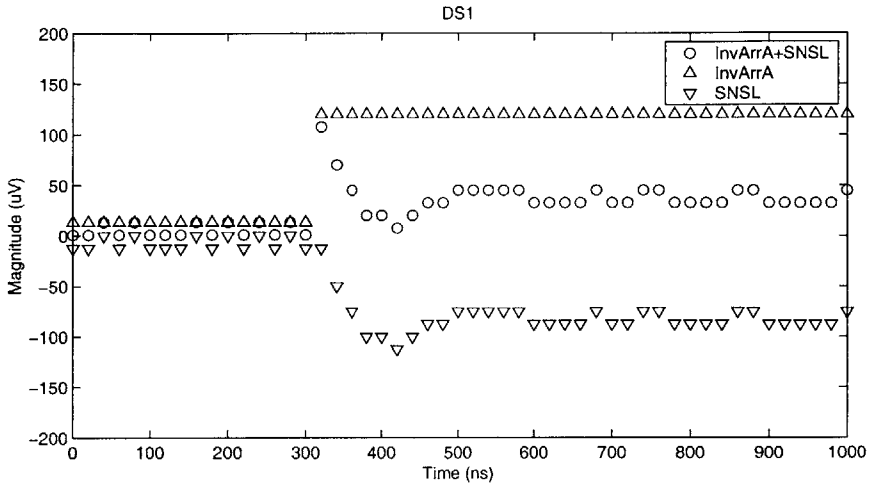


(a)

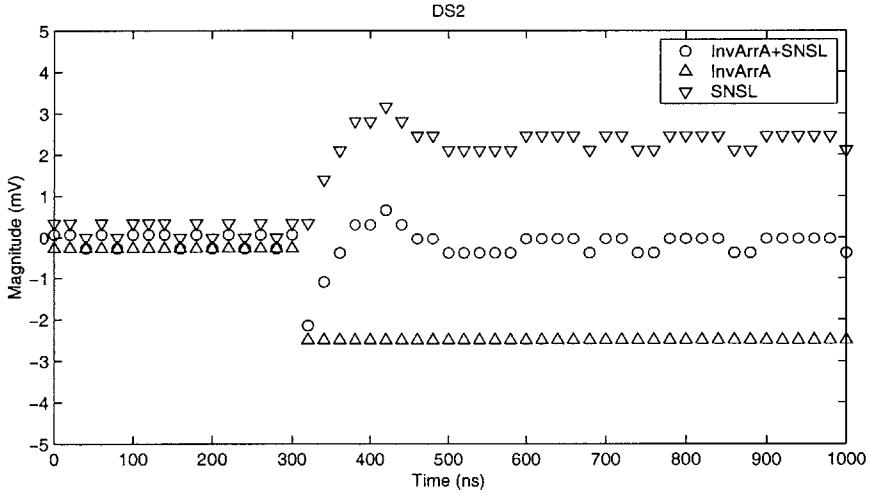


(b)

Figure 4-36: Simulated continuous time domain waveforms of SNSL canceling substrate noise generated by InvArrA. The simulation used a clock frequency of 50MHz instead of 5MHz (the clock frequency used on the test chip) so that more detail of the continuous time waveforms could be shown. Coupled substrate noise and substrate noise components generated by InvArrA and the SNSL are shown. Ultimately the InvArrA+SNSL waveform is sampled by DS1 and DS2 as indicated by the circles. (a) DS1 (b) DS2.

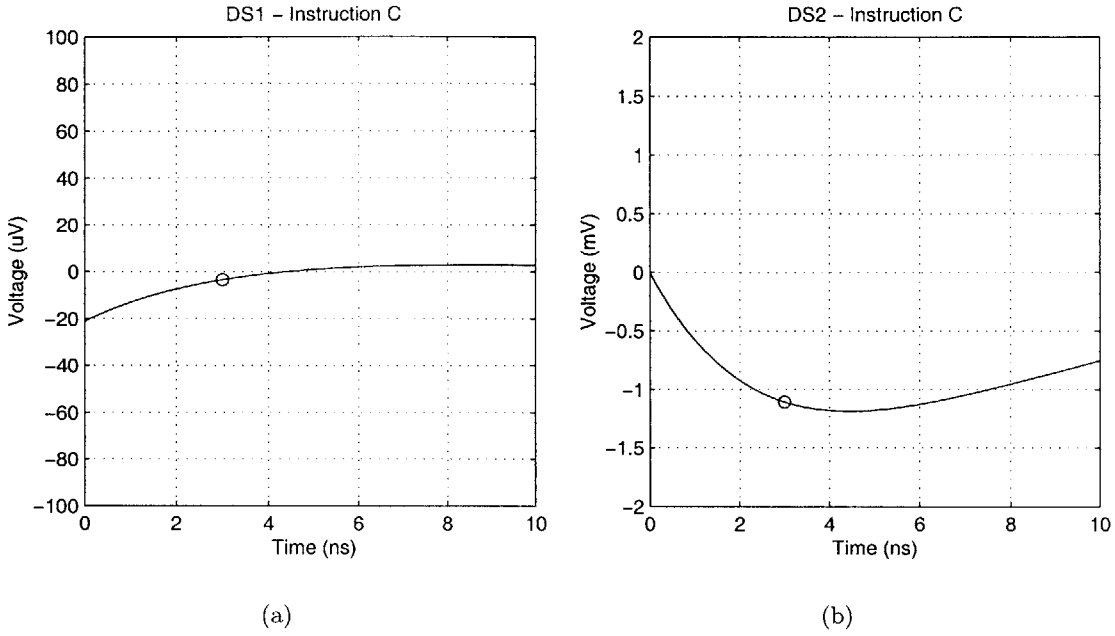


(a)



(b)

Figure 4-37: Simulated discrete time domain waveforms of SNSL canceling substrate noise generated by an InvArrA. Component and resultant waveforms are shown. The simulation used a clock frequency of 50MHz. The times correspond to those in Figure 4-36. (a) DS1 (b) DS2.

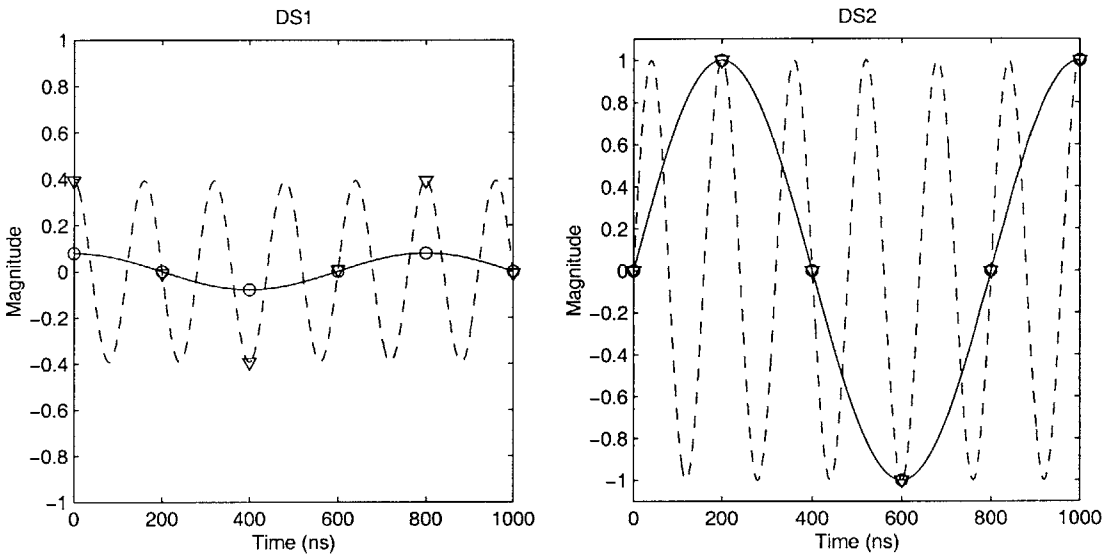


(a) (b)

Figure 4-38: Hypothetical coupled substrate noise and substrate noise waveforms generated by DigCktA, a circuit similar to the DSRCP. (a) DS1 - DigCktA Instruction C (b) DS2 - DigCktA Instruction C.

generated by the DSRCP.

An implication of the SNSL sensing the substrate noise instead of the coupled substrate noise is that coupled substrate noise sampled in DS1 may be uncorrelated with substrate noise sampled in DS2 if the substrate noise is generated by arbitrary digital logic. In the previous example, DigCktA alternated between two instructions that created the same substrate noise and coupled substrate noise waveform every time. However, most likely a digital circuit will produce many different substrate noise and coupled substrate noise waveforms even for the same instruction if the data operated on is different. Even worse, two different instructions may have the same substrate noise value as sampled by DS2/SNSL, but not the same coupled substrate noise value as sampled by DS1. This is illustrated in Figure 4-38. This third instruction of DigCktA, Instruction C, produces a different coupled substrate noise and substrate noise waveform than that of Instruction B. However, the sampled value of the substrate noise waveform for both Instruction B and C are the same while the sampled value of the coupled substrate noise waveform is different. This problem can happen because the slopes of the substrate noise waveforms at sampling points are different. This effect can also be seen in the measured data of Figure 3-24 on Page 76. At about 2ns and 5ns, the values in DS2 are the same, but the values in DS1 are very different. The reason for this problem is aliasing.



(a) (b)

Figure 4-39: Aliasing problems that give rise to different DS1 sampled values even though the sampled values in DS2 are the same. The simulated substrate noise waveforms seen by DS2 are tones at 1/4 and 5/4 of the sampling frequency. The waveform in DS1 is the derivative of the waveform in DS2. Circles and triangles indicate sampled values. (a) coupled substrate noise waveform sampled in DS1. (b) substrate noise waveform sampled in DS2.

Figure 4-39 shows two sets of coupled substrate noise and substrate noise waveforms seen by DS1 and DS2, respectively. The substrate noise is a tone at 1/4 the sampling frequency and a tone at 5/4 the sampling frequency. This implies the higher frequency tone is aliasing. Both substrate noise waveforms have the same sampled values in DS2, but give different sampled coupled substrate noise values in DS1. The coupled substrate noise values sampled by DS1 cannot be reliably predicted by the substrate noise values sampled in DS2. The only case where the coupled substrate noise value sampled by DS1 can be predicted by the substrate noise value sampled by DS2 is if the substrate noise has the same shape every clock cycle. Having the same shape in time means its frequency content is the same and thus the tones that alias down are always the same. Scaling the magnitude of the time waveform scales the magnitude of the frequency content uniformly. It does not change the tones that alias nor their relative proportions.

4.2.5.4 Proper SNSL Sensing

Since DS1 is in the configuration of a typical converter (converting a signal, not the substrate), the coupled substrate noise seen in DS1 is the important quantity to be minimized. For substrate noise generated by InvArrA which is similar to pad drivers and clock buffers, the SNSL sensing the substrate noise is adequate and will result in a reduction of coupled substrate noise sampled in DS1. For substrate noise generated by arbitrary digital logic like the DSRCP, the SNSL should sense the coupled substrate noise to be effective. Note that for substrate noise generated by InvArrA, the SNSL can also sense the coupled substrate noise to be effective. The straightforward solution of having SNSL sense the coupled substrate noise is to copy the input sampling circuit of DS1 and use it as the input sampling circuit of the SNSL so that substrate noise couples into DS1 and SNSL the same way. One problem with using this sensing scheme is that the amount of coupled substrate noise sensed is very small because the amount of substrate noise that couples into the input sampling circuit is solely due to mismatch. This reduces dynamic range and the effective gain of the D2Inv of the SNSL, which may render the SNSL useless as it oscillates wildly and eventually saturates in response to any disturbances.

One way of amplifying the coupled substrate noise is to increase mismatch of the differential halves of the SNSL input sampling circuit. This can be done with a non-zero DC bias or intentionally mismatched physical layout. However, in doing this the bandwidth of the SNSL input circuit may become mismatched with the bandwidth of the DS1. In fact, even if the sampling circuits of SNSL and DS1 are the same there will still be different bandwidths because of mismatches: input voltage independent mismatch and input voltage dependent mismatch. This difference in bandwidths might result in different amounts of aliasing depending on the nature of the substrate noise. In turn, this will result in different amounts of coupled substrate noise in the input sampling circuits of DS1 and SNSL as shown before. The solution to this problem is to prevent aliasing by running the SNSL loop very fast. Since the SNR requirements of the SNSL are not high, the SNSL can be designed as a small circuit, which can then be run at high frequencies without excessive power consumption. Of course, it should be noted that the problem of aliasing and thus coupled substrate noise sensing, can be minimized in the first place by reducing the input sampling bandwidths of the analog circuits as mentioned before in Section 3.3.7.

4.2.5.5 Applicability of SNSL to Analog Circuits in General

The SNSL can be configured to sense substrate noise the same way it couples into a delta-sigma modulator by replicating the input sampling circuit of the delta-sigma modulator. This is effective because noise in the first stage of a delta-sigma modulator is the most important; noise entering later stages is noise-shaped by the loop filter. However, this may not be true in other circuits where noise in later stages is not attenuated. For example, a 3rd order switched-capacitor filter does not have noise shaping. Any noise entering in the 2nd or 3rd stage of the filter can be as bad as entering in the first stage since each stage of the filter usually has roughly the same amount of gain. Despite this, the SNSL can still be effective if the input sampling circuits are all designed in a similar fashion. This will

result in less substrate noise cancellation because the coupled substrate noise sensed by the SNSL may not be exactly the same as coupled substrate noise in each part of an analog circuit. To maximize the effectiveness of the SNSL, analog circuits should reduce sampling bandwidths to minimize problems of aliased coupled substrate noise and run the SNSL at high enough frequencies to prevent aliasing effects.

4.3 Comparison of Techniques

Comparisons of techniques are difficult to make for substrate noise reduction and subsequent analog circuit performance improvement because the source of digital substrate noise varies, the substrates are not the same, packaging differs, etc. Also, the analog circuit, on which performance should be based, differs from system to system. Despite these difficulties in comparison of techniques, an attempt at summary has been made here for a quick comparison. Details of each technique can be found in the references. Table 4-2 summarizes some active and passive techniques. It is not an exhaustive list.

4.4 Summary

In this chapter, two techniques for minimizing substrate noise and its effects were explained and evaluated. The first technique uses a replica delta-sigma modulator to subtract coupled substrate noise out of the spectrum of the delta-sigma modulator converting a signal. This is effective in canceling input signal independent noise, but not input signal dependent noise, which dominates the delta-sigma modulator noise spectrum for large input signal amplitudes. The second technique uses an active substrate noise cancellation system, the substrate noise shaping loop (SNSL), to cancel generated coupled substrate noise in the band of interest. This technique works well for coupled substrate noise generated by an inverter array similar to pad drivers and clock buffers. This technique can also be effective for arbitrary digital logic as well. However, the DSRCP, the arbitrary digital logic used for this test chip, was not a suitable candidate because it did not generate much coupled substrate noise. For arbitrary digital logic that does generate enough coupled substrate noise, the SNSL can be reconfigured to sense the proper signal for delta-sigma modulator performance improvement. Simulations show that proper sensing for arbitrary digital logic results in cancellation of coupled substrate noise, which is the substrate noise coupling into useful analog circuits.

	Technique	Substrate noise reduction	Extra burden	Analog circuit	Improvement in analog circuit performance	Digital circuits used for substrate noise	Process technology	Comments
ACTIVE	Active Guard Band Filter [34]	40dB (8MHz)	Area, Power	–	–	Off-chip source	0.8um CMOS non-epi	Off-chip Opamp
	Active Noise Reduction [37]	15dB (1MHz)	Area, Power	–	–	Inverters	1.2um NMOS non-epi	
	Replica [0]	0dB	Area, Power (18mW)	16b DS	SNDR: 6dB (0-20kHz)	Inverters	0.25um CMOS epi	
	SNSL [0]	19dB (0-20kHz)	Area, Power (3mW)	16b DS	SNDR: -14dB (0-20kHz))	DSRCP	0.25um CMOS epi	
	SNSL [0]	27dB (0-20kHz)	Area, Power (3mW)	16b DS	SNDR: 10dB (0-20kHz)	Inverters	0.25um CMOS epi	
PASSIVE	Guard Rings [8]	0dB(Peak)	Area	–	–	Off-Chip Inverter	2um CMOS epi	
	Guard Rings [8]	14dB(Peak)	Area	–	–	Off-Chip Inverter	2um CMOS non-epi	
	Digital Clock Skewing [23]	5dB(Peak)	Extra Clocks	–	–	IQ Demodulator	0.35um CMOS epi	
	Wafer Cut [30]	35dB (1MHz)	Processing	–	–	Inverters	1um CMOS epi	
	Wafer Faraday Cage [29]	20dB (1GHz)	Processing	–	–	–	Si w/DRIE	No circuits
	SOI [32]	–	Cost	16b DS	8dB (0-50kHz)	IIR/FIR Filter	Bonded SOI	
	Low-Noise Digital Circuits	45dB(Peak)	Power (2X)	–	–	SCL	2um CMOS	
	Kelvin Grounding [5]	6dB (50MHz)	Routing & Dedicated supplies	–	–	Shift Registers and Adders	0.6um CMOS	
	Power Supply Filtering [5]	18dB (50MHz)	Routing & Dedicated supplies	–	–	Shift Registers and Adders	0.6um CMOS	

Table 4-2: Comparison of techniques for substrate noise minimization. [0] This work.

Chapter 5

Conclusions and Future Directions

5.1 Thesis Summary

This thesis presented a study of substrate noise and its effects on analog circuits. In addition, some techniques for minimizing substrate noise and its effects were explored in the context of improving analog circuit performance.

In the study of substrate noise, two delta-sigma modulators using the sampling scope concept were used to characterize substrate noise and its effects on analog circuits. An array of inverters was used to generate controlled substrate noise which allowed conclusions to be made about substrate noise characteristics and modes of coupling into a representative analog circuit, a delta-sigma modulator converting an external signal. It was found that substrate noise, which has decay time constants of a few nanoseconds and ringing frequencies of about 300MHz, couples in mainly through differential circuit asymmetries. Differential circuit asymmetries are input signal independent (*e.g.* process variations and layout) which gave rise to input signal independent noise (additive). Differential asymmetries are also input signal dependent (*e.g.* nonlinearity of circuit parasitics) which give rise to input signal dependent noise (mixing). Furthermore, substrate noise couples into the delta-sigma modulator primarily through parasitic capacitances which result in a high-pass version of the substrate noise appearing at the delta-sigma modulator input. These problems can be minimized with certain design techniques.

In the second part of this thesis, two techniques for minimizing substrate noise and its effects were examined. The first technique involves a replica delta-sigma converter which allowed post-processing of the output to correct for substrate noise effects. The second technique involves an active substrate noise cancellation system which is substantially different from past implementations. Both techniques allow cancellation of input signal independent noise, however only the latter technique reduces input signal dependent noise because it uses an array of inverters to reduce the actual substrate noise. The use of an active substrate noise cancellation system shows significant delta-sigma modulator performance improvement for substrate noise generated by an inverter array which is similar to digital pad drivers and clock buffers. However, the SNSL, the specific implementation of the substrate noise cancellation system, worsens delta-sigma modulator performance for substrate

noise generated by arbitrary digital circuits. This design can be modified for substrate noise generated by random digital logic by redesigning the SNSL to sense and cancel the coupled substrate noise seen by the analog circuits. Specifically, a replica of the input sampling circuit of the analog circuits can be used as the SNSL input sampling circuit.

5.1.1 Key Points

In short, the key points of this thesis are:

- Substrate noise, signals on the substrate voltage, and coupled substrate noise, apparent input signal to the analog circuits caused by the substrate noise, are different. For switched capacitor circuits, coupled substrate noise is a high-pass version of the substrate noise because substrate noise couples in mainly through mismatches of parasitic capacitances in the input sampling circuit.

- Since the mismatches of an input sampling circuit are input voltage independent (*e.g.* process variations and physical layout) and input voltage dependent (*i.e.* the input signal changes the differential symmetry because switch impedances and junction capacitances are non-linear), coupled substrate noise has an additive as well as a mixing (input-modulated) component. Furthermore, the additive component of coupled substrate noise dominates DS performance at low input amplitudes while the mixing component dominates DS performance at high input amplitudes.

- To cancel or reduce the effects of substrate noise on analog circuits, substrate noise should be sensed and characterized as it couples into the analog circuits. In an active substrate noise cancellation system such as the SNSL, substrate noise should be sensed the same way it couples into the analog circuits if substrate noise seen by the SNSL is not correlated with coupled substrate noise seen by the analog circuits. For the active substrate noise cancellation system to sample coupled substrate noise, a replica of the input circuit for the analog circuits can be used as the input circuit of the active substrate noise cancellation system.

- Analog circuits should minimize sampling bandwidths so that the aliasing of coupled substrate noise is reduced. Aliasing effects in sampled data circuits can also be reduced by running analog circuits, including the active substrate noise cancellation system, faster to reduce aliasing.

- Digital circuits have different characteristics which impact the amount and type of substrate noise they generate. Arbitrary digital logic circuits that implement complex functions have many relatively small gates that all switch at different times due to clock skew and gate delay, resulting in relatively low frequency substrate noise. On the other hand, clock drivers and pad drivers have large inverter gates all switching at the same time, resulting in relatively high frequency substrate noise.

5.2 Future Directions

The problem of substrate noise will continue to worsen as feature sizes scale down and system integration scales up. Although this thesis begins to tackle some of the associated problems, more will need to be done. The following are suggestions for further investigating substrate noise and its effects on analog circuits as well as improving on the active substrate noise cancellation system presented in the second part of this thesis.

5.2.1 Substrate Noise Study

The substrate noise produced by different digital circuits should be characterized as well as the effects of that noise on different types of analog circuits. The degradation of analog circuit performance depends on the mode of substrate noise coupling. Substrate noise study should also include different substrate materials such as non-epitaxial substrates. Their benefits should be quantified. The data gathered should allow greater insight to substrate noise and suggest circuit design practices that would be helpful to minimize substrate noise and its effects in different integrated circuits.

5.2.2 Active Substrate Noise Cancellation System

Although the SNSL shows decent coupled substrate noise and substrate noise reduction, performance of the system can be improved. First, proper sensing of the quantity to be canceled should be incorporated so that coupled substrate noise due to random digital logic can be canceled. Second, the inverter array, the D2Inv, can be designed to create more substrate signal and thereby increase the open loop gain of the feedback loop which increases dynamic range and the amount of noise reduction.

The SNSL can also be designed to run faster and shape substrate noise for a high frequency band of interest using a band-pass SNSL. An initial candidate may be intermediate frequencies (IF) applications where bandpass delta-sigma modulators are used. Ultimately, the maximum frequency band of interest will be limited by the speed of the circuits in the SNSL.

The SNSL should also be implemented on a high-resistivity substrate where chip geometry becomes important. Most likely, multiple and strategically placed substrate noise shaping loops will be needed to account for spatially dependent substrate noise.

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