Distributed Switch Circuits for High Voltage Pulse Applications

by

John Israel Rodriguez

S.B. in E.E., Massachusetts Institute of Technology (1997)

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

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Abstract

A distributed switch, in this work, is a "super switch" device formed by cascading individual switches in series. Series distributed switches can be used in situations where single solid state devices would otherwise fail to provide enough voltage blocking capability. Because the parasitics inherent in these circuits can hinder faster switching action, finding ways to overcome these parasitic effects requires knowledge of how they influence a cascaded switch. Models that describe the impact of the parasitic inductance and capacitance in these circuits are presented and studied. The approach taken is to realize that parasitics in a distributed switch form uniform LC ladders similiar to those used for modeling transmission lines by lumped approximation. As a result, the total circuit forms a switched LC ladder network. The natural LC structure of these switched networks are shown to share many interesting properties with classical lumped LC lines. Furthermore, when the parasitic elements of the line dominate the distributed switch response, the introduction of a defined uniform delay in the firing pattern of the individual switches can be used to enhance the speed of response. Experimental results to support these claims are presented for circuit responses in the microsecond to nanosecond regimes.

Thesis Supervisor: Chathan M. Cooke
Title: Principal Research Engineer

After ten years of apprenticeship, Tenno achieved the rank of Zen teacher. One rainy day, he went to visit the famous master Nan-in. When he walked in, the master greeted him with a question, "Did you leave your wooden clogs and umbrella on the porch?"

"Yes," Tenno replied.

"Tell me," the master continued, "did you place your umbrella to the left of your shoes, or to the right?"

Tenno did not know the answer, and realized that he had not yet attained full awareness. So he became Nan-in's apprentice and studied under him for ten more years.

-Zen Stories to Tell Your Neighbors

Acknowledgments

I wish to thank Dr. Chathan Cooke for suggesting this research topic and guiding me at every step of its development. I have always been amazed by his keen sense of intuition and savvy for engineering. Needless to say, his supervision and talents were instrumental to the completion of this thesis. He is a continual source of motivation to me and I am a better engineer because of him.

I am also deeply indebted to Professor Jeffrey Lang, my academic advisor. Whether Jeff realizes it or not, there were times when I was convinced he was the only person in the department who believed in me. In fact I owe my start as a TA in 6.002 Circuits and Electronics to him personally. The times I spent teaching under him, as well as Professors Wilson, Schlecht and Ram are perhaps the memories I treasure most about MIT. My experiences as a TA have complemented my education in ways that course work simply could not. The reason for this is simple; it's the students. Simply put, they are "amazing". Each unique in his or her own way and on the whole unbelievably diverse. I pray for their continued success and I cherish deeply the time I have spent coming to know and befriend them. I hope some of them will say the same.

Warmest thanks to Anne Hunter for rescuing me from those numerous department related jams I'm always finding myself in. But more importantly, for the pivotal role she played in my admission to the Masters of Engineering program. "Big" John Sweeney, for all of the equipment he lent me throughout my research, and always saying to me, "GO HOME!". And Jaydeep Bardhan, technical writer extraordinare, for his numerous suggestions and extensive editing of my thesis.

Also, my unending gratitude to those individuals I often owe my very sanity to. My colleagues Tim Denison, Steve Paik and Ketan Patel who listened to my incessant prattling about distributed switches. The Park Street Gang for their prayers and continual support. Kofi Aidoo, who I am convinced is just another aspect of myself, although, I'm sure he thinks it's the other way around. My roommate and long time friend, Carl Hibshman, who has come through for me time and time again. He is quite conceivably the most generous person I know. Did I mention he also proofread and corrected earlier drafts of my thesis, just because?

And of course, my caring family who never pressured me into doing something I did not want, but through love and affection supported me with all they had at times. I just want them to know, we did it.

En Domino Speas Mea.

John Israel Rodriguez

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Chapter 1

Introduction

1.1 The Problem

All solid state switches are limited by the maximum voltage they are capable of supporting while in their "off" state. Exceeding this voltage can cause a device to conduct prematurely or even destroy it. If a higher voltage switch is desired, a "super switch" structure can be constructed by cascading individual switches in series. This cascade is referred to as a distributed switch because it forms a switch which is "distributed" in space. Distributing a switch in space provides a means of dividing its voltage requirement amongst the individual devices that comprise it. This makes it possible to achieve a factor of N increase in holding voltage capability, where N is the number of single devices comprising the overall switch.

This higher voltage capability does not come without consequence. Because switches are devices that conduct current, energy must be stored in an associated magnetic field. This implies that each individual switch has a non-zero inductance associated with it. Device leads, for instance, account for this inductance to a first order approximation. Furthermore, if two conducting surfaces are present and insulated from each other, then electric fields must also exist, giving rise to capacitance. Such a capacitance exists between the pad to which a device is soldered, and the circuit's ground plane. An illustration of these parasitic inductances and capacitances is shown in Figure 1-1. As a result of cascading individual switches, these inductances

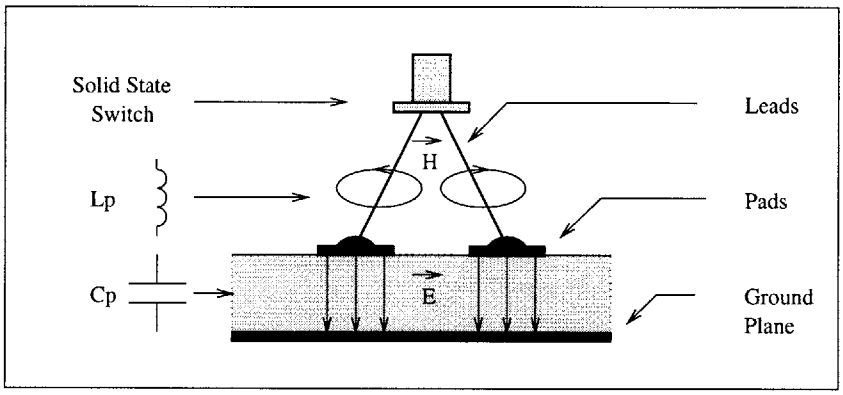


Figure 1-1: Switch Parasitics

and capacitances produce a very regular lumped LC line in which the switches are embedded. When the switching speed of the individual devices is slow compared with the dynamics of the LC line, the response of the system is dominated by the device physics, and the parasitics can be ignored. When the speed of the individual devices becomes comparable to the dynamics associated with the LC line, however, the parasitics effects can hinder peak switching action and should be taken into account.

1.2 Parameters of Interest

The behavior of a distributed line structure depends on a number of parameters. In order to understand the response of such a system, these parameters must be identified, and their influence on specific characteristics of the line studied. In particular, it is important to understand how the rise time, delay time, and overshoot of the output as well as the internal stresses are functions of the following parameters:

1. The number of stages or "N effects"

2. The inductance and capacitance of the line

3. Loading effects at both ends of the structure

4. Introduction of a fixed inter-switch delay into the switch firing pattern

The first three parameters apply to all lumped LC line structures, and the fourth parameter applies only to the switched line case.

1.3 Approach

The project began with a review of what is currently known about modeling lumped LC lines. The effects of the previously mentioned parameters were studied in the context of fixed LC line models via a combination of analysis and simulation. These models were later modified to include ideal switch elements to represent the first order behavior of solid state switches, and wave propagation in the cascade was then studied for different fixed inter-switch delays. In both of these cases, the systems were initially at rest; all inductor currents equaled zero and all of the capacitors were uncharged. Next the switched line was precharged in order to simulate how an actual distributed switch would behave in a high voltage pulse circuit. Lastly, experiments were conducted on three different distributed switches in order to verify the accuracy of the simulations and modeling.

1.4 Thesis Outline

The remainder of this thesis proceeds in stages. Chapter 2 forms the groundwork, starting with classical lumped LC lines. Their similarities to transmission lines, as well as their uses for modeling transmission lines, are discussed. Many important properties of these structures are also reviewed. Chapter 3 then introduces the uncharged, switched LC line by modifying the classic LC line to include switches. The behavior of this distributed switch is studied and compared against its classic counterpart. Chapter 4 discusses the advantages of "precharging" the switched line and how the precharging process affects the switch behavior. Chapter 5 documents the experiments used to validate the simulation models. Conclusions are drawn in Chapter 6 and areas for further research are suggested. Finally, Appendices A - H provide ancillary information relating to this research.

Chapter 2

Lumped LC Lines

2.1 Introduction

The topic of LC lines is one that has a rich history in electrical engineering. LC ladder networks have traditionally been prized for their uses in filtering as well as modeling the behavior of lossless transmission lines by lumped element approximation[5, 7]. LC lines serve as a starting point for understanding the behavior of distributed switches because they make up the structure in which the individual switches reside.

2.2 Modeling Lumped LC Lines

A variety of lumped element models exist for the purpose of describing transmission lines. One commonly used model consists of a series inductance L and a shunt capacitance C to ground as seen in Figure 2-1 below. Because of its shape this model

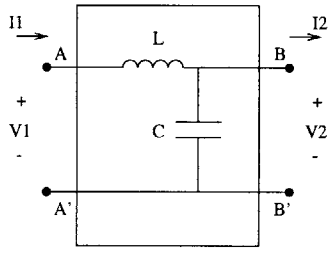


Figure 2-1: L-cell

is referred to as the L-cell for an LC line. The L-cell is an "unbalanced" model in the sense that it lumps all of the inductance on one side of the shunt capacitance. Other models exist that correct this asymmetry, such as the T-cell model, which does so by splitting the inductance equally on each side of the capacitance, or the π model, which chooses to split the capacitance instead. The accuracy of these various models is similar regardless of which particular model is used[3].

A lumped element line can be modeled by cascading N elementary L-cells to produce the two port network shown in Figure 2-2. Traditionally, the total inductance and capacitance of the line is divided evenly amongst the N cells for the purposes of approximating transmission lines (this convention is followed throughout this work). Each cell represents a discretization of the space variable for a true transmission line. Increasing the number of cells creates a greater resolution of the true behavior in space. This model is essential to understanding how distributed parasitics affect the propagation of waveforms through a lumped line structure.

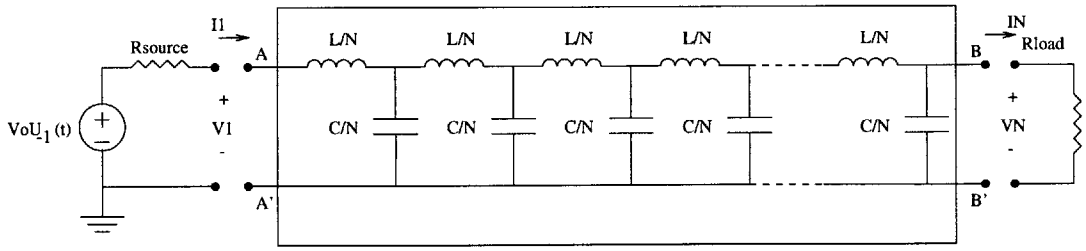


Figure 2-2: Lumped LC Line

2.3 Previous Work

Although lumped element models are mentioned frequently in literature there are few publications that discuss the number of cells needed to accurately model a transmission line[3, 8]. There are three major criteria that are traditionally investigated for demonstrating how the number of stages influences the behavior of a lumped LC line.

1. Relative Error on the ABCD Matrix Coefficients

2. Relative Error on the Propagation Delay T_o and Characteristic Impedance Z_o

3. Relative Error on the Natural Frequencies

The first and second criteria are intimately related and briefly discussed here because they are germane to the development of this thesis. The reader is referred to the appropriate references for further discussion of the third metric[3, 8].

2.3.1 ABCD Matrices

One way to describe the behavior of an L-cell is with its ABCD matrix. ABCD matrices provide a convenient method of describing the input output relationship of a two port system, doing so with the following equation

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix}. \tag{2.1}$$

Other system properties, such as the characteristic impedance of an L-cell and its associated propagation delay, can both be determined from its ABCD matrix. The corresponding ABCD matrix for the L-cell is given below

$$ABCD_{L-cell} = \begin{bmatrix} \frac{LCs^2}{N^2} + 1 & \frac{Ls}{N} \\ \frac{Cs}{N} & 1 \end{bmatrix}. \tag{2.2}$$

It is possible to describe the input output relationship of a lumped LC line that is N stages long by raising the $ABCD_{L-cell}$ matrix to the N^{th} power as shown

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \frac{LCs^2}{N^2} + 1 & \frac{Ls}{N} \\ \frac{Cs}{N} & 1 \end{bmatrix}^N \begin{bmatrix} V_N \\ I_N \end{bmatrix}. \tag{2.3}$$

As $N \to \infty$ it is known that a lumped LC line becomes a transmission line; likewise, its corresponding ABCD matrix is equivalent to the transmission line matrix. The

transmission line matrix equation is

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} Cosh(T_o s) & Z_o Sinh(T_o s) \\ Sinh(T_o s)/Z_o & Cosh(T_o s) \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix}, \tag{2.4}$$

where Z_o, the characteristic impedance and T_o, the propagation delay for a lossless line, are defined as

$$T_o = \sqrt{LC}, \tag{2.5}$$

$$Z_o = \sqrt{\frac{L}{C}}. \tag{2.6}$$

Using (2.5) and (2.6) the matrix relationship of an N stage LC line is recast into a form that resembles the matrix relationship of a transmission line,

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \frac{T_o^2 s^2}{N^2} + 1 & \frac{T_o Z_o s}{N} \\ \frac{T_o s}{Z_o N} & 1 \end{bmatrix}^N \begin{bmatrix} V_N \\ I_N \end{bmatrix}. \tag{2.7}$$

This manipulation allows for extraction of the characteristic impedance and propagation delay of the L-cell by pattern matching.

2.3.2 Characteristic Impedance and Propagation Delay

The properties of a transmission line can be completely described by its characteristic impedance and propagation delay. Consequently, the closer the corresponding lumped LC line parameters are to a true transmission line, the better the approximation becomes. Because discrepancies in the characteristic impedance will result in wrong reflections, and error in the propagation delay will cause poor propagation behavior, it is necessary to relate these parameters to lumped LC lines as functions of N.

Characteristic Impedance

The characteristic impedance of an L-cell is defined to be

$$Z_o^{L-cell} = \sqrt{\frac{B_{L-cell}}{C_{L-cell}}} = \sqrt{\frac{L}{C}}. \tag{2.8}$$

The L-cell has the same characteristic impedance as a lossless transmission line, unlike other models such as the T-cell, which only approach Z_o for large N. Furthermore, it can be shown by induction that the characteristic impedance of a cascade of L-cells is also Z_o.

Propagation Constant

Examination of equations (2.2) and (2.4) reveals that the corresponding propagation delay for the L-cell is

$$T_o^{L-cell}s = Sinh^{-1}(\frac{B_{L-cell}}{Z_o}). \tag{2.9}$$

Using the series expansion for Sinh and solving for T_o gives the following relationship:

$$T_o = NT_o^{L-cell}\left[1 + \frac{1}{3!}(\frac{T_o^{L-cell}s}{N})^2 + \frac{1}{5!}(\frac{T_o^{L-cell}s}{N})^4 + \frac{1}{7!}(\frac{T_o^{L-cell}s}{N})^6 + \cdots\right]. \tag{2.10}$$

It is evident from (2.10) that as N becomes larger, the propagation delay of an individual L-cell approaches $\frac{1}{N^{th}}$ the delay of a transmission line.

2.3.3 Rule of Thumb for Selecting the Number of Cells

Unfortunately it is difficult to quantify how many cells are needed to accurately model the behavior of a transmission line. Often a simple rule of thumb is used: *the propagation delay caused by an elementary cell should be smaller than one fifth the shortest rise time expected.* Mathematically, this can be expressed as

$$N \geq 5\frac{\sqrt{LC}}{t_{r10\%-90\%}}. \tag{2.11}$$

This guideline was derived under the assumption of an allowed 2.5% error on the relative characteristic impedance of a lossless T-cell[3].

2.4 MATLAB Simulation

Although current literature on lumped model approximations provides some insight into the lumping effects of LC lines, it does little to further one's understanding of the line's time domain behavior. To gain this understanding a study of lumped LC lines was conducted using time domain simulation techniques. A 10 stage, uniform LC line driven by a unit step voltage source was simulated in Matlab using state space models (See Appendix A). The following waveforms graphically illustrate various properties of lumped LC lines. The following major topics are considered: scaling in T_o and Z_o, the effects of load and source mismatching, and the influence of N.

2.4.1 Scaling by $T_o = \sqrt{LC}$

All other parameters held constant, varying an LC line's propagation delay results in a scaling of the time axis. As a result normalizing the time axis by T_o yields a general waveform in time. Figure 2-3 illustrates this by showing the output of a lumped LC line for two different propagation delays and then normalizing them. In all cases it is clear that changing T_o only results in a compression or expansion of the time axis.

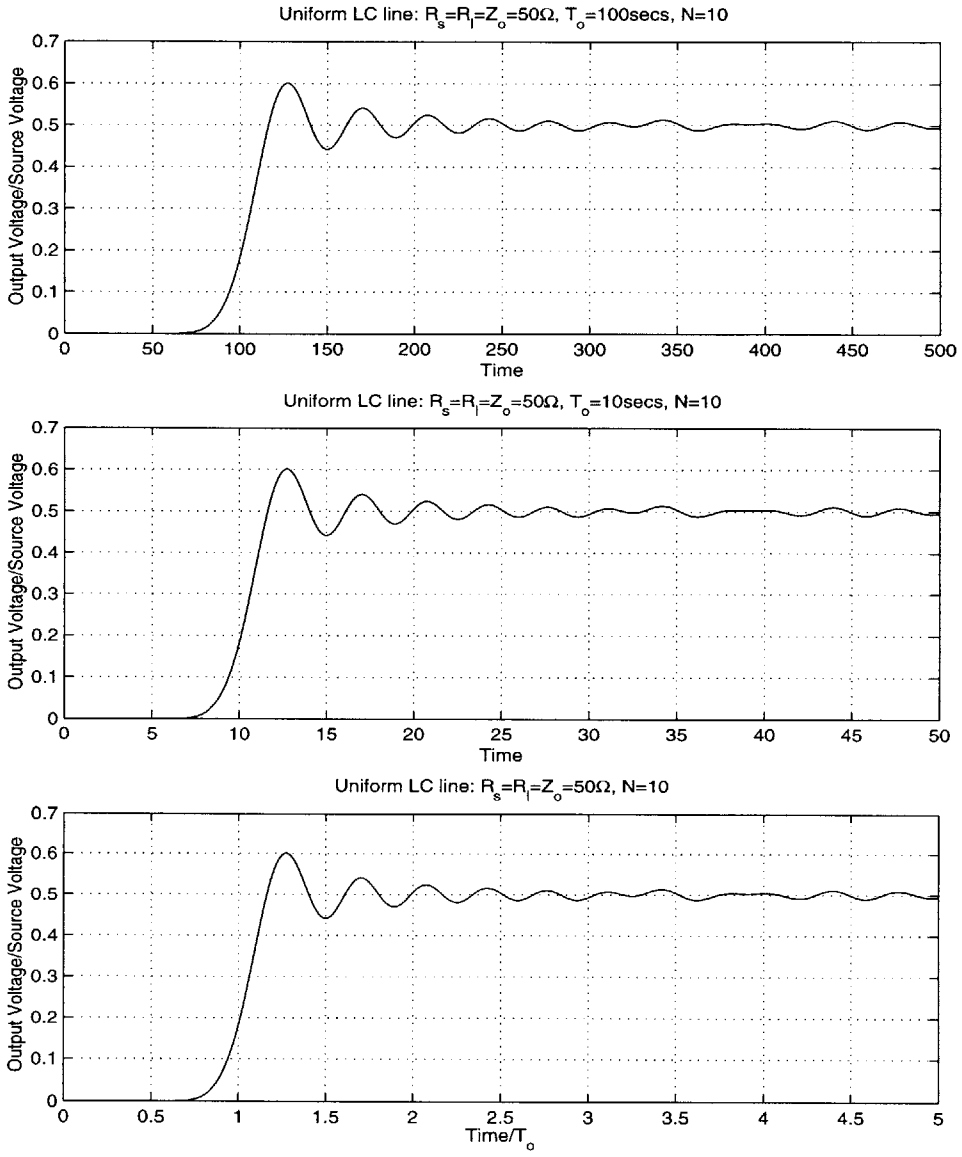


Figure 2-3: T_o Scaling on the output of various 10 stage LC lines

2.4.2 Scaling by $Z_o = \sqrt{\frac{L}{C}}$

For a normalized time axis, it can be shown that the wave behavior along a lossless LC line, depends only on the input, the number of stages and the relative impedances along the line. Mathematically,

$$WaveBehavior = f(Input, N, \frac{R_{Source}}{Z_o}, \frac{R_{Load}}{Z_o}). \tag{2.12}$$

Figure 2-4 shows this by giving the output response of two separate, double-matched LC lines. Although the characteristic impedance of each line is different, the behavior depends only on the the impedance relative to the source and load resistors.

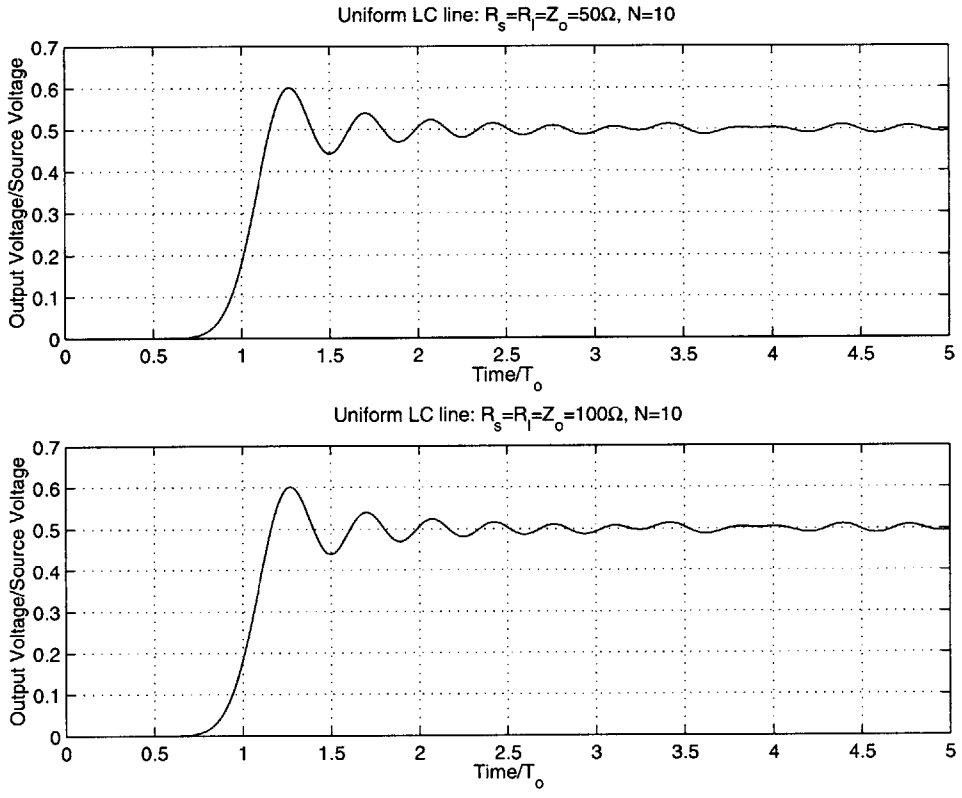


Figure 2-4: Z_o Scaling on the output of various 10 stage LC lines

2.4.3 Load and Source Mismatching

In an ideal transmission line driven by a step source, matching the load to the characteristic impedance results in no reflections. The value of the source resistance only affects the amplitude of the output. Similar responses are exhibited by an analogous LC line. In Figure 2-5 it is seen that the response is identical (excepting the amplitude) until about $3T_o$. Because the LC line is not a perfect transmission line, some

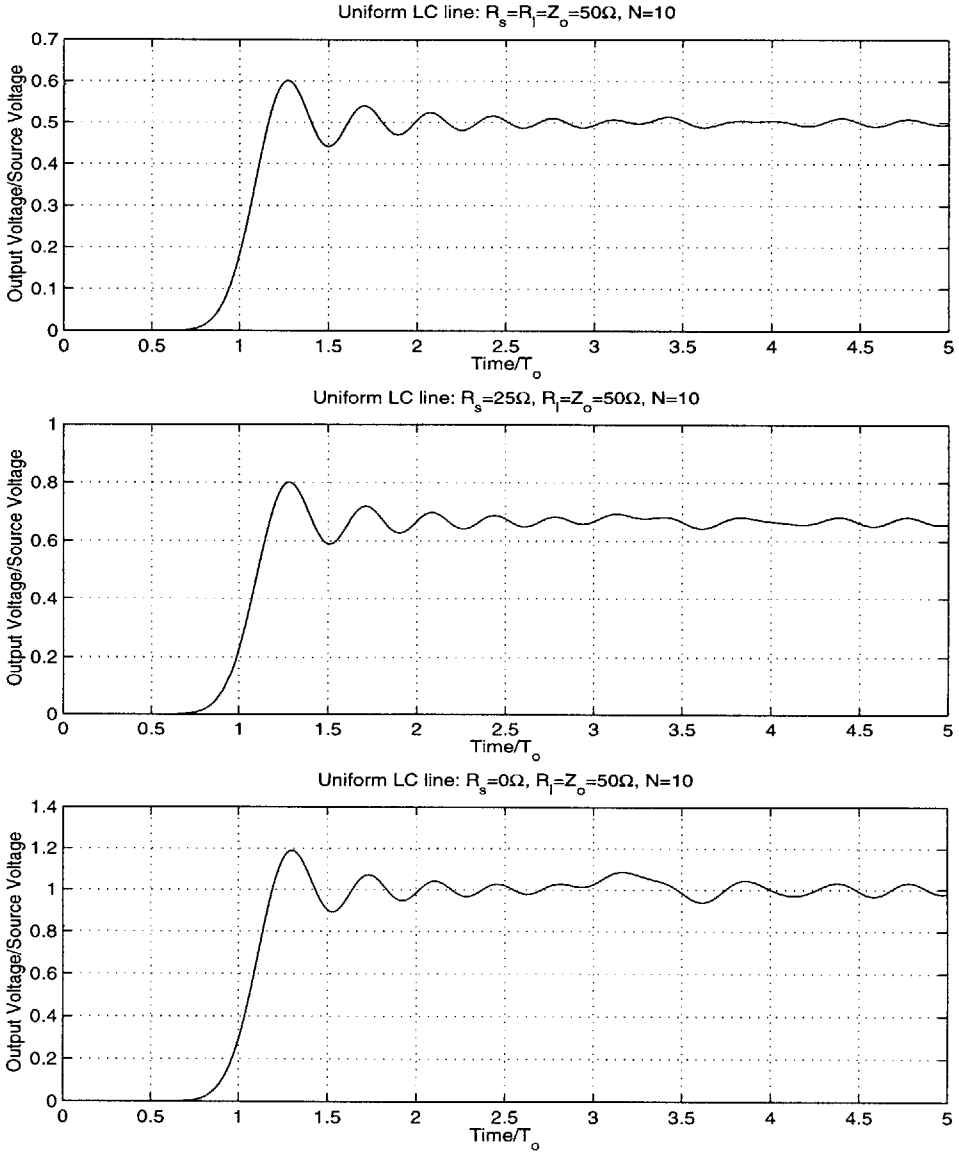


Figure 2-5: Output of a 10 stage LC line Driven by a Unit Step when R_{load} is matched and R_s is mismatched

reflections are evident after $3T_o$ which is approximately the time it would take the reflected wave to reach the output.

In Figure 2-6 R_{Load} and R_{Source} are mismatched to Z_o by a factor of two smaller and larger. As expected, the output behavior is the same (although the internal reflections, not seen here, are different).

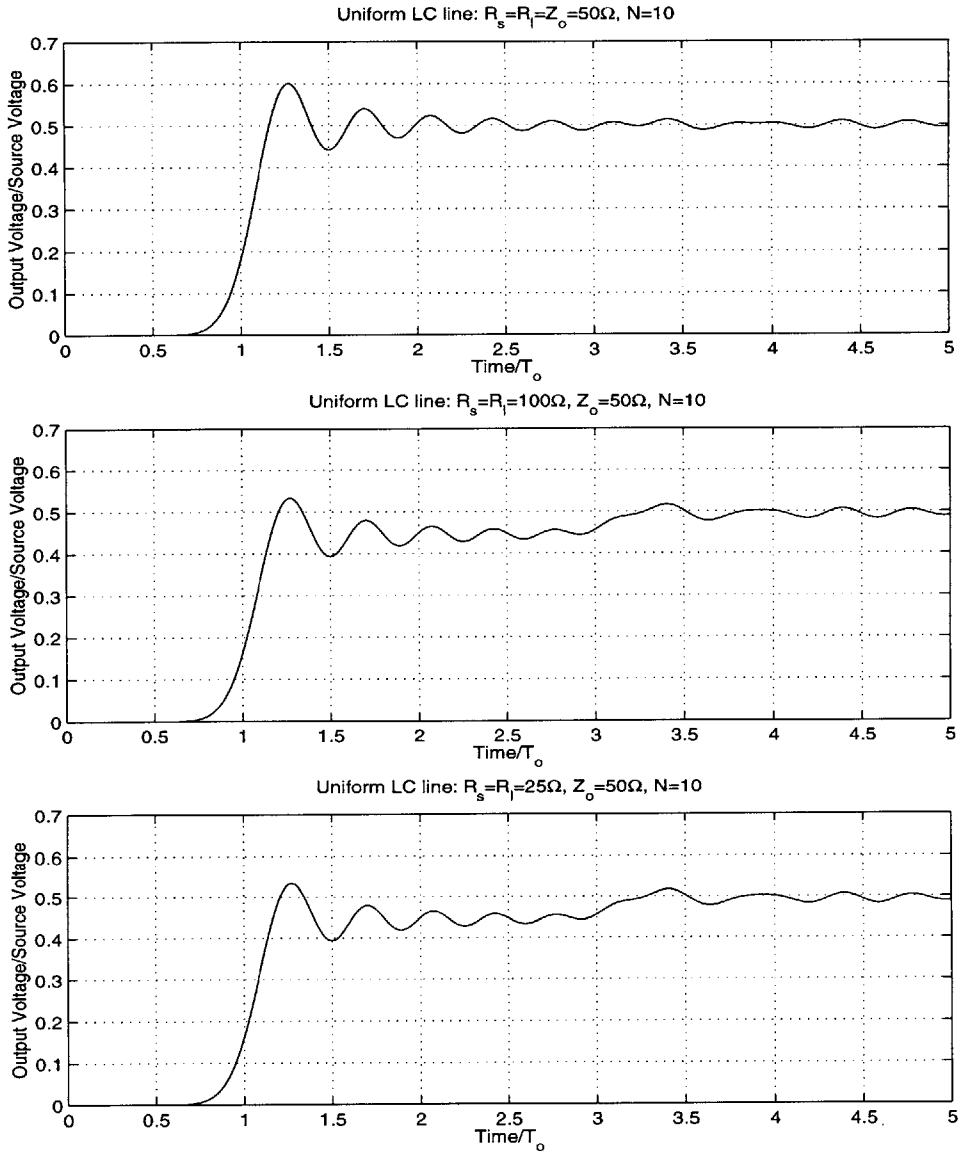


Figure 2-6: Output of a 10 stage LC line Driven by a Unit Step when $R_{load} = R_s = 2Z_o$ or $.5Z_o$

In Figure 2-7 R_{Load} is mismatched to Z_o by factors of two again, but R_{Source} has been set to zero. The lack of a source resistance to absorb reflections is now evident in the output response after $3T_o$.

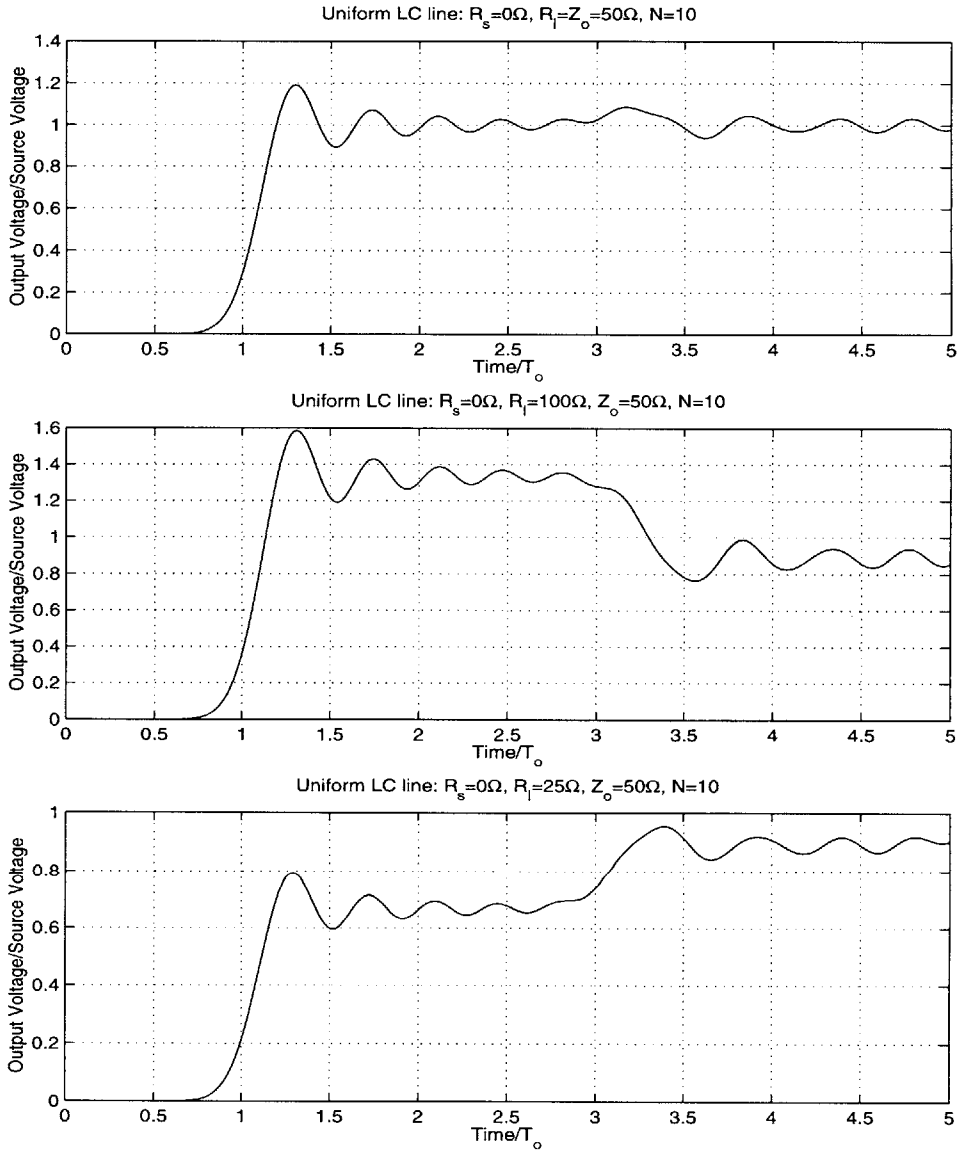


Figure 2-7: Output of a 10 stage LC line Driven by a Unit Step when $R_{load} = 2Z_o$ or $.5Z_o$ but $R_s = 0$

2.4.4 N-effects

The number of cells in an LC line plays an important role in the behavior of the structure. It is helpful to think of the influence of N from two viewpoints. The first is to keep the "electrical length" of the line fixed, and to subdivide the inductance and capacitance by N. This was seen earlier, and is the method by which transmission lines are approximated by lumped models. This interpretation is known as the viewpoint of increased resolution in space. The second interpretation is that increasing N lengthens the line; the inductance and capacitance per stage are kept constant and a larger N means a longer "electrical length". Because of the T_o scaling property, both viewpoints are related in time by a factor of N. To convert from increased resolution to greater length, one needs only to multiply the time axis by N. Figure 2-8 shows how increasing the resolution of the system affects the step response of a double-matched uniform LC line.

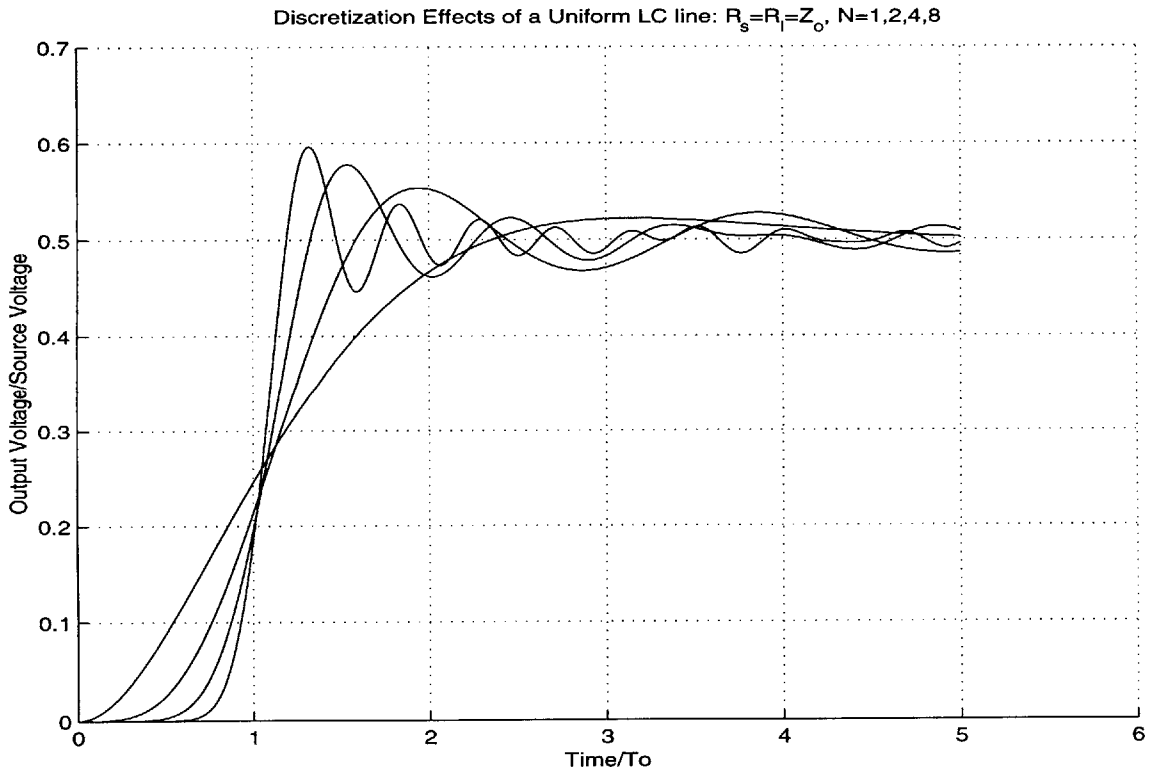


Figure 2-8: Discretization Effects of a Double-Matched, Uniform LC line: N=1,2,4,8

As expected, the rise time of the system decreases and the delay time approaches one T_o as N goes up. The system also exhibits a fair amount of ringing and overshoot as N is raised. This behavior is similar to the Gibbs phenomena except that in the limit, Gibbs approaches an overshoot of approximately 9% at the discontinuity while in this case it is higher than 25%. Figure 2-9 supports this by showing the behavior of a higher N system.

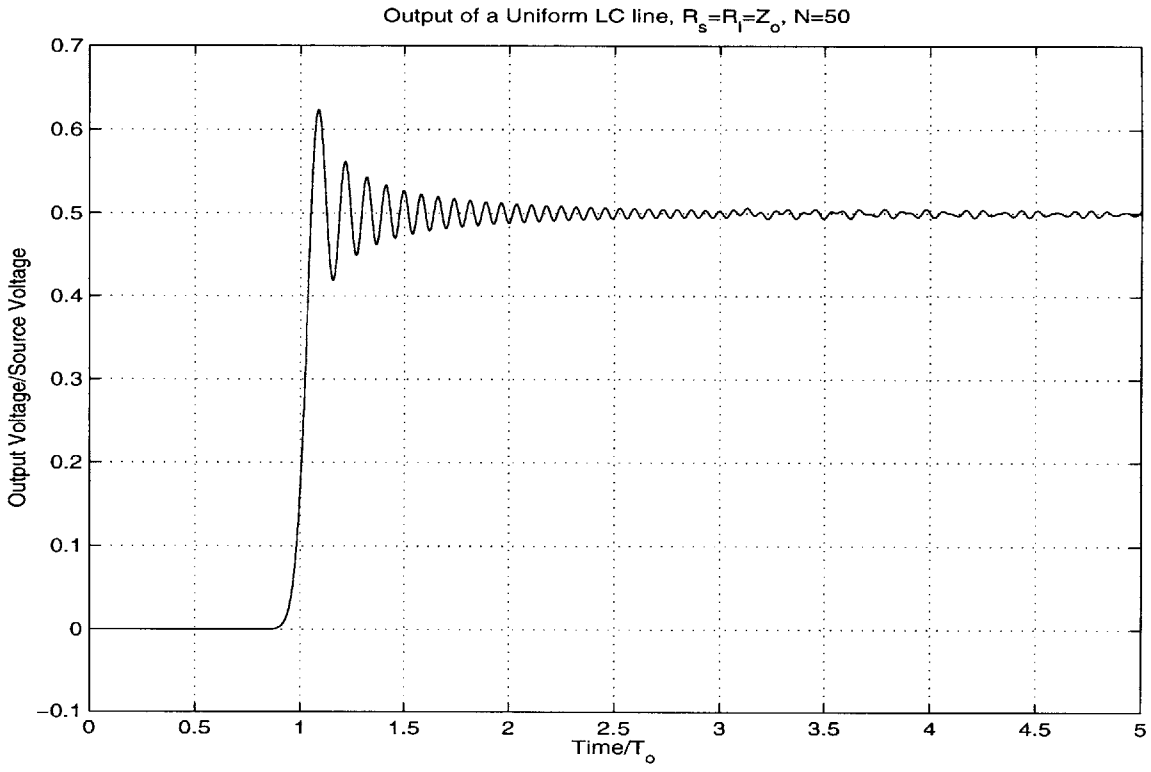


Figure 2-9: Unit Step Response of a Double-Matched, Uniform LC line: N=50

Overshoot

Figure 2-10 depicts the overshoot trend as a function of N for up to 50 stages. The overshoot increases rapidly to about 20% for the first 10 stages and then begins to taper off, steadily increasing to overshoots greater than 25% for N=50+.

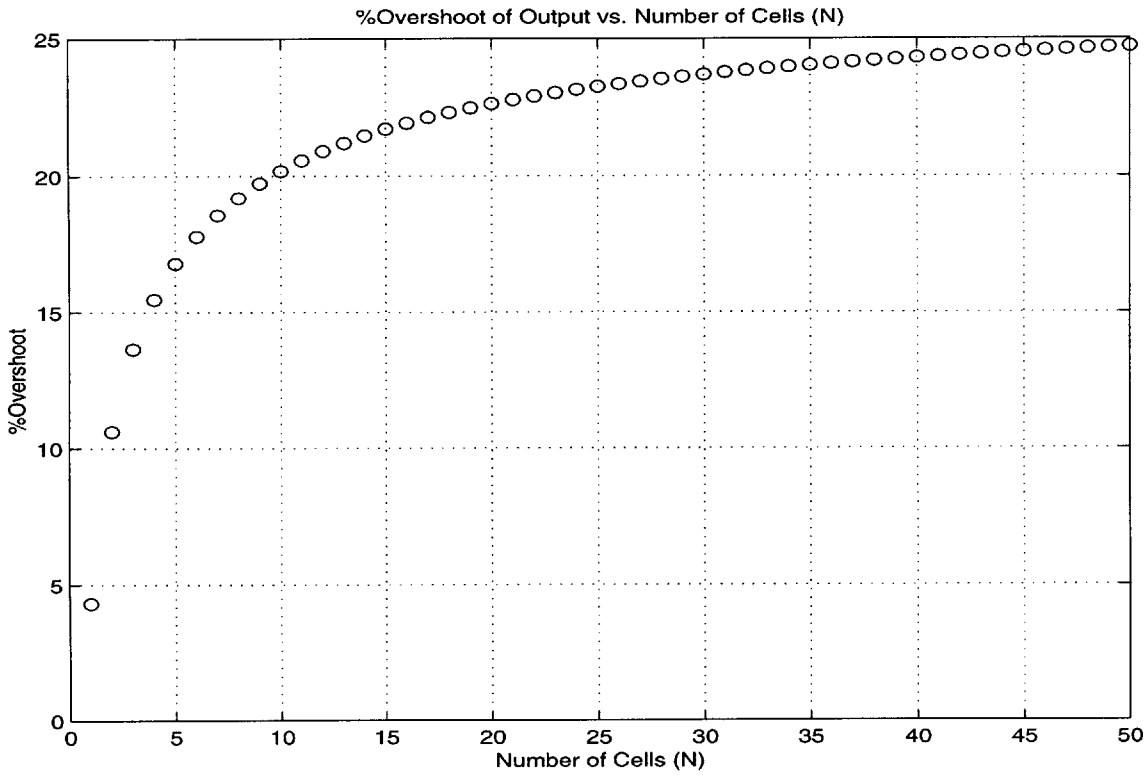


Figure 2-10: Output Overshoot of a Double-Matched, Uniform LC line vs. N

Rise Time

Figure 2-11 shows the influence of N on the output rise time. The time axis has been normalized by both T_o and $\frac{T_o}{N}$ to illustrate both interpretations of changing N. In the former, increased resolution, the rise time tends towards zero for large N. For the latter, lengthening the line causes the rise time to increase towards infinity with N.

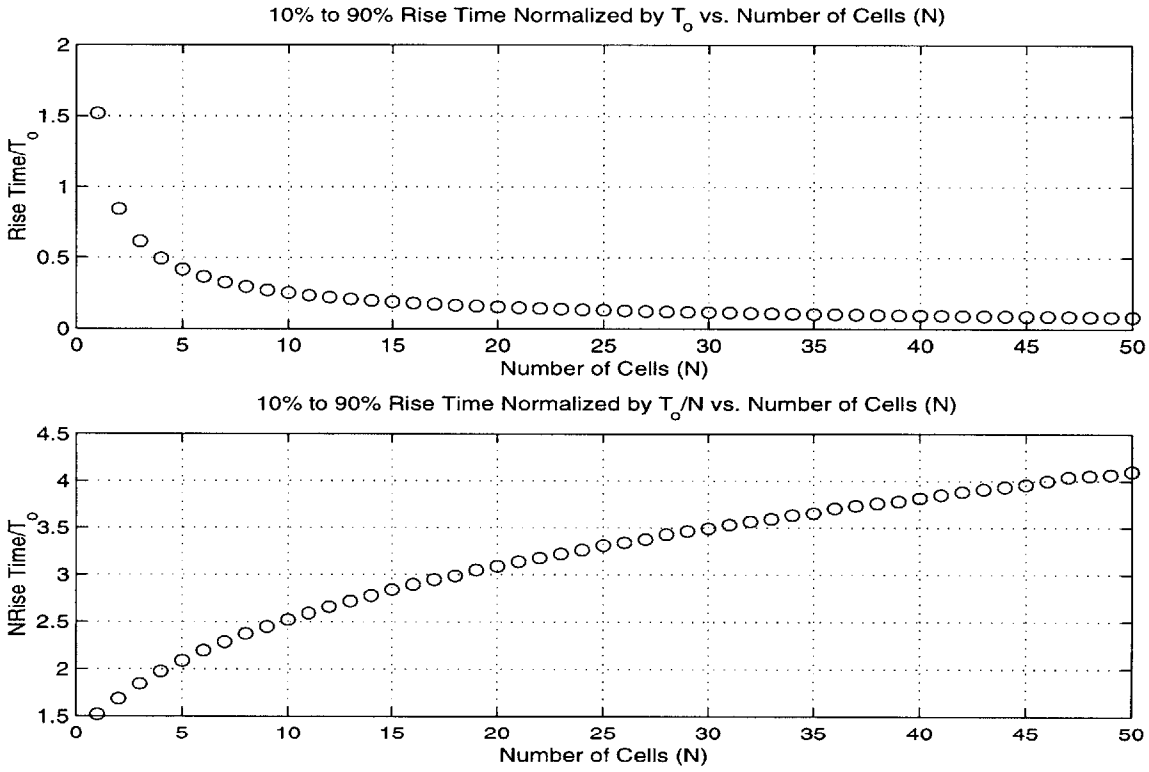


Figure 2-11: Output Rise Time of a Double-Matched, Uniform LC line vs. N

Delay

Lastly, Figure 2-12 presents the effect of N on the output delay. As expected, the delay approaches one T_o for higher N's, except for the case of N=1 which apparently has a delay very close to T_o to begin with. Similarly, lengthening the line simply results in a greater delay.

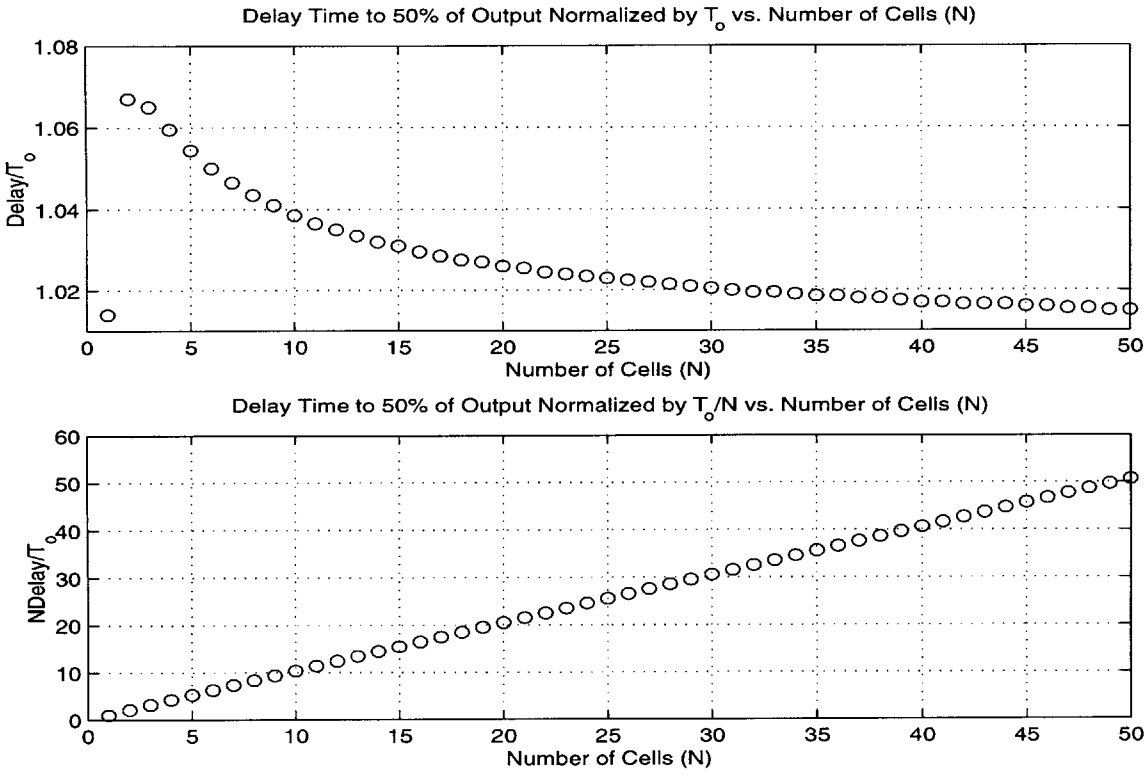


Figure 2-12: Output Delay of a Double-Matched, Uniform LC line vs. N

Chapter 3

Uncharged, Switched LC Lines

3.1 Introduction

This chapter introduces the uncharged, switched LC line. This structure is not a practical distributed switch because it does not properly divide the voltage across each switching element: its main purpose is to study how the inclusion of switch elements in the LC structure affects wave propagation through the line. In particular, the firing pattern of the switching elements gives a new degree of freedom for modifying the output response of the line.

3.2 Modeling Uncharged, Switched LC Lines

The LC model introduced in Chapter 2 is modified to include an ideal switch in series with the inductance L as seen in Figure 3-1. For now, the switch is specified to close at some arbitrary time, $T_{close} = t_0$, and the cell is defined to be at rest at that time.

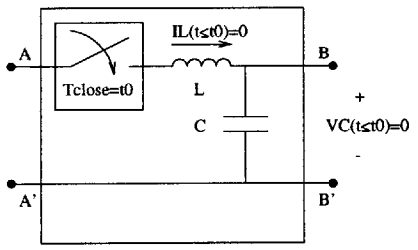


Figure 3-1: Uncharged Switch Model

The line model, given in Figure 3-2, follows as before by cascading N of the cells in series. Once again, the line is terminated at both ends and is driven by a voltage source in order to provide a means of exciting the system. Because the entire system is at rest at time t_0 the line is said to be "uncharged".

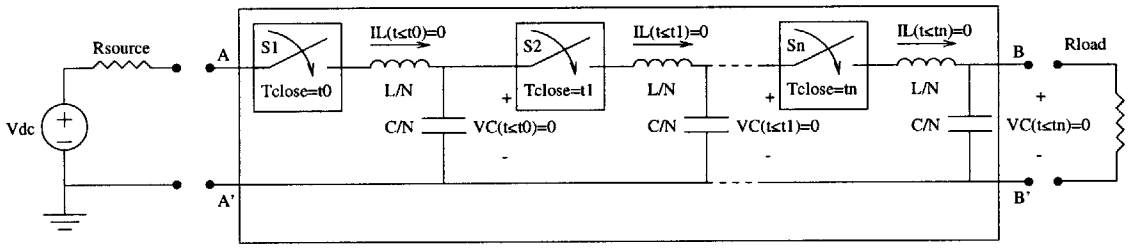


Figure 3-2: Uncharged, Switched LC Line Model

3.2.1 Scaling Property

In general, the inclusion of switching elements into a linear network yields a network that is nonlinear. However, if it is permissible to model the switching elements as ideal, then the system can be thought of as piecewise LTI[6]. Because these models use ideal switches exclusively, they are also piecewise LTI. It is this attribute that preserves the properties of scaling seen in Chapter 2.

Scaling by T_o

By definition, an ideal switch commutates instantaneously: no time is lost before the next stage is completely cascaded in the line. As each switch closes, it leads to a

longer LC line that inherits its current state from the previous line. In other words, with each switch transition, a new circuit topology is formed, whose initial conditions are set by the previous topology prior to switching. As long as the switch closing times are also scaled then the system's state from transition to transition will be identical on a normalized time axis.

Scaling by Z_o

Ideal switches constitute either a zero or infinite impedance, depending on their state. Consequently, the impedance from an LC cell relative to the switch impedance is also zero or infinite, regardless of the characteristic impedance of the line. Since it is only the relative impedance that matters, this property also holds.

3.3 Distributed Switch Triggering

This thesis does not attempt to study the impact of all possible firing schemes on a distributed switch; instead, one specific scheme, referred to as Fixed Inter-Switch Delay Triggering (FIDT) is investigated. FIDT is most readily compared to a sequence of N dominoes equally spaced in distance. Tipping the first domino starts a chain reaction in which each successive domino falls at a fixed time with respect to the previous domino.

Using a FIDT scheme the closing time of a switch, S_n, can be described mathematically as follows,

$$T_{close}(n) = K\frac{T_o}{N}(n-1), \tag{3.1}$$

$$T_o = \sqrt{LC}, \tag{3.2}$$

where the closing time referenced to the previous switch is equal to $\frac{T_o}{N}$ scaled by an arbitrary variable referred to as 'K'. It can be shown that 'K' is the inter-switch delay, ΔT_{ISD}, normalized by $\frac{\sqrt{LC}}{N}$. First define the inter-switch delay to be

$$\Delta T_{ISD} = T_{close}(n+1) - T_{close}(n). \tag{3.3}$$

Substituting and simplifying,

$$T_{close}(n+1) - T_{close}(n) = \frac{KT_o}{N}. \tag{3.4}$$

Solving for K,

$$K = \frac{[T_{close}(n+1) - T_{close}(n)]}{T_o/N}. \tag{3.5}$$

The circuit interpretation of this relationship is shown in Figure 3-3.

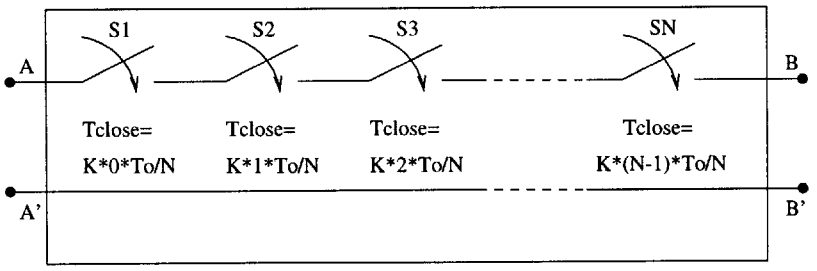


Figure 3-3: Fixed Inter-Switch Delay Triggering Scheme

3.4 PSPICE Simulation

To further the understanding of how a FIDT scheme affects the response of an uncharged switch line, a simulation study was conducted using PSPICE. PSPICE's component library includes switch models (in addition to traditional passive components) which facilitated the modeling of distributed switch lines. In addition, its ability to post-process waveforms made it well suited to this study. Unfortunately, the version of PSPICE used has a component limitation that prevented the study of lines greater than 15 stages. Because of the sheer number of parameter combinations and a desire to experimentally verify simulation results, the majority of simulated lines were chosen to be five stages long. A distributed switch of N=5 is long enough to demonstrate the major effects of the lumping process, but is short enough to build hardware versions for testing.

3.4.1 Wave Propagation(K)

Of primary interest is how the K factor influences the way waves propagate through a distributed switch. In order to establish a reference, the base case is defined to be K=0, which corresponds to simultaneously triggering all of the switches. From a circuit viewpoint all of the switches are shorts at time t=0, meaning that the switched structure is identical to the lumped LC line seen in Chapter 2. Figure 3-4 shows the voltage propagation at each node for a step input into a double-matched, uncharged switch line for K=0. It is observed that the 3rd to last wave has the greatest amount of overshoot, but that the 2nd to last wave suffers the greatest sustained ringing. Also because of the lumped model approximation, the input is able to affect the output starting at t=0+, although only by an infinitesimal amount.

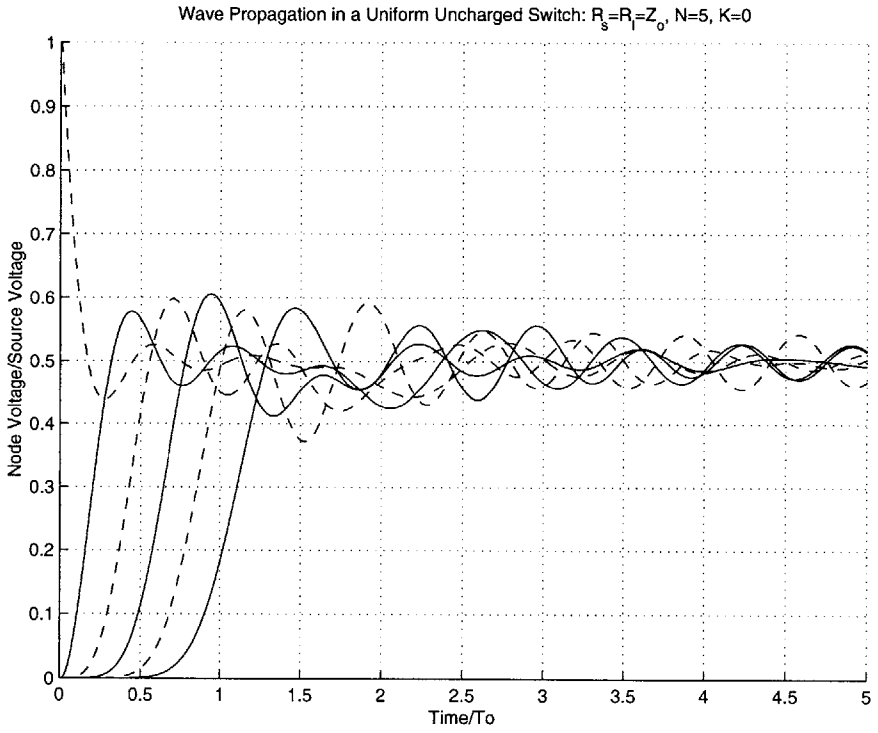


Figure 3-4: Voltages in a Uniform Uncharged Switch: $R_s = R_l = Z_o, N = 5, K = 0$

If a K=1 is used, a noticeable effect is clearly seen on the capacitor voltages with time. Specifically, the overshoot throughout the structure has increased. In essence, the switches have provided a means of building up the energy in the preceding stages

before charging up the next cell. Again, the third to last node has the greatest overshoot, and the second to last has the most sustained ringing. In addition, the switch delays have produced a "sharpening" effect on the node voltages, the rise times have decreased throughout. This improvement in rise time can be attributed to two major factors. The increased voltage driving each stage implies a larger $L\frac{di}{dt}$ and hence a faster rise time. Also, the switches prevent the source from affecting the response at each node before they are switched; this further sharpens the initial rise of each wave.

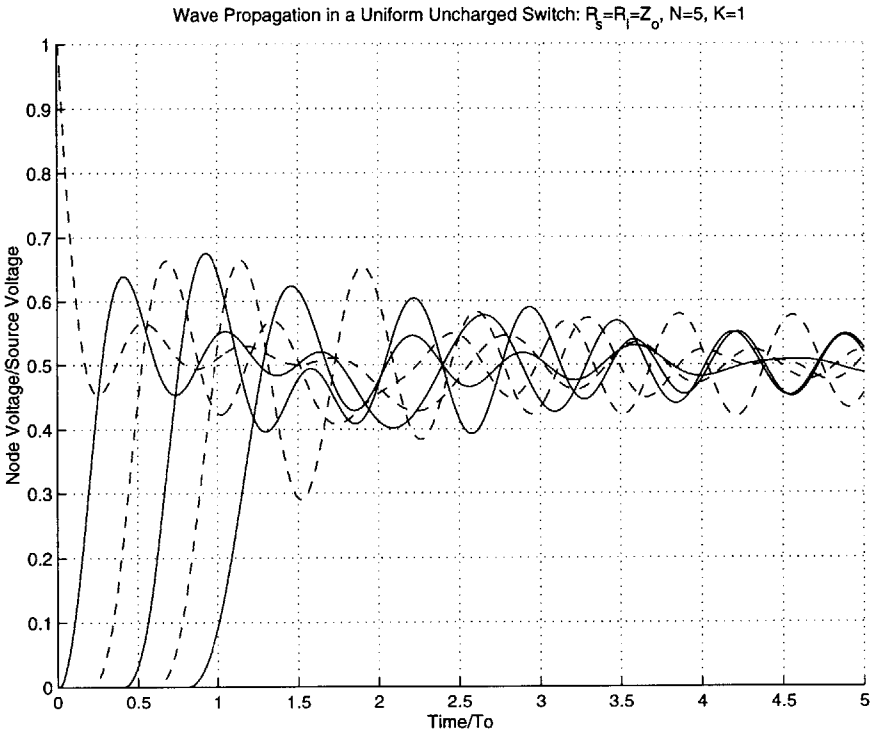


Figure 3-5: Voltages in a Uniform Uncharged Switch: $R_s = R_l = Z_o, N = 5, K = 1$

3.4.2 Internal Stresses

When designing an actual high voltage switch, care must be taken to insure that not only is the output response of the system well behaved, but that the internal behavior is not destructive. This raises the issue of controlled internal stress, since eventually a structure that contains real switches internally is to be built. Introducing

a systematic delay into the LC structure provides a means by which wave propagation can sum destructively within the distributed switch. However, since the uncharged, switched line does not reduce the individual switch stress correctly[1], the focus here is exclusively on the voltage across each capacitor and the current through each inductor. A study of the "true" switch stress will be saved for the precharged case where it is appropriate.

Capacitor Voltages

Parametric sweeps of the peak positive and negative capacitor voltages for $0 \leq K \leq 3$ were conducted. Figure 3-6 shows the plot of peak positive voltages. It is noted that the peak voltage of C5 is actually below 63% of the source voltage for $K < 1$. This corresponds to an overshoot at the output of less than 26%, because the final voltage is actually half of the source voltage due to the equal double-ended termination. For

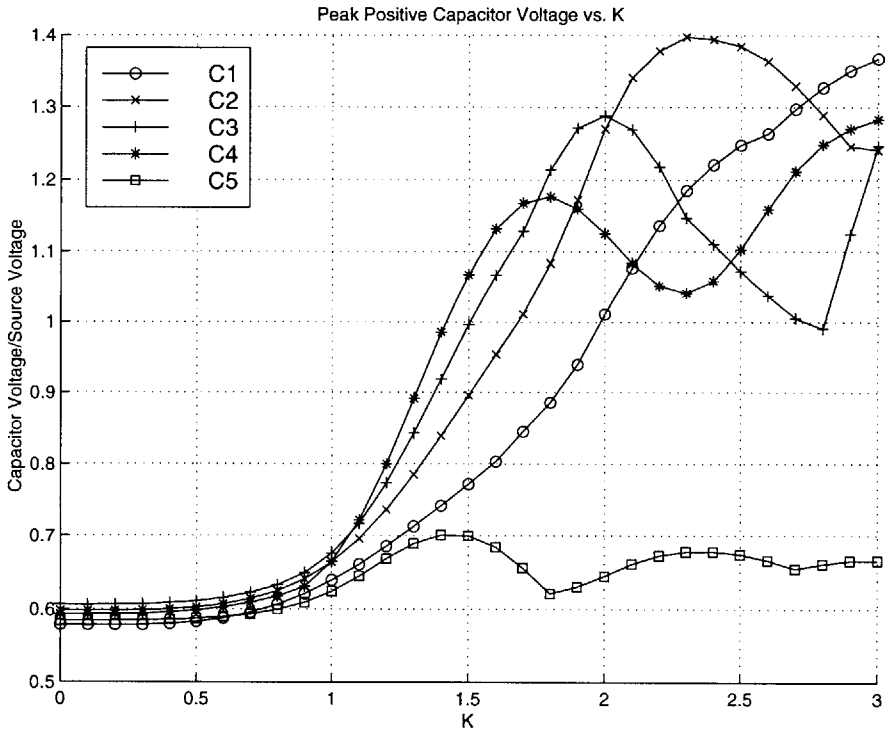


Figure 3-6: Peak Positive Capacitor Voltage vs. K

[1]This should be obvious because the first switch has all of the source voltage across it at t=t_0.

$K > 1$ the stress at the internal nodes grows rapidly although the output remains bounded up to at least K=3.

Figure 3-7 provides additional insight into the behavior of the system for higher values of K. In particular, starting around K=1.4, oscillatory behavior large enough to cause the node voltages to swing negatively is seen. This phenomena begins at the second to last node, the node which typically exhibited the most sustained ringing. As K is increased, this negative transition moves down the structure towards the source end. At no time does the output exhibit a negative peak voltage for $K < 3$.

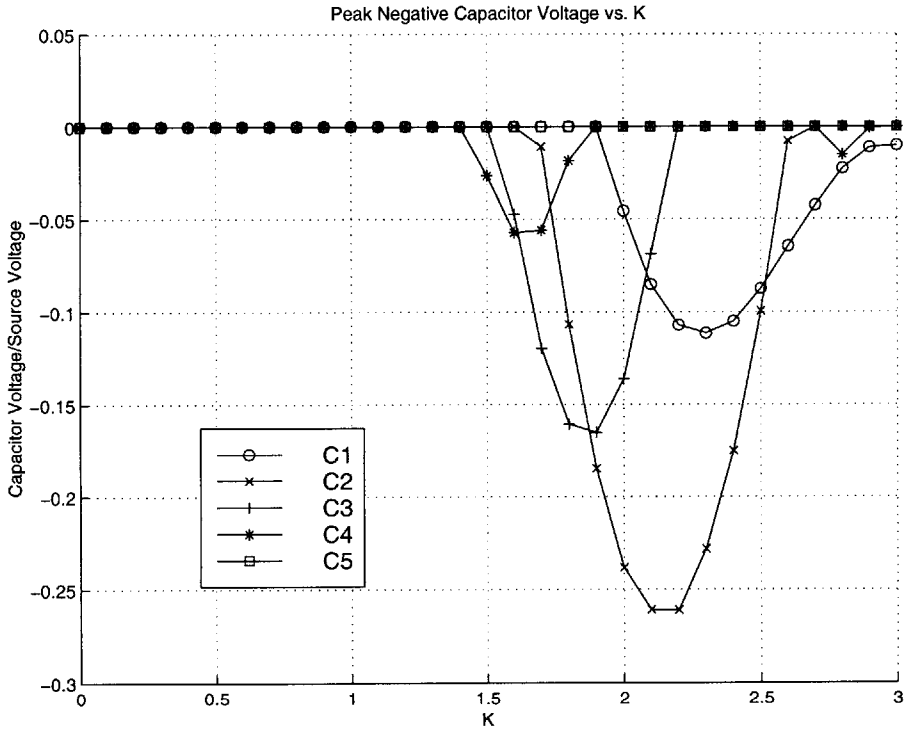


Figure 3-7: Peak Negative Capacitor Voltage vs. K

Inductor Current

Perhaps more important in terms of the switch stress is knowledge of how the inductor current behaves throughout the line. Because the inductor is modeled in series with the switch, this is the current the switch must tolerate. Figure 3-8 shows how the peak

current of each inductor, normalized by the steady state DC current[2] is influenced by K. Here the inductors closer to the load must tolerate greater currents for $K < 1$. Again as K is increased beyond one $\frac{T_o}{N}$ additional reflections cause ringing to increase quickly. Interestingly, the inductors at the extremes of the line suffer less overshoot than those within the line, presumably because they are closer to the termination resistors.

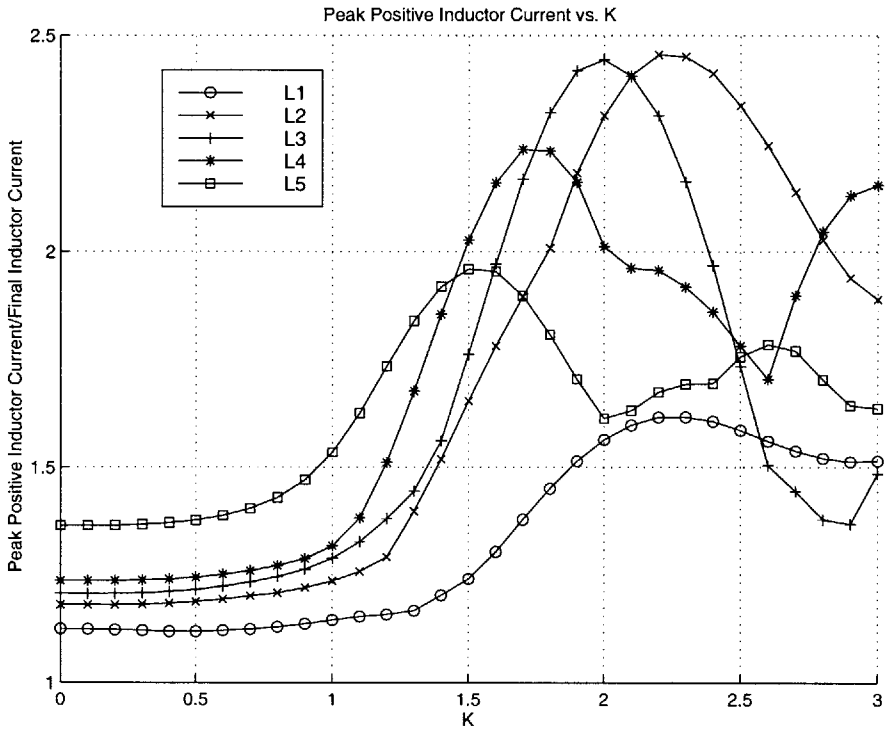


Figure 3-8: Peak Positive Inductor Current vs. K

Figure 3-9 gives further evidence that operating around K's greater than one can be hazardous. In particular, around K=1.5 the currents in the inductors begin to reverse directions completely! This corroborates the phenomena seen previously with the capacitor voltages and suggests that the mode of operation in the line is changing. In a true switched line, careful attention should be paid to look out for similar behavior, especially since many solid state switches do not support bidirectional current!

[2] $I_{DC} = V_{source}/(R_{source} + R_{load})$.

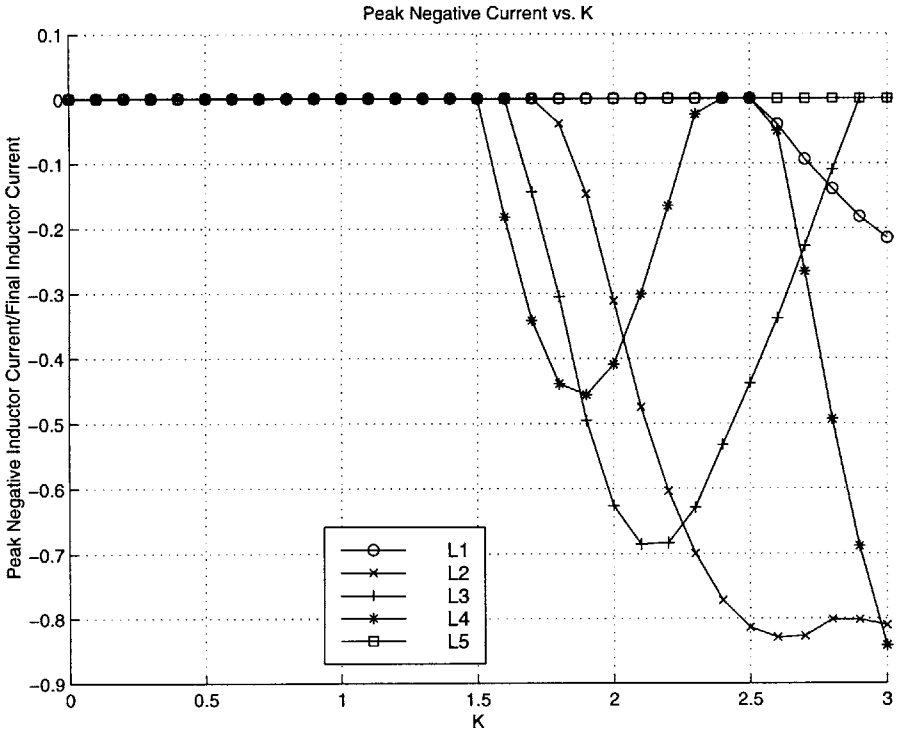


Figure 3-9: Peak Negative Current vs. K

3.4.3 N Effects

The influence of the number stages in an uncharged switched line is just as important as in the fixed LC line case. Unfortunately, the introduction of the K variable greatly increases the parameter space. Consequently, an exhaustive study of how N affects the response of the line over a broad K space is difficult. To make study of this aspect feasible, K was limited to values of one and smaller. This is a reasonable constraint, since it was seen that for large K the switched line began to suffer increased internal stresses. As mentioned earlier, the data was further restricted to N$\leq$ 15 due to simulation limitations. The following plots show the 10% to 90% rise time of the output versus the delay time to 50% of the output for double-matched, uniform, uncharged switched lines as functions of the implicit variables K and N.

T_o Normalization

When these results are normalized by T_o an interesting picture emerges in Figure 3-10. As witnessed in Chapter 2, when K=0, increasing N, and hence resolution, eventually yields a line that has zero rise time and a delay of T_o. Introducing a finite K means that the delay will be greater than this. However, it appears that for $0 \leq K \leq 1$, increasing the resolution yields a response that still converges to the step response of an ideal transmission line. To understand this behavior, the response of an infinitely resolved switched line needs to be understood.

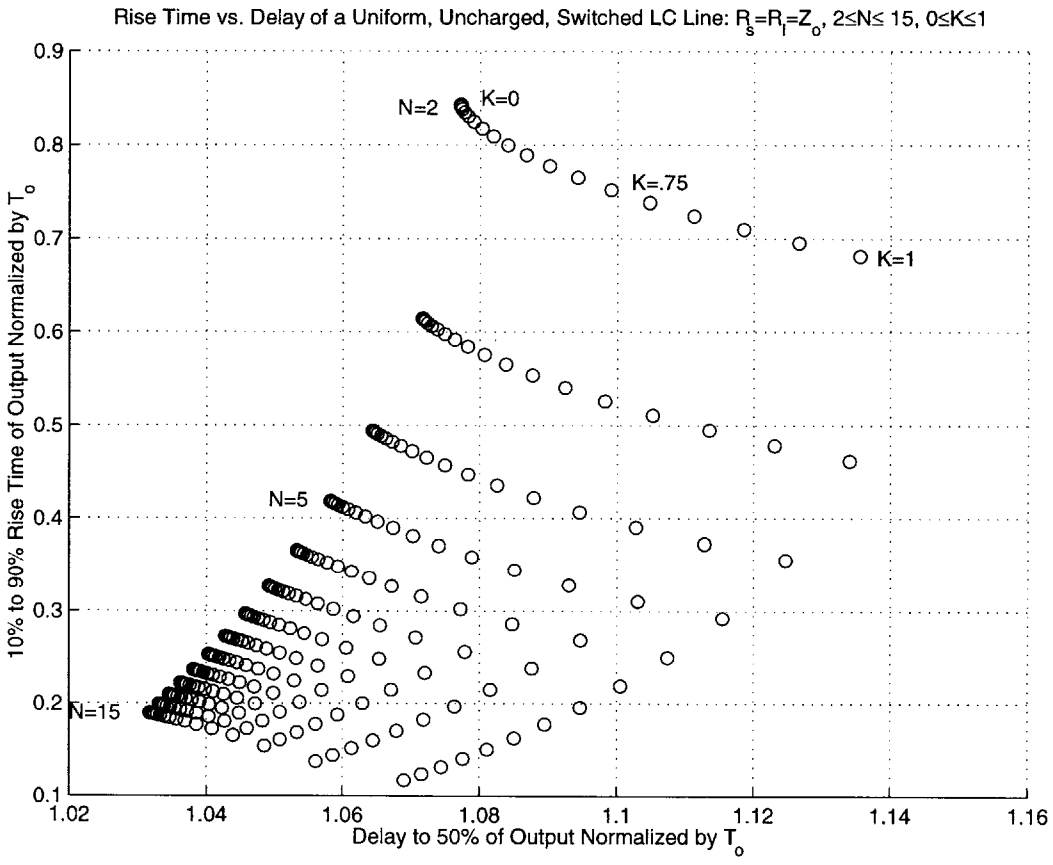


Figure 3-10: Rise Time vs. Delay of Uncharged LC Line Normalized by T_o

An easy way to understand the limiting behavior of an infinitely resolved switched line is to examine a similar structure whose limiting behavior is the same, but whose analysis is easier. First, note that as $N \to \infty$ the two port behavior of an L-cell is identical to an infinitesimal slice of a transmission line as depicted in Figure 3-11.

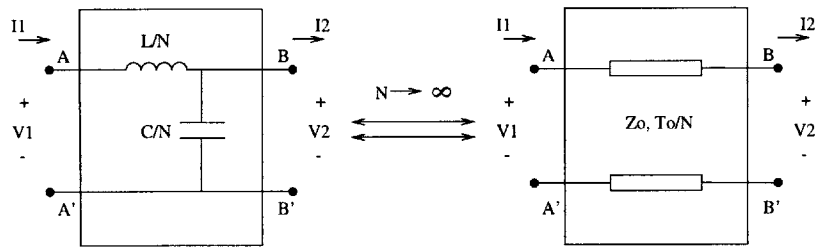


Figure 3-11: Single L-cell equivalence for Large N

Next, develop the analogous switched line model shown in Figure 3-12, where instead of LC cells, individual transmission line sections have been used. In the limit, this model has a behavior that is identical to an infinitely resolved switched LC line. Unlike in the switched LC case, however, the response of this model can be determined by inspection using transmission line theory.

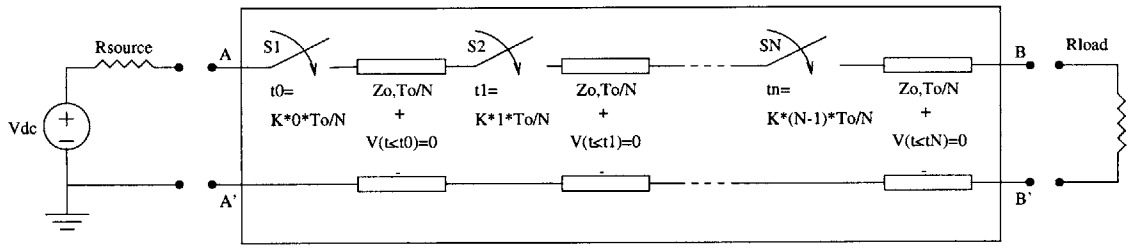


Figure 3-12: Uncharged Switched, Transmission Line Model

It is now clear why, for K≤1, the step response of an uncharged, switched LC line approaches the step response of an unenergized transmission line. In the limit the switches close at the moment the wave front reaches them or sooner. As a result their presence is not noticed in the structure! In a future study, it would be interesting to confirm that for values of K>1 diverging behavior does occur due to switch induced reflections.

$\frac{T_o}{N}$ Normalization

Figure 3-13 shows how varying N and K affect the rise time and delay time of the uncharged switched line. Here, normalization by $\frac{T_o}{N}$ was chosen to provide the longer line interpretation. The primary value of this plot is that it allows a designer to see

how to trade off additional delay for increased rise time performance. As expected, the output delay and rise time increase as the line is made longer. Also evident is that making the line longer makes the K factor more significant. This makes sense, since increasing the number of stages also provides more distributed delay in the structure, thereby making it more effective. Lastly, unlike the previous viewpoint, lengthening the line does not converge to a solution since the delay and rise time simply approach infinity in the limit.

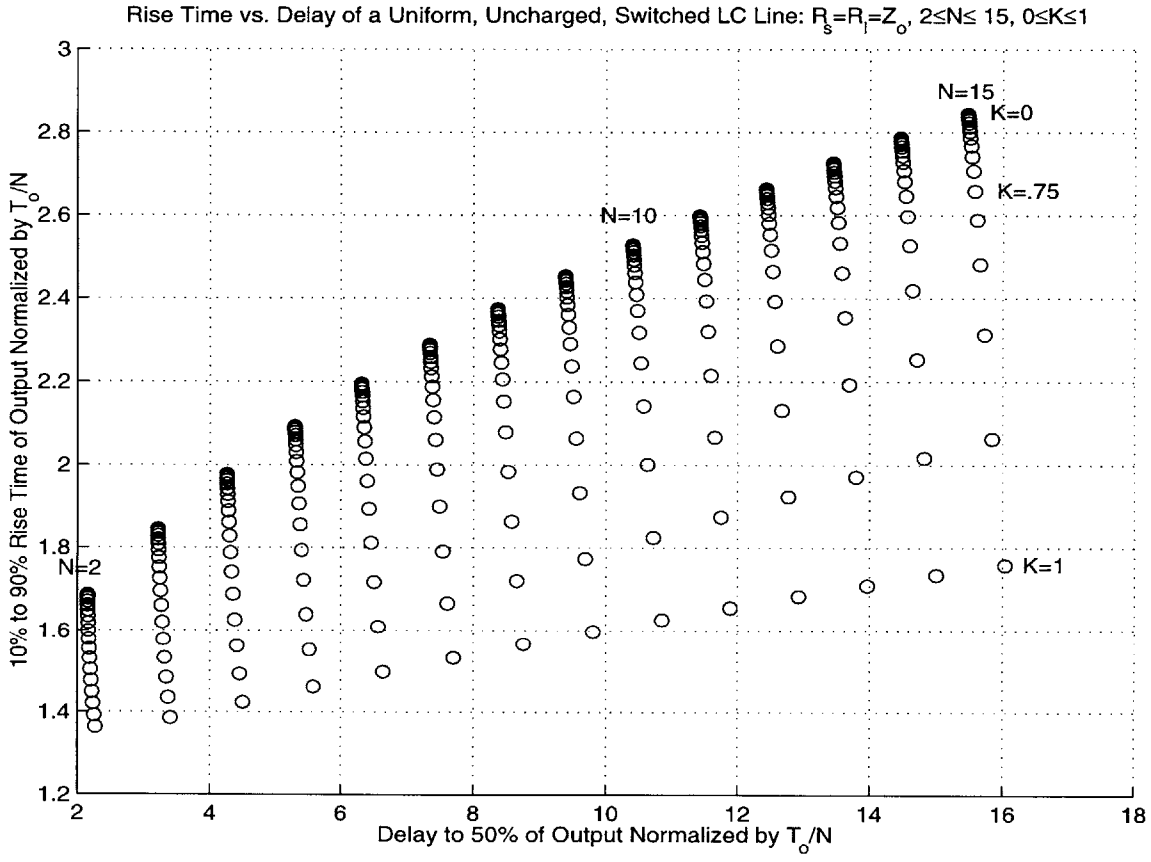


Figure 3-13: Rise Time vs. Delay of Uncharged LC Line Normalized by $\frac{T_o}{N}$

Chapter 4

Precharged, Switched LC Lines

4.1 Introduction

This chapter introduces the precharged, switched LC line. Unlike the uncharged switch, the precharged switch is a practical circuit. Precharging the switch allows for the equal distribution of voltage throughout the line prior to switching. This goal, equalizing the voltage across each switching element, is the primary reason for studying and building distributed switch lines. Consequently, this chapter focuses on understanding how the precharging process affects the behavior of a switched LC line.

4.2 Modeling Precharged, Switched LC Lines

The precharged switch model is a natural extension of the uncharged version, in which the capacitance of the former model is charged to an arbitrary voltage before the switch closes. Furthermore, the inductor current is again defined to be zero in order to be consistent with the switch's off state as illustrated in Figure 4-1.

Cascading N cells yields the analogous two port line model given in Figure 4-2. Here the individual capacitors are precharged in such a way as to insure that voltage across each switch is $\frac{1}{N^{th}}$ the total voltage across the line. In addition some changes in the external networks are evident from the uncharged model. Notably, there is no

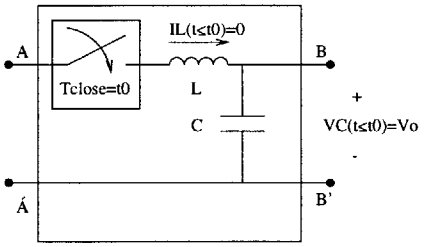


Figure 4-1: Precharged Switch Model

need for a voltage source to drive the A-A' port; pulse generation is accomplished by charging a sizeable output capacitor during the precharging process. The Thevenin network is therefore replaced by a termination resistor, R_{term}. The load resistance, R_{load}, is coupled via the output capacitor to the switch B-B' port. Besides supplying the necessary charge for the outgoing pulse, the capacitor insures that in steady state (prior to switching) the voltage across R_{load} is zero.

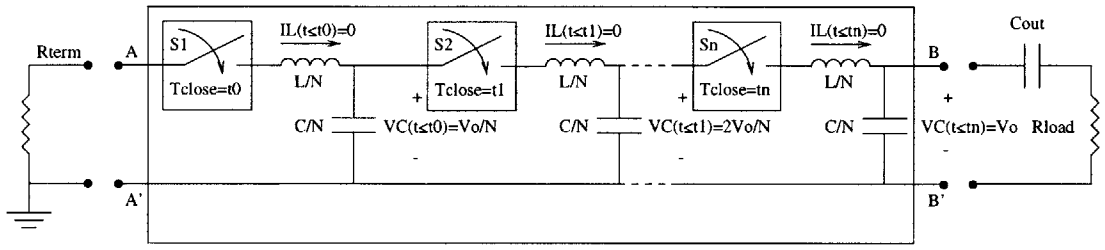


Figure 4-2: Precharged, Switched LC Line Model

4.3 PSPICE Simulation

As with the uncharged switch model, an extensive study of the precharged switch model was conducted using PSPICE. Again, the majority of precharged switches studied were five stages long, uniform and double-matched. Studies on the effect of mismatching R_{term} to the characteristic impedance in a uniform line were carried out. Additionally, the benefits of tapering the impedance of the line to match a smaller R_{term} while still matching R_{load} on the opposite side is shown.

4.3.1 Wave Propagation(K)

As was the case with the uncharged switch, the primary interest for simulating the precharged switch is to see the influence of the K factor on the output. For comparison, the K=0 case shown in Figure 4-3 is examined. Starting at time zero, each node voltage begins at its respective precharge value and eventually approaches half of the precharge voltage after the parasitic transients have died down[1]. The output, which is capacitively coupled, experiences a negative outgoing pulse as the switch collapses. The output takes approximately T_o to rise to its final value and resembles a ramp in the process. This is to be expected, the voltage along the line is linearly distributed at discrete points at t=0.

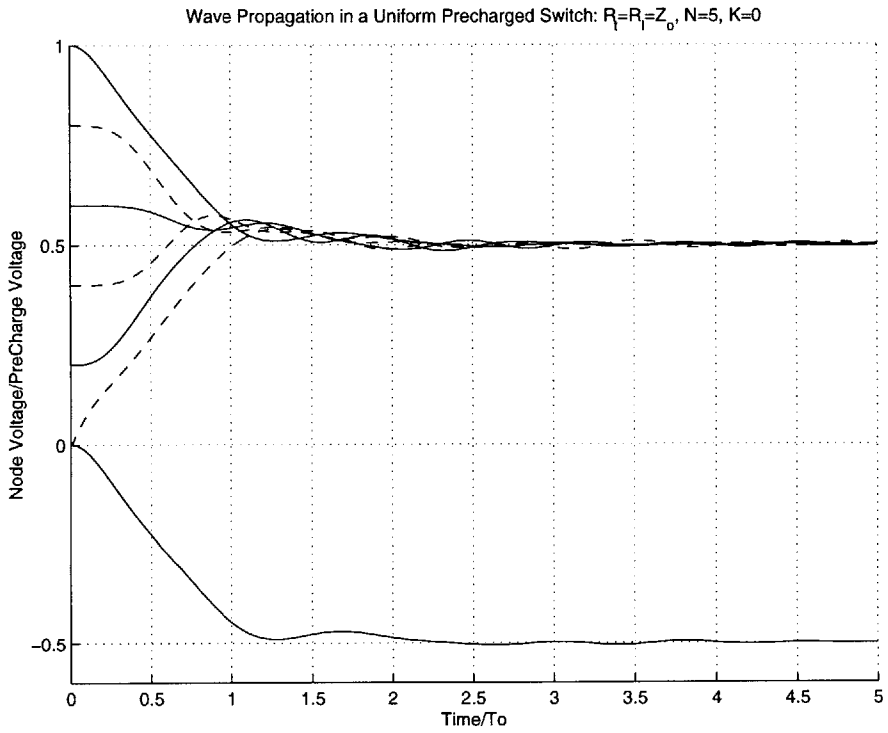


Figure 4-3: Voltages in a Uniform Precharged Switch: $R_t = R_l = Z_o, N = 5, K = 0$

It was seen in the uncharged case that larger values of K provide a decrease in the rise time of the output at the cost of additional delay and overshoot of the output. A

[1]The output capacitor was chosen to be large enough to prevent any noticeable droop of the output while the parasitic induced transients were decaying away.

similar phenomena holds for the precharged case too. Figure 4-4 shows the response of the system for K=1. The triggering delay has decreased the rise time by about a factor of three, and increased the overshoot to about 20% of the final value. Increased internal ringing is also apparent when compared to the base case.

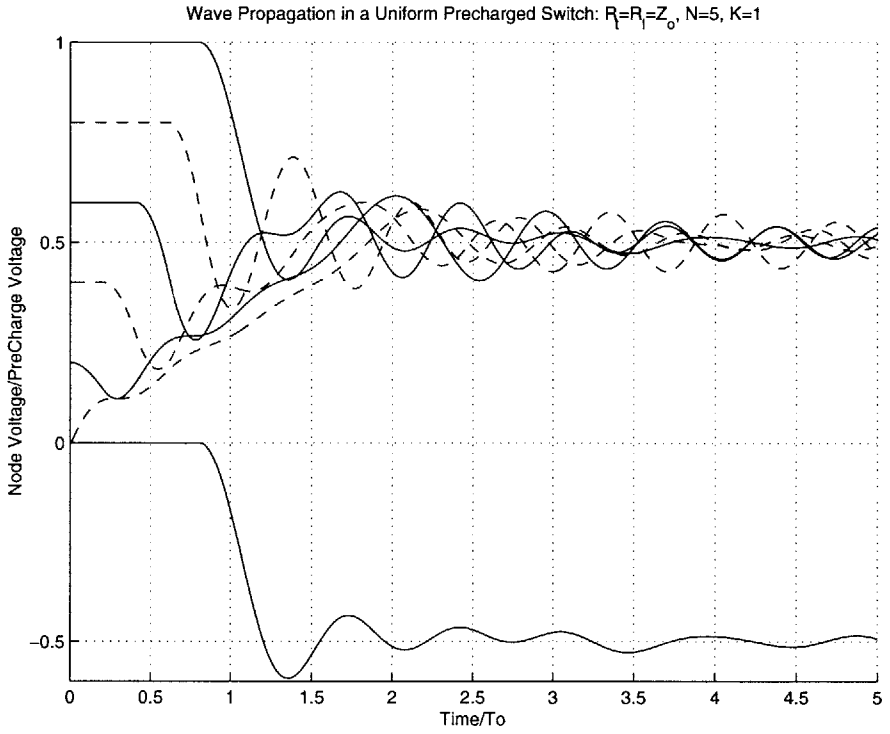


Figure 4-4: Voltages in a Uniform Precharged Switch: $R_t = R_l = Z_o, N = 5, K = 1$

4.3.2 Impedance Matching

The topic of impedance matching is important when building a precharged switch. Until this point, only distributed switches matched to Z_o at both ends have been examined. Unfortunately, terminating the line in its characteristic impedance on the non-load end results in a loss of half the voltage at the output. It is therefore appropriate to ask what effect a smaller R_{term} will have, since this would result in a higher output voltage. Classical transmission line theory suggests that a mismatch will produce reflections at that end of the line. However, it is unclear whether introducing a finite K might "worsen" those reflections.

Termination Mismatching

The effects of mismatching the precharged switch by terminating it in half of its characteristic impedance and then by simply shorting it are examined. In both cases, the response was calculated for two values: K=0 and K=1. If the termination resistance is chosen to be half of the characteristic impedance, the output voltage is expected to be be two-thirds of the precharged voltage instead of one-half. This increase is seen in Figure 4-5. The effect of mismatching is seen sooner in the precharged switch than the uncharged switch because the energy is already present in the line. For K=0 the effect is seen after one T_o, the time it takes the reflected wave to return to the output. In addition, this reflection has increased the rise time of the output, because the output must now swing through a higher voltage.

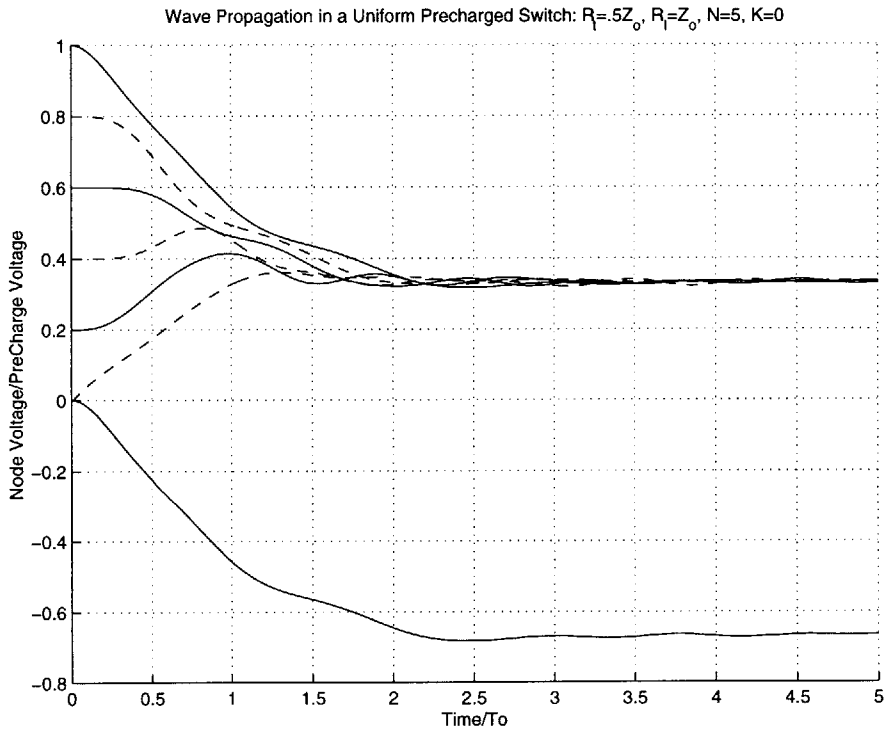


Figure 4-5: Voltages in a Uniform Precharged Switch: $R_t = .5Z_o, R_l = Z_o, N = 5, K = 0$

If the K factor is increased to one, the response of the system speeds up as before but the increase in reflections at the output becomes more evident as seen in Figure 4-6.

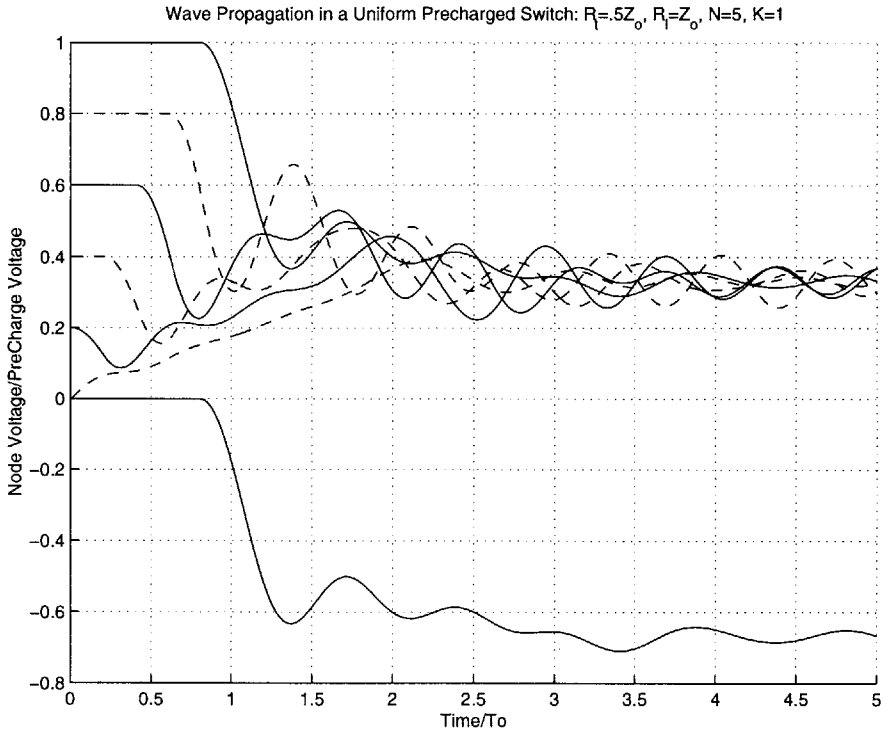


Figure 4-6: Voltages in a Uniform Precharged Switch: $R_t = .5Z_o, R_l = Z_o, N = 5, K = 1$

If the termination resistance is set to zero, then the full voltage is applied to the load. The consequence of doing this is that it takes twice as long for the output to reach its final value as seen in Figure 4-7. In this case, the importance of the termination resistor is made clear when the K=1 case is observed. Without the resistor to dampen out the multiple reflections caused by the switching, the output behavior becomes erratic and a significant decrease in output fidelity is seen as shown in Figure 4-8. To convey how long the ripples in the output can last, Figure 4-9 show the output responses of the previous two figures over longer time axes. For the K=0 plot, the ripples are almost nonexistent, whereas for the K=1 case, oscillatory behavior is evident even after $10T_o$.

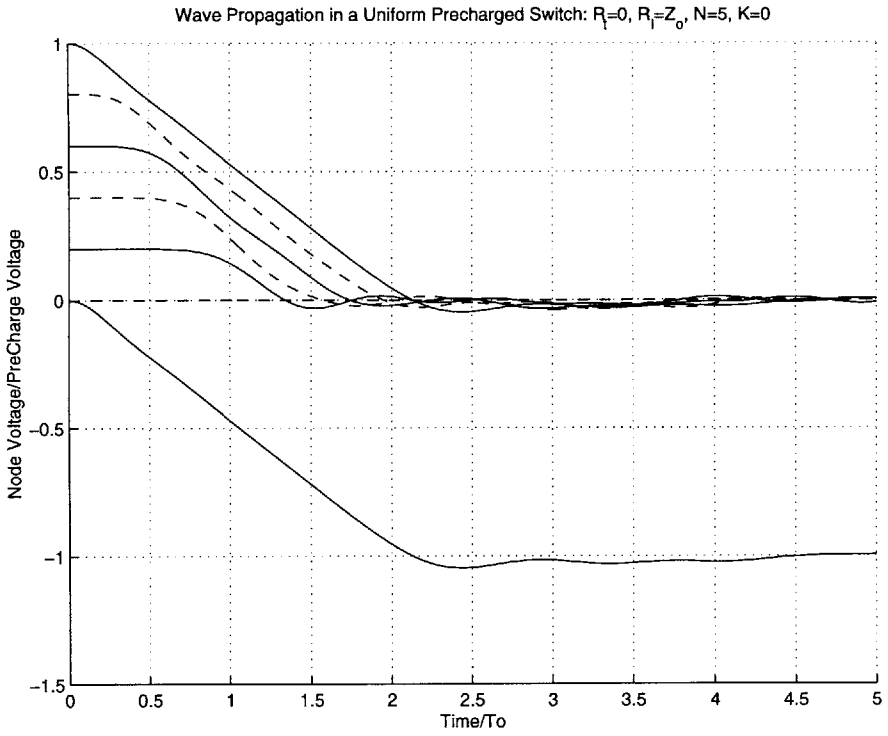


Figure 4-7: Voltages in a Uniform Precharged Switch: $R_t = 0, R_l = Z_o, N = 5, K = 0$

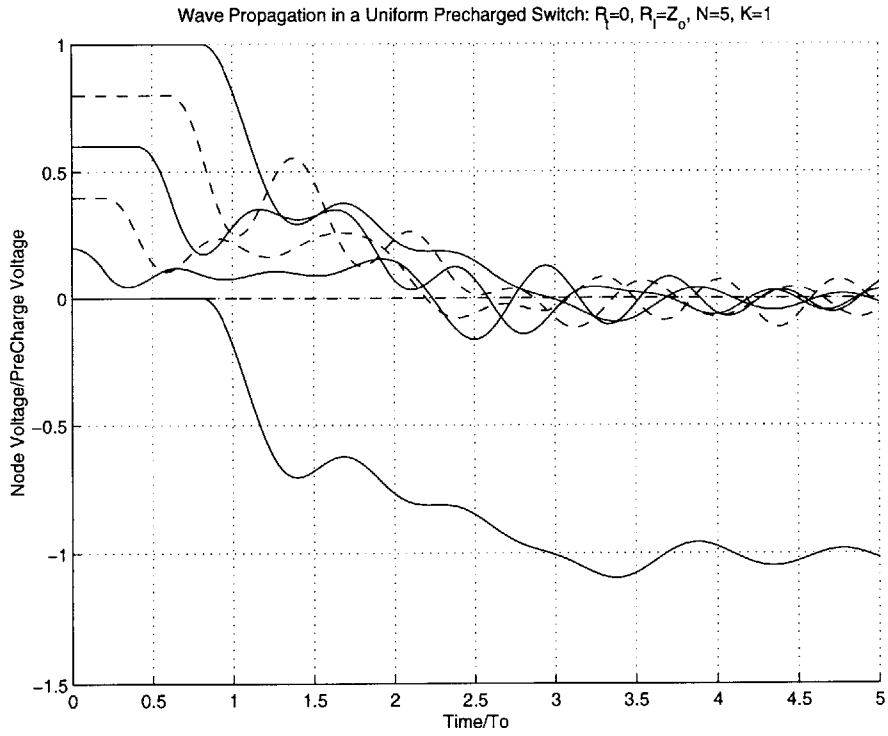
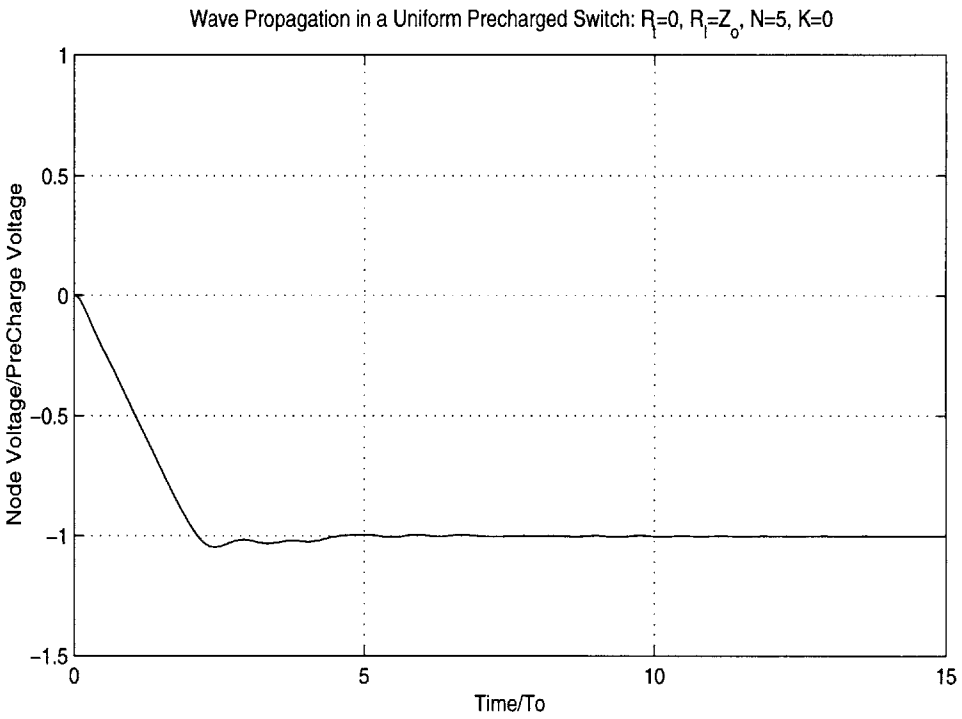


Figure 4-8: Voltages in a Uniform Precharged Switch: $R_t = 0, R_l = Z_o, N = 5, K = 1$



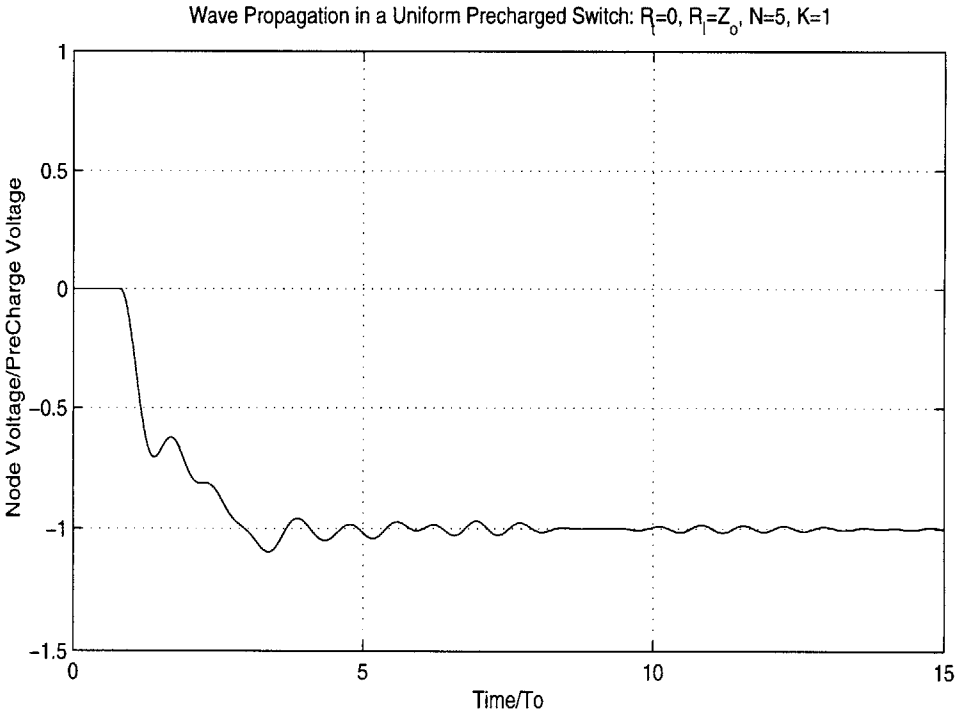


Figure 4-9: Output of Previous Switches (Extended Time Axis): $R_t = 0, R_l = Z_o, N = 5, K = 0, 1$

Tapering the Characteristic Impedance of the Line

A compromise must be made when choosing the termination resistor of a uniform precharged distributed switch; a designer must trade off greater output voltage for improved pulse fidelity, especially for nonzero values of K. It is possible, however, to recoup some of the advantages of both cases by "tapering" the characteristic impedance of the line. Tapering the line allows a designer to use a smaller termination resistor for increased voltage, and also to reduce the reflections that would be experienced if the line was uniform. Thus it is again possible to match the line at both ends. Furthermore, if the impedance of the line is tapered gradually enough, the internal reflections can be minimized as well.

The response time of a tapered precharged switch is presented here in Figures 4-10 and 4-11 to suggest the value of this impedance transformation. This particular line was tapered in a linear[2] fashion according to the following scheme:

$$R_{term} = \frac{R_{load}}{N}, \tag{4.1}$$

$$Z_o^{cell(n)} = \frac{nR_{load}}{N}, \tag{4.2}$$

$$T_o^{cell(n)} = \frac{T_o}{N}, \tag{4.3}$$

for n=1,2,3,...,N. It is clear from the response that tapering results in a higher output voltage and improved fidelity. In many respects the response is similar to the double-matched uniform line and deserves further investigation. Some additional plots of the internal stresses associated with this tapered switch are presented in Appendix C. However, an extensive analysis of tapered switched lines is saved for future study.

[2]This is by no means the only way to taper the line; previous work in tapering waveguides suggests that exponential tapering is better for minimizing internal reflections.

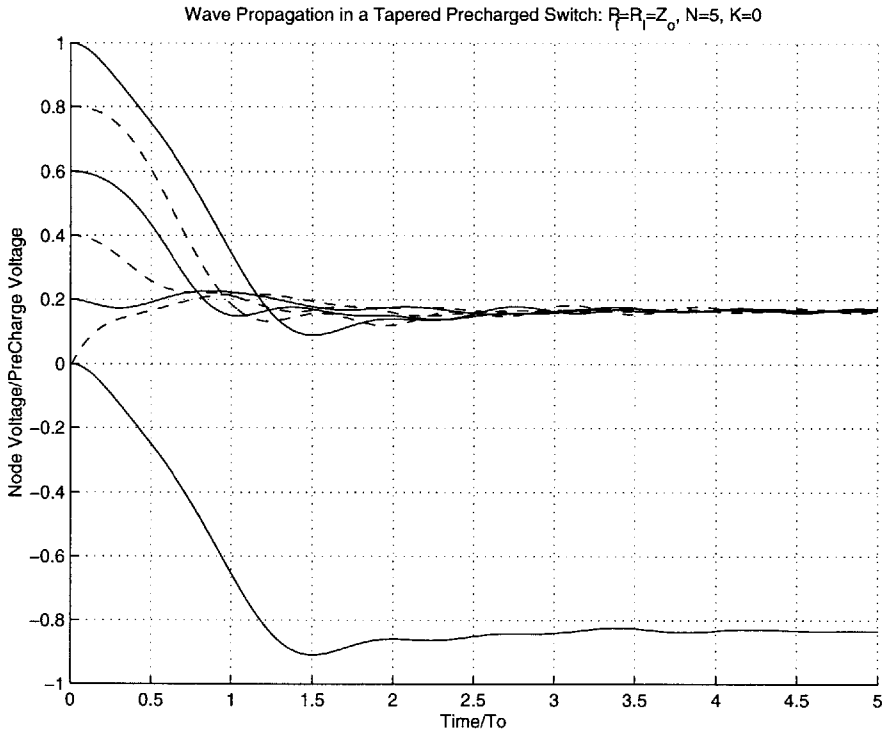


Figure 4-10: Voltages in a Tapered Precharged Switch: $5R_t = R_l = Z_o^{cell(5)}, K = 0$

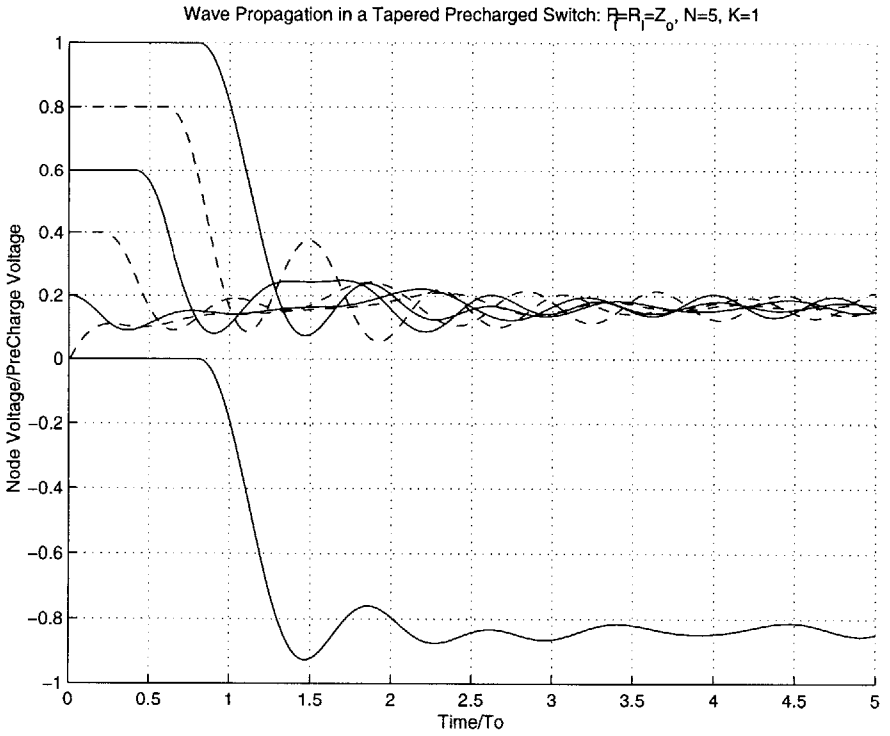


Figure 4-11: Voltages in a Tapered Precharged Switch: $5R_t = R_l = Z_o^{cell(5)}, K = 1$

4.3.3 Switch Stresses

The desire to build actual precharged switches motivates the need to understand how the FIDT scheme changes the stresses of the switching elements in a distributed system. Of specific interest is the affect of K on the voltage across each switch before switching and on the current through each switch after it is closed.

Switch Voltage

The purpose of precharging a distributed switch is to reduce the voltage each switch will tolerate when off. Staggering the switch trigger times momentarily increases the voltage across a switch before it closes. This behavior propagates up the ladder and each succeeding switch experiences a higher over-voltage than the previous one. This is referred to as the "crack-the-whip" effect[4] and is depicted by Figure 4-12 which shows how the voltages across each switch evolve with time for K=1. From a practical standpoint a certain amount of over-voltage is favorable because it can increase the

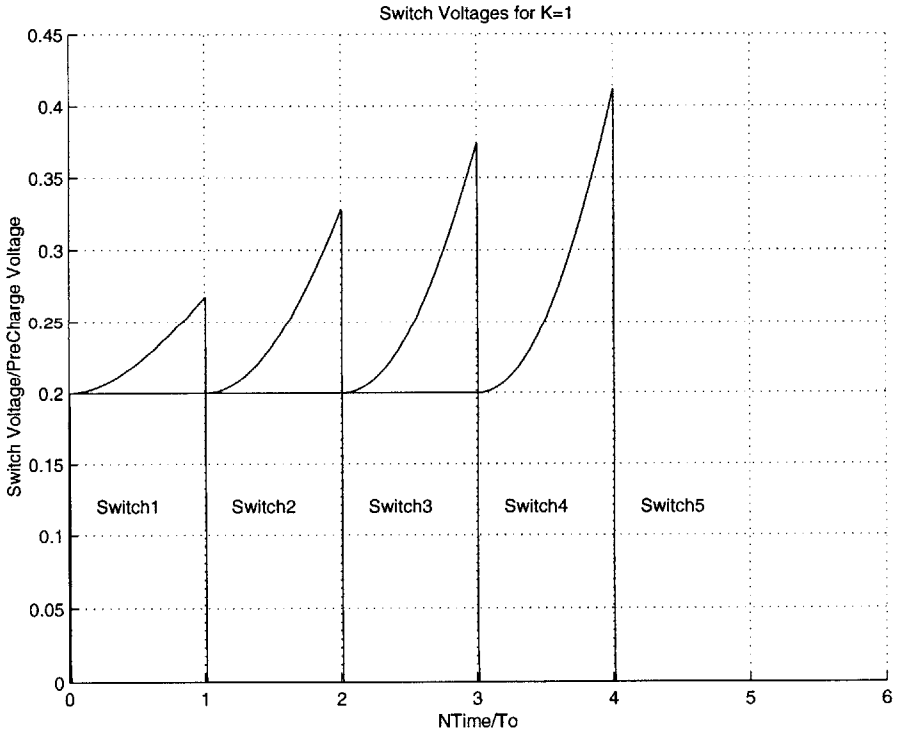


Figure 4-12: Switch Voltages for K=1

response time of a solid state switch— assuming the over-voltage is within the SOA (Safe Operating Area) of the device.

Figure 4-13 shows the maximum voltage of each switch for $0 \leq K \leq 3$. In all cases each succeeding stage sees a higher voltage than the previous stage. It is noted that for K=1, the last stage experiences close to twice the voltage of the first stage.

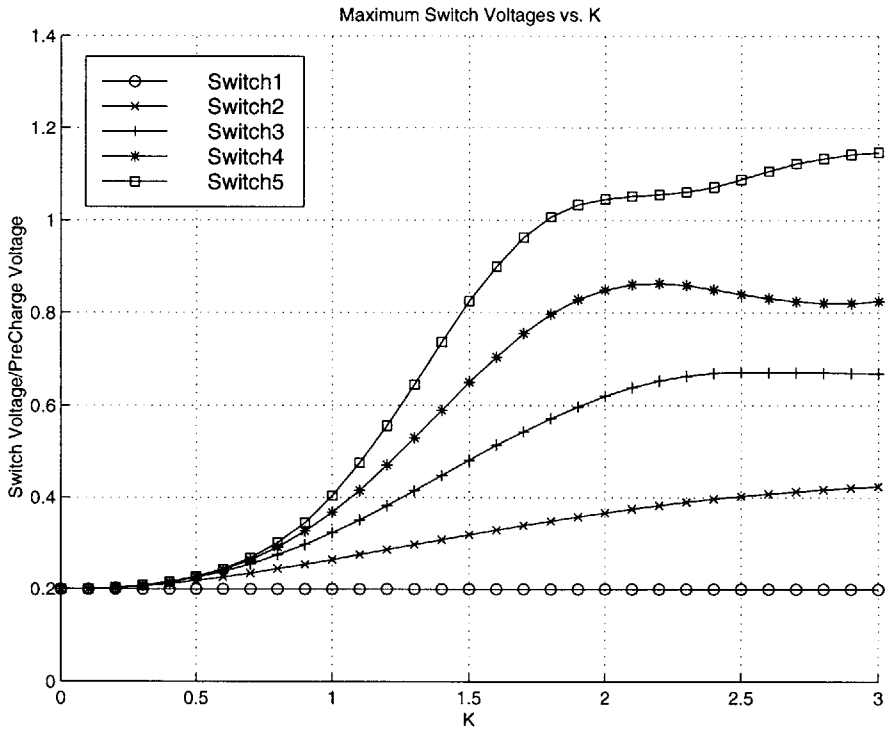


Figure 4-13: Maximum Switch Voltage vs. K

Switch Current

When designing a precharged switch it is just as important to consider the current limitations of solid state devices. Parametric sweeps of the peak positive and negative currents were conducted. As seen in Figure 4-13, a K=1 will result in a peak current through the last switch that is nearly 50% greater than the final current. Figure 4-14 suggests that like the uncharged case, the precharged switch also undergoes a mode change around K=1.5, during which current flow reverses direction. This evidence suggests that precharged switches should also be operated below K=1.

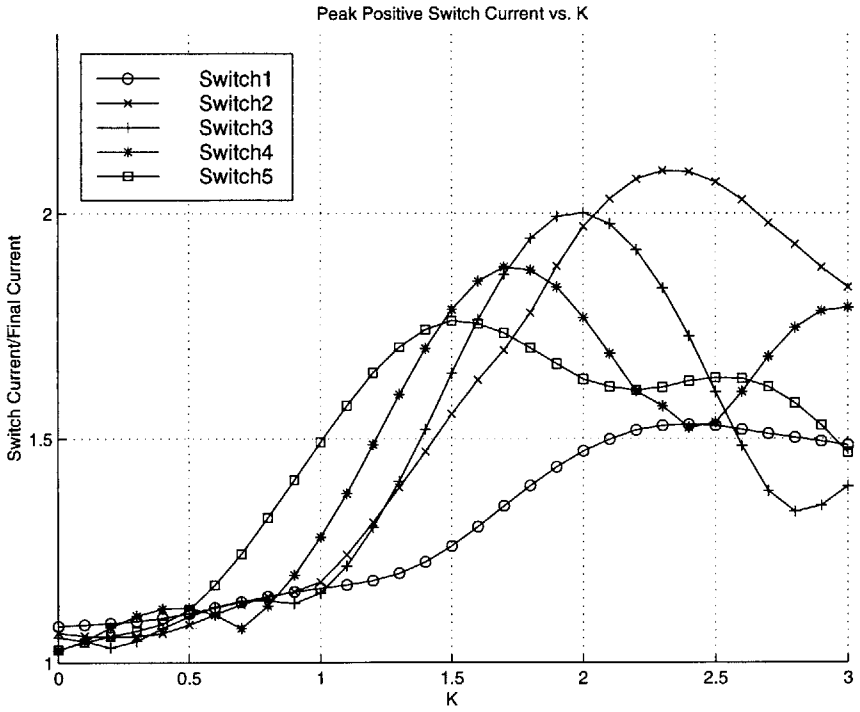


Figure 4-14: Peak Positive Switch Current vs. K

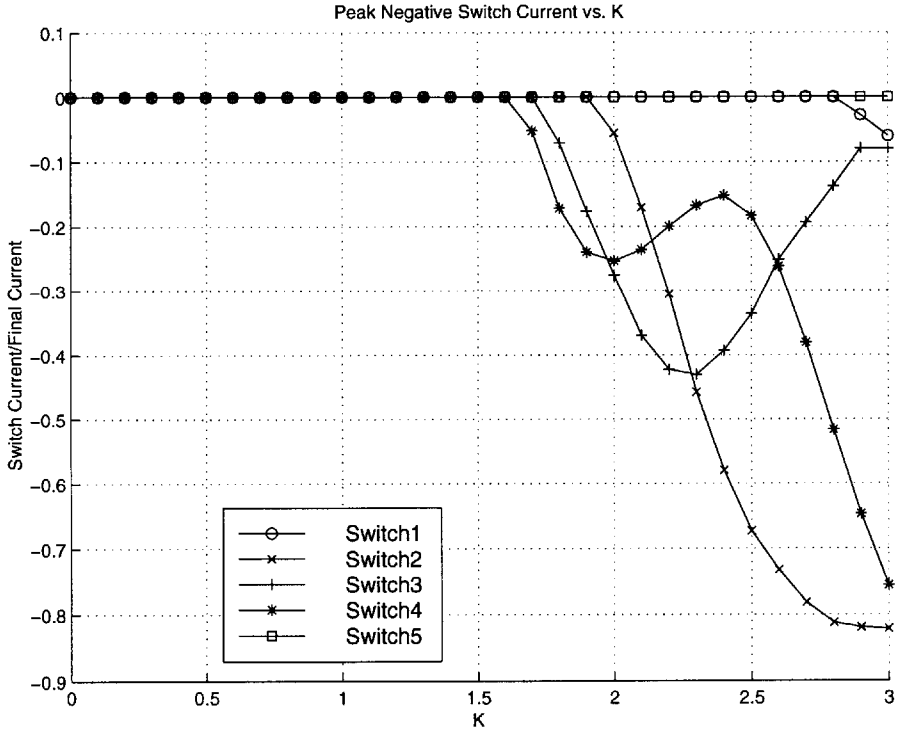


Figure 4-15: Peak Negative Switch Current vs. K

4.3.4 N-effects

The maximum voltage a precharged switch can hold off is directly related to the number of stages that make up the line. In order to meet higher voltage requirements, it is therefore important to understand how the number of stages affects the behavior of a precharged switch. Parametric sweeps for $0 \leq K \leq 1$ and $2 \leq N \leq 15$ were conducted for the precharged case to see the effect on the rise time and delay of the switch output. Results are presented using the two normalizations seen thus far.

T_o Normalization

To understand what the behavior of a precharged distributed switch converges to when infinitely resolved, it is necessary to normalize by T_o. It is clear from Figure 4-16 that higher values of K result in greater delays but also in faster rise times.

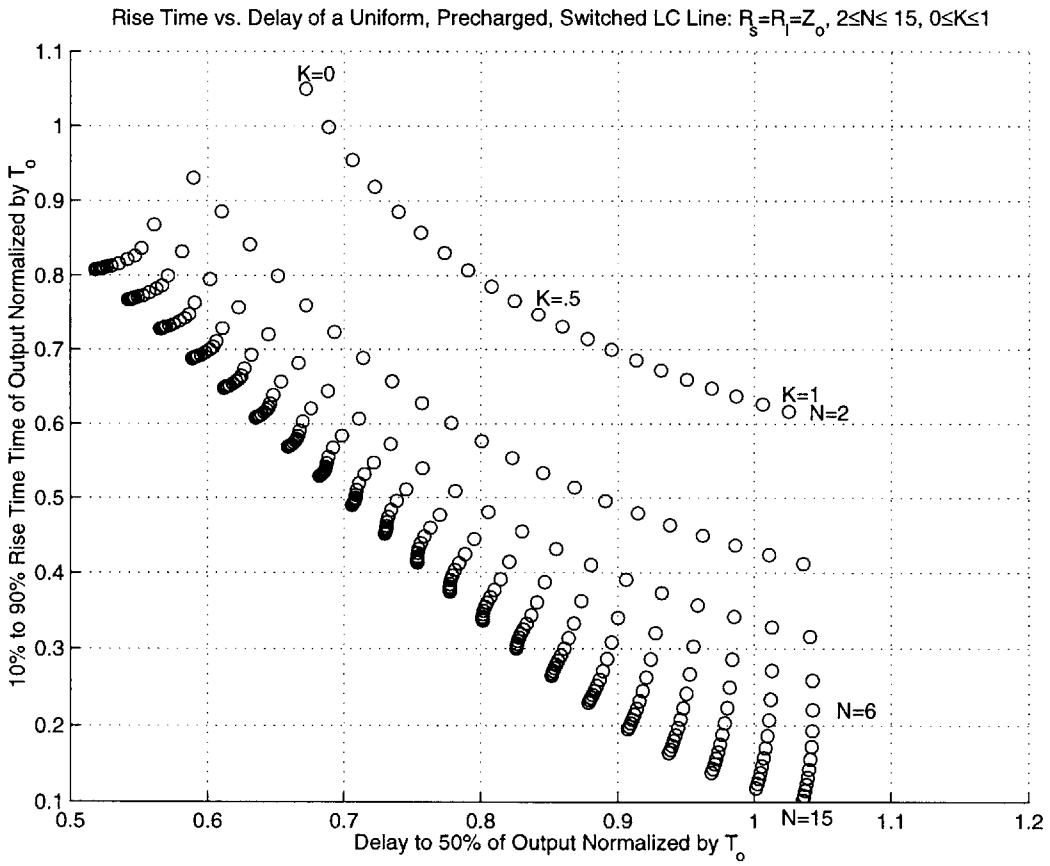


Figure 4-16: Rise Time vs. Delay of Precharged LC Line Normalized by T_o

Increasing N, however, generally produces shorter delays and faster rise times. Another interesting phenomenon is that the behavior converges faster for lower values of K. One possible explanation is that the output for larger K's has a higher frequency content than small K's, which is a reasonable hypothesis since the number of frequencies a lumped LC line models increases with N. As shall be seen, there is additional evidence to support this hypothesis.

Using the technique seen in Chapter 3, a precharged, switched transmission line model whose limiting behavior, as $N \rightarrow \infty$, is the same as the precharged, switched LC line is developed. The model is presented in Figure 4-17. It can be shown that the

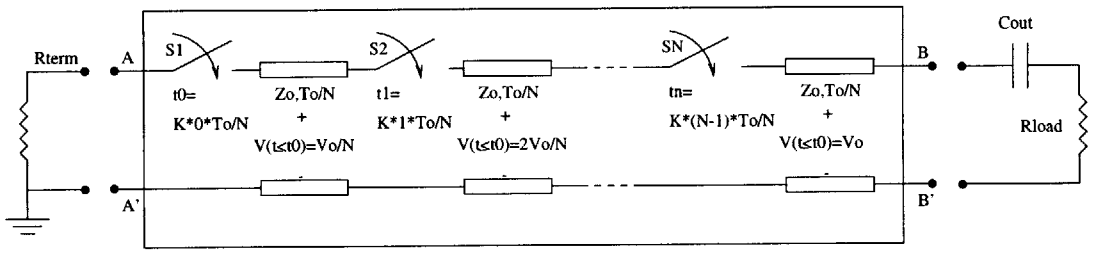


Figure 4-17: Precharged Switched, Transmission Line Model

output behavior of a precharged, switched transmission line model has two distinct modes of operation. The first mode exists for $K < 1$ and the second for $K \geq 1$. Because of the very regular output behavior of this structure it is easy to see how the output converges in the limit.

The output of the first mode resembles a descending staircase that makes as many transitions as there are stages. As N increases, the number of transitions grows, while the step size approaches zero. The limiting behavior of this process is a ramp and is shown in Figure 4-18. By inspection, it is clear from the ramp waveform that in the limit the normalized delay and rise time are given as follows:

$$\frac{DelayTo50\%(K<1)}{T_o} = \frac{(1+K)}{2}, \tag{4.4}$$

$$\frac{10\%To90\%RiseTime(K<1)}{T_o} = 0.8(1-K). \tag{4.5}$$

These equations help to confirm the limiting behavior seen in Figure 4-16. It is

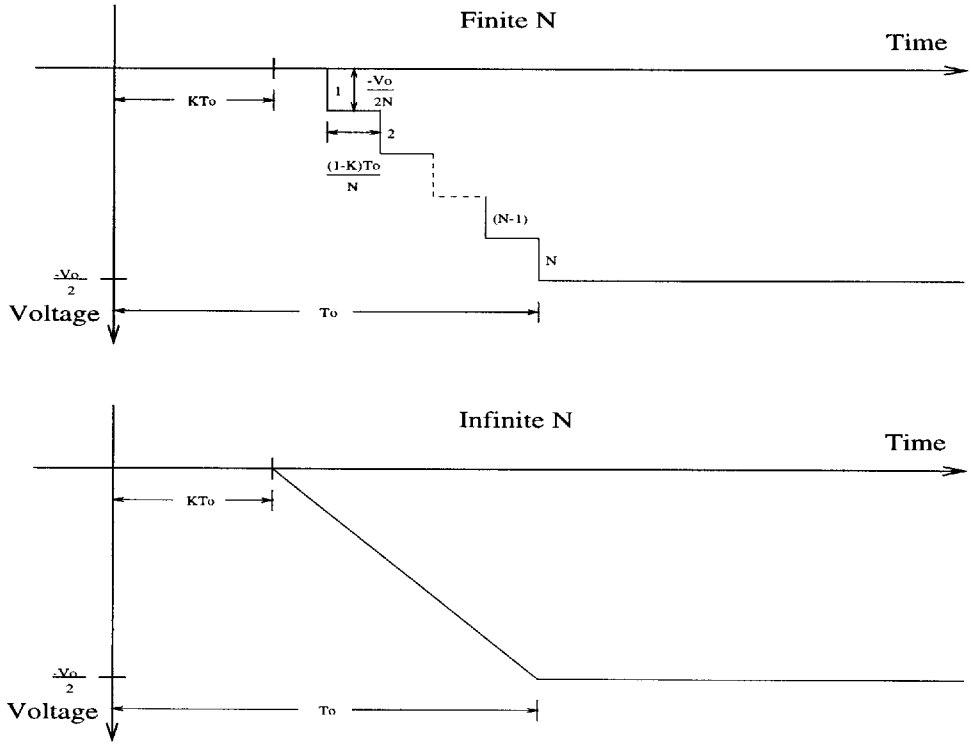


Figure 4-18: Limiting Output Behavior of a Precharged, Switched LC Line for K<1

important to note that the value K=1 causes all of the internal waves to line up, yielding a zero rise time pulse whose delay is T_o (regardless of N).

For $K \geq 1$ the output response is still a negative step because the line has had ample time to completely discharge before the output capacitor is connected. As a result, a $K \geq 1$ simply produces a greater delay at the output. This behavior is shown in Figure 4-19. For the second mode the normalized delay and rise time become

$$\frac{DelayTo50\%(K \geq 1)}{T_o} = K, \tag{4.6}$$

$$\frac{10\%To90\%RiseTime(K \leq 1)}{T_o} = 0 \tag{4.7}$$

in the limit of large N.

These results help to explain why the response for small K converges more rapidly. They support the previous hypothesis that the associated frequency content of larger K systems is higher. This is evident from the demonstrated output response, because

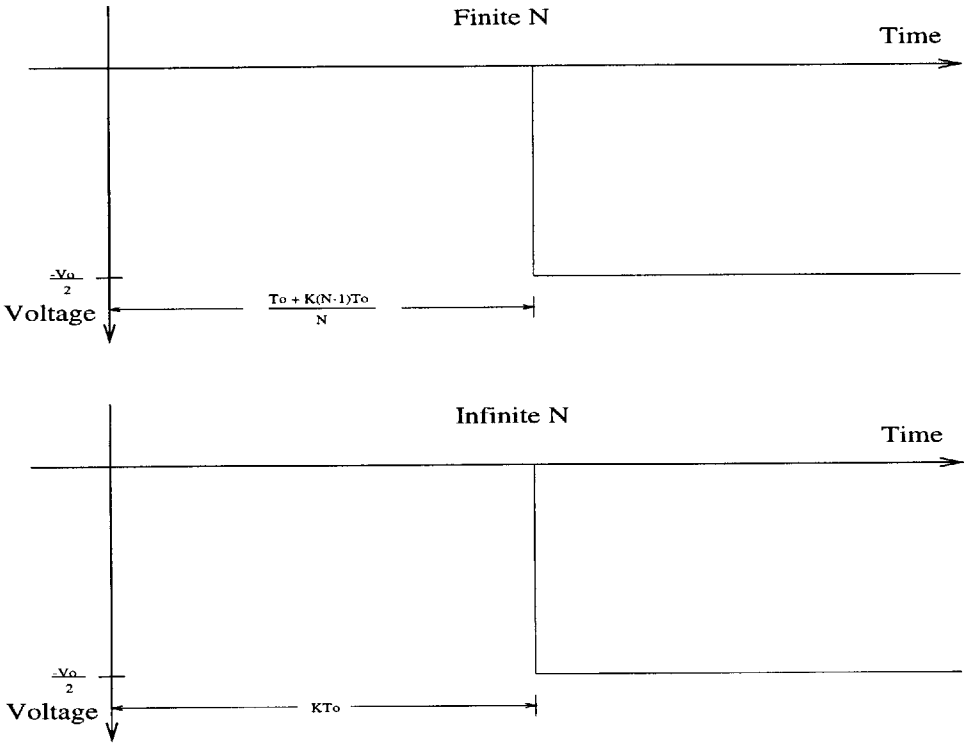


Figure 4-19: Limiting Output Behavior of a Double-Matched, Precharged, Switched LC Line for K>1

a step output clearly contains more frequency components than a ramp output.

$\frac{T_o}{N}$ Normalization

The viewpoint of increased resolution is valuable from a theoretical standpoint. However, when building physical systems emphasis is on building longer lines, since the physical inductance and capacitance associated with a switch are fixed quantities. Figure 4-20 shows how increasing the number of stages to N for various K's affects the output response. When interpreted this way a very regular pattern emerges. Again, as expected, increasing N contributes to longer delays and rise times, and increasing K's correspond to faster rise times at the expense of additional delay. However, insofar as the normalized rise time is concerned, a K=1 produces an almost constant rise time regardless of N. This means that the "effectiveness" of K on the system is increasing with N. A similar phenomena in the uncharged case was previously seen; there, it was argued that more stages implied more distributed delay and hence a

greater impact of K. This appears to hold true here as well.

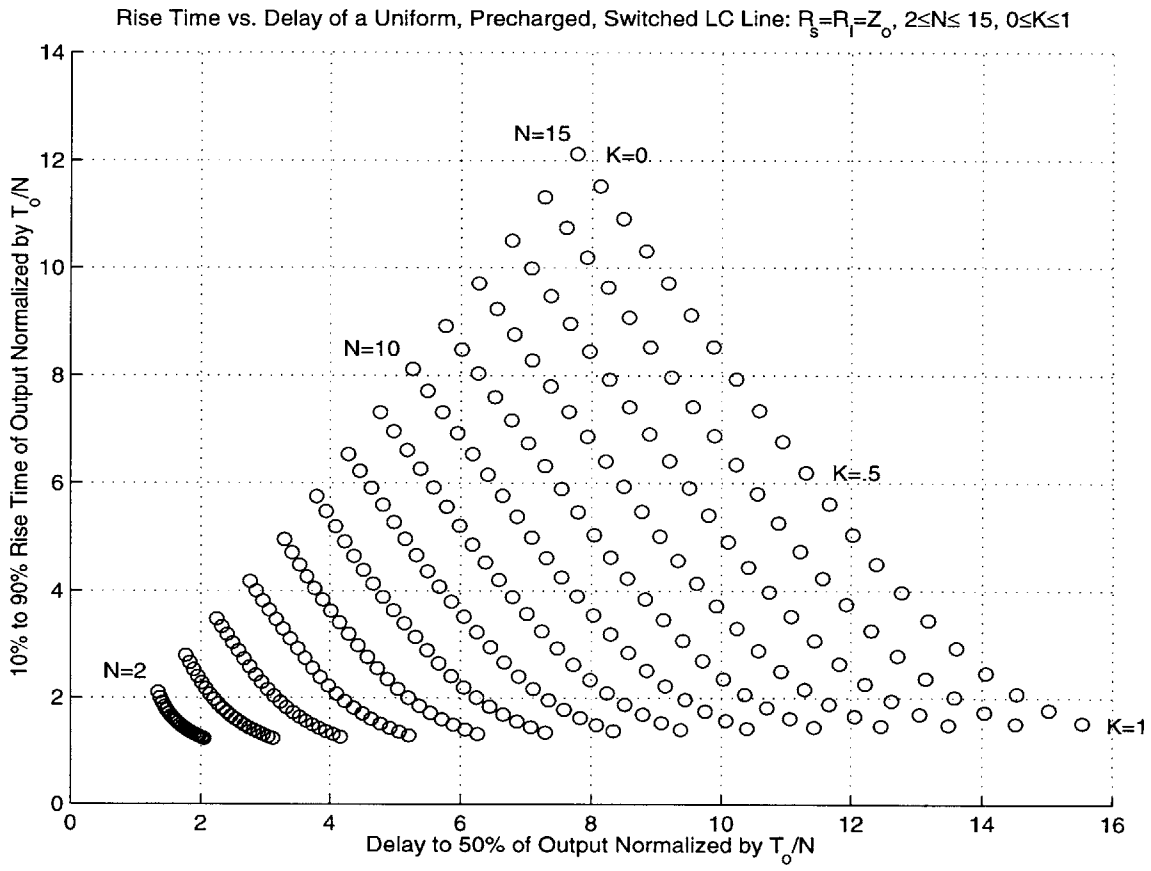


Figure 4-20: Rise Time vs. Delay of Precharged LC Line Normalized by $\frac{T_o}{N}$

4.4 A Comparison of Output Behavior

At this point, it is beneficial to examine how the behavior of the precharged models studied thus far differs from that of the uncharged models. Specifically, the overshoot and rise times as functions of K for the three, N=5, switched lines seen thus far: uncharged uniform, precharged uniform, and precharged tapered are compared.

Overshoot

Figure 4-21 shows the percent overshoot of the output voltage for the three switch lines as a function of $0 \leq K \leq 3$. Immediately, it is seen that the uncharged line has the greatest overshoot for a given K. One possible explanation for this behavior is that in the uncharged case the entire voltage wave begins propagating from the source and must work its way through all 5 stages before reaching the load. Because of the lumped nature of the line, each stage offers an opportunity for added reflections to accumulate at the output. In the precharged switch, initial voltage is already present

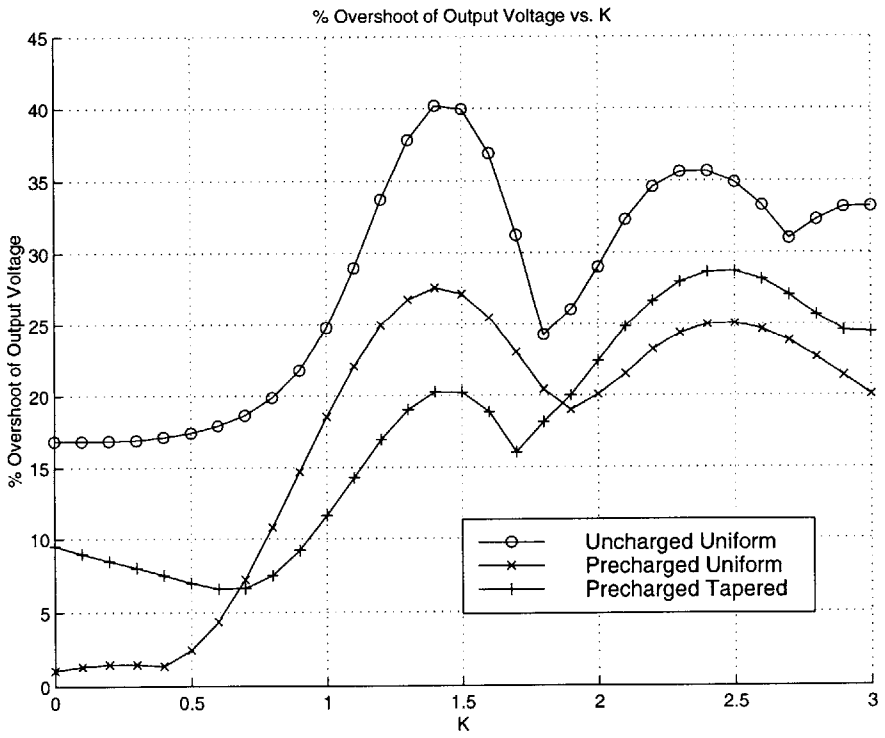


Figure 4-21: Comparison of Overshoot

in the line. Hence, less additional voltage needs to propagate through the line to fully energize it— less additional voltage means less ringing. Furthermore, about $K < 0.7$ it is found that the precharged tapered line has more overshoot than the corresponding uniform line. This is consistent with the fact that each stage here is even more dissimilar than in the uniform case, and thus more reflections are likely. However, for approximately the following range: $0.7 < K < 1.9$ the tapered line actually has less overshoot! This is partly because the tapered line is switching more voltage; hence, for a given amount of overshoot, the overshoot as a percentage appears to have decreased.

Rise Times

Figure 4-22 shows how the rise times of the three lines compare for $0 \leq K \leq 3$. From this plot it is clear that the uncharged switch is clearly the fastest for low values of K, which was expected since the precharged switches have ramp-like responses until K=1. The tapered line appears to be the slowest, but it is also switching 83% of

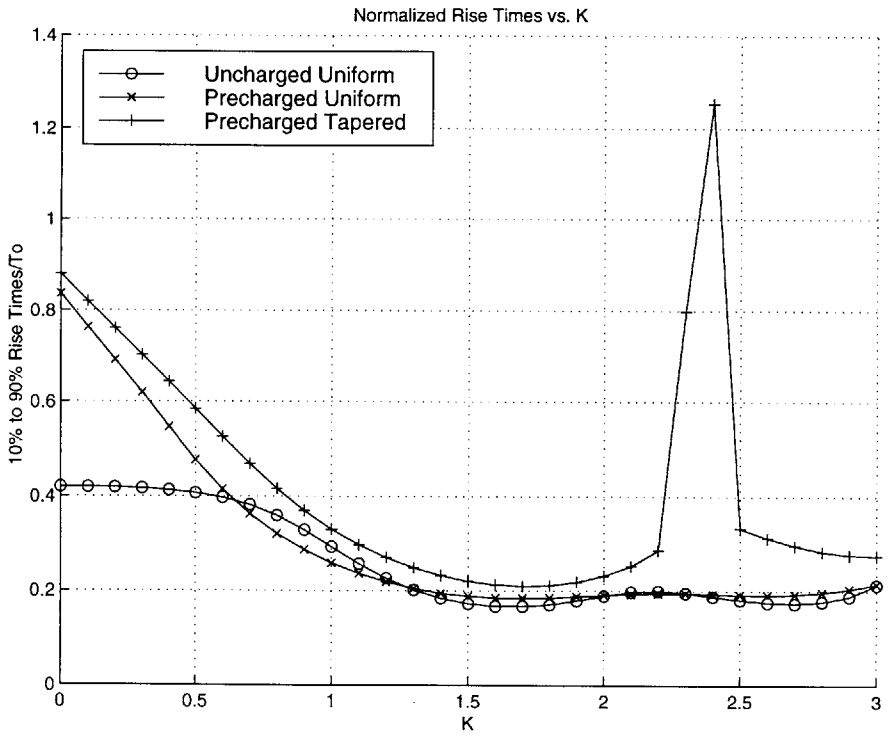


Figure 4-22: Comparison of Rise Times

the precharge voltage as opposed to only 50%. It is noted that for approximately $2.3 < K < 2.5$, the tapered switch exhibits a strange behavior that results in a very slow rise time. However, in practice a designer would probably not operate a distributed switch in this region because of the undue internal stress caused by $K > 1$.

Chapter 5

Experimental Validation of Models

5.1 Overview

In order to verify the models and simulations developed in the previous chapters, four circuits were chosen and built for the purposes of experimental validation. Tests were conducted and their corresponding time waveforms captured for comparison against simulations. The first circuit built was a five stage lumped LC ladder. The purpose of the ladder was simply to verify that wave propagation throughout the line was consistent with that seen in Chapters 2 and 3. Because the remaining three circuits were all variants on precharged switches, extensive single stage device characterization was carried out before building cascaded structures.

Next, the first of the three precharged switches was built. The first switch was designed to verify the precharged model seen in Chapter 3. Inductance and capacitance were inserted within the switch structure to represent the modeled parasitics. These "artificial parasitics" were chosen with two purposes in mind. The first purpose was to dominate the behavior of the natural parasitics in the line, thereby insuring a better correlation with the precharged model. The other purpose was to slow the response of the system to the point where the switch dynamics were considered negligible. For this reason, this switch is referred to as the "Slow Switch".

The second precharged switch was designed to verify the time scaling property of these structures. To this end, it was designed to be ten times faster, but still slow

compared to the cell switch speed. This switch is thus referred to as the "Medium Switch". For the final precharged switch, no artificial inductance and capacitance were added. Instead, this circuit relied on the pre-existing natural parasitics. This "Fast Switch" was built mainly for gathering experimental information, since the switch dynamics were no longer negligible and no modeling of finite switch commutation was done.

5.2 Design and Implementation

Design and implementation of the four test circuits is discussed here. Special attention in this section is paid to component selection, triggering schemes and other practical issues.

5.2.1 Hardwired LC Line

Construction of the LC Ladder shown in Figure 5-1 was straightforward and involved only passive components. The rest of the network was completed by the addition of a 47Ω load resistor and a 50Ω square wave generator.

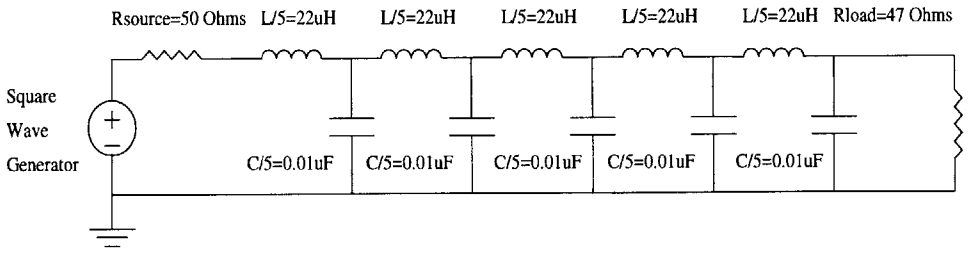


Figure 5-1: Fixed LC Line Schematic

Artificial L and C Selection

The selection of standard inductors and capacitors was facilitated by plots of Z_o and $\frac{T_o}{N}$ as functions of L and C. These selections curves are in Appendix D. Component selection was subject to the following criteria:

1. A characteristic impedance close to 50Ω

2. A cell delay much greater than 10ns

Because many circuit applications are required to drive a 50Ω load, a similar characteristic impedance was desired. The requirement on the cell delay allowed these values to be used for the future slow switch as well. Essentially, a $\frac{T_o}{5}$ much slower than the switching speed of a typical solid state device was required. These constraints yielded the values in Table 5.1.

Table 5.1: Hardwired LC Line Component Values

	L/5	C/5	Z_o	$T_o/5$
Hardwired LC Line	22μH	0.01μF	47Ω	469ns

5.2.2 Precharged Distributed Switches

The construction of a precharged switch is more complex than the previously seen LC ladder, since the ladder forms only a portion of the switching network. A general schematic for the three distributed precharged switches is shown in Figure 5-2.

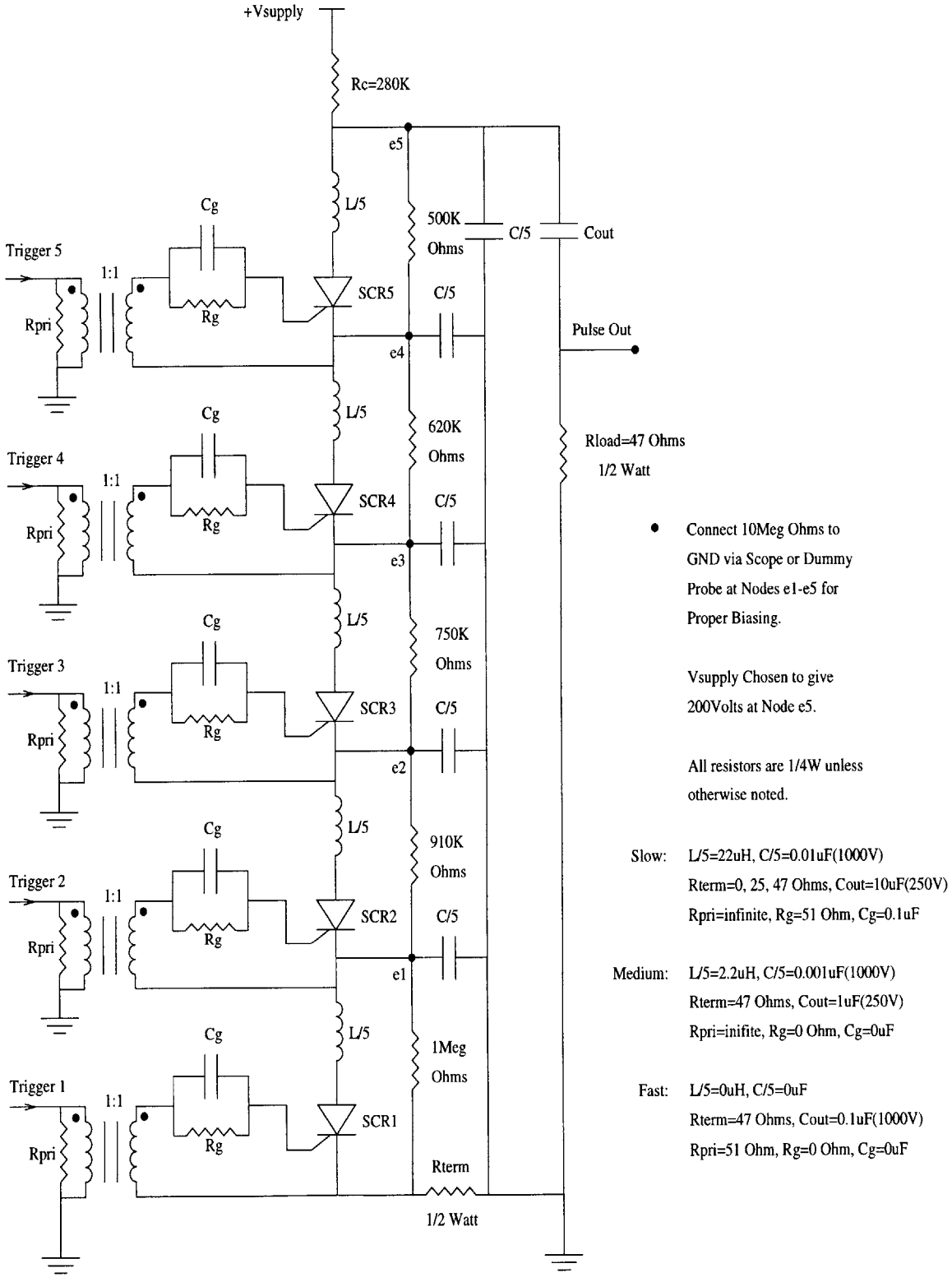


Figure 5-2: Precharged Switch Schematic

Artificial L and C Selection

The L and C values chosen for the hardwired line also form the backbone of the slow precharged switch. The values for the medium precharged switch were picked to give cell delays an order of magnitude faster than those in the corresponding slow switch. The fast switch did not require additional inductance or capacitance, and simply used the natural parasitics inherent in the circuit. These values and their corresponding properties are summarized in Table 5.2.

Table 5.2: Precharged Switch L and C Values

	L/5	C/5	Z_o	$T_o/5$
Slow Switch	22μH	0.01μF	47Ω	469ns
Medium Switch	2.2μH	0.001μF	47Ω	46.9ns
Fast Switch	N/A	N/A	N/A	N/A

Solid State Switches

Silicon Controlled Rectifiers were selected to implement the individual switch cells of the three precharged distributed switches. SCR's have relatively low power requirements for triggering, and their self commutating properties make them well suited to these circuits. The thyristor switch chosen was Microsemi's GA301A. The GA301A is a commercial thyristor capable of switching 1A in less than 10ns. The actual rise time of the switch depends on many factors including, but not limited to the following: drive circuitry, the precharge voltage and the amount of current to be switched. See Appendix F for additional information from Microsemi Corporation on these devices.

Biasing Network

The biasing network serves to ensure that the precharge voltage is equally distributed across each thyristor prior to switching[1]. This network is usually a resistor ladder

[1] Without this network, unequal leakage currents might cause poor voltage sharing.

whose total resistance is designed to be large enough to minimize static power consumption, and to prevent possible interference with the rest of the switching network. Ordinarily, voltage sharing is accomplished by making each resistor in the ladder of equal value; a typical value is 1MΩ. Unfortunately, the need to measure voltages at nodes formed by the biasing network with the LC ladder presents a problem. Because the impedance of typical oscilloscope probes is 10MΩ, a loading effect occurs when a probe is connected to the bias network. This is because the bias network can be on the order of the probe impedance, or even higher, if enough stages are used.

To insure that voltage measurements could be made without changing the intended bias voltages, the network was designed to work with the added 10MΩ impedance of the scope probes. This lead to the following general network problem shown in Figure 5-3. Essentially, each R_n must be picked to equally divide the total voltage across the ladder when each node in the ladder has a fixed R_{probe} shunt to ground.

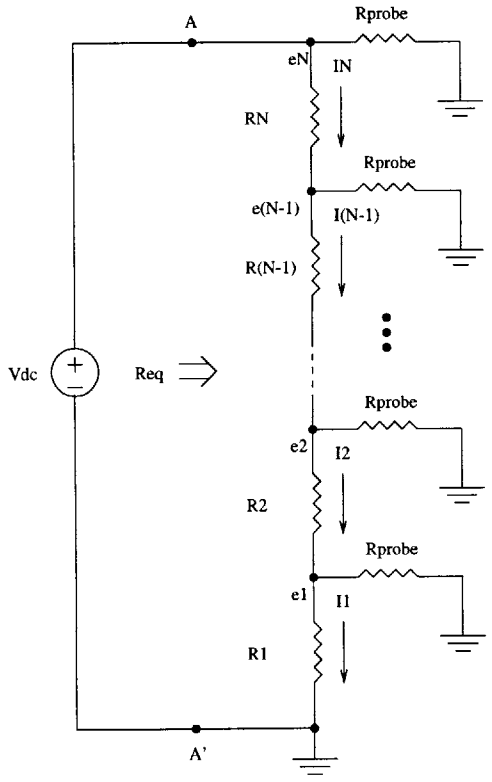


Figure 5-3: Biasing Network

The general solution for obtaining the correct resistor values is given by the following recurrence relationships.

$$R_n = \frac{e_n}{NI_n} \tag{5.1}$$

for n=1,2,3,...N, which is simply a statement of equal voltage sharing.

$$I_{n-1} = I_n - \frac{[e_n - \frac{e_n}{N}]}{R_{probe}}, \tag{5.2}$$

which follows from (5.1) and KCL.

$$I_N = e_N[\frac{1}{R_{eq}} - \frac{1}{R_{probe}}], \tag{5.3}$$

which calculates the current through R_N based on a desired equivalent resistance, R_{eq}, looking into the A-A' port. Once this current is constrained all of the other currents and resistors can be calculated iteratively starting with R_N and ending with R_1. It is important to note, that this analysis was carried out with the explicit assumption that the termination resistance R_{term} was negligible when compared to R_1. Fortunately, this is often the case.

It should be clear from (5.3) that the equivalent resistance looking into port A-A' cannot be larger than 10MΩ. It was found that for N=5, choosing R_{eq}=2MΩ resulted in close to standard resistor values. Table 5.3 lists the desired values as well as the closest standard value. Individual resistors were then hand picked to get values as close to the desired values as possible. Voltage sharing within 5% was accomplished.

Table 5.3: Bias Resistors

	R_1	R_2	R_3	R_4	R_5
Desired	500KΩ	625KΩ	769KΩ	909KΩ	1MΩ
Standard	500KΩ	620KΩ	750KΩ	910KΩ	1MΩ

R_c Selection

R_c serves as a bleed resistor for charging C_{out} and the LC network prior to switching. In addition, R_c must be large enough to limit the DC switch current below the minimum "holding current" of the thyristors, which allows them to recover their voltage blocking capability between pulses. The typical holding current for a GA301A is 2mA, but it can be as low as 0.3mA at room temperature. Since R_c forms a voltage divider with the biasing network, choosing R_c=280KΩ implies a V_{supply}=228 Volts (in order to charge C_{out} to 200 Volts). For these values, the DC current was limited to 0.8mA; this was sufficient to guarantee reverse blocking.

C_{out} Selection

In all PSPICE simulations, C_{out} was chosen large enough to make any droop at the output unnoticeable for the time scales of interest. In a physical system, this is not feasible, since a sizeable capacitor can take a significant amount of time to charge up. Consequently, C_{out} was chosen to limit the droop to no more than 5% for a $10T_o$ pulse length. Using this criteria and the exponential decay for a first order response gives the following inequality,

$$0.95 < e^{-\frac{10T_o}{\tau_{discharge}}}. \tag{5.4}$$

Solving for the lower limit on $\tau_{discharge}$ yields

$$\tau_{discharge} > \frac{10T_o}{-\ln(0.95)}. \tag{5.5}$$

Since,

$$\tau_{discharge} = (R_{load} + R_{term})C_{out}, \tag{5.6}$$

the lower limit on the output capacitor must be

$$C_{out} > \frac{10T_o}{-\ln(0.95)(R_{load} + R_{term})}. \tag{5.7}$$

Because some experiments call for values of R_{term} that are smaller than R_{load}, a conservative estimate of the droop was calculated with a worst case R_{term}=0. The values for the various C_{out}'s and their corresponding droop for a $10T_o$ pulse are summarized in Table 5.4.

Table 5.4: C_{out} and Corresponding Droop Assuming Worst Case R_{term}=0

	R_{load}	C_{out}	$\tau_{discharge}$	$10T_o$	Droop at $10T_o$
Slow Switch	47Ω	10.0μF	470μS	23.45μS	4.86%
Medium Switch	47Ω	1.0μF	47μS	2.345μS	4.86%
Fast Switch	47Ω	0.1μF	4.7μS	N/A	N/A

Repetition Rate

The maximum repetition rate of these pulse circuits can be limited by one of two factors: the rate at which the output capacitor, C_{out}, can be charged and discharged or the maximum power dissipation in the load, R_{load}. The time constant associated with the rate of charging or discharging is determined by the appropriate resistors and the output capacitor, or

$$\tau_{charge} = (R_c + R_{load})C_{out} \tag{5.8}$$

and

$$\tau_{discharge} = R_{load}C_{out}. \tag{5.9}$$

The actual charging and discharging time is approximately five of the corresponding time constants or

$$ChargeTime \approx 5\tau_{charge} \tag{5.10}$$

and

$$DischargeTime \approx 5\tau_{discharge}. \tag{5.11}$$

According to these constraints, the cycling period must be at least

$$T_{min} = ChargeTime + DischargeTime. \tag{5.12}$$

This corresponds to a maximum repetition rate of

$$f_{max} = \frac{1}{5(R_c + 2R_{load})C_{out}}. \tag{5.13}$$

If $R_c \gg R_{load}$, as is the case here, the following simplification can be made:

$$f_{max} \approx \frac{1}{5R_cC_{out}}. \tag{5.14}$$

Once f_{max} is determined, the power dissipation should be checked to ensure that it is not a limiting factor, especially if the the pulse voltage is high. A conservative estimate of the average power delivered to the load is to assume that all of the energy stored in C_{out} is delivered when the capacitor is discharged[2]. This leads to the following equation for the maximum average power delivered,

$$Max\langle P_{load}\rangle = \frac{C_{out}V^2_{precharge}f_{max}}{2}. \tag{5.15}$$

Again, this equation assumes a worst case scenario of R_{term}=0. The maximum repetition rate and the corresponding maximum average power consumed by the load for the three switches are summarized in Table 5.5. From the table it is evident that the size of the output capacitor and bleed resistor have resulted in a very slow repetition

Table 5.5: Maximum Repetition Rate, f_{max}, Assuming a Worst Case R_{term}=0

	f_{max}	T_{min}	$Max\langle P_{load}\rangle$
Slow Switch	0.07Hz	14s	14.3mW
Medium Switch	0.7Hz	1.4s	14.3mW
Fast Switch	7Hz	.14s	14.3mW

[2]Energy is also consumed during the charging portion of the cycle, but is negligible given the size of R_c in relation to R_{load}.

rate. The power delivered to the load is also well within the tolerance for a half watt resistor.

Isolation of Triggering Circuitry from High Voltage Switch

High voltage switches of this sort present a problem when trying to interface with the thyristor's triggering circuitry. The problem arises because often the thyristor's cathode is floating with respect to ground. As a result, these gate drives require some form of galvanic isolation to separate the trigger circuit's ground from the thyristor's cathode. This isolation is often accomplished with optocouplers or pulse transformers. Because optocouplers are slow, pulse transformers were chosen for trigger signal coupling.

The PE-64973 pulse transformer from Pulse A Technitrol Company was selected for this application. The PE-64973 is a 1:1 transformer with low leakage inductance and fast rise time capability. It is also capable of providing $1500V_{rms}$ isolation which is more than adequate for the constructed high voltage switches. More information on the PE-64973 is available from Pulse in Appendix F. In addition, Appendix G contains the results of experimental tests that help to characterize this pulse transformer's performance when used in conjunction with the triggering circuits in these experiments.

Triggering Schemes

The ability to vary the amount of fixed inter-switch delay in a distributed switch requires that some flexibility be designed into the triggering circuit. This was accomplished through two different triggering schemes. The first scheme, a TTL circuit, was applied to the slow and medium switches and takes advantage of the slower time scales of these circuits. The TTL triggering circuit uses an external, variable clock to synchronize the delays of five different trigger signals. Schematics and timing diagrams of this circuit are available in Appendix E. For the fast switch, digital control was not an option because of the extremely small delays required. Instead, fixed inter-switch delays were accomplished by using varying lengths of RG-178 coaxial

cable[3].

As mentioned previously, the speed at which a thyristor can commutate is partially dependent on its drive circuitry. To understand how the drive circuit impacts the device's speed, single stage device characterization for various triggering schemes was conducted. These results are available in Appendix H. In general, device speeds of approximately 10ns were achieved for a preswitched anode-to-cathode voltage of 40 Volts.

5.3 Experiment I: Fixed LC Line

The first experiment was designed to show the step response of a five stage LC ladder. The ladder network was driven by a low frequency square wave, and the node voltages along the ladder were recorded using the setup shown in Figure 5-4.

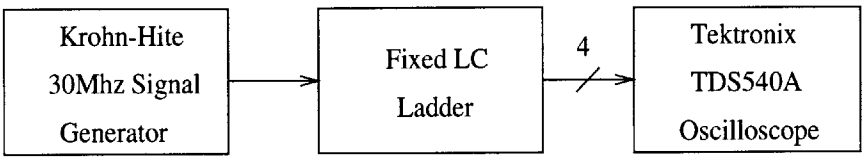


Figure 5-4: Test Setup for Experiment I: Fixed LC Line

5.3.1 Captured Waveforms

The captured waveforms for the step response of the LC ladder network are shown in Figure 5-5. In general the waveforms appear consistent with the simulations performed in Chapter 2. The most striking difference is evident after the transient behavior has decayed; the individual node voltages settle to different values, instead of to half the supply voltage as expected. This is explained by a lack of resistive loss in the simulations. Because R_{load} and R_{source} are close to 50Ω, it only takes about 1-2Ω of resistance in each inductor to be noticeable. Because the inductors look like "shorts" in the steady state of the step response, only their resistance is seen. Thus,

[3]The propagation delay of this cable is very close to 5ns per meter.

a resistor ladder is formed and the behavior associated with one is evident after the transients have decayed.

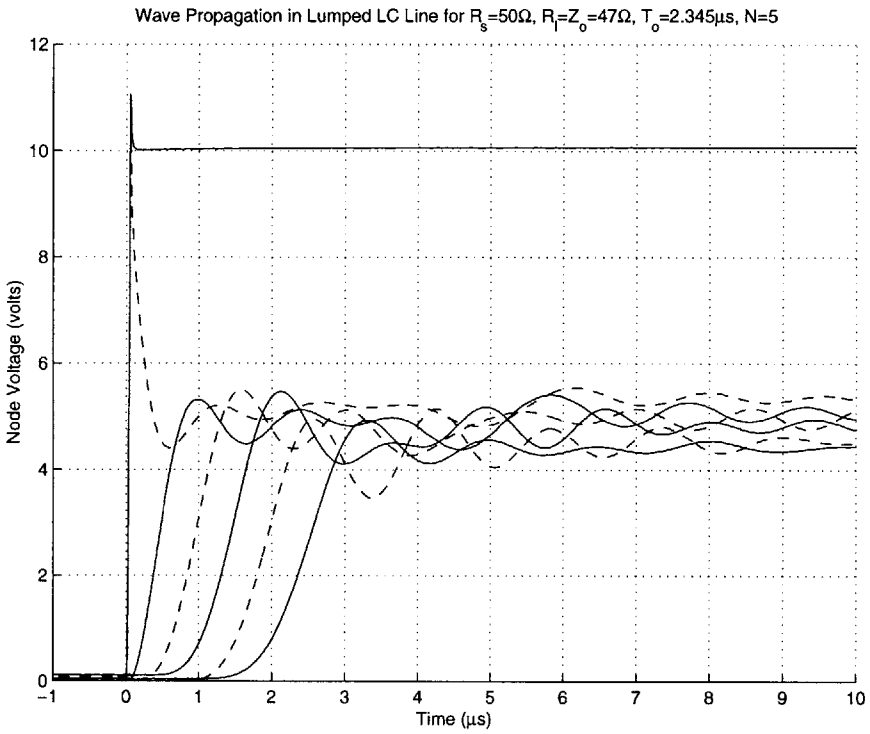


Figure 5-5: Captured Waveforms: Hardwired LC Line

5.3.2 Actual Output vs. Simulated Output

The captured output from the LC ladder was plotted against its corresponding simulation in Figure 5-6. By comparison, it is clear that the experimental output is slightly more damped than the simulation. The lack of resistance in the simulation is another explanation. In addition, the measured output appears to be slightly compressed when compared to the simulation. Because the inductors and capacitors used are typically accurate within 10%, it is possible for the "nominal" value of T_o to vary accordingly. If the nominal T_o of 2.345μs is adjusted to 2.22μs, a difference of about 5.3%, a better fit is ascertained.

Nominal T_o

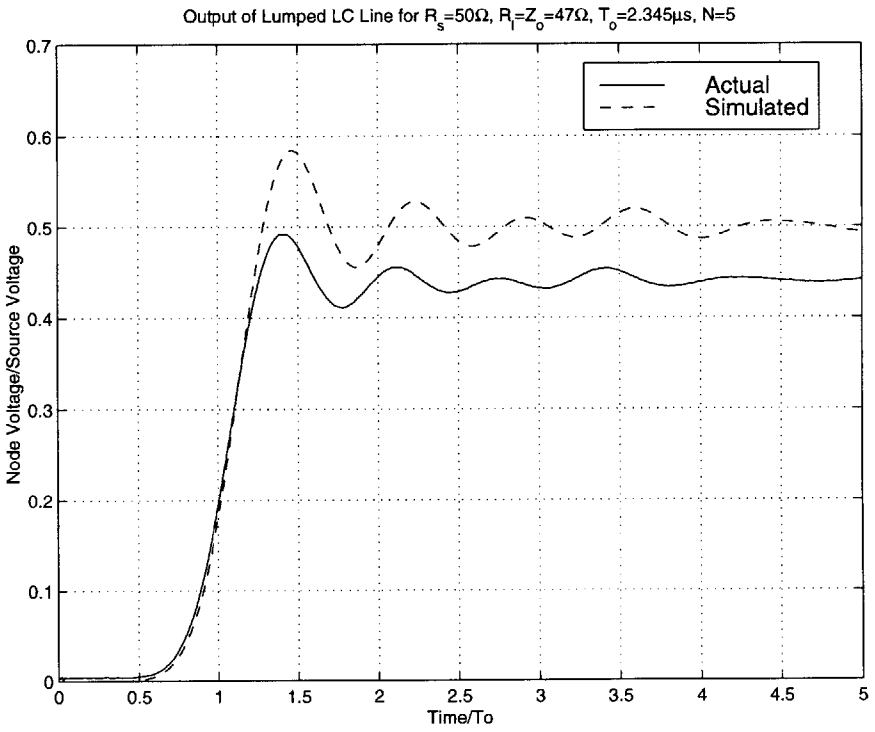


Figure 5-6: Hardwired LC Line: Actual vs. Simulation for Nominal T_o

Adjusted T_o

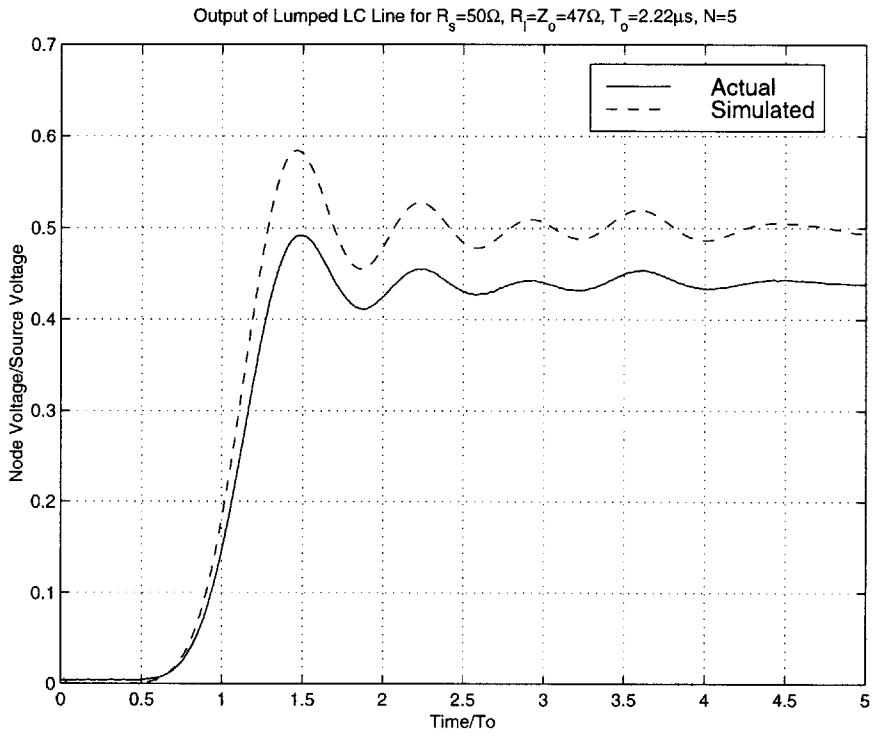


Figure 5-7: Hardwired LC Line: Actual vs. Simulation for Adjusted T_o

5.4 Experiment II: Slow Precharged Switch

The second experiment demonstrates various behavioral aspects of a precharged switch. The response of the system for K=0,.75 and 1 was investigated for the double-matched case. In addition, some experiments with R_{term} mismatching, R_{term}=0Ω and 25Ω for K=0 and 1, were also conducted. This experiment was carried out using the setup in Figure 5-8. A variable 240 Volt power supply was used to precharge the switch to 200 Volts. The slow switch received its trigger signals from a separate TTL circuit. The exact value of K was controlled by a variable 30Mhz Krohn-Hite signal generator that provided a clock signal to synchronize the delays of the TTL circuitry.

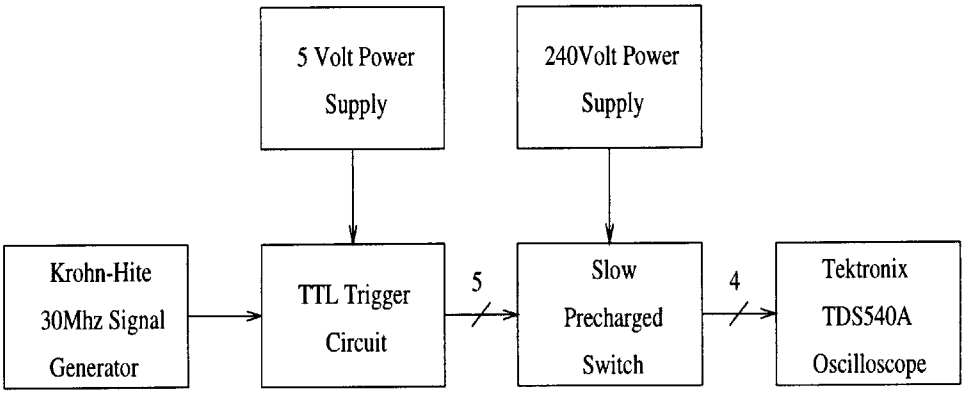


Figure 5-8: Test Setup for Experiment II: Slow Precharged Switch

5.4.1 Captured Waveforms

The captured waveforms for the various slow switch experiments are shown in the upcoming Figures. Figures 5-9 through 5-11 show the results of the double-matched switch for increasing values of K. Figures 5-12 to 5-15 are the waveforms for the various mismatched cases studied. Again, the waveforms presented are consistent with the models presented in Chapter 4. As per the fixed LC line experiment, the resistance in the inductors is noticeable again in the steady state.

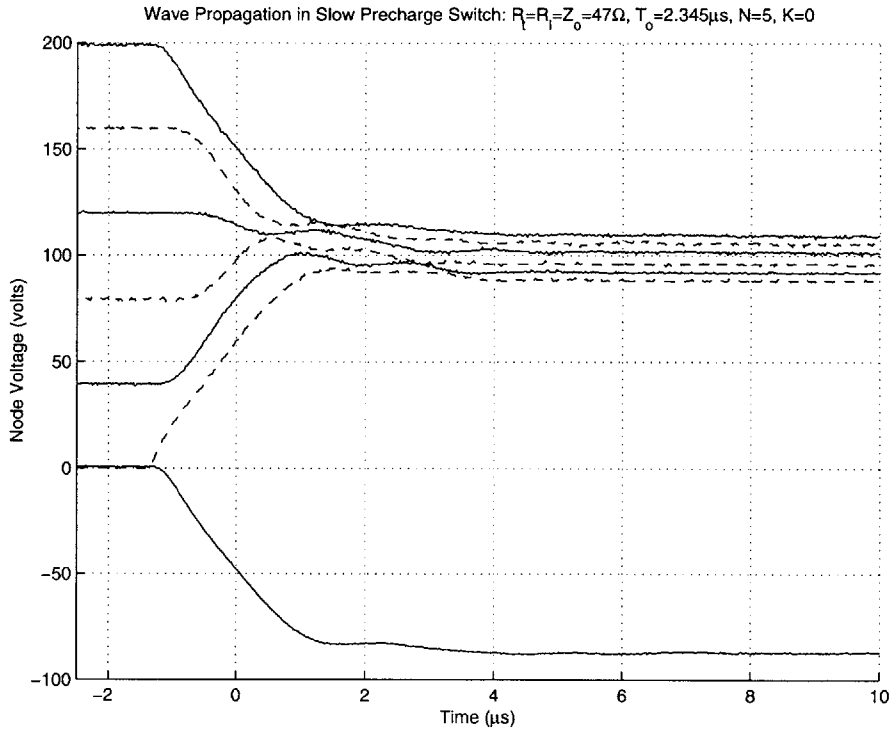


Figure 5-9: Captured Waveforms: Slow Switch, $R_t = R_l = 47\Omega$, K=0

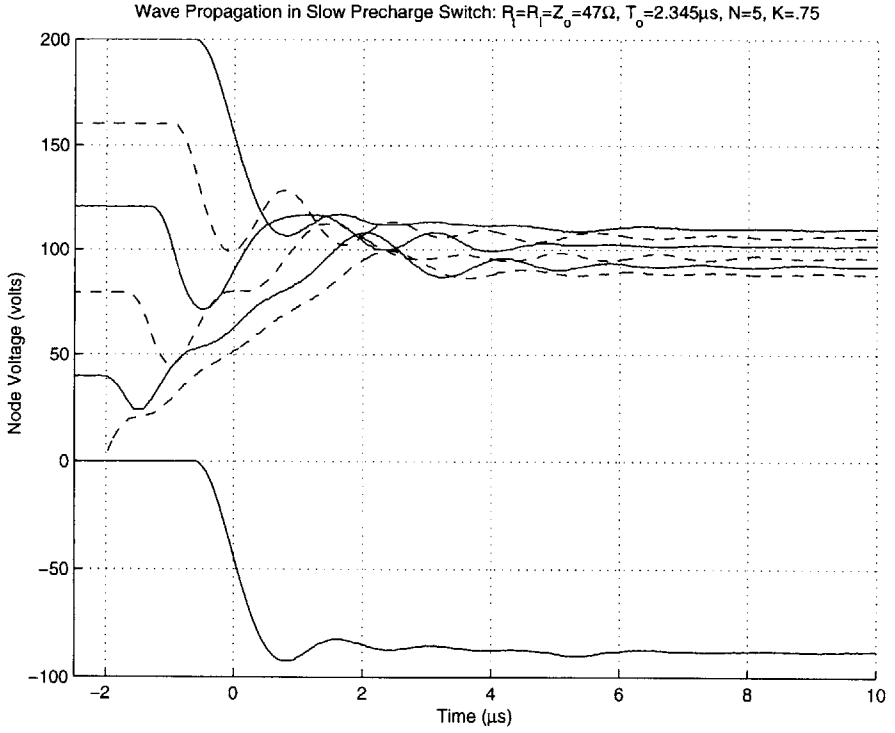


Figure 5-10: Captured Waveforms: Slow Switch, $R_t = R_l = 47\Omega$, K=.75

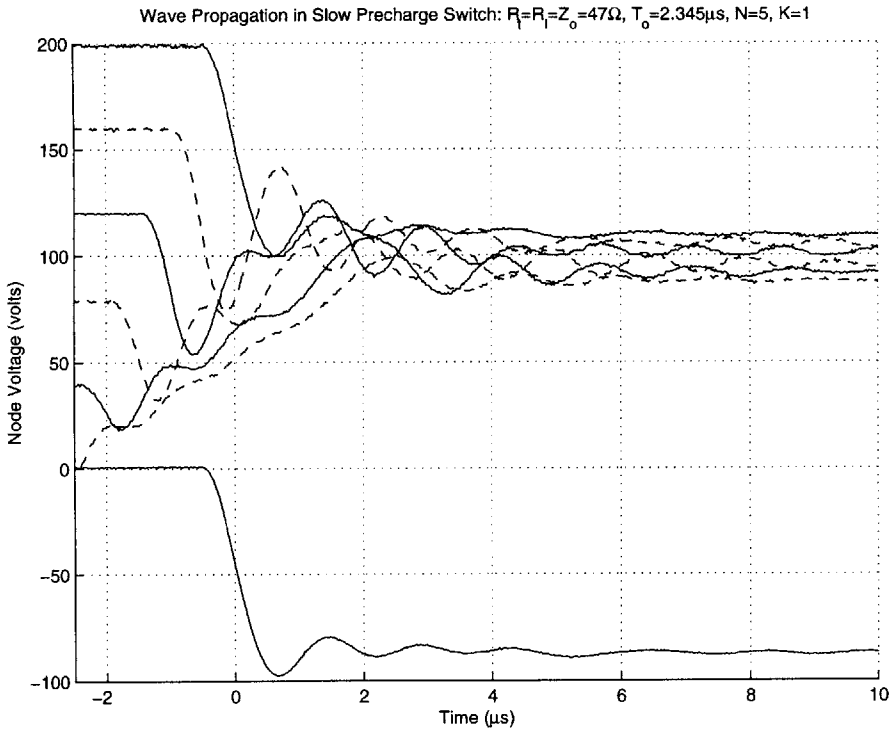


Figure 5-11: Captured Waveforms: Slow Switch, $R_t = R_l = 47\Omega$, K=1

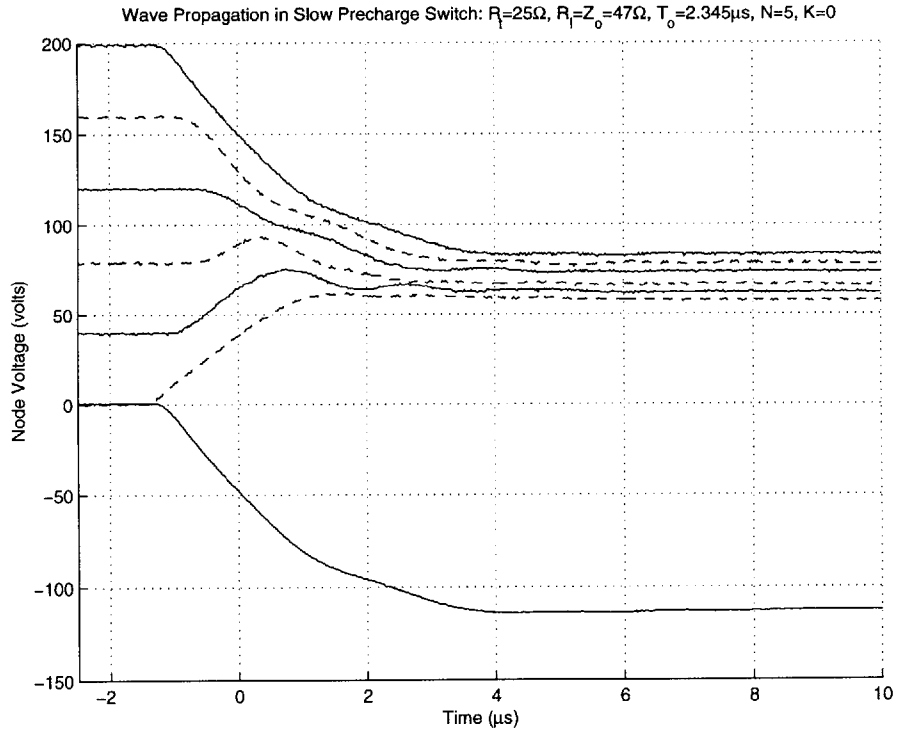


Figure 5-12: Captured Waveforms: Slow Switch, $R_t = 25\Omega, R_l = 47\Omega$, K=0

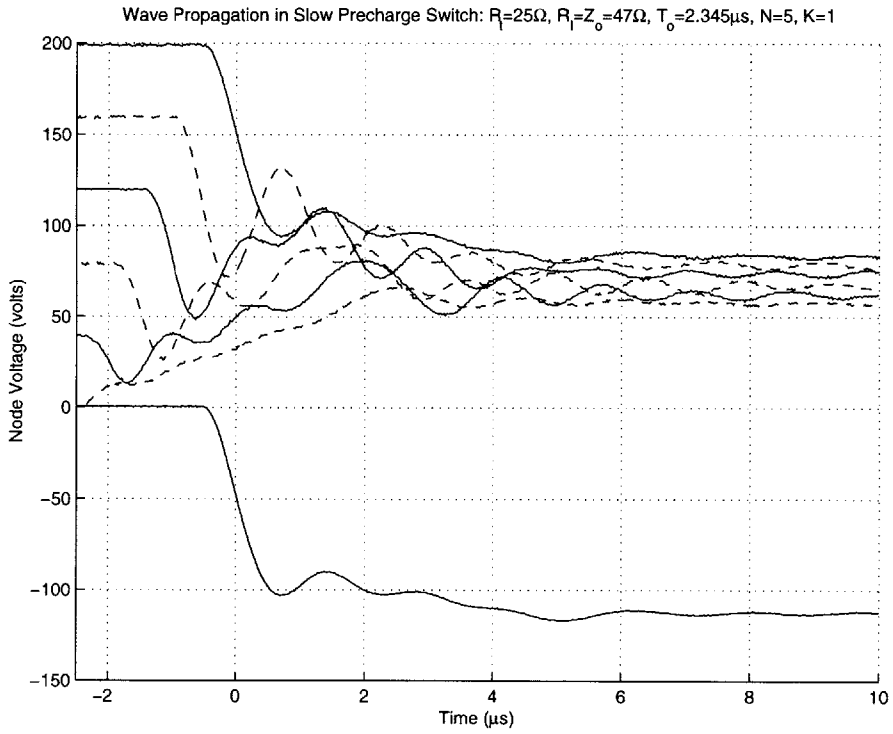


Figure 5-13: Captured Waveforms: Slow Switch, $R_t = 25\Omega$, $R_l = 47\Omega$, K=1

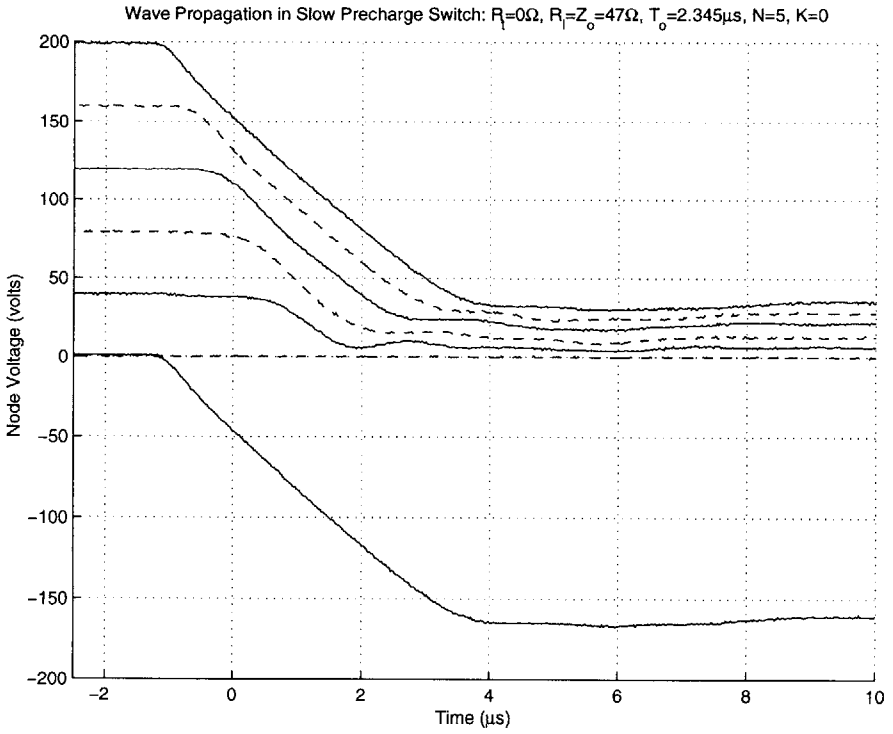


Figure 5-14: Captured Waveforms: Slow Switch, $R_t = 0\Omega$, $R_l = 47\Omega$, K=0

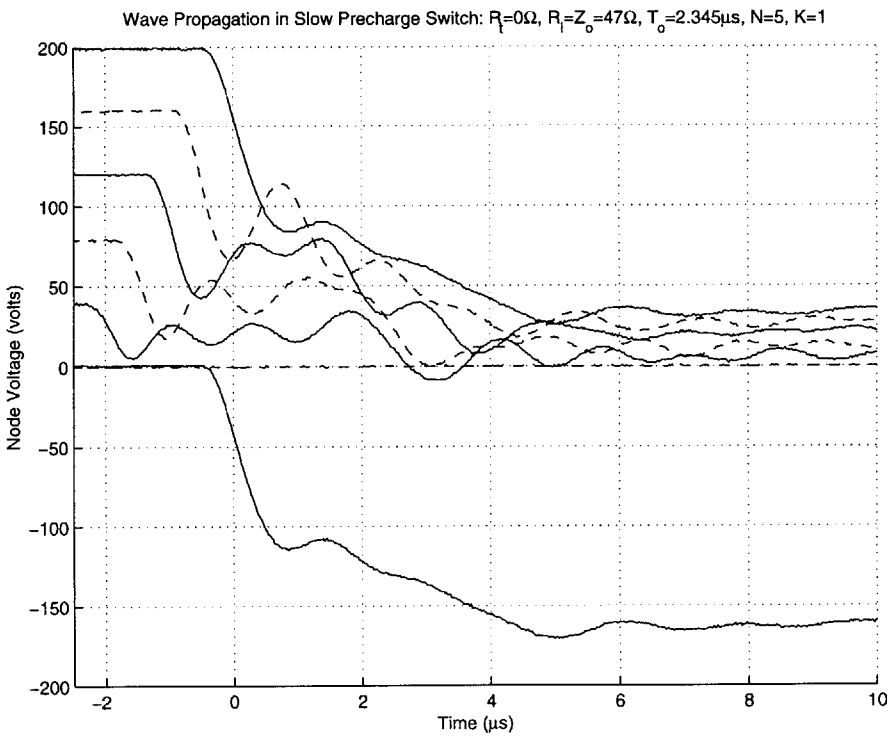


Figure 5-15: Captured Waveforms: Slow Switch, $R_t = 0\Omega, R_l = 47\Omega$, K=1

5.4.2 Actual Waveform vs. Simulated Waveform

The experimental outputs from the slow precharged switch were plotted against their predicted nominal responses, and are presented in Figures 5-16 to 5-22. Additional damping and loss of voltage at the output are evident in all of these figures. For instance, the final voltage at the output of the matched case is close to -87 Volts out of the full -100 Volts. This can be explained again by resistance in the inductors (which are identical to the ones used in Experiment I) as well as the voltage drops in the thyristors. Again, an error of close to 5% in the nominal T_o is seen. The previous hypothesis that component inaccuracies are to blame for the poor time scaling is supported by Figure 5-23, in which the output of the matched switch for K=1 is rescaled using the adjusted T_o from Experiment I.

Nominal T_o

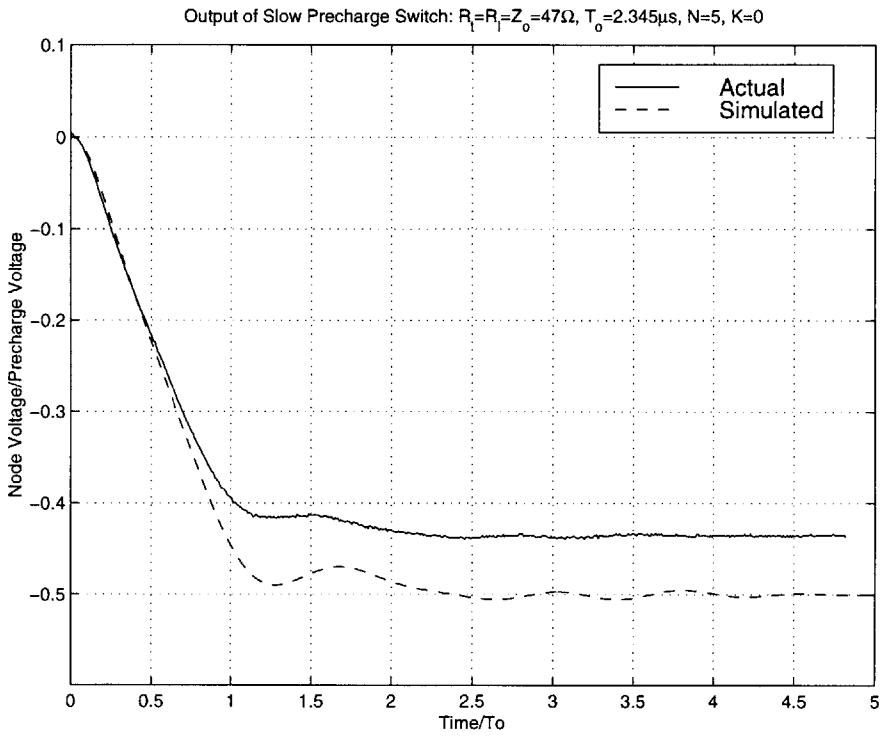


Figure 5-16: Slow Switch: Actual vs. Simulation for Nominal T_o, $R_t = 47\Omega$, K=0

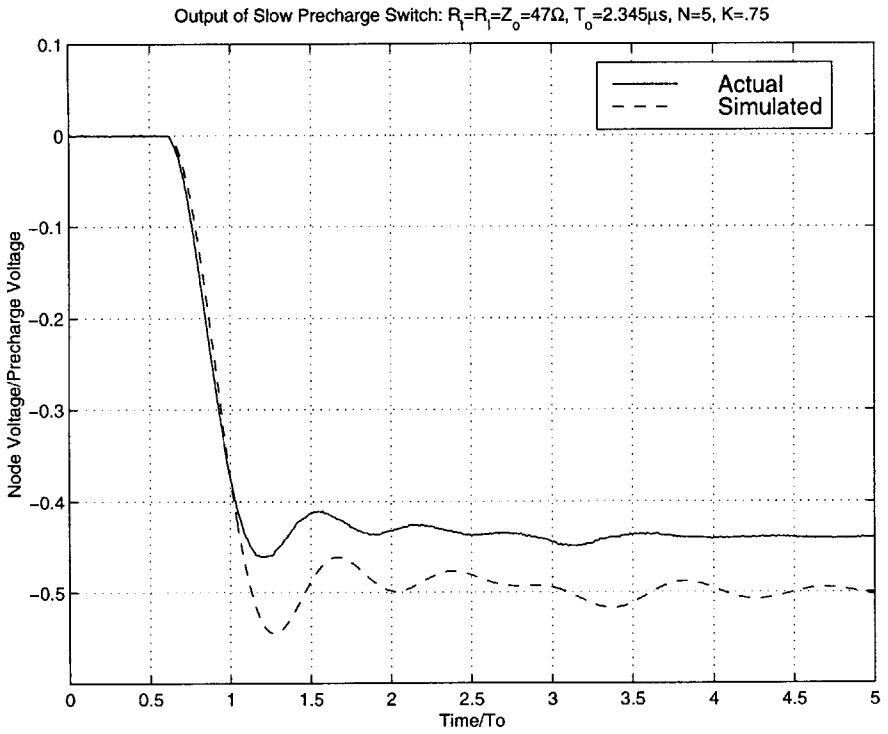


Figure 5-17: Slow Switch: Actual vs. Simulation for Nominal T_o, $R_t = 47\Omega$, K=.75

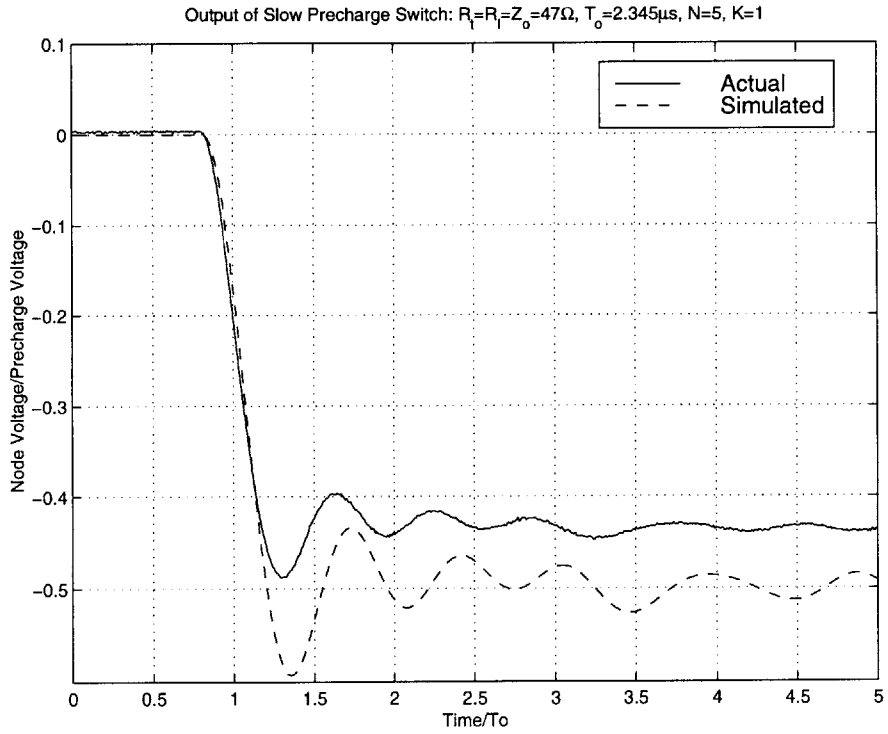


Figure 5-18: Slow Switch: Output vs. Simulation for Nominal T_o, $R_t = 47\Omega$, K=1

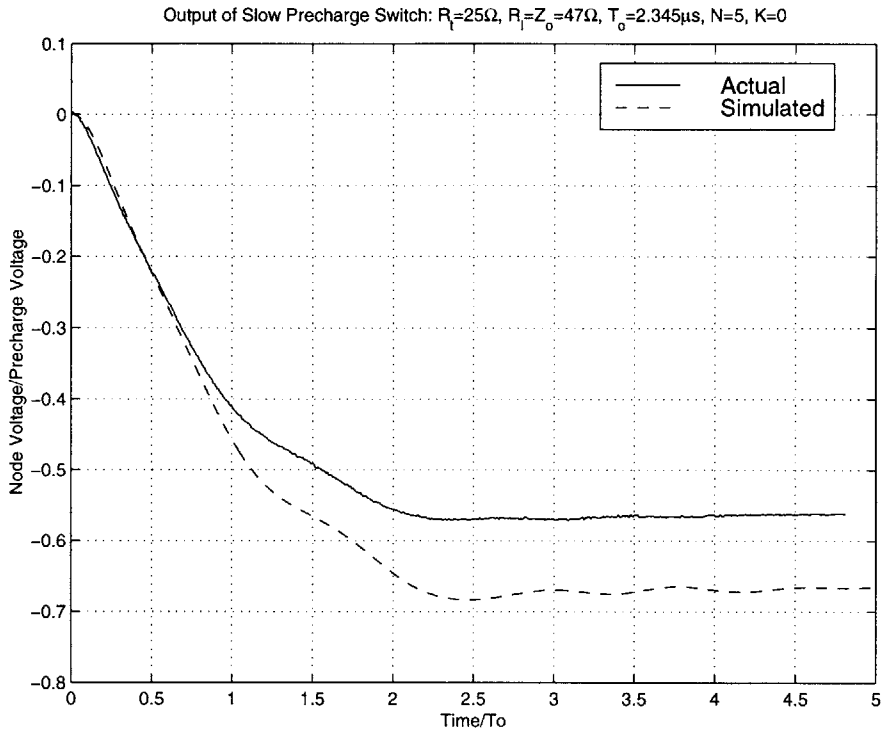


Figure 5-19: Slow Switch: Actual vs. Simulation for Nominal T_o, $R_t = 25\Omega$, K=0

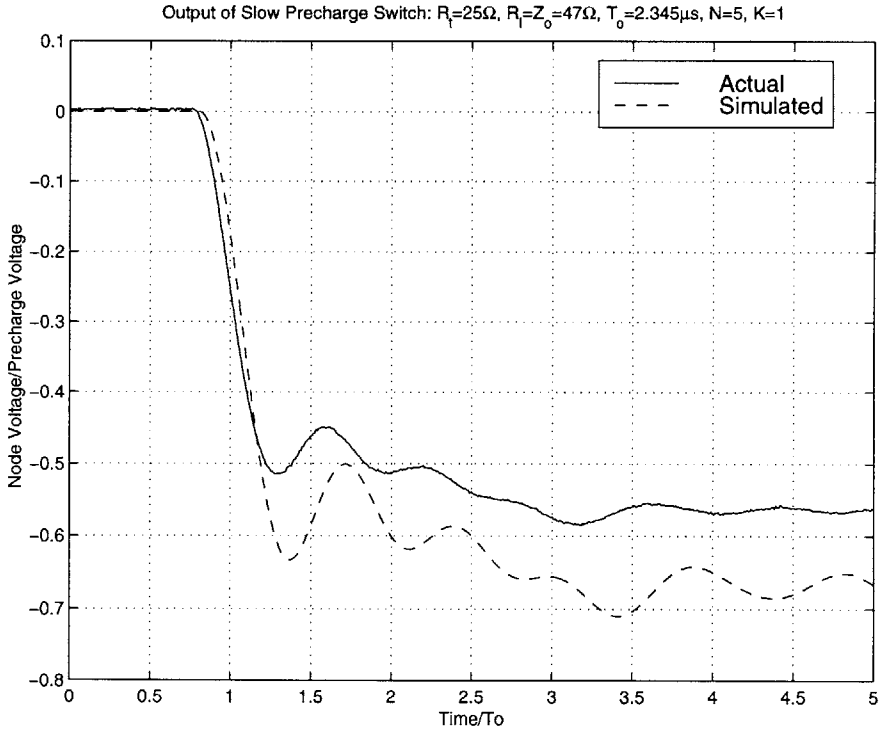


Figure 5-20: Slow Switch: Actual vs. Simulation for Nominal T_o, $R_t = 25\Omega$, K=1

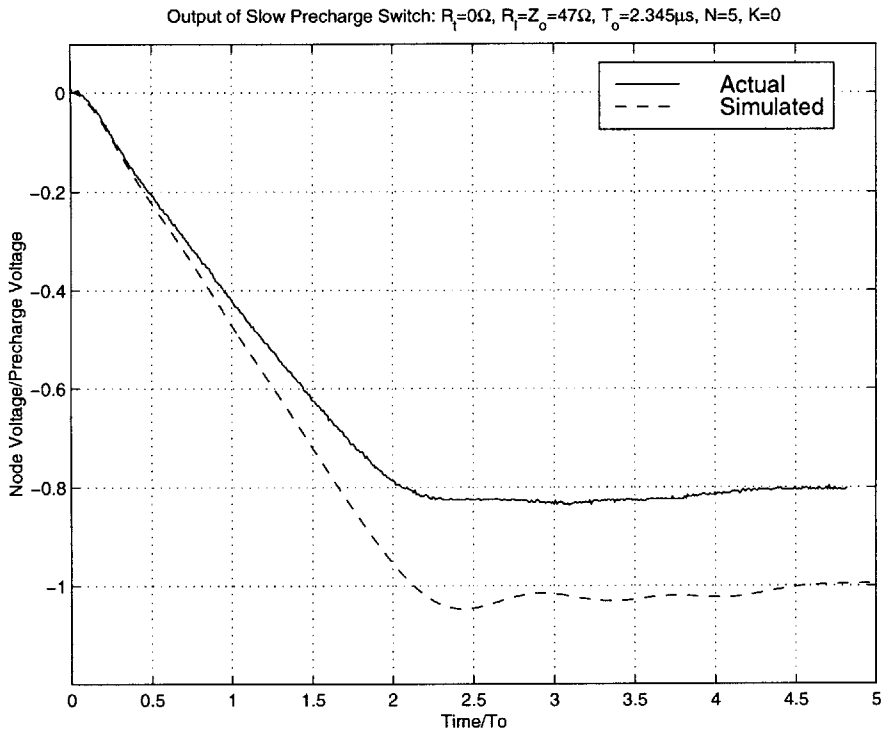


Figure 5-21: Slow Switch: Actual vs. Simulation for Nominal T_o, $R_t = 0\Omega$, K=0

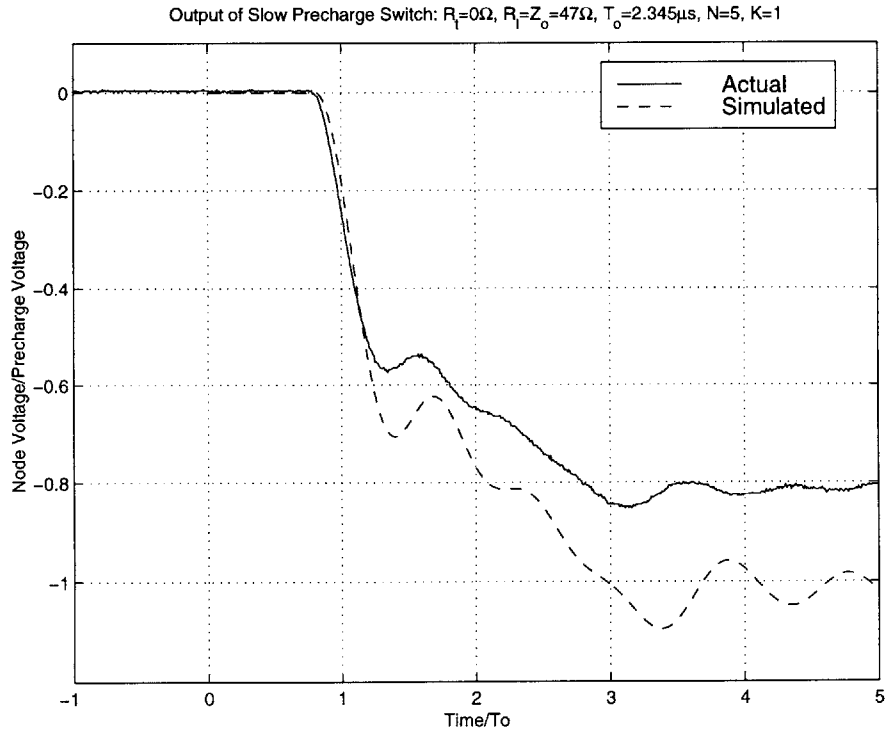


Figure 5-22: Slow Switch: Actual vs. Simulation for Nominal T_o, $R_t = 0\Omega$, K=1

Adjusted T_o

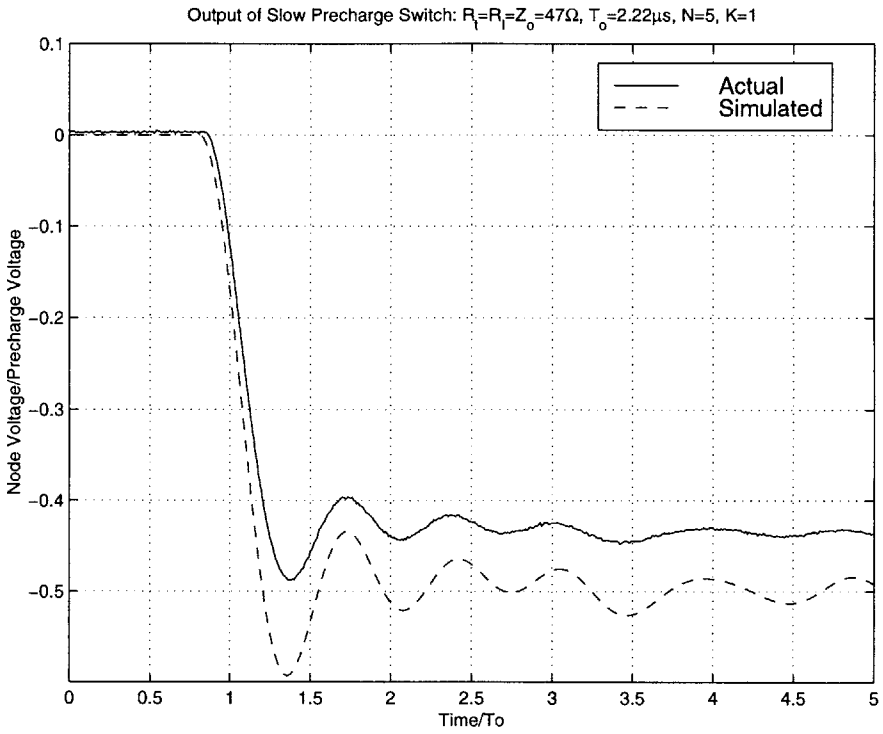


Figure 5-23: Slow Switch: Actual vs. Simulation for Adjusted T_o, $R_t = 47\Omega$, K=1

5.5 Experiment III: Medium Precharged Switch

The third experiment was designed mainly to illustrate the time scaling property of these structures. As a result, it was designed to operate at ten times the speed of the previous experiment. With the exception of the switch, the setup was otherwise identical to the one used in Experiment II and is shown in Figure 5-24.

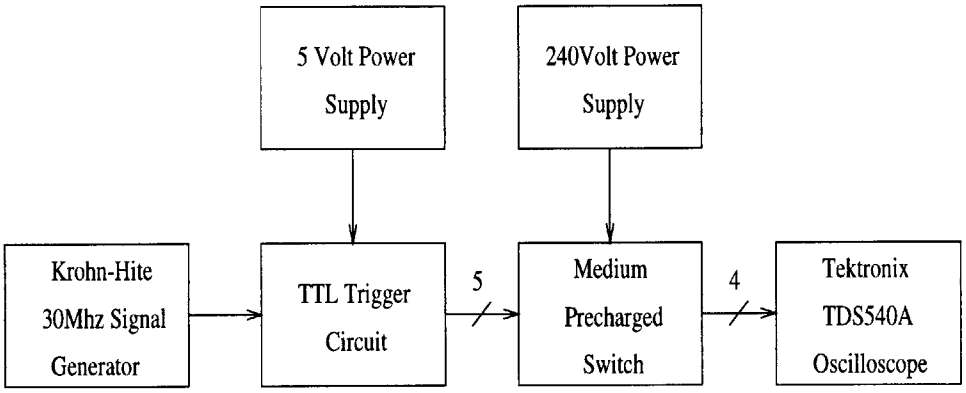


Figure 5-24: Test Setup for Experiment III: Medium Precharged Switch

5.5.1 Captured Waveforms

The experimental responses of the medium precharged switch are presented in Figure 5-25 and 5-26. Only the double-matched case is considered for K=0 and 1. For the most part, these responses are not as damped as was the slow case. A cursory inspection of the plots reveals that the internal waveforms of the medium switch converge more closely in the steady state than for the slow switch. This tends to suggest that the corresponding parasitic resistance of the inductors here is less— a reasonable assertion, given that smaller inductors often use less windings and hence have less resistance.

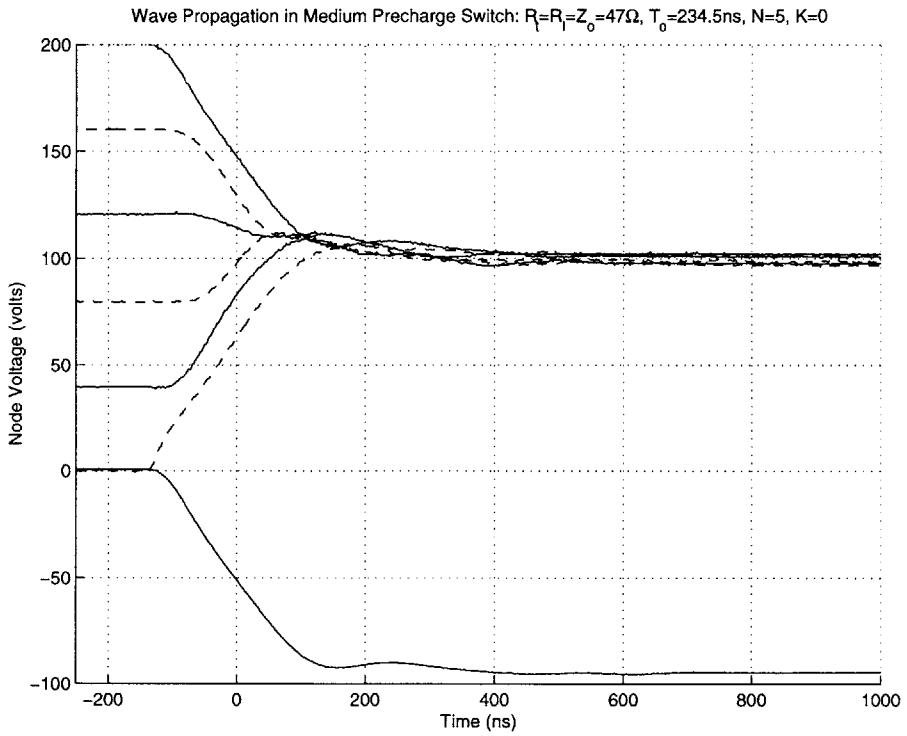


Figure 5-25: Captured Waveforms: Medium Switch, $R_t = R_l = 47\Omega$, K=0

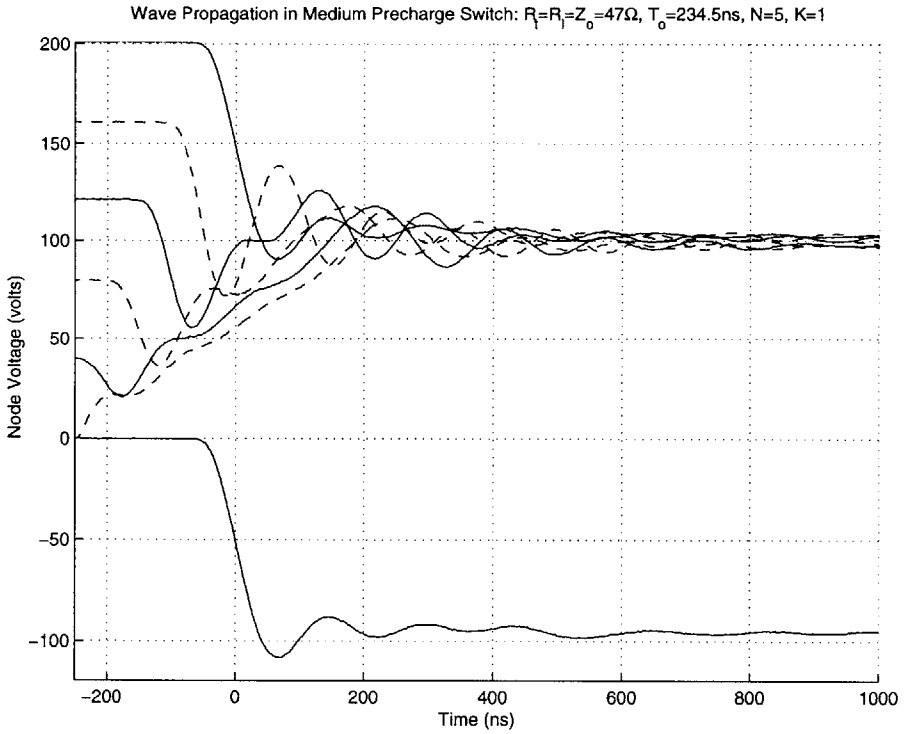


Figure 5-26: Captured Waveforms: Medium Switch, $R_t = R_l = 47\Omega$, K=1

5.5.2 Actual Waveform vs. Simulated Waveform

The investigated output responses for the medium switch are presented against their simulated predictions in Figures 5-27 to 5-29. Unlike the slow switch experiment, less voltage is lost and the output approaches nearly -95 Volts (out of -100 Volts). This is quite reasonable considering that the on-state voltage of the GA301A is approximately 1 Volt. As with the previous experiments there appears to be a small error in the nominal T_o of 234ns used. If the simulations are refitted using an adjusted T_o of 225ns (an error of less than 4%) a better correlation is found. Lastly, although the amount of resistance is almost negligible, the response still appears to have some damping associated with it. It is possible that at these time scales the nonlinear switching behavior of the thyristors is responsible for this damping process.

Nominal T_o

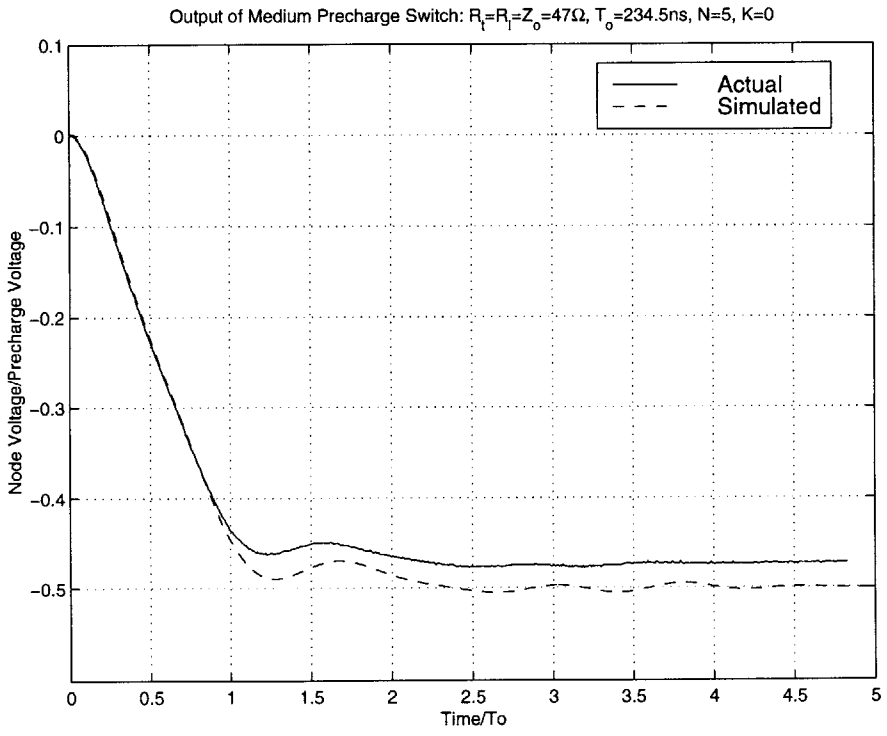


Figure 5-27: Medium Switch: Actual Output vs. Simulation for Nominal T_o, K=0

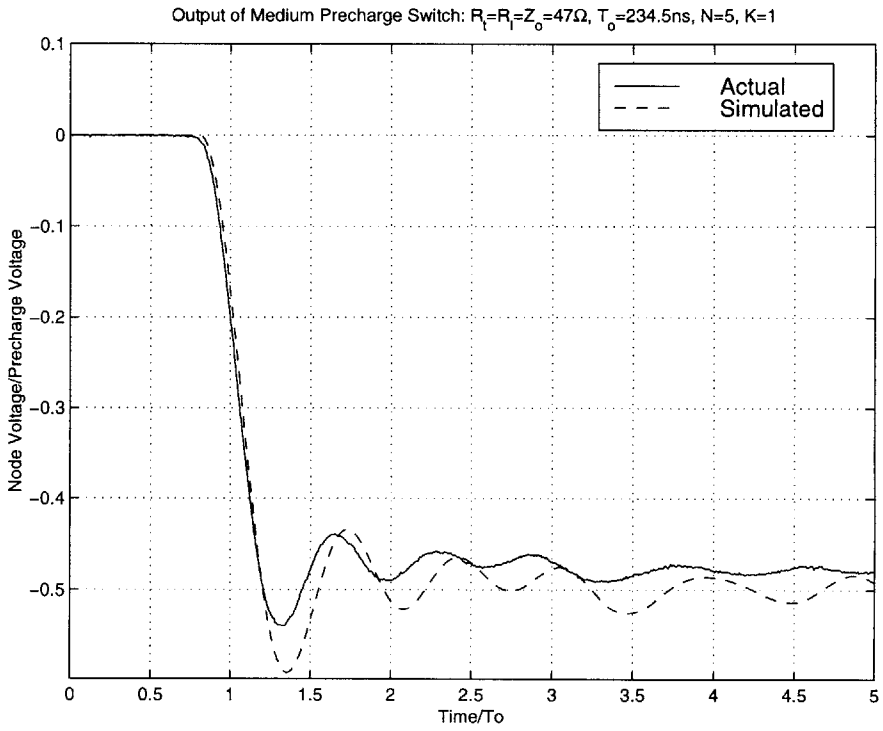


Figure 5-28: Medium Switch: Actual Output vs. Simulation for Nominal T_o, K=1

Adjusted T_o

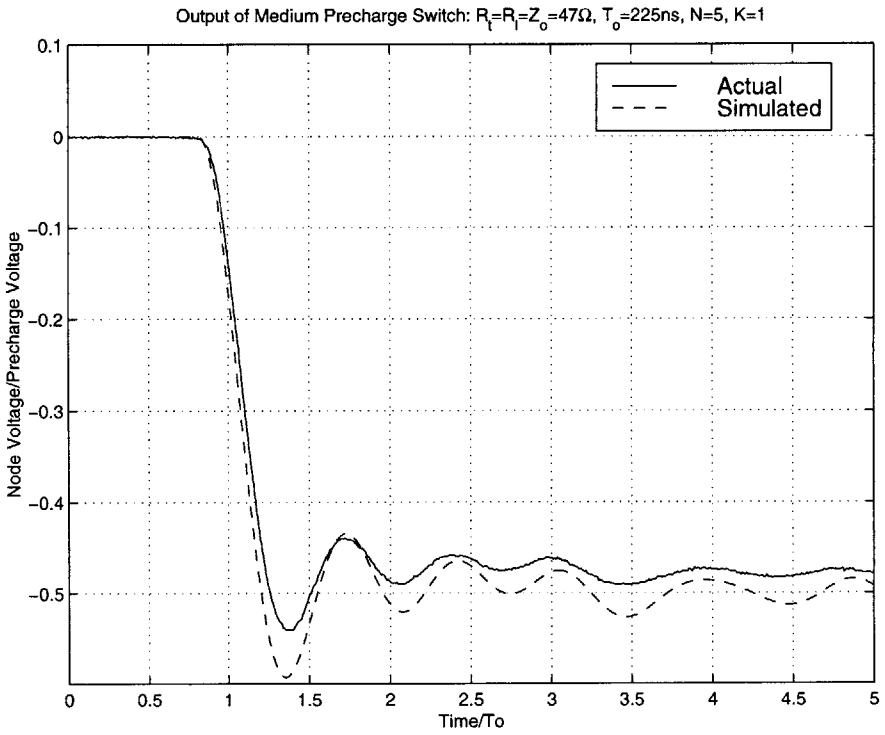


Figure 5-29: Medium Switch: Actual Output vs. Simulation for Adjusted T_o, K=1

5.6 Experiment IV: Fast Precharged Switch

For the final experiment, a fast switch that incorporated no additional inductance or capacitance was studied. The faster time scales associated with this circuit precluded the use of a TTL triggering circuit. Instead, each inter-switch delay was "hardwired" into the system by means of five variable-length coaxial cables. A Wavetech pulse generator was then used to drive all five lines simultaneously. In addition, every line was terminated with a 51Ω resistor in parallel with the primary side of each pulse transformer to minimize reflections. Delays of 0ns, 1ns and 2ns were implemented in this fashion. A block diagram of the setup used is shown in Figure 5-30.

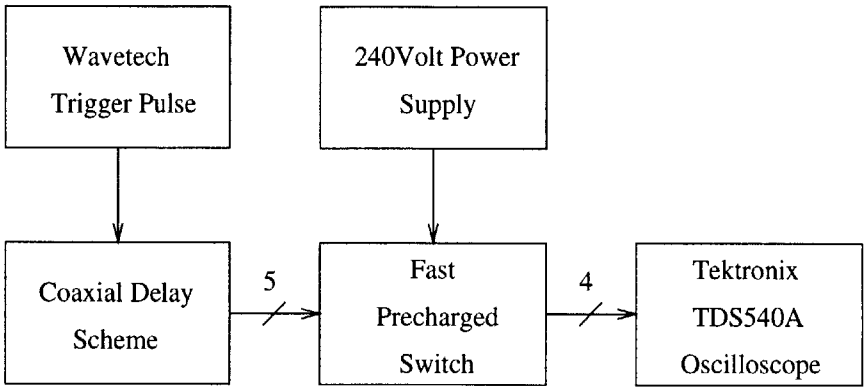


Figure 5-30: Test Setup for Experiment IV: Fast Precharged Switch

5.6.1 Captured Waveforms

Figures 5-31 through 5-33 show the behavior of the fast precharged switch for 0ns, 1ns, and 2ns inter-switch delays respectively. It is apparent that the delays have some effect on the wave propagation through the switch. However, without additional processing, it is difficult to say exactly how this is occurring. A comparison of the three output responses does reveal a sharpening phenomena as seen in Figure 5-34. Post-processing of these waves in Matlab yield the rise times in Table 5.6 which corroborate this effect.

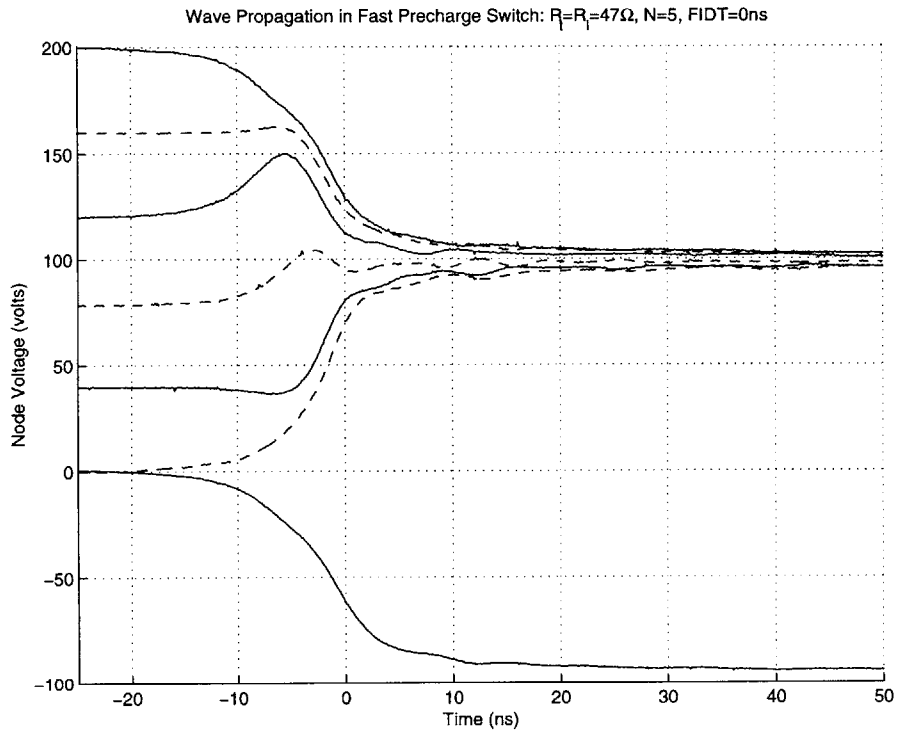


Figure 5-31: Captured Waveforms: Fast Switch, FIDT=0ns

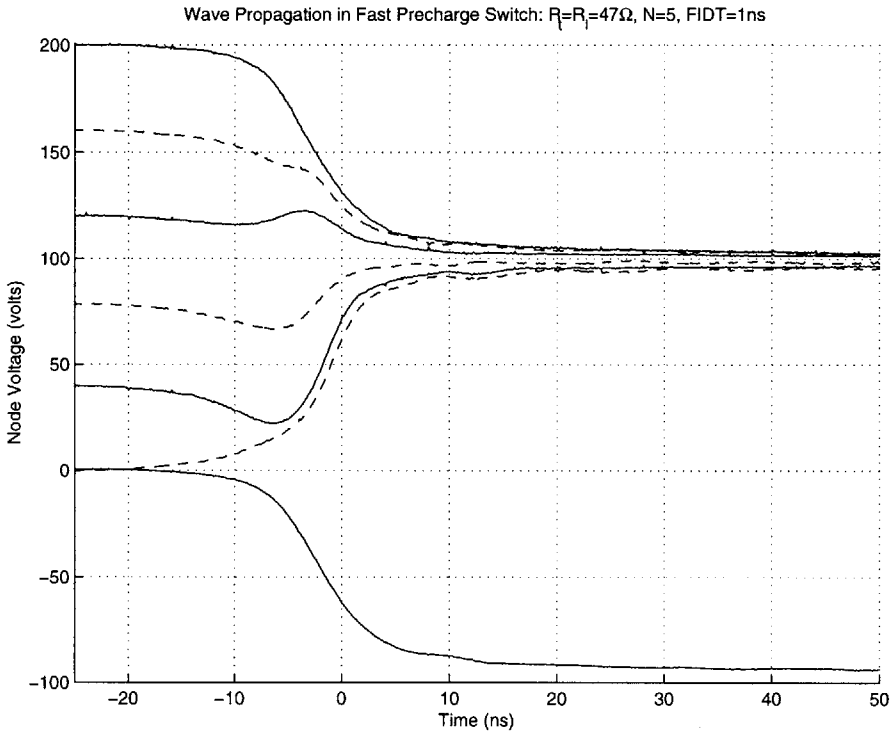


Figure 5-32: Captured Waveforms: Fast Switch, FIDT=1ns

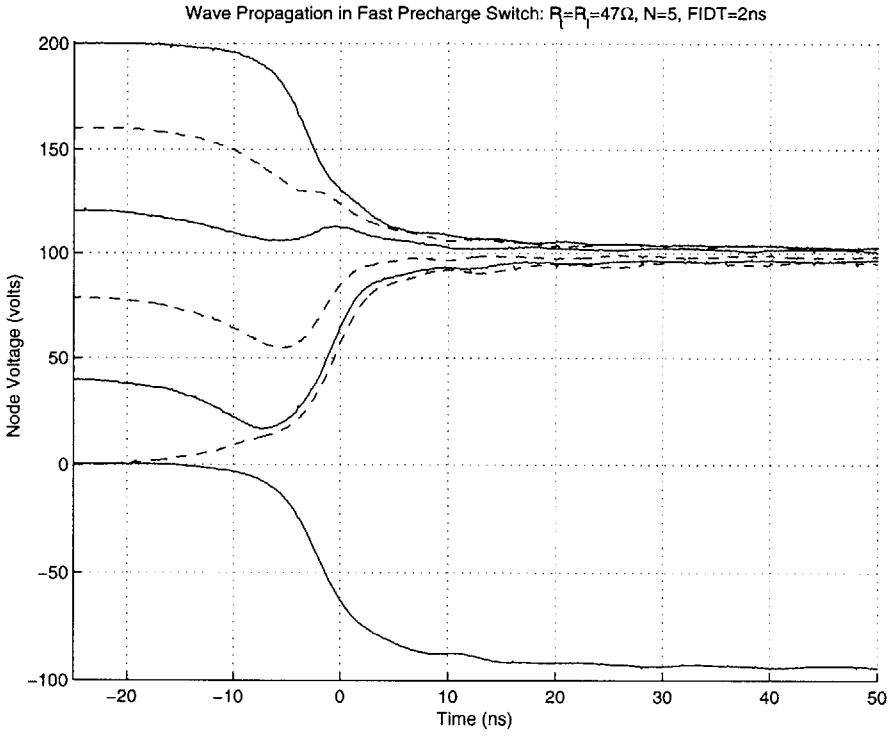


Figure 5-33: Captured Waveforms: Fast Switch, FIDT=2ns

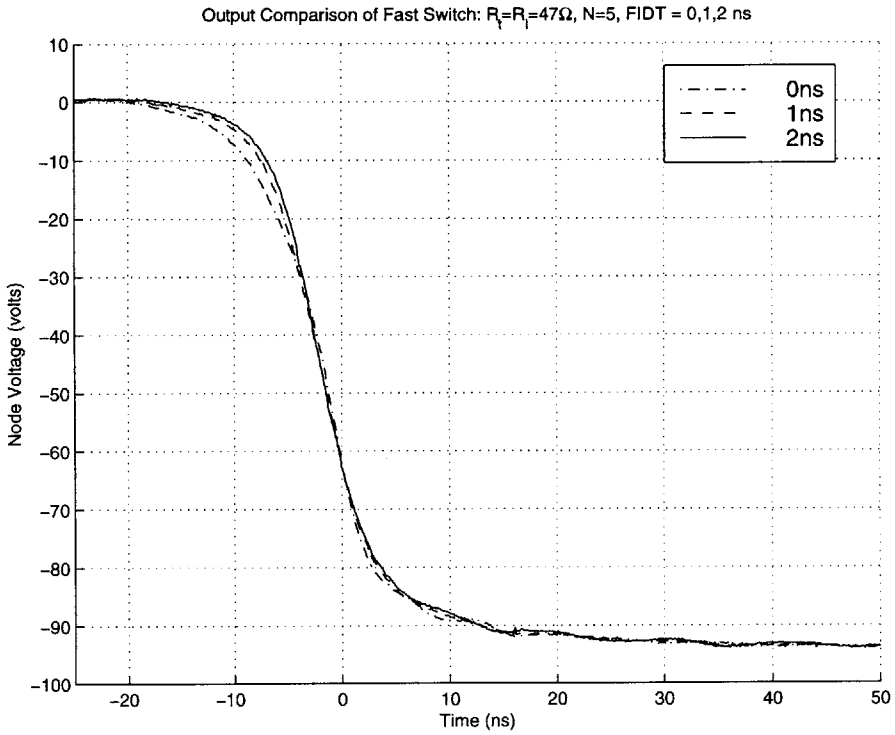


Figure 5-34: Output Comparison of Fast Switch for FIDT=0ns,1ns,2ns

Table 5.6: Rise Times for Fast Switch

Delay	0ns	1ns	2ns
Rise Time	15.8ns	13.4ns	13.1ns

5.6.2 Discussion

The fast precharged switch provided an opportunity to study how a FIDT scheme might affect a precharged switch which, strictly speaking, could be different from the models developed in this thesis. Because the thyristor speeds of this circuit are inevitably slower than the natural delays of the system, the models used until now begin to break down. It is possible that K is influencing the circuit more at the "device" level than as seen previously in the models presented. A better feel for this influence can be gained by examining the differential switch voltages instead of the node voltages. The previously captured waveforms were post-processed in Matlab to show the corresponding switch voltages. These plots are given in Figures 5-35 through 5-37.

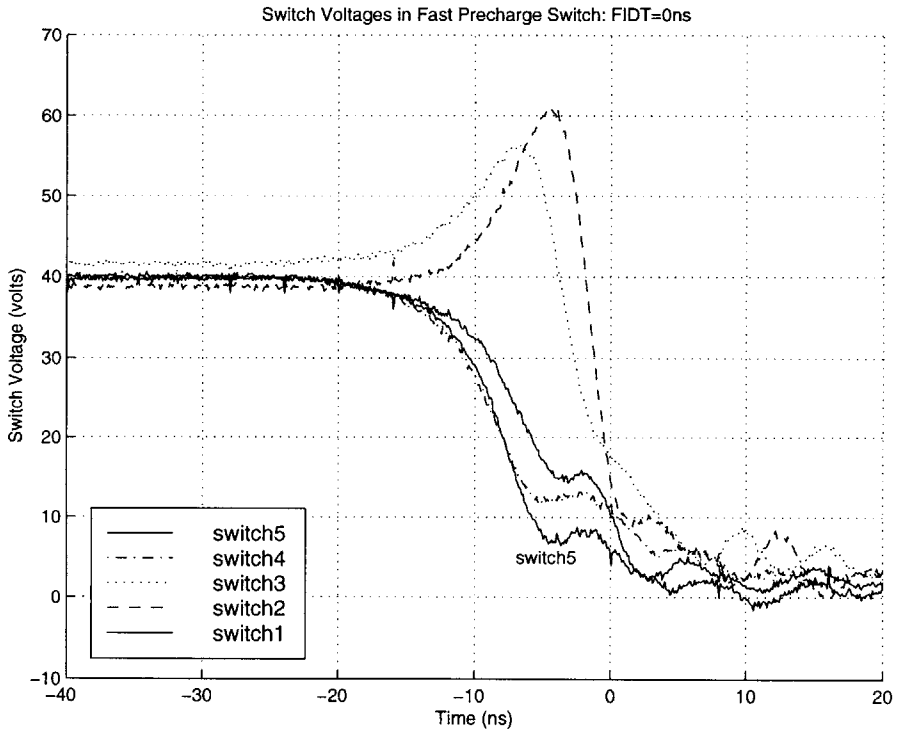


Figure 5-35: Switch Voltages in Fast Switch: FIDT=0ns

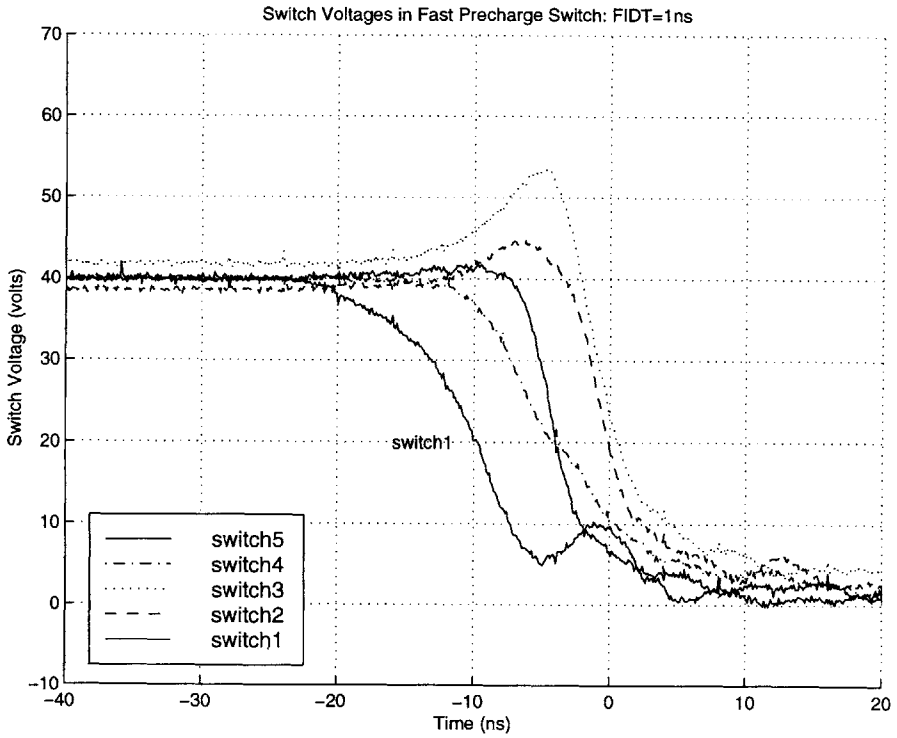


Figure 5-36: Switch Voltages in Fast Switch: FIDT=1ns

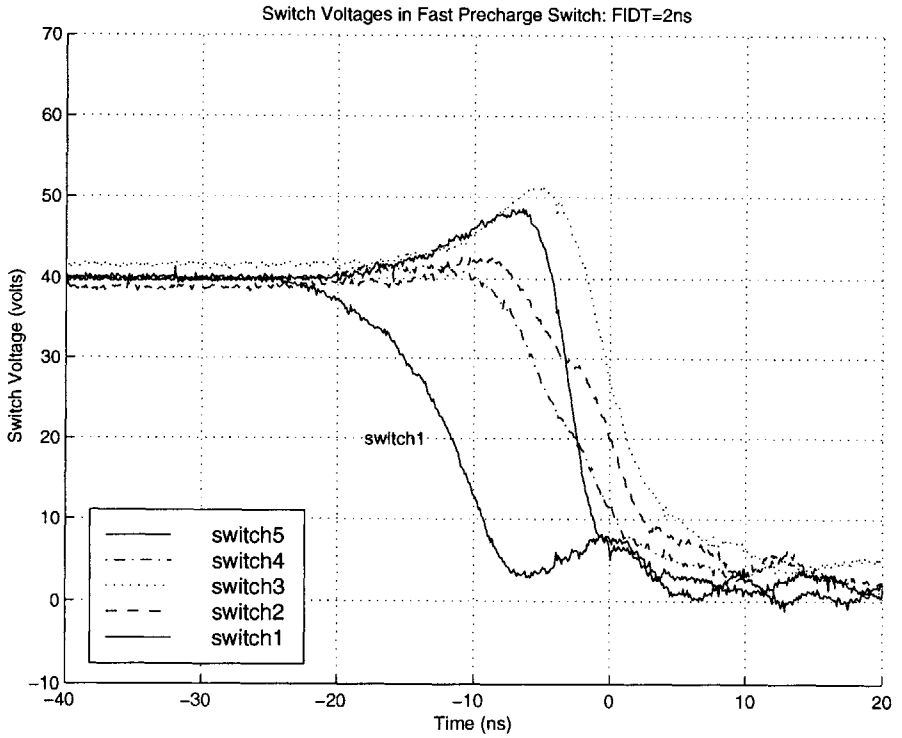


Figure 5-37: Switch Voltages in Fast Switch: FIDT=2ns

These plots reveal some interesting facts about the system's internal behavior. For instance, when no delay is added, one would expect all of the switches to commutate in roughly the same amount of time. However, this is not seen in Figure 5-35. Instead, switches 4 and 5 begin to commutate first, followed by switch 1. This causes a voltage in excess of 50 Volts to appear across these switches before they close. It is difficult to say why this occurred. One possible explanation is simply that individual device variation is present, and as a result, some thyristors in the stack are slower than others.

Based on the previous models, if an inter-switch trigger delay is introduced into the system, one would expect to see each device closing in succession with a higher differential voltage than the previous one. At 1ns of delay, this does not appear to be the case, but the waveforms are at least tending towards this configuration. Switch 1 is closing first, while 4 and 5 are approaching 2 and 3. When 2ns of delay is added, switch 5 is closing before 3 but after 2. Presumably if enough delay was added, this behavior would eventually resolve itself. These plots also lend some insight as to why the rise times are decreasing with additional delay. Because the rise time is essentially determined by how fast the last switch can trigger, a higher differential voltage across switch 5 would result in faster rise times as recorded in the experimental device characterization of Appendix H. In all plots it is clear that the differential voltage across switch 5 is increasing with the added delay. However, for the delays seen here the cascade still fails to close as quickly as a single stage thyristor would— roughly 10ns.

Before concluding that the devices are largely responsible for the previously seen behavior, it is important to verify that poor trigger coupling is not the culprit. The trigger signals into the primaries of their respective pulse transformer are shown in Figure 5-38. From this plot, it is clear that the trigger signals are reasonably staggered 2ns apart. Furthermore, these signals take about 4ns to reach 1 Volt, which is slow considering they are only about 2.5 times faster than the devices they are meant to trigger. From an experimental control standpoint, faster would certainly have been better. At the very least, however, the relative rise times are much closer, which is

good.

More importantly than what is seen at the primaries are the signals into the thyristor gates. Figure 5-39 shows the triggering signals into the primaries as well as their corresponding outputs at the secondaries. Here, it is seen that the secondary voltages start close to the gate-to-cathode voltage of the thyristor, approximately 0.6 Volts. In general, the outputs of the secondaries follow the inputs well, although small lags of about 2ns are also evident. Additionally, a greater variation in the relative spreading of the secondary signals when compared to the primaries is noticed. This may be caused by differences in the pulse transformers and differing parasitics at each coupling point. Whatever the case may be, it is unlikely that the small variations in the arrival of the triggering signals[4] would have the impact seen in Figure 5-37. Consequently, the original hypothesis that the devices themselves are responsible is still maintained.

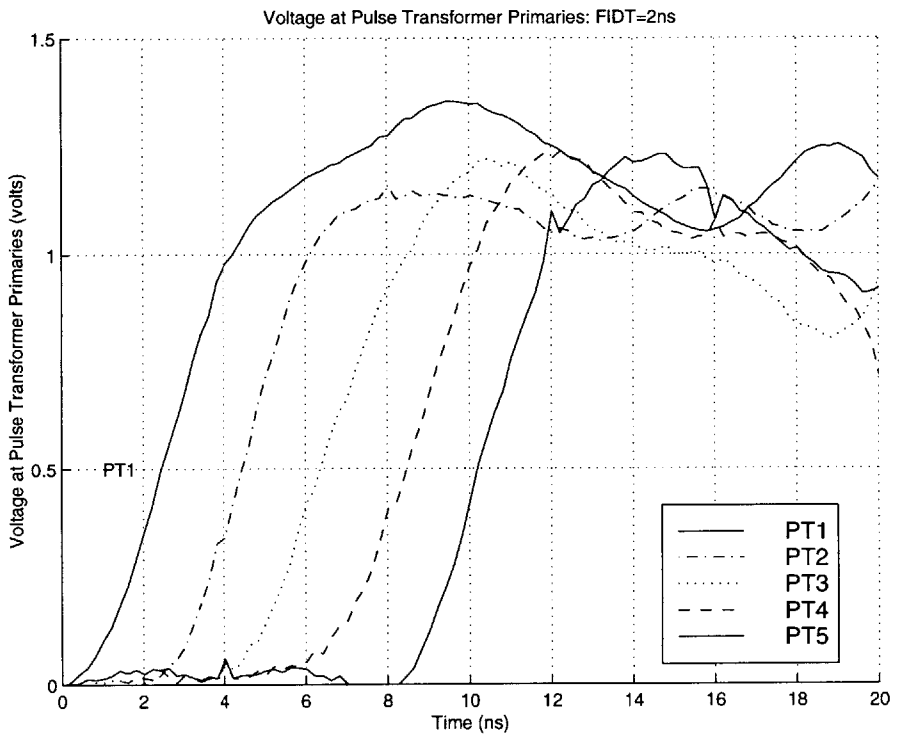


Figure 5-38: Voltage at Pulse Transformer Primaries: FIDT=2ns

[4]This is not to say that faster trigger signals would not help, since the variation in thyristor behavior might be dependent on the rise time of their respective trigger signals.

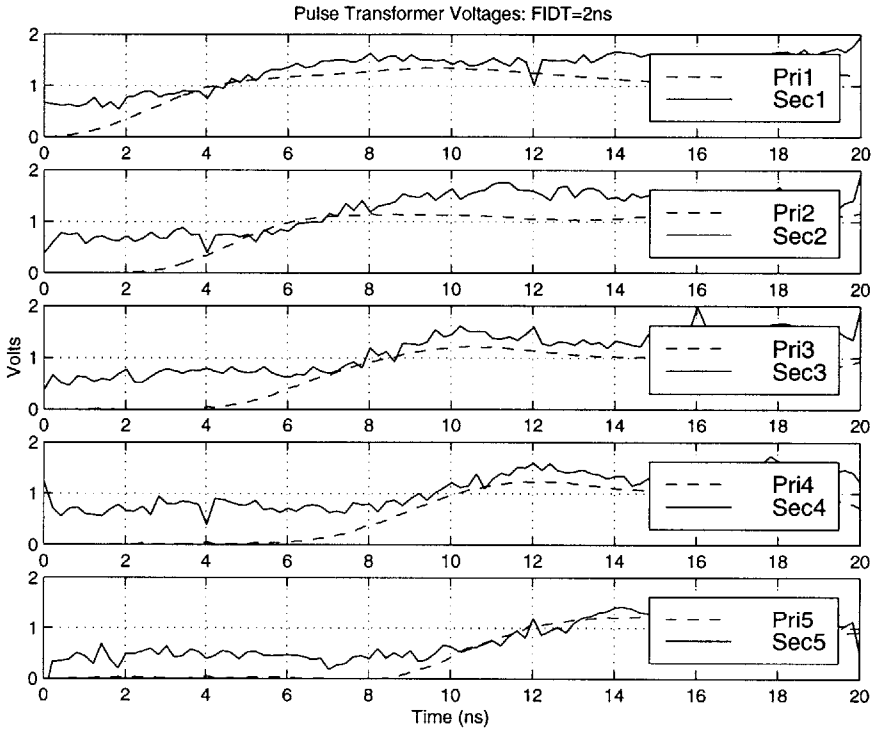


Figure 5-39: Pulse Transformer Voltages: FIDT=2ns

Chapter 6

Conclusions

6.1 Summary

6.1.1 The Problem

The purpose of this thesis was to formulate an understanding of how a series distributed cascade switch behaves. This goal was accomplished through a combination of means: modeling, simulation and experimental validation. Because the author is unaware of any previous publications specifically on the topic of distributed switch behavior, the initial work on this subject was only concerned with understanding the first order behavior of these networks. Consequently, practical modeling choices are evident and certain simplifications made. For instance, the models employed were limited to piecewise LTI networks, consisting only of passive components and ideal switching elements. Furthermore, it has been assumed that the parasitic inductance and capacitance in these circuits form lumped LC lines, similar to those used for approximating the behavior of transmission lines.

6.1.2 Approach

Under the assumption that the parasitics in a distributed switch form a uniform LC ladder structure, the previous work in this area served as a starting point upon which to build. LC line models were subsequently modified to include ideal switching

elements. These uncharged, switched LC lines were then studied for different values of K, where

$$K = \frac{\Delta T_{ISD}}{T_o/N}, \tag{6.1}$$

a normalized delay factor that governs the switch closing time along the cascade. The impact of K on the output response and internal behavior was carefully interpreted. The uncharged switch model was later energized to produce the precharged model of a switch that could be used in practice. As before, the role of delays in the switching sequence was also studied for the precharged switch.

6.1.3 Simulation Based Results

From simulation, it was seen that K provides a means by which a designer can speed up the rise time of a distributed switch. It was also seen that this improvement in rise time came at the expense of increased overshoot of the output and longer global delays. Furthermore, it was clear that the amount of stress internal to these structures increased with rising K's. Even so, studies showed that K's less than one produced reasonable improvements. For instance, using a $K = 0.75$, a designer can more than halve his expected rise time and only pay for it with a 10% overshoot at the output! This tradeoff is seen in Figure 6-1 where the percent overshoot versus rise time for a five stage, double-matched, uniform precharged switch is presented.

As an additional issue, the importance of proper impedance matching in these switches was also confirmed. It was shown that the need to terminate the ends of these lines in their characteristic impedance was commensurate with increasing K's. As an aside, because matched terminations result in a 50% loss of output voltage for the uniform precharged switch, the benefits of tapering the line impedance were mentioned briefly.

6.1.4 Experimental Results

To determine the validity of these models, four different five stage circuits were built for experimentation. The first experiment was a simple unswitched LC ladder. This

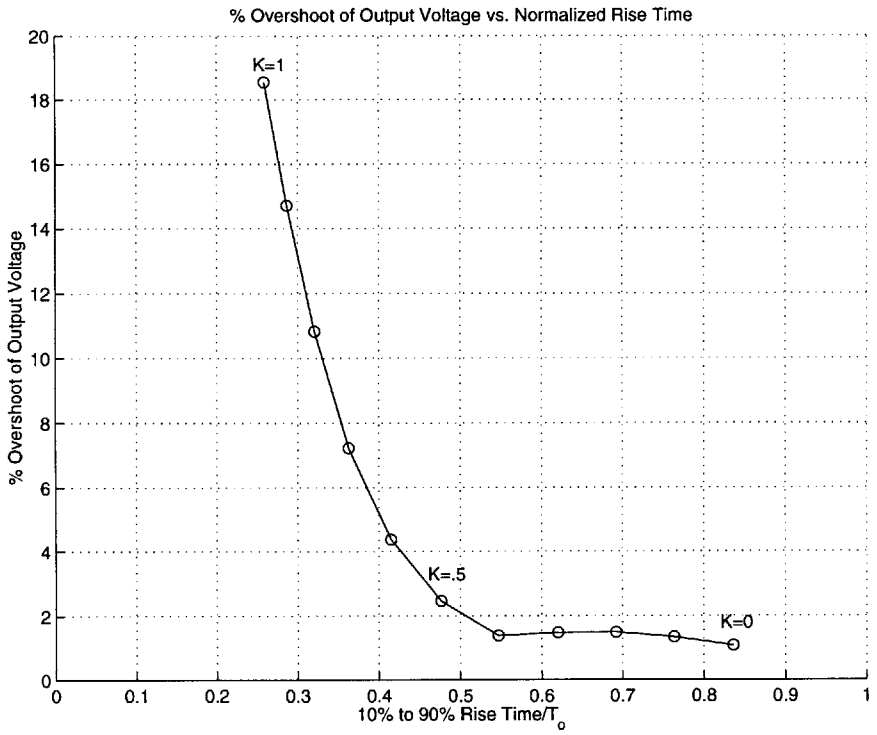


Figure 6-1: Overshoot vs. Rise Time for Precharged Switch: R_t=R_l=Z_o, N=5

circuit confirmed that the models introduced in Chapters 2 and 3 were generally in good accord with the results obtained experimentally, with the possible exception of unmodeled resistive losses in the line. However, it should be mentioned that these losses were a direct result of the large artificial inductances placed throughout the network. In many practical (natural) cases, the resistive loss associated with these systems is negligible.

The remaining experiments were all precharged switched lines. Experiment II was designed to show how the K factor would come into play if Experiment I now included switches in the line. Again, the models predicted the behavior well, with the exception of resistive losses. In the third experiment, the test circuit was designed to be ten times faster than the previous slow switch. This was done to confirm the property of time scaling discussed earlier. The results for the third circuit, the so-called medium switch, were in some respects even better than the prior experiments, because there was less resistance from the inductors. However, because the $\frac{T_o}{N}$ delay

of each cell in the medium switch was only about 4.5 times faster than the switching time of the SCR's, the onset of some second order effects was evident.

Finally, in the fourth and last experiment, the fast switch, it was shown that when the $\frac{T_o}{N}$ of the line was small compared to the switching speeds of a cell, the models developed here were no longer adequate to describe the complete behavior of the switched line. However, even for the fast switch, it was observed that increasing K still resulted in a beneficial effect on the output of the switch. What is not clear is how much of the benefit was a result of the influence of K as shown in these models versus its influence on unmodeled effects. One such effect is the influence of additional over-voltage on later switches caused by finite K's.

6.2 Future Directions

Although this thesis represents a significant step forward in understanding how a distributed switch behaves, a great deal remains unanswered. Currently, there is a lot of room for improving the models seen here as well as for variations on a theme that should be explored.

6.2.1 Modeling

All the models herein (or otherwise) are predicated upon certain basic assumptions. When these assumptions break down, modifications are necessary for accurate results. One example of this was seen during the fast switch experiment. Because no modeling of switch commutation was carried out, poor model correlation was found. A desire to apply the information presented here to fast distributed switches will inevitably prompt a need to augment the simple switch model used. A time varying resistor would be a reasonable improvement. At first, a fixed trajectory for the resistance with time may be used, and a more complicated model that continually updates its resistance based on the associated current and voltage of the device would be appropriate later.

Besides the additional modeling of actual solid state devices, better models for the

parasitics are also important. The LC model used throughout this thesis represents a first order parasitic model, but in different layouts where these parasitics may be distributed differently, the L-cell used here might be less adequate. Under some circumstances, including the parasitic capacitance that is in parallel with the switch may be important.

6.2.2 Variations

The majority of all structures studied were uniform LC lines. However, it was seen that a modification as simple as tapering the impedance could result in a significant improvement in response time and output voltage. For these reasons the tapered line deserves further study. One of the questions that needs to be answered for this topology is how to taper the line to minimize reflections, while still achieving optimal voltage transfer.

Another issue that must be addressed as higher voltage switches are built is how to couple the trigger signals. Pulse transformers provide a convenient way as long as the number of switches is not prohibitive. But, regardless of the number of devices, there is always a limitation to the amount of isolation a transformer can provide. Higher voltages require larger transformers and larger means more costly and slower. Furthermore, if devices requiring a constant drive are used, core saturation becomes a significant problem. One approach that might be taken in the future is to build a switch that requires one trigger signal and "auto fires" the remaining switches. In fact, there are already a variety of topologies and devices that lend themselves to this, such as capacitive triggering networks and avalanche transistors[1, 4].

Appendix A

Matlab Code

A.1 Lumped LC Line (LCline.m)

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%This script file calculates the output behavior of m lumped LC     %
%lines, where the number of cells is varied from 1 to m. The        %
%following parameters are calculated: Overshoot, Rise Time, and     %
%Delay to 50% of the Output. The time waveform of the mth iteration %
%is also produced. The user specifies the number of iterations (m), %
%the propagation delay of the line (To), the characteristic         %
%impedance (Zo) of the line and the source resistance (rS) and load %
%resistance (rL).                                                   %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function ans=LCline(m,To,Zo,rS,rL);
for n=1:m

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Network Parameters                                                 %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
c=To/Zo; %Total Capacitance
l=To*Zo; %Total Inductance
```

```
%Propagation Parameters
TD=(l*c)^.5;  %To
UD=TD/n; %To/N

%switch from total capacitance and inductance to cell values.
c=c/n; %Cell Capacitance
l=l/n; %Cell Inductance

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%SubMatrices                                                                 %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
RLC=[0 1/c; -1/l -rS/l];
C1=[0 -1/c; 0 0];
L1=[0 0; 1/l 0];
LC=[0 1/c; -1/l 0];
LCR=[-1/(rL*c) 1/c; -1/l 0];
RLCR=[-1/(rL*c) 1/c; -1/l -rS/l];

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Calculate system matrix "A".                                               %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
if n>=2
A=zeros(n*2,n*2);

A(1:2,1:2)=[RLC];
A(2*n-1:2*n,2*n-1:2*n)=[LCR];

j=1;
for k=2:n-1;
```

```
A(k+j:k+1+j,k+j:k+1+j)=[LC];
j=j+1;
end

j=1;
for k=2:n;
A(k+j:k+1+j,k-2+j:k-1+j)=[L1];
A(k-2+j:k-1+j,k+j:k+1+j)=[C1];
j=j+1;
end

else
A=RLCR;
end

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Generate the remaining state space vectors, etc.                          %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
B=zeros(size(1:2*n));
B(1,2)=1/1;
B=B';

C=zeros(size(1:2*n));
C(2*n-1)=1;

D=0;

Sys=ss(A,B,C,D);        %Generate State Space system
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Determine step function of lumped line.                                      %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
t=5*TD;
T=linspace(0,t,10000);
norm=length(T)/t;
[Y,T,X]=step(Sys,T);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Call params subroutine and perform both normalizations                        %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
temp=params(Y,rS,rL, norm);
OS(n)=temp(1);
Delay1(n)=temp(2);
Delay2(n)=temp(2)*n;
tr1(n)=temp(3);
tr2(n)=temp(3)*n;
end

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Plot Results                                                                  %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
figure(1)
plot(T,Y)
title('Output of a Uniform LC line, R_{s}=R_{l}=Z_{o}, N=50')
ylabel('Output Voltage/Source Voltage')
xlabel('Time/T_{o}')
grid on

figure(2)
```

```
plot(OS, 'o')
title('%Overshoot of Output vs. Number of Cells (N)')
ylabel('%Overshoot')
xlabel('Number of Cells (N)')
grid on

figure(3)
subplot(2,1,1)
plot(Delay1, 'o')
title('Delay Time to 50% of Output Normalized by T_{o} vs.
Number of Cells (N)')
ylabel('Delay/T_{o}')
xlabel('Number of Cells (N)')
grid on
subplot(2,1,2)
plot(Delay2, 'o')
title('Delay Time to 50% of Output Normalized by T_{o}/N vs.
Number of Cells (N)')
ylabel('NDelay/T_{o}')
xlabel('Number of Cells (N)')
grid on

figure(4)
subplot(2,1,1)
plot(tr1,'o')
title('10% to 90% Rise Time Normalized by T_{o} vs.
Number of Cells (N)')
ylabel('Rise Time/T_{o}')
xlabel('Number of Cells (N)')
grid on
```

```
subplot(2,1,2)
plot(tr2, 'o')
title('10% to 90% Rise Time Normalized by T_{o}/N vs.
Number of Cells (N)')
ylabel('NRise Time/T_{o}')
xlabel('Number of Cells (N)')
grid on
```

A.2 Parameters (params.m)

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%This script calculates the Overshoot, Rise Time, and Delay of a    %
%lumped LC line. It takes as input the output response (Y), the     %
%source resistance (rS), the load resistance (rL) and a             %
%normalization factor that is essentially the # of samples per time.%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function ans=params(Y,rS,rL,norm);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Calculate the DC steady state Voltage.                              %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Final=rL/(rS+rL);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Calculate the Overshoot.                                            %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
OS=(max(Y)-Final)/Final*100;
n=1;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Calculate the time to 10%, 50% and 90% of the final value.          %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
while Y(n) <.1*Final
n=n+1;
end
t1=n;

while Y(n) < .5*Final
```

```
n=n+1;
end
Delay=n;

while Y(n) <.9*Final
n=n+1;
end
t2=n;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Return the Overshoot, Delay and Rise Time to the Main script file. %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
OS;
Delay;
tr=t2-t1;
ans=[OS Delay/norm tr/norm];
```

Appendix B

PSpice Netlists

B.1 Uncharged Uniform Switch

```
* Schematics Netlist *

R_Rload    0 $N_0001  50
C_C5       0 $N_0001  .4pF
V_V2       $N_0002 0 100V
X_U1       $N_0003 $N_0004 Sw_tClose PARAMS: tClose={K*0*ID} ttran=0ps
+  Rclosed=0.00001 Ropen=100Meg
C_C1       0 $N_0005  .4pF
L_L1       $N_0004 $N_0005  1nH
C_C2       0 $N_0006  .4pF
L_L2       $N_0007 $N_0006  1nH
C_C3       0 $N_0008  .4pF
C_C4       0 $N_0009  .4pF
X_U2       $N_0005 $N_0007 Sw_tClose PARAMS: tClose={K*1*ID} ttran=0ps
+  Rclosed=0.00001 Ropen=100Meg
X_U3       $N_0006 $N_0010 Sw_tClose PARAMS: tClose={K*2*ID} ttran=0ps
```

```
+  Rclosed=0.00001 Ropen=100Meg
X_U4        $N_0008 $N_0011 Sw_tClose PARAMS: tClose={K*3*ID} ttran=0ps
+  Rclosed=0.00001 Ropen=100Meg
X_U5        $N_0009 $N_0012 Sw_tClose PARAMS: tClose={K*4*ID} ttran=0ps
+  Rclosed=0.00001 Ropen=100Meg
R_Rsource   $N_0002 $N_0003  {Rs}
L_L3        $N_0010 $N_0008  1nH
L_L4        $N_0011 $N_0009  1nH
L_L5        $N_0012 $N_0001  1nH
```

B.2 Precharged Uniform Switch

```
* Schematics Netlist *



X_U1        $N_0001 $N_0002 Sw_tClose PARAMS: tClose={K*0*ID} ttran=0ps
+  Rclosed=0.00001 Ropen=100Meg
R_Rsource   0 $N_0001  {Rs}
R_Rload     0 $N_0003  50
X_U3        $N_0004 $N_0005 Sw_tClose PARAMS: tClose={K*2*ID} ttran=0ps
+  Rclosed=0.00001 Ropen=100Meg
L_L2        $N_0006 $N_0004  1nH
X_U2        $N_0007 $N_0006 Sw_tClose PARAMS: tClose={K*1*ID} ttran=0ps
+  Rclosed=0.00001 Ropen=100Meg
L_L1        $N_0002 $N_0007  1nH
X_U4        $N_0008 $N_0009 Sw_tClose PARAMS: tClose={K*3*ID} ttran=0ps
+  Rclosed=0.00001 Ropen=100Meg
C_C1        $N_0007 0  .4pF IC=20V
X_U5        $N_0010 $N_0011 Sw_tClose PARAMS: tClose={K*4*ID} ttran=0ps
```

```
+  Rclosed=0.00001 Ropen=100Meg
C_C4        $N_0010 0   .4pF IC=80V
C_C3        $N_0008 0   .4pF IC=60V
C_C2        $N_0004 0   .4pF IC=40V
C_C5        $N_0012 0   .4pF IC=100V
C_Cout      $N_0012 $N_0003   1uF IC=100V
L_L3        $N_0005 $N_0008   1nH
L_L4        $N_0009 $N_0010   1nH
L_L5        $N_0011 $N_0012   1nH
```

B.3 Precharged Tapered Switch

```
* Schematics Netlist *



X_U1        $N_0001 $N_0002 Sw_tClose PARAMS: tClose={K*0*ID} ttran=0ps
+  Rclosed=0.00001 Ropen=100Meg
R_Rsource   0 $N_0001   {Rs}
R_Rload     0 $N_0003   50
X_U3        $N_0004 $N_0005 Sw_tClose PARAMS: tClose={K*2*ID} ttran=0ps
+  Rclosed=0.00001 Ropen=100Meg
X_U2        $N_0006 $N_0007 Sw_tClose PARAMS: tClose={K*1*ID} ttran=0ps
+  Rclosed=0.00001 Ropen=100Meg
X_U4        $N_0008 $N_0009 Sw_tClose PARAMS: tClose={K*3*ID} ttran=0ps
+  Rclosed=0.00001 Ropen=100Meg
X_U5        $N_0010 $N_0011 Sw_tClose PARAMS: tClose={K*4*ID} ttran=0ps
+  Rclosed=0.00001 Ropen=100Meg
C_C5        $N_0012 0   .4pF IC=100V
C_Cout      $N_0012 $N_0003   1uF IC=100V
```

```
L_L5        $N_0011 $N_0012  1nH
C_C1        $N_0006 0  2pF IC=20V
L_L1        $N_0002 $N_0006  .2nH
C_C2        $N_0004 0  1pF IC=40V
C_C3        $N_0008 0  .666pF IC=60V
C_C4        $N_0010 0  .5pF IC=80V
L_L2        $N_0007 $N_0004  .4nH
L_L3        $N_0005 $N_0008  .6nH
L_L4        $N_0009 $N_0010  .8nH
```

Appendix C

Tapered Switch Stresses

Plots of the voltage and current stresses experienced by the tapered precharged switch mentioned in Chapter 4 follow. These plots parallel those for the uniform precharged switch discussed previously. They are self explanatory and provided as purely supplemental information.

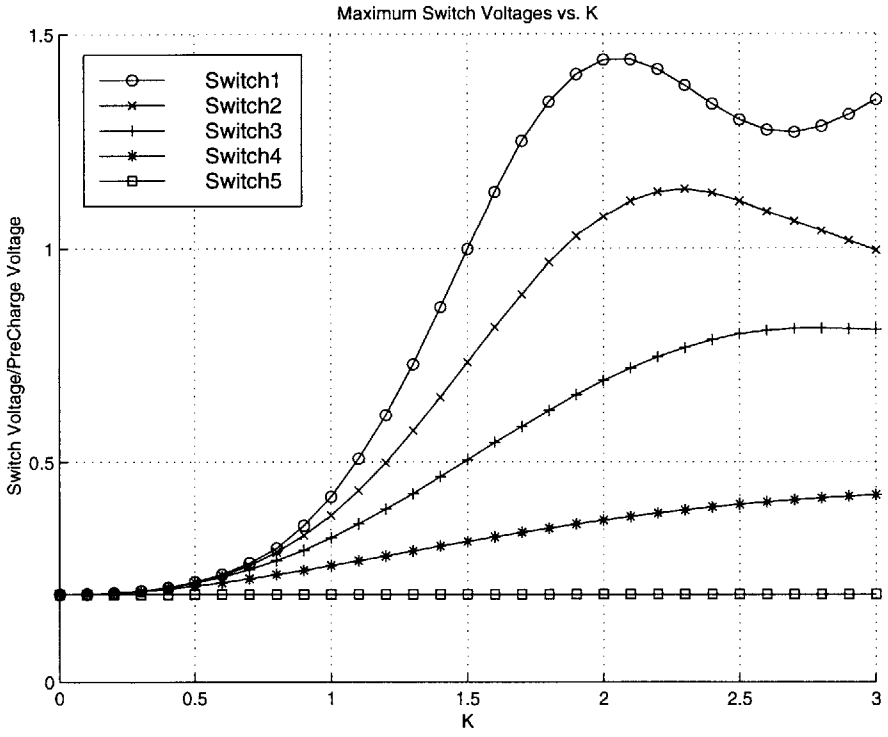


Figure C-1: Maximum Switch Voltage vs. K

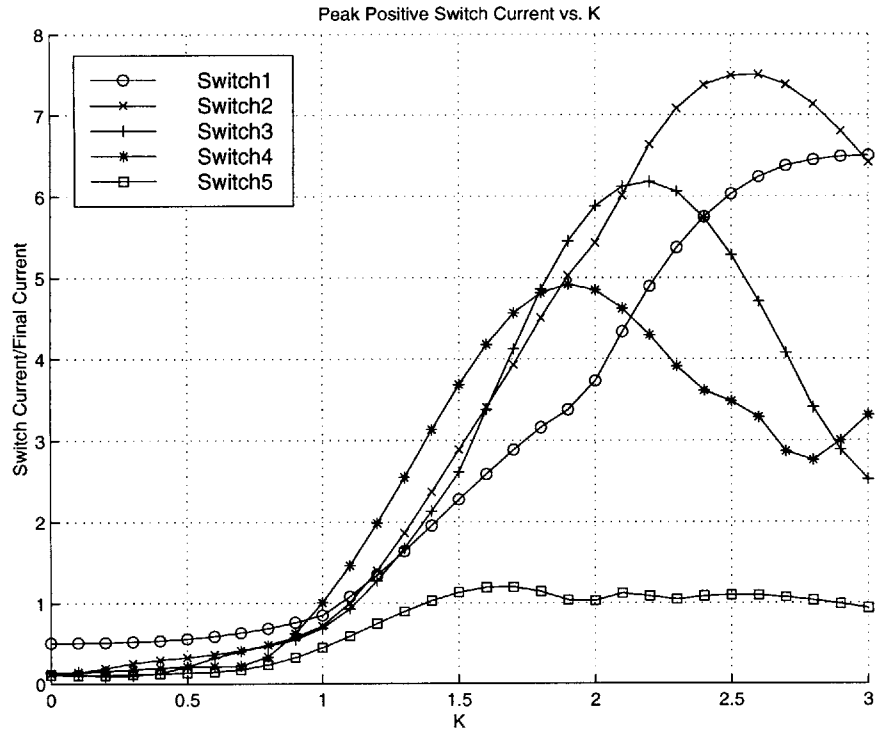


Figure C-2: Peak Positive Switch Current vs. K

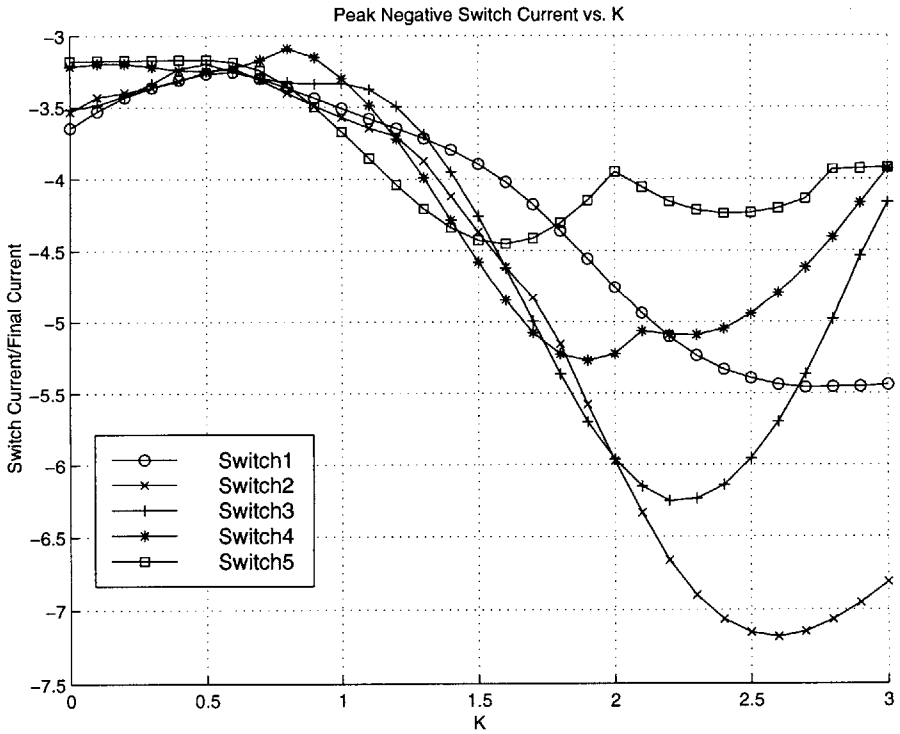


Figure C-3: Peak Negative Switch Current vs. K

Appendix D

L and C Selection Plots

The following plots were useful for selecting the artificial stage inductance and capacitance used in Experiments I-III.

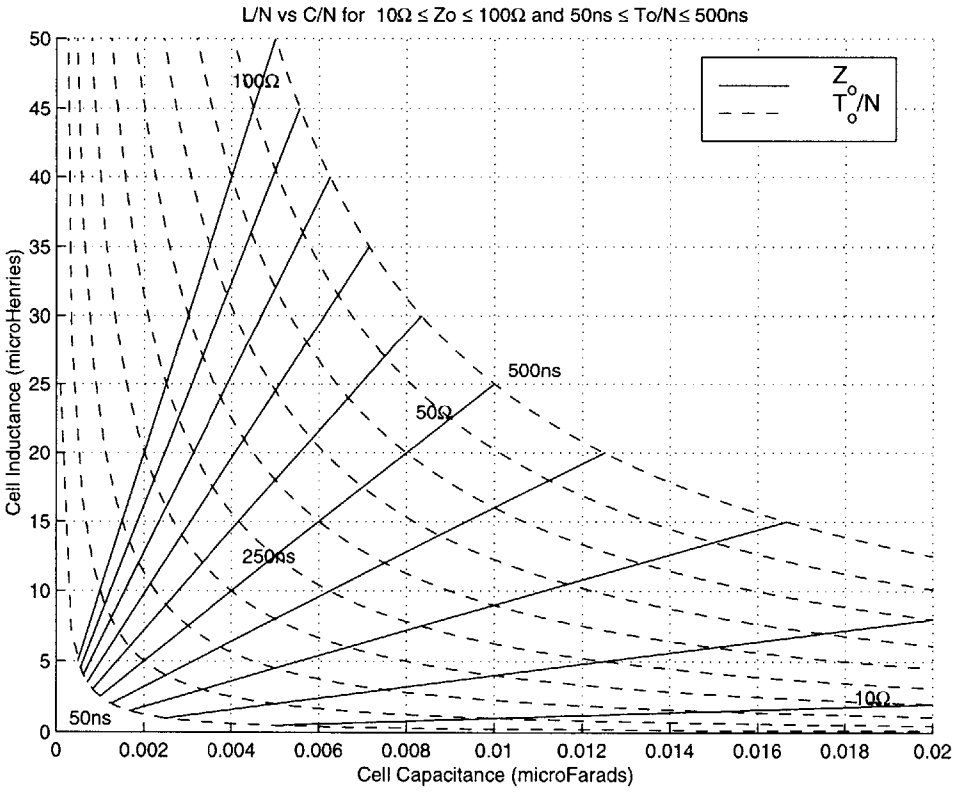


Figure D-1: $\frac{L}{N}$ and $\frac{C}{N}$ Selection Plot for the LC Ladder and Slow Switch

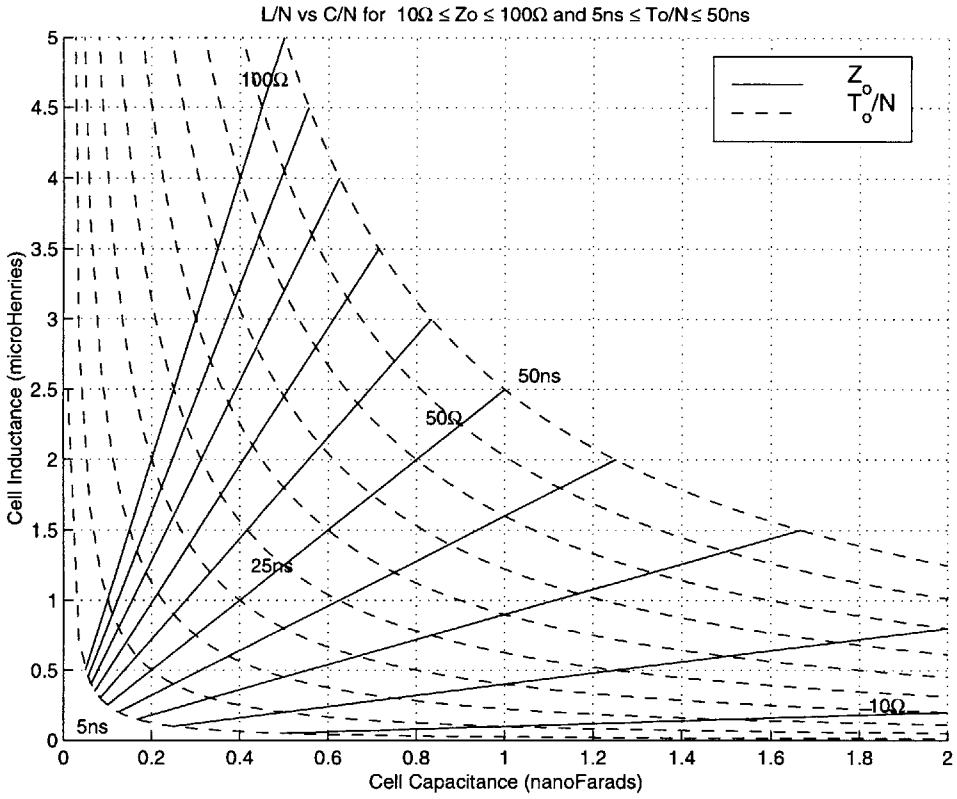


Figure D-2: $\frac{L}{N}$ and $\frac{C}{N}$ Selection Plot for Medium Switch

Appendix E

TTL FIDT Circuit

E.1 Theory of Operation

The digital circuit shown in Figure E-1 was built to provide the triggering mechanism for Experiments II and III. The circuit was implemented with FAST TTL components and has two modes of operation:

1. Fixed Inter-Switch Delay Triggering
2. Simultaneous Triggering

The appropriate timing diagrams for each mode are available in Figures E-2 and E-3. A brief description of how the circuit operates follows.

E.1.1 Shift Register

The heart of the trigger circuit is an eight bit shift register made by cascading two F194, four bit shift registers. Only the first five bits of this eight bit register are used. The register is configured to serially load a high input when clocked and S1 is selected low. With each rising clock edge, the output of the next succeeding bit in the register goes high until the register is cleared. If the clock input is variable, the delay until the next bit goes high becomes controllable.

Unfortunately, small delays require faster and faster clock speeds and a zero delay would require an infinitely fast clock! Instead, simultaneous triggering is achieved by

selecting S1 high. This results in a parallel load operation during the next clock cycle. Providing all of the input bits are tied high, the outputs also go high and remain so until cleared.

E.1.2 555 Timer

A 555 Timer was configured to run as the system clock. The timer defines the repetition rate for the trigger by active low clearing the shift register over every half cycle. The timer behavior is controlled by two external resistances and a capacitor, which govern the following relationships:

$$T_{555} = 0.7(R_a + R_b)C \tag{E.1}$$

and

$$DutyCycle = \frac{R_b}{(R_a + R_b)}. \tag{E.2}$$

For simplicity a potentiometer was used to implement R_a and R_b. The duty cycle for this application is not crucial and was selected experimentally to be close to 50%. Components' values were chosen to provide periods longer than the T_{min} required for recharging the switch. The values used for Experiments II and III are summarized in Table E.1 The need for large capacitance required the use of electrolytics. Because electrolytic capacitors are leaky by nature, they would ordinarily never be used for timing applications. But because precise timing is not required here, their use is acceptable.

Table E.1: Precharged Switch L and C Values

	$(R_a + R_b)$	C	T_{555}	T_{min}
Slow Trigger	100KΩ	220μF	15.4s	14s
Medium Trigger	100KΩ	22μF	1.54s	1.4s

E.1.3 Pulse Generation

The shift register's output is not designed for driving a pulse transformer coupled thyristor's gate. The duration of the register's output must be limited to prevent saturation of the transformer core. Consequently, external circuitry was needed to convert the positive output of each shift register into a small $\approx$ 50ns TTL pulse[1]. Pulse formation was achieved by passing the register's output through a high pass RC filter. These filters "edge detect" transitions in the shift register's output. Each step transition results in an exponential decay that drives a F365 Buffer. The exponential decay causes the output to go high until the decaying input falls below the V_{IH} threshold of the buffer. The result is a short duration pulse, whose width is controlled by changing the RC time constant of the filter.

Unfortunately, the high pass filter is sensitive to both negative and positive transitions of the shift register's output. This means that negative exponentials are also driving the TTL buffers after the register is cleared. To prevent possible jitter that might occur as the buffer's internal clamp circuitry attempts to protects the input, the buffer output is disabled and placed in a high impedance state prior to the register being cleared.

[1]Because this pulse duration is orders smaller than the firing period, T_{555}, no additional circuitry for core reseting was needed.

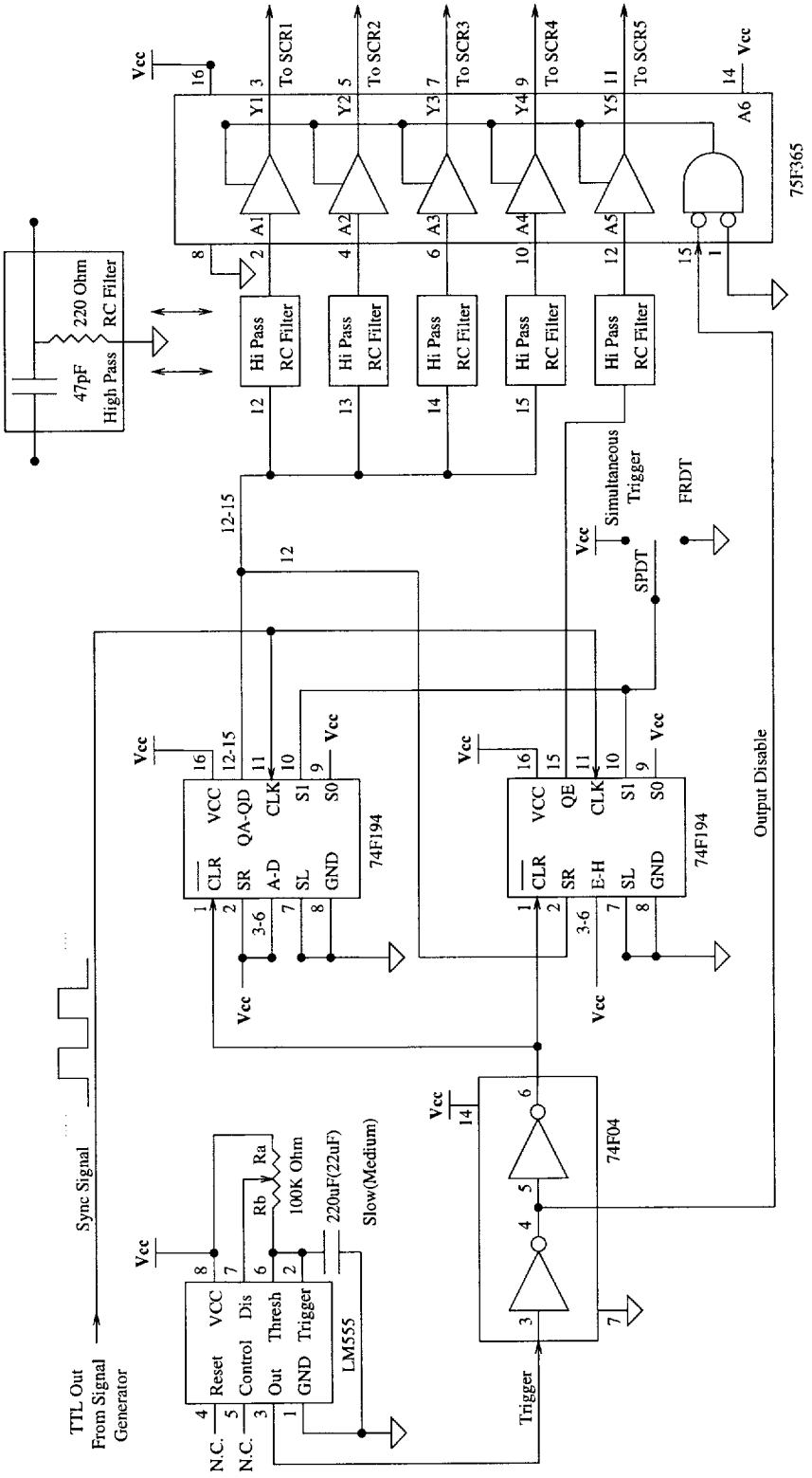
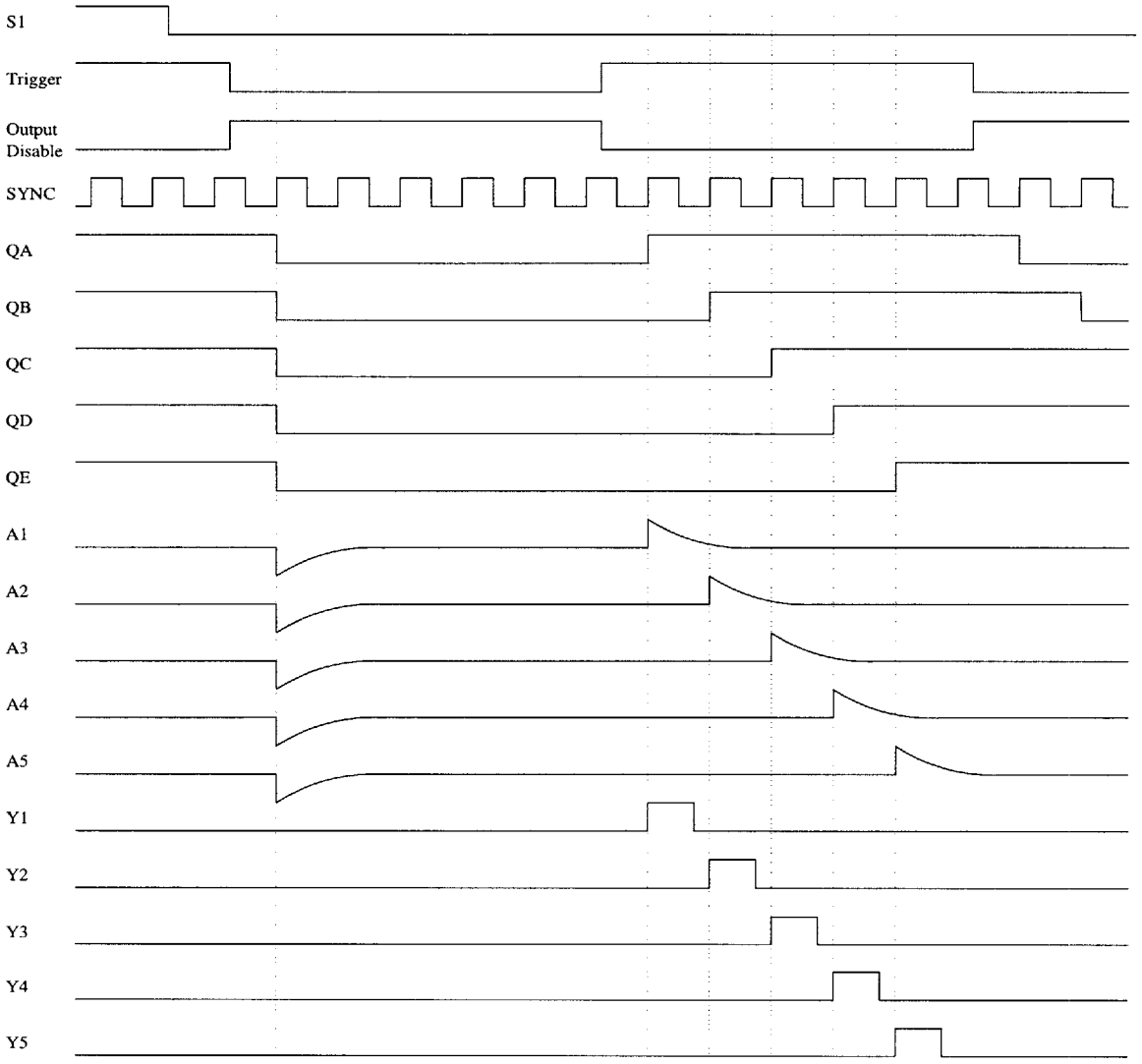


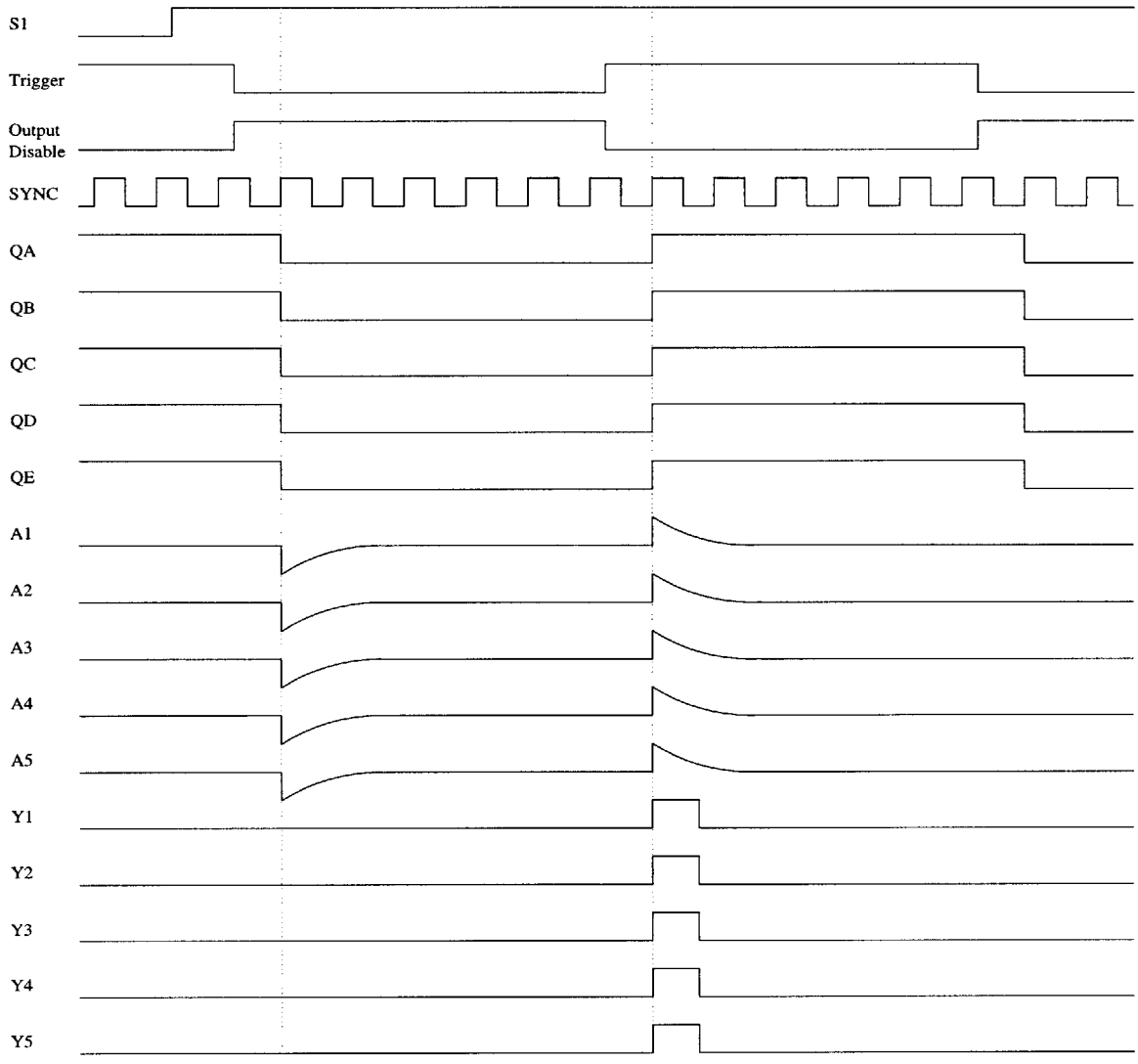
Figure E-1: TTL Trigger Circuit Schematic

E.2 Timing Diagrams



Not To Scale

Figure E-2: Fixed Inter-switch Delay Triggering



Not To Scale

Figure E-3: Simultaneous Triggering

Appendix F

Additional Information

F.1 GA301A Thyristor Switch

F.2 PE-64973 Pulse Transformer

GA301A

PartID: 6785 | Rev: 9/12/98
SearchPage | Datasheet | Watertown

- Package: TO-18 (STD-Thru Hole)

Silicon Controlled Rectifier

0.2 Amps

100 Volts

Maximum Ratings and Electrical Characteristics

Property	Symbol	Value	Unit
Average On-State Current	IT (Av)	0.2	Amps
Peak On-State Voltage	VTM	1.5	Volts
Holding Current	IH	5	mAmps
Gate Trigger Voltage	VGT	0.75	Volts
Gate Trigger Current	IGT	200	uAmps
Turn-Off Time	tq	500	nsec
Reverse Blocking Voltage	Vrrm	100	Volts
Gate Trigger-On Pulse Width	tpg(on)	0.05	usec

Mechanical Characteristics

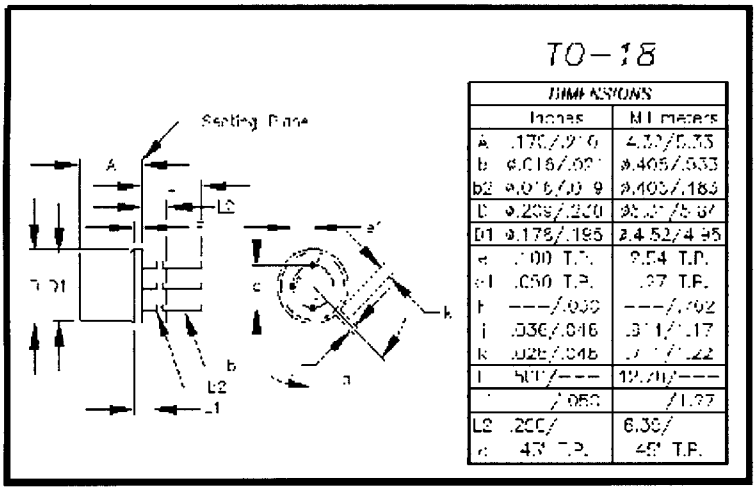
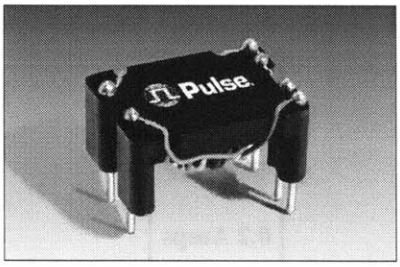


Figure F-1: GA301 Thyristor Information

500 KHz GATE DRIVE TRANSFORMERS

Pulse
A TECHNITROL COMPANY



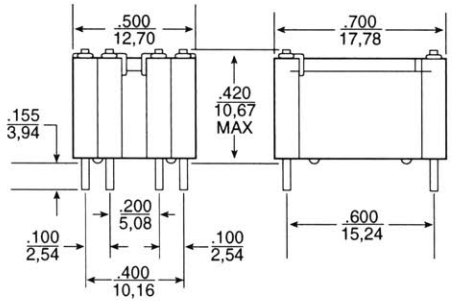
- Designed and optimized for 500 KHz
- Low leakage inductance and fast rise time
- 1500 VRMS isolation

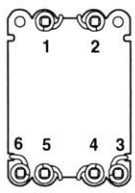
Electrical Specifications @ 25°C — Operating Temperature -30°C to 130°C

Part Number	Turns Ratio (±5%)	OCL PRI[1] (µH MIN)	Leakage Inductance[1] (nH MAX)	DCR Drive Winding (Ω MAX)	DCR Gate Winding (Ω MAX)	Cww[1] Drive To Gate (pf MAX)	Cww[1] Gate To Gate (pf MAX)
PE-64972	1:1:1	70	180	0.05	0.05	5.0	5.0
PE-64973	1:1	70	180	0.05	0.05	5.0	NA

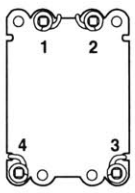
Note: 1. @ 500 KHz, 0.02 V

Mechanicals



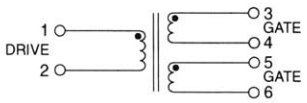


PE-64972

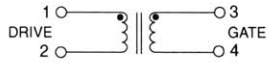


PE-64973

Schematics



PE-64972



PE-64973

Dimensions: Inches / mm

Unless otherwise specified, all tolerances are ± .010 / 0,25

Figure F-2: PE-64973 Pulse Transformer Information

Appendix G

PE-64973 Pulse Transformer Characterization

G.1 Transformer Testing

The response of the PE-64973 was examined for short 50ns pulses of 5 Volts amplitude. The pulses were transmitted through a one meter RG-178 coaxial cable that connects with the primary of a pulse transformer. Three different loading cases using the test circuit in Figure G-1 were considered:

1. R_{pri}=∞, R_{sec}=51Ω
2. R_{pri}=51Ω, R_{sec}=∞
3. R_{pri}=51Ω, R_{sec}=51Ω

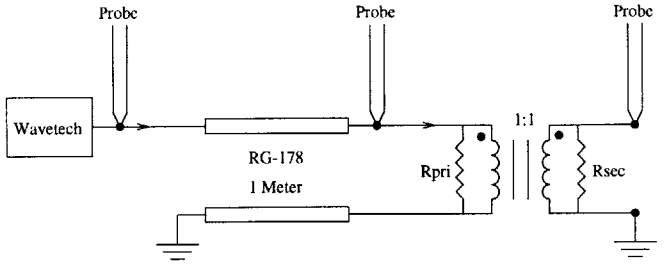


Figure G-1: PE-64973 Test Circuit

G.2 Transformer Responses

Figures G-2 through G-4 show cases 1 to 3 respectively. In case 1, the transformer is driving a 51Ω load resistor at the secondary. It is clear from the waveforms that there is approximately a 2ns delay from 50% of the input to 50% of the output. In addition, it can be seen that some of the higher frequencies of the pulse are being lost in transmission because the rise time at the secondary is slower. For case 2, the secondary is open circuited, and instead the primary is terminated with a resistor to minimize reflections. In this case the delay to 50% is only about .5ns and the higher order frequencies are better preserved. The reason for this is that the output is no longer dominated by a noticeable $\frac{L}{R}$ time constant as before. In the final case, both the primary and secondary are loaded. The delay and rise time here are similar to those seen in case one. The only major difference is that the amplitude has been halved, because the equivalent resistance seen by the transmission line is closer to 25Ω now.

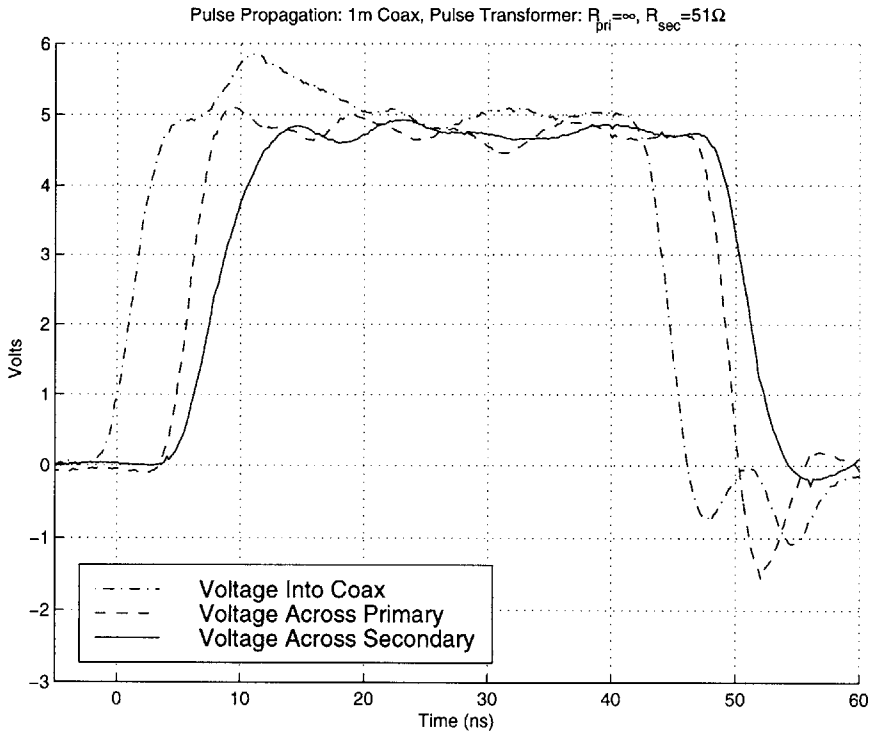


Figure G-2: Pulse Propagation: 1m Coax, Pulse Transformer: R_{pri}=∞, R_{sec}=51Ω

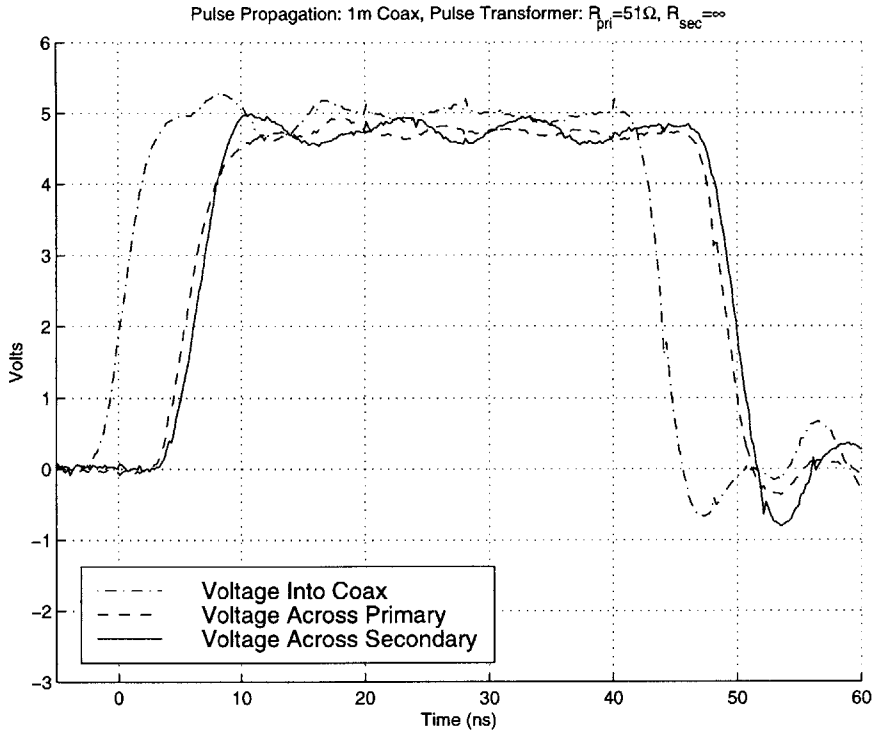


Figure G-3: Pulse Propagation: 1m Coax, Pulse Transformer: R_{pri}=51Ω, R_{sec}= ∞

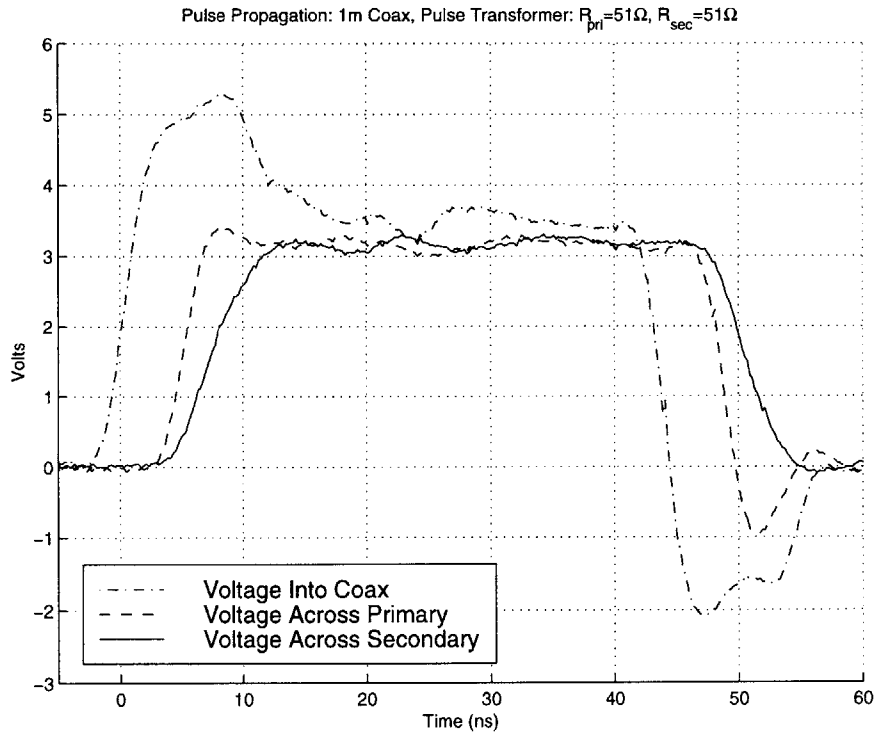


Figure G-4: Pulse Propagation: 1m Coax, Pulse Transformer: R_{pri}=51Ω, R_{sec}=51Ω

Appendix H

GA301 Device Characterization

H.1 Trigger Scheme Testing

The 10% to 90% rise time and delay from 50% of the input to 50% of the output behavior of a typical GA301 thyristor were characterized for six different triggering schemes as a function of V_{AK} over the range: 5 Volts $\leq V_{AK} \leq$ 100 Volts. Data points were obtained using the automated measurements of a Tektronix, TDS540A oscilloscope on the test circuit given in Figure H-1. Both the TTL circuit in Appendix E as well as a Wavetech pulse generator were used as drives in these tests.

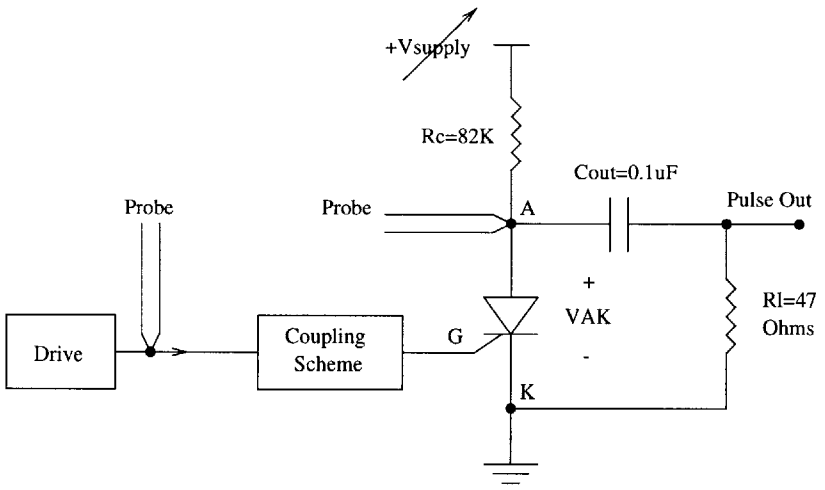


Figure H-1: GA301 Test Circuit

H.2 Measured Data

The following six plots illustrate the rise time and delay behavior of a typical GA301A. Figure H-2 shows the results for a TTL drive that is resistively coupled to the thyristor gate. Figures H-3 through H-5 display the effects of coupling through a pulse transformer when the secondary has different series impedances into the thyristor gate. In Figures H-6 and H-7 a Wavetech pulse generator is used instead of the TTL drive, and the signal is now coupled through different coaxial cable schemes into a corresponding pulse transformer. For these two cases, the primary has a 51Ω resistor in parallel with it to terminate the line, while the secondary is tied directly to the gate.

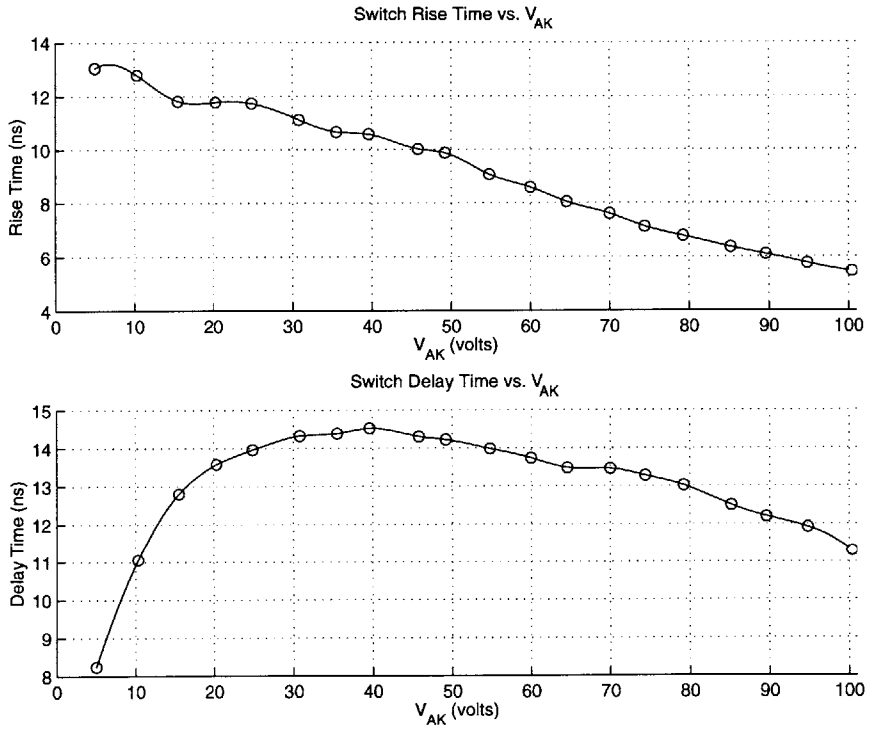


Figure H-2: TTL Drive, R_g=51Ω

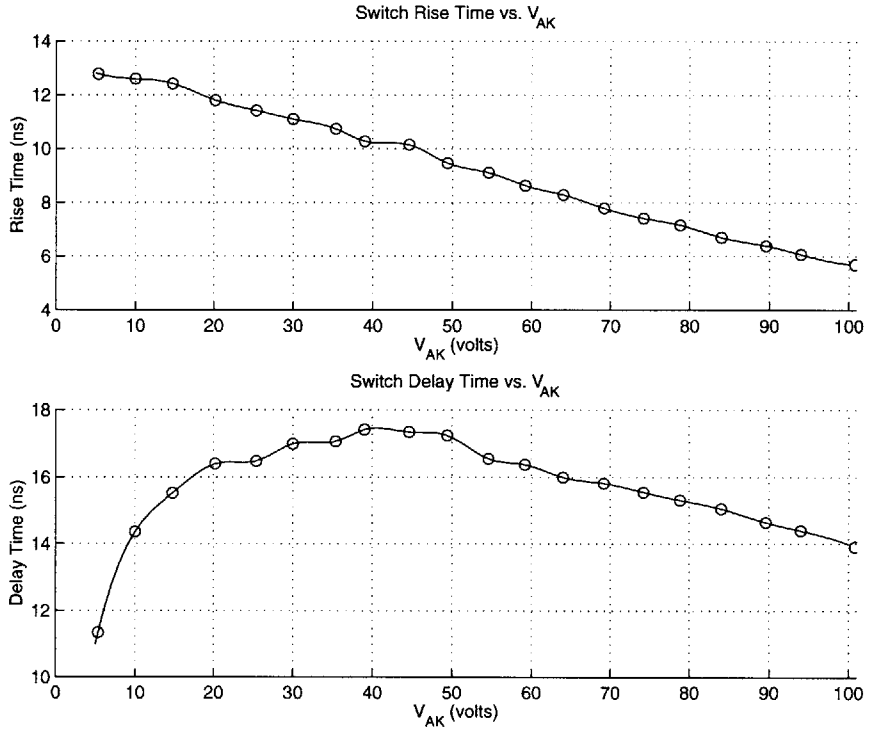


Figure H-3: TTL Drive, Pulse Transformer, R_g=51Ω

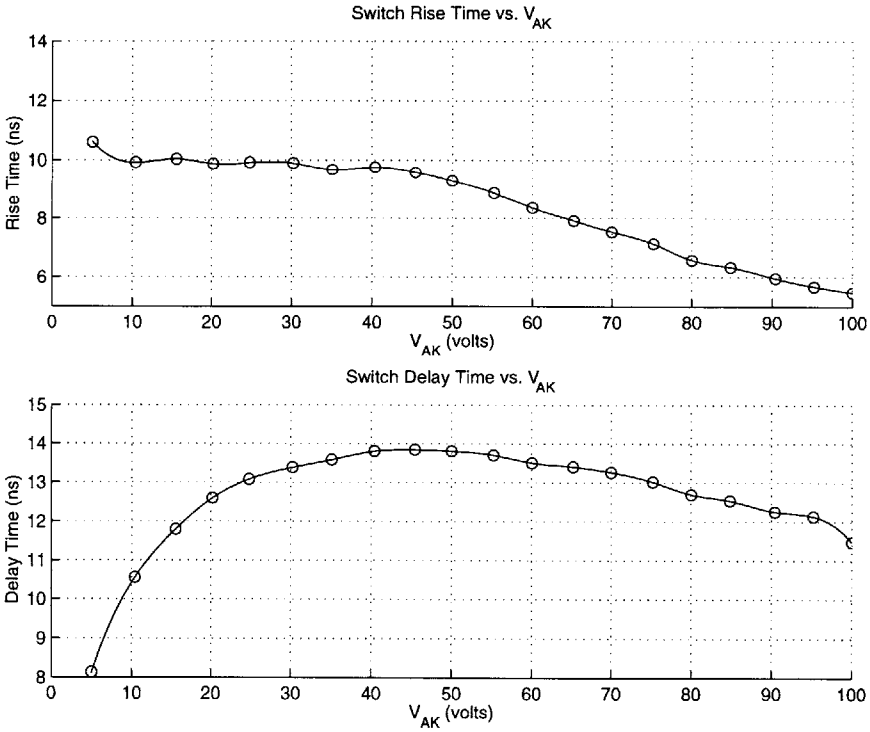


Figure H-4: TTL Drive, Pulse Transformer, R_g=51Ω||C_g=0.1μF

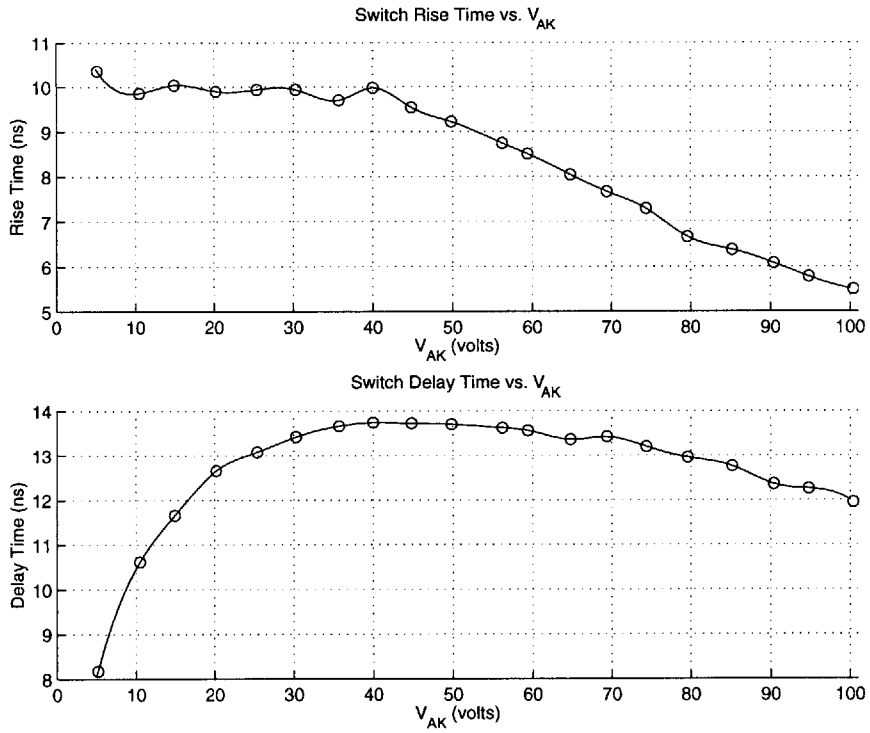


Figure H-5: TTL Drive, Pulse Transformer, R_g=0Ω

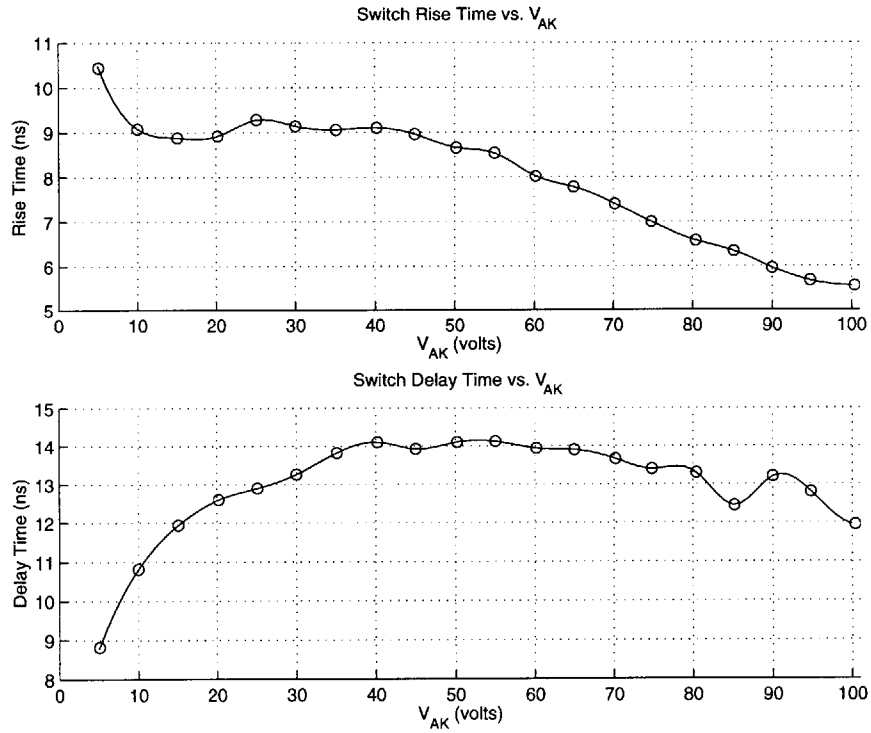


Figure H-6: Wavetech, 1m coax, Pulse Transformer$||R_{pri}$=51Ω, R_g=0Ω

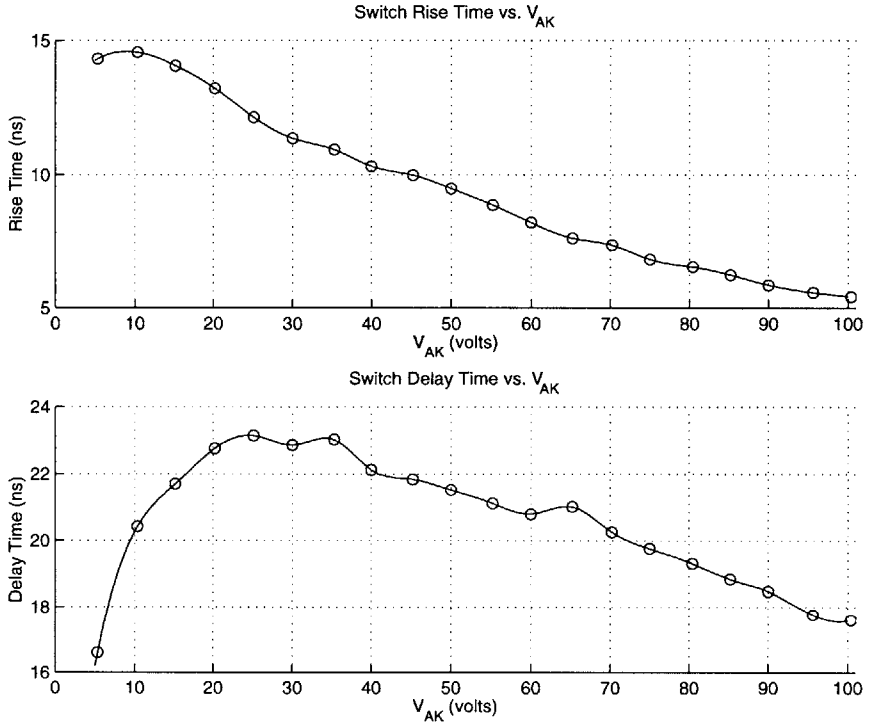


Figure H-7: Wavetech, 5 || 10cm coaxes, Pulse Tranformer||R_{pri}=51Ω, R_g=0Ω

References

[1] Microsemi Corp. Design note #14: Nanosecond scr switch for reliable high current pulse generators and modulators.

[2] Microsemi Corp. *Semiconductor Data Book.* Watertown, MA, 1994c.

[3] Tom Dhaene and Daniel De Zütter. Selection of lumped element models for coupled lossy transmission lines. *IEEE Trans. on Computer-Aided Design*, 11(7):805–815, Jul 1992.

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[7] Jin Au Kong, Ann W. Morgenthaler, and David H. Staelin. *Electromagnetic Waves.* Prentice Hall, 1994c.

[8] K. A. Schmidt and G. L. Wilson. Transmission line models for switching studies:design criteria ii. selection of section length, model design and tests. *IEEE Trans. Power App. Syst.*, PAS-93:389–395, Jan/Feb 1974.

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