Chip-Scale Modeling of Pattern Dependencies in Copper Chemical Mechanical Polishing Processes

by

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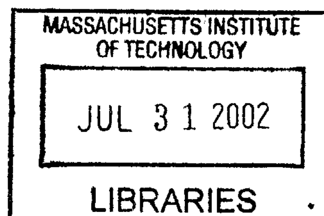
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Abstract

Chemical mechanical polishing (CMP) has become a necessary processing step in the fabrication of copper interconnects. Copper CMP is recognized to suffer from pattern dependent problems such as dishing and erosion, which cause increased line resistance and non-uniformity within the die. The non-uniformity on one metal level can lead to cumulative non-uniformity on higher metal levels, leading to potential integration and manufacturing problems. Predictive pattern dependent models of copper CMP processes are therefore highly desirable for predicting dishing and erosion on random layouts, assessing the effectiveness of dummy fills in minimizing within-die non-uniformity, aiding in the generation of smart interconnect design rules, and identifying potential bulk copper clearing problems in multi-level metallization designs.

In this thesis, the first predictive semi-physical chip-scale pattern dependent model for copper CMP processes is developed. A comprehensive model calibration methodology for any multi-step copper CMP process is also developed. The model takes into account the initial long range electroplated topography, the effective pattern density, and the initial local step heights within the arrays. The model also accounts for the temporal evolution of the bulk copper thickness during CMP, the temporal evolution of dishing and erosion, and the layout dependencies of dishing and erosion. A three step conventional copper CMP process experiment and a single step abrasive-free copper CMP process experiment are performed to test the accuracy of the model and the calibration methodology. The results show that the model predicts the trends in the experimental data accurately, and fits the data to within acceptable errors.

The model and the calibration methodology are integrated with an empirical pattern dependent electroplating model and calibration methodology, to form a chip-scale copper electroplating and CMP simulator. Once the models that form the simulator are calibrated for a given copper CMP process, and a given copper electroplating process, the simulator can be used to: (1) predict dishing and erosion across an entire chip, for a random layout; (2) assess the effectiveness of dummy fills in minimizing within-die non-uniformity; (3) identify bulk copper clearing problems in multi-level metallization designs; and (4) aid in the generation of smart interconnect design rules. Preliminary experimental results show that the simulator predicts dishing and erosion across an entire chip reasonably well, for a random layout.

Thesis Supervisor: Duane S. Boning
Title: Associate Professor of Electrical Engineering and Computer Science

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Chapter 1

Introduction

As critical dimensions shrink aggressively into the deep submicron regime, interconnect delay, reliability, and manufacturability are becoming major issues in ultra large-scale integrated circuit (ULSI) design and fabrication. Aluminum has been the metal of choice for interconnects for more than three decades, while silicon dioxide has been the inter-level dielectric (ILD) of choice in multi-level interconnect systems. The inherent high resistivity of aluminum and the high permittivity of silicon dioxide cause very high interconnect delay in the deep submicron regime, as illustrated in figure 1.1 [1]. In addition, aluminum has a low electromigration resistance, and poses a difficult etching problem in the deep submicron regime. In an effort to reduce interconnect delay, and improve interconnect reliability, the semiconductor industry is replacing aluminum with copper, and aggressively looking for a lower permittivity material to replace silicon dioxide. Copper has a much lower electrical resistivity and a higher electromigration resistance compared to aluminum [1].

Unlike aluminum, copper is difficult to pattern with a subtractive RIE process. Instead, copper requires a damascene process, which can either be single or dual. In a single damascene process, ILD is deposited and patterned to define trenches where the copper lines or copper vias will lie. A very thin barrier layer (Ta, TaN, Ti, or TiN) is then deposited typically by PVD, followed by the deposition of a thin seed layer of copper by PVD. After the deposition of the seed layer, a thicker copper film is deposited by electroplating. The barrier layer prevents the copper film from diffusing into the dielectric and the silicon substrate, and it also serves as an adhesive

for the copper film. The thin seed layer also serves as an electrically conducting surface for electroplating to be carried out. Ultimately, chemical mechanical polishing (CMP) is used to remove the bulk or overburden copper, and the barrier on top of the ILD in the spaces between the copper lines. The process flow for a single damascene process is illustrated in figure 1.2. The main difference between single damascene and dual damascene processes is that in dual damascene processes, interconnect lines on a particular level and the vias connecting them to lower level interconnects are formed at the same time. Thus, the number of CMP steps performed in dual damascene processes is less than that performed in single damascene processes.

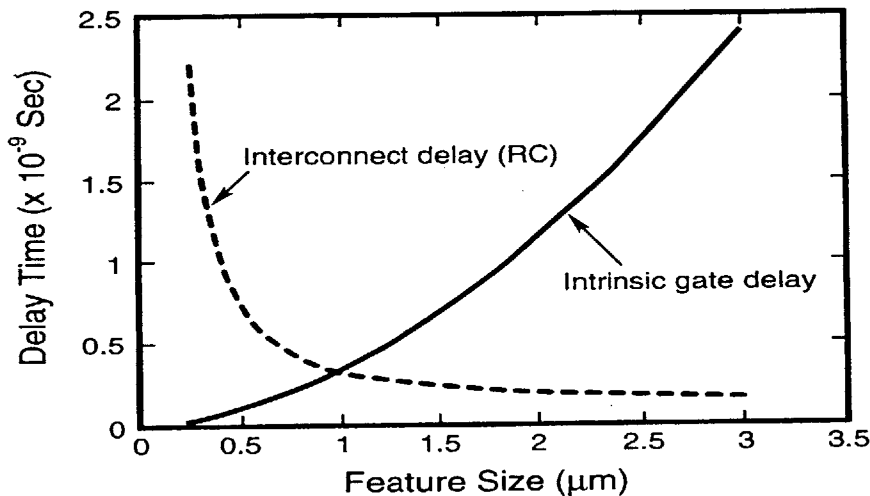


Figure 1.1: Delay versus feature size (from [1])

Copper CMP is known to suffer from pattern dependent problems such as dishing and erosion, which lead to increased line resistance and within die non-uniformity. Dishing and erosion on a given metal level could lead to cumulative non-uniformity on higher metal levels, which might cause integration, yield, and manufacturing problems. There is an urgent need for an accurate and efficient predictive chip-scale model of dishing and erosion for copper CMP processes. In this thesis, such a model is developed, and it is used to form the backbone of a chip-scale copper CMP simulator.

This chapter briefly discusses pattern dependent issues in copper CMP. Section 1.1 gives a brief description of the CMP process in general, and section 1.2 deals with copper CMP processes. Section 1.3 discusses the thesis goals, and section 1.4 describes the thesis organization.

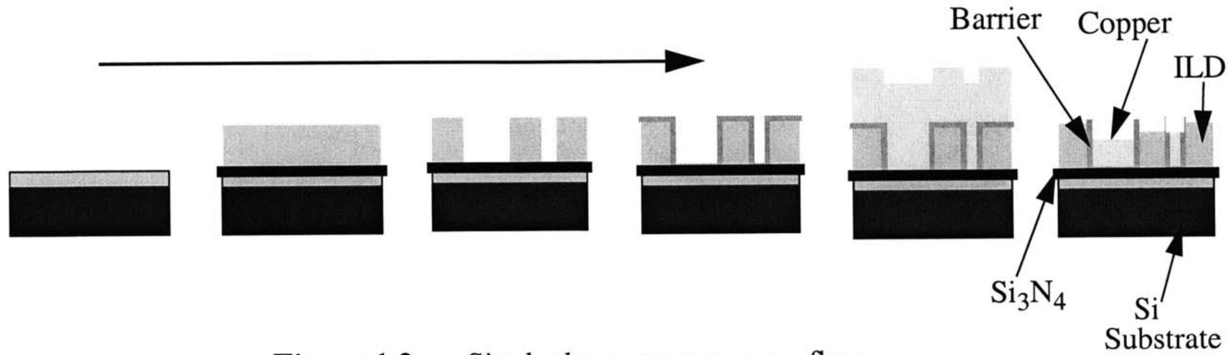


Figure 1.2: Single damascene process flow

1.1 Chemical Mechanical Polishing (CMP) Processes

CMP is a complex process with a large number of variables. In CMP a wafer is held face down by a carrier and pressed into a platen that is covered with a polyurethane material known as the pad. The platen and carrier move relative to each other, in a rotary, linear or orbital fashion, with the motion type categorizing the tool (linear tools, orbital tools, and rotary tools). A slurry containing a combination of chemicals, fluids, and abrasive particles is deposited on the pad during polishing. Over time, the pad surface becomes glazed, resulting in a decrease in the polish rate. To minimize this effect during the effective lifetime of the pad, a diamond-tipped conditioning head is often used to scratch the surface of the pad to expose a fresh pad surface during polishing.

Rotary CMP tools are the most common in the industry. For such tools, the platen and carrier are circular, and they both rotate in the same direction, but about different centers as shown in figure 1.3. The axis of rotation of the carrier changes from time to time during the polishing.

The Applied Materials Mirra-Mesa and the SpeedFam-IPEC 472 are examples of rotary tools available in the market. Orbital and linear tools also exist, although they are less common. In linear tools, the carrier rotates in the x-y plane, while the pad is setup like a belt that moves linearly in the x-direction. The LAM Research Terres is an example of a linear tool, and a simplistic version of it is illustrated in figure 1.5 [2].

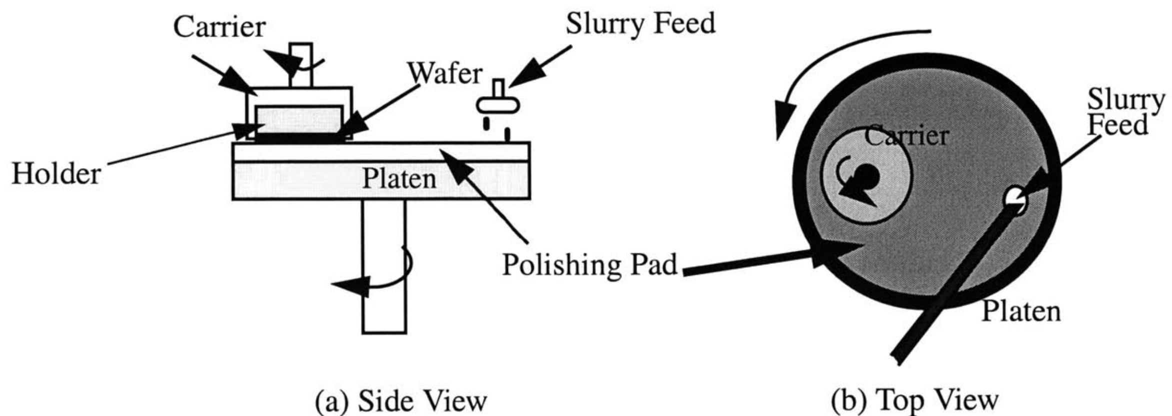


Figure 1.3: A sample rotary CMP tool

CMP is widely used for the planarization of inter-level dielectrics (notably silicon dioxide), the planarization of bare silicon wafers, and in the formation of shallow trench isolation (STI). It has also become a critical process in the formation of tungsten studs/vias, the formation of copper interconnects, and in the polishing of other materials [1, 3]. Despite the increased use of CMP in the semiconductor industry, the fundamental mechanisms involved in the process remain a topic of much debate. Generally, the chemicals in the slurry react with the work piece to form a modified surface film, which is abraded by the pad and the abrasive particles. The abraded or dislocated portions of the work piece are either dissolved in the slurry, or swept away by its turbulent motion [1, 4, 5]. What is clear, however, is that the mechanical action exerted the pad (directly or indirectly) largely determines the evolution of pattern features during polishing.

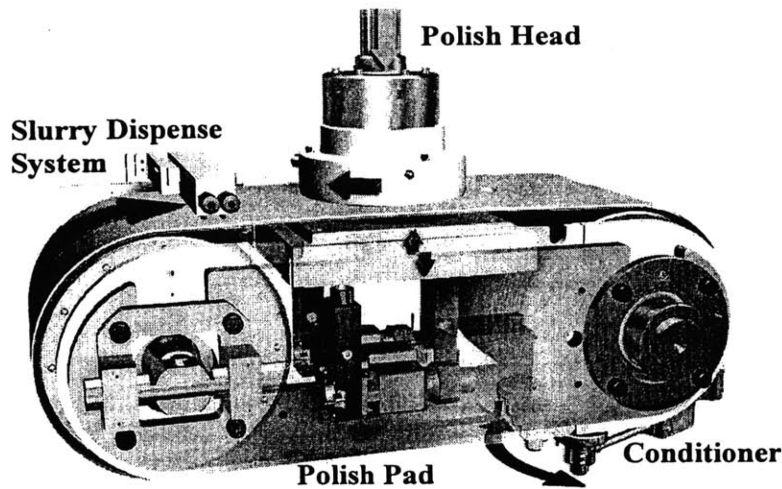


Figure 1.4: A simplified version of the Lam Teres (from [2])

1.2 Copper CMP Processes and Issues

Copper CMP has been described as a heterogeneous CMP process because it involves the simultaneous polishing of multiple materials: copper, dielectric and barrier [6]. In this sense, it is similar to other metal CMP processes and STI CMP processes, but very different from and more complex than dielectric CMP processes which only involve the polishing of one material. In copper CMP, we want to clear the overburden copper and remove the barrier on top of the dielectric spaces separating the copper interconnect lines. This is essential to avoid shorts between adjacent interconnect lines. The heterogeneous nature of the process necessitates using a consumable set and choosing polish process parameter settings that achieve specific relative removal rates for the different materials.

Copper CMP is known to suffer from pattern dependent problems such as dishing and erosion, as illustrated in figure 1.5. Dishing is defined as the difference between the height of the copper in the trench, and that of the dielectric in the spaces surrounding the copper trench in question. If the height of the copper in the trench is lower than the height of the neighboring

dielectric, then dishing is positive. When dishing is negative, the copper interconnect sticks-up above the neighboring dielectric level. Erosion on the other hand, is defined as the difference between the dielectric thickness before CMP and that after CMP. Hence, it is the loss in dielectric thickness during CMP, and it is always positive. The sum of dishing and erosion gives the copper

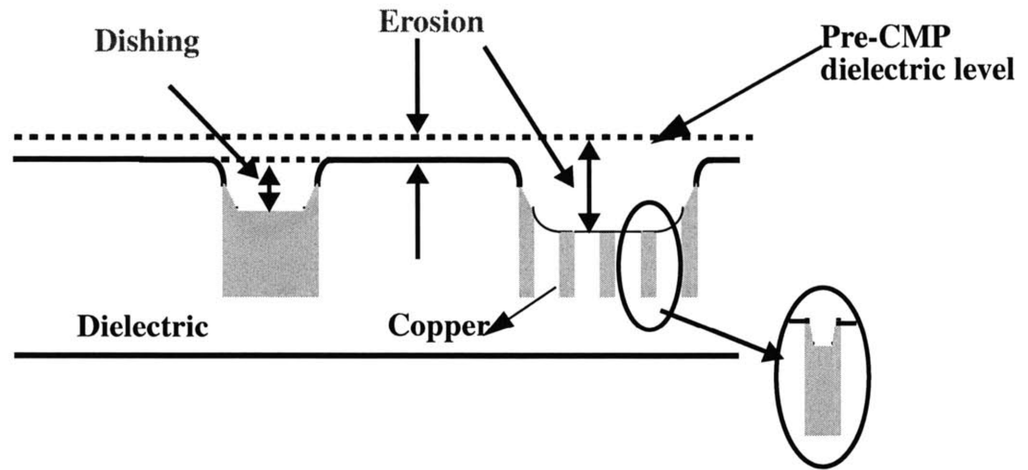


Figure 1.5: Definition of dishing and erosion

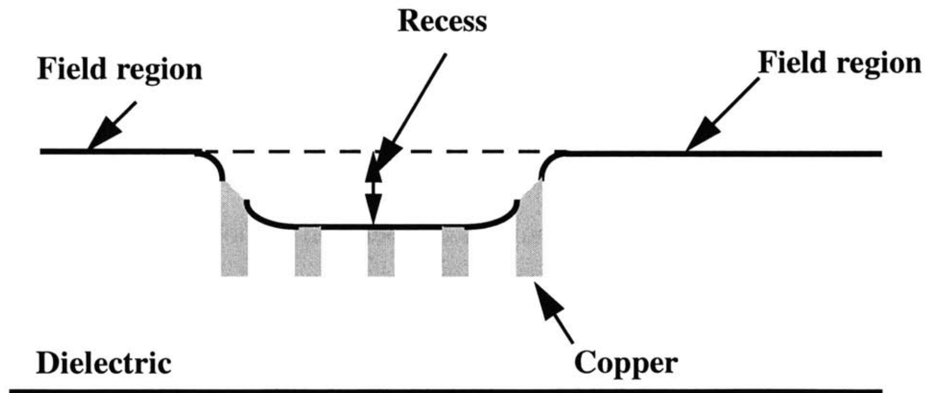


Figure 1.6: Definition of recess

thickness loss (also known as the copper thinning) during CMP. Note that in the published literature, erosion is sometimes referenced to the height of a neighboring field dielectric region, and a separate "field dielectric loss" parameter is then specified. In this thesis, a single dielectric

erosion term is used to represent dielectric loss everywhere, as this is found to be more amenable to modeling use.

Recess is another term that is often used to describe pattern dependent problems in copper and other metal CMP processes. The recess of a copper line is the same as the dishing of that line. The recess of the dielectric in an array of lines is the difference between the dielectric height (at the location of interest) and the height of the dielectric field surrounding the array. In this thesis, recess represents the height of the field surrounding an array minus the height of the location of interest within the array of lines, as illustrated in figure 1.6.

Dishing and erosion depend on layout patterns (line width, line space, and pattern density), the polish process settings (down force, table speed, and slurry flow rate), the consumable set used, the overpolish time, and the incoming electroplated topography [7-11]. The incoming electroplated topography in turn depends on the layout patterns, thereby making the dependency of dishing and erosion on layout patterns a complex one [12]. In addition, dishing and erosion on metal level one could lead to increased dishing, erosion and surface non-uniformity on metal level two as illustrated in figure 1.7 [13]. This effect could worsen on higher metal levels and could lead to uncleared copper residue, shorts between adjacent interconnect lines, and photolithographic problems. Thus, it has the potential of causing yield, integration and manufacturing problems. To minimize the problem of cumulative non-uniformity, the inter-level dielectric is often planarized using CMP, before any new interconnect level is defined. This increases the number of processing steps and the cost of the process.

In an effort to minimize dishing, erosion, and within die non-uniformity, while maintaining a relatively high throughput in copper CMP, copper CMP processes have evolved from single step processes to multi-step processes. In a single step process, a single slurry, pad,

and a single set of polish process parameters (down force, table speed, and slurry flow rate) are used until the overburden copper and the unwanted barrier are cleared. With such a process, it is difficult if not impossible to minimize dishing and erosion, while maintaining a high throughput. Minimizing dishing and erosion for such a process requires the selectivity of the removal rates (copper, barrier, and dielectric rates) to be ideally 1:1:1, and for the absolute removal rate (which is then approximately equal for the three materials) to be reasonably low. The 1:1:1 selectivity

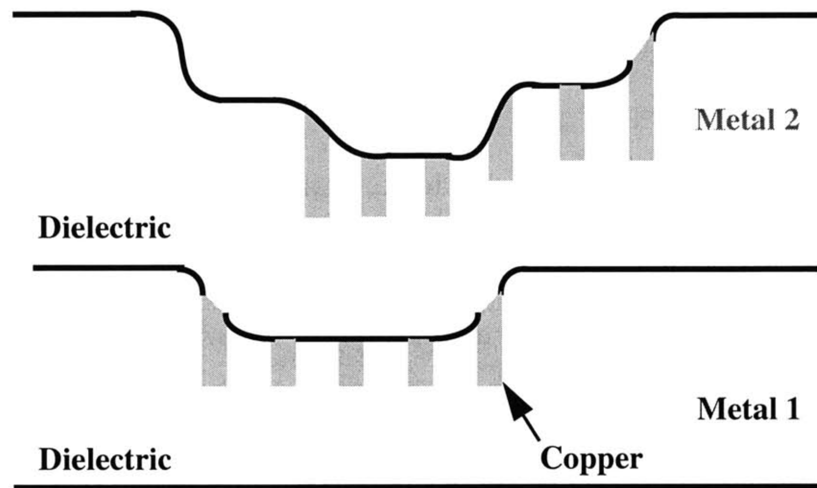


Figure 1.7: Cumulative non-uniformity effect

ensures that dishing is equal to zero (assuming that the step heights in the overburden copper are eliminated before the overburden copper is completely cleared), while the low material removal rate ensures that the erosion is kept to a minimum during overpolishing. Overpolishing is unavoidable because of pattern (density, line width and line space) differences across the die, and deposited copper thickness and CMP process non-uniformities across the wafer.

High throughput, on the other hand, requires a high copper removal rate in order to remove the overburden copper quickly, and a reasonably high barrier removal rate in order to clear the barrier in the spaces between the interconnect lines quickly. Hence, the requirements for high throughput and those for minimum dishing and erosion are in conflict. Single step processes that

were typically used in the early days of copper CMP had reasonably high copper removal rates (5000 - 8000 Å/min), with barrier and dielectric rates in the range 100 - 1000 Å/min [6]. Such processes led to high erosion and dishing when significant overpolishing was required to clear the overburden copper and the unwanted barrier across the entire wafer.

Multi-step copper CMP processes use different consumable sets and different polish process parameter settings at different stages during the polishing process. End-point detection is vital to the successful execution of such processes. In a two step polish process, a high copper removal rate process is used to clear the copper overburden in the first step, while the second step is geared towards removing the unwanted barrier across the wafer. A low selectivity process with moderate removal rates (500 - 1000 Å/min) is used in the second step. The end-point detection algorithm set by the CMP engineers dictates when to switch from step one to step two. Typically this occurs when sufficient barrier material has been exposed across the wafer. Non-uniform copper thickness deposition across the wafer, non-uniform copper removal rates across the wafer, and within die pattern differences lead to the need for overpolishing in the first step. This translates to substantial dishing and erosion. The dishing in the first step could be reduced during the second polish step, if a slurry that removes dielectric faster than copper is used in the second step. The disadvantage of this dishing reduction mechanism is that it might lead to negative dishing (i.e. the copper lines sticking above the dielectric level) for very fine features, and this could cause potential yield and integration problems.

The inability of a two-step process to minimize dishing and erosion while maintaining a high throughput, has led to the adoption of a three step and sometimes (although rarely) a four step polish process. Three step or four step processes require a CMP tool with three or more platens and sophisticated end-point detection for high throughput and minimum defects. In a three

step polish process, the first step uses a highly selective copper removal rate process with a high copper removal rate (typically above 8000 Å/min) to remove a large amount of the overburden copper without completely clearing it. The aim is to remove most of the overburden copper quickly, while leaving the remaining overburden film highly planarized. An end-point detection technique that directly or indirectly measures the copper thickness remaining on the wafer during polishing is needed in the first step. This step is typically stopped when a particular thickness of copper overburden remains on average across the wafer.

The second step is intended to clear all overburden copper residue across the wafer, while achieving low dishing and erosion. In this step, a low removal rate copper process with relatively low removal rate selectivity compared to the step one process is used. This step typically uses the same type of slurry and the same type of pad as those used in step one. However, the polish process settings (down force, table speed, and slurry flow rate) are different from those used in step one. It is commonly known as a soft landing step because of the low down force used. In addition, the end-point technique used in this step is different from that used in step one; rather than stop at a target copper thickness, this end-point is typically based on optical reflectance to detect clearing on the wafer surface.

In step three, a different polish process setting, a different type of slurry, and possibly a different type of pad is used. The process is typically a low selectivity process, with low removal rates for copper, barrier and dielectric. No end-point detection is required in this step. Instead a fixed time polish is done with the time determined based on knowledge of the barrier removal rate and the non-uniformity of the process in general. Negative dishing often occurs for fine features after this step because the dielectric removal rate may be slightly higher than the copper removal rate.

Apart from dishing and erosion, other issues in copper CMP (not necessarily pattern dependent) include corrosion, scratching and particulate contamination. Scratching can be caused by large abrasives in the slurry or some of the diamond particles that come off the conditioning wheel. To minimize scratching caused by large abrasive particles, filters are used to remove such particles from the slurry. Copper corrosion is a chemical phenomena, and is primarily due to the reaction of the chemicals in the slurry with the copper metal, or reactions of chemicals in the cleaning solution with the copper metal during CMP clean [1]. To minimize corrosion, the copper metal should be passivated. Adding BTA to the slurry is one way of achieving this [1]. Particulate contamination occurs when particles remain on the wafer after CMP, and can lead to yield and reliability problems.

In an effort to minimize dishing, erosion, scratches from abrasive particles, and other defects in copper CMP, CMP consumable vendors in collaboration with tool companies and IC manufacturers are formulating an abrasive-free slurry that can be used with conventional polishing pads, in what has been termed abrasive-free polishing or AFP. These slurries do not necessarily exhibit the same polishing relationships as conventional CMP slurries with abrasives. For instance, the Hitachi C-430 exhibits a non-linear relationship between copper removal rate and polishing pressure [14 - 16]. Preliminary experiments with this slurry show great promise in significantly minimizing dishing and erosion, while achieving a copper removal rate as high as 6000 Å/min [14 - 16].

1.3 Thesis Goals

To fully get the benefits of replacing aluminum with copper, dishing and erosion must be minimized. Minimizing dishing and erosion requires an understanding of the layout and process

dependencies involved in copper CMP, and the ability to accurately predict the dishing and erosion first across an entire die, and ultimately across an entire wafer, for any given process. In this thesis, a semi-physical chip-scale pattern dependent modeling and characterization methodology for copper CMP processes is developed. Specifically, the primary goals of the thesis are as follows:

1. Identify the layout and process parameter dependencies in copper CMP, through experimentation with specially designed test masks.
2. Use experimental data and physical principles to develop a semi-physical model that captures the pattern (topography) effects. The model should predict the evolution of the overburden copper removal and the dishing and erosion for multi-step copper CMP processes.
3. Develop a methodology for rapidly calibrating the model for multi-step copper CMP processes.
4. Develop a general chip-level simulator for copper CMP processes based on the model equations. The simulator should predict dishing, erosion, and copper overburden thickness evolution for random layouts.

1.4 Thesis Organization

The thesis is divided into eight chapters. Chapter 2 shows the framework of the modeling and characterization methodology used in this work. First, some of the input and output parameters of a typical copper CMP process are shown to illustrate the complexity of modeling the process. Second, a literature review of currently available copper CMP models is presented. This is followed by a discussion of our approach to modeling and characterizing pattern dependencies in copper CMP processes.

Chapter 3 describes the density-step-height model for single step Prestonian copper CMP processes. First, the model is formulated, and the model calibration methodology is described. A design of experiment is performed and the model calibration methodology is applied to see how well the model fits the experimental data. This is followed by a discussion of some of the limitations of the model, and suggestions for rectifying them.

In chapter 4, the framework of the density-step-height model is applied to non-Prestonian copper CMP processes. Specifically, a density-step-height model is formulated for single step abrasive-free copper CMP processes, and tested against experimental data.

Single step copper CMP processes are now rare, and have been replaced with multi-step copper CMP processes. A multi-step copper CMP process uses different consumable sets (pads and slurries) and different polish process settings (down force, table speed, and slurry flow rate) in different phases of the copper CMP process. The density-step-height modeling framework is applied to multi-step copper CMP processes in chapter 5. An extensive three step copper CMP process experiment is conducted, and used to test the accuracy of the formulated multi-step copper CMP model.

Current bottom-up fill electroplating techniques introduce long range height variation that the density-step-height model fails to take into account. By failing to take this effect into account, the density-step-height model incorrectly assumes that the polishing pad initially contacts all up-areas with non-zero pressure. To rectify this, an integrated contact mechanics and density-step-height model is formulated in chapter 6. Contact mechanics takes into account any long range wafer surface height variation, in computing the polish pressure at all points of interest within the die. Once the pressure is computed, the density-step-height formulation is used to compute the removal rates in the local up-areas and down-areas.

In chapter 7, the integrated contact mechanics and density-step-height model is incorporated into a chip-scale simulator, in conjunction with an empirical pattern dependent copper electroplating model. The simulator is used to predict the dishing and erosion performance of a calibrated copper CMP process on random layouts.

The thesis concludes in chapter 8 with a summary of the contributions, and an identification of future work.

Chapter 2

Framework for Modeling Pattern Dependencies in Copper CMP Processes

Copper CMP is a complex process with a large number of input and output variables, some of which are illustrated in figure 2.1. The development of a comprehensive model of this process is still several years away. In this chapter, a literature review of the currently available copper CMP models is presented in section 2.1, followed by a description of the framework of the modeling and characterization methodology developed in this thesis, in section 2.2. In section 2.3,

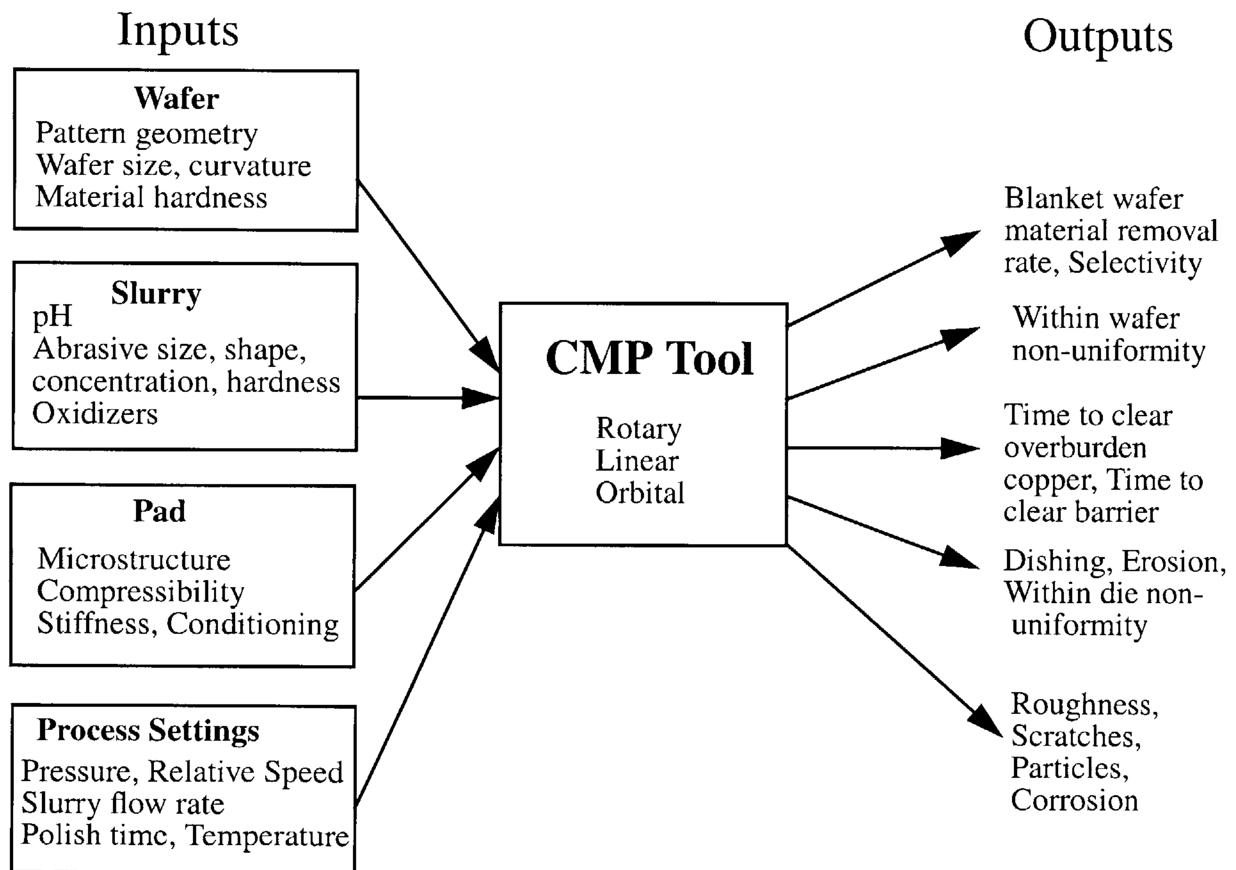


Figure 2.1: Copper CMP input and output variables

the test masks used in the model development are described, and in section 2.4 the metrology used in collecting experimental data is described. Finally, in section 2.5, the framework for characterization and prediction of dishing and erosion on random layouts is described briefly.

2.1 Literature Review of Copper CMP Modeling

There has been an explosion in the number of published papers on CMP modeling, in the last few years [17-19]. Only a few of these models deal with pattern dependent issues in copper CMP processes, and hardly any of them can be considered an efficient chip-scale model. In this section, the key copper CMP models that have been proposed and their limitations are discussed.

All the models proposed for copper CMP are based on Preston's glass polishing model [20]. According to that model, the polish rate at any position on the wafer is given by equation 2.1, where $\frac{\Delta H}{\Delta t}$ is the rate of change in material thickness over time Δt, K the Preston coefficient, L the applied load, A the contact area, and s the relative distance travelled between the pad and the wafer position in question. Quite often, equation 2.1 is written as in equation 2.2, where RR is the material removal rate, K the Preston coefficient, P the polish pressure, and V the relative speed

$$\frac{\Delta H}{\Delta t} = K\left(\frac{L}{A}\right)\left(\frac{\Delta s}{\Delta t}\right) \qquad \textit{(Equation 2.1)}$$

between the platen and the carrier. The Preston model assumes mechanical abrasion although chemical effect is known to aid polishing [20]. The chemical contributions are lumped in Preston's coefficient.

$$RR = KPV \qquad \textit{(Equation 2.2)}$$

Yang has developed a semi-physical model for copper CMP, based on Preston's equation

[21]. The model expresses the pressure in Preston's equation in terms of the compression distance of the pad, pad conformation, pad thickness, and pad elasticity. By assuming that the pad expands instantaneously as it moves from a high area to a low area, and that the relative change of compression distance is directly proportional to the relative change of the feature size, Yang derives the analytical expressions given in equations 2.3 and 2.4 for step-height and copper dishing. In these equations, h_s is the step-height, h_{so} the initial step-height, w the line width, w_o the effective minimum line width (which he assumes to be 0.01 mm), P the applied pressure, H the thickness of the pad, E the elasticity of the pad, V the linear velocity of the pad relative to the

$$h_s = h_{so} e^{\frac{-K_{Cu} E V t}{H}} + \frac{PH}{E}\left(\xi \ln\left(\frac{w}{w_o}\right) - 1\right)\left(1 - e^{\frac{-K_{Cu} E V t}{H}}\right) \qquad \textit{(Equation 2.3)}$$

$$h_D = \frac{(S-1)PH}{SE} \xi \ln\left(\frac{w}{w_o}\right)\left(1 - e^{\frac{-K_{Cu} E V t_1}{H}}\right) \qquad \textit{(Equation 2.4)}$$

wafer, S the removal rate selectivity of copper to the barrier material, ξ the pad conformity, K_{Cu} the Preston coefficient for copper, t_1 the elapsed time after the copper end-point, t the polish time, and h_D the copper dishing.

By further assuming that the copper is fully recessed below the ILD surface during the overpolish step, Yang derives the expression given in equation 2.5, for ILD erosion. The variable η is the pattern area coefficient (defined as the ratio of effective patterned area to measured patterned area), ρ the pattern density (defined as the ratio of copper line width to the pitch), W the

$$h_E = \eta\rho\frac{PH}{E}\xi\ln\left(\frac{W}{w_o}\right)\left(1 - e^{\frac{-K_{ox}EVt_1}{H(1-\eta\rho)}}\right) \qquad \textit{(Equation 2.5)}$$

width of the pattern array, and all the other parameters are as defined in equations 2.2 and 2.3.

The above dishing and step height equations do not have a pattern density or line space dependence. It has been found experimentally that dishing depends on both line width and pattern density or line space [7, 8]. Second, Yang does not explicitly show how to compute the time it takes to clear the copper overburden and the barrier film. Third, his assumption that the copper is fully recessed below the ILD during overpolish makes the model restrictive. Furthermore, he mentions that step height plays a role in determining when a pad touches a low area. However, the model equations do not account for this dependency. It has been shown experimentally that in cases where the step height is greater than a critical value, the step-height decreases linearly with time, and not exponentially with time as Yang's model suggests [22 - 23]. Finally, it is not clear how Yang's model can be applied to an entire chip with an arbitrary layout.

Chekina et al., view the CMP problem as a wear-contact problem similar to those found in contact mechanics [24]. Although they do not specifically develop a model for copper CMP, the fact that they consider the case where two different materials are polished simultaneously, as well as the case where only one material is polished, make their model applicable to copper CMP. The model treats the pad as a massive elastic body whose surface is flat, and the wafer as a rigid body. Using contact mechanics, the model assumes the relationship between the displacement of the pad surface w and the contact pressure p, given in equation 2.6, where ω is the contact area, ν the poisson ratio of the pad, and E the pad elasticity. In addition, the model assumes that in steady

$$w(x,y) = \frac{(1-\nu^2)}{\pi E}\int_{\omega} p(\xi,\eta)\frac{1}{\sqrt{(x-\xi)^2+(y-\eta)^2}}d\xi d\eta \qquad \text{(Equation 2.6)}$$

state the pressure relation over the one-dimensional region *[0,l]* is given by equation 2.7, where p_1 is the average pressure in region 1 which spans [0,a], p_2 the pressure in region 2 which spans [a,l], p the average pressure, and l is the pitch.

$$p_1 a + p_2(l-a) = pl \qquad \text{(Equation 2.7)}$$

Using the above equations and Preston's equation, Chekina and Keer derive a formula which shows a linear relationship between steady-state dishing and pitch. Such a relationship is not supported by experimental data for conventional copper CMP processes [7, 8]. Furthermore, it is difficult to envision how the model can be efficiently applied to an entire chip.

Elbel et al., have developed a model for tungsten CMP, and they argue that it is applicable to all metal CMP processes [25]. In a situation where the oxide and tungsten are being polished simultaneously, the model expresses the pressure on the oxide p_{ox} and that on the tungsten p_w as given in equations 2.7 and 2.8, where p is the applied pressure, Φ the pattern density, d the metal dishing, and d_{max} the maximum dishing. Using Preston's equation to relate material removal rate to relative speed and pressure, together with equations 2.7 and 2.8, Elbel derives dishing and erosion equations in terms of pattern density, maximum dishing, and material removal rates.

$$p_{ox} = \frac{p}{1-\Phi} \qquad \text{(Equation 2.8)}$$

$$p_w = \begin{cases} p\left(1-\frac{d}{d_{max}}\right) & d < d_{max} \\ 0 & d = d_{max} \end{cases} \qquad \text{(Equation 2.9)}$$

One of the assumptions that Elbel makes is that the linear relationship between the metal pressure and the dishing is only applicable when the dishing is close to the maximum dishing. This makes the model restrictive. In addition, if the metal pressure decreases with dishing, the oxide pressure should increase with dishing, if the forces are to be conserved. The idea of force conservation is key to the model developed in this thesis. Furthermore, Elbel states that the maximum dishing is a function of line width only, and attempts to use a spring model to establish the relationship between the two. It is true that the maximum dishing depends on line width, but it should also depend on line space or pattern density. Finally, Elbel does not explicitly show how to compute the time it takes to clear the bulk tungsten and the barrier.

Yoshida has developed a three-dimensional chip-scale CMP model for single material polishing, using contact mechanics, Preston's equation, and a boundary element methodology [26]. The model treats the pad as an isotropic elastic body, and assumes the same relationship between the pad displacement and the concentrated load as given in equation 2.5. By defining a reference plane, and measuring all quantities relative to it, Yoshida argues that when the pressure is known, the displacement is unknown and vice-versa. Using the known quantities (pressure or displacements at different locations on the chip) and the necessary boundary conditions, a methodology for solving for the pad displacements and the pressure at all discretized points on the chip is proposed. This leads to a prediction of the evolution of the wafer surface during polishing. The model becomes computationally inefficient if it is used to capture the feature-scale dependencies on the chip, something that is necessary for chip-scale copper CMP modeling. Second, it lumps the compression of a pad and the long-range pad bending behavior into one constant, thereby making the constant difficult to interpret physically. The model is best suited for capturing long range pressure distribution across the entire chip. In this thesis, some of the ideas

in Yoshida's model are used, but appropriate engineering approximations are made, and fast fourier transforms are used to gain computational efficiency.

Vlassak has developed a contact mechanics based model of dishing and erosion in copper CMP, dielectric CMP, and STI CMP [27]. He assumes that the local heights of the pad asperities are exponentially distributed, and that the force transmitted by each asperity is given by Hertz's formula [28]. By assuming that the pressure between the wafer and the pad is due to pad asperities in contact with the wafer, and using the plain-strain deformation equation to relate pad displacement and wafer pressure (equation 2.5), Vlassak solves for the pressure distribution and the pad displacement numerically. With the pressure distribution known, Preston's equation is used to compute the material removal rate. This leads to the computation of dishing and erosion for arrays of lines with different densities and line widths. The effect of pad stiffness on dishing and erosion is also simulated for an array of lines.

Vlassak's model recognizes that pad compression, and long range pad deformation both play key roles in determining the polish pressure. However, Vlassak fails to mention how to compute the time it takes to clear the bulk copper and the barrier film. In addition, it is difficult to envision how to efficiently implement his model for an entire chip. Attempting to numerically solve for the pressure and pad displacements for an entire chip on a time stepped basis can be computationally intensive, especially if the discretization is fine enough to capture all features.

Runnels has developed a two-dimensional feature-scale erosion model for CMP processes [29, 30]. He models the pad as a network of vertical springs with the same spring constant, and horizontal springs with another spring constant. The springs are intended to capture the elastic behavior of the pad, with the vertical springs accounting for the pad compression, and the horizontal spring accounting for the long range bending or deformation of the pad. The

connection of the vertical and horizontal springs to form a network of springs couples the pad's compression with its long range bending or deformation.

In Runnels' model, pattern cross-section profiles are discretized using line segments connected at points called nodes. The pad is also discretized into the same number of nodes. Hooke's law is used to formulate a system of linear equations for the force exerted at each node. This system of equations is solved by Gaussian elimination. After solving for the forces at each node, Preston's equation is then used to compute the erosion rate at each node. A three-dimensional version of the model has also been developed for chip-scale simulations [31]. To fully capture the features on the entire die or a cross-section of the die, the discretization size must be very small. This raises the issues of computational efficiency and accuracy when the model is applied to an entire chip. If the discretization size is small, the model will be computationally intensive. If the discretization size is large, on the other hand, the model will be inaccurate.

In addition to the models discussed above, several others dealing with the simultaneous polishing of two different materials have been proposed [32 - 34]. They are all either restrictive to certain conditions or difficult to apply to an entire chip. Nevertheless, the ideas in these models will serve as a starting point, in the effort to develop a semi-physical chip-scale model for copper CMP processes, in this thesis.

2.2 Modeling and Characterization Framework

In copper CMP, the goal is to clear the bulk copper and the unwanted barrier film quickly, while keeping dishing, erosion and defects to a minimum. During this process, three materials are polished. First only copper is polished, followed by the polishing of copper and barrier film simultaneously. Finally, copper, barrier, and dielectric are polished simultaneously. To model the

process, three intrinsic stages of polish are identified: a bulk copper removal stage, a barrier clearing stage, and an overpolish stage, as illustrated in figure 2.2. In the bulk copper removal stage, only copper is being polished. In this stage, the evolution of the copper thickness across the chip, and the time it takes to remove the bulk copper across the chip, are of interest. The time to clear the bulk copper will vary across the die because of pattern differences and incoming electroplated topography variation.

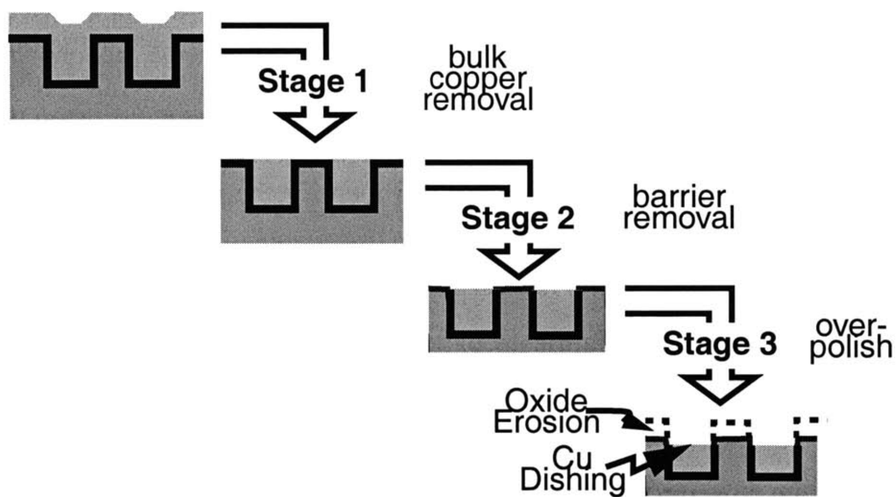


Figure 2.2: Three intrinsic stages in copper CMP processes

In the barrier clearing stage, copper and the barrier are being polished simultaneously. In this stage, the time it takes to clear the barrier, and the dishing that results when the barrier is just cleared at any spatial position, are of interest. Due to polish process variation across the wafer, deposited copper thickness variation across the wafer, and pattern differences across the die, by the time the bulk copper and barrier film are cleared at one point on the die, they might have been cleared already at another point on the die. Hence, the latter point on the die is overpolished. Overpolishing is defined as any polishing that is done beyond the time it takes to clear the bulk copper and the barrier film at the location of interest. During overpolishing, copper, barrier and dielectric are polished simultaneously. It is during overpolishing that the dielectric is eroded. In

addition, the dishing that might have started during the barrier clearing stage can worsen during overpolishing. This overpolishing is identified as the third intrinsic stage in copper CMP processes. The dishing and erosion that occur during this stage, are of interest. In computing the dishing during the overpolish stage, the dishing that occurs during the barrier clearing stage is used as an initial condition. It is important to note that the term overpolishing is used loosely in the CMP literature, and in the CMP industry. In the CMP industry, overpolishing means polishing beyond the end-point time.

The evolution of the bulk copper thickness, the time it takes to clear the bulk copper, the time it takes to clear the barrier, dishing and erosion, all depend on the patterns on the die, and the incoming electroplated topography. In an attempt to identify the pattern dependencies of these quantities, several masks with large ranges of line widths, line spaces, and pattern densities are designed. These masks are used to fabricate patterned wafers, and the wafers used to conduct polishing experiments. The data from these experiments and the known physics of the process are then used to formulate a semi-physical model that explicitly expresses several variables as functions of pattern factors (line width, line space, and pattern density), and provides unknowns that capture the effect of the polish process parameters.

2.3 Test Masks

To capture pattern dependencies in copper CMP, several test masks have been designed in collaboration with SEMATECH and semiconductor IC manufacturers [35 - 37]. In this section, each of these masks is briefly described.

2.3.1 MIT Cu Mask Version 1.2

This mask is a slight variation of the MIT-SEMATECH 931 mask [35]. It is a single level mask of dimensions 20 mm by 20 mm, with electrical and physical structures. The mask contains

arrays of lines, isolated lines, slotted pads, serpentines, combs, and other structures, as shown in figure 2.3. The minimum feature size on it is 0.25 μm, with line widths in

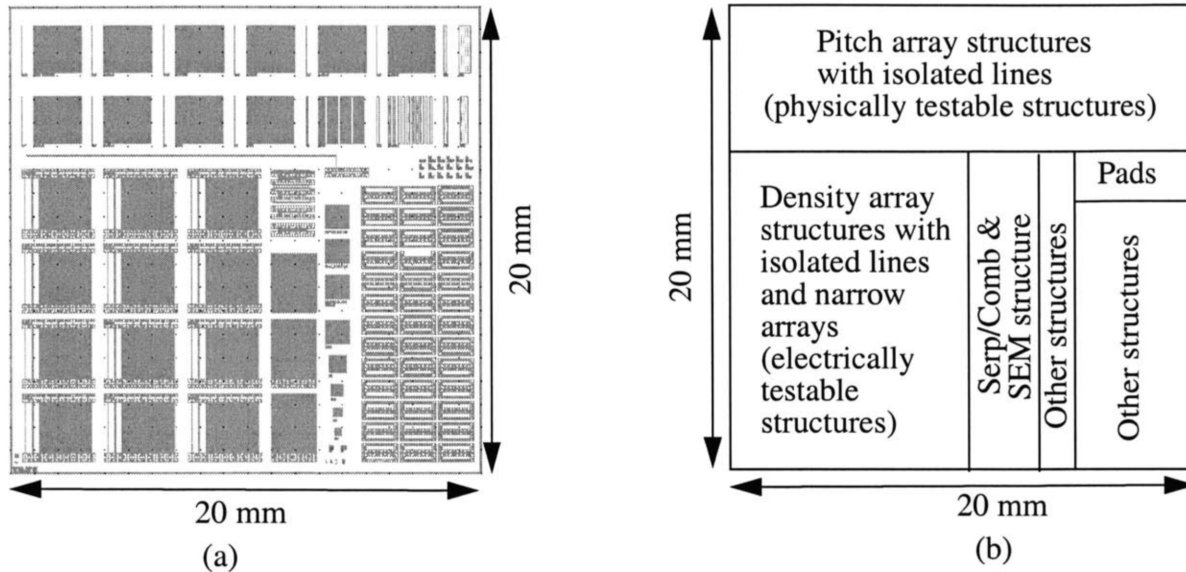


Figure 2.3: MIT copper mask version 1.2: (a) Layout (b) Floor plan

the range 0.25 μm to 100 μm, line spaces in the range 0.25 μm to 100 μm, and array layout densities in the range 10% to 90%. The arrays of lines are divided into pitch structures and density structures. The pitch structures are non-electrical structures, with a fixed layout density of 50%, and an array size of 2 mm. The density structures are electrically testable structures with certain lines within the array connected to form kelvin structures that are connected to bond pads. The array size of these density structures is about 2.3 mm. The arrays of lines are separated by large field regions to measure dishing, erosion, step heights and recess easily, and to minimize neighboring array effects.

2.3.2 GA303 Mask

This is a three level mask of dimensions 19.2 mm by 19.2 mm, designed to capture pattern dependencies mainly for sub-micron features. Levels one and three are metal levels while level two is a via level. The layouts and floor plans for the two metal levels of the mask are illustrated in

figures 2.4 and 2.5. Level one of the mask is divided into 64 squares, each of dimension 2.4 mm. Most of these squares contain arrays of lines and isolated lines that have the same line width as the lines in the arrays. Each array of lines contains several lines that are connected as kelvin structures and connected to bond pads. In addition, a special feature is added to each array to electrically test for shorts between adjacent

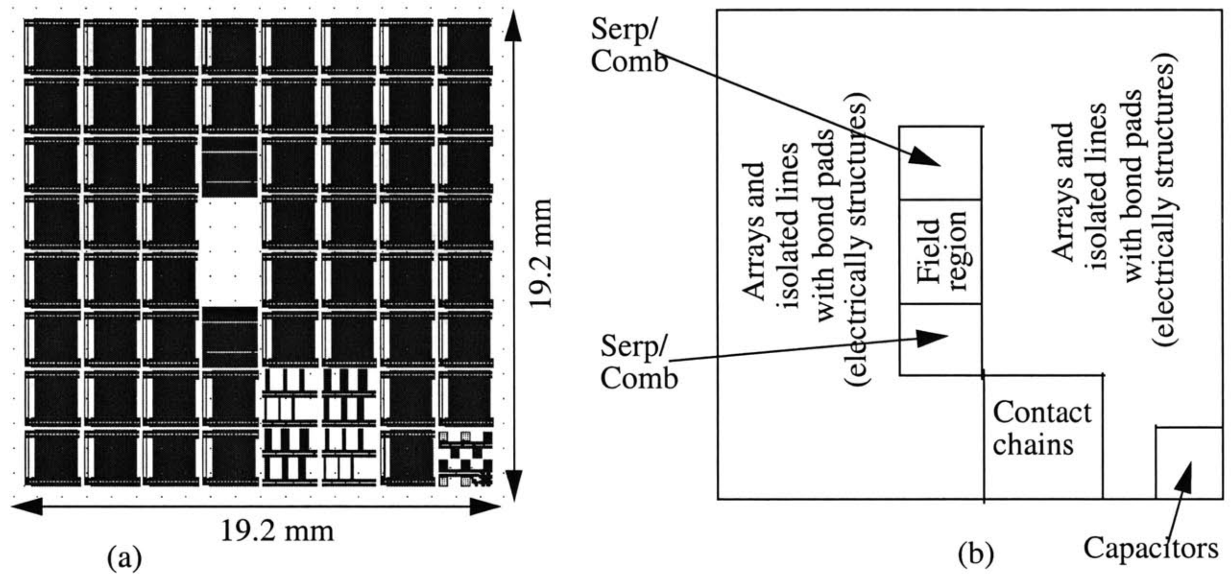


Figure 2.4: Metal level one of GA303: (a) Layout (b) Floor plan

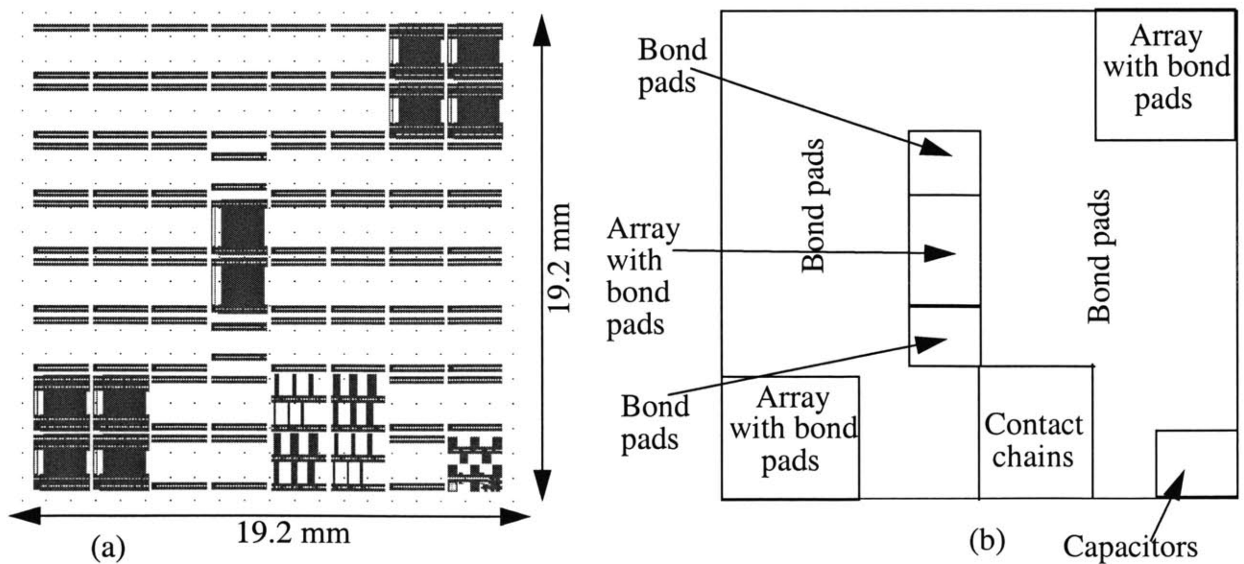


Figure 2.5: Metal level two of GA303: (a) Layout (b) Floor plan

lines. A sample array of lines with the isolated line on metal level one is illustrated in figure 2.6. The arrays have line widths and line spaces predominantly in the range of 0.18 μm to 1 μm, with a few in the range 1.5 μm to 15 μm. The layout pattern densities of these arrays range from 10% to 97%. The mask is designed such that the arrays of lines are separated by reasonably large fields regions to measure dishing, erosion, recess, and step-heights easily. The rest of the squares on the first metal level contain via chains, capacitor plates, serpentines, combs, and two unpatterned regions for measuring the erosion in large field areas.

The second level of this mask contains vias for the via chains and vias connecting the bond pads on the first level to those on the third level. The third level has ten array structures, capacitor plates, and mostly bond pads. These bond pads are electrically connected to the bond pads on level one. The goal is to be able to measure resistances of lines on metal level one directly from metal level two. The array structures on metal level two are intended to study the impact of the amount of dishing and erosion on metal level one on the amount of dishing and erosion on metal level two. A sample array on metal level two is shown in figure 2.7.

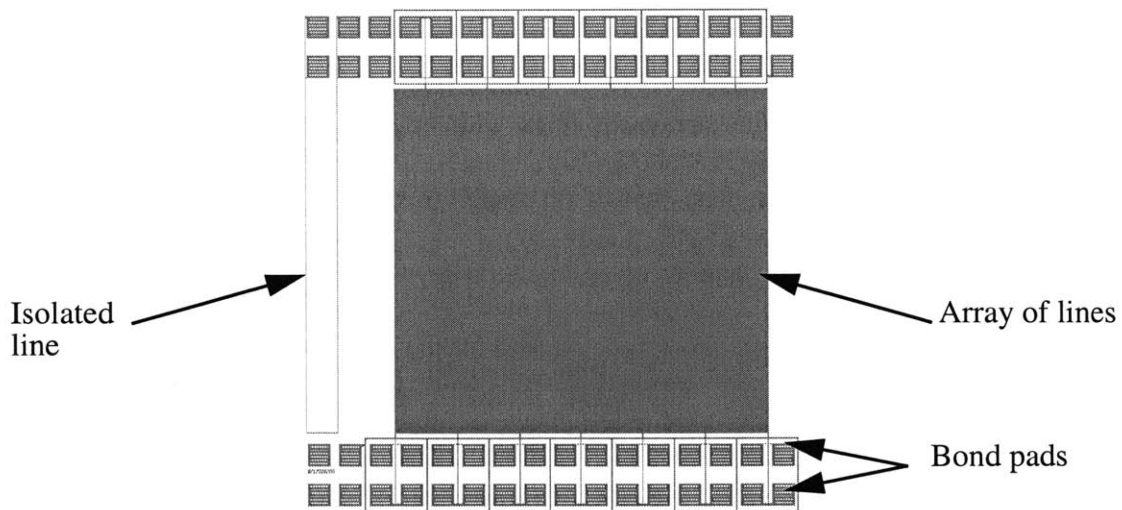


Figure 2.6: Sample array on metal level one of GA303 mask

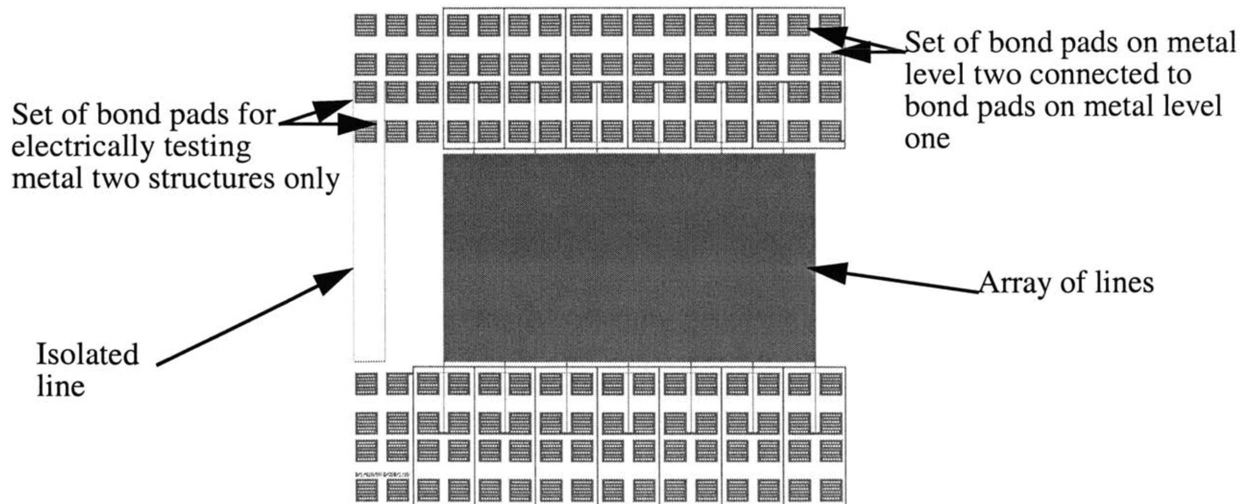


Figure 2.7: Sample array on metal level two of GA303 mask

2.3.3 MIT-SEMATECH 854 Mask

The information obtained from CMP experiments with the above two masks led to the design of the MIT-SEMATECH 854 mask [36]. This mask is a three layer mask with two metal levels, and its dimensions are 20 mm by 20 mm, as illustrated in figure 2.8. Metal level one contains arrays of lines with line widths and line spaces in the range 0.18 μm to 100 μm, and layout pattern density in the range 1% to 99%. In addition, metal level one also contains via chains, capacitors, slotted structures, and SEM structures for determining the true line widths of the lines. Metal level two contains arrays of lines with line width and line space of 0.5 μm, capacitor plates, and via chains. The arrays on metal level two are laid out to thoroughly investigate the impact of dishing and erosion on metal level one, on the dishing, erosion, and within-die non-uniformity on metal level two. Almost all the arrays are electrical structures, i.e., certain lines within the arrays are kelvin structures connected to bond pads. The arrays are isolated from each other by large field regions, to allow accurate surface profile measurements to be taken, and to avoid neighboring array effects.

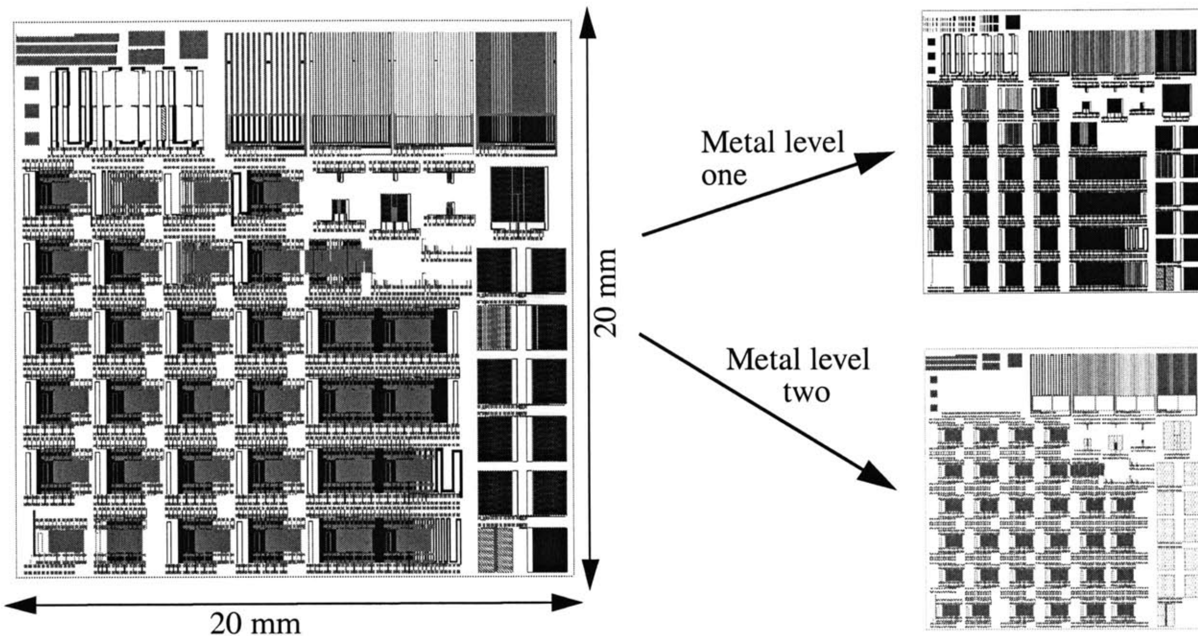


Figure 2.8: MIT-SEMATECH 854 mask

2.3.4 SEMATECH-MIT 862 Mask

The main idea behind this mask is to study the effects of polish process parameters and consumable sets on planarization during the bulk copper polishing stage [37]. In addition, it is designed to investigate the impact of varying line length, varying line space within an array, and varying line width within an array, on dishing and erosion in the overpolish stage. The mask is illustrated in figure 2.9, and it contains square trenches with dimensions in the range 1 μm to 8 mm, and arrays with line widths and line spaces in the range 1 μm to 100 μm. In addition, the lengths of some lines is varied from 1 μm to 1 mm.

The key to using this mask is the arrangement of the structures on the wafer, which is depicted in figure 2.10. The structures on the mask are repeated five times on the wafer, to obtain the interaction between wafer level non-uniformity and planarization. In addition to the structures on the mask, squares of dimensions in the range 10 mm to 25 mm are directly exposed on the wafer without the use of a mask. These squares are at the same distance from the wafer center in

order to avoid within wafer non-uniformity (WIWNU) bias.

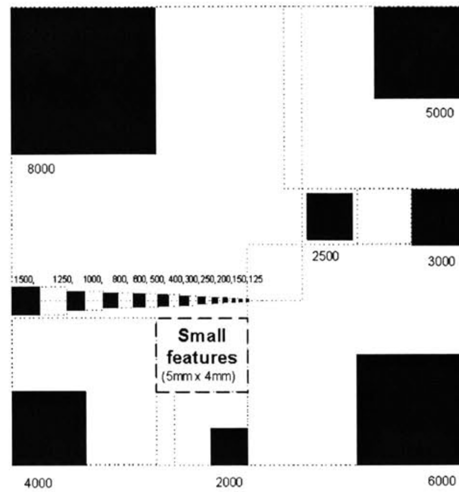


Figure 2.9: SEMATECH-MIT 862 mask

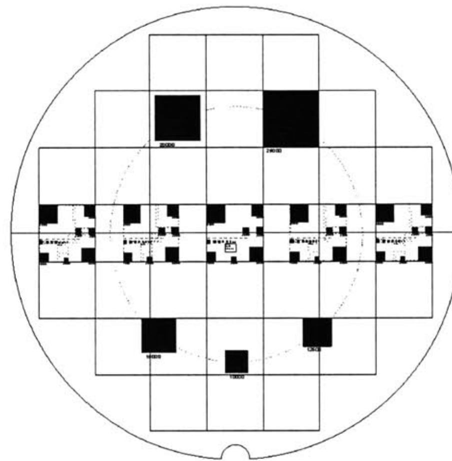


Figure 2.10: Wafer layout scheme for 862 mask

2.4 Metrology

Metrology is an important component of the overall CMP process. The ability to accurately measure copper thickness, dielectric thickness, and surface profiles, is essential to the development of a pattern dependent model for copper CMP processes. In this section, the

different measurements used in the model development, and the measurement tools used to take these measurements, are described.

2.4.1 Copper Thickness Measurements

To investigate the evolution of copper thickness during the bulk copper polishing stage, copper thickness measurements on patterned wafers are needed. While measuring copper thickness on blanket wafers can be easily accomplished with a four point probe, accurately measuring copper thickness on a patterned wafer when the overburden copper is still on the wafer, is not an easy task. Several companies are developing tools to accomplish this task.

The iScan which is a product of Applied Materials Inc., measures copper thickness indirectly by establishing and measuring eddy currents while polishing of the overburden copper is in progress [38]. It enables effective end-pointing to be done during the bulk copper stage, and it also makes possible the measurement of the instantaneous copper removal rate on blanket copper wafers while polishing is in progress [38]. The MetaPulse 200X from Rudolph, and the Impulse 300 [39] from Philips, can measure copper thicknesses ex-situ, in large field areas on patterned wafers with good accuracy. These tools can also measure the copper thickness within an array of lines (while bulk copper is everywhere on the array) provided that the spot size is less than the width of the region where the thickness is to be measured.

Copper thickness measurement is also essential after the bulk copper has been cleared, as copper thickness can be used together with dielectric thickness to get dishing information. The Impulse 300 [39], and the MetaPulse 200X can measure the thickness of some copper lines within arrays and the thickness of copper on bond pads, after the bulk copper is cleared. Alternatively, electrical measurements can be used to measure the thickness of copper lines after the bulk copper and the unwanted barrier film are cleared [35]. In this case, the resistance is measured, and with

knowledge of the resistivity, the accurate width of the line, and the length of the line, the copper thickness can be computed. It is important to note that this measurement is the average thickness of the copper line, taken along the entire line. In this thesis, electrical measurements are not used. In addition, in this thesis, the Impulse 300 or the Metapulse 200X are not used to measure the copper thickness after the bulk copper and the barrier are cleared. Instead, copper thickness is only measured in wide field areas with the Metapulse 200X or the Impulse 300, while there is still bulk copper on the wafer.

2.4.2 Surface Profile Measurements

To measure dishing, step height, and recess, a surface profile measurement is taken. A surface profile measurement is a one or two dimensional measurement that gives the relative heights of the different regions of the surface in question. This measurement is done with a high resolution profiler, typically the HRP from KLA-Tencor or the Veeco profiler. Figure 2.11 shows a sample levelled surface profile measurement for a structure after the bulk copper has been cleared and overpolishing completed. The dishing and recess associated with this structure are indicated in the figure. Levelled profile means that the relative height of the left of the profile (field region) and that of the right of the profile (another field region) are set to the same reference value (typically zero). Every measurement is taken relative to this reference value. Figures 2.12 and 2.13 show sample levelled profiles for two array structures while there is still bulk copper on the wafer. The recess and step heights associated with these structures are indicated in the figures.

In order to measure the copper thickness within an array while there is bulk copper on the wafer, both a surface profile measurement across the array and copper thickness measurements in the large field regions next to the array are used. If the point within the array is an up-area, then the copper thickness at that point is the mean copper thickness of the two field regions that

surround the array, minus the recess at the point in question. On the other hand, if the point of interest within the array is a down-area, the copper thickness at that point is the mean of the field copper thicknesses surrounding the array, minus the recess at that point, minus the step height at the down-area of interest. It is important to note that if the relative height of the up-area is greater than that of the surrounding field region, then the recess is negative and vice-versa.

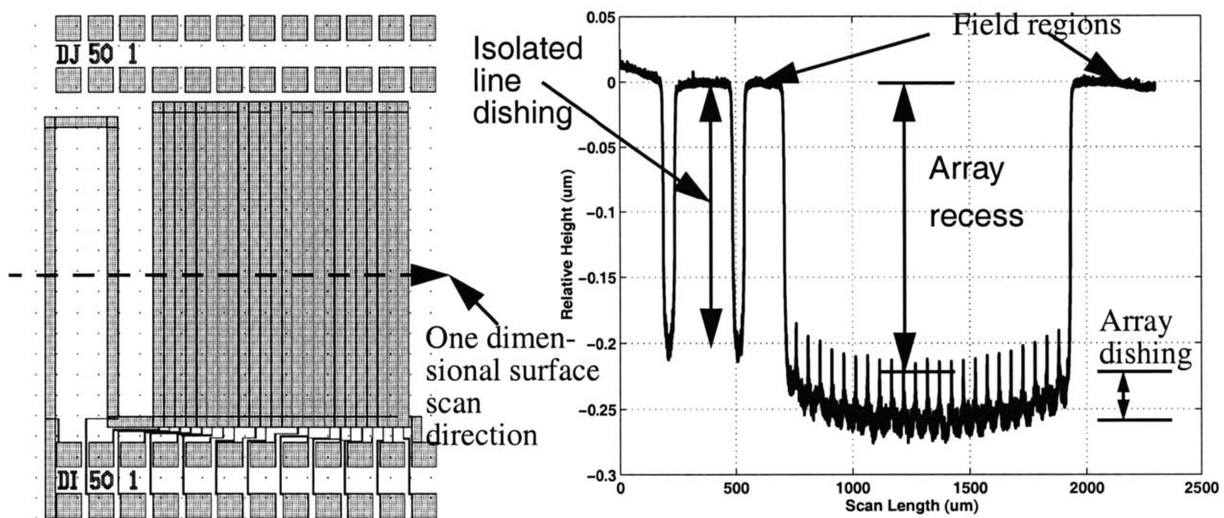


Figure 2.11: Profilometer scan of large feature array after the bulk copper and the barrier are completely cleared on wafer

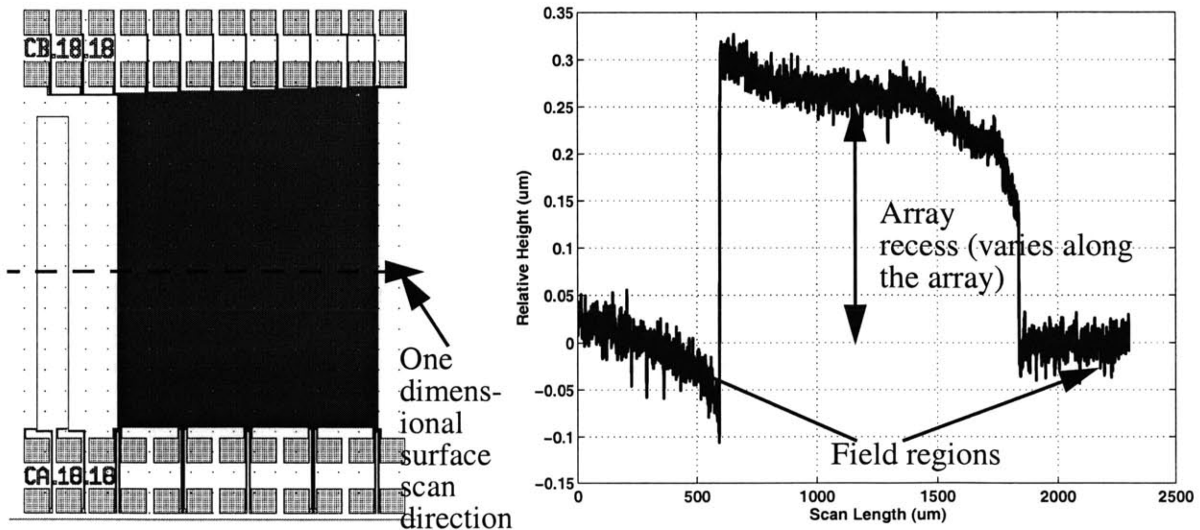


Figure 2.12: Profilometer scan of electroplated fine-feature array

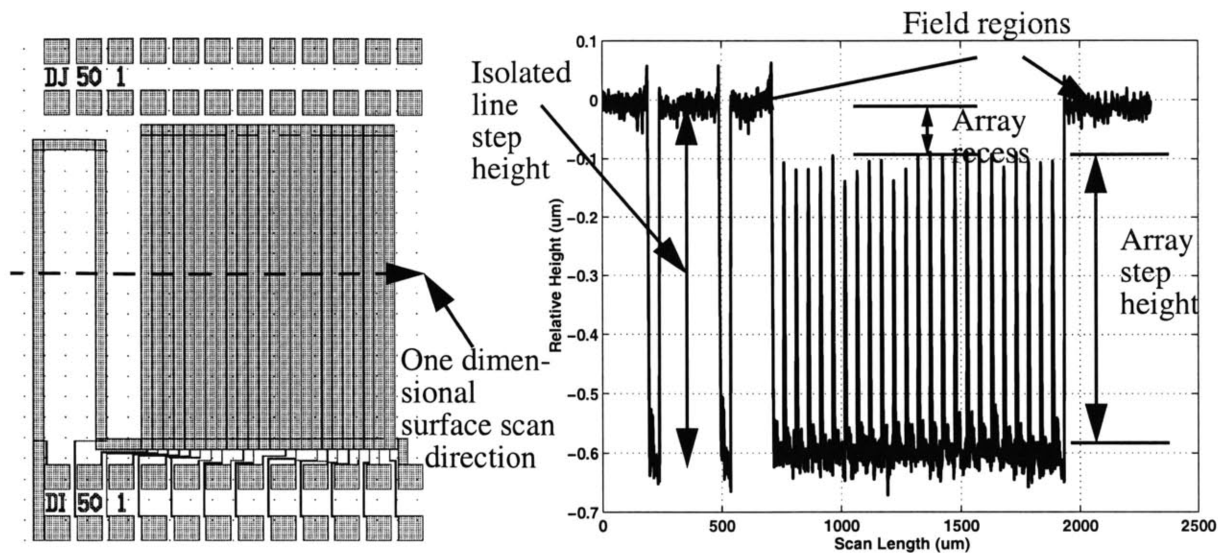


Figure 2.13: Profilometry scan of electroplated large feature array

Erosion of dielectric spaces within an array of lines can be obtained by combining surface profile measurements of the array with dielectric thickness measurements in the field regions surrounding the array. The erosion at any dielectric point within the array is the mean thickness loss in the field regions surrounding the array plus the recess at the dielectric point of interest. Alternatively, erosion of the dielectric within an array can be obtained by measuring (using the UV1250 or UV1280 or F5 from KLA-Tencor) the deposited dielectric thickness at the location of interest, and the dielectric thickness at the same location after CMP. The erosion at that location is the difference between the deposited and post-CMP dielectric thicknesses.

One of the problems with using a surface profile scan to obtain erosion, dishing, and copper thickness within arrays, is that the field regions of the surface scan are levelled to the same reference height, even though they might be of different thicknesses. The greater the thickness difference between the two field regions, the greater the error in the measurements obtained from the surface scan in question. When the field regions are reasonably large, the thickness difference

between the left and right field regions is typically small.

2.4.3 Dielectric Thickness Measurements

Dielectric thickness measurements can be obtained using KLA-Tencor's UV1250, UV1280 or F5. These tools have spot sizes of about 5 μm or less in high magnification, and can accurately measure dielectric (notably oxide and nitride) thickness to within 100 Å or better.

2.5 Characterization and Prediction Methodology

The general framework of formulating the model from experimental data and the known physics of the CMP process has been described. Once the model is formulated, one of the goals is to use it to predict dishing and erosion for any random layout. Figure 2.17 illustrates the characterization and prediction methodology. First, for a given process (fixed down force, table speed, slurry flow rate, and consumable set), polish experiments are conducted where the polish times are varied on different wafers. Second, the data from these experiments are used to calibrate the model for the given process. Once the model has been calibrated, it can then be used to predict dishing and erosion on any random layout polished under the same process conditions as those used in the model calibration. The electroplated topography and the layout features (density, line width, and line space) of the random layout are needed for dishing and erosion prediction. These are obtained from an empirical pattern dependent electroplating model [36], and a layout extractor respectively. The layout dependent dishing and erosion prediction can also be used to assess the effectiveness of dummification in reducing within-die non-uniformity.

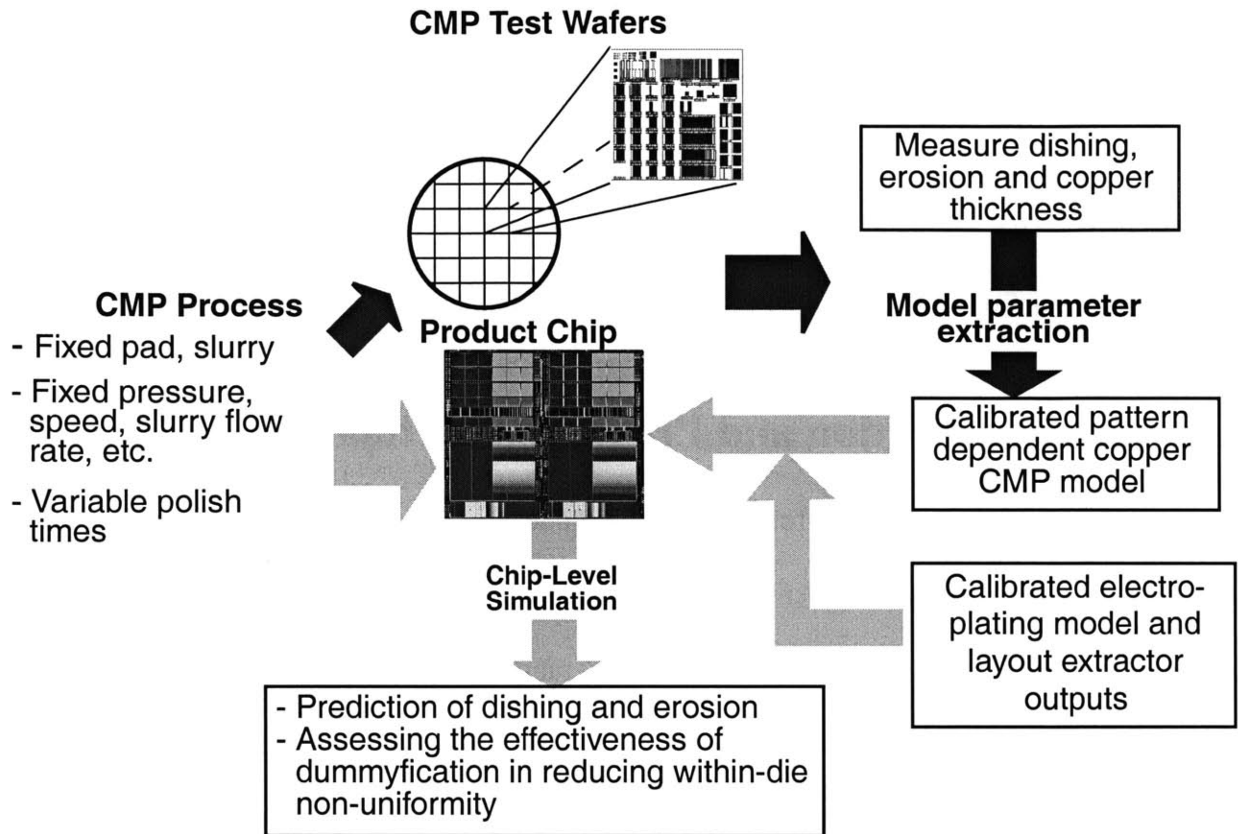


Figure 2.14: Framework of characterization and prediction methodology

Chapter 3

The Density-Step-Height Model for Single Step Copper CMP Processes

The density-step-height model views copper CMP processes as chemically enhanced mechanical processes. The contact of the polishing pad and abrasive particles with the wafer at some applied pressure and speed is responsible for the removal of material during copper CMP. This mechanical contribution is enhanced or suppressed by the active chemical reactions between the slurry and the materials that are being polished.

By applying regression analysis to data from blanket wafer polishing experiments conducted to investigate the relationship between material removal rate and pressure, the model establishes an empirical relationship between the material removal rate and polish pressure, for a specific consumable set and speed. It then uses Hooke's law to relate the polish pressure to the local step height and the pattern density. The relationship between material removal rate and polish pressure, and that relating polish pressure to step height and pattern density, are then used to relate removal rate to step height and density.

In this chapter, the density-step-height model for single step copper CMP processes is presented. Single step copper CMP processes use the same consumable set (pad and slurry), and the same polish process settings (such as down force, table speed, and slurry flow rate) throughout the process. In sections 3.1 - 3.3, the model equations are derived for the three intrinsic stages of a copper CMP process, followed by a description of the model parameters and a discussion of special effects in copper CMP, in sections 3.4 - 3.6. A methodology for calibrating the model is

proposed in section 3.7, and used to show how well the model fits experimental data in section 3.8. In section 3.9, some of the limitations of the density-step-height model are discussed, and extensions of the model are proposed to deal with these limitations. Finally, the chapter concludes in section 3.10 with a summary of the contributions.

3.1 Model Formulation for Intrinsic Stage One: Bulk Copper Clearing Stage

In the bulk copper clearing stage, the main goals are computing the evolution of the bulk copper thickness and the time it takes to clear the bulk copper at any spatial location of interest. Figure 3.1 shows a sample electroplated topography for an array of lines with an initial step height H_0. If the initial step-height for this array is greater than a critical step height H_{ex}, the pad and abrasives combination will not contact the down-area initially. Consequently, there will be no pressure exerted on the down-area initially [9,22]. The up-area, on the other hand, will have a non-zero constant pressure exerted on it initially. This constant up-area pressure is equal to the applied force divided by the effective contact area, where the effective contact area is the total up-area within the region where the influence of the applied force is felt. Thus, the effective up-area pressure can be expressed as the applied pressure P_1 divided by the effective electroplated copper pattern density ρ_{cu} at the position of interest [3,40]. The effective electroplated copper pattern density is the total up-area fraction in the effective contact region [3,40].

As polishing progresses, the step height H decreases as illustrated in figure 3.1. When the step height becomes less than the critical step height H_{ex}, the pressure exerted on the down-area becomes non-zero. By Hooke's law, this non-zero down-area pressure increases linearly as the step-height decreases, while the up-area pressure decreases linearly as the step-height decreases.

Step height reduction continues until the step height is eliminated and the copper surface is flat. The pressure exerted on this flat surface is the applied pressure P_1. Figure 3.2 illustrates the relationship between the polish pressure and the step-height, for both the down-area and the up-area during bulk copper polishing. The up-area and down-area pressures illustrated in the figure are expressed mathematically in equations 3.1 - 3.2. From these equations, it can be shown that the total force on the up-area and down-area is always equal to the applied force F_1. This is expressed in equation 3.3, where A is the area of influence of the applied force F_1, and $P_1A = F_1$.

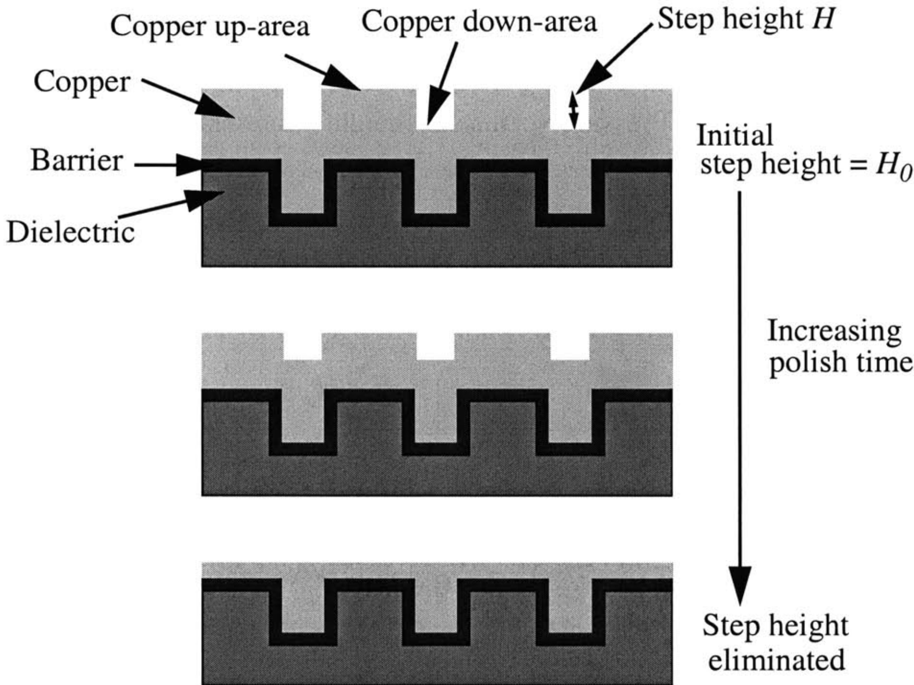


Figure 3.1: Step height evolution during bulk copper polishing

For the sake of simplicity, and without loss of generality, suppose the copper CMP process is Prestonian (most conventional copper CMP processes are approximately Prestonian), i.e., the material removal rate is linearly proportional to the polishing pressure, for copper, dielectric, and barrier polishing, as illustrated in figure 3.3. Strictly speaking, Prestonian means that the removal rate is directly proportional to the product of the pressure and relative speed. Using this Prestonian

relationship together with the pressure versus step height relationship illustrated in figure 3.2, the removal rate diagram for intrinsic stage one is constructed as shown in figure 3.4.

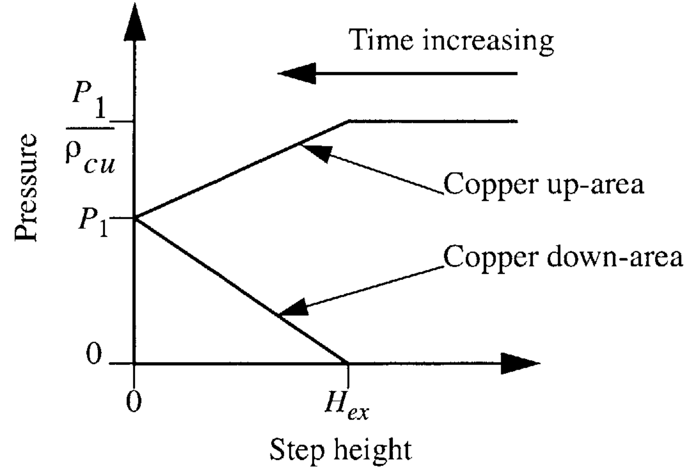


Figure 3.2: Pressure versus step height relationship

$$P_{up} = \begin{cases} P_1 + P_1\left(\frac{1-\rho_{cu}}{\rho_{cu}}\right)\frac{H}{H_{ex}} & 0 \le H < H_{ex} \\ \frac{P_1}{\rho_{cu}} & H \ge H_{ex} \end{cases} \quad \text{(Equation 3.1)}$$

$$P_{down} = \begin{cases} P_1\left(1 - \frac{H}{H_{ex}}\right) & 0 \le H < H_{ex} \\ 0 & H \ge H_{ex} \end{cases} \quad \text{(Equation 3.2)}$$

$$P_{up}A\rho_{cu} + P_{down}A(1-\rho_{cu}) = F_1 \quad \text{(Equation 3.3)}$$

A removal rate diagram plots removal rate versus step height (or dishing). The up-area and down-area removal rates illustrated in the removal rate diagram for intrinsic stage one are expressed mathematically in equations 3.4 - 3.5, where RR_{up} is the up-area removal rate and RR_{down} the

down-area removal rate. From these first order differential equations, and given the appropriate boundary conditions, one can solve for the evolution of the step height, the evolution of the copper thickness in the up-area and down-area, and the time it takes to clear the bulk copper at any spatial position of interest. This is discussed in the subsections to follow.

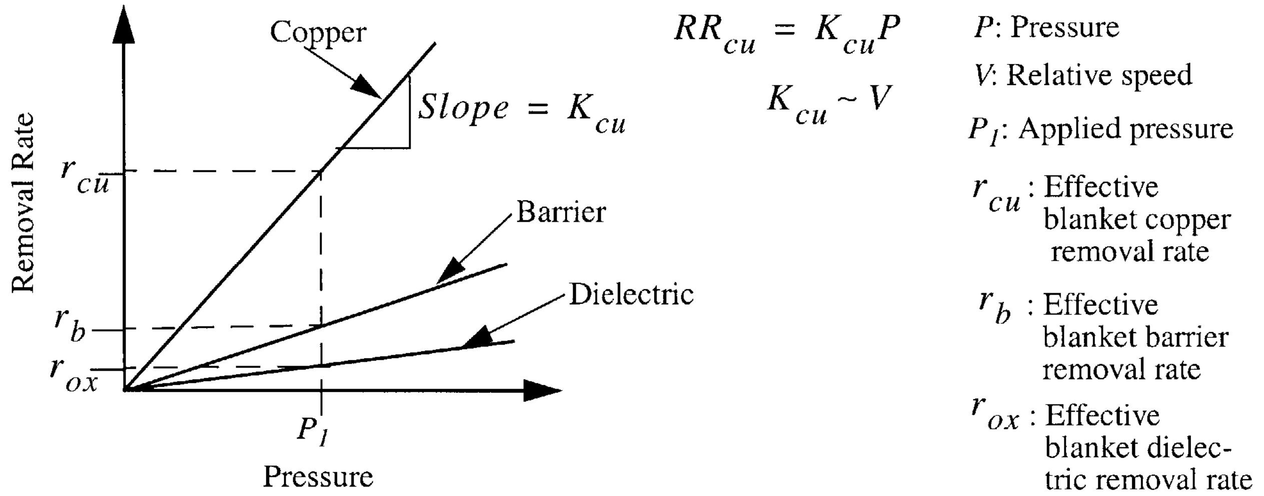


Figure 3.3: Relationship between removal rate and pressure

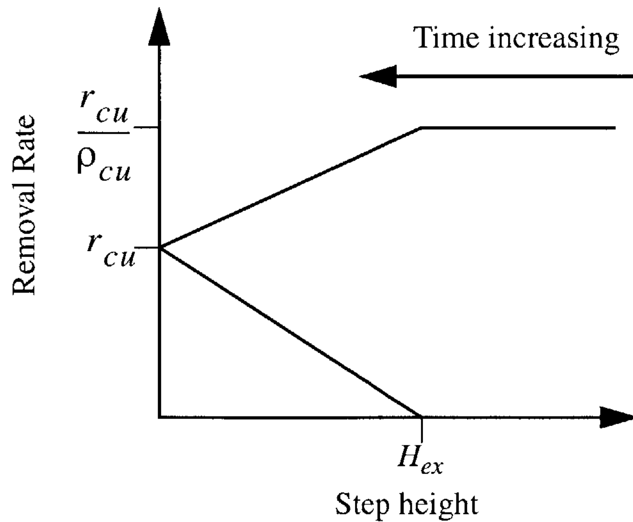


Figure 3.4: Removal rate diagram for bulk copper polish stage

$$RR_{up} = \begin{cases} r_{cu} + r_{cu}\left(\frac{1-\rho_{cu}}{\rho_{cu}}\right) & 0 \le H < H_{ex} \\ \frac{r_{cu}}{\rho_{cu}} & H \ge H_{ex} \end{cases} \qquad \text{(Equation 3.4)}$$

$$RR_{down} = \begin{cases} r_{cu}\left(1 - \frac{H}{H_{ex}}\right) & 0 \le H < H_{ex} \\ 0 & H \ge H_{ex} \end{cases} \qquad \text{(Equation 3.5)}$$

3.1.1 Evolution of Step Height

The rate of change of the step height H with respect to polish time t is given in equation 3.6. The temporal evolution of the step height depends on whether the initial step height H_0 is less than or greater than the critical step height H_{ex}. Each of these scenarios is examined below.

$$\frac{dH}{dt} = RR_{down} - RR_{up} \qquad \text{(Equation 3.6)}$$

1. Case 1: $H_0 > H_{ex}$ (The initial step height is greater than the critical step height.)

If the initial step height is greater than the critical step height, the step height reduces linearly with polish time until it is equal to the critical step height at a time denoted by t_{ex}. After time t_{ex}, the step height decreases exponentially with polish time. This is expressed in equation

$$H = \begin{cases} H_0 - \frac{r_{cu}}{\rho_{cu}} t & 0 \le t < t_{ex} \\ H_{ex} e^{\frac{-(t - t_{ex})}{\tau_1}} & t \ge t_{ex} \end{cases} \qquad \text{(Equation 3.7)}$$

3.7. The time at which the step height reaches the critical step height, and the time constant τ_1 with which the step height decreases exponentially are given in equations 3.8 and 3.9 respectively.

$$t_{ex} = \frac{(H_0 - H_{ex})\rho_{cu}}{r_{cu}} \qquad \textit{(Equation 3.8)}$$

$$\tau_1 = \frac{H_{ex}\rho_{cu}}{r_{cu}} \qquad \textit{(Equation 3.9)}$$

2. Case 2: $H_0 \le H_{ex}$ (the initial step height is less than or equal to the critical step height)

When the initial step height is less than or equal to the critical step height, the step height decreases exponentially with polish time as given in equation 3.10. The time constant τ_1 of the exponential decrease is given in equation 3.9.

$$H = H_0 e^{\frac{-t}{\tau_1}} \qquad t \ge 0 \qquad \textit{(Equation 3.10)}$$

3.1.2 Evolution of Bulk Copper Thickness

Figure 3.5 shows the electroplated topography for an array of lines, with the definitions of some of the variables used in this section. Let Z_{up} represent the copper up-area thickness relative

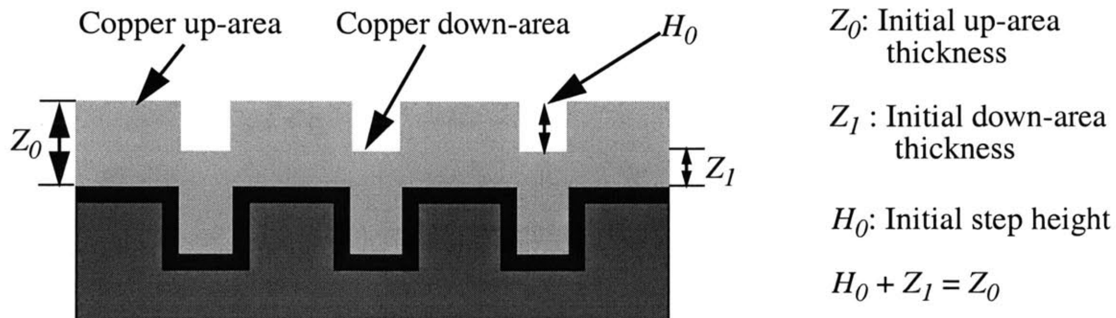


Figure 3.5: Pre-CMP electroplated topography of an array

to the barrier surface, Z_{down} the copper down-area thickness relative to the barrier surface, AR_{up} the amount of copper thickness removed in the up-area, AR_{down} the amount of copper thickness removed in the down-area, and t the polish time. The evolution of Z_{up}, Z_{down}, AR_{up} and AR_{down} are expressed below.

1. Case 1: $H_0 > H_{ex}$ (the initial step height is greater than the critical step height)

The rate of change of the up-area thickness and the down-area thickness with respect to time are given in equations 3.11 and 3.12. When the initial step height is greater than the critical

$$\frac{dZ_{down}}{dt} = -RR_{down} \qquad \text{(Equation 3.11)}$$

$$\frac{dZ_{up}}{dt} = -RR_{up} \qquad \text{(Equation 3.12)}$$

$$Z_{up} = \begin{cases} Z_0 - \dfrac{r_{cu}}{\rho_{cu}}t & 0 \le t < t_{ex} \\ Z_0 - \dfrac{r_{cu}}{\rho_{cu}}t_{ex} - r_{cu}(t - t_{ex}) + H_{ex}(1 - \rho_{cu})\left(e^{\frac{-(t - t_{ex})}{\tau_1}} - 1\right) & t \ge t_{ex} \end{cases}$$

(Equation 3.13)

$$Z_{down} = \begin{cases} Z_1 & 0 \le t < t_{ex} \\ Z_1 - r_{cu}(t - t_{ex}) - H_{ex}\rho_{cu}\left(e^{\frac{-(t - t_{ex})}{\tau_1}} - 1\right) & t \ge t_{ex} \end{cases} \qquad \text{(Equation 3.14)}$$

step height, the evolution of the copper up-area and down-area thickness are given in equations 3.13 and 3.14, where τ_1 is given in equation 3.9. The amount of copper removed in the up-area and down-area are given in equations 3.15 and 3.16 respectively.

$$AR_{up} = Z_0 - Z_{up} \qquad \text{(Equation 3.15)}$$

$$AR_{down} = Z_1 - Z_{down} \qquad \text{(Equation 3.16)}$$

2. Case 2: $H_0 \le H_{ex}$ (the initial step height is less than or equal to the critical step height)

$$Z_{up} = Z_0 - r_{cu}t + H_0(1-\rho_{cu})\left(e^{\frac{-t}{\tau_1}} - 1\right) \qquad t \ge 0 \qquad \text{(Equation 3.17)}$$

$$Z_{down} = Z_1 - r_{cu}t - H_0\rho_{cu}\left(e^{\frac{-t}{\rho_1}} - 1\right) \qquad t \ge 0 \qquad \text{(Equation 3.18)}$$

When the initial step height is less than or equal to the critical step height, the evolution of the copper thickness in the up-area and the down-area are given in equations 3.17 and 3.18 respectively. In both cases 1 and 2 (when the initial step height is greater than the critical step height, and when it is less than or equal to the critical step height), the time it takes to clear the overburden copper at an up-area can be computed by setting the amount of copper removed in the up-area to the initial up-area thickness, and solving for the time that satisfies the resulting equation. Similarly, the time it takes to clear the copper thickness in a down-area can be computed by setting the amount removed in the down-area to the initial down-area thickness and solving the resulting equation for the time. In the case where the step height is eliminated before the bulk

copper is cleared for a particular array of lines, the time it takes to clear the bulk copper in the up-area is equal to that to clear the bulk copper in the down-area.

3.2 Model Formulation in Intrinsic Stage Two: Barrier Clearing Stage

In the barrier clearing stage, the copper in the trenches and the barrier film in the spaces between the trenches are being polished simultaneously. The time it takes to clear the barrier and the dishing that results when the barrier has just been cleared, at any spatial location, are of interest in this stage. Figure 3.6 shows the initial topography and the final topography for an array of lines polished through intrinsic stage two. The assumption made in this figure is that the array is planarized before the bulk copper film is completely cleared, i.e., the starting height of the copper in the trenches is equal to that of the barrier in the spaces between the trenches.

For an applied pressure of P_1, figure 3.3 shows that the blanket copper removal rate is greater than the blanket barrier removal rate. As polishing progresses, the copper surface recesses below the barrier surface. The difference between the relative height of the barrier and that of the copper in the trenches is termed pre-dishing. As the pre-dishing increases, the effective pressure

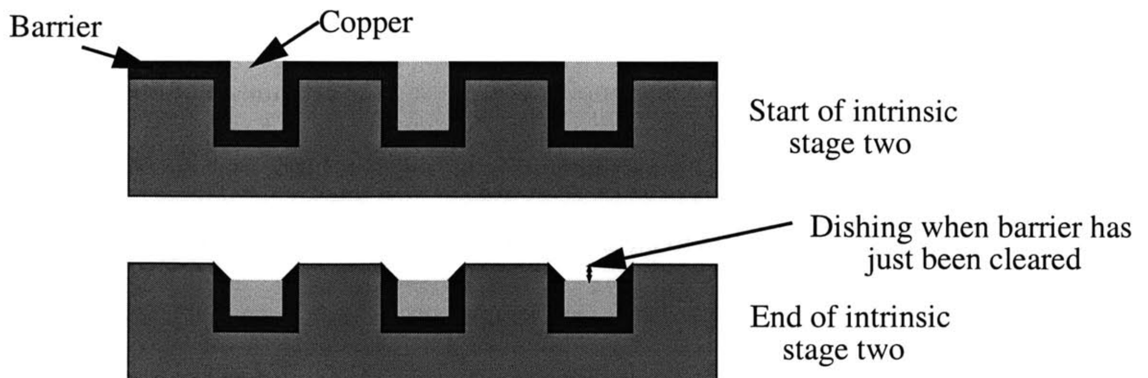


Figure 3.6: Sample topography at the beginning and the end of the barrier clearing stage

on the copper in the trenches decreases, and that on the barrier in the spaces between the trenches increases. By Hooke's law, the pressure on the copper (the down-area) decreases linearly with increasing pre-dishing, while that on the barrier (the up-area) increases linearly with increasing pre-dishing. The pre-dishing at which the pressure on the copper is zero is called the maximum dishing d_{max}, and it is a model parameter. At this pre-dishing value, the pressure on the barrier is equal to the applied pressure P_1 divided by the effective layout barrier pattern density (which is one minus the effective layout copper pattern density Φ_{cu} in stage two). A different symbol is used to distinguish the effective layout copper pattern density in stage two from the effective electroplated copper pattern density ρ_{cu} in stage one. Figure 3.7 illustrates the relationship between pressure and pre-dishing, and equations 3.19 and 3.20 express this relationship mathematically.

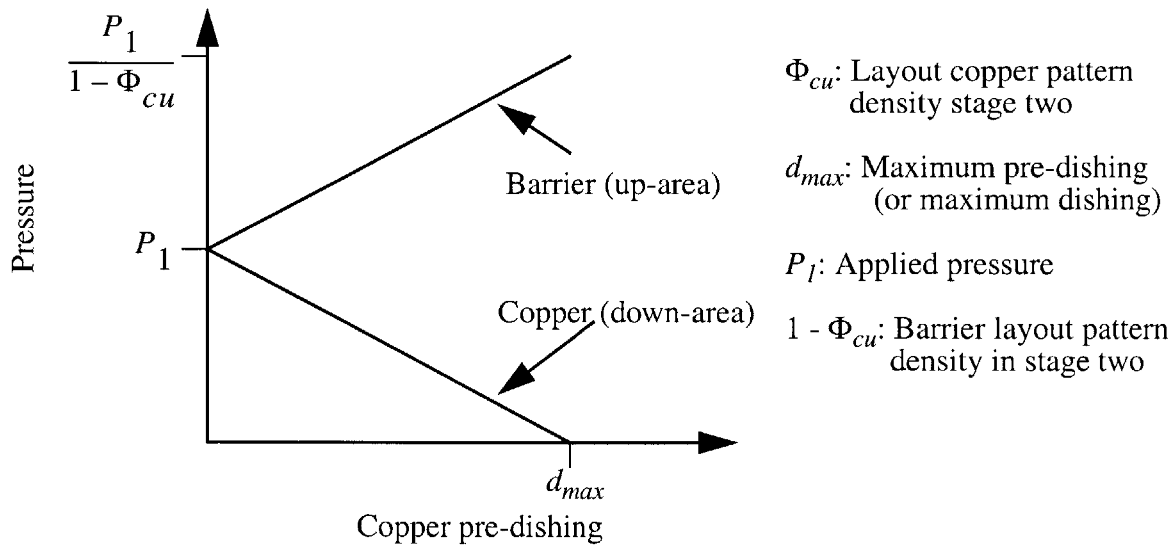


Figure 3.7: Pressure versus copper pre-dishing

$$P_b = P_1 + P_1\left(\frac{\Phi_{cu}}{1-\Phi_{cu}}\right)\frac{d_{cu}}{d_{max}} \qquad \textit{(Equation 3.19)}$$

$$P_{cu} = P_1\left(1 - \frac{d_{cu}}{d_{max}}\right) \qquad \textit{(Equation 3.20)}$$

By combining the removal rate versus pressure relationship (figure 3.3) with the pressure versus pre-dishing relationship (figure 3.7), the removal rate diagram for the barrier clearing stage is constructed as shown in figure 3.8. This diagram plots removal rate versus copper pre-dishing. When the surface is flat (i.e., when the pre-dishing is zero) the removal rate of the copper is the instantaneous blanket copper rate while that of the barrier is the instantaneous blanket barrier rate. As polishing progresses and the pre-dishing increases, the barrier removal rate increases and the copper removal rate decreases. If polishing continues for a long time, a pre-dishing of d_{ss} is reached, at which point the removal rate of the barrier and that of the copper are equal. This condition is called steady-state pre-dishing, and when it is achieved, the pre-dishing remains unchanged (provided that the process conditions and the consumable set are not changed). The

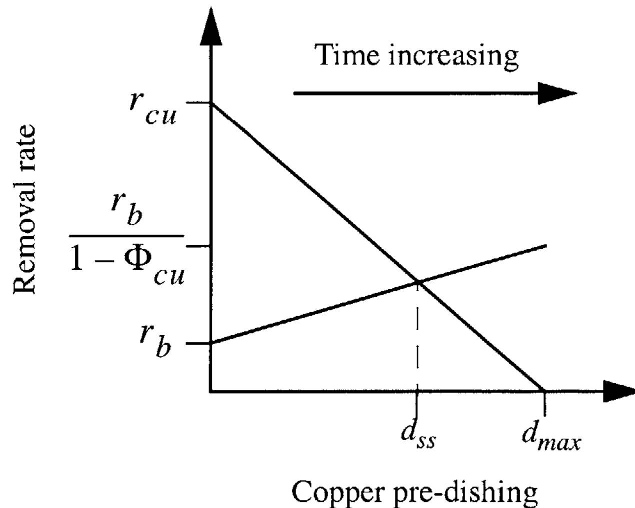


Figure 3.8: Removal rate diagram for intrinsic stage two

relationship illustrated in figure 3.7 is expressed mathematically in equations 3.12 and 3.22, where RR_{cu} is the copper removal rate and RR_b is the barrier removal rate. From these equations,

the barrier thickness loss E_b and the amount of copper pre-dishing d_{cu} are computed in equations 3.23 - 3.28. The time t_2 that it takes to clear the barrier at any spatial location of interest is obtained from solving equation 3.29 numerically, where Z_2 is the initial barrier thickness. In addition, the dishing d_2 that results when the barrier has just been cleared is given in equation 3.30.

$$RR_b = r_b + r_b\left(\frac{\Phi_{cu}}{1-\Phi_{cu}}\right)\frac{d_{cu}}{d_{max}} \quad \text{(Equation 3.21)}$$

$$RR_{cu} = r_{cu}\left(1 - \frac{d_{cu}}{d_{max}}\right) \quad \text{(Equation 3.22)}$$

$$d_{cu} = d_1 e^{\frac{-(t-t_1)}{\tau_2}} + d_{ss}\left(1 - e^{\frac{-(t-t_1)}{\tau_2}}\right) \quad \text{(Equation 3.23)}$$

$$E_b = X_1(t-t_1) + X_2(d_{ss}-d_1)\left(e^{\frac{-(t-t_1)}{\tau_2}} - 1\right) \quad \text{(Equation 3.24)}$$

$$d_{ss} = \frac{d_{max}(r_{cu}-r_b)(1-\Phi_{cu})}{r_{cu}(1-\Phi_{cu}) + r_b\Phi_{cu}} \quad \text{(Equation 3.25)}$$

$$\tau_2 = \frac{d_{max}(1-\Phi_{cu})}{r_{cu}(1-\Phi_{cu}) + r_b\Phi_{cu}} \quad \text{(Equation 3.26)}$$

$$X_1 = \frac{r_{cu}r_b}{r_{cu}(1-\Phi_{cu}) + r_b\Phi_{cu}} \quad \text{(Equation 3.27)}$$

$$X_2 = \frac{r_b \Phi_{cu}}{r_{cu}(1-\Phi_{cu}) + r_b \Phi_{cu}}$$ *(Equation 3.28)*

$$X_1(t_2 - t_1) + X_2(d_{ss} - d_1)\left(e^{\frac{-(t_2 - t_1)}{\tau_2}} - 1\right) = Z_2$$ *(Equation 3.29)*

$$d_2 = d_1 e^{\frac{-(t_2 - t_1)}{\tau_2}} + d_{ss}\left(1 - e^{\frac{-(t_2 - t_1)}{\tau_2}}\right)$$ *(Equation 3.30)*

3.3 Model Formulation in Intrinsic Stage Three: Overpolish Stage

In the overpolish stage, the copper in the trench, the barrier on the side wall of the trench, and the dielectric in the space between the trench, are all being polished simultaneously. The dielectric erosion and the copper dishing that occur during this stage are the variables of interest. Figure 3.12 shows the relationship between pressure and dishing in this stage. This relationship is based on Hooke's law in the same manner as those in stages one and two. Equations 3.31 and 3.32 express the pressure versus dishing relationship mathematically. The effective layout copper pattern density Φ_{cu} and the maximum dishing d_{max} are the same for intrinsic stages two and three. The reason for this will become clear when the modeling parameters are described in a later section of this chapter.

By combining the removal rate versus pressure relationship illustrated in figure 3.3, with the pressure versus step height relationship illustrated in figure 3.9, the removal rate diagram for

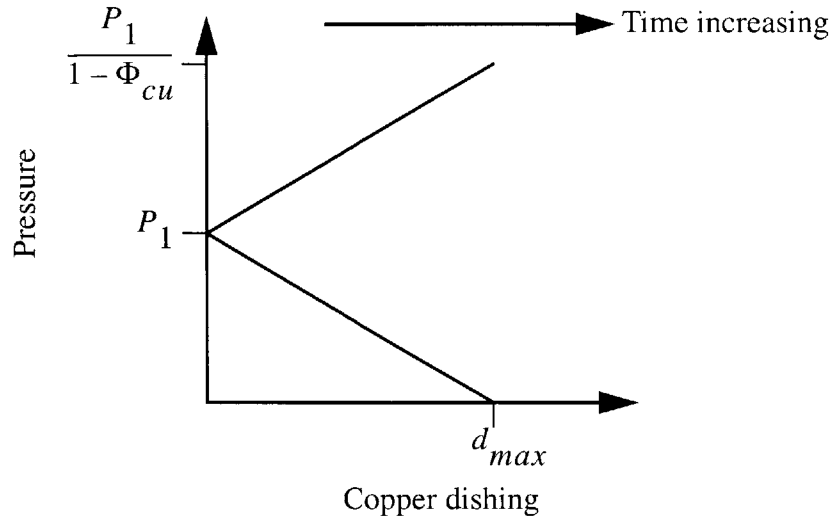


Figure 3.9: Pressure versus copper dishing

$$P_{ox} = P_1 + P_1\left(\frac{\Phi_{cu}}{1-\Phi_{cu}}\right)\frac{D_{cu}}{d_{max}} \qquad \textit{(Equation 3.31)}$$

$$P_{cu} = P_1\left(1 - \frac{D_{cu}}{d_{max}}\right) \qquad \textit{(Equation 3.32)}$$

intrinsic stage three is derived as illustrated in figure 3.13. This diagram plots removal rate versus copper dishing. If the surface is flat initially, the copper and the dielectric removal rates are the respective effective blanket removal rates. As polishing progresses, the copper in the trench dishes because of the selectivity of the process. As dishing increases, the removal rate of the copper in the trench decreases linearly and that of the dielectric increases linearly. If polishing continues long enough, a steady state dishing of D_{ss} is reached at which the copper and dielectric removal rates are equal. The relationship illustrated by the removal rate diagram is expressed mathematically in equations 3.33 and 3.34, where RR_{ox} is the dielectric removal rate, and RR_{cu} the copper removal rate. From these equations, the dishing D_{cu} and erosion E_{ox} as functions of

time are derived in equations 3.35 - 3.40, where t is the polish time, t_1 the time to clear the bulk copper at the position of interest, and t_2 the time to clear the barrier at the position of interest.

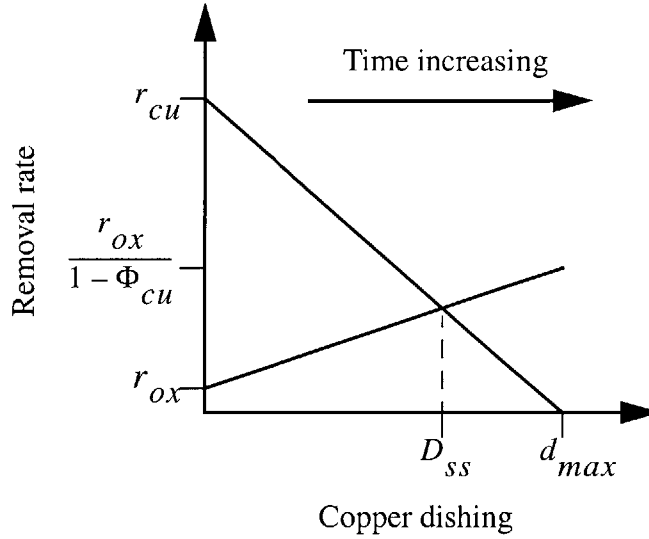


Figure 3.10: Removal rate diagram for intrinsic stage three

$$RR_{ox} = r_{ox} + r_{ox}\left(\frac{\Phi_{cu}}{1-\Phi_{cu}}\right)\frac{D_{cu}}{d_{max}} \qquad \text{(Equation 3.33)}$$

$$RR_{cu} = r_{cu}\left(1 - \frac{D_{cu}}{d_{max}}\right) \qquad \text{(Equation 3.34)}$$

$$\frac{dD_{cu}}{dt} = RR_{cu} - RR_{ox} \qquad \text{(Equation 3.35)}$$

$$\frac{dE_{ox}}{dt} = RR_{ox} \qquad \text{(Equation 3.36)}$$

$$D_{cu} = d_2 e^{\frac{-(t-t_3)}{\tau_3}} + D_{ss}\left(1 - e^{\frac{-(t-t_3)}{\tau_3}}\right) \qquad \text{(Equation 3.37)}$$

$$E_{ox} = Y_1(t-t_3) + Y_2(D_{ss}-d_2)\left(e^{\frac{-(t-t_3)}{\tau_3}} - 1\right)$$ (Equation 3.38)

$$D_{ss} = \frac{d_{max}(r_{cu}-r_{ox})(1-\Phi_{cu})}{r_{cu}(1-\Phi_{cu})+r_{ox}\Phi_{cu}}$$ (Equation 3.39)

$$\tau_3 = \frac{d_{max}(1-\Phi_{cu})}{r_{cu}(1-\Phi_{cu})+r_{ox}\Phi_{cu}}$$ (Equation 3.40)

$$Y_1 = \frac{r_{cu}r_{ox}}{r_{cu}(1-\Phi_{cu})+r_{ox}\Phi_{cu}}$$ (Equation 3.41)

$$Y_2 = \frac{r_{ox}\Phi_{cu}}{r_{cu}(1-\Phi_{cu})+r_{ox}\Phi_{cu}}$$ (Equation 3.42)

$$t_3 = t_1 + t_2$$ (Equation 3.43)

3.4 Model Parameters

The model parameters introduced in the formulation of the model equations are described in detail below. At the end of the detailed descriptions, the parameters and the symbols used to represent them are summarized in table 3.1.

3.4.1 Model Parameters in Intrinsic Stage One

The model parameters in intrinsic stage one are as follows:

1. Planarization length: The planarization length in intrinsic stage one is denoted by L_1. It is the

length scale over which the effective electroplated copper pattern density ρ_{cu} is computed. The effective electroplated copper pattern density at any location of interest is a weighted average of the local electroplated densities (i.e., the total up-area fractions in small discretized cells) of the points that lie within a planarization length of the location in question [3]. The weights allocated to the local electroplated densities is based on their distance from the point of interest (i.e., the point at which the effective electroplated density is being computed). Thus, the planarization length in intrinsic stage one tells us the extent to which a copper CMP process can planarize the electroplated topography. The longer the planarization length, the better the planarization capability of the process in question, and the more uniform will be the polishing across different densities within the die.

Theoretically, the planarization length is the characteristic length of the deformation or long range bending of the pad in the x-y plane, under the influence of an applied force. It is believed to depend on the pad stiffness, the microscopic properties of the pad, the slurry, the process settings (such as down force, and relative speed), the CMP tool, and the properties of the material being polished (e.g. hardness of the material). It does not depend on layout or electroplated topography, but it greatly influences the evolution of the topography during CMP.

There is no direct way of computing or measuring the planarization length. Lefevre et al., proposed a methodology for obtaining the "average planarization length" for copper CMP processes from polishing experiments with a wafer scale test mask [37]. Although the length so defined is useful for comparing the planarization capabilities of different processes, it is not necessarily the same as the planarization length used in the density-step-height model. To get the planarization length for intrinsic stage one of the density-step-height model, a design of

experiment that captures the evolution of the bulk copper topography is performed, and the model equations are fitted to the data. The planarization length is the length (along with the other model parameters) that yields the minimum RMS error between the experimental data and the model equations, subject to certain constraints. This is discussed in detail later in the chapter. The planarization length for a conventional copper CMP process is typically in the millimeter range.

2. Critical height: The critical height in intrinsic stage one is denoted by H_{ex}. It is the step height above which the pressure on the down-area is zero. From the equations for step height evolution in intrinsic stage one, it is shown that the critical height is the step height above which the step height decreases linearly with time, and below which the step height decreases exponentially with time. This means that the critical height can be estimated from measured step height versus time plots. Figure 3.11 shows step height versus polish time plots for isolated copper lines with widths of 15 μm and 300 μm, respectively (the electroplated widths are the same as the etched trench widths for such wide lines).

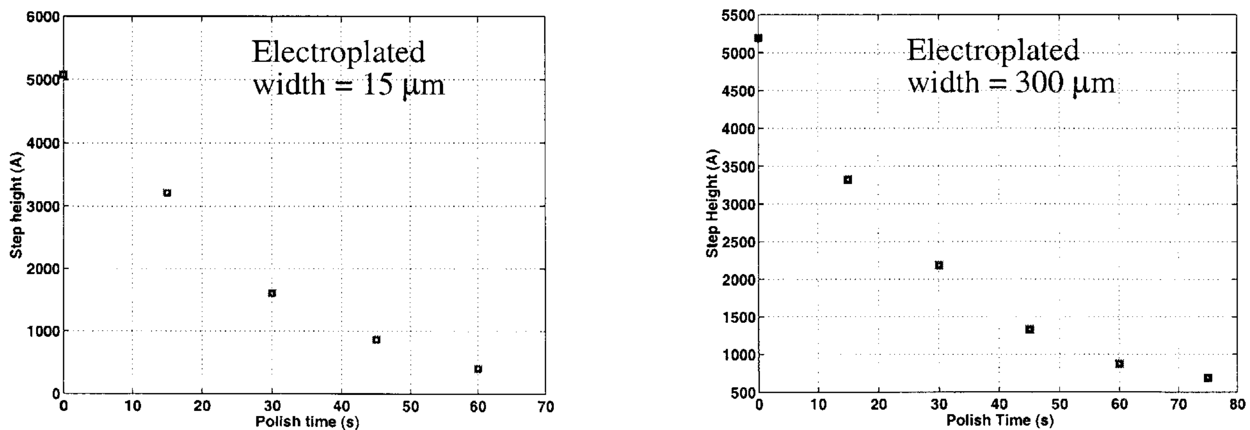


Figure 3.11: Step height reduction with polish time:

Theoretically, H_{ex} captures the extent to which the pad compresses into a down-area. It is dependent on the electroplated trench width, the electroplated spaces (up-area) surrounding a trench or the electroplated copper density surrounding the trench, the consumable set (slurry and pad), and the process settings (down force and relative speed). For a given process, the larger the electroplated trench width, the easier it is for the pad to compress into the trench and the higher the value of H_{ex}. However, data shows that as the trench width increases, the rate of increase of H_{ex} with respect to the trench width decreases. In addition, the wider the electroplated up-area surrounding the trench, the larger the value of H_{ex}. As the up-area surrounding the trench increases, the rate of increase of H_{ex} with respect to the surrounding up-area decreases.

For a given conventional CMP process, if H_{ex} is modeled as a function of the electroplated trench width and the surrounding electroplated trench space, the underlying assumption is that the length scale of the compression of the pad is very short, i.e., the compression of the pad is a local phenomena. On the other hand, if it is modeled as a function of the electroplated trench width and the effective electroplated pattern density, the underlying assumption is that the compressibility of the pad and the long range pad bending are somehow coupled. For conventional copper CMP processes, data suggests that the length scale for H_{ex} is very short. Based on the observation of experimental data, two empirical formulae expressing H_{ex} as a function of the electroplated trench width w_p (in units of microns) and the electroplated space s_p (in units of microns) are proposed in equations 3.44 and 3.45, for conventionally copper CMP processes. In these equations, A is a constant in units of angstroms and is greater than or equal to zero, α_1 and β_1 are unitless constants between zero and one, s_1 is the compression

length scale in microns (about 100 μm for conventional processes), s_o and w_o are normalization lengths equal to 1 μm, s_{min} is the effective minimum electroplated feature size in microns, and "ln" is the natural logarithm function. The dependence on the electroplated line width and space is sub-linear as dictated by experimental data.

$$H_{ex} = \begin{cases} A\left(\frac{w_p}{w_o}\right)^{\alpha_1}\left(\frac{s_p}{s_o}\right)^{\beta_1} & s_p < s_1 \\ A\left(\frac{w_p}{w_o}\right)^{\alpha_1} & s_p \geq s_1 \end{cases} \qquad \text{(Equation 3.44)}$$

$$H_{ex} = A\left(\frac{w_p}{w_o}\right)^{\alpha_1} \ln\left(\frac{s_p}{s_{min}}\right) \qquad s_p \geq s_{min} \qquad \text{(Equation 3.45)}$$

3. Effective blanket copper removal rate: The effective blanket copper removal rate is denoted by r_{cu}. It is an instantaneous as opposed to an average removal rate. In this thesis, this rate is typically set equal to the measured instantaneous blanket copper removal rate $\bar{r}_{cu}$. In cases where this is not done, the effective blanket copper rate is allowed to float, to better fit the model equations to the experimental data.

3.4.2 Model Parameters in Intrinsic Stages Two and Three

The model parameters in intrinsic stages two and three are as follows:

1. Planarization length: The planarization lengths in stages two and three are denoted by L_2 and L_3, respectively. They are the lengths used to compute the effective layout copper densities in these stages, in the same way that L_1 is used to compute the effective electroplated copper density in stage one. They indicate the planarization capability during these stages. The thin barrier is removed more rapidly in some areas of the chip than in others, due to pattern inho-

mogeniety across the die and inequality in the barrier thickness deposited within the die (e.g. the deposited barrier thickness in array regions is suspected to be much less than that in large field regions). Thus, while only barrier and copper are being polished simultaneously in a small localized region on the chip, dielectric and copper might be polishing simultaneously in a neighboring small localized region. In essence, during the barrier clearing stage, copper, dielectric, and barrier are being polished together when one looks at a larger region on the chip.

During the overpolish stage, the copper in the trench, the barrier on the side walls of the trench, and the dielectric in the space are all being polished simultaneously. Strictly speaking, therefore, in both stages two and three, copper, barrier, and dielectric are being polished at the same time, when one considers a large region (millimeter length scale) on the chip. It is therefore practical to assume for modeling purposes, that $L_2 = L_3$. This assumption is the reason why the same effective copper layout pattern density Φ_{cu} is used in both the equations for stages two and three derived earlier.

2. Effective blanket barrier and dielectric removal rates: The effective blanket barrier and dielectric removal rates are denoted by r_b and r_{ox} respectively. These rates are instantaneous as opposed to average removal rates. They must be distinguished from the measured instantaneous blanket barrier removal rate $\bar{r}_b$ and the instantaneous blanket dielectric removal rate $\bar{r}_{ox}$ respectively. They are extracted from measured pattern wafer data in some cases, and set equal to the measured instantaneous blanket removal rates, in others. This is discussed in detail in section 3.7.
3. Effective blanket copper removal rate: This is denoted by r_{cu} just as in stage one. In single step copper CMP processes, the value of r_{cu} in stages two and three is the same as that in stage one,

provided that there is no chemical interaction between the barrier and the copper that affects the rate during the barrier removal and overpolish stages.

4. Maximum dishing: The maximum dishing is denoted by d_{max}. By definition, it is the dishing at which the effective polish pressure exerted on the copper in the trench (down-area) is zero. When the effective blanket dielectric removal rate is zero, the maximum dishing is the steady-state dishing that is obtained in intrinsic stage three.

Theoretically, d_{max} captures the extent to which the pad compresses into the copper lines. It depends on the line width, the line space or density (or more generally the up-area surrounding the line in question), the consumable set (pad and slurry), and the polish process settings (down force and relative speed). For a given process, the larger the line width, the higher the dishing. This is because the pad can easily compress into, and (together with the abrasives) exert pressure on the copper line. For conventional copper CMP processes, experimental data shows that as the line width increases, the dishing rate with respect to line width decreases. This is illustrated in figure 3.12 which shows a plot of measured dishing at end-point time versus line widths, for isolated copper lines. In addition, for conventional copper CMP processes, the wider the line space surrounding a given line, the higher the

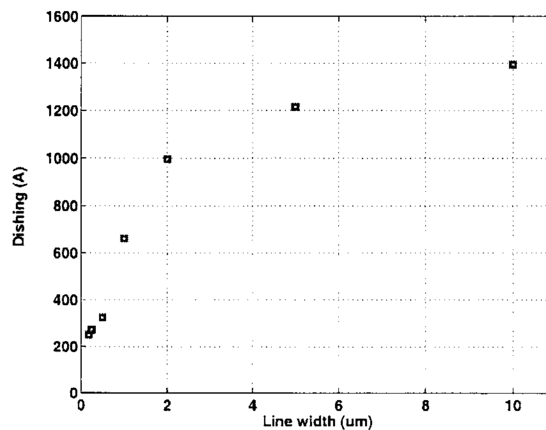


Figure 3.12: Measured dishing versus line width for isolated lines

dishing of that line. As the line space increases, the dishing rate with respect to the line space decreases. The line width and line space dependency of dishing are accounted for by d_{max}.

The dependencies of d_{max} on line width and line space, in intrinsic stage three, are similar to the dependencies of H_{ex} on electroplated line widths and spaces, in intrinsic stage one. The functional forms of the two modeling parameters should therefore be similar. However, the two parameters are not necessarily equal. For instance, a 0.25 μm isolated line dishes, meaning that such a line has a non-zero d_{max}. On the other hand, for a 0.25 μm isolated electroplated line, the value of H_{ex} is zero. If pad compression was the only factor determining the values of d_{max} and H_{ex}, the two parameters will be identically equal. Because these parameters also account for the effects of the slurry and abrasives on dishing and contact height (if any), they are therefore not necessarily equal.

To capture the sub-linear dependencies of dishing on line width and line space, for conventional copper CMP processes, the empirical relationships in equations 3.46 and 3.47 are proposed for d_{max}. Either of these functional relationships can be used to model d_{max} with good accuracy in conventional copper CMP processes. In these equations, w is the line width in microns, s is the line space in microns, w_o is the normalization line width equal to 1 μm, s_o is the normalization line space equal to 1 μm, B is a constant in angstroms and is greater than or equal to zero, α_2 and β_2 are unitless constants between zero and one, s_l is a dishing

$$d_{max} = \begin{cases} B\left(\frac{w}{w_o}\right)^{\alpha_2}\left(\frac{s}{s_o}\right)^{\beta_2} & 0 \le s < s_l \\ B\left(\frac{w}{w_o}\right)^{\alpha_2}\left(\frac{s_l}{s_o}\right)^{\beta_2} & s \ge s_l \end{cases} \qquad \text{(Equation 3.46)}$$

$$d_{max} = B\left(\frac{w}{w_o}\right)^{\alpha_2} \ln\left(\frac{s}{s_m}\right) \qquad s \geq s_m \qquad \text{(Equation 3.47)}$$

length scale (approximately 100 μm for conventional processes), s_m is the effective minimum line space in microns, and "ln" is the natural logarithm function.

3.4.3 Summary of Model Parameters

The model parameters for a single step copper CMP process described in sections 3.4.1 and 3.4.2 are summarized in table 3.1. It is important to note that each of the parameters H_{ex} and d_{max} have three sub-parameters as given in the equations relating them to line width and line space.

Table 3.1: Modeling parameters for single step copper CMP processes

Intrinsic stage one		Intrinsic stage two		Intrinsic stage three	
	Name		Name		Name
r_{cu}	Effective blanket copper removal rate	r_{cu}	Effective blanket copper removal rate	r_{cu}	Effective blanket copper removal rate
L_1	Planarization length	r_b	Effective blanket barrier removal rate	r_{ox}	Effective blanket dielectric removal rate
H_{ex}	Critical step height	L_3	Planarization length	L_3	Planarization length
		d_{max}	Maximum dishing	d_{max}	Maximum dishing

3.5 Edge Rounding

Dielectric erosion depends on pattern density and on line space, with density being the dominant factor in cases of wide regular arrays of lines (regular meaning constant line width and space for the entire array) [7]. The higher the copper pattern density, the higher the rate of

dielectric polish, and the higher the erosion. Figure 3.13 shows profilometer scans after overpolishing, for two wide regular arrays of lines. The scan on the left is for an array that has a line width of 1 μm and a line space of 1 μm. The effective layout copper pattern density at the center of this array (effective meaning density computed over the planarization length) is about 50%. The scan on the right is for an array that has a line width of 9 μm and a line space of 1 μm, with the effective layout copper density at the center of the array being close to 90%. From the two scans, it is clear that the higher the layout copper pattern density, the higher the dielectric erosion. It is important to note that in the two scans, the erosion in the field regions is negligible. Hence, the recess of the arrays relative to the field regions is approximately equal to the erosion in the arrays. Figure 3.14 shows a plot of erosion versus time for the two arrays for which profile scans are shown in figure 3.13. From this figure it is clear that the higher the pattern density, the higher the rate of erosion.

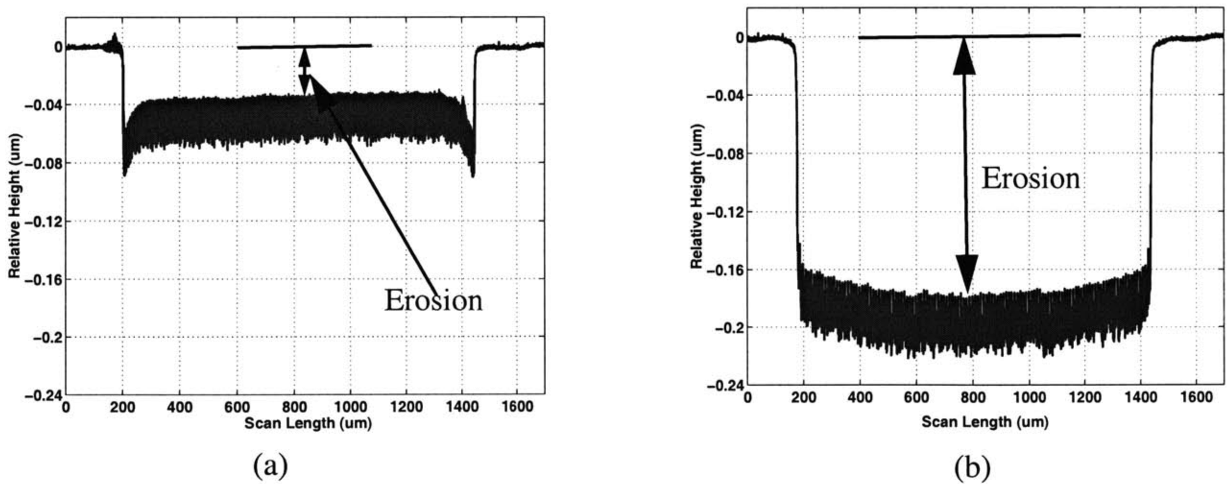


Figure 3.13: Profilometer scans of two regular arrays, showing the density effect on erosion: (a) Line width = 1 μm; line space = 1 μm; (b) Line width = 9 μm; line space = 1 μm

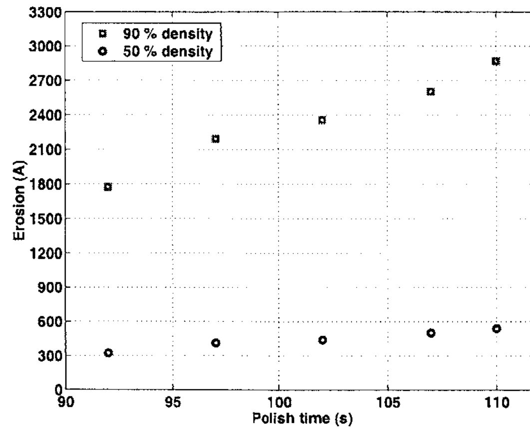


Figure 3.14: Erosion versus polish time

For a given pattern density, the smaller the line space, the higher the erosion rate and the higher the erosion. This is particularly noticeable for very narrow arrays of lines or arrays with varying line spaces. Figure 3.15 shows the profilometer scans after overpolishing, for an array with a fixed line width of 20 μm and line spaces varying from 1 μm to 100 μm. The array is narrow (about 500 μm wide) compared to the planarization length of the process. Hence, the pattern density range along the array is very small, and the density effect is therefore negligible. By observing the two scans corresponding to two different overpolish times, it is clear that the smaller the line space, the higher the erosion rate, and the higher the erosion. The larger line spaces have negligible erosion rates and negligible erosion. Figure 3.16 shows two plots of erosion versus line space for the profilometer scan shown on the right in figure 3.15. The graph on the left is plotted on a linear-linear scale, and that on the right is plotted on a linear-logarithmic scale.

The density-step-height model as formulated so far for single step copper CMP processes, fully accounts for the density dependence of erosion. However, the line space effect only shows up in the d_{max} term in the erosion equation. In essence, the line space effect is currently treated as

a second order effect. The density-step-height model parameters are extracted by fitting the model equations to the experimental data, as discussed in the model calibration methodology section

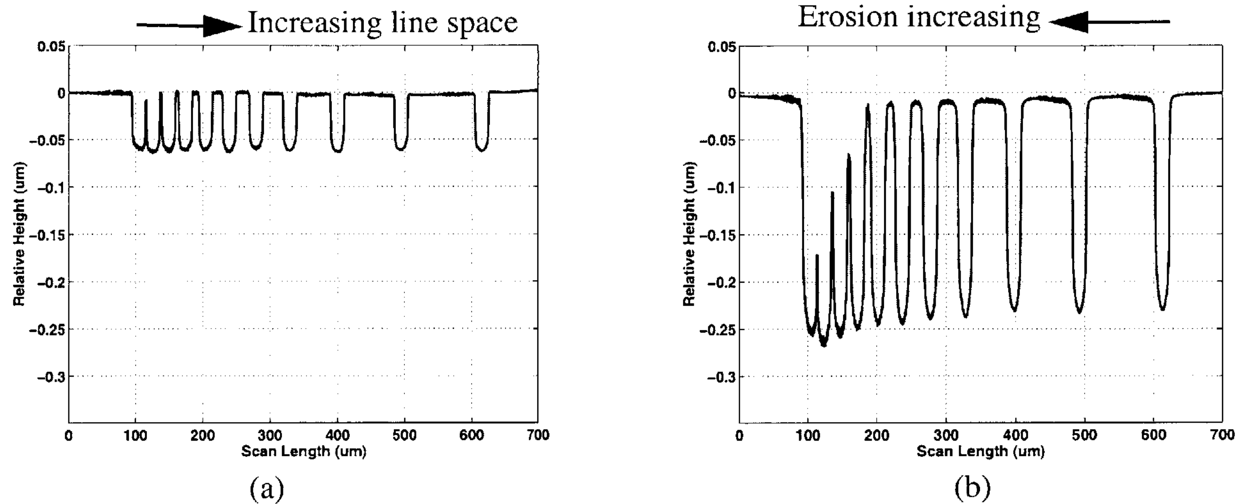


Figure 3.15: Line space effect on dielectric erosion: (a) polish time = 98 s (bulk copper cleared; just entered overpolish stage); (b) polish time = 114 s (in overpolish stage)

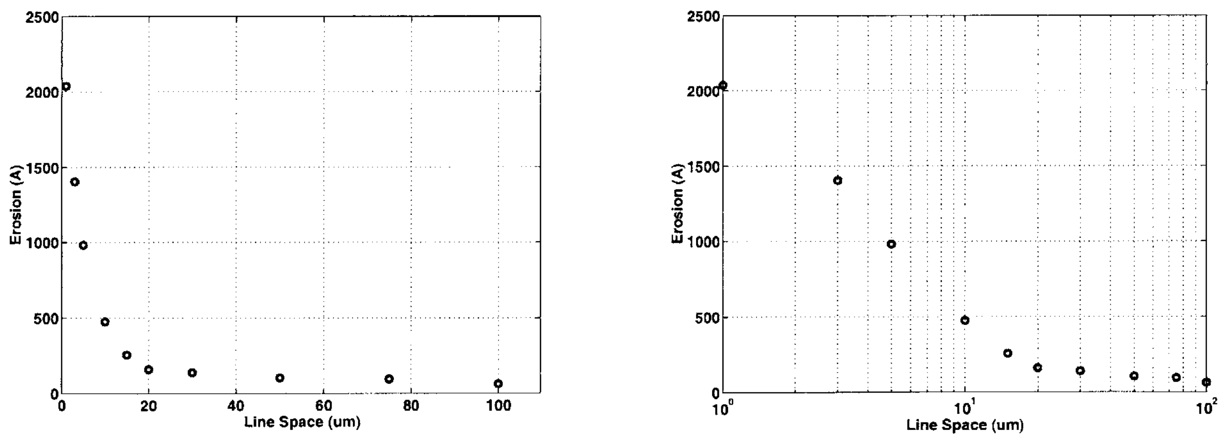


Figure 3.16: Dielectric erosion versus line space

of this chapter. If the effective blanket oxide rate is allowed to float during the extraction, the extracted value is typically much higher than the measured instantaneous blanket oxide removal rate. This happens because the floated parameter tries to account for the line space effect apparent in the erosion data. It does so by averaging the line space effect over the range of line spaces used

in the extraction. If the calibrated model is then used to predict erosion on a layout not used in the calibration process, it will over predict erosion in large field areas and possibly under predict it for very small line spaces. It is therefore necessary to properly account for the line space effect on erosion, when such an effect is significant.

The line space effect can be attributed to higher local pressure on the edge or corner of a line space (the up-area). Figures 3.17 shows the local pressure on a line space. As the line space gets smaller, the high local pressure peaks at the edges move closer together. Theoretically, when the line space becomes infinitely small, the local pressure on it will be a delta-like function. The high local pressure on the edges or corners of the line spaces lead to rounding of these spaces - a phenomena hence forth termed edge/corner rounding - and consequently to an accelerated reduction in the space thickness. The pattern density approach to computing up-area pressure misses this local pressure effect because it averages it out when it takes an average of the pressure over the planarization length.

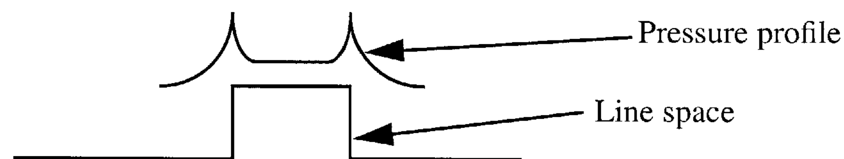


Figure 3.17: Local pressure on a line space (up-area)

Edge rounding leads to a reduction in the effective line space, and consequently an increase in the effective line width for the line neighboring the space. Thus, edge rounding decreases the total up-area, and hence the dielectric pattern density 1 - Φ_{cu} decreases. This occurs over time, suggesting that the effective layout copper pattern density Φ_{cu} could be made a function of time, to account for the line space effect. However, this is extremely difficult to do within the framework of the density-step-height model. The density-step-height model does not

say anything about how the pressure at the edge of a line space can be computed. A rigorous treatment of the edge rounding effect requires a time stepped contact wear model where the discretization is small enough to fully capture all the features on the layout. Such a model also accounts for the pattern density effect indirectly. However, it is computationally prohibitive as discussed in chapter 6 of this thesis.

A crude but simple way of dealing with the line space effect within the framework of the density-step-height model is to model the effective blanket removal rate of the dielectric (or the material experiencing this effect) as a function of line space. The empirical formula should be such that as the line space increases, the effective pattern dependent blanket removal rate decreases towards the measured instantaneous blanket removal rate. Thus, when dealing with a blanket wafer, the effective pattern dependent blanket removal rate will be very close to, or ideally equal to the measured instantaneous blanket removal rate. With this, a pattern dependent multiplicative factor ψ is used to make the effective blanket dielectric removal rate a function of line space, as given in equation 3.48, where $\tilde{r}_{ox}$ is the pattern dependent effective dielectric removal rate, and r_{ox} is the pattern independent effective blanket dielectric removal rate. A possible empirical function relating ψ to line space is proposed in equation 3.49. The parameter C is a unitless constant greater than or equal to zero, s is the line space in microns, and s_c is the edge rounding length scale in units of microns. The multiplicative factor ψ is an additional modeling parameter (when the edge rounding effect is included in the model equations) with two sub-parameters C and s_c.

$$\tilde{r}_{ox} = \psi r_{ox}$$

(Equation 3.48)

$$\psi = Ce^{\frac{-s}{s_c}} + 1 \qquad \text{(Equation 3.49)}$$

Instead of making the effective blanket dielectric (or up-area) removal rate pattern dependent, one could introduce the line space effect in the pressure versus dishing (or step-height) relationship as shown in figure 3.17, where P_1 is the applied pressure, and ψ is the line space dependent function introduced earlier. The rationale here is that ψ accounts for the local pressure

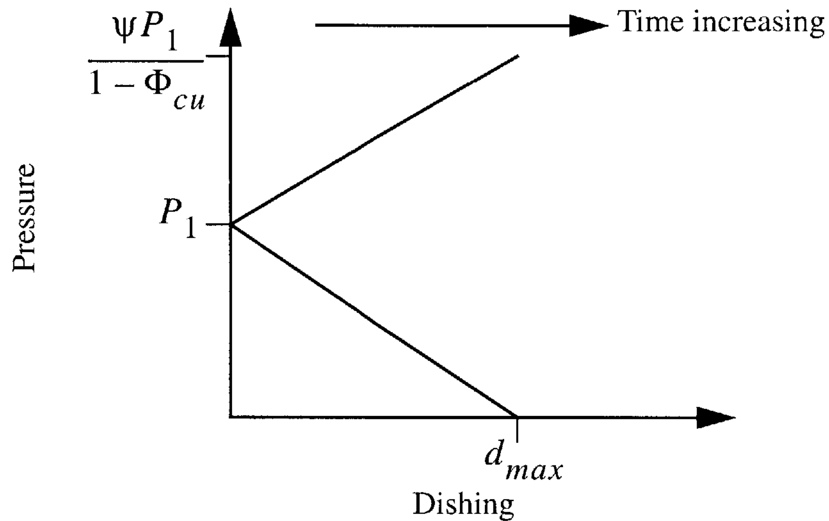


Figure 3.18: Pressure versus dishing

effect. It introduces a correction to the effective layout pattern density, due to edge rounding. Introducing ψ in the pressure versus dishing relationship or in the effective blanket removal rate yields similar results. The latter is done in this thesis to account for the edge rounding effect.

If the line space effect is due to high local pressure at the edges of the line space, then the same effect should apply to all up-areas. Indeed it does, but the extent of the edge rounding depends on the process and the material in the up-area. To avoid introducing too many modeling parameters, the edge rounding effect is only included where necessary. For instance, in the first

intrinsic step where copper is the up-area, the edge rounding effect does not seem to play a significant role.

3.6 Time Dependency of Blanket Removal Rate

In the formulation of the density-step-height model for single step copper CMP processes, the effective blanket copper, effective blanket dielectric and effective blanket barrier removal rates were introduced as modeling parameters. They were defined as instantaneous blanket removal rates. One must distinguish between average blanket removal rate and instantaneous blanket removal rate. The latter is the rate of change of the amount removed on a blanket wafer, with respect to time, while the former is the amount removed on a blanket wafer divided by the polish time. In practice, the blanket rate is often thought to be a constant. It is obtained by polishing one or two blanket wafers for sixty or more seconds, and finding the average rate. A constant blanket rate means that the amount of material removed on a blanket wafer is a linear function of time, and that the average blanket removal rate is equal to the instantaneous blanket removal rate.

To investigate the assumption of a constant blanket rate, several experiments involving polishing blanket copper wafers for different polish times, have been conducted on the Mirra. The process settings and consumable set used in these experiments are summarized in table 3.2. Each experiment is conducted on a different day, and the first experiment is repeated to study process stability. The repeated experiment is numbered four in table 3.2.

Figures 3.19 - 3.22 show plots of the amount of copper removed versus polish time, and plots of the corresponding average removal rate versus polish time, for the four experiments. The average removal rate is not a constant over time. Instead, it increases with polish time at a decreasing rate, and tends to reach a saturation value. If the average rate is not a constant, then it

means that the amount of copper removed is a non-linear function of time, and that the instantaneous blanket removal rate is also a function of time.

Table 3.2: Time dependency of blanket rate experiments

Experiment #	Platen #	Slurry	Pad	Down force (psi)	Carrier speed (= platen speed) (rpm)
1	1	EPC-5001	Stacked	5	63
2	1	EPC-5001	Stacked	2	43
3	1	EPC-5001	Stacked	4	75
4	1	EPC-5001	Stacked	5	63

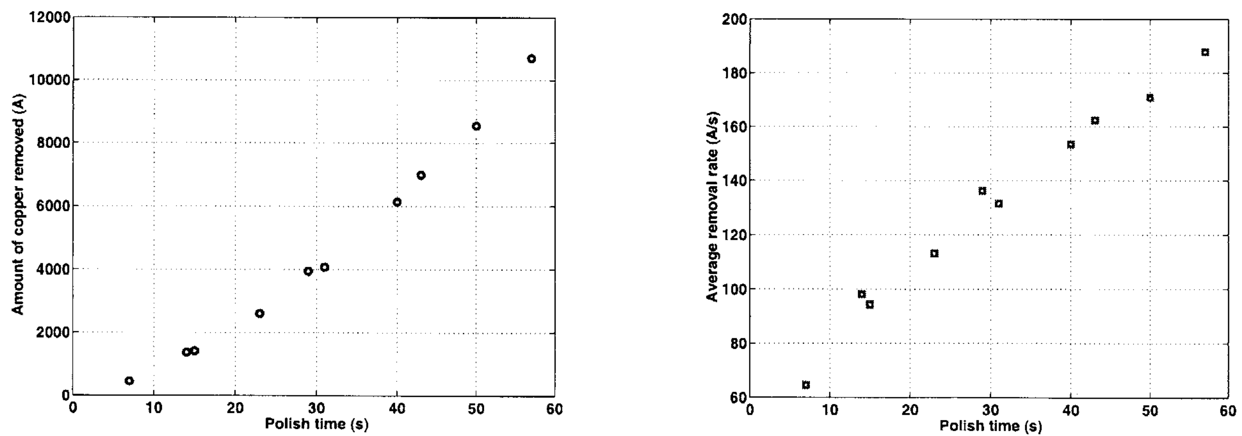
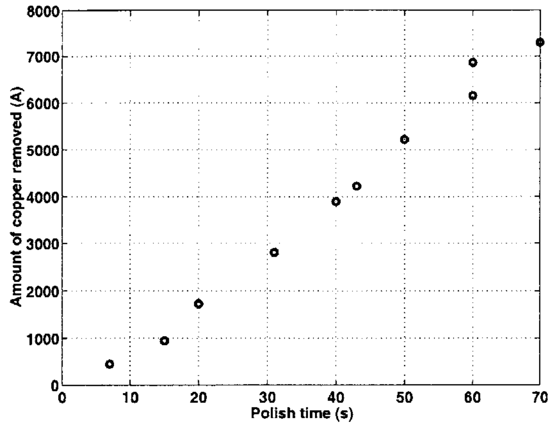


Figure 3.19: Amount of copper removed and average removal rate for experiment # 1

The apparent time dependency of the instantaneous rate complicates the model equations. It makes the removal rate diagrams snap-shots in time of the removal rate versus step-height or dishing relationships. It is therefore necessary to investigate this issue further in an effort not to add unnecessary complication to the model, or not to exclude an important effect thereby confounding the extraction of the modeling parameters.



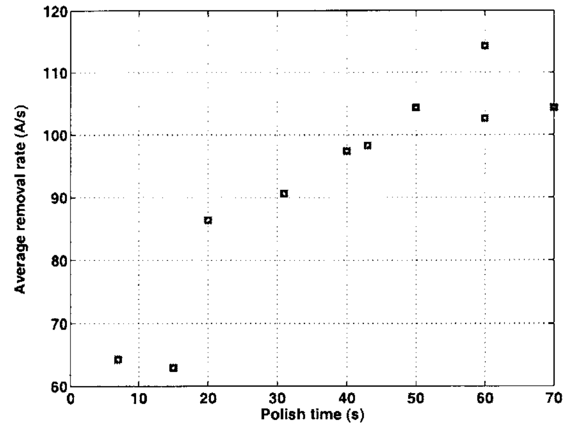
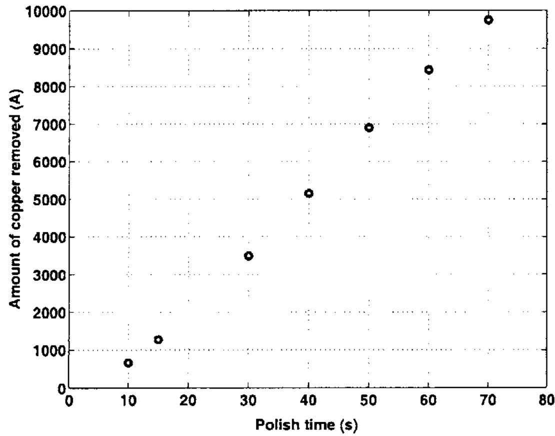


Figure 3.20: Amount of copper removed and average removal rate for experiment #2



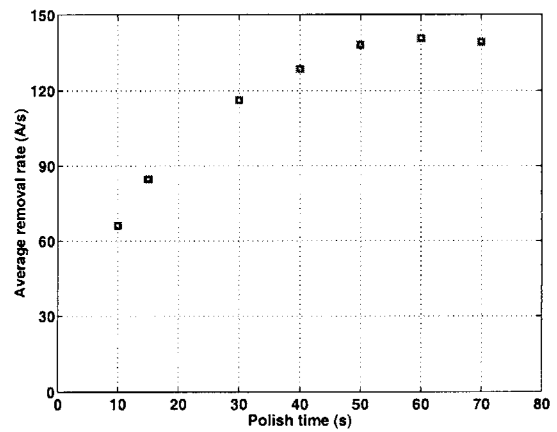


Figure 3.21: Amount of copper removed and average removal rate for experiment # 3

Park et al. [38], report the results of blanket copper wafer experiments that further study the apparent effects shown in the data presented in figures 3.19 - 3.22. Several blanket copper wafers are polished on the Mirra, and the iScan is used to measure the amount of copper removed on average across the wafer, with a time sample taken once per second. This corresponds to the instantaneous blanket removal rate [38]. They conclude that the amount of copper removed on blanket copper wafers is a non-linear function of time, and that the average and instantaneous blanket copper removal rates are functions of time. To fit the data obtained in their experiment, they propose an empirical function for the amount of copper removed on a blanket wafer (denoted

by AR) in terms of polish time t, as given in equation 3.50. The variable a_1 is a constant in units of Å/s, a_2 and a_3 are constants in units of Å, and τ is a time constant in units of seconds. By using the initial condition that the amount of copper removed is zero when the polish time is zero, the variable a_3 should equal the negative of the variable a_2. The empirical relationship given in equation 3.50 is rewritten in equation 3.51 to reflect this initial condition.

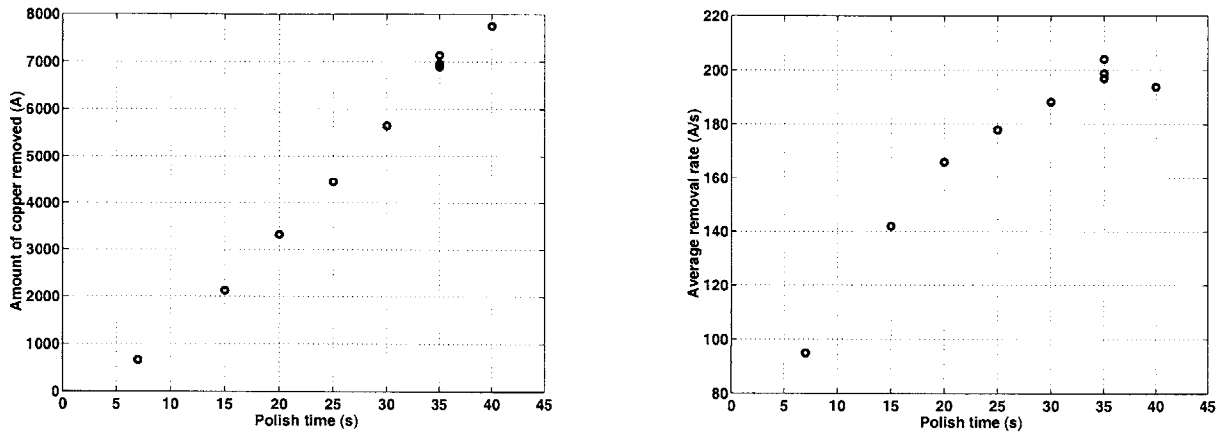


Figure 3.22: Amount of copper removed and average removal rate for experiment #4

The equation for the amount of copper removed versus time implies that as polish time tends to infinity, the amount of copper removed tends to a linear function. By dividing the left hand side and right hand side of this equation by the polish time t, the average blanket copper removal rate is obtained. This is given in equation 3.52, where r_A is the average removal rate in units of Å/s. Furthermore, by taking the derivative of equation 3.51 with respect to polish time t, the instantaneous blanket copper removal rate is obtained. This is given in equation 3.53, where r_I is the instantaneous removal rate in units of Å/s.

$$AR = a_1 t + a_2 e^{\frac{-t}{\tau_r}} + a_3 \qquad \textit{(Equation 3.50)}$$

$$AR = a_1 t + a_2 \left(e^{\frac{-t}{\tau_r}} - 1 \right) \quad \textit{(Equation 3.51)}$$

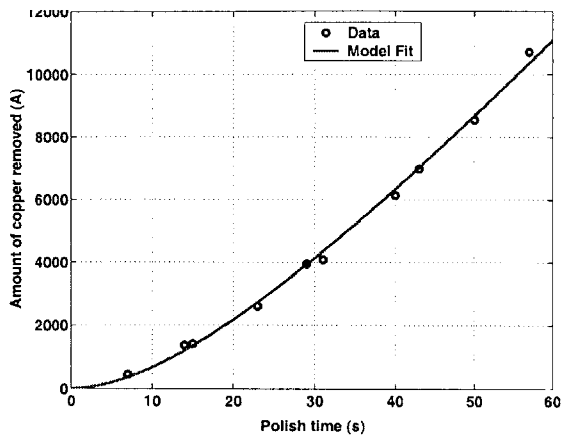
$$r_A = a_1 + \frac{a_2}{t} \left(e^{\frac{-t}{\tau_r}} - 1 \right) \quad \textit{(Equation 3.52)}$$

$$r_I = a_1 - \frac{a_2}{\tau_r} e^{\frac{-t}{\tau_r}} \quad \textit{(Equation 3.53)}$$

The equation for the instantaneous removal rate implies that at time equal to zero, the instantaneous rate is not necessarily zero. As the polish time increases, this rate exponentially approaches a saturation rate. The average removal rate is initially less than the instantaneous rate, and it increases at a decreasing rate. If polishing continues infinitely long under the same polishing conditions (e.g. the pad does not become clogged with slurry particles), the average rate approaches the saturation instantaneous removal rate. By fitting the data presented in figures 3.19 - 3.22, to the above equations, the values of the parameters a_1, a_2, and τ_r are extracted, as summarized in table 3.2. The model fits versus the measured data are shown in figures 3.23 - 3.26.

Table 3.3: Extracted blanket rate equation variables

Experiment #	a_1 (Å/s)	a_2 (Å)	τ_r (s)	RMS error (Å)
1	249.5	3986.6	16.4	168.5
2	120.0	924.0	9.71	195.5
3	159.0	1176	7.7	102.4
4	239.6	1424	6.3	137.3



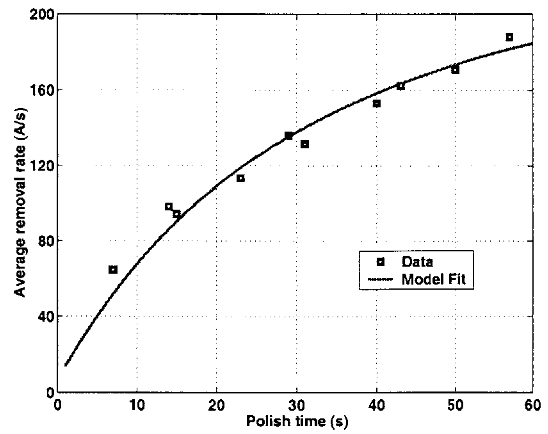
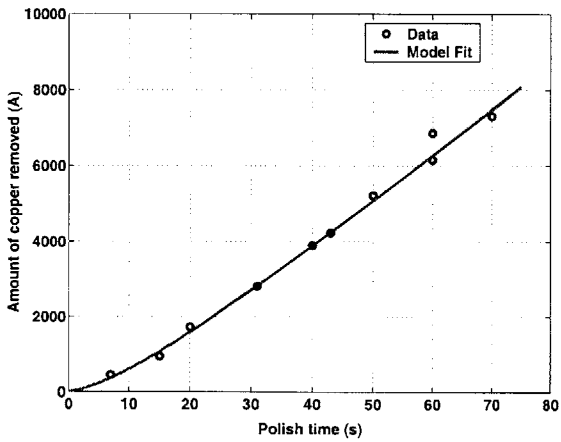


Figure 3.23: Non-linear removal rate model fit versus data for experiment #1



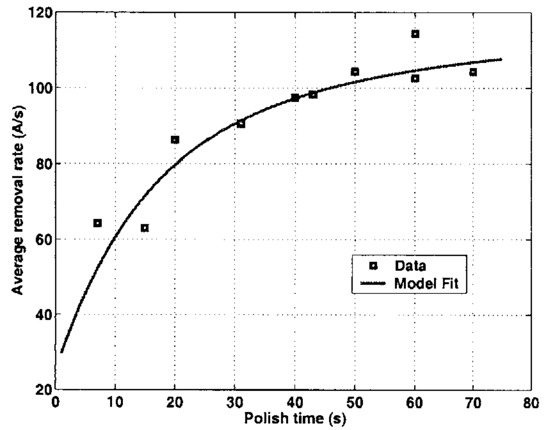
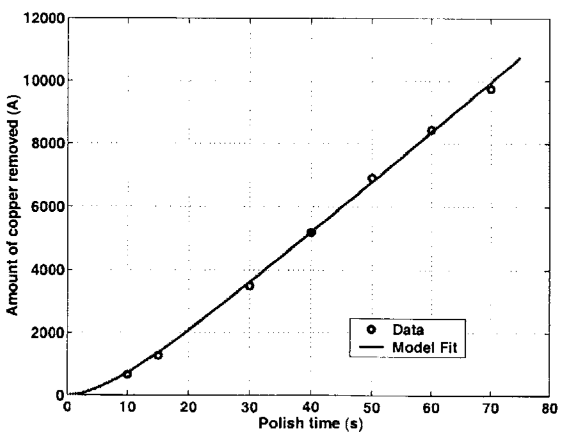


Figure 3.24: Non-linear removal rate model fit versus data for experiment # 2



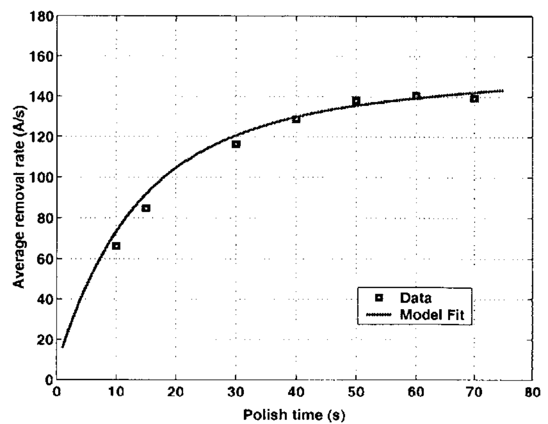
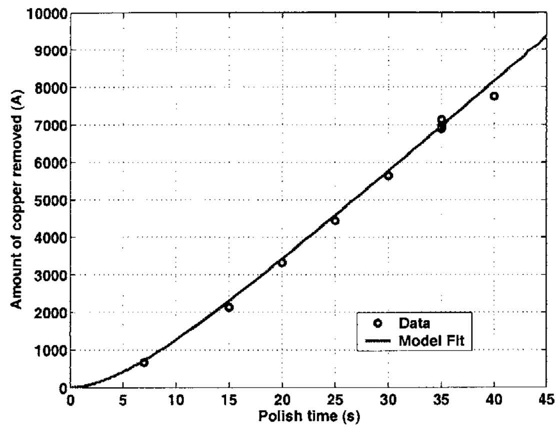


Figure 3.25: Non-linear removal rate model fit versus data for experiment # 3



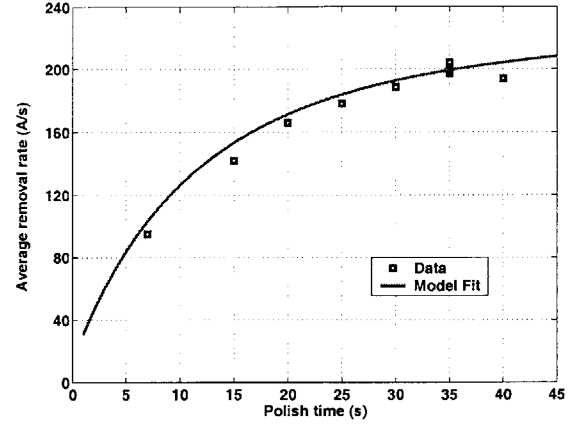
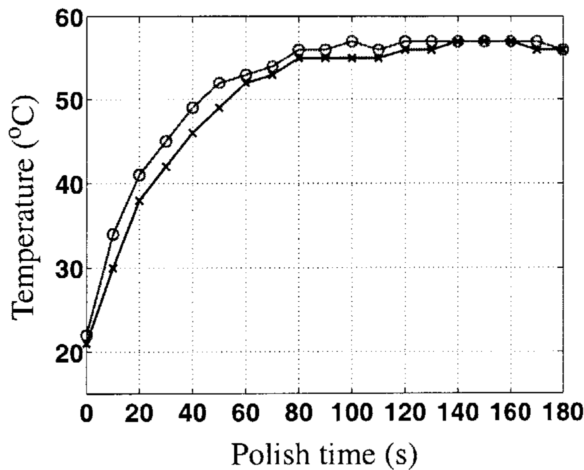


Figure 3.26: Non-linear removal rate model fit versus data for experiment # 4

To provide a physical explanation for the observed time dependency of the instantaneous removal rate, Park et al., suggest that the exponential nature of this rate might be linked to the temperature during polishing. They show a plot of temperature versus polish time illustrated in figure 3.27. The temperature tends to increase exponentially towards steady state just as the instantaneous removal rate increases exponentially towards steady state.



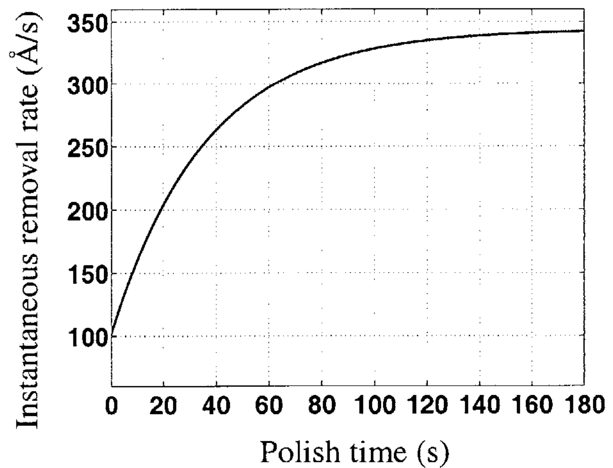


Figure 3.27: Temperature and instantaneous removal rate versus polish time

The time dependence of the instantaneous removal rate introduces additional modeling parameters (a_1, a_2, and τ_r). However, these parameters are obtained from blanket wafer experi-

-ments, as opposed to patterned wafer experiments. Hence, the additional parameters do not complicate the extraction of the other model parameters, which requires patterned wafer data. In cases where the measured instantaneous blanket removal rate is very small (< 25 Å/s), the effective blanket removal rate for the material in question is treated as a constant over time, and allowed to float in a reasonable range of values, during the extraction of the model parameters. This is usually the case for the effective blanket dielectric and barrier removal rates, in a single step copper CMP process.

Experimental data shown in chapter 5 seems to suggest that when the saturation instantaneous removal rate (denoted by a_I in this thesis) is small, that rate is achieved almost "instantaneously". It is worth mentioning that the time dependency of the instantaneous removal rate is not observed on some CMP tools.

3.7 Model Calibration Methodology for Single Step Processes

Calibrating the model for a given copper CMP process involves performing CMP experiments on blanket and patterned wafers, measuring the copper thickness, dishing, and erosion at specific sites on a die, and extracting the unknown model parameter values. The model parameter extraction criteria is the minimization of the RMS error between the model equations and the data, subject to certain constraints.

The model is formulated to capture the pattern dependent evolution of a copper CMP process. To extract the correct model parameters that achieve this goal, two things must be done. First, a test mask that contains a full range of densities, line widths and line spaces must be used to pattern the wafers. The MIT-SEMATECH 854 mask and the MIT mask version 1.2 are the most

suitable of the currently available masks for this task. Second, time split experiments must be performed with both patterned and blanket wafers. Time split experiments involve polishing several wafers for different polish times. To avoid lot to lot variation, it is recommended that all blanket wafers used in the experiment are from the same lot, and all patterned wafers are from the same lot. The different steps of the calibration procedure are described in the following sections.

3.7.1 Calibration Experiments and Measurements

Calibration experiments are conducted to capture the pattern dependent evolution of the CMP process in two of the three intrinsic stages of a single step copper CMP process. In addition, pre-CMP and post-CMP metrology is done to obtain the necessary experimental data. The experiments and measurements required for calibrating a single step copper CMP process are described below.

1. Wafer processing and first pre-CMP metrology: A short flow damascene process should be run to make patterned wafers with a suitable test mask, notably MIT-SEMATECH 854 mask or MIT mask version 1.2. The dielectric thickness after the trenches are etched and before the deposition of the barrier film, should be measured at certain array and field sites.
2. Additional pre-CMP metrology: Before conducting any CMP experiments, the material thickness on all blanket wafers (copper, barrier, and dielectric), the copper thickness at several array (if possible) and field sites on a sample of the patterned copper wafers, the step height and recess for several arrays on a sample of the patterned copper wafers, must be measured. If accurate copper thickness measurements can be obtained within arrays of lines (at up and down-area sites), the number of surface scans required will be reduced considerably. However, it is sometimes difficult to set up recipes that give accurate copper thickness measurements within arrays, and in this thesis no such measurements are used. To obtain accurate

copper thickness measurements within arrays, surface profile scans are used in combination with copper thickness measurements in large field regions, on the patterned wafers.

3. Intrinsic stage one experiments: These experiments are intended to capture the bulk copper thickness evolution. First, at least six blanket copper wafers should be polished for times ranging from 15 s to 70 or 80 s. This is intended to capture the time dependency of the instantaneous blanket copper rate. Second, at least four patterned copper wafers should be polished for different times, with the times selected to remove targeted amounts of copper thickness (on average) on each wafer. An end-point detector such as the iScan makes the task of accurately targeting a certain amount of copper thickness removed easier. To capture the stability of the removal rate during polishing, at least two blanket copper wafers should be polished between the polishing of the patterned wafers. The times of polish for these blanket wafers can be two of the times used to polish the blanket wafers in the earlier blanket wafer experiment. This will give repeated data points.

4. Intrinsic stage two experiments: It is extremely difficult, if not impossible to perform experiments that capture or isolate the evolution of the barrier clearing on patterned wafers. This is because the norminal barrier thickness deposited is typically small (200 - 250 Å). The amount sucessfully deposited on fine arrays is believed to be even smaller. Thus, there is no easy way of setting up patterned wafer experiments to target particular amounts of barrier removed on average across the wafer.

5. Intrinsic stage three experiments: The experiments in this stage are intended to capture the evolution of dishing and erosion. First, blanket barrier and dielectric wafers must be polished to obtain the blanket removal rates for these materials. By the time this stage is reached in a typical one step process, the time of polish will be long enough such that the instantaneous

removal rates of the materials being polished would have reached saturation. Thus, only three dielectric and three barrier blanket wafers should be polished for 60 s, 90 s, and 120 s respectively, or some other suitable polish times. The blanket rates of these materials is typically low for single step polishing.

After the blanket barrier and dielectric wafer experiments, at least four patterned wafers must be polished for different times including end-point time and overpolish: t_{ep}, $t_{ep} + t_0$, $t_{ep} + 2t_0$, and $t_{ep} + 3t_0$ where t_0 is based on the copper removal rate and a targeted amount of equivalent blanket copper removed. The end-point time t_{ep} is the time it takes to clear the bulk copper and expose sufficient barrier across the wafer. It is typically determined by a reflection-based end-point detector. By the end-point time, dishing and erosion of the arrays would have started. The time t_0 should be larger than the variation in end-point times for the four different wafers. In addition, it should be chosen such that excessive overpolishing is not done. Excessive overpolish can lead to extraction of the wrong model parameter values. To monitor process stability, it is recommended that at least two blanket copper wafers be polished in-between the four patterned wafers.

6. Post-CMP Metrology: When all the above experiments are complete, post CMP measurements must be done. First, the thicknesses on all polished blanket wafers must be measured. Second, the copper thicknesses at several sites on all patterned wafers with copper residues should be measured. The same sites measured before CMP, should be used for the post-CMP measurements. Third, surface scans should be taken for certain arrays on all patterned wafers with copper residue and all patterned wafers without copper residue (i.e., those that are overpolished). These arrays should be the same as those used for the pre-CMP surface scans. Finally the thickness of the dielectric in the field and some array regions of patterned wafers

without copper residue should be measured. From these measurements, copper thickness removed during the bulk copper removal stage, step height remaining during the bulk copper stage, dishing and erosion in arrays after overpolishing, and erosion in field regions after over-polishing, are obtained. This data should be filtered to remove questionable data values, and the filtered data is used to extract the model parameters.

3.7.2 Extraction of Model Parameters

Extraction of model parameters involves fitting the model equations to the measured experimental data subject to certain constraints. The constraints are intended to force the parameters to take values in a given range in accordance with the physical interpretation of these parameters. The extraction of the model parameters related to each of the three stages (with the exception of the second intrinsic stage) is done independently. The methodologies for extracting the model parameters in the three intrinsic stages are described below.

1. Extraction of model parameters in intrinsic stage one

   The measured copper thicknesses removed in the array and field regions of the patterned wafers, the measured step height remaining in the arrays of patterned wafers, the measured copper thicknesses removed on the blanket copper wafers, the local electroplated densities for the entire layout, the electroplated line widths and line spaces, are used for extraction of the intrinsic stage one model parameters. These parameters are the effective blanket copper removal rate r_{cu}, the planarization length L_1, and the critical height H_{ex}. Figure 3.28 shows a flow chart detailing the extraction procedure. The overall extraction criteria is the minimization of the RMS error between the filtered measured data and the model equations for stage one, subject to certain constraints.

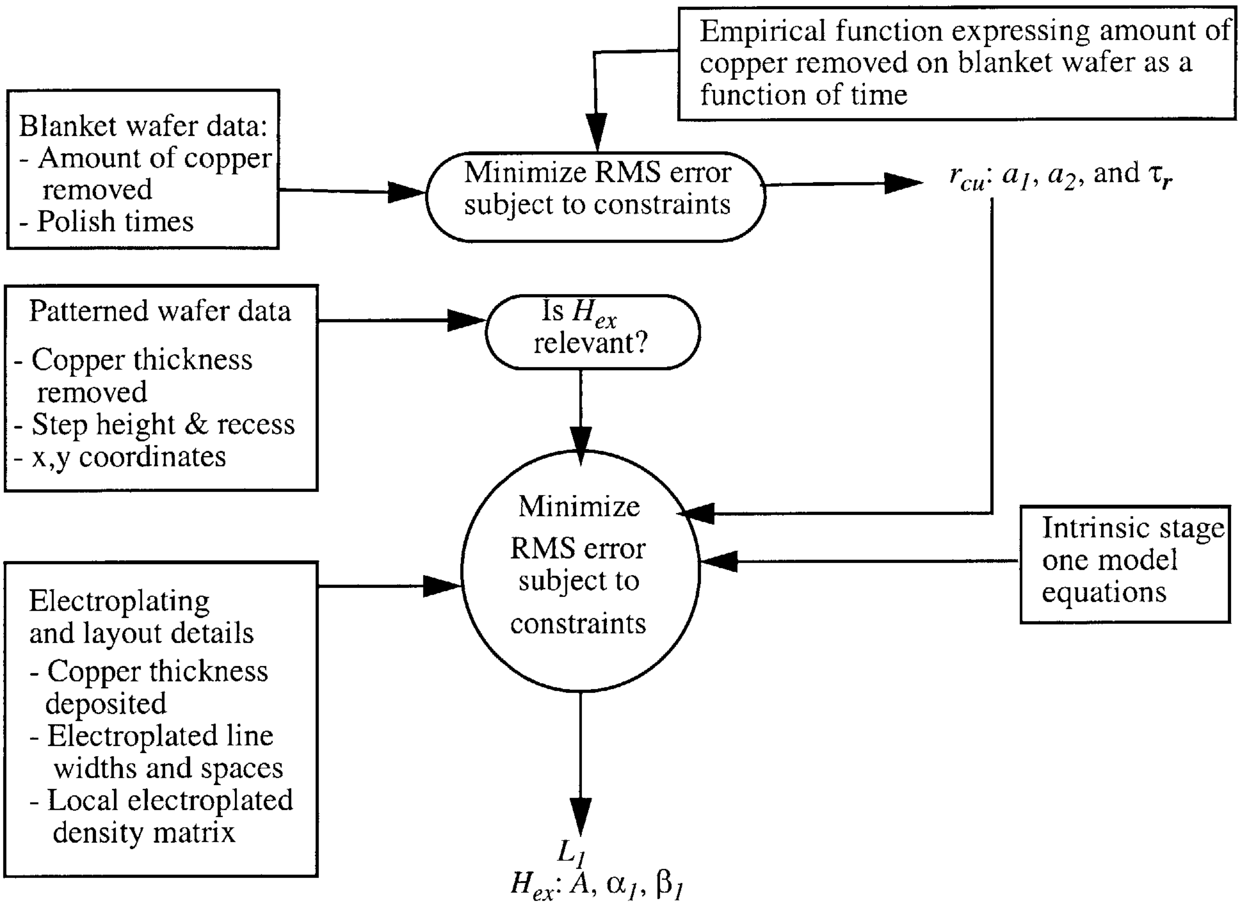


Figure 3.28: Model parameter extraction procedure for intrinsic stage one

First, the blanket wafer data is used to extract the measured instantaneous blanket removal rate effective blanket copper removal rate. This rate is a function of time as given in equation 3.53. The proposed empirical function has three unknowns (a_1, a_2, and τ_r), all of which must be extracted from blanket wafer data. The effective blanket copper removal rate is set equal to the measured instantaneous blanket removal rate.

Second, an examination of the step height data should indicate whether or not H_{ex} is significant. If the step height versus time plot for the large feature sizes (e.g. 100 μm line width and 100 μm line space) is linearly decreasing until the step height is approximately zero, then H_{ex} can be neglected. If the plot tends to change from linear to exponential at a

relatively high step height, then H_{ex} cannot be ignored. This parameter is a function of the electroplated line width and space as proposed in equation 3.44 (for conventional copper CMP processes). The function proposed has three unknowns: A, α_1, and β_1. If H_{ex} is significant, then L_1, A, α_1, and β_1, should be extracted from the patterned copper wafer data, after the effective blanket copper removal rate is extracted from blanket copper wafer data. Otherwise, only L_1 should be extracted from the patterned copper wafer data.

2. Extraction of model parameters in intrinsic stage three

The measured dishing and erosion in the array regions, the measured erosion in the field regions, the local densities of the layout in discretized cells, the extracted effective blanket copper removal rate (extracted in intrinsic stage one), the measured blanket dielectric data, and the layout line width and line space information, are all used in extracting the model parameters in intrinsic stage three. These parameters are the effective blanket copper removal rate r_{cu} (same as that extracted in stage one), the effective blanket dielectric removal rate r_{ox}, the planarization length L_3, the maximum dishing parameter d_{max}, and the edge rounding factor ψ (if necessary). Figure 3.29 shows a flow chart detailing the extraction procedure in intrinsic stage three. The measured dishing and erosion at end-point time (or the lowest polishing time in the stage three experiments) are used as initial conditions. The sum of squared errors between the model equations for intrinsic stage three and the rest of the dishing and erosion data is minimized, subject to certain constraints.

The maximum dishing parameter is a function of line width and line space, as proposed in equation 3.46. The analytic function proposed has three unknowns: B, α_2, and β_2. In addition, the edge rounding factor ψ is a function of line space, as proposed in equation 3.49. The

function proposed has two unknowns: C and s_c. Hence, a total of seven parameters (excluding the blanket copper removal rate which is already known from stage one) need to be extracted.

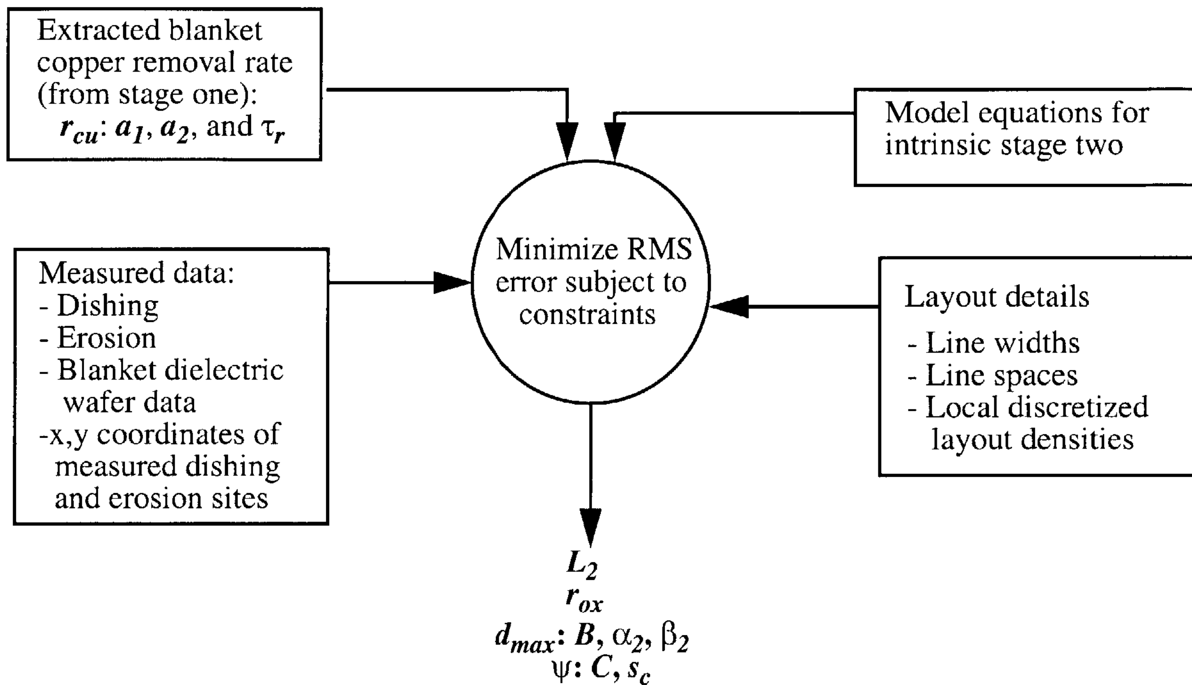


Figure 3.29: Model parameter extraction procedure for intrinsic stage three

It is important to note that the measured instantaneous dielectric removal rate (i.e. the rate extracted from blanket dielectric wafer data) is typically very small in single step copper CMP processes. It is therefore recommended that the effective blanket dielectric removal rate be treated as an unknown constant, and this constant value is one of the seven parameters that are extracted from the patterned wafer data. When the edge rounding effect is included in the model equations, the constant extracted effective blanket dielectric rate tends to be closer to the measured instantaneous blanket dielectric removal rate.

3. Extraction of model parameters in intrinsic stage two

The model parameters for intrinsic stage two are obtained from the extracted parameters in stages one and three, and the measured blanket barrier and dielectric data. The planarization

length and the maximum dishing parameter are the same in stages two and three as discussed in section 3.4.2. In addition, the effective blanket copper removal rate in stage two is equal to that in stages one and three. If edge rounding is taken into consideration, it is assumed that the barrier film experiences the same edge rounding phenomena as the dielectric film, given that they are both up-areas in a single step process. Hence, the edge rounding factor ψ is the same in stages two and three. The only remaining unknown parameter in stage two is the effective blanket barrier removal rate r_b.

Using the extracted model parameters in stage three, the times at which the barrier is cleared at the array and field sites can be computed. These times correspond to the times when erosion is equal to zero at the sites of interest. In addition, the dishing at the array sites for these times can also be computed. Using the extracted model parameters in intrinsic stage one, the times at which the bulk copper is cleared at the array and field sites, and the values of any pre-dishing that occurs when the bulk copper is just cleared at the array sites, can be computed. These computed values should be sufficient to estimate the effective blanket barrier removal rate r_b.

The procedure outlined above to estimate the effective blanket barrier removal rate is idealistic and impractical. The thinness of the barrier film, the lack of knowledge of the exact barrier film thickness (especially in the array regions), extraction errors in stages one and three, and random errors in the measured data, often make the computed values inconsistent. The computed time when the barrier is cleared can be less than the computed times when the bulk is cleared at the same sites. This is inconsistent because the times when the barrier is cleared at all sites should equal the clearing time of the bulk at such sites plus the time it takes to clear the barrier at the same sites. To avoid this inconsistency, it is recommended to use a

first order approximation based on measured to extracted blanket removal rate ratios, to extract the effective blanket barrier removal rate. It is assumed that the ratio of the measured to extracted blanket dielectric removal rate in stage three, is equal to the ratio of the measured to extracted blanket barrier removal rate ratio in stage two. This assumption is mathematically expressed in equation 3.56, where $\bar{r}_{ox}$ is the measured instantaneous blanket oxide removal rate, r_{ox} the extracted effective blanket dielectric removal rate, $\bar{r}_b$ the measured instantaneous blanket barrier removal rate, and r_b the extracted effective blanket barrier removal rate. One of the constraints used in the extraction of the effective blanket dielectric removal rate ensures that the effective blanket barrier removal rate extracted as in equation 3.54 is less than the extracted effective blanket copper rate (recall that a typical single step copper CMP process uses a slurry and process settings that have a higher blanket copper removal rate than the blanket barrier removal rate).

In this thesis, it is assumed that the barrier film is removed instantaneously in array regions because the exact initial thickness of the barrier in these regions is usually unknown. Thus, the clearing of the barrier is only an issue in large field regions where it is known that the initial barrier thickness is equal to the norminal deposited barrier thickness.

$$\frac{r_{ox}}{\bar{r}_{ox}} = \frac{r_b}{\bar{r}_b} \qquad \textit{(Equation 3.54)}$$

3.7.3 Checking the Accuracy of the Model Parameter Extraction Procedures

The model parameters in intrinsic stages one and three are extracted independently using different data sets. To check the accuracy of the extraction procedure, at least two things must be done. First, the extraction in each stage (stages one and three only) must be checked for accuracy

independently. In stage one, this means using the extracted model parameters to predict the copper thicknesses at the field and array sites not used in the model parameter extraction procedure. In stage three, it means using the extracted model parameters to predict the dishing and erosion values at the array sites, and the erosion at the field sites, not used in the extraction of the stage three model parameters. It is important to not use the data for all measured sites, for extraction of model parameters, if possible.

Second, a full simulation of the entire process should be done. The extracted model parameters in all three intrinsic stages are used to simulate the time to clear the bulk, the dishing and erosion at several sites on the die. The dishing and erosion simulation results should be compared to the measured dishing and erosion. Running a full simulation involving all the intrinsic stages is a good way of testing how well the model parameters, extracted independently in the stages, fit together to capture the pattern dependent evolution of the entire process.

3.8 Model Fits versus Experimental Data

In this section, we test the derived model and the proposed calibration methodology for single step copper CMP processes against experimental data. Two sets of single step copper CMP process experiments are used for this purpose. These two sets of experiments use the same polish process settings, the same slurry, but different types of pads. The dielectric used is oxide and the barrier used in tantalum nitride (TaN). Unfortunately, at the time these single step copper process experiments were performed, there was no access to equipment for accurately measuring copper thickness on patterned wafers. Furthermore, no end-point sensor was available to conduct polish experiments to capture the bulk copper clearing process. Thus, only overpolish patterned wafer

experiments, and blanket wafer experiments were done. The details of the experiments are given in tables 3.4 - 3.8.

With no experimental data for extracting the model parameters in stage one, the emphasis in this section is on extracting stage three model parameters only. The accuracy of the extraction in stage three is tested by using the extracted parameters to predict the dishing and erosion amount for the test structures not used in the extraction procedure (where data is available for such structures). Extraction of intrinsic stages one and two parameters and a full simulation of the entire process will be done when the model is applied to multi-step copper CMP processes in chapter 5.

Table 3.4: Experimental description

Experi-mental set #	Test mask set	Tool	Pad	Slurry	Down force (psi)	Speed (rpm)	Slurry flow rate (ml/min)
1	854	Mirra	Stacked	EPC-5001	4	75	175
2	854	Mirra	Solo	EPC-5001	4	75	175

Table 3.5: Blanket wafer experiments in experimental set # 1

Wafer #	Wafer type	Polish time (s)
C-1	Copper	10
C-2	Copper	15
C-3	Copper	30
C-4	Copper	40
C-5	Copper	50
C-6	Copper	60
C-7	Copper	70
B-1	Barrier	90
B-2	Barrier	120
D-1	Oxide	90
D-2	Oxide	120

Table 3.6: Patterned copper wafer experiments in experimental set # 1

Wafer #	End-point time (s)	Total polish time (s)	Wafer status after CMP
P-1	N/A	92	Overpolished
P-2	97	97	Overpolished
P-3	97	102	Overpolished
P-4	97	107	Overpolished

Table 3.7: Blanket wafer experiments in experimental set # 2

Wafer #	Wafer type	Polish time (s)
C-8	Copper	12
C-9	Copper	18
C-10	Copper	26
C-11	Copper	36
C-12	Copper	53
C-13	Copper	64
C-14	Copper	79
B-3	TaN	90
B-4	TaN	120
D-3	Oxide	90
D-4	Oxide	120

Table 3.8: Patterned copper wafer experiments in experimental set # 2

Wafer #	End-point time (s)	Total polish time (s)	Wafer status after CMP
P-5	153	153	Overpolished
P-6	153	158	Overpolished
P-7	153	164	Overpolished
P-8	153	173	Overpolished

3.8.1 Model Parameter Extraction in Intrinsic Stage Three, for Experimental Set # 1

Using the extraction procedure described earlier, the model parameters are extracted for two cases: No edge rounding taken into account, and edge rounding taken into account. The functionality used for d_{max} is as given in equation 3.46, and that used for ψ when edge rounding is taken into account is as given in equation 3.49. The effective blanket dielectric removal rate is treated as a constant, and it is allowed to float in a small range that includes the measured instantaneous blanket dielectric removal rate.

The analysis of blanket wafer data given in equations 3.53 and 3.54 is applied to the measured blanket copper data, to extract the effective blanket copper removal rate (the effective blanket copper removal rate is set equal to the measured instantaneous blanket copper removal rate). The extracted effective blanket copper removal rate r_{cu} is given in table 3.9.

The array sites on the MIT-SEMATECH 854 mask used in the extraction of the planarization length L_3, the maximum dishing d_{max}, the effective blanket dielectric removal rate r_{ox}, and the edge rounding factor ψ, are indicated on the mask in figure 3.30. The values of the extracted model parameters are summarized in table 3.9, and the fits between the model equations and the measured data for the array sites used in the extraction procedure are illustrated in figures 3.31 - 3.32. It is clear from the table 3.9 that when the edge rounding factor ψ is not included in the model equations, the extracted effective blanket dielectric removal rate is almost six to ten times the measured blanket dielectric rate (the measured rate is less than 1 Å/s). As explained earlier, the model equations compensate for the absence of this factor by averaging the edge rounding effect over the available line space range and including the averaged effect in the extracted value of r_{ox}. This leads to a minimum RMS error between the data and the model

equations.

Table 3.9: Extracted model parameters in intrinsic stage three, for experimental set # 1

r_{cu} (Å/s)			r_{ox} (Å/s)	L_3 (μm)	d_{max} (Å)			ψ		RMS Error (Å)
a_1 (Å/s)	a_2 (Å)	τ_r (s)			B (Å)	α_2	β_2	C	s_c (μm)	
159	1176	7.7	4.34	1309	294.2	0.303	0.292	N/A	N/A	107
159	1176	7.7	2.22	1498	333.0	0.303	0.259	3.04	22.5	70

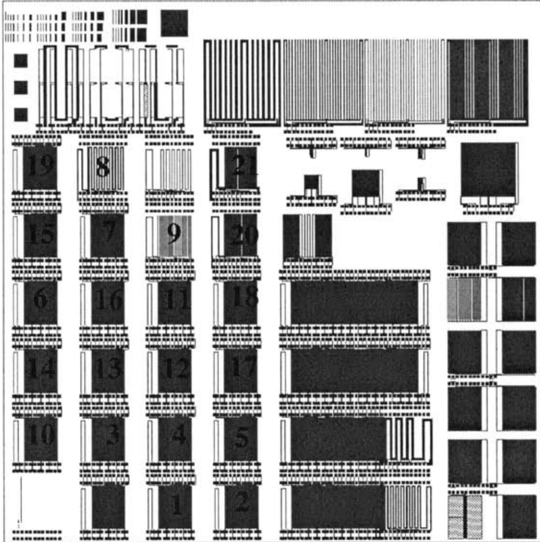


Figure 3.30: Array sites used in the extraction of model parameters for stage three

To test the accuracy of the extraction, the extracted model parameters for stage three are used to predict the dishing and erosion for several array sites not used in the extraction procedure. These array sites are numbered on the test mask used, in figure 3.33. The measured dishing and erosion at the minimum polish time are used as the initial condition in intrinsic stage three, for predicting the dishing and erosion at other polish times in intrinsic stage three. The predicted results match the measured data well as shown in figures 3.34 - 3.35.

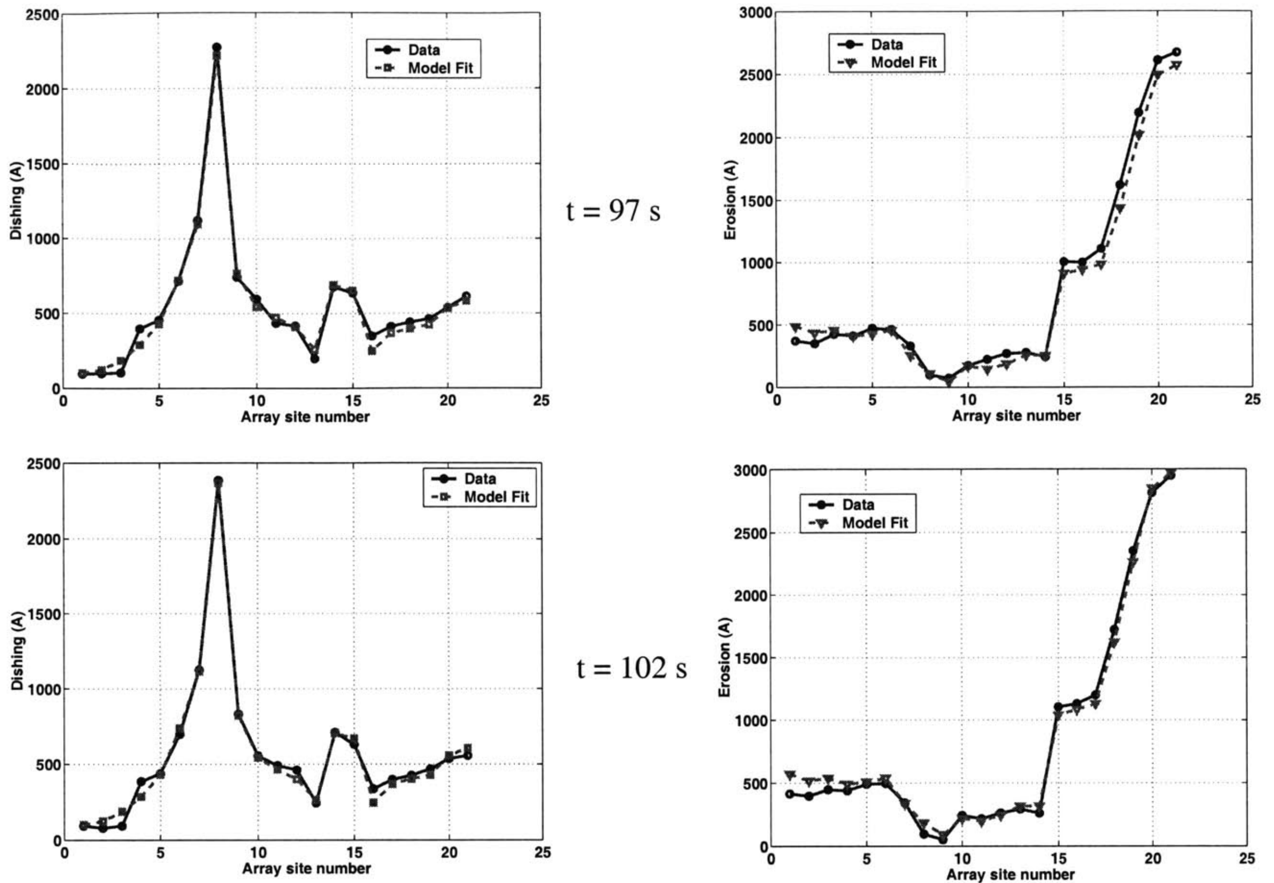


Figure 3.31: Model fit versus data for experiment set # 1, for extraction without edge rounding

3.8.2 Model Parameter Extraction in Intrinsic Stage Three for Experimental Set # 2

The extracted model parameter values for experimental set # 2 are summarized in table 3.11. The blanket copper wafer data is used to extract the effective blanket copper removal rate r_{cu}, with the same methodology applied to the data for experimental set # 1. The same array sites used in experiment set # 1 are used in the extraction of the model parameters for experimental set # 2. Figures 3.40 - 3.41 show the model fits versus the data for the array sites used in the extraction.

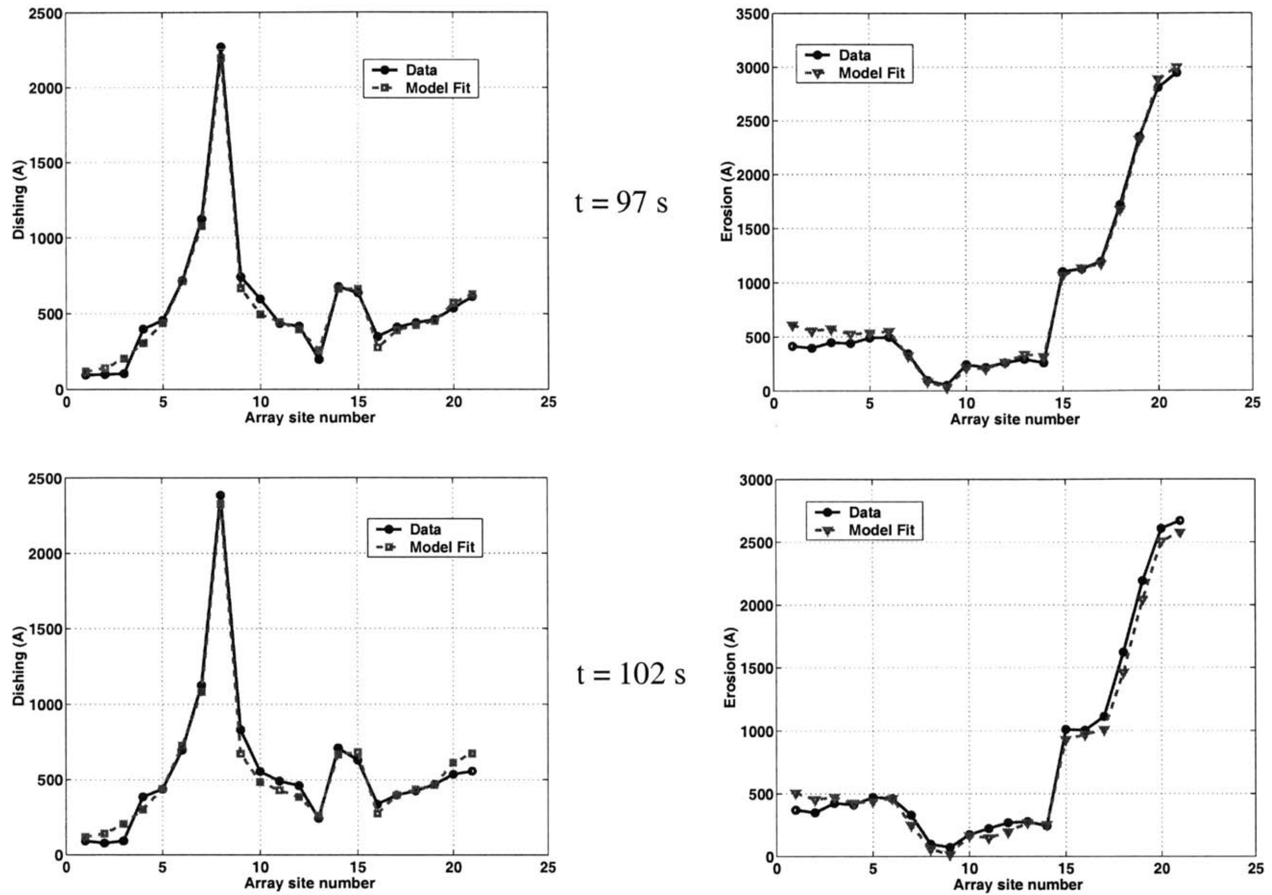


Figure 3.32: Model fit versus data for experimental set # 1, for extraction with edge rounding

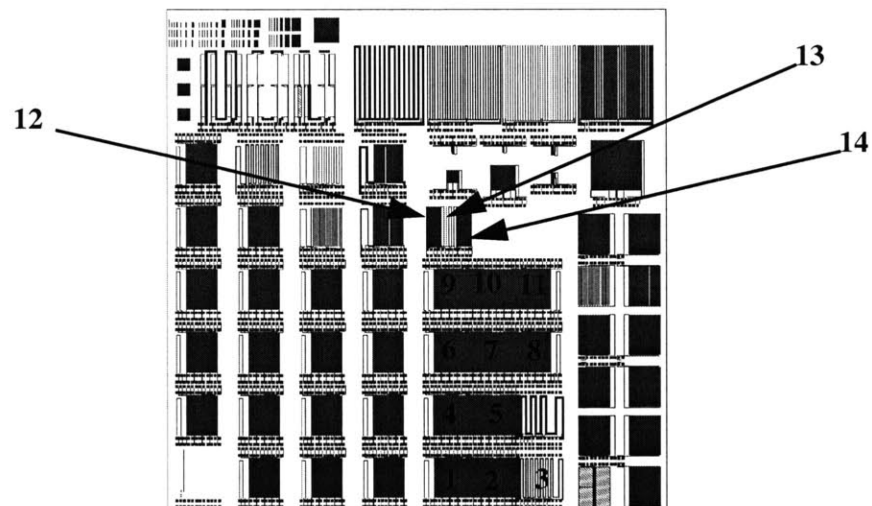


Figure 3.33: Array structures used in testing the accuracy of the extraction in stage three

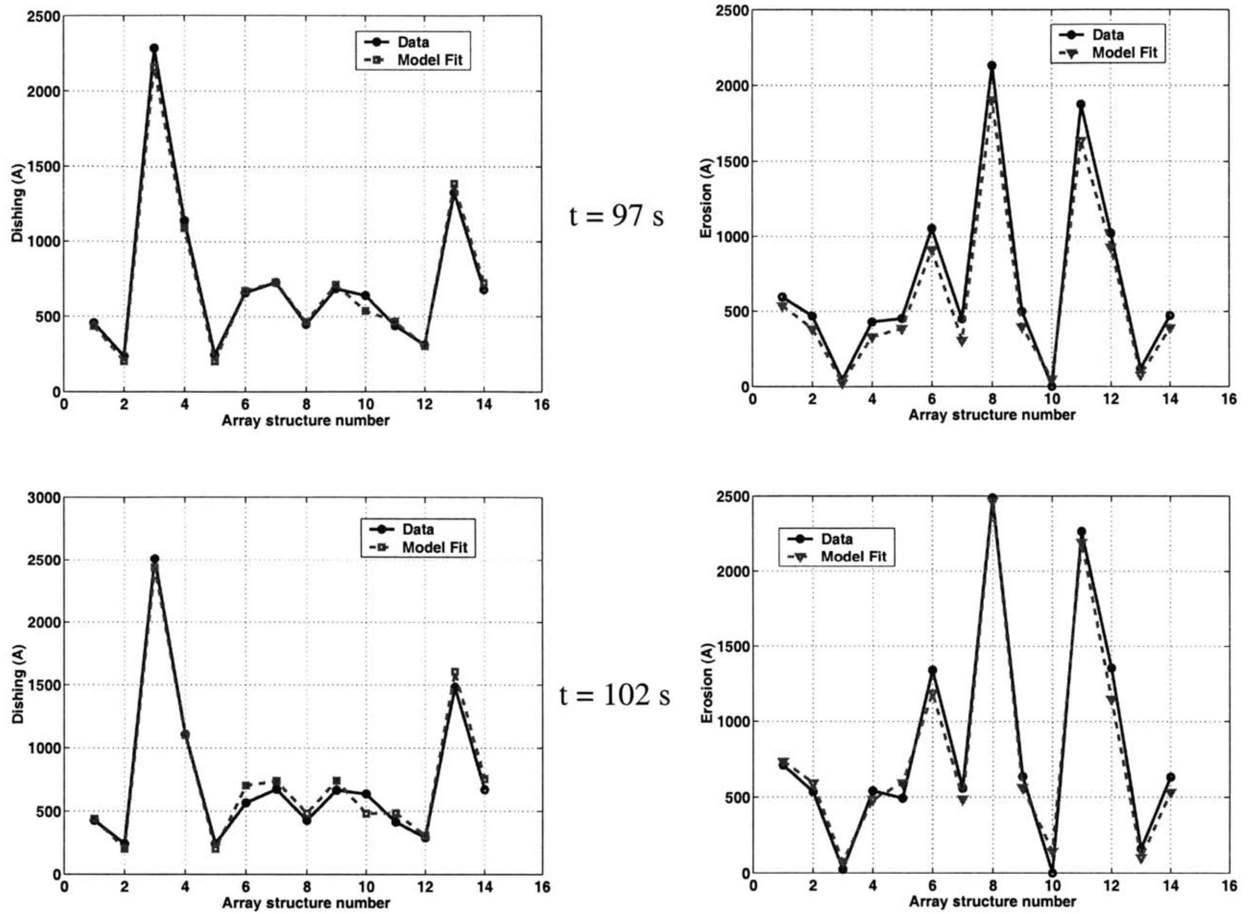


Figure 3.34: Model prediction versus data in experimental set # 1, to test the accuracy of the extraction (with the edge rounding effect included) procedure in intrinsic stage three

Table 3.10: Intrinsic stage three extracted model parameter values for experimental set # 2

r_{cu} (Å/s)			r_{ox} (Å/s)	L_3 (μm)	d_{max} (Å)			ψ		RMS Error (Å)
a_1 (Å/s)	a_2 (Å)	τ_r (s)			B (Å)	α_2	β_2	C	s_c (μm)	
115	2373	15.0	4.34	1385	337.0	0.174	0.240	N/A	N/A	74
115	2373	15.0	0.9	1529	372.4	0.188	0.185	7.4	15.4	46

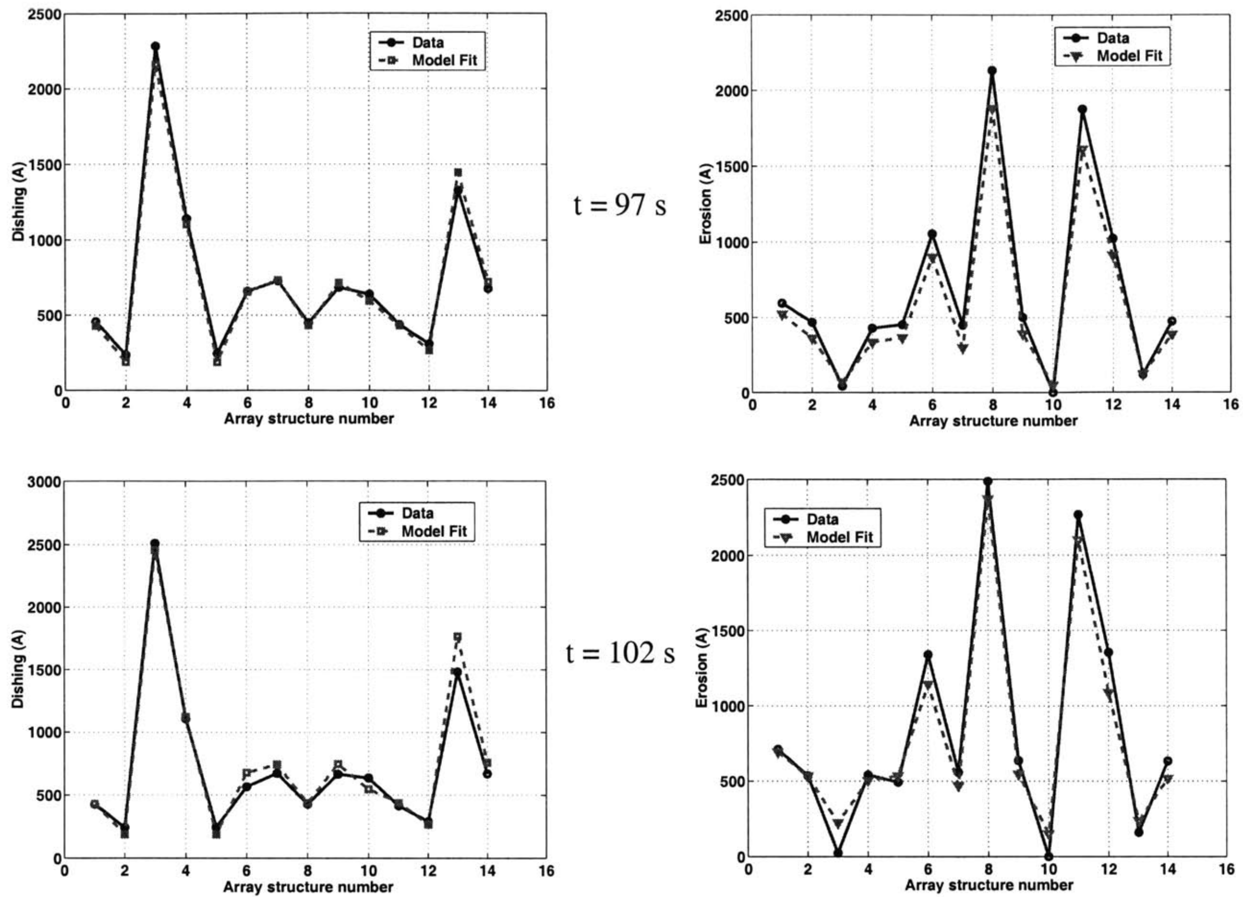


Figure 3.35: Model prediction vs. data in experimental set # 1, to test the accuracy of the extraction (with the edge rounding effect neglected) procedure in stage three

3.9 Limitations of the Density-step-height Model

The density-step-height model as formulated in this chapter ignores some effects observed from experimental data. Hence, it cannot be used to explain these effects or any impacts they might have on dishing and erosion. Two of the limitations of the density-step-height model are discussed in sections 3.9.1 and 3.9.2, with suggestions of how these effects can be included in the framework of the model.

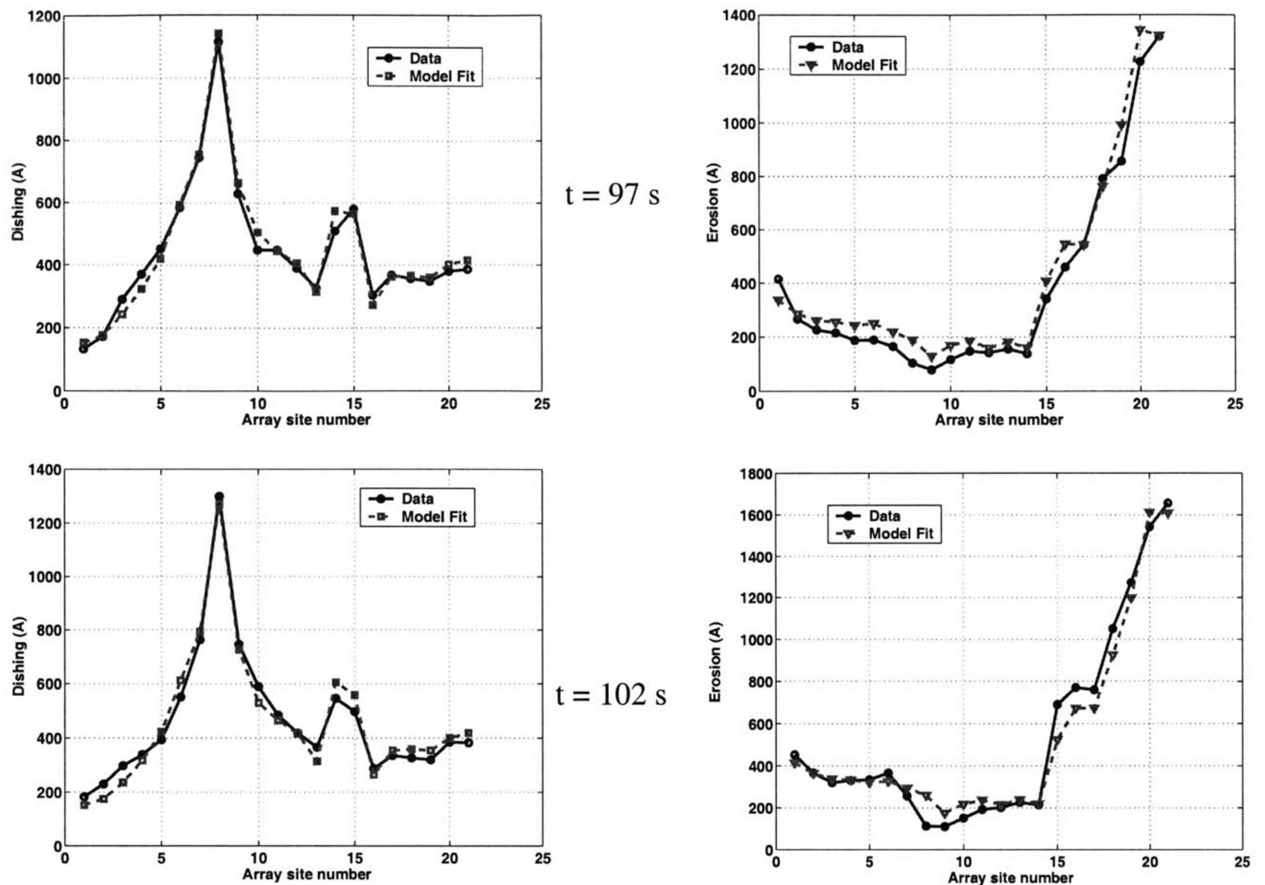


Figure 3.36: Model fits versus data (experimental set # 2) for extraction without edge rounding, in stage three

3.9.1 The "Ear" or "Array-edge" Effect

In conventional copper CMP processes, data shows that erosion at the edge of an array is sometimes greater than erosion at the center of the array. This effect which is termed the "ear effect" or the "array-edge" effect in this thesis, is particularly prevalent for small feature and low density array structures surrounded by large field areas. Figure 3.38 shows a profilometer scan for an array, where the array-edge or ear effect is present.

There are very few publications in the CMP literature that specifically mention this effect [1, 6]. In one of these publications, the ear effect is attributed to pad rebounding [6]. However, this view is not supported by experimental data. When a different slurry is used with the same pad,

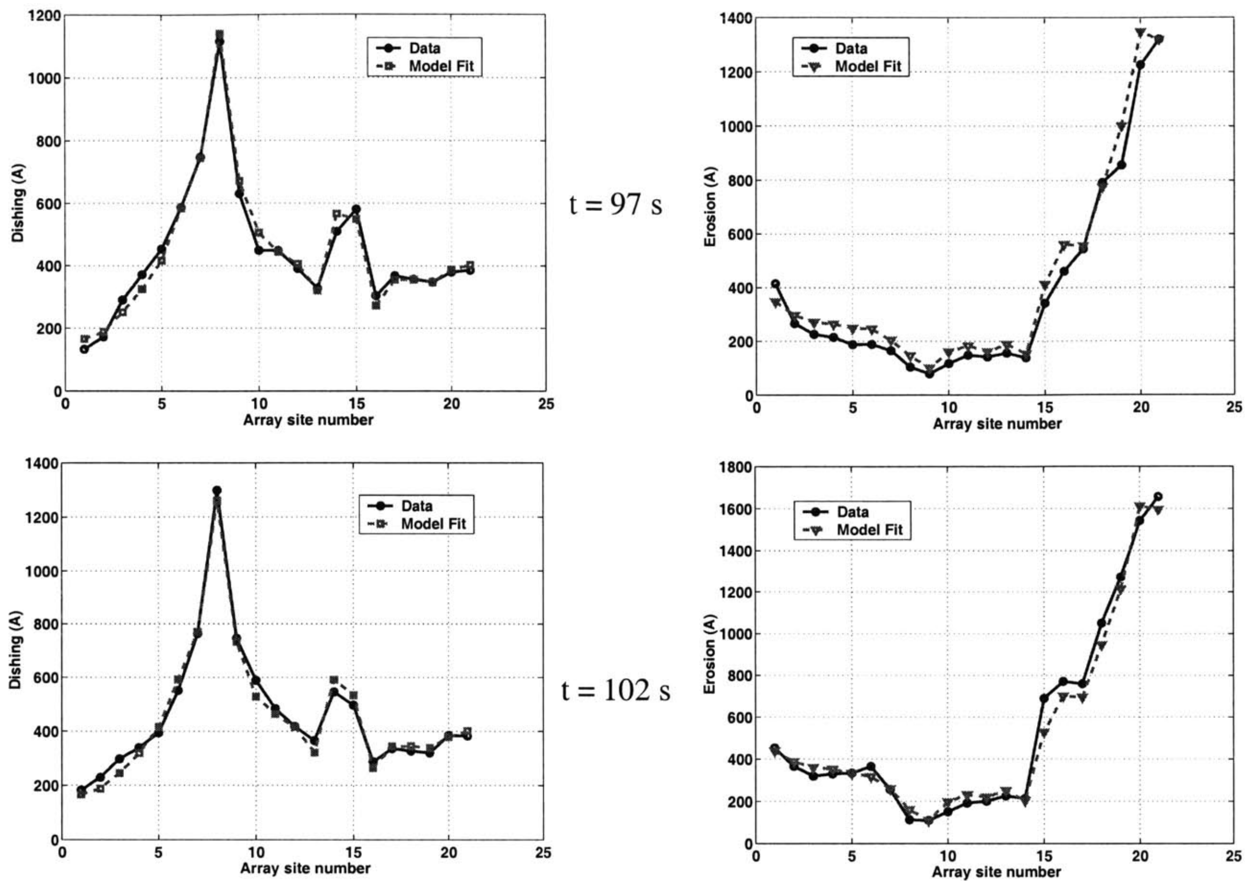


Figure 3.37: Model fits versus data (experimental set 2) for extraction with edge rounding, in intrinsic stage three

this effect is not observed. For example, the Hitachi and the Fujimi copper CMP slurries do not show this effect. Experimental data for the Hitachi slurry is shown in chapter 4.

The ear effect seems to be pattern dependent. While it occurs for small feature, low to medium density array structures, it is not observed on high density array structures. For high density array structures, the center of the array erodes more than the edge. This is purely due to the density effect, according to the density-step-height model. Figure 3.39 shows a profilometer scan of a high density array (9 μm line width, and 1 μm line space). The ear effect is not present for this array. In addition, it has been privately reported that this effect is not observed when dummy fills are inserted into a layout.

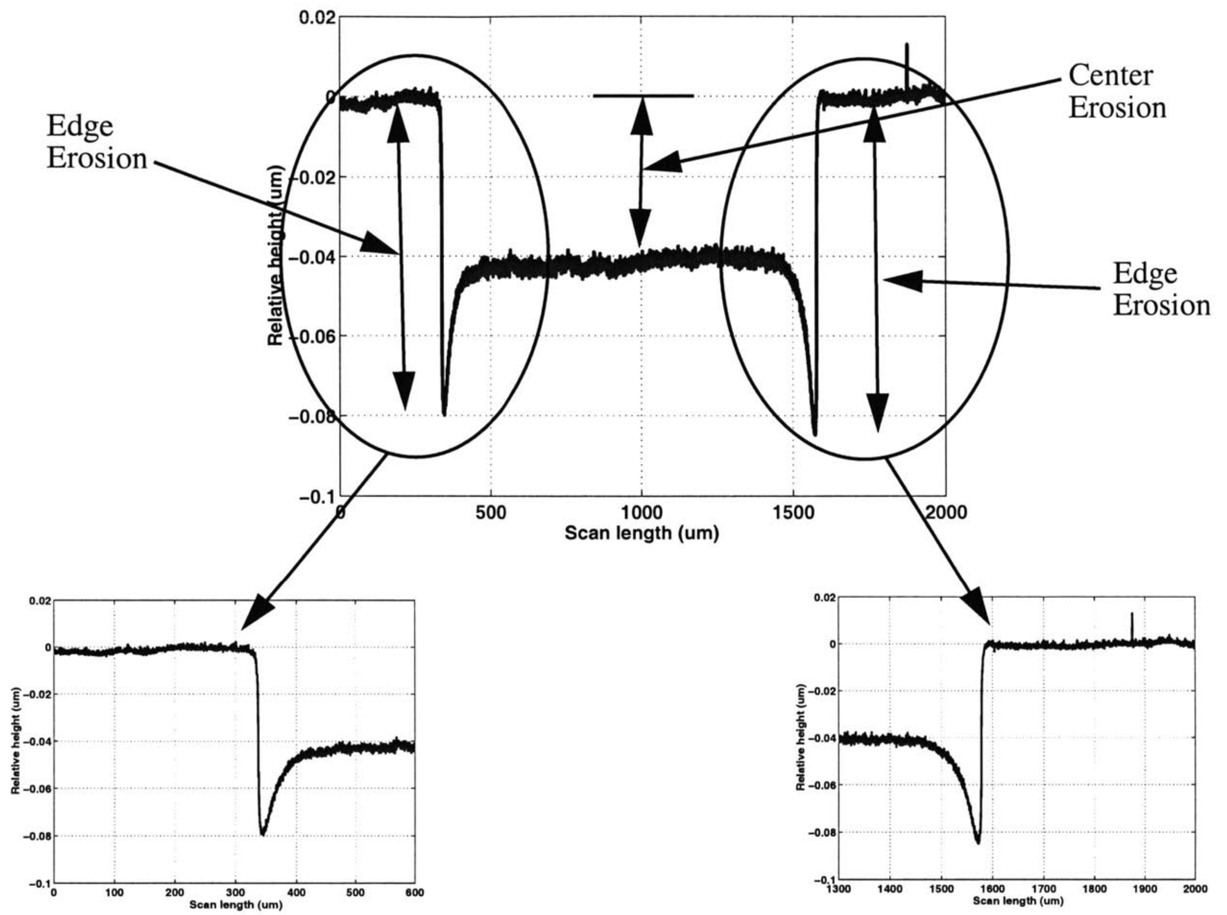


Figure 3.38: Profilometer scan of array with line width of 0.18 μm and line space of 0.18 μm, showing the ear effect

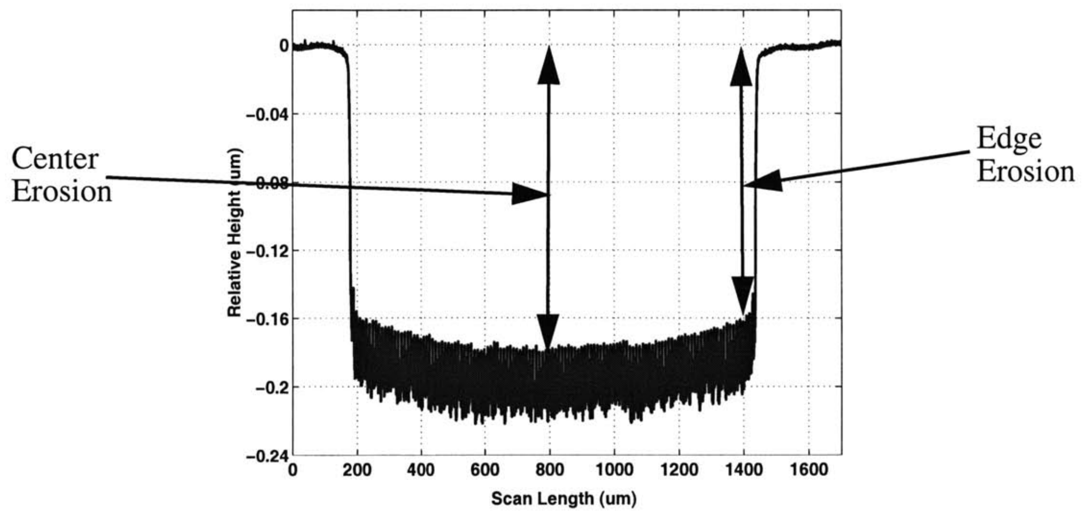


Figure 3.39: Profilometer scan of high density array structure showing no ear effect

The observations from experimental data lead to the speculation that the ear effect is a pattern dependent chemical effect that results from an interaction among the barrier, copper, and the slurry [1]. Experimental data suggests that the larger the amount of barrier available in a local region (e.g a large field region), the more prevalent the ear effect. This seems to explain why the ear effect is seen on layouts without dummy fills while it is not seen on those with. On layouts with dummy fills, no region can be called a field region. They all have dummy metals, thereby decreasing the amount of barrier in such regions.

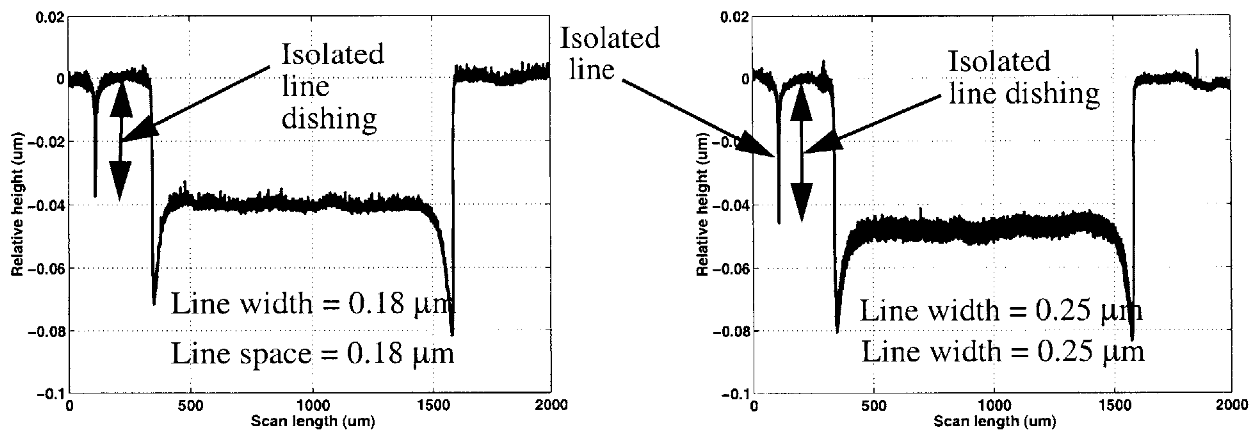


Figure 3.40: Profilometer scans showing dishing of sub-micron isolated lines

The idea of the ear effect being related to the amount of barrier in a local region, might be used to explain why an isolated copper line as small as 0.25 µm or even 0.18 µm dishes. Generally, it might be partly responsible for the increased dishing of isolated lines compared to array lines with the same line widths. Figure 3.40 shows the profilometer scans of two arrays with line widths of 0.25 µm and 0.5 µm respectively. The arrays have line spaces equal to their line widths. Each array has an isolated line of the same width as the lines in the array, located about 500 µm from the array. The figure clearly shows that the dishing of the isolated line is greater than that of the array lines, for both arrays. The ear effect might shed some light on why d_{max} and H_{ex}

are not identically equal. It was stated earlier that while a 0.25 μm isolated line dishes, meaning that it has a non-zero d_{max}, a 0.25 μm isolated line has an H_{ex} of zero.

The ear effect can be incorporated into the density-step-height model by making the effective copper blanket removal rate and the effective barrier blanket removal rate pattern dependent, i.e., they become functions of width and space or of the amount of barrier in a local region. There is definitely a length scale associated with the ear effect as shown in figure 3.38. This length scale might be used to define the extent of the local region. Making the effective blanket copper and barrier removal rates pattern dependent functions introduces additional modeling parameters, and therefore complicates the extraction of model parameters. Further experimental work is needed to fully understand the ear effect, so that it could easily be incorporated into a copper CMP model.

3.9.2 Excessive Overpolishing

According to the density-step-height model, the dielectric erosion increases linearly with polish time after steady-state dishing is achieved. Steady-state dishing is achieved very early in stage two or three, in conventional copper CMP processes. This means that erosion should be mainly linear with time in the overpolish stage. Hence, if excessive overpolishing is done, the erosion for a high density array surrounded by a field region is projected to become excessively high. This is not supported by experimental data.

Figure 3.41 shows a plot of dielectric erosion versus polish time for an array structure with a line width of 100 μm and a line space of 1 μm (effective copper pattern density of approximately 99%). The data indicates that the rate of erosion decreases if the polishing becomes excessive. The data in the plot is associated with the first experimental data set used to test the density step height model in section 3.8. Two extra wafers are polished for what

constitutes excessive overpolishing. Since the density-step-height model has already been calibrated for this experiment, excluding the excessively overpolished data points, figure 3.46 compares the model prediction to the experimental data with the excessively overpolish data points included. The figure indicates that the model over-predicts erosion for the excessively overpolished times.

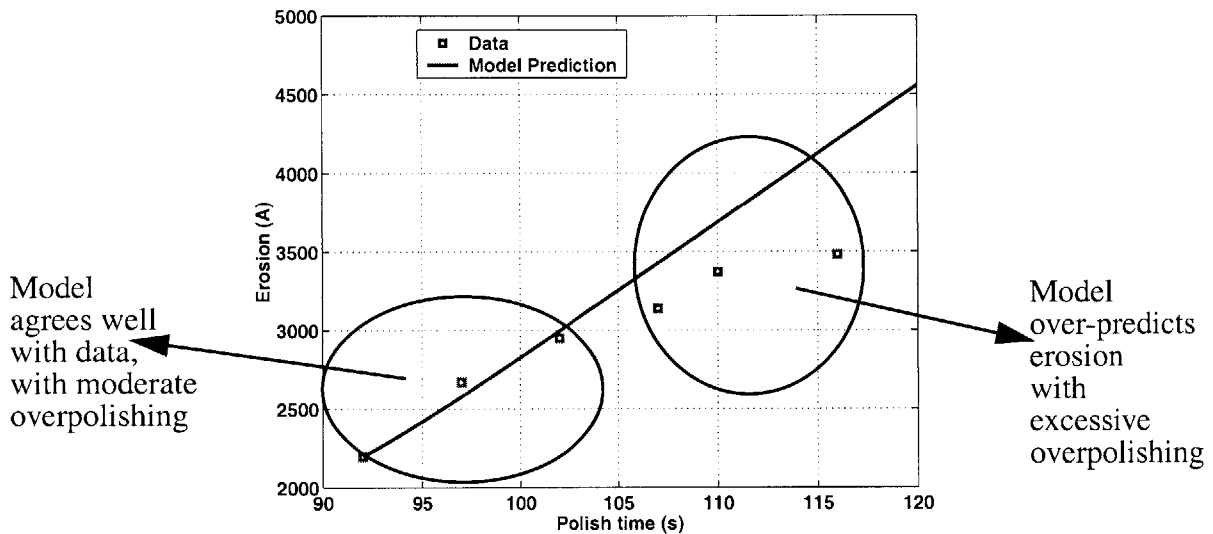


Figure 3.41: Plot of erosion versus polish time showing model failure when excessive overpolishing is done

Generally, the density-step-height model over-predicts erosion when the polishing is excessive because it fails to take into account the impact of long range height variation on the effective polishing pressure. When dealing with an array that is surrounded by large field regions, the array erodes faster than the field regions. As the level of the dielectric in the array recesses well below the level of the dielectric in the field regions, the pressure exerted by the polishing pad on the dielectric in the array as a whole decreases, while that on the dielectric in the field region increases slightly. As the pressure on the dielectric in the array decreases, the rate of erosion should also decrease. Ultimately, the rate of the dielectric erosion in the array will be in steady-state with the rate of the dielectric erosion in the field region. A removal rate diagram with the

field being the up-area and the array being the down-area can be used to explain this effect, with the complication that there is a need to identify large region "up" and "down" areas on the layout. An alternative is to include this effect in the model by integrating the density-step-height model with contact mechanics to account for pressure in different regions of the chip; this approach is discussed in chapter 6 of this thesis.

3.10 Summary

In this chapter, the density-step-height model for single step copper CMP processes is formulated and tested against experimental data. The model uses blanket wafer experiments to establish an empirical relationship between material removal rate and polish pressure. It then uses Hooke's law to establish a relationship between pressure and step height (or dishing). The removal rate versus pressure relationship and the pressure versus step height relationship are used to formulate removal rate diagrams. Removal rate diagrams are plots of removal rates versus step height (or dishing). From these diagrams the model equations are obtained and used to compute the evolution of copper thickness, the time to clear the bulk copper, and the evolution of dishing and erosion. The model introduces the parameters d_{max} and H_{ex} that relate dishing and the evolution of step height to the layout features. The model as formulated in this chapter ignores the "ear" effect, and fails to take into account long range height variation when apportioning polish pressure. The latter is rectified in chapter 6 of this thesis.

Chapter 4

Application of the Density-Step-Height Model to Non-Prestonian Copper CMP Processes

The density-step-height model as formulated in chapter 3 captures certain effects - pressure as function of step height or dishing, pressure as function of pattern density, removal rate as function of pressure, and acceleration in erosion due to localized feature scale pressures - that appear to be important in most, if not all, copper CMP processes. The framework of the model has some flexibility and extendability in the sense that the dependencies of dishing, erosion, and other parameters, on line width, line space or pattern density can be adapted to account for a variety of effects seen in different copper CMP processes. In this chapter the framework of the density-step-height model introduced in chapter 3 is extended to model non-Prestonian abrasive-free copper CMP processes. For simplicity, a single step abrasive-free copper CMP process is emphasized. In section 4.1, a brief overview of abrasive-free copper CMP processes is given. This is followed by the formulation of the model in the three intrinsic stages of such processes, in section 4.2. In section 4.3, the accuracy of the model is tested against experimental data. Finally, the chapter concludes in section 4.4 with a summary.

4.1 An Overview of Abrasive-Free Copper CMP Processes

In an attempt to reduce dishing, erosion, and scratching in copper CMP processes, consumable companies in collaboration with IC manufactures and research institutions are developing abrasive-free copper CMP slurries. These slurries have no abrasive particles in them.

This suggests that chemical reactions in combination with soft friction are responsible for material removal when these slurries are used. They are used in conjunction with conventional polishing pads and conventional CMP tools, in what has been termed "Abrasive-Free Copper CMP" (AFP).

Hitachi Chemicals Inc., was one of the first companies to publish experimental results on abrasive-free copper CMP processes. Their 430-1 slurry shows great promise in reducing dishing and erosion [14-16]. One interesting property of the 430-1 slurry is that different concentrations of the chemicals in the slurry lead to different removal rate versus pressure relationships. Figure 4.1 shows the removal rate versus pressure relationships for three different abrasive-free slurry solutions [14-16]. In addition, different removal rate versus pressure dependencies can be obtained on different platforms using the same slurry, as illustrated in figure 4.2 [43]. In theory, therefore, it is possible to manipulate the slurry in such a way that an ideal removal rate versus pressure relationship can be obtained - ideal from the point of view of planarization, and dishing and erosion minimization.

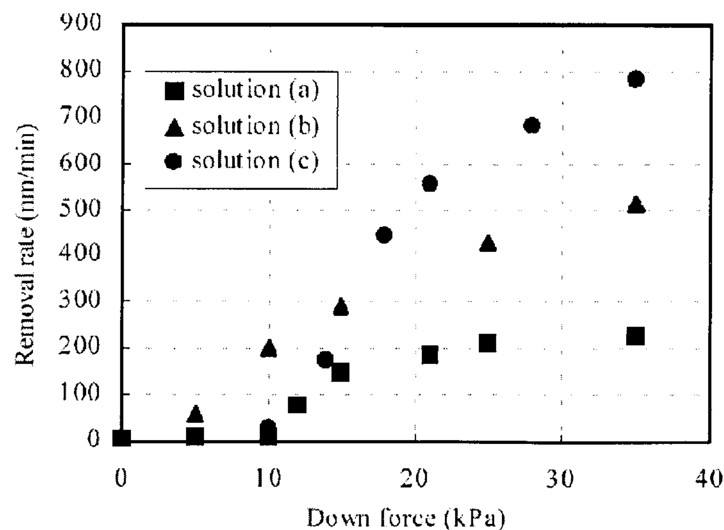


Figure 4.1: Removal rate versus down force for different abrasive-free slurry solutions (from [16])

The advantages of abrasive free copper CMP processes are substantially improved dishing and erosion performance, reduced solid content in effluent, and reduced scratching during CMP. The challenge for such processes is that in some cases, it may be difficult to clear the copper in certain regions on the die, and the wafer in general. It is important to note that abrasive-free copper CMP processes are at the final stages of development. They are envisioned to be used in a two-step polish process framework, where in both polish steps would use abrasive-free processes, or the first step would use an abrasive-free process and the second a conventional copper CMP process or even an etching process [14-16].

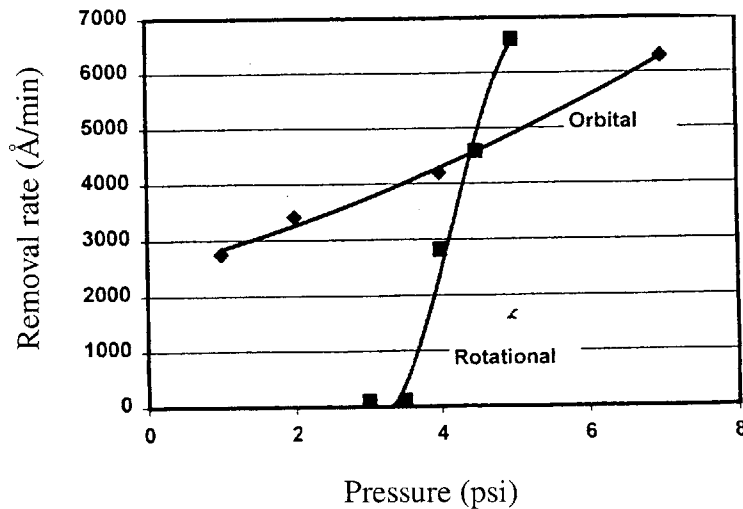


Figure 4.2: Removal rate vs. pressure curves for 430-1 Hitachi slurry on different CMP tools (from [43])

4.2 Model Formulation for Single Step Abrasive-Free Copper CMP Processes

Figure 4.3 shows an abstraction of the removal rate versus pressure relationships for copper, dielectric, and barrier, approximating the relationships observed for a particular mixture of the Hitachi 430-1 abrasive-free slurry. The relationship for copper is non-Prestonian, and

comprises two linear regions. There exists a threshold pressure P_0 at and below which the copper removal rate is zero, and a breakpoint pressure P_2 at which the slope of the copper removal rate versus pressure curve changes. At an applied pressure of P_1, the instantaneous blanket copper removal rate is r_{cu}, and the instantaneous blanket barrier and oxide removal rates are equal to r_{ox}. The removal rate versus pressure relationship for the barrier and the dielectric (oxide in this case) is approximately Prestonian. These removal rate versus pressure relationships are used in formulating the density-step-height model in the three intrinsic stages of a single step abrasive-free copper CMP process below.

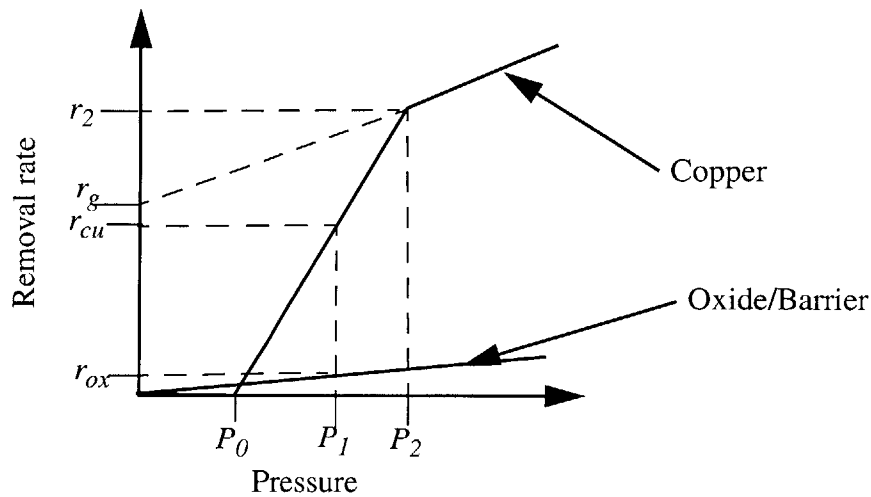


Figure 4.3: Approximate removal rate versus pressure relationship

4.2.1 Model Formulation in Intrinsic Stage one: Bulk copper polishing

Figure 4.4 shows the relationship between pressure and step height in intrinsic stage one. In the figure, ρ_{cu} is the electroplated copper density, H_0 is the step height which corresponds to a pressure of P_0 on the down-area, and H_{ex} is the critical step height. By combining this relationship with that illustrated in figure 4.3, the removal rate diagram for intrinsic stage one of the single step abrasive-free copper CMP process is obtained, as illustrated in figures 4.5 - 4.6. If the quantity P_1/

ρ_{cu} is greater than or equal to the break pressure P_2, the removal rate diagram is given in figure 4.5. Otherwise, the removal rate diagram is given in figure 4.6. From the removal rate diagrams, the removal rate equations can be derived, and used to solve for the step height evolution, the copper thickness evolution, and the time it takes to clear the bulk copper at any spatial position of interest.

From figures 4.5 and 4.6, it is clear that the step height at and above which the removal rate on the down-area becomes zero is H_0, as opposed to the critical step height H_{ex}. This is because of the occurrence of a non-zero positive threshold pressure P_0 below which the copper removal rate is zero. The parameter H_0 is related to H_{ex} as given in equation 4.1. Having H_0 less than H_{ex} implies that this abrasive-free process has a higher planarization efficiency than a conventional copper CMP process with a similar H_{ex} value. The planarization efficiency is a measure of the local planarization capability of the process, and is defined as one minus the ratio of the amount removed in the down-area and that removed in the up-area.

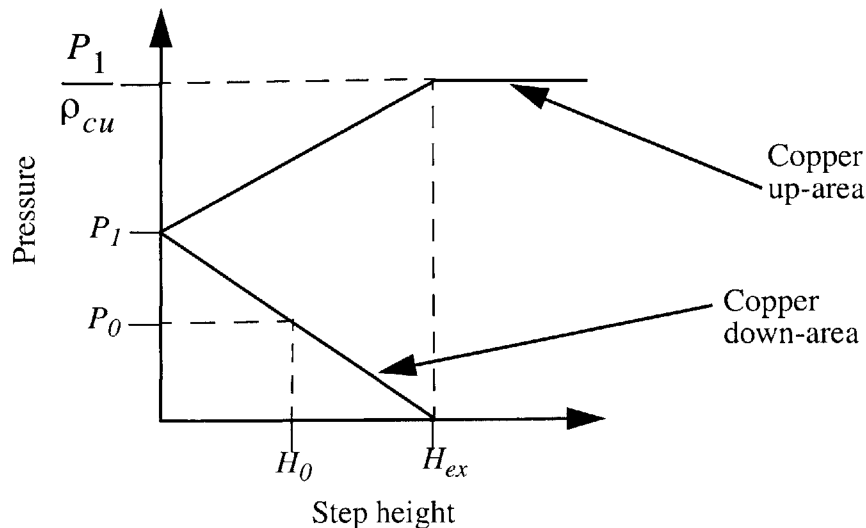


Figure 4.4: Pressure versus step height relationship

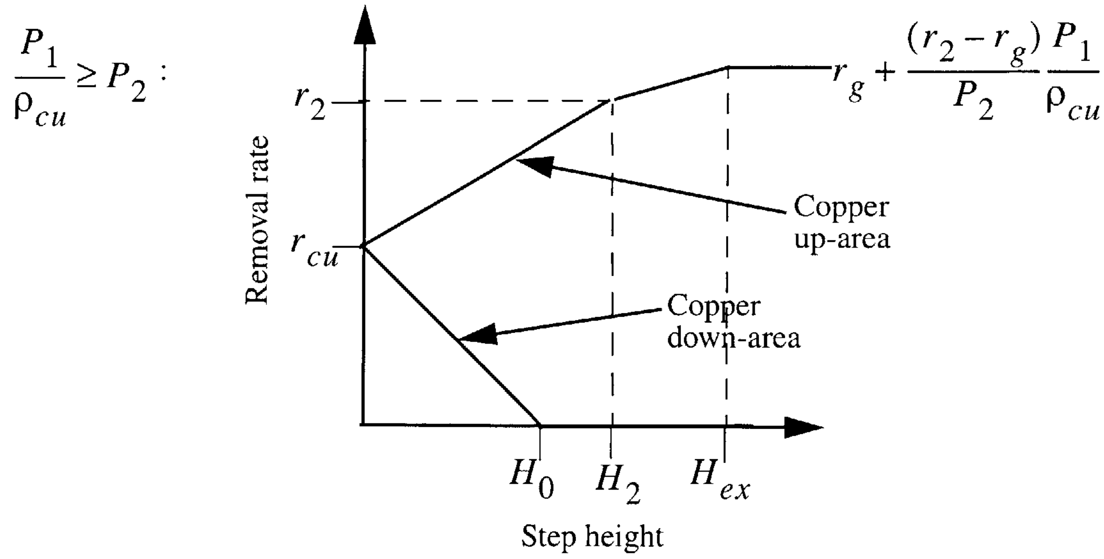


Figure 4.5: Removal rate diagram for intrinsic stage of abrasive-free copper CMP process

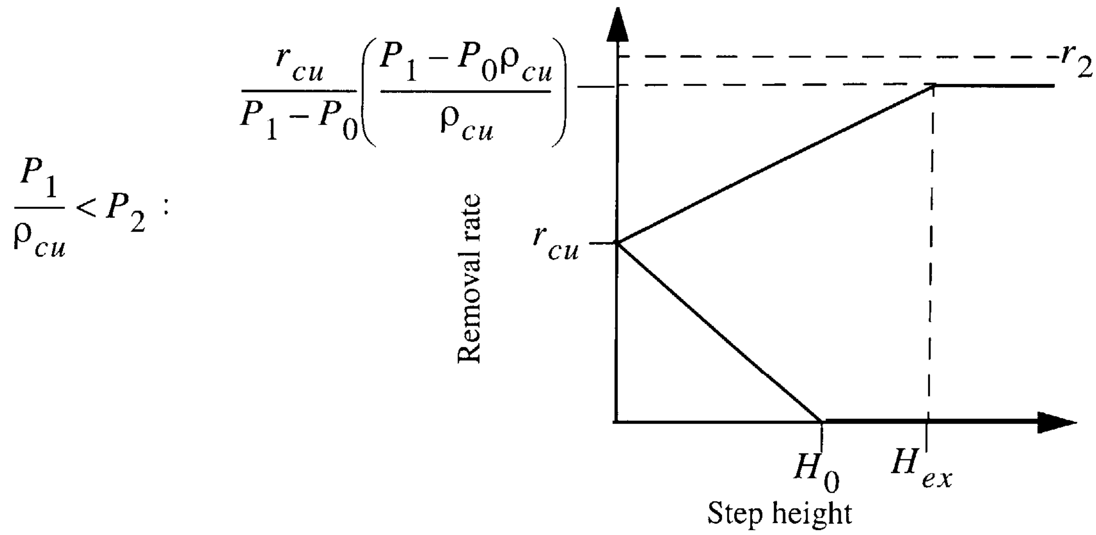


Figure 4.6: Removal rate diagram for intrinsic stage one of abrasive-free CMP process

$$H_0 = \left(\frac{P_1 - P_0}{P_1}\right) H_{ex} \qquad \textit{(Equation 4.1)}$$

4.2.2 Model Formulation in Intrinsic Stage Three: Overpolish Stage

Figure 4.7 shows the pressure versus dishing relationship in intrinsic stage three of an abrasive-free copper CMP process, where d_0 is the dishing associated with a pressure of P_0, Φ_{cu} is the effective layout copper pattern density, and P_1 is the applied pressure. Combining this relationship with the removal rate versus pressure relationship illustrated in figure 4.3 gives the removal rate diagram illustrated in figure 4.7. It is important to note that this removal rate diagram

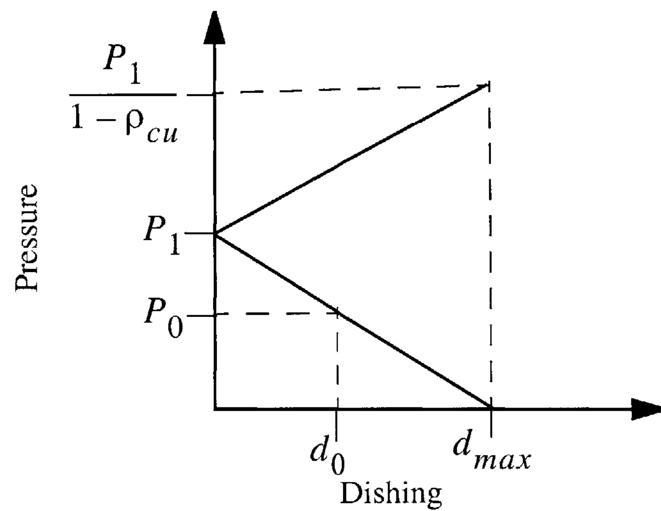


Figure 4.7: Pressure versus dishing relationship in intrinsic stage three

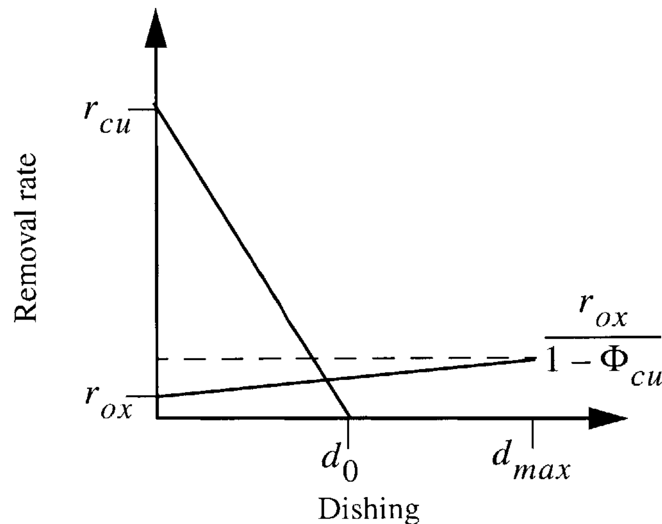


Figure 4.8: Removal rate diagram for intrinsic stage three of abrasive-free process

is the same as that for intrinsic stage two of this process because the removal rate versus pressure curves for both the dielectric and the barrier are the same for this abrasive-free process.

As seen in figure 4.8, the dishing at which the copper removal rate becomes zero is less than the maximum dishing value of d_{max}. This is due to the non-zero threshold pressure, similar to the case of the critical step height discussed earlier. It implies that the steady-state dishing for this process is much less than that for a conventional copper CMP process which has a similar blanket copper removal rate and similar maximum dishing values. The maximum dishing d_{max} is related to d_0 as given in equation 4.2. The removal rate diagram is expressed mathematically in equations 4.3 - 4.4, where RR_{ox} is the dielectric removal rate, and RR_{cu} is the copper removal rate. From these equations, the amount of dishing D_{cu} and erosion E_{ox} can be obtained as functions of time, as in equations 4.5 - 4.12. The variable t_3 represents the time it takes to clear the bulk copper and the barrier at a spatial location of interest, t represents the polish time, and d_3 represents the dishing when the barrier has just been cleared at the location of interest.

$$d_0 = \left(\frac{P_1 - P_0}{P_1}\right) d_{max} \qquad \textit{(Equation 4.2)}$$

$$RR_{cu} = \begin{cases} r_{cu}\left(1 - \dfrac{D_{cu}}{d_0}\right) & 0 \le D_{cu} < d_0 \\ 0 & d_0 \le D_{cu} \le d_{max} \end{cases} \qquad \textit{(Equation 4.3)}$$

$$RR_{ox} = r_{ox} + r_{ox}\left(\frac{\Phi_{cu}}{1 - \Phi_{cu}}\right)\frac{D_{cu}}{d_{max}} \qquad 0 \le D_{cu} \le d_{max} \qquad \textit{(Equation 4.4)}$$

$$\frac{dD_{cu}}{dt} = RR_{cu} - RR_{ox}$$ *(Equation 4.5)*

$$\frac{dE_{ox}}{dt} = RR_{ox}$$ *(Equation 4.6)*

$$D_{cu} = d_3 e^{\frac{-(t-t_3)}{\tau_3}} + D_{ss}\left(1 - e^{\frac{-(t-t_3)}{\tau_3}}\right) \qquad t \geq t_3$$ *(Equation 4.7)*

$$E_{ox} = X_1(t-t_3) + X_2\left(e^{\frac{-(t-t_3)}{\tau_3}} - 1\right) \qquad t \geq t_3$$ *(Equation 4.8)*

$$\tau_3 = \frac{d_0 d_{max}(1-\Phi_{cu})}{r_{cu} d_0 (1-\Phi_{cu}) + r_{ox} d_{max} \Phi_{cu}}$$ *(Equation 4.9)*

$$D_{ss} = (r_{cu} - r_{ox})\tau_3$$ *(Equation 4.10)*

$$X_1 = r_{ox} + \frac{r_{ox}}{d_{max}}\left(\frac{\Phi_{cu}}{1-\Phi_{cu}}\right) D_{ss}$$ *(Equation 4.11)*

$$X_2 = \frac{r_{ox}}{d_{max}}\left(\frac{\Phi_{cu}}{1-\Phi_{cu}}\right)(D_{ss} - d_3)\tau_3$$ *(Equation 4.12)*

4.2.3 Model Parameters and Model Calibration Methodology

The modeling parameters for this single step abrasive-free process are summarized in table 4.1 and they are similar to those for a single step conventional copper CMP process

discussed in chapter 3. The effective blanket removal rates are instantaneous removal rates, with the same time dependence as given for conventional copper CMP processes. The edge rounding factor ψ has the same functionality as in chapter 3 (it is not included in the equations for dishing and erosion above). In addition, the functional dependence of the critical step height H_{ex} and the maximum dishing d_{max} on layout features are not necessarily the same as those for conventional copper CMP processes, as discussed in section 4.3. The methodology for extracting the model parameters is the same as that described earlier for single step conventional copper CMP processes.

Table 4.1: Model parameters for single step abrasive-free copper CMP processes

Intrinsic stage one		Intrinsic stage two		Intrinsic stage three	
	Name		Name		Name
r_{cu}	Effective blanket copper removal rate	r_{cu}	Effective blanket copper removal rate	r_{cu}	Effective blanket copper removal rate
L_1	Planarization length	r_b	Effective blanket barrier removal rate	r_{ox}	Effective blanket dielectric removal rate
H_{ex}	Critical step height	L_3	Planarization length	L_3	Planarization length
		d_{max}	Maximum dishing	d_{max}	Maximum dishing
		ψ	Edge rounding factor	ψ	Edge rounding factor

4.3 Model Fit versus Experimental Data

To test the accuracy of the model for abrasive-free copper CMP processes, a single step copper CMP experiment is conducted using the MIT-SEMATECH mask 854, the Hitachi 430-1 slurry, and an IC1000 solo pad. The threshold pressure P_0, applied pressure P_1, and breakpoint pressure P_2 are 3.0 psi, 4.7 psi, and greater than 6.0 psi, respectively. The rest of the experimental

details are given in tables 4.2 - 4.3. At the time the experiments were conducted, there was no access to equipment that measured copper thickness on pattern wafers accurately. Consequently, only step height and recess measurements are used to capture the evolution of the bulk copper polishing; step height and recess data are insufficient to fully extract the model parameters in intrinsic stage one. Therefore, no extraction of model parameters is done for the first intrinsic stage. Instead, the emphasis is on the overpolish stage.

Table 4.2: Blanket wafer abrasive-free CMP experiments

Wafer number	Wafer material	Polish time (s)
T-1	Copper	7
T-2	Copper	17
T-3	Copper	33
T-4	Copper	50
T-5	Copper	60
S-1	Oxide	90
S-2	Oxide	120
U-1	Barrier (TaN)	90
U-2	Barrier (TaN)	120

Table 4.3: Patterned wafer abrasive-free CMP experiments

Wafer number	End-point time (s)	Total polish time (s)	Wafer status after CMP
Q-6	143	143	Overpolished
Q-7	142	152	Overpolished
Q-8	141	161	Overpolished
Q-9	142	172	Overpolished
Q-10	143	203	Overpolished
Q-11	142	262	Overpolished

4.3.1 Experimental Data and Model Parameter Extraction

The data for the amount removed on the blanket copper wafers shows that the effective blanket copper removal rate (i.e. the instantaneous blanket copper removal rate) is a constant with a value of 86.7 Å/s. This confirms what was stated earlier in chapter 3 that depending on the polishing tool used, the instantaneous rate can be time dependent or not. The measured instantaneous removal rates for the dielectric and the barrier are both less than 0.5 Å/s, implying that the slurry hardly removes the dielectric and barrier material. As a result of this, significant overpolishing of the patterned copper wafers had to be done to get a reasonable amount of erosion, which is necessary for extracting the correct planarization length in the third intrinsic stage.

The experimental data for the overpolish stage show that dishing is a function of line width. The larger the line width, the greater the dishing. The same effect is observed in conventional copper CMP processes. It is believed to be due to the fact that the larger the line width, the easier it is for the pad to compress into the line and exert pressure on the copper. Figures 4.9 shows profilometer scans for two array structures that have the same layout density, but different line widths. The structure with the larger line width has the larger dishing. Figure 4.10 plots dishing versus line width for structures with 50% layout pattern density. The figure shows that the rate of dishing with respect to line width decreases as the line width increases.

In addition to the line width dependence, the data also suggest that dishing depends on copper pattern density, and that the density effect seems to be dominant. Figure 4.11 shows the profilometer scans of two array structures with the same line width, but different layout copper density, and figure 4.12 shows a plot of dishing at the center of an array versus copper layout density. These figures indicate that the higher the copper layout density, the higher the dishing.

This dependence is the complete opposite of what is observed in conventional CMP processes. There, the higher the copper density, the lower the copper dishing. The apparent density dependence of dishing for this abrasive-free process, is contrary to expectation particularly since the data also suggest that the higher the pattern density, the higher the dielectric erosion, as illustrated in figure 4.13. Clearly then, this density dependence of dishing needs careful examination.

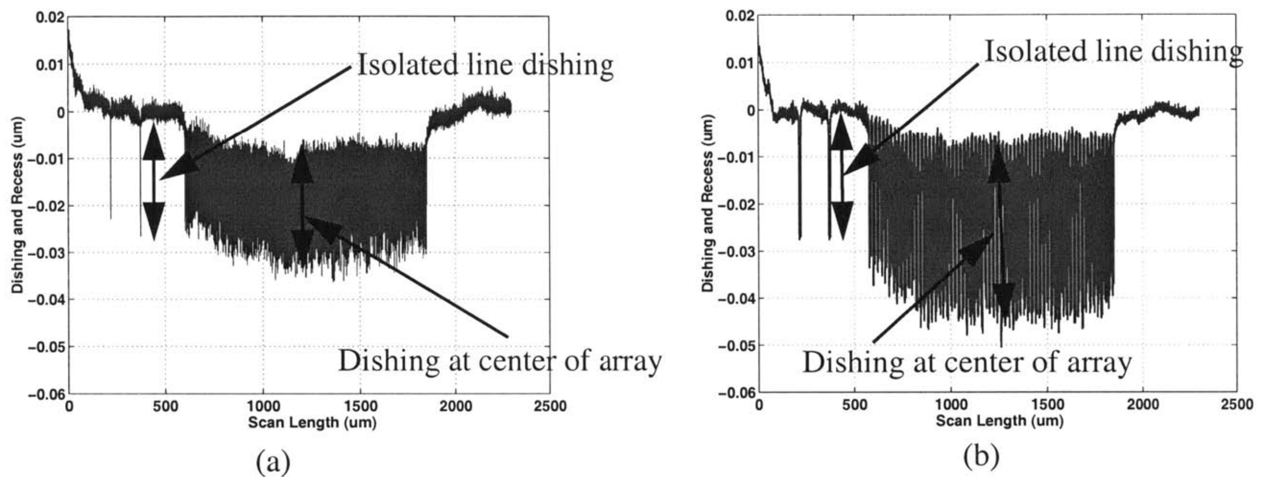


Figure 4.9: Profilometer scans for two arrays with same density, but different line widths: (a) Line width = 1 μm; Line space = 1 μm (b) Line width = 10 μm; Line space = 10 μm

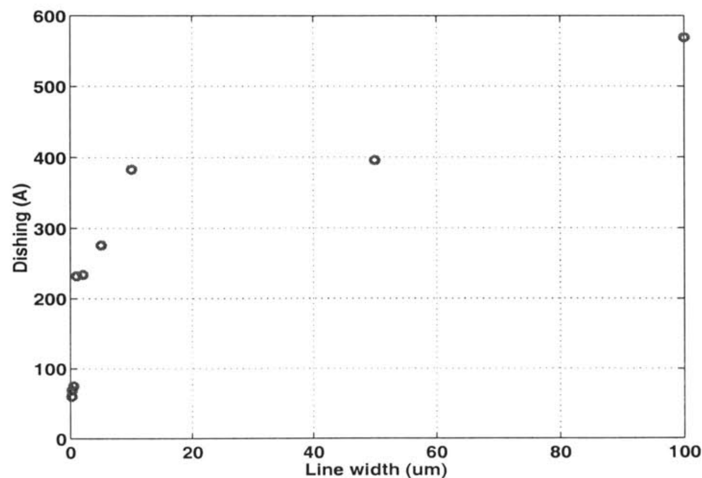


Figure 4.10: Measured dishing versus line width for arrays with copper pattern density of 50%

For any array, the data shows that dishing peaks in a finite region at the center of the array. The size of this finite region remains relatively unchanged for all the arrays. The size of the finite region, and its distance from the edge of the array indicates that the density length scale for dishing is approximately 500 μm. In an earlier publication [39], this length scale was called the planarization length, and the apparent density effect was interpreted as a layout pattern density effect. Upon further examination of the data, it is likely that the interpretation in the earlier publication was inaccurate.

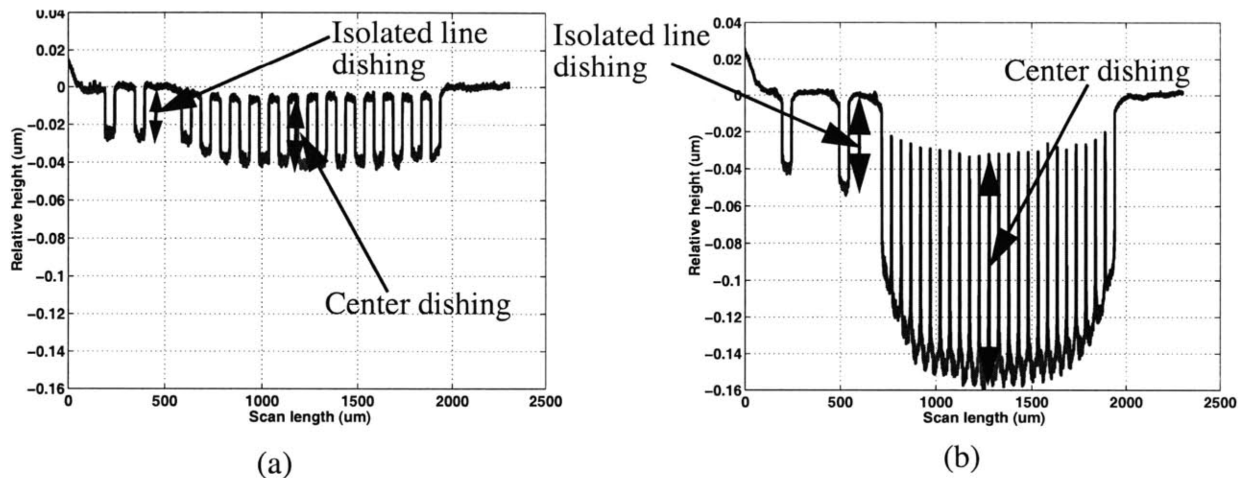


Figure 4.11: Profilometer scans of two arrays with same line width, but different densities: (a) Line width = 50 μm; Density = 50% (b) Line width = 50 μm; Density = 99%

The length scale of 500 μm is far shorter than the millimeter range length scale expected for the planarization length. This suggests that the apparent density dependence of dishing is not related to the long range pad deformation, which is captured by the planarization length. It is therefore misleading to call it a pad pressure related density effect, which relates the geometric up-area and geometric down-area ratio to pressure with a planarization length notion. Instead, it seems to be a chemical effect that occurs in the presence of an applied force. It is conjectured to be linked to the formation of Cu^{2+} ions as a by-product of the Hitachi 430-1 slurry [44]. The

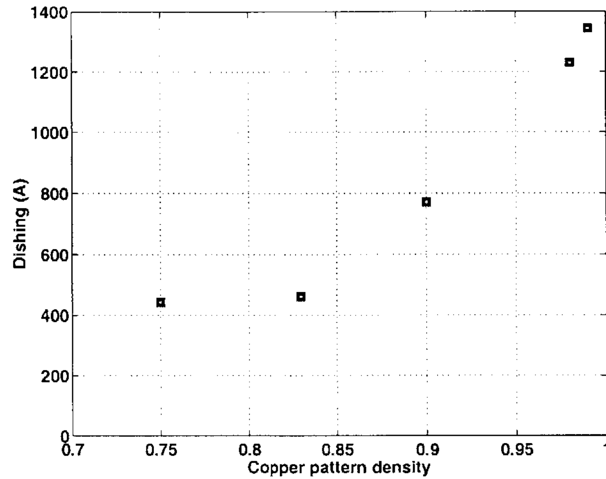


Figure 4.12: Measured dishing versus layout copper pattern density for AFP

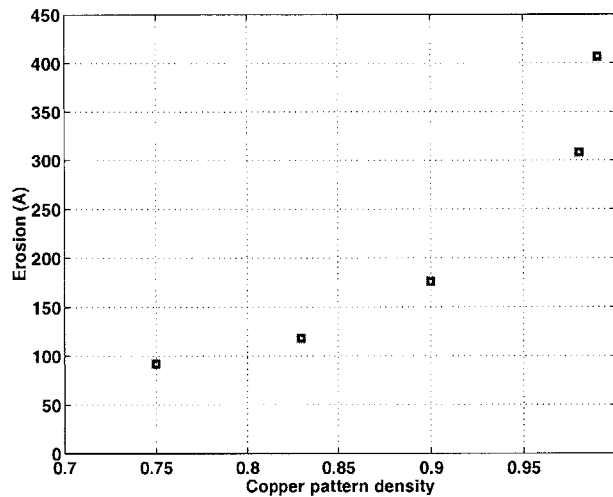


Figure 4.13: Measured erosion versus layout copper pattern density for AFP

higher the amount of copper within the chemical related length scale (500 μm in this case), the higher the concentration of Cu^{2+} ions and the higher the amount of dishing. How exactly the presence of Cu^{2+} ions result in higher dishing is not clear. The fact that dishing reaches a steady-state in this process means that static etching is negligible and not responsible for this effect.

To account for the conjectured chemically induced dishing effect (which occurs in the presence of pressure), a new variable θ which represent the ratio of the copper in a region (whose

size is determined by a chemically induced dishing length scale L_c, which is 500 μm in this experiment) is introduced. The higher the ratio of copper at any spatial position, the higher the dishing. The longer the chemically induced dishing length scale, the more non-uniform the dishing profile within an array, and vice-versa. This length scale can be obtained from observing the shape of the dishing profile for several arrays of lines. Hence, the introduction of this new variable does not complicate the model parameter extraction methodology.

This conjectured chemical effect is incorporated into the density-step-height model through the model parameter d_{max}. An empirical function relating d_{max} to the line width w (in microns) and the copper ratio θ is proposed in equation 4.13. In this equation, α_2 and β_2 are unitless constants between zero and one, B is a constant in units of angstroms and is greater than or equal to zero, and w_o is a normalization line width of 1 μm. To avoid having an unrealistic value of infinity for d_{max} when the parameter θ is equal to one, as suggested by the proposed function, the proposed function is modified as given in equations 4.14 - 4.15. The variable δ is a unitless constant, and it is set equal to 0.01 in this thesis. The functionality of d_{max} captures the sub-linear dependence of dishing on line width, and the power-like dependence of dishing on copper ratio.

$$d_{max} = B\left(\frac{w}{w_o}\right)^{\alpha_2}\left(\frac{1}{1-\theta}\right)^{\beta_2} \qquad \textit{(Equation 4.13)}$$

$$d_{max} = B\left(\frac{w}{w_o}\right)^{\alpha_2}\left(\frac{1}{1-\tilde{\theta}}\right)^{\beta_2} \qquad \textit{(Equation 4.14)}$$

$$\tilde{\theta} = \begin{cases} 0 & \theta \le \delta \\ \theta - \delta & \theta > \delta \end{cases} \qquad \textit{(Equation 4.15)}$$

If the conjectured chemically induced effect affects the value of d_{max}, then within the framework of the density-step-height model, it must also affect the critical step height H_{ex} in intrinsic stage one. In particular, the functional dependence of H_{ex} on layout parameters is typically the same as that of d_{max}. In intrinsic stage one, the copper ratio is one everywhere because there is bulk copper everywhere (in up and down areas). This implies that the only layout parameter on which H_{ex} is dependent is line width, as proposed in equation 4.16, where α_1 is a unitless constant between zero and one, w is line width in microns, w_o is a normalization line width of 1 µm, and A is a constant in units of angstroms and is greater than or equal to zero.

$$H_{ex} = A\left(\frac{w}{w_o}\right)^{\alpha_1} \qquad \text{(Equation 4.16)}$$

Using the proposed functionality for d_{max}, the blanket wafer data, and the dishing and erosion data measured from the overpolished wafers, the model parameters are extracted as summarized in table 4.4. The model parameter r_{ox} (instantaneous blanket dielectric removal rate) is floated in a restricted range during extraction. The arrays used in the extraction of the model parameters are marked on the test mask used in the experiment, in figure 4.14. The model fits versus the measured data for the extracted values of the model parameters are shown in figures 4.15 - 4.17. The model predicts the trend in the data accurately, and fits the data to within measurement errors.

Table 4.4: Extracted model parameters in intrinsic stage three of abrasive-free copper CMP process (r_b is obtained from r_{ox} as described in chapter 3)

r_{cu} (Å/s)			r_{ox} (Å/s)	r_b (Å/s)	L_3 (Å)	d_{max} (Å)			ψ		RMS Error (Å)
a_1 (Å/s)	a_2 (Å)	τ_r (s)				B (Å)	α_2	β_2	C	s_c	
86.7	0	0	0.34	0.34	1269	557	0.17	0.29	N/A	N/A	78.1

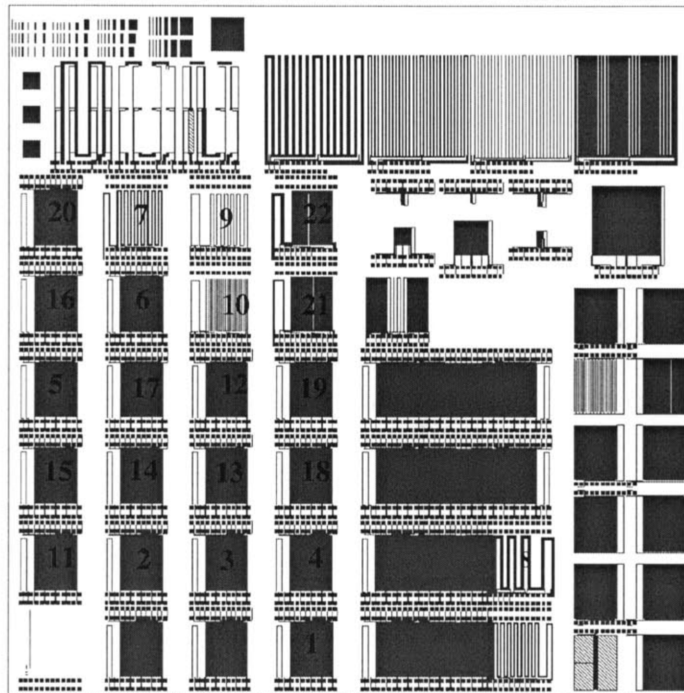


Figure 4.14: Array sites used in the extraction of model parameters

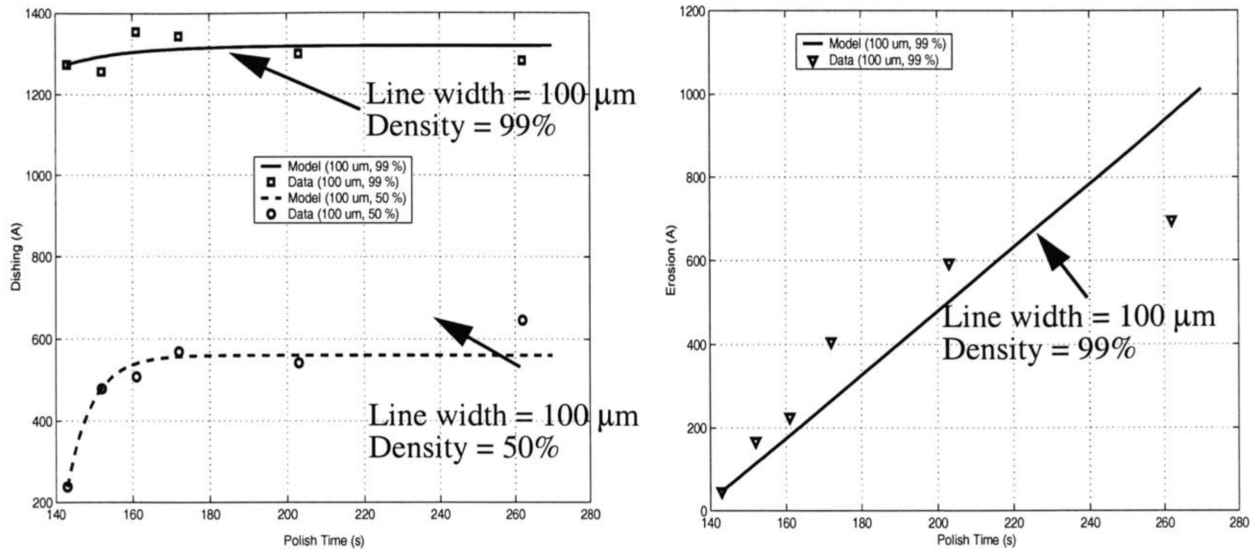
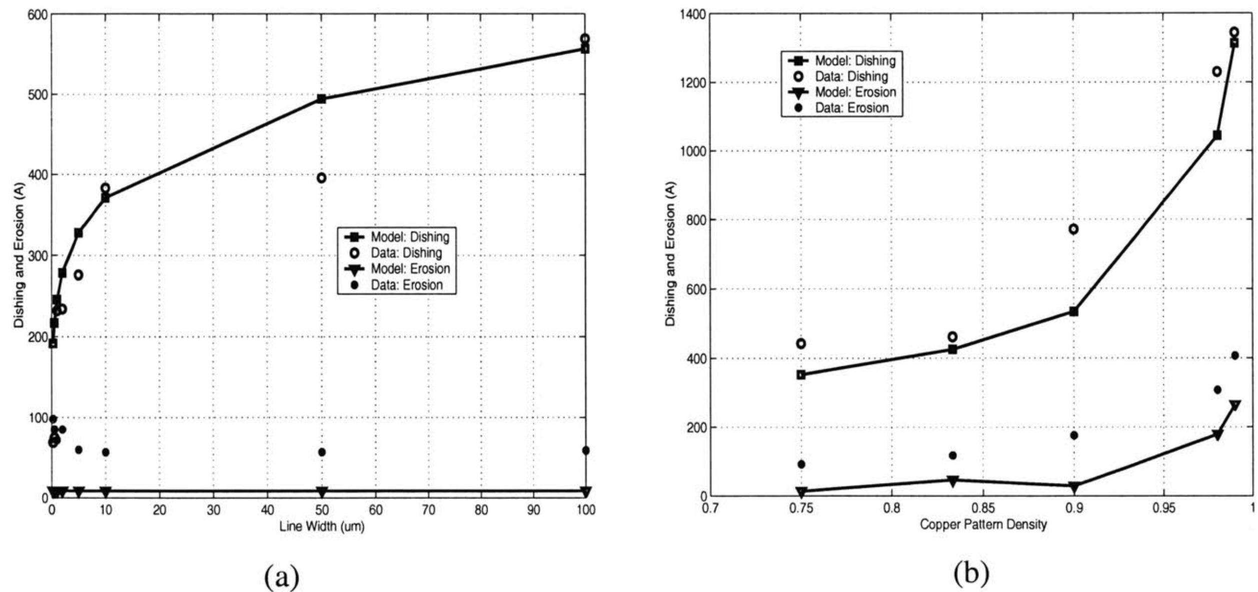


Figure 4.15: Dishing and erosion versus polish time



(a) (b)

Figure 4.16: Dishing and erosion versus line widths and pattern density:
(a) Density = 50%; Polish time = 172 s (b) Line space = 1 μm; Polish time = 172 s

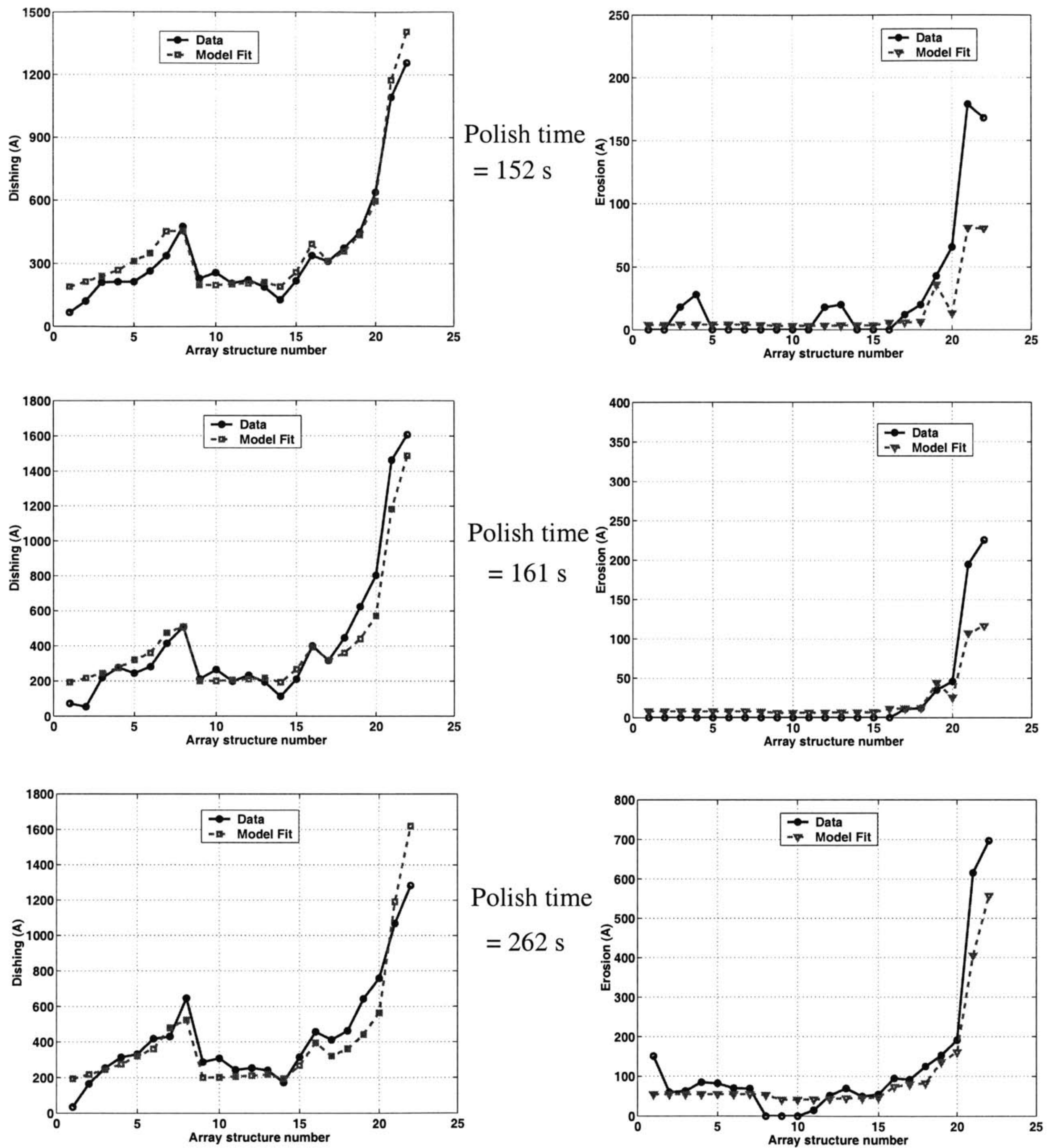


Figure 4.17: Model fits vs. experimental data (for AFP) for different array sites on test mask

4.4 Summary

The framework of the density-step-height model is applied to non-Prestonian processes. Specifically, the model is formulated for a single step abrasive-free copper CMP process, and tested against experimental data for the overpolish stage. Experimental data shows that abrasive-free processes are different from conventional copper CMP processes. First, the absence of abrasives makes the effective blanket dielectric removal rate very small. This leads to very low erosion, even after significant overpolishing. Second, dishing depends on line width and the amount of copper within a specific region. The latter effect, speculated to be a chemical effect in the presence of pressure, dominates the amount of dishing.

Chapter 5

Application of the Density-Step-Height Model to Multi-Step Copper CMP Processes

Single step copper CMP processes have been replaced in practice with multi-step copper CMP processes, where different consumable sets and different polish process parameter settings (down force and relative speed) are used at different phases of the polishing process. A typical multi-step copper CMP process has three steps. In such a process, the first step is intended to remove a large amount of the bulk copper, while leaving the remaining copper film highly "planarized". The second step is intended to clear the remaining bulk copper across the entire wafer, while keeping dishing and erosion low. This step uses a low down force and an average relative speed, and is often referred to as a soft landing step. The third step clears any remaining barrier film from the spaces between the interconnect lines, and across the entire wafer.

In this chapter, the framework of the density-step-height model developed in chapter 3 is applied to modeling conventional Prestonian multi-step copper CMP processes. In section 5.1, the density-step-height model equations for a three-step process are derived. This is followed by the development of a calibration methodology in section 5.2. The model and calibration methodology are tested against experimental data in section 5.3. Finally, the chapter concludes with a summary in section 5.4.

5.1 Formulation of Model for Multi-Step Processes

The key to modeling a multi-step copper CMP process is to treat it as a combination of separate single step CMP processes, where each step is comprised of three intrinsic stages: bulk copper polishing, barrier clearing, and overpolishing [42].

Each of the separate single step processes in a multi-step process is intended to emphasize or achieve results in a different phase of the polishing process. As a result, for each single step process, not all three intrinsic stages are necessarily relevant or active. Figure 5.1 summarizes the intrinsic stages that are relevant in a three step copper CMP process. For such a process, the first step is used to remove a large amount of the bulk copper, without completely clearing it. Therefore, this step only involves intrinsic stage one behavior. Step two is used to clear the remaining bulk copper from the entire wafer. The time of polish in step two is typically the end-point time plus an additional time to ensure clearing of bulk copper across the wafer. Hence, step two involves bulk copper polishing (stage one), barrier polishing (stage two), and overpolishing (stage three) at some points on the die. The bulk copper stage in step two involves polishing of a pattern-free copper surface with thickness differences across the surface, i.e., the step height is approximately zero everywhere on the die during the bulk copper clearing stage in step two.

Step three is used to clear the remaining barrier across the wafer. This step involves barrier polishing (stage two) and overpolishing (stage three). The slurry and the polish process parameter settings used in this step typically have a higher blanket dielectric removal rate compared to the blanket copper removal rate. In addition, the blanket copper removal rate might be higher or lower than the blanket barrier removal rate. In formulating the model equations, only the relevant intrinsic stages in each step are taken into account.

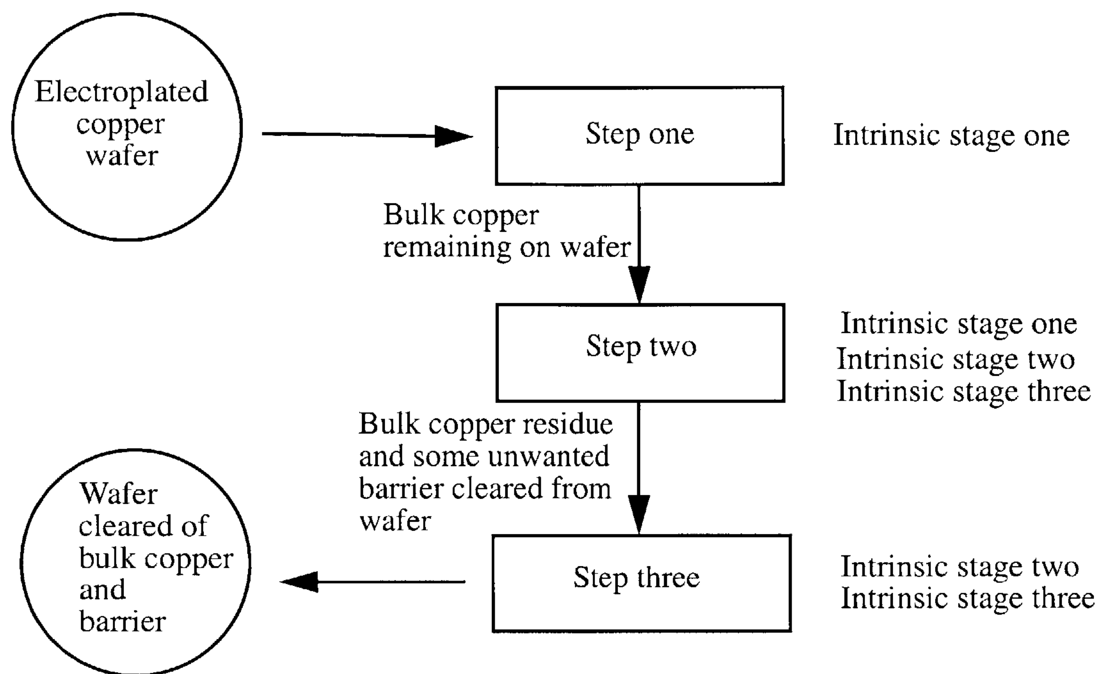


Figure 5.1: Relevant intrinsic stages for the steps of a three step copper CMP process

The pressure versus step height (or dishing) diagrams and the removal rate diagrams for the relevant intrinsic stages in each polish step, are illustrated in figures 3.36 - 3.40. All the parameters used in these figures are defined in tables 5.1 - 5.4. The assumption made in deriving the removal rate diagrams is that each of the three separate single step processes is approximately Prestonian. This assumption is valid for conventional multi-step copper CMP processes.

The removal rate diagram for the overpolish stage of the third step shown in figure 5.6 is particularly interesting. In the overpolish stage of the third polish step, the copper in the trench is the up-area and the dielectric in the space is the down-area. This is because, by definition, the down-area contains the material with the higher blanket removal rate and the up-area contains the material with the lower blanket removal rate, in the case where two materials are being polished simultaneously, starting with a flat surface. However, at the start of the third intrinsic stage of the third step, the initial dishing due to the previous step and the second stage of the third step might

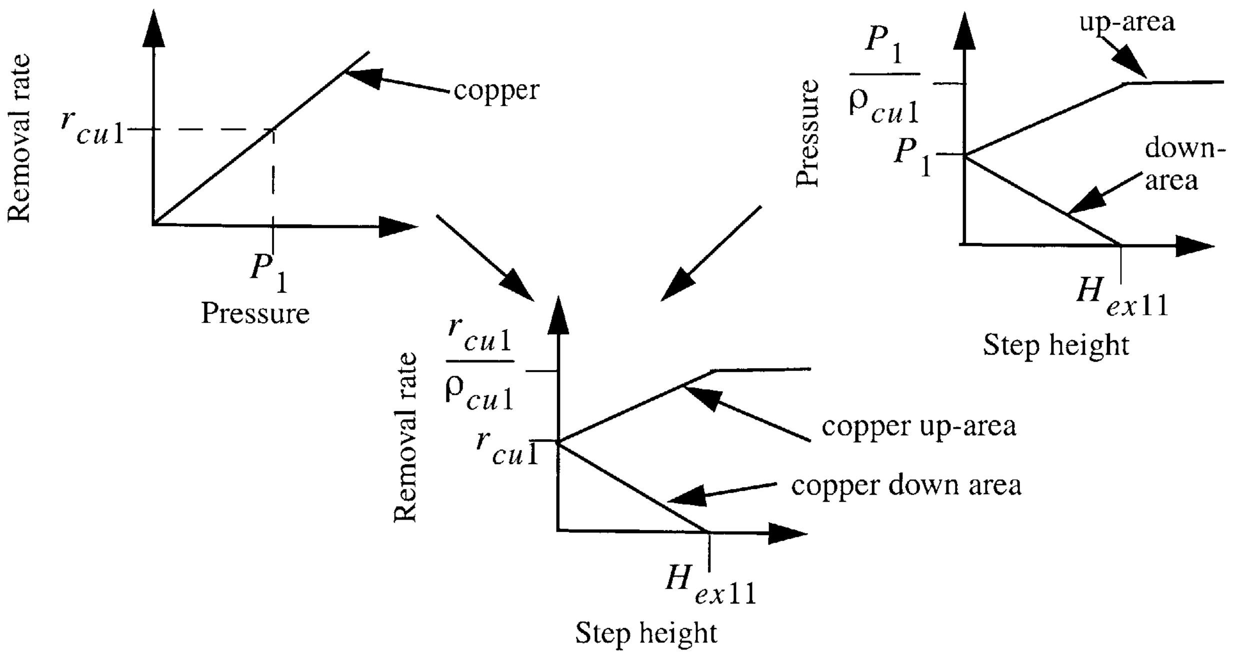


Figure 5.2: Formulation of removal rate diagram for intrinsic stage one (bulk copper polish) of step one in a three step copper CMP process

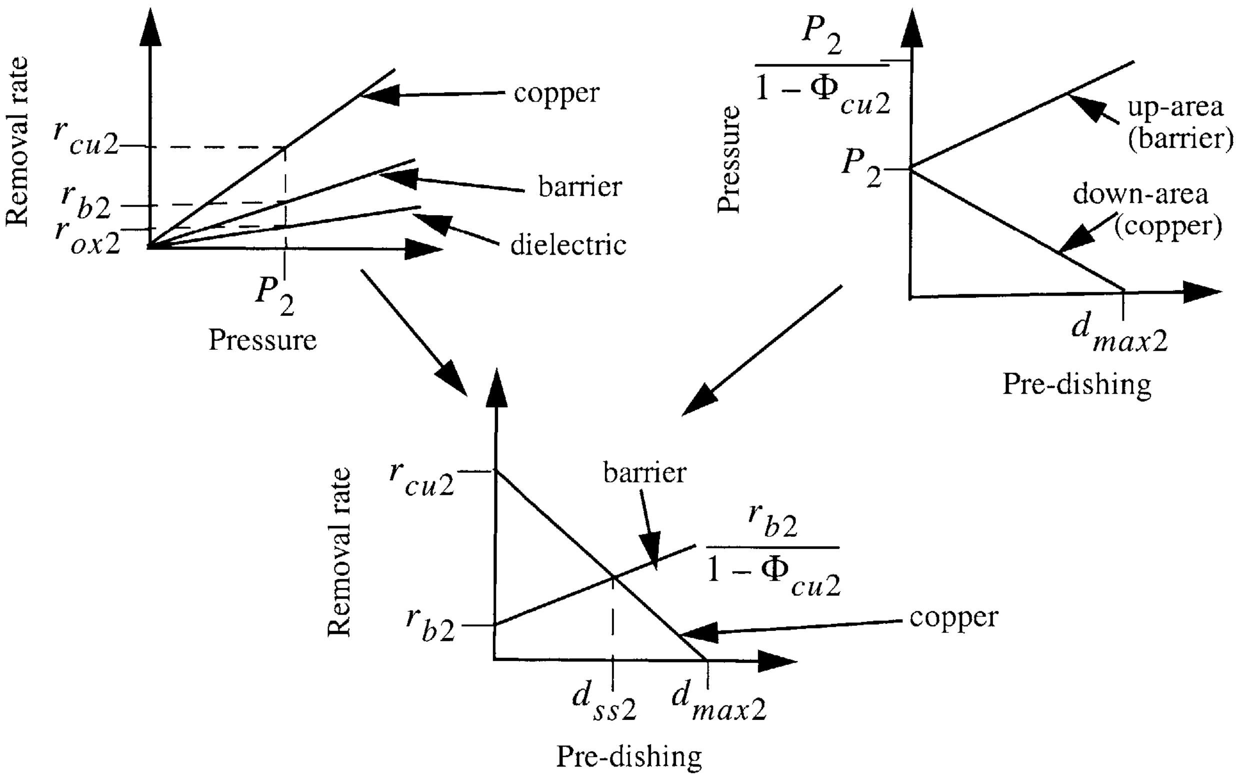


Figure 5.3: Formulation of removal rate diagram for intrinsic stage two (barrier removal) of step two in a three step copper CMP process

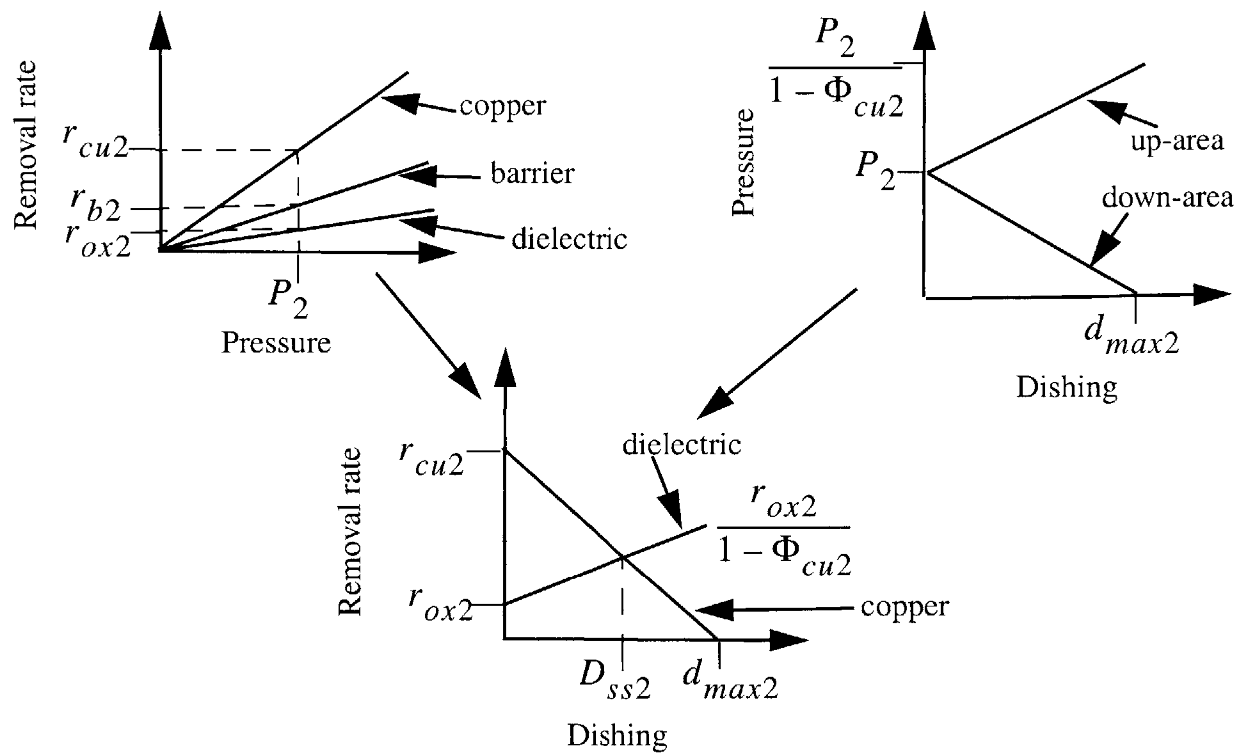


Figure 5.4: Formulation of the removal rate diagram for intrinsic stage three (overpolish) of step two in a three step copper CMP process

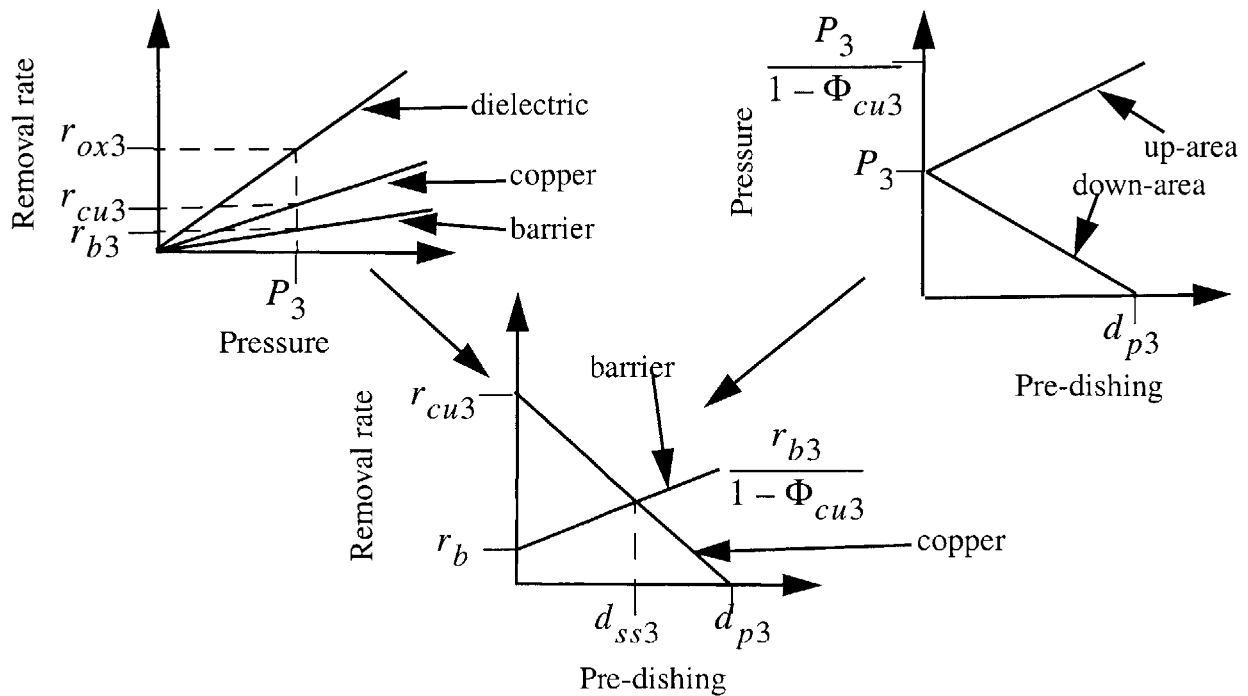


Figure 5.5: Formulation of the removal rate diagram for intrinsic stage two (barrier clearing) of step three in a three step copper CMP process

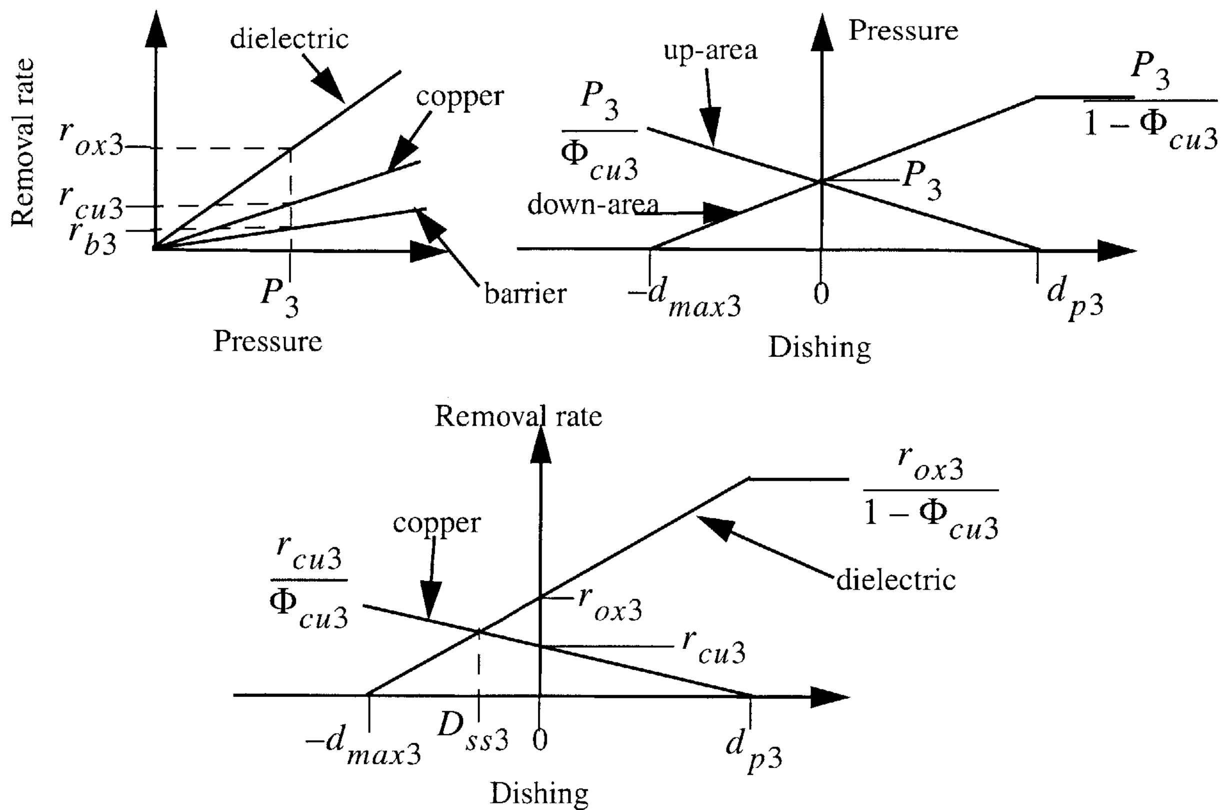


Figure 5.6: Formulation of the removal rate diagram in intrinsic stage three (overpolish) of step three in a three step copper CMP process

be large and positive. In this case, the third stage of the third step starts with the dielectric being the up-area and the copper being the down-area. If the initial dishing is greater than a critical dishing d_{p3}, there will be no removal of copper in the trench initially, and the dielectric in the space will be removed at a constant rate, initially. As polishing progresses, the dishing decreases. When the dishing becomes less than the critical dishing, the removal rate of the copper in the trench increases linearly as the dishing decreases, while that of the dielectric in the space decreases linearly as the dishing decreases. At a dishing of zero, the removal rate of the dielectric is the effective blanket dielectric removal rate r_{ox3}, while that of the copper is the effective blanket copper removal rate r_{cu3}. The inequality of these two effective removal rates forces dishing to become negative if polishing progresses beyond the time when dishing becomes zero. Ultimately,

a negative steady-state dishing of D_{ss3} is reached at which point the removal rate of the copper now in the up-area and that of the dielectric now in the down-area are equal. Recall that negative dishing means that the copper level is above the neighboring dielectric level.

The removal rate equations in steps one and two can be easily written from the removal rate diagrams for these steps. The removal rate diagram for the third stage of the third step is expressed mathematically in equations 5.1 - 5.2. These equations can be solved for the dishing and erosion during the third stage of the third step, as given in equations 5.3 - 5.14. The model parameters for a three step process, and all other variables used in the removal rate diagrams and the formulated equations are summarized in tables 5.1 - 5.4.

$$RR_{ox33} = \begin{cases} r_{ox3}\left(1 + \dfrac{D_{cu3}}{d_{max3}}\right) & -d_{max3} < D_{cu3} \le d_{p3} \\ \dfrac{r_{ox3}}{1 - \Phi_{cu3}} & D_{cu3} > d_{p3} \end{cases} \quad \textit{(Equation 5.1)}$$

$$RR_{cu33} = \begin{cases} r_{cu3} - r_{cu3}\left(\dfrac{1 - \Phi_{cu3}}{\Phi_{cu3}}\right)\dfrac{D_{cu3}}{d_{max3}} & -d_{max3} < D_{cu3} \le d_{p3} \\ 0 & D_{cu3} > d_{p3} \end{cases}$$

(Equation 5.2)

<u>Solving for dishing D_{cu3} and erosion E_{ox3} in the third intrinsic stage (overpolish stage) of step three, in a three step copper CMP process</u>

$$\frac{dD_{cu3}}{dt} = RR_{cu33} - RR_{ox33} \quad \textit{(Equation 5.3)}$$

$$\frac{dE_{ox3}}{dt} = RR_{ox33} \quad \text{(Equation 5.4)}$$

1. Case 1: $d_3 > d_{3p}$ (initial dishing in stage three of step three is greater than the critical dishing in the stage)

$$D_{cu3} = \begin{cases} d_3 - \frac{r_{ox3}}{1-\Phi_{cu3}} t & 0 \le t < t_{p3} \\ d_{p3} e^{\frac{-(t-t_{p3})}{\tau_{33}}} + D_{ss3}\left(1 - e^{\frac{-(t-t_{p3})}{\tau_{33}}}\right) & t \ge t_{p3} \end{cases} \quad \text{(Equation 5.5)}$$

$$E_{ox3} = \begin{cases} \frac{r_{ox3}}{1-\Phi_{cu3}} t & 0 \le t < t_{p3} \\ \frac{r_{ox3}}{1-\Phi_{cu3}} t_{p3} + X_3(t-t_{p3}) + Z_3\left(1 - e^{\frac{-(t-t_{p3})}{\tau_{33}}}\right) & t \ge t_{p3} \end{cases}$$

(Equation 5.6)

$$t_{3p} = \frac{(d_3 - d_{p3})(1-\Phi_{cu3})}{r_{ox3}} \quad \text{(Equation 5.7)}$$

$$D_{ss3} = \frac{d_{max3}(r_{cu3} - r_{ox3})\Phi_{cu3}}{r_{cu3}(1-\Phi_{cu3}) + r_{ox3}\Phi_{cu3}} \quad \text{(Equation 5.8)}$$

$$\tau_{33} = \frac{d_{max3}\Phi_{cu3}}{r_{cu3}(1-\Phi_{cu3}) + r_{ox3}\Phi_{cu3}} \quad \text{(Equation 5.9)}$$

$$X_3 = r_{ox3} + \frac{r_{ox3} D_{ss3}}{d_{max3}} \qquad \textit{(Equation 5.10)}$$

$$Z_3 = \frac{r_{ox3}\tau_{33}(d_{p3} - D_{ss3})}{d_{max3}} \qquad \textit{(Equation 5.11)}$$

2. Case 2: $d_3 \le d_{p3}$ (initial dishing in stage three of step three is less than the critical dishing in the stage)

$$D_{cu3} = d_3 e^{\frac{-t}{\tau_{33}}} + D_{ss3}\left(1 - e^{\frac{-t}{\tau_{33}}}\right) \quad t \ge 0 \qquad \textit{(Equation 5.12)}$$

$$E_{ox3} = X_3 t + Y_3\left(1 - e^{\frac{-t}{\tau_{33}}}\right) \quad t \ge 0 \qquad \textit{(Equation 5.13)}$$

$$Y_3 = \frac{r_{ox3}\tau_{33}(d_3 - D_{ss3})}{d_{max3}} \qquad \textit{(Equation 5.14)}$$

The critical dishing parameter in step three d_{p3} is the positive dishing above which no pressure is exerted on the copper in the down-area, and consequently, no removal of copper takes place above it. This parameter is similar to the maximum dishing parameter in intrinsic stage three of a single step copper CMP process in the sense that it is associated with a set-up wherein the copper in the trench is the down-area and the dielectric in the space is the up-area. Thus, it can be modeled with either of the empirical relationships given in equations 5.15 - 5.16, for conventional copper CMP processes. In these equations, s is the line space, in microns w is the line width in

microns, A_3 is a constant in units of angstroms and is greater than or equal to zero, s_o is a normalization line space equal to 1 μm, w_o is a normalization line width equal to 1 μm, s_1 is a dishing length scale (easily obtained from measured profilometer scans of polished arrays. It is about 100 μm - 250 μm for conventional CMP processes), α_3 and β_3 are unitless constants between zero and one, "ln" is the natural logarithmic function, and s_{min} is an effective minimum line space in microns.

$$d_{p3} = \begin{cases} A_3\left(\frac{w}{w_o}\right)^{\alpha_3}\left(\frac{s}{s_o}\right)^{\beta_3} & 0 < s \le s_1 \\ A_3\left(\frac{w}{w_o}\right)^{\alpha_3}\left(\frac{s_1}{s_o}\right)^{\beta_3} & s > s_1 \end{cases} \qquad \text{(Equation 5.15)}$$

$$d_{p3} = A_3\left(\frac{w}{w_o}\right)^{\alpha_3}\ln\left(\frac{s}{s_{min}}\right) \qquad s \ge s_{min} \qquad \text{(Equation 5.16)}$$

Table 5.1: Relevant model parameters in step one of a three step process

Intrinsic stage one		Intrinsic stage two		Intrinsic stage three	
	Description				
r_{cu1}	Effective copper blanket removal rate	N/A		N/A	
L_{11}	Planarization length				
H_{ex11}	Critical step height				

Table 5.2: Relevant model parameters in step two of a three step process

Intrinsic stage one		Intrinsic stage two		Intrinsic stage three	
	Description		Description		Description
r_{cu2}	Effective copper removal rate	r_{cu2}	Effective blanket copper removal rate	r_{cu2}	Effective blanket copper removal rate
		r_{b2}	Effective blanket barrier removal rate	r_{ox2}	Effective blanket dielectric removal rate
		L_{23}	Planarization length	L_{23}	Planarization length
		d_{max2}	Maximum dishing	d_{max2}	Maximum dishing
		ψ_2	Edge rounding factor (if necessary)	ψ_2	Edge rounding factor (if necessary)

Table 5.3: Relevant model parameters for step three of a three step process

Intrinsic stage one		Intrinsic stage two		Intrinsic stage three	
			Description		Description
N/A		r_{cu3}	Effective blanket copper removal rate	r_{cu3}	Effective blanket copper removal rate
		r_{b3}	Effective blanket barrier removal rate	r_{ox3}	Effective blanket dielectric removal rate
		L_{33}	Planarization length	L_{33}	Planarization length
		d_{p3}	Maximum dishing in step two (same as critical dishing in stage three)	d_{p3}	Critical dishing in step three (related to the maximum dishing in stage three, and same as maximum dishing in stage two)
		ψ_3	Edge rounding factor (if necessary)	ψ_3	Edge rounding factor (if necessary)

Table 5.4: Description of other variables used in the removal rate diagrams and equations derived earlier

Variable	Description
RR_{cu33}	Copper removal rate in stage three of step three
RR_{ox33}	Dielectric removal rate in stage three of step three
P_i	Applied pressure in the i th step
ρ_{cu1}	Effective electroplated copper pattern density in step 1
Φ_{cui}	Effective layout copper pattern density in the i th step
D_{ssi}	Steady state dishing in the i th step
d_{ssi}	Steady state pre-dishing in the i th step
D_{cui}	Dishing in the i th step
E_{oxi}	Erosion in the i th step
d_3	Dishing at the start of stage three in step three

The critical dishing d_{p3} in step three is related to the maximum dishing d_{max3} (the maximum dishing is defined as a positive quantity) in that step as given in equation 5.17. This relationship can be derived from the removal rate diagram for stage three of step three, shown in figure 5.6. In the case of a wide array of lines (wider than the planarization length) with constant line width and space, the effective copper layout pattern density is related to the line width and space as given in equation 5.18. Substituting this relationship in equation 5.17 leads to equation 5.19. The d_{max3} versus d_{p3} relationship given in equation 5.19 stresses the local nature of both parameters. Generally, it is recommended to use equation 5.19 to relate d_{max3} to d_{p3} when dealing with random layouts, where the arrays are not necessarily wide, and the line spaces and widths for an array are not necessarily constant.

The maximum dishing parameter d_{max3} in stage three of step three is associated with the case where the copper in the trench is the up-area, and the dielectric in the space is the down-area. Therefore, by duality, it could be modeled by either of the empirical functions given in equations 5.20 - 5.21, for conventional copper CMP processes. In these equations, w is the line width in microns, s the line space in microns, w_o a normalization line width of 1 μm, s_o a normalization line space of 1 μm, w_1 the dishing length scale in microns similar to s_1 in equation 5.15, w_{min} the effective minimum line width similar to the effective minimum line space s_{min} in equation 5.16, B_3 a constant in units of angstroms and is greater than or equal to zero, and λ_3 and η_3 are unitless constants between zero and one.

$$d_{max3} = d_{p3}\left(\frac{1-\Phi_{cu3}}{\Phi_{cu3}}\right) \quad \text{(Equation 5.17)}$$

$$\Phi_{cu} = \frac{w}{w+s} \quad \text{(Equation 5.18)}$$

$$d_{max3} = d_{p3}\left(\frac{s}{w}\right) \quad \text{(Equation 5.19)}$$

$$d_{max3} = \begin{cases} B_3\left(\frac{s}{s_o}\right)^{\lambda_3}\left(\frac{w}{w_o}\right)^{\eta_3} & 0 \le w < w_1 \\ B_3\left(\frac{s}{s_o}\right)^{\lambda_3}\left(\frac{w_1}{w_o}\right)^{\eta_3} & w \ge w_1 \end{cases} \quad \text{(Equation 5.20)}$$

$$d_{max3} = B_3\left(\frac{s}{s_o}\right)^{\lambda_3}\ln\left(\frac{w}{w_{min}}\right) \qquad w \ge w_{min} \quad \text{(Equation 5.21)}$$

5.2 Calibration Methodology for Multi-Step Copper CMP Processes

Calibrating a multi-step copper CMP process involves conducting CMP experiments, metrology, and extracting the model parameters. It was stated earlier that not all intrinsic stages are relevant for the respective single step processes that comprise a multi-step process. Consequently, only experiments that capture the parameters in the relevant intrinsic stages must be conducted. The calibration experiments for a three step copper CMP process are described below. This is followed by a description of the model parameter extraction methodology.

5.2.1 Calibration Experiments and Metrology

The experiments and metrology needed to calibrate a three step copper CMP process are described below.

1. Wafer processing: The processing needed is the same as in the case for a single step copper CMP process.
2. Pre-CMP metrology: The measurements needed are similar to those needed for the calibration of a single step copper CMP process.
3. Step one polish experiments: Only bulk copper polishing occurs in this step. Hence, the experiments needed to calibrate this step are exactly the same as those used to calibrate intrinsic stage one of a single step copper CMP process.
4. Step two polish experiments: The polish process in step two is intended to clear the bulk copper remaining after step one. Because the bulk copper remaining after step one polish is typically pattern-free, i.e., almost all step heights are eliminated after step one polish, there is no need to conduct experiments intended to capture the bulk copper thickness evolution in this step. The typical polish time in step two is the end-point time plus an additional polish time to

ensure complete clearing of the remaining bulk copper. Thus, overpolish experiments are needed to properly calibrate the process in step two.

First, blanket wafer experiments must be conducted. The polish time in step two is typically long enough and the removal rates are low enough, such that the effective blanket copper, barrier, and dielectric removal rates can be treated as constants. For instance, a typical step two process has a measured blanket copper instantaneous removal rate in the range 2000 - 3500 Å/min, and barrier and dielectric blanket instantaneous removal rates in the range 20 - 350 Å/min. The measured blanket average removal rates in this step are representative of the measured blanket instantaneous removal rates. Thus, only three blanket copper wafers, three blanket barrier wafers, and three dielectric wafers need to be polished. The blanket copper wafers should be polished for 40 s, 60 s, and 90 s respectively, and the blanket dielectric and barrier wafers should be polished for 60 s, 90 s, and 120 s respectively.

After the blanket wafers have been polished, the overpolish experiments must be conducted. Overpolish experiments involve polishing at least four patterned copper wafers in step one, targeting the norminal thickness typically removed in that step on all four of them. Then, each wafer should be polished in step two for a different polish time including the end-point time t_{ep} and overpolish: t_{ep}, $t_{ep} + t_1$, $t_{ep} + 2t_1$, and $t_{ep} + 3t_1$, respectively. Alternatively, the polish times could be $t_{ep} - t_1$, t_{ep}, $t_{ep} + t_1$, and $t_{ep} + 2t_1$, respectively. The time t_1 should be chosen based on knowledge of the measured instantaneous blanket copper removal rate in step two, and a targeted amount of blanket copper thickness removed.

5. Step three polish experiments: The polish process in step three is intended to clear any barrier residue across the wafer. Generally, by the time this step is started, no bulk copper residue remains on the wafer. Thus, only barrier polishing and overpolishing occur in this step. First,

the instantaneous blanket copper removal rate, instantaneous blanket barrier removal rate, and the instantaneous blanket dielectric removal rate should be measured. These rates are typically low (300 - 1800 Å/min), and are attained almost "instantaneously". Three blanket copper wafers, three blanket barrier wafers and three blanket dielectric wafers should be polished for 60 s, 90 s, and 120 s respectively, and the average of the removal rates for each material is an accurate measure of the instantaneous blanket removal rate for that material.

After the blanket wafer experiment is conducted, at least four patterned copper wafers should be polished in step one, targeting the nominal amount removed in that step, followed by polishing in step two for the norminal polish time (i.e., end-point time plus the norminal time that is added to the end-point time to ensure complete bulk copper clearing), and polishing in step three for fixed times of 20 s, 40 s, 60 s and 75 s or 80 s respectively.

6. Post-CMP metrology: The post-CMP metrology and the data filtering for multi-step copper CMP processes are similar to those done for single step copper CMP processes.

5.2.2 Model Parameter Extraction Methodology

Extraction of model parameters involves minimizing the RMS error between the model equations and the measured data, subject to several constraints. Some of the constraints include limiting the possible values of the model parameters in order to obtain results that are in line with the known physics of the process. The procedures for extracting the model parameters in a three step process are described below. It is important to note that the model parameters for each step are extracted independent of those for the other steps.

1. Extraction of model parameters for step one polish process: The relevant model parameters in step one are listed in table 5.1. The procedure for extracting these parameters is similar to that used for extracting the model parameters in stage one of a single step copper CMP process.

2. Extraction of model parameters for step two polish process: The relevant modeling parameters in this step are listed in table 5.2. The procedure for extracting these parameters is similar to that used for extracting the model parameters in stage three of a single step copper CMP process. The effective blanket copper rate is set equal to the measured instantaneous copper blanket removal rate, while the effective blanket dielectric removal rate is floated in a range of values including the measured instantaneous dielectric removal rate. This is done because the measured instantaneous dielectric removal rate in this step is typically small. The effective blanket barrier removal rate is obtained from the measured instantaneous dielectric removal rate, the measured instantaneous barrier removal rate, and the extracted effective dielectric removal rate, using the same method described in section 3.7.2 of chapter 3.
3. Extraction of model parameters for step three polish process: Figure 5.7 illustrates the extraction methodology in step three. The relevant model parameters in this step are listed in table 5.3. Using the measured dishing and erosion data and the measured blanket wafer data in step three, all parameters are extracted. It has been found that for conventional copper CMP processes, the edge rounding effect must be included if the model is to fit the data very well. Including the edge rounding effect introduces two more parameters. Hence, it is practical to set the effective blanket removal rates to the measured instantaneous blanket removal rates to reduce the number of unknowns, and avoid over fitting.

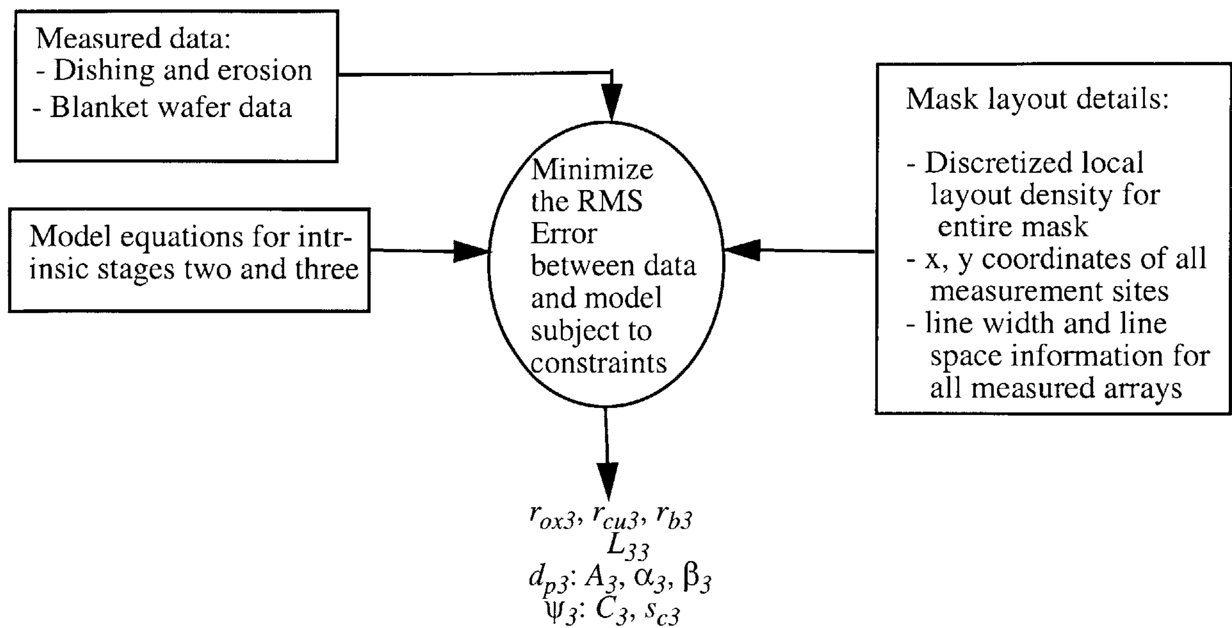


Figure 5.7: Model parameter extraction methodology for step three of a three step process

5.2.3 Checking the Accuracy of the Extraction Results

The extraction results in each step must be checked for accuracy. In step one the extracted parameters, the initial copper thicknesses and the model equations, are used to predict the remaining copper thicknesses or the amount of copper thicknesses removed at certain sites not used in the extraction procedure, if data is available for such sites. In step two, the measured dishing and erosion at end-point time (or the lowest polish time), the extracted parameters, and the model equations are used to predict the dishing and erosion for the array structures not used in the extraction procedure (for all polish times excluding the minimum polish time). In addition, prediction of the erosion at the field sites not used in the extraction should also be done, if measurements are available for such field sites. In step three, using the measured dishing and erosion data after norminal steps one and two polishing as the initial condition, the extracted model parameters and the model equations, the dishing and erosion for the array and field sites not used in the extraction procedure should be predicted. The predicted results should be

compared to the available measured data.

After checking the accuracy of the model parameter extraction in each of the three polish steps separately, the accuracy of the parameters should be checked together. This is done by running a full simulation of the entire three step polish process to predict the dishing and erosion after step two polish and the dishing and erosion after step three polish for arrays and field sites used in the extraction as well as those not used in the extraction. The extraction of parameters is done independently in each polish step. The accuracy of this overall simulation indicates how well the different steps fit together in the model, as one unit.

5.3 Model Fits versus Experimental Data for Multi-Step Copper CMP Processes

To test the model and the calibration methodology proposed for multi-step copper CMP processes, a comprehensive CMP experiment is conducted for a three step polish process, on Applied Materials Mirra tool. The dielectric used is oxide, the barrier used is tantalum nitride (TaN), and the MIT mask version 1.2 is used to pattern the copper wafers for the experiment. The experimental design is summarized in tables 5.5 - 5.11. Model parameter extraction and a verification of the accuracy of the extraction are done in the subsections following the experimental description.

Table 5.5: Three step process experimental design

Step #	Platen #	Pad	Slurry	Down force (psi)	Speed (rpm)
1	1	Stacked	EPC-5001	5	63
2	2	Stacked	EPC-5001	2	43
3	3	Stacked	10K-1	3	100

Table 5.6: Blanket copper wafer experiments in polish step one

Wafer number	Polish time (s)
B-1	7
B-2	15
B-3	23
B-4	31
B-5	40
B-6	50

Table 5.7: Patterned wafer experiments with monitor blanket wafers in polish step one

Wafer number	Copper wafer type	Targeted copper thickness remaining (kÅ)	Polish time (s)
P-1	Pattern	13.5	14
B-7	Blanket	N/A	14
P-2	Pattern	11	29
B-8	Blanket	N/A	29
P-3	Pattern	8.5	43
B-9	Blanket	N/A	43
P-4	Pattern	6	58
B-10	Blanket	N/A	57
P-5	Pattern	3.5	64
B-11	Blanket	N/A	65

Table 5.8: Blanket wafer experiments in polish step two

Wafer number	Wafer material	Polish time (s)
B-12	Copper	40
B-13	Copper	60
B-14	Copper	90
C-1	Oxide	60
C-2	Oxide	90

Table 5.8: Blanket wafer experiments in polish step two

Wafer number	Wafer material	Polish time (s)
C-3	Oxide	120
D-1	Barrier	60
D-2	Barrier	90
D-3	Barrier	120

Table 5.9: Copper pattern wafer experiments in polish step two

Wafer number	Nominal polish time in step one (s)	End-point time in step two (s)	Total polish time in step two (s)
P-6	63	76	76
P-7	67	74	94
P-8	63	75	110
P-9	63	74	124
P-10	65	78	98

Table 5.10: Blanket wafer experiments in polish step three

Wafer number	Wafer material	Polish time (s)
B-15	Copper	60
B-16	Copper	90
B-17	Copper	120
C-4	Oxide	60
C-5	Oxide	90
C-6	Oxide	120
D-4	Barrier	60
D-5	Barrier	90
D-6	Barrier	120

Table 5.11: Copper pattern wafer experiments in polish step three

Wafer number	Norminal polish time in step one (s)	Norminal polish time in step two: (End-point time + 20 s) (s)	Total polish time in step three (s)
P-11	63	99	20
P-12	67	98	35
P-13	63	100	50
P-14	63	102	65

5.3.1 Extraction of Model Parameters for Step One Polish Process

The amount of copper removed on the blanket wafers is plotted against polish time in figure 5.8. Using equation 3.51 to analyze this data, the extracted fitting parameters associated with the effective blanket copper removal rate r_{cu1} (a_1, a_2 and τ_r) are given in table 5.12 (the effective blanket copper removal rate is set equal to the measured instantaneous blanket copper removal rate.). The plot of the modeled amount of copper removed, average blanket copper removal rates versus measured data, and modeled instantaneous removal rate are shown in figures 5.9 - 5.10.

Table 5.12: Parameters for effective blanket copper removal rate in step one, as per equation 3.51

r_{cu1} (Å/s)			RMS Error (Å)
a_1 (Å/s)	a_2 (Å)	τ_r (s)	
249.5	3986.6	16.4	168.5

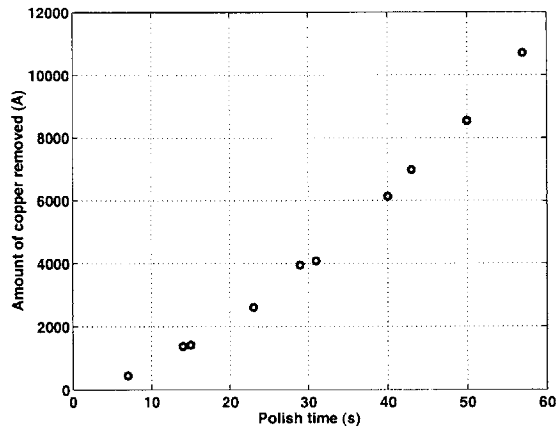
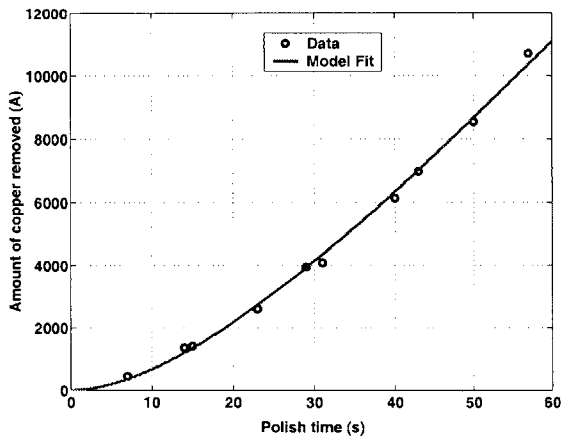


Figure 5.8: Amount of copper removed on blanket wafers versus polish time



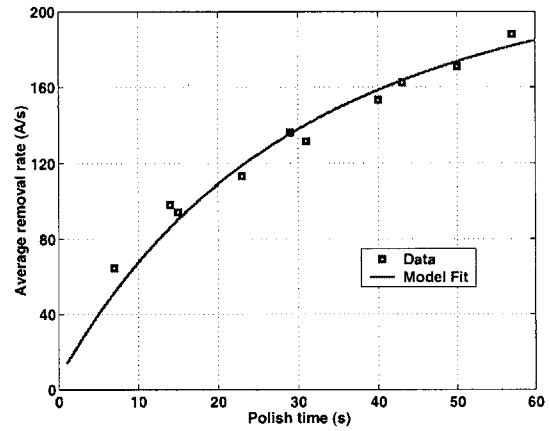


Figure 5.9: Model fit versus data for blanket copper removal rate, as per equation 3.50

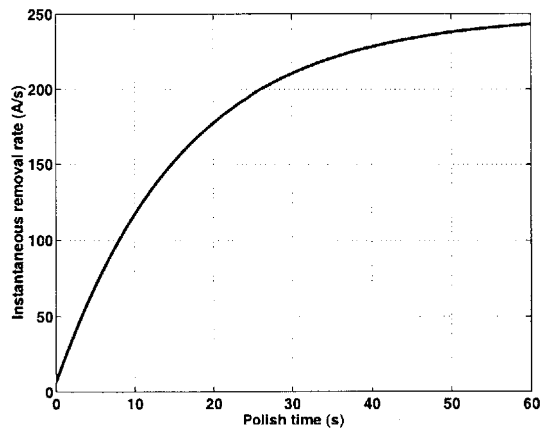


Figure 5.10: Extracted effective blanket copper removal rate for step one process versus time

Figure 5.11 shows a plot of the measured step height versus polish time for the 100 μm line width, and 100 μm line space array structure on the test mask used in the experiment. From the figure, it is clear that the step height decreases linearly with polish time until the step height is approximately zero. This indicates that the parameter H_{ex11} is negligible to first order, for this structure. This structure has the largest line width and space of all the arrays used in the extraction. If its value of H_{ex11} is negligible, then all other structures used in the extraction procedure should have negligible H_{ex11} values also. Hence, in extracting the model parameters for step one, H_{ex11} is considered negligible.

Using the extracted effective blanket copper removal rate parameters shown in table 5.12, the planarization length (L_1) in step one is extracted using the procedure for extracting intrinsic stage one model parameters for a single step process. The step one extracted model parameters are summarized in table 5.13. The model fit versus the measured data for the amount of copper removed at several array and field sites, are shown in figure 5.12. The array and field sites used in the extraction of the model parameters are illustrated in figure 5.13.

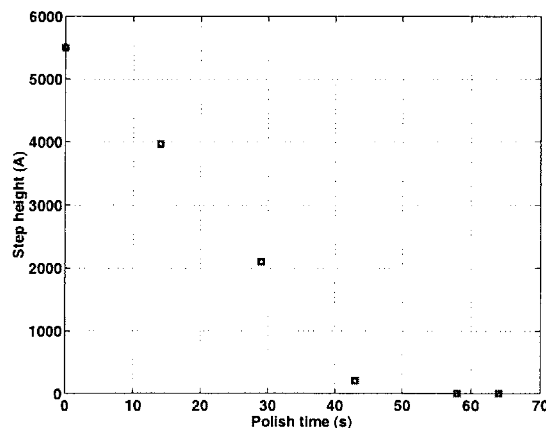
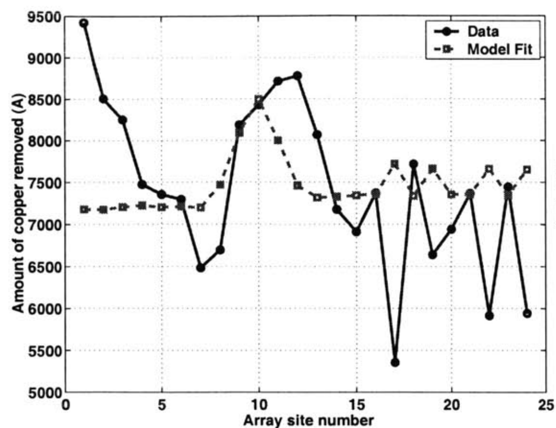
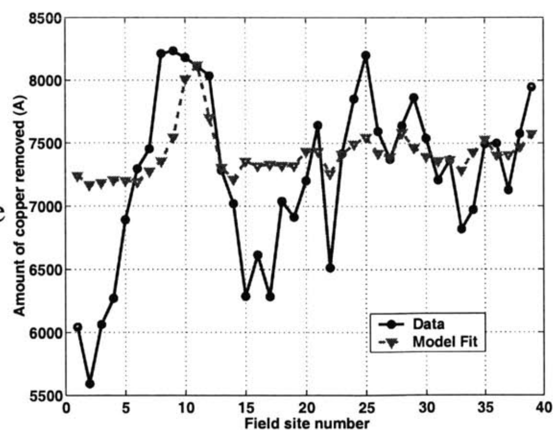
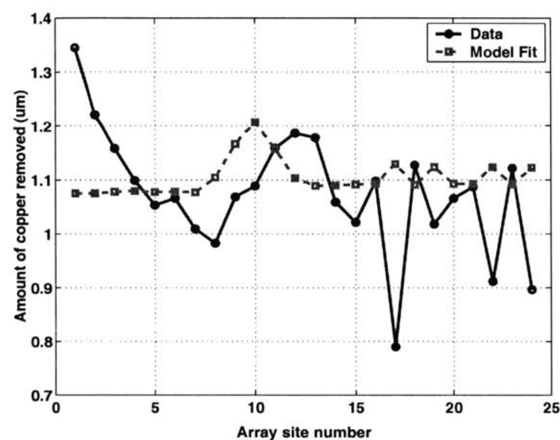


Figure 5.11: Step height versus polish time for 100 μm line width, 100 μm line space structure array structure, in step one

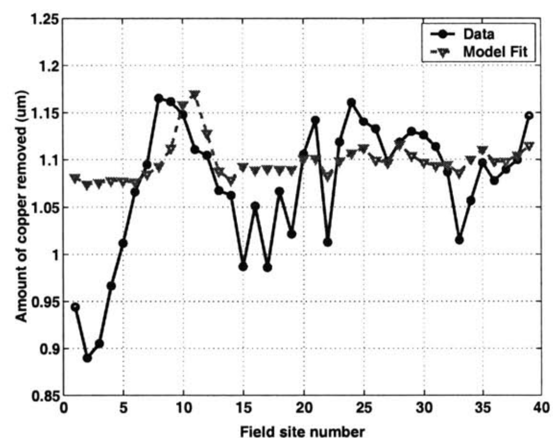


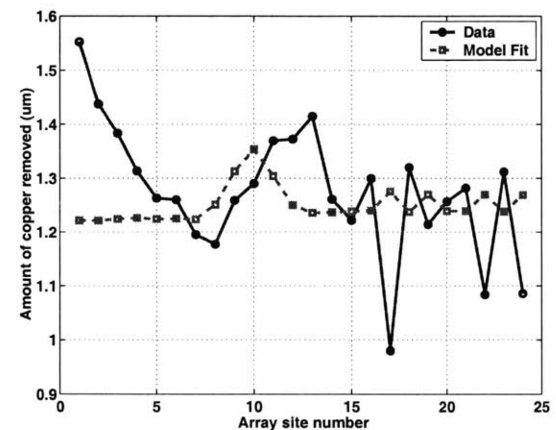
Step one polish time = 43 s



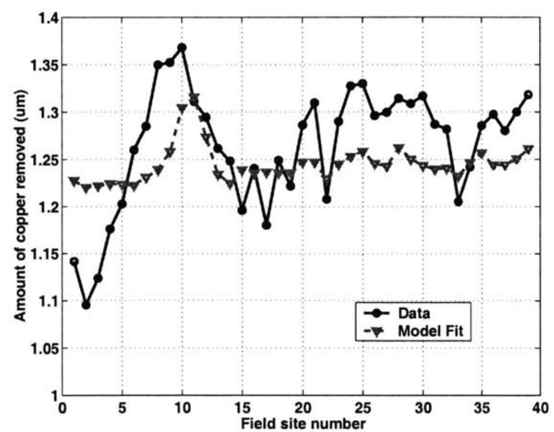


Step one polish time = 58 s





Step one polish time = 64 s



(a) (b)

Figure 5.12: Model fits versus experimental data for model parameter extraction in step one: (a) Array up-area site (b) Field sites

Table 5.13: Extracted model parameter values in step one

L_{11} (μm)	r_{cu1} (Å/s)			H_{ex11} (Å)			RMS Error (Å)
	a_1 (Å/s)	a_2 (Å)	τ_r (s)	A_1 (Å)	α_1	β_1	
4893	249.5	3986.6	16.4	N/A	N/A	N/A	817

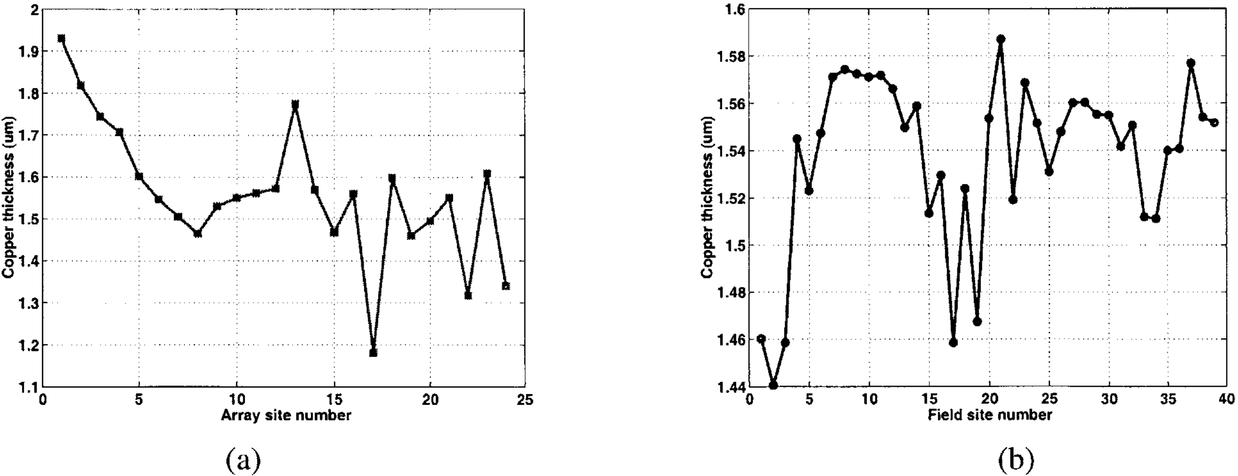
(a) (b)

Figure 5.13: Array and field site numbers of sites used in extraction of model parameters, for three-step copper CMP process (the mask is MIT mask version 1.2): (a) Array up-area sites (b) Field sites

The extracted planarization length L_{11} is 4894 μm, and the RMS error of the extraction is 817 Å. The planarization length is slightly higher than expected, and the error is high. The individual errors at the different spatial sites used in the extraction have a large spread, and this makes the results unacceptable. As seen in figure 5.12, the model generally does not fit the data very well. This result exposes one of the limitations of the density-step-height model: the model

wrongly assumes that all up-areas are initially contacted by the pad and abrasive combination with a non-zero pressure.

The incoming electroplated copper topography exhibits long range height variation which affects the pressure on the up-areas and down-areas. Figure 5.14 shows plots of measured initial electroplated thickness at the array and field sites shown in figure 5.13. Note that these thicknesses are measured relative to the top of the barrier film. Hence the variation in the measured thicknesses represent long range height variation. If the long range height variation is large, the pad and abrasive combination might not be contacting certain up-areas initially. At sites where there is contact, the polish pressure might be larger than or less than the pressure computed by the density-step-height model. In addition, as polishing progresses and the long range height variation changes, the pressure needs to be re-distributed to account for this change. The density-step-height model fails to do this.



(a) (b)

Figure 5.14: Measured initial electroplated copper thickness: (a) Array up-area sites (b) Field sites

In an attempt to remedy this flaw in the model, and minimize the RMS error, the extraction procedure gives a longer planarization length. This planarization length is influenced by the long range height variation in the plating topography. As stated in section 3.4.1 of chapter

3, the planarization length is supposed to be independent of topography. An improvement is made to the density-step-height model in chapter 6 to remedy this limitation. It is worth mentioning that the density-step-height model works well in cases where the electroplated topography is conformal. In these cases, long range height variation in the incoming electroplated thickness is minimal or ideally non-existent, i.e., the up-areas for all structures are at the same height after electroplating, or the differences in these heights are small.

5.3.2 Extraction of Model Parameters for Polish Step Two Process

The blanket copper, dielectric, and barrier wafer experimental data are shown in figures 5.15 - 5.17. Also shown in these figures are the fits to the data presented, as dictated by equation 3.51 in chapter 3. The linear fits obtained for the amount of material removed on the blanket wafer implies that the measured instantaneous blanket removal rates and the measured average blanket removal rates are the same in this step, as was discussed in section 5.1.1. The measured instantaneous blanket removal rates are summarized in table 5.14.

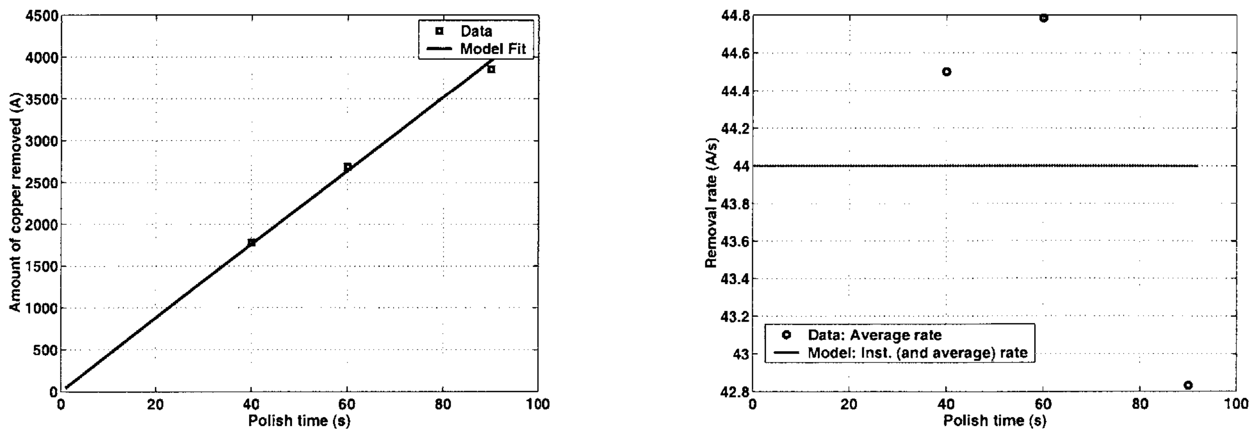
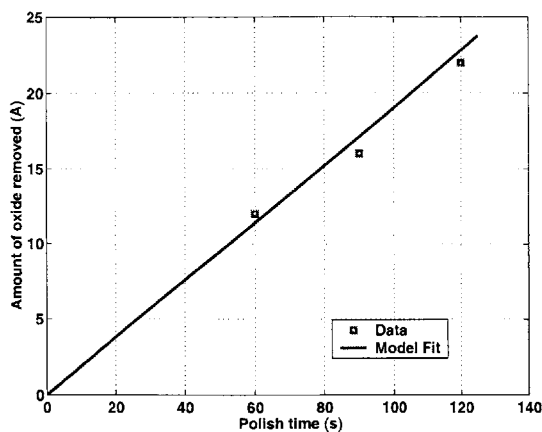


Figure 5.15: Amount of copper removed and measured blanket removal rate vs. time, for step two process



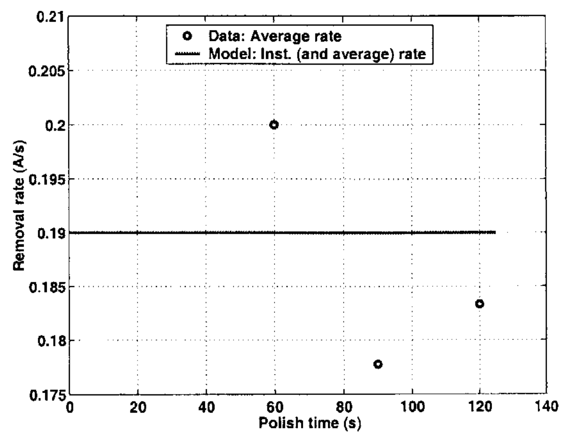
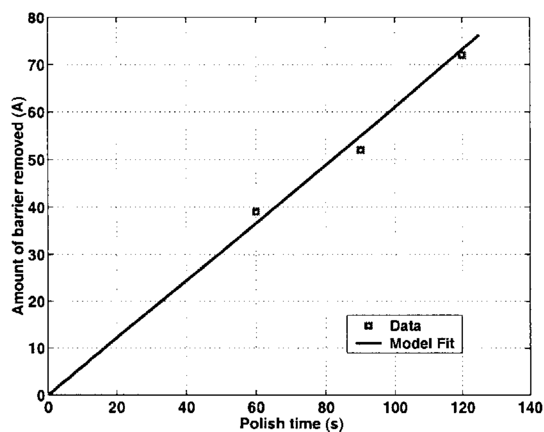


Figure 5.16: Amount of oxide removed and measured blanket oxide removal rate vs. time, for step two process



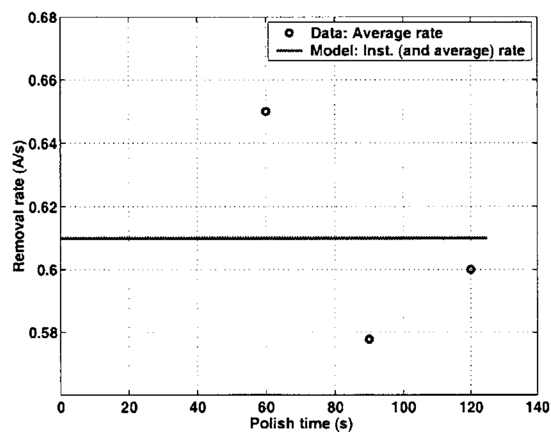
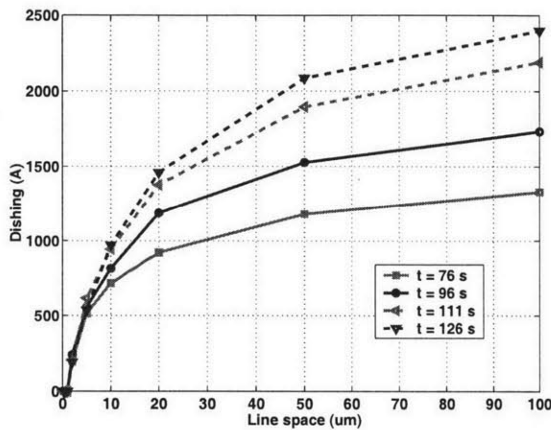


Figure 5.17: Amount of barrier removed and measured blanket barrier removal rate vs. time, for step two process

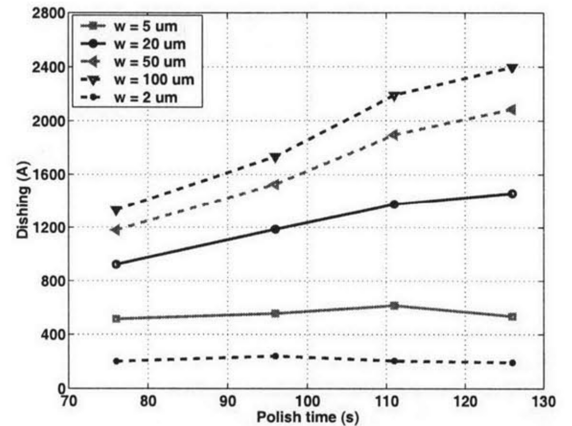
Table 5.14: Instantaneous blanket wafer polish rates as extracted from blanket wafer data, using equation 3.51

Instantaneous rate	a_1 (Å/s)	a_2 (Å)	τ_r (s)	RMS Error in amount removed (Å)
$\bar{r}_{cu2}$ (Å/s)	44	0	0	67
$\bar{r}_{ox2}$ (Å/s)	0.19	0	0	0.86
$\bar{r}_{b2}$ (Å/s)	0.61	0	0	0.46

Figures 5.18 shows a plot of measured dishing versus line width for different polish times, and a plot of measured dishing versus polish time for several arrays. From these figures, it is clear that dishing reaches steady state rather quickly for small feature sizes. Also, the higher the line width, the higher the dishing, for a fixed pattern density. Figure 5.19 shows a plot of measured erosion versus polish time for different arrays, as well as a plot of measured erosion versus pattern

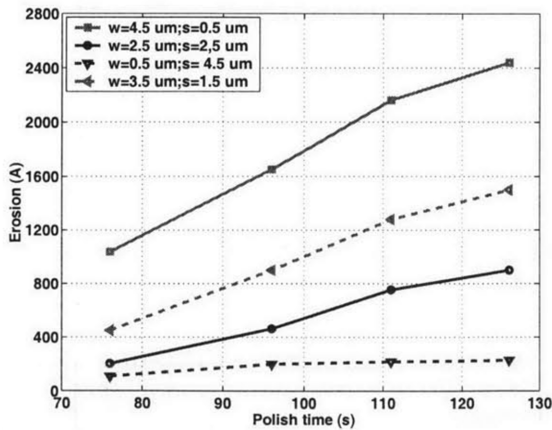


(a)

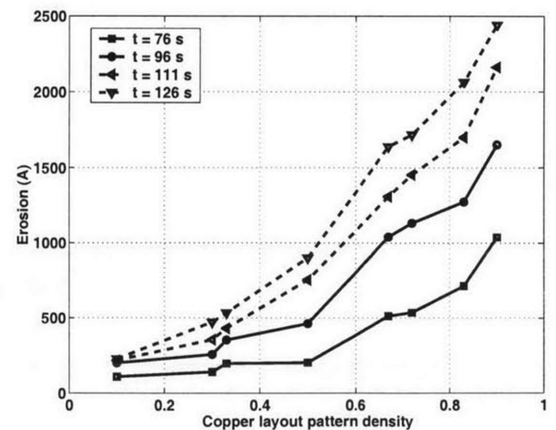


(b)

Figure 5.18: Measured dishing versus polish time in step two and line width, for arrays with line width equal to line space: (a) t represents polish time (b) w represents line width



(a)



(b)

Figure 5.19: Measured erosion versus polish time and density for several array structures: (a) w and s represent line width and line space respectively (b) t represents polish time

density for different polish times. The higher the pattern density, the higher the erosion. In addition, the higher the polish time, the higher the erosion.

Using the measured dishing and erosion data at the array sites shown in figure 5.12, the measured blanket wafer rate information shown in table 5.14, and the extraction procedure described in section 5.1.1, the model parameters for step two are extracted as summarized in table 5.15. The effective blanket copper removal rate r_{cu2} is set equal to the measured instantaneous blanket copper removal rate given in table 5.12. The effective blanket dielectric rate is allowed to float in a range during the extraction. In the case where no edge rounding effect is included in the model equations (the extracted parameters for this case are in the first row of table 5.14), the possible range is from $0.5\bar{r}_{ox2}$ to $15\bar{r}_{ox2}$, where $\bar{r}_{ox2}$ is the measured instantaneous blanket dielectric removal rate. In the case where the edge rounding effect is included in the model equations (the extracted model parameters for this case are in the second row of table 5.14), the range is from $0.3\bar{r}_{ox2}$ to $5\bar{r}_{ox2}$. The effective blanket barrier removal rate is extracted from the measured instantaneous blanket dielectric rate, the measured instantaneous blanket barrier removal rate and the extracted effective blanket dielectric removal rate, using equation 3.56 in chapter 3.

Table 5.15: Extracted model parameters in step two

r_{cu2} (Å/s)	r_{ox2} (Å/s)	r_{b2} (Å/s)	L_{23} (μm)	d_{max2} (Å)			Ψ_2		RMS Error (Å)
				B_2 (Å)	α_2	β_2	C_2	s_{c2}	
44	7.95	25.5	1596	159.3	0.467	0.468	N/A	N/A	120
44	2.36	7.58	2456	173.6	0.427	0.331	4.03	4.19	73

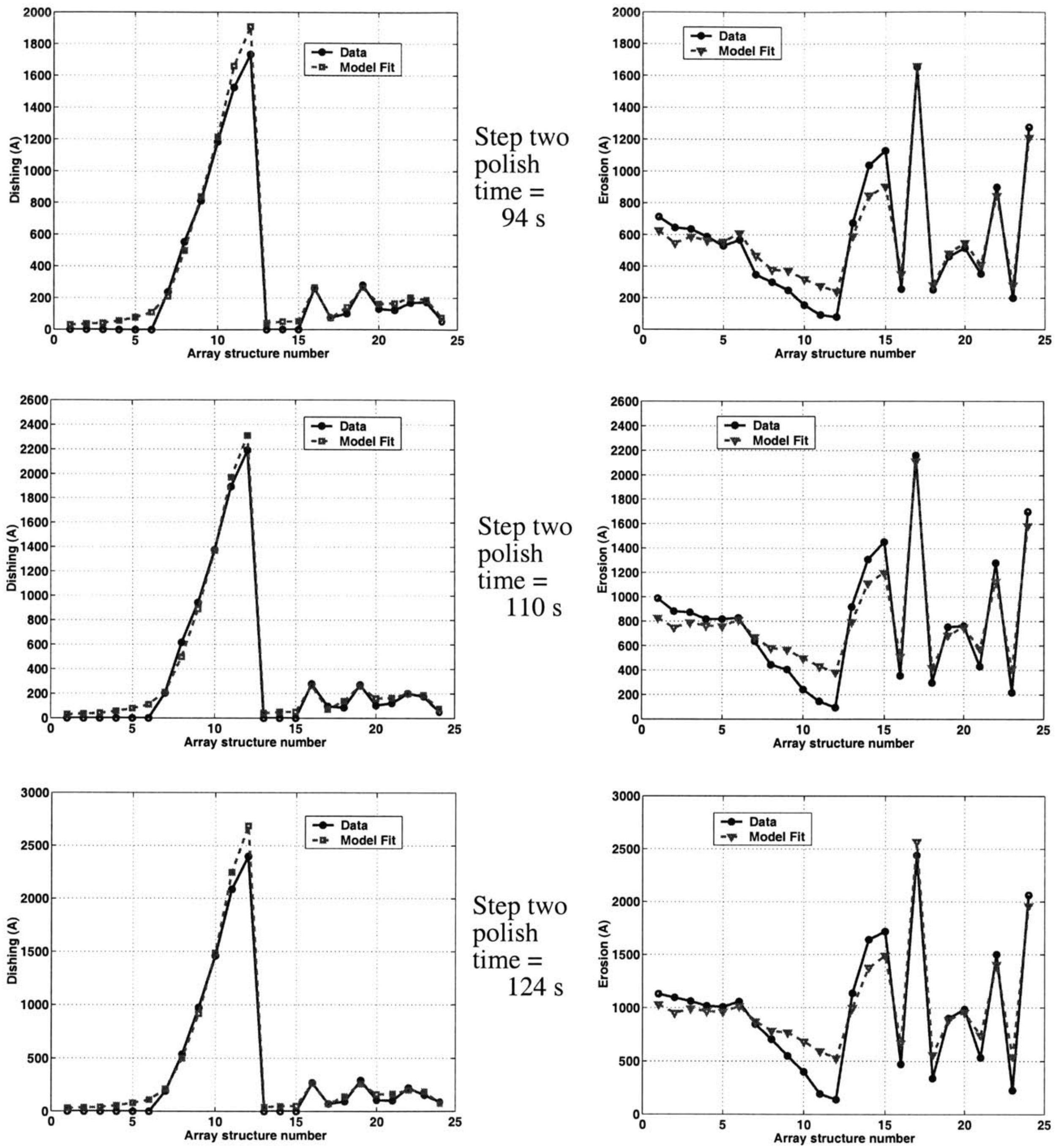
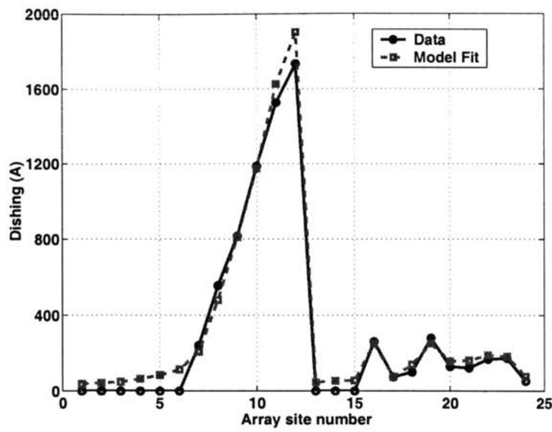
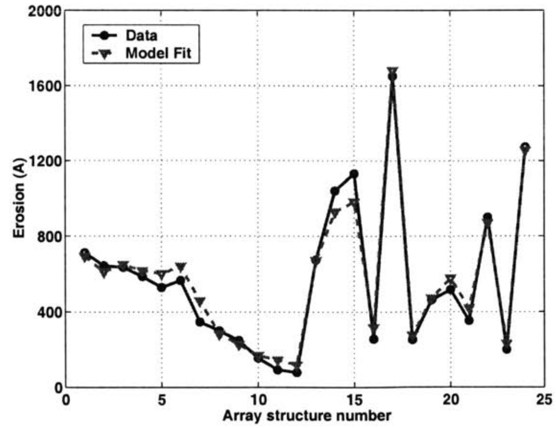
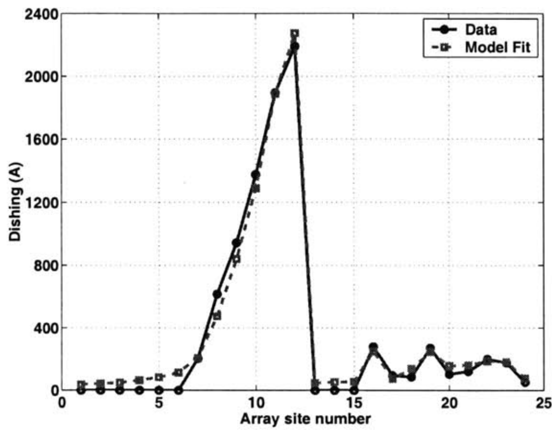


Figure 5.20: Model fits versus experimental data for model parameter extraction in step two, with no edge rounding effect included in the model equations

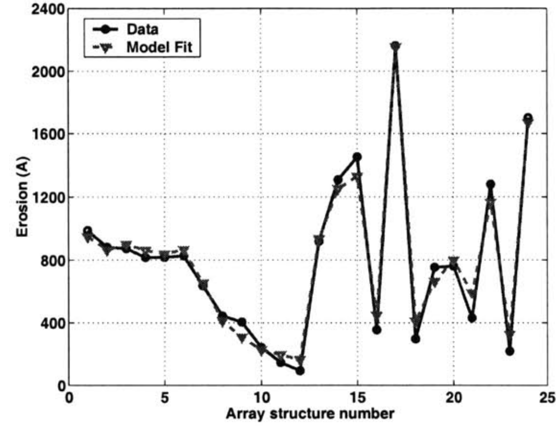


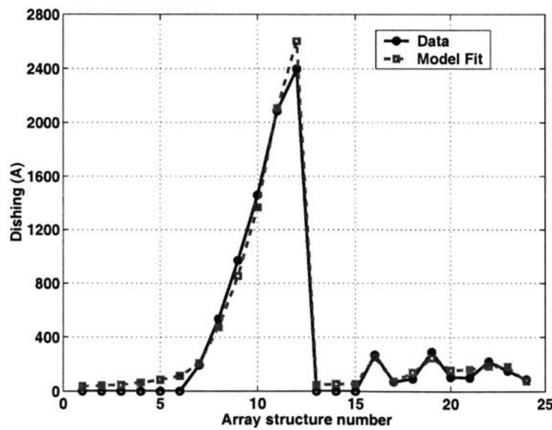
Step two polish time = 94 s





Step two polish time = 110 s





Step two polish time = 124 s

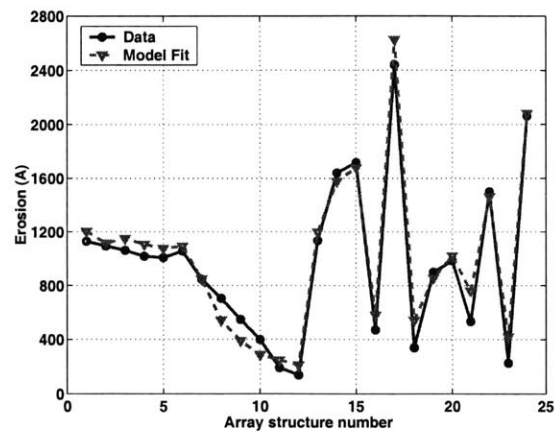


Figure 5.21: Model fits versus experimental data for extraction in step two, with the edge rounding effect included in the model equations

The extracted effective blanket oxide removal rate is much higher than the measured instantaneous blanket oxide removal rate when no edge rounding effect is taken into

consideration, and it is closer to the measured instantaneous blanket removal rate when the edge rounding effect is included in the model equations. Figures 5.20 shows plots of the model fit versus experimental data for the case when the edge rounding effect is not included in the model equations, while figure 5.21 shows plots of the model fit versus experimental data for the case when the edge rounding effect is included in the model equations. Generally, the model fits the data very well for all the array sites used in the extraction. The fit is much better for the erosion data when the edge rounding effect is taken into account. It is important to note that the long range height variation that affected the accuracy of the extraction results in step one does not exist in this step. By the time the overpolishing stage is reached in step two, the long range height variation in the electroplated copper thicknesses has already been minimized significantly. In addition, because the overpolish experiments did not involve excessive overpolishing, the limitation of the density-step-height model described in chapter 3 is not an issue in this case.

5.3.3 Extraction of Model Parameters for Step Three Process

The measured instantaneous blanket rates in step three are constant as expected. Table 5.16 gives the values of these measured rates. Post-CMP profilometer scans of the array structures

Table 5.16: Measured instantaneous blanket removal rates in step three

$\bar{r}_{cu3}$ (Å/s)	$\bar{r}_{ox3}$ (Å/s)	$\bar{r}_{b3}$ (Å/s)
20.0	9.0	4.0

on the patterned wafers show severe edge rounding of the dielectric. The problem is so severe that there seems to be voids or empty spaces between the copper in the trenches and the dielectric in the spaces. Figures 5.22 shows a profilometer scan for an array after a long step three polish,

that clearly illustrates the severity of the edge rounding problem. Edge rounding seems to be the signature of the 10K-1 slurry that is typically used in the third step of a three step process. Figure 5.23 shows the evolution of array dishing and recess for a particular array during polish step three.

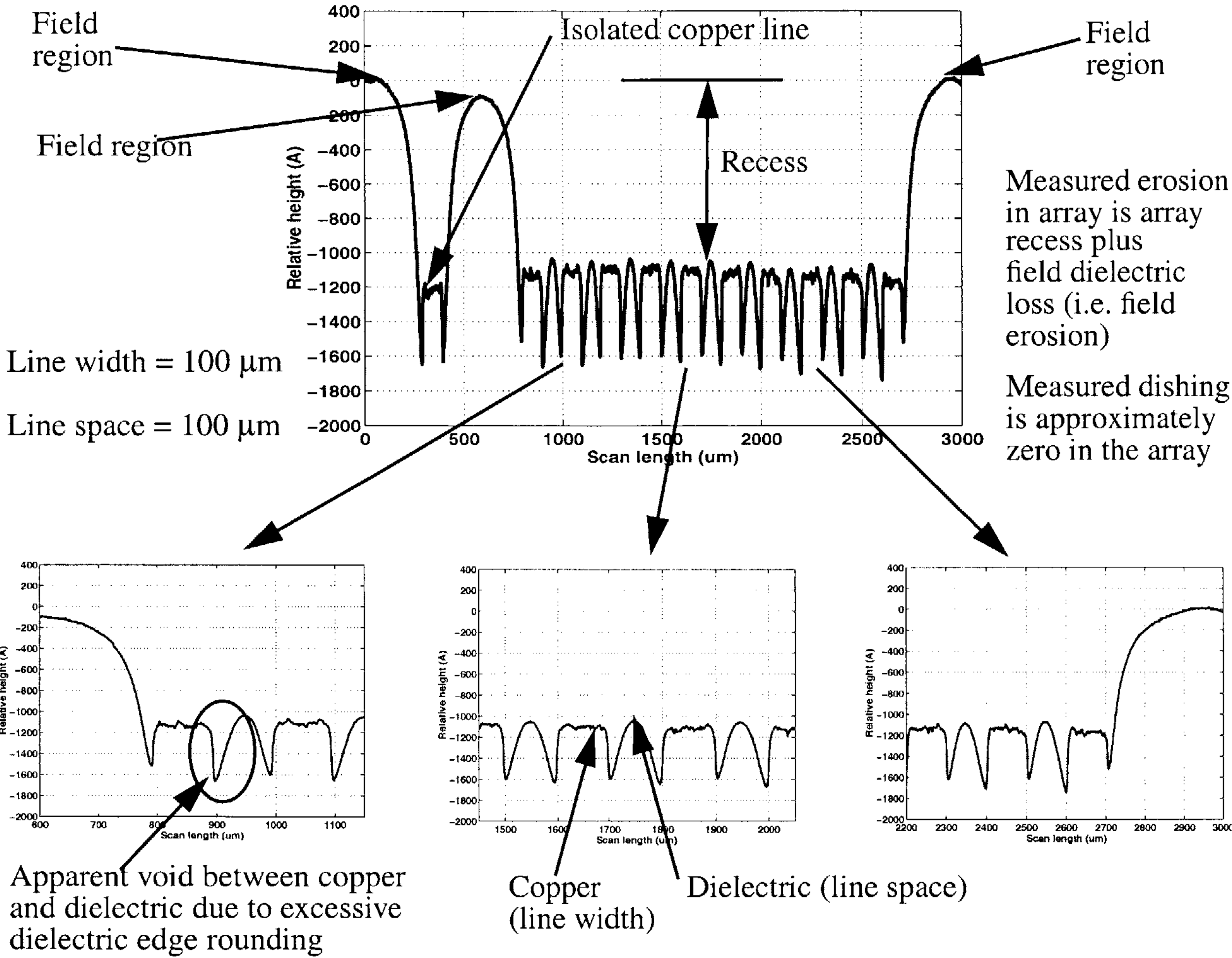
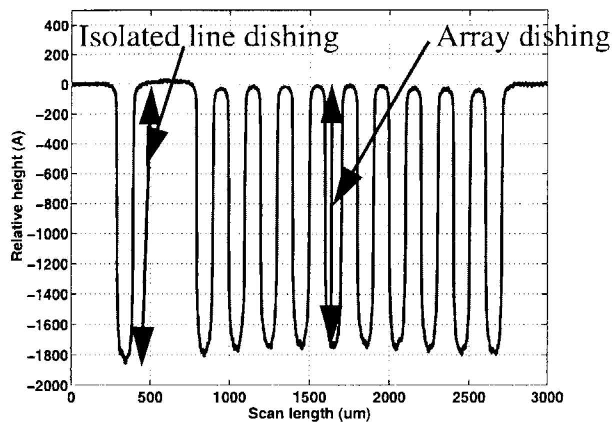
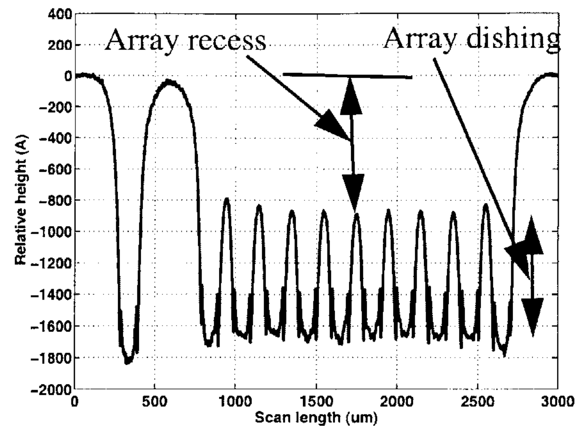


Figure 5.22: Profilometer scan of an array showing severe edge rounding in step three

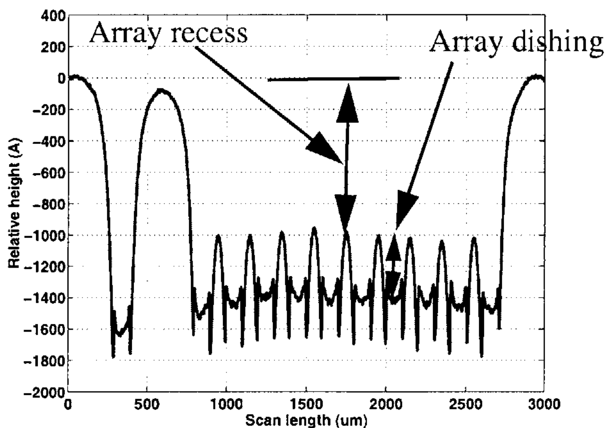
The severe edge rounding problem could lead to an inaccurate reading of the profilometer scans. When the dielectric in the large field regions are severely rounded, levelling the two field regions that surround an array becomes difficult. Hence correctly reading the recess value for any dielectric point on the array, relative to the levelled field point, becomes very challenging. In addition, the points where the oxide thickness loss in the field are measured may not match the



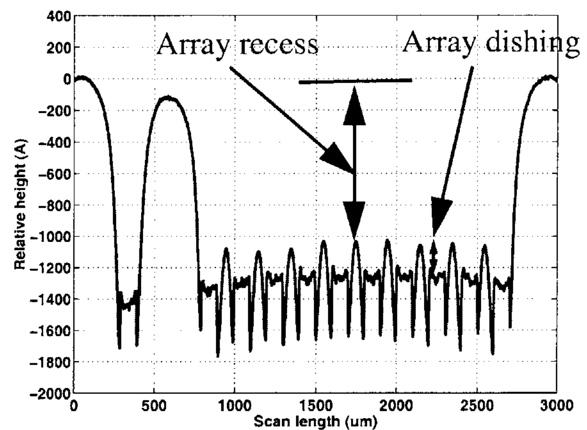
Polish time in step three = 0 s
(dishing and recess at end of norminal
step two polishing)



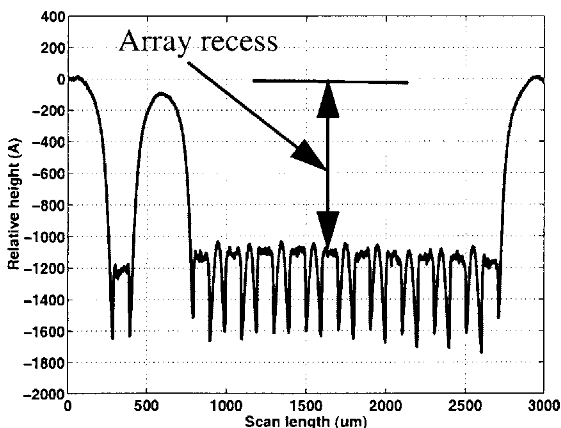
Polish time in step three = 20 s



Polish time in step three = 35 s



Polish time in step three = 50 s



Polish time in
step three = 65 s

Array dishing is
approximately zero

Figure 5.23: Evolution of dishing and recess during step three polish for a 100 μm line width and 100 μm line space array structure, with an isolated line

points at which the field regions are levelled. Because erosion is measured as the field thickness loss plus the recess at the dielectric position of interest (relative to the levelled field region), the measured erosion value could be incorrect. The effect is to increase the potential measurement inaccuracy in this step by 100 - 400 Å in erosion values for some structures.

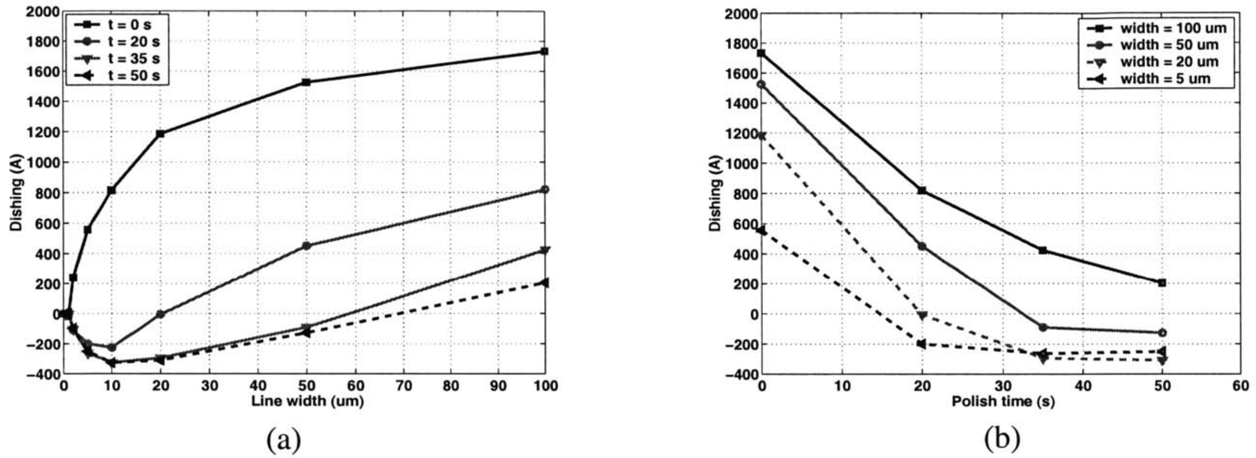


Figure 5.24: Measured dishing versus line width and polish time for several arrays: (a) *t* represents polish time (b) width represents line width

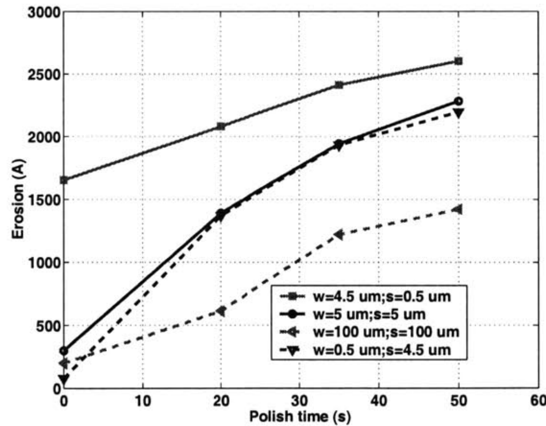


Figure 5.25: Measured erosion versus polish time in step three, for several arrays. The variable *w* represents line width and the variable *s* represents line space. An estimate of the layout copper pattern density is the line width divided by the sum of the line width and space

As stated in the formulation of the model equations in section 5.1, when the blanket dielectric rate is greater than the measured blanket copper rate, steady state dishing is negative.

Figure 5.24 show a plot of measured dishing versus polish time for four array structures, and a in these plots has equal line width and space. The measured dishing for each array decreases with polish time. Erosion, on the other hand increases with polish time. Figure 5.25 shows a plot of measured erosion versus polish time for two arrays.

It is worth mentioning that the copper in the trench does not experience any significant edge rounding, even though it ultimately becomes the up-area when the dishing becomes negative. From this observation, it is clear that the edge rounding effect should only be included in the equations for the dielectric removal rate in polish step three. If the edge rounding effect is excluded from the model equations, the effective blanket copper and dielectric removal rates need to be floated for the model to fit the data well, i.e., by ignoring the edge rounding effect, the extracted values for the effective blanket copper, dielectric, and barrier removal rates, are not necessarily equal to the measured blanket rates.

If edge rounding is included in the equations, then setting the effective blanket and dielectric rates to the measured instantaneous blanket rates yields a good fit of the model to the data. Note that when edge rounding is incorporated into the model, two additional modeling parameters (ψ_3: C_3, s_{c3}) are added to the parameters that need to be extracted. It is therefore practical to set the effective blanket copper and dielectric removal rates to the measured instantaneous blanket rates, to reduce the number of fitted parameters, and avoid over fitting the model to the data. The extracted model parameters for the step three process are summarized in table 5.17. The first row of the table corresponds to the case when the edge rounding effect is excluded from the model equations, while the second row corresponds to the case when it is included in the model equations. As seen in table 5.17, when the edge rounding effect is excluded from the model equations, the extracted effective blanket dielectric removal rate is almost twice

the measured rate. If these extracted model parameters (in the case when edge rounding is neglected) are used to predict the dishing and erosion for a different chip polished with the same three step process, the model will definitely over predict the erosion in step three, especially in large dielectric field areas. The plots comparing the model fits to the experimental data are shown in figures 5.26 and 5.27. Generally, the model fits the data well. The fits to the erosion data are better when the edge rounding effect is included in the model equations.

Table 5.17: Extracted model parameters in step three

r_{cu3} (Å/s)	r_{ox3} (Å/s)	r_{b3} (Å/s)	L_{33} (μm)	d_{p3} (Å)			ψ_3		RMS Error (Å)
				A_3 (Å)	α_3	β_3	C_3	s_{c3}	
13.7	45.2	9.0	3707	54.5	0.896	0.014	N/A	N/A	137.0
9.0	20.0	4.0	4500	31.0	0.625	0.014	3.41	57.3	126

5.3.4 Checking the Accuracy of the Extraction

The extraction of model parameters for the three polish steps uses all the array structures for which measurements are taken. As a result of this there is no opportunity to use the extracted model parameters in each polish step to predict dishing and erosion, or copper thickness, on array structures not used in the extraction process. Running a full simulation of all the polishing steps to predict dishing and erosion in steps two and three (for all the structures used in the extraction), is the only possible way of testing the accuracy of the model parameter extraction procedures for this three step polish experiment.

The simulation results for all the array sites marked in figure 5.12 are compared to experimental data in figure 5.28. The large extraction errors in step one affect the accuracy of the simulated dishing and erosion (especially erosion) in steps two and three. At the first four array sites, for

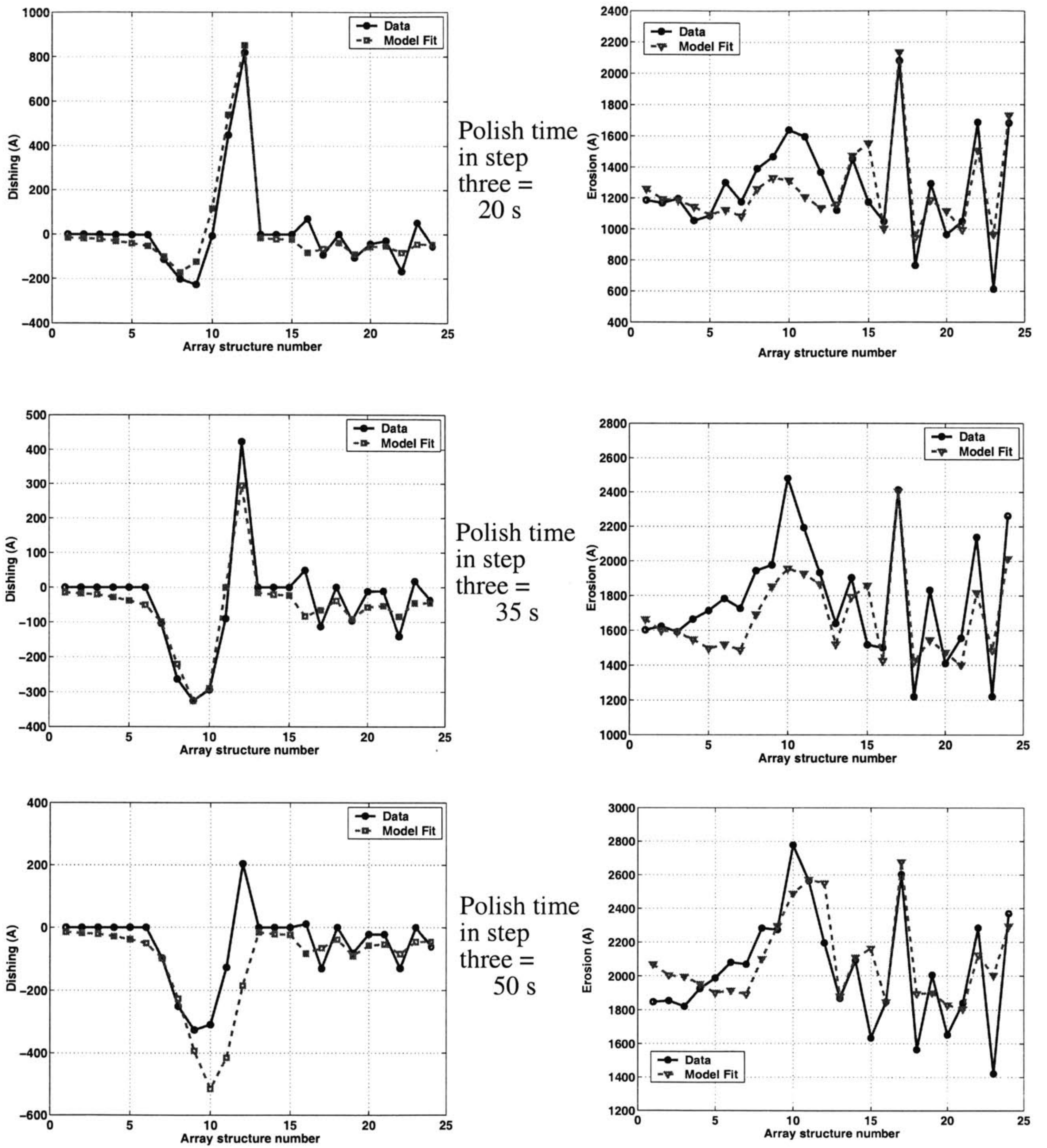
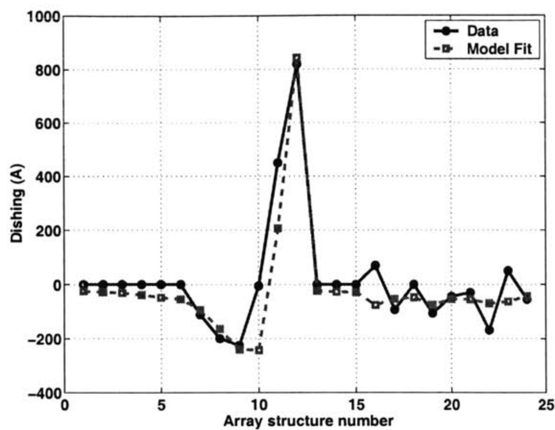
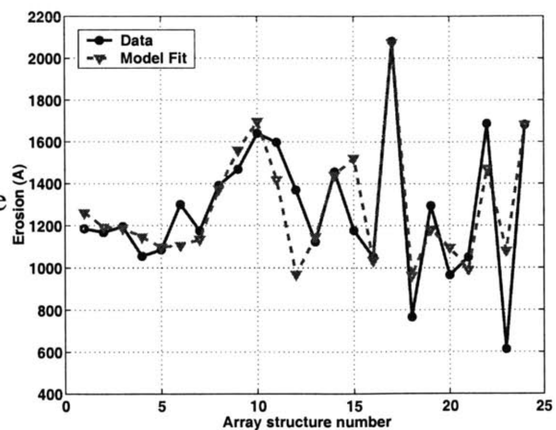
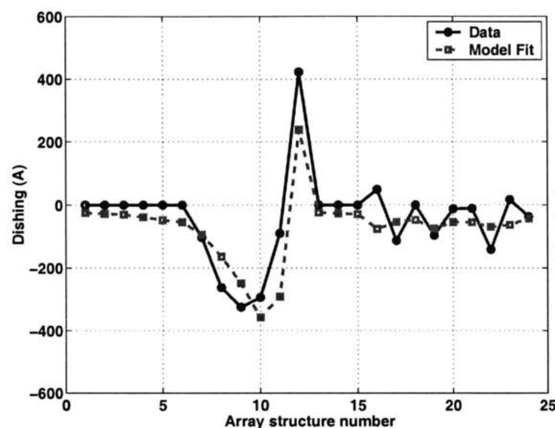


Figure 5.26: Model fit versus experimental data, in the case where the edge rounding effect is neglected

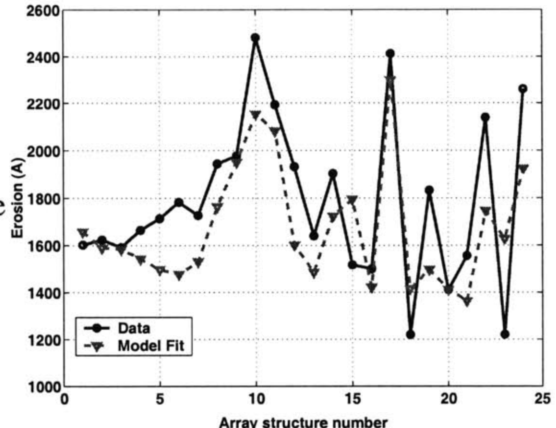


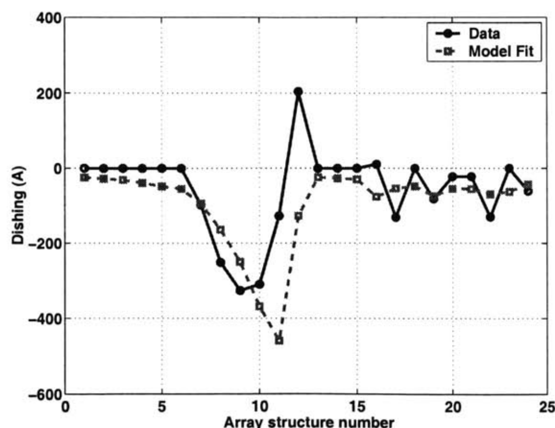
Polish time in step three = 20 s





Polish time in step three = 35 s





Polish time in step three = 50 s

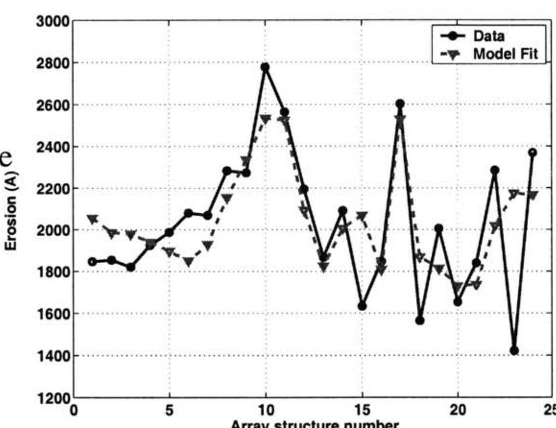


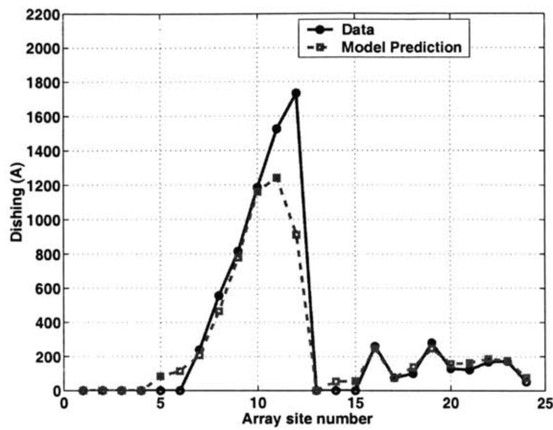
Figure 5.27: Model fits versus experimental data, in the case where the edge rounding effect is included in the model equations

instance, the bulk copper is not cleared even after step three polish, and the simulated dishing and erosion at these sites are thus zero. For array sites where there is a large positive recess in the electroplated topography, the density-step-height model clears the bulk copper very quickly, thereby leading to a high computed overpolish time. This results in high simulated erosion at these array sites. For array structures where the electroplating is conformal, and where the surrounding area does not have large long range height variation in the electroplated thickness, the simulation results agree with the measured data. Again, the simulation results presented here highlight the need to extend the density-step-height model to account for long range electroplating height variation. This is done in chapter 6.

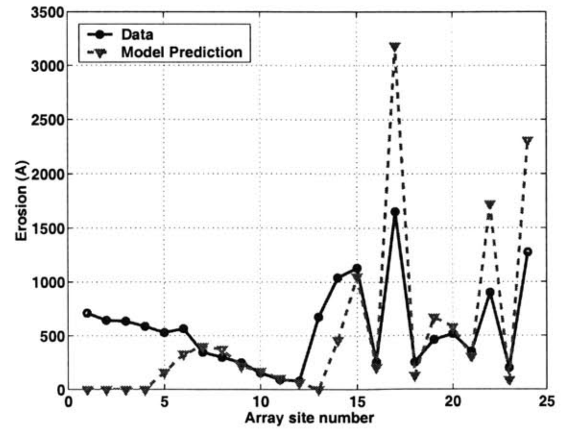
5.4 Summary

In this chapter, the density-step-height model is formulated for multi-step copper CMP processes, and a model calibration methodology is developed. A comprehensive three step copper CMP polish experiment is conducted to test the accuracy of the model. The edge rounding effect is found to be important for the model to fit the data (without over fitting) accurately during extraction of model parameters, particularly in steps two and three.

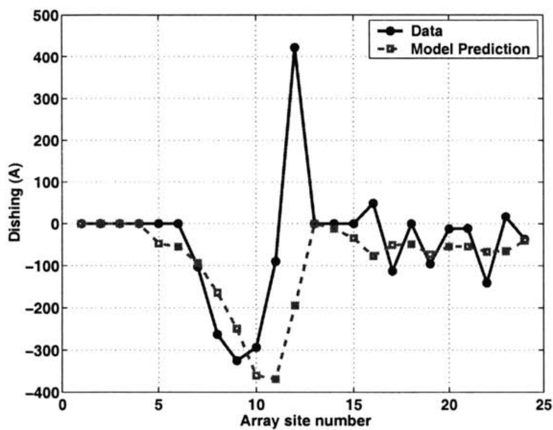
The model is anticipated to work accurately when the electroplating process is conformal. In this case, the long range height variation introduced by the electroplating process is either small, or ideally zero. The model presented in this chapter, fails to take into account large long range height variation introduced by the electroplating process, in computing the initial pressure on the up and down areas. In addition, it fails to re-distribute the pressure correctly, when the long range height variation changes during polishing. These limitations of the model are rectified in chapter 6.



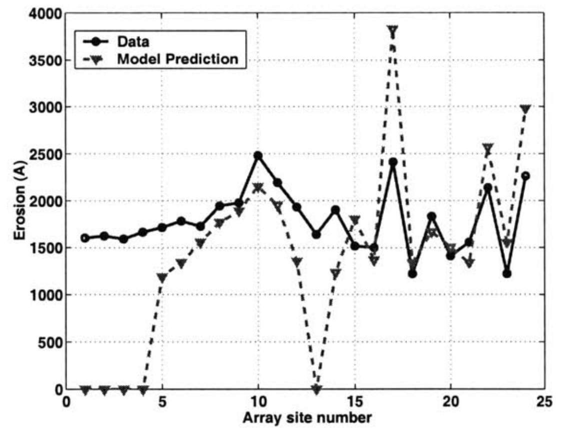
Norminal steps one and two polish



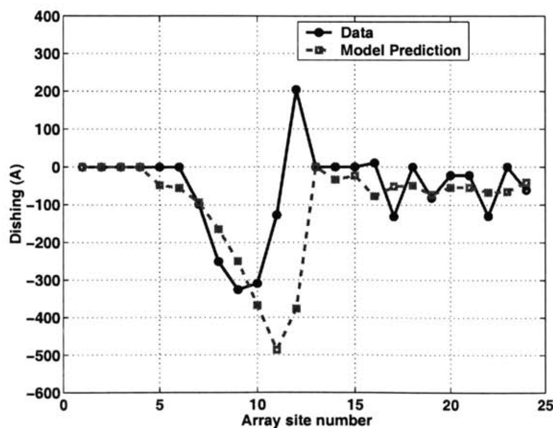
Norminal steps one and two polish



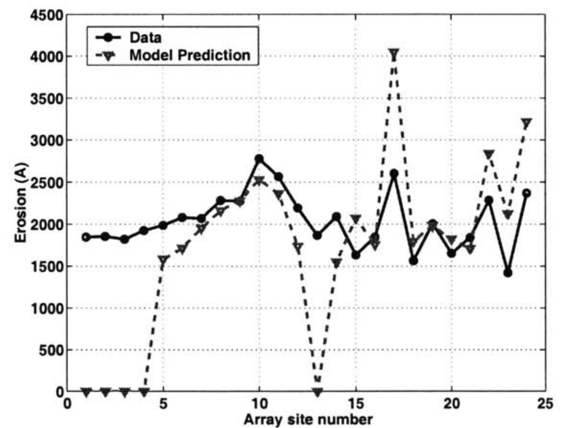
Norminal steps one and two, and 35 s step three polish



Norminal steps one and two, and 35 s step three polish



Norminal steps one and two, and 50 s step three polish



Norminal steps one and two, and 50 s step three polish

Figure 5.28: Complete simulation of three step process compared to experimental data

Chapter 6

Integrated Contact Mechanics and Density-Step-Height Model

The density-step-height model is capable of rapidly simulating thickness evolution on an entire chip, and it is effective at capturing local feature-scale pattern dependent effects. However, this model fails to take into account long range height variation (such as that introduced by electroplating) when apportioning the effective polish pressure on the up and down areas of an array. In addition, it does not correctly redistribute the polishing pressure when the long range height variation changes as the polishing progresses. With this limitation, the density-step-height model cannot accurately predict dishing and erosion performance when the electroplating process introduces large long range height variation, when significant overpolishing is done, and when multi-level metallization schemes are involved.

Contact mechanics based wear models (usually called contact wear models) have been used to model dielectric and copper CMP processes [26, 27, 28, 45]. These models account for the initial long range height variation caused by the copper electroplating process, and they also redistribute the pressure to take into account the changing long range height differences as polishing progresses. However, they can be computationally prohibitive or inaccurate when simulating an entire chip or a small section of a chip, depending on the discretization size used. In copper metallization, the feature sizes on the lower metal levels are very small. Hence, the discretization size for a full chip simulation must be very small, if the feature-scale polishing evolution is to be computed accurately. Such a discretization size will lead to long and impractical

simulation times. If the discretization size is made too large, on the other hand, the simulation time will be reasonable, but the prediction of feature-scale polishing evolution will be inaccurate.

The contact wear model and the density-step-height model are not individually suited for practical and accurate chip-scale simulations in copper CMP. However, a combination of the two will yield a model that is ideal for the task. Contact mechanics can readily account for long range height variation effects, while the density-step-height formulation can accurately account for local feature-scale pattern dependent material removal during the polishing process. In this chapter, an integrated contact mechanics and density-step-height model for copper CMP processes is formulated. In section 6.1, the framework of contact wear models is described briefly. This is followed by the formulation of the integrated model in the three intrinsic stages of a single step copper CMP process, in sections 6.2 - 6.4. A calibration methodology is then developed in section 6.5, and used to test the integrated model against experimental data in section 6.6. Finally, the chapter concludes with a summary in section 6.7.

6.1 Framework of Contact Wear CMP Models

Contact wear CMP models use a wear law that relates the material removal rate to the polishing pressure (via Preston's equation), and a classic contact mechanics pressure versus displacement relationship. According to this classic relationship, if the pad is treated as a massive elastic body, and the wafer a rigid body, then the pad displacement W and the contact pressure P are related as given in equation 6.1, where ν is the poisson's ratio and E the elasticity of the pad [26 - 28]. If the displacement is known, the contact pressure P can be computed and vice-versa. Once the pressure has been computed, it can then be substituted into the wear law to compute the material removal rate.

$$W(x,y) = \frac{1-\nu^2}{\pi E}\iint_A \frac{P(\xi,\eta)}{\sqrt{(x-\xi)^2+(y-\eta)^2}}d\xi d\eta \qquad \textit{(Equation 6.1)}$$

In practice, neither the pad displacement nor the contact pressure is known at all spatial positions of interest, initially. Yoshida proposes a boundary element methodology (BEM) that discretizes the wafer surface into small cells, where the contact pressures and pad displacements can be assumed constant [26]. He then uses the known pad displacements in certain cells, and the known contact pressures in other cells to fully solve for the pad displacements and the contact pressures at every spatial position of interest [26].

In formulating the integrated contact mechanics and density-step-height model, the classic pressure-displacement relationship given in equation 6.1 is combined with the density-step-height model presented in chapter 3. Yoshida's methodology is exploited to solve equation 6.1. However, instead of using matrix manipulations to fully solve the problem, as Yoshida does, an FFT-based approach is proposed. For the sake of simplicity, the model is formulated for Prestonian single step copper CMP processes; the model can be extended to non-Prestonian copper CMP processes by using alternative non-Prestonian removal rate versus polish pressure relationships. In addition, since multi-step copper CMP processes are combinations of single step copper CMP processes, the model can also be applied to such multi-step processes. The experiment used to test the accuracy of the model is the three step copper CMP process experiment used in chapter 5.

6.2 Formulation of Integrated Model in Intrinsic Stage One: Bulk Copper Polishing Stage

Consider the electroplated topography of several arrays of lines, illustrated in figure 6.1. The topography shows height differences among the different array up-areas. These height

differences (hence forth called long range height variation) influence the effective polishing pressure on the different up-areas (as well as on the down-areas). The density-step-height model formulated in chapter 3 does not take this into account. To remedy the situation, an envelop function is introduced that captures the long range height differences over the entire chip or region of interest. To obtain the envelop function, the chip or region of interest is first discretized into cells small enough to capture the long range thickness differences, and large enough to enable efficient computation. Typical discretization sizes studied here have ranged from 200 μm by 200 μm to 400 μm by 400 μm for a 20 mm by 20 mm chip (a discretization size of 240 μm by 240 μm is used to obtain the results presented in this thesis). After discretization, each cell is represented by the average, maximum or some other appropriate statistic of the local up-area heights within the cell. Figure 6.2 shows the envelop function for the electroplated topography shown in figure 6.1.

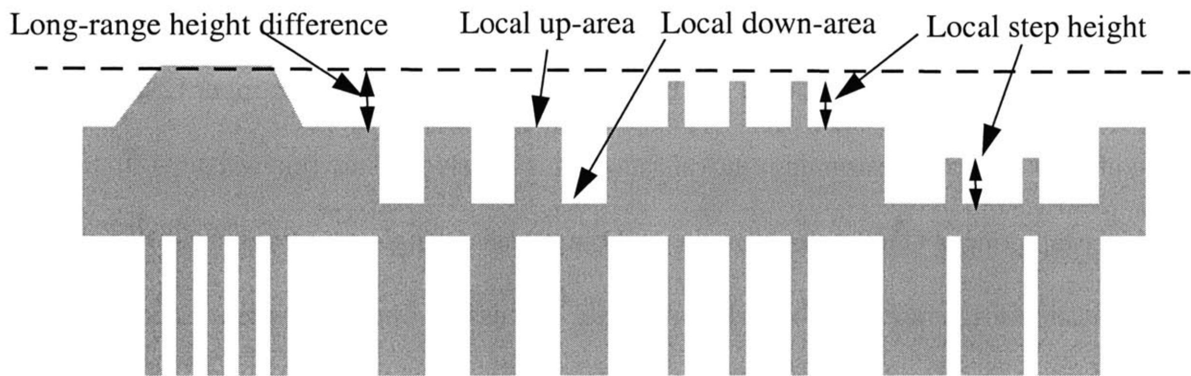


Figure 6.1: Bottom-up fill electroplated profile for several arrays of lines

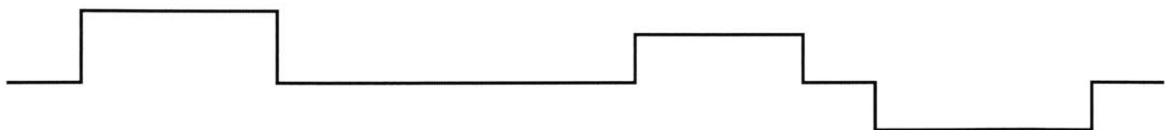


Figure 6.2: Envelop function for the electroplated profile shown in figure 6.1

The pressures on the different cells making the envelop function are computed by using the pressure versus displacement relationship expressed in equation 6.1. Let P_e denote this envelop pressure, with a value that depends on the location of the cell. After taking into account the long range height variation through the envelop function, the computed envelop pressures are then used in the density step-height model, to compute the up-area and down-area removal rates. The process of computing the envelop pressures for the different cells and using them to compute the removal rates is done iteratively as illustrated in figure 6.3. The iterations are needed so that the envelop and the envelop pressures reflect the evolution of the long range height variation.

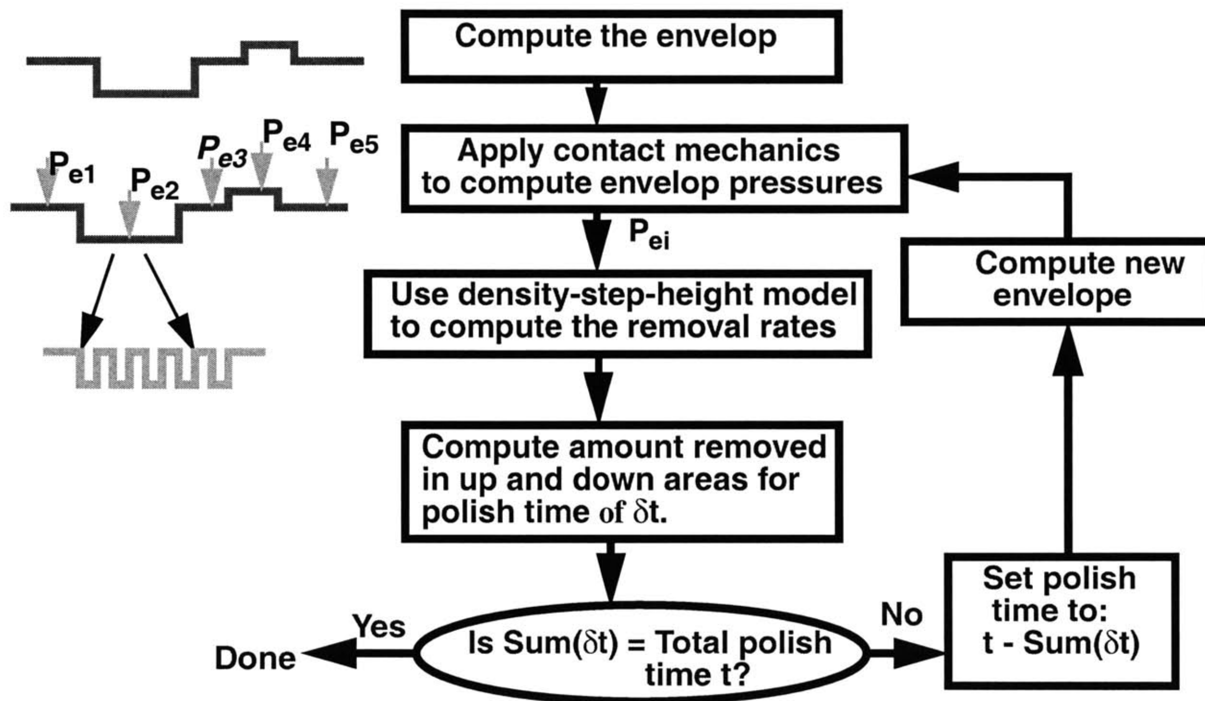


Figure 6.3: Iterative implementation of integrated model for intrinsic stage one

The removal rate equations for each iteration time interval in intrinsic stage one can be expressed as in equations 6.2 - 6.3, where RR_{up} is the removal rate of the copper up-area, RR_{down} is the removal rate of the copper down-area, r_{cu} is the effective blanket copper removal rate for an

applied pressure of P_1 (pressure setting on the CMP tool), ρ_{cu} is the effective electroplated copper pattern density after accounting for the long range thickness variation through the envelop function, and H_{ex} is the critical step height as defined in chapter 3. The up-area and down-area removal rates linearly depend on the pressure ratio term P_e/P_1 because of the assumed Prestonian nature of the process. This pressure ratio term could be thought of as a correction factor for the long range height variation.

$$RR_{up} = \begin{cases} \dfrac{r_{cu}}{\rho_{cu}}\left(\dfrac{P_e}{P_1}\right) & H \geq H_{ex} \\ r_{cu}\left(\dfrac{P_e}{P_1}\right)\left\{1 + \left(\dfrac{1-\rho_{cu}}{\rho_{cu}}\right)\dfrac{H}{H_{ex}}\right\} & 0 \leq H < H_{ex} \end{cases} \qquad \textit{(Equation 6.2)}$$

$$RR_{down} = \begin{cases} 0 & H \geq H_{ex} \\ r_{cu}\left(\dfrac{P_e}{P_1}\right)\left(1 - \dfrac{H}{H_{ex}}\right) & 0 \leq H < H_{ex} \end{cases} \qquad \textit{(Equation 6.3)}$$

6.2.1 Calculation of Envelope Pressure P_e

In the iterative implementation of the integrated model, illustrated in figure 6.3, the envelope pressure in each cell is computed in every iteration. In this section, a methodology for computing the envelope pressure for a single iteration is proposed.

Suppose there is a wafer whose surface is similar to the envelope profile shown in figure 6.2, and suppose the wafer is pressed against a polishing pad with an applied pressure of P_1, as shown in figure 6.4. If the wafer surface is flat (i.e. the envelope is constant, meaning there is no long range height variation), then the top pad surface will also be flat and in contact with the wafer

surface everywhere. This means that the pad displacement Wp is constant everywhere, and the pad pressure P_b and the wafer (envelope) pressure P_e will then be equal to the applied pressure P_I in every cell making up the envelope. If the wafer surface is not flat, when a pressure of P_I is applied the polishing pad bends and displaces to conform to the wafer surface. Hence, there is a perturbation to the otherwise constant pad displacement W_b. Let the line AD represent a reference level in the wafer-pad geometry. The perturbation pad displacement w_b is defined as the reference level minus the height of the top of the pad surface (the top of the pad surface is the surface that touches the wafer when there is contact between the two) as shown in figure 6.4. In addition, let there exist a wafer perturbation displacement w_e defined as the reference level minus the top surface of the wafer, as illustrated in figure 6.4. Both the perturbation pad displacement and the perturbation wafer displacement vary along their surfaces, i.e., they vary from cell to cell.

The long range non-planarity of the wafer surface leads to a perturbation in the wafer and pad pressures, i.e., these pad and wafer pressures deviate from the applied pressure P_I. The perturbation pad pressure is denoted by p_b and it is related to the perturbation pad displacement as given in equation 6.4. The parameter k_c is a model parameter referred to as the contact factor. Theoretically, k_c is related to the pad elasticity and the poisson ratio as in equation 6.1. It therefore has inverse pressure units (e.g. 1/pascal or 1/psi).

It is recognized that equation 6.4 is a convolution, and can be re-written as in equation 6.5, where f is a kernel function given in equation 6.6. Fast fourier transforms (FFTs) can be used to solve equation 6.5. However, the kernel function f has a pole at the origin, so that at (x,y) = (0,0) this function is infinite. It therefore needs to be modified slightly without significantly changing the physics of the problem. A modified kernel function f_I is proposed in equation 6.7,

where the new term ε is small but greater than zero. In this thesis, the new term ε is set equal to 0.1 in discretized units. With the new kernel function, equation 6.6 is approximated as in equation 6.8. Taking the FFT of equation 6.8 leads to equation 6.9. If the perturbation pad displacement w_b is known, then the perturbation pad pressure p_b can be computed as in equation 6.10, where "Real" means the real part of a complex number, "IFFT" means inverse fast fourier transform, and "FFT" means fast fourier transform.

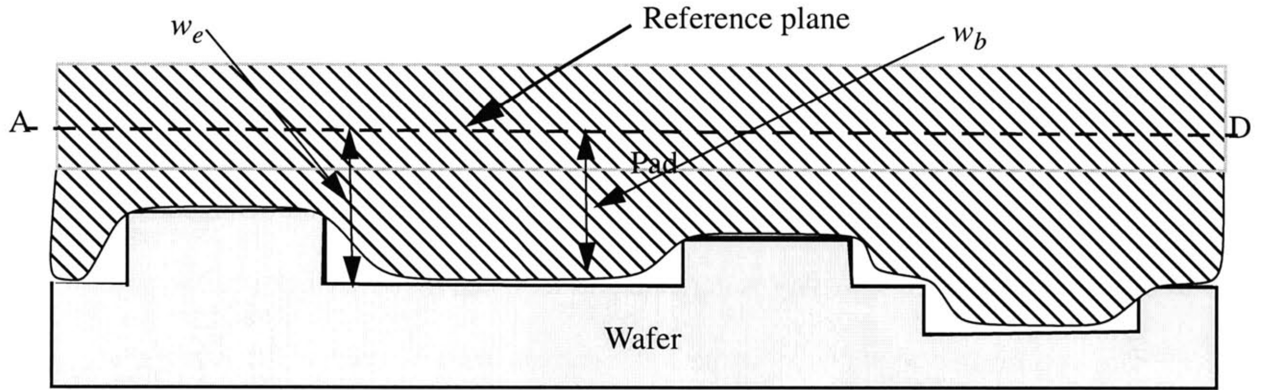


Figure 6.4: Wafer-pad set up for envelope pressure computation

$$w_b(x,y) = k_c \iint_A \frac{p_b(\xi,\eta)}{\sqrt{(x-\xi)^2 + (y-\eta)^2}} d\xi d\eta \qquad \textit{(Equation 6.4)}$$

$$w_b(x,y) = k_c p_b(x,y) \otimes f(x,y) \qquad \textit{(Equation 6.5)}$$

$$f(x,y) = \frac{1}{\sqrt{x^2 + y^2}} \qquad \textit{(Equation 6.6)}$$

$$f_1(x,y) = \frac{1}{\sqrt{x^2 + y^2 + \varepsilon}} \qquad \textit{(Equation 6.7)}$$

$$w_b(x,y) = k_c p_b(x,y) \otimes f_1(x,y)$$

(Equation 6.8)

$$FFT[w_b(x,y)] = k_c(FFT[p_b(x,y)]) \bullet (FFT[f_1(x,y)])$$

(Equation 6.9)

$$p_b(x,y) = \frac{1}{k_c}\left(Real\left\{IFFT\left[\frac{FFT[w_b(x,y)]}{FFT[f_1(x,y)]}\right]\right\}\right)$$

(Equation 6.10)

To implement the FFT-based approach to solving for the perturbation pad pressure, the perturbation pad displacement w_b is initially assumed equal to the perturbation wafer displacement w_e, which is known. This is equivalent to assuming that the pad is in contact with the wafer everywhere, initially. Then, the perturbation pad pressure is computed using equation 6.10. After computing the perturbation pad pressure in every cell making up the envelope, the constraint expressed in equation 6.11 is checked. If the constraint is violated in any cell, it means that the pad is not in contact with the wafer in that cell. Consequently, the perturbation pad displacement associated with that cell is decreased by a small amount, and equation 6.10 is solved for the new perturbation pad pressure in every cell, including the cells where the constraint was originally satisfied. This procedure is continued iteratively until the constraint is satisfied in all cells. At that point, the resulting perturbation pad pressure and the corresponding perturbation pad displacement are said to constitute a consistent solution. The procedure just described is illustrated in figure 6.5.

Once a consistent perturbation pad pressure is found, the envelope pressure P_e is computed as given in equation 6.12 and the pad pressure is given in equation 6.13. If the perturbation pad displacement is equal to the perturbation wafer displacement, then the pad

surface and the wafer surface are in contact, and the wafer or envelope pressure is equal to the reference pressure minus the perturbation pad pressure. The pad pressure is equal to the wafer pressure. If, on the other hand, the perturbation pad displacement in a cell is less than the wafer displacement in the same cell, the pad surface and the wafer surface are not in contact in that cell. Consequently, the wafer or envelope pressure in that cell is zero, while the pad pressure is the reference pressure minus the perturbation pad pressure.

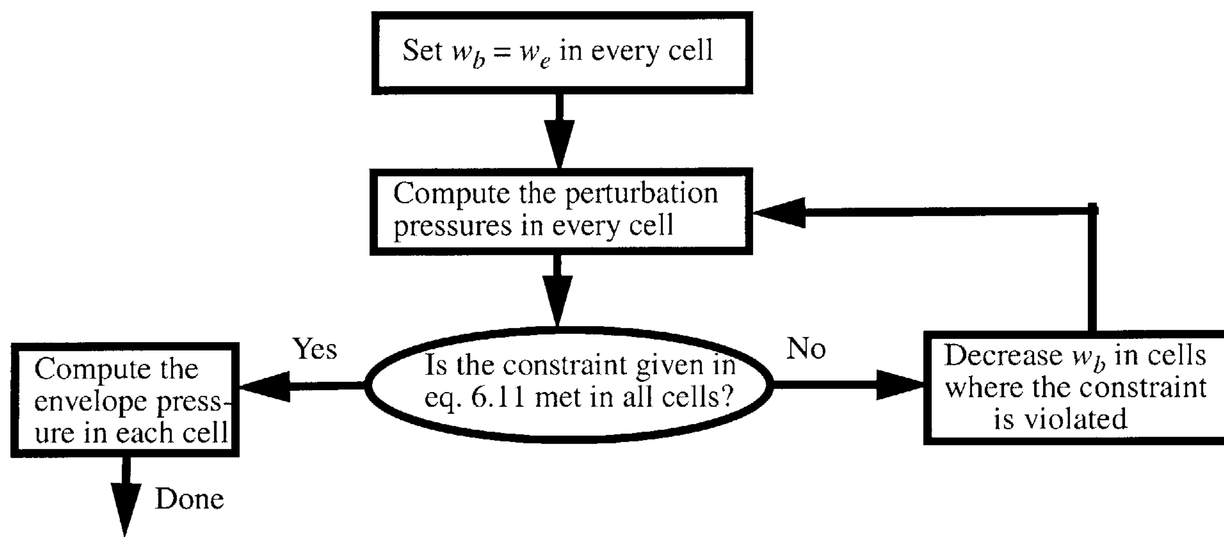


Figure 6.5: Iterative methodology for computing the envelop pressures

$$P_1 - p_b \geq 0$$

(Equation 6.11)

$$P_e = \begin{cases} P_1 - p_b & w_e = w_b \\ 0 & w_e > w_b \end{cases}$$

(Equation 6.12)

(Equation 6.13)

$$P_b = P_1 - p_b$$

6.3 Formulation of Integrated Model in Intrinsic Stage Three: Overpolish Stage

The model formulation in intrinsic stage three is similar to that in intrinsic stage one. Here, the dual material surface (copper in the trenches and dielectric in the spaces) is first discretized into cells. In each cell (a cell might contain both materials), the average, maximum, minimum or some other appropriate statistic of the up-area heights is computed to represent the envelope in that cell. When the envelope is computed, a similar iterative implementation of the integrated model described in section 6.2 is applied. This implementation is illustrated in figure 6.6.

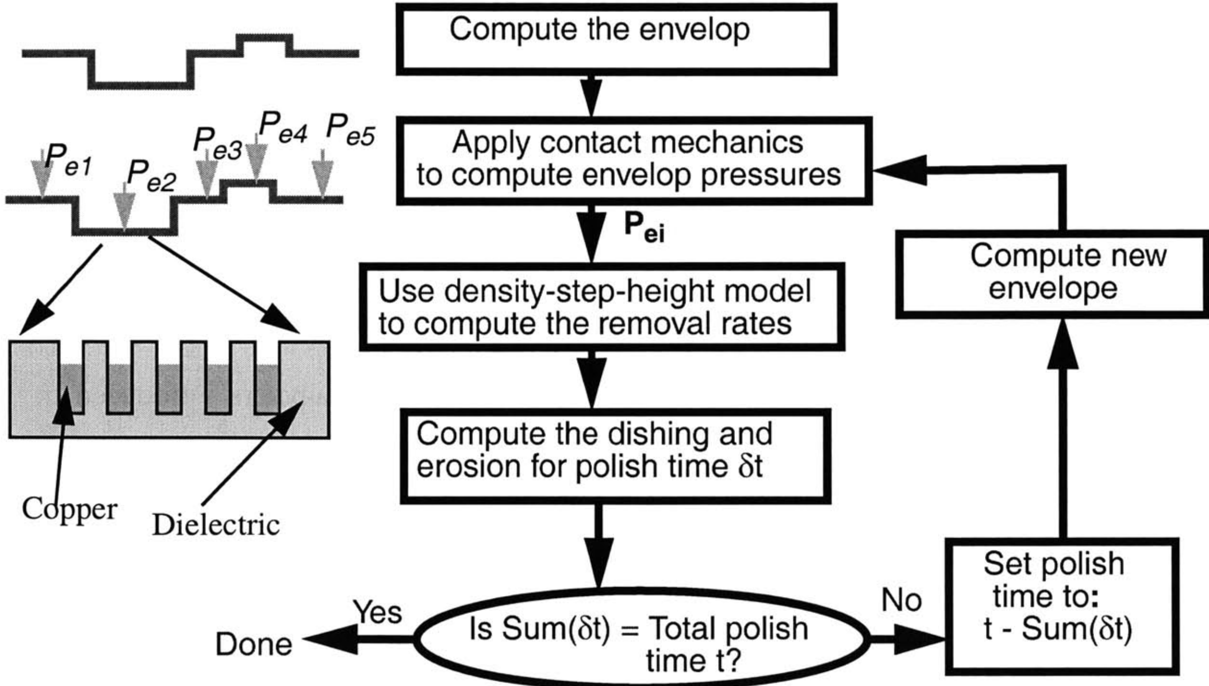


Figure 6.6: Iterative implementation of integrated model in intrinsic stage three

The removal rate equations for intrinsic stage three, originally derived in chapter 3, now change due to the envelop pressure being different from the applied pressure, as given in equations 6.14 - 6.15. In these equations, D_{cu} is the copper dishing, d_{max} the maximum dishing

parameter, RR_{ox} the dielectric removal rate, RR_{cu} the copper removal rate, r_{cu} the effective blanket copper removal rate, r_{ox} the effective blanket dielectric removal rate, and Φ_{cu} is the effective layout copper pattern density. The new equations are for each iteration in figure 6.6. The pressure ratio term P_e/P_1 takes care of the limitation of the density-step-height model in the excessive overpolishing regime, which was discussed in chapter 3. The formulation of the integrated model in intrinsic stage two (the barrier clearing stage) is similar to that in intrinsic stage three.

$$RR_{cu} = r_{cu}\left(\frac{P_e}{P_1}\right)\left(1 - \frac{D_{cu}}{d_{max}}\right) \qquad \textit{(Equation 6.14)}$$

$$RR_{ox} = r_{ox}\left(\frac{P_e}{P_1}\right)\left\{1 + \left(\frac{1-\Phi_{cu}}{\Phi_{cu}}\right)\frac{D_{cu}}{d_{max}}\right\} \qquad \textit{(Equation 6.15)}$$

6.4 Model Parameters and Calibration Methodology

The integrated contact mechanics and density-step-height model parameters for a single step copper CMP process are the contact factor k_c, and all the parameters introduced in the formulation of the density-step-height model for single step copper CMP processes, in chapter 3. These parameters are summarized in table 4.1. Theoretically, the contact factor k_c is related to the stiffness of the pad. The stiffer the pad, the smaller the contact factor, and the more difficult it is for the pad to conform to any long range height variation on the wafer, i.e., the pad is then less likely to contact lower height areas, for a given applied pressure. On the other hand, the softer the pad, the larger the contact factor, and the easier it is for the pad to conform to the long range height variation on the wafer. The contact factor therefore indicates the extent to which long range height variation can be eliminated.

The contact factor should not be confused with the planarization length. Both parameters are indicators of the planarization capability of a CMP process. The longer the planarization length and the smaller the contact factor, the higher the planarization capability of the process. One way to distinguish between the two is to think of pad bending in three dimensions. The planarization length captures the length scale of the pad deformation in the x-y plane, while the contact factor captures the extent of the deformation in the z-plane.

The contact factor may be influenced by the process settings (e.g. speed) and the consumable set (slurry). It does not depend on topography (topography meaning long range height variation). However, it does determine the evolution of topography during CMP. The contact factor is a model parameter and it is not computed from first principles. Instead, it is extracted from experimental data. In order for the value of k_c to be extracted from single level copper CMP experiments, the electroplating process must introduce large long range height variation, or excessive overpolish experiments must be performed. It is assumed in this thesis, that for a single step copper CMP process, the contact factor is the same in all intrinsic stages.

6.4.1 Model Calibration Methodology

The experiments needed for calibrating the integrated model for single step copper CMP processes are similar to those proposed for calibrating the density-step-height model for single step copper CMP processes. However, the extraction methodology for the integrated model is different from that proposed for the density-step-height model. The integrated model requires the computation of an envelope function which captures the long range height variation. Computing the envelope function requires knowledge of the thicknesses or relative heights across the entire die or across the large region of interest. For instance, to compute the envelope function of the electroplated die surface, the electroplated copper thicknesses all across the die must be known.

The electroplated copper thicknesses across the entire die can only be obtained through simulations.

Table 6.1: Integrated model parameters for a single step copper CMP process

Intrinsic stage one		Intrinsic stage two		Intrinsic stage three	
	Description		Description		Description
r_{cu}	Effective blanket copper removal rate	r_{cu}	Effective blanket copper removal rate	r_{cu}	Effective blanket copper removal rate
k_c	Contact factor	r_b	Effective blanket barrier removal rate	r_{ox}	Effective blanket dielectric removal rate
L_1	Planarization length	k_c	Contact factor	k_c	Contact factor
H_{ex}	Critical step height	L_3	Planarization length	L_3	Planarization length
		d_{max}	Maximum dishing	d_{max}	Maximum dishing
		ψ	Edge rounding factor	ψ	Edge rounding factor

A simulator that predicts the electroplated copper thicknesses across an entire chip has been developed by Park [36]. This simulator is based on an empirical pattern dependent electroplating model [36]. Using the measured electroplated copper thicknesses at specific points on the die (for a wafer patterned with a specially designed test mask), the electroplating model is calibrated. The calibrated model is then used to simulate the electroplated copper thicknesses across the entire die [33]. The simulator predicts the copper thicknesses across the die to within 500 - 800 Å accuracy. The errors in the simulation affects the computed envelope and consequently, the computed envelope pressures.

The model parameter extraction principle for the integrated model is the minimization of the RMS error between the measured data and model, subject to several constraints. Figures 6.7 -

6.8 illustrate the procedures for extracting the integrated model parameters in intrinsic stages one and three of a single step process. The modeling parameters related to intrinsic stage two are obtained from the extracted modeling parameters in intrinsic stage three, as described in chapter 3.

6.5 Model Fits versus Experimental Data

In chapter 5, an extensive three step copper CMP experiment was reported to evaluate the accuracy of the density-step-height model, for multi-step copper CMP processes. The density-step-height model did not fit the experimental data for the first polish step satisfactorily. This is because of the density-step-height model's failure to account for the influence of long range height variation (introduced by the electroplating) on polishing pressure. The integrated model has been formulated to remedy this limitation of the density-step-height model. This model is therefore tested against the same experimental data obtained from the three step copper CMP process used in chapter 5.

The integrated contact mechanics and density-step-height model has been formulated for single step copper CMP processes in section 6.2. Applying this model to multi-step copper CMP processes requires treating multi-step processes as combinations of single step processes, each comprised of three intrinsic stages. Once again, it is important to note that not all intrinsic stages are relevant for the different polish steps. Hence, the model parameters related to irrelevant intrinsic stages are ignored.

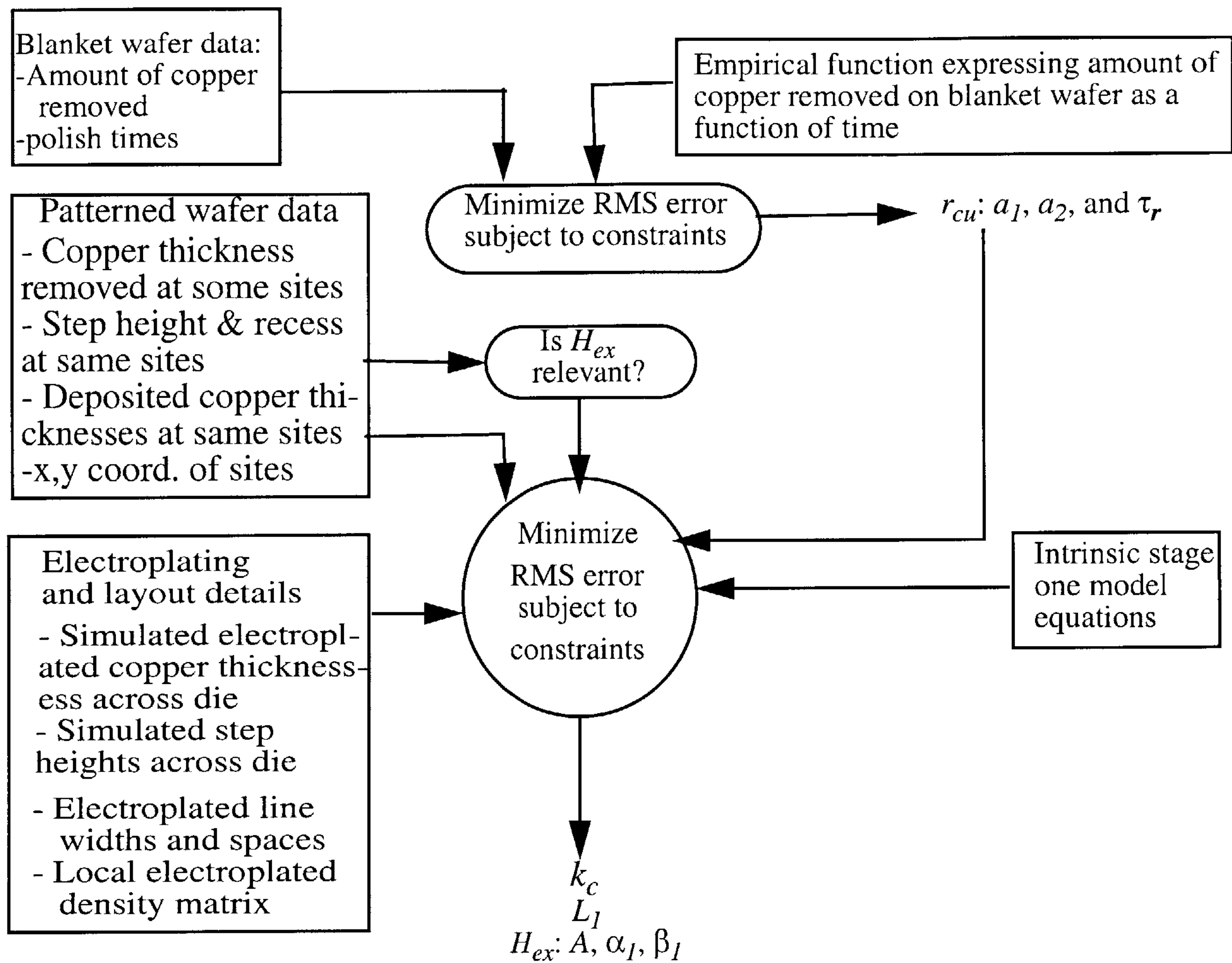


Figure 6.7: Integrated model parameter extraction procedure in intrinsic stage one of single step copper CMP process

6.5.1 Extraction of Model Parameters for Step One Process

Only intrinsic stage one is relevant for step one as discussed in chapter 5. Thus, the model parameters that need to be extracted are the effective blanket copper removal rate r_{cu1}, the planarization length L_{11}, the contact factor k_{c1}, and the critical step height H_{ex11}. As discussed in chapter 5, the critical step height can be neglected for this experiment. Post-CMP step height data for this experiment indicates that the critical step height is negligible (for the structures on the test mask used in the model parameter) extraction. The relevant extracted model parameters for step

one are summarized in the first row of table 6.2. For the sake of comparison, the extracted model parameters for the density-step-height model are summarized in the second row of the same table.

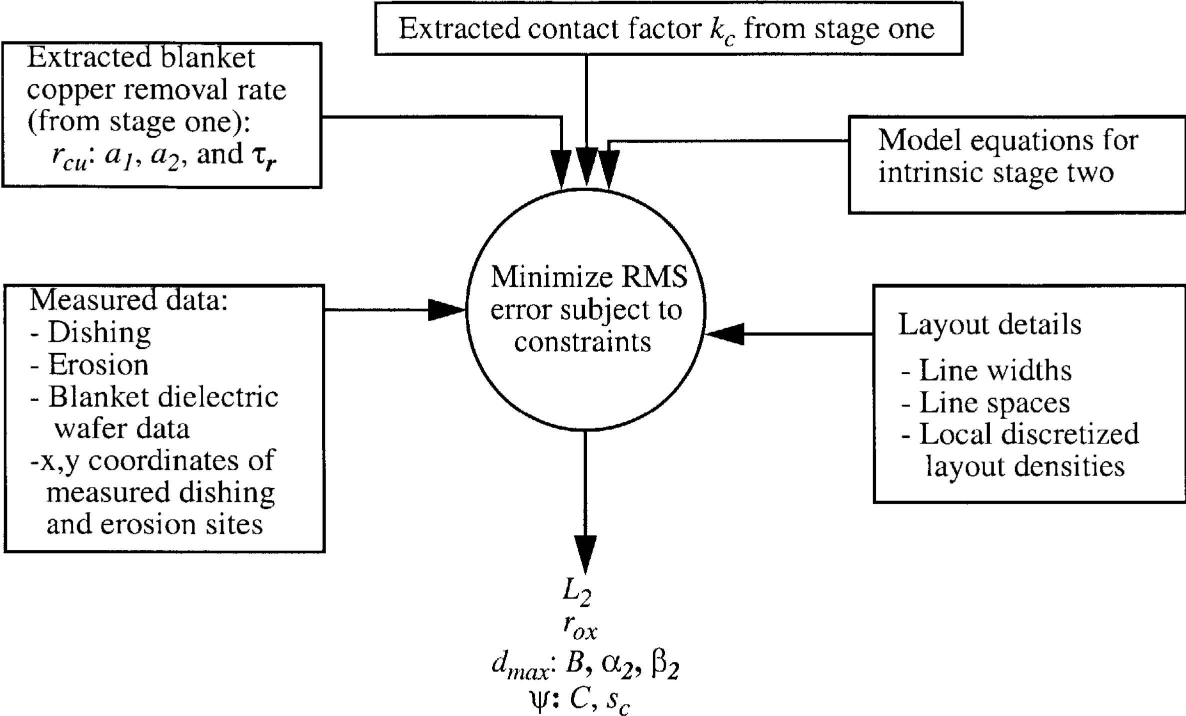


Figure 6.8: Integrated model parameter extraction procedure in intrinsic stage three of a single step copper CMP process

Table 6.2: Extracted model parameters in step one of three step copper CMP process

r_{cu1} (Å/s)			L_{11} (μm)	k_{c1} (1/kPa)	H_{ex11} (Å)	RMS Error (Å)
a_1 (Å/s)	a_2 (Å)	τ_r (s)				
249.5	3986	16.4	2758	9.95	negligible	569
249.5	3986	16.4	4893	N/A	negligible	817

The initial simulated electroplated copper thickness profile used to compute the initial envelope function and the initial envelope pressures during the model parameter extraction is

illustrated in figure 6.9. The simulated thicknesses at certain points on the die are compared to measured electroplated copper thicknesses in figure 6.10. The points on the die used for this comparison are illustrated in figure 6.11. The initial envelope function computed from the simulated electroplated copper thicknesses is illustrated in figure 6.12. In addition, the initial envelope pressures are also shown in figure 6.12.

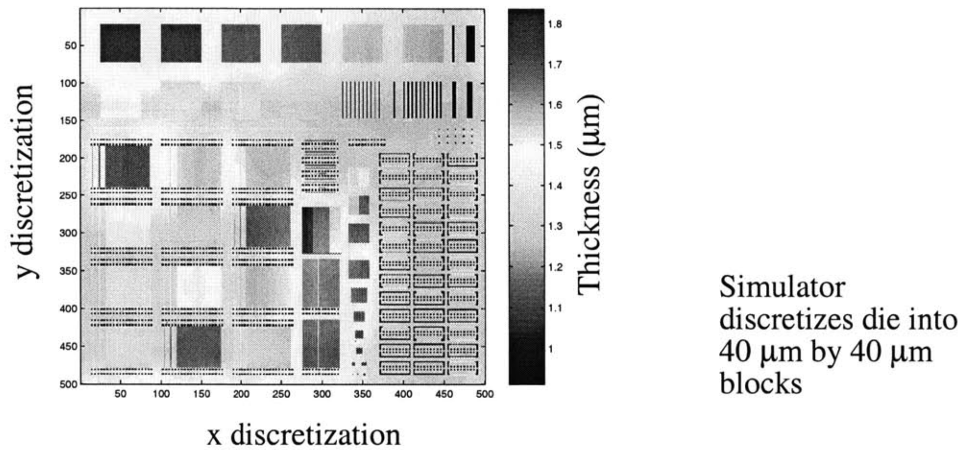


Figure 6.9: Simulated electroplated copper thicknesses across die

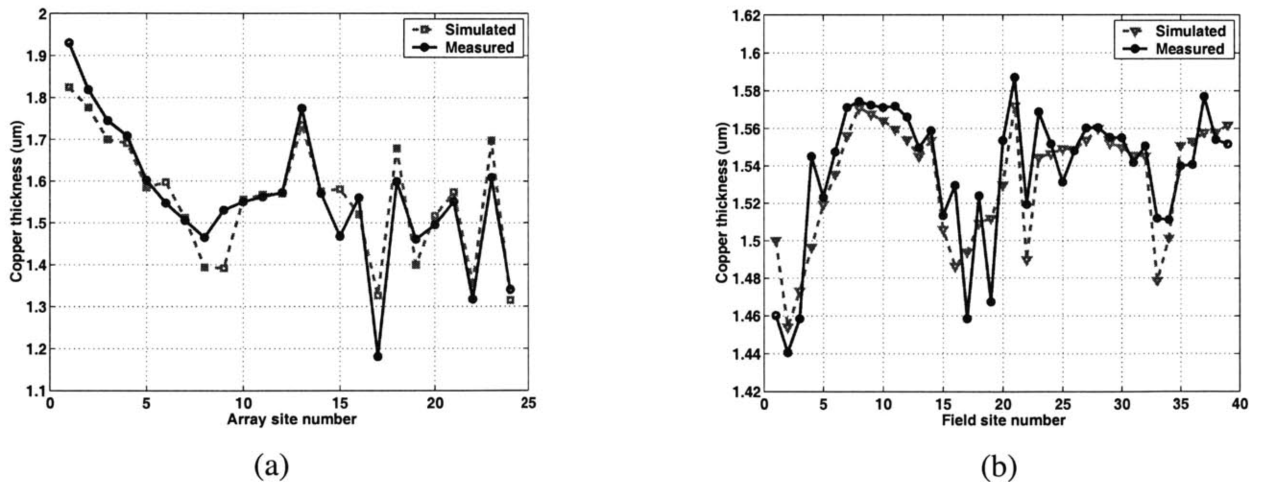
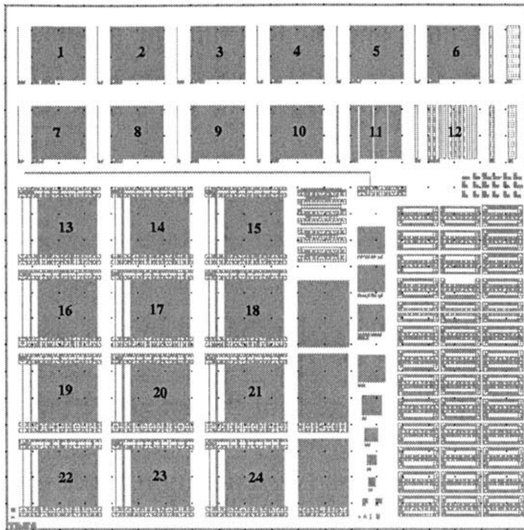
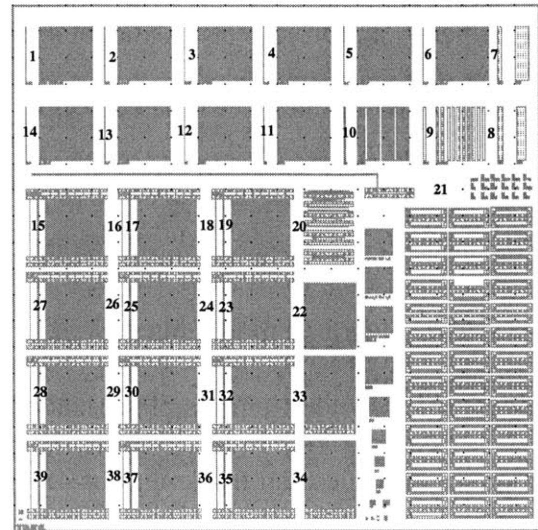


Figure 6.10: Simulated versus measured electroplated copper thickness: (a) Array (b) Field

The model fits versus experimental data for the extraction of model parameters in step one are shown in figure 6.13. For the sake of comparison, the model fits for the density-step-height

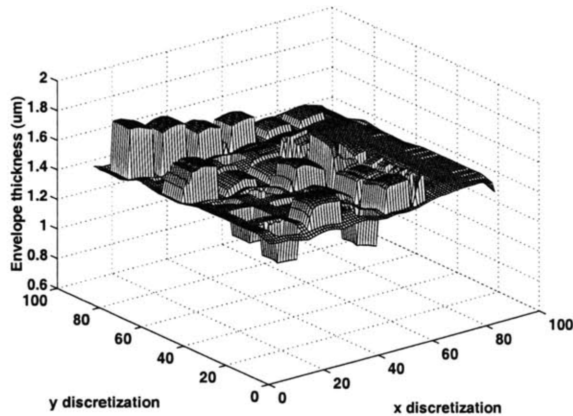


Array site numbers

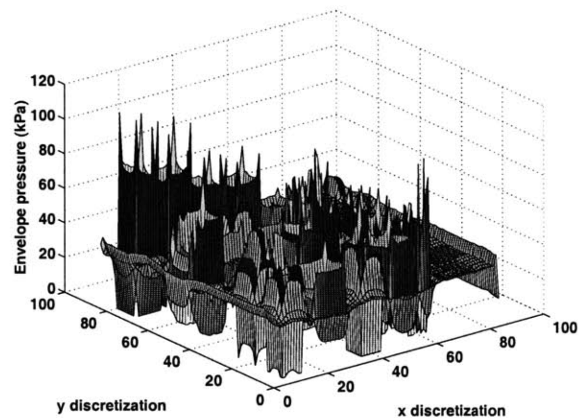


Field site numbers

Figure 6.11: Array and field sites used in extraction of model parameters



Initial envelope function for discretized die (each cell is 240 μm by 240 μm)



Initial envelope pressure for discretized die (each cell is 240 μm by 240 μm)

Figure 6.12: Initial envelope function and the corresponding initial envelope pressure (the die is discretized into cells, each of size 240 μm by 240 μm)

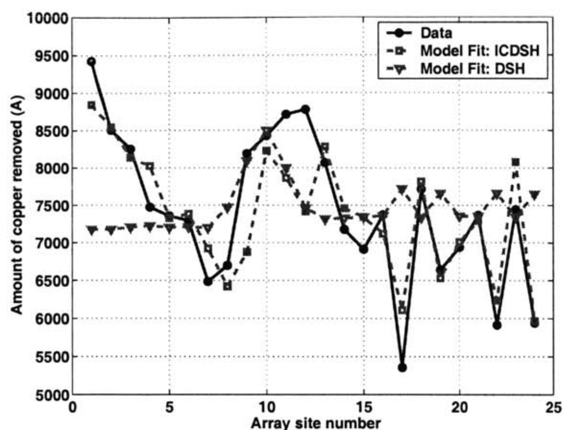
model of chapter 5 are shown on the same graph. The integrated model fits the data with an RMS error of 569 Å (RMS error for density-step-height model is 817 Å). This error is acceptable given that the copper thickness measurements on the patterned wafers are only accurate to within 300 -

500 Å (copper thicknesses in array regions are estimated from copper thickness measurements in nearby fields, and from recess data obtained from surface scans), and the fact that the model used to simulate the initial electroplated copper surface for use in the estimation of the envelope and the envelope pressures, has RMS errors on the order of 500 Å. More importantly, the spread in the fitting errors at the different sites is small.

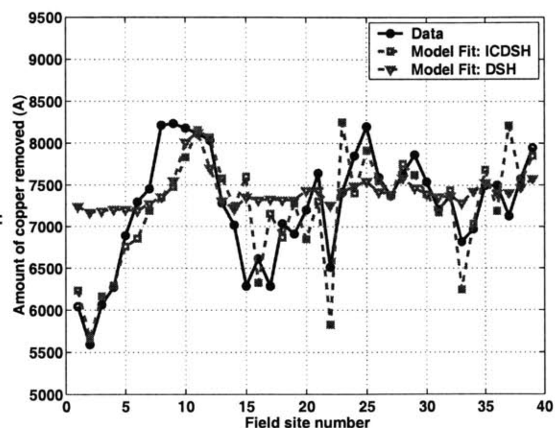
The integrated model fits the data much better than the density-step-height model, as seen in figure 6.13. In addition, the planarization length of 2758 μm extracted for the integrated model is more reasonable than the length of 4893 μm extracted for the density-step-height model. The latter length is unexpectedly large given the high down force process used in step one.

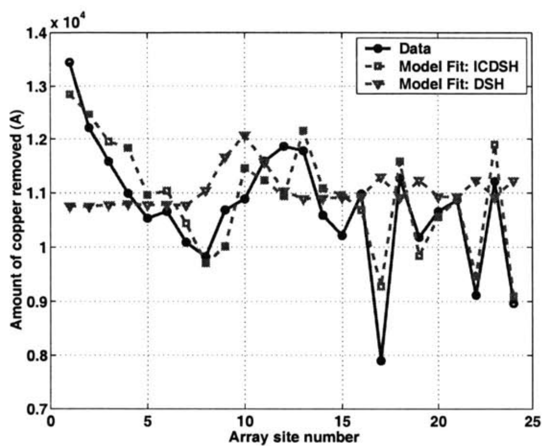
6.5.2 Extraction of Model Parameters for Step Two Process

The extracted model parameters in step two are given in table 6.3. The edge rounding effect is included in the equations to better fit the model to the data, and to get the extracted effective dielectric removal rate closer to the measured rate. The parameters have the same values as those extracted for the density-step-height model with the edge rounding effect included, in chapter 5. The extracted contact factor is unrealistically high, suggesting that there is not enough long range height variation for the correct value of the contact factor to be extracted. Whenever the contact factor does not have a significant impact on the evolution of the topography, it is impossible to extract its correct value from the data. The model fits versus the data are shown in figure 6.14.

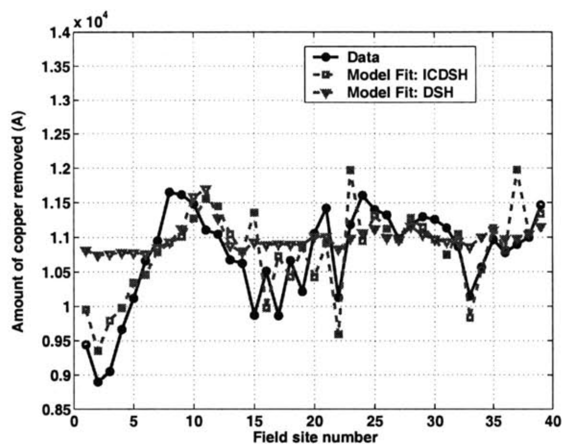


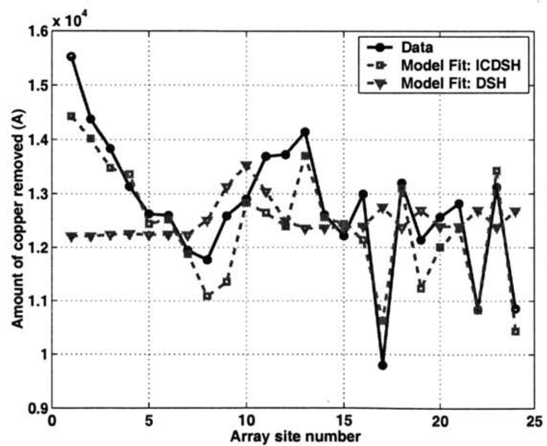
Polish time in step one = 43 s



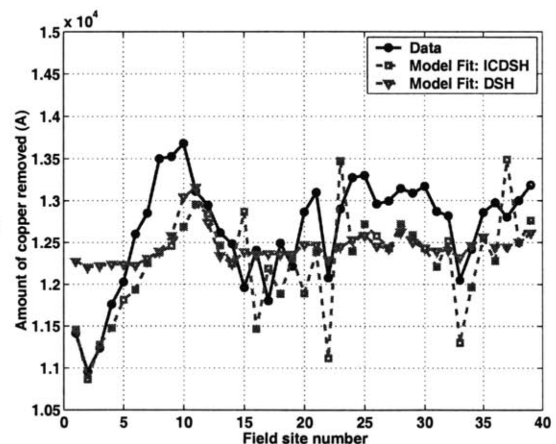


Polish time in step one = 58 s





Polish time in step one = 64 s



Array sites

Field sites

Figure 6.13: Model fits versus experimental data for model parameter extraction in step one - ICDSH: Integrated contact mechanics and density-step-height model DSH: Density-step-height model

6.5.3 Extraction of Model Parameters in Step Three

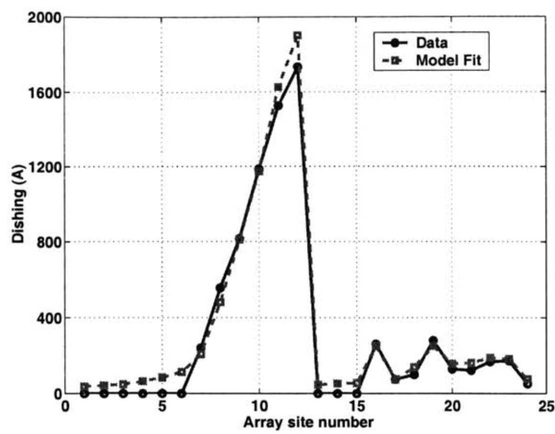
The extracted model parameters in step three are summarized in table 6.4. The edge rounding effect is included in the model equations, and the effective blanket copper and dielectric removal rates are set equal to the measured instantaneous rates. The extracted model parameters are equal to those extracted for the density-step-height model in chapter 5. The contact factor in step three does not impact the evolution of the topography significantly because the long range height variation is small, and hence the extracted value of the contact factor is suspect. The model fits versus the measured data are shown in figure 6.15. The model agrees with the trend in the data, and fits the data to within measurement errors.

Table 6.3: Extracted model parameters in step two for three step copper CMP process

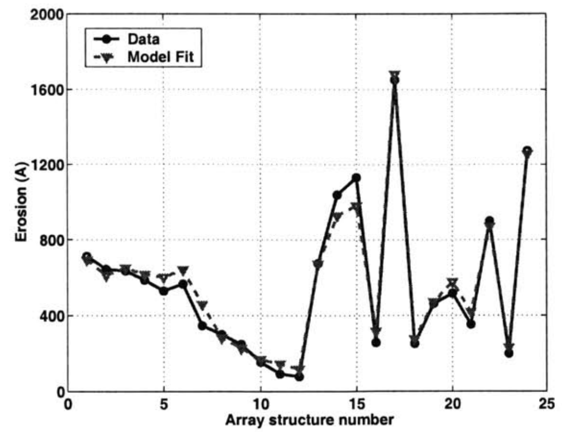
r_{cu2} (Å/s)	r_{ox2} (Å/s)	r_{b2} (Å/s)	L_{23} (μm)	k_{c2} (1/kPa)	d_{max2} (Å)			ψ_2		RMS Error (Å)
					B_2 (Å)	α_2	β_2	C_2	s_{c2}	
44	2.36	7.58	2456	2.3e3	173.6	0.427	0.331	4.03	4.19	73

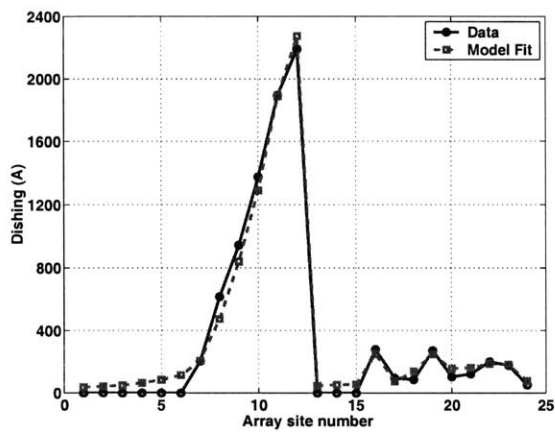
Table 6.4: Extracted model parameters in step three for three step copper CMP process

r_{cu3} (Å/s)	r_{ox3} (Å/s)	r_{b3} (Å/s)	L_{33} (μm)	k_{c3} (1/kPa)	d_{p3} (Å)			ψ_3		RMS Error (Å)
					A_3 (Å)	α_3	β_3	C_3	s_{c3}	
9.0	20.0	4.0	4500	2.5e3	31.0	0.625	0.014	3.41	57.3	126

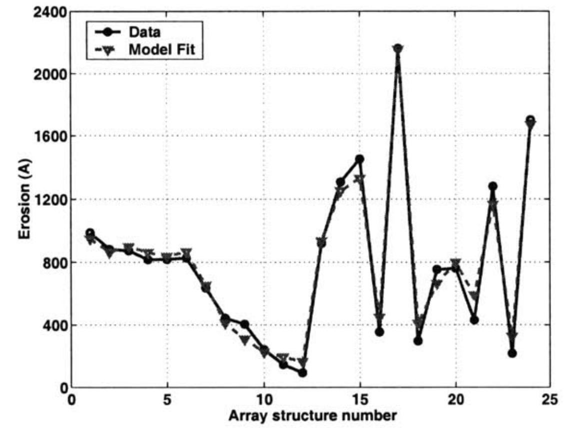


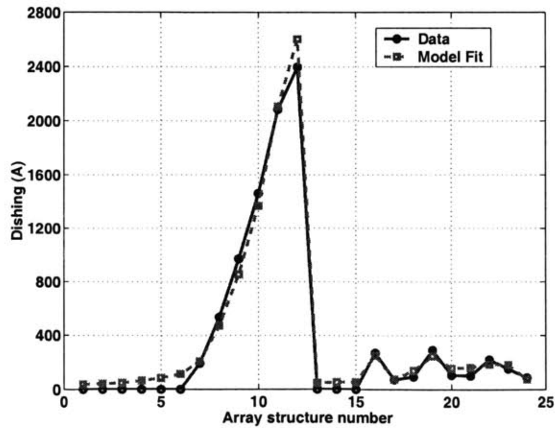
Polish time in step two = 94 s





Polish time in step two = 110 s





Polish time in step two = 124 s

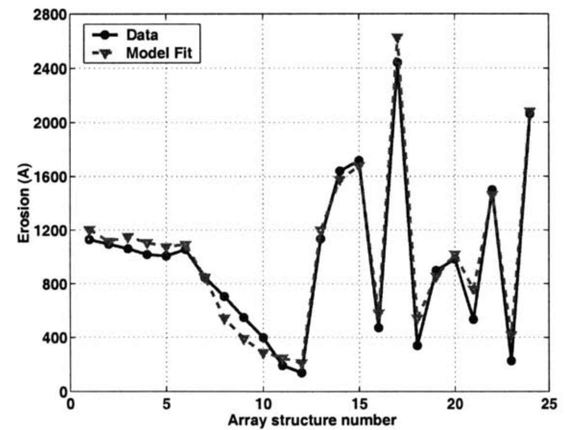


Figure 6.14: Model fits versus experimental data, for model parameter extraction in step two

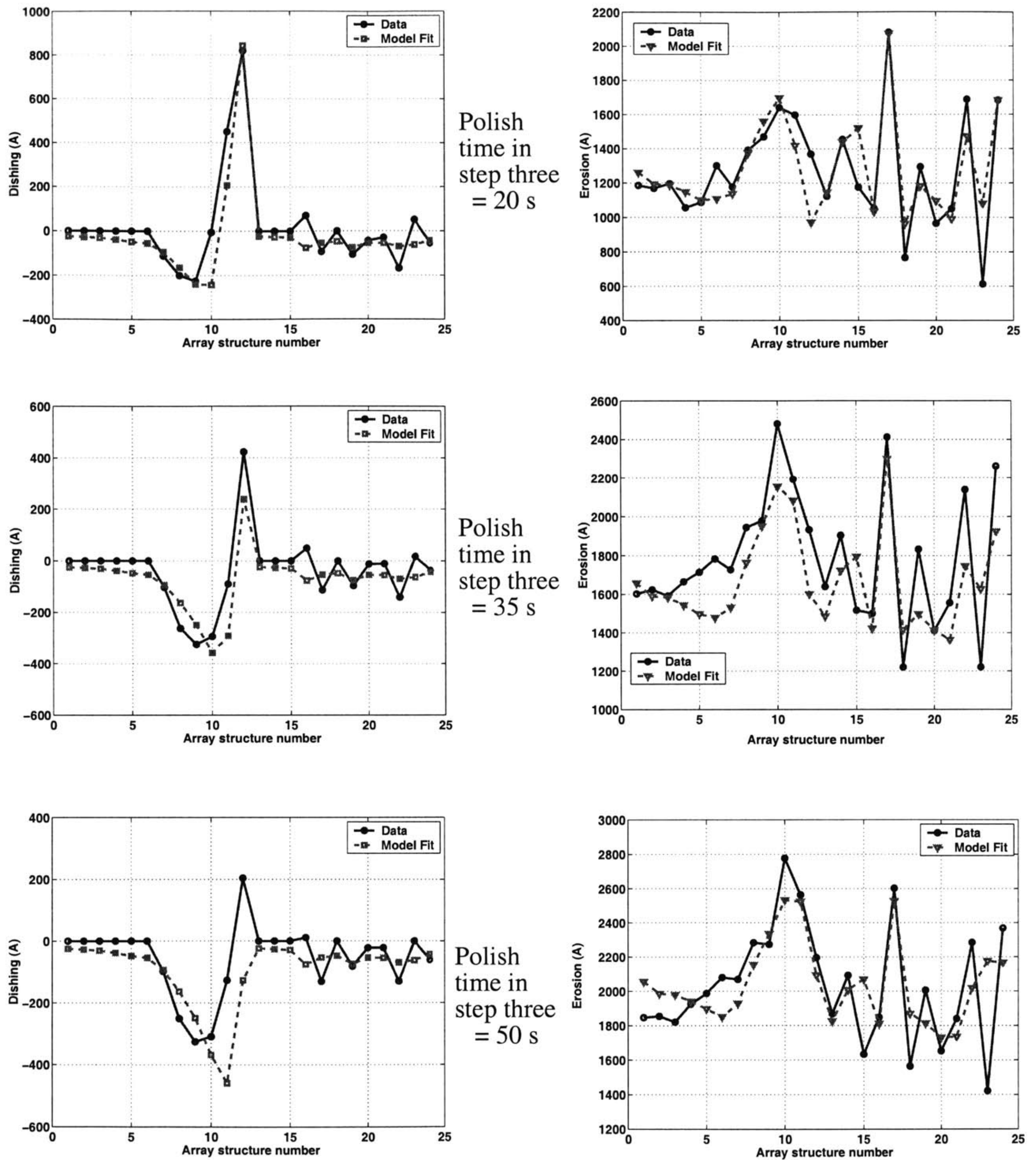


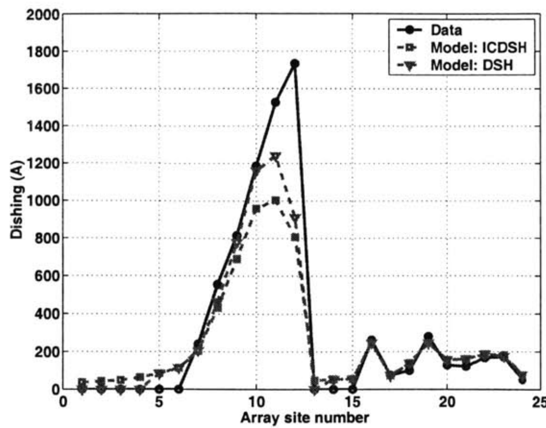
Figure 6.15: Model fits versus experimental data for model parameter extraction in step three

6.5.4 Checking the Accuracy of the Extraction

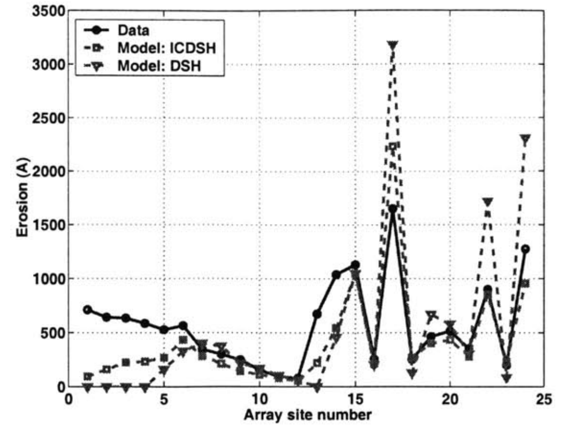
In chapter 5, the accuracy of the extraction of the density-step-height model parameters for the three step copper CMP process is tested by running a full simulation of all the polish steps, and comparing the simulated results to the measured dishing and erosion. This testing procedure is repeated in this chapter for the integrated contact mechanics and density-step-height model. The simulation results are compared to the measured data in figure 6.16. For the sake of comparison, the simulation results obtained in chapter 5 for the density-step-height model are shown in the same figure.

It is clear from figure 6.16 that the integrated model fits the measured erosion much better than the density-step-height model. This is not surprising because the integrated model computes the bulk copper clearing times and hence the overpolish time much more accurately than the density-step-height model. Dielectric erosion is strongly dependent on overpolish time. If the overpolish time is underestimated, the dielectric erosion is underestimated and vice-versa.

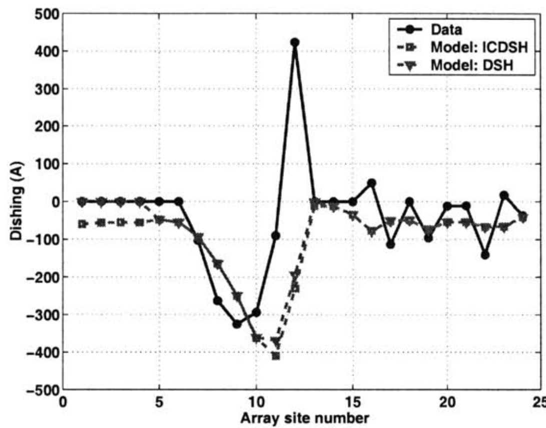
There is little difference between the two models with regards to the simulated dishing values. This should not be surprising because dishing tends to reach steady state rapidly. Therefore, even though the density-step-height model does not accurately simulate the overpolish times, it is able to compute the correct steady state dishing values for most of the array sites (both models extracted the same values for the maximum dishing of all the arrays). This does not mean that the density-step-height model is able to accurately predict dishing, particularly for short overpolish time.



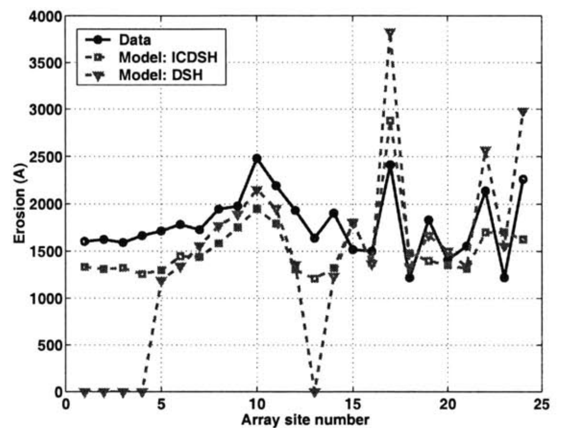
Norminal steps one and two polish



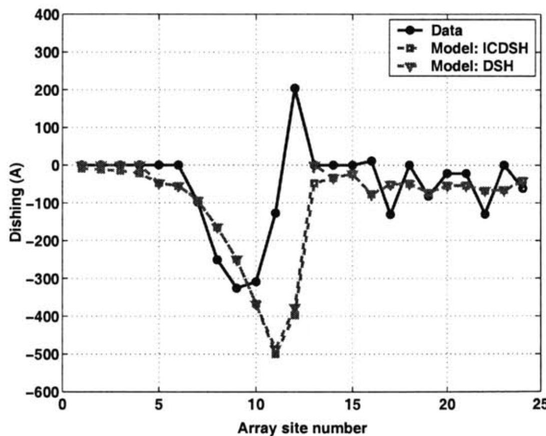
Norminal steps one and two polish



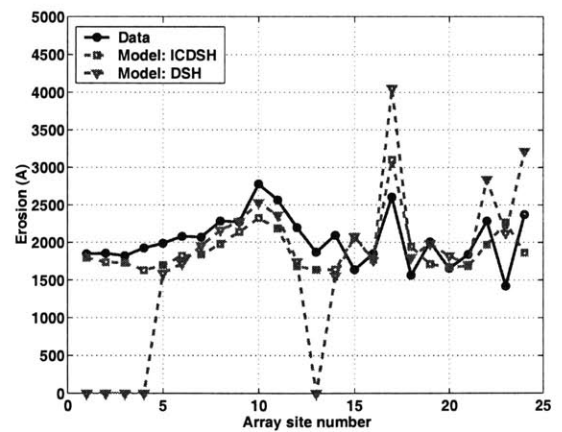
Norminal steps one and two polish, plus 35 s step three polish



Norminal steps one and two polish, plus 35 s step three polish



Norminal steps one and two polish, plus 50 s step three polish



Norminal steps one and two polish, plus 50 s step three polish

Figure 6.16: Complete simulation of three step process compared to experimental data - ICDSH: Integrated contact mechanics and density-step-height model DSH: Density-step-height model

6.6 Summary

In this chapter an integrated contact mechanics and density-step-height model is developed. Contact mechanics is used to compute the polish pressure on an envelope function that captures the long-range height variation on the die, while the density-step-height model formulation uses this pressure to compute the removal rates in the local up-areas and down-areas. A methodology for calibrating the model is proposed, and used to test the model against experimental data obtained from a comprehensive three step copper CMP process. The model predicts the trend in the experimental data well, and fits the data to within acceptable errors.

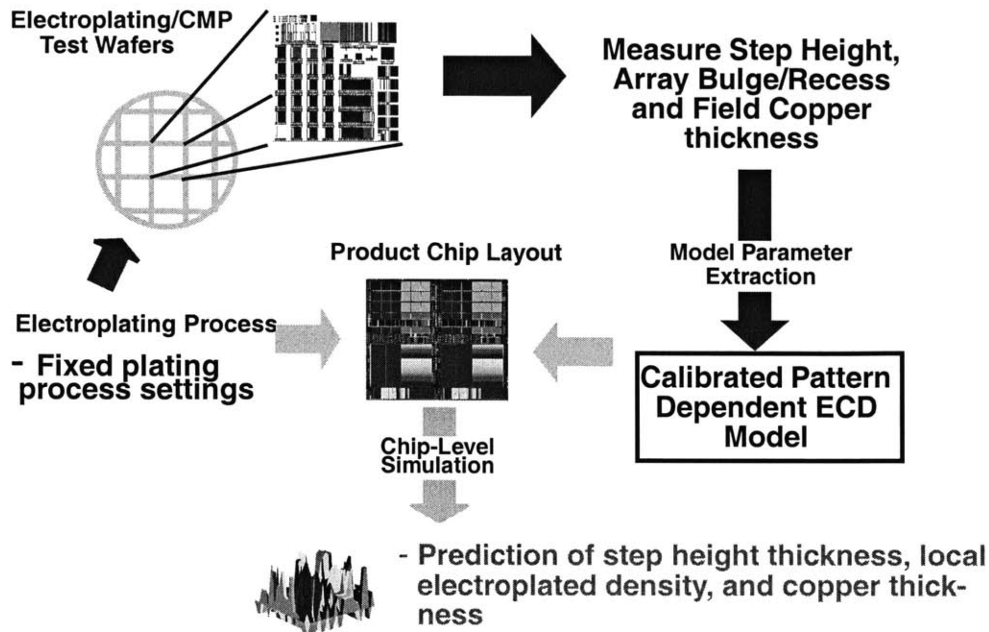
Chapter 7

Chip-Scale Simulation

The main goals of this thesis are to develop a semi-physical pattern dependent model for copper CMP processes and to incorporate the model into a simulator for predicting the dishing and erosion performance, as well as the copper thickness polish evolution, on an entire chip. In this chapter, the components of the simulator, and the methodology for using the simulator to do chip-scale predictions are described. In section 7.1, the framework for chip-scale simulations is described briefly. This is followed by brief descriptions of the components of the chip-level simulator, in sections 7.2 - 7.5. In section 7.6, the predictive accuracy of the simulator is tested, and the chapter concludes in section 7.7 with a summary.

7.1 Framework for Chip-Scale Simulation

The framework for doing chip-level simulation is illustrated in figure 7.1. The simulator integrates an electroplating modeling methodology with a copper CMP modeling methodology. A modeling methodology comprises a model and a calibration/characterization procedure for the model. Calibration involves performing CMP and electroplating experiments, to extract the models' parameters for a given copper CMP process, and a given electroplating process. Prediction involves using the calibrated models to simulate the copper thicknesses deposited by electroplating, the copper thickness evolution during CMP, and the dishing and erosion after CMP, for any random layout. The requirements are that the random layout must be plated with the calibrated electroplating process, and polished under similar conditions (down force, relative speed and consumable set) as the calibrated copper CMP process.



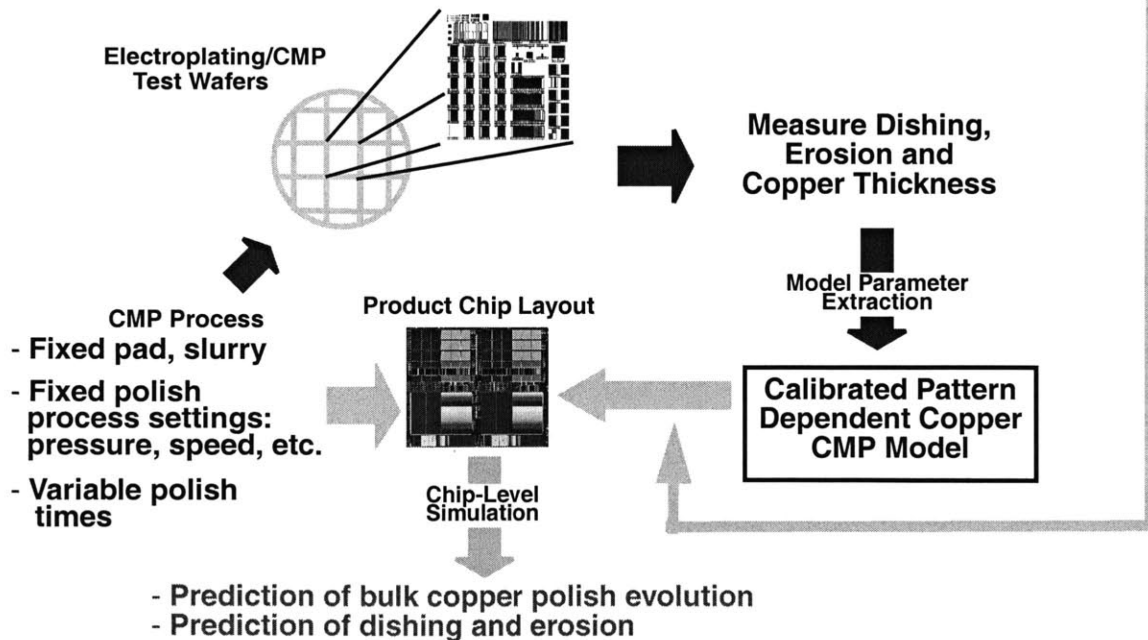


Figure 7.1: Framework for chip-level copper interconnect simulation

The chip-scale simulator has several components, including the electroplating model, the copper CMP model (the integrated contact mechanics and density-step-height model developed in this thesis), a layout extractor, a standard test mask, and a standard calibration experimental plan. These components are described in sections 7.2 - 7.5.

7.2 Layout Extractor

Dishing and erosion depend on line width, line space, and pattern density. The copper thickness evolution during CMP depends on the electroplated copper pattern density, the electroplated line width and space, and the long range electroplated copper height variation. In addition, the copper thickness deposited by electroplating also depends on the line width, and line space on a layout [12,36]. Hence, for the simulator to predict the dishing and erosion on a random layout or to calibrate the model using the test mask, the layout details of these masks must be known. A layout extractor is a tool that takes in any layout, and summarizes the layout patterns on it, calculating desired discretized statistics for the line widths, line spaces, line lengths, and local layout pattern density.

A typical layout has many objects in it: lines, squares, and other polygons. It would be impractical to have a layout extractor that gives the details of every object on the layout. Instead, a typical layout extractor discretizes the layout into small cells. In each cell, the layout extractor computes the average, maximum, and minimum line widths, line lengths, and line spaces [36]. It also computes the number of lines in certain line width ranges, and the layout density of the lines (corresponding to copper lines in a damascene process) in the cell.

The size of the cell should be chosen such that the extractor provides accurate information about the layout features, while maintaining computational efficiency. The larger the cell size, the

faster the computation, but the less accurate the layout information it provides. Typical cell sizes are 20 μm by 20 μm and 40 μm by 40 μm.

7.3 Electroplating Model

The electroplating model is an empirical model that expresses the thickness of the copper deposited, the array recess and step height in terms of line width and line space [36]. The model needs to be calibrated for every electroplating process. The calibration experiment needed is the electroplating of at least two wafers patterned with a specific test mask. Once the wafers are patterned and plated, the copper thickness deposited at specific sites, and the step height and recess for certain arrays are measured. This data is used to extract the model parameters.

Once the model is calibrated for the given electroplating process, it can then be used to predict the electroplating thickness, the step height, and the recess across an entire chip, for any random layout. The layout details for random layouts provided by the layout extractor are used as as inputs to the model, to do the predictions.

After computing the step heights in every cell of the random layout, the electroplating model also computes the local electroplated copper density in every cell. This local density is simply the total copper up-area in the cell. A detailed description of the electroplating model can be found in the thesis by Park [36].

7.4 Copper CMP Model

The copper CMP model used by the simulator is the integrated contact mechanics and density-step-height model formulated in chapter 6 of this thesis. For a given copper CMP process, simulated electroplated thicknesses, simulated electroplating step heights, and simulated local

electroplated copper densities for a standard test mask, and the calibration experimental plan described in chapter 6, are used to fully calibrate the model. The simulated results used in the calibration are provided by the electroplating model described above.

Once calibrated, the model can then be used to predict the copper thickness evolution during CMP, the bulk copper clearing times, and the dishing and erosion for any random layout. The requirement is that the wafers patterned with the random layout be polished using the same process (consumable set, slurry flow rate, down force and relative speed) as the process for which the model has been calibrated. It is important to note that the polish times of the test wafers used in the calibration need not be the same as the polish time for the wafers patterned with the random layouts. The model captures time dependencies accurately.

The layout details of the random layout provided by the layout extractor are used as inputs in the model prediction. For instance, the line width and line space information provided by the layout extractor are used to compute the maximum dishing parameter. Because the layout extractor provides statistical information of the layout features in a particular cell of the layout, the model prediction should also be interpreted as a statistic for the cell in question. For example, with information about the average line width and average line space in a cell, the model predicts the average dishing and erosion in that cell.

7.5 Test Mask

The test mask used in calibrating these models for any given CMP process and plating process, should have a wide range of patterns: line widths, line spaces, and pattern densities. The MIT-SEMATECH 854 mask, and the MIT mask version 1.2 are the most suitable of the currently available masks, for this task. These masks are described in chapter 2 of this thesis.

7.6 Testing the Predictive Accuracy of the Chip-Scale Simulator

To test the accuracy of the simulator, the three step copper CMP process described in chapters 5 and 6, is used to polish wafers patterned with a complex layout. This layout (hereafter referred to as mask Z) is different from the layout of the standard test mask used to calibrate the electroplating and copper CMP models. The experimental details including the polish times for two of the wafers patterned with mask Z are summarized in tables 7.1 - 7.2.

Table 7.1: Three step copper CMP experiment on the Mirra

Step #	Platen #	Pad	Slurry	Down force (psi)	Speed (rpm)
1	1	Stacked	EPC-5001	5	63
2	2	Stacked	EPC-5001	2	43
3	3	Stacked	10K-1	3	100

Table 7.2: Polish times of wafers patterned with mask Z

Wafer #	Step one	Step two	Step three
Z-1	63	102	55
Z-2	63	117	0

Some of the layout details for mask Z, obtained from the layout extractor are shown in figures 7.2 - 7.3. For the purpose of comparison, the same layout details for the calibration test mask are shown along side those for mask Z. The simulated average electroplated copper thicknesses, simulated electroplated step heights, and simulated local electroplated copper pattern densities, for both mask Z and the calibration mask are shown in figures 7.4 - 7.6.

Using the extracted values of the copper CMP model parameters for the three step copper CMP process in chapter 6, the electroplating model results, the layout extractor results, and the polish times for the Z-patterned wafers, the simulator predicts the dishing after polish step two, the dishing after polish step three, the erosion after polish step two, the erosion after polish step three, and the bulk copper clearing time. The simulated results are shown in figures 7.7 - 7.10. To check the accuracy of the simulated results, dishing and erosion measured at several spatial locations on the polished Z-patterned wafers, are compared to the simulated results at the same sites in figures 7.11 - 7.13. As seen in these figures, the simulated results match the trends in the measured data well. In addition, the simulated results are close to the measured results within errors of 100 - 500 Å. These errors are reasonable given that the model parameter extraction errors in steps one and three, the simulated electroplating error, and the dishing and erosion measurement errors, are in the same range. This indicates that the developed copper CMP model, the electroplating model, and the chip-scale simulator can be used to gain important insight into pattern dependent effects in copper interconnect formation.

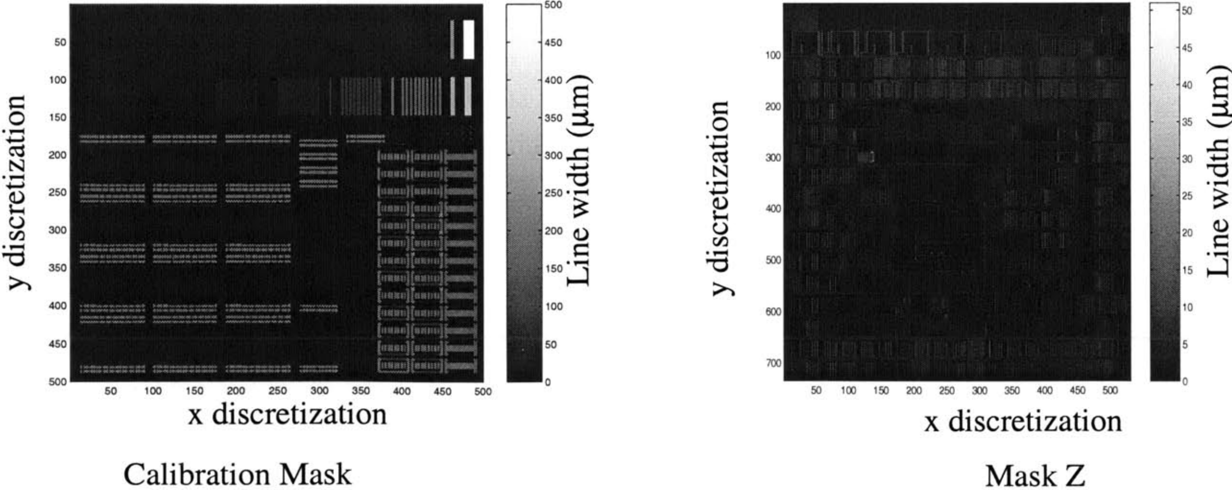


Figure 7.2: Average line widths extracted by layout extractor

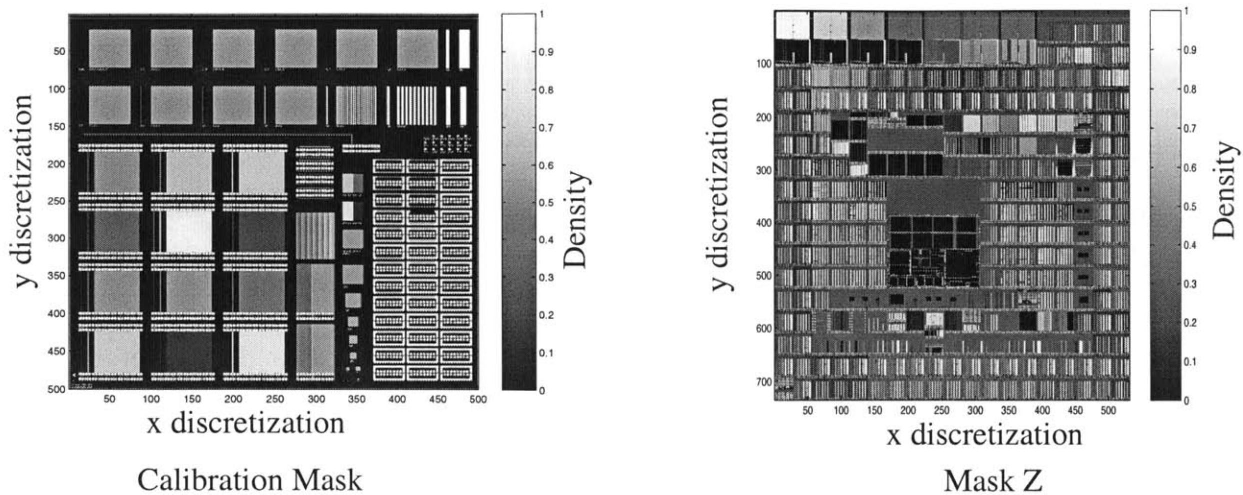


Figure 7.3: Local discretized layout density computed by layout extractor

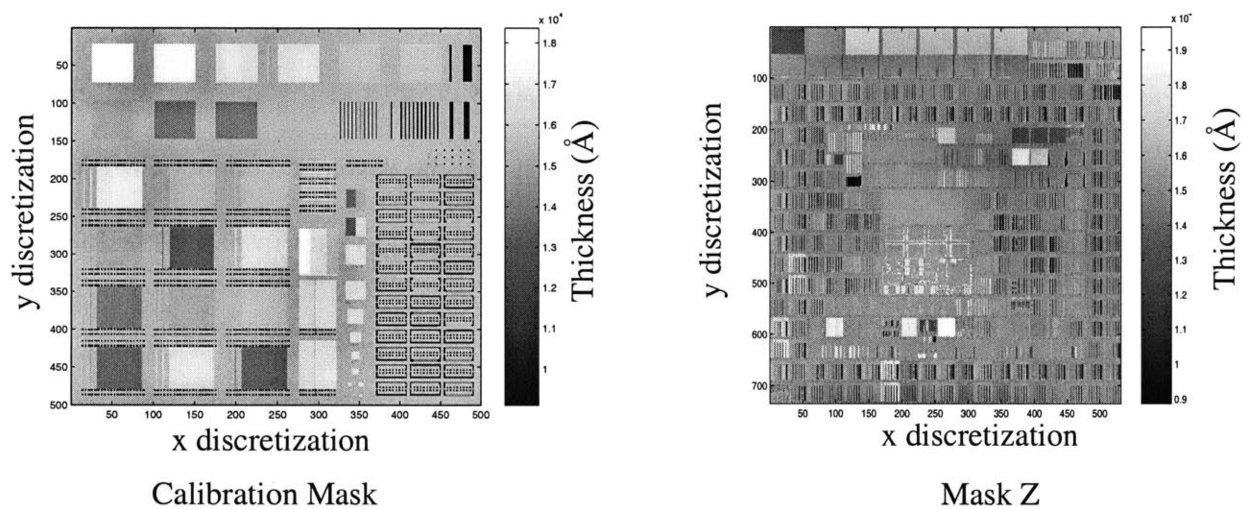


Figure 7.4: Simulated electroplated copper thickness across chip

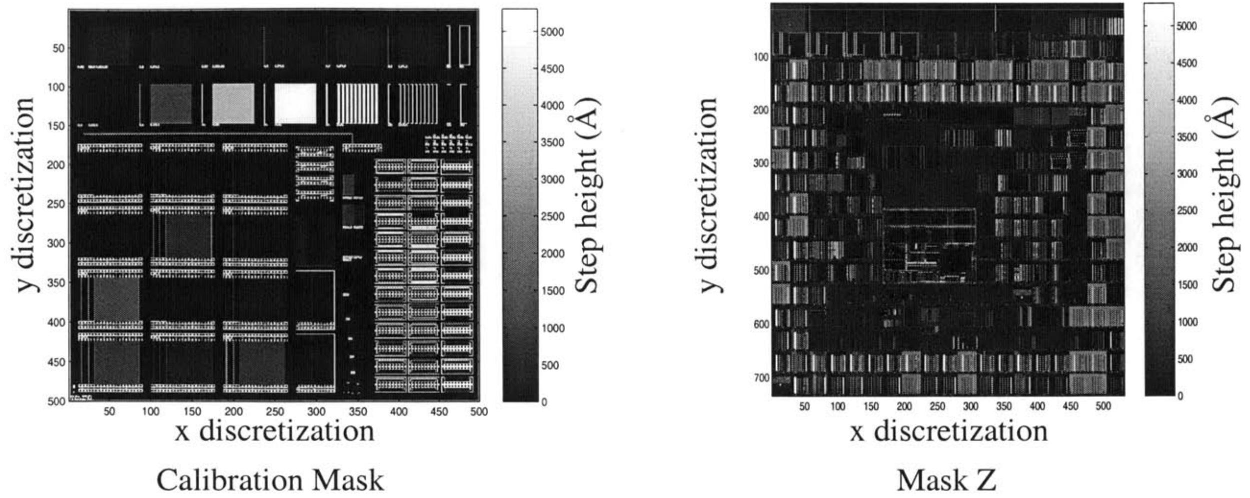


Figure 7.5: Simulated electroplated step heights across entire chip

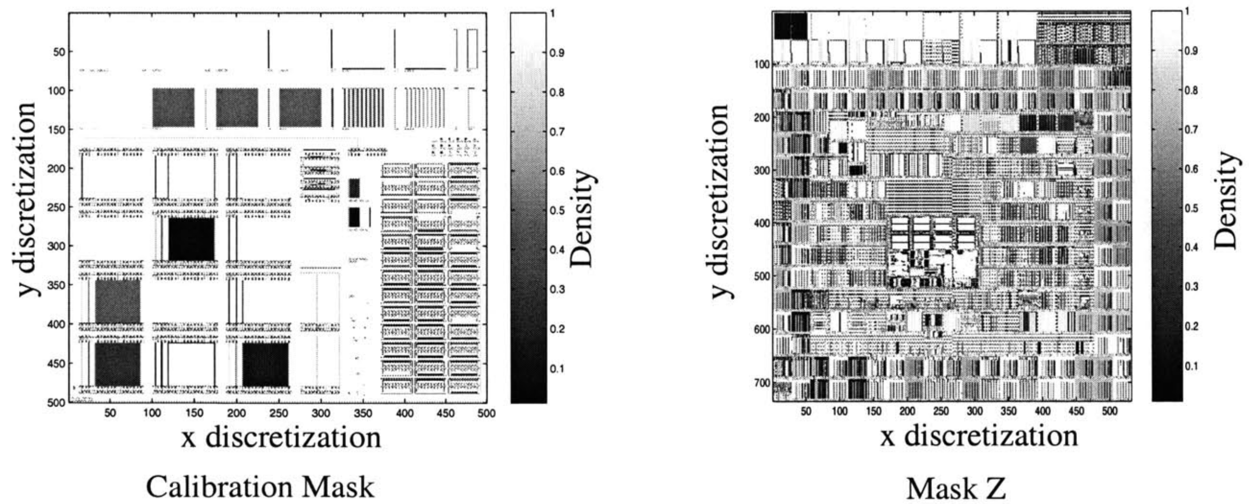
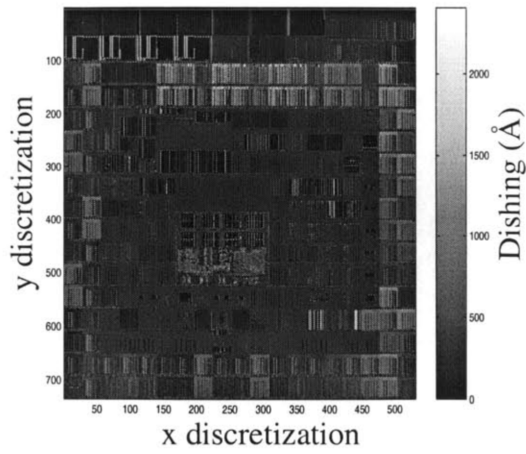
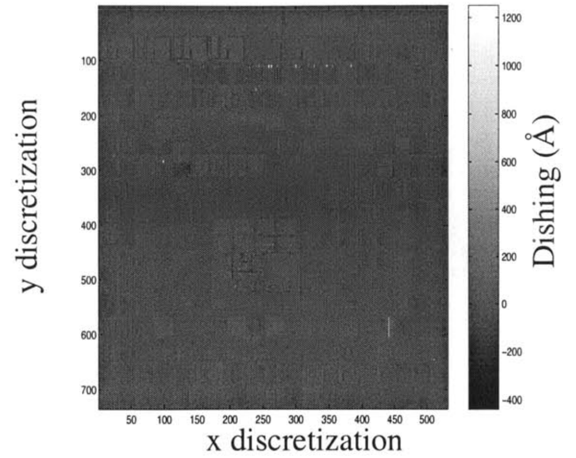


Figure 7.6: Simulated local electroplated copper pattern density

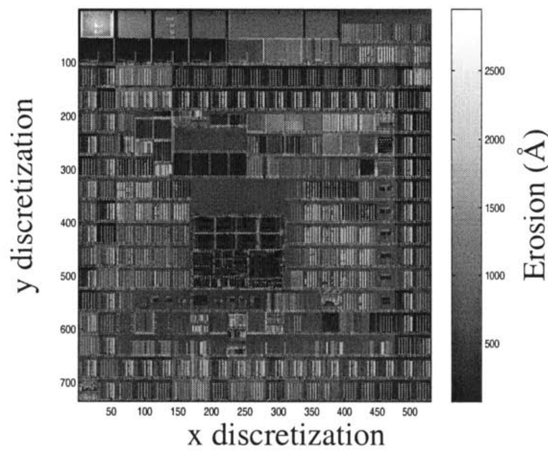


Dishing after step two polish

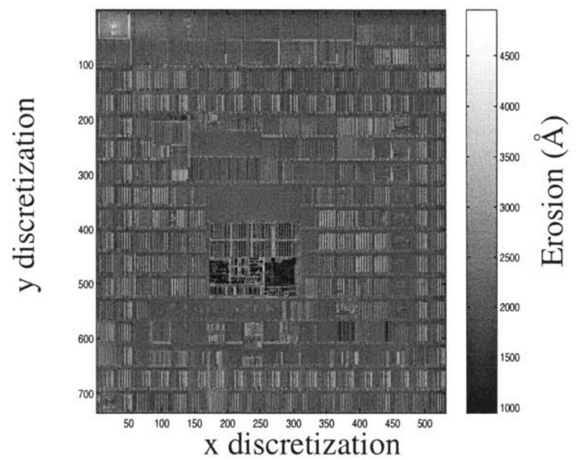


Dishing after step three polish

Figure 7.7: Simulated dishing across die, after steps two and three polish of wafer Z-1

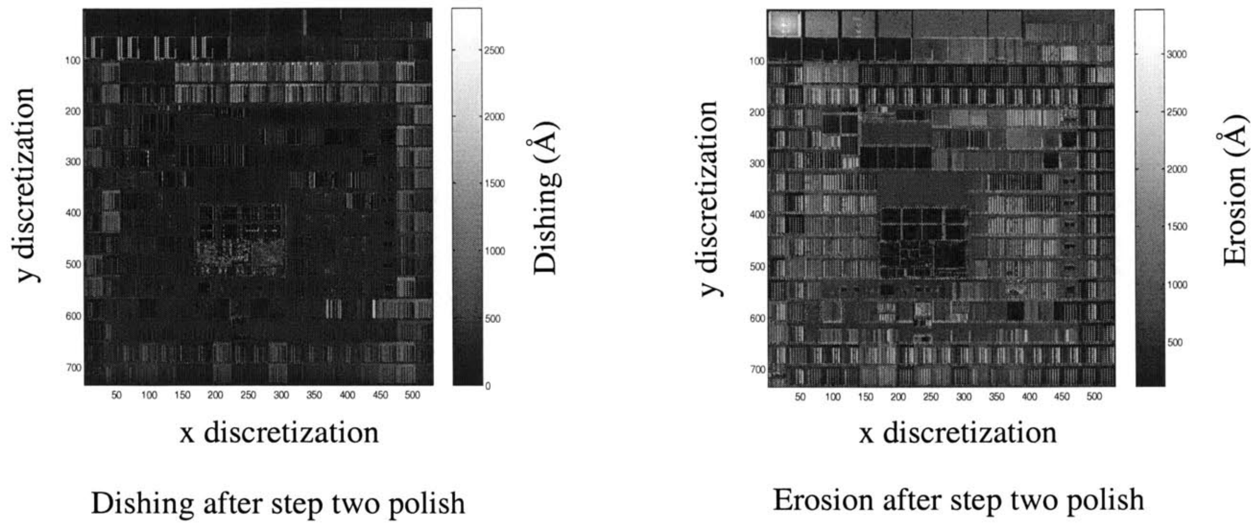


Erosion after step two polish



Erosion after step three polish

Figure 7.8: Simulated erosion across chip, after step two and three polish of wafer Z-1



Dishing after step two polish

Erosion after step two polish

Figure 7.9: Simulated dishing and erosion across entire die, after step two polish of wafer Z-2

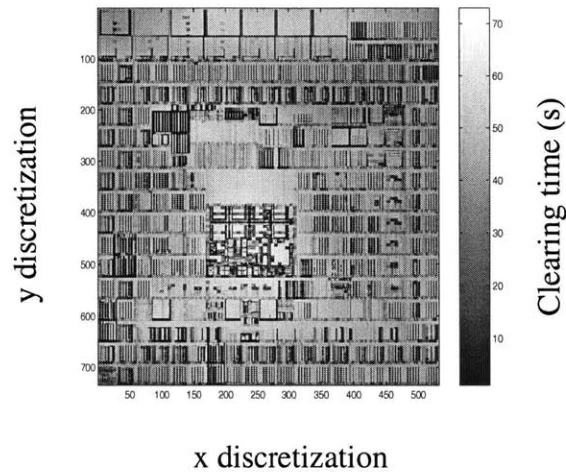
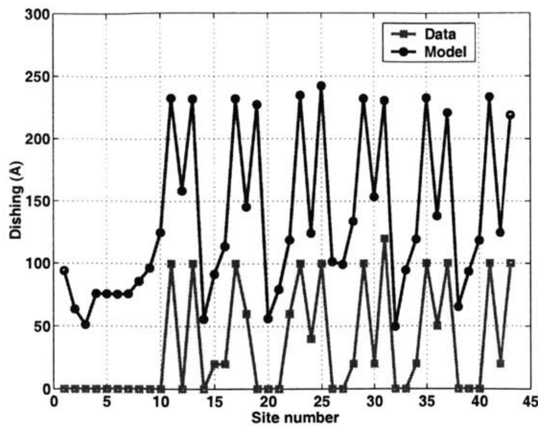
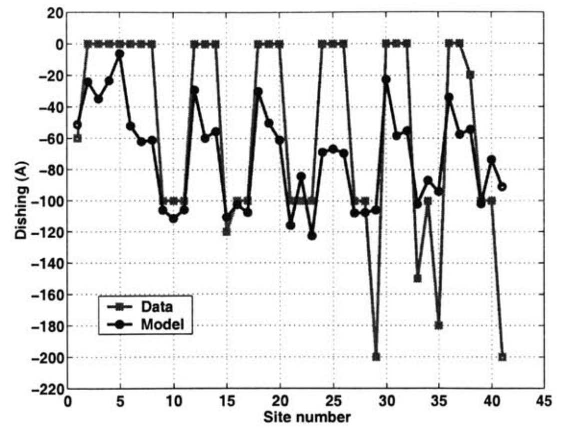


Figure 7.10: Simulated bulk copper clearing time across entire die, during step two polishing, of wafers Z-1 and Z-2

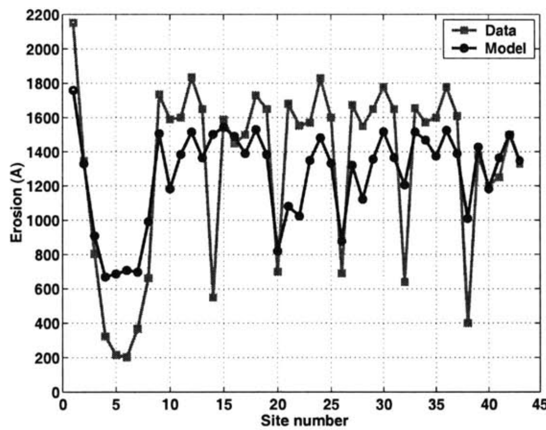


Dishing after step two polish

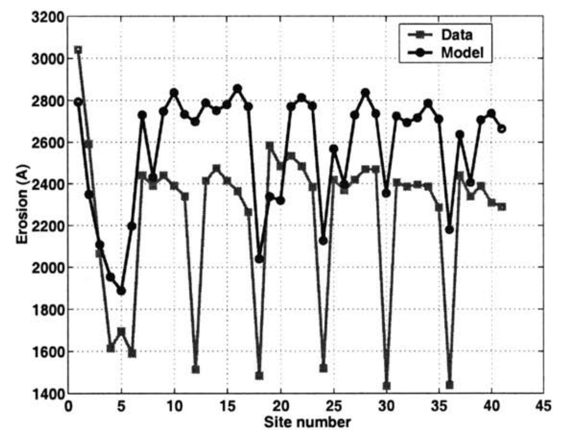


Dishing after step three polish

Figure 7.11: Simulated dishing versus measured dishing at selected sites on die, after steps two and three polish, of wafer Z-1

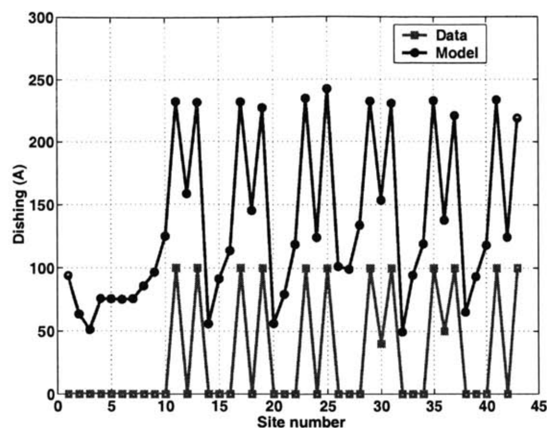


Erosion after step two polish

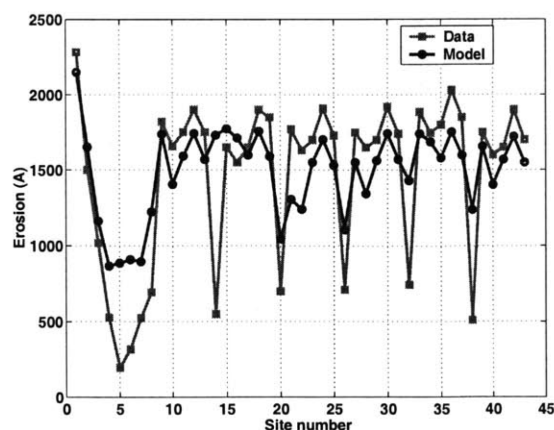


Erosion after step three polish

Figure 7.12: Simulated erosion versus measured erosion at selected sites on die, after steps two and three polish, of wafer Z-1



Dishing after polish step two



Erosion after step two polish

Figure 7.13: Simulated dishing and erosion versus measured dishing and erosion at selected sites on die, after step two polish, of wafer Z-2

7.7 Summary

In this chapter, the integrated contact mechanics and density-step-height model developed in this thesis is combined with an empirical pattern dependent model for copper electroplating processes, to form a chip-scale simulator for copper CMP and copper electroplating processes. The models making up the simulator need to be calibrated for every copper CMP process and every electroplating process, respectively. Once the models are calibrated, the simulator can be used to predict the dishing and erosion performance for any random layout polished under the same process conditions as those of the copper CMP process for which the copper CMP model has been calibrated. In addition, the plating process used to deposit copper on the wafers patterned with the random layout must be the same as that for which the electroplating model has been calibrated.

The simulator uses a layout extractor to extract the layout details (line widths, line spaces, line lengths, and local layout pattern density) on any given layout. The layout extractor discretizes

the layout into small cells, and extracts appropriate statistics of the lines, and polygons in each cell. In addition, it computes the layout density in each cell, based on the objects (lines and polygons) in the cell. The discretization or cell size is chosen to achieve accurate extraction of the layout details, without making the extraction process computationally prohibitive. Typical cell sizes are 20 μm by 20 μm and 40 μm by 40 μm.

To test the accuracy of the simulator, the three step copper CMP process calibrated in chapter 6 of this thesis is used to polish wafers patterned with a layout that is different from that used in the model calibration. A bottom-up fill electroplating process is used in depositing copper on the wafers. The electroplating model has already been calibrated for that process [36]. A comparison of the measured dishing and erosion to the simulated dishing and erosion shows that the simulated results follow the trends in the measured data quite accurately. In addition, the simulated results are close to the measured data within errors of 100 - 500 Å.

Chapter 8

Conclusion and Future Work

This chapter summarizes the key contributions of this thesis in section 8.1, and identifies areas for future work in section 8.2.

8.1 Summary

The main contribution of this thesis is the development of a chip-scale predictive semi-physical pattern dependent model for copper CMP processes. The model is integrated with an empirical chip-scale pattern dependent model for copper electroplating processes, to form a chip-scale copper CMP and copper electroplating simulator. The simulator predicts the dishing and erosion performance of calibrated copper CMP processes, on any layout. It also predicts the bulk copper thickness evolution during copper CMP, and can possibly identify clearing problems that tend to plague the CMP of multi-level copper interconnects. In addition, it can be used to assess the effectiveness of dummy fills in reducing dishing and erosion, and to generate smart design rules in conjunction with circuit simulators.

An extensive three step copper CMP experiment has been conducted to test the accuracy of the chip-scale simulator. For these experiments, it has been found that the simulator predicts the trends in dishing and erosion accurately. In addition, the predicted dishing and erosion are close to the measured dishing and erosion on real layouts, considering the errors in the model parameter extraction, electroplating simulation, and metrology.

The predictive copper CMP model developed in this thesis is an integrated contact mechanics and density-step-height model. It uses contact mechanics to compute the polish

pressure in each large region on the chip. Given the effective polish pressure, the density-step-height formulation computes the removal rates of the local up-areas and down-areas.

The model must be calibrated for every copper CMP process, before it can be used for predictive purposes. A comprehensive calibration methodology has been developed in this thesis. It includes the use of a specialized test mask, the polishing of several blanket and patterned wafers to capture the evolution of the copper CMP process, and pre-CMP and post-CMP metrology.

8.2 Future Work

The results presented in this thesis show that the developed copper CMP model and chip-scale simulator can be used to gain important insight into pattern dependent effects in copper interconnect formation. Additional work is needed to statistically include wafer level and polish process variations in the model, and to study the relationships between the model parameters and polish process parameters such as down force, relative speed, pad stiffness, abrasive size, abrasive concentration in slurry, chemical concentration in the slurry, and slurry flow rate.

Including wafer variation in the model will make it possible for the simulator to predict the evolution of the bulk copper thickness, and the dishing and erosion performance on any die across the wafer. In addition, including process variation in the model will make it more robust. Finally, understanding the relationships between the model parameters and polish process parameters will make it possible for the simulator to be used to optimize copper CMP processes.

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