Liquid Embossing: A Technique for Fabricating Sub-micron Electrical, Mechanical, and Biological Structures

by

Colin A. Bulthaup

Submitted to the Department of Electrical Engineering and Computer Science

in Partial Fulfillment of the Requirements for the Degrees of

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and Master of Engineering in Electrical Engineering and Computer Science

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February 6, 2001

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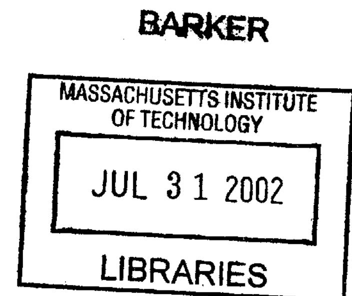

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ABSTRACT

I have developed an all-additive patterning technique, liquid embossing, in which a thin liquid film is embossed by an elastomeric stamp. I have shown that for sufficiently thin films isolated features are produced as the stamp contacts the underlying substrate, and that the liquid remains patterned even after removal of the stamp. This technique enabled the rapid patterning of inorganic nanocrystal solutions, since capping groups and solvents could volatilize efficiently at the exposed liquid surface. Using this technique I have fabricated all-printed all-inorganic transistors, photodetectors, capacitors and resistors as well as multi-layer structures with sacrificial layers and vias. I have also created micromechanical systems such as electrostatic motors and patterned biochips for mediated cell growth. The liquid embossing technique may enable a new route to inorganic semiconductor logic and machines as well as novel device architectures in a broad range of fields.

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1.0 Introduction

Electronic and electromechanical components are presently fabricated in large, immobile manufacturing facilities that are tremendously expensive to build and operate. Semiconductor device fabrication generally requires specialized microlithography and chemical etching equipment, as well as extensive measures to avoid process contamination. The total amount of time required for processing of a single chip is often measured in weeks, and typically requires repeated transfer of the chip into and out of vacuum conditions.

In addition to their expense, the fabrication processes ordinarily employed to create electronic and electromechanical components also involve harsh conditions such as high temperatures and/or caustic chemicals which limit their integration with functionally related but environmentally sensitive elements. For example, the high temperatures used in silicon processing are incompatible with heat-sensitive materials such as organic and biological molecules. High temperatures also preclude fabrication on substrates such as conventional flexible plastics, which offer widespread availability and low cost.

There are many motivations for developing technological alternatives to conventional photolithography. Recent developments in non-photolithographic methods of micro- and nano-fabrication may have importance in a number of fields including biotechnology, optics, and semiconductor device fabrication *(1)*. And yet, despite intensive effort to develop alternatives to conventional processes, no truly feasible techniques have yet emerged.

Dr. Paul Carey at Lawrence Livermore National Laboratory has developed a low-temperature roll-to-roll process for creating thin-film transistors on plastic substrates *(2)*. Unfortunately, this approach faces numerous technical hurdles, and does not substantially reduce the large cost and complexity associated with conventional photolithography and etching processes.

Dr. Stephen Chou at Princeton has developed a process called nanoimprint lithography (NIL) that utilizes a silicon mold, which is pressed under high pressure and temperature into a thin film of material *(3-5)*. Following cooling with the mold in place, the material accurately retains the features of the mold. The thin film may then be treated to remove the small amount of material remaining in the embossed areas. Thus patterned, the film may be used as a mask for selectively etching underlying layers of functional materials. This process is capable of producing patterns with very fine resolutions at costs significantly below those associated with conventional processes. But it is quite complicated, requiring numerous time-consuming steps to create a single layer of patterned functional material. The technique requires high application pressures

and temperatures at very low ambient pressures, thereby imposing significant complexity with attendant restriction on the types of materials that can be patterned. Perhaps most importantly, this technique is limited to producing single-layer features, thereby significantly limiting its applicability to device fabrication.

Dr. George Whitesides at Harvard has pioneered the use of elastomeric stamps for non-photolithographic patterning of materials. Perhaps the most well known technique that he has developed is micro contact printing (μCP) *(6-16)*. An elastomeric stamp is cast on top of a silicon master and the surface features of the wafer are thus replicated in the stamp. The stamp is then inked and a self-assembled molecular monolayer (SAM) can be transferred onto a Au surface. This SAM acts as an etch resist, and the underlying Au layer may be selectively etched to form patterns of conducting material. And yet, the technique is prone to very large defect rates and there are certain limitations on the maximum resolution with which the SAM can be patterned. In addition, this technique, like nanoimprint lithography, is limited to patterning single layers of material, and both of the processes rely on a chemical etch step which is expensive, time-consuming, and environmentally harmful.

Dr. Whitesides has developed a related technique called MIMIC (Micromolding In Capillaries) *(17-22)*. In this technique the elastomeric stamp is brought into conformal contact with a substrate forming small microfluidic channels between the recessed features of the stamp and the substrate. Functional liquid materials, such as a solution of carbon black, can then be deposited around the edges of the stamp and sucked into the microfluidic channels by capillary action. The material undergoes a phase change while in the channels and the stamp is then removed. This technique can directly pattern functional materials without an etch step, but the technique is generally limited to low-resolution features (in excess of 10μm), and more importantly, the types of geometries amenable to molding by this technique are severely limited.

Although not comprehensive, this list of prior art is representative of the current techniques being pursued to produce low-cost microelectronics on plastic substrates. Among all of these techniques there is still certain fundamental functionality which is lacking. It was therefore the objective of my research to develop a technique for producing microelectronics which met the following set of requirements.

- Provide an easily practiced, low-cost process for directly patterning functional materials without the need for multi-stage etching procedures.
- Increase the speed with which layers of functional materials can be patterned.

- Provide a fabrication process that requires no unusual temperature, pressure, or ambient conditions, thereby increasing the range of materials amenable to patterning.
- Facilitate convenient sub-micron patterning of multiple adjacent layers.
- Planarize deposited materials as part of the application process, eliminating the need for additional planarizing processes (such as chemical mechanical polishing), thereby facilitating fabrication of complex three-dimensional devices employing many layers.

The technique that I developed – liquid embossing – is similar to the work Dr. Whitesides conducted with micromolding, but it differs in two critical ways. The first is that the material that I am patterning remains a liquid throughout the embossing process, requiring no chemical reaction or phase change to occur during the actual patterning. This allows the rapid processing of a diverse set of materials that ranges from aqueous biomolecules to polymers and inorganic nanocrystals in heavy organic solvents. The second difference is that the emboss pushes completely through the thin liquid film, contacting the substrate beneath and enabling the additive fabrication of electrically isolated features and the direct formation of vias, both without the etching required for contact-printing *(6-16)* and imprint *(3-5)* schemes. I have achieved emboss times of less than 10 seconds, resolutions down to 200 nm, and embossing over areas exceeding 75 cm^2. Thus, liquid embossing is uniquely enabling for the rapid all-additive printing of inorganic structures through the use of nanocrystal solutions *(23-25)*.

2.0 Process

Liquid embossing consists of the following steps: creation of a master pattern with physical relief; casting of an elastomeric stamp using the master as a mold; creation of a thin liquid film and patterning this film by embossing with the stamp; removal of the stamp; and conversion of the patterned liquid film to a solid film by heat, light, or other means. Typically the master was an etched silicon wafer or a patterned layer of photoresist. Stamps were made by casting a silicone elastomer – PDMS Sylgard 184 (Dow Corning) – on the silicon master, (Fig. 001). Lateral deformation of the stamp while embossing was minimized by embedding a thin sheet of Mylar or other low strain material just under the embossing surface of the stamp.

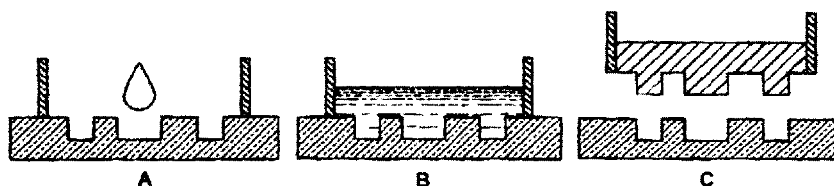

Figure 001: Schematic of stamp formation. **a)** A well is placed on top of a patterned silicon wafer and uncured elastomer is poured into the well. **b)** The elastomer is cured at 60° C for 3 hours. **c)** The cured elastomeric stamp is peeled off of the silicon wafer. The walls of the well can be included with the stamp to add additional stiffness.

Liquid films less than 500 nm thick were applied to glass or polyimide substrates by spin-coating or a draw-down method, in which a cylindrical bar is placed in contact with a drop of fluid and moved over a surface, (Fig. 002). A meniscus forms between the trailing edge of the bar and the substrate, leaving behind a uniform thin film. As shown in Fig. 003, the stamp was brought into contact with the liquid film along one edge and tilted forward so that the raised features of the stamp displaced the liquid and directly contacted the substrate. The continuous tilting motion created a moving line of contact that pushed air away from the gas-liquid interface, preventing bubble formation and aiding in mass transfer, a problem observed with imprint techniques *(26)*. When the stamp was brought into contact with the liquid film the raised features of the stamp would pierce through the liquid to create conformal contact with the underlying substrate. The excess liquid underneath the raised features of the stamp was pushed aside into the recessed features of the stamp. The embossing procedure required no pressure beyond the attractive forces between the stamp and the substrate, and excess pressure actually degraded the quality of the pattern.

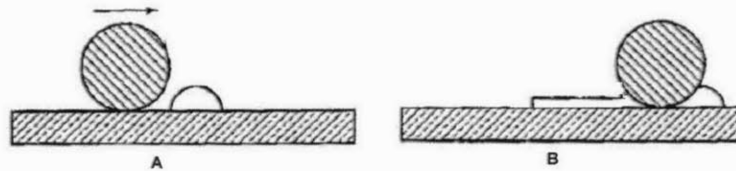

Figure 002: Schematic of the drawdown process for producing thin films of liquids. **a)** A small amount of liquid is placed on a substrate and a cylindrical bar is dragged across the surface of the substrate. **b)** A meniscus of liquid forms between the trailing edge of the bar and the substrate, leaving behind a very uniform thin film of liquid.

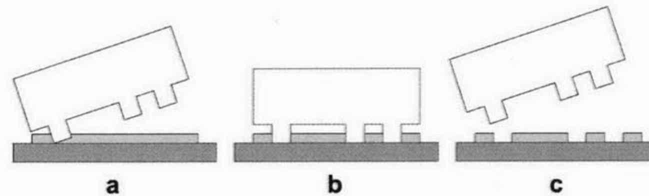

Figure 003: Schematic of the liquid embossing process. **a)** A thin film of liquid is produced on a substrate and a PDMS stamp with raised features is brought into contact with one edge of the liquid film. **b)** The PDMS stamp is tilted down into conformal contact with the underlying substrate. **c)** The stamp is then removed while the material is still liquid, and the liquid remains patterned.

After removing the stamp the film was still liquid and remained patterned. In fact, the stamp could be used to re-emboss the same film of patterned liquid with a new and different pattern. All of the liquid remained on the substrate and the stamp could be reused immediately without any cleaning. It is believed that the liquid remained patterned due to the thinness of the film and due to the fact that the liquid material had been completely displaced by the stamp leaving behind the exposed substrate. The surface tension between the liquid and the substrate keeps the liquid in its patterned state. Theoretically, this process of patterning a liquid would not work with a surface-emboss, ie an embossing step that does not penetrate through the material to the underlying substrate.

After removal of the stamp, the liquid could be converted to a solid. For most materials this was typically done by curing at 300° C for 300 seconds, although cure times as short as 30 seconds were achieved with laser-induced heating. All of the patterning and thin film preparation was conducted under ambient conditions outside of a clean room.

I have conducted a large number of experiments to characterize the liquid embossing process. One of the most important things to determine was how far the PDMS stamp could push material.

When the raised features of the stamp emboss through the liquid film they must displace the underlying liquid. For liquids with non-zero viscosities there is a finite distance over which the PDMS stamp can push this material. Fig. 004 shows a schematic of the test structures that I designed to characterize this finite distance, and Fig. 005 shows an optical image of the results.

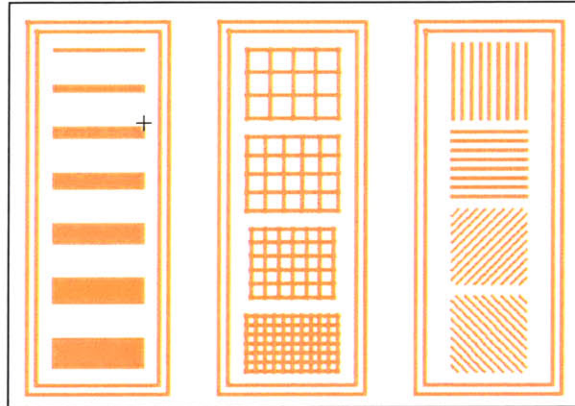

Figure 004: Overhead view of the designed test structures which were used to characterize the liquid embossing process.

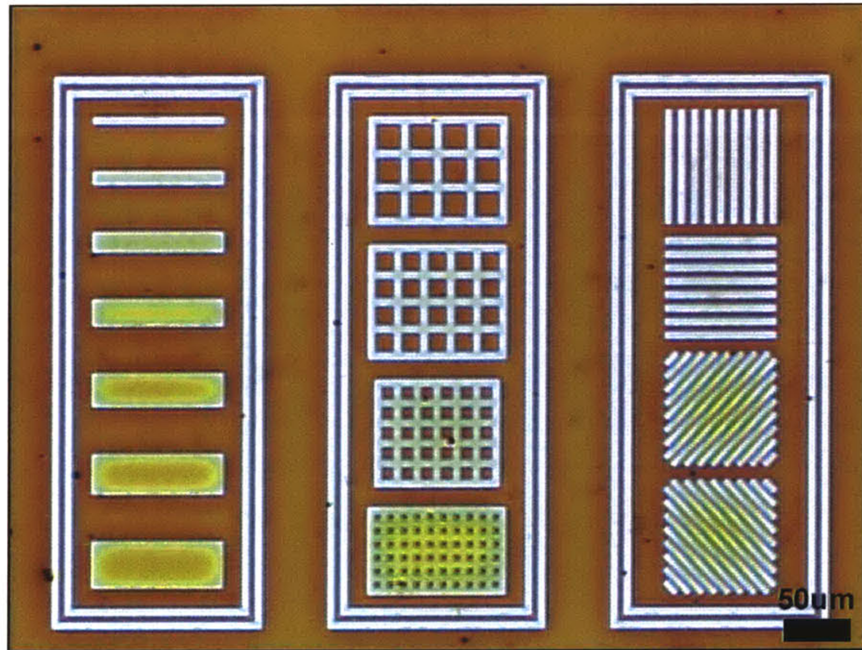

Figure 005: Optical image of test structures fabricated in Ag. The colored areas are Ag, and the white areas are the exposed substrate.

The results from the test structures indicated that liquid embossing could completely clear the liquid material from features 5μm wide, but with features larger than 5μm wide there was a small film of residual material left behind. In addition, the test structures also showed that there is a

maximum on the percentage of the patterned film that can be cleared away. The middle set of features in Fig. 005 show that features with greater than 50% cleared out area will have problems with residual films. This is because there is a finite volume in the recessed features of the PDMS stamp, and if that volume is overfilled then there will be an excess film that forms underneath the raised features of the stamp.

Both of these limitations of liquid embossing suggest a particular set of design rules for building circuits. Rather than patterning the features directly, liquid embossing instead patterns the outlines of features. This is a slightly different paradigm than that currently used in designing circuits, but the end result is identical. Whether the features are patterned or their outlines are patterned, the circuit will still be identical in the end. The second design rule is that the percentage of cleared area in any region of the chip should not exceed 50%, although by using thinner films of material this number can easily be increased. In Sections 3.1-3.13 I discuss the large number of circuits that I have created using the liquid embossing process and these two design rules.

3.1 Optical Gratings

The first structures that I fabricated with the liquid embossing process were optical gratings. These structures were an ideal first candidate for fabrication for several reasons. They were relatively large (> $4cm^2$) so it was easy to work with them, they had a variety of different feature sizes ranging from 200nm – 1μm, the features could be seen using an optical microscope, and perhaps most importantly, I could order gratings from Edmund Scientific cheaply and quickly. The gratings that I used were 1" x 1" with repeating parallel grooves spaced 400nm – 3μm apart. The blaze angle of the gratings ranged from 10° to 45°. I created wells on the surface of these gratings by either epoxying a plastic box to the grating surface or else by taping the edges of the grating with scotch tape, (Figs. 006-007). I then filled the wells with PDMS elastomer – Sylgard 184 (Dow Corning) – and cured the stamps in place at 60-70°C for 3 hours.

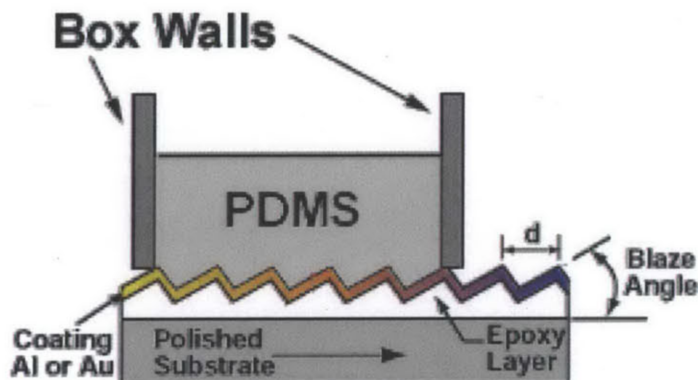

Figure 006: Schematic for casting a PDMS stamp on top of an optical grating. The walls surrounding the PDMS were either a box epoxied onto the surface of the grating, or else pieces of scotch tape attached to the edge of the grating.

[Image modified from Edmund Scientific original]

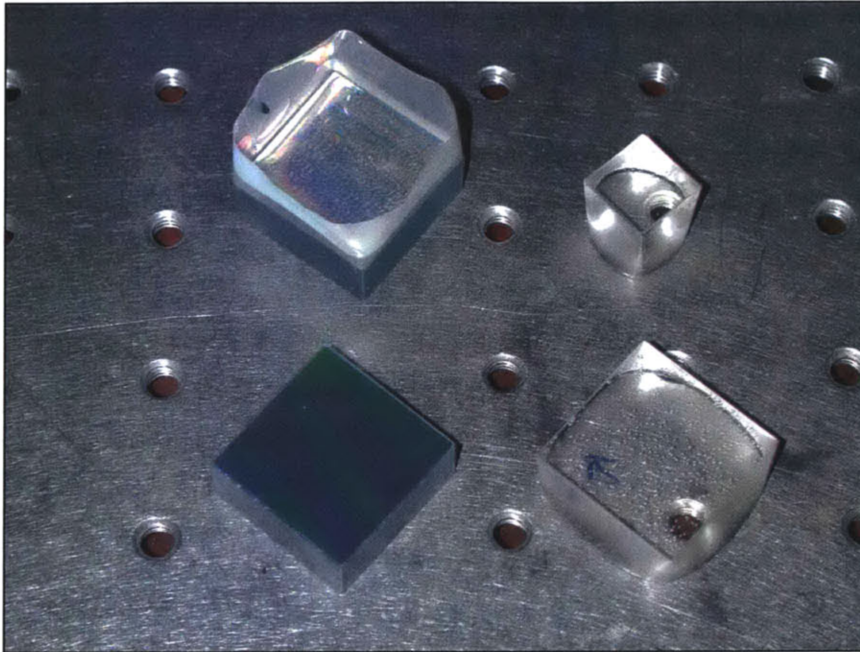

Figure 007: A collection of optical gratings and PDMS stamps. Going counterclockwise from the upper-left: 1) An optical grating with scotch tape around the edges and PDMS cured in place, 2) A blank optical grating, 3) A PDMS stamp that has been peeled off of the master grating, 4) Another PDMS stamp cast off of a smaller grating.

The particular materials that I was interested in patterning were nanocrystalline colloids of various different metals. These colloids have been used in screen printing to pattern metal lines on printed circuit boards. They have resistivities within a factor of 10 of the bulk material and because they are nanocrystals they can be sintered at vastly reduced temperatures. For example, although gold normally melts at 1100°C, gold nanocrystals will sinter at 200-300°C, (depending on their particular size.) Another advantage of these colloids is that after sintering them there is very little organic material left behind which was important when fabricating inorganic transistors. I typically worked with either gold (Au), silver (Ag), or cadmium selenide (CdSe) nanocrystalline colloids in solutions of α-terpineol or pyridine.

I produced thin films of the nanocrystals by either spin coating or by dropping a small amount of the liquid on a glass slide and rubbing a second glass slide on top of the drop to decrease the thickness of the film. Typical thicknesses were 100-300nm and the spincoating produced significantly more uniform films than the two slide technique. I brought the stamp into contact with the liquid film and allowed it to make complete contact with the underlying substrate. I typically left the stamp in place for 1-5 minutes prior to removing it in order to allow the liquid to completely equilibrate under the stamp. After removing the stamp all of the liquid remained on the substrate and the stamp could be used to make subsequent embossings. If the stamp did get

dirty it could be cleaned by applying isopropanol and rubbing lightly and then rinsing with methanol.

After removing the stamp I immediately cured the patterned material at 300° C for 10 minutes. I also investigated what happens if the material is first cured at 150° C to drive off the solvent prior to curing at 300° C, and what happens if the material is placed under vacuum to boil off the solvent prior to curing at 300° C. In both cases the quality of the patterning and the material characteristics were virtually identical to the results obtained by simply curing the material at 300° C immediately. By curing at temperatures higher than 300° C I was able to improve the conductivity of the metallic nanocrystals, probably because the higher temperatures increased the density of the film.

The metal gratings that I fabricated showed remarkably good pattern transfer over large areas. Fig. 008 shows an overhead light diffracting off of several patterned gratings. You can see that the gradient of the color of the diffracted light is very uniform across each of the devices. By shining a laser through the gratings you could very clearly see the different diffracted modes, and gratings with different periodicities demonstrated differently spaced modes.

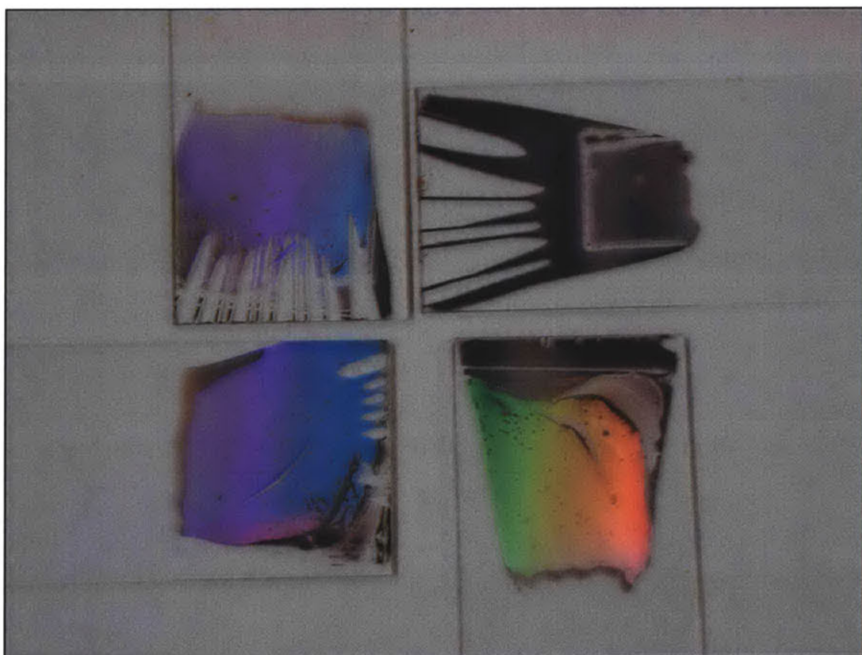

Figure 008: Overhead view of several liquid-embossed metallic gratings. Each grating was fabricated by spinning-down metal nanocrystals on the end of a glass slide and then embossing with a PDMS master. Three of the gratings shown are diffracting light from overhead, while the fourth grating has a different periodicity and thus is not diffracting light into the camera.

Inspection under an optical microscope revealed very uniform patterns of parallel metallic lines with regions of the exposed substrate between the lines, (Figs. 009-011). Gratings with periodicities of 3μm, 800nm, and 660nm could be discerned under the optical microscope, while gratings with periodicities below 400nm could not be discerned.

Figure 009: Optical image of metallic grating with 3μm periodicity fabricated in Au.

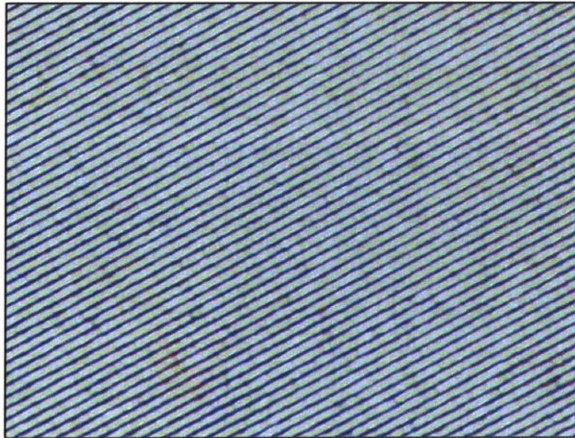

Figure 010: Optical image of metallic grating with 800nm periodicity fabricated in Ag.

Figure 011: Optical image of metallic grating with 660nm periodicity fabricated in Au.

In order to discern gratings with periodicities smaller than 500nm, and in order to better characterize the 3-dimensional structure of the gratings, I analyzed them with an Atomic Force Microscope (AFM). These early structures were quite rough as seen by the AFM images, (Figs. 012-013). And yet, it is still quite clear that the grating pattern was being clearly transferred to the metal, and the areas between the metal lines was cleared of material. In section 3.5 there are several AFM images of multi-layer gratings that show much more uniform edges and cleared areas between lines.

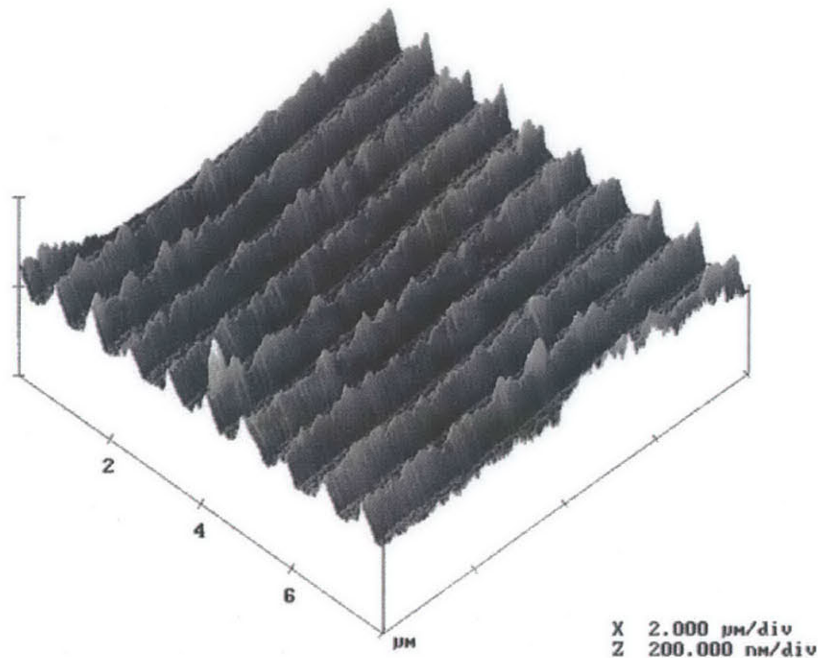

Figure 012: AFM image of a Ag grating with 800nm periodicity.

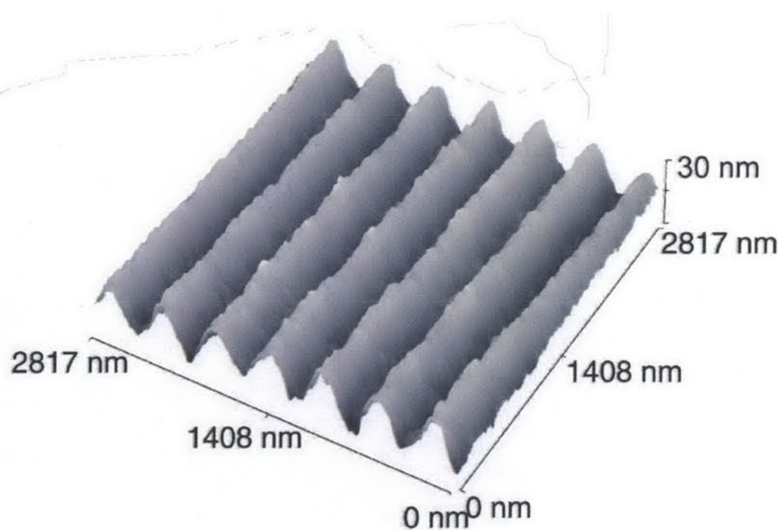

Figure 013: AFM image of a Au grating with 400nm periodicity.

The conductivity of the metal lines was measured by depositing three pieces of Indium shot on top of the grating and sintering at 150° C. These pieces of shot were deposited to act as macroscopic pads which could be more easily probed. In addition to Indium shot, I have also used Acheson Silver and large droplets of metallic nanocrystals to make pads. Two of the three pads were oriented running in the same direction as the parallel metal lines, and the third pad was oriented perpendicular to the metal lines, (Fig. 014). I probed the conductivity between the two pads running parallel to the lines and found the metal to be highly conductive, (Fig. 015). It was difficult to determine a value for the resistivity of the crystalline Au since I couldn't determine exactly how many lines were connected by the two pads and I did not take an AFM of the lines to determine their height. Still, the rough value was within an order of magnitude of the resistivity for bulk Au. A more exact calculation of the resistivity of the nanocrystalline metal is presented in Section 3.3. I also probed the conductivity between the two pads which were perpendicular to the grating lines and found the resistance to be greater than 20 GΩ. This strongly indicates that the nanocrystalline material was completely removed from between the metal lines by the raised features of the stamp

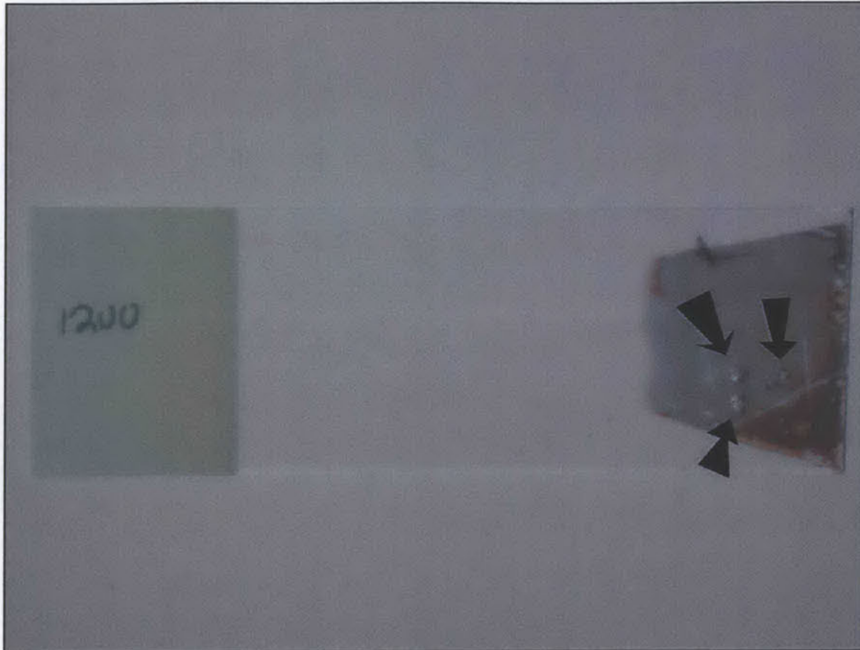

Figure 014: Glass slide with a patterned 800nm periodicity Au grating. Three pieces of Indium shot were sintered onto the grating where the arrows are pointing. The grating is oriented with the parallel lines running from left to right, and therefore there is conductivity between the two shots that are oriented horizontally, and zero conductivity between the shots oriented vertically.

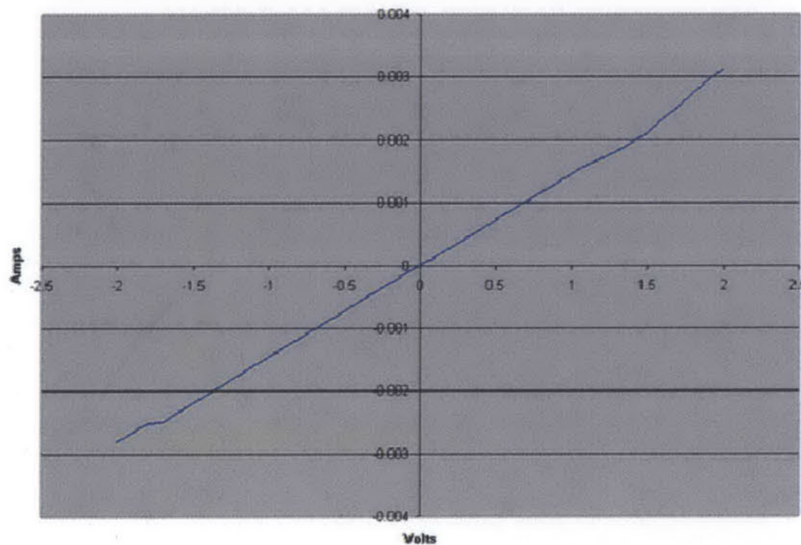

Figure 015: IV curve of the 800nm periodicity grating shown in Fig. 014, demonstrating conductivity between the horizontal pads and zero conductivity between the vertical pads.

3.2 Complicated Patterns

After fabricating metallic gratings, the next thing to demonstrate was the ability to pattern arbitrary non-repeating non-trivial patterns. I used the software package Ledit, produced by Tanner Tools, to create a GDSII description of the patterns that I wanted to fabricate. The first mask that I created, (Fig. 016,) was designed for a 4" wafer, and it was designed to be reduced 10x by an optical stepper. Other subsequent masks that I designed typically were designed for 1x contact mode lithography. I had the mask fabricated by the company Photronics Inc., and I then used the facilities in the Microsystems Technology Lab (MTL) to fabricate a number of wafers with a 1μm layer of photoresist which had been patterned by the mask. I cast PDMS stamps off of these silicon master wafers and the stamps showed very sharp pattern replication and there was no problem with adhesion to the silicon wafer or delamination of the photoresist. Additional stamps could be cast off of the same wafer with no apparent degradation in quality.

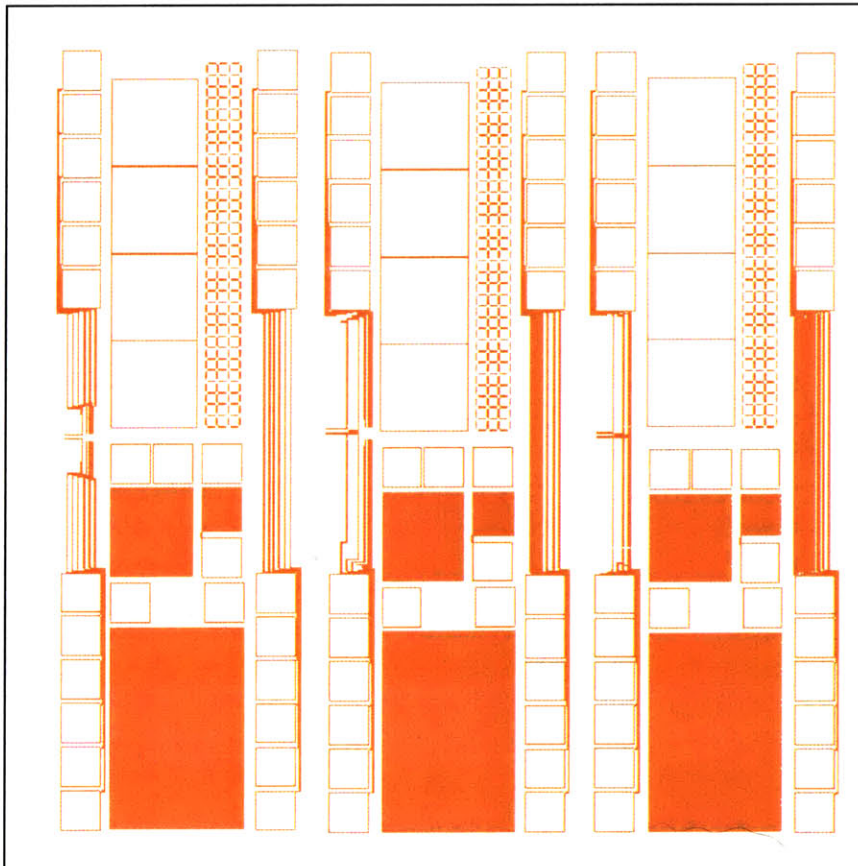

Figure 016: Image of the first mask that I designed with arbitrary features. The three replicated regions contained identical patterns with 1μm, 3μm, and 5μm features.

The first mask contained a number of interesting devices which I will discuss in later sections, but for this section I want to simply demonstrate the ability to pattern arbitrary features in a wide variety of materials. The mask contained long lines, small interdigitated features, large fields of replicated features, large open areas, and small intricate patterns. Each pattern on the mask was replicated three times with three different feature sizes: 1μm, 3μm, and 5μm. Fig. 017 shows a close-up of the mask with a large field of crosses and a simple tiled pattern. The areas that are colored are features that are raised on the stamp, and they are the features which will emboss through the thin liquid film and contact the underlying substrate. When I designed this mask I assumed that there would be problems with the recessed areas of the stamp touching down in large open areas where there were no supports, which is a common problem with micro-contact printing. I therefore filled the large square in Fig. 017 with crosses in order to prevent touch-down.

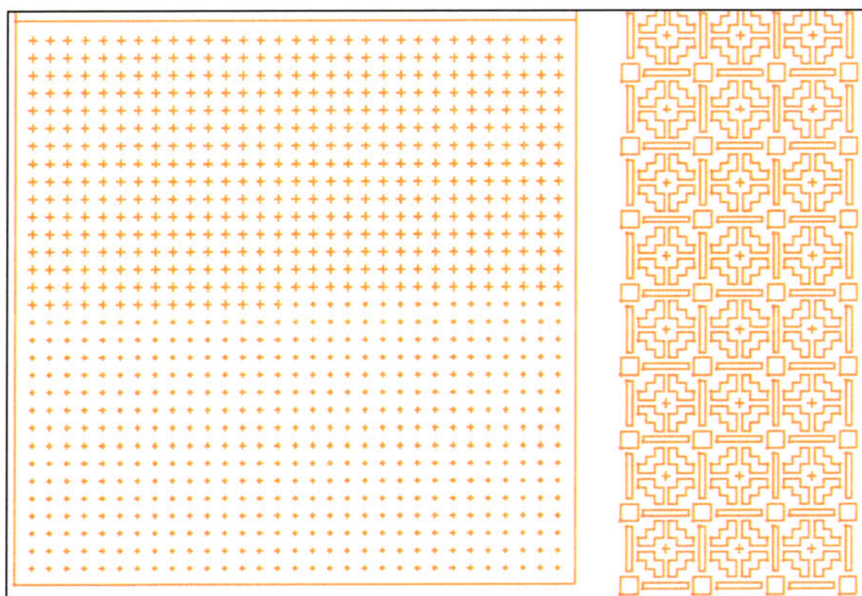

Figure 017: Close-up of 3μm patterns in the mask.

I used the drawdown technique to create thin films of Ag nanocrystals, and I then patterned the films with the PDMS stamps, (Fig. 018). Although there were several defects with these early patterns, (most notably the light diagonal lines caused by non-uniform lowering of the stamp,) in general the patterning was remarkably good. Perhaps the most surprising result though was that there appeared to be no problem at all with touch-down. Large open regions were patterned just as well as regions with a high density of features. You can also see in this optical image the slight non-uniformity around the edges of features where the excess liquid from the embossing process is pushed. Fig. 019 shows a zoomed in view of the patterned features which highlights

the non-uniform edges. In addition, this zoomed in view also shows that the areas between features have been completely cleared of nanocrystalline material.

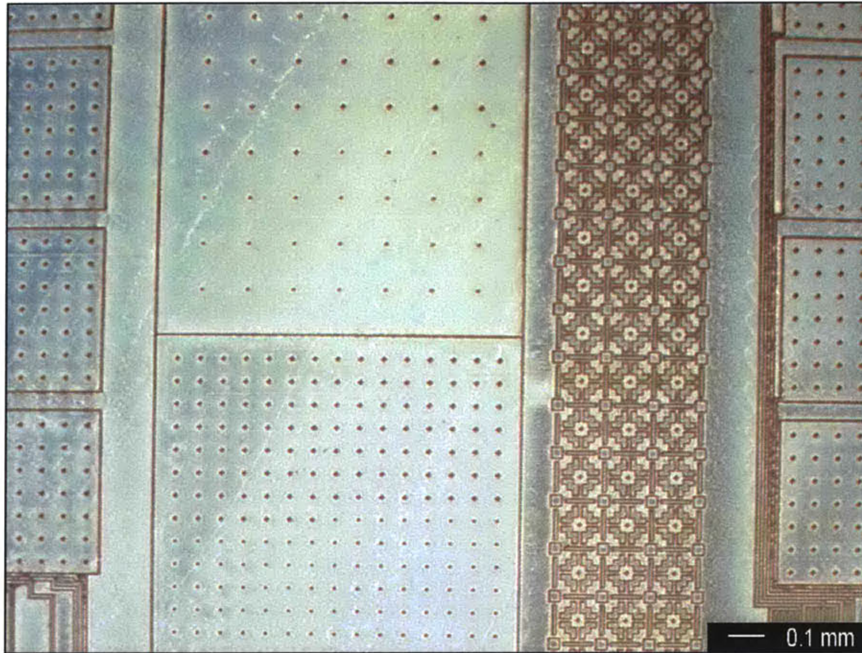

Figure 018: Optical image of 3μm patterns fabricated in Ag.

Figure 019: Zoomed in view of 3μm Ag features. This view shows the slightly thicker regions near the edge of features, and it shows that the material between features has been completely removed.

One potential limitation of the liquid embossing process is that the raised features of the stamp are moving around material, and therefore the thicknesses of different features can vary. Fig. 020 shows another zoomed in region of 3μm Ag features, and it can be seen that certain features are noticeably brighter, (ie thicker,) than other features. This problem can be reduced somewhat by allowing the stamp to sit in place longer while the liquid equilibrates. Another solution is to work with thicker films so that slight variations in thickness have less of an effect on device performance. The final point to note is that for 99% of all digital devices the actual conductance of the interconnect lines doesn't matter just so long as the conductance is greater than a certain minimum value.

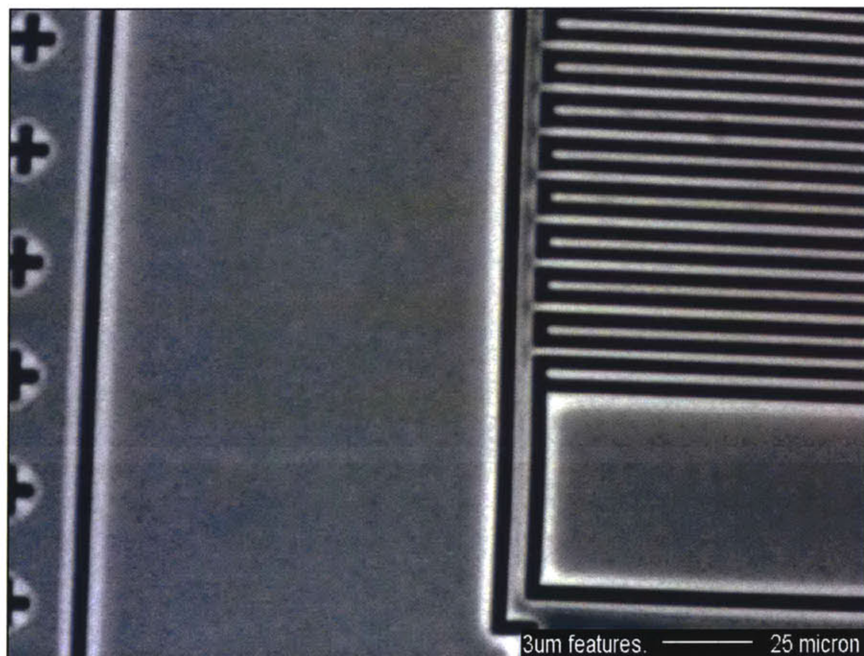

Figure 020: Zoomed in view of 3μm Ag features. This view shows the variation in thickness of different features.

Features that were fabricated in Au had much thicker films and therefore there was less evidence of variation between different features. In Figs. 021-022 the features showed very good uniformity and the quality of the features was remarkably sharp. Fig. 022 is especially interesting since it shows long snaking lines that are 1μm wide and several centimeters long. These long wires are completely intact with zero defects over the entire patterned area. It is this ability to pattern arbitrary features with very fine resolution over large areas with no defects that truly sets liquid embossing apart from other techniques like micro-contact printing.

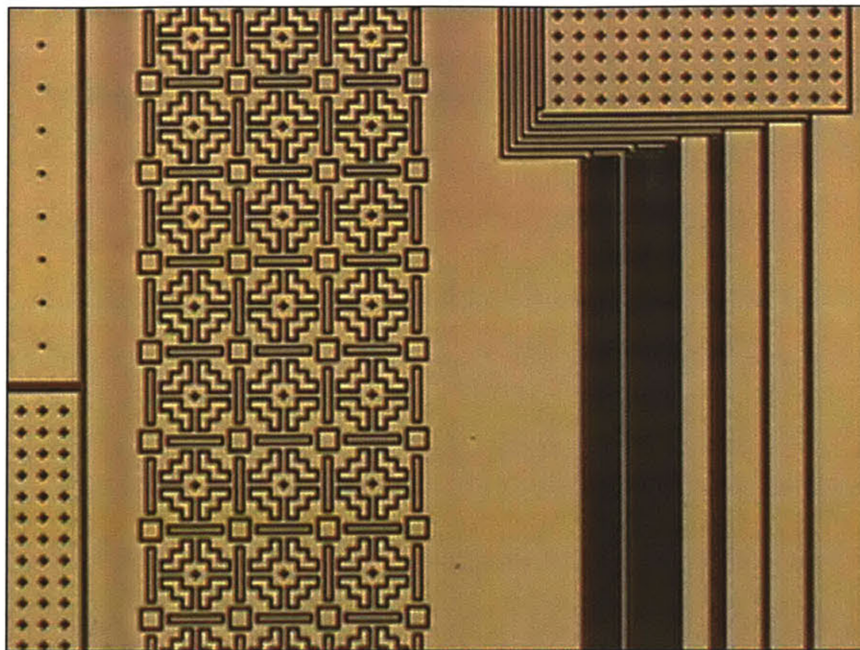

Figure 021: Optical view of 1μm Au features.

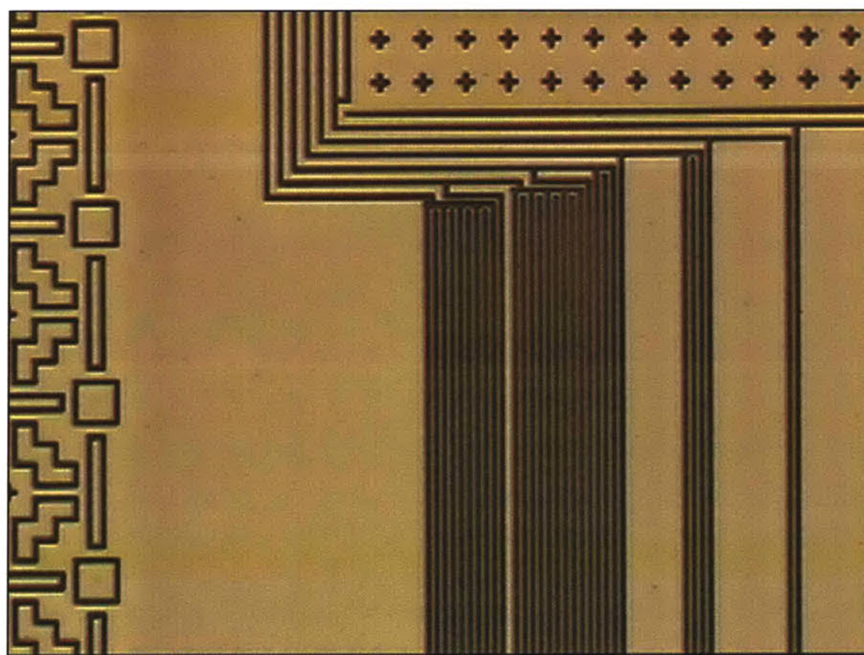

Figure 022: Zoomed-in view of 1μm Au features. The features are very uniform and the patterns are remarkably sharp.

In addition to Ag and Au I also patterned features in CdSe, (Figs. 023-024). The solution of CdSe that we synthesized had two problems with it that made it difficult to pattern. First of all, the mass percentage of CdSe nanocrystals was very low so the resulting film was very porous. The

second problem was that the solvent for the CdSe nanocrystals was pyridine which has a much lower boiling point than α-terpineol. This meant that it was very difficult to form a thin film of the CdSe solution and pattern it before it evaporated. I therefore used the PDMS stamp as both a drawdown bar and as a tool for embossing. I placed a small droplet of CdSe on a substrate, contacted one edge of the stamp to the droplet and then slowly lowered the rest of the stamp. As the stamp came into contact with the substrate it pushed the excess CdSe ahead of it and thus produced a thin film of CdSe and embossed it at the same time. I tried to use this technique with other liquid solutions, but I found that the technique only works with very low viscosity solvents, such as pyridine. The patterns that it produced in CdSe were quite sharp.

The CdSe solution had large agglomerates which formed over time and a film of CdSe would typically have an even distribution of these agglomerates, as can be seen in Fig. 024. A surprising capability of liquid embossing is that it could emboss these agglomerates in the same way that it embossed the liquid. A close inspection of Fig. 024 shows that only a very small minority of the agglomerates were left to span across a channel. When small dust particles have landed on thin films of liquid prior to embossing I have observed similar behavior.

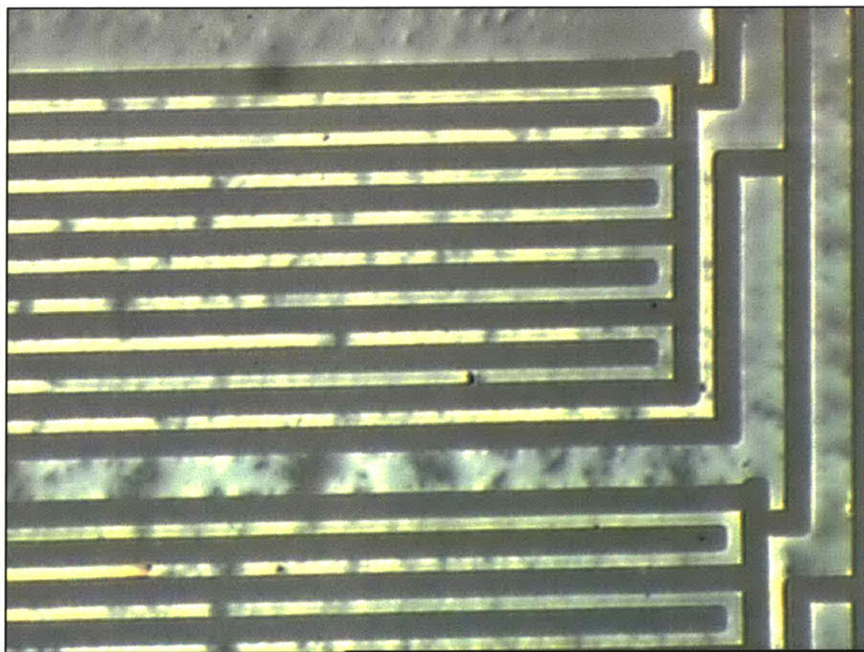

Figure 023: Zoomed-in view of 3μm CdSe features. The porosity of the film was due to the low mass-percentage of the CdSe solution.

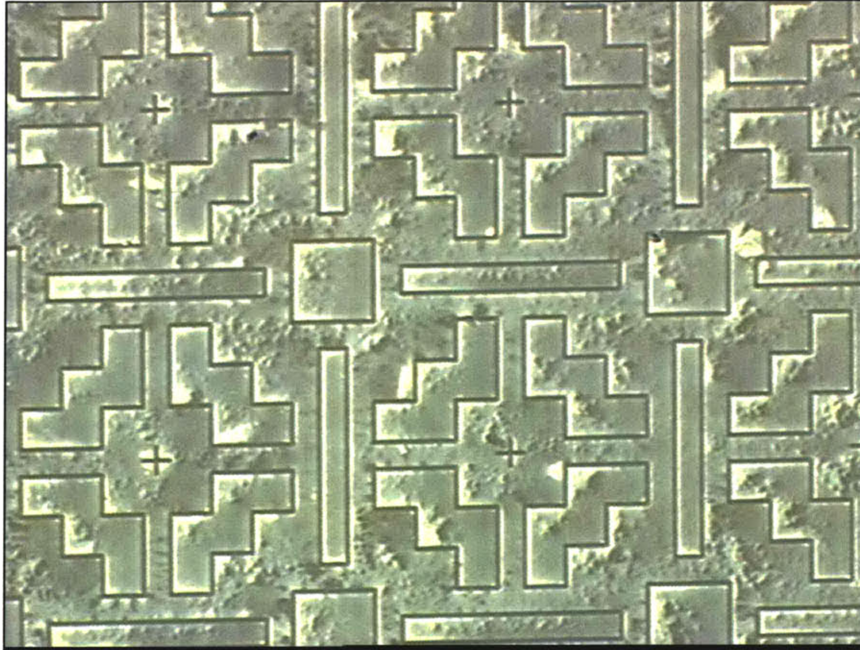

Figure 024: Zoomed in view of 1μm CdSe features. This image shows the ability of liquid embossing to move solid agglomerates as well as pure liquids.

Atomic Force Microscope (AFM) images of the patterned features illustrate several other important points. Fig. 025 shows 3μm Au features which are long interdigitated fingers. The edges of the features are slightly thicker due to the excess material that was pushed away by the embossing stamp. This is especially visible at the tips of the fingers where a large amount of excess material was pushed. Fig. 026 shows similar features fabricated in Au but with 1μm spacing instead of 3μm. In these features the 1μm wide fingers are thin enough that there is no variation between their edges and their centers. The triangular profile of the fingers and the rounded corners are both artifacts of the MTL photolithography process which created the original silicon master. Fig. 027 is a cross-sectional view of the AFM in Fig. 026. The fingers have a triangular profile which is 1μm wide and 100nm tall. There is a height difference between the two different sets of interdigitated fingers, and this is probably due to the fact that the taller features have a direct liquid connection to the large region which is in the lower-left of the AFM image, (although it may also be an artifact of the MTL photolithography). These slight variations in liquid height could pose a problem for making features with exact resistances, (although the variations are quite uniform, and therefore possibly predictable.) Another important feature of the cross-sectional view is that the region between metallic lines is completely flat, indicating that the region has been completely cleared of any material.

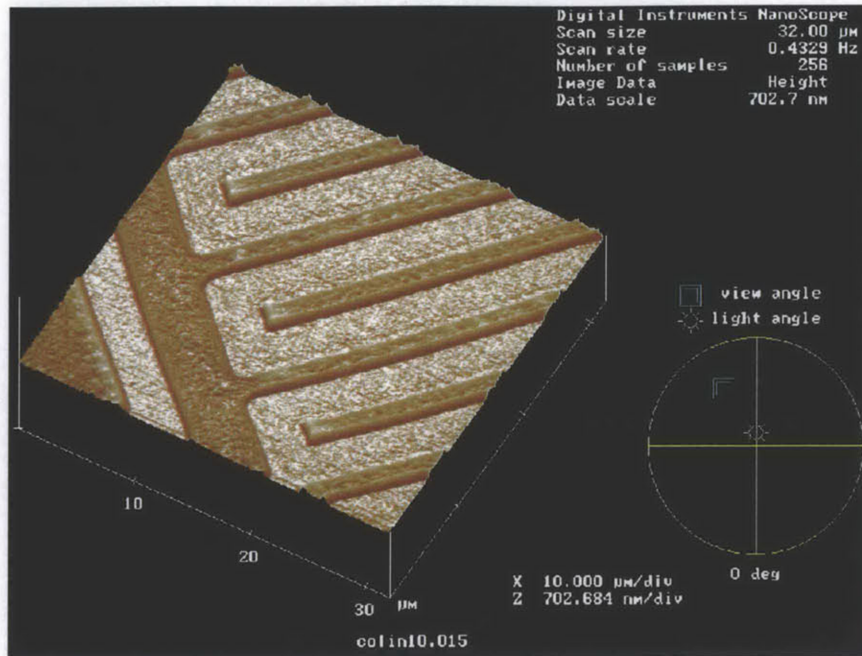

Figure 025: AFM image of 3µm Au features.

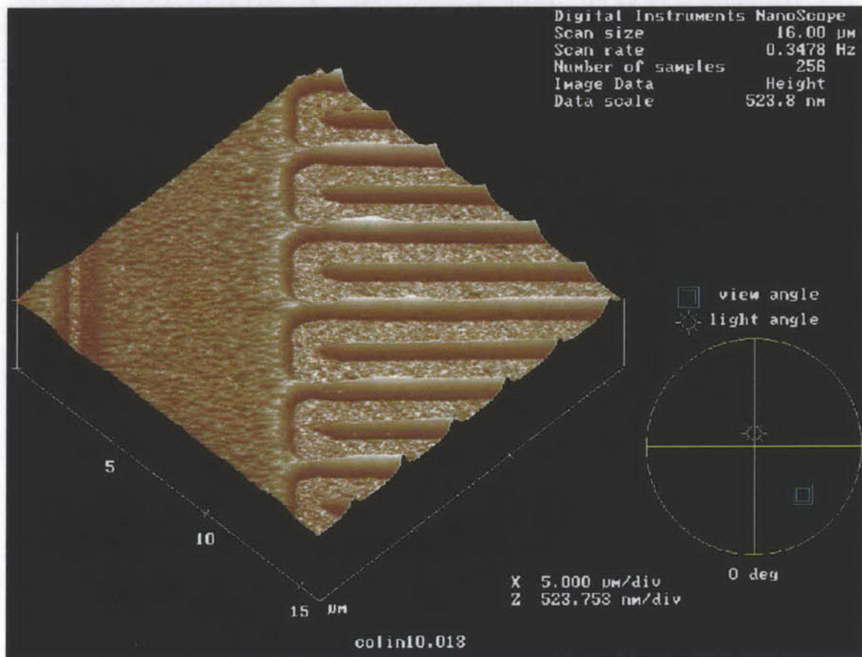

Figure 026: AFM image of 1µm Au features.

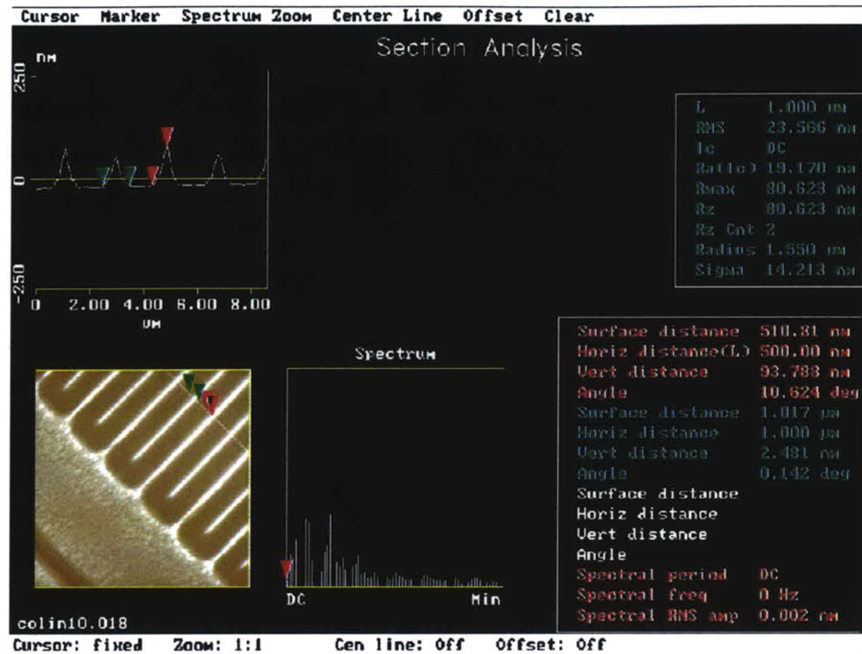

Figure 027: Cross-sectional view of an AFM of 1µm Au features.

The MTL facilities are suitable for fabricating silicon masters with features greater than 1µm. Unfortunately, it is difficult to use the facilities to pattern anything smaller than 1µm so I therefore sent out my sub-micron patterns to a company named FIB International. Using a focused ion beam (FIB) they were able to carve out the patterns in a silicon wafer with 10nm accuracy. I only made a few patterns with these masters and there were some extraneous problems, but the results were still promising. In Figs. 028-029 I patterned 500nm interdigitated features similar to the 1µm features shown in Fig. 026. The liquid surface got covered in dust prior to embossing so the fabricated device was unusable, but the features in the areas that were free of dust appeared quite sharp. In the far right line in Fig. 029 you can see the subtle waviness that was caused by the FIB and which was replicated directly by the liquid embossing process. Fig. 030 shows a different structure with 500nm features created by the FIB and then patterned by liquid embossing. In this case the PDMS stamp was removed from the silicon master too early and it left behind pieces of PDMS attached to the wafer. The imperfections in the PDMS stamp were then replicated directly in the 500nm Au features.

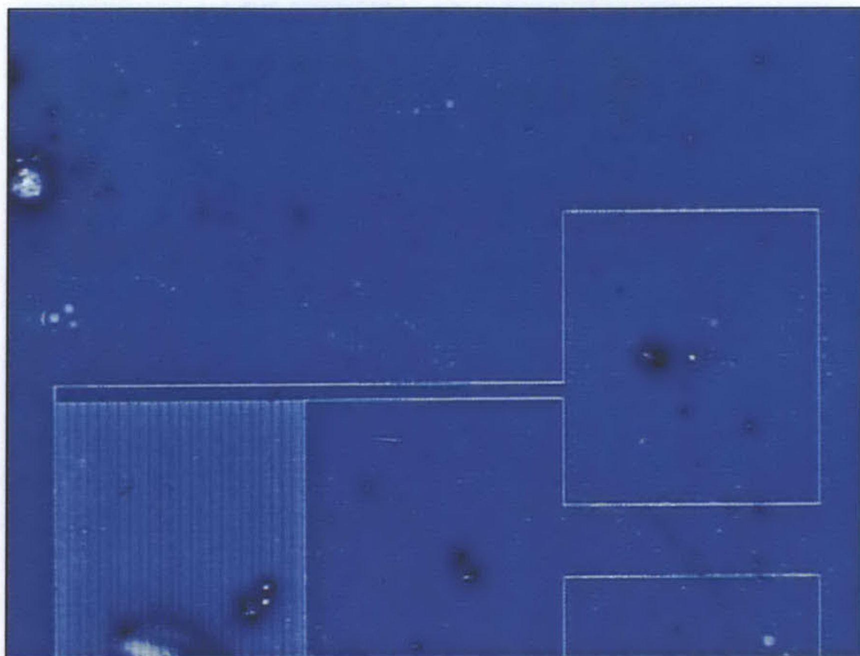

Figure 028: Optical image of 500nm features fabricated in Au.

Figure 029: Zoomed-in view of 500nm features fabricated in Au.

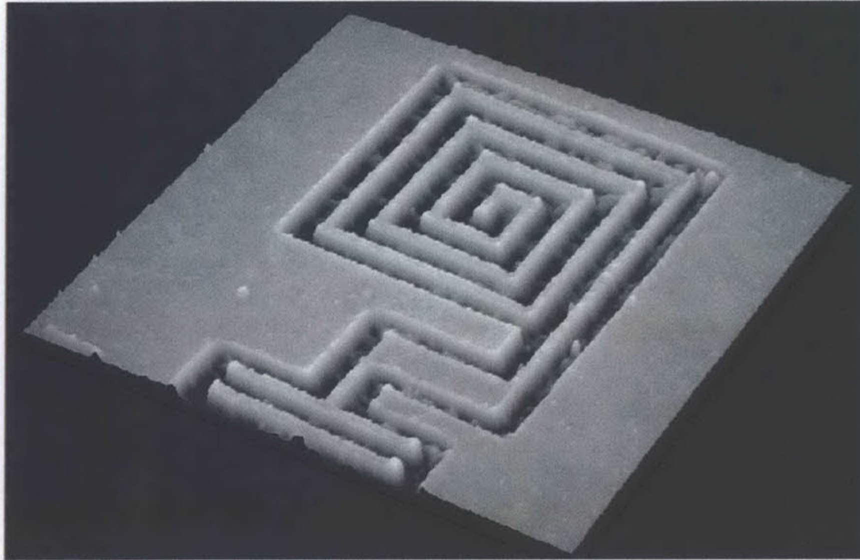

Figure 030: AFM image of 500nm Au features patterned by a damaged stamp.

The patterning process has improved significantly since the first early patterns were made. Figs. 031-033 show some typical current patterns with uniform film thickness, very sharp features, and flexibility.

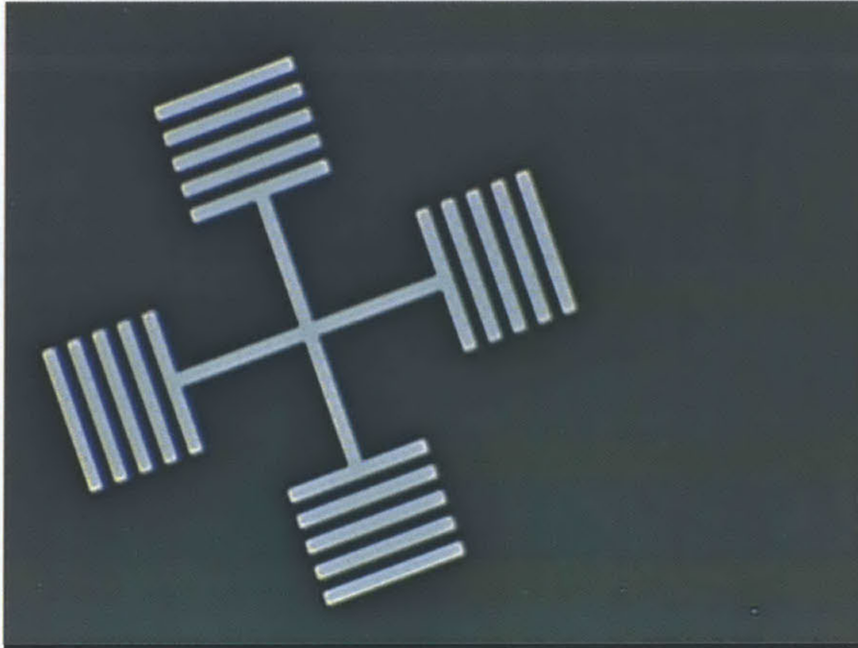

Figure 031: Optical image of 5µm Ag features.

Figure 032: Optical image of 5μm Ag features.

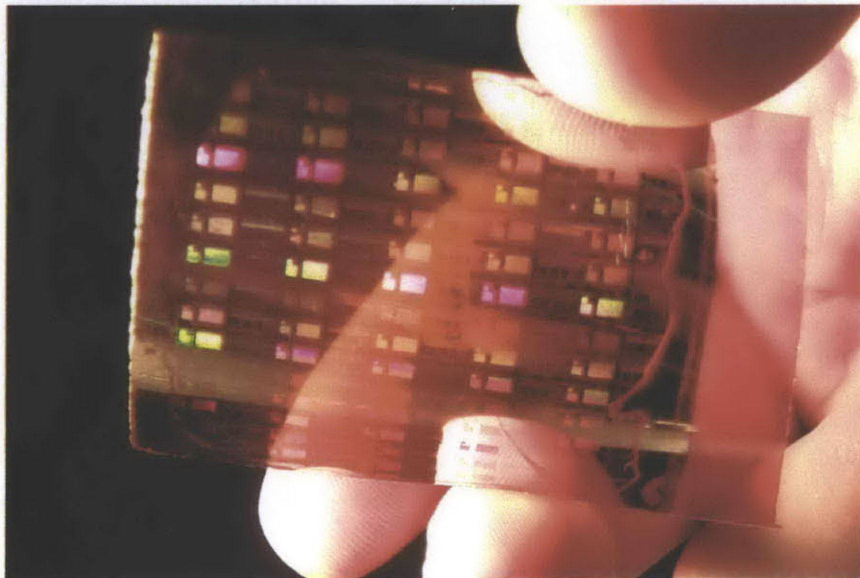

Figure 033: Zoomed-out view of 1μm Au features patterned on flexible polyimide.

3.3 Resistors

After verifying that liquid embossing was capable of patterning arbitrary non-trivial patterns, the next thing to characterize was the quality of the materials that were being patterned. I included long resistor structures on the first mask in order to measure the conductivity of the metallic films that I was patterning. These resistors were thin very long wires that snaked back and forth between large contact pads, (Fig. 034). I created resistors that snaked back and forth 1, 3, and 9 times, and these corresponded with wire lengths of 6, 12, and 30mm. The width of the metal lines was either 1, 3, or 5μm. For the longest, thinnest resistor (1μm wide by 30mm long) this corresponded to a length:width aspect ratio of 30,000 to 1. These very fine resolution resistors snaked back and forth over large areas with zero defects, (Fig. 035).

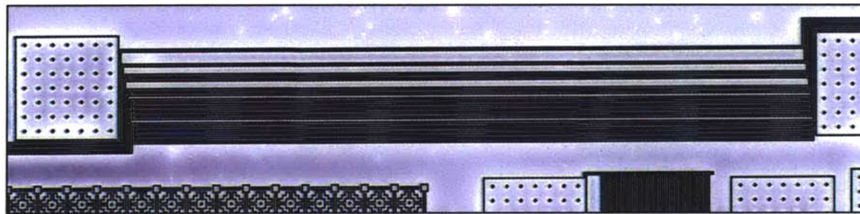

Figure 034: Optical image of serpentine resistors. The size of the device in this image is 4mm.

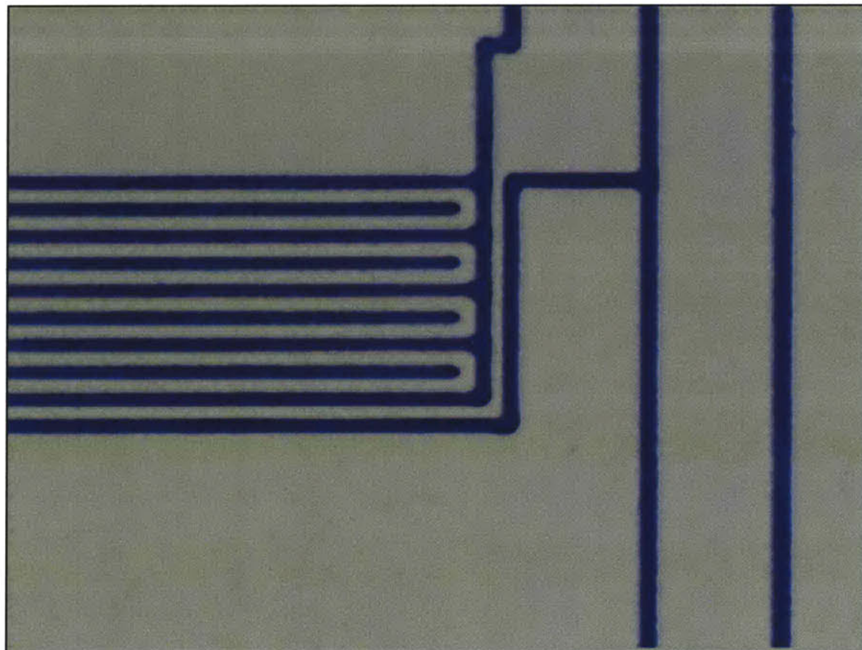

Figure 035: Zoomed in view of 1μm Au resistor features. There were zero patterning defects over the entire length of these resistors (30mm).

By measuring the resistance (R) of these long thin wires a value for the resistivity (ρ) of the metallic material could be calculated. AFM images of the resistors were used to determine the width and height of the thin metal lines, (Fig. 036). Looking at one particular 30mm long resistor, the average half-height width was found to be 3.75μm with an average height of 160nm. The measured resistance was 4.16 kΩ. Plugging into the equation $\rho = Rhw/l$, the value for ρ was calculated to be 8.32×10^{-6} Ω-cm, with a standard deviation of 5×10^{-7} Ω-cm among the 6 devices tested. This value is roughly a factor of four higher than that of bulk Au (2.04×10^{-6} Ω-cm). In later experiments I found that by heating the material above 300° C it was possible to further densify the material and thus decrease the resistivity. For almost all applications that I was interested in though, a factor of four within the bulk resistivity was perfectly acceptable.

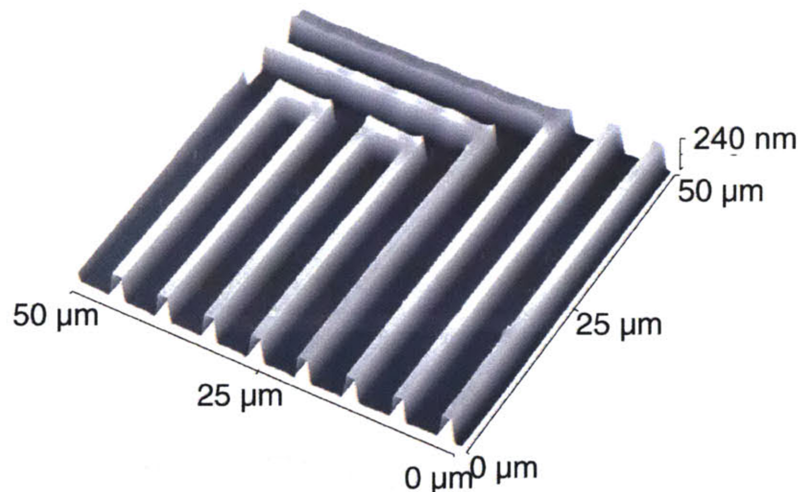

Figure 036: AFM image of 3μm Au resistor features. The data from these AFM images were used to calculate the resistivity (ρ) of the Au nanocrystalline material.

By comparing the resistances of different lengths of resistors scattered across different regions of the embossed pattern it was possible to determine the uniformity of the metallic film. As can be seen in Fig. 037, the resistance of the thin metal lines was in perfect agreement with their linear length even for features that were significantly separated from each other. Another important point is that the resistance did not change in relation to the number of times that the resistor snaked indicating that there was no conductance across the channel. The resistance between the thin metal lines and the surrounding metal was greater than 20 GΩ, (the maximum that our equipment could detect.)

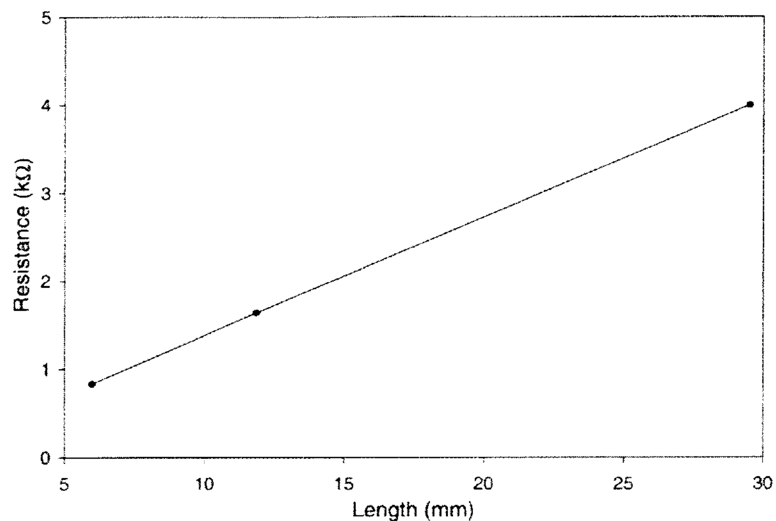

Figure 037: Curve comparing the resistance of thin metal lines vs. their length. The linear agreement shows that there is very good material uniformity over the entire patterned metal film.

3.4 Field Emission Displays

In collaboration with Motorola I began a project to use liquid embossing to create structures for Field Emission Displays (FED). Fig. 038 shows a schematic for how a conventional FED is fabricated. The FED is turned on by applying a large voltage (~100V) between the Cathode and the Anode. Electrons stream from the spindt-tip on the anode and are accelerated before colliding with the cathode and thus interacting with a fluorescent material to create light. In order to turn off this stream of electrons a voltage is applied to the gate which causes the electrons leaving the spindt-tip to go to the gate rather than the cathode. The work function of the spindt-tip is much lower than the work function of the gate so although electrons will stream from the anode to the cathode they will not stream from the gate. Fig. 039 shows a conventional spindt-tip which has been fabricated in Professor Henry Smith's Nanostructures Research Laboratory at MIT.

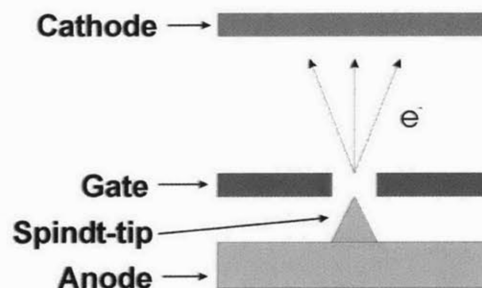

Figure 038: Schematic for a conventionally fabricated FED.

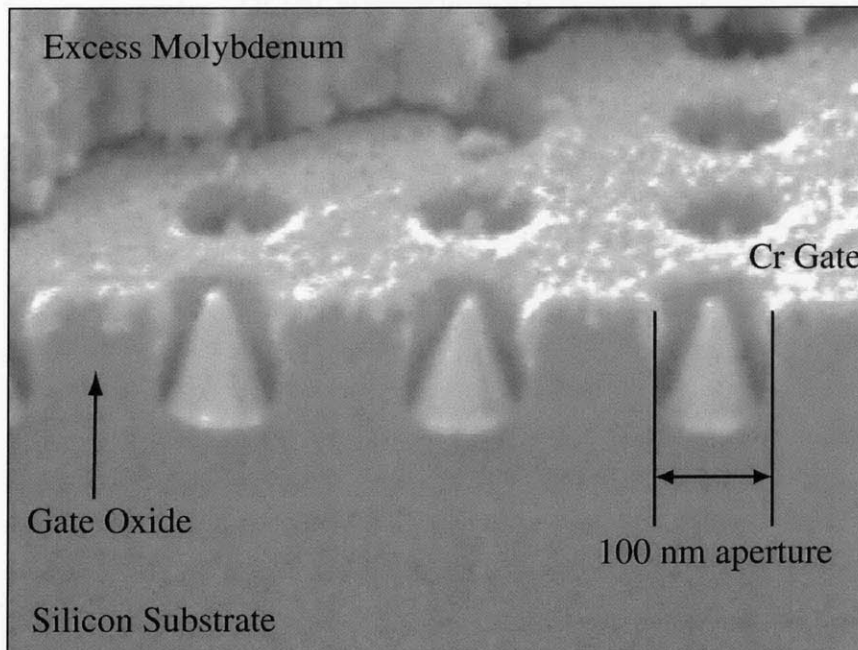

Figure 039: SEM image of conventionally fabricated FED spindt-tips.

[Photo courtesy of Prof. Henry Smith at MIT]

Although conventional FEDs have several very nice properties, their one main disadvantage is their cost. The spindt-tip is a very complex and expensive structure to fabricate, especially when you need to create them over areas greater than 100 square inches. An interesting alternative to spindt-tips are carbon nanotubes. Carbon nanotubes have a naturally low work-function and thus they could be a direct replacement for the current spindt-tips. In addition, an alternative architecture which used interdigitated electrodes would have higher density than the current 0-dimensional spindt-tips, and would also be easier to fabricate than the multilayer conventional architecture.

Fig. 040 shows a schematic for this alternative architecture, and Fig. 041 shows an overhead view of the design. The basic idea is that one set of the interdigitated fingers have exposed nanotubes and act as the anodes, the other set of fingers have gold covering their nanotubes and thus can act as a gate. A top cathode is attached after the features have been patterned. These structures can be fabricated by a simple two layer embossing step, but for now I will concentrate on just the first layer, (multi-layer patterning is discussed in Section 3.5).

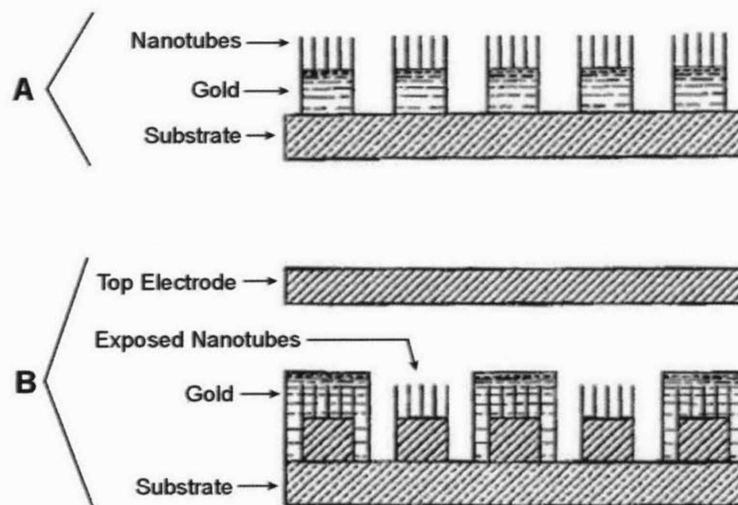

Figure 040: Schematic for alternative FED structure created by liquid embossing. Part A shows a first layer of Au and nanotubes patterned to create separate interdigitated wires. Part B shows a second layer of Au applied to reduce the work function of one set of the interdigitated wires, and a top electrode attached to the structure.

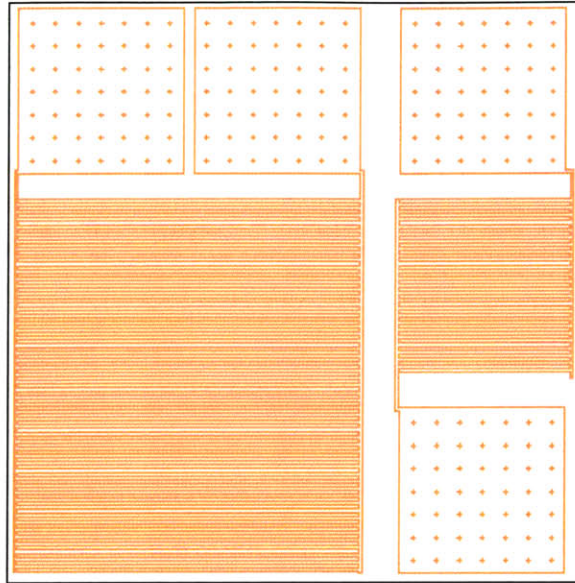

Figure 041: Overhead view of mask design of interdigitated fingers for FED displays. The white areas are Au, and the colored areas correspond to areas where there is no Au.

I fabricated several different versions of these single-layer FED structures, the largest of which was a pixel 2mm x 1.5mm. I also created the structures at three different resolutions: 1µm, 3µm, and 5µm. Fig. 042 shows an optical image of one of these structures. You can see the high consistency of the patterned metal lines. Fig. 043 shows a further zoomed in view of a structure with 5µm features. By probing the device it was possible to verify that the metal lines were all conducting, and that the two sets of interdigitated features were electrically isolated from each other. This is a very important result. It demonstrates that liquid embossing can pattern large areas, 2mm x 1.5mm, with absolutely zero defects. For the devices that were composed of 1µm wide wires this is particularly impressive since each FED structure had 1000 interdigitated wires, and each of these wires were 1.5mm long. This corresponds to 1.5 meters of wiring which is spaced 1µm apart with absolutely no conductivity between the two wires.

Unfortunately, Motorola's FED effort was cancelled so I never built any devices with more than one layer. The FED structures were still useful benchmarks and the technique of integrating nanotubes with Au proved useful when making transistors, (as discussed in Section 3.9).

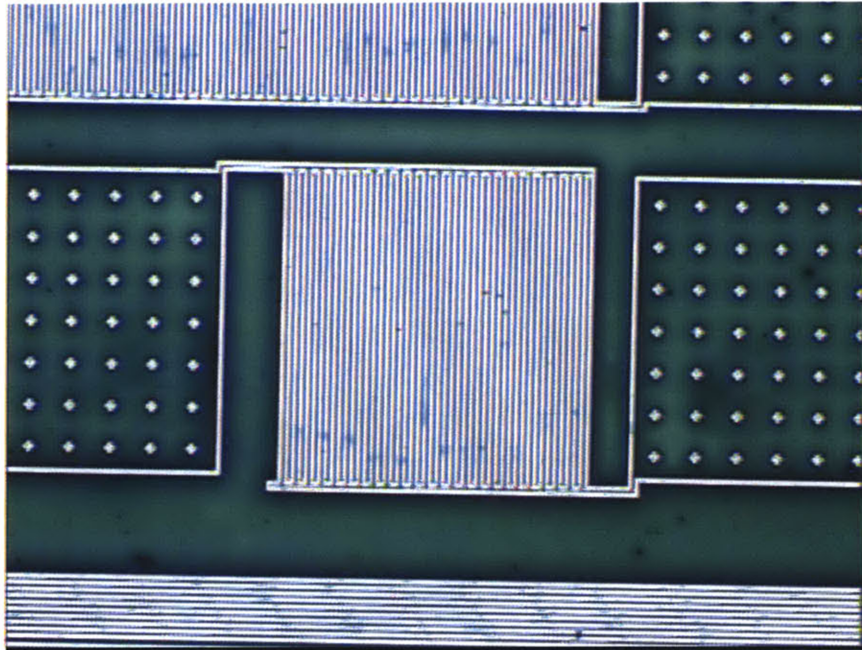

Figure 042: Optical image of an interdigitated FED structure with 5µm Au features.

Figure 043: Zoomed-in view of 5µm Au features.

3.5 Multiple Layers

One of the biggest problems with other non-lithographic patterning techniques – such as NIL or micro contact printing – is the fact that they cannot easily pattern multiple layers of material. One of the biggest advantages of liquid embossing is the fact that patterning multiple layers of material is as easy as patterning a single layer.

The PDMS stamp that does the embossing is highly conformal. It has been demonstrated by the Whitesides group at Harvard that a PDMS stamp can make conformal contact with a substrate that has variations of up to 45°. Given that the wetting angle for most of the materials that I am patterning is less than 45° this implies that it should be possible for the PDMS stamp to make conformal contact with a previously patterned layer of material. In addition, during liquid embossing the recessed features of the stamp do not touch-down, so height variations should make no difference to the quality of the patterning. Figs. 044-045 show schematic representations of this conformal patterning. Fig. 044 shows features being patterned at different heights, and Fig. 045 shows the formation of a via hole. These techniques are powerful because they can pattern multiple layers without the need for expensive and complicated planarization, polishing, and etch steps.

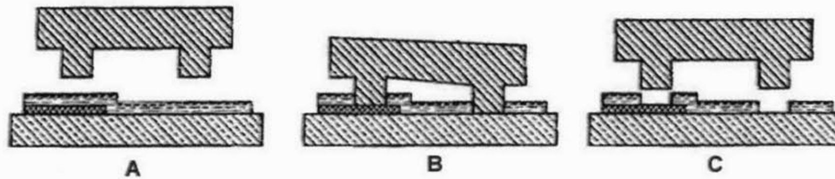

Figure 044: Schematic of multi-layer embossing. **a)** A thin film of liquid is formed on top of existing solid patterns. **b)** The PDMS stamp is brought into conformal contact with the underlying layers of material. **c)** The stamp is removed and the material can then be cured and the process repeated.

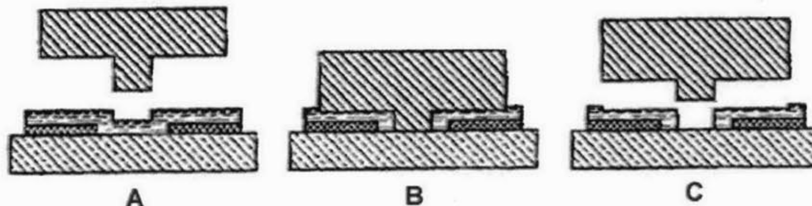

Figure 045: Schematic of multi-layer embossing of a via hole. **a)** A thin film of liquid is formed on top of the previous patterns. **b)** The stamp is brought into conformal contact with the underlying layers. The stamp makes contact with the underlying substrate, and the recessed features of the stamp make contact with the top layer of the liquid. **c)** The stamp is removed and the via hole has been patterned.

Early on I explored a different technique for fabricating multi-layer structures which I will mention briefly. If the PDMS stamp is brought into contact with a very thick layer of liquid it will remove some of the liquid when it is lifted off. This stamp can then be applied to a second substrate and the material on the raised features will be transferred. This technique is identical to the macro scale technique of rubber stamp printing. Unfortunately, at the micro scale the process is very unreliable and the transferred patterns often have a large number of defects. When I was first exploring multi-layer patterning I tried using the transfer technique to pattern a second layer of material on top of a previously embossed first layer. The resulting log-cabin structures had a number of defects, but they still looked good over small areas, (Fig. 046).

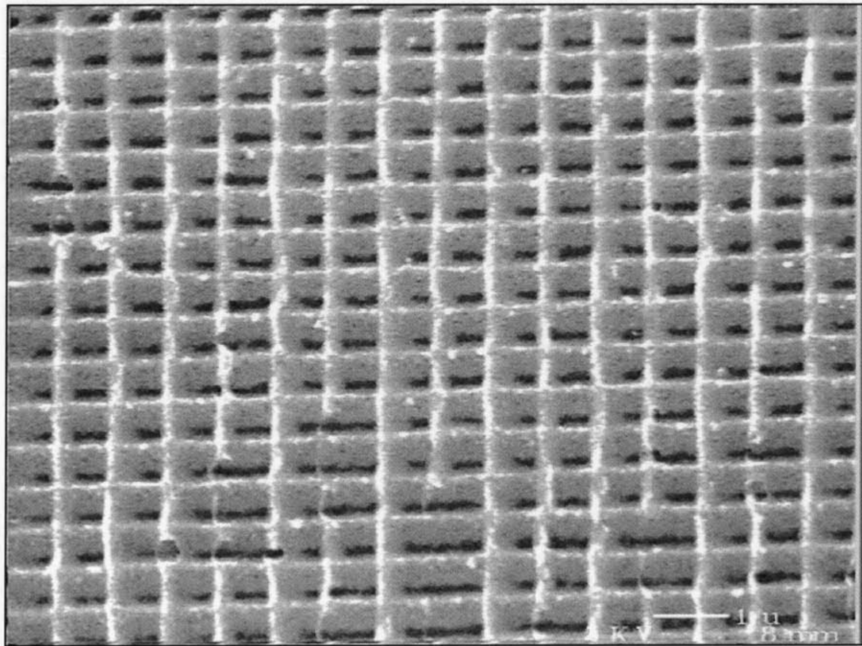

Figure 046: SEM image of a log-cabin structure fabricated in Au with 800nm features. The top layer was created by transferring material in a rubber-stamp fashion.

AFM images of the log-cabin structures though revealed that the top layer followed the contour of the underlying layer so the structure was not a true log-cabin since there were no freely supported features, (Fig. 047). The cross section of the AFM image also showed that the underlying embossed layer had a very regular cross section with no excess material in the areas between lines, even after the second layer of material was transferred, (Fig. 048).

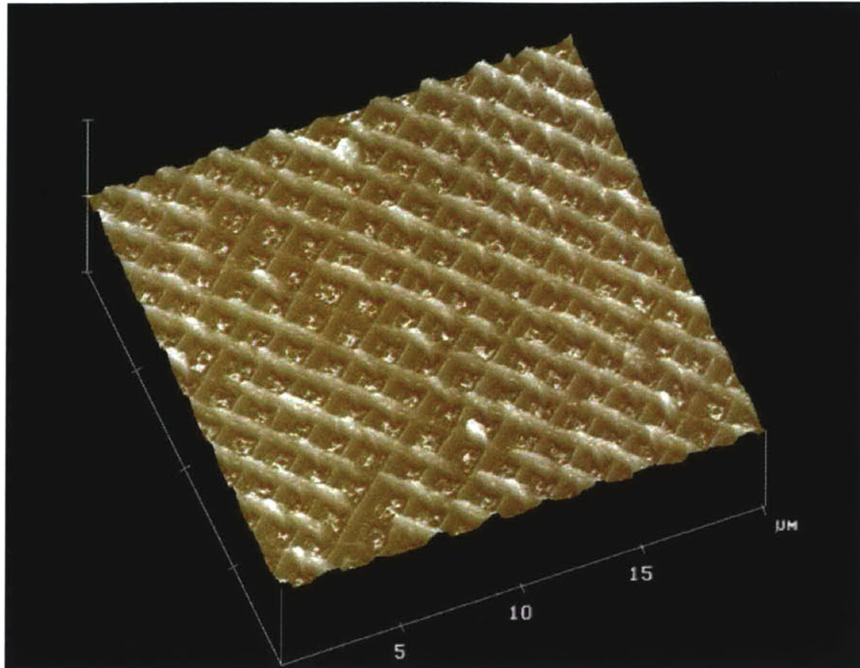

Figure 047: AFM image of log-cabin structure created by transferring a second layer of material onto a previously embossed layer.

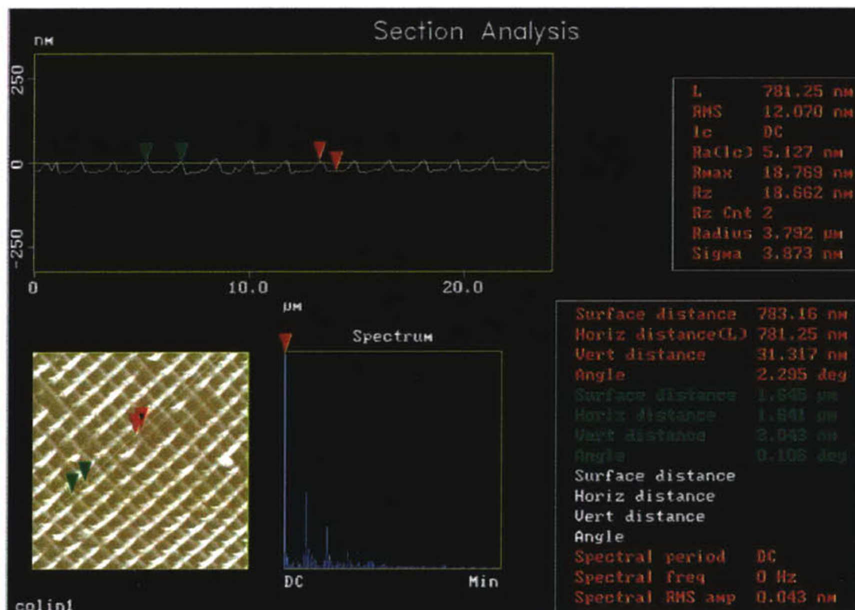

Figure 048: Cross-section of AFM of log-cabin structure.

After it became obvious that the transfer technique would never be reliable, I switched entirely to the embossing technique for patterning multiple layers of material. I created grid patterns by embossing a first grating structure, and then embossing a second grating on top of and perpendicular to the first. SEM images of these structures showed that the patterns of both

layers were quite sharp, (Fig. 049). There was no reason why the process should be limited to two layers, so I proceeded to create hexagonal grids with three layers of gratings oriented 60° apart from each other. Optical images of these gratings showed great regularity over large areas, (Fig. 050,) and it was possible to shine a laser through the grating and see a beautiful hexagonally oriented diffraction pattern. An AFM image of this hexagonal grid, (Fig. 051,) shows that the 2nd and 3rd layer gratings are conformal to the underlying layers. In addition, this AFM also shows the very important result that the areas where the three gratings intersect are completely cleared of material. Whenever a new layer is patterned a thin film of liquid is deposited everywhere and the PDMS stamp can emboss through this liquid and make conformal contact with the underlying substrate even over the roughness of the previously patterned features. Another example of this multi-layer patterning can be seen in Fig. 052 where three different gratings were used to make a hexagonal pattern. The features of each layer are very sharp, and the intersecting regions remain totally cleared of excess material.

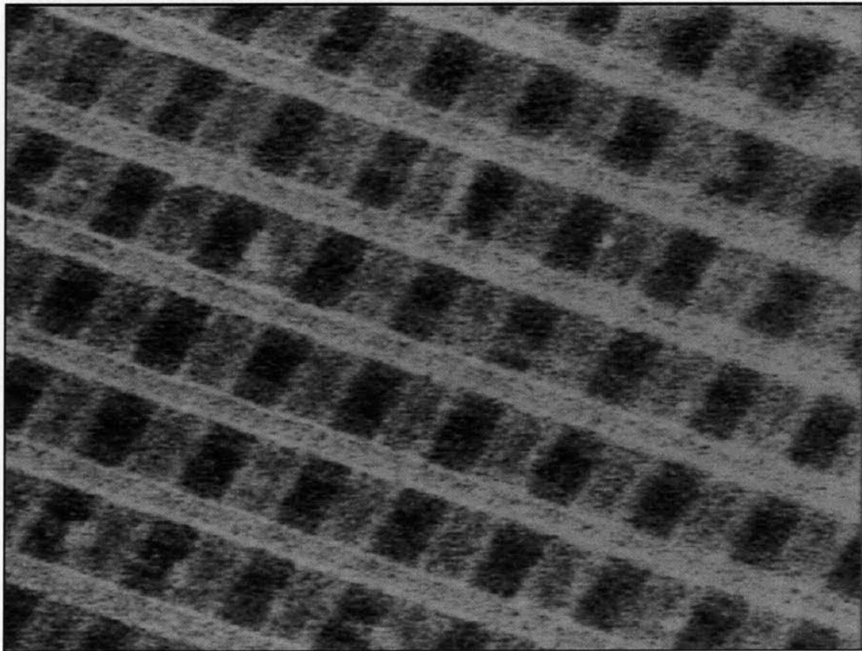

Figure 049: SEM image of a grid structure produced by embossing a second grating structure on top of a first grating. The periodicties for the two gratings were 1.6μm and 1.2μm.

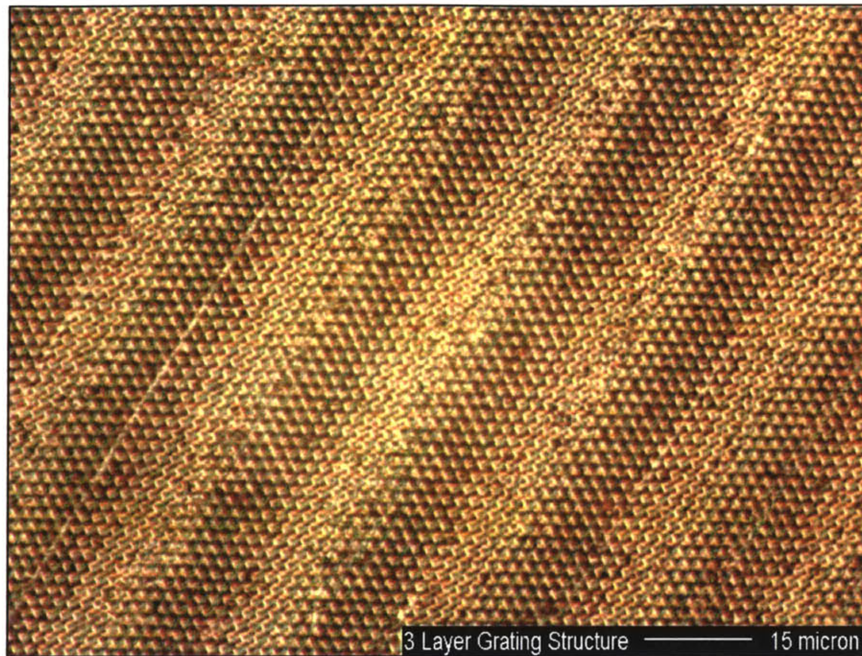

Figure 050: Optical image of 3-layer hexagonal grid structure fabricated by embossing three grating patterns on top of each other and oriented 60° apart.

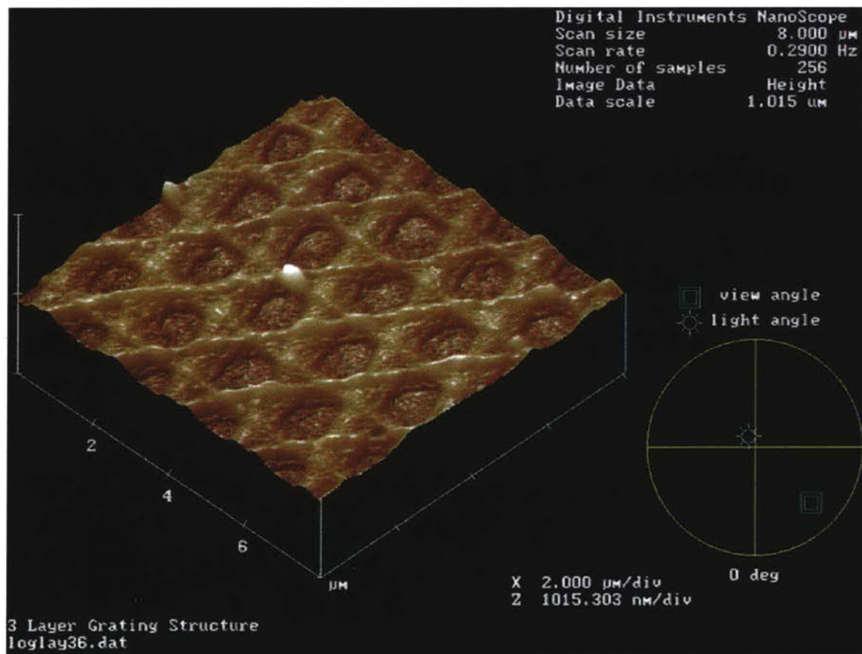

Figure 051: AFM image of 3-layer hexagonal grid. The hexagonal areas where the three gratings intersect have been completely cleared of all material, leaving only the exposed substrate.

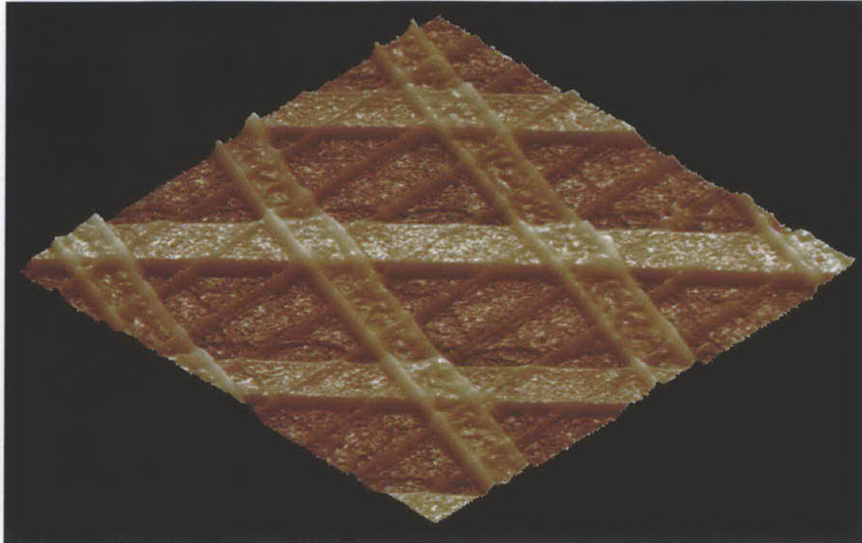

Figure 052: AFM image of 3-layer hexagonal grid. The first and third layer gratings had a periodicity of 3μm and the second layer had a periodicity of 1μm.

After patterning grid structures, I moved on to pattern more complicated multi-layer structures. Fig. 053 shows an optical image of two layers of 15μm x 15μm squares patterned on top of each other. The squares are perfectly intact, and if you zoom out you can see that the field of overlapping squares extends for millimeters on a side. The transmission mode optical image in Fig. 054 shows that there are small white squares where the negative features of the two layers intersect. These white squares correspond with regions where all material has been removed and the underlying substrate has been exposed. An AFM image of the overlapping squares, (Fig. 055,) shows that the top layer of squares is completely conformal with the bottom layer. In fact, the two layers are so conformal that it is often difficult to tell which layer was patterned first. The AFM also shows that the material has been completely removed from the regions that correspond with the small white squares in the transmission mode image.

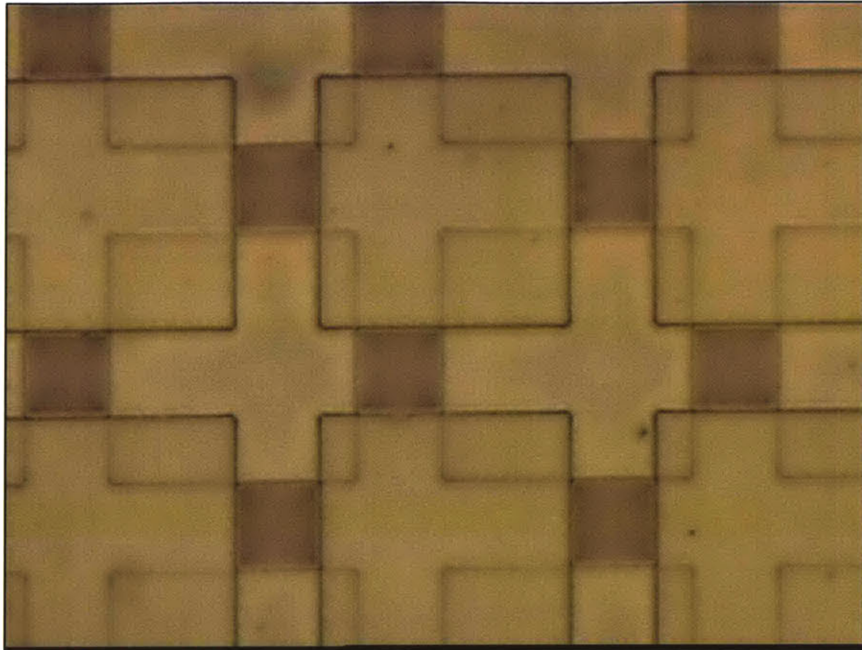

Figure 053: Optical image of two layers of overlapping 15μm x 15μm Au squares.

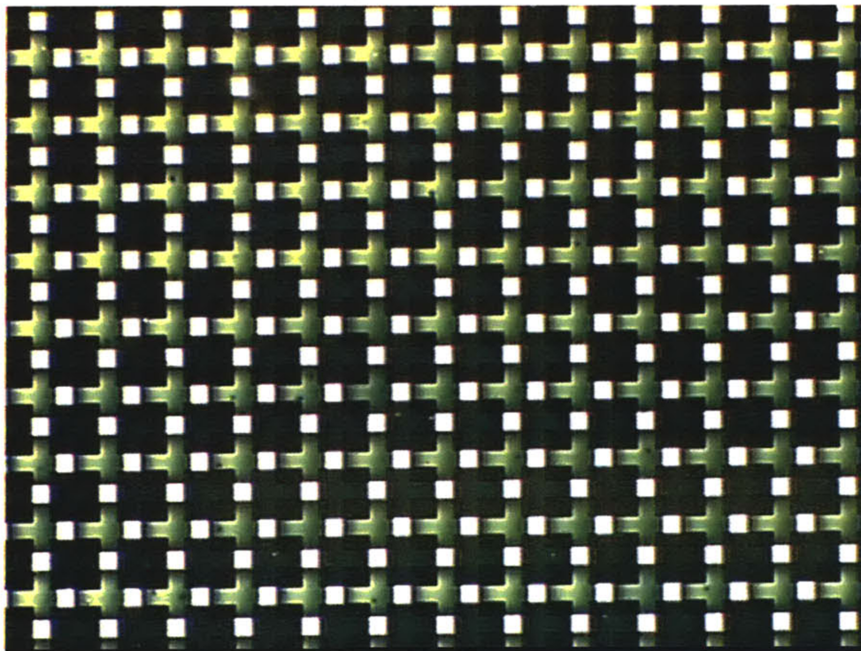

Figure 054: Zoomed-out transmission mode image of overlapping squares.

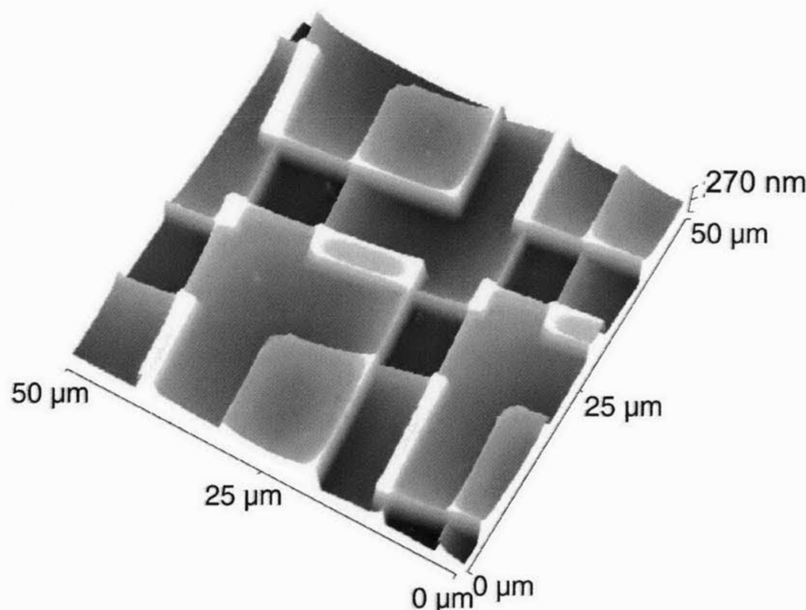

Figure 055: AFM image of overlapping 15µm x 15µm Au squares.

Another interesting multi-layer structure that I fabricated is shown in Fig. 056. This structure is similar to the overlapping gratings that were shown earlier, but there are some important differences. The gratings have a triangular profile with a small height:width ratio. This limits the maximum thickness of the thin films that the gratings can pattern to about 100nm. The stamps that were fabricated on silicon masters, on the other hand, have much deeper recessed features and thus they can pattern much thicker films of liquid, (100-700nm). In the structure shown in Fig. 056, films 300nm thick were patterned. These thicker films had the surprising result of decreasing the amount of surface roughness in the top layer of material. Although the raised features of the stamp are conformal to the underlying substrate, the liquid film being patterned tends to be planar. This means that the top of a film of liquid will have less surface roughness than the features on which it is being patterned. Effectively, each time another layer of material is put down the top of the structure becomes more planar.

This is demonstrated in an AFM of the structure, (Fig. 057.) Prior to the second layer being patterned the structure had a certain roughness that was created by the grating pattern. When the second layer was put down it created perpendicular surface roughness, but at the same time it also decreased the surface roughness caused by the first layer. This can be seen if you compare the roughness of the top of the top grating with the roughness of the underlying layer. The top layer has effectively increased the planarization of the entire structure. It is for this reason that I claim that liquid embossing is a self-planarizing process. The more layers that are put down the more planar the overall structure will become. Admittedly, there are certain patterns

that will become less planar over time, but in general, liquid embossing appears to be uniquely capable of creating structures with a very large number of layers.

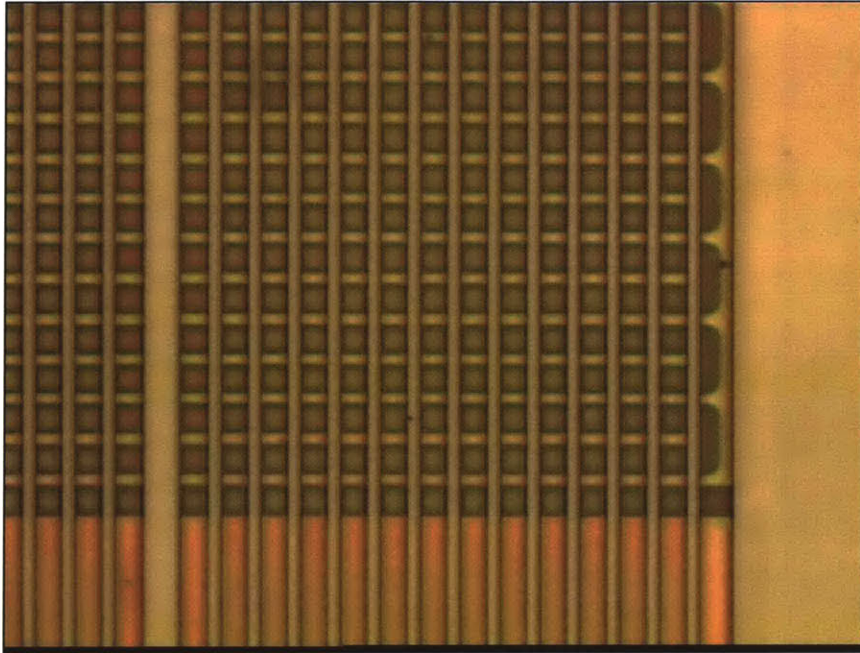

Figure 056: Optical image of overlapping 5µm wide lines.

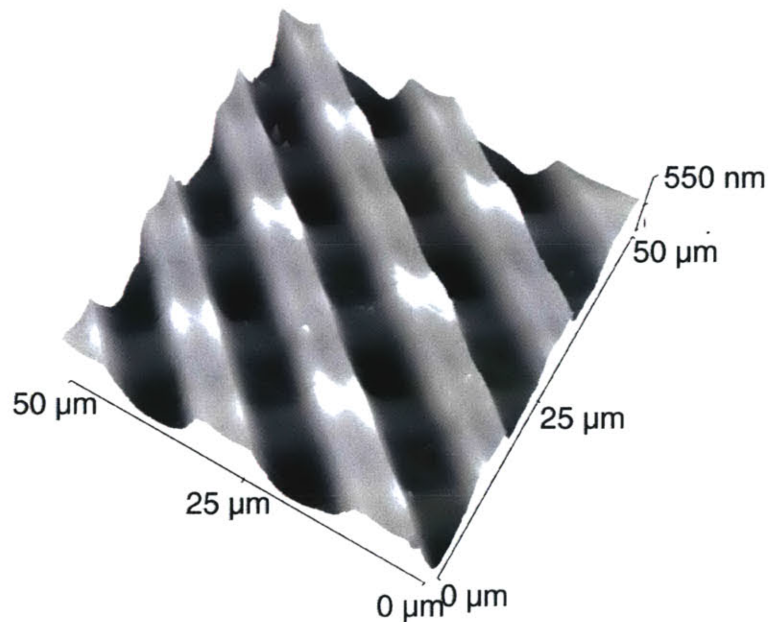

Figure 057: AFM image of overlapping 5µm wide lines. The top of the top layer is more planar than the previously patterned features.

3.6 Alignment

In order to make interesting multi-layer structures, I needed to develop a technique for aligning multiple layers with each other. Since the stamp was clear, the obvious solution was to use an optics system with alignment marks on the stamp and on the patterned substrate. There was one non-obvious trick that I employed though. Rather than using a separate stamp for each layer of a structure, I instead included each layer on a single stamp and spatially separated them, (Fig. 058). In this way I could guarantee, (based on the precision of the tools which were used to make the silicon master,) that each layer would be precisely offset from each other layer with less than 100nm of error. By including each layer in the same stamp I also removed the need to do rotational alignment, since each layer was oriented in the same direction. And finally, it was much easier to build a mechanism which used a single stamp rather than multiple stamps.

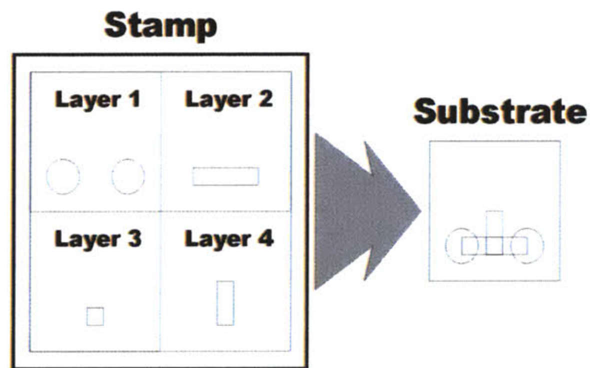

Figure 058: Schematic for including multiple layers in the same stamp but spatially separated.

I wrote a script which took my Ledit multi-layer masks and filtered them into a single layer mask with each layer spatially separated. Each layer had several alignment marks which were used to optically align that layer with the other layers. An example of a typical alignment mark prior to being spatially separated can be seen in Fig. 059.

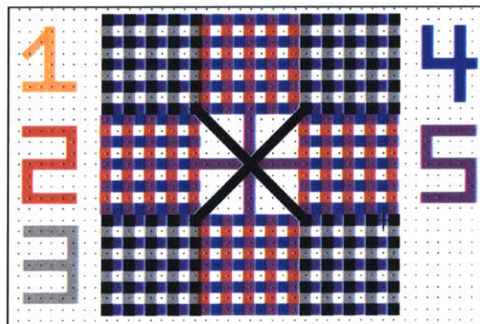

Figure 059: Mask image of a typical multi-layer alignment mark. Each color corresponds to a different layer.

I theorized that even without optical alignment it should be possible to get crude alignment by simply moving the stamp the appropriate amount on a precision stage and then stamping blindly. The technique was marginally successful and it would typically give me alignment to within 40μm, although occasionally I would get lucky and get 5μm alignment, (Fig. 060). Even though the technique didn't give perfect alignment, it did get the stamp close enough to the correct position that it was very easy to do quick optical alignment.

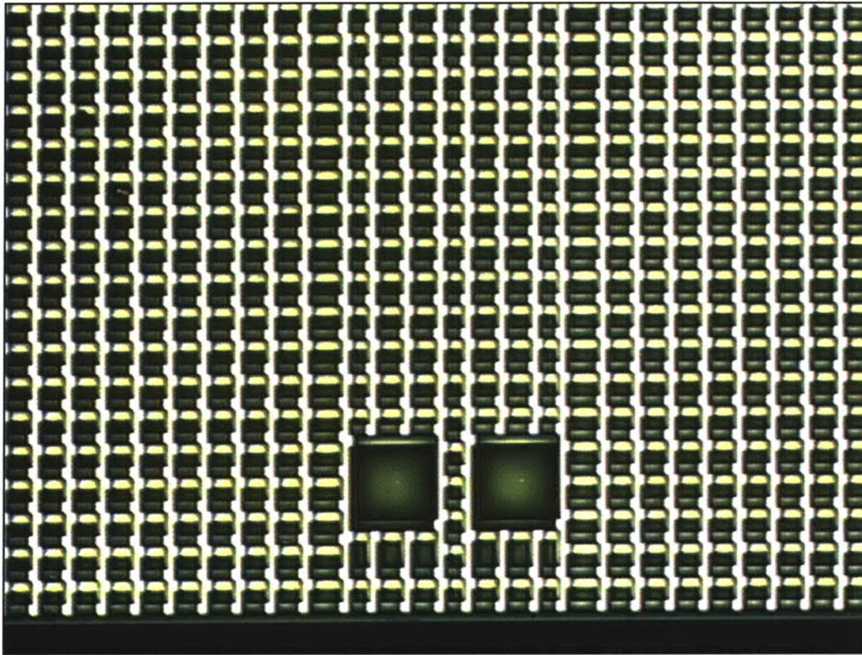

Figure 060: Multi-layer structure demonstrating alignment to within 5μm without the use of optical feedback.

With the use of optical feedback I was able to get my alignment to within 5μm all the time, and typically to within 2μm, (Figs. 061-062.) The main limitations in improving the alignment beyond 2μm were the optics system that I was using. With greater magnification it should be possible to push the alignment to within less than 1μm. Fig. 063 shows three still images taken right before, during, and after the contact of the stamp with the previously patterned film. These images clearly show the alignment mark on the stamp lining up with the alignment mark on the substrate.

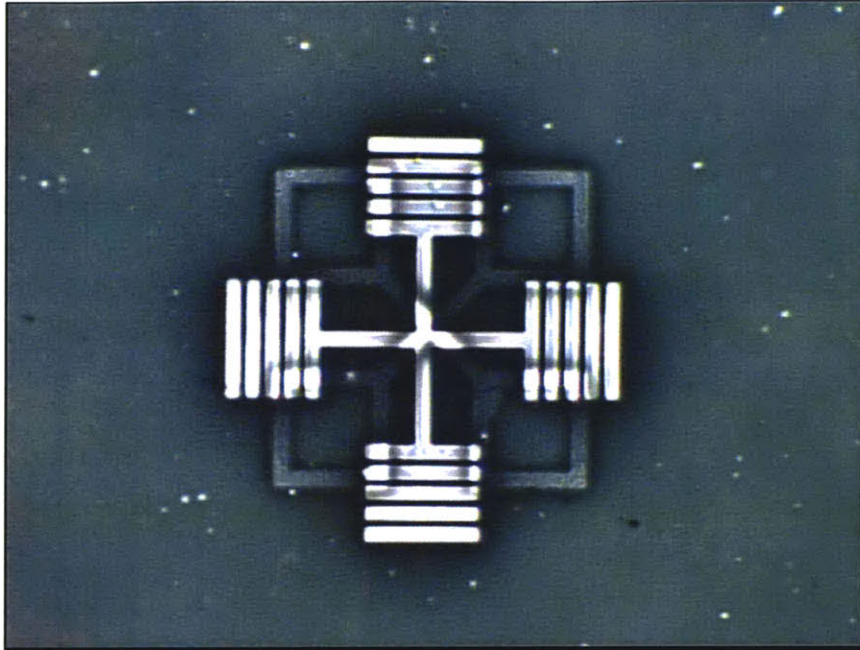

Figure 061: Optical image of 2 layers of alignment marks aligned to within 5µm.

Figure 062: Optical image of 4 layers of alignment marks aligned to within 2µm.

Figure 063: Three optical images showing the alignment mark of the stamp coming into contact with the liquid and the previously patterned metal film. (Time proceeds from left to right.)

3.7 Insulators

In previous sections all of the materials that I discussed patterning were metallic or semiconducting nanocrystalline colloids. In this section I will present a collection of insulating materials that I have used to fabricate capacitors and other electrically isolated structures.

I considered a collection of six different materials as insulator candidates:

- Inkjet Coding Ink provided by ABM Marking Ltd, (IJI).
- AL 3046 polyimide provided by Japanese Synthetic Rubber (JSR).
- Pyralin Polyimide provided by Dupont (Pyralin).
- T-7 high-polymer spin-on glass provided by Tokyo Ohko Kogyo Co. Ltd. (T7).
- 21F low-polymer spin-on glass provided by Filmtronics (21F).
- 500FX high-polymer spin-on glass provided by Filmtronics (500FX).

I conducted an initial test of each of these six materials to determine their insulating abilities and their ability to wet various substrates. I took a conducting p-type wafer and spun down a small portion of each of the six materials around the edge of the wafer, (Fig. 064.) From this experiment I could determine whether the materials wetted to the silicon substrate. I then cured the materials at either 200° C or 350° C for 10 minutes. I spun down a small amount of Ag nanocrystals on top of each of the six insulators and noted whether the Ag would wet to the cured insulator. I cured the wafer at 350° C for 10 minutes to sinter the Ag.

I could then probe each of the six samples to determine whether they had successfully insulated the Ag from the underlying silicon wafer. I also tested the material to see if it would still insulate if there was significant pressure applied to the probe tip. This was important to know since I would later be probing my devices in a probe station and I wanted to determine the robustness of the insulating layer. The results of these test can be seen in Fig. 065. The final column, 'Still Wet After Spin?', indicates whether the material was still a liquid after spincoating or if all of the solvent had evaporated away. The 500FX material failed since it was unable to wet the silicon surface and the Ag failed to wet it. The JSR was also unusable since it completely failed to insulate the Ag from the underlying silicon. The prime candidates seemed to be either the T7, the IJI cured at high temperature, the Pyralin, or the 21F. The T7 and the IJI both dried out very quickly so I did a solvent exchange with α-terpineol to increase their boiling point and keep them liquid longer. One other thing to note is that the glass-based materials were more robust than the polymer based materials.

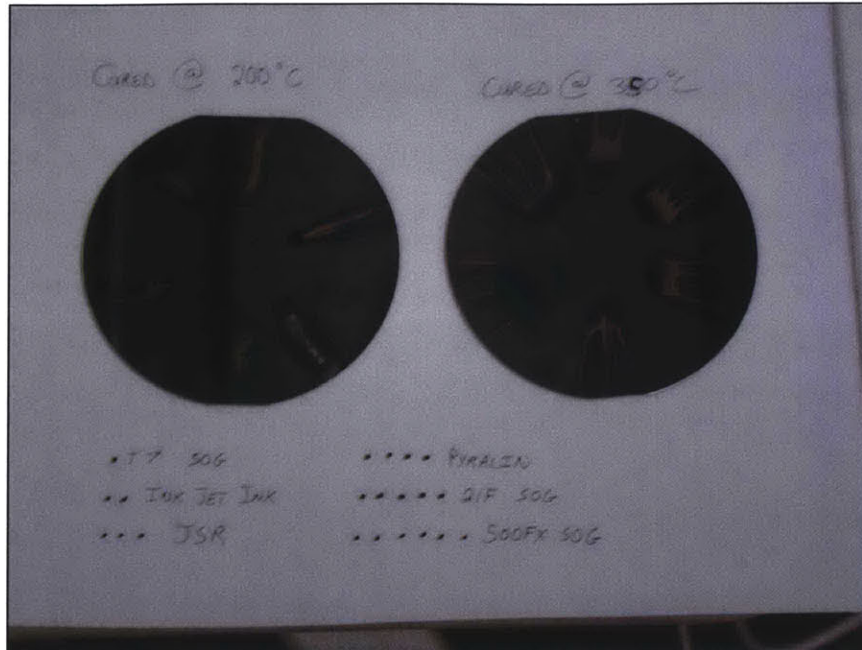

Figure 064: Test wafers used for determining the material characteristics of each of the candidate insulator materials.

Material	Cure Temp	Wets Si?	Ag Wets?	Insulates?	Insulates w/ pressure?	Still wet after spin?
T7 SOG	200° C	Yes	Yes	Good	Yes	No
Ink Jet Ink	200° C	Yes	Yes	Bad	No	No
JSR	200° C	Yes	Yes	Bad	No	Yes
Pyralin	200° C	Yes	Yes	Med	No	Yes
21F SOG	200° C	Yes	Yes	Med	Yes	Yes
500fx SOG	200° C	No	No	n/a	n/a	Yes
T7 SOG	350° C	Yes	Yes	Good	Yes	No
Ink Jet Ink	350° C	Yes	Yes	Med	No	No
JSR	350° C	Yes	Yes	Bad	No	Yes
Pyralin	350° C	Yes	Yes	Great	No	Yes
21F SOG	350° C	Yes	Yes	Good	Yes	Yes
500fx SOG	350° C	Yes	No	n/a	n/a	Yes

Figure 065: Table showing the results from the insulation tests.

The next thing that I need to test was whether or not it was possible to pattern each of these materials by liquid embossing. What I found was that 5 out of the 6 materials patterned very well.

The JSR replicated features remarkably well, even replicating tiny sub-micron scratches in the PDMS stamp, (Fig. 066). The IJI also patterned remarkably well, (Fig. 067,) and a surprising result is shown in Fig. 068. The nanocrystalline colloids that I have patterned are highly viscous materials and thus it is difficult for the PDMS stamp to clear the material out of large areas since it is difficult to push the material far distances. This typically limits the maximum channel width of these patterns to 5μm. The IJI on the other hand is low viscosity and Fig. 068 shows a region 90μm wide that has been completely cleared of material.

Each of the spin-on glasses could also be patterned easily, although as mentioned, the T-7 material needed to have a solvent exchange to increase its evaporation time. Fig. 069 shows a collection of 1μm features patterned in the 21F spin-on glass. The Pyralin polyimide, on the other hand, did not pattern at all. When the stamp was brought into contact with the Pyralin some sort of reaction happened which cross-linked the Pyralin in place, creating a white film that stuck tenaciously to the stamp and which was difficult to clean off. One possibility is that the Pyralin solvent can diffuse quickly through the PDMS stamp although this does not explain why the material would stick to the inert PDMS stamp when no other material tends to stick to it.

These tests indicated that either the T-7 or the 21F spin-on glasses were the primary insulator candidates. I used these materials to create many devices with patterned insulating layers between patterned conducting layers, as shall be described in the following sections.

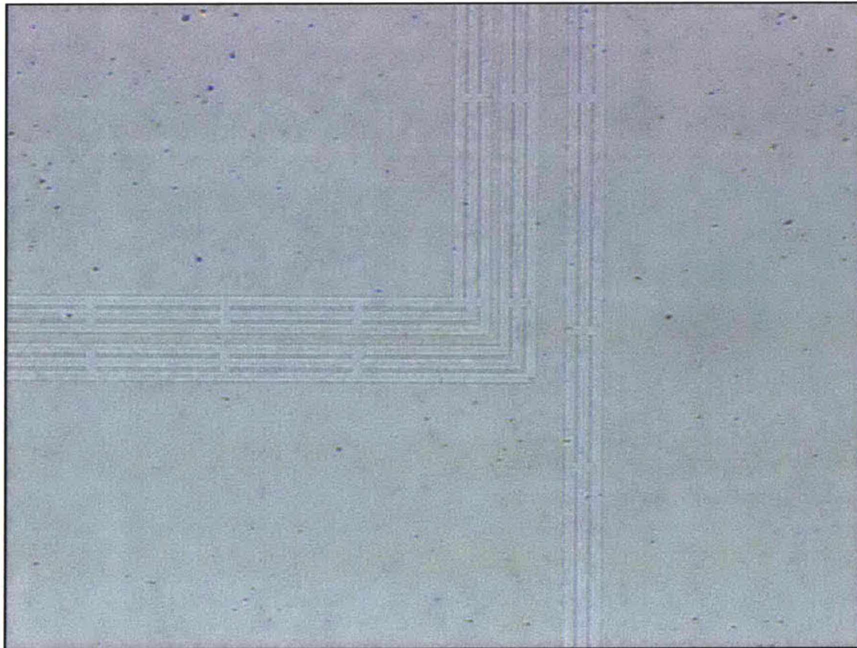

Figure 066: Optical image of 5μm features patterned in the JSR material.

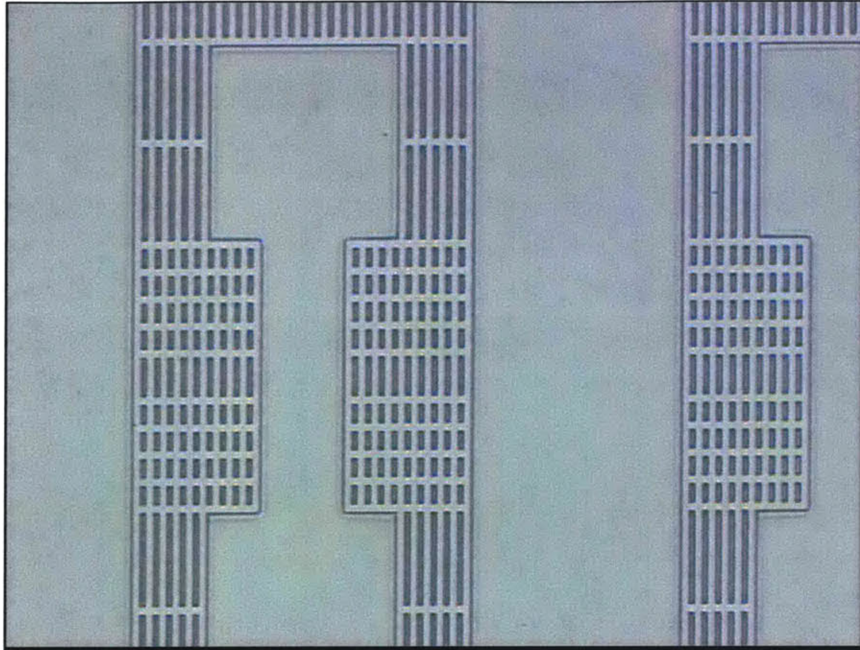

Figure 067: Optical image of 5μm features patterned in Inkjet Ink.

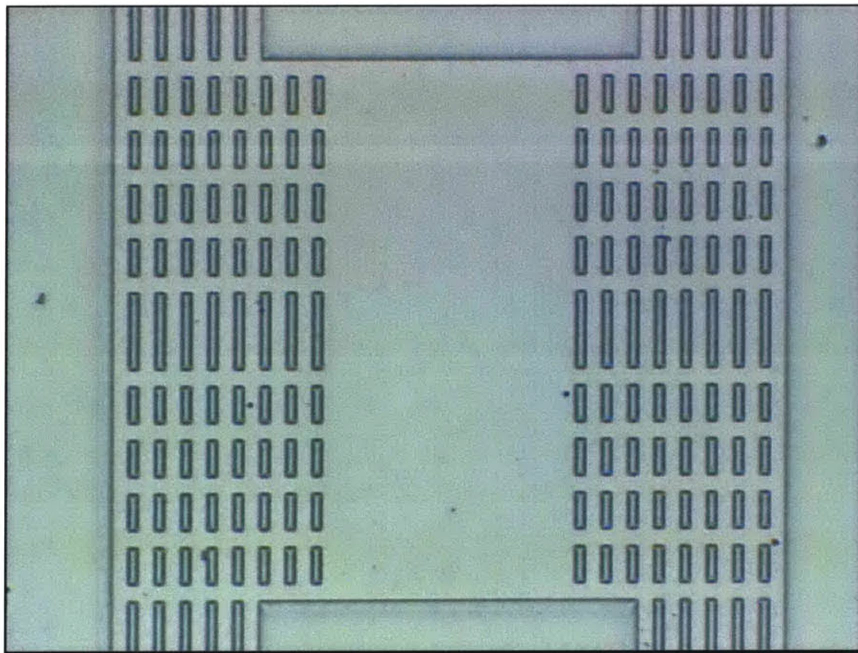

Figure 068: Optical image of 5μm features patterned in Inkjet Ink. In the center of this image is a region 90μm wide where all of the Inkjet Ink has been cleared away.

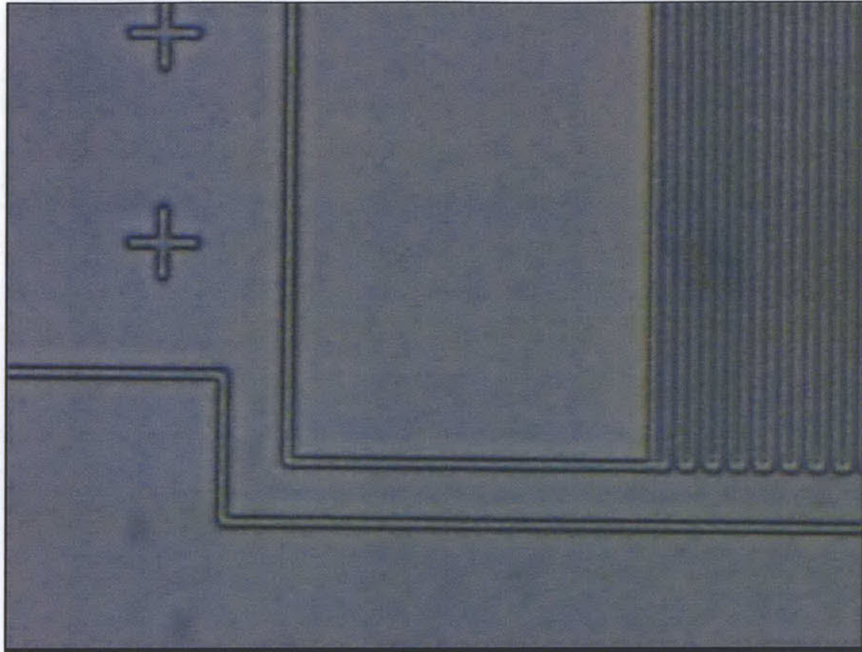

Figure 069: Optical image of 1μm features patterned in 21F spin-on glass.

3.8 Vias

After verifying that I could pattern insulators and create simple capacitors, the next obvious thing to work on was the creation of a via. In conventional semiconductor fabrication there are two separate halves to the fabrication process: the front-end, and the back-end. All of the transistor fabrication happens in the front-end, and all of the metal interconnects are created in the back-end. 40% of the complexity of making a modern chip is the creation of metal wires which connect all of the transistors on the chip. These back-end interconnects are typically 5 layers of patterned metal with vias connecting different layers together, (Fig. 070).

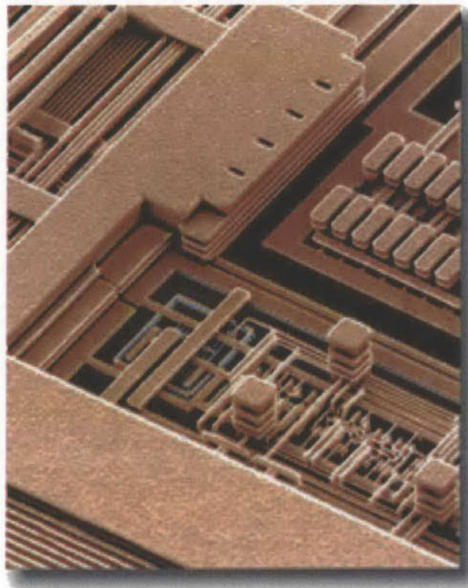

Figure 070: Picture of IBM copper interconnects.
[Photo copyrighted by IBM.]

My work with patterning multiple layers of material had convinced me that I should be able to pattern complex metal interconnects with vias. Fig. 071 shows two layer of overlapping squares. The small white squares are areas where there is no patterned material and the substrate is exposed. If I were to deposit a third layer of material on those squares it would be able to make contact through that hole to the underlying substrate. In addition, since the patterning process is conformal I would not have to planarize the structure before putting down that third layer of material.

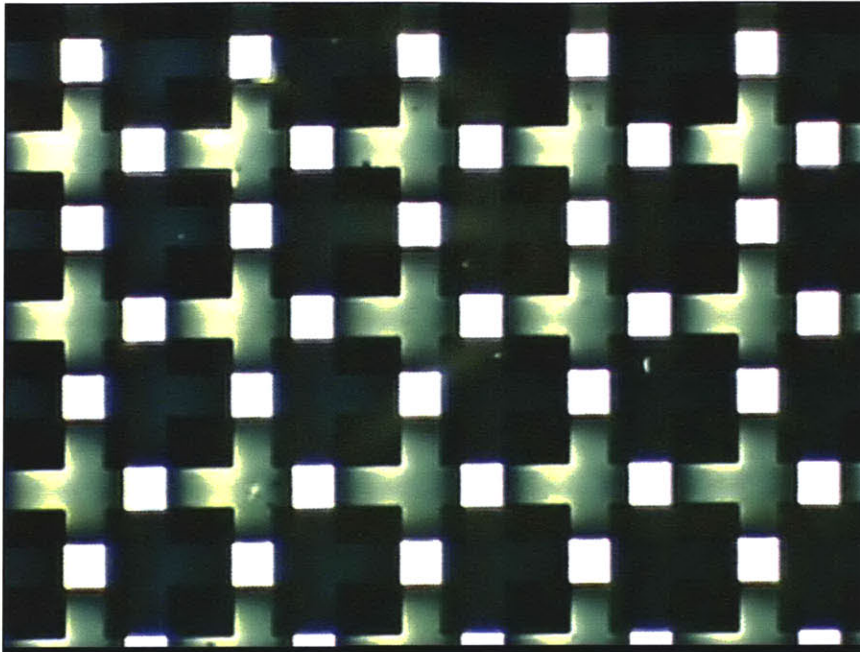

Figure 071: Transmission mode optical image of two overlapping layers of 15μm x 15μm Au squares. The small white squares are regions with no Au where the substrate is exposed.

I designed some test structures to verify this ability to pattern vias, (Fig. 072). These structures had two vias each which connected a top layer of patterned metal with a bottom layer of patterned metal. In some structures there were no vias patterned in the insulator and thus there was no conduction path from the left side of the structure to the right side. In other structures a via hole was patterned and this created a connection between the left side and the right side.

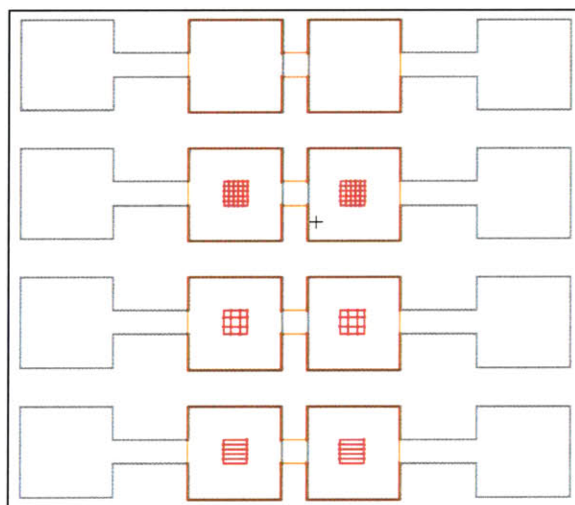

Figure 072: Overhead view of the design of a collection of three layer vias. The blue is the outline of the top metal layer, the brown is the outline of the bottom metal layer, and the red is the patterned holes in the insulating material.

When I was fabricating these via structures my ability to align multiple layers was still limited to roughly 20μm tolerance. For this reason I designed the structures to be large to give them room to be misaligned, although there is no reason why similar smaller structures would not work as well. Fig. 073 shows an overhead view of two of the devices that were fabricated. As shown in the figure, the top device did not have via holes and therefore there was no conduction path. The bottom device, on the other hand, had via holes and thus conducted. In addition to probing from the left pad to the right pad I also probed between the pads and the surrounding metal. I was able to verify that each of the patterned structures was completely insulated from the surrounding metal. This is important because it shows that liquid embossing can pattern electrically isolated features on top of existing patterns. Fig. 074 shows a zoomed in view of the via hole and the regions where the top pattern intersects with the underlying pattern.

The structures in these images were fabricated using the 21F spin-on glass, but I have fabricated similar structures with the T-7 spin-on glass and Inkjet Ink. It's important to note that in addition to fabricating vias, I have also fabricated capacitors in this work. The structure in the image with no via holes is effectively a capacitor between the underlying patterned metal and the top patterned metal. The spin-on glasses are low-k dielectric materials so structures based on them are not ideal capacitors, but they can act as basic passive components for logic design.

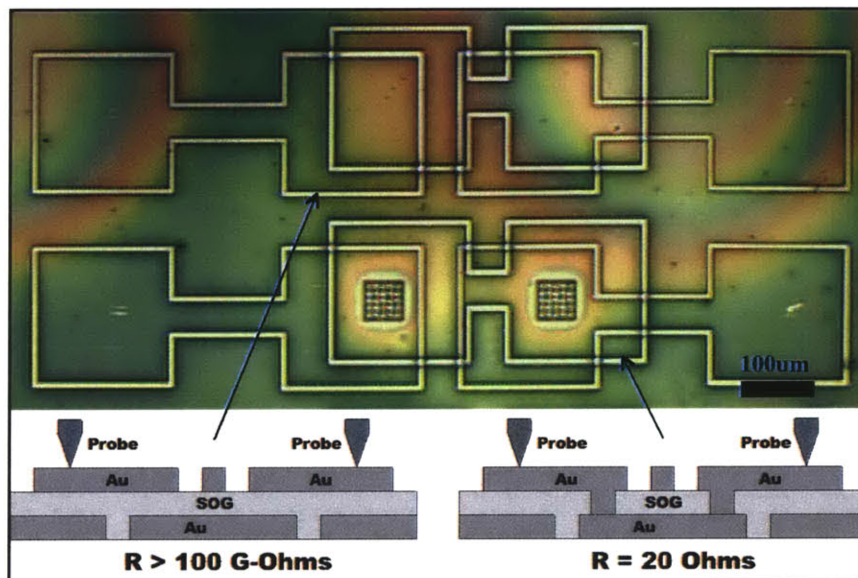

Figure 073: Optical image of multi-layer via structures. The top structure had no vias and thus there was no conduction path from the left pad to the right pad. The bottom structure did have vias and thus conducted.

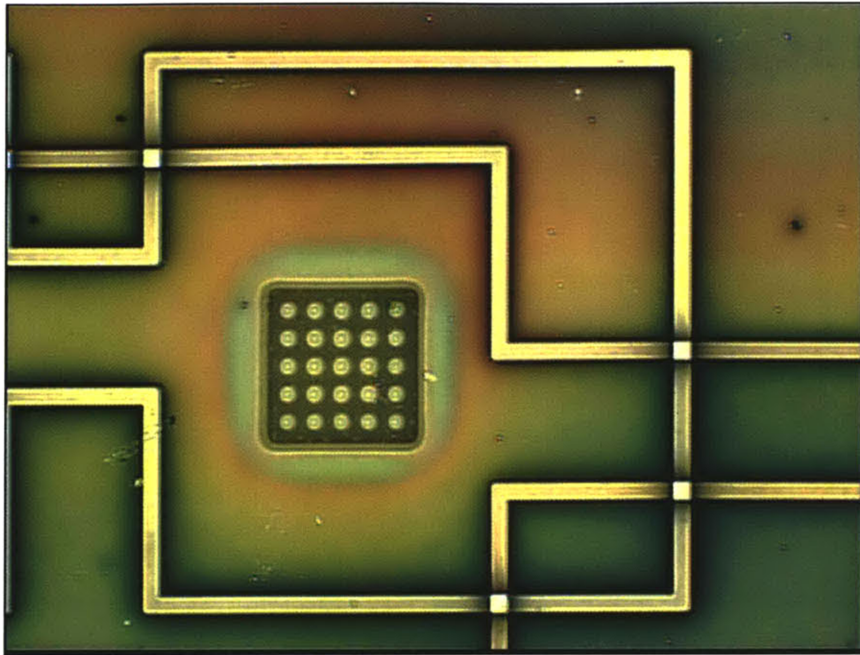

Figure 074: Zoomed-in view of the via and areas where the top pattern intersects with the underlying pattern.

The next step in proving the suitability of liquid embossing for fabricating metal interconnects will be creating more complicated multi-layer circuits like those shown in Fig. 075. This work is currently being pursued.

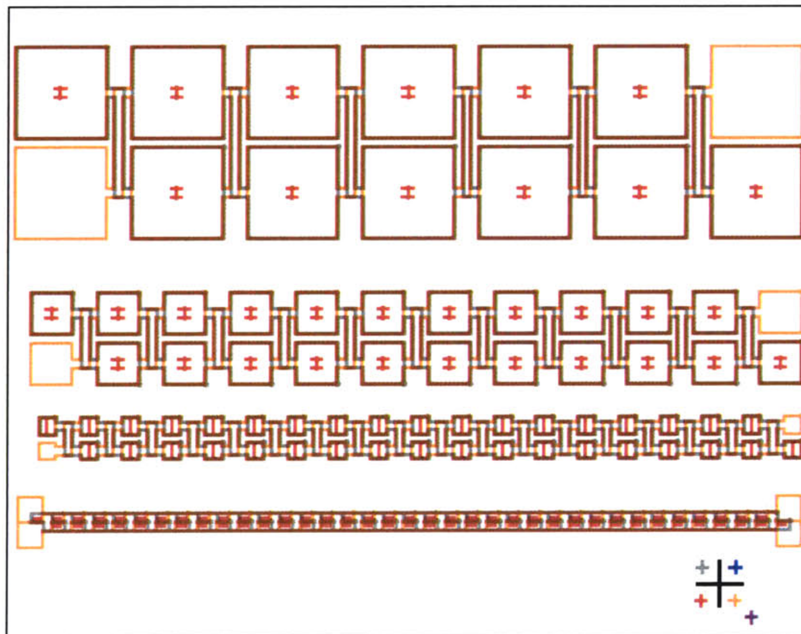

Figure 075: Design for various different 3-layer inductors.

3.9 Transistors

In order to fabricate transistors our group needed to develop a novel semiconducting material that could be solution processed. Brent Ridley, the lead chemist in our group, investigated the possibility of using organic systems such as pentacene. He ultimately decided though that based on the results achieved with single-crystal pentacene, there was an intrinsic limit in the mobility which could be achieved by organic materials. So instead, our group began work on inorganic nanocrystalline colloids *(23)*. Brent developed a nanocrystalline colloid of Cadmium Selenide (CdSe) which was capped with a loosely bound organic group. These CdSe nanocrystals were soluble in various solvents and had a tight size distribution. When heated, the solvent and the organic capping groups would boil off leaving behind only CdSe. The nanocrystals of CdSe would then sinter together, and it was discovered that the lattice planes of the nanocrystals would line up to form surprisingly large crystalline grains, (Fig. 076).

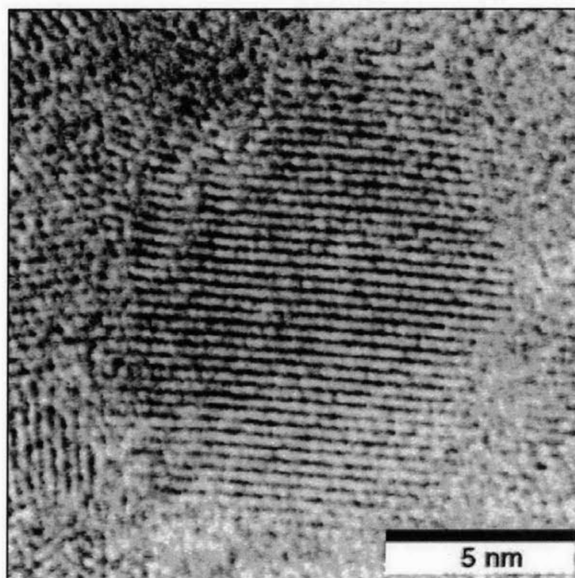

Figure 076: TEM of a polycrystalline grain of sintered CdSe nanocrystals

In order to test this semiconducting material we fabricated a number of test wafers. The wafers consisted of a p-type Si wafer with 300nm of thermal oxide and Au source/drain electrodes patterned on top of the oxide. Droplets of the CdSe solution were deposited on top of the source/drain electrodes and the wafer was heated to 350°C in order to drive off the solvent and sinter the nanocrystals, (Fig. 077). The transistor could then be probed, (Fig. 078) and the values for the on/off ratio and the mobility of the semiconductor were calculated. The on/off ratio was found to be $3x10^4$, and the mobility was 1 $cm^2V^{-1}s^{-1}$ which exceeded all previously published mobility results for solution-processed organic semiconductors.

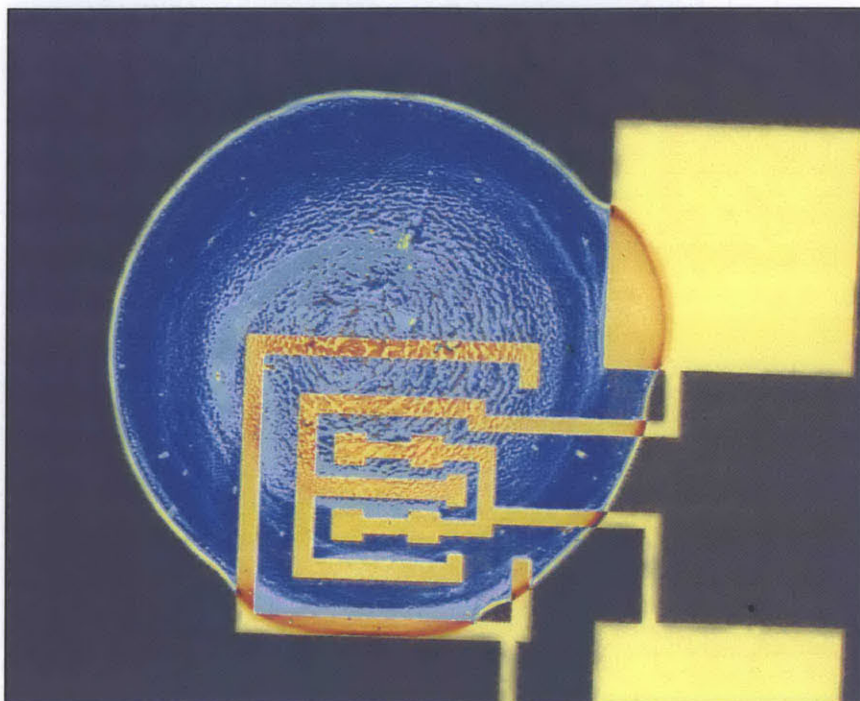

Figure 077: Au source/drain electrodes patterned by photolithography with a droplet of sintered CdSe nanocrystals.

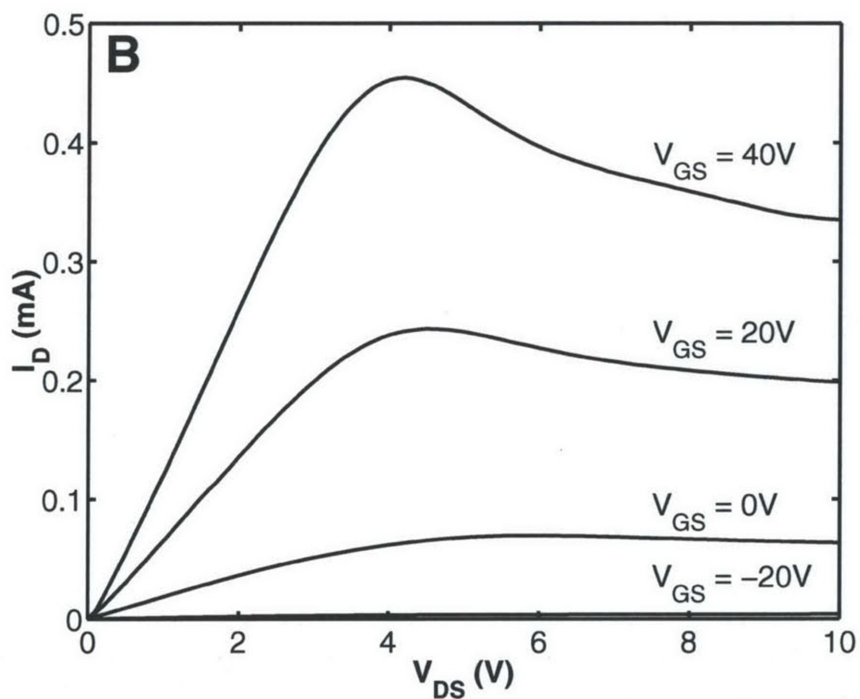

Figure 078: IV curve for a CdSe transistor fabricated on conventionally processed source/drain electrodes. A linear regime mobility of 1 $cm^2V^{-1}s^{-1}$ and an on/off ratio of $3x10^4$ were calculated.

Although these initial results with CdSe FETs were very promising, the only portion of the device that was printed were the CdSe droplets. I therefore fabricated half-printed source/drain electrodes which consisted of a p-type Si wafer with 300nm of thermal oxide and liquid embossed Au source/drain electrodes on top of the oxide, (Figs. 079-080). Droplets of CdSe were then deposited on top of the channels and heated to 350°C to sinter the nanocrystals. The devices were encapsulated with an optical adhesive and then taken out of the glove box and probed under ambient conditions, (Fig. 081). The mobility of these devices was calculated to be .1 $cm^2V^{-1}s^{-1}$ which is within an order of magnitude of the mobility for the conventionally processed devices. The on/off ratio was greater than 10^3. In addition, other identical devices were taken out of the glove box without encapsulation and the source/drain resistance was measured under various different light intensities to measure the device's photocurrent, (Fig. 082).

Figure 079: Schematic of a half-printed CdSe FET. The top Au source/drain electrodes were fabricated by liquid embossing.

Figure 080: Overhead view of patterned source/drain electrodes. The green areas are Au and the line running down the middle is a 3um wide channel.

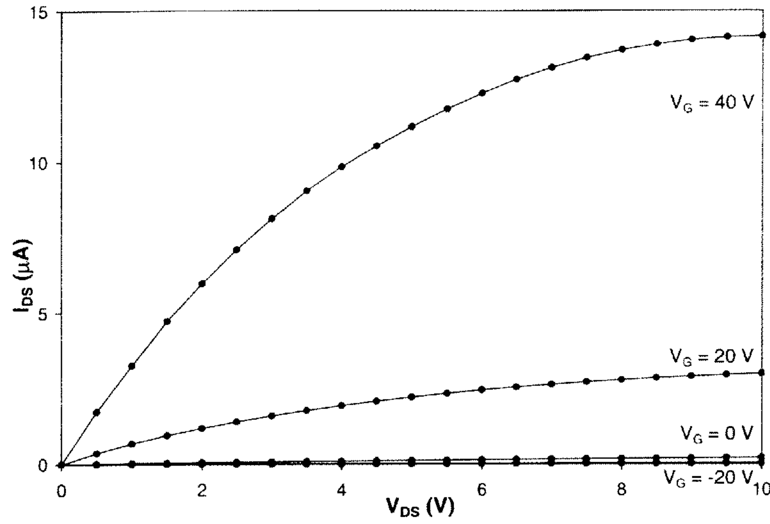

Figure 081: IV curve for a CdSe transistor fabricated with liquid-embossed source/drain electrodes on top of a Si wafer gate with 300nm of thermal oxide. The calculated mobility was .1 $cm^2V^{-1}s^{-1}$ and the on/off ratio was greater than 10^3.

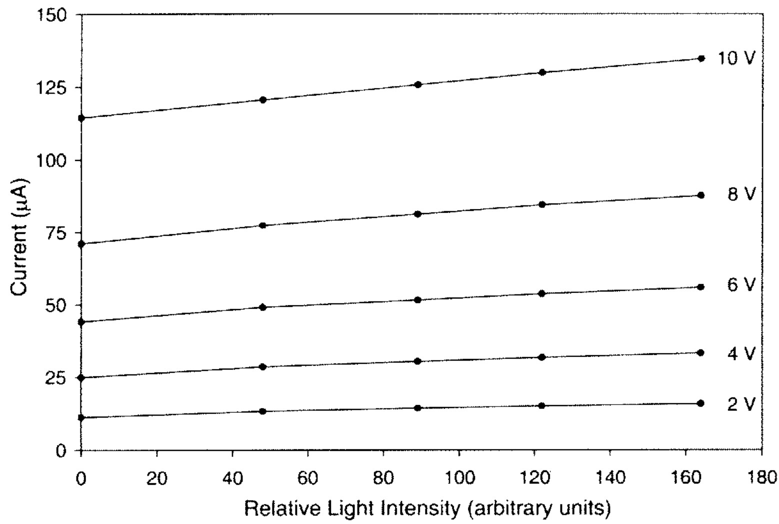

Figure 082: Source/drain resistance vs. light intensity at various gate voltages for a half-printed CdSe FET.

All-printed CdSe FETs were also fabricated. These devices consisted of a glass slide substrate with a first layer of liquid-embossed Au as a gate, a second layer of liquid-embossed spin-on-glass (21F) as a gate dielectric, a third layer of liquid-embossed Au as the source/drain electrodes, and a droplet of CdSe, (Fig. 083). These devices were encapsulated with optical adhesive and then probed in ambient conditions, (Fig. 084). The resulting currents were much lower than expected with a calculated mobility of .001 $cm^2V^{-1}s^{-1}$. We believe that this lower mobility is the result of a poor interface between the spin-on-glass and the CdSe. Recent work has indicated that this number can be improved significantly. The calculated on/off ratio for this device was 10^3.

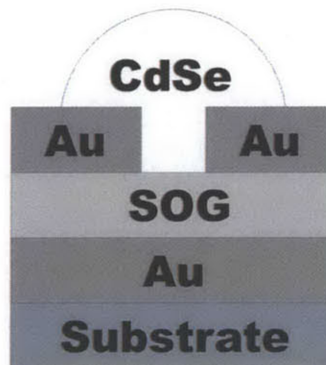

Figure 083: Schematic of an all-printed CdSe transistor with a Au bottom-gate, spin-on-glass gate dielectric, Au source/drain electrodes, and a droplet of sintered CdSe.

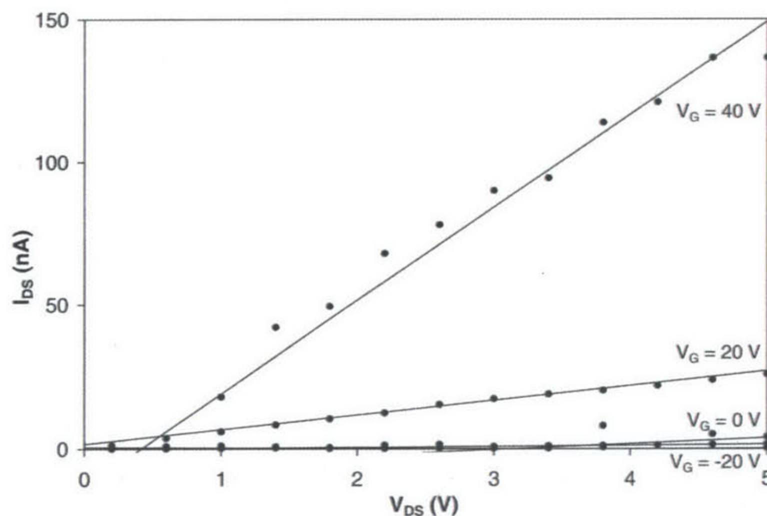

Figure 084: IV curve for a CdSe transistor fabricated with liquid-embossed source/drain electrodes, gate, and gate dielectric layer. The calculated on/off ratio was 10^3.

In addition to working with CdSe nanocrystals I have also fabricated transistors using evaporated amorphous silicon as the semiconductor. The structure of these devices is identical to the structure of the half-printed CdSe devices, except that rather than depositing droplets of CdSe nanocrystals on top of the source/drain electrodes, I instead evaporated amorphous silicon on top of the electrodes. In addition, I also fabricated the devices with Ag instead of Au, since Au diffuses very rapidly through silicon, (Fig. 085). I deposited three different thicknesses of amorphous silicon: 10nm, 50nm, and 200nm. The devices with 10nm of silicon showed zero off-current across the channel indicating that there was either too little silicon to completely bridge the channel or else that all of the silicon in the channel had oxidized. The devices with 200nm of silicon showed large off-currents with very little field effect. In addition, a number of the devices behaved like a rectified diode between the drain and the gate. Both of these results seem to indicate that depositing 200nm of silicon somehow damaged the gate oxide.

The devices with 50nm of silicon on the other hand showed very good field effect, (Fig. 086). The measured on/off ratios were in excess of $3x10^3$, and there was very little variation between different devices. The mobility was calculated to be .01 $cm^2V^{-1}s^{-1}$ which is still quite low, although I believe that the limitation in mobility is due to the interface between the Ag and the amorphous silicon. In conventional amorphous silicon devices a thin N+ layer is used to improve electron transport between the metal and the semiconductor *(27)*. Including an N+ layer with these printed devices will almost certainly improve the measured mobility.

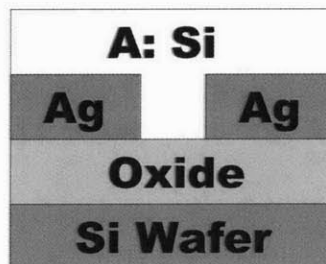

Figure 085: Schematic of a half-printed amorphous silicon device. Ag souce/drain electrodes were fabricated by liquid embossing on top of a p-type silicon wafer with 300nm of thermal oxide. Amorphous silicon was then evaporated on top of the structure.

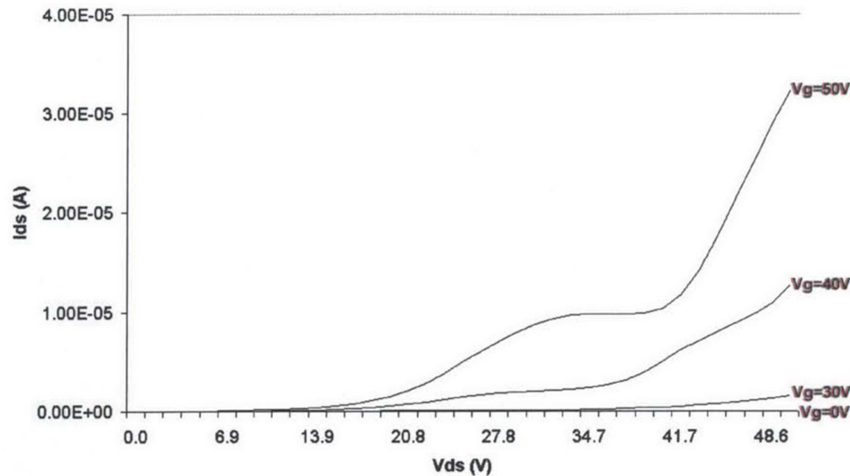

Figure 086: IV curve for an amorphous silicon transistor fabricated with liquid embossed source/drain electrodes and a p-type wafer gate with 300nm of thermal oxide. An on/off ratio of $3x10^3$ was measured.

The final material that I chose to use as a semiconductor was carbon nanotubes. It has been demonstrated that carbon nanotubes can have mobilities as high as 20 $cm^2V^{-1}s^{-1}$ *(28)*. Unfortunately, carbon nanotubes can have a variety of different chiralities, and it is the chirality of the tube that determines whether it is metallic or semiconducting. There is currently no viable technique for creating nanotubes of specific chiralities, and it is therefore impossible to fabricate transistors that have only semiconducting tubes spanning across the channel. I theorized that it should be possible to selectively remove all of the metallic tubes from the channel by applying a ramping voltage and selectively blowing up all of the highly conductive tubes, leaving behind the semiconducting tubes, (Fig. 087). If you apply a constant voltage across the channel, the current density will be much higher in the metallic tubes as compared with the semiconducting tubes. It has been shown that the maximum current that a nanotube can carry is on the order of 10 μA, and after exceeding this maximum current the nanotube will break irreversibly.

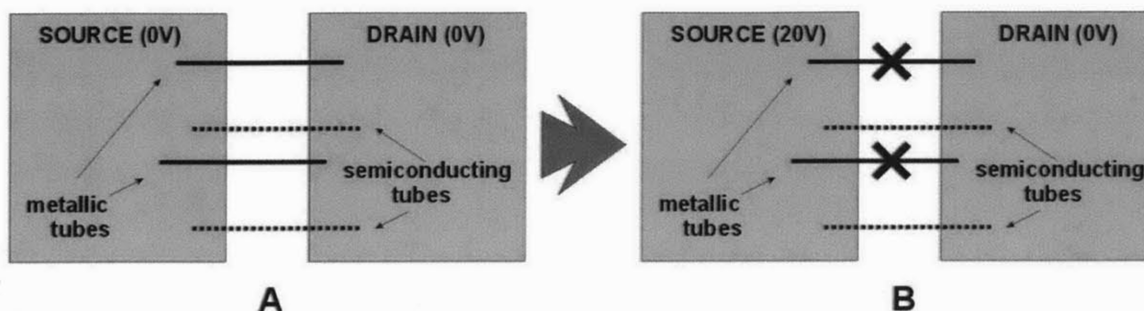

Figure 087: Schematic for the selective blowing of metallic nanotubes. **a)** A selection of both metallic and semiconducting nanotubes are deposited across the channel between two electrodes. **b)** When a voltage is applied between the two electrodes the metallic tubes carry a large current and thus blow up, leaving behind the semiconducting tubes.

I fabricated a device identical to the half-printed CdSe device, with liquid-embossed source/drain electrodes on top of p-type wafer with 300nm of thermal oxide. I then deposited a very dilute slurry of carbon nanotubes in water on top of the structure. By measuring the IV curve of the device I verified that there were now conducting tubes spanning across the channel. I then began slowly ramping up the voltage across the channel and measuring the resulting current. As I increased the voltage I observed a sequence of discontinuous drops in current until at 21 V there was zero current being passed across the channel, (Fig. 088). Each of the discontinuous drops in current happened suddenly and they corresponded to a drop in total current across the device of 10 μA, indicating that the device that was destroyed was carrying 10 μA when it blew. This result is a very strong indication that by slowly increasing voltage it is possible to selectively and controllably destroy individual carbon nanotubes stretching across a channel.

I was hoping that by probing the resultant device I would be able to detect field effect from the remaining semiconducting tubes, but unfortunately I was unable to detect any field effect. This could indicate a number of different things. 1) There were no semiconducting tubes stretching across this particular device, 2) the semiconducting tubes were blown up in the same way that the metallic tubes were, (possibly because the off-current through the semi-conducting tubes was very large,) or 3) the nanotubes were in bundles and therefore, even though the metallic tubes were destroyed, the semiconducting tubes did not have a good interface with the underlying dielectric which led to zero field effect. I will be conducting a number of further experiments in this area with purified nanotubes in order to determine why no field effect was observed.

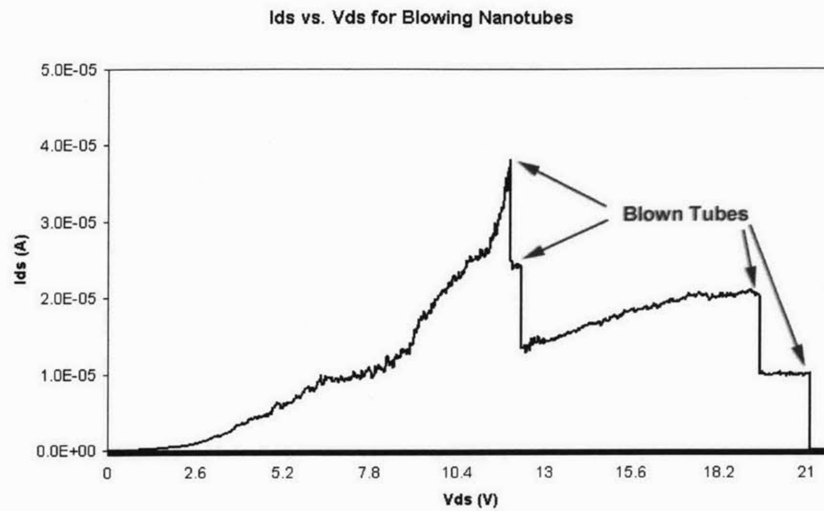

Figure 088: IV curve showing the discontinuous blowing of individual carbon nanotubes. Each drop in current corresponds to exactly 10 μA, which is the expected maximum current density for a carbon nanotube.

3.10 Logic Design

The designs that I have used when fabricating logic devices have evolved significantly over the past year. Fig. 089 shows an early design for a 3-layer inverter. The power, ground, input, and output lines all fanned out to large pads which are not visible in the image. The power line, (at the top of the image,) connected to the source and gate of a transistor and acted as a pull-up resistor. The input line switched a second transistor which connected the ground line to the output line. In this way, when the input signal was high the output would go low, and otherwise the pull-up resistor would pull the output high. This particular design, although accurate, was virtually impossible to fabricate at the time though since it required alignment to within several microns.

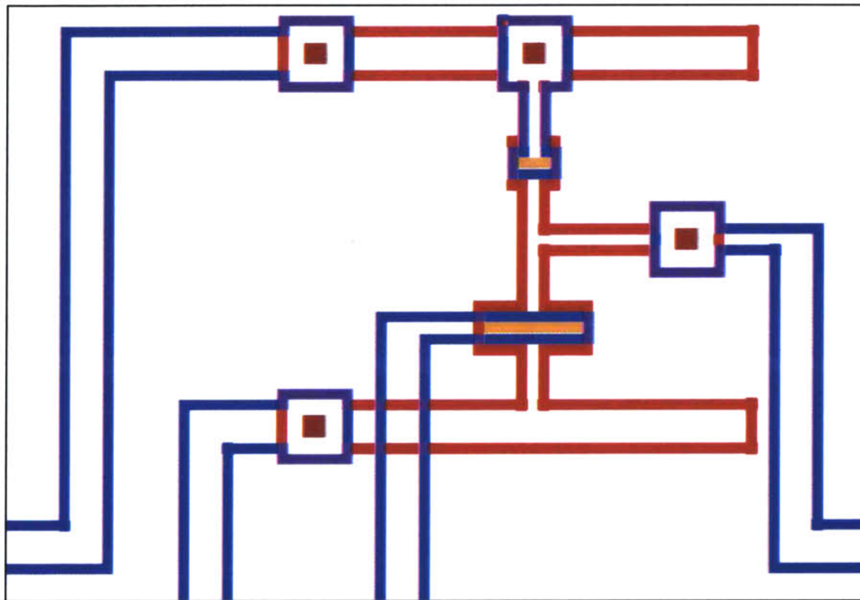

Figure 089: Early design for an NMOS inverter. The bottom metal layer is outlined in red and the top metal layer is outlined in blue. The four squares are vias which connect the top layer to the bottom layer. The two orange areas in the center are transistors, with the top one acting as a pull up resistor.

Wishing to avoid the problem of alignment, I designed a second inverter structure as shown in Fig. 090 which was largely alignment invariant. Each of the features were made very large so that any slop in alignment would not effect the final device. I was able to successfully fabricate these structures, but at the time we were having difficulties with the interface between the CdSe and the spin-on glass so the structure was too complicated. What we truly needed was a very simple transistor design that it would be easy to iterate CdSe samples on.

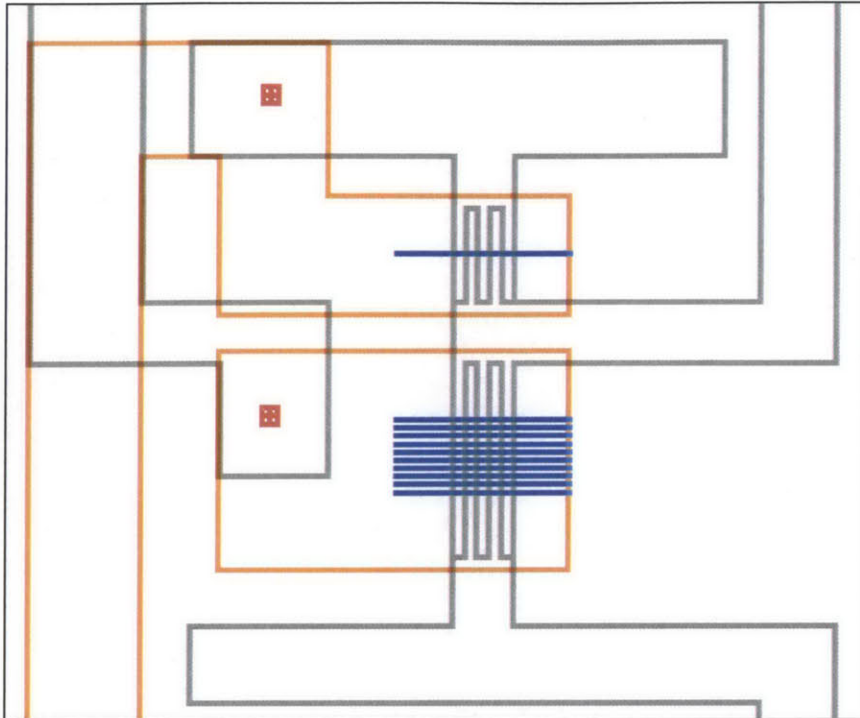

Figure 090: Design for an alignment-invariant 4-layer inverter. The gray lines outline the top layer of metal, and the orange lines outline the bottom metal layer. The red squares are vias, and the blue lines are the transistors.

In order to make it easy to test CdSe samples I designed a very large transistor structure that was 5mm on a side, (Fig. 091). This structure had a single channel which separated the left half of the device from the right half, and on different devices I varied the channel length from 1μm, 3μm, and 5μm. The entire structure looked like a large X so it was easy to deposit a single droplet of CdSe solution across the channel. In addition, the droplet could be encapsulated without completely covering the Au electrodes so it was possible to probe the device. Fig. 092 shows a photograph of an array of these structures with encapsulated CdSe droplets. We have iterated through close to a hundred of these liquid-embossed wafers while improving our CdSe chemistry.

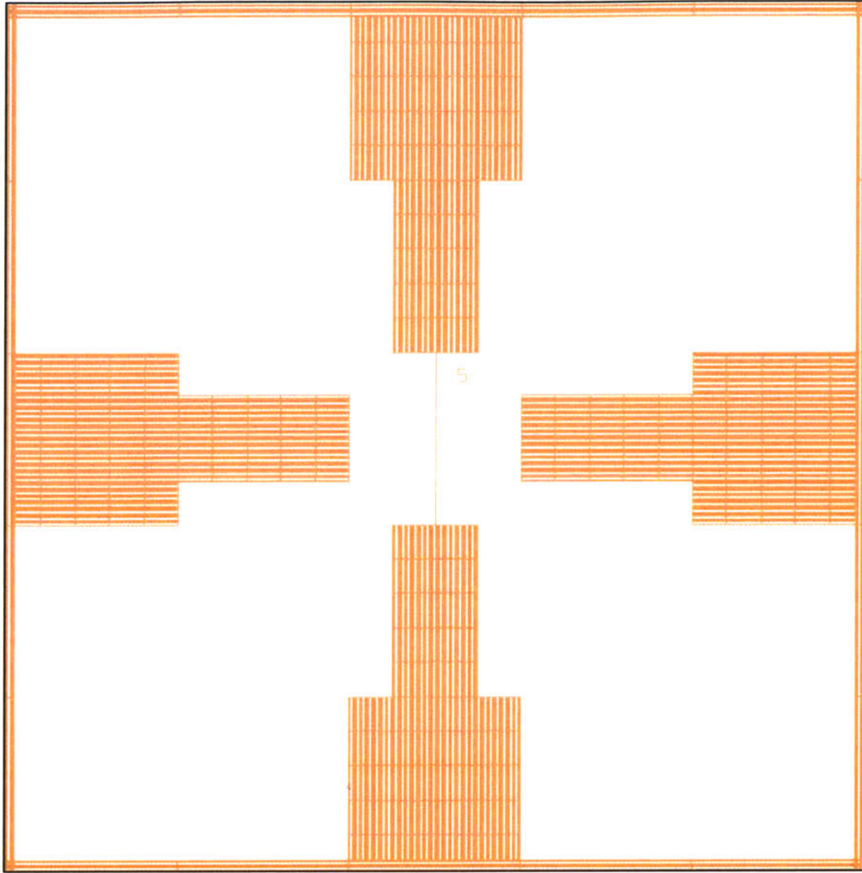

Figure 091: Schematic of large area transistor structure for iterating through CdSe samples. The left side is the source, the right side is the drain, and in the center is a 5μm wide channel.

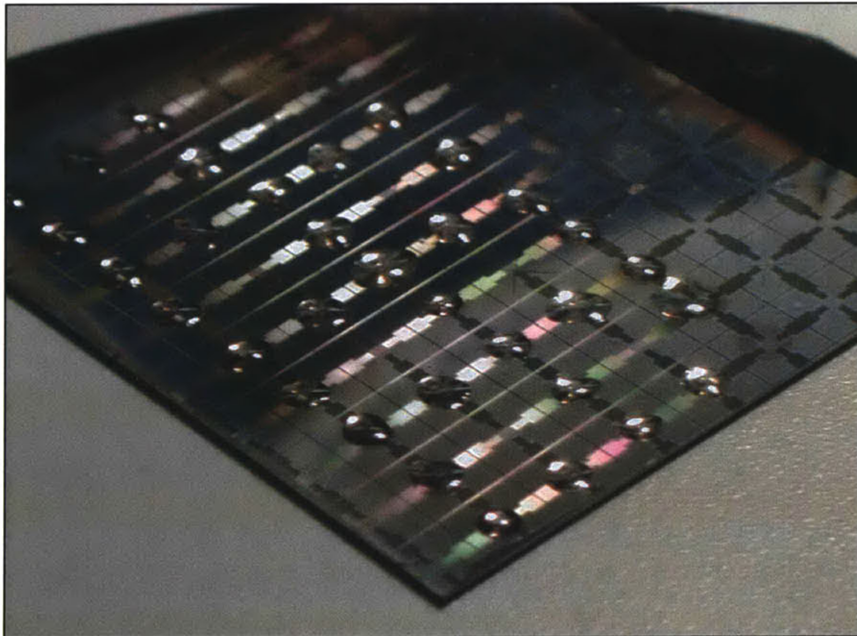

Figure 092: Photograph of an array of transistor test structures with encapsulated CdSe.

Given the usefulness of the large-area transistor structures, I decided to fabricate similar structures for more complex logic gates. Fig. 093 shows a large-area 3-layer NOR device. The upper-left corner is the A input, the lower-left corner is the B input, the left-center area is 0V input, the right center area is 5V input, and the bottom-center is the output. The transistor on the right acts as a pull-up resistor on the output, and if either of the inputs goes high then the left transistor will pull the output down to 0V. This structure is particularly well suited to CdSe transistors since a droplet can be deposited in the center of the structure and encapsulated without covering any of the input/output pads. I'm currently working on fabricating these devices.

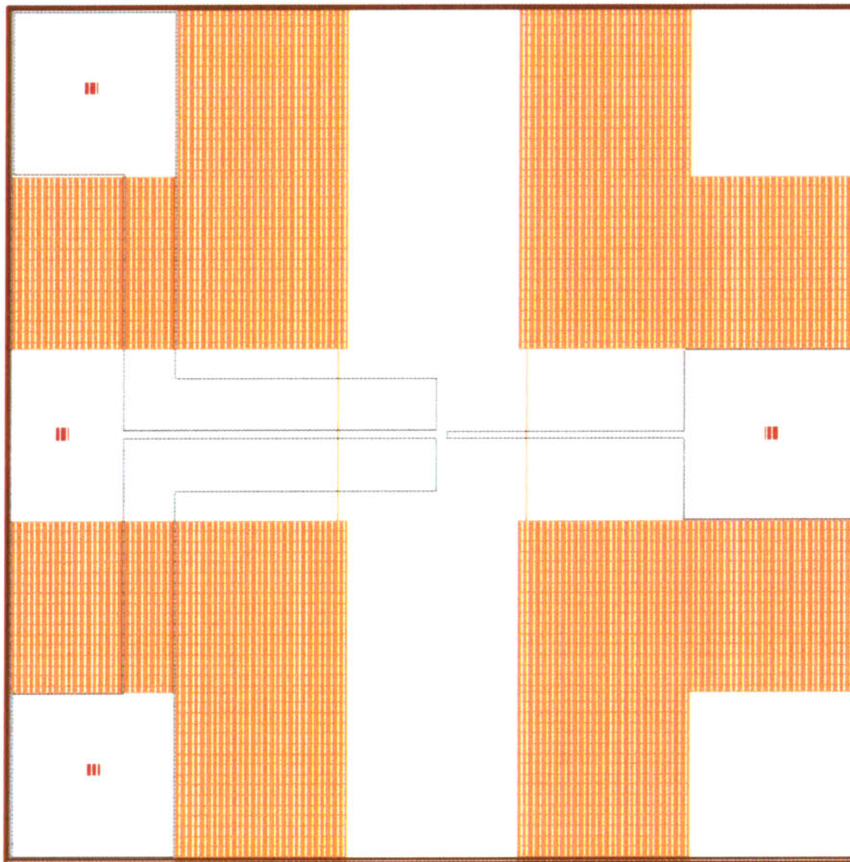

Figure 093: Large area NOR device. The orange features the outline of the top layer of metal and the gray lines are the outline of the bottom layer of metal. The red squares are vias. The two vertical orange lines in the center are the transistor channels.

For transistors based on amorphous silicon there is no need to make the structures large-area since there is no need to hand place droplets of material. I therefore designed a set of logic devices for use with amorphous silicon, (Fig. 094). These devices had redundant vias so that I

could test the quality of each probe/pad contact. These devices are also currently being fabricated.

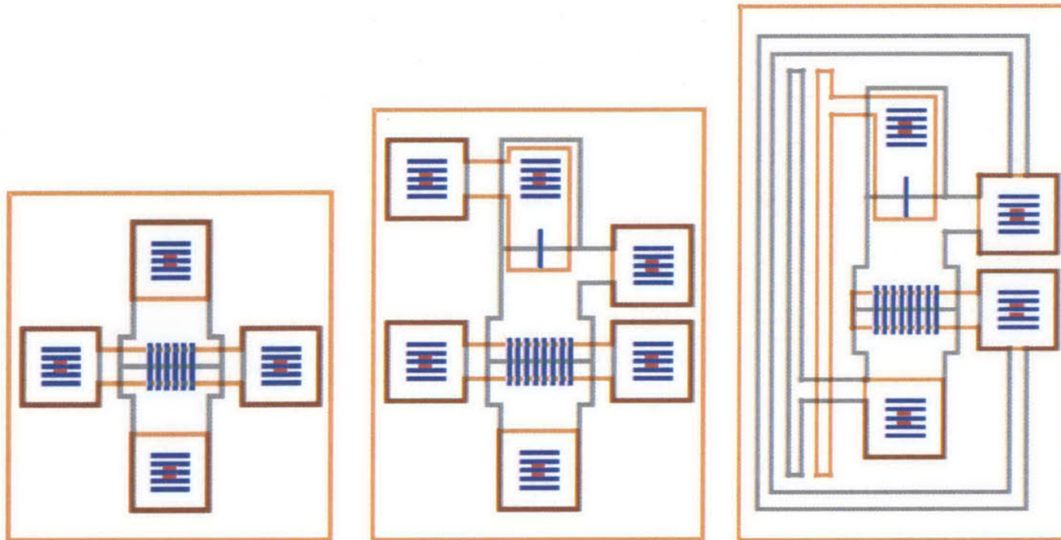

Figure 094: Schematics for several different amorphous silicon devices. The left device is a simple transistor, the middle device is an inverter, and the right device is a single stage ring oscillator.

3.11 Released MEMS

In addition to logic, another very interesting application of liquid embossing is in the area of Micro Electro Mechanical Systems (MEMS). Sandia National Labs has pioneered the development of MEMS and the structures that they have fabricated are very impressive, (Fig. 095). The gears shown in the image were fabricated in polycrystalline silicon with a SiO_2 sacrificial material. After the structure was entirely fabricated the SiO_2 was etched away with HF leaving behind the released gears.

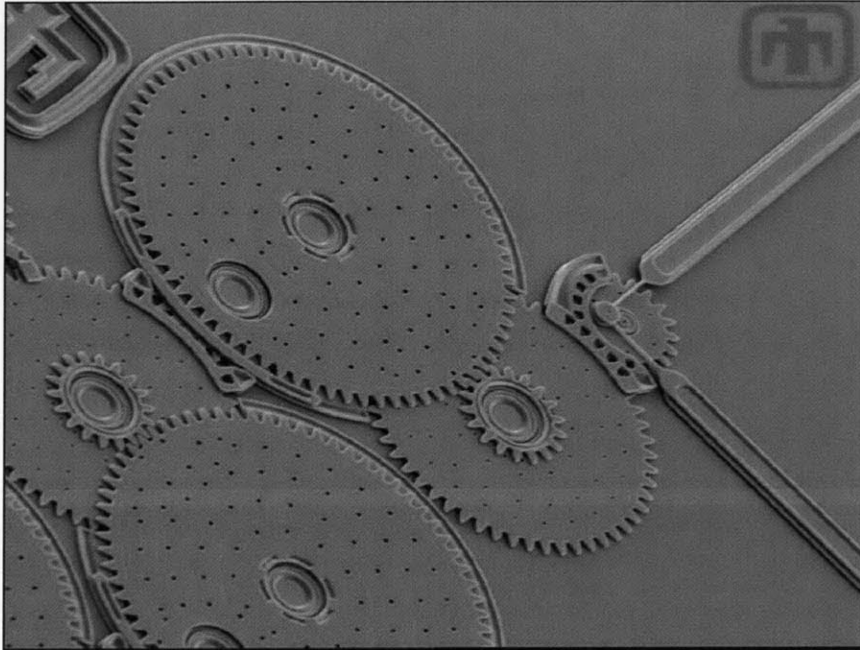

Figure 095: MEMS gears fabricated by Sandia National Labs using conventional processes.
[Photo copyrighted by Sandia National Labs]

There are three significant problems with the conventional process for fabricating MEMS devices. First of all, the cost of a MEMS foundry is extreme which in turn means that the cost per device is extremely high. Paying hundreds of dollars per square inch is typical. The second problem is that MEMS processing takes a very long time. Typically there is a 4-6 month turn around time between submitting a design to a foundry and having the product. Since MEMS devices are very complicated this long iteration time has significantly hampered innovation. The third and perhaps most significant problem is that current MEMS processes are limited to at most 5 layers of material. The cost per layer of material goes up exponentially so anything beyond 5 layers is prohibitively expensive. This is the reason why almost all MEMS devices are planar with very little 3-dimensionality.

So in these three areas – cost, turn-around time, and number of layers – liquid embossing has the potential to be very useful. In addition, liquid embossing can create metallic structures whereas most conventional processes work exclusively with poly-silicon.

In order to create MEMS devices I needed to find an appropriate sacrificial release material. After numerous experiments two different material sets emerged as promising. The first material was the AL 3046 polyimide produced by Japanese Synthetic Rubber (JSR). This material could be patterned, cured, and then etched in 1-methyl-2-pyrrolidinone under light sonication. The only difficulty with this material was that if the JSR was cured above 300° C it would become impossible to etch away. The second material set was either the T-7 or the 21F spin-on glass. These glasses patterned very well, could be cured at almost any temperature, and they could be etched by immersion in HF acid. Unfortunately, I am not overly comfortable working with HF so I built the vast majority of my structures with JSR.

The first structures that I built were simple released cantilevers. I coated half of a glass slide with JSR and then patterned Ag gratings on top of this edge so that the lines were half on the glass substrate and half on the JSR. I cured the Ag at 300° C for 10 minutes and then etched away the JSR and observed the results, (Fig. 096). The portions of the metal lines that were in direct contact with the substrate were unchanged and stayed adhered to the substrate. On the other hand, the portions of the lines that had been sitting on the JSR were completely released from the substrate and these lines formed a tangled mess similar to spaghetti. What was important though was that these 400nm wide lines were structurally intact over lengths of up to several millimeters. As the liquid which etched the JSR evaporated away most of these metal lines were sucked down into conformal contact with the substrate, but several of these lines were later jarred loose and stuck up out of the plane.

Fig. 097 shows a zoomed-in view of these spaghetti cantilevers. In this region the edge of the underlying JSR was very straight so you can see exactly where the cantilevers were attached and where they were released. Many of the wires snapped off at this interface, but many others remained intact. An AFM image of these released wires, (Fig. 098,) showed that each wire had a triangular profile 400nm wide and 150nm tall. This profile is in agreement with the grating structure upon which the PDMS stamp was cast.

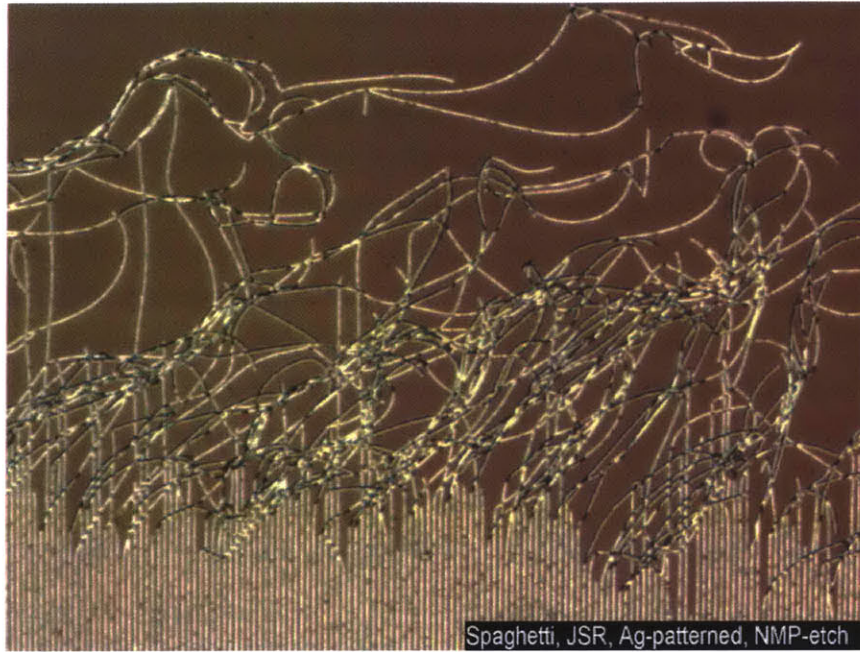

Figure 096: A collection of 400nm wide Ag wires that have been released from the substrate.

Figure 097: Zoomed-in view of released 400nm wide Ag wires.

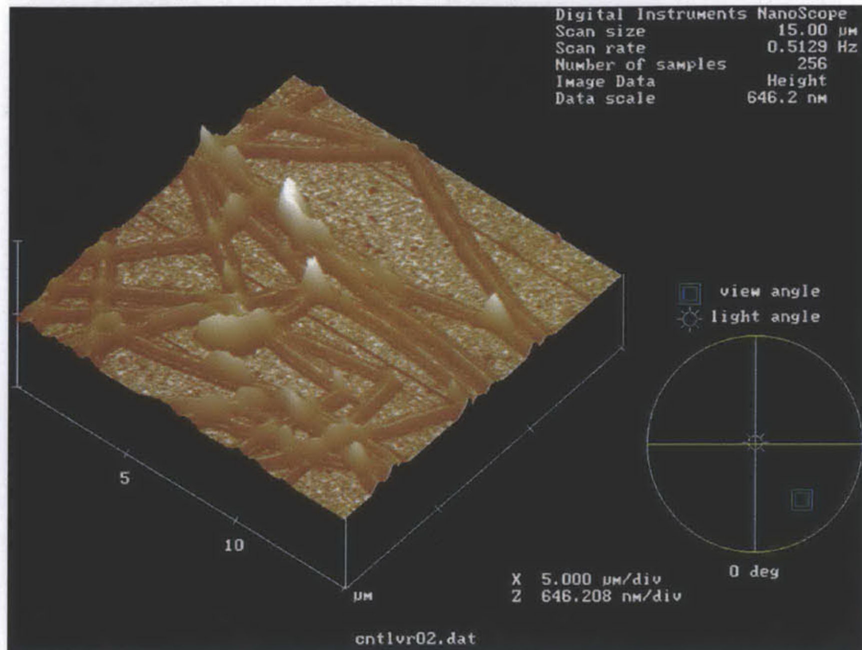

Figure 098: AFM of released metal wires. Each wire has a triangular profile 400nm wide and 150nm tall.

The second released structure that I fabricated was also based on gratings. I created a thin film of 21F spin-on glass on top of a silicon wafer and patterned it with an 800nm periodicity grating. I then created a grating pattern of Au on top of and perpendicular to this underlying glass grating. I etched the whole structure in HF for 1 minute and then took an SEM of the structure, (Fig. 099). As can be seen, the Au lines remained intact but the underlying glass lines were completely etched away. This left periodic triangular holes in each of the Au lines with the Au lines bridging 80nm above the surface of the substrate. The Au lines were quite structural and did not show any sign of being based on nanocrystals. This image also shows that it is possible to pattern features with side walls of 30°.

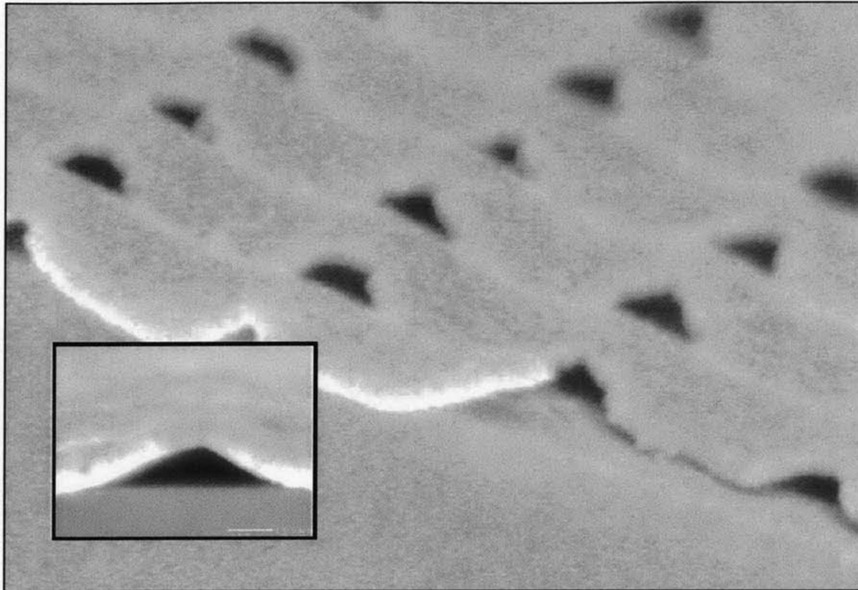

Figure 099: SEM of released Au aqueducts. The holes in the aqueducts were spaced 800nm apart. The inset shows a zoomed-in view of one of the triangular holes.

Since liquid embossing works with liquid materials the angle of the side-walls of a feature will be based at least in part on the wetting angle of that material with the substrate. It is therefore difficult to directly fabricate features with vertical side-walls, which is a requirement for most MEMS devices. After much thought, I came up with the following scheme to create arbitrary vertical features, (Fig. 100). Since each layer of patterned material is thin, it should be possible to create structures with many layers of material that have an arbitrary aspect ratio, sort of like a tall stack of plates. The excess metal in each layer is patterned into small pieces so that it can easily flow away after the release material is etched. The metal structure is firmly connected to itself through via holes in the release material. The release material inside the structure is integrated with the structure since the etchant has no way of reaching that material. The process shown in Fig. 100 can be repeated arbitrary many times in order to create tall structures with steep walls.

Fig. 101 shows an optical image of such a structure prior to the release material being etched away. The two large squares are anchored to the substrate by via holes in the resist material and the small squares are unanchored. After the release material is etched away, (Fig. 102,) the small squares are free to float away and the two large squares remain anchored to the substrate. Using this technique I have fabricated structures with 3 layers of metal and 3 layers of resist, and by etching the release I have completely removed the excess pieces of metal while keeping the metal pillars anchored to the substrate.

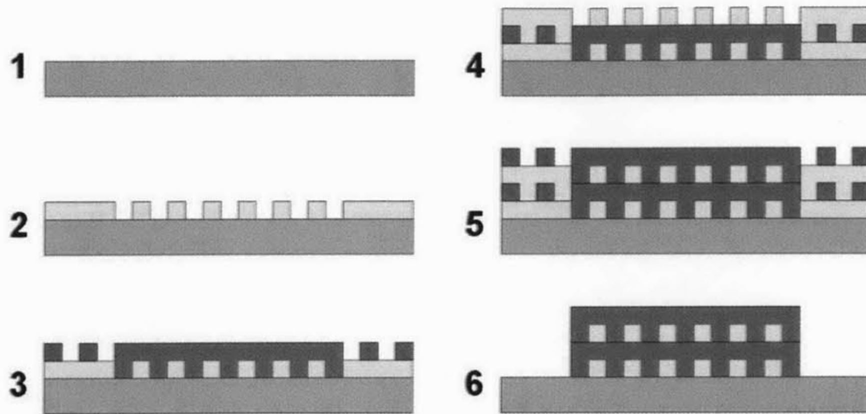

Figure 100: Schematic for the formation of vertical walls. **1)** The initial substrate. **2)** Pattern release material. **3)** Pattern metal. **4)** Pattern release with identical pattern. **5)** Pattern metal with identical pattern. **6)** Etch release material and wash away excess pieces of metal.

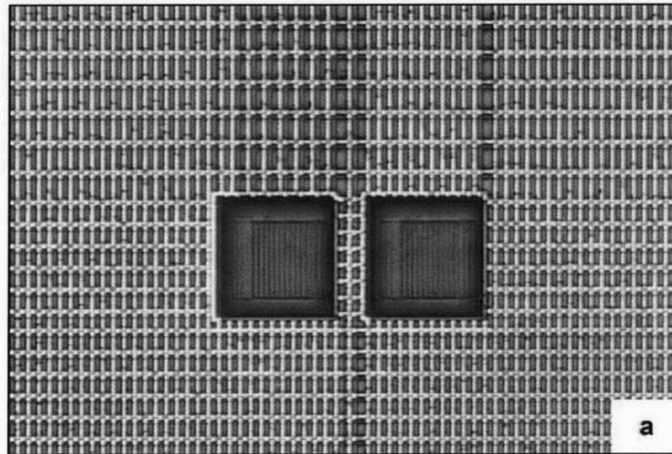

Figure 101: Optical image of Ag squares patterned on JSR. The large squares are connected to the substrate through patterned holes in the JSR.

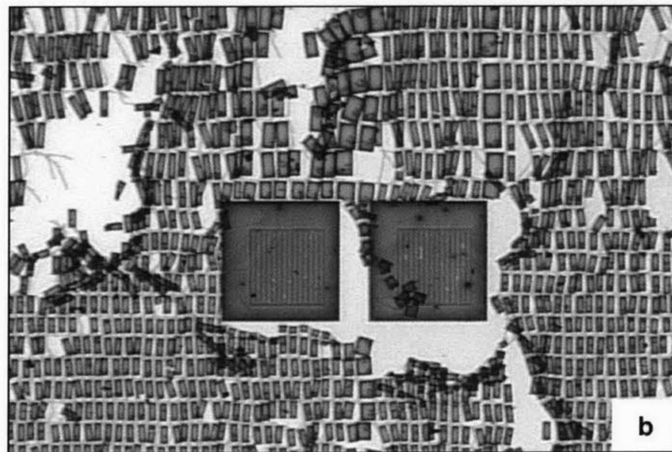

Figure 102: Optical image of the same structure after the JSR has been etched away.

Using this technique for creating vertical side walls I have designed a number of different MEMS structures. Fig. 103 shows a side-view schematic of a released wheel captured on a bearing. The first two layers are release material and they create a hole for the axle to connect to the substrate and dimples which will help the wheel to rotate easier. The third layer is the metal layer which creates the wheel and the axle. This layer and the previous release layer can be repeated an arbitrary number of times to create a thicker wheel. The fourth layer is another release layer, and the fifth layer patterns the cap on the axle. The wheel can then be released by etching away the release material. An overhead view of this design is shown in Fig. 104, and a version with the layers separated from each other is shown in Fig. 105.

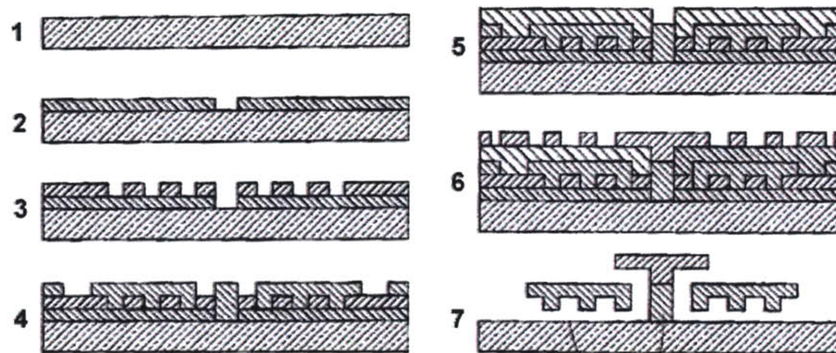

Figure 103: Schematic diagram for the fabrication of a captured wheel. **1)** The initial substrate. **2)** Patterned release material. **3)** Patterned release material. **4)** Patterned metal. **5)** Patterned release material. **6)** Patterned metal. **7)** The release material is etched away.

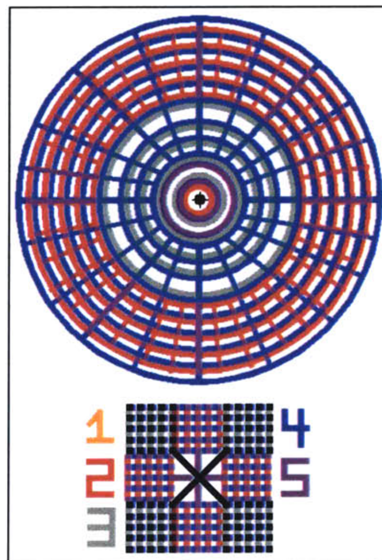

Figure 104: Overhead view of the captured-wheel design.

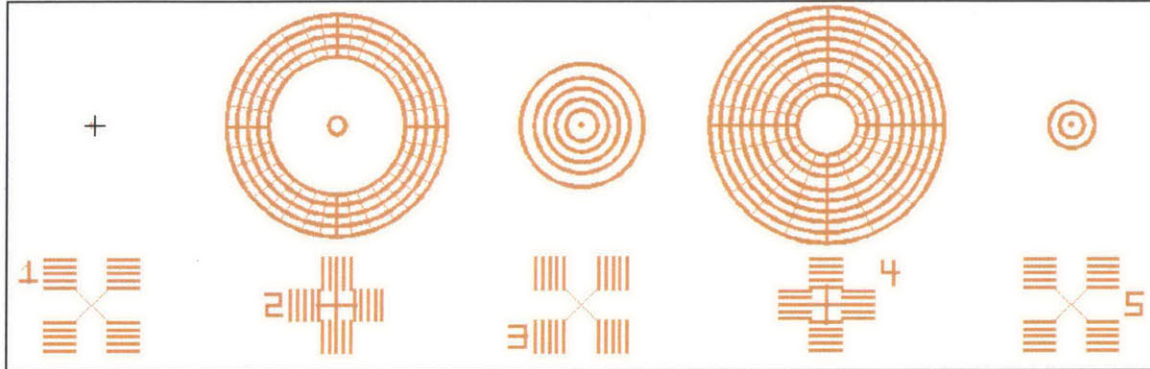

Figure 105: Overhead view of the captured wheel design with each layer spatially separated.

Another interesting MEMS structure is the heatuator *(29)*. A released wire loop is created which is connected to two pads on the substrate. One side of this wire loop is much thicker than the other side, so that when current is passed through the loop the current density in the thinner side is much larger and thus that side heats up more. This difference in heating causes the entire structure to bend, and this bending motion can be used to do mechanical work. Fig. 106 shows an overhead view of this heatuator design, and Fig. 107 shows a view with the different layers separated. I am now beginning the process of fabricating both the heatuator and the captured wheel.

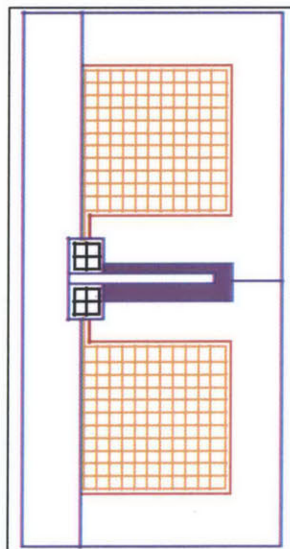

Figure 106: Overhead view of the 6-layer heatuator design.

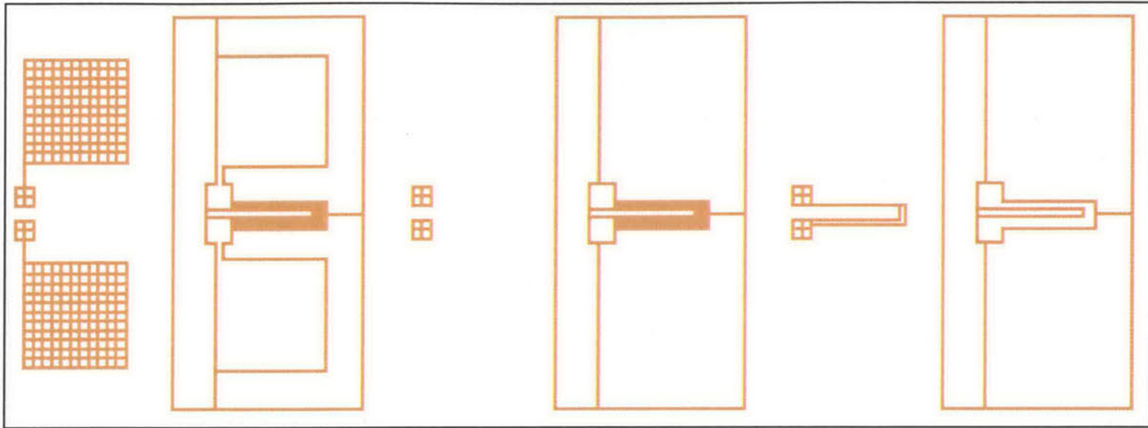

Figure 107: Overhead view of the 6-layer heatuator design with the different layers separated. Starting from the left, the 1st, 3rd, and 5th layers are release material, and the 2nd, 4th, and 6th layers are metal.

3.12 Electrostatic Motors

In addition to released structures I have also used liquid embossing to create other interesting MEMS devices. An electrostatic motor is a planar metal structure that can move objects around electrostatically. Electrostatic motors are much thinner than conventional DC motors and thus they have attracted the interest of Swatch. In collaboration with Swatch, our group has been working on creating printed electrostatic motors for use in very thin watches.

Fig. 108 shows a rotary electrostatic motor which was fabricated by inkjet printing nanocrystalline colloids *(29)*. An electrostatic motor consists of a number of different metal wires arranged perpendicular to the direction of motion. These wires are grouped together into three or more phases and each phase can be driven at a different voltage from the other phases. The motor is designed so that these phases are interdigitated with each other. A rotor composed of some dielectric material is placed on top of the motor.

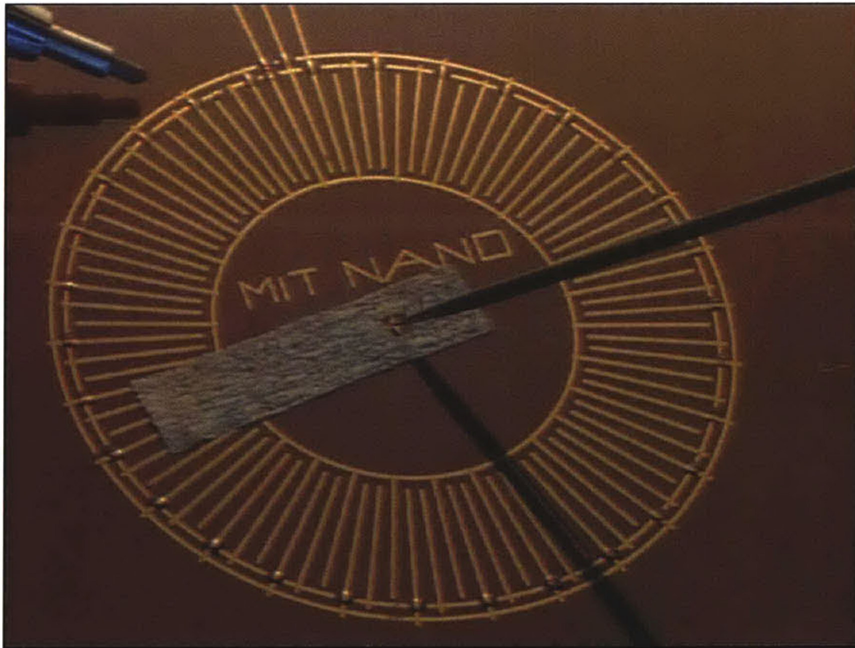

Figure 108: Inkjet printed rotary electrostatic motor. The three metal lines at the top of the image are connected to each of the three separate phases of the motor.

The motor is driven by cycling a large voltage difference through each of the different phases. Fig. 109 shows what happens when the voltage switches from one phase to another. In the first part of the figure the dielectric rotor has taken on the opposite charge of the electrode that it is sitting on. In the second part the voltage has switched so that the second phase is charged (+) and the induced voltages in the rotor have not had a chance to relax so there is a mismatch

between the rotor and the phases. In the third part the rotor physically moves over one phase in order to fix the mismatch. This procedure is repeated in order to keep the rotor continuously moving.

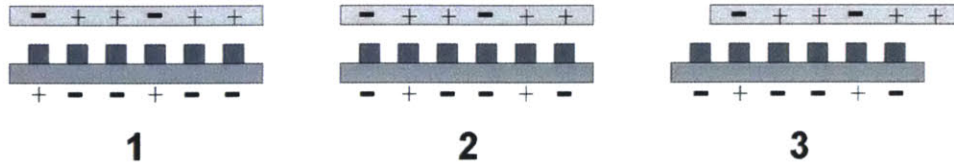

Figure 109: Schematic for how an electrostatic motor works. **1)** The dielectric rotor takes on the opposite charge of the phase that it is sitting on. **2)** The (+) voltage switches to the next phase and the rotor stays charged the way it was. **3)** The rotor is electrostatically pulled over to the next phase in order to correct the mismatch.

For the motor created by inkjet printing the individual phases were fabricated using multiple layers of material with an insulating material between each of the phases. Unfortunately, the electrostatic motor is typically driven at high voltages (>700V) so the insulating layer often broke down. For that reason, (and also to ultimately decrease fabrication cost,) I came up with a novel electrostatic motor design that had three separate phases all patterned on a single layer of material, (Fig. 110). The basic idea is that there are two phases of the motor running along the top and bottom of the motor and a third phase which snakes between these first two phases. If the yellow phase is charged and the charge then switches to the blue serpentine phase the rotor will be drawn to the right because the portion of the serpentine on the right is much thicker than the portion on the left. The force exerted upon the rotor is proportional to the area of electrostatic charge. This difference in thickness is what breaks the symmetry of the motor.

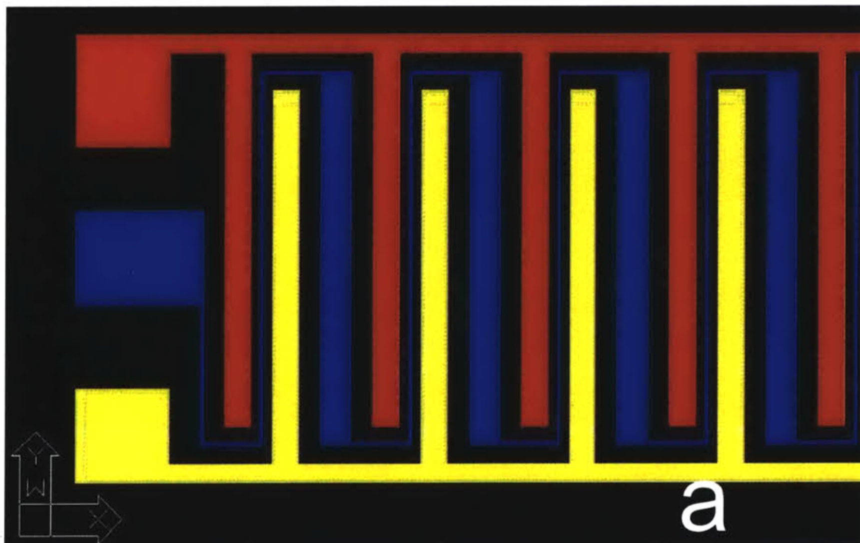

Figure 110: Schematic for the single-layer 3-phase serpentine electrostatic motor.

A linear version of this serpentine electrostatic motor was designed, (Fig. 111,) and fabricated, (Fig. 112). The motor was encapsulated with a spin-on glass in order to reduce the chance of dielectric breakdown between the phases, and a piece of tissue paper was used as the dielectric rotor. I ran the motor at 300V and succeeded in moving the tissue paper back and forth across the motor, (Fig. 113). In addition to tissue paper, I was also able to move small glass beads back and forth across the motor. This result was particularly promising since earlier motors fabricated by inkjet printing were unable to run at voltages below 700V. I am now working on building a rotary version of the serpentine electrostatic motor, (Fig. 114).

One last thing to note is that the serpentine phase of these motors stretched for 85mm over an area 5mm x 1.5mm, and the phase was only 5μm wide. This corresponds to an aspect ratio of greater than 10,000:1, and it gives an indication of how defect free liquid embossing can be.

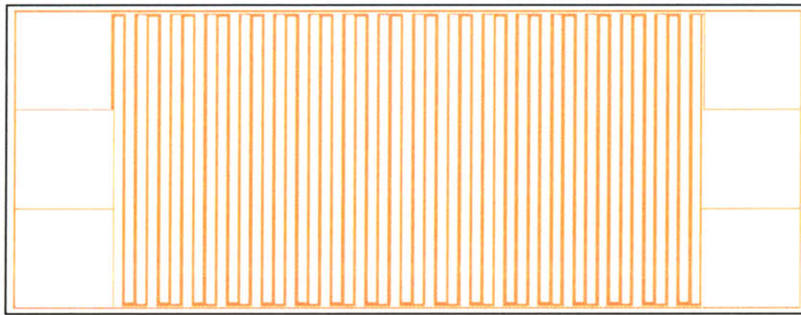

Figure 111: Overhead view of the linear serpentine electrostatic motor design.

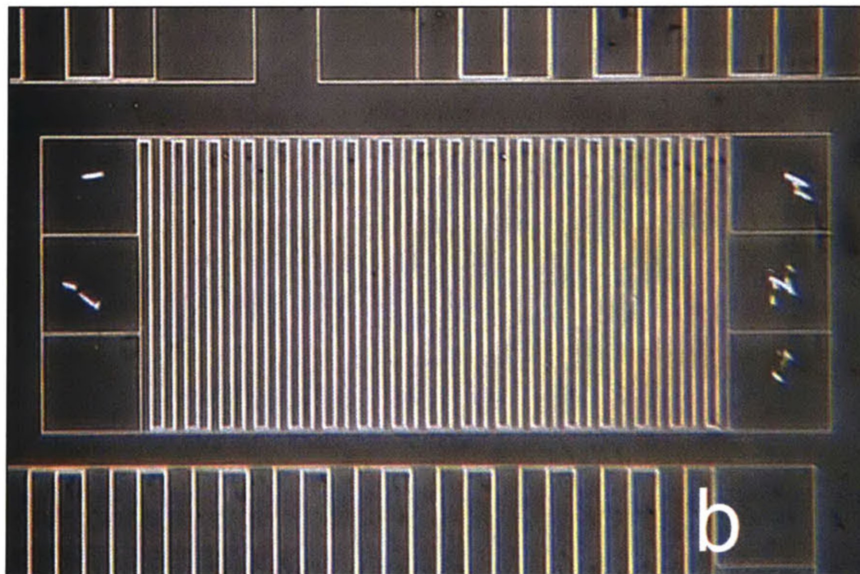

Figure 112: Overhead view of a serpentine electrostatic motor fabricated in Ag.

Figure 113: Three images from a movie which shows a piece of tissue paper, (the dielectric rotor,) being moved across the surface of a serpentine electrostatic motor.

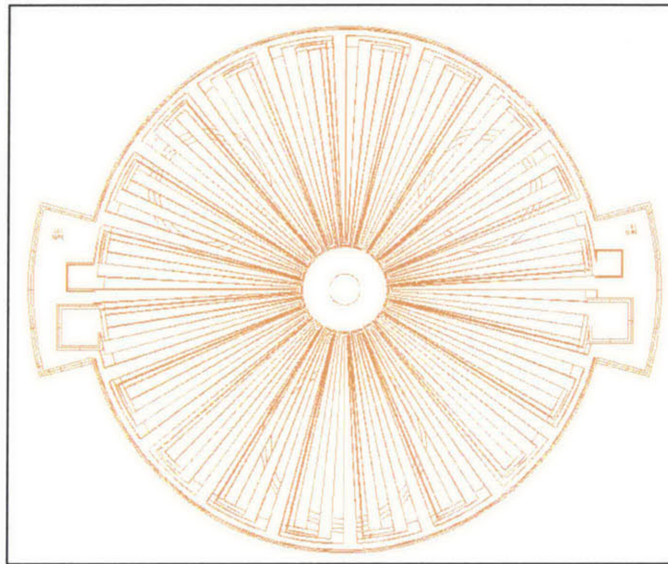

Figure 114: Overhead view of the design for a rotary serpentine electrostatic motor.

3.13 Patterned Proteins and Cells

The final area that I have explored with liquid embossing is Biology. I recently began a collaboration with MIT Professor Shuguang Zhang who has achieved some very impressive results with patterning cells, (Fig. 115). Professor Zhang has developed a number of different chemicals which can be patterned on a surface and which either promote or inhibit the growth of cells. To promote cell growth he uses a peptide sequence named RADSC14 which is attached to an alkane thiol group which in turn can be covalently bound to a Au surface. To inhibit cell growth he uses a collection of polar ethylene glycol groups attached to the end of an alkane thiol which can be bound to a Au surface *(30)*. For his previous work, Professor Zhang patterned the SAMs on a Au surface using micro-contact printing and he then grew fibroblast cells on the substrate. The cells would only attach and grow on regions of the surface that were prepared with the promoter SAM.

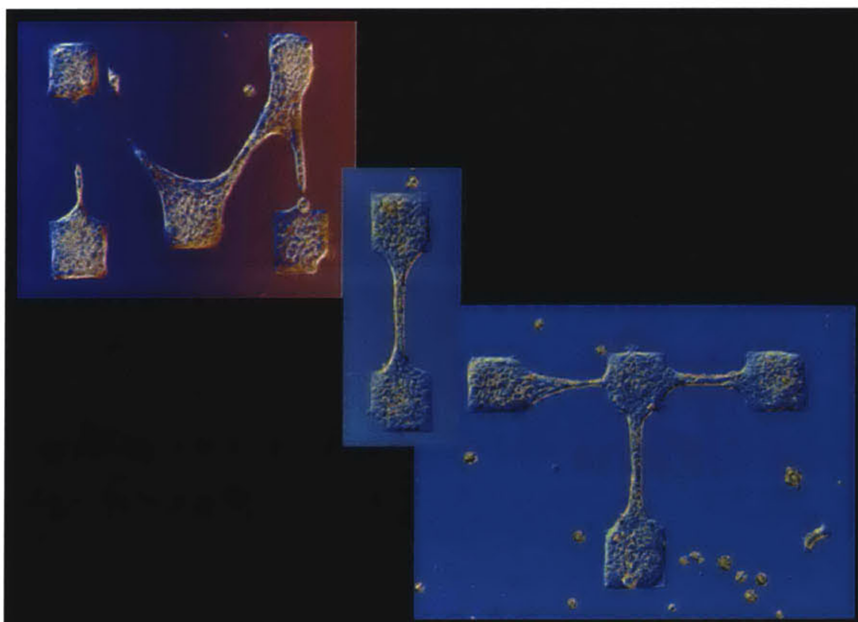

Figure 115: Previous work on patterning cells, conducted by MIT Professor Shuguang Zhang.

The problem with this previous work, and the reason why Professor Zhang chose to collaborate with us, is that the micro-contact printing technique was very prone to defects and it was impossible to create complex features with an acceptable yield. I developed a set of two techniques for patterning SAMs on a surface, (Fig. 116). In the first technique I created a substrate with a uniform coating of Au. I then liquid embossed a solution of the inhibitor SAM on the Au surface and kept the stamp in place for 5 minutes before removing the stamp and rinsing the substrate in methanol. During those 5 minutes while the stamp was in place the SAMs were able to attach to the surface, but only in the areas that were recessed in the stamp. The raised

features of the stamp selectively protected the Au surface from the SAMs. After patterning the inhibitor SAM I then coated the substrate with the promoter SAM which attached to the exposed Au regions. The SAM monolayer was far too thin to see optically and I did not have access to a Lateral Force Microscope (LFM) which is what is typically used to image SAM patterns. What I did observe though is that the SAMs changed the wetting characteristics of the substrate. While rinsing the sample with methanol I noticed that the methanol would bead up into the pattern which I had previously patterned, (Fig. 117). Although not conclusive, this was strong evidence that the SAMs had been successfully patterned.

And yet, when fibroblast cells were grown on these substrates there was no selectivity in where the cells grew, they simply grew everywhere. This confused us, and after consultation with Professor Zhang it was decided that the particular inhibitor that we were using, HSEG3, was too short to actually inhibit the cell growth. The previous work with cell patterning had been done with HSEG6 which had three more ethylene glycol groups than the HSEG3. We were unable to obtain any HSEG6 so I began exploring a second alternative technique.

The second technique that I explored did not require that the SAM be patterned directly. Instead I patterned Au on a surface and then coated the substrate with the SAM and let it selectively attach to the Au. The assumption was that the cells would be inhibited by untreated glass and thus that the cells would only grow on the Au patterns.

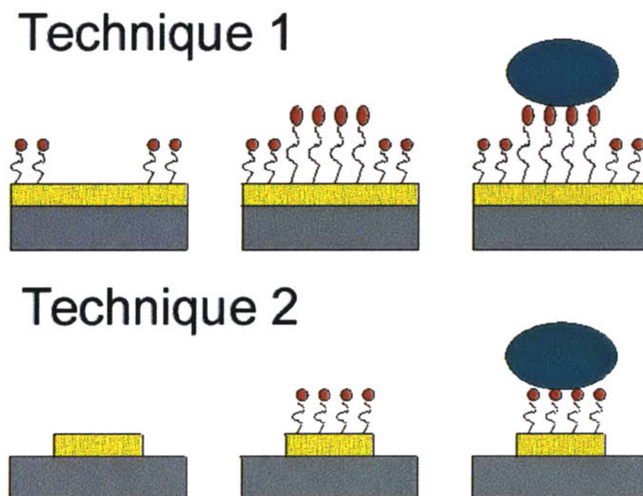

Figure 116: Schematic of two possible techniques for patterning cells on a surface. **1)** A substrate is coated with Au. A SAM of inhibitory material is patterned, and the structure is then coated in a second SAM which promotes cell growth. **2)** A film of Au is patterned on a substrate and the entire structure is then coated in a SAM which promotes cell growth.

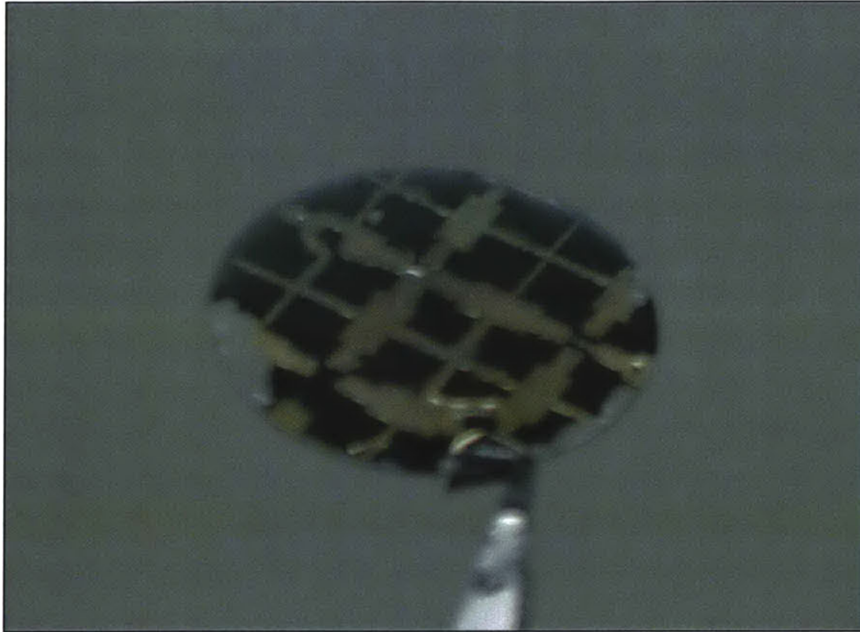

Figure 117: Photograph of methanol selectively wetting to regions of the Au coverslip which had previously been patterned by a SAM.

I was concerned that the SAMs might not be attaching correctly to the nanocrystalline based Au material, so for the first experiment I used wafers that were patterned by conventional lithography. The wafers were p-type with Au patterned on top of 200nm of thermal oxide. I coated these wafers with the RADSC14, HSEG3, and I left several of them uncoated. After coating I rinsed each wafer vigorously with methanol. In order to sterilize the substrates they were subsequently soaked in ethanol and exposed to UV. The substrates were then placed in a fibroblast cell culture and left for 3 days. Subsequent examination of the substrates revealed some very surprising results.

Fig. 118 shows cell growth on the control wafer that was not coated with either RADSC14 or HSEG3. There was no selectivity in where the cells grew, and the cells seemed perfectly happy to grow on the exposed SiO_2 surface. In comparison, Fig. 119 shows cell growth on a wafer which was coated with HSEG3. There is an incredibly sharp delineation between where the cells grew and where they did not. Fig. 120 shows 20μm Au lines upon which the cells happily grew. Fig. 121 shows a region where the cells were able to bridge across the SiO_2 in order to connect two separate Au features. What is remarkable though, is that based upon our expectations none of these results made any sense. The control experiment showed that the cells would happily grow on SiO_2, but for some reason after the substrate was coated in a SAM which should only bond to the Au the cells were suddenly unable to grow on the SiO_2. Our best theory is that the SAM interaction with the Au doesn't matter. What matters is that the hydrophobic alkane chains

on the SAMs are lying down flat on the silicon surface and forming some sort of loose waxy mesh. It is this waxy surface which is inhibiting cell growth and creating the sharply defined cell features. We will be continuing to conduct experiments to determine exactly what is going on.

Figure 118: Cell growth on Au and SiO_2. This was the control wafer and thus was not coated with a SAM.

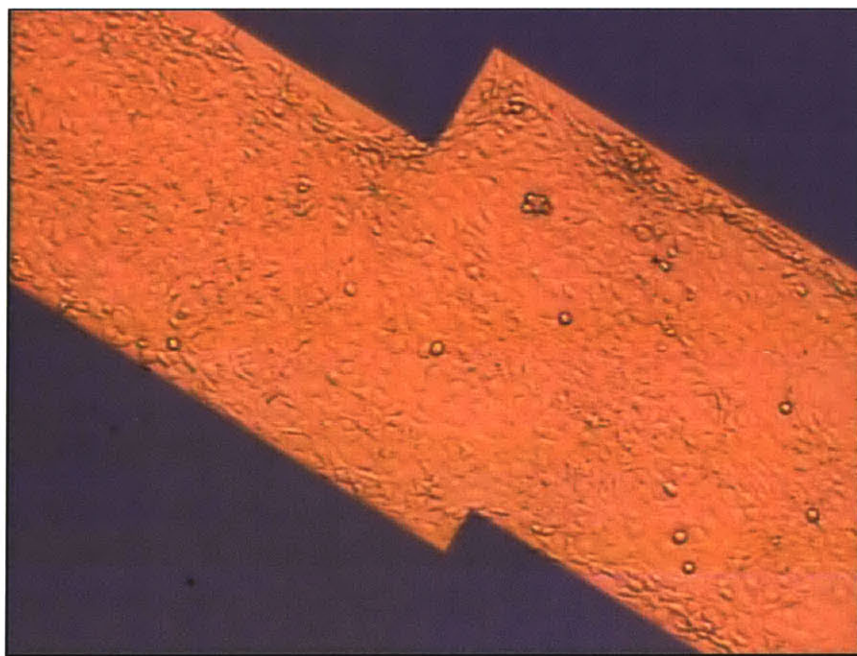

Figure 119: Cell growth on Au and SiO_2 coated in HSEG3.

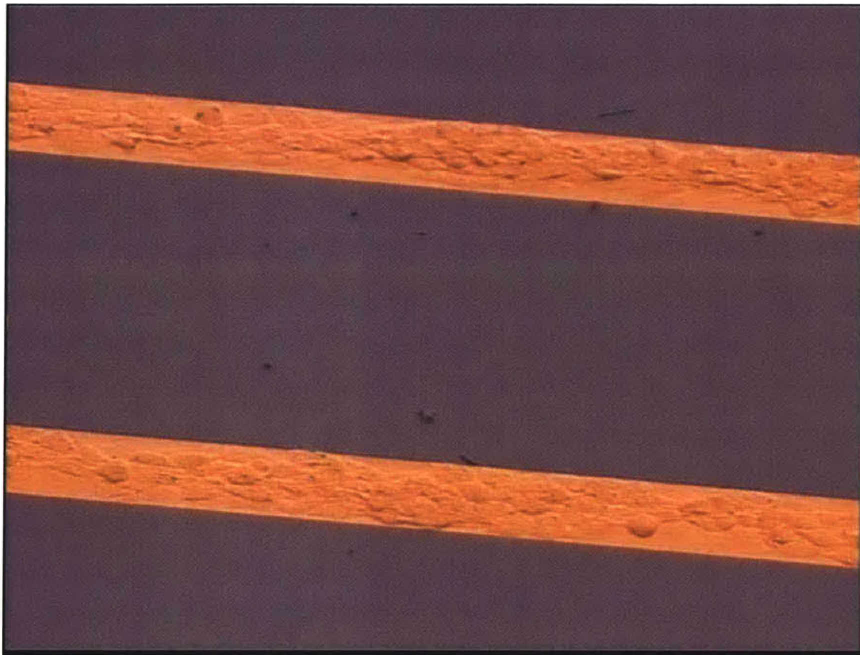

Figure 120: Cell growth on Au and SiO_2 coated in HSEG3. These features are 20μm wide.

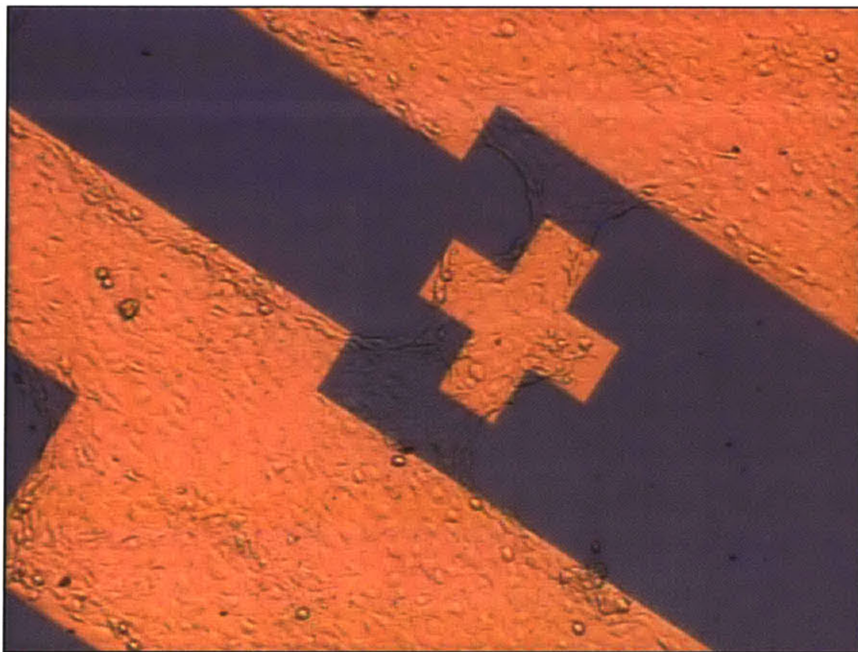

Figure 121: Cell growth on Au and SiO_2 coated in HSEG3. Cells were able to bridge across the 20μm that separated the Au features.

4.0 Conclusion

The rapid and additive fabrication of transistors, photodetectors, resistors, sacrificial layers and vias demonstrates the practical utility of liquid embossing. Although I have primarily focused my work on the patterning of inorganic nanocrystal solutions for microelectronics, I have also shown that liquid embossing can be used in the fabrication of micro-mechanical systems and biological chips. The ability of liquid embossing to pattern arbitrary liquids at resolutions below a micron should have broad applicability in a wide number of fields.

With liquid embossing it should be possible to directly integrate devices which have widely different materials and properties. For example, the ability to pattern transistors and MEMS with the same process should hopefully make it easier to create integrated mechanical and electrical microsystems. Or another possibility would be the creation of an ultra low-cost diagnostic chip which integrates a patterned protein surface with the electronics needed to analyze the resulting signal.

The ability to emboss many layers of functional materials is another intriguing notion. No technique exists to date which can fabricate true three dimensional logic and machines. Liquid embossing is very promising though since it can pattern multiple layers of material without the need for an external planarization step. As the technique matures it should be possible to create devices with many layers of interconnected transistors. These three dimensional architectures will be particularly well suited to simulating complex three dimensional environments such as fluid dynamics or neuronal interconnects.

And yet, the most promising field for liquid embossing is almost certainly the fabrication of ultra low-cost electronics. Current silicon costs more than $4 per square inch. This cost prohibits the possibility for very large area displays or disposable electronics. Liquid embossing on the other hand can pattern electronics for pennies per square inch. At that cost it should be possible to make computational intelligence pervasive. For example, every product in a kitchen could have a unique RFID tag which the kitchen as a whole could identify. The kitchen would know when you are running low on sugar, or when the milk has gone bad. The possibilities are virtually limitless.

To date, liquid embossing has demonstrated all of the constituent elements for logic, micromechanics, and biochips. The task now is to begin combining these elements together to form interesting and useful devices.

References

1. Y. Xia, and G. M. Whitesides, Annu. Rev. Mater. Sci. **28**, 153 (1998).
2. P. G. Carey, P. M. Smith, S. D. Theiss, P. Wickboldt, and T. W. Sigmon, SPIE Proceedings, **3636**, 4 (1999).
3. S. Chou, P. Krauss, P. Renstrom, Science **272**, 85 (1996).
4. L. Guo, P. R. Krauss, and S. Y. Chou, Appl. Phys. Lett. **71**, 1881 (1997).
5. Z. Yu, S. J. Schablitsky, and S. Y. Chou, Appl. Phys. Lett. **74**, 2381 (1999).
6. A. Kumar, H. A. Biebuyck, and G. M. Whitesides, Langmuir **10**, 1498 (1994).
7. Y. Xia, X-M. Zhao, E. Kim, and G. M. Whitesides, Chem. Mater. **7**, 2332 (1995).
8. Y. Xia, E. Kim, and G. M. Whitesides, J. Electrochem. Soc. **143**, 1070 (1996).
9. Y. Xia, E. Kim, M. Mrksich, and G. M. Whitesides, Chem. Mater. **8**, 601 (1996).
10. L. B. Goetting, T. Deng, and G. M. Whitesides, Langmuir **15**, 1182 (1999).
11. T. K. Whidden *et al.*, Nanotechnology **7**, 447 (1996).
12. D. Wang, S. G. Thomas, K. L. Wang, Y. Xia, and G. M. Whitesides, Appl. Phys. Lett. **70**, 1593 (1997).
13. P. M. St. John, and H. G. Craighead, Appl. Phys. Lett. **68**, 1022 (1996).
14. J. Hu *et al.*, Appl. Phys. Lett. **71**, 2020 (1997).
15. J. Hu, R. G. Beck, R. M. Westervelt, and G. M. Whitesides, Adv. Mater. **10**, 574 (1998).
16. N. L. Jeon, J. Hu, G. M. Whitesides, M. K. Erhardt, and R. G. Nuzzo, Adv. Mater. **10**, 1466 (1998).
17. E. Kim, Y. Xia, and G. M. Whitesides, Nature **376**, 581 (1995).
18. J. A. Rogers, Z. Bao, and V. R. Raju, Appl. Phys. Lett. **72**, 2716 (1998).
19. C. Marzolin, S. P. Smith, M. Prentiss, and G. M. Whitesides, Adv. Mater. **10**, 571 (1998).
20. O. Schuler, G. M. Whitesides, J. A. Rogers, M. Meier, and A. Dodabalapur, Appl. Optics **38**, 5799 (1999).
21. N. L. Jeon, I. S. Choi, B. Xu, and G. M. Whitesides, Adv. Mater. **11**, 946 (1999).
22. W. S. Beh, I. T. Kim, D. Qin, Y. Xia, and G. M. Whitesides, Adv. Mater. **11**, 1038 (1999).
23. B. A. Ridley, B. Nivi, and J. M. Jacobson, Science **286**, 746 (1999).
24. Mat. Res. Soc. Symp. Proc. **581**, 115 (1999).
25. Mat. Res. Soc. Symp. Proc. **625**, 135 (2000).
26. H-C. Scheer, H. Schulz, T. Hoffmann, and C.M. Sotomayor Torres, J. Vac. Sci. Technol. *B* **16**, 3917 (1998).
27. D. B. Thomasson, M. Dayawansa, J. H. Chang, and T. N. Jackson, IEEE Electron Device Letters, **18**, 117 (1997).
28. R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and P. Avouris, Applied Physics Letters, **73**, 2447 (1998).
29. S.B. Fuller, J.M. Jacobson, Proc. of IEEE MEMS 2000 Conf. (2000).
30. S. Zhang et al, Biomaterials, **20**, 1213 (1999).

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Figure 122: Starting from the left: Myself, Kim Hamad, Brent Ridley, Brian Hubert, Saul Griffith, Dave Mosley, Murray Whitehead, Eric Wilhelm, and Joe Jacobson.