Electrical Degradation of InAlAs/InGaAs Metamorphic High-Electron Mobility Transistors

by
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Submitted to the Department of Electrical Engineering and Computer Science in Partial Fulfillment of the Requirements for the Degree of Master of Science in Electrical Engineering at the Massachusetts Institute of Technology

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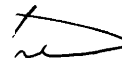

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Abstract

InAlAs/InGaAs metamorphic High Electron Mobility Transistors (HEMT) hold promise for power-millimeter wave applications. A major reliability concern in some of these devices is the degradation of the drain resistance that is observed when the device is electrically stressed for a long time at bias conditions necessary for power applications. The goal of this thesis was to find the physical origin of this reliability problem and to suggest solutions to it. State-of-the-art InAlAs/InGaAs metamorphic HEMTs, provided by our sponsor, Hewlett Packard, were stressed under different bias schemes. It was found that most figures of merit associated with the drain-side of the device degrade under severe bias stress. In particular, the drain resistance, R_D, has been found to increase significantly. In order to understand the physical origin of this degradation, we have studied the degradation of simpler Transmission Line Model (TLM) structures. We have found that in TLMs and HEMTs there appear to be two different degradation modes, both associated with hot electrons. In the first degradation mechanisms, we postulate that hot electrons are trapped by defects at the interface between the GaAs etch-stopper and the AlInAs Schottky barrier layer, depleting the carrier concentration in the channel underneath. In the second mechanism hot electrons degrade the InGaAs ohmic contacts. No degradation mechanism associated with the metamorphic nature of the structure has been identified.

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Chapter 1

Introduction

1.1. Introduction to InAlAs/InGaAs mHEMTs

InAlAs/InGaAs High Electron Mobility Transistors (HEMT), also known as Modulation Doped Field Effect Transistors (MODFET) have started to fulfill their promises for low-noise and power millimeter-wave applications that results from their extremely high frequency response. The major issues that have to be resolved before these devices can live up to their expectations can be found in the areas of reliability and manufacturing.

The devices studied in this thesis are called metamorphic HEMTs, as the active structure of the device is lattice matched to InP while the substrate is GaAs. This reduces the costs of the substrate significantly and allows the use of a larger diameter wafer. Since these devices have a lattice constant of InP and are grown on a substrate with a different lattice constant, a linearly graded buffer layer has to be grown. This buffer has the lattice constant of GaAs on the bottom and the lattice constant of InP on top and adapts to this without introducing too many defects into the structure. Fig. 1-1 shows a sketch of the structure. In this sketch, both the supply layers are δ-doped to form a 2D-Electron Gas in the channel, none of the HP devices are δ-doped. The channel in these devices has a high In-content in the channel to improve the electrical characteristics, because the electron

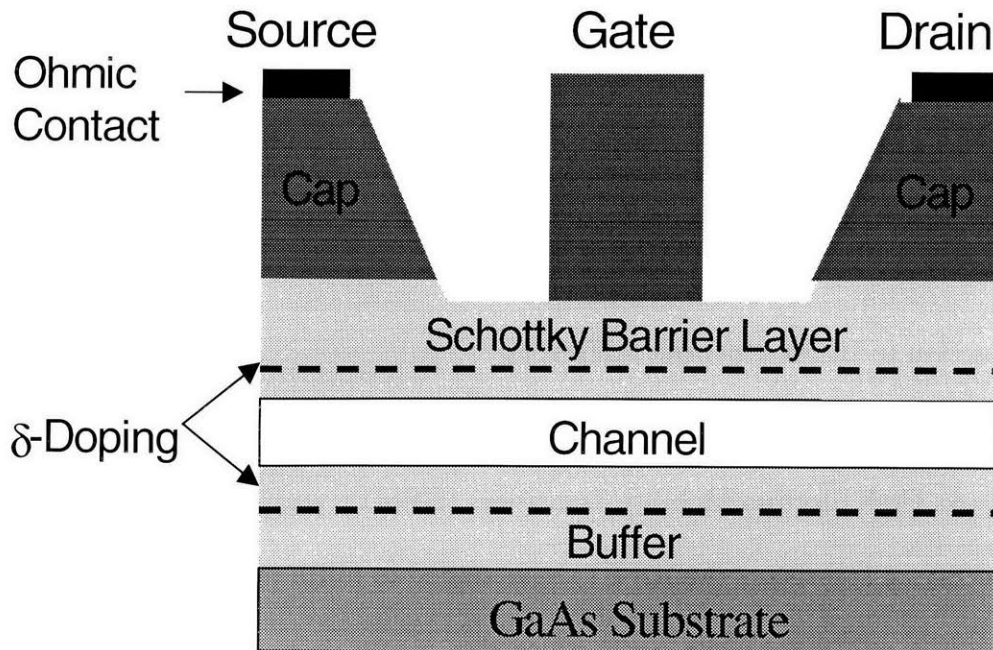


Fig. 1-1: Sketch of a metamorphic HEMT with dopants in the buffer and the insulator.

velocity increases with the In-content ([1] and [2]). This material system currently holds the world record, amongst all three-terminal devices, for the highest cut-off frequency f_T= 350 GHz [3] and the highest maximum frequency of oscillation f_{max}= 600 GHz [4].

1.2. Motivation

High power is an important specification for these devices. Therefore they have to be able to withstand high bias voltages and allow high currents. The aggressive mode of operation for these devices makes reliability issues very important. The high currents and fields cause several degradation and failure mechanisms to occur ([5] and [6]).

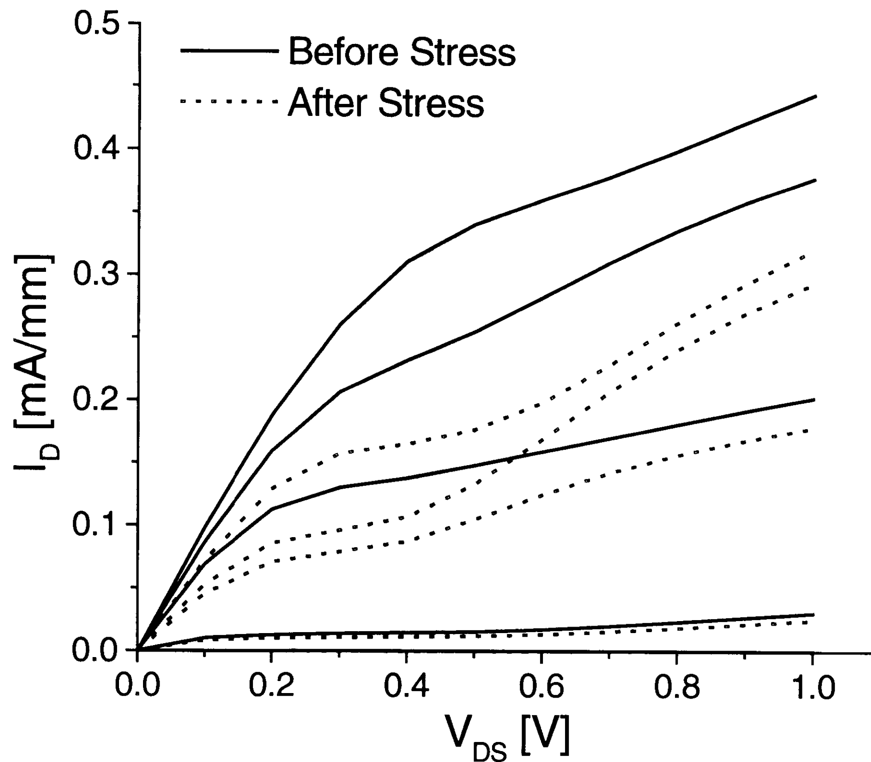


Fig. 1-2: Drain Current I_D vs. The Drain-Source Voltage V_{DS} before and after electrical stress was applied to a mHEMT. The device from wafer 453S036 was stressed at a constant V_{DGo}=1.5 V and a constant I_D=250 mA/mm for 714 minutes.

This thesis will cover the soft degradation of a specific type of mHEMTs produced by electrical stressing, as reported by Wakita et al. [7], which is most significantly characterized by a significant increase of the drain resistance. This degradation mode may not critically damage the device, but it does hinder its use in the intended applications, as can be seen on Fig. 1-2. This figure shows the I-V characteristics of a device before and after having been biased at a relatively moderate bias point at room temperature for some time. One can see that the low field resistance has increased significantly. The drain currents have also degraded significantly and a kink has appeared. Understanding this damage and suggesting strategies to mitigate it is the goal of this thesis.

1.3. Review of electrical stressing of InAlAs/InGaAs HEMTs

Virtually all aspects of InP-based HEMTs have been observed to degrade under electrical stress. The variety of reported degradation mechanisms is almost as big as the variety of material structures and metallizations that are used in the fabrication of HEMTs. Amongst the different degradation mechanisms that have been reported the most important are described in the following paragraph.

Schottky gate contact degradation, due to metallurgical interactions, has been reported for different HEMT structures [8]. In particular, gate sinking has been seen for many structures [9]. In this mechanism the gate metal diffuses into the Schottky-barrier layer, causing the threshold voltage to shift and the drain current to degrade [10]. The ohmic contacts have also been found to be prone to degradation because of hot electrons in the Gate-drain region [11]. Surface degradation, caused by hot electrons has also been reported as a mode of degradation [12]. Deterioration of the InAlAs surface has also been reported as a cause of drain current degradation for InP lattice matched HEMTs [13]. If the surface layer is not passivated, the Al diffuses out of the lattice to oxidize at the surface as reported in [13]. Fluorine-contamination from the air has also been seen as a failure mechanism [14], where the F decreases the sheet carrier concentration. The diffusion of Ti in the AlInAs layer has also been reported to have a similar effect [15]. The crystalline structure of the channel and the isolation layer can also degrade under certain circumstances [16]. This degradation causes the mobility in the channel to degrade, which is reported to only occur if the layers are lattice matched to InP [16].

Other authors claim to have fabricated very reliable devices, with an InP lattice matched structure, with lifetimes of 4×10^{11} h [17], using alloyed ohmic contacts.

1.4. Outline of Thesis

The thesis will be organized in the following way. Chapter 2 contains a presentation of the data obtained through electrical stress experiments on mHEMTs using different stressing schemes. We will discuss how we selected one of these schemes to be physically the most revealing. This chapter will be concluded by a presentation of the time evolution during stress and bias-dependence of the key figures of merit during stress. The bias dependence of the degradation of the different figures of merit will also be shown in this chapter. Out of this data we conclude that the drain resistance is the figure of merit that is most affected by the degradation. We also find indications that several degradation mechanisms seem to be taking place.

In chapter 3, we will show the results of degradation experiments performed on Transmission Line Method structures, TLMs. They have the same material structure as the mHEMTs, but no gate has been fabricated. A TLM is basically a channel, contacted by two ohmic contacts a certain distance apart, acting like an integrated resistor. These experiments enabled us to better isolate the physics of degradation. Electrical and thermal degradation experiments are here explained and a summary of the results is given.

Chapter 4 contains the discussion of the different experimental results. The results of stress experiments on both TLMs as mHEMTs with different material structures are

reported in this chapter. The differences in degradation that are observed are then related to their physical cause This gives us an insight in the origin for the observed degradation of both mHEMTs as of TLMs. A description of the two degradation mechanisms concludes this chapter.

Chapter 5 concludes this thesis with a description of the identified degradation mechanism. It also contains some suggestions for further work in this research topic.

Chapter 2

Degradation of HEMTs

2.1. Introduction

The state-of-the-art InAlAs/InGaAs mHEMTS, provided by our sponsor Hewlett-Packard, have been found to degrade under bias stress, as reported by Wakita et al [7]. The dominant degradation mode that has been observed affects the drain resistance R_D. The physical origin of this degradation is not well understood. Other figures of merit than the drain resistance have also been found to degrade, so there is a need for detailed characterization of these devices during stress. The breakdown of these devices has been reported in [18], but this thesis has not studied this aspect of the device reliability.

This chapter describes detailed electrical stress-experiments that we performed on these mHEMTs. We have developed an automated measurement setup to stress the mHEMTs and measured several key figures of merit during the stress. This chapter starts with a description of the set-up and the measurement suite. Then we will present the results we obtained using different stressing schemes.

2.2. Device Technology

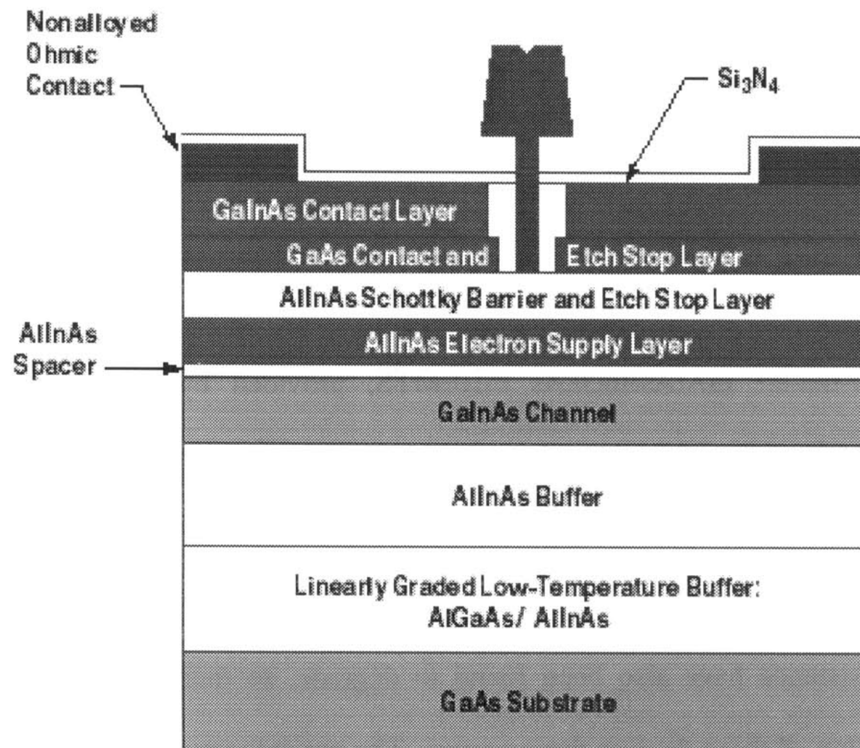


Fig. 2-1:Sketch of the InAlAs/InGaAs mHEMT studied in this thesis. The figure is adapted from [20] courtesy of H. Rohdin.

A cross-section of the devices that have been tested can be seen on Fig. 2-1. ([19] and [20]). The epitaxial structure is grown by Molecular Beam Epitaxy on a GaAs substrate. A linearly graded low-temperature buffer allows the growth of an undoped $Al_{0.52}In_{0.48}As$ buffer with the lattice constant of InP on this substrate [21]. The active channel is made out of $In_{0.53}Ga_{0.47}As$. A heavily doped $Al_{0.52}In_{0.48}As$ electron supply layer is grown above the channel, separated by an undoped thin $Al_{0.52}In_{0.48}As$ spacer layer, to provide the carriers in the channel. Above the supply layer, an $Al_{0.52}In_{0.48}As$ schottky barrier and etch-stop layer are grown. The cap structure consists of a heavily-doped GaAs and $In_{0.53}Ga_{0.47}As$. The GaAs etch stop layer is the only layer in the epitaxial structure above the buffer that is not lattice matched to InP. The ohmic contacts are non-alloyed tunneling

contacts. The device features a 0.12 μm T-gate that is defined using e-beam lithography [22]. The gate width W_g of these devices is 120 μm.

A typical virgin device has a current gain cut-off frequency f_T of 150 GHz. The extrinsic transconductance is g_{mpeak}=1065 mS/mm. The output conductance is g_o=75 mS/mm. These values are measured at V_{DS}=1.3 V and V_{GS} at the peak of the transconductance curve, V_{Gspeak}=-0.09 V. The current at V_{GS}=0 V, for V_{DS}=1.3 V is I_{DSS} = 370 mA/mm with a maximum drain current I_{max} of 790 mA/mm. The off-state breakdown voltage BV_{DGoff} of this device is 4.75 V. The threshold voltage V_T is -0.38 V. Before stressing, a typical value for the drain resistance is R_D=0.29 Ω.mm, while the source resistance is R_S=0.26 Ω.mm. Fig. 1-2 shows a set of virgin output characteristics.

2.3. Stress and Measurement Set-up

To study the degradation of the mHEMTs we developed a stress and measurement setup, which enables us to stress a device under a variety of conditions, while monitoring its key parameters. At first, we developed a measurement suite that characterizes a device as completely as possible without causing degradation. Early on, it was established that this stress and measurement set-up should be completely automated to make long stressing experiments possible. Two experimental installations were realized, the set-up developed at MIT was copied and improved on at HP Santa Rosa. A detailed description of the two stress and measurement set-ups will now be given, followed by a description of the characterization suite that was used.

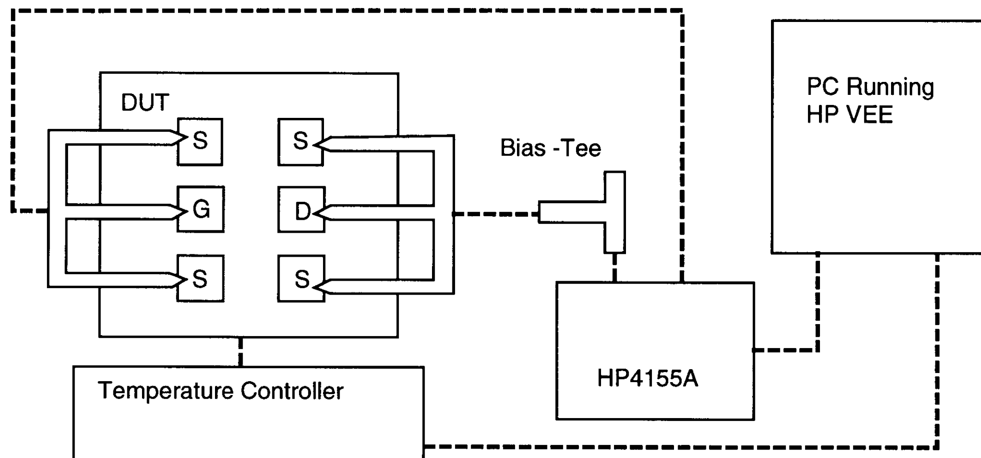


Fig. 2-2: Scheme of the stress and measurement set-up installed at MIT.

2.3.1. The Experimental Installation

Fig. 2-2 shows a scheme of the set-up as installed at MIT. A similar set-up has been built at HP Santa Rosa, as can be seen on Fig. 2-3. At MIT, the device is probed on a Cascade Microtech probe station using Cascade GSG 150 coplanar microwave probes. This probe station encapsulates the sample, so it can be degraded in a N2 environment. A

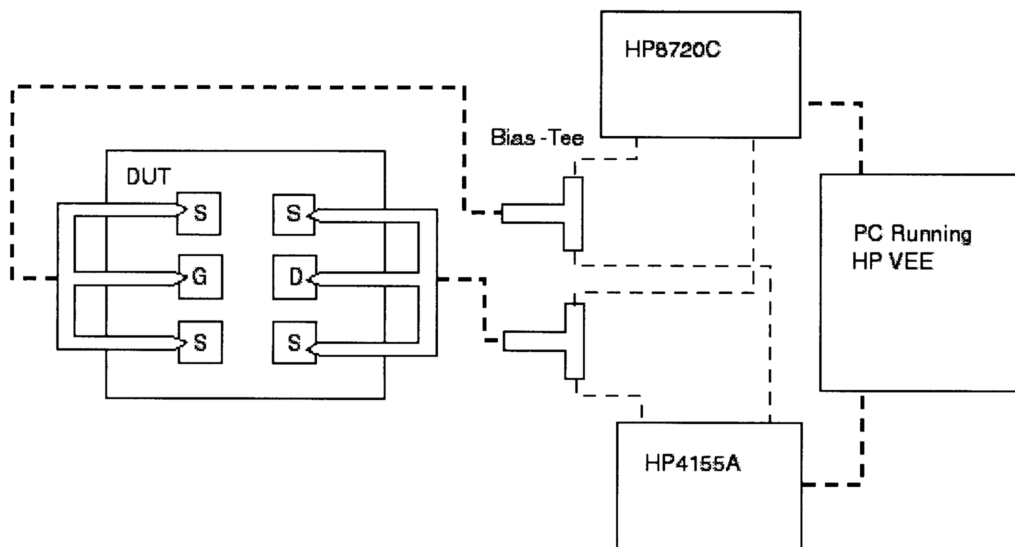


Fig. 2-3: Scheme of the stress and measurement set-up installed at HP Santa Rosa.

Temptronic temperature controller is installed, which can set the temperature of the chamber between –65 and 200 °C. A HP4155A semiconductor parameter analyzer is used to make DC measurements of the device and to stress it. A bias-tee is put on the drain to reduce oscillations in the DC signal. A PC running HP VEE with a HP82341C network card is used to control the measurements.

The set-up at HP Santa Rosa differs as the probe station is a Rucker&Kolls Model 260 Probe station. This probe station does not encapsulate the sample. A HP8720C network analyzer has been added to make RF measurements possible. Low series resistance bias tees are used on both gate and drain to separate the DC and RF signals while reducing oscillations.

We wrote a program in HP VEE 4.0 to automatically run a complete stress and measurement experiment. This involves stressing the device under certain bias conditions, while performing a complete characterization measurement suite at certain time intervals. This requires minimal input from the operator. Once the set-up is completely hooked up, everything can run automatically without any intervention. The program starts by characterizing the device prior to stressing it. Every piece of data that is collected during the experiment, is saved away in different text-files. The program extracts automatically the key figures of merit and bundles them in one separate file, to allow for quick and easy data processing.

We have also written a program that reads a data file generated by the stress and measurement software and displays an animation of how the I-V, gd-V and transfer

characteristics change in time during stress. This provides a new tool to see degradation. The time interval can be specified and the display scaled, to view a region of interest, for example the knee region or near pinch-off versus time. This enables us to see the evolution of a whole set of characteristics instead of just one figure of merit.

2.3.2. The Characterization Suite

The goal of this measurement suite is to characterize the device as completely as possible, without degrading it. A device that has not been probed is very sensitive to almost any measurement. Therefore some measurements are only executed after a few minutes of stressing, after which they do not degrade the device in a measurable way. The benchmark is that ten successive measurements should not affect the device characteristics. We will now go over the different figures of merit that have been characterized.

2.3.2.a I-V Characteristics

At first a set of I-V curves is measured by sweeping V_{DS} from 0 to 1 V, while stepping V_{GS} from –0.6 to 0.2 V. This allows a more global analysis of the degradation. A typical set of I-V characteristics can be seen on Fig. 1-2.

2.3.2.b. Resistance Measurements

The measurement schemes for the different resistances are shown on Fig. 2-4. The drain resistance R_D is measured by sweeping the drain current I_D from –83 to -4 mA/mm, while synchronously stepping the gate current I_G=-I_D. The ratio of V_{DS} to I_D is the resistance of

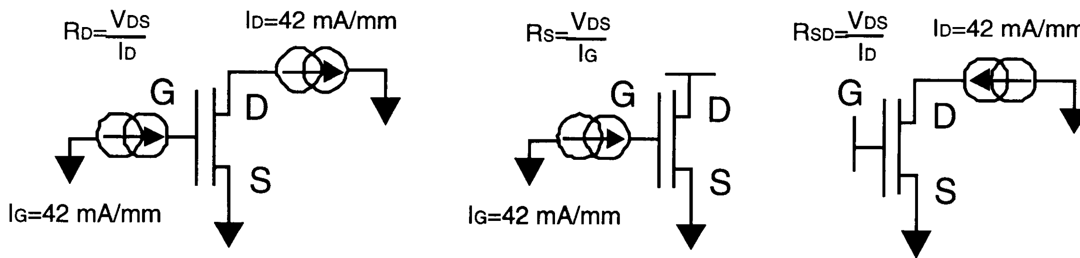


Fig. 2-4: Schematics for different resistance measurements in the characterization suite. A) The drain resistance R_D measurement, B) The Source Resistance R_S measurement and C) The total resistance R_{SD} measurement.

the drain, as no current flows through the source. The program corrects the resistance by subtracting the external series resistance. This external series resistance is measured separately during a calibration of the test system. R_D is defined at I_D=-43 mA.

The source resistance R_S is measured by sweeping I_G from 4 to 83 mA/mm with I_D=0 and measuring V_{DS} using voltage monitors. At high enough I_G, the ratio of V_{DS} to I_G approaches R_S. The value of R_S at I_G=43 mA/mm is the reported value.

The total resistance R_{SD} is extracted by sweeping I_D from 4 to 83 mA/mm, while keeping the gate floating, as can be seen on Fig. 2-4. By measuring V_{DS}, R_{SD} can be calculated as the ratio of V_{DS} to I_D. The value of R_{SD} at I_D=43 mA/mm is reported.

2.3.2.c. Transfer Characteristics

The transfer characteristics are measured by sweeping V_{GS} from –0.7 to 0.2 V, while keeping V_{DS} constant at 1.3 V. An example of the transfer characteristics can be seen on Fig. 2-5.

The program also extracts the peak transconductance g_{mpeak} from the transfer characteristics, as can be seen on Fig. 2-5. g_{mpeak} is defined as the maximum value of $g_m=dI_D/dV_{GS}$.

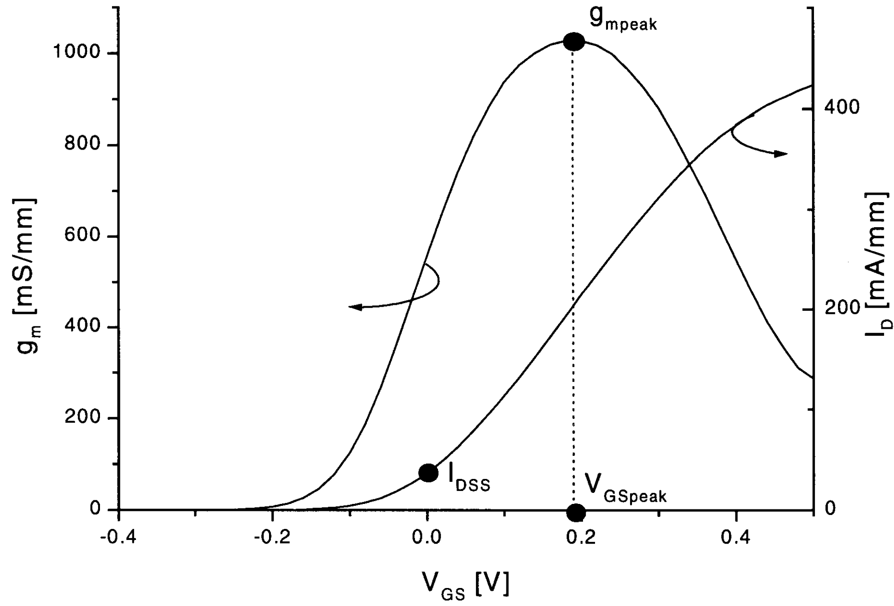


Fig. 2-5: Transfer characteristics of a 4μm S-D m-HEMTs from wafer 515S032 after 120 s of stressing at V_{DGo}= 1.65 V and I_D= 250 mA/mm.

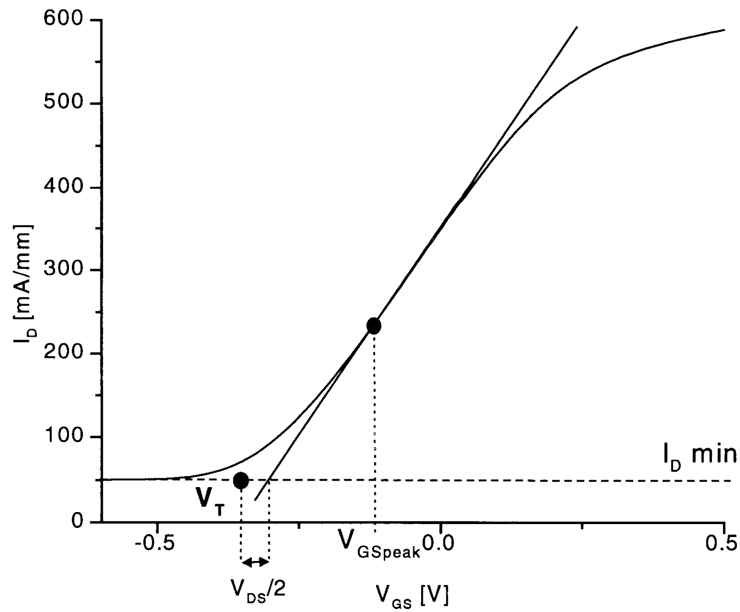


Fig. 2-6: Definition of VT as the intersection between the tangent of the inflection point of the ID-VGS characteristics for VDS=0.1 V and ID=ID(min) corrected by VDS/2.

The program extracts I_{DSS} from the transfer characteristics. I_{DSS} is the value of the drain current I_D for V_{GS}=0 V as can be seen on Fig. 2-5.

I_{max} is a measure for the maximum drain current for this device. I_{max} is measured by finding the value of I_D at V_{DS}= 1.3 V and V_{GS}=0.75 V.

The threshold voltage V_T is being measured by sweeping V_{GS} from –0.7 to 0.2 V, while keeping V_{DS} constant at 0.1 V. It is defined as the intersection between the tangent of the inflection point of the I_D-V_{GS} characteristics for V_{DS}=0.1 V and I_D=I_D(min) corrected by 0.05 V [20]. Fig. 2-6 illustrates this definition.

2.3.2.d. Output Conductance g_o

The output conductance g_d is being measured at V_{DS}=1.3 V and V_{GS}=V_{Gspeak}, with V_{GSpeak} the value of V_{GS}, where the maximum of g_m is found, as can be seen on Fig. 2-7.

2.3.2.e. Kink-related Metrics

To study devices that show a kink in their output characteristics, as can be seen on Fig. 1-2, some kink-related figures of merit were introduced. These are measured for V_{GS}=V_{GSpeak}. Fig. 2-7 shows some of these figures on a g_o-V_{DS} curve for a device that shows a kink. If no kink is present, no local minimum can be found for V_{DS} > 0 V. The metrics for the kink are the difference and the ratio of the value of g_o at the maximum of the kink to the value of g_o in the local minimum before the kink, which is a global knee-metric.

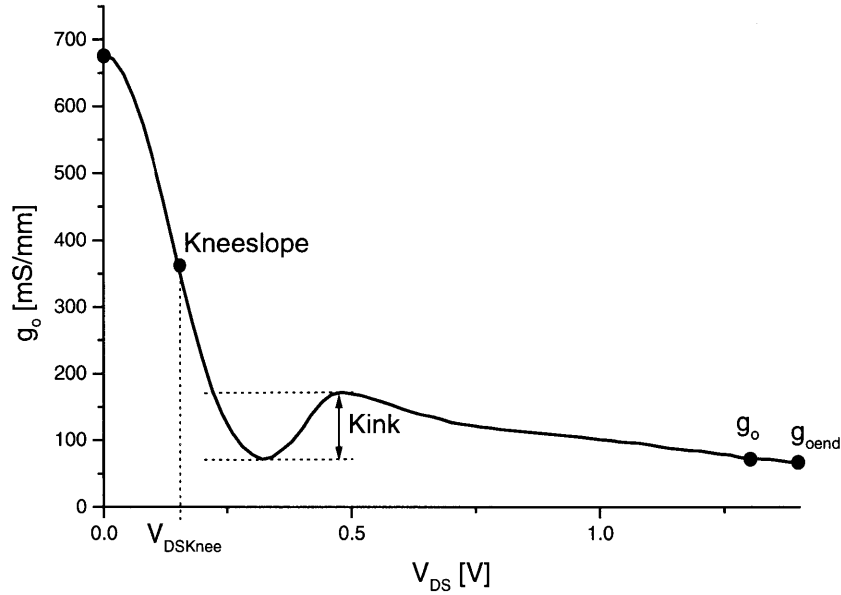


Fig. 2-7: Locations of the different kink and knee-related figures of merit on a measured g_d-V_{DS} curve for V_{GS}=V_{Gspeak} (the value that corresponds to a peak g_m) from a device of wafer 453S036.

2.3.2.f. Knee-related Metrics

We are also tracking some figures of merit to describe the quality of the knee of the I-V curve. Fig. 2-7 shows the location of the knee-related metrics on a g_0-V_{DS} curve. We measure the knee at V_{GS}=V_{GSpeak}. We can define the knee-voltage V_{DSKnee} as the inflection point of g_o in function of V_{DS}, i.e. the point where $d^3I_D\backslash dV_{DS}{}^3= 0$. The slope of the output conductance g_o (= $d^2I_D\backslash dV_{DS}{}^2$) in the knee-point is another metric we measure. This figure reflects the local sharpness of the knee.

2.3.2.g. Ideality Factors of Source and Drain Diodes n_{dd} and n_{sd}

We also measure the ideality factors of the source-gate and the drain-gate diode, n_{sd} and n_{dd}. We evaluate these metrics by measuring the I-V characteristics of the gate-to-source and the gate-to-drain diodes separately. For the gate-to-drain diode measurement, this

involves sweeping I_D while keeping I_G=-I_D. These curves are then fitted to the equation $I \approx I_S.\exp(qV/nkT)$ and n is extracted.

2.3.2.h. S-Parameters

At HP Santa Rosa we were also using the HP8720C to measure the S-parameters of the mHEMT during stressing. During this measurement a bias point of V_{DS}=1.3 V and V_{GS}=V_{GSpeak}. The S-parameters are measured by averaging over 12 sweeps from 1 to 20 GHz. These S-parameters were converted to Y-parameters. Using the model of [23] C_{gd} is then calculated out of the imaginary part of Y_{12}. The value of C_{gd} is an average of the measured values from 2 to 6 GHz.

f_T was also measured by calculating the absolute value of h_{21} for different frequencies. By extrapolation, the frequency for which $|h_{21}|$ =1 is found and this is called f_T.

2.3.2.i. The Off-state Breakdown Voltage BV_{DGoff}

The off-state breakdown voltage BV_{DGoff} was measured by the drain-current injection technique [24]. A drain current of 0.25 mA/mm is injected and V_{GS} is swept from 0 to –1.2 V.

2.4. Stressing Schemes

Using a PC to run the stressing experiment allows for different stressing schemes that go beyond the capabilities of the HP4155A. We will now go over the several schemes we have explored.

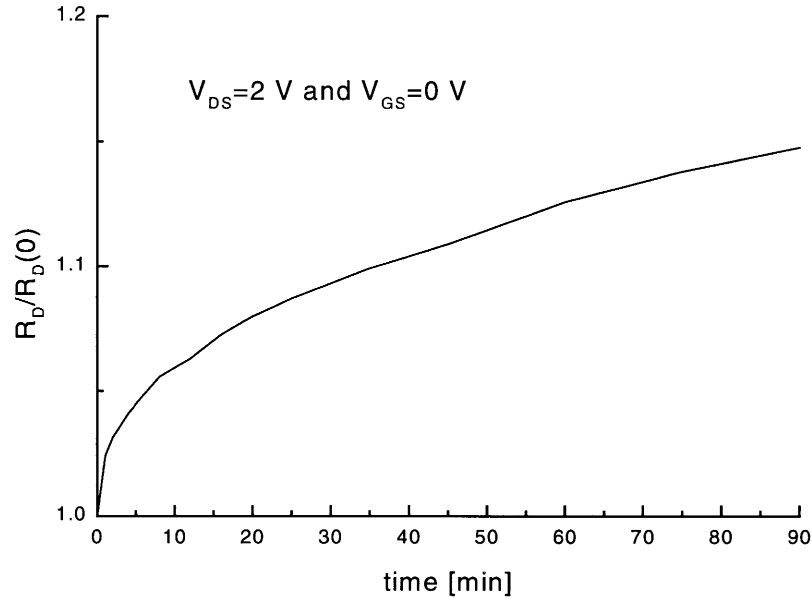


Fig. 2-8: Time evolution of the drain resistance R_D (normalized to its value at t=0) of a device from wafer 453S036.

2.4.1. Constant V_{DS}-Constant V_{GS}

We started by using the stressing scheme from [7], which is a constant V_{DS}-constant V_{GS} scheme. This is executed easily, but as R_D increases as can be seen on Fig. 2-8, the internal drain bias decreases. So during stress, I_D decreases significantly. Additionally V_{DS} and V_{GS} are not as physically meaningful. [7] concluded that impact-ionization was the cause of R_D degradation. However, this stressing scheme does not keep the amount of impact-ionization or even the internal fields in the device constant.

2.4.2. Constant I_D-Constant I_G

Another approach is to keep I_D and I_G constant. This is physically more meaningful if impact ionization is behind device degradation. It has been reported that a constant I_G implies a constant amount of impact-ionization, if I_D is large enough [25]. The constant I_D-constant I_G stressing scheme has the disadvantage that it can not be used anymore in a

device where a leakage path to the gate has appeared, as it was found to happen frequently. This scheme also exhibits a runaway V_{DG}, which can result in destructive damage to the device. The runaway V_{DG} occurs because the transconductance is decreasing during stress, which means V_{GS} or V_{DS} have to increase. Since V_{GS} is predominantly set by I_G, it can not increase enough to keep I_D constant. This means that V_{DS} has to increase beyond the increase caused by the R_D degradation, causing an increasing V_{DG}. The choice of stressing parameters is also restricted because of the presence of multiple stable bias points under some conditions.

2.4.3. Constant V_{DGo}-Constant I_D

Our next approach was to keep V_{DG} and I_D constant, as these are the two parameters that control the impact-ionization rate. This scheme suffers from the fact that the internal V_{DGo} does not remain constant. We quickly found that this scheme could be improved upon by keeping the internal V_{DGo} constant by correcting the value of V_{DG} with the voltage drop over R_D and the external resistance, that arises from leads and contacts. This way, the internal field is kept constant, despite the increase of R_D.

We have investigated the degree to which this stressing scheme keeps the impact ionization rate constant. We did this by monitoring the side gate current I_{SG} on mHEMTs with a sidegate structure. This current is well known to be proportional to the impact ionization rate in HFETs [26]. The side gate current was extracted by setting a large negative voltage V_{SG} on the side gate, between –20 and –25 V. V_{SG} is selected to maximize the amount of side gate current that is extracted, while minimizing its influence

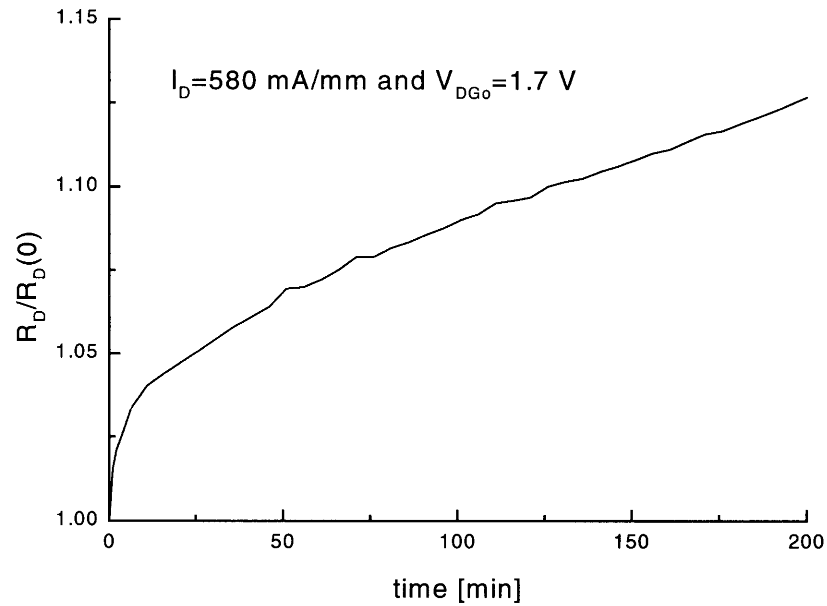


Fig. 2-9: Time evolution of R_D of a structure from wafer 453S036 with a sidegate, during a constant I_D-constant V_{DGo} experiment.

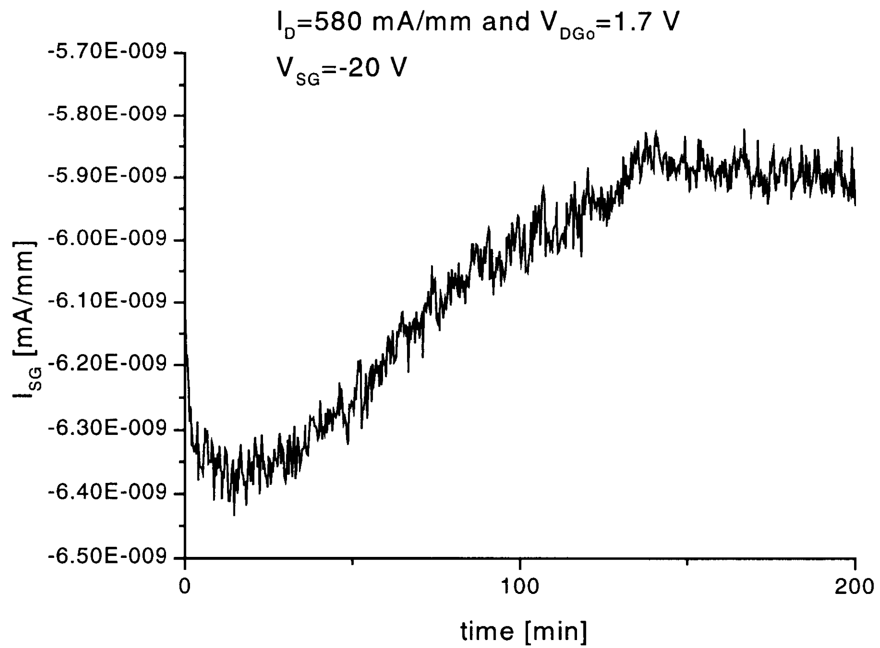


Fig. 2-10: Time evolution of I_{SG} during the same stressing experiment as Fig. 2-9.

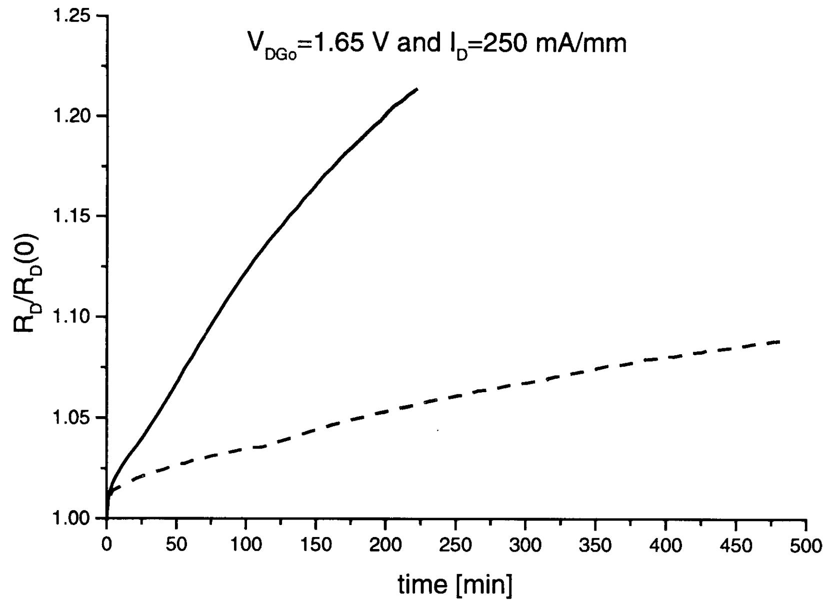


Fig. 2-11: Time evolution of R_D for two identical devices from wafer 515S032 during a constant I_D-constant V_{DGo} experiments under identical bias conditions.

on the I-V characteristics. At first, we checked that I_{SG} is indeed dominated by the impact-ionization generated holes, using the method of [26] and found this to be the case.

Fig. 2-9 shows the time evolution of R_D for a device that was stressed at a constant V_{DGo}=1.7 V and I_D=580 mA/mm. We monitored I_{SG} while stressing the device. Fig. 2-10 shows the time evolution of I_{SG} during stressing. I_{SG} changes less than 10 % of its value during the degradation process. The same was also found for a constant I_D-constant I_G stressing scheme. It seems that both stressing schemes keep the impact ionization rate relatively constant. As the constant I_D-constant V_{DGo} stressing scheme has several experimental advantages, we think this is the best stressing scheme to use for a single device.

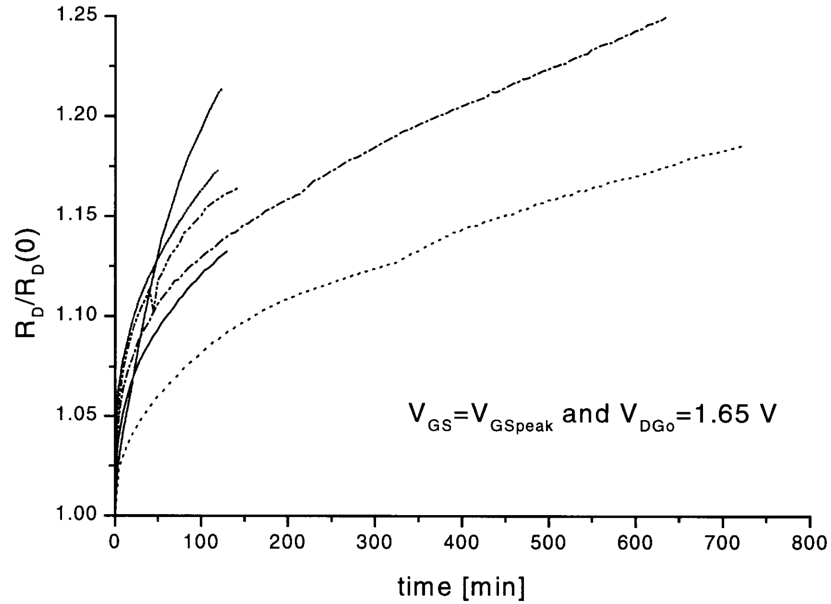


Fig. 2-12: Time evolution of R_D for six identical devices from wafer 515S027 during a constant $V_{GS}=V_{GSpeak}$-constant V_{DGo} experiments under identical bias conditions. Every device is being stressed at a V_{GS} of its own V_{GSpeak}.

2.4.4. Constant V_{GS}-V_{GSpeak}-Constant $V_{Dgo}+V_T$

If we stress several devices under identical constant I_D-constant V_{DGo} bias conditions, the degradation of R_D will show a wide scatter, as can be seen on Fig. 2-11. This suggests that this stressing scheme stresses different devices in different ways. This makes comparisons across devices difficult.

The origin of this problem is that different devices of the same wafer and same type, can show a different V_T. The devices are degraded in a different regime, as their transfer characteristics are different. If this is the cause, the uniformity of degradation should improve significantly if we degrade the devices at a constant $V_{GS}=V_{GSpeak}$ since this way every device is degraded the same way relative to its own transfer characteristic. This is

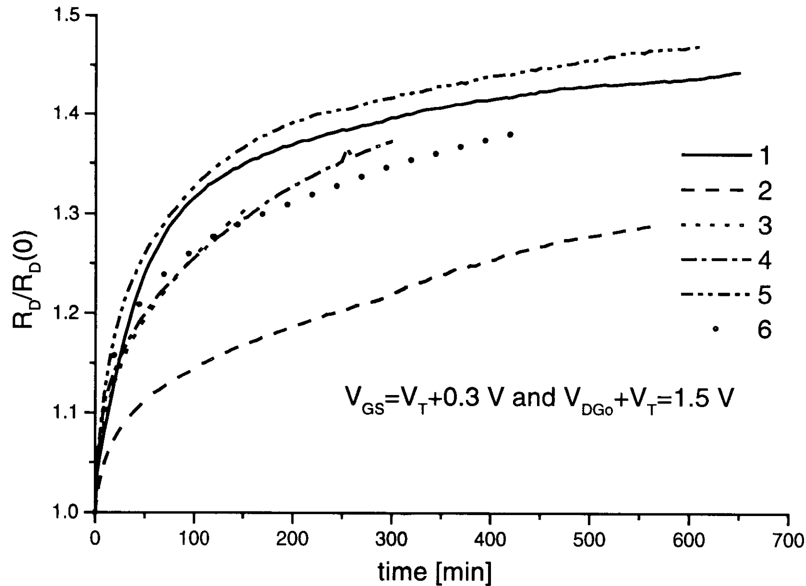


Fig. 2-13: Time evolution of R_D for six identical devices from wafer 515S027 during a constant $V_{GS}=V_T+0.3$ V-constant $V_{DGo}+V_T$ experiments under identical bias conditions.

not the case as can be seen on Fig. 2-12. The variation of degradation is not caused by the different ways the devices are stressed relative to their transfer characteristics.

2.4.5. Constant V_{GS}-V_T-Constant $V_{DGo}+V_T$

The problems with the uniformity of degradation have a different origin and we have to look closer into impact-ionization to find the answer. The rate of impact-ionization is linearly related to I_D and has an exponential dependence of $(V_{DS}-V_{Dssat})^{-1}$, which can be approximated by $[V_{DS}-(V_{GS}-V_T)]^{-1}=(V_{DG}+V_T)^{-1}$. By keeping I_D and $V_{DGo}+V_T$ constant, we should be able to keep the impact ionization rate identical among different devices. If devices are degraded at the same amount of overdrive, i.e. V_{GS} is kept constant at $V_T+V_{overdrive}$, and at a constant value of $V_{DGo}+V_T$, the degradation of different devices is significantly more uniform. This is shown on Fig. 2-13. This stressing scheme keeps I_D between all devices and during degradation within 10 % of its value. This is less critical

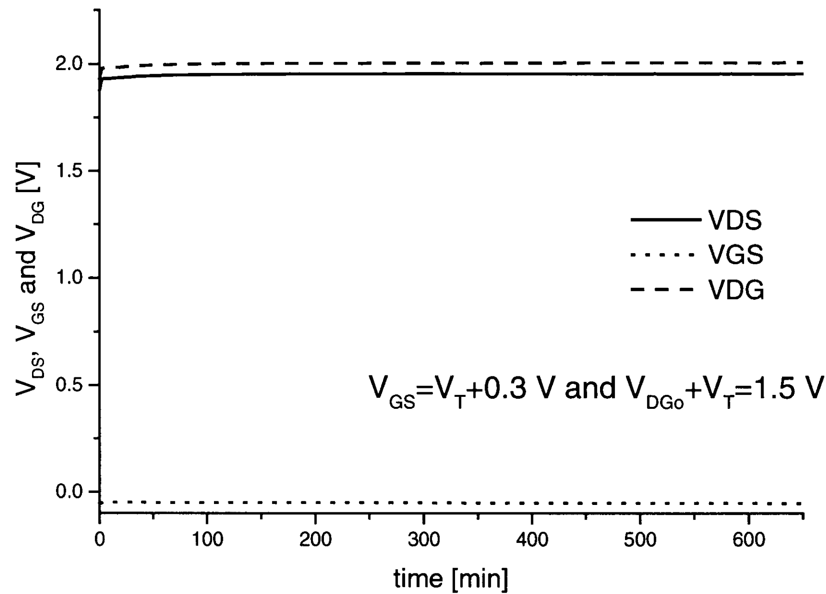


Fig. 2-14: Time evolution of V_{DS}, V_{GS} and V_{DG} for device 1 from wafer 515S027 during a constant $V_{GS}=V_T+0.3$ V-constant $V_{DGo}+V_T=1.5$ V experiment.

since the impact ionization rate is linearly dependent on I_D and not exponentially. During stress V_T stays reasonably constant. The average of V_T of the first 5 measurement is used as a constant V_T throughout the rest of the stressing experiment. This and the fact that I_D is kept relatively constant means that the constant (V_{GS}-V_T)-constant (V_{DGo}+V_T) scheme has the same properties as the constant I_D-constant V_{DGo} scheme for an individual device. Fig. 2-14 shows the time evolution of V_{DS}, V_{GS} and V_{DG} during stress for device 1 from Fig. 2-13.

2.5. Time Evolution of Device Figures of Merit during Stress

We will go over the time evolution of the different figures of merit for a device that has been degraded using the constant V_{DGo}+V_T – constant V_{GS}+V_T scheme. As can be seen on Fig. 2-13, R_D of device 1 degrades about 45 % after 200 minutes. Two degradation

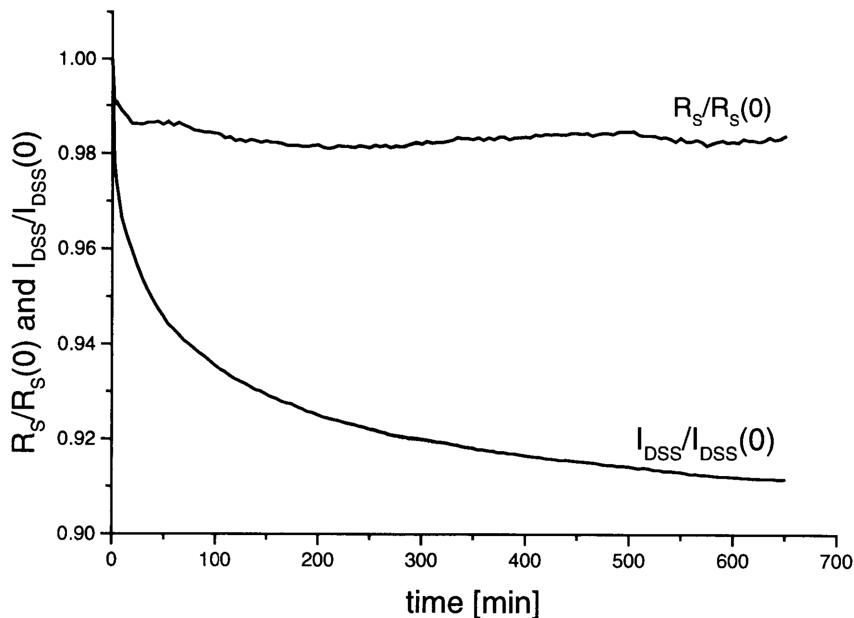


Fig. 2-15: Time evolution of the normalized value of R_S and I_{DSS} for device 1 from Fig. 2-13 during a constant $V_{GS}=V_T+0.3$ V-constant $V_{DGo}+V_T=1.5$ V experiment.

modes can be seen, The degradation is initially very fast but after 10 minutes, the degradation rate starts slowing down significantly and then stays relatively constant until the end of the experiment.

Fig. 2-15 shows the time evolution of R_S for the same device during the same experiment. After an initial drop in resistance, R_S seems to return slowly to its initial value. The change in R_S never exceeds 2 %. The time evolution of the total resistance, R_{SD}, looks very similar to the degradation of R_D.

I_{DSS} degrades 9 % during the experiment. The time evolution, as can also be seen on Fig. 2-15 is very similar to that of R_D, with a fast initial degradation and a slower constant degradation rate after 10 minutes. I_{max} decreases by 12 %, but the degradation rate does

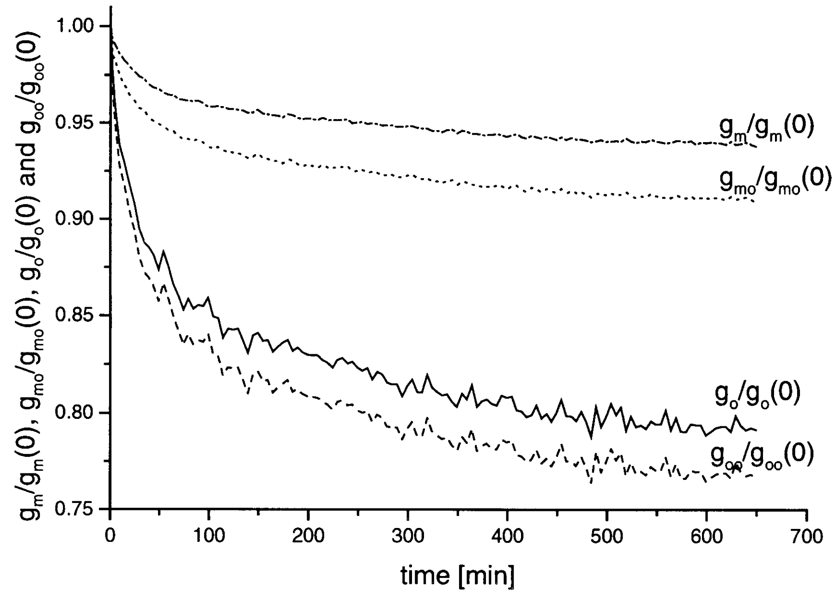


Fig. 2-16: Time evolution of the normalized values of g_m, g_{mo}, g_o and g_{oo} for device 1 from Fig. 2-13 during a constant $V_{GS}=V_T+0.3$ V-constant $V_{DGo}+V_T=1.5$ V experiment.

not saturate as quickly. The time evolution of the transconductance g_m and the intrinsic transconductance g_{mo} can be seen on Fig. 2-16. g_{mo} is the transconductance of the intrinsic device without the extrinsic R_S and R_D. g_{mo} can be computed from g_m, R_S and R_{SD} as explained in [27]. Similarly an intrinsic output conductance g_{oo} can be calculated. The intrinsic device seems to degrade somehow since g_{mo} degrades by 8 %, while g_m only degrades by 5 %. The intrinsic output conductance g_{oo} improves by 26 %, with a similar time evolution as g_{mo}.

During stress V_T tends to initially increase by a few mV after which it stays constant, as can be seen on Fig. 2-17. On the other hand, V_{Gspeak} and the knee-voltage remain constant throughout the stress. The kneeslope degrades by 16 %, with a time evolution similar to R_D. The breakdown voltage improves initially by 18 % after which it tops off and saturates, consistent with the R_D behavior, this can be seen on Fig. 2-18.

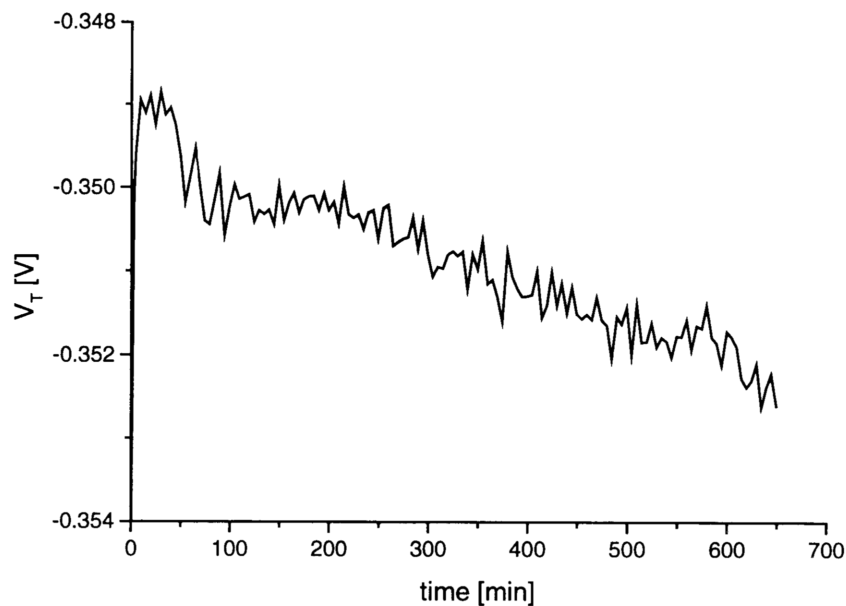


Fig. 2-17: Time evolution of V_T for device 1 from Fig. 2-13 during a constant $V_{GS}=V_T+0.3$ V-constant $V_{DGo}+V_T=1.5$ V experiment.

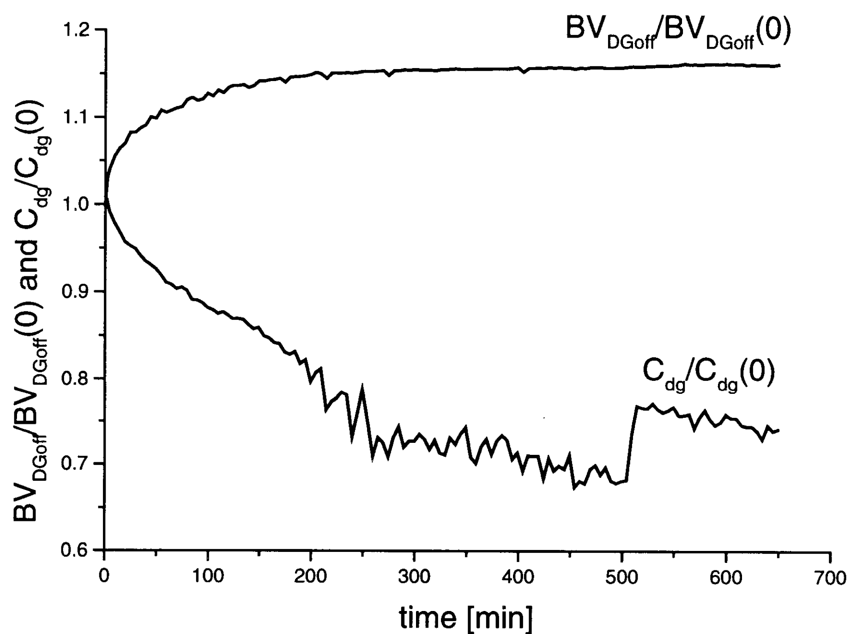


Fig. 2-18: Time evolution of the normalized value of BV_{DGoff} and C_{dg} for device 1 from Fig. 2-13 during a constant $V_{GS}=V_T+0.3$ V-constant $V_{DGo}+V_T=1.5$ V experiment.

Regarding high-frequency parameters, C_{gd} decreases by 30 % during the experiment, as can be seen in Fig. 2-18. Initially the decay is fast, but it slowly saturates. The cut-off frequency f_T degrades 12 %, with a time evolution that resembles the R_D degradation. The ideality constants of the source and drain-diode change less than 1% during stress.

The time evolution of all these figures of merit shows that the main degradation takes place in the drain region of the device, while the source region is almost completely unaffected by the degradation. This fits in the impact-ionization picture, as the high fields will be found on the drain side of the device. The intrinsic device is degraded slightly by electrical stress, as can be seen by the g_{mo} degradation. But since the shift in V_T is so small, it is likely that only little damage has occurred in the intrinsic region. No figure of merit has been found to be as sensitive to the degradation as the drain resistance, R_D.

2.6. Bias Dependence of Degradation

2.6.1. Constant Stress Experiments

By degrading several devices at different values of $V_{DGo}+V_T$ and a constant $V_{GS}-V_T$, the bias dependence of degradation can be better understood. Fig. 2-19 shows the time evolution of R_D for different devices from the same wafer that have been degraded at $V_{DGo}+V_T$ changing from 1.2 to 1.7 V and a constant $V_{GS}-V_T=0.3$ V. As $V_{DGo}+V_T$ increases, R_D degrades more. This increase of degradation can be found both in the fast initial degradation as the slower degradation afterwards.

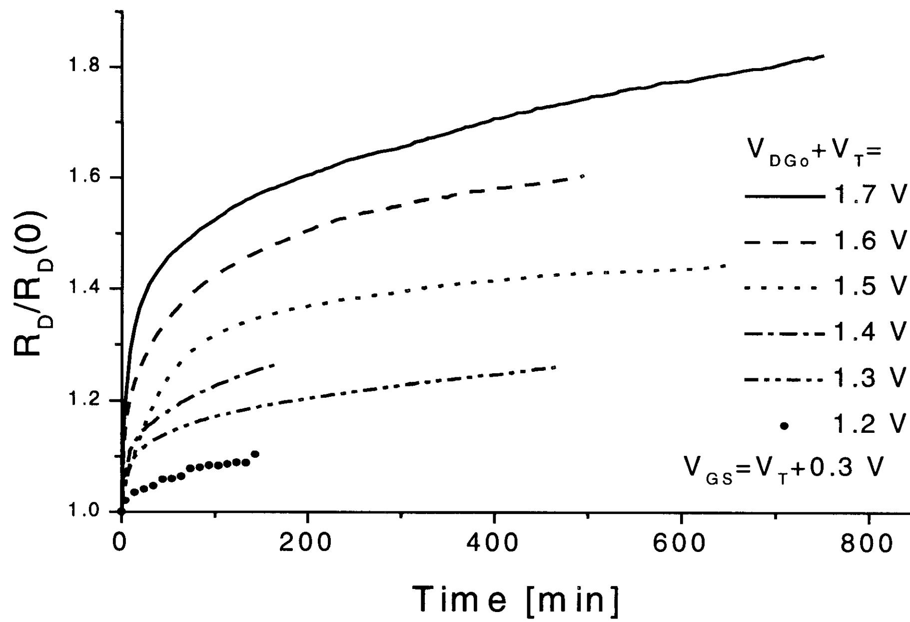


Fig. 2-19: Time evolution of R_D for six devices from wafer 515S027 stressed at $V_{GS}=V_T+0.3$ V and $V_{DGo}+V_T=1.2$ V to 1.7 V.

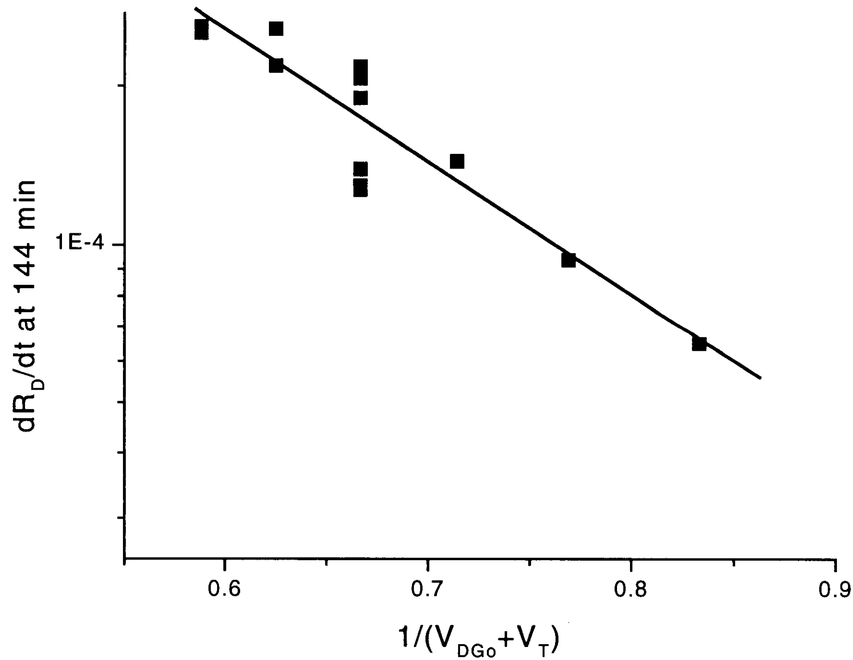


Fig. 2-20: Semi-log plot of the degradation rate dR_D/dt after 144 min, in function of $(V_{DGo}+V_T)^{-1}$ for several devices from wafer 504S27 that were stressed at $V_{GS}=V_T+0.3$ V and a constant $V_{DGo}+V_T$.

The time evolution of R_S during stress seems to be largely independent of the bias. The degradation of I_{DSS}, I_{max}, g_{mo}, f_T and BV_{DGoff} has the same bias dependence as the degradation of R_D. The degradation tends to be more severe for a higher value of $V_{DGo}+V_T$. These figures of merit show a smaller degradation than R_D. The bias dependence of other figures of merit tends to follow the same trend as R_D. A higher field increases the degradation of the device.

We can use the degradation data, to examine whether impact-ionization correlates with the degradation rate. Fig. 2-20 plots the degradation rate of R_D at a fixed point in time of the stressing experiment, in function of $(V_{DGo}+V_T)^{-1}$. This was done for dR_D/dt at 144 minutes, which is past the fast initial increase of R_D. The exponential dependence of the degradation rate on $(V_{DGo}+V_T)^{-1}$ is exactly what could be expected if the degradation is proportional to the amount of impact-ionization [28]. The value of I_D, which is the variation in the current, during these experiments only changed between 280 and 310 mA/mm.

One figure of merit that has an interesting bias dependency for its degradation is C_{dg}, as can be seen on Fig. 2-21. This figure shows that for low bias stress C_{dg} is not affected by the degradation, while for high bias stress C_{dg} decreases. This could mean that two degradation mechanisms are taking place at high bias stress, but this does not have to be the case as we will show later.

The off-state breakdown voltage tends to walk out more as $V_{DGo}+V_T$ increases as is shown on Fig. 2-22. The relationship between the degradation and $V_{DGo}+V_T$ is not as simple as in the case of R_D. In Fig. 2-23 BV_{DGoff} is plotted in function of R_D for these devices during the different points in the stressing. Fig. 2-24 shows the normalized

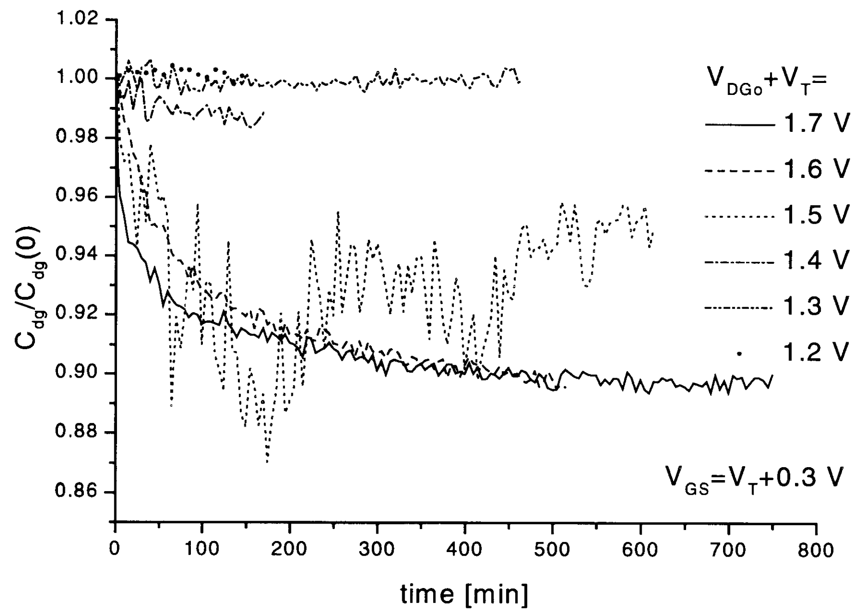


Fig. 2-21: Time evolution of C_{dg} for the six devices of Fig. 2-19 stressed at $V_{GS}=V_T+0.3$ V and $V_{DGo}+V_T=1.2$ V to 1.7 V.

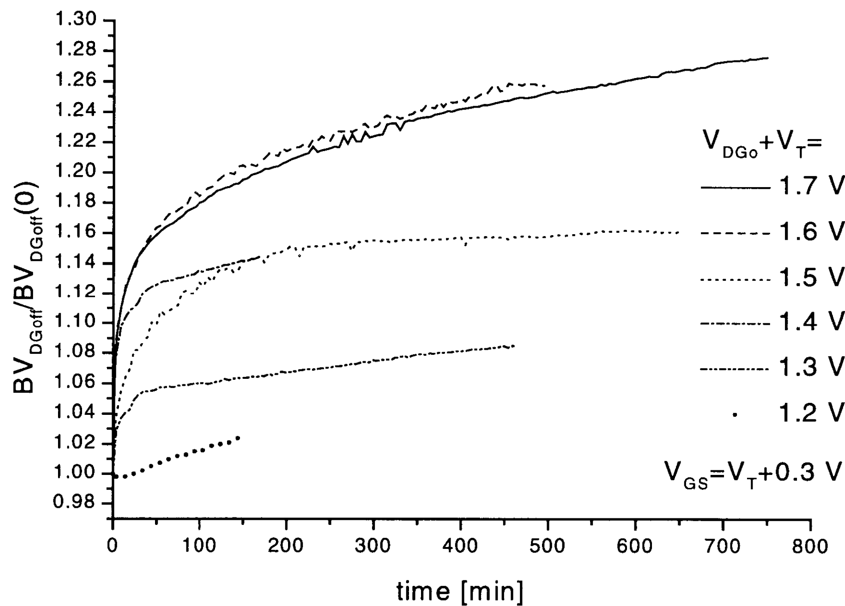


Fig. 2-22: Time evolution of the normalized value of BV_{DGoff} for the six devices of Fig. 2-19 stressed at $V_{GS}=V_T+0.3$ V and $V_{DGo}+V_T=1.2$ V to 1.7 V.

BV_{DGoff} vs. the normalized R_D. There is almost a linear relationship between BV_{DGoff}, independent of the device or the stressing condition. This shows a universal relationship between BV_{DGoff} and R_D. The degradation of R_D and the BV_{DGoff}-walkout can both be attributed to a decrease of the sheet carrier concentration n_s in the region between the gate and the drain. Only if the decrease in n_s is the origin of the degradation would such a relationship exist between both metrics. This shows that the degradation is caused by a decrease in n_s in the external drain region.

2.6.2. Step-Stress Experiments

In our stressing experiments there is some non-uniformity of the degradation mode between devices on the same wafer. To deal with this, we measured several devices at different values of the field. This is a very time-and device consuming process. To study the bias dependence of the degradation of a device in a more efficient way we starteddoing step-stress experiments. At first, the device is stressed at a low value of $V_{DGo}+V_T$ and after a fixed time interval, the field is increased. This method has the disadvantage that the degradation could be dependent on the history of the device. Upon comparing the results of such a step stress measurement with separate constant stress measurements such as the experiments, described in 2.6.1., we observed the same trends to be present. This method allows us to study the bias dependency of the degradation of several figures of merit of a device in a fast way, showing the same dependencies as separate experiments.

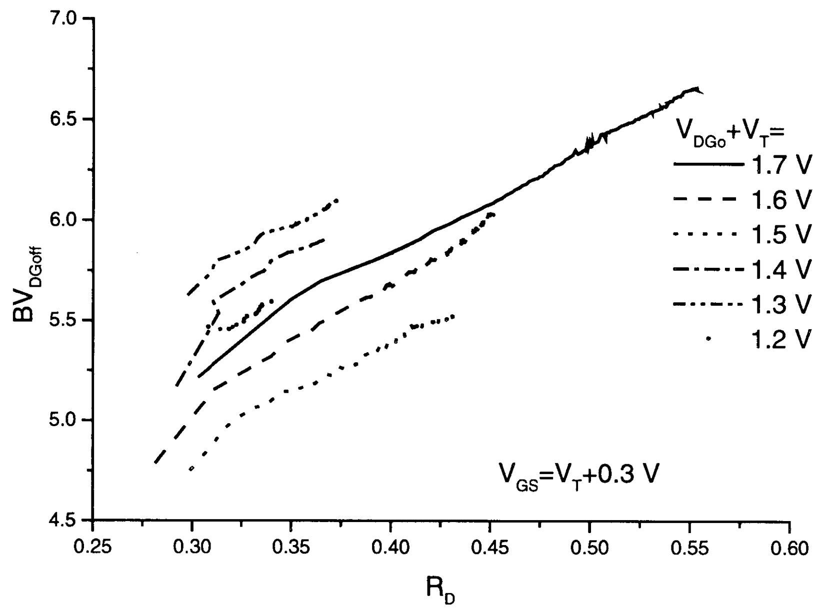


Fig. 2-23: BV_{DGoff} vs R_D during degradation for the six devices of Fig. 2-19 stressed at $V_{GS}=V_T+0.3$ V and $V_{DGo}+V_T=1.2$ V to 1.7 V.

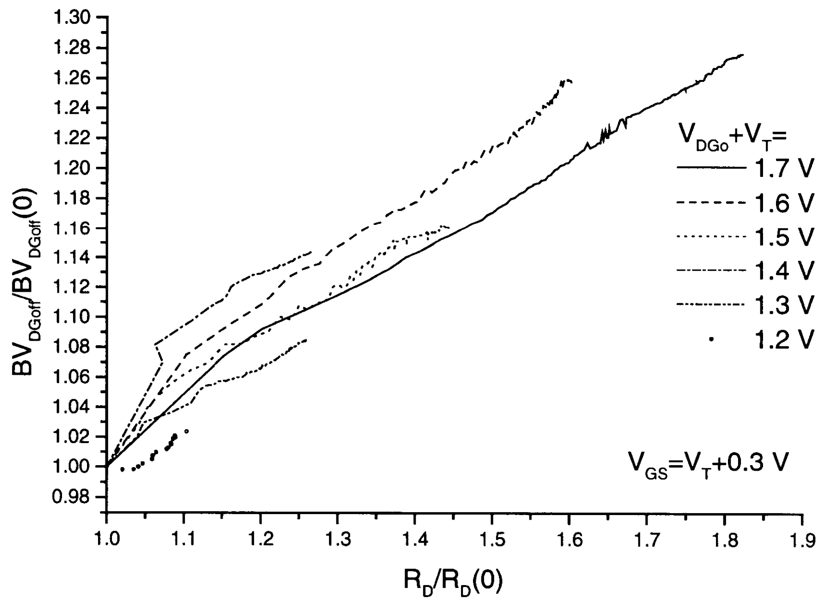


Fig. 2-24: $BV_{DGoff}/BV_{DGoff}(0)$ vs. $R_D/R_D(0)$ during degradation for the six devices of Fig. 2-19 stressed at $V_{GS}=V_T+0.3$ V and $V_{DGo}+V_T=1.2$ V to 1.7 V.

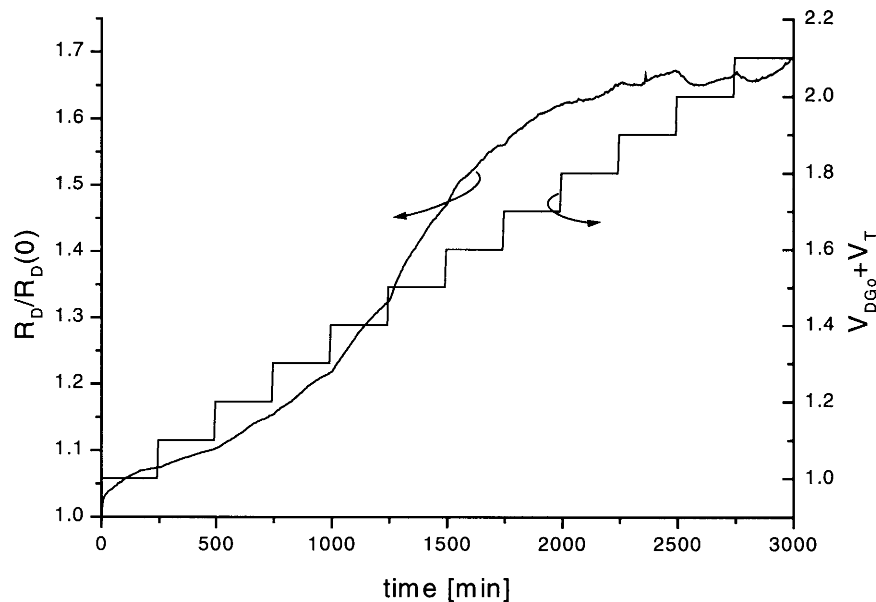


Fig. 2-25: Time evolution of $R_D/R_D(0)$ for an m-HEMT from wafer 515S027 stressed at $V_{GS}=V_T+0.3$ V and $V_{DGo}+V_T=$ 1 to 2.1 V, stepped up with 0.1 V increments in 250 min time intervals.

Fig. 2-25 shows the degradation of R_D of a device stressed at $V_{GS}= V_T+0.3$ V and $V_{DGo}+V_T$ stepped in 0.1 V intervals from 1 to 2.2 V, with a time interval of 250 minutes can be seen. Here we can see that until $V_{DGo}+V_T=$ 1.5 V the degradation rate is increasing with the value of $V_{DGo}+V_T$. At higher values, the degradation appears to saturate. The device zapped at $V_{DGo}+V_T=$ 2.2 V. This degradation behavior is consistent with the experiments from 2.6.1, if we take the history effects into account. We have observed that stressing the device also increases the zapping voltage, even if we take the voltage drop over the degraded R_D into account. The degradation of I_{DSS}, I_{max}, g_d , f_T and g_m seem to mirror the R_D degradation.

During the experiment shown in Fig. 2-25, V_T only moved around in a 25 mV wide interval. V_{GSpeak} decreased by 90 mV. The ideality factors of the diodes do not change during the stress. Fig. 2-26 shows I_D during this step-stress experiment. I_D is only

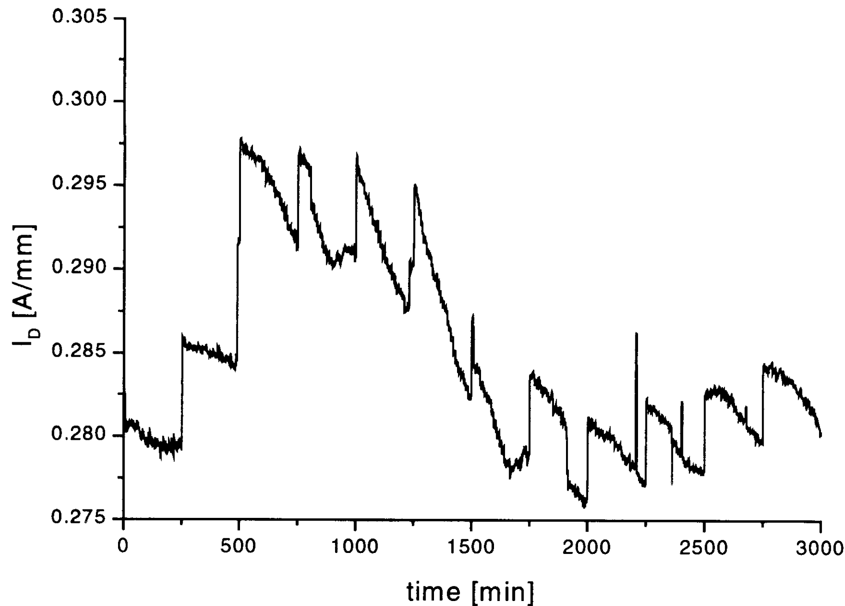


Fig. 2-26: Time evolution of I_D during the step stress-experiment of Fig. 2-25.

changing over an interval of 10 % of its value. As a good approximation it is constant throughout the experiment.

The time evolution of C_{dg} can be seen on Fig. 2-27. C_{dg} is unaffected by the stress until $V_{DGo}+V_T$ is greater than 1.3 V. At this voltage, R_D degradation and the other parameters that seem to follow its trend, like BV_{DGoff}, g_{mo} and I_{DSS} also show a significant increase in their degradation rate. This does not have to be caused by a second mechanism.

Fig. 2-28 shows the normalized BV_{DGoff} vs. the normalized R_D during the same step-stress experiment. This shows again that there is a universal relationship between BV_{DGoff} and R_D as long as $V_{DGo}+V_T$ is smaller than 2 V. This means that the degradation is caused by a drop of n_s in the region between the drain and the gate.

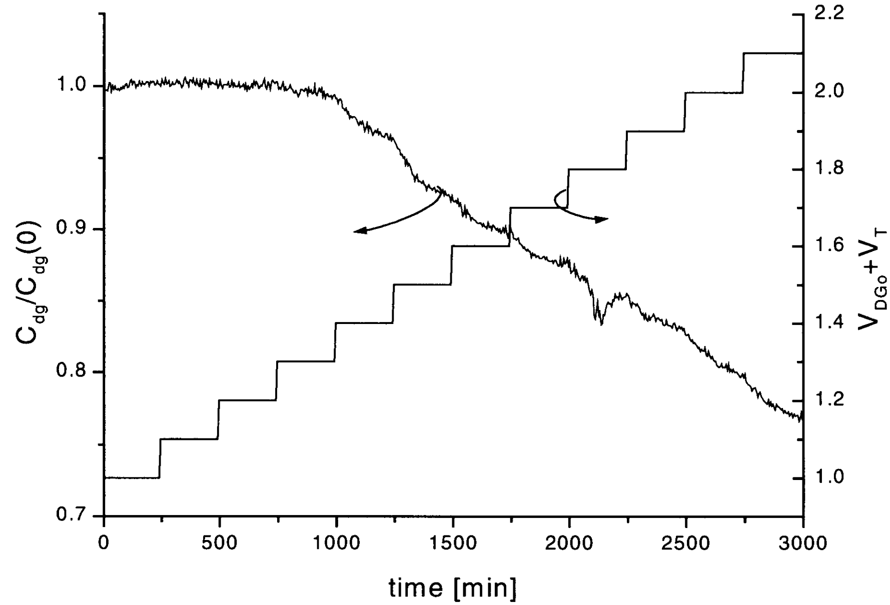


Fig. 2-27: Time evolution of $C_{dg}/C_{dg}(0)$ for an m-HEMT stressed at $V_{GS}=V_T+0.3$ V and $V_{DGo}+V_T=$ 1 to 2.1 V, stepped up with 0.1 V increments in 250 min time intervals this is the same experiment as Fig. 2-25.

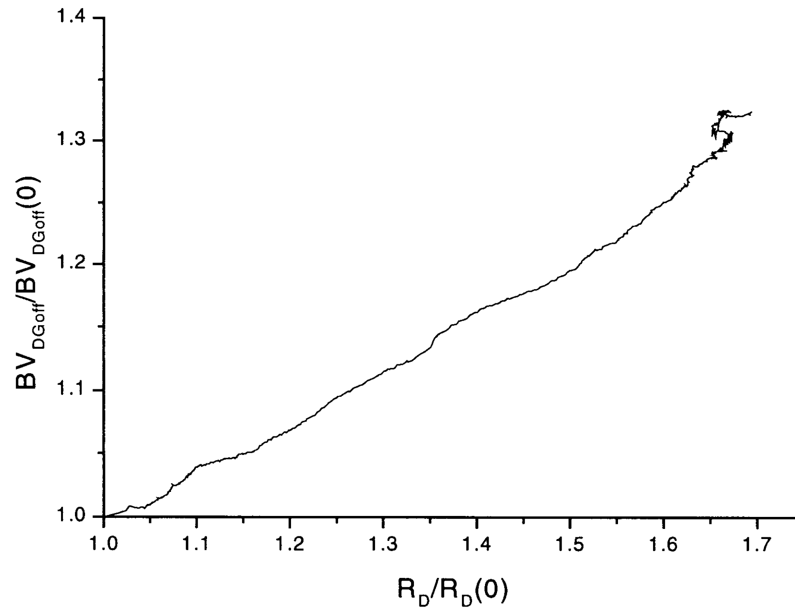


Fig. 2-28: Time evolution of $R_D/R_D(0)$ vs. $BV_{DGoff}/BV_{DGoff}(0)$ for an m-HEMT from wafer 515S27 stressed at $V_{GS}=V_T+0.3$ V and $V_{DGo}+V_T=$ 1 to 2.1 V, stepped up with 0.1 V increments in 250 min time intervals this is the same experiment as Fig. 2-25.

2.7. Conclusions

We have developed a system to stress and measure metamorphic HEMTs to study the degradation of several figures of merit. We have observed that R_D is the metric that shows the highest degradation, though several other key figures of merit are also affected. We have found a stressing scheme that enables us to keep the impact-ionization rate constant. In this scheme, V_{GS}-V_T and V_{DGo}+V_T are kept constant during the stressing experiment. This stressing method shows a good uniformity for the degradation of different devices that are stressed under the same conditions.

The degradation takes place at the drain side of the device. The source side is almost unaffected. The intrinsic part of the device is degrading slightly. The bias dependency of the drain resistance degradation shows that the degradation rate is correlated to the amount of impact-ionization. We have shown that step-stress experiments are an efficient way to study the bias dependency of the degradation, as it shows similar trends as individual experiments.

We have found a universal relationship between BV_{DGoff} and R_D during the degradation as long as the bias voltage is not too high. This reveals the degradation is caused by a drop of n_s in the region between the gate and the drain.

These experiments have shown that different mechanisms of degradation could be present. The field distribution in the channel and the interactions between all figures of merit make the analysis of the physical origin of the degradation very complex. Therefore, we decided to study Transmission Line Method structures (TLMs) which have a much simpler structure than mHEMTS. These experiments are reported in the next chapter.

Chapter 3

Degradation of TLMs

3.1. Introduction

Chapter 2 showed that the electrical degradation of metamorphic HEMTs is very complex. The correlation between the different metrics makes it hard to separate the different effects of the degradation. Therefore we carried out experiments on TLMs, transmission line method structures. A sketch of this structure can be seen on Fig. 3-1. The TLM has exactly the same material structure as the metamorphic HEMT, but no gate structure has been fabricated. No part of the cap has been removed in a TLM. This way the field in the channel should be uniform lengthwise. This structure also has a more limited number of figures of merit. This should simplify the analysis.

This chapter will first show the effects of electrical degradation of TLMs and show that different modes of degradation are occurring. If the device is cooled down during stress, the device is more resistant to degradation. We then look into the dependence of the critical voltages for degradation with the length of the channel. We have studied the uniformity of the degradation. We also thermally stressed some devices by heating them up. We have seen that thermal degradation does not behave exactly like electrical degradation. We tried to degrade devices by using a strong light source, but were unsuccessful in achieving this.

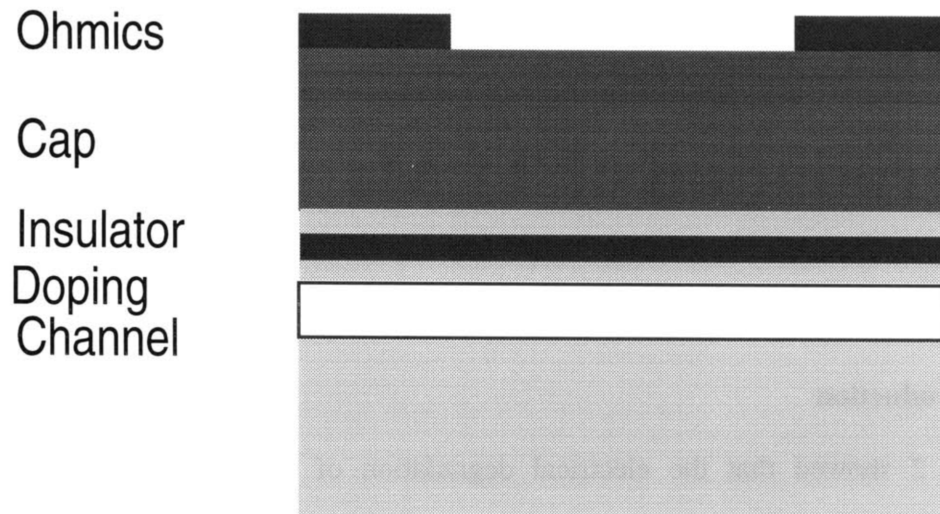


Fig. 3-1: Sketch of a TLM.

3.2. Experimental Set-up

The TLMs are being stressed and measured inside a Cascade probe station, using DC probes. A HP4155A semiconductor parameter analyzer, controlled through a PC running HP VEE 4.0, is being used to stress and measure the devices. Due to the limitations of the HP4155A on currents, two SMUs are connected in parallel to each contact, so a higher current can be driven.

The resistance is being measured using a Kelvin-measurement technique. This way two probes are used to contact every pad. One probe acts as a voltage meter, while the other drives the current through the contact. This eliminates the input of the external resistance on the measurement.

The device is being stressed by applying a constant voltage between the two contacts. In a typical experiment the device is first characterized by taking an I-V curve. This is done without degrading the device, by limiting the voltage. Out of this I-V curve the low-field resistance, R, is extracted by the program. The saturation current, I_{sat}, is also measured for the devices for which this is possible without causing degradation.

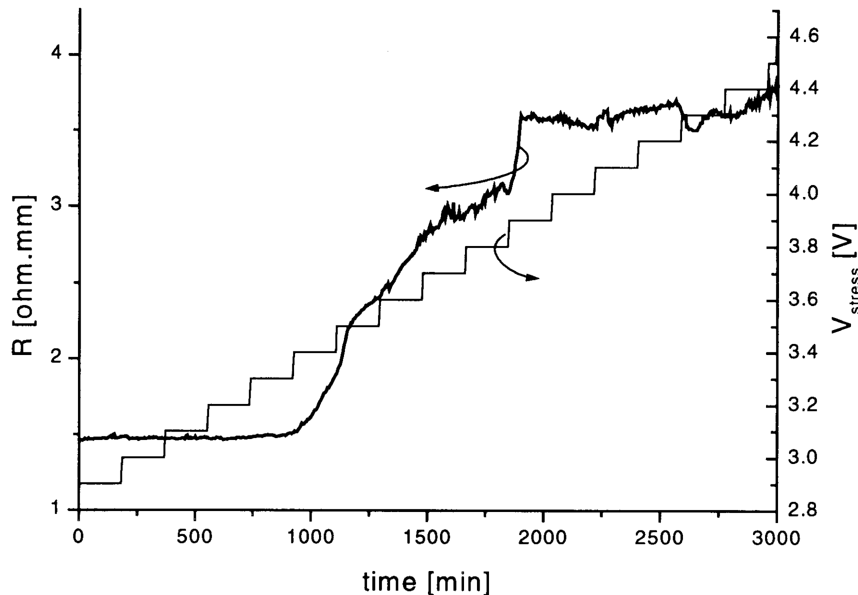


Fig. 3-2: Time evolution of R, at a low voltage, during step-stress of a 12 μm TLM of wafer 453S036. The voltage over the TLM (not excluding the drop over the probes) is also indicated.

3.3. Electrical Degradation of TLMs

3.3.1 Observations

In the first series of experiments, we put a relatively high voltage on these devices and found that both I_{sat} and R seriously degraded on a very short time-scale. At high voltages, even millisecond pulses degrade the device. But the degradation seems to saturate.

We have carried out step-stressed experiments in which the stressing voltage is held constant for a while and then it is increased. The time-evolution of the resistance during a typical step-stress experiment can be seen on Fig. 3-2. There seems to be a critical voltage, beyond which degradation suddenly takes place. For a 12 μm TLM this voltage is around 3.4 V as can be seen on the figure. It seems that degradation saturates, until a

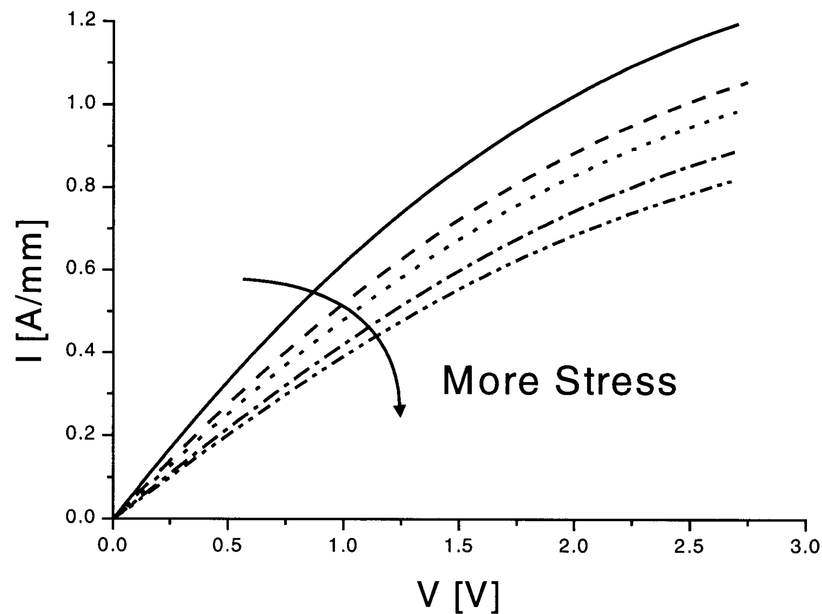


Fig. 3-3: I-V characteristics of a 12 μm TL, during step-stress. The solid line is the first measurement taken during stress.

second critical voltage is reached at 3.8 V where it starts again. At these high voltages even a TLM can zap. Of these devices I_{sat} could not be measured without seriously degrading the device, since the critical voltage for degradation is lower than the saturation voltage.

Though I_{sat} cannot be measured with great precision, I_{sat} is degrading through bias stress. Fig.3-3 shows the I-V curves of the TLM at different points in time of the stressing experiment of Fig. 3-2. It can be seen that I_{sat} is degrading, it is harder to see by how much.

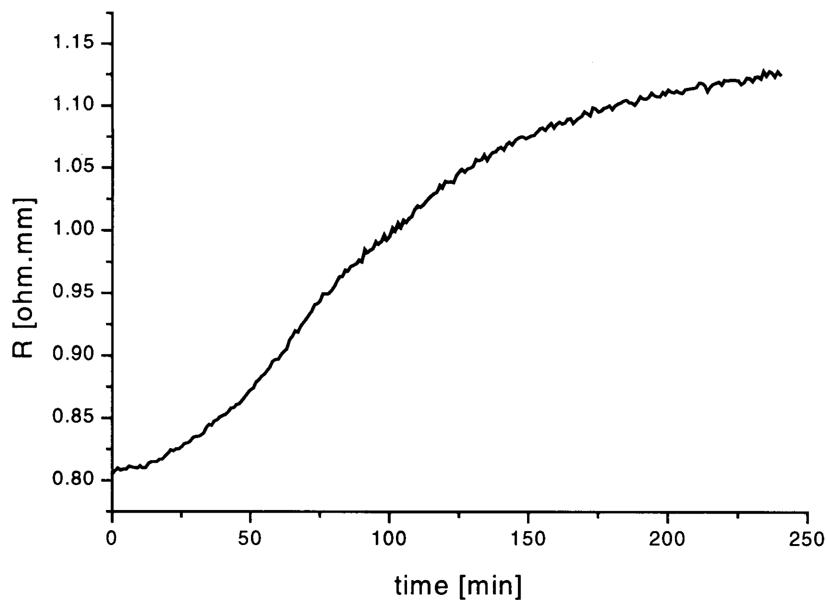


Fig. 3-4: Time evolution of R for a 6 μm TLM from wafer 453S036 stressed at 2.55 V, the critical voltage for degradation for this TLM.

If we look closer in the time evolution of the degradation near the critical voltage, as is shown in Fig. 3-4 we see that initially the degradation is very slow, then it starts to accelerate and reaches a maximum rate of degradation. After this time, the degradation seems to slow down, and finally saturates. The duration of the initial slow-degradation regime seems to be dependent on the bias conditions. Very near to the critical voltage this initial delay for degradation can take over 100 minutes. If the bias is much higher than the critical voltage, this regime is not visible. The degradation will be too fast to see this initial delay.

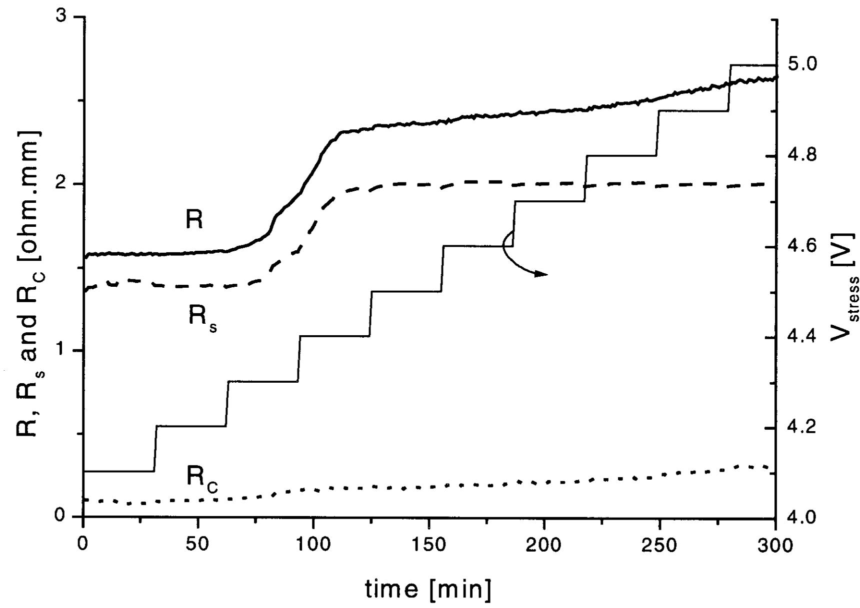


Fig. 3-5: Time evolution of R, the sheet resistance R_S and the contact resistance R_C for a 12 μm TLM that was stressed at –65 °C.

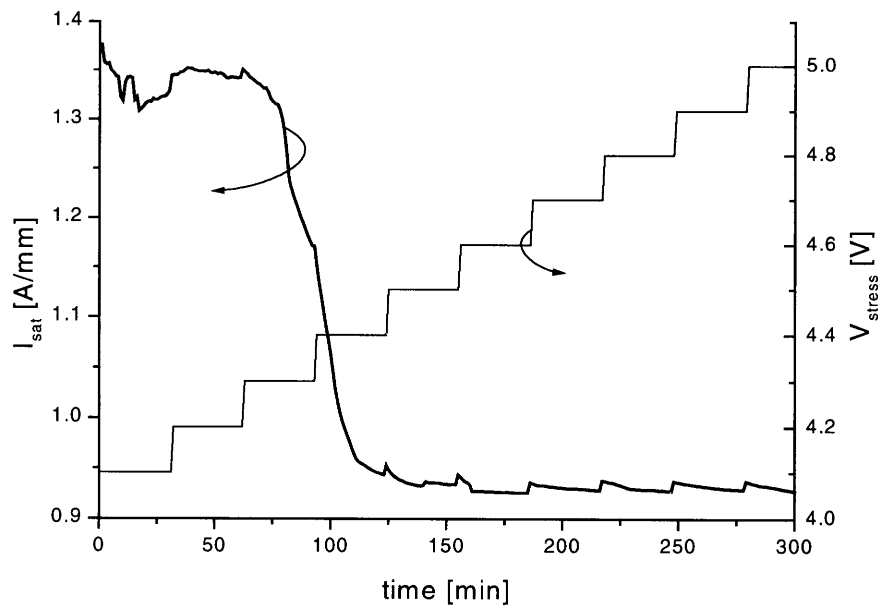


Fig. 3-6: Time evolution of I_{sat} during the same stressing experiment of Fig. 3-5.

3.3.2. Influence of Temperature on Degradation

At lower temperatures, we observed that the TLMs become far less sensitive to bias stress. At room temperature, a good measurement of I_{sat} was not possible since the saturation bias is higher than the voltage where degradation starts to occur. At a lower temperature a higher bias can be applied to the device without degrading it. This enables a better measurement of I_{sat}.

The time evolution during degradation of a 12 μm wide TLM at –65 °C can be seen on Fig. 3-5. The device starts degrading at 4.3 V. Fig.3-6 shows the time evolution of I_{sat}. Here, there is only one degradation mode, as I_{sat} starts degrading at 4.3 V and then saturates. The critical voltage for degradation is significantly higher than a similar device at room temperature, which can be seen on Figs. 3-7 and 3-8. There are two distinct degradation modes. There is a fast increase in the resistance at 4.3 V and a slow and almost constant degradation mode at voltages higher than 4.4 V. If we look at the time evolution of I_{sat}, only one degradation mode is apparent, as I_{sat} starts degrading at 4.2 V and then saturates. This measurement of I_{sat} is the value of I that was measured at the stressing voltage during stress. This voltage is higher than the voltage that is used for the I-V curve. The second degradation mechanism seems to not degrade the sheet carrier concentration since the saturation current remains constant.

This material system has a lower impact ionization rate at a lower temperature [29]. If the degradation rate correlates with the amount of impact-ionization, it was to be expected that the device would only start degrading at a higher voltage.

A similar device that was stressed at room temperature shows a different degradation behavior as can be seen on Figs. 3-7 and 3-8. This device starts degrading at a much

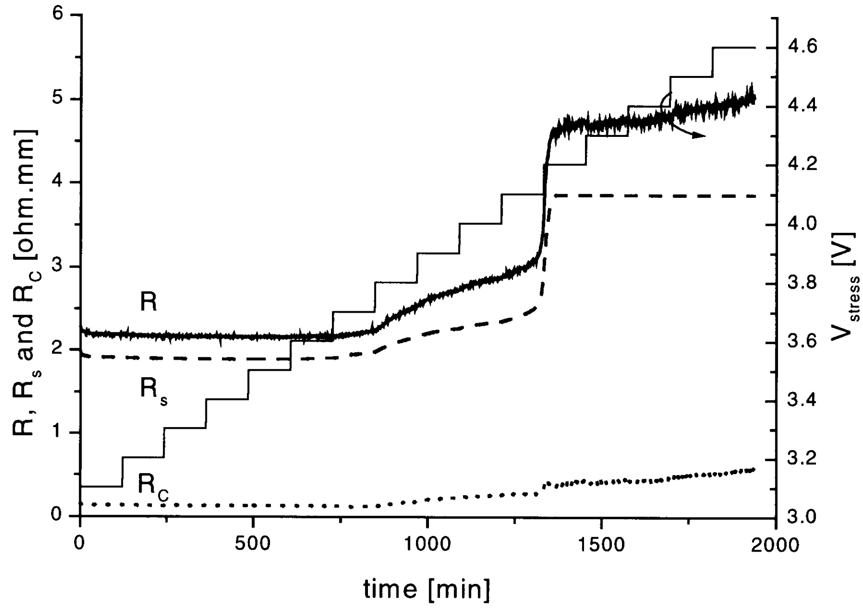


Fig. 3-7: Time evolution of R, the sheet resistance R_S and the contact resistance R_C for a 12 μm TLM that was stressed at room temperature.

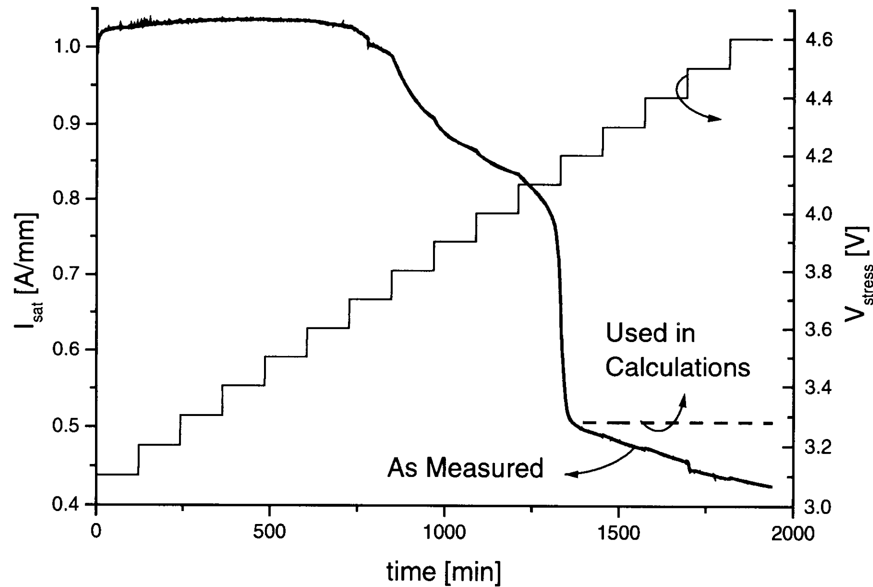


Fig. 3-8: Time evolution of I_{sat} , during step-stress of a 12 μm TLM. One of the curves is our measurements of I_{sat} from the I-V curves. The other is the curve we used for the calculation of R_C as an approximation.

lower bias. It also shows two degradation modes, at 3.7 V and at 4.2 V, in stead of the one mode of degradation at 4.3 V for the device at –65 °C.

3.3.3. Relationship between R_C Degradation and n_s Degradation

The degradation of the TLM I-V characteristics can be caused by degradation of the contact and the channel. There is clearly degradation of the channel, since I_{sat} goes down. But it is not clear whether the contacts are also degrading. We wanted to separate these two mechanisms.

I_{sat} should be independent of changes in R_C, so we can use I_{sat} to estimate the degradation of the channel. In these calculations we assume the field distribution in the channel to be uniform. If we normalize everything to a unit width, the I-V characteristics of a TLM are given by [28]:

$$I = \frac{qn_s v_{sat}}{1 + \frac{v_{sat} L}{\mu_e (V - 2R_C I)}} \tag{1}$$

The saturation current is given by:

$$I_{sat} = qn_s v_{sat} \tag{2}$$

Postulating that v_{sat} does not change, I_{sat} follows the evolution of n_s, which is affected by degradation. We can see on Fig. 3-6, that I_{sat} is decreasing. This can be explained by a degradation of n_s. By measuring I_{sat} we can extract $n_s/n_s(0)$.

For small fields, the TLM behaves as a resistor with a large-signal resistance given by:

$$R = \frac{V}{I} = 2R_C + \frac{v_{sat} L}{\mu_e (I_{sat} - I)} \tag{3}$$

For a small I, this expression becomes:

$$R = 2R_C + \frac{L}{\mu_e q n_s} \tag{4}$$

At t=0, that is before any degradation we have:

$$R(0) = 2R_C(0) + \frac{L}{\mu_e q n_s(0)} \tag{5}$$

If we subtract (5) from (4) and solve for R_C we get:

$$R_C = \frac{1}{2}\left[R - \left[R(0) - 2R_C(0)\right]\frac{n_s(0)}{n_s}\right] \tag{6}$$

So if R_C is known at the start of the experiment, we can use (6) to extract the evolution of R_C during degradation. This is valid if μ_e does not change during the stress. The results of this for the TLM that was stressed at –65 °C, can be seen on Fig. 3-5. For the TLM that was stressed at room temperature, the results of the calculation of R_C are found on Fig. 3-7. For this last calculation, we assume that the value of I_{sat} remains constant at voltages higher than 4.2 V. The degradation behavior of R in this bias range is similar to that of the low temperature stressing. The measurement of I_{sat} is certainly not good enough to distinguish between an increase of R_C or a drop in n_s at room temperature.

For degradation at lower voltages ($V<4.2$ V) and at room temperature, a relationship between R_C and n_s has been found. Fig. 3-9 shows three extractions of $R_C/R_C(0)$ vs. $n_s(0)/n_s$ on a log-log scale for a TLM that was stressed at room temperature at a low voltage. The calculation was performed for three different values of $R_C(0)$, as there is some uncertainty on its exact value. We find that there is a strong correlation between R_C and $1/n_s$. It seems $R_C \propto (1/n_s)^x$ with x between 2.5 and 3.5. R_C will increase by a

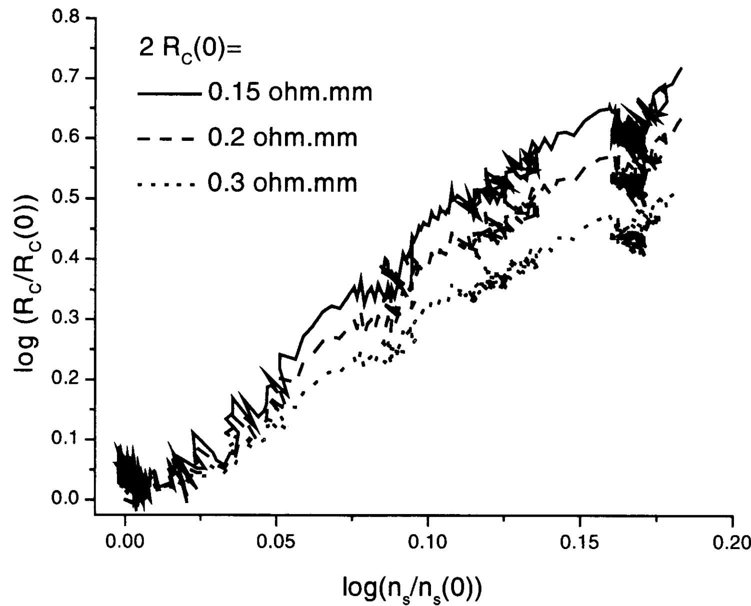


Fig. 3-9: Time evolution of R_C, supposing three different initial values, during step-stress of a 12 μm TLM

maximum of 0.4 Ω.mm for a 12 μm TLM, so the major change in R in device, is caused by a decrease in n_s

We performed step-stress experiments on devices from different lengths on the same wafer. Fig. 3-10 shows the calculation of $R_C/R_C(0)$ vs $n_s(0)/n_s$ on a log-log scale for devices from four different lengths. All lengths seem to trace the same curve more or less. This seems to indicate a very fundamental relationship. R_C probably increases just because n_s decreases, as expected from simple ohmic contact theory based on electron tunneling.

If we look at the degradation of the wafer at room temperature from Fig. 3-7 two distinct degradation modes can be distinguished. The first degradation mode is from 800 to 1400 minutes. In this mode R_C is increasing while n_s is dropping in a linear way on a log-log plot. The fast increase of the degradation rate around 1250 minutes could be a third

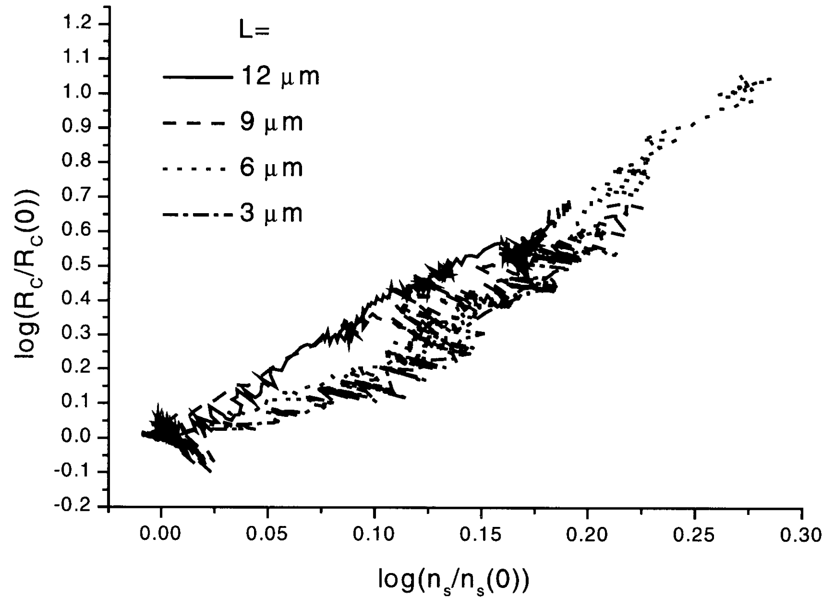


Fig. 3-10: $\ln(R_C/R_C(0))$ vs $\ln(n_{so}/n_s)$ calculated with $R_C(0)$=0.2 Ω.mm for a 3, 6, 9 and 12 μm TLM.

degradation mechanism appearing. At –65 °C, we also see a sudden increase in the degradation, but it is less clear if there are two mechanisms playing a role or only one. This is something we also have not observed in a mHEMT. Later than 1400 min, the second degradation mode appears, where R_C is increasing while n_s is unaffected.

3.3.4. Critical Voltage as a Function of Length

We know turn our attention to the critical voltage as a function of the channel length. This is plotted in Fig. 3-11. During step-stress degradation, we have realized that the TLM seems to degrade in several regimes, each one characterized by a critical voltage. Fig. 3-7 shows a typical example. We have examined the two degradation modes for different TLMs of different lengths.

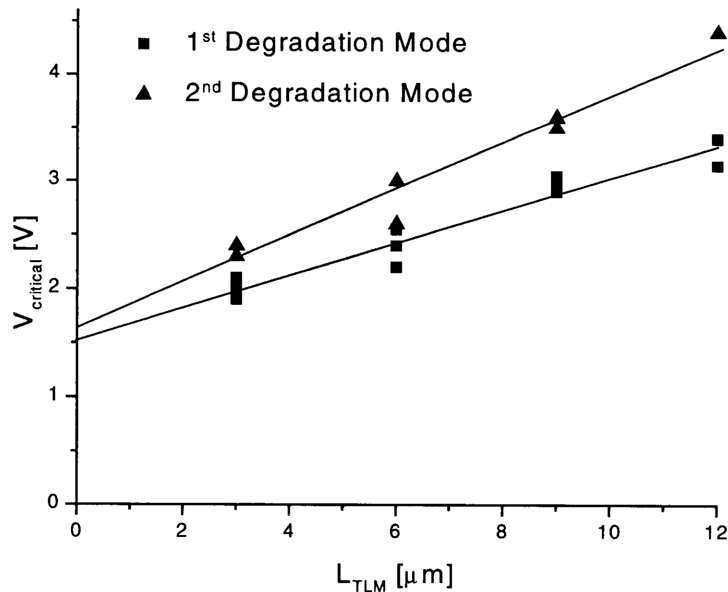


Fig. 3-11: The critical voltages for the first and the second degradation mode, in function of the channel length of the TLM.

Fig. 3-11 shows a plot of the critical voltages for the first and second degradation modes as a function of the length for devices of one wafer. A linear relationship can be found between the critical voltage and the length. There is an offset at L=0 μm of 1.5 V for the first critical voltage. This measurement does not take the drop over the ohmic contacts into account, which is about 0.4 V. This leaves an intrinsic offset voltage of about 1.1 V. This means that the minimal energy, that an electron has to gain to degrade the material seems to be 1.1 eV. This is comparable to the 0.7 eV, the energy an electron needs for impact-ionization to occur in InGaAs [1]. This is consistent with the view that hot electrons and/or holes are responsible for the degradation of the material. This material system has a similar threshold energy for velocity saturation as for impact-ionization. We see strong degradation occurring as soon as the current is saturating.

This figure also shows a higher field and a higher minimal potential drop is necessary for the second degradation mode to start about 1.7 V. The field for the first degradation mode

is about 1500 V/cm and for the second degradation mechanism is about 2200 V/cm. The minimum potential drop seems to be 1.35 V for the second mechanism. This is after taking the external voltage drop, including the ohmic contact resistance, into account.

3.3.5 Uniformity of Degradation

We have performed systematic field-reversal degradation experiments in order to examine the uniformity of degradation along the TLM. We stressed TLMs at different voltages. After saturation degradation had occurred we flipped the direction of the field using the HP4155, while keeping the field constant. We noticed that for lower voltages the rate of degradation did not increase. In some cases a slight recovery of the resistance was observed. While for higher voltages a significant additional degradation took place immediately after the field reversal. Fig. 3-12 (a) shows a typical degradation for a relatively small degradation voltage, while Fig. 3-12 (b) shows a typical degradation for a higher bias stress.

We performed several of such experiments on devices with different lengths, where we stressed the device until saturation occurred and then flipped the polarization of the field while keeping the amplitude of the bias constant. A summary of all field-reversal experiments is shown on Fig. 3-13, which graphs the change in resistance after the field-reversal ΔR_2 normalized to the change before flipping the field ΔR_1, as a function of the field normalized to the first critical degradation voltage. For degradation around the 1st critical voltage, i.e. the x-coordinates are around 1, the degradation that takes place after flipping the polarization, ΔR_2, is small compared to the degradation that took place before the field was reversed, ΔR_1. If the stress bias increases, ΔR_2 becomes significant

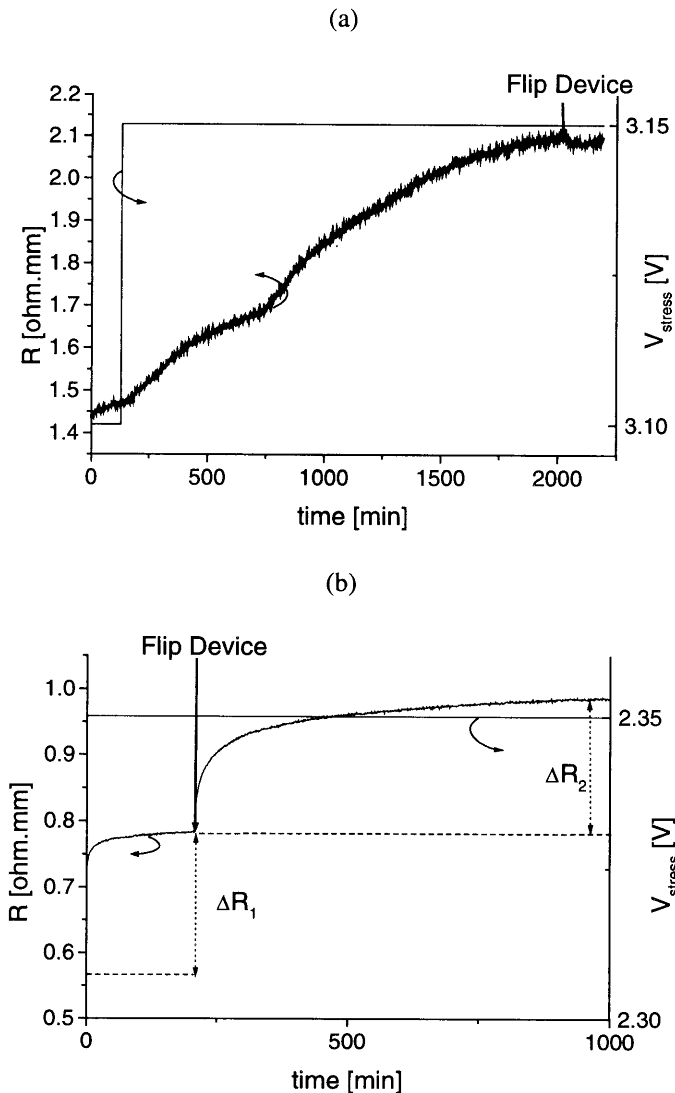


Fig. 3-12: (a) Time evolution of R for a 12 μm TLM degraded by a bias stress of 3.1 V during the first 100 min and 3.15 V after that. The polarity of the field was flipped around 2000 min. This device was stressed near the first critical voltage of degradation. (b) Time evolution of R for a 3 μm TLM degraded by a bias stress of 2.35 V. This device was stressed near the second critical voltage of degradation.

compared to ΔR_1. Reversing the field seems to affect the degradation at a higher bias stress. It seems that at a low voltage the damage that causes degradation occurs symmetrical in the channel. For high voltage there is asymmetry in the damage. This confirms that both modes are not caused by the same degradation mechanism.

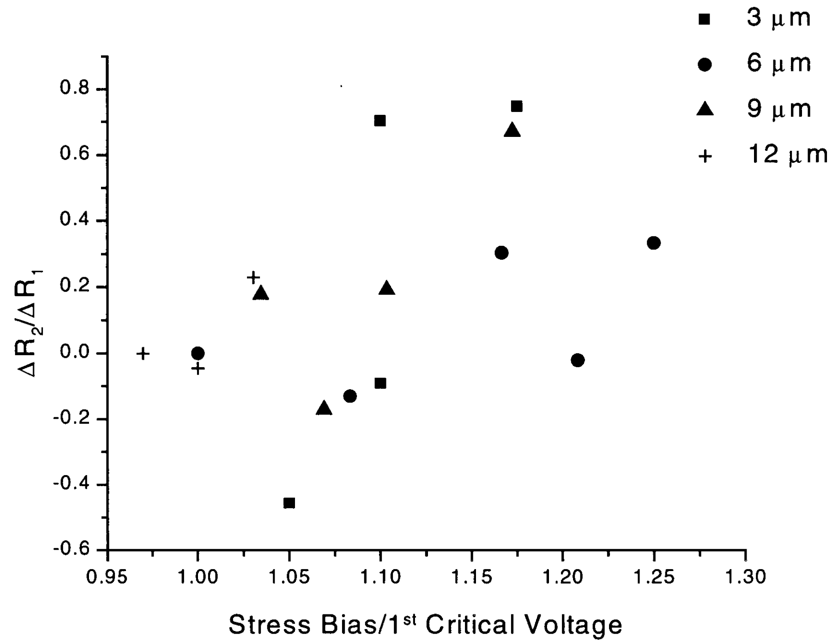
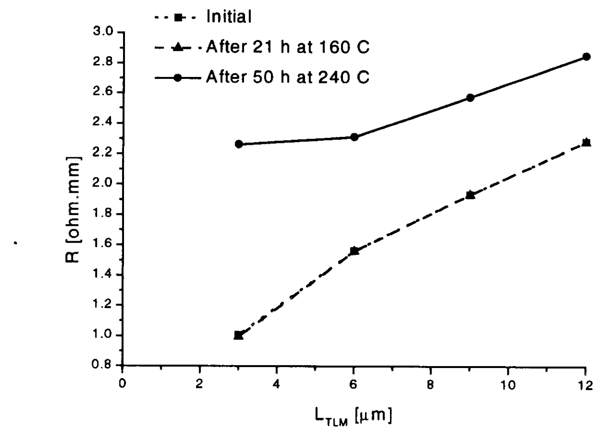


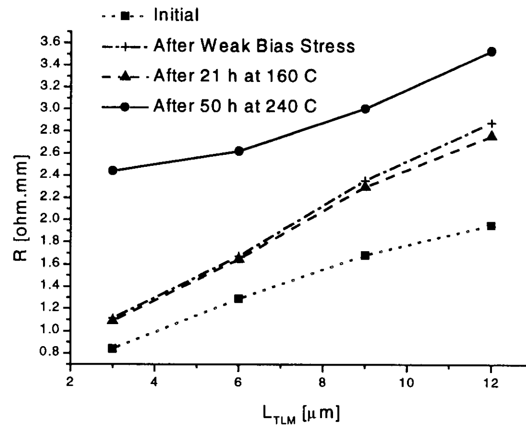
Fig. 3-13: After a device has been degraded until saturation, the polarization of the degradation bias was flipped, while the bias was kept constant. This figure shows the additional degradation after field reversal ΔR_2 normalized to the degradation before the field reversal ΔR_1 versus the stress bias normalized to the critical voltage for this particular device.

3.4. Thermal Degradation Experiments

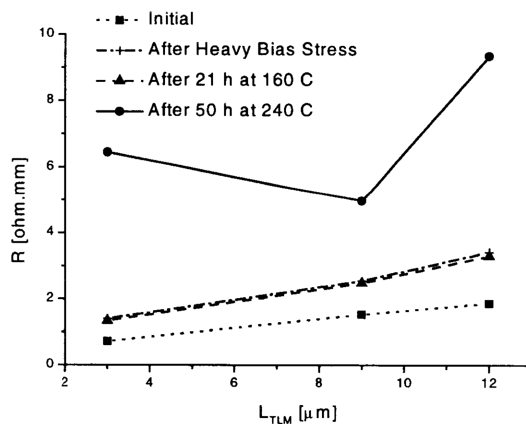
We found that the TLMs degrade at higher temperatures in the absence of bias. We investigated if this degradation is similar to the degradation caused by electrical stress. We have performed thermal stressing experiments. In these experiments three chips each one with 4 TLMs were heated in an N_2-environment. The TLMs of two of these chips were electrically degraded before the thermal treatment. The three chips were then put through the same temperature cycle. The evolution of the low-field resistance R for the two chips can be seen on Figs. 3-14 a), b) and c).



a)



b)



c)

Fig. 3-14: The resistance of the different TLMs, after different thermal steps on a a) virgin chip, b) on a chip that first was electrically stressed at a stressing voltage below the second critical voltage and c) on a chip, of which the 3 and 12 μm device first were electrically stressed at a stressing voltage far above second critical voltage, that were thermally stressed at 160 and 240 °C.

For the virgin devices on Fig. 3-14 a), R is found to increase at 240 °C, while it is unaffected at lower temperatures. The resistance increases by the same amount in all four devices. This suggests that the contact resistance is degrading. Fig. 3-14 b) shows a TLM of which the 4 devices have been electrically degraded weakly prior to thermal stressing but the stressing voltage never went over the second critical voltage. The electrical stressing both affects the contact as the sheet resistance, as the slope of R vs. L increases. R slightly recovers from the electrically induced damage by annealing at 160 °C. This recovery saturates very quickly with time. It is not possible to recover more than a few percent of the electrical stress damage. Further resistance degradation takes place at 240 °C. Here the additional degradation that is caused by the thermal stress is as large as the amount of thermal degradation of a virgin device as in Fig. 3-14 a). This suggests that the thermal stressing and the electrical stressing are independent.

Fig. 3-14 c) shows R during the critical steps of the same experiment for a TLM for which the devices were very heavily degraded before the thermal stressing. Now the effects of thermal degradation are a lot bigger than in the previous cases. Here it seems the electrical stress enhances the thermal degradation a lot. The thermal degradation now seems to affect both the sheet as the contact resistance, since the longer device show a greater degradation.

In a separate experiment, we have seen that the recovery takes place at temperatures between 140 and 180 °C. The thermal degradation was seen to take place at temperatures higher than 210 °C.

3.5. Light Experiments

Several possible mechanisms of degradation involve generation of electrons and holes. These can recombine and give their energy to the lattice, there by damaging it [31]. They also can get trapped by some defect and deplete the channel [40]. This generation of holes and electrons can also be caused by illumination.

We have tried to degrade these devices by illuminating them strongly, using an array of different light sources and optical systems. None of these experiments have caused any degradation. The strongest system we used involved a 100 mW laser focused on the channel, so that 10 % of its power uniformly is shined on the channel. The 1.6 eV photons of this system are able to generate electron-hole pairs. But even if all photons are absorbed and generate e-h pairs, then this results in only a current of 3 mA. The actual current could be a lot lower though. So it is plausible that no degradation was noticed even after illumination times of 10 hours, because not enough e-h recombination events took place. Focussing the beam more strongly heated up the device, causing it to degrade but not through e-h generation, as damage to the channel could be seen by visual inspection.

3.6. Conclusions

Electrical stress causes different degradation modes in TLMs. The sheet resistance is affected by the first mode of degradation, the contact resistance also degrades, but proportionally to the degradation of the sheet carrier concentration. When the bias

increases more, a second degradation mechanism appears where the contact resistance degrades without affecting the sheet carrier concentration.

The length dependence of the critical voltage for the different degradation modes shows that they appear at a constant field value. The uniformity of the degradation is also different for the two mechanisms, which shows that the damage occurs in different locations.

Thermal stressing experiments show that the TLMs recover slightly at temperature between 140 and 180 °C and that degradation takes place at temperatures higher than 220 °C. This degradation is additional to previous electrical degradation. It is independent of this electrical damage if the stress bias was kept below the second critical voltage. The thermal damage can then be attributed to an increase in the contact resistance. If the electrical stress is high, the subsequent thermal stress degrades both the contact and the sheet resistance.

We have been unsuccessful in degrading TLMs through light emission. But this could be explained by a too low intensity of the light source.

Chapter 4

Key Findings and Results

4.1. Introduction

This chapter contains results of degradation experiments that were done on TLMs and HEMTs with different heterostructures. A general discussion of these data follows, where we try to identify the different degradation mechanisms. We will conclude with a discussion of the mechanisms responsible for mHEMT degradation.

4.2. Degradation of TLMs with different Heterostructures

We have degraded devices with different cap structures that were grown at different locations. These devices were found to degrade in a different way. This section summarizes the results.

TLMs that were built at MIT on standard InP HEMT heterostructures [30] only showed R_C-degradation, as can be seen for the devices on Fig. 4-1. These devices do not have such a low resistance as the HP devices do. Their contact resistance has not been fully optimized. These devices are also InP lattice matched, but are grown on an InP substrate. The cap consists of undoped InGaAs. For these devices I_{sat} remained almost constant during stress. This suggests the sheet carrier concentration is unaffected by stress. These

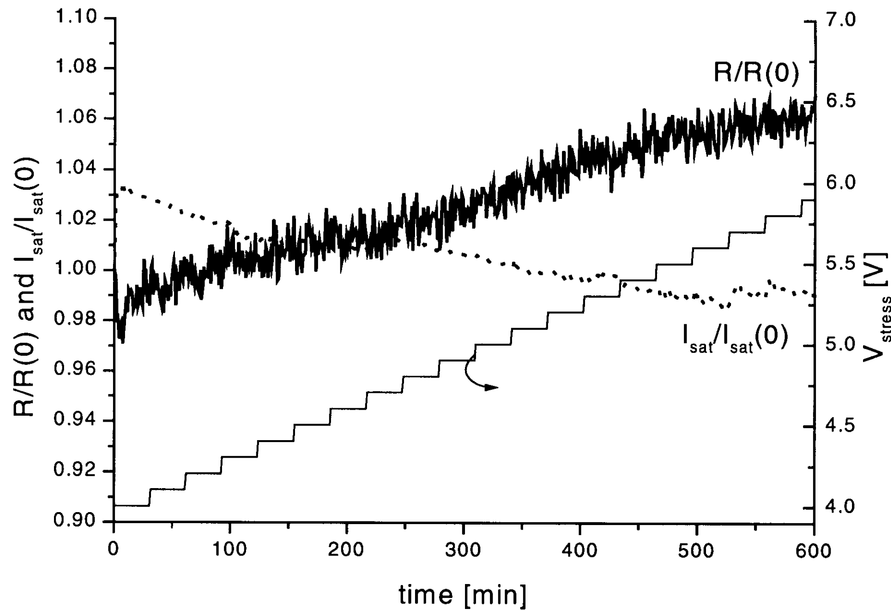


Fig. 4-1: Time evolution of R/R(0) and $I_{sat}/I_{sat}(0)$ during a step-stress experiment on a 10 μm wide TLM that was built at MIT. $R_D(0)$ is 5.44 Ω.mm.

devices do not show degradation similar to the first degradation modes of the HP devices that can be seen on Fig. 3-7, where the carrier concentration degrades. The degradation takes place at a very high voltage for the MIT device. It could be a similar kind of degradation as the second degradation mode in Fig. 3-7, where only the contact resistance is affected. This suggests the observed modes of degradation in the HP devices are related to their specific material structure.

If we look at other structures fabricated by Hewlett-Packard at HP Laboratories and degrade them in a similar way, we notice that they also show different degradation behavior. This can be seen on Fig. 4-2, which shows the time evolution of R for three devices with different structures. Fig. 4-3 shows the time evolution of I_{sat} during these

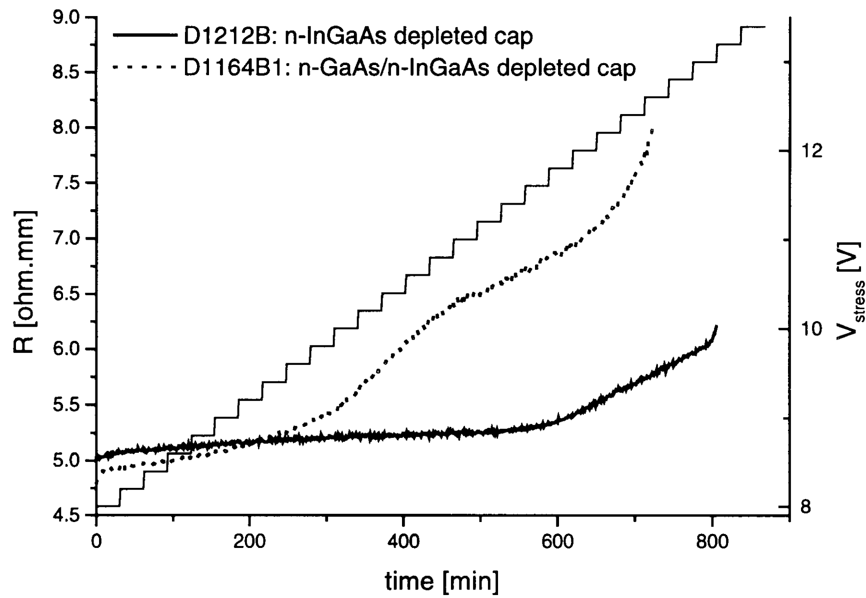


Fig. 4-2: Time evolution of R during step-stress for two 28 μm wide TLMs with a different structure.

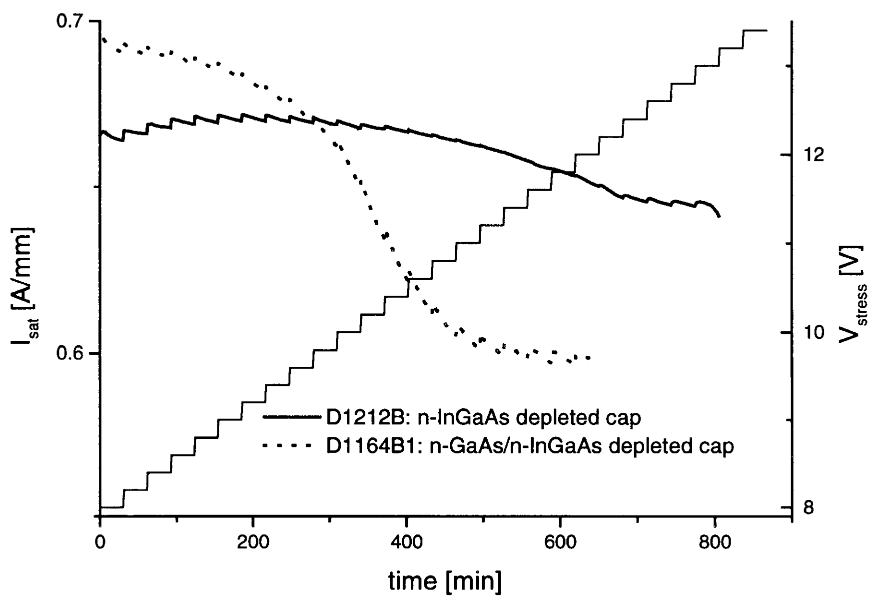


Fig. 4-3: Time evolution of I_{sat} during step-stress for two 28 μm wide TLMs with a different structure.

stress experiments for these three devices. All these devices have alloyed ohmic contacts.

One of these devices, D1164B1, has an n-GaAs/n-InGaAs depleted cap. For reference, the devices that were described in chapter 3 have an undepleted n-GaAs/n-InGaAs cap. This device shows a similar degradation behavior to the previously studied samples in chapter 3. Two degradation modes are clearly distinguishable. The first starts to occur at 8.8 V, while the second starts at 11.8 V for both samples. The first critical voltage also scales linearly with the length of the device as can be seen on Fig. 4-4. The offset is 2.7 V at L=0 μm, even after correction of $2R_CI \approx 0.8$ V, this is higher than in chapter 3. The constant field is 2200 V/cm. This field is about 600 V/cm higher than for the other devices in 3.3.4. The degradation for voltages below 11.8 V seems to be affecting both the sheet resistance and the contact resistance, since both I_{sat} and R degrade. The second degradation mode cannot be seen for the shortest devices from Fig. 4-4, as the device zaps before degrading. So we can not assess the length dependence of this second critical voltage. This second degradation mode seems to be caused by the degradation of R_C since I_{sat} is not degrading at this voltage as can be seen on Fig. 4-3. The observed degradation is very similar to that of the TLMs in chapter 3. The devices made at HP Laboratories seem to degrade at a higher voltage than the devices studied in chapter 3.

We studied an additional sample with an undoped InGaAs cap without the GaAs etch stop, this is marked D1212B on Figs. 4-2 and 4-3. This sample does not show the characteristic two degradation modes. Only the second degradation mode around 12 V seems to occur in this sample. There is a slight degradation of R and I_{sat} before 11.8 V,

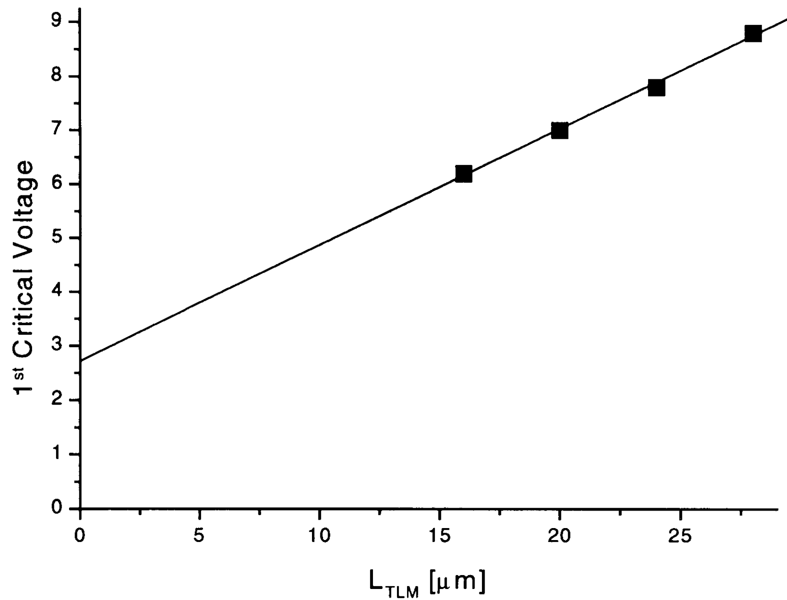


Fig. 4-4: First Critical Voltage for TLMs from wafer D1164B1, with a depleted n-InGaAs/GaAs cap, as a function of the length.

but it is a lot smaller than in the previous devices. The degradation of R at voltages higher than 12 V is not tracked by I_{sat}. This degradation mode only seems to only cause a degradation of the contact resistance, as it did with the samples from D1164B1 at high voltages.

All these samples from HP Labs started degrading at a higher voltage than the samples studied in chapter 3. The sample from HP Laboratories that degrades at the lowest critical voltage (D1164B1, which has a depleted GaAs-InGaAs cap) starts degrading at a voltage that is approximately 2 V higher than for the samples of similar described in chapter 3, with the undepleted GaAs-InGaAs cap.

4.3. Degradation of HEMTs with different Heterostructures

We also have performed some step-stress experiments on HEMTs grown at HP Labs on the different heterostructures. It was found that the devices on these wafers showed widely different initial characteristics, because of the different experimental cap structures. These device were stressed at a constant I_D and a constant $V_{DGo}+V_T$. The value of $V_{DGo}+V_T$ was incremented after constant time intervals.

The mHEMTs from the wafer with the depleted n-GaAs/n-InGaAs cap, D1164B1, show a time evolution during degradation that is very similar to the degradation of its TLMs. The time evolution of R_D and g_{mo} can be seen on Fig. 4-5. The two degradation modes that can be found in the degradation of a TLM from the same wafer on Fig. 4-2, at V=8.8 and 11.8 V can be found here at respectively $V_{DGo}+V_T$=1.4 V and 3.2 V. It seems that the degradation mechanisms are identical for the TLM and the mHEMT. The first degradation mechanism involves degradation of n_s and the second degradation mechanism only degrades the contact resistance. This is mirrored in the degradation of g_{mo}, where g_{mo} is not degrading at a higher voltage. At the start of the degradation, both sheet resistance and contact resistance degrade, where the contact resistance degrades at a higher voltage.

The mHEMTS from the wafer with a cap consisting out of depleted n-InGaAs (no GaAs etch-stop), D1212B, showed to degrade only very slightly as can be seen on Fig. 4-6. This figure shows the time evolution of R_D and g_{mo} during a step-stress experiment of a device with width 2×60 μm. The degradation that is occurring in this sample is probably

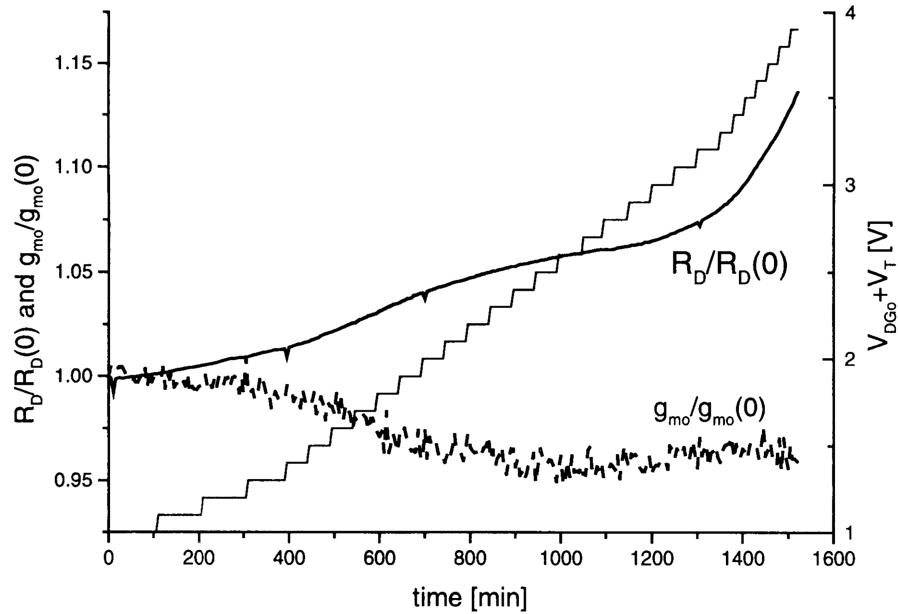


Fig. 4-5: Time evolution of R_D and g_{mo} during a step stress experiment on an mHEMT from wafer D1164B1, which has a depleted n-GaAs/n-InGaAs cap, with width 2×60 μm. $R_D(0)$ is 1 Ω.mm.

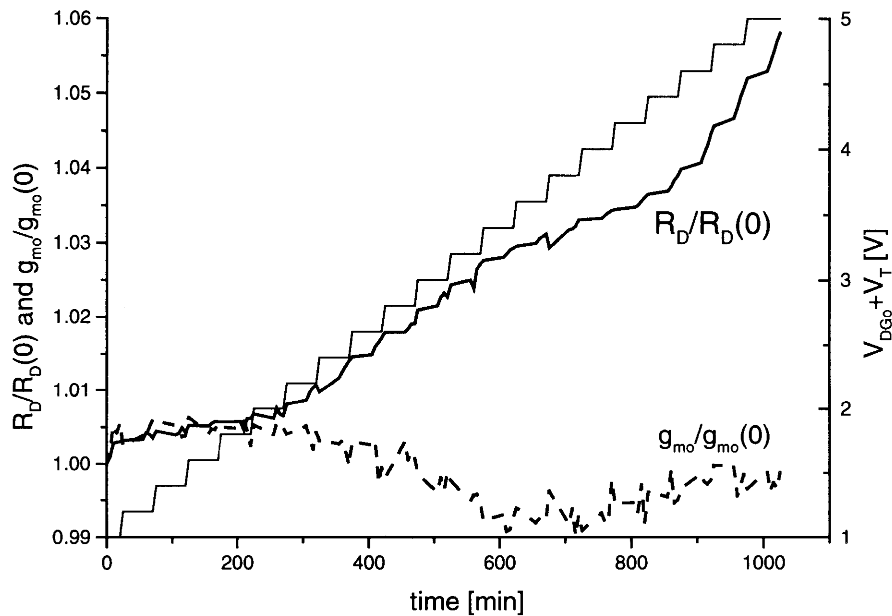


Fig. 4-6: Time evolution of R_D and g_{mo} during a step stress experiment on an mHEMT from wafer D1212B with width 2×60 μm, which has a depleted n-InGaAs cap. $R_D(0)$ is 1.06 Ω.mm.

caused by degradation of the contact resistance, since g_{mo} is unaffected by the stress. The voltage at which a change in R_D is occurring is a lot higher than with the devices from chapter 2. Some devices from this wafer, showed an anomalous degradation mode, where both R_S and R_D degraded. But none showed any observable degradation of n_s. The device degradation is consistent with a degradation of the contact resistance. This shows the same degradation pattern as the degradation of a TLM without the GaAs etch stop, where the sheet resistance does not degrade. This degradation of the contact resistance seems to occur at a higher voltage than the degradation of the sheet resistance.

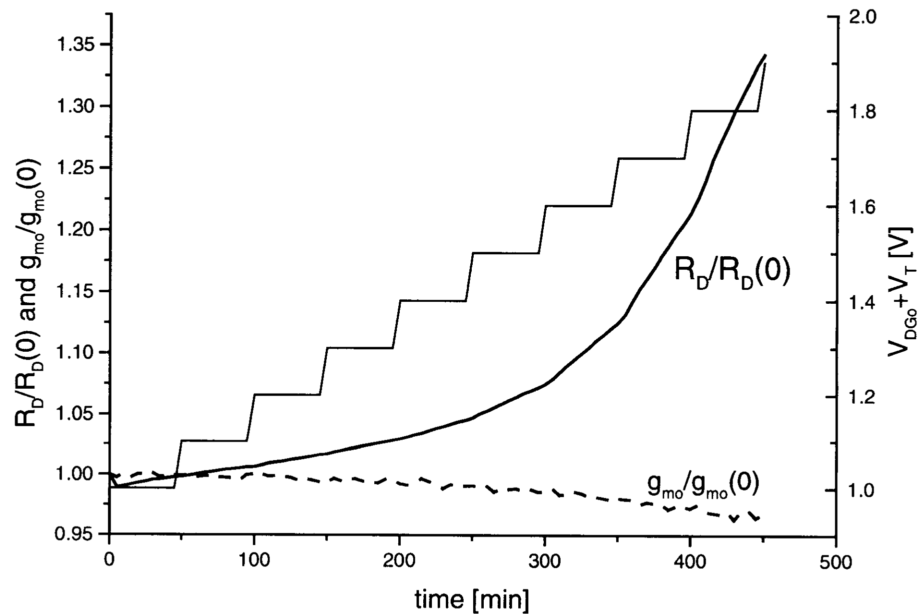


Fig. 4-7: Time evolution of R_D and g_{mo} during a step stress experiment on an mHEMT from wafer D1078B, which has an undepleted n-GaAs/n-InGaAs cap, with width 2×75 μm. $R_D(0)$ is 0.338 Ω.mm.

Wafer name	Cap	1st degradation mechanism	2nd degradation mechanism
all samples from chapters 2 and 3	Undepleted n-GaAs/n-InGaAs	Present	Present
D1212 B	Depleted n-InGaAs	Not Present	Present
D1164B1	Depleted n-GaAs/n-InGaAs	Present	Present
D1078 B	Undepleted n-GaAs/n-InGaAs	Present	Present

Table 4-1: Summary of the presence of the 1st and 2nd degradation mechanisms in the different wafers that have been studied. The 1st degradation mechanism is the mechanism where n_s decreases, causing R_s and R_C to degrade. The 2nd degradation mechanism causes only degradation of R_C without affecting R_s, this mechanism is noticed at higher voltages.

The mHEMTs from wafer D1078B, which has an undepleted n-GaAs/n-InGaAs cap, have a similar structure to the mHEMTs studied in chapter 2, but was grown at a a different location. These devices zap earlier than the other devices in this section, this could also be related to different factors like the recess width. The TLMs from this wafer could not be stressed and measured on our set-up as their I_{sat} is too high. The time evolution of R_D and g_{mo} can be seen on Fig. 4-7. We can see that the degradation is similar to the step-stress degradation in chapter 2. The same degradation pattern can be found for these devices. There also is a great similarity with the degradation of the depleted n-GaAs/n-InGaAs cap devices from wafer D1164B1. The same degradation mechanisms are occurring here.

Table 4-1 summarizes the results of this section.

4.4. Discussion on the Influence of the Heterostructure on the Degradation Mechanisms in TLMs and HEMTs

The first degradation mode, as seen for a 12 μm wide TLM in Fig. 3-7 at V=3.8 V, is characterized by a degradation of both the sheet and the contact resistance. However, as discussed in 3.3.3, R_C degrades because n_s is being reduced. We have found that for this mechanism the degradation is symmetric in the channel (3.3.5). We have seen this degradation mode in all mHEMTs and TLMs that contain both InGaAs and GaAs in the cap. This is independent of whether the cap is depleted or undepleted.

This first degradation mechanism seems to disappear when the GaAs layer is removed out of the cap. The GaAs etch-stop layer is not lattice matched to its neighboring layers. Several defects, such as misfit dislocations, could be present in such a layer. If they are not present to start with, the layer can act as a nucleation surface, as on such an interface the formation energy for a defect is significantly lowered. The different defects could then grow through some recombination-enhanced defect growth [31]. In this mechanism impact-ionization generated electrons and holes recombine and in doing so give their energy to the lattice. This energy is then used to aid the growth of dislocations or other crystallographic defects. These dislocations can also trap hot electrons thereby depleting the channel and causing R_s and R_C to increase significantly [32].

For the second degradation mode in TLMs, as in Fig. 3-7 for the 12 μm wide TLM, for V>4.5 V, the contact resistance degrades while the sheet resistance does not change. This is similar to the thermal degradation of a device at temperatures higher than 220 °C.

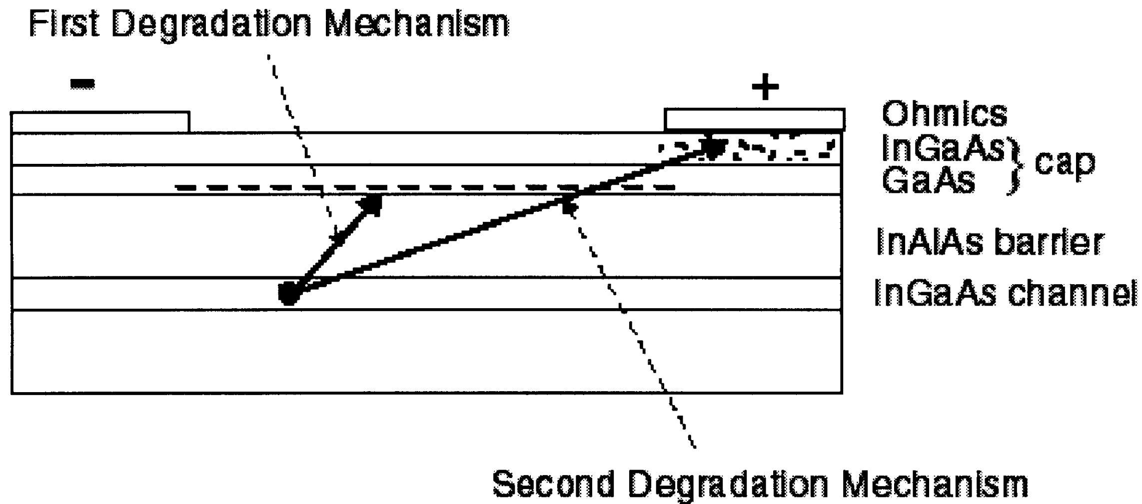


Fig. 4-8: Sketch of the two degradation mechanisms for a TLM.

Thermal degradation has been reported on non-alloyed ohmic contacts (such as the devices from chapter 3) on an InGaAs layer [33]. Indium has been found to leave the top InGaAs layer causing the contact resistance to increase. But the electrical degradation that we see is probably not caused by self-heating of the device. The power dissipated in the TLM during the second degradation mechanism is significantly lower than the power at the start before degradation can be seen. It is possible that local heating takes place through energy transfer from hot electrons to the lattice [34] and [35]. This mechanism has a signature that the damage cannot be annealed out. In fact, in this study we have never been able to anneal out any damage.

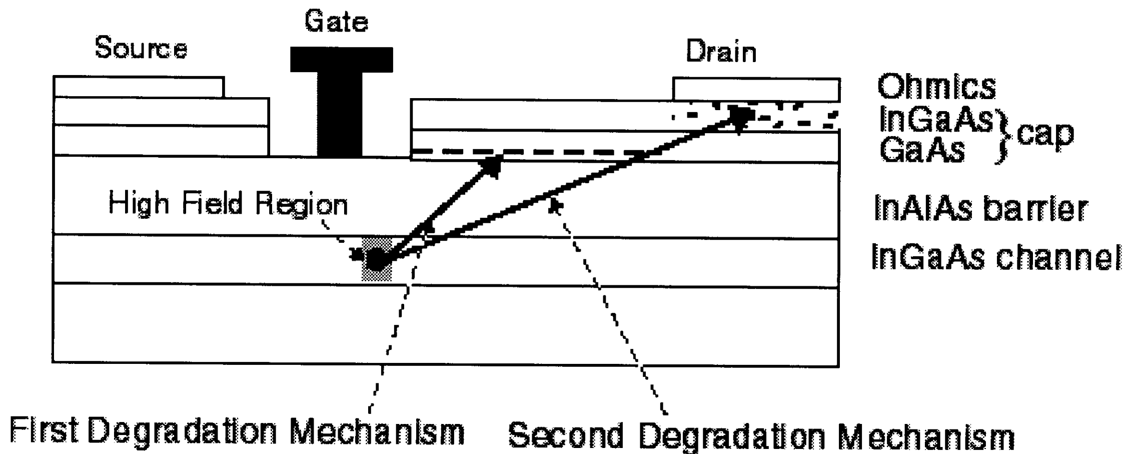


Fig. 4-9: Sketch of the two degradation mechanisms for an mHEMT.

4.5. The Degradation Mechanisms

In our experimental work, we have identified two different degradation mechanisms. This chapter will put all the evidence together and will give a description of those degradation mechanisms. There is one mechanism at low voltage where the sheet carrier concentration degrades, causing an increase in the sheet and the contact resistance. The second mechanism at higher voltage only involves a degradation of the contact resistance. Figs. 4-8 and 4-9 show a sketch of the two degradation mechanisms occurring in respectively a TLM and a HEMT.

4.5.1. The 1st Degradation Mechanism: Degradation of the Sheet Carrier Concentration

In a step-stress degradation of a HEMT from chapter 2 or a TLM from chapter 3, the first degradation observed is a decrease of sheet carrier concentration n_s which takes place at relatively low voltages. Table 4-2 contains the principal observations we made about this degradation mechanism and the conclusions we can make out of them.

TLM-Observation	HEMT-Observation	Conclusion
• At lower temperature the critical voltage drops • The degradation occurs at field when hot electrons start to appear/when impact-ionization starts to occur	• The degradation rate is proportional to $\exp(-B/(V_{DGo}+V_T))$ • We see Impact-Ionization occurring	Hot electrons and/or Impact-Ionization dominate the degradation
• I_{sat} decreases	• Degradation of BV_{DGoff} and R_D are related.	n_s decreases
• Some evidence for growth of defects	• No evidence of growth of defects	If growth of defects happens it needs holes
• No 1st degradation mechanism if there is no GaAs etch-stop in the cap.	• No 1st degradation mechanism if there is no GaAs etch-stop in the cap.	The damage takes place at the mismatched interface between GaAs and InAlAs
• The damage takes place symmetrically in the channel	• Most of the damage takes place at the drain side of the device, the source side is unaffected and the intrinsic device degrades slightly.	The damage takes place where the field is the highest
• The 1st degradation mechanism can not be produced thermally alone.		
• The critical voltage is linearly dependent on the length of the channel		Degradation occurs at constant field

Table 4-2: Observations and conclusions on the 1st degradation mechanism, which involves the degradation of the sheet carrier concentration.

All features of this degradation mechanism are consistent with trapping of hot electrons at defects that might exist inside the GaAs etch-stop layer or at the interface between the GaAs etch stop layer in the cap and the InAlAs isolation layer. These charged traps deplete the channel causing n_s to drop and subsequently the sheet resistance R_s and the contact resistance R_C to increase.

We have collected several pieces of evidence that correlate this degradation mechanism with the onset of impact-ionization. All these findings are also consistent with the existence of hot electrons. The experiments from 2.6.1, where the bias dependency of the degradation rate is studied, show that the degradation rate is proportional to the impact-ionization rate as can be seen on Fig. 2-19. This figure shows that there is an exponential relationship between the degradation rate of the drain resistance dR_D/dt and $(V_{DGo}+V_T)^{-1}$. This is a signature for impact-ionization, but this is also a signature for the energy of the hot electrons in the channel. We have also seen in 2.4.5 that the variance in the degradation between devices that were degraded under similar bias conditions decreased, if we decreased the variance in the impact-ionization rates during stress. For TLMs we have seen in 3.3.2 that this degradation mechanism starts at a higher critical voltage if the temperature is lowered to –65 °C. This is in agreement with impact-ionization playing a role as the impact-ionization rate is decreasing with decreasing temperature [29]. But hot electrons in this material system have a similar temperature dependence [36]. For TLMs we have seen that at room temperature degradation starts to take place at a field for which velocity saturation starts to occur. This material system has an equal threshold field for velocity saturation and for impact-ionization. The field at which this mechanism takes place is also around the threshold value (1400 V/cm) for which the hot electrons start to become hot [37], as we have seen in 3.3.4. The rate of impact-ionization is very strongly correlated with the amount of hot electrons. It is very hard to distinguish, between hot electrons and hot impact-ionization generated electrons.

We have seen that in HEMTs, the drain resistance is the figure of merit that is most affected by the degradation, while the source resistance is unaffected and the intrinsic region only degrades slightly. This is consistent with degradation taking place at the drain side of the device where a high electric field exists. We also have found convincing evidence that this degradation mechanism is caused by a decrease of n_s on the drain side of the device. For mHEMTs we have found in 2.6.2 that both the off-state breakdown voltage BV_{DGoff} and the drain resistance R_D are increasing during degradation in a universally related way, as can be seen in Figs. 2-22 and 2-23. The increase of BV_{DGoff} is linked to an increase of n_s on the drain side of the device [32]. Since both degradations seem to have a common origin, this can only be a decrease of n_s on the drain-side of the device. In TLMs we have seen in 3.3.1 that the saturation current I_{sat} decreases. As we have shown in 3.3.3, this can only be explained by a decrease in n_s. This decrease of n_s will increase both the sheet resistance, as the resistance is inversely proportional to $n_{s,}$ and the contact resistance, which can be explained through simple ohmic contact theory.

There are two possible mechanisms for this first mode of degradation, one where the hot electrons are trapped at the GaAs etch-stopper and deplete the channel [8]. There is also a possibility that holes reach the drain side of the cap and there recombine and through a recombination enhanced defect growth process, aid the growth of dislocations, which deplete the channel. The problem with this mechanism for HEMTs is that impact-ionization takes place at a distance of about 0.1 μm from the gate, where the high-field region is present [20]. The fields are forcing these holes towards the drain. Since the cap is 0.15 μm away from the gate, it is not possible that many holes reach the cap. If they

would do so they would be driven away from the drain, causing damage at a small part of the cap. This is in contradiction with the fact that the normalized degradation of the resistance of TLMs, where holes are created throughout the channel, and the drain resistance of HEMTS, where hole damage only can take place at a limited part of the cap, is of the same order of magnitude.

Now we have shown that the degradation of n_s exists and needs hot electrons. This degradation mechanism disappears if the GaAs etch stop layer is not present in the cap, as we have reported in 4.2 and 4.3. This layer is not lattice matched to its neighboring layers. This causes a high density of defects to be present at the interfaces of this layer. This interface could also act as a nucleation surface for several defects, such as misfit dislocations. These defects can trap hot electrons which will be collected at the interface by the traps. These negatively charged traps then deplete the channel, causing n_s to decrease. This layer has been reported to be of good quality in [19], the thickness should be small enough to have a good doping efficiency [38]. The effects of hot electrons have been previously described in [12],[39] , [40] and [41].

There have been some clues in TLMs that the defects can grow through a recombination enhanced defect growth mechanism. In such a mechanism the impact-ionization generated holes recombine with electrons, thereby giving their energy in the form of phonons to the lattice. These provide the extra energy needed for a defect to grow. In TLMs we have reported in 3.2.1 that there was an initial period were the degradation was very slow, before suddenly taking off. This could be explained through a mechanism

where the defects first have to grow before being able to trap enough electrons to affect the resistance. This could explain the sudden increase in degradation rate we observed in 3.2.2. We have not seen such a delay in mHEMTs. This recombination enhanced mechanism could not take place in a mHEMT, since the holes are being swept up by the gate and do not reach the cap layer on the drain-side of the device.

It is uncertain if the decrease in C_{dg} at a higher bias stress reported in 2.6.1 and 2.6.2 is caused by a new degradation mechanism. If damage would occur very close to the gate, this could increase the depletion layer for high drain bias. This would decrease the capacitance. Maybe at a lower voltage the damage takes place far enough from the gate not to affect the capacitance.

This degradation of n_s can explain the degradation of the different figures of merit. Since the high field necessary for hot electrons to exist or impact-ionization to take place occurs between gate and drain the depletion of n_s will take place in that region. A decrease of n_s there will increase R_D but should not affect R_S, which it is observed does not change. A decrease of n_s near the gate should decrease g_{mo} and g_{do} somehow. BV_{DGoff} will increase if n_s decreases. This decrease in n_s will also decrease f_T and I_D to some extent. We have reported on these changes in 2.5 and have seen the expected degradations occur.

In summary, this section shows that the degradation mechanism where hot electrons get trapped by defects at the interface between the GaAs and InAlAs layers, depleting the channel and decreasing n_s, is consistent with the observed degradation of these devices.

TLM-Observation	HEMT-Observation	Conclusion
• I_{sat} does not decrease	• g_{mo} does not degrade	n_s is unaffected , the ohmic contacts degrade
• 2nd degradation mechanism is present if there is no GaAs etch-stop in the cap.	• 2nd degradation mechanism is present if there is no GaAs etch-stop in the cap	The damage is not related to the GaAs etch-stopper.
• The damage does not take place symmetrically in the channel	• The drain resistance degrades but the source resistance does not	The damage takes place at the ohmic contact the hot electrons are impinging on
• The damage is similar to that caused by thermal stress		
• The critical voltage is linearly dependent on the length of the channel		The degradation is caused by a constant field

Table 4-3: Observations and conclusions on the 2nd degradation mechanism which involves the degradation of the ohmic contacts.

4.5.2. The 2nd Degradation Mechanism: Degradation of the Contact Resistance

We have reported in 3.3.3 that a second, different degradation mechanism occurs at higher voltages. This mechanism degrades the contact resistance without changing the sheet resistance. This mechanism is likely to be caused by hot electrons, which damage the ohmic contacts, there by increasing the contact resistance. In 4.4 we saw that this mechanism clearly occurred in mHEMTs. At a high voltage, the intrinsic transconductance, g_{mo}, of a HEMT is not affected by stress, while R_D still increases significantly.

This second mechanism is caused by hot electrons. This explains that the degradation of a TLM is not symmetric any more at a high voltage as reported in 3.3.5, since the hot electrons only go through one contact. This is also the degradation mechanism that takes

place in TLMs during the thermal degradation experiments of 3.5. Thermal degradation causes the contact resistance to increase.

4.6. Conclusions

TLMs fabricated at MIT only showed a degradation of the contact resistance. Devices fabricated at the Hewlett-Packard Labs with different material structures, showed different degradation patterns. There was a great similarity in the time evolution of the degradation of a TLM and an mHEMT from the same wafer during step-stress degradation experiments.

The wafers with a n-GaAs/n-InGaAs cap degraded in a similar way, irrespective if the cap was depleted or not. In these samples, we could see both degradation mechanisms taking place.

The devices without a GaAs layer in the cap only showed degradation of the contact resistance at high voltage. This suggests that the sheet resistance degradation in devices with the GaAs etch-stop is caused by the interface between the GaAs and the InAlAs layer or within the GaAs layer itself. The GaAs cap and its interface with the InAlAs are likely to have defects since their relaxed lattice constants are very different.

We have identified two degradation mechanisms. In the first mechanism, the sheet carrier concentration in the channel decreases. This causes the sheet and contact resistance to degrade. This degradation is likely caused by hot electrons being trapped by dislocations

present at the interface between the InAlAs barrier layer and the GaAs etch stop layer. In the second mechanism at higher voltages, the contact resistance of the device degrades without degradation of the sheet resistance.

We have seen that the degradation of the sheet carrier concentration saturates if enough damage has occurred. It seems the contact resistance degradation does not seem to saturate. This could be explained as degradation might not saturate before critical damage occurred to the device.

In the next chapter we will summarize our conclusions and our suggestions to mitigate this problem of degradation.

Chapter 5

Conclusions and Suggestions

5.1. Conclusions

We have developed a stress and measurement set-up to study the electrical degradation of metamorphic High Electron Mobility Transistors (mHEMTs) and Transmission Line Method structures (TLMs).

For mHEMTs, we found electrical degradation, as reported in [7], where the drain resistance R_D degrades severely, the intrinsic device degrades slightly and at the source side of the device no degradation takes place. We found that a degradation scheme that kept the impact-ionization rate constant, delivered the physically most meaningful results. We validated step-stress experiments as an efficient technique to study the bias-dependence of the degradation. We found that the degradation was related to a decrease of the sheet carrier concentration at low voltages. At high voltages the degradation is related to a degradation of the ohmic contacts.

For TLMs, we also saw degradation of the low-field resistance, R, and the saturation current, I_{sat}. With TLMs we could clearly identify two different degradation mechanisms. As for mHEMTs we could see that the sheet carrier concentration is degrading at low stress bias. But we also saw that at a high stress bias R degrades without affecting I_{sat}. The TLMs have also been seen to degrade through thermal stress, with the thermal degradation being caused by the changes in the non-alloyed ohmic contacts.

By studying TLMs and mHEMTs with a different heterostructure, we found that the novel heterostructure of these devices may lie at the origin for their degradation behavior. We found that degradation of the sheet resistance did not take place in samples lacking the GaAs etch-stop.

Our experiments have identified two different degradation mechanisms in metamorphic HEMTs. The first degradation mechanism, which occurs at a relatively low field, appears to be caused by hot electrons that get trapped by defects at the interface between the AlInAs barrier layer and the GaAs etch-stop in the cap. These negatively charged traps deplete the channel, causing the sheet carrier concentration n_s to drop. This causes the observed degradation of the device, with the increase of R_D as the most serious symptom. The second degradation mechanism, which occurs at a higher field is caused by the degradation of the non-alloyed InGaAs ohmic contacts through hot electrons impinging onto it.

Both of these mechanisms appear to be caused by hot electrons. We have seen that the impact-ionization rate seems to be important in the degradation of these devices, but this rate is also a measure for the flow and energy of the hot electrons. We have seen that at the fields needed for the hot electrons to cross the barrier separating the channel from the cap and get trapped, impact-ionization takes place.

We have not seen any evidence that would link the degradation to the GaAs substrate or the metamorphic nature of the structure.

5.2. Suggestions

We have seen that the electrical degradation probably takes place at the interface between the GaAs etch-stop and the InAlAs barrier layer or inside the GaAs etch-stop layer itself. The degradation could be caused by hot electrons that are trapped in this layer or at the interface. The formation of hot electrons can not be prevented and it is probably unpractical to stop them from going over the barrier. The best way to stop the degradation is to eliminate the defects where they can get trapped. This could be done by replacing the GaAs etch-stop layer by a lattice-matched layer. Some wafers with the n-GaAs/n-InGaAs cap have recently been found to be reliable until higher voltages [42], so the quality of the layers could play an important role in the degradation. These layers have been reported to be of good quality though [20], so it could be possible to improve the quality of the layers to avoid having traps. This has been reported on some of the newest devices grown [43].

We have not been able to induce any damage through light. This deserves further study because it would be an interesting confirmation for the trapping mechanism in the degradation. It would also be interesting to follow the degradation of a Hall bar. This could reconfirm the drop in sheet carrier concentration.

The degradation of the ohmic contacts could be further investigated through micro-Raman or some other analytical technique, which can map the elements that can be found under the contact. We also have not been able to do some direct physical observations on the interface between the GaAs etch-stop and the AlGaAs barrier. Planar or cross-section

TEM pictures might reveal more about the nature of the trapping defects. It could also teach us if growth of defects is taking place or not.

It would be interesting to study the temperature dependence of the degradation. A better knowledge of the dependence might enable us to separate impact-ionization from hot electron effects. There is still some uncertainty about the initial condition of the sample with the pure n+ GaAs cap. We do not exactly know what the meaning is of the intersection with L=0 of the critical voltage versus channel length plot. It would be interesting to learn more about the meaning of the slope of this line. This could fit in a theory of Gunn domain formation currently being developed by H. Rohdin [43].

We have also observed that the degradation caused the devices to zap at higher fields. More study into this might help our understanding of the destructive breakdown of these devices.

References

[1] S. Krishnamurthy, A. Sher and A.-B. Chen, "Velocity-field characteristics of III-V semiconductor alloys: Band structure influences," *J. Appl. Phys.*, vol. 61, pp. 1475-1479, 1987.

[2] K.Hikosaka, S. Sasa, N. Harada and S. Kuroda, "Current-gain cutoff frequency comparison of inGaAs HEMTs, " *IEEE Device Lett.*, vol. 9, no. 5, pp.241-243, 1988.

[3] L. Nguyen, A. Brown, M. Thompson and L. Jelloian, "50-nm self-alligned-gate pseudomorphic AlInAs/GaInAs high electron mobility transistors," *IEEE Trans. Electron Devices*, vol. 39, pp. 2007-2014, 1992.

[4] P. Smith, S.-M. Liu, M.-Y. Kao, P. Ho, S. Wang, K. Duh, S. Fu and P. Chao, "W-Band high efficiency InP-based power HEMT with 600 GHz f_{max}," *IEEE Microwave Guided Wave Lett.*, vol. 5, no. 7, pp. 230-232, 1995.

[5] E. Zanoni, "Reliability of active microwave devices: a tutorial," *G-SC1: GAAS98*, EuMicrowave Week, 1998.

[6] J.-M. Dumas and D. Lecrosnier, "Status of the parasitic effects and reliability issues of InP electron devices, " *Proc. 4th InP and Rel. Mat. Conf.*, pp.214-17, 1992.

[7] A. Wakita, H. Rohdin, C.-Y. Su, n. Moll, A. Nagy and V. Robbins, "Drain resistance Degradation Under High Fields in AlInAs/GaInAs MODFETs," *Proc. 9th InP and Rel. Mat. Conf.*, pp. 376-379, 1997.

[8] G. Meneghesso, F. Magistrali, D. Sala, M. Vanzi, C. Canali and E. Zanoni, "Faillure Mechanisms due to metallurgical interactions in commercially available AlGaAs/GaAs and AlGaAs/InGaAs HEMTs," *Microelectron. Reliab.*, vol. 38, no. 4, pp.497-506, 1998.

[9] Y. Ashizawa, C. Nozaki, T. Noda and A.Sasaki, "Thermal Stability of Interfaces between metals and InP-based materials," *Journal of Electronic Materials*, vol. 25, no. 4, pp. 715-719, 1996.

[10] C. Canali, F. Castaldo, F. Fantini, D. Ogliari, L. Umena and E. Zanoni, "Gate Metallization "Sinking" into the active channel in Ti/W/Au metallized Power MESFET's", *IEEE Electron Device Lett.*, vol. 7, no. 3, pp. 185-186, 1986.

[11] K. Christianson, C. Moglestue and W. Anderson, "Faillure Mechanisms in AlGaAs/GaAs HEMTs," *Solid-State Electronics*, vol. 38, no. 9, pp. 1623-1626, 1995.

[12] R. Menozzi, M. Borgarino, Y. Baeyens, M. Van Hove and F. Fantini, "On the effects of hot electrons on the DC and RF characteristics of lattice-matched InAlAs/InGaAs/InP HEMT's," *IEEE Microwave and Guided Wave Letters*, vol. 7, no. 1, 1997.

[13] Y. Ashizawa, C. Nozaki, T. Noda, A.Sasaki and S. Fujita, "Surface related degradation of InP-Based HEMTs during thermal stress," *Solid-State Electronics*, vol. 38, no. 9, pp. 1627-1630, 1995.

[14] T. Ishida, Y. Yamamoto, N. Hayafuji, S. Miyakuni, R. Hattori, T. Ishikawa and Y. Mitsui "Fluorine limited reliability of AlInAs/InGaAs high electron mobility Transistors with molybdenum gates," *Proc. 9th Int. Conf. on InP and Rel. Mat*, pp. 201-204, 1997.

[15] H. Sasaki, K. Yajima, N. Yoshida, O. Ishihara and S. Mitsui, "Reliability of InAlAs/InGaAs/InP HEMT with Wsi ohmic contacts," *Proc. 7th Int. Conf. on Inp and Rel. Mat.*, p. 745-748, 1995.

[16] M. Tutt, G. Ng, D. Pavlidis and J. Mansfield,"Reliability issues of InAlAs/InGaAs high-electron-mobility transistor", *Proc. 3rd InP an Rel. Mat. Conf.*, pp. 349-352, 1991.

[17] Hafizi and M. Delaney ,"Reliability of InP-based HBT's and HEMT's:experiments, faillure mechanisms, and statistics," *Proc. 6th Int. Conf. on InP and Rel. Mat.*, p. 299-302, 1994.

[18] H. Rohdin, S.-Y. Su, N. Moll, A. Wakita, A. Nagy, V. Robbins and M. Kauffman, "Semi-analytical Analysis for optimization of 0.1 μm InGaAs-channel MODFETs with emphasis on on-state breakdown and reliability," *Proc. 9th Int. Conf. on Inp and Rel. Mat*, p. 357-360, 1997.

[19] H. Rohdin, A. Wakita, A. Nagy, V. Robbins, N. Moll and C.-Y. Su,"A 0.1 μm mHEMT millimeter-wave IC technology designed for manufacturability," *Solid State Electronics*, To Be Published, 1999.

[20] H. Rohdin, A. Nagy, V. Robbins, A., C.-Y. Su, Wakita, J. Seeger, T. Hwang, P. Chye, P. Gregory, S. Bahl, F. Kellert, L. Studebaker, D. D'Avanzo and S. Johnsen, "0.1 μm Gate-length AlINAs/GaInAs/GaAs MODFET MMIC process for applications in high-speed wireless communications," *The Hewlett-Packard Journal*, Art.4, February, 1998.

[21] A. Wakita, H. Rohdin, V. Robbins, N. Moll, C.-Y. Su, A. Nagy and D. Basile, "Low-noise bias reliability of AlInAs/GaInAs MODFET's with linearly graded low-temperature buffer layers grown on GaAs substrates," *Proc. 10th Int. Conf. on Inp and Rel. Mat*, p. 1-4, 1998.

[22] A. Wakita, C.-Y. Su, H. Rohdin, H.-Y. Liu, A. Lee, J. Seeger and V. Robbins, "Novel high-yield trilayer resist process for 0.1 mu m T-gate fabrication," *Journal of Vacuum Science & Technology B*, vol.13, no.6, pp.2725-8, 1995.

[23] G. Dambrine, A. Cappy, F. Heliodore and E. Playez, "A new method for determining the FET small-signal equivalent Circuit," *IEEE Trans on Microwave Theory and Techniques*, Vol. 36, no. 7, p. 1151-1159, 1988.

[24] S. Bahl and J, del Alamo, "A new drain-current injection technique for the measurement of off-state breakdown voltage in FET's," *IEEE Transactions on Electron Devices*, Vol. 40, no. 8, p.1558-1560, 1993.

[25] M. Somerville, R. Blanchard, J. del Alamo,G. Duh,and P.C. Chao, "A new gate current extraction technique for measurement of on-state breakdown voltage in HEMTs," *IEEE Electron Device Letters*, vol.19, no.11, p.405-7, 1998.

[26] A. Moolji, S. Bahl and J. del Alamo, "Impact ionization in InAlAs/InGaAs HFET's," *IEEE Electron Device Letters*, vol.15, no.8, p.313-15. 1994.

[27] S. Chou and D. Antoniadis, "Relationship between measured and intrinsic transconductances of FETs," *IEEE Transactions on Electron Devices*, vol.ED-34, no.2, pt.1, .448-50, 1987.

[28] J. del Alamo, "Physics of Semiconductor Devices," *Course Notes of MIT class 6.720.*

[29] G. Meneghesso, A. Mion, A. Neviani, M. Matloubian, J. Brown, M. Hafizi, L. Takyiu, C. Canali, M. Pavesi, M. Manfredi, E. Zanoni, "Effects of channel quantization and temperature on off-state and on-state breakdown in composite channel and conventional InP-based HEMTs," *Technical Digest International Electron Devices Meeting*, p.43-46, 1996.

[30] R. Blanchard,"Hydrogen Degradation of InP HEMTs," *PhD Thesis*, EECS, MIT, 1999.

[31] T. Henderson, “Model for degradation of GaAs/AlGaAs HBTs under temperature and current stress,” *International Electron Devices Meeting 95*, p.811-814, 1995.

[32], R. Menozzi, M. Borgarino, K. van der Zanden and D.Schreurs, ”On the correlation between Drain-Gate Breakdown and hot-electron reliability in InP HEMT’s,” *IEEE Electron Device Lett.*, Vol. 20, no. 4, 1999.

[33] C.-T. Lee, K.-L. Jaw and C.-D. Tsai, “Thermal stability of Ti/Pt/Au ohmic contacts on InAs/graded InGaAs layers,” *Solid-State Electronics*, Vol. 42, no. 5, p. 871-875, 1998.

[34] A. Wakita, N. Moll, S. Rosner and A. Fischer-Colbrie,”Thermal stability of MoAu and TiPtAu nonalloyed InGaAs contacts,” *J. Vac. Sci. Technol. B*, Vol. 13, no. 5, p.2092-2099, 1995.

[35] Y. Shinuzoka, “Mechanism of defect reactions in semiconductors,” *Mat. Res. Soc. Symp. Proc.*, Vol. 442, p. 225-230, 1997.

[36] E. Martinez, M. Shur and F. Schuermeyer, “Analysis of the hot-electron regime of operation in heterostructure field effect transistors,” *URSI International Symposium on Signals, Systems, and Electronics*, p.167 –170, 1995.

[37] M. Fischetti, N. Sano, S. Laux, K. Natori, “Full-band-structure theory of high-field transport and impact ionization of electrons and holes in Ge, Si,and GaAs,” *IEEE Transactions on Semiconductor Technology Modeling and Simulation.*

[38] P. Pizani, T. Boschi, F. Lanciotti Jr, J. Groenen, R. Carles, P. Maige, M. Gendry, “Alloying effects on the critical layer thickness in $In_xGa_{1-x}As$/InP heterostructures analyzed by Raman scattering,” *Applied Physics Letters*, Vol.72, no.4, p. 436-438. 1998.

[39] M. Borgarino, R. Menozzi, Y. Baeyens, P. Cova and F. Fantini, "Hot electron degradation of the DC and RF characteristics of AlGaAs/InGaAs/GaAs PHEMT's," *IEEE Transactions on Electron Devices*, Vol. 45, no. 2, p. 366-371, 1998.

[40] G. Meneghesso, E. De Bortoli, P. Cova and R. Menozzi, "On temperature and hot electron induced degradation in AlGaAs/InGaAs PM-HEMT's," *IEEE 1995Workshop on High Performance Electron Devices for Microwave and Optoelectronic Applications*, p. 136 –141, 1995.

[41] R. Menozzi, M. Borgarino, Y. Baeyens, K. van der Zanden, M. Van Hove and F. Fantini, "The effect of passivation on the hot electron degradation of lattice-matched InAlAs/InGaAs/InP HEMTs," *Proc. 9th Int. Conf. on Inp and Rel. Mat*, p. 153 –156, 1997.

[42] L. Studebaker, private communication.

[43] H. Rohdin, private communication.

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