Characterization of Bonded Copper Interconnects for Three-Dimensional Integrated Circuits

by

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Abstract

The unprecedented growth of the semiconductor industry is demanding ultra large-scale integrated (ULSI) circuits with increasing performance at minimum cost and power dissipation. As the critical dimensions in ULSI design continue to shrink, system performance of integrated circuits will be increasingly dominated by interconnect delay.

Three-dimensional (3-D) ICs can reduce interconnect delay problems by offering flexibility in system design, placement and routing. 3-D ICs can be formed by vertical integration of multiple device layers using wafer bonding, recrystallization or selective epitaxial growth. The flexibility to place devices along the vertical dimension allows higher device density and reduced total interconnect lengths in 3-D ICs.

One approach to fabrication of 3D integrated circuits is to bond previously-processed device layers using metal-metal bonds that also serve as layer-to-layer interconnects. Evaluation of the feasibility of wafer bonding for 3-D integration relies on our ability to characterize bonded interconnects. The reliability of devices containing multi-layer thin film structures is strongly influenced by the adhesion properties of the many interfaces present. Interface fracture failure is highly likely given the high thermal stresses developed during processing and also during service.

A four-point bend test technique has been used to evaluate the strength of Cu-Cu bonds. Test structures were fabricated by bonding wafers containing copper lines (with Ta barrier) that were patterned on silicon dioxide. Tests on the thermocompression-bonded copper lines yielded reproducible fracture toughness values (1-10 J/m²) for bonds created at 300°C-400°C. The effect of process parameters on bond strength was studied. It was found that surface copper oxide removal prior to bonding using a forming gas purge (95%Ar-5%H₂) resulted in higher toughness values and lesser variations compared to a N₂ purge. Also, bond strength was found to increase with increasing bonding temperature. Thicker bonded films resulted in stronger bonds. Interface failure was found to be most likely at the Cu-Cu and Ta-Silicon dioxide interfaces. The results obtained from different process conditions were used to optimize the bonding process.

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**Contents**

**LIST OF FIGURES**

**LIST OF TABLES**

<table>
<thead>
<tr>
<th>1</th>
<th>INTRODUCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>Motivation</td>
</tr>
<tr>
<td>1.2</td>
<td>Three-Dimensional Integration</td>
</tr>
<tr>
<td>1.2.1</td>
<td>Interconnect Wire Length Reduction with 3-D Integration</td>
</tr>
<tr>
<td>1.2.2</td>
<td>System-on-a-Chip Design</td>
</tr>
<tr>
<td>1.2.3</td>
<td>Technology Options for 3-D Integration</td>
</tr>
<tr>
<td>1.3</td>
<td>Processed Wafer Bonding</td>
</tr>
<tr>
<td>1.3.1</td>
<td>Technology Options for Vertical Interconnects</td>
</tr>
<tr>
<td>1.4</td>
<td>3-D Integration: Challenges</td>
</tr>
<tr>
<td>1.4.1</td>
<td>Thermal Issues</td>
</tr>
<tr>
<td>1.4.2</td>
<td>Electromagnetic Interactions</td>
</tr>
<tr>
<td>1.4.3</td>
<td>Reliability Issues</td>
</tr>
<tr>
<td>1.5</td>
<td>Quantitative Analysis of Bond Reliability for 3-D Integration</td>
</tr>
<tr>
<td>1.5.1</td>
<td>Measurement of Interface Adhesion</td>
</tr>
<tr>
<td>1.5.2</td>
<td>Application of Fracture Mechanics to Interface Adhesion</td>
</tr>
<tr>
<td>1.5.3</td>
<td>Four-Point Bend Test</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>2</th>
<th>EXPERIMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1</td>
<td>Fabrication</td>
</tr>
</tbody>
</table>

7

9

10

10

11

12

12

13

15

16

18

18

18

19

21

22

23

26

29

29
2.2 Mechanical Testing

3 RESULTS AND DISCUSSION

3.1 Testing of Bonded Continuous Films
3.2 Testing of Bonded Cu/Ta Lines
   3.2.1 Effect of Ambient on Bond Quality
   3.2.2 Effect of Temperature on Bond Quality
   3.2.3 Effect of Pre-Bonding Clean Step on Bond Quality
   3.2.4 Effect of Copper Film Thickness on Bond Quality
3.3 Analysis of Fractured Surfaces

4 SUMMARY AND FUTURE WORK

4.1 Summary
4.2 Future Work

APPENDIX A – Fabrication Process Flow of 3-D ICs Based on Wafer Bonding

BIBLIOGRAPHY
List of Figures

1-1 The wire-length distribution in 2-D and 3-D implementation of logic circuits. Three-dimensional integration results in narrower wire-length distribution. 12

1-2 Cross-section of a 3-D integrated circuit formed by face-to-back Cu-Cu wafer bonding. 16

1-3 Schematic illustration of the dependence of G on \( \psi \). Different tests for the measurement of G involve a wide range of \( \psi \) values. 25

1-4 Four-point bend test specimen. 27

2-1 The process flow for fabrication of four-point bend test structures- (a) (100) silicon DSP wafer; (b) 1000Å-thick LPCVD silicon nitride; (c) patterned photoresist used as etch mask for silicon nitride patterning; (d) silicon nitride dry etched; (e) 50\( \mu \)m deep anisotropic silicon etch using KOH; (f) silicon nitride stripped using phosphoric acid; (g) cross-sectional view rotated 90\(^0\) shows 3000Å-thick thermal oxide grown; (h) image-reversal photoresist patterning and 500Å/3000Å Ta/Cu deposition using e-beam evaporation; (i)-(l): steps (g) and (h) performed on (100) silicon SSP wafer. 31

2-2 Fabrication process flow, continued. (a) and (b): Lift-off done on wafers 2-1 (h) and (l); (c) thermocompression bonding of the patterned wafers; (d) cross-sectional view (90\(^0\) rotation) shows bonded wafer-pair with trench in bottom (DSP) wafer made by diamond saw. 32

2-3 (a) Infra-Red Camera image of bonded wafer; each rectangular strip is a four-point test specimen, and contains a set of parallel metallization lines. (b) Four-Point test
specimens were diced from the bonded wafer; rectangle in (a) shows single specimen.

3-1 Typical Load-Displacement behavior from Four-point test. (a) elastic loading of bulk material. (b) plateau load-steady state crack propagation. (c) unloading.

3-2 Four-point test result for thick (0.12μm) Cu stack. The initial elastic loading is seen followed by abrupt dip in load due to Mode I Crack Propagation.

3-3 (a) Cu fracture surface- Ductile Failure, (b) Ta/SiO₂ fracture surface showing Brittle Failure.

A-1 The process flow for fabricating 3-D ICs.

A-2 The process flow for fabricating 3-D ICs.
List of Tables

3-1 Fracture Toughness values for samples bonded under different ambient. 38

3-2 Fracture Toughness values (J/m²) for samples bonded at different temperatures. 41

3-3 Fracture Toughness values (J/m²) for samples bonded with different pre-bonding clean steps. 42

3-4 Variation of Fracture Toughness with Cu Stack thickness. 43
Chapter 1

Introduction

1.1 Motivation

The unprecedented growth of the semiconductor industry is demanding ultra large-scale integrated (ULSI) circuits with increasing performance at minimum cost and power dissipation. Components such as high performance microprocessors and static or dynamic random access memories (SRAMs or DRAMs) rely on transistor and interconnect scaling to meet density and performance targets. Transistor scaling improves both speed and density. However, interconnect scaling improves density at the expense of degraded delay. Also, increasing interconnect loading affects the power consumption in high performance chips. A significant fraction of the total power consumption can be due to the wiring network used for clock distribution, which is usually realized using long global wires [1].

In traditional 2-D ICs, chip size is continually increasing due to the growing demand for functionality and higher performance. Chip design is increasingly complex, requiring more and more transistors to be closely packed and connected. Such complex chip design has a negative impact on the performance of interconnect wires. Interconnect pitch is reduced to meet the wiring density requirement. This reduction in pitch, coupled with smaller wire cross sections and longer lines to traverse larger chips, increases the resistance and capacitance of these lines resulting in a significant increase in RC delay. As interconnect scaling continues, RC delay is increasingly becoming the dominant factor determining the performance of advanced ICs [2].

Traditional materials for multi-level metallization, namely, Al and SiO₂, are being replaced by low resistivity metal such as Cu and low-k inter-level dielectrics (ILDs). Technology solutions based on Cu and low-k dielectrics are expected to alleviate the adverse effect of increasing interconnect delay [3]. However, in deep-submicrometer
dimensions, material effects come into play. Increased electron surface scattering of copper leads to increasing metal resistivity. Finite barrier layer thickness also contributes to higher resistivity. As shown in the international technology roadmaps for semiconductors (ITRS) [4], below 130-nm technology node, substantial interconnect delays will result in spite of the introduction of these new materials. This will severely limit chip performance. This limitation necessitates a paradigm shift from present IC architecture for the performance enhancement of advanced ULSI circuits. Greater performance and greater complexity at lower cost are the drivers behind large-scale integration. In order to sustain these driving forces, technologies must be developed that enable the continued increase in the number of devices on a chip, yet limit the chip size, to prevent interconnect delay from affecting chip performance. Potential solutions are:

- Three-dimensional integration
- On-chip or Off-chip optical/RF interconnects
- Novel system architectures

1.2 Three-Dimensional Integration

Three-dimensional integration to create multilayer Si ICs is a concept that can significantly improve deep-submicrometer interconnect performance, increase transistor packing density, and reduce chip area and power dissipation [5]. Also, 3-D ICs can be very effective tools for large-scale on-chip integration of different systems.

In the 3-D design architecture, an entire chip is divided into a number of blocks, and each block is placed on a layer of Si. The blocks are stacked on top of each other, with each layer of the stack possibly containing multiple interconnect levels. A high density of interconnections facilitate face-to-face stacking of multiple device levels, and through-wafer interconnects allow face-to-back or back-to-back stacking.
1.2.1 Interconnect Wire-length Reduction with 3-D Integration

Three-dimensional ICs are expected to reduce the semi-global and global wiring requirements significantly, therefore, allowing higher packing density in wiring-limited ICs and smaller interconnect delay [6]. Fig. 1-1 shows the projected wire-length distribution of 2-D and 3-D logic circuits. By mapping a 2-D IC in 3-D, the number and length of long wires can be reduced significantly at the expense of a higher number of short wires. The total and average wire-length also become shorter, leading to smaller wiring-limited chip area and higher system performance. The 3-D architecture offers extra flexibility in system design, placement, and routing. The availability of additional silicon layers in a 3-D chip gives extra flexibility to designers that can be exploited to minimize area, improve performance and power dissipation, or any combination of these [1].

![Log-log Plot]

**Figure 1-1.** The wire-length distribution in 2-D and 3-D implementation of logic circuits. Three-dimensional integration results in narrower wire-length distribution (Arifur Rahman, Ph.D 2001, MIT)

1.2.2 System-on-a-Chip Design

System-on-a-Chip (SoC) is a broad concept that refers to the integration of nearly all aspects of a system design on a single chip [7]. These chips are often mixed-signal and/or
mixed technology designs, including such diverse combinations as embedded DRAM, high-performance and low-power logic, analog, RF, etc. They can also involve technologies like MEMS, bioelectronics, and optical input-output (I/O) devices. 3-D chip design technology can be exploited to build SoCs by placing circuits with different voltage and performance requirements in different layers. Three-dimensional integration can reduce the wiring, thereby reducing the capacitance, power dissipation, and chip area and therefore improving chip performance. Additionally, digital and analog components in the mixed-signal systems can be placed on different Si layers thereby achieving better noise performance due to lower electromagnetic interference between such circuit blocks. From an integration point of view, mixed-technology assimilation could be made simpler and cost-effective by fabricating such technologies on separate substrates followed by physical bonding.

1.2.3 Technology Options for 3-D Integration

Presently, there are several possible fabrication technologies that can be used to realize multiple layers of devices separated by ILDs for 3-D circuit processing. The choice of a particular technology for fabricating 3-D circuits will depend on the requirements of the circuit system, since the circuit performance is strongly influenced by the electrical characteristics of the fabricated devices as well as on manufacturability and process compatibility with the relevant 2-D technology. The approaches to 3-D integration are as follows

- Thin film Technology
- Package-level Integration
- Processed Wafer Bonding

Silicon thin film technology lends several options for 3-D integration. A popular method of fabricating a second active Si layer on top of an existing substrate is to deposit polysilicon and fabricate thin-film transistors (TFT). To enhance the performance of such transistors, an intense laser or electron beam is used to induce recrystallization of the
polysilicon film [8] to reduce or even eliminate most of the grain boundaries. The beam recrystallization technique may not be practical for 3-D devices because of the high temperature involved during melting of the polysilicon and also due to difficulty in controlling the grain size variations [9]. However, high-performance TFTs fabricated using low-temperature processing have been demonstrated [10] that can be employed to fabricate advanced 3-D circuits.

*Silicon Epitaxial Growth* is another thin film technology applicable to 3-D integration. Additional Si layers are fabricated by etching a hole in a passivated wafer followed by epitaxial growth of single-crystal Si seeded from open window in the ILD. The silicon crystal grows vertically and then laterally to cover the ILD [11]. In principle, the devices fabricated on these epitaxial layers can be as good as those fabricated underneath on the seed wafer surface. However, the high temperatures (1000C) involved in this process cause significant degradation in the quality of devices on lower layers. Also, this technique cannot be used over metallization layers.

*Solid Phase Crystallization* (SPC) is an alternative to high-temperature epitaxial growth. This technique involves low-temperature deposition and crystallization of amorphous silicon on top of the lower active layer devices. The amorphous film can be randomly crystallized to form a polysilicon film [12]. Local crystallization can be induced using low-temperature processes (<600C) such as patterned seeding of Germanium [13]. Ge seeds implanted in narrow patterns made on amorphous-Si can be used to induce lateral crystallization and inhibit additional nucleation. CMOS transistors can be fabricated within these islands that are nearly single-crystal. Another approach based on the seeding technique employs Ni seeding to induce simultaneous lateral recrystallization and dopant activation after the fabrication of the entire transistor on an amorphous-Si layer. This technique known as the metal induced lateral crystallization (MILC) [14] offers even lower thermal budget (<500C) and can be employed to fabricate high-performance devices on upper active layers even with metallization layers below.

*Package-level 3-D integration* technology is a technique where bare dies or packaged chips are stacked vertically, and interconnections between them are formed at the chip periphery. Using package-level integration, dense memory modules can be fabricated
Area interconnections formed by through-wafer vias or solder balls in the case of face-to-face bonding can also be used to provide vertical interconnections between stacked multi-chip modules. Utilizing the area interconnection technology, vertical integration of ASICs and memory, signal processing circuits, and microprocessors have been implemented [16]. The drawback in package-level 3-D integration technology is the lower density of vertical interconnects compared to monolithic 3-D integration.

1.3 Processed Wafer Bonding

An attractive option for 3-D integration is to bond two fully processed wafers on which devices are fabricated on the surface, including multiple layers of interconnects, such that the wafers completely overlap [17]. Interchip vias are etched to electrically connect both wafers after metallization and prior to the bonding process at 400 °C. Low temperature (<450 °C) copper-copper or polyimide based wafer bonding can be used to bond two fully processed wafers for fabricating 3-D ICs [17,18]. In one approach to 3-D IC technology based on wafer bonding, after the fabrication of an individual device layer, a top wafer is attached to a handle wafer, and is thinned down from the backside. Then the back side of the top wafer is bonded to the front side of the bottom wafer. The handle wafer is released after the bonding process [17]. This bonding technique is a back-to-front bonding. This technique is very suited for further processing or the bonding of more pairs in this vertical fashion. However, to achieve the maximum efficiency in 3-D integration, a very high density of interconnections is necessary to minimize total wire length and hence, RC delay. Such a high via density can be achieved by front-to-front bonding wherein high-aspect ratio through-wafer vias provide the communication between pairs of device layers. Advantages of wafer bonding technology lie in the similar electrical properties of devices on all active levels and the independence of processing temperature since all chips can be fabricated separately and later bonded. Ideally, the processing steps required to bond two wafers can be repeated to bond as many wafers as desired. However, thermal issues, processing cost or complexity etc, may dictate the number of wafers that can be profitably integrated.
Using low-temperature wafer bonding technology, functional blocks that require different process technologies can be placed in different device layers to form 3-D SOC. A cross-sectional view of a 3-D IC formed by Cu-Cu wafer bonding is shown in Fig. 1-2. One of the limitations of wafer bonding technology is the lack of precision (best case is ± 2 μm) in aligning Cu or metallic bumps using IR alignment to form inter-device layer interconnections. Novel techniques based on non-optical methods are envisioned for sub-micron precision alignment. However, for applications where each chip is required to perform independent processing before communicating with its neighbor, this technology can prove attractive. Also, this limitation can be eliminated to a large extent by using bonding pads that can be sized for alignment, provided that the footprint area is sufficient.

![Diagram of 3-D IC with layers and bonding description](image)

**Figure 1-2.** Cross-section of a 3-D integrated circuit formed by face-to-back Cu-Cu wafer bonding

### 1.3.1 Technology Options for Vertical Interconnects

3-D technology can yield improved chip performance with increased utility of vertical interconnections. Vertical interconnects form the communication between the different device layers in a 3-D integrated circuit.
Direct wafer bonding techniques have demonstrated interlayer vertical interconnect schemes. One method is based on the optically adjusted bonding of a thinned top wafer to a bottom wafer with an organic adhesive layer of polyimide in between [18]. Interchip vias are etched through the ILD, the thinned top Si wafer and through the cured adhesive layer, with an approximate depth of 20μm prior to the bonding process. The interchip via made of chemical vapor deposited (CVD) TiN liner and the CVD-W provides a vertical interconnect between the uppermost metallization levels of both layers. The bonding between the two wafers is done using a flip-chip bonder with split beam optics at a temperature of 400C.

A second technique relies on the thermocompression bonding between metal pads in each wafer [17]. In this method, Cu-Ta pads on both wafers serve as electrical contacts between the interchip via on the top thinned Si wafer and the uppermost interconnects on the bottom Si wafer. The Cu-Ta pads can also function as small bond pads for wafer bonding. The Cu-Ta bilayer pads with a combined thickness of 700 nm are fused together by applying a compressive force at 400C. This technique offers the advantage of a metal-metal interface that will lower the interface thermal resistance between the two wafers and hence, provide better heat conduction while simultaneously serving as electrical contact.

Compared to non-monolithic approaches to 3-D integration, the density of inter-device layer interconnections in monolithic approach is 30x to 50x higher. The relative cost for integrating various modules or components monolithically is generally smaller compared to packaging alternatives [19]. The potential improvements in form factor, power dissipation, or I/O bandwidth by monolithic 3-D integration may reduce the system cost compared to 2-D or 3-D package level integration. Presently, Cu-Cu wafer bonding technique is being actively researched at MIT to demonstrate the feasibility of monolithic 3-D ICs.
1.4 3-D Integration: Challenges

1.4.1 Thermal Issues

Heat dissipation is a core issue in 3-D ICs [20]. Thermal effects are known to significantly impact interconnect/device reliability and performance in high-performance 2-D ICs [21]. The problem is expected to be exacerbated by the reduction in chip size, assuming the same power generated in a 2-D chip will now be generated in a smaller 3-D chip, resulting in a sharp increase in the power density.

Most of the heat energy generated in integrated circuits arises due to transistor switching. This heat is typically conducted through the silicon substrate to the package and then to the ambient by a heat sink. With multilayer device designs, devices in the upper layers will also generate a significant fraction of heat. Also, all the active layers will be insulated from each other by layers of dielectrics which typically have much lower thermal conductivity than Si. Hence, the heat dissipation issue can become even more acute for 3-D ICs and can cause degradation in device performance and a decrease in chip reliability due to increased junction leakage and electromigration failures.

Simulation results of power dissipation and thermal analysis for 2-D and 3-D implementation of microprocessors have shown that, for similar system performance, the amount of power dissipation in 3-D ICs is comparable to that of 2-D ICs [22]. However, if 3-D ICs operate at higher clock frequency compared to that of 2-D ICs, power dissipation could reach an unacceptable level. For reliable operations of devices and interconnects at a reasonable chip temperature, low-power circuit techniques will be integral to system design. At the same time, heat sinks with better cooling technology will be needed [1].

1.4.2 Electromagnetic Interactions

In 3-D ICs, additional coupling between the top layer metal of the first active layer and the devices on the second active layer is expected to be present. This needs to be addressed at the circuit design stage. For technologies with very small aspect ratio, the
change in interconnect capacitance due to the presence of an additional silicon layer could be significant [23]. Also, on-chip inductive effects arising due to increasing clock speeds, decreasing rise times, and increasing length of on-chip interconnects is a concern for overall performance [1]. For long global wires, inductance effects are more severe due to the lower resistance of these lines, and also due to the presence of significant mutual inductive coupling between wires, resulting from longer current return paths [1]. In 3-D ICs, the reduction of wire lengths will certainly help reduce inductance.

1.4.3 Reliability Issues

Three-dimensional integration introduces reliability issues, some of which are currently present in 2-D ICs but need to be addressed on a different level, and some of which are unique to vertical integration. Electromigration and joule heating are issues that come under the former category, while electrothermal and thermomechanical effects between various active layers form a part of the latter. Interconnect reliability concerns have grown significantly because of the phenomenal increase in the total number of wire segments on a chip due to higher wiring requirements for increased numbers of transistors per chip. A brief description of the reliability concerns for bonded 3D ICs is given below.

Electromigration is the transport of atoms of a conducting material due to momentum transfer from flowing electrons. The rate of electromigration is directly related to the current density in a segment of an interconnect tree in an integrated circuit. It has been shown that the reliability of a segment of an interconnect tree also depends on the current densities in the linked segments [24]. Electromigration effects are severe for modern IC interconnects because of the high current densities in the narrow segments. The flux of atoms causes compressive stress at the anode end that can cause the conducting metal to extrude. The compressive stress in Cu interconnects causes liner materials to crack or rupture leading to Cu diffusion through the ILD. Void formation is another failure mode in electromigration due to tensile stress at the cathode ends of segments.
Increased joule heating arising from higher power dissipation is another reliability concern for 3-D ICs. Today’s high performance microprocessors run at temperatures close to 100 C [25]. Such a high temperature causes the electromigration effects to be severe as the median time to failure due to electromigration decreases with increasing temperature [26]. Heat dissipation is a challenge in 3-D ICs due to the smaller chip area compared to 2-D ICs. Innovative circuit design and heat sink technologies are envisioned as solutions to the joule-heating problem.

Reliability of bonds in a wafer bonding technology is a concept that is unique to 3-D ICs. Heterogeneous integration of technologies using 3-D architecture drives the need to understand mechanical and thermal behavior of material interfaces prior to and during operation. In order to understand this behavior, quantitative knowledge about the bond strength and quality is essential. The interfaces in a vertically stacked circuit are subjected to intrinsic stresses during fabrication and thermal cycling during device operation. Such high stresses can cause failure of interfaces that leads to overall system failure. Therefore, it is necessary to develop models for bond reliability that can be used to predict the reliability of the circuit from the standpoint of mechanical integrity.

Recently, a framework for reliability analysis in 3-D ICs named ERNI-3D (Electromigration Reliability in Networked Interconnects) has been developed [27]. For completeness, a novel layout methodology (3DMagic) for designing 3-D ICs has also been developed. ERNI-3D is capable of using the circuits laid out in 3DMagic and applying reliability models for assessing electromigration and bond reliability, and the effects of increased joule heating. This initial version of ERNI-3D works with 3D circuits with two wafers or device-interconnect layers in the stack. However, the data structures and algorithms are generic enough to make it compatible with 3D circuits with more than two wafers, and to allow incorporation of reliability models such as bond reliability.
1.5 Quantitative Analysis of Bond Reliability for 3-D Integration

The preceding discussions have lead to the important conclusion that a quantitative analysis of the reliability of bonds is crucial for estimating the overall feasibility of three-dimensional integration with copper wafer bonding. The reliability of devices containing multi-layer thin film structures is strongly influenced by the adhesion properties of the many interfaces present. The concern for mechanical reliability exists in present day 2-D ICs containing millions of transistors on a microprocessor chip, where the interconnect layers are densely stacked to form the multi-layer interconnect structure. In such a structure, the interconnect lines and the vias are embedded in a matrix of the ILD. Due to the large difference in thermal expansion coefficient between the metal, barrier layer and the surrounding ILD, tensile stresses generated in the interconnect lines are large enough to make the interfaces vulnerable to fracture failure. Interface decohesion is only bound to be a much more potent problem when a switch is made from 2-D to 3-D ICs involving wafer bonding. In 3-D ICs fabricated using wafer bonding technology, not only are more interfaces present compared to 2-D ICs, but there also exists the crucial Cu-Cu bonded interface. Though work has been done towards measurement of adhesion properties of multi-layer thin film structures, the bond quality and reliability of Cu-Cu bonds for 3-D applications have not been studied in detail. This thesis aims to provide the first step towards characterization of copper wafer bonding for 3-D ICs. Using robust and reliable quantitative measurements, the strength of copper bonds is obtained and is used as a tool for optimizing the processing conditions to obtain uniform reliable bonds at low temperatures. During the course of the work, several properties of copper-copper bonds have been identified. The toughness of the bonds depends on several parameters that include the surface preparation prior to bonding, thickness of the metal stack that is bonded and also the material used as a barrier layer for Cu. This work also provides valuable information needed to further analyze copper wafer bonding and develop a reliability model for bond quality.
1.5.1 Measurement of Interface Adhesion

Experimental techniques capable of systematically characterizing interface fracture have been developed.

One fundamental quantity that characterizes an interface is the energy, $2\gamma$, required to separate a unit area of two bonded surfaces. This is often referred to as the thermodynamic work of adhesion ($W_A$) and is denoted as

$$2\gamma = (\gamma_1 + \gamma_2) - \gamma_{12},$$

(1)

where $\gamma_{12}$ is the energy of the interface, and $\gamma_1$ and $\gamma_2$ are the surface energies of the two materials, 1 and 2, on either side of the interface. The theoretical strength of the interface corresponds to the thermodynamic work of adhesion. Interfaces, however, do not generally fail in an ideal fashion and hence, one does not measure the theoretical strength. More typically, delamination occurs through crack growth by localized breaking of bonds in the highly stressed region at the tip of a propagating crack. This localization results in failure occurring at applied stresses much lower than the theoretical maximum.

A framework for analyzing crack growth has been established in the field of fracture mechanics. An important concept is that the change in the total mechanical energy of a system associated with the propagation of a crack provides the driving force for delamination. This driving force, $G$, which is also referred to as the strain energy release rate, is the energy available to separate a unit area of interface, and is given by

$$G = \frac{\partial}{\partial A} (W - U),$$

(2)

where $A$ is the crack area, $W$ is the work done by any external loads, and $U$ is the elastic strain energy stored in the system. The crack propagates, and delamination occurs if $G$ is larger than the energy required to separate a unit area of the interface, $\Gamma$. This quantity, $\Gamma$, is referred to as the toughness, or the fracture resistance, of the interface. Fracture toughness is measured experimentally by determining the load required to propagate a sharp crack, performing an elastic calculation to calculate the value of $G$ appropriate for the load and geometry, and equating the toughness of the interface to this value of the energy release rate. The fracture toughness, $\Gamma$, is ideally equal to the quantity $2\gamma$ defined
in equation (1) [28]. However, this equality is found experimentally only in very weak interfaces, such as when the interfacial bonding is provided by the capillary force of a liquid [29]. Generally, the surface energy represents only a small portion of the total energy consumed in separating an interface by a propagating crack. The bulk of the energy is dissipated by dislocation emission, flow, or other irreversible processes occurring in a process zone at the crack tip. This contribution from plastic dissipation is generally denoted by $W_{pl}$.

1.5.2 Application of Fracture Mechanics to Interface Adhesion

Delamination of a film from a substrate or a bonded interface can be expected to occur only if there is both a pre-existing flaw and a driving force for crack propagation. One might imagine that, in microelectronic devices, processes such as corrosion, localized plastic flow in high-stress regions, or contamination could introduce suitable flaws. In general, the driving force, $G$, depends on both the flaw size and film thickness. However, when the length of the interface crack is substantially larger than the film thickness, $G$ often exhibits a maximum value which is independent of the crack length and scales only with the film thickness.

Solutions for Delamination

The value of fracture toughness, $\Gamma$, is obtained by experimentally measuring the energy release rate, $G$. Since $G$ is equal to $\Gamma$ at the point of fracture, this experimental measurement gives the value of fracture toughness. The energy-release rate is related to the stress intensity factors, which are the components of a vector quantity that characterizes the crack-tip stress field in an elastic body. The stresses at a crack tip exhibit a square-root singularity, and the stress-intensity factors indicate the value of the stresses at a fixed distance from the crack tip. For the purposes of analyzing interface adhesion of bonded structures, two types of stresses are considered: normal stresses acting across the crack plane and in-plane shear stresses. The stress-intensity factors
associated with these stresses are designated the mode-I and mode-II components, $K_I$ and $K_{II}$ respectively. The energy-release rate is related to the stress-intensity factors by

$$ G = \frac{(1 - \nu^2)(K_I^2 + K_{II}^2)}{E}, $$

where $\nu$ and $E$ are the poisson’s ratio and elastic modulus of the bulk substrate, respectively.

**Mixed-mode Fracture**

In an isotropic material with no interfaces, a crack propagates along a path that locally minimizes the energy-release rate. This trajectory is one for which $K_{II}$ is essentially zero, also called a pure-tensile fracture mode. In contrast, a crack forced to grow along an interface is generally subject to some shear. Hence, failure is essentially one of a mixed-mode type. It is this effect that is frequently responsible for what is termed “cohesive” failure (when fracture occurs in the vicinity of the interface, but leaves the interface intact) rather than “adhesive failure” at the interface itself. Mode mixity is defined by a parameter $\psi$, which is given by

$$ \psi = \tan^{-1}(K_{II}/K_I). $$

$\psi$ is the phase angle associated with the normal to shear stress ratio ahead of the crack tip. For example, $\psi = 0^\circ$ represents a pure mode-I (opening) deformation, and $\psi = 90^\circ$ represents a pure mode-II (shear deformation) [Fig 1-3]. In the case of mixed-mode failure, both the fracture toughness and the interface crack growth mechanism are dependent on $\psi$ [30]. The criterion for crack extension can be written as

$$ G \geq \Gamma(\psi). $$
Figure 1-3. Schematic illustration of the dependence of $G$ on $\psi$. Different tests for the measurement of $G$ involve a wide range of $\psi$ values.

A fracture-mechanics based method to measure interface adhesion will necessarily

A fracture-mechanics-based method to measure interface adhesion will require a detailed knowledge of $\Gamma(\psi)$ for the interface of interest. Direct measurement of $\Gamma(\psi)$ relies on the premise that it is possible to experimentally determine the critical load just sufficient for incipient crack growth. By definition, at the critical load, the corresponding critical strain energy release rate, $G_c$, equals the interface fracture energy, i.e.,

$$G_c = \Gamma(\psi).$$

The critical strain energy release rate, $G_c$, is a function of both material properties such as the interface chemistry, adjacent microstructures and elastic-plastic constitutive behavior, and mechanical parameters such as the loading mode mixity near the crack tip. Interface morphology and the thickness of adjacent thin film layers have important effects on adhesion [31].

Various test methods have been devised for measurement of $G_c$. Indentation methods rely on the formation of a dilated plastic zone in the film to cause the film to blister [32]. Values of $G_c$ may be related to the indentation volume (or plastic zone size) and extent of debonding. The technique and its derivatives typically lead to qualitative results because of the assumptions made about complex deformation fields.

Another commonly used test method is the peel test [33] wherein a force is applied at the edge of a film to cause the peeling of the film from the substrate. In this technique, $G_c$
can be accurately related to the forces and moments transmitted to the thin film. A liability of the peel test is that it is difficult to separate the plastic bending in the thin film during debonding from the measured adhesion energy [34].

The blister test involves debonding the film by creating a cavity in the substrate below the film and causing the film to bulge by pressurizing the cavity [35]. The technique has proven successful for some thin films systems, but is often compromised by the inherently compliant loading system, chemical interactions between the debond and the pressurized environment, and the etching or machining procedures needed to produce the cavity.

The common limitation of all the above techniques, however, is that during debonding, residual stresses in the thin film relax and contribute to the debond driving force. The effects of such relaxation on the measured adhesion values can be large [36], and in some cases, it may not be possible to measure the residual film stress prior to debonding.

1.5.3 Four-Point Bend Test

For bonded interfaces embedded in bulk materials, crack growth can be well controlled by applying a load on the bulk material sandwiching the interface. The 4-point bend test is an adhesion testing technique which potentially overcomes some of the limitations associated with existing thin film tests. The specimen to be tested is a sandwich structure, illustrated in Fig. 1-4. The specimen is loaded between 4 loading points and an equal load is applied at all points as shown. As the bending moment increases with increasing load, a pre-crack initiates from the top surface (usually facilitated by a machined notch) and propagates vertically to the interface. If the interface is sufficiently weak, the crack deflects into the interface and propagates along it. This particular design has the advantage that the strain energy release rate for the interface crack is independent of the crack length, as long as the crack tip is not too close to the pre-crack or the loading points. This feature facilitates steady-state behavior and significantly reduces the difficulties involving crack length measurements. Applying beam theory, the strain energy release rate is related to measurable quantities by [37]:

26
\[ G = \frac{M^2(1 - v^2)(1/I_2 - 1/I_c)(1/F)}{2E}, \]

where \( M \) is the net bending moment per unit width and is equal to \( P l/2w \), where \( P \) is the plateau load, \( l \) is the distance between the inner and outer loading points and \( w \) is the specimen width. \( v \) is the Poisson’s ratio of the bulk substrate, \( E \) is the elastic modulus of the bulk substrate, and \( I_2, I_c \) are the moments of inertia per unit cross-section area for the lower layer and the composite beam, respectively, and \( F \) is the area fraction of the copper bonds in the specimen.

**Figure 1-4.** Four-Point Bend test specimen

An advantage of this 4-point bend technique is that during debonding, stress relaxation of the film is constrained and so does not contribute to the debond driving force. A small contribution to the measured value of \( G \) will arise from elastic curvature of the wafers containing the thin film after debonding. It has been shown that this contribution to the debond driving energy is negligible [31]. However, for the material system under test, the contribution from stress relaxation has to be considered and the magnitude taken into account. Another advantage of the sandwiched sample configuration is that fracture-mechanics-based tests to characterize the subcritical crack growth rate behavior associated with environmentally-assisted or fatigue processes are easily facilitated. Another factor which has to be taken into account during the 4-point bend test is the
energy dissipation by plastic deformation. Plastic deformation is certain to occur in the copper stack surrounding the bonded interface [38] and has to be considered while making predictions about the quality of bonding.

In this work, the 4-point bending technique has been extended to measure interface adhesion in bonded copper structures for 3-D ICs applications. The copper/barrier multilayers present on two wafers are bonded together using thermocompression bonding. A pre-machined notch serves as the stress concentration point for the origin of the crack. The crack propagates into the weak interface in the bonded stack and the steady state value of the strain energy release rate gives the fracture toughness of the interface. Fracture toughness values are used to optimize the processing conditions to obtain high quality bonds at low temperatures. The effects of both processing and specimen configuration on the bond quality are analyzed. The preliminary results obtained serve as the foundation for building a bond reliability model for 3-D integration with copper wafer bonding.
Chapter 2

Experiments

2.1 Fabrication

Appendix A shows a process flow for fabricating monolithic 3-D ICs based on wafer bonding [17]. The fabrication process consists of making the device layer on the top wafer followed by mechanical grind-back and chemical etching for via filling. To maintain mechanical integrity during the grind-back process, the wafer is bonded to a handle wafer. The processed top wafer is bonded to the bottom wafer which has another device level. A typical Copper wafer bonding process is a thermo-compression process at 400° C for 30 minutes, followed by a 30 minute anneal at 400° C.

The aim of work was to fabricate bonded test structures representative of the configuration seen in a 3-D IC. The results from mechanical testing of these structures would give information on the quality of bonding for 3-D IC applications.

Various configurations of copper bonding are of interest.

1. Blanket copper films.
2. Patterned copper/barrier lines.
3. Patterned copper/barrier pads.

100mm Si (100) wafers were used as substrates for all thin film deposition and bonding studies. The thickness of the wafers ranged from 475 \( \mu \text{m} \) (for double-side polished wafers) to 525 \( \mu \text{m} \) (for single-side polished wafers). Each bonded wafer pair consists of one single-side polished wafer and one double-side polished wafer. The necessity for the latter arises from the alignment configuration in the EV Bonder tool used for wafer bonding. The tool provides front-to-back optical alignment capability and
therefore, one of the wafers (the double-side polished one) must have alignment marks on both front and back sides.

The fabrication process flow chart is shown in Figs 2-1 and 2-2. The first step in the fabrication process was alignment mark registration on the front side of single-side polished (SSP) wafers and on both sides of double-side polished (DSP) wafers. Next, silicon dioxide films of 300nm thickness were thermally grown on the SSP wafers, after subjecting the wafers to a standard RCA clean prior to diffusion. The oxidation temperature was 1100°C. 100nm-thick silicon nitride films were deposited on the DSP wafers using Low Pressure Chemical Wafer Deposition (LPCVD), involving the decomposition of silane gas and ammonia. A 500μm-wide trench was then patterned at the center of the DSP wafers using a standard positive photoresist. After etching of the nitride in the exposed region using a CF₄ plasma (using resist as the mask), Si was etched to a depth of 50μm using a KOH wet etch, the silicon nitride serving as the hard mask. The anisotropic etching characteristics of KOH on Si yield a sloped-walled grooved trench at the center of the DSP wafers. The nitride hard mask was then stripped off by treating the wafers with hot phosphoric acid (175°C). The trench was made to facilitate machining of a notch for 4-point testing of the bonded wafer-pair. The DSP wafers were then subjected to an RCA clean prior to thermal oxidation at 1100°C to obtain 300 nm thick oxide films.

The next step in the fabrication process was metal deposition. The copper deposition step was preceded by the deposition of a barrier layer to prevent copper diffusion into silicon dioxide. Also, the wafers are subjected to high enough temperatures during bonding (300-400°C) which could cause copper diffusion in the absence of a barrier layer. Tantalum was chosen both as a diffusion barrier and an adhesion promotion layer for copper metallization.
Figure 2-1. The process flow for fabrication of four-point bend test structures- (a) (100) silicon DSP wafer; (b) 1000Å-thick LPCVD silicon nitride; (c) patterned photoresist used as etch mask for silicon nitride patterning; (d) silicon nitride dry etched; (e) 50μm deep anisotropic silicon etch using KOH; (f) silicon nitride stripped using phosphoric acid; (g) cross-sectional view rotated 90° shows 3000Å-thick thermal oxide grown; (h) image-reversal photoresist patterning and 500Å/3000Å Ta/Cu deposition using e-beam evaporation; (i)-(l): steps (g) and (h) performed on (100) silicon SSP wafer.
**Figure 2-2.** Fabrication process flow, continued. (a) and (b): Lift-off done on wafers 2-1 (h) and (l); (c) thermocompression bonding of the patterned wafers; (d) cross-sectional view (90° rotation) shows bonded wafer-pair with trench in bottom (DSP) wafer made by diamond saw.

The first test structures were continuous Cu/Ta films on the processed SSP and DSP wafers. The metals were deposited using physical vapor deposition (PVD) in an evaporative deposition unit. Ta was deposited first, followed by Cu without breaking vacuum. The chamber pressures were around 4E-7 torr for Ta deposition and 7E-7 torr for Cu deposition. These wafers were then bonded together in an Electronic Visions (EV) bonder.

Patterned copper lines were the next set of test structures fabricated and tested. The lift-off technique was used for patterning. The other option for patterning, namely etching, was also tried. However, etching required a combination of HCl-based wet etching for Cu and BCl₃-based dry etching for Ta. The Cu etching rate was too high to control lateral etching. Also, plasma-based etching for Ta was not entirely selective to the oxide layer underneath. Plasma also hardened the photoresist and this affected post-etching resist removal. Hence, lift-off was preferred to etching, for metallization. The
wafers were coated with image reversal photoresist. After exposure using a light-field mask, the patterned areas were developed. Ta and Cu were deposited on these patterned wafers and then the wafers were soaked in acetone for a few hours. Ultrasonic agitation of these wafers in acetone was done to lift-off the resist (along with the metal film above it) leaving behind lines of metallization on the wafers. The wafers were then cleaned in methanol and rinsed with water and dried.

The next step in the process was wafer bonding. The processed wafers were subjected to a prebonding clean in 1:1 HCl:H2O for one minute just prior to bonding. The wafers were then rinsed with deionized (DI) water and spin-dried. This cleaning step was done to dissolve surface copper oxide. A UV-ozone clean to remove organic contaminants was also tried, but this step caused non-uniform oxide formation on the copper surface, which was detrimental to the bonding process. However, even after cleaning with HCl, native oxide formation could not be avoided since the wafers remain in the cleanroom atmosphere for some time before being transferred to the bonding chamber.

The first step in the bonding process was the alignment of the two wafers. Though precision (micron level) alignment is not a necessity for bonding wafers with continuous copper films, it was a crucial step for bonding wafers with patterned metallization levels. The alignment tool (Electronic Vision EV 450 Aligner) made use of an optical alignment method. The top wafer (SSP) was first placed on the unit facedown and the alignment marks were recorded on the screen in the form of computer-generated cross-hairs. The bottom wafer (DSP) was then placed face-up and adjusted to match its alignment marks to the cross-hairs. The wafers were viewed from the bottom and hence the need for backside alignment marks on the second wafer. The alignment accuracy obtained using this method was ± 3μm [17]. After alignment, the wafers were clamped together in a bond chuck, but separated by three 30μm-thick metal flaps. The bond chuck was then transferred to a bonding chamber which had provisions for heating, and purging with gas. Nitrogen and forming gas (95 % Ar, 5% H2) were the purge gases experimented with. The bonding recipe was altered for various runs to optimize the process. The basic structure of the recipe involved repeated pump-purge cycles to clean the chamber.
followed by pumping down the chamber to the lowest possible pressure (1E-3 torr). The wafers were then brought into contact and heated to the predetermined bonding temperature. The wafers were subjected to the constant maximum temperature for 30 minutes under an applied load of 0.4 MPa. Finally, the wafers were cooled down to room temperature in the chamber. Variations in the forming gas purge portion of the bonding recipe using were carried out and the results tabulated. The final step in the processing was a 30-minute anneal in a nitrogen ambient at the bonding temperature.

The bonded wafer pair was inspected for large macro-voids using IR imaging. This inspection process would give a qualitative estimate of the bond quality by checking for any conspicuous defects. A typical IR image of a bonded wafer pair is shown in Fig. 2-3 (a).

The bonded wafers were next diced into strips of 8mm width using a diamond saw. Prior to this dicing action, a notch was made for the 4-point bending test by dicing through the thickness of the DSP wafer till the cut met the KOH-etched trench. Each bonded wafer-pair yielded seven samples for the 4-point bending test.

![Test Specimen](image)

**Figure 2-3.** (a) Infra-red camera image of bonded wafer; each rectangular strip is a four-point test specimen, and contains a set of parallel metallization lines. (b) Four-Point test specimens were diced from the bonded wafer; rectangle in (a) shows single specimen.
2.2 Mechanical Testing

Four-point bending tests were carried out in an Instron Model 8500 Plus Dynamic Testing System. Prior to testing, the jig used for holding the specimen was aligned. The alignment process involved adjustment of the vertical positions of the loading pins to make sure the sample could rest in-plane in its slot, to eliminate any asymmetric bending moment effects. The bending test relies on the principle of constant bending moment between the inner loading pins for a given load, and the steady state strain energy release rate is proportional to the square of the moment, M. Any asymmetry in the moment would result in asymmetric loading of the sample and could, therefore lead to erroneous fracture toughness values. The calibration of the jig was done using a novel strain gage structure attached to a 8mm strip of a dummy bonded wafer. The jig was designed by Turner et al [42]. The strains on the 2 ends of the specimen were noted and were equalized by adjusting the heights of the loading pins.

After the calibration process, the dummy specimen was removed and bonded copper specimens were tested. The specimen was observed using an optical telescope for crack initiation and propagation events. The load was measured by a load cell and the displacement was incremented using a hydraulic actuator. The outer loading points were spaced 40mm apart and the inner loading points were 10mm from the outer points. All tests were displacement controlled and were done at a constant displacement rate of 0.12mm/min. A computer was used to record load, displacement and time simultaneously during a test. The actuator was comprised of a built-in LVDT for the measurement and control of actuator piston during the test. The tests were conducted at room temperature.

The load-displacement behavior from the tests was recorded and then analyzed to calculate peak load, and hence, the fracture toughness values.
Chapter 3

Results and Discussion

3.1 Testing of Bonded Continuous Films

The first tests were performed on bonded continuous copper film structures. Obtaining data from these high strength bonds was for the most part unsuccessful. Rather than delaminating along the interface, the crack would begin to propagate along the interface and quickly deflect into the unnotched bulk silicon layer. The crack, therefore, deflected from the interface to follow a mode I path and subsequently lead to fracture of the upper silicon beam. Hence, useful bond toughness could not be obtained. This result could be attributed to the deflection of the crack into the brittle stack of Ta/Silicon dioxide/Si which has a considerably lower mode-I fracture toughness compared to the interface toughness of the ductile bonded copper stack [39].

3.2 Testing of Bonded Cu/Ta Lines

The next set of structures tested were bonded patterned copper lines. The global interface toughness of these structures is lesser than that of bonded continuous films since the bonded area fraction is considerably lesser. For these structures, delamination and crack propagation along the interface were routinely observed. As expected, crack propagation would begin at a critical load and then propagate at a constant load until it reached the inner loading points. Fig. 3-1 shows a typical force-displacement curve that demonstrates this expected behavior. The critical load that is required for the calculation of the bond toughness is the load during steady-state crack growth, which corresponds to the plateau in the force-displacement curve. The area fraction of the bonded interface is incorporated
into the calculation of fracture toughness (Equation 5) and hence, the resultant interface adhesion value is given in terms of energy per unit area of bonded interface.

The value of interface fracture toughness was calculated using equation (5). By expanding the moments of inertia (Equation 5) in terms of the specimen dimensions, fracture toughness is given by

\[ G = \frac{3P^2l^2(1-v^2)}{2w^2EF} \left\{ \frac{1}{h_1^3} - \frac{1}{(h_1 + h_2)^3} \right\} , \]  

(6)

![Figure 3-1. Typical Load-Displacement behavior from Four-point test. (a) elastic loading of bulk material. (b) plateau load-steady state crack propagation. (c) unloading.](image)

where \( h_1 \) is the thickness of the top wafer, and \( h_2 \) is the thickness of the bottom wafer.

The expression for \( G \) is therefore given in terms of specimen dimensions (\( l, w, h_1, h_2 \)), material properties (\( v, E \)) and the peak load \( P \). Since the specimen dimensions are easily measurable and the material properties known, \( G \) could be readily calculated. The results from the patterned copper specimens served as the launching pad for testing various processing conditions and modifications. The fracture toughness values from the different configurations were compared and optimum conditions determined.
3.2.1 Effect of Ambient on Bond Quality

The effect of the bonding chamber ambient on the final bond quality was studied. The purge gases considered were Nitrogen and Forming gas (95%Ar-5% Hydrogen). The main concern during copper bonding is the surface oxidation of copper. Copper forms a native oxide at room temperature [40] and the issue of oxide removal has to be addressed to ensure clean copper-copper bonds. This was the motivation behind use of a forming gas ambient since it is known that native copper oxide could be reduced to copper metal using H₂ gas at high temperatures [41]. However, utilization of reducing properties of forming gas at high temperatures (400°C) demanded a high vacuum (1E-6 to 1E-8 torr) ambient. The EV bonder was designed to pump the chamber down to a minimum pressure of 1E-3 torr, and at this pressure, surface reoxidation of copper could not be avoided. Hence, the unavailability of high vacuum system was a serious limitation.

The first bonding recipe tried out was as follows:
1. Pump-Purge cycles to displace existing air, end with pump to 1E-3 torr.
2. Wafers brought into contact at room temperature.
3. Heated to high temperature.
4. Break vacuum at high temperature, pump with forming gas for 10 minutes, and vacuum back.
5. Apply maximum force (0.4 MPa), maintain at high temperature for 30 minutes and cool down to room temperature.

<table>
<thead>
<tr>
<th></th>
<th>( G_{AVG} , (J/m^2) ) – Run 1</th>
<th>( G_{AVG} , (J/m^2) ) – Run 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nitrogen Purge</td>
<td>6.8 (( \sigma = 2 ))</td>
<td>8.7 (( \sigma = 2.1 ))</td>
</tr>
<tr>
<td>Forming Gas Purge</td>
<td>7.3 (( \sigma = 1.1 ))</td>
<td>11 (( \sigma = 0.5 ))</td>
</tr>
</tbody>
</table>

Table 3-1. Fracture Toughness values for samples bonded under different ambient
The results of this run are tabulated in Table 3-1. The comparison between Nitrogen purge and Forming gas purge is shown. The forming gas run not only gave higher fracture toughness values but also gave more uniformity in bond strength, as seen from the lower standard deviation values. This result underlines the importance of copper oxide removal for bonding. However, most effective usage of forming gas for copper oxide reduction could be realized only if the chamber had ultra-high vacuum [41]. This condition could not be realized with the bonder configuration available. Analysis of fractured surfaces of the two runs showed non-uniform crack paths for the nitrogen-purge-bonded wafers and uniform failure modes for the forming-gas-purge bonded wafers.

The average fracture toughness value for the bonded copper lines was 10 J/m². Previously reported values for continuous copper-copper bonds [31] show similar values albeit for more rigorous bonding conditions. However, no previously reported value exists for patterned copper lines. The toughness value has been divided by the area fraction bonded to obtain bond strength per unit bonded area. This extrapolation was found to be valid for Si-Si bonds, which have no plasticity [42]. However, there is significant plastic dissipation in the ductile copper stack [38] and the extrapolation from patterned lines to continuous films may have to be determined experimentally. The contribution of the work of adhesion to the final toughness value is more or less constant. However, the contribution of the plastic dissipation energy changes depending on the thickness of the copper stack [38].

In an attempt to try to make effective use of forming gas for surface oxide removal, different recipes were tried out. One approach pursued was bonding in a forming gas ambient. In this recipe for bonding, the wafers were heated to 400°C with simultaneous forming gas purge. The gas was purged for 10 minutes at the maximum temperature and the wafers were brought into contact at maximum force (0.4MPa). They were allowed to be in contact for 30 minutes and then cooled down to room temperature. However, this recipe yielded very poor bonds because a large fraction of the bonded area was filled with
trapped gas. This result was seen using the IR camera image of the bonded wafers. These wafers even failed the qualitative razor-blade test wherein a thin blade was slid between the bonded wafers to prize them open. To overcome the problem of gas entrapment, a small deviation of this approach was tried. After the wafers were heated in forming gas, the chamber was pumped down to minimum pressure (1E-3 torr) and then the wafers were brought into contact. The pump down was done to ensure that the space between the wafers was free of gas bubbles. However, the poor vacuum meant that the surface of copper reoxidized, and hence, the bond was not of the quality desired. The mechanical tests of these wafers yielded similar or lower toughness values compared to the samples brought into contact at room temperature. Hence, it was concluded that, given the system limitations of poor vacuum, the best recipe for bonding was to bring wafers into contact at room temperature though this meant that the room temperature native oxide could not be removed.

3.2.2 Effect of Temperature on Bond Quality

With the introduction of Cu/Low-k dielectric technology to reduce RC delay in ICs [43], it is foreseen that there will exist a limit on the maximum processing temperature. The conventional dielectric material, namely silicon dioxide, can withstand temperatures well in excess of 400\(^\circ\) C. However, polymer-based low-dielectric-constant materials are known to be unstable at 400\(^\circ\) C [44]. Hence, there is a motivation for limiting the processing temperature within the stability range of the dielectric material. Though all processing was done with silicon dioxide as the dielectric material, low temperature bonding was explored keeping in mind the future of 3-D ICs wherein Cu and low-k dielectric technology may be used.
<table>
<thead>
<tr>
<th></th>
<th>200°C</th>
<th>250°C</th>
<th>300°C</th>
<th>400°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Forming gas purge</td>
<td>0.77</td>
<td>0.81</td>
<td>2.8</td>
<td>9.1</td>
</tr>
<tr>
<td>Nitrogen purge</td>
<td></td>
<td></td>
<td>1.7</td>
<td>7.5</td>
</tr>
</tbody>
</table>

*Table 3-2.* Fracture Toughness values (J/m²) for samples bonded at different temperatures.

To study the effect of temperature on bond quality, wafers patterned with copper lines were bonded at temperatures ranging from 200°C to 400°C. Four-point bending tests were performed and fracture toughness values tabulated as shown in Table 3-2. The results show a trend of increasing bond strength with increasing bonding temperature. Since the bonding was a thermocompression process, this trend was expected. The higher toughness values at higher temperatures may be attributed to the increased rate of diffusion of copper atoms across the interface which would have caused an increase in the chemical bond strength (work of adhesion). Future tests have to be performed to analyze the reliability of bonds at low temperature.

### 3.2.3 Effect of Pre-Bonding Clean Step on Bond Quality

Two different cleaning steps were tried to determine their effect on the bond strength. A standard solvent clean followed by a DI water rinse and spin dry was done prior to these cleaning steps. The first cleaning procedure was a one-minute dip in 1:1 Dil. HCl followed by a DI water rinse and spin dry. The other cleaning procedure involved use of a hydrogen-plasma bombardment of the wafer surface for 80 seconds [45]. Both methods were aimed at reducing surface copper oxide.
<table>
<thead>
<tr>
<th></th>
<th>300° C</th>
<th>400° C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dil. HCl Clean</td>
<td>2.9</td>
<td>9.1</td>
</tr>
<tr>
<td>N₂-H₂ Plasma Clean</td>
<td>2.9</td>
<td>5.7</td>
</tr>
</tbody>
</table>

**Table 3-3.** Fracture Toughness values (J/m²) for samples bonded with different pre-bonding clean steps

The results of the mechanical tests are tabulated in Table 3-3. The fracture toughness values are similar for the two steps and indicate that one cleaning step does not hold an advantage over the other in terms of surface oxide reduction. This result also suggests that native oxide removal in the bonding chamber just prior to bringing the wafers into contact is the critical step. However, it must be noted that the use of a prebonding clean step resulted in much higher toughness values than that observed in bonds created without any prebonding clean.

### 3.2.4 Effect of Copper Film Thickness on Bond Quality

It has been shown earlier that the thickness of the metal stack influences the fracture toughness value. The toughness increases for thicker stacks owing to the greater volume of metal available for plastic dissipation [38]. This result has been verified for both Cu [38] and Au film stacks [46]. The effect of the thickness of the Cu stack on the bond strength was also studied here.

Three different Cu stack (combining both wafers) thickness were analyzed. They were 0.1μm, 0.6μm, and 1.2μm. The results from the four-point bend tests of these specimens are tabulated in Table 3-4.
<table>
<thead>
<tr>
<th>Cu Stack Thickness (μm)</th>
<th>G (J/m²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1</td>
<td>8.5</td>
</tr>
<tr>
<td>0.6</td>
<td>9.1</td>
</tr>
<tr>
<td>1.2</td>
<td>No Delamination (for bonds created at 300⁰C and above)</td>
</tr>
</tbody>
</table>

**Table 3-4. Variation of Fracture Toughness with Cu Stack thickness**

The results show very little variation in fracture toughness values for Cu stacks of thickness below 0.6μm. However, for thicker Cu films, it was not possible to measure useful toughness value from the four-point test. This was a drawback similar to that encountered in the tests with continuous films. Due to a large amount of plastic dissipation in thicker films [38], the toughness of the interface increased. The crack propagated in a mode I path through the silicon layer, and hence, interface toughness could not be measured. The load-displacement curve for this type of behavior shows the linear portion corresponding to elastic loading of Si followed by an abrupt dip in load to zero, corresponding to mode I failure (Fig. 3-2). The constant load plateau behavior, indicative of mixed-mode steady state crack propagation, was absent.

Mode I crack propagation behavior was observed in bonds created between thicker copper films at temperatures above 300⁰C. This result shows that bonds created at low temperatures (300⁰C) using thicker copper films exhibit high fracture toughness values. This result therefore, provides an opportunity to optimize the copper film thickness to obtain strong bonds at low temperatures.
Figure 3-2. Four-point test result for thick (0.12μm) Cu stack. The initial elastic loading is seen followed by abrupt dip in load due to Mode I Crack Propagation.

This result could to be attributed to the change in the relative magnitudes of the interface fracture toughness and the mode I toughness value of the brittle stack surrounding the interface. For thicker metal stacks, the plastic dissipation increases and hence, interface fracture toughness increases. Therefore, the ratio of the interface toughness to the mode I fracture toughness of brittle stack increases. This causes a condition where the crack propagation has a preference towards a mode I path instead of interfacial delamination [47].

This result also underlines the fact that the testing method and the chosen specimen configuration limit the measurement of fracture toughness values for very strong bonds. Clearly, the higher plastic dissipation in tougher bonds contributed to this limitation. Also, the toughness of the surrounding Ta/Silicon dioxide/Si stack influenced this result. If the mode I toughness of the stack could be reduced, then crack propagation along the interface could be expected. Also, the chosen specimen configuration may have an effect on the maximum measurable fracture toughness values using four-point bend tests. The inherent limitations of the testing method for high strength bonds have also been discussed elsewhere [42].
3.3 Analysis of Fractured Surfaces

Two failure modes were predominantly found in the thin-film stacks tested. The weak interfaces were the Ta/Silicon dioxide interface and the copper-copper bonded layer. SEM micrographs of the two interfaces are shown in Figs. 3-3 (a) and (b). The Ta/Silicon dioxide interface shows smooth brittle failure. The copper-copper fracture surface shows ductile failure as identified by the dimple formations. This suggests homogeneous copper bonding. A profilometer scan of the fractured surfaces showed non-equal thickness of the delaminated thin films confirming that fracture occurred through the copper stack and not exactly at the interface.

The fracture analyses also lead to an important observation on the nature of the Ta/Silicon dioxide interface. Since the patterning of metal was done using a lift-off process, there was a concern about traces of photoresist left undeveloped on the oxide surface, which could potentially weaken the Ta/Silicon dioxide interface. The traces of resist could not be viewed using a microscope. A cleaning step was performed wherein the resist patterned wafer was subjected to a quick ashing step using an oxygen plasma. The metal was deposited after the cleaning step. This cleaning step, also known as resist descum, was found to have a significant impact. The mode of fracture changed from a mixture of Ta/Silicon dioxide and Cu-Cu to one of predominantly Cu-Cu. Hence, it was concluded that resist residue caused weakening of the Ta/silicon dioxide interface, which was otherwise inherently stronger than the Cu-Cu bond layer. This result also clearly showed the limitation of the chamber vacuum, which precluded effective copper oxide removal and cleaner Cu surfaces for bonding. Inefficient copper oxide removal could be the main reason for Cu-Cu bonds being weaker than the Ta/silicon dioxide interface.
Figure 3.3 (a) Cu fracture surface: Ductile Failure. (b) La 80 fracture surface showing Brittle Failure.
Chapter 4

Summary and Future Work

4.1 Summary

Characterization of copper wafer bonding and a quantitative analysis of bond quality are crucial to the successful implementation of 3D integration using the interconnect-based wafer bonding approach. In this work, a fracture toughness-based approach was used to evaluate bond strengths of patterned Cu lines bonded to each other using thermocompression bonding. The four-point bend test was used for interface adhesion measurements. Results from mechanical tests show reproducible fracture toughness values for copper bonds created at 300°C to 400°C.

Various processing parameters were used to arrive at optimum bonding conditions. It was found that a forming gas purge in the bond chamber, prior to bonding, yielded higher and more uniform fracture toughness values compared to a nitrogen gas purge. However, it was not possible to effectively use forming gas to remove surface copper oxide at high temperatures owing to poor vacuum conditions in the chamber. The average fracture toughness value for copper bonds created at 400°C was found to be 10J/m²

SEM analyses of the fractured surfaces show a ductile fracture mode for Cu-Cu cohesive failure and a brittle fracture mode of Ta/Silicon dioxide adhesive failure. An oxygen plasma ashing of the silicon dioxide surface prior to metal deposition ensured clean Ta/silicon dioxide interface (devoid of resist contamination) and hence, adhesive failure mode was less common.

Bond strength was found to increase with the bonding temperature. However, relatively high and uniform fracture toughness values were obtained for bonds at 300°C, indicating scope for low temperature wafer bonding. Fracture toughness of Cu-Cu bonds
was also found to increase with increasing thickness of the copper stack. Greater plasticity in thicker stacks caused higher energy dissipation and hence, stronger bonds. Mode-I failure observed in thicker bonded stacks indicates that bonds created at low temperatures (300°C) using thicker copper films exhibit high fracture toughness values. This result therefore, provides an opportunity to optimize the copper film thickness to obtain strong bonds at low temperatures. The test method had limitations for measuring high toughness bonds. Mode I failure was more likely in high toughness bonds and hence, useful interface adhesion values could not be measured. The same limitation was seen in the case of bonded continuous copper films.

4.2 Future Work

Quantitative characterization and optimization of copper wafer bonding are fundamental results which could be the starting points for further studies on bond quality. Testing of bonded parallel lines could be followed by testing of specimens with lines bonded perpendicular to each other on the two wafers. This would yield information on configurations with high-density small-area bonds. Wafer bonded 3D integrated circuits are envisioned to contain high-density bond pads to serve as electrical interconnections and for mechanical integrity. Testing these copper pad-structures would be crucial to the evaluation of feasibility of vertical integration.

Reliability assessment is an important issue that has to be addressed for any new technology. Reproducible bond strength values were obtained at room temperature laboratory conditions. The component in service would be exposed to thermal cycles and possibly stress-corrosion. Hence, there is a need to evaluate performance of the components under service conditions. Accelerated thermo-mechanical tests will provide useful information on the lifetime of components and hence, yield reliability estimates. Thus, reliability assessment methods and models should be developed to complete the picture of wafer bonding characterization.
Appendix A

Fabrication Process Flow of 3-D ICs Based on Wafer Bonding

In this section, the process flow for fabricating 3-D ICs based on wafer bonding will be presented [17]. The necessary fabrication steps are shown in Fig. A-1 and Fig. A-2 and they include:

1. Fabrication of bulk Si wafers which will be used as the bottom most stratum and patterning of Cu bumps for wafer bonding. Cu is deposited by e-beam evaporation.
2. Fabrication of SOI wafers which will be used as upper strata. Deposition of Cu layer, and patterning of Cu bumps.
3. Attachment of the SOI wafer with a handle wafer using a sacrificial layer. Cu is used to bond the handle wafer and a metal which could be selectively etched off is used as the sacrificial layer.
4. Mechanical grind back and chemical etching (using KOH) of the back side of SOI wafers.
5. Via opening through the thin Si layers.
6. Via filling.
7. Deposition of Cu film and patterning of Cu bumps for wafer bonding.
Figure A-1: The process flow for fabricating 3-D ICs

8. IR alignment of bulk Si and SOI wafer and wafer bonding.
9. Handle wafer release by dissolving the sacrificial layer. After releasing the handle wafer, another SOI wafer can be integrated following steps 1-9.
Figure A-2: The process flow for fabricating 3-D ICs
Bibliography


46. C. H. Tsau. private communication.
