Technology Strategy and Business Development at a Semiconductor Equipment Company: A Process Definition and Case Study of a New Technology

by

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Bachelor of Science in Mechanical Engineering, Northwestern University, 1998

Submitted to the Sloan School of Management and the Department of Mechanical Engineering in partial fulfillment of the requirements for the degrees of

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ABSTRACT

The technology strategy literature is growing quickly, both in the volume of titles and the number of pages. It is increasingly difficult for senior management, strategists and researchers to keep abreast of what is written in the technology strategy field. In addition, technology strategy thought has yet to pervasively saturate these types of key employees, let alone employees at lower levels. This is largely because disruptive technologies and significant changes made in sustaining technologies, by nature, occur infrequently when compared to an industry's clockspeed[i].

This thesis opens with a basic review of key technology strategy literature, including past efforts at process definition, in an effort to make it more accessible to more people and for internal use within the thesis body. The thesis then defines a more detailed process model for making technology strategy evaluations and applies the process to a specific issue facing a specific semiconductor equipment manufacturing company.

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The author wishes to acknowledge God, the Leaders for Manufacturing Program, fellow students and co-workers for the support of this work.

Biographical Note

The author attended Northwestern University from 1993-1998, earning a Bachelor of Science in Mechanical Engineering and 'minoring' in art theory. After school, he worked for the tooling department of a Chicago-based custom aerospace control system hardware company for two years. In the summer of 2000, he entered MIT's Leaders for Manufacturing program and will earn a Masters of Science in Mechanical Engineering and in Business Administration at the 2002 graduation. In August of 2002, he will begin Discipleship Training School with the Youth With A Mission organization and will be working in one of several asian countries until January of 2003. After this period, he plans to return to a more traditional management position.

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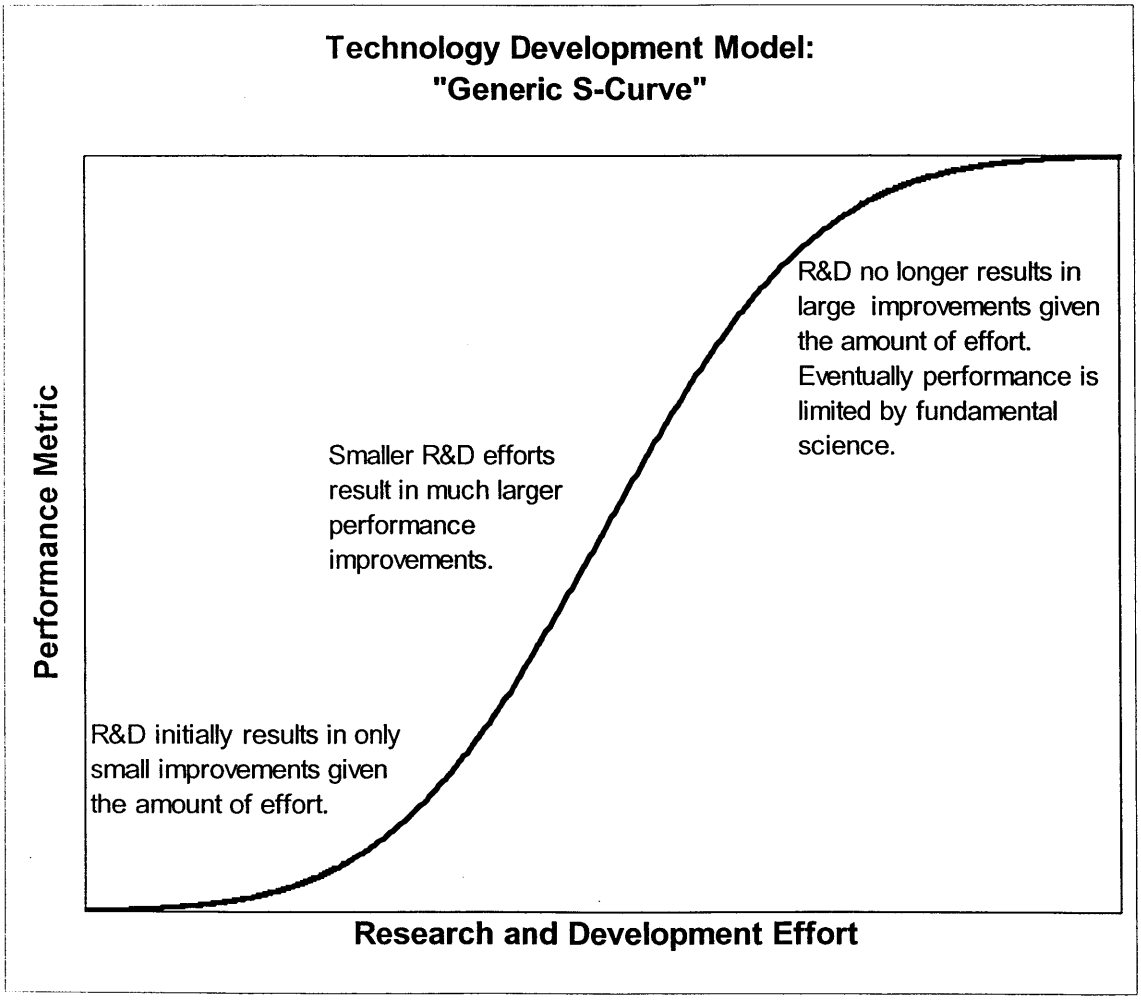
II. TECHNOLOGY STRATEGY LITERATURE REVIEW

Technology strategy consists of an intricate interaction between technology development' and 'market development'. Although hard to separate, these two areas can be treated separately at first and their interactions can be discussed together then second.

A. Technology Development

The first key technology strategy concept is the S-curve. The S-curve is simply a graph depicting research and development effort on the X-Axis and a performance metric on the Y-Axis. It predicts that most technologies, when they are first discovered and researched, do not show significant performance gain for the amount of scientific effort expended on them. Eventually, the work and science builds to a point where the technology becomes better and better for much less effort expenditure. In the end, however, technologies run up against fundamental scientific limits and only marginal performance gains are created by further effort expenditure. Below is a graph depicting this curve:

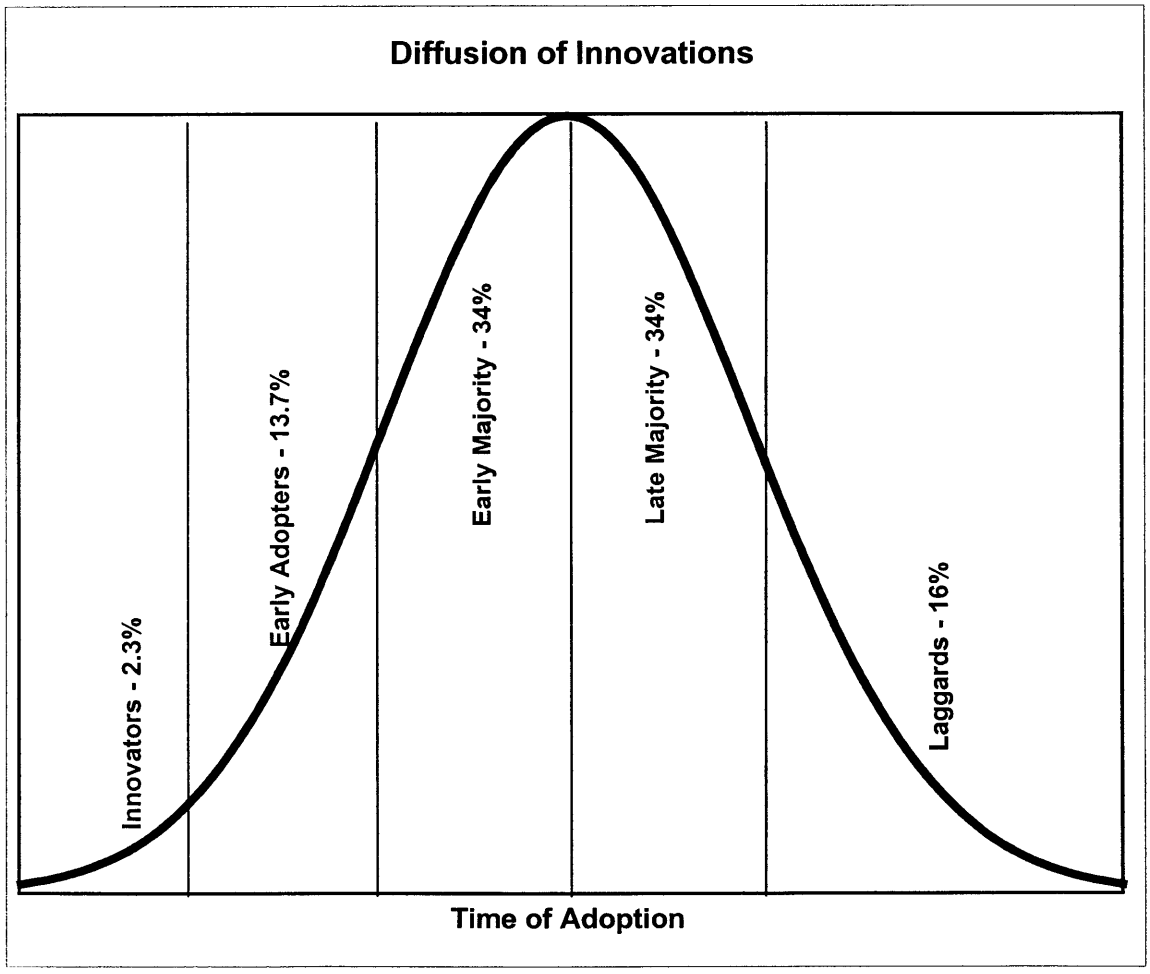


B. The Diffusion of Innovations

In Diffusion of Innovations[ii], Everett M. Rogers presented a model that describes how customers absorb new technologies. The model says that the adoption time falls into a normal curve and separates customers into five groupings, based upon when they will adopt a new technology. Rogers separates each group along lines of standard deviation:

1. Innovators, the first 2.3% of customers (those outside 2 standard deviations on the early side)
2. Early Adopters, 2.3%-16% (those within 2 to 1 standard deviations on the early side)
3. Early Majority, 16%-50% (within 1 standard deviation on the early side)
4. Late Majority, 50%-86% (within 1 standard deviation on the late side)
5. Laggards, the last 86%-100% of customers (outside 1 standard deviation on the late side)

A graph depicting Rogers' model follows:



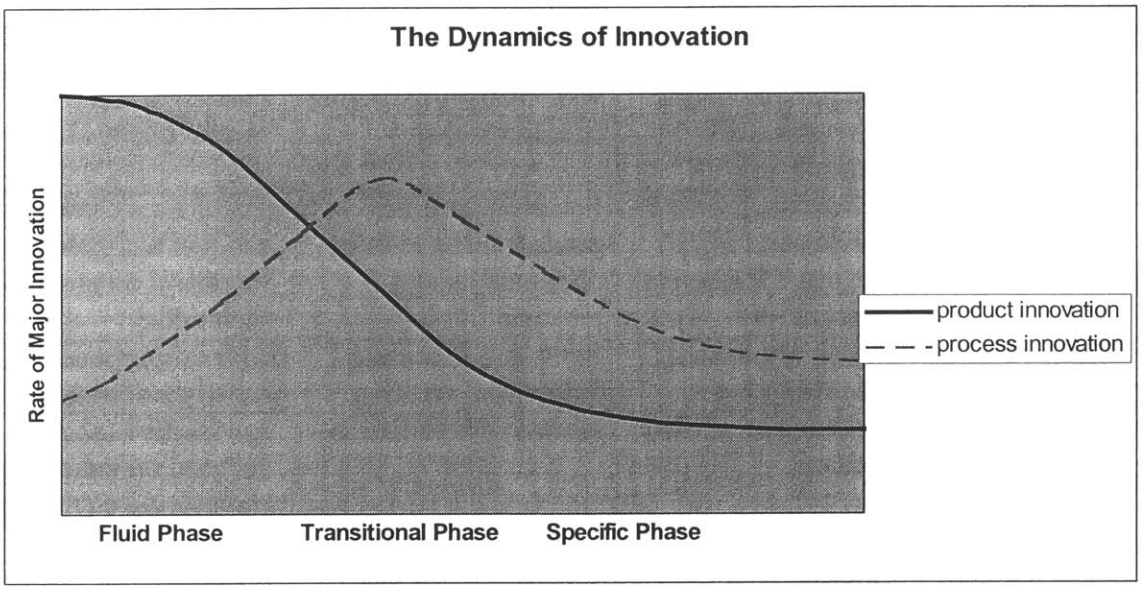
C. Technology Development: Product and Process Innovation

Utterback[iii] and Abernathy lower the microscope onto product performance and have developed an intriguing model about the two sources of innovation that improve performance: Product and Process Innovation. They separate the product life cycle into three phases: Fluid, Transitional and Specific.

During the 'Fluid Phase', Product design and operational characteristics experience great experimentation and contention while Process remains relatively unattended; generally, companies are more caught up in finding/designing what customers will buy than in the process for how the product will be produced – they are learning as they go along.

Eventually, the Fluid Phase gives way to the 'Transitional Phase', where the Product becomes more standardized (due to market forces or the decrees from an authoritative body), but the Process for making that product changes greatly. These 'standardized' products are often termed 'dominant designs[1]' which are typically created initially by piecing several other technologies together in a novel way.

Further on, an industry may enter the 'Specific Phase', where both Product and Process Innovation slows to a great degree; the industry becomes very stable and, thanks to having chosen a 'dominant design' can now focus on costs, volumes and capacities instead of performance requirements. This pattern is depicted pictorially for Assembled products:



Utterback[iv] is careful to point out some differences between 'Assembled' and 'Nonassembled' products. Assembled Products tend to hit upon the dominant design after an extended period of both manufacture and use of the product. Process innovation generally focuses on automation. Non-assembled products also undergo much experimentation, but Process experimentation is much more prominent. The process of choice is named an 'Enabling Technology' and shifts the focus away from process

[1] dominant design:

innovation and towards process refinement. Typically, Enabling Technologies are implemented with major equipment installations.

Utterback thoroughly and methodically deconstructs Product Evolution through the three phases, by carefully characterizing a dozen of the most compelling points of interest in each phase. The full explanation deserves many pages to completely flush out, but he has summarized much of his thinking (for Assembled Products) in one convenient chart:

1. Utterback's Summary of 'The Three Phases' for Assembled Products[v]

	Fluid Phase	**Transitional Phase**	**Specific Phase**
Innovation	Frequent major product changes	Major process changes by rising demand	Incremental for product; cumulative improvements in productivity and quality
Source of Innovation	Industry pioneers; product users	Manufactures; users	Often suppliers
Products	Diverse designs, often customized	At least one product design (dominant design), stable enough to have significant production volume	Mostly undifferentiated, standard products
Production Processes	Flexible and inefficient, major changes easily accommodated	Becoming more rigid, with changes occurring in major steps	Efficient, capital intensive, and rigid; cost of change high
Research and development	Focus unspecified because of high degree of technical uncertainty	Focus on specific product features once dominant design emerges	Focus on incremental product technologies; emphasis on process technology
Equipment	General-purpose, requiring heavy reliance on skilled labor	Some sub-processes automated, creating islands of automation	Special-purpose, mostly automatic, with low-skilled labor focused on tending and monitoring equipment
Plant	Small-scale, located near user or source of innovation	General-purpose with specialized sections	Large-scale, highly specific to particular products
Cost of Process Change	Low	Moderate	High
Competitors	Few, but growing in numbers with widely fluctuating market shares	Many, but declining in numbers after emergence of dominant design	Few; classic oligopoly with stable market shares

Basis of Competition	Functional product performance	Product variation; fitness of use	Price
Organizational Control	Informal and entrepreneurial; *organic*[2] *firms*	Through project and task groups	Structure, rules and goals; *mechanistic*[3] *firms*
Vulnerabilities of Industry Leaders	To imitators, and patent challenges; to successful product breakthroughs	To more efficient and higher-quality producers	To technological innovations that present superior product substitutes
Performance Criteria[4]	Ill-defined; confused market	Definition imminent; Based upon dominant design	Well-defined
Market[5]	Fragmented, unstable		Commodity-like, largely undifferentiated

Much of this thought hinges upon the idea of the 'dominant design' and the changes that the industry/market undergoes when the dominant design is brought to light. As dominant designs come into existence, Utterback stresses Co-specialized assets, industry regulation/government intervention, strategic maneuvering by individual firms and communication between producers and users. Controlling market channels, building a positive brand image, increasing customer switching costs, controlling standards, opening the architecture to rivals/partners while still controlling it, creating close ties to the customer and pursuing 'lead users' are all strategies that Geoffrey Moore might suggest during the early stages of the Technology Adoption Life Cycle.

The previous discussion has mainly been meant for assembled products; however, Utterback has much to say about non-assembled products as well. Non-assembled products tend to lend themselves to Process Innovation sooner and more intensively than assembled products. This innovation results in an 'Enabling Technology' that dramatically improves the product and becomes the de-facto standard and preferred production process, much as the 'dominant design' becomes the preferred product architecture. For non-assembled products, discontinuities are typically found in the process, instead of the product. For the most part, however, non-assembled and assembled products are very similar in the Fluid and Specific Phases; they differ mostly in the Transitional Phase. Utterback summarizes the many differences between assembled and non-assembled products in the following chart:

[2] Organic Firms: frequent adjustment and redefinition of tasks, limited hierarchy, and high lateral communication. Increased potential for gathering and processing information for decision-making.
[3] Mechanistic Firms: increased structure, rules and goals, rigid communication, routine operations, developed market relationships
[4] Thesis author addition, developed from Utterback's text - not on Utterback's original chart.
[5] Thesis author addition, developed from Utterback's text - not on Utterback's original chart.

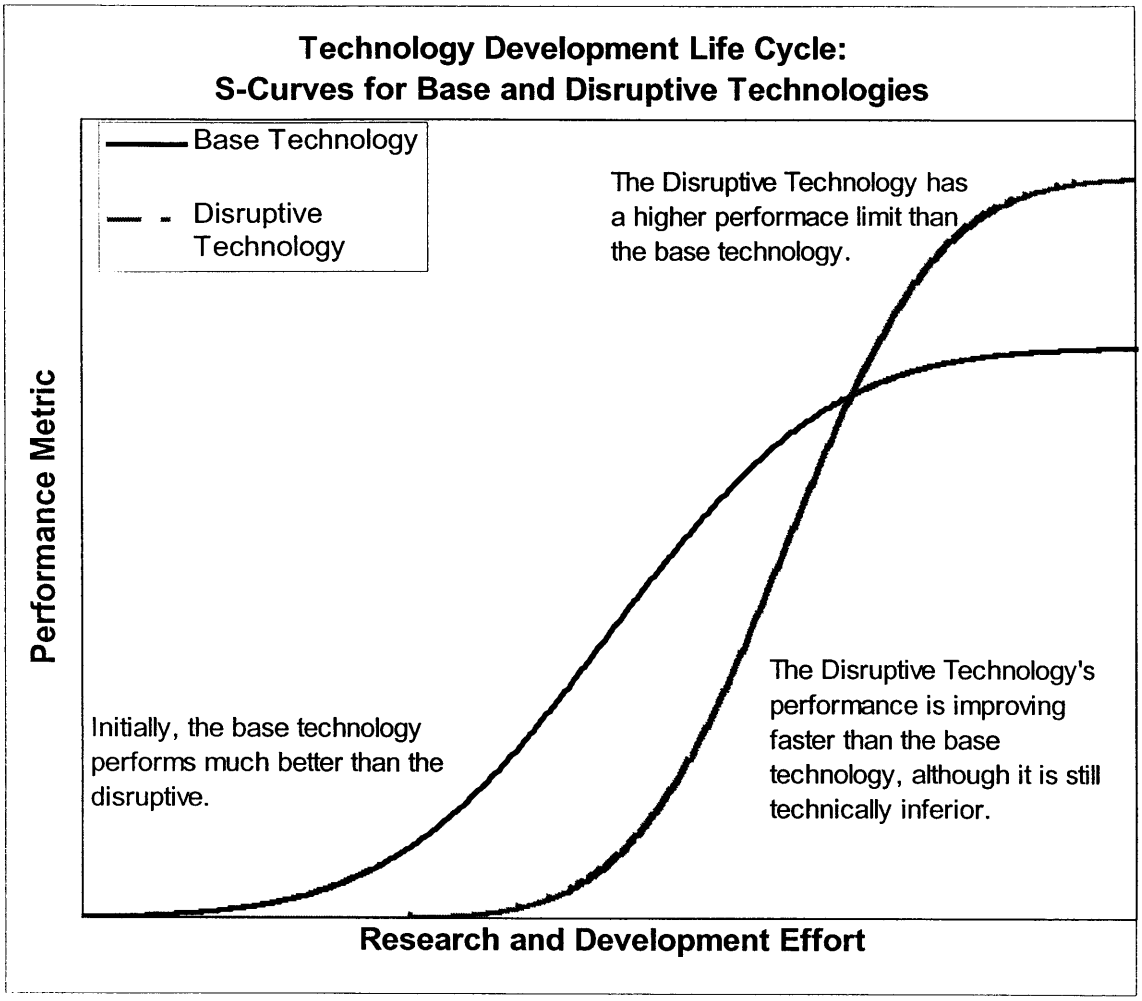
2. Utterback's Summary of Differences for the Transitional Phase between Assembled and Non-Assembled Products

	Assembled	**Non-Assembled**
Innovation	Emphasis on incremental product variation and product variation	Emphasis on process changes required by rising demand
Source of Innovation	Manufactures; users	Manufacturers; equipment makers
Products	Many features unique to individual producers	Increasingly undifferentiated
Production Processes	Some processes automated, creating islands of automation	Becoming more rigid, more continuous, more capital intensive
Research and development		
Equipment	Special-purpose equipment being introduced	Special-purpose equipment
Plant	General purpose with specialized sections	Single purpose, but small
Cost of Process Change	Moderate	High
Competitors	Many, but declining in numbers after emergence of *dominant design*	Many, but declining in numbers after emergence of *enabling process*
Basis of Competition		
Organizational Control		
Vulnerabilities of Industry Leaders	To both improved products and more efficient producers of current products	To more efficient and higher-quality producers

D. Disruptive Technologies

Just as vacuum tubes were surpassed by semiconductors in most applications, few (if any) technologies perform better than any other solution forever. New, less developed technologies that develop and improve in performance that overcome older, more developed technologies are often referred to as 'disruptive technologies'. Disruptive technologies are essentially an entirely new form or architecture of a dominant design.

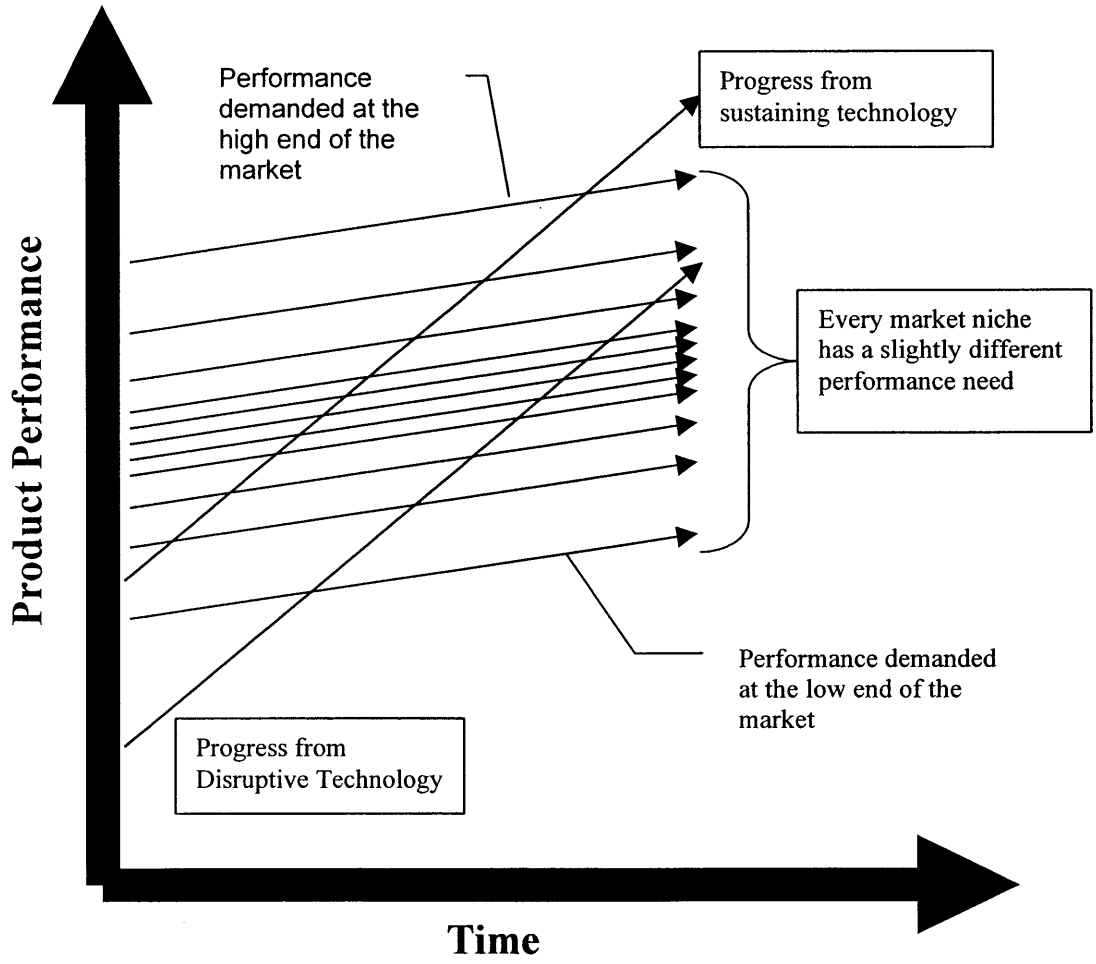
Disruptive technologies are subject to the same types of S-curves that older incumbent technologies experience. As such, the disruptive technology will start out undeveloped and will improve only with continued research and development. Often times, Incumbents ignore disruptive technologies, since they are underdeveloped and usually are sold on completely different performance metrics for completely 'uninteresting' markets. Eventually, however, the disruptive technology develops until it performs better than the incumbent technology, either because of a steeper S-curve (indicating faster improvement) or higher ultimate scientific limitations.



When incumbents see that a disruptive technology is taking the market, many times they will create a flurry of performance improvements and innovations that can improve performance dramatically and stave of the disruptive technology for a time. However, in the end, the disruptive technology meets market needs better, either because it improves too fast and overcomes the base technology on Performance Measures or the base technology reaches 'technology overcapacity' and greatly surpasses the market need.

1. Disruptive Technologies and Market Needs

Disruptive technologies are often technically superior on important performance metrics; this alone would be enough to replace Incumbent technologies. However, sometimes incumbent technologies improve beyond what the market needs or what certain niche markets need – leaving an opening for disruptive technologies between the market need for performance and the supply of performance. Christensen illustrates this with a graph:



Christensen suggests that when faced with this view, there are three strategies to take: match performance to market need and do not surpass it, improve performance and move up-market and to increase market demands for performance while improving product performance.

Of course, this particular view of disruptive technologies and market capture is entirely dependent upon the different rates of performance needs and supplies. It could be equally true that a 'disruptive technology' could come from above, if market needs accelerated rapidly or if the higher-performing technology made some performance metric-altering adjustments with a product or process Innovation. However, under Christensen's argument, he does not include this type of disruption when he normally talks about 'disruptive technologies'.

E. The Interaction between Technology Development and Market Development

New technologies are often introduced into small, niche markets that have peculiar needs where current solutions are not satisfactory. Generally, the new technology at this point is not well developed or well marketed when compared to the base technology. Over time, however, the new technology gains more and more market share and performs better and better. Market share is gained in several ways:

1. The new technology's performance on conventional metrics improves
2. The new technology's marketing effort improves
3. More niches are found where the new technology is suitable
4. Mass market needs change in favor of the performance metrics where the new technology is particularly suitable
5. The incumbent technology 'oversupplies' the market need, called 'technology oversupply' – or the state where the offered incumbent technology performs better than what the market needs or will pay for. New technologies, although they may still perform worse than the incumbent technology, may satisfy the market need quite well.

Recent authors have focused their attention on one or two of these types of changes (such as Christiansen with numbers 4 and 5 and Moore with number 3). More traditional thought tends to focus on numbers 1 and 2. Any way it comes, however, the interesting new technologies enter into the mass market and eventually push out the incumbent technology.

Utterback and Pistorius have presented one interesting model[vi]. They produced a framework that helps strategists to think about how any number of technologies engaging the same market area could interact with each other. They illustrate this with the simplest case of two technologies (A and B):

		Effect of A on B's growth rate	
		Positive	Negative
Effect of B on A's growth rate	Positive	Symbiosis	Predator (A) - Prey (B)
	Negative	Predator (B) – Prey (A)	Pure competition

While 'Symbiosis' and 'Pure competition' are familiar concepts, they illustrate the 'Predator-Prey' concept from two points of view. At first, they illustrate the typical disruptive technology story about how a new technology can 'hide' in a niche market and enjoy follower advantages from the mature technology. Then, they proceed to illustrate how a mature technology could 'wake up' when they see a new technology approaching a new market or promising to make a marked performance improvement.

In the paper, they also present a system of coupled differential equations that can be solved numerically when calibrated with historical data. This can be used to help make predictions about future growth. However, their formulation involves several variables that are considered constant for simplicity's sake but could change with time and may even change polarity (positive to negative or vice versa).

F. Review of processes for new technology cultivation

Technology cultivation requires two major activities: monitoring and decision-making. James Bright[vii] defines monitoring as four activities:

1) Searching the environment for signals that may be forerunners of significant technological change.
2) Identifying the possible consequences (assuming that these signals are not false and the trends that they suggest persist).
3) Choosing the parameters, policies, events and decision that should be observed and followed to verify the true speed and direction of technology and the effects of employing it.
4) Presenting the data from the forgoing steps in a timely and appropriate manner for management's use in decisions about the organization's reaction.

1. Utterback's Monitoring Process

Utterback draws heavily on Bright's work to illustrate how one should monitor innovation[viii]. He suggests that one can use 'signals' to develop a hypothesis. The hypothesis can lead to greater refinement in how to discover and 'pick up' future signals. For early innovations, Utterback suggests three highly significant signals: the Formation of New Firms, Patent Activity and the Commitment of Resources.

This assists companies to deal with 'contingent uncertainty' in that they can make more intelligent decisions as more data is revealed and examined. In this sense, the 'monitoring' activity is almost something of a real option.

2. Christiansen's Disruptive-Technology Based Process

Christiansen, who chiefly discusses disruptive technologies, defines how to spot and cultivate them:[ix]

1) Determine whether the technology is disruptive or sustaining
   a) Often engineering support, but marketing and finance opposition mark a disruptive technology.
2) Define the strategic significance of the disruptive technology
   a) Ask: "Will the technology surpass the markets' performance needs?" and "How quickly will the new technology improve?"
   b) Asking, "Will the technology surpass the performance of the old technology?" is relatively unimportant.
3) Locate the initial market for the disruptive technology
   a) No concrete market exists when the company must make the decision to invest.
   b) Must create information instead.... who customers are, what they value, etc.
   c) Experiment rapidly and inexpensively with both product and market.
   d) Do not rely on traditional channels or customers. Often times, they lead companies down the wrong path.
4) Place responsibility for building a disruptive technology business in an independent organization
   a) Only necessary when the profit margin is lower and the customers are different.
5) Keep the disruptive organization independent

a) Avoid bringing in the independent organization when the market grows larger. This is because arguments over resources and cannibalization generally spring up.

3. Geoffrey Moore's Marketing-Based Process

Moore takes a distinctly marketing-based perspective on cultivating new technologies in a generic sense. However, it is removed from the thesis body because we feel it is not quantitatively rigorous. That said, it does have a quite a following among practitioners. Moore's 'process' is laid out in great detail in Appendix II.

III. NEW PROCESS MODEL DEFINITION

The processes previously reviewed are solid and fine as far as they go. However, they make some assumptions about prior industry knowledge and leave some questions unanswered. For instance, how exactly does one determine if a technology is disruptive or not? What kind of background information is needed to make that determination? What kind of current information is needed? How might information be gained to make that determination? What might one check on to see if the market will, indeed, adopt a new technology? What does a company do, internally, to respond to an opportunity caused by a new technology? How does one convince a conservative organization to pursue a 'risky' new technology opportunity? How might the new technology be developed? This thesis attempts to answer these questions by defining a generic new process framework for technology evaluation, strategy and then applying the process to one particular technology.

A. Process For Creating Technology Strategy At A Semiconductor Equipment Maker

1) Know the technology strategy and new product marketing literature
   a) Jim Utterback, Clayton Christensen, Richard Foster, Geoffrey Moore, etc.
2) Know the existing industry dominant designs, paradigms and problems
   a) Dominant Design(s)
   b) Paradigms: Moore's Law
   c) Problems: Power consumption, heat transfer, design productivity, etc.
3) Recognize where the overall industry is in the technology strategy thought
   a) Draw an S-curve
   b) Compare the industry as it relates to the S-curve
4) Understand the your company's competitive position
   a) Measure the current situation
   b) Predict the likely direction that customer needs industry will move in
5) Identify new technology opportunities and threats.
   a) Sustaining Innovations: New substrates, new design techniques, etc.
   b) Disruptive Threats: biological computing, nanotechnology, etc.
6) Pick one technology to thoroughly investigate.
   a) One technology may deserve special investigation because:
      i) Our tooling/ process/ knowledge is used to create the main benefits
      ii) The technology substitutes for some of your own products/ specialties
      iii) Our research and development scientists/engineers have an interesting technology that could enable the market
7) Technical Review of the chosen new technology
   a) What is it?
   b) What does it do?
   c) Are there variants of the technology?
   d) How is it made?
   e) What is the current status?
   f) This information can be found from many sources:

i) Prospecti, 10Ks, public statements, news announcements, other financial statements of public companies
ii) Industry journals and publications
    (1) Online (internet and searchable databases)
    (2) Paper
iii) Patents
    (1) U.S.
    (2) Worldwide
iv) Experts (have opinions and vital contacts)
    (1) Internal
    (2) External (often found in industry publications, patents)

8) Market review for the new technology
   a) How does it fit into the competitive picture?
   b) Who is advocating or denouncing the technology? Why? What are the technical or market arguments? Do they make sense?
   c) What is the current market situation? What companies are involved, making, complementing or using the technology?
      i) Competing processes
         (1) Check on the number and the dominant processes.
         (2) Look for a clear winner, but do not worry if it is not clear yet.
      ii) Suppliers
         (1) Check on the number and the dominant suppliers.
         (2) Check on quality of product/ customer satisfaction
         (3) Check on strength
         (4) Value companies for mergers and acquisition
      iii) Complements
         (1) Check on the number of new announcements and their commitment.
         (2) This is especially important in networked environments like semiconductors.
      iv) Customers
         (1) Check on their current offerings and roadmaps.
         (2) Talk to contacts/ qualification divisions
      v) Alliances
         (1) Check on the number and their strength/ commitment
   d) What might the future market look like? What process might win out over the others?
      i) Consider creating an original model, perhaps based upon the Lotka-Volterra Model[x]
      ii) Check for market forecasts – note that believability decreases from top to bottom.
         (1) Industry groups
         (2) ITRS, SIA, SRC Roadmaps
         (3) Customers – roadmaps/ public statements
         (4) Private Firms – Dataquest, IC Insights, Rose Associates
         (5) Suppliers of the new technology

   e) 'Step back' a moment and ask some questions:

i) What are the benefits? Who are the advocates?
ii) What are the disadvantages? Who are the detractors?
iii) What are the complications? What do we know that is still unknown?
iv) Show discernment in your opinion!
(1) Experts/ research scientists/ marketers/ companies/ publications have their own opinions, experiences and/or agendas. These may be quite different.
(2) Current benefits do not equal future benefits
(3) Future benefits are probably currently undefined!

f) For some new technologies:
i) The advocates are respected, but do not have the highest volumes or profit margins, so can't drive it.
ii) The detractors dominate the industry and publicly denounce the new technology, while privately piling up a lot of patents.
iii) The disadvantages and Complications are rapidly decreasing as more and more effort is expended.
iv) Although the current benefits are somewhat diminishing, other, future benefits, could be enormous.

9) Think about where the technology fits into technology strategy thought
a) How does the technology fit into the industry?
b) How does the technology help/hurt the end customer or your customers?
c) How could the technology affect your company?

10) Gut check
a) It will probably be hard to predict the true size of the market
b) Often times, there will be extremely divergent opinions on a new technology and on the market for the new technology
c) Scenario building
d) Make your own predictions
e) Decide if your company needs to take action based on your predictions

11) Identify company options and evaluate on multiple criteria
a) Gather opinions/ insights/ history from research and development, marketing, operations and senior staff about company options
b) Evaluate each of these options on multiple criteria
c) Delve into areas that could possibly make the project fail

12) Suggest a strategy to key decision makers

13) Business development - implement approved recommendations
a) Get going!
i) Write a business plan for internal technology developments
ii) Identify interests and negotiate joint development programs
iii) Start due diligence for mergers/ alliances that enable the strategy
iv) Time your moves/ announcements to your advantage
(1) Do you do everything all at once to hide your actions from competition or get information from one project before starting another?

14) Continuously monitor the technology and market
a) Look for signs of weakness or for strong opportunities.
b) Make sure that the organization wherein you place the new technology has the resources and freedom to fully pursue the opportunity.

IV. KNOW THE EXISTING INDUSTRY PARADIGMS AND PROBLEMS

A. CMOS on Silicon is the Dominant design

Richard N. Foster, a former McKinsey Consulting senior partner and author of "Innovation: the Attackers Advantage", wrote this:

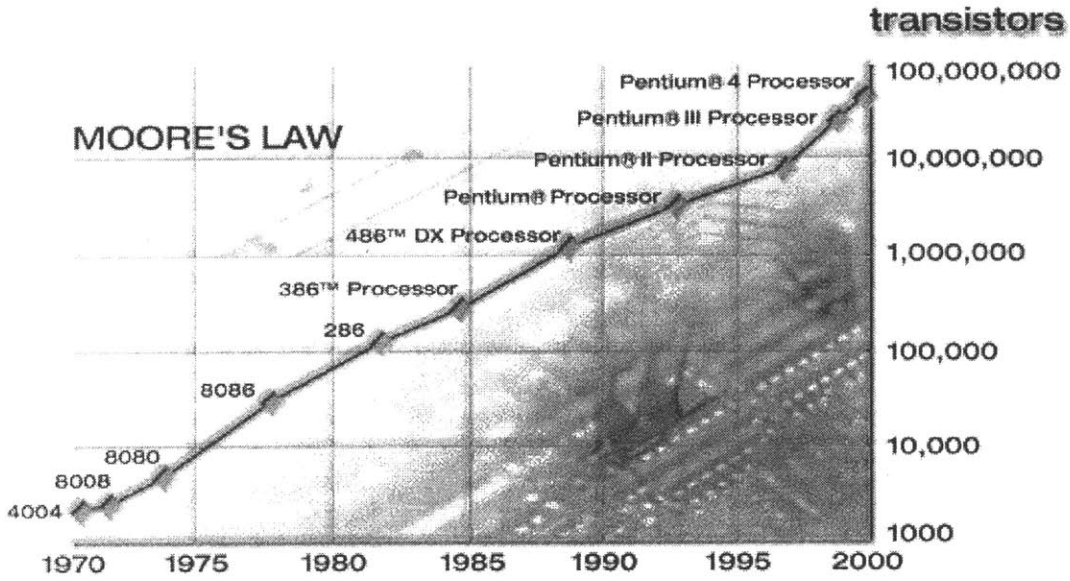
> 'In electronics there have been many fast and traumatic transitions... Germanium lost 12 share points per month at the height of the transition to silicon. Integrated circuits went from 20 percent to 80 percent of the market in six years. Within integrated circuits we have seen rapid transitions from PMOS to NMOS to CMOS. In each case the attacking technology gained about 10 to 15 market share points per year after it caught on.'

CMOS on Silicon is the most common type of semiconductor in the market. Most computer chips use this 'dominant design' near exclusively. Other materials and other semiconductor architectures (such as Bipolar, FinFets or junction-FETs) are mainly used in specialty niche applications such as high-end communication equipment, highly advanced servers, etc. However, CMOS on silicon is the dominant design without question.

B. Moore's Law

Bulk Silicon, grown by pulling a crystal through molten silicon, was the preferred substrate architecture for semiconductors for years. As time went on, chip manufacturers needed ever-higher quality Silicon for their devices and, unfortunately, Bulk Silicon did not deliver. Epitaxial Silicon, grown in a special process on top of bulk, proved itself to be much purer and has been the preferred substrate architecture for years. Although bulk has become increasingly better over the years, Epitaxial Silicon is still the most pure substrate available. On both of these substrate architectures, better device performance has been achieved by relentlessly decreasing the size of the individual devices/transistors. Shrinking device sizes has led to faster speeds, lower power requirements per instruction and reduced costs.

"Moore's Law", which states that 'the number of transistors per integrated circuit doubles every 18 months', is the most famous expression of this observation. (Originally, however, Moore predicted that the number of transistors per integrated circuit doubles every 12 months.) The following Intel-specific graph depicts the general truth of Moore's Law.



xi

Moore's Law, in fact, has proven itself correct for far longer than Gordon Moore predicted. (In 1965, he had originally predicted that the number of transistors per chip doubles every year this trend to continue up to 1975[xii]). Today, Moore's Law has become so pervasive and so well-established that forecasts, chip-makers, Wall Street and the U.S. Government all depend on it as if it is a fundamental law of science, like gravity or entropy. As a result of expectation and the economics of production, researchers and developers have knocked down every wall, every obstacle to remaining on the curve predicted by Moore's Law...and the industry has spent ever more to knock down those obstacles. An interesting addition to Moore's Law, is the lesser known "Rock's Law", which states that the cost of capital equipment will double every four years. Of course, Rock's Law is a bit unconstructive, because it says nothing about the performance of new capital equipment, the throughput or (more generally) the 'Cost of Ownership'. Nevertheless, it points out the fundamental problem that the Semiconductor Industry faces: The tail end of the Technology S-curve for the current product architecture.

C. Moore's Law does not predict true technical progress

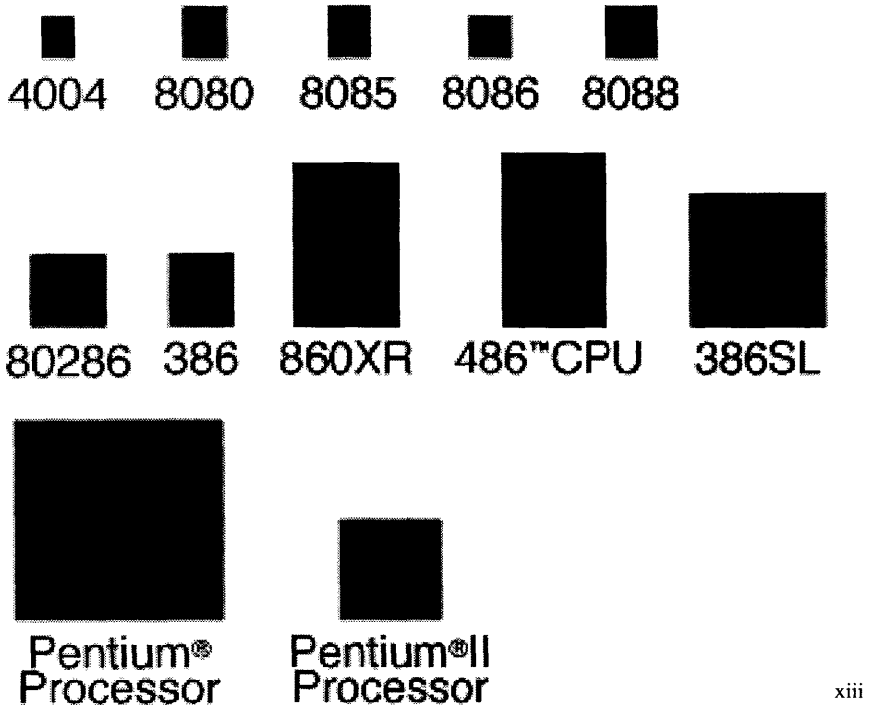
Although most people believes that Moore's Law indicates true technological progress within the semiconductor industry, Moore's Law is somewhat deceptive because Transistors per Chip is a function of four things:

1. Device size (line widths),
2. Memory on chip
3. Isolation methods
4. Chip size.

Not to trivialize the complications of creating larger chips[6], chipmakers have always been able to stay on Moore's Law by increasing the chip size when device

[6] Holding everything else equal, chips that are four times the size of other chips, have four times the chance for a defect within the starting material or for a defect to occur during each processing step. Therefore, maintaining acceptable yields requires ever-increasing purity, quality and repeatability.

shrinkage/ new isolation methods could not maintain the curve predicted by Moore's law. Note how Intel's chip sizes have changed:

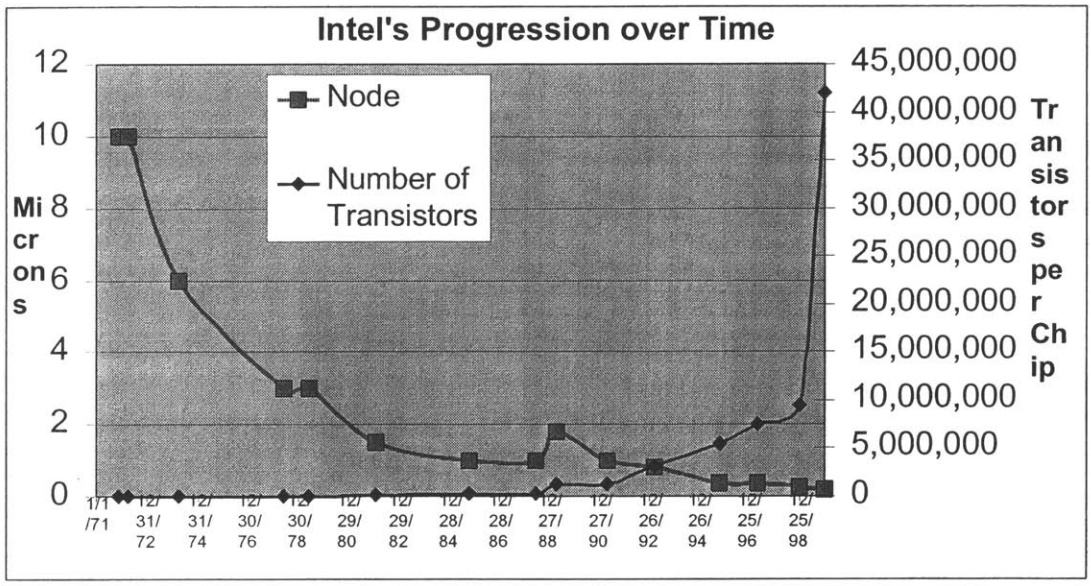


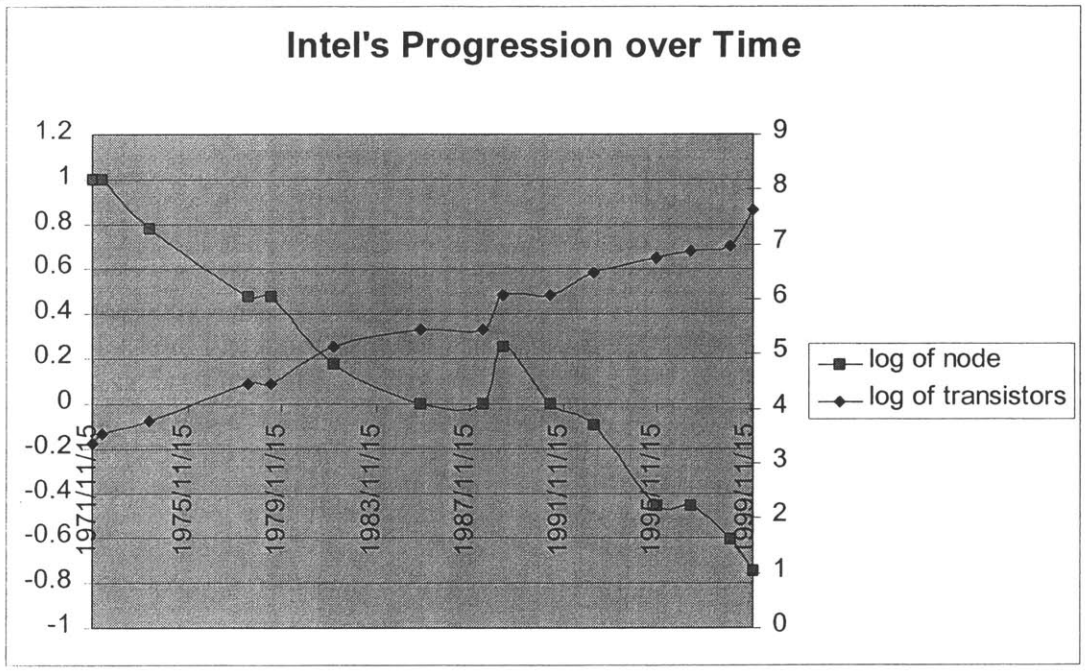
xiii

To illustrate this point, Intel's 386 and Pentium processors are a good choice. Intel's 386 Processor, at the 1-micron node, had 275,000 transistors and Intel's Pentium Processor, at the 0.8-micron node, had 3,100,000 transistors. The Pentium had 11.27 times the number of transistors that the 386 contained, but was also roughly 9 times larger[7]. This implies that simply looking at the number of transistors on a chip is not an adequate metric to judge the true scientific progress in this field because the number of transistors in confounded with chip size.

Shrinking Line Widths means that the 'working area' for each individual transistor shrinks. Therefore, the same size defect is less important on an older, larger Line Width node versus a newer, smaller Line Width node. For example, a 0.25-micron defect on the 10-micron node may be acceptable, but a 0.25-micron defect on the 0.13-micron node will destroy the circuit. Therefore, maintaining acceptable Yields requires ever-increasing purity, quality and repeatability.

[7] Note that 11.27*(0.8/1) (the scale factor between these two Processors) = 9.02. Therefore, 9.02 is, approximately, how much larger one would expect the new chip generation to be, while remaining on the curve predicted by Moore's Law. One should also note that the addressable and virtual memory on these chips remained constant, so memory addition did not force Intel into using a larger chip. Do not, however, believe that all generations display this behavior; some generations show much more shrinkage than this process predicts, some less. This example has only been chosen to illustrate the point.





xiv

D. Heat and Power Consumption are Big Industry Challenges

Heat. Power. Nearly all chipmakers acknowledge that heat and power will be two of their biggest problems in the future if they do not already do so. As transistors get smaller, they get denser and chips can make more calculations. As transistors get denser and make more calculations, chips get hotter and use more power. This turns into a problem for battery science and for heat dissipation, because mobile chips would soon deplete their batteries and chips could conceivably melt their way right out of the computer. Of course, these are just the problems of fundamentally making the system work – it says nothing about the need to conserve energy and how more and more of the

world's energy is created to feed chips. As Mark Dean, IBM fellow and vice president of systems research, said,

> "Very quickly, energy and heat will go from being irritants to major product development limitations. The demand for increasingly powerful systems is driving up the amount of heat within many new products. If we don't address the power issue, products will become so hot that you'll be able to cook with them rather than compute with them."[xv]

Below is a small chart displaying the power used (and the heat dissipated) by three generations of Intel chips:

[xvi]	486	Pentium	400 MHz Pentium II
Watts	<5	10	28

Notice the dramatic growth in power usage. Continued power consumption growth with this type of ramp would indicate serious trouble as chips hit the 2-3 gigabit realm.

E. Unnecessary Power Consumption:

Semiconductors, however, do not need to use as much power as they do today. In fact, the actual power that is involved in the useful logic is similar in size to the power that is 'wasted'. There are three main sources of unnecessary power consumption within semiconductors:

1) Dynamic switching
   a) Capacitance
      i) Output capacitance of gate – mostly junction parasitic capacitance due to drain diffusion regions
      ii) Total interconnect capacitance – becoming the dominate capacitance
      iii) Input capacitance at the driven gates – mostly gate oxide capacitances determined mostly by the gate area of the transistor
2) Short-Circuits
3) Leakage
   a) Reverse Bias Leakage
   b) Subthreshold Leakage
   c) Gate Leakage

Detailed discussions, mostly garnered from a Worchester Polytechnic Institute web course[xvii], for each of these 'unnecessary power consumptions' follows.

1. Switching Power Dissipation

The Power used to switch a transistor on and off again is commonly:

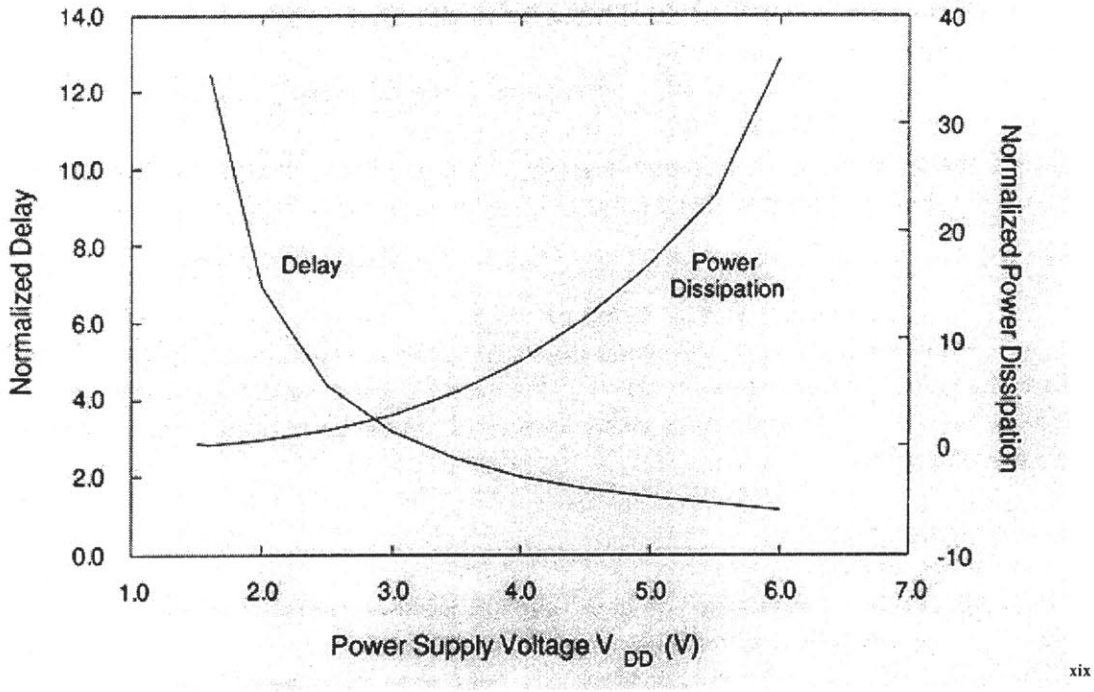
$$P_{avg} = C_{load}V_{DD}^2/T \quad \text{or} \quad P_{avg} = C_{load}V_{DD}^2 f$$

So, for any given desired switching frequency (f), the way to cut power is to lower V_{DD} and C_{load}. But, decreasing V_{DD} increases propagation delays:

$$\tau_{PHL} = \frac{C_{load}}{k_n\left(V_{DD} - V_{T,n}\right)}\left[\frac{2\,V_{T,n}}{V_{DD} - V_{T,n}} + ln\left(\frac{4\left(V_{DD} - V_{T,n}\right)}{V_{DD}} - 1\right)\right]$$

[xviii]

Graphing these two equations together, while holding all variables constant except V_{DD}, we see this:



[xix]

However, the propagation delay limits the switching frequency, so that the frequency is sometimes lower than expected.

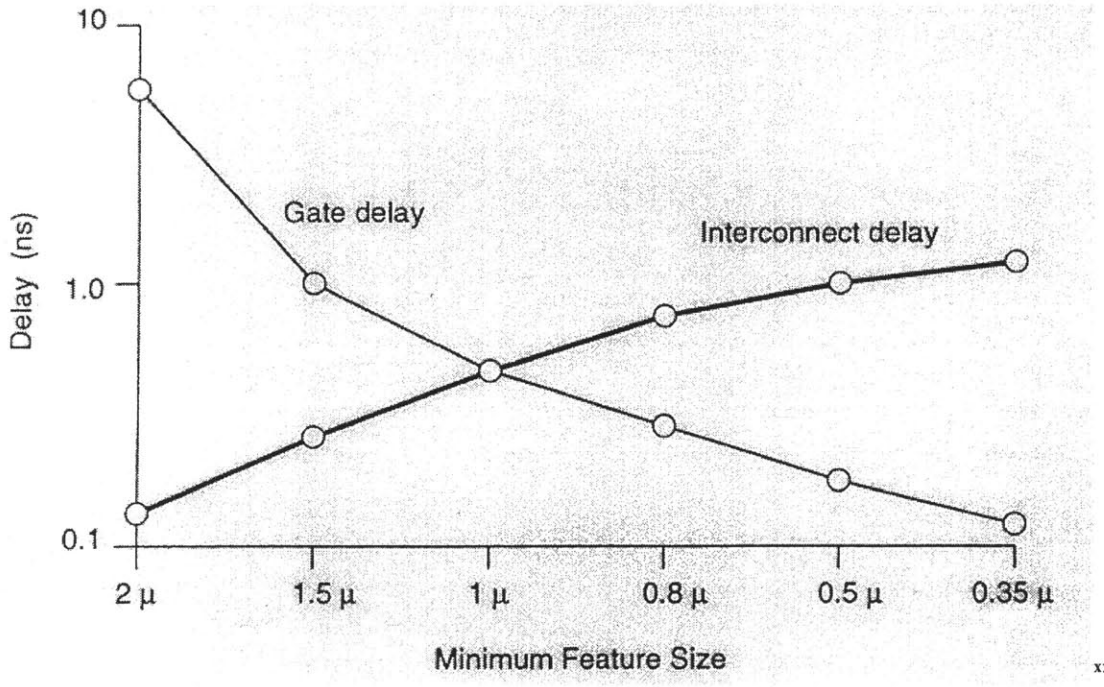
$$P_{avg} = \alpha_T \cdot C_{load} \cdot {V_{DD}}^2 \cdot f_{CLK}$$

[xx] where α_T is the expected number of transitions per clock cycle (generally less than one). However, Voltage transitions sometimes occur at voltages less than V_{DD}. The generalized expression for Power consumption due to Dynamic Switching is:

$$P_{avg} = \left(\sum_{i=1}^{\#\ of\ nodes} \alpha_{Ti} \cdot C_i \cdot V_i\right) \cdot V_{DD} \cdot f_{CLK}$$

[xxi]

It is interesting to note, however, that as a percentage of the total circuit delay, Interconnect Delay is rapidly swamping Gate Delay. In other words, while Junction Capacitance remains important, its importance relative to other problems is decreasing. The next diagram illustrates this point:

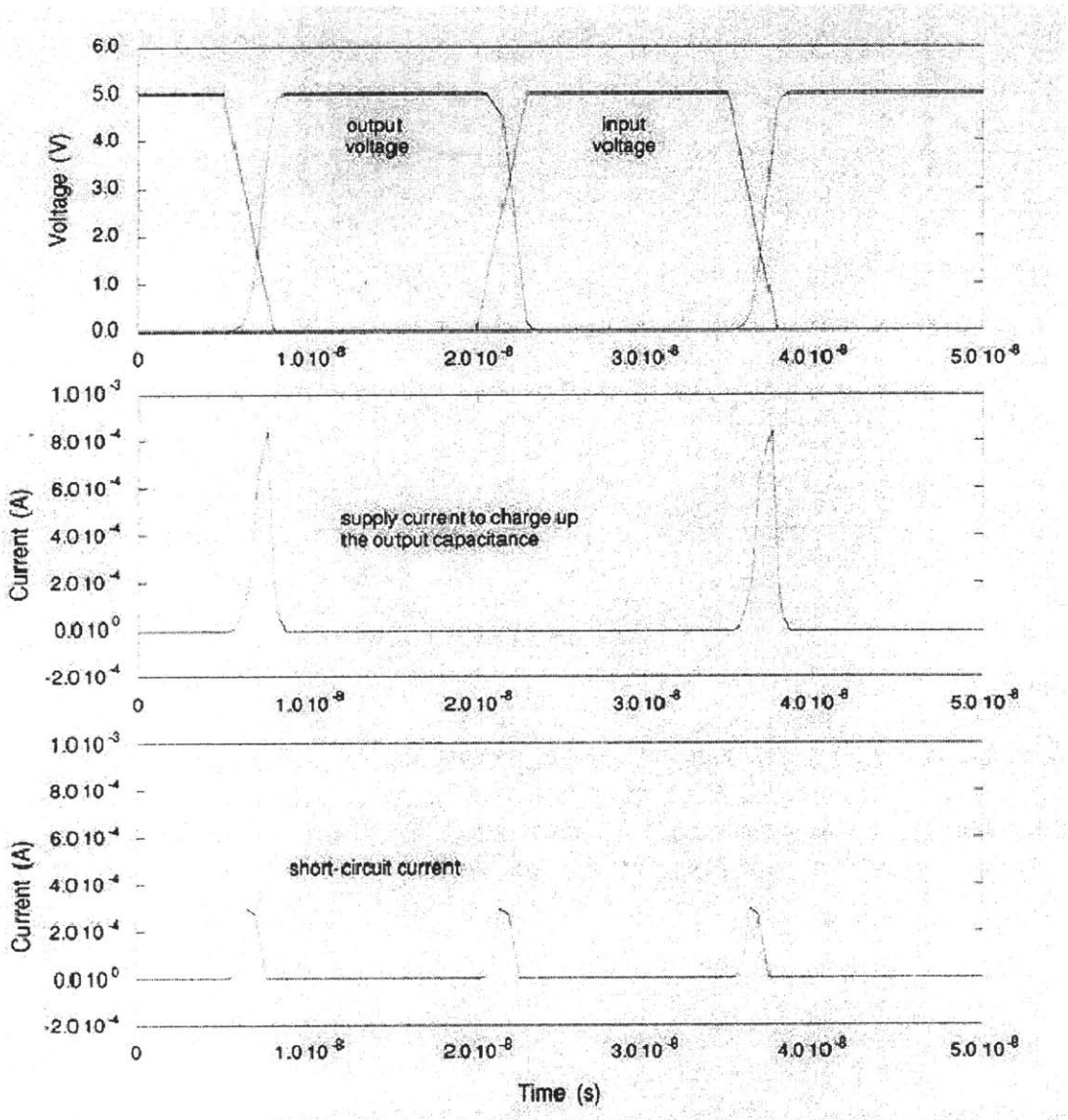


xxii

2. Short-Circuit Power Dissipation

Because input signals are not perfectly instantaneous and it takes time for the input signals to rise and fall, the nMOS and pMOS transistors may conduct current for a short period of time simultaneously.[8] This creates a direct current path and a short circuit. Following is a graph that illustrates this point:

[8] The nMOS transistor conducts when the input voltage reaches V_T and the pMOS transistor conducts when the output voltage reaches (V_{DD}-|V_T,p|). Since both these voltages are changing at the same time, there is a chance that these 'conduction voltages' will be reached during the same time interval, thus creating a short circuit.



[xxiii]

Therefore, we wish to minimize the time it takes to reach the desired input and output voltages or to sufficiently space the signals. Nevertheless, the problem still exists that there is a current draw (and therefore a power draw). The generalized expression for power consumption due to the short circuit effect is[9]:

$$P_{avg}(short-circuit) = \frac{1}{12} \cdot k \cdot \tau \cdot f_{CLK} \cdot (V_{DD} - 2V_T)^3$$

[xxiv]

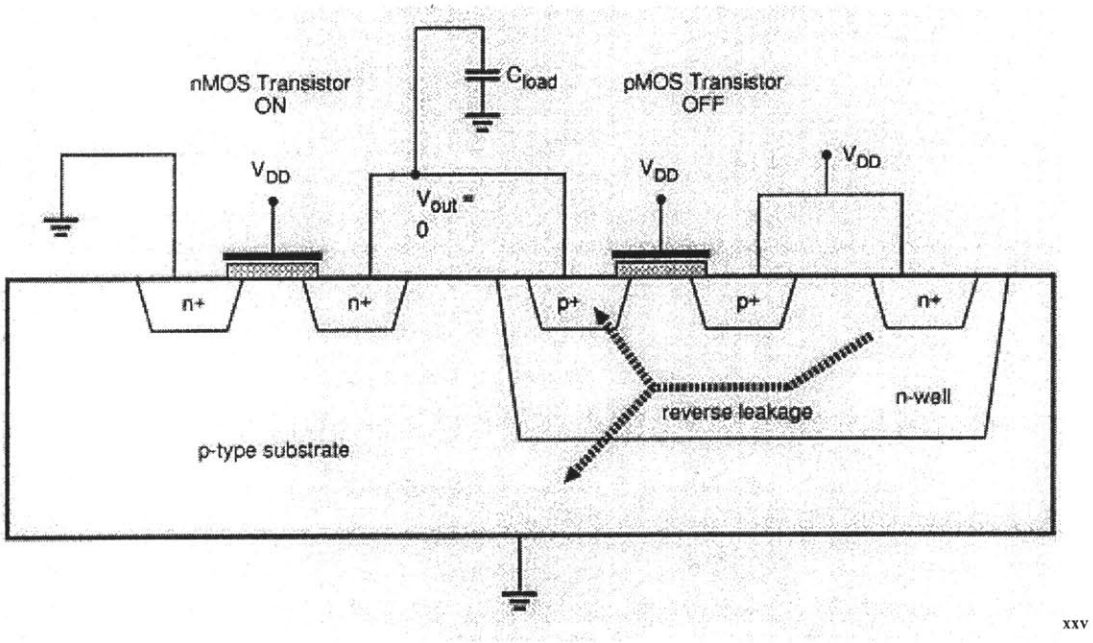
Intuitively then, designers want ramp up and ramp down to happen at different times (make output transition slower and input transition faster). In addition, they want to minimize V_{DD} and make $V_T \sim 1/2V_{DD}$.

[9] Assuming a very simple CMOS model where ramp up and ramp down times are equal, $V_T=V_{T,n}=|V_{T,p}|$ and $k=k_n=k_p$.

3. Leakage Power Dissipation

CMOS transistors usually have a small current flow, even when the transistor is in the 'off' state. This is sometimes referred to as subthreshold current or reverse leakage or gate leakage, but is really made up of all of these types of leakages.

Reverse leakage is caused by imperfect isolation. In the figure below, the pMOS transistor on the right is 'off' and held at V_{DD}. Although it does not contribute to the logic, there is still a reverse leakage current from V_{DD} to ground.

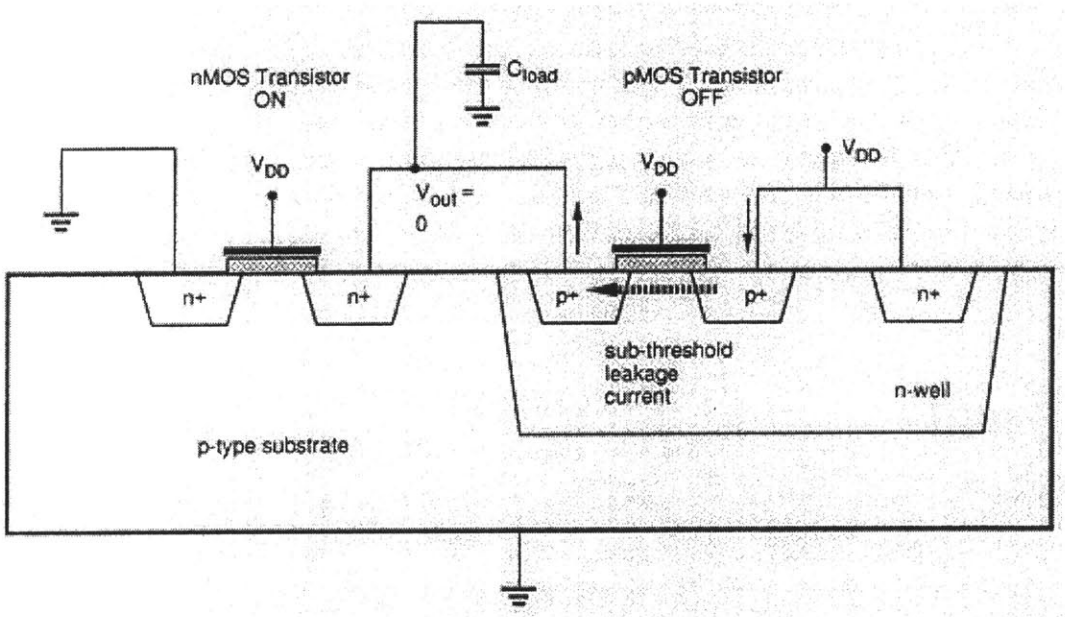


[xxv]

When the transistors are switched on and off in the opposite way, there is another leakage current in the nMOS transistor. When both transistors are off, there is double the leakage current. The generalized expression for the reverse current leakage in a pn junction is:

$$I_{reverse} = A \cdot J_S \left(e^{\frac{q V_{bias}}{kT}} - 1 \right)$$ [xxvi] where V_{bias} is the reverse bias voltage across the junction, Js is the reverse saturation current density and A is the junction area.

Subthreshold current is due to carrier diffusion between the source and drain. Basically, it means that one transistor looks to be 'on', even though the gate has not reached V_T yet and the transistor is not supposed to have turned on yet. Below is a diagram depicting subthreshold current:



xxvii

The generalized expression for subthreshold leakage is described by:

$$I_D(subthreshold) \cong \frac{qD_n W x_c n_0}{L_B} \cdot e^{\frac{q\phi_r}{kT}} \cdot e^{\frac{q}{kT}(A \cdot V_{GS} + BV_{DS})}$$

xxviii

Note that subthreshold current is exponential with terminal voltages and that it occurs even when both transistors are in the 'off' state. This makes designers want to avoid low V_{TS} for both the nMOS and pMOS transistors so that V_{GS} and V_{DS} are well inside the 'safe' zone and below V_T.

Gate leakage occurs when current flows through the gate oxide and into the gate. This happens when the gate oxide is not thick enough or does not have a high enough value for "k" (electrical insulation), given a certain gate voltage. Chipmakers respond to this problem by lowering the gate voltage, thickening the gate oxide or finding a gate oxide with a higher 'k' value.[xxix]

F. The Effect of Unnecessary Power Consumption:

The net effect of these three types of leakage is that there is always a small current draw in a MOSFET. As the number of transistors per chip grows and transistor density increases exponentially the power draw and the heat also rise exponentially.[10] Exponential power increases and exponential heat dissipation needs are not sustainable. Therefore, industry needs to design new transistors, new chips and create new design/cooling paradigms that will minimize power draw and increase the cooling rates.

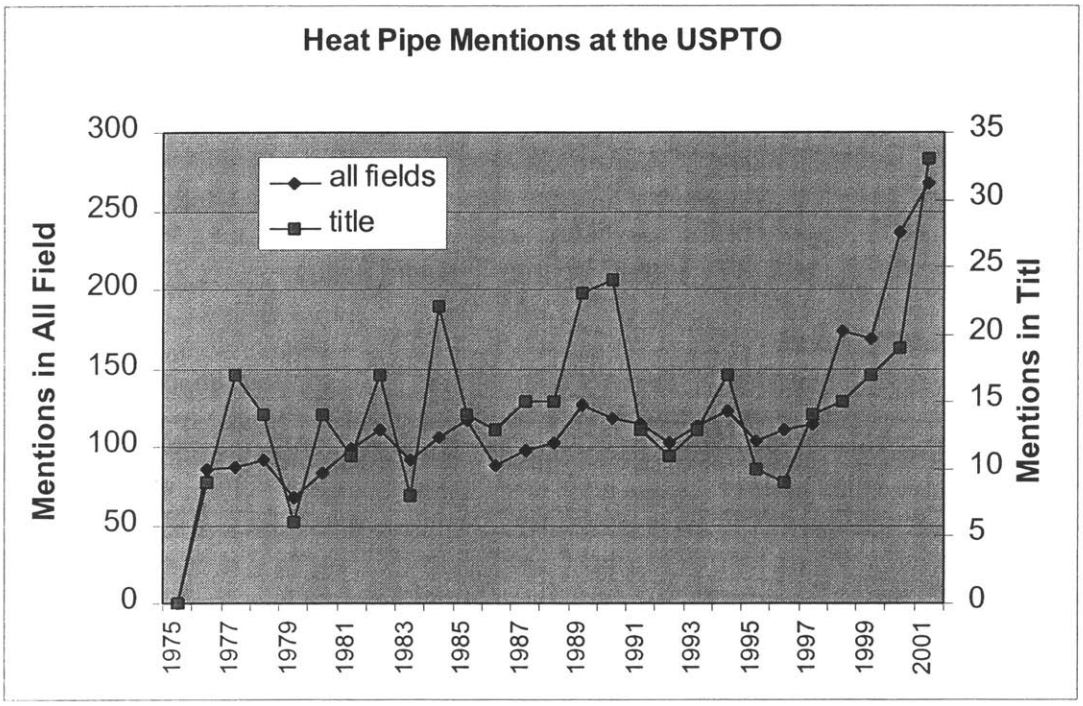
[10] Too make things worse, higher temperatures generally lead to still higher off-state leakage currents (I_{OFF}) and still higher power draws.

At the extreme, EVERYTHING that reduces power consumption and heat in semiconductor operation or helps to draw heat out of the device will eventually be used. Of course, everything is too strong a word; it is more accurate to say that everything that is in the proper stage of development and does not exclude a better heat/power saving technology (that is also in a proper stage of development) will eventually be used. This assertion is implied by the generalized S-curve model, wherein technologies that are approaching the flat, upper portion may adopt many different 'sustaining technologies' to achieve higher performance (even moderate improvement gains).

G. Heat Removal

There are, fundamentally, three ways to remove heat: conduction, convection and radiation. Most computers use convection to cool their chips with built-in fan assemblies. However, electric fans are susceptible to breakage because of their moving parts, make noise, draw power, require a lot of valuable real estate within the computer and draw in dust and debris.[xxx] Most computers also use conduction to cool their chips with a substantial heat sink. However, heat sinks must increase in size and weight to cool larger loads.[xxxi] In addition, heat sinks are much hotter near the heat load than the extremities, limiting their effectiveness and allowing 'hot spots' on the chip. Some computers use both heat sinks and fans together, often with the fan targeting the heat sink. Many computers are kept in air-conditioned rooms to increase the effectiveness of convection. Some exotic systems even use a chilled liquid to increase the heat transfer.

Heat Pipes are a newer foray into chip cooling and demonstrate far better cooling abilities than heat sinks. Heat Pipes consist of a sealed tube, partially filled with a liquid such as water. The pipe is placed near a heat source and the liquid in that area vaporizes. The vapor travels throughout the tube, bringing the tube to a near-uniform temperature. Fins, far from the heat source, use conduction to carry the heat away from the tube, returning the vapor to a liquid state. Convection or forced convection carries the heat away from the fins. Although the technology has been around for 25 years, Heat Pipe patents have increased exponentially in the past six years and year 2001 patents nearly doubled those from 2000. This indicates an increased interest in heat transfer and recognition of the need for cooling.



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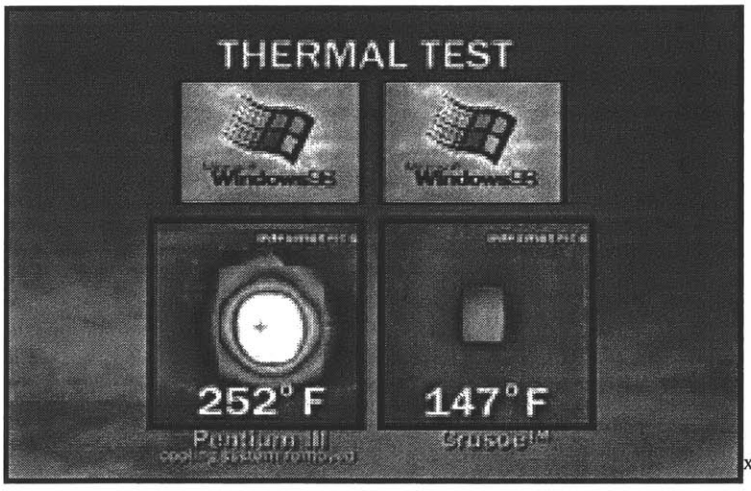
H. Power Reduction

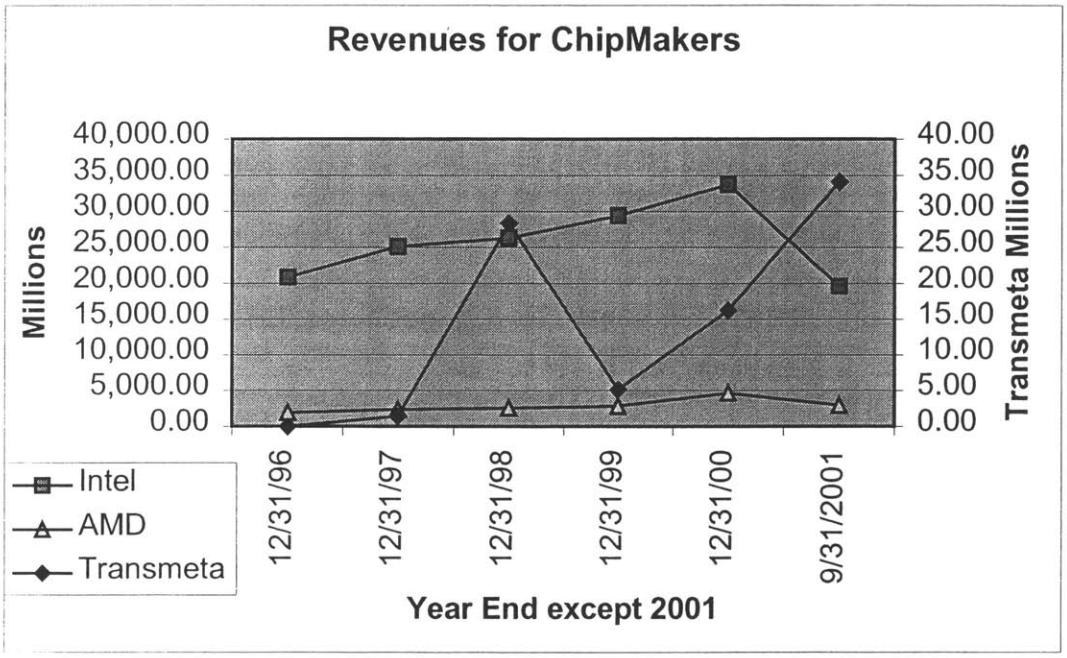
By reducing power usage, heat creation and the need for heat dispersion falls. In recent years, industry has grown more and more aware that power reduction is a vital need. Indeed, many power-saving design modifications have found their way into common usage. However, the proliferation of the use of these designs is not easily demonstrated.

Transmeta Corporation uses a particularly effective combination of on-chip techniques (Very Long Instruction Word architecture) along with a specialized software package to draw less power and to create less heat than other processors. Thermal image cameras captured this side-by-side demonstration of an Intel Pentium III 500MHz, 1.6-volt part (with the cooling apparatus removed) versus a Transmeta Crusoe TM5600 600MHz, 1.6-volt part:



xxxiii

Transmeta's product strategy takes into account the fact that most software applications do not require the full attention of the entire processor; their software simplifies instructions sent to the chip, while changing both the voltage and frequency on the chip in real-time and *based on the application requirements*.[xxxiv] This results in dramatic power savings and has driven revenues exponentially (despite 2001's drastic industry retraction and Transmeta's fabrication processing difficulties):



[xxxv]

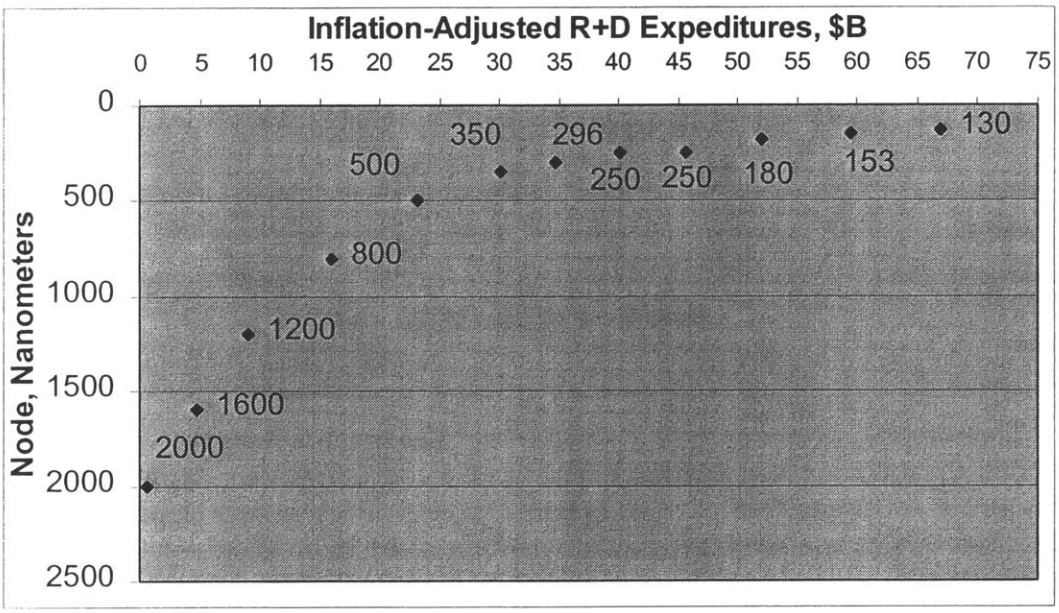
Transmeta's exponential rise in revenue over the last two years shows that there is market demand for processors that use less power than other processor designs. In addition, Intel, AMD and IBM have also revealed their new low-power chips. This indicates that these manufacturers (and their customers) are more interested than ever in saving power.

It is quite possible that Transmeta's design of removing some of the complexity from the silicon and adding it to the software represents a 'disruptive technology'. Software code is generally much easier to change and to simulate than silicon non-linearities. It may indicate that software could become the more important piece of the puzzle than the silicon itself and it is taking over more and more functions that the silicon used to handle alone; in a sense, software could be disrupting silicon or many of the functions that used to be built into the silicon. However, exploring this line of thought could be the subject of another thesis entirely.

V. RECOGNIZE WHERE THE OVERALL INDUSTRY IS IN THE TECHNOLOGY STRATEGY THOUGHT

A. The Semiconductor S-Curve

While Moore's Law has proven itself useful as a predictor (and perhaps as a self-fulfilled prophecy) within the semiconductor industry, Nodes and MIPS (Millions of Instructions Per Second) are more instructive indicators of true progress than Moore's Law. While MIPS is very useful for processing power and speed (much more so than clock speed), it is, itself, derived from such variables as the number of transistors and clock speed. It is, therefore, more interesting to customers than it is useful for indicating true scientific progress. True scientific progress, therefore, is best measured by one variable: the 'manufacturing node' or the size of individual transistors. Since scientific advance is driven by research and development, it is instructive to examine inflation-adjusted research and development expenditures versus the manufacturing node[11]:



xxxvi

For equivalent reductions in the size of the manufacturing nodes (500 to 350, 350 to 250, 250 to 180, 180 to 130) research and development expenditures are growing significantly[12]. This indicates that the semiconductor industry is on the Tail End of the Technology S-curve. So, as past experience has proven, the industry is now scrambling

[11] Ideally, only research and development expenditures that specifically resulted in the ability or attempted to reduce the node size would be collected and used in the graph. However, it would be nearly impossible to collect and review 30 years of data for hundreds of companies and to sort all their research and development expenditures on the intent (or the result) of node reduction. For the purpose of this graph, it is assumed that 100% of the industry's research and development expenditures went into node reduction. The graph would be equally useful, assuming any fixed percentage of the research and development budget went into node Reduction. In actuality, the true data could show that the industry is spending much more or much less for any given node reduction.

[12] Note that, although the research and development expenditures between these nodes have increased dramatically, research and development expenditures between nodes in the future are likely to be more constant. This is predicted by the near-linear nature of the tail end of S-Curves.

to find alternative ways to improve performance (rather than focusing almost entirely on node reduction.) In keeping with this, the industry has begun to seriously examine or re-examine alternative materials and basic architectures. In some cases, this is referred to as "equivalent scaling" because it is an attempt to achieve increased performance (on the order of one node reduction) by means other than the traditional scaling method.

B. The Industry's state as it moves into the top portion of the S-curve

Semiconductors are mature. As the S-curve suggests, technology advances are less obvious and require more research, more experimenting, more testing, etc. In addition, the ultimate basis of competition is no longer based purely on technology and is moving toward more service-centric metrics like variety, customization, delivery time and price. [xxxvii] We also see the number of available chip designs and process techniques growing and becoming ever more specialized...moving somewhat towards mass customization instead of mass manufacturing.

As Christensen warns, the performance of semiconductor chips is outpacing the performance required by the customer (reaching performance oversupply). Although there is a lot of additional performance being demanded by hungrier and hungrier operating systems and software, people will soon find that they simply do not need most of the technology to simply read and write email or to edit documents. While certain applications, such as video and voice programs, hold the promise of really increasing the market demand for performance, but today's chips are simply overkill for most of today's applications.

All of this indicates that the technology is somewhere on the tail-end of the S-curve, that the industry is in the 'Specific Phase' and that even the most stalwart and formerly suspicious customers have even bought into the technology (Can you imagine any company not using semiconductors without a highly technical reason?). Altogether, it is a mature technology, product, process and market.

VI. UNDERSTAND YOUR COMPANY'S INDUSTRY SEGMENT AND COMPETITIVE POSITION

Although it is too sensitive to repeat specifics here, it is essential to understand how your company's market segment(s) are structured in terms of product/service offerings, how customer needs are being met and how those needs are split between all of the different vendors. A good starting place would be to find out how customers or industry research groups segment the market and to discover the revenues/ market shares for every different vendor. In addition, it is often useful to understand some of the history behind how the market came to appear as it currently might.

In this process, particular emphasis must be placed upon first understanding how your company's products meet customer needs and how they are positioned in customer minds. This special emphasis is required because any technology strategy must also take into account your greater portfolio and capabilities/ resources.

It is also necessary to look carefully at where the overall industry is and where it is going, then to take this knowledge and diligently apply it to your own company's situation and product offering. For instance, shrinking transistors have required all equipment makers to conduct research and create better machines for smaller transistors. Customers are always buying tools that can meet their changing needs and any vendor must anticipate those changing needs and then alter their research and product portfolio.

VII. IDENTIFY NEW TECHNOLOGY OPPORTUNITIES AND THREATS

A. Sustaining Innovations

There are, literally, dozens of alternative (non-node reduction focused) efforts being made to improve performance. For the most part, however, they are sustaining innovations because they are not challenging the fundamental technology or the assumptions behind the fundamental technology. Here are some of the most popular efforts and the fundamental change that each implies.

1. Material Changes

Silicon On Insulator: Semiconductor structures insulated from the rest of the wafer by a thin layer of insulating material. This reduces capacitance and leakage.
Silicon On Nothing: Semiconductor structures are insulated by not allowing them to touch anything – they are insulated by Air or vacuum, both of which have very high electrical insulation properties. This reduces capacitance and leakage.
Silicon-28: isotopically pure Silicon wafers that have a higher heat transfer rate
Stressed Silicon: artificially stressed Silicon crystals spread the crystalline structure and move the atoms further apart, resulting in higher speeds
Silicon Germanium: one form of stressed Silicon
Epi Wafers: Epi wafers are more pure and better crystallized than normal bulk wafers.
Indium Phosphide (InP): fundamentally different materials which have much better natural responses/characteristics than Silicon
Gallium Arsenide (GaAs): fundamentally different materials which have much better natural responses/characteristics than Silicon

2. Design Changes

"Brownouts": Designers are finding ways to 'turn off' entire sections of chips when they are not in use. This, in effect, 'turns off' the unnecessary power loss associated with the transistors in that section.
Multiple gate structures: Multiple gates increase the power that can flow through the circuit, resulting in higher speeds.
Multiple Voltages on Chip: Traditional chips use one voltage on all transistors. However, certain transistors do not actually need as much voltage as others. This makes them function faster than necessary, creating waste both when 'on' and when 'off'.
Clockless Chips: Traditional chips run calculations on dozens of transistors and dump the results into a register. These 'dumps' do not need to be in any particular order because of an interaction with the 'clock'. If you get rid of the clock, energy use goes down, but now signals must enter the registers in a prescribed order. This is difficult to engineer.
3D Structures: Interconnects are getting longer and longer and more and more complicated. This is because more and more connections are necessary, but we are limited to a 2D silicon space. Moving to 3D dramatically shortens the lengths, uses less energy and causes less signal distortion, but is difficult to engineer.
'Standard Components': chips are beginning to be made by selecting many different 'modules' that can each perform some specific function and together achieve an end goal.

Although the modules may not be optimized to each other, this can make more highly customized chips and improve performance.

B. Identify existing Disruptive Threats

Disruptive Technologies generally do not look like much of a threat at first, because their performance lags very far behind existing solutions. For this reason and because they often come out of completely different industries, they often blindside entire industries. With this in mind, here are a few identifiable disruptive threats:

Biological Computing: Uses biological organisms and structures to process and store data instead of semiconducting materials.
Nanotubes: Uses carbon structures to effectively create transistor-like operations.
Software: Uses more advanced software to take over many of the functions currently performed in-silico.

VIII. PICK ONE TECHNOLOGY TO THOROUGHLY INVESTIGATE

With so many technologies to choose from, it can be difficult to pick one to thoroughly investigate. It is imperative to quickly think through them and to focus, one at a time, on those technologies most relevant to your company.

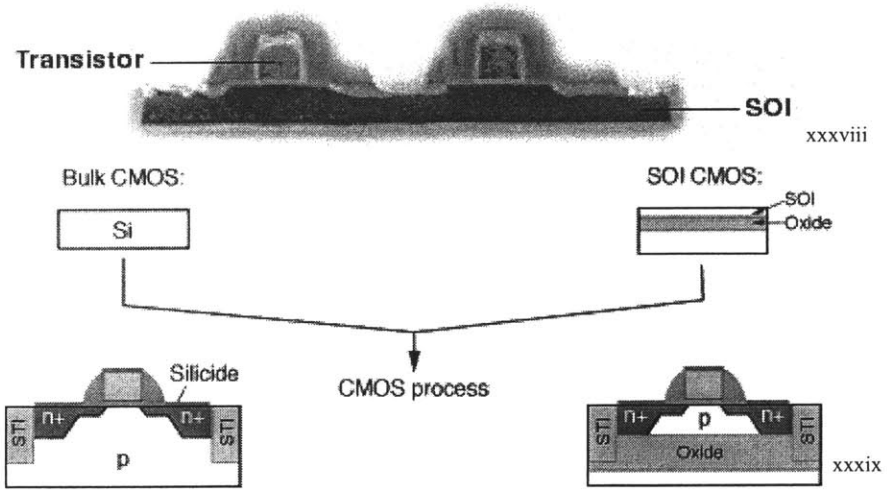
While the identified architectures, substrates and design changes are very interesting SOI largely builds on the existing installed base of semiconductor equipment, requires many of the same design skills and is relatively easy to insert into existing processes (as apposed to many of the other choices). However, since SOI is a different transistor architecture from what is currently the dominant design, certain types of processing equipment may enjoy extra demand, while others may see some decline in demand. All chip companies and equipment manufacturers must be prepared to make choices about whether to and how to participate in the SOI market.

IX. TECHNICAL REVIEW OF THE CHOSEN NEW TECHNOLOGY

A. SOI: What is it?

SOI stands for Silicon On Insulator. SOI is an architecture in which every transistor sits on top of an insulating layer (SiO_2, quartz, sapphire, etc) instead of a traditional deep well architecture (involving p or n-type implant). SOI research goes back to the late 1970s, but SOI has never really achieved large quantities. SOI, for a long time, was found almost exclusively in chips that required radiation hardness and Alpha particle resistance in space applications. Recent research and a flurry of attention have brought SOI back into the limelight.

Fundamentally, the insulating layer physically replaces the substrate immediately underneath the gates, drains and sources. As long as this insulating layer is thick enough, there is no material beneath the transistors that will significantly interact with device operation anymore; there are no carrier movements from the deep well to the gate channel and there are no carrier movements from the gate channels down into the substrate. The transistors are electrically isolated. This kind of electrical isolation has both positive and negative implications for chip performance, chip designers and process engineers that could even require changes even in the type of equipment used within the fabrication plants.



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B. SOI: What does it do?

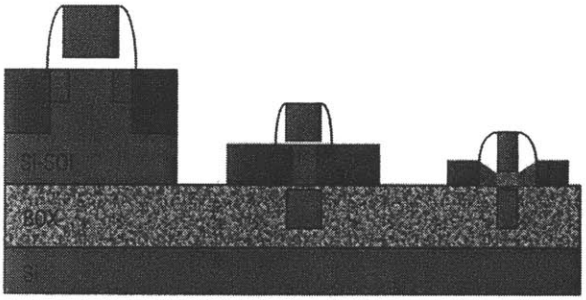
Electrically isolating the transistors is a fundamentally different architecture from the 'deep-well CMOS' that is currently popular. This creates serious differences, some positive and some negative. Generally, SOI is touted for speeding up processors and for using less energy, but lambasted for creating a number of non-linearities that complicate the circuit design. An attempt to characterize most of these differences can be found in Appendix IV.

C. SOI: different variants

1. Fully Depleted vs. Partially Depleted SOI[xl]

SOI can be built in two major ways. The first is much like CMOS on Bulk, in that the entire semiconductor is built with a layer of silicon beneath the gates, and wells. This layer is thin, certainly, but the layer is nevertheless present. The second way is to place the gates and wells directly on top of the BOX layer. These two different structures cause different performance characteristics – the second is better than the first at stopping leakage and easier to design with, while the first is easier to manufacture. Below is a chart depicting the three different structure types and their relative advantages:

	Fully Depleted	**Partially Depleted**	**Bulk**
Junction Capacitance	Small	Small	Large
Body Effect	Small	Large	Large
Floating Body Effect	Small	Large	None
Vth Control	Difficult	Easy	Easy
Subthreshold Leakage	Small[13]	Larger	Large
S/D Silicidation	Difficult	Easy	Easy
Lay-out Area	Small	Small	
Circuit Design	Easy	Difficult	
Scalability	Difficult	Easy	Difficult
Manufacturability	Difficult	Easy	



D. SOI: How is it made?

While initially glass, quartz, sapphire and others fought amongst each other, SiO_2 clearly emerged as the dominant design for SOI insulating layers in the late 1990s. With the dominant design set, attention shifted to Process Design and the pace of Process Innovation has quickened. There are now over ten processes that are competing for market share that all use SiO_2 for the insulating layer; the major processes are listed in the table below:

[13] Requires ultra-thin silicon layer for highly scaled devices.

0+ SOI	Bonded SOI Wafers	Other
Advantox MLD	SmartCut – uses H+	Epitaxial Lateral Overgrowth
Advantox	Nanocleave –uses H+	Silicon On Saphire
ITOX	ELTRAN	Oxygen Precipitation
	Laminox	

SOI is now in the 'Transitional Phase' and we expect to see one or two clear market winners among these various processes. An extensive SOI process discussion is provided in Appendix V. At this point, the two processes with the largest market share (>95%) involve O+ or H+ ions. For each of these popular processes, there are varying pros and cons; in the tables below, these pros and cons are explicitly laid out:

1. (O+ SOI)

PRO	Con
1 substrate,	All processes must be done on one wafer
Si layer uniformity,	Must be 1st process: anneal Temperatures >1300°C destroys other structures
Patterned wafers easily created	
Simple process: implant, clean, anneal (7 hrs)	
BOX integrity: low pinholes, leakage	Generally creates thinner BOX layers that are more sensitive to particles and more likely to leak
As voltages continue to lower in the future, ever thinner BOX layers/ lower O+ dosages become acceptable	Harder to make thick BOX layers

2. Wafer Bonding

PRO	Con
Wide range of BOX thickness 50-3000nm	>1 wafer/substrate
Choice of various materials: stacked together or alone	Complicated process: oxidize surface, implant, clean, anneal, split, etch, grow epi-layer, smooth, clean, bond
Different layers can be processed differently	Yields?: each of the above steps has a yield
	Epi-layer defect density: smaller geometry needs better layers
	Particles remain in interface: cause voids, shorts
	Patterned wafers difficult to create

Each of these processes has an advantage, based upon the thickness of the Silicon Layer that is desired. Below is a table describing these two types of SOI wafers:

3. Types of SOI

Type:	THICK	THIN
Top Si Layer Thickness	1000 to >5000 Å	Hundreds of Å
Voltages	Higher	Lower
Typical Applications	Bipolar, MEMS, plasma displays, discrete, analog, mixed-signal power	Digital CMOS, memory, "smart" power amplifiers, digital IC applications, radio-frequency (RF) devices in Bluetooth connections, multiplexer optical components, logic devices
Function of Oxide	Isolation only	Intimate electrical interaction between the buried oxide and device operation
Benefit	Separation from main substrate	Higher device speeds, lower power usage
Difficulties		Difficulty processing, floating body effects complicate circuit design
Special Note		Si thickness must scale with channel length

The width of the BOX layer (the SOI thickness) depends on the number of Oxygen atoms inside the Silicon wafer. O+ implantation is currently very time-consuming; as the BOX layer thickness increases, the expense and time scale up with the dosage and grow to a point where it is cheaper and more expedient to use a bonding process. On the other hand, bonding has many more process steps than O+ implant; as the BOX thickness decreases, these extra process steps do not scale down with the dose and direct O+ implant becomes cheaper and more expedient.

Thinnest SOI SIMOX Advantage | Thin SOI SIMOX and Bonding Compete | Thick SOI Bonding Advantage

Of course, both types of companies (promoting think and thin technologies) state that their process is the most cost-effective solution for a wider range of thickness than I have indicated. Below is a chart that depicts some of the major process steps for the two leading processes and my belief about whether or not that process scales with dosage:

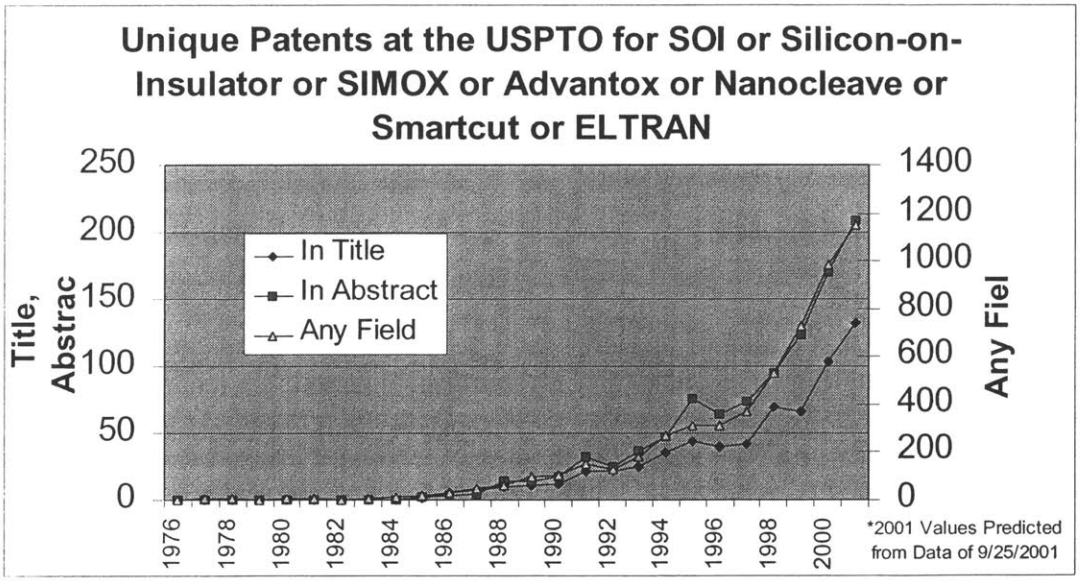
Advantox MLD Process Steps	**Scales with dose?**	**SmartCut Process Steps**	**Scales with dose?**
Clean Wafer	No	Clean 2 Wafers	No
Implant O+	Yes – Very Strongly	Grow SiO_2	Yes
Clean Wafer	No	Clean Wafer	No
Anneal	Slight	Implant H+	No

Clean Wafer	No	Clean Wafer	No
Implant O+[14]	Some	Bond Wafers	No
Clean Wafer	No	Clean Wafer	No
Anneal	Slight	Anneal Wafers	No
Clean Wafer	No	Cleave Wafers	No
		Chemical Mechanical Polish 2 Wafers	No
		Clean 2 Wafers	No

To date, customers have not indicated that one process demonstrates superior quality or performance. In fact, many processes are still in qualification at most chip companies; many customers literally have not yet chosen one type of wafer over another type, as they have not completed their evaluations.

E. SOIs' Current Status

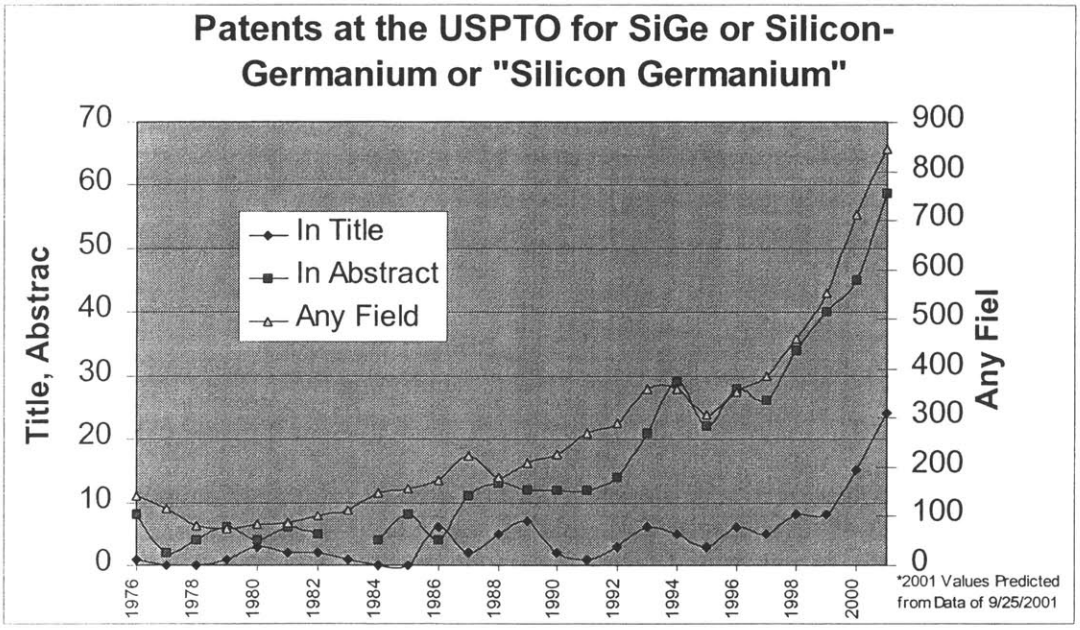
There are, literally, thousands of Patents and Research Papers devoted to SOI and SOI-related topics. Many of these are found online at the U.S. Patent Office or IEEEXplore. In the graph below, the exponential trend in the number of patents (presumably a proxy for effort and progress) is demonstrated. Many of the complications and disadvantages that once plagued SOI have been overcome by this research.



[xli]

[14] It is somewhat unconventional to require an implant, an annealing and another implant, but there is a fundamental physical reason for this. Implanted Oxygen, in silicon, will migrate to the surface and to a highly concentrated layer within the Silicon itself. This layer within the Silicon, however, will not form the insulating SiO_2 until the second implant, which acts as a catalyst to get the crystalline structure to become amorphous. This strange process had been created because it reduces by a factor of 3-4 the quantity of O+ atoms needed to create the insulating layer. This reduces implant damage to the device layer and it increases implanter throughput.

To see if this exponential trend truly means anything, it is important to compare SOI patents to the patents generated by SOIs' main competition, SiGe. SiGe's graph also demonstrates an exponential trend, however the quantity of citations in any field, the abstract or the title is quite a bit lower than those citing SOI. It is not clear from this data whether this means that SOI is favored over SiGe among researchers to become the new substrate of choice, or that SOI simply requires more research for full-scale production worthiness. It does, however, intimate that there has been more SOI research recently than SiGe research.



[xlii]

In recent years, SOI has enjoyed tremendous research activity. Most of the quality problems and design complications that prevented SOI's earlier adoption have been overcome; chipmakers can now design around SOIs' shortcomings and capitalize on SOIs' advantages. As SOI continues its' march into the high-end chip market and into other specialty niches, SOI wafer costs continue falling, SOI wafer availability increases, researchers continue to improve the technology and designers learn to handle SOI more adeptly. Qualitative discussions with many researchers hold that cost has decreased and quality has increased dramatically in recent years. SOI is finally at a stage where it could truly invade the mainstream wafer market, should the chipmakers desire this.

Despite the obvious research activity and progress concerning SOI and even if we assumed that SOI would become mainstream, there are still many questions about which SOI process or processes would win out over the others; which is the cheapest, which has the highest quality or which has the most momentum? In addition to these questions, there is still the question of the cost and the availability of SOI wafers. There are still many questions unanswered.

X. MARKET REVIEW FOR THE NEW TECHNOLOGY

A. How does SOI fit into the competitive picture?

SOI competes with SiGe, 28Si, GaAs, Epi, Perfect Bulk, H annealed Si, Clockless Chips, System on Chip (SOC), SON (Silicon on Nothing), 3D Structures and more to become the new technology of choice for higher speeds and lower power consumption[xliii] as scaling becomes more and more difficult and system performance becomes less and less limited solely by chip speed. SOI, uncharacteristic of many of these other technologies, can exist side-by-side with most of these other options. Here are three examples:

- There are several research groups actively investigating Silicon Germanium on Insulator (SiGeOI) and there are several SOI processes that involve creating an Epi layer for the active layer.
- SOI would be a natural complement to a clockless chip[15]
- SOI is perhaps the enabling process for 3D structures[16].
- Silicon-28 vendors believe that SOI is compatible with their wafers.[xliv]

B. SOI research is supported with significant resources

IBM has long been a driving force behind developing SOI. They have a long history of developing technologies and introducing them into mainstream semiconductor production:

> IBM "has wagered heavily on basic research and development in many areas, and so far it seems to have paid off, especially in chips. It was the first company to transition to copper from aluminum interconnects, and has had much success with low-k dielectrics, shallow-trench isolation and e-beams. Its success in the chip-fab technology race has left the rest of the industry gasping for air."[xlv]

Despite IBM's record of success however, it is equally important to remember their difficulties in developing X-Ray Lithography, the massive expenses incurred for that project and the lack of X-Ray Lithography machines on the market today.

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[15] One of SOI's disadvantages is that it has a floating threshold voltage, which causes a variable delay. This variation is difficult to deal with in clocked chips, as every operation must be completed with one cycle of the clock. Clockless chips, naturally, are not tied to a clock. Operations are instead tied to each other and therefore the variable timing of an SOI circuit is easier to design around is some instances. In other words, clocks are slowing chips down and using a lot of power because the entire chip must run at the speed of the slowest operation and obtain signals from the clock. Intel has placed some clockless features on their Pentium 4 and designed a Pentium-compatible test chip in 1997 that ran three times as fast on half the power as the clocked equivalent. An additional advantage of clockless chips is that they give off lower levels of electromagnetic noise, thus producing less interference; this is important for mobile devices.

[16] Each layer in a 3D structure requires electrical isolation from every other layer. SOI, especially bonded SOI, is an obvious enabling technology. Note that 3D structures reduce interconnect lengths by orders of magnitude and will greatly increase chip speed and reduce power consumption. Intel once cited that interconnect capacitance is growing more and more important every day in comparison to in-Silicon capacitance. They are right in that assertion, but while SOI does not solve this problem today, 3D structures will. So, in a sense, one can say that SOI may one day reduce interconnect capacitance as well.

Technologies have to find the right market AND work to become a success. SOI is still in this process.

C. SOI also has detractors

For several years, Intel has been SOIs' major detractor. According to a Intel study[xlvi], SOIs' performance stems from three factors, but each factor decreases with scaling and the current SOI advantage will decrease or be eliminated as line widths continue shrinking.

Several well-respected Intel scientists wrote a paper that begins by saying that SOI's performance gains are caused by three main areas/reasons. They then shoot each one of those reasons down individually. Below the three reasons are listed, along with Intel's arguments:

SOI Performance gains from:	**Intel's Argument**
Minimizing the area junction capacitance	Junction Capacitance is dramatically decreasing in importance as lower nodes are reached. Junction Capacitance Decreases as L^2 while gate capacitance decreases as L (Line Width).
Utilizing a Floating Body	SOI's Ground to Body coupling comes with a history effect[17]. The history effect is bigger when (V_G-V_T) is smaller. (The V_T of a SOI transistor changes with switching history.) This causes a variable delay as well, which is difficult to design around.
No Body Effect: SOI floats close to the sources	Bulk CMOS in stacks show a body effect, but it is diminishing as I_{OFF} increases on chips. (and I_{OFF} is presumably increasing as nodes are reduced.)

However, detractors claim that the benefits of SOI, for each of these factors, will disappear within a generation: one Intel design engineer said, "We believe the speed-up enabled by SOI reduces with scaling".[xlvii] In addition, detractors remain adamant that delays due to in-Silicon capacitance will reduce in importance compared to that from interconnect capacitance.[xlviii] Intel asserts that the 'body effect (in bulk) is diminishing as I_{OFF} increases'[xlix]. While this is a true assertion, it does not recognize that increasing I_{OFF} or allowing I_{OFF} to remain constant also increases power consumption, an unwanted effect and one ever growing in significance.

SOI believers, however, are not convinced by the detractors. One manager for a major supporter's SOI program said that some critics did not optimize their circuitry, design or process technique for SOI and instead essentially just port a bulk design over to a SOI wafer and ignore the special nature of SOI.[l] In other words, it is possible that the critics did not really give SOI a fair trial and that SOI may have more market potential that the critics assert. The large amount of research activity among SOI advocates demonstrates their commitment and beliefs.

[17] 'History Effects' describes, in essence, the phenomena wherein a circuit's characteristics change with switching history.

D. Examining Detractor Motivations

Both sides of the debate have some grain of truth within them. While the disadvantages cited are true, one must examine a detractor's behavior, motivations and needs before blindly agreeing:

- First, Intel generally follows major process changes and 'rarely ventures off the familiar semiconductor road map into emerging areas.'[li] They let others develop riskier technologies, while they go for sure things (improving bulk silicon, dopant engineering, interconnect aspect ratios, etc)[18]. Then, if a new and 'outside' technology is successful, they buy in when the technology has been fully developed and the risk is gone. When they are interested in a 'risky' technology, often times they will off-load some risk by seeking a partial equity stake in a startup or small company. For instance, Intel indicated interest in Silicon Germanium, a substrate technology that 'competes' with SOI, when it made a large investment in a company that produces these wafers. As quoted in EETimes, Intel 'has less incentive to move to a leading-edge technology like SOI if the technology doesn't have performance legs or the supporting infrastructure. Instead, the company has said it will push standard bulk silicon as far as it can go, relying on new circuit and architectural techniques to boost performance, as it has done in the past.'[lii]
- Second, Intel's business is very high-volume and they hold a lot of market power. As such, they will skirt away from anything that appears to increase costs, provides lower yields and doesn't have a well-developed supply infrastructure. The supply infrastructure is a particular sticking point: "wafer availability alone makes SOI a moot point" for Intel, said the process architecture and integration director at Intel's Hillsboro, Oregon facility.[liii] Also, a principal engineer at Intel's Circuit Research Lab said, "Who's going to make 100 million SOI wafers? Ultimately it's a business decision." [liv] Even the director of logic technology development at AMD (AMD is one of SOI's most staunch proponents) said, "SOI wafer availability is the biggest issue" facing companies with significant volumes.[lv]
- Third, *Intel said nothing about how SOI affects heat and power usage.* Their arguments centered around frequency, junction capacitance and non-linearities only; they never mention leakage reduction or power reduction. Intel's processors are famous for high power usage; they have a serious need to reduce power.

E. 'Evidence' That Intel May Be More Interested In SOI Than They Reveal

If what detractors say is true, SOI will not be state-of-the-art within a few years and, therefore, they are not interested. Upon further examination, however, Intel displays more interest in SOI than they reveal in public statements:

- Intel's 'technology research group, located at Hillsboro is taking a fresh look at SOI'[lvi]

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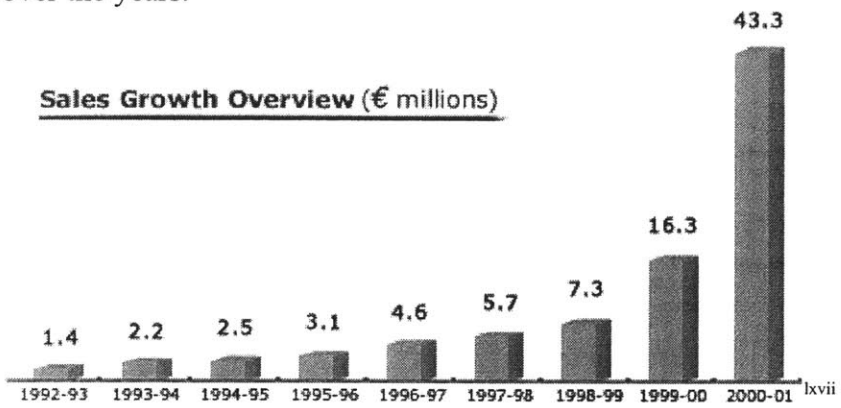
[18] During their 2001 Annual Shareholder's meeting, AMD's chairman and CEO together said, "We have been more aggressive than our competitor in adopting leading-edge processes and manufacturing innovations for PC processors, such as flip-chip packaging and copper interconnects, and we expect to be among the first to employ silicon-on-insulator (SOI) technology with our next-generation processor family." AMD Website, http://www.amd.com/us-en/Corporate/InvestorRelations/0,,51_306_2317,00.html (Retrieved 10/11/2001)

- "We are looking pretty hard at SOI right now," said a Intel strategic planning manager citing the improved junction leakage possible with SOI technology.[lvii]
- Intel has 46 patents that mention SOI and 15 patents that mention Silicon On Insulator.[lviii] Most of their early patents and papers (1999) were pessimistic, but most of their later work (2001) is more promising[lix]
- On May 8, 2000, an Intel research scientist patented a new SIMOX Process.[lx]
- On July 17,2001, this same Intel research scientist patented an IC design utilizing dynamic threshold voltage.[lxi] (Remember that dynamic threshold voltages cause the floating body effect, one of Intel's technical barriers. This barrier has been removed by this work, among others.)
- Intel's Circuit Research Lab revealed that they are investigating SOI specific circuit solutions.[lxii]
- Intel also revealed that, "Intel is investigating dual gate, vertical gate, surround gate, fin-FETs fully depleted SOI, and other promising device geometries to mitigate short channel effects associated with decreasing device dimensions."[lxiii]
- There are also some new Intel papers concerning SOI.[lxiv]
- Intel has a standing agreement to produce HP's IA-64 chip, which will be based on HP's new SOI chip.[lxv] It is not necessary for this second generation to be based on SOI, however.

F. SOI Market Review – SOI Production

1. Representative SOI Wafer Manufacturer

SOITEC came out of France's LETI science labs. They control the Smartcut process, which is the most commonly used process for making SOI wafers (~80% of the market according to SOITEC[lxvi]). Revenues have shown consistent and exponential growth over the years.



[lxvii]

SOITEC is currently constructing a new facility capable of producing 1.2 million (8 inch equivalent) wafers per year in both 200 and 300mm sizes. They predict that construction will be completed by June and they will begin moving in equipment in July of 2002.

2. Other SOI Wafer Manufacturers

There are at least nine more vendors of SOI wafers or highly targeted SOI equipment. It is important to understand what vendors are doing in the market space and how they compare to each other.

G. SOI Market Review – Complements

The semiconductor industry can rarely do anything in a vacuum. For any major change in design, multiple partners must come together and create the various systems, subsystems and interconnections that allow these complicated processes to work together in a real-world fabrication plant. Without partners and without every piece of a system available, nothing new can be implemented on a widespread basis.

There are at least 20 different vendors making these essential pieces of a successful SOI introduction. Together, they provide solutions for automated wet-bench cleaning systems, bonders, modeling analysis, extraction tools, process design, making ultra-thin double-sided polished wafers, wafer thinning, metrology equipment, clean, dry, align and bond tools, electron-beam and optical inspection systems, modules, transistor model libraries, laser ellipsometers/ reflectometers, characterization, non-invasive debugging, wafer cleaning, and wafer-inspection.

Most of this new equipment is for 300mm, with bridge capability to 200mm. This intimates that these companies are targeting new plant installations rather than replacing existing equipment. Existing equipment is notoriously difficult to displace because chipmakers only need to worry about variable costs, rather than both variable costs and Capital expenditures.

H. SOI Market Review – Customers

There is a lot of activity (at least 26 customers) within the marketplace concerning SOI wafers. All activity is still, at this point, relatively small, but could become much larger in short order.

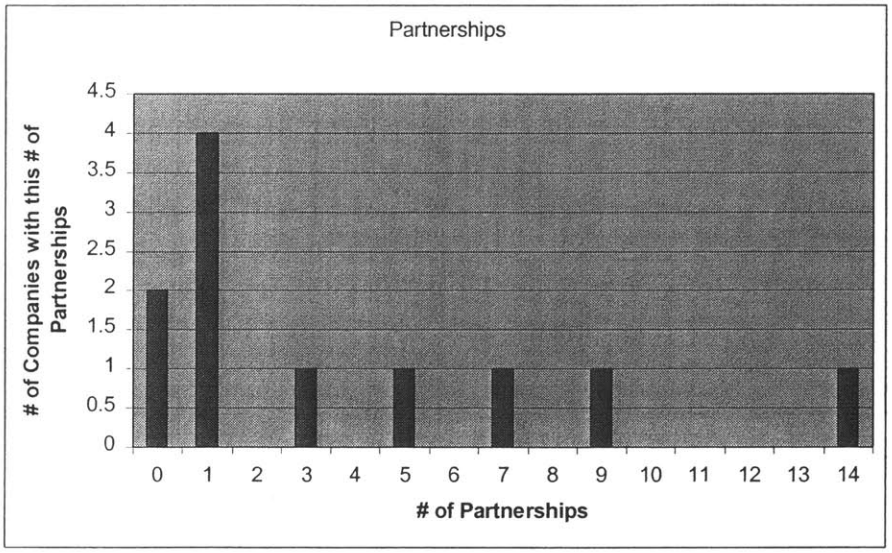
Company	Product
AMD	high-end servers CEO claimed they would use SOI in 100% of their CPUs by 2003, representing >300,000, 8" wafers/year.
Analog Devices	op-amps
Apple	X704, PowerPC
Bookham	micro-photonics, ASOC
Compaq	Alpha EV68
'Finnish Customer'	Power4, Regatta
Fujitsu	32-bit adder, ASIC CMOS
Gemplus	Smartcards
Harris Semiconductor	
Honeywell	SpacePC
HP	PA-RSOIC, PA-8700

IBM	Alpha, PowerPC, AS400, RS6000, SA85 RSOIC, DRAM, p-series, Power4, digital, RF
IBM/Sony/Toshiba	Cell processors
Intel	If Intel decides to follow AMD's lead and manufacture all of their microprocessors on SOI wafers, they would require approximately 2 million 8" equivalent wafers/year.
Kopin	small LCDs
Mitsubishi	high speed mobile apps, DRAM
Motorola	PowerPC, HiP7, Altivec G4, DRAM, mixed-signal, G5
NEC	Athlon
Peregrine	EEPROM, PLL chips
Philips	EZ-HV, amplifiers, CAN transceivers
Samsung	Alpha RSOIC
Sanyo	wireless handsets, digital boxes, cameras
Seiko Epson	Watches
Sharp	mobile equipment
Silicon Wave	BiCMOS for Bluetooth
Sun	SPARC
TI	Microprocessors, op amps
Toshiba	SoC, DRAM

For some, volume shipments were supposed to begin in 2001, others in 2002. Some (such as IBM, Sharp, Seiko Epson, Oki, Mitsubishi, Sanyo, Samsung and TI) are already using SOI wafers for a limited number of chips. Some indicate no introduction date[lxviii].

I. SOI Market Review – Collaborations

SOI is not just business as usual. It requires new skills that most companies do not have internally. Companies are joining together to drive SOI toward production worthiness. Below is a chart depicting some metadata about the partnership landscape:



J. Current Situation

To assess the current situation, as much data as possible was collected on wafer pricing, wafer quality, equipment pricing and equipment functionality.

The 2001 McLean Report has current wafer prices for several substrates and several wafer sizes. SOI wafers appear to cost about 4X the cost of Epitaxial and 7X the cost of Bulk.

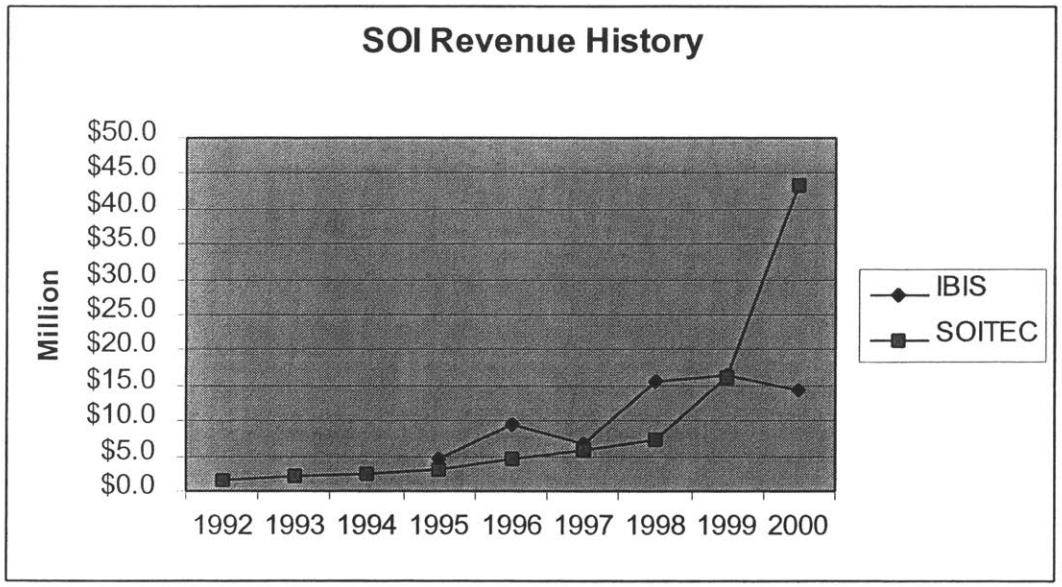
2000 Starting Wafer Costs

Wafer Size	100	125	150	200	300	mm
Bulk	16	21	29	70	450	$
Epitaxial	32	42	55	110	1000	$
SOI	75	150	210	450		$
GaAs	140		400			$
Area	79	123	177	314	707	cm^2
Bulk Cost/Area	0.20	0.17	0.16	0.22	0.64	$/cm^2
Epi Cost/Area	0.41	0.34	0.31	0.35	1.41	$/cm^2
SOI Cost/Area	0.95	1.22	1.19	1.43		$/cm^2
GaAs Cost/Area	1.78		2.26			$/cm^2

McLean Report, 2001 [lxix]

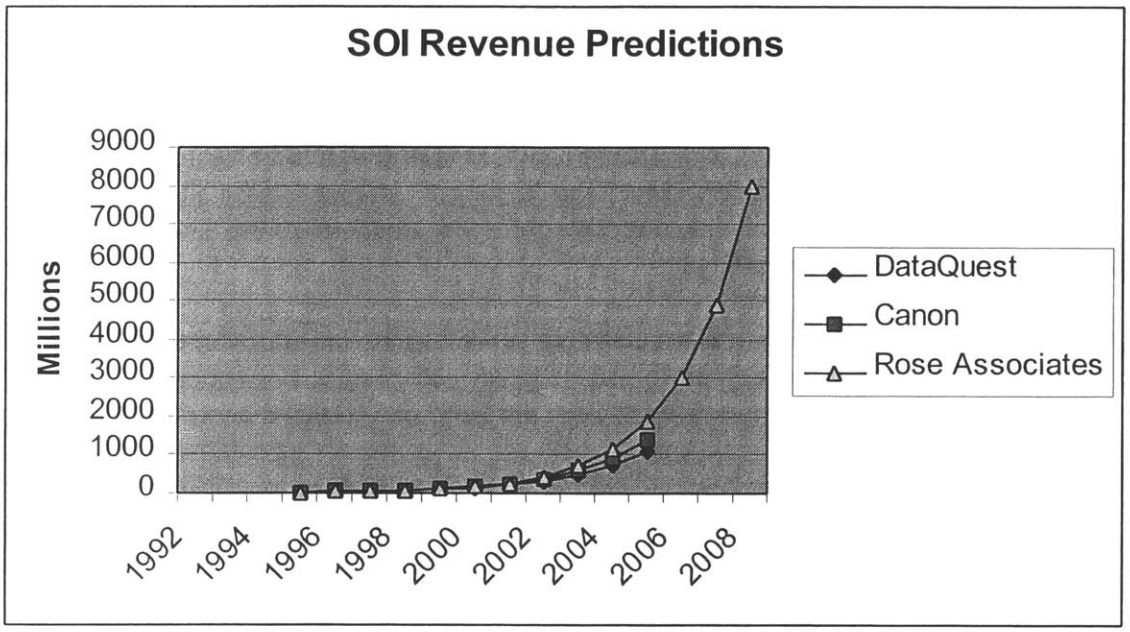
K. Market Outlook:

The market for SOI is still very young and very uncertain. Although in recent years SOI has enjoyed tremendous growth in volume and shrinkage in price, it is not clear how popular SOI will become or which process or processes will be the most popular. It is thought that much of the value in developing a SOI tool is in having the option to provide the tool, should SOI really take off. With this in mind, here is the revenue history and forward-looking forecast from Dataquest and Rose Associates:



[19]

[19] SOITEC Year End is actually March 31st.



For this case, making a prediction using the Lotka-Volterra[lxx] method would be extremely difficult. The revenue history that is available reflects high variability in the price per wafer given during different time periods and to different customers in the same time period. This immediately refutes the assumption that the coefficients in the Lotka-Volterra equations are constants. In addition, the total number of wafers supplied by any company is unknown. Given that the existing bulk wafers did not vary in price the same way and that the exact volume of wafers shipped is unknown, it is impossible to compare the penetration on a revenue basis or a volume basis.

Additionally, there were more than a dozen more technologies that were competing with SOI to become the preferred new technology for development during this time. To use the Lotka-Volterra method properly would require gathering data for each one of these technologies as well and throwing them all into a much more complicated set of algorithms.

1. H+ SOI Market

Presently, SOITEC is the leading producer of SOI wafers in the world and is rapidly expanding their facilities to accommodate the expected growing demand. A Japanese firm has already licensed SOITEC's Smart Cut process and the industry expects them to invest in more capital equipment in the future.

2. O+ SOI Market

The O+ SOI market is considerably less certain. It is not clear and has not been reported that any significant investments will be made in the coming year. This may be because the new Advantox MLD process was only recently released and test wafers are still in qualification.

L. Future Outlook for some SOI Applications

There are many niches, serviced by SOI, which have recently experienced extraordinary growth and are likely to continue growing in the future. Some of these niches include mobile processing, analog, communications, power-sensitive application, automotive, pressure sensors, MEMS, radiation-resistant devices, etc. Since SOI physically and electrically isolates circuitry, SOI is well suited to be designed into such products. In addition, SOI creates less noise, meaning better precision and better performance for mixed signal devices. Here are a few comments from industry experts about the growth of these markets:

- "The transition to 300-mm is accelerating as well as the introduction of the 0.13-micron technology for high performance integrated circuits, corresponding to a rapid increase in demand for portable and high performance systems using these devices."[lxxi]
- According to Rose Associates, Los Altos, Calif., a market research firm, the SOI market is currently at $40 million per year and growing at a compound annual growth rate (CAGR) of 40 to 50 percent. This market is projected to reach 10 percent of the silicon market by the year 2005.[lxxii]
- 'According to data from both IDC and Dataquest, the notebook market looks to outpace the desktop market with a 14 percent CAGR, moving from around 23 million units shipped in 2000 to roughly 40 million units shipped in 2004. The "sweet spot" of the market looks to be the thin and light segment, which will grow to represent over 60 percent of the notebook market by 2004.'[lxxiii]
- Analog IC Market Surged 40% in 2000, It is now a $31B market.
  - Mark Levi, marketing VP of the National Semiconductor analog division said: "(The market is booming because of) the continuing growth of digital systems that must be surrounded with analog (so they can) communicate with humans,". Such products include cell phones, PDAs, displays, sound systems, keyboards, Ethernet and DSL products, among many others. All communications systems need analog, he pointed out. There's lots of analog "stuff" in base stations.[lxxiv]
- Power management ICs also show tremendous growth due to portable devices and other products[lxxv]

M. Relative Future Advantages for Different Processes

ITRS has mapped SOI requirements through 2005:

[lxxvi]	1999	2000	2001	2002	2003	2004	2005	NOTE	Dim
Wafer Diameter	200	200	200	300	300	300	300		mm
Si Thickness Low	30	30	30	30	30	20	20	within wafer	nm
Si Thickness High	200	200	200	200	200	100	100	within wafer	nm
BOX Thickness	200	200	200	200	200	100	100	max	nm
BOX Defects (DRAM)	0.106	0.1	0.096	0.091	0.085	0.08	0.069	max	cm^{-2}
BOX Defects (MPU)	0.359	0.46	0.352	0.344	0.275	0.254	0.208	max	cm^{-2}
Inclusions (DRAM)	0.127	0.12	0.115	0.109	0.102	0.096	0.082	max	cm^{-2}
Inclusions (MPU)	0.431	0.415	0.422	0.413	0.33	0.305	0.25	max	cm^{-2}
Threading Dislocations (BOTH)	2.00E+06	2.00E+06	2.00E+06	2.00E+06	2.00E+06	2.00E+06	2.00E+06	max	cm^{-2}

One can see that both the required Si thickness and the required BOX thickness decrease by a factor of 50-67% over a five year period. (Lower device voltages do not require as thick a BOX layer and allow for a thinner silicon device layer.) With these kinds of reductions, wafer processes that will become easier or quicker along with this reduction have significant advantages over processes that will not.

In addition to these considerations, it is also important to consider how market needs may change over time. Wafer Bonding is more effective at making thick BOX layers. With wafer bonding, companies can make Thick SOI (for MEMS, Optoelectronics/ LCD-type screens, Pressure sensors, Silicon on Anything (Quartz, Sapphire, etc.), make 3D chip structures[20] more easily or put alternative materials on top of bulk (SiGe, InPb, etc. On the other hand, O+ SOI can create patterned SOI chips more directly than Wafer Bonding and with less capital expenditures or throughput disruption.

[20] 3D structures greatly reduce interconnect lengths and can use different materials on different layers (Si on layer one, SiGe on layer two, InPb on layer three, etc.)

XI. HOW SOI FITS INTO TECHNOLOGY STRATEGY THOUGHT

A. How does the technology fit into the industry?

SOI is competence enhancing for the industry as a whole. SOI expands on the industry's general knowledge of silicon, and still requires circuit modeling, ion implant, masks, CVD, RTP, test etc. It builds upon the accomplishments and the knowledge of the past, to predict the performance of a new type of transistor structure.

SOI is an architectural innovation for the industry. Compared to normal CMOS, SOI involves several fundamental differences in terms of process, design, function and in-Silicon physical structure. It is fundamentally different in a number of ways, but similar enough to remain competence enhancing.

However, SOI is a disruptive technology and technological discontinuity for some pieces of the semiconductor industry. Circuit designers, model software companies and machine OEMs can all expect some level of pain as there old skills and technologies will need great modification for SOI. Over time, DRAM makers[21], interconnect design specialists[22], new fabrication plants[23] and wafer suppliers[24] may all be disrupted by the coming of SOI.

Semiconductor design and process are so intertwined that they cannot easily be separated out from each other. In *Product Design and Development*, Ulrich and Eppinger say,

> ...process-intensive products include semiconductors, foods, chemicals, and paper. For these products, the production process places strict constraints on the properties of the product, so that the product design cannot be separated, even at the concept phase, from the production process design.[lxxvii]

SOI requires large changes in both the physical processing and the design of semiconductors. It should help to enable the continued shrinkage that has characterized the industry for decades, but it destroys some skills and some knowledge that used to be commonly used by certain industry players. For instance, design skills to fix incomplete isolation and older circuitry designs cannot be used or are no longer needed with SOI. For these reasons, SOI is both an enabling technology and a disruptive technology.

B. How does the technology help/hurt the end customer or your customers?

SOI started out primitive, costly and in price-insensitive niche markets (radiation-hardened chips and special military applications). More and more research outfits studied it and SOI grew in volume slightly as it improved on the traditional metrics of quality and price that were used to evaluate Silicon, SiGe and GaAs against each other. However, at this point, while it seems like many of the small orders are not turning into production quantities, there definitely seems to be something stirring among the key players.

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[21] Since SoC and SOI can make on-chip DRAM.

[22] Since SOI enables 3D.

[23] Since older generation fabrication plants are more competitive with newer fabrication plants if they use SOI.

[24] Since SOI circuitry is more isolated and uses less square inches.

For now, SOI chips are substitutes for normal silicon chips, replacing normal chips in high-end servers, AMD boxes and other smaller markets. In the coming years, SOI should prove to have an even greater substitute effect as 3D SOI structures and SOC with SOI[lxxviii] surpass the abilities of the older processing techniques and designs. In addition, we may see SOI equipment sales into older fabrication plants, where SOI chips will replace normal chips. However, some equipment for SOI, such as SOI modeling software, have been market-broadening.

C. How could the technology affect your company?

Depending on which SOI process becomes popular, SOI could be competence enhancing or competence destroying for any particular equipment manufacturer. While SOI is certainly not an architectural innovation for anyone but the chip companies, the market direction of SOI could require architectural innovations within any equipment company that wishes to participate.

SOI could potentially make certain equipment manufacturers a side-victim of the classical story about disruptive technologies and incumbents. Although SOI technologies are well their capabilities, some companies were not actively engaged in commercial development. But they were not developing products for very good reasons: they saw a very volatile, unproven and small market and a technology that was difficult and fraught with quality problems in the early days. As the years went by, larger machine makers continued to ignore the miniscule and confusing market. Meanwhile, wafer quality, tool quality and design capabilities were improving right under their proverbial noses.

Now that the SOI market looks like it may grow dramatically in the coming years, the larger toolmakers do not have strong product offerings that are market ready.

At this point, it may be tempting to point to the larger toolmakers and say that they should have been more aggressive with SOI. Upon further review, however, this is a hard viewpoint to support. Seeing that the greater industry is working its way into a major problem with power dissipation and heat is non-obvious for the certain toolmakers, which are a step away from this problem and have become more tuned towards just creating the science to make continued line shrinkage possible than in anticipating the side-effects of that line shrinkage and in understanding what those side effects will mean to them.

So, when the industry sees a technology, full of quality problems and lacking customers, it looks too risky in terms of both technology and market for a large company to enter. This is especially true because large companies constantly need to find big markets to solve their growth needs (entry into small markets hardly makes a dent into the overall revenue numbers for large companies). But, as Christensen writes, these 'small markets' can look pretty large and attractive to a very small company and these small companies will happily develop such tools.

In addition, large competitors and small competitors have very different internal processes and views of the world. Small companies are completely dedicated to making their products work, while large companies have the 'cushion' of their other revenue sources. When the technology or the market starts to look bad, the large competitor may

exit while the small competitor remains. Frankly, large producers find small producers underpowered, ignorable and small: somewhat akin to Dennis-the-Menace and his dog Ruff. However, small producers find large producers to be tired, over-powered, sleeping giants whom they do not want to wake up until firmly tying them down: somewhat akin to Mr. Wilson and his garden. In other words, small producers will avoid direct conflict with large producers and large producers will not see a problem until it is almost too late.

XII. GUT CHECK

A. It will probably be hard to predict the true size of the market

SOI, as we have seen, is still only in infancy when compared to bulk silicon. There is still so much to learn about SOI, so many doors that are opened by SOI and so many new ideas to try out on SOI that predicting the SOI market is a seemingly futile task. As Takashi Ogawa, Dataquest's principal SOI analyst, said about 300mm SOI wafers, "it's difficult to estimate the real demand".[lxxix] No one can accurately predict the SOI market or the SOI penetration rate - not suppliers, customers, Dataquest, Rose Associates or the author of this thesis.

B. Often times, there will be extremely divergent opinions on a new technology and on the market for the new technology

There are four camps on SOI:

1) 'SOI will always stay small, it's a niche. There is no point in re-directing resources. Don't invest!'
2) 'SOI is a mystery, though it is now a lot better in terms of quality, availability and cost... It's a good technology, but the market is small. Let's wait.'
3) 'SOI is a mystery, but very dangerous to our revenue streams. We have to invest, but we don't have to like it. Let's explore development/ mergers and acquisition.'
4) 'SOI will grow aggressively and take over vast swaths of the market, soon in CMOS and more later. Invest now, buy everybody, go big!'

Given all of these intelligent, divergent opinions, what are companies to do about SOI? The key is to carefully think about what SOI does for the chipmaker and to build scenarios.

C. Scenario Building:

If SOI remains a small player, SOI wafer demand will be weak. Existing suppliers will meet demand easily and be forced into very tight competition. Any OEM that jumped into the market under this scenario at this point would have a difficult time recouping their investment.

If SOI grows into a larger player, however, both wafer vendors and equipment suppliers will benefit from the opportunity. There may be room for additional players to enter.

Either way, however, the equipment vendors, which specialize in SOI, could eventually start selling their machines for other applications. Actually, many technology strategy classics would suggest entering a major market through a related niche market (such as SOI). In this mindset, smaller manufacturers may have held off from marketing their products in more mainstream applications this long just to increase their focus on one niche and to prevent inducing larger players' ire. If this is true, it will not last much longer; like all small competitors that are overlooked for long enough, they will start to look for larger markets in the future...mainstream markets are probably their first targets!

D. WHY SOI WILL BECOME MAINSTREAM (Make your own predictions)

1. Qualitative Assertions

As Moore's Law bravely asserts, the number of transistors on a chip rises exponentially. The line shrinkages and design techniques that have allowed this to happen have also made individual transistors quicker and less power-hungry. However, when taken as a whole, the exponential rise in the number of transistors has outpaced the power-reducing results of line shrinkage, voltage reduction and novel design techniques during that same period. This is leading to an exponential rise in the power usage of the overall chip (chiefly due to leakage currents).

Since leakage and unneeded capacitance are the main culprits of unnecessary power usage, industry must find a way to eliminate them before power draw and heat become too much of a problem. SOI has two very clear advantages:

- First, better transistor isolation is the clearest solution to sub-threshold and reverse leakage and a Buried Oxide Layer isolates better than any other substrate or technology. In addition, SOI enables dual-gate and multiple-gate transistor structures, allowing the gate voltages to be dropped. Lower gate voltages lead to lower Gate Leakage currents, without moving to high-k dielectrics for the Gate Oxide. Virtually all of the other advantages that SOI offers pale in comparison to this advantage in leakage reduction; added up, it is doubtful that all of the other advantages could drive the industry to adopt it as the new substrate standard.
- Second, the 'extra' Silicon, beneath the actual device, which electrically effects the device above, causes much of the transistor's junction capacitance. SOI effectively removes this extra Silicon and therefore removes that power loss when the transistor is turned switched. This means that the voltage delivered to the gate can be lowered, thus lowering gate leakage and power draw due to interconnect resistance[25] and interconnect capacitance hysteresis.

Since Buried Oxide layers can be introduced to virtually any of the basic wafer chemistries, it will survive if the industry (or different niches) wants to adopt anything other than silicon. However, since silicon is currently the chemistry of choice and other chemistries are not yet viable, SOI will become a mainstream technology. If other chemistries improve and industry wants to use them more, Buried Oxides will still grow in popularity as the need to prevent leakage grows increasingly important.

The only technology that challenges SOI is SON[26] (Silicon on Nothing). "Nothing" is actually air; air, of course, is a much better insulator than SiO_2 and would be a superior choice if excellent insulation were all that was needed. However, SON is still in the very early stages, has not proven itself in actual circuitry and will not be ready for some time[27]. In addition, since there is nothing underneath the channel, SON cannot be used to create certain dual-gate structures (which are on the ITRS roadmap as a needed future technology). SON's developer, Toshiba[lxxx], however claims that SON is very easy

[25] General Resistance Power Consumption= V^2/R
[26] Author's opinion.
[27] Author's opinion.

to make and to work with. If this is so, SON can ride on SOI's coattails in a predator-prey relationship, using much of the same special circuitry that was developed for SOI.

2. Quantitative predictions

While the assertions just made indicate that SOI will become a mainstream player, it is often necessary to try and frame an assertion with some measure of confidence. To do this, percentages can be placed on the 'four camps' that were for and against SOI in the earlier sections:

'Confidence'	Argument
5%	'SOI will always stay small, it's a niche. There is no point in re-directing resources. Don't invest!'
8%	'SOI is a mystery, though it is now a lot better in terms of quality, availability and cost... It's a good technology, but the market is small. Let's wait.'
30%	'SOI is a mystery, but very dangerous to our revenue streams. We have to invest, but we don't have to like it. Let's explore development/ mergers and acquisition.'
65%	'SOI will grow aggressively and take over vast swaths of the market, soon in CMOS and more later. Invest now, buy everybody, go big!'
100%	**Total**

E. Decide if your company needs to take action based on your predictions:

Obviously, the predictions just made are indicating that I believe that SOI will indeed make serious progress in the market and must be dealt with. Therefore, active involvement in the SOI market is vital for most companies, if not to aggressively grow the market or to benefit the potentially rapid growth, then just to have a measure of control over the SOI penetration rate, a market monitoring mechanism and to hedge existing revenue streams. All companies must identify and weigh their options for the SOI space.

XIII. IDENTIFY COMPANY OPTIONS AND EVALUATE ON MULTIPLE CRITERIA

A. Identify Opportunities for Your Company

The job of thinking about what your company can do is too much for one person, especially in larger organizations. To discover all of the potential actions that your company can take, many employees must be polled. This particular search included several Vice Presidents, respected senior scientists, the research manager, the engineering manager, the Chief Technology Officer and several marketing managers. By involving these people in these interviews, an exhaustive list of possible actions was created. When examined, the list reveals several main types of interest:

1 Internal developments on existing machines
2 Internal developments on brand-new machines
3 Joint developments on brand-new machines
4 Advanced research projects

B. Identify Criteria on which to Choose Your Project(s)

After identifying all of the different projects that a company might begin, those projects must be compared on specific success criteria. In the interviews mentioned earlier, many of these criteria were identified and discussed. In this case, the most important criteria were identified as:

1 Time to market
2 Probability of technical success
3 Spin-off possibilities of technologies that will be developed for this project
4 Degree of differentiation over competition
5 Internal cultural reactions to beginning and running this project
6 Capital resource needs of the project
7 Engineering or research resource needs of the project

This criteria is startling in its' internal-focus. Where are the customer needs really well included? However, many semiconductor equipment machines are extremely complex; this complexity makes it extremely difficult to predict, in advance, how well or how much better any of the concepts will perform when compared to any of the others on any particular customer-centered metric. Therefore, only the 'probability of technical success' and 'degree of differentiation over competition' are included in this example. In most other cases, getting more customer-centered metrics, based off of customer needs discovered in direct interviews, is absolutely invaluable.

C. Compare the Projects against the Criteria

Once the projects and the evaluation criteria are chosen, they can be placed in a simple two-dimensional matrix for the first rough cut. For illustration, the matrix used for this technology initially looked something like the following:

	Time to market	Technical success	Spin -offs	Differentiation	Cultural reactions	Capital resources	Human resources

Project 1							
Project 2							
Project 3							
Project 4							
Project 5							
Project 6							
Project 7							
Project 8							
…							

The matrix was filled-out by one well-informed person, but it was viewed by many others to verify its 'correctness'. As the matrix can be difficult to view, a color-coding scheme was applied over all of the fields: red for negative, yellow for neutral and green for positive. Once completed, the matrix looked like this:

	Time to market	Technical success	Spin-offs	Different-iation	Cultural reactions	Capital resources	Human resources
Project 1	Period 1	High	Few	High	Mixed	High	Low
Project 2	Period 1	High	Med	Med	Difficult	Low	Low
Project 3	Period 2	Medium	Few	Low	Hostile	Med	Med
Project 4	Period 2	Medium	Few	Low	Happy	Low	Low-med
Project 5	Period 3	Low	Very many	Very, very high	Mixed	High	High
Project 6	Period 3	Very low	Many	Med	Happy	High	High
Project 7	Period 1	High	None	Low	Happy	Low	Very low
Project 8	Period 1	High	None	Low	Happy	Low	Very low
…							

Of course, this method is really only a shadow of much more complete concept selection/ project decision methods. One particularly effect method, Stuart Pugh's Concept Selection process, is put forth in Eppinger and Ulrich's book[lxxxi]. Pugh's process is very well thought out and involves quantitative scoring of each concept against one reference concept. This can be used very well to reduce the number of concepts down very quickly in a rational, quantitative manner. Unfortunately, getting organizations to strictly follow this process is difficult. Some concepts may already be underway and the involved parties have a significant and vested interest in seeing them succeed. In addition, some concepts may hurt other projects that are already in existence. Together, these concerns can often lead to difficult political situations or can so confuse the decision-making process that this kind of rationality is often not pursued.

D. Characterization of the Projects

One interesting concept is to characterize the projects as either defensive or offensive whenever a company is faced with a technology 'hostile' to their business. With a defensive project, a company is playing 'not to lose'. With an offensive project, a company is playing 'to win'. Defensive projects tend to stick close to the corporations'

earlier products (the designs that they know will work already) while offensive projects frequently force the corporation to venture into a new, unchartered direction that might mean a vast improvement. For the projects mentioned before, most of them turn out to be defensive in nature:

Defense	Offense
Project 1	Project 5
Project 2	
Project 3	
Project 4	
Project 6	
Project 7	
Project 8	

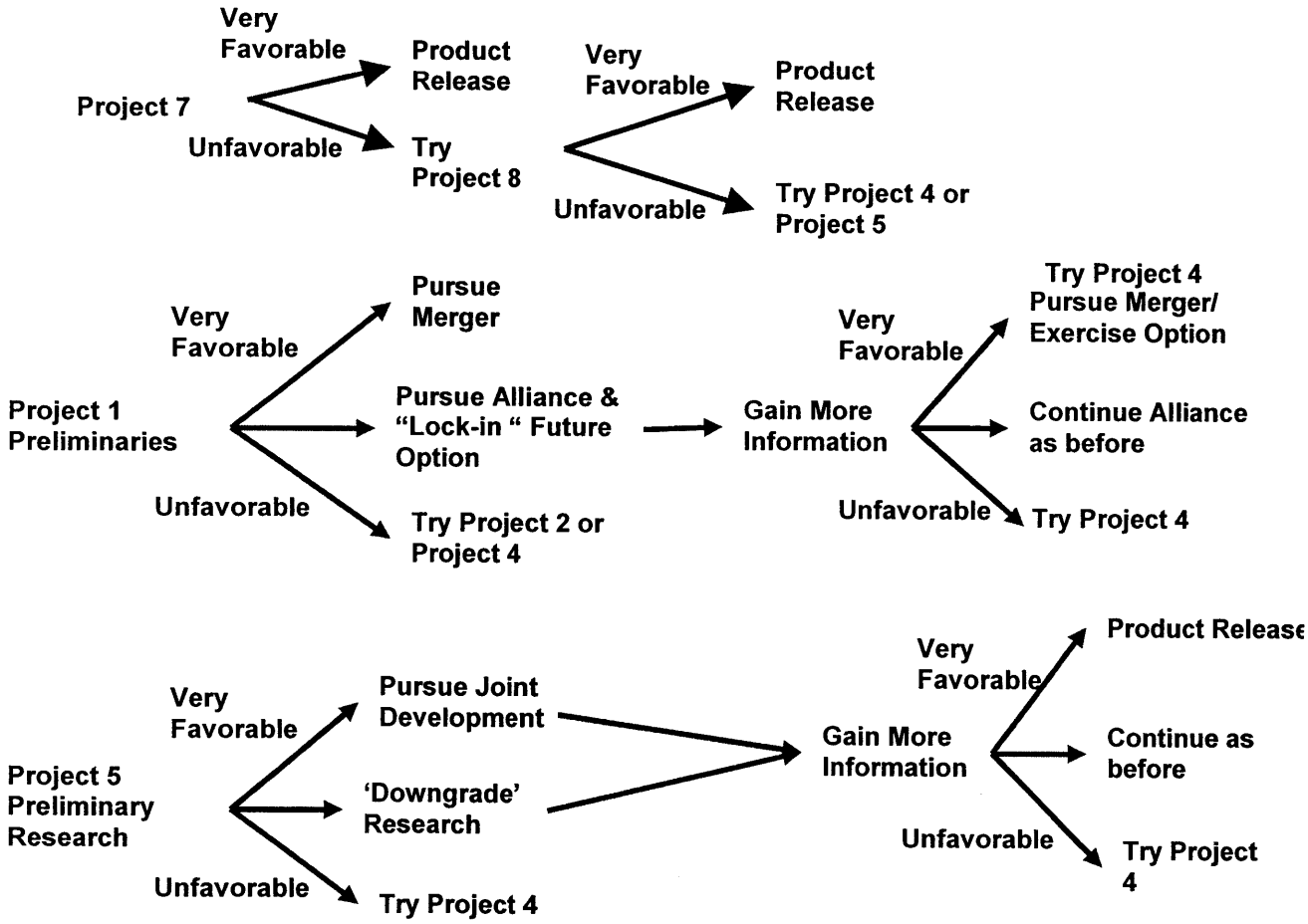
It is not surprising that defensive projects are more common than offensive projects. Because they are based upon established technologies in which the company had ample expertise, defensive projects are the obvious path to take whenever faced with a technology need.

XIV. SUGGESTED SOI STRATEGY

The strategy we created focuses on discovering, creating and using real options[28]. The company will continue down one path until such time as the technology shows that it will not work or the market shows that it will never accept SOI. The following plan was presented to upper management:

1. Continue Project 5 research and discuss a joint development program with an interested party
2. Continue Project 7 and begin the customer engagement process
3. Conduct the preliminary discussions for Project 1

Consistent with real options theory, these three actions were presented as just the beginning of a string of nested decisions and technology discoveries. This web is displayed below:



There are a number of issues concerned with company actions and the timing of announcements, developments and agreements that must be taken under consideration; the intricacies of the web above are delicate. In addition, it is important to remember that

[28] See Appendix III, Real Options.

making information public can have unexpected results! There are hundreds of intricate possibilities that could lead to unanticipated effects.

XV. BUSINESS DEVELOPMENT – Implementing the Approved Recommendations

As is always the case, once a strategy is evaluated and approved by management, it is imperative to implement that strategy. Implementation should begin immediately, so that the momentum from and interest surrounding management's approval cannot die out before any real actions are taken. To assist in this, it may be wise to build an informal support network and an excited team before hand, so that swift implementation is a real possibility.

XVI. CONTINUOUSLY MONITOR THE TECHNOLOGY AND THE MARKET

A. AMD Places an Order with SOITEC

On November 12, 2001, AMD announced a 'multi-million dollar order for 200-mm Silicon On Insulator (SOI) wafers'.[lxxxii] These wafers are being used to pilot production of AMD's Hammer processor, slated for full release in 2003H1. SOITEC mentioned that the order was the largest order ever for the company, both in the number of wafers and in revenue.[lxxxiii] SOITEC also revealed plans to add capacity for 1.2 million more 200mm wafers per year, more than doubling the current operations.

B. Intel 'Changes' Their Story

In late November 2001, Intel announced that "it will incorporate" SOI "by as early as 2005" in "a transistor with a gate length of 15nm that could take switching speeds beyond 1THz".[lxxxiv] Intel's plan, however, is to use full-depleted SOI, instead of the partially depleted SOI that other chip companies have been using.

Intel's announcement about SOI was part of a larger announcement for a new 20GHz, 15nm node, chip with 1 THz transistor switching speeds and is slated for release around 2007. This chip 'will have greater power density than a nuclear reactor'[lxxxv] and creates many problems for power consumption and heat dissipation. Using fully depleted SOI is an attempt to lower power consumption and to reduce the need for heat dissipation. SOI is 'considered a key step in reducing transistor leakage and voltages'.[lxxxvi]

Intel's director of components research said "There is no fundamental physical problem with making these transistors really small and fast. The problem is, they start to consume too much power."[lxxxvii] He went on to say that "fully depleted SOI offers better junction capacitance, lower off-state leakage, fewer soft errors, lower operating voltages and lower gate delay than the partially depleted variety." and that "it eliminates the so-called floating-body effect associated with conventional SOI, or the tendency for unwanted charge to build up in the transistor body."[lxxxviii] He also claimed that 'partially depleted SOI has a 100x higher off-state figure than fully depleted SOI' and that 'Raising the source/drain regions improves drive current 30 percent for a given voltage threshold and given geometry.'[lxxxix] Finally, he added that ""What we're saying is that fully

depleted SOI is the right answer, and we think everyone will have to do this in three to five years."

1. Wafer-makers Reactions

Most of the SOI wafer makers followed the Intel announcements with their own statements which all indicated that they were pleased by Intel's announcement and that they could make the types of wafers that Intel would need for their implementation.

2. Equipment-makers Reactions

Equipment makers that were active in SOI beforehand also issued statements indicating that their equipment could be used to make the thin-style Intel wafers. It is likely that equipment makers that were not actively involved may have decided to re-evaluate SOI.

3. Research Reactions

The research world was largely silent after Intel's announcement. However, one IBM research fellow said that even fully-depleted SOI (which is the research term for what Intel is indicating it will use) is not immune to floating body effects and that fully depleted SOI has more difficulty with short-channel effects than partially depleted SOI. [xc] In addition, he said that analog circuitry needs a body contact – impossible in fully depleted SOI.

4. Other Chip-Maker Reactions

While other chip makers were largely silent after Intel's announcement, IBM announced a few days after Intel's announcement that they had developed a double-gate transistor. Double-gate transistors carry double the current, operate at twice the speed and, amazingly, take up less room than single-gate transistors. This technology requires thin-film SOI, much like Intel's announcement about using fully depleted SOI. IBM sources suggested that the technology might be used as early as 2005.[xci]

XVII. CONCLUSION:

This thesis has reviewed some of the major approaches in technology strategy. It has also reviewed some key pieces and problems specific to the semiconductor industry and one semiconductor equipment manufacturer's competitive position within their market segment.

Several technical advances were reviewed and evaluated against the semiconductor industry's needs. Of these, one was chosen for special review because it specifically had implications for the specific market segment of an interested semiconductor equipment maker. This special review consisted of an extensive survey of technical and market literature about SOI and an extensive study of the options available to the company.

From this study, it seems that the selected technology will become ever more important and that SOI wafer volume will dramatically grow in the future. While SOI is not a disruptive technology for the semiconductor industry, it is an important sustaining technology and requires a significantly different transistor architecture. Because it is a different architecture and there have been many quality problems with SOI wafers in the past, many companies have not adopted it yet. However, AMD, seeing the advantages of SOI, came out as a vocal early adopter in mid-2001, presumably to gain an advantage over their long-time rival, Intel. They promised to put SOI into all of their chips, beginning in 2003. Similarly, Intel also came out in support of SOI in late 2001. They, however, promised to adopt SOI in 2007, much later than AMD. With these two companies on board, many other major wafer users are bound to make similar announcements. In time, even old factories and old processes may port over to SOI. Companies that can harness this technology with the appropriate strategy framework and the ability to implement this strategy will benefit by its future.

APPENDIX I: Disruptive Technologies

A. The Four Market Periods of the Attacker - Defender Model[xcii]

In the book, "Innovation: the Attackers Advantage", Richard N. Foster characterizes the market cycle for introduction of new technologies that compete with or substitute for older technologies. He separates the market cycle into four periods:

Period	Pricey niche markets	Market penetration	Near total penetration	Remaining niches filled
Speed	slow introduction, many problems	very sudden	slow	slow
Defender Characteristics	Defender overconfident, economically healthy	Defender's sales and prices sag, then collapse	Defender very economically unhealthy, driven to remaining niche markets	
Notes	While the economics appear unchanged, the relative technological performance is deteriorating	Global expansion, total cost parity		low price, special needs

Foster's work, however, is one of the first to really popularize these ideas.

B. Disruptive Technologies

In the Innovator's Dilemma, Clayton Christensen notes that sustaining technology leaders do no better than sustaining technology followers. However, disruptive technology leaders do much better than disruptive technology followers (around 30 times better or $1.9BB vs. $64.5MM in average revenues). He has this to say:

> 'no one - not us, not our customers- can know whether, how, or in what quantities a disruptive product can or will be used before they have experienced using it. Some managers, faced with such uncertainty, prefer to wait until others have defined the market. Given the powerful first-mover advantages at stake, however, managers confronting disruptive technologies need to get out of their laboratories and focus groups and directly create knowledge about new customers and new applications through discovery-driven expeditions into the marketplace.'[xciii]

Christensen has a number of very interesting things to say about disruptive technologies. In particular, he has uncovered a stereotypical storyline of how incumbents

lose to these technologies, what incumbents should think about changing in their internal processes and how to succeed when given a new/disruptive technology.

1. Why great firms fail....

Interestingly, disruptive technologies are often first developed within established, incumbent firms and can be a completely new technology, but are often a new technology architecture made from many proven pieces. Marketing personnel seek reactions from *their* current lead customers about the technology and receive negative feedback. The project gets shelved, but new companies are formed (often by existing employees) to develop the technology further.

These new companies find their markets typically through a reiterative process of trial and error, perhaps hitting on a few market niches early on. Eventually, this small competitor finds a small niche market with different performance measurements from the mainstream market. The incumbent, using Voice of Customer analysis and detailed market forecasts, continues to ignore the technology. Why is that?

Forecasts sometimes may not look promising because it appears to be a small market to a large company or because the product has a lower margin (is 'down market'). Incumbents that helped create and grew with the current dominant design are set up specifically to efficiently create that dominant design and are very good at making component-level innovations and pulling resources away from smaller projects to sustain and feed the current product offering(s). Often times, these incumbents have cost structures set up under the dominant design that may not port over to the new technology and are difficult to change. In addition, the Ultimate uses/markets for the new technology are unknowable and unforeseeable in advance.[29] The incumbent develops sustaining technologies instead.

Over time, however, the new technology improves and occasionally the needs of the mainstream market change to favor the new technology. Since new technologies often improve faster than mature technologies and often have better or higher limitations, the new technology takes a larger and larger piece of the market. Other times, the market will find that their needs are over-supplied by the incumbent technology and that the disruptive technology is perfectly adequate for their needs.

Once the new technology begins to take serious market share, the incumbent scrambles and often times improves their technology by a very large amount. Ultimately, however, the new technology overtakes the old technology and becomes the new dominant design. Incumbents, when they see that they are fighting a losing battle, belatedly jump on the bandwagon to defend their market and customer base. Often times, they pull the old prototypes off of the shelf, blow the dust off and try to make a sale. Other times, they scramble to create a completely new design. However, the new entrant's product has several more years of development behind I; the new entrant has first mover advantage, better designs and a lower cost structure. In the end, the incumbent eventually withdraws from the market or survives in a subsistent manner.

[29] The ultimate uses for Semiconductors and the markets that they enabled, were, themselves, absolutely unknowable in advance.

2. What companies need to think about....

- Firms typically have no process designed to deal with disruptive technologies – disruptive technologies are too intermittent.
- Ultimately, customers control resource allocation because companies can remain viable only by developing what will sell.
- Senior management does not see all technological ideas because lower level employees screen ideas based on their own thoughts about the industry.
- Small markets do not solve immediate big company growth needs, so they might not be pursued.
- The ultimate uses and applications for many technologies are unknowable in advance. 'Markets that do not exist can not be analyzed.' And large companies make decisions upon analyses.
- Organizations possess capabilities in their processes and values that can help or hinder their evaluation and development of new technologies.
- Technology supply may not equal market demand. 'Unattractive' product characteristics in one market or at one time may be very attractive in another market or at another time.

3. How to succeed with a new technology....

- Introduce the technology into an organization whose customers need it.
- Find and develop new markets that value the new technologies' attributes instead of making the technology perfect for the mainstream market before introduction.
- Use small organizations that can get excited over small wins.
- Use the resources of larger organizations, but not their processes or values.
- Plan to fail early and inexpensively when searching for a market. The first few markets you attempt will probably not work out. The key is to try those markets, without spending everything there and 'putting all the eggs in one basket'. Otherwise, you will lose vital resources and credibility.
- Plan for early learning, not execution
- Encourage product managers to work with this type of new technology even if there are more stable options. Do not punish them for failure.
- Do not push the market to grow.
- Do not wait for the market to grow large enough to be interesting. Note that the forecasts from 'experts' will probably be wrong.
- Do not wait for a technological breakthrough.
- Do not expect quantified information about market, financial return, revenues, costs, etc.
- Expect and develop few new technologies.
- Market risk is often a better option than competitive risk.

4. How to succeed as an Incumbent when faced with a disruptive technology

- If the organizations capabilities aren't suitable, use:
  - Acquisitions
    - Need to discover what is valuable in the target company: resources, processes or values? This effects the decision to integrate the company, let it stand alone, merge partially, etc.
      - Note: finance/merger specialists generally have a poor feel for the value of processes and values, rather they have an excellent feel for value if everything stays the same.
  - Attempt to create new capabilities internally
    - A record of spotty success, generally because there is little attention paid to processes, which are much less flexible than resources - one process can not pursue two disparate goals (for both the new and old technologies)
  - Create a spin-off organization
    - Generally good only for currently small markets or products that will require a different cost structure.
    - Requires attention from the CEO to ensure that enough resources are provided and that the spin-off has the freedom to create their own processes and values.
- consider the fit within the organization (Clark/Wheelwright)

5. How to Spot and Cultivate disruptive technologies[xciv]

- Determine whether the technology is disruptive or sustaining
  - Often engineering support, but marketing and finance opposition mark a disruptive technology.
- Define the strategic significance of the disruptive technology
  - Will the technology surpass the markets' performance needs? How quickly will the new technology improve? Asking "Will the technology surpass the performance of old technology?" is relatively unimportant.
- Locate the initial market for the disruptive technology
  - No concrete market exists when the company must make the decision to invest. Must create information instead...who customers are, what they value, etc. Experiment rapidly and inexpensively with both product and market. Do not rely on traditional channels or customers.
- Place responsibility for building a disruptive technology business in an independent organization
  - Only necessary when the profit margin is lower and the customers are different.
- Keep the disruptive organization independent
  - Avoid bringing in the independent organization when the market grows larger. This is because arguments over resources and cannibalization generally spring up.

APPENDIX II - Geoffrey Moore's Marketing-Based Process

Moore[xcv] picks up on Rogers' work and bases almost his entire book(s) upon the thought that different customer categories have different needs/personalities and therefore make their purchasing decisions on different metrics or with different processes. While I have not located any scientific studies that corroborate this assertion, this thought has enormous appeal among marketing practitioners and is currently very popular. Its popularity is why it is included here.

Both Rogers and Moore attempt to characterize each customer group. While their characterizations are extremely similar in some ways, their characterizations are often diametrically apposed as well. It may be that the disagreement between the two authors is explained away by the 30+ year difference in publishing time and the extremely different markets[30] that the two authors examine. Below is a run-down of some of the general characteristics that Moore identifies within each customer group, including volume, service requirements and the markets that they, themselves, are pursuing:

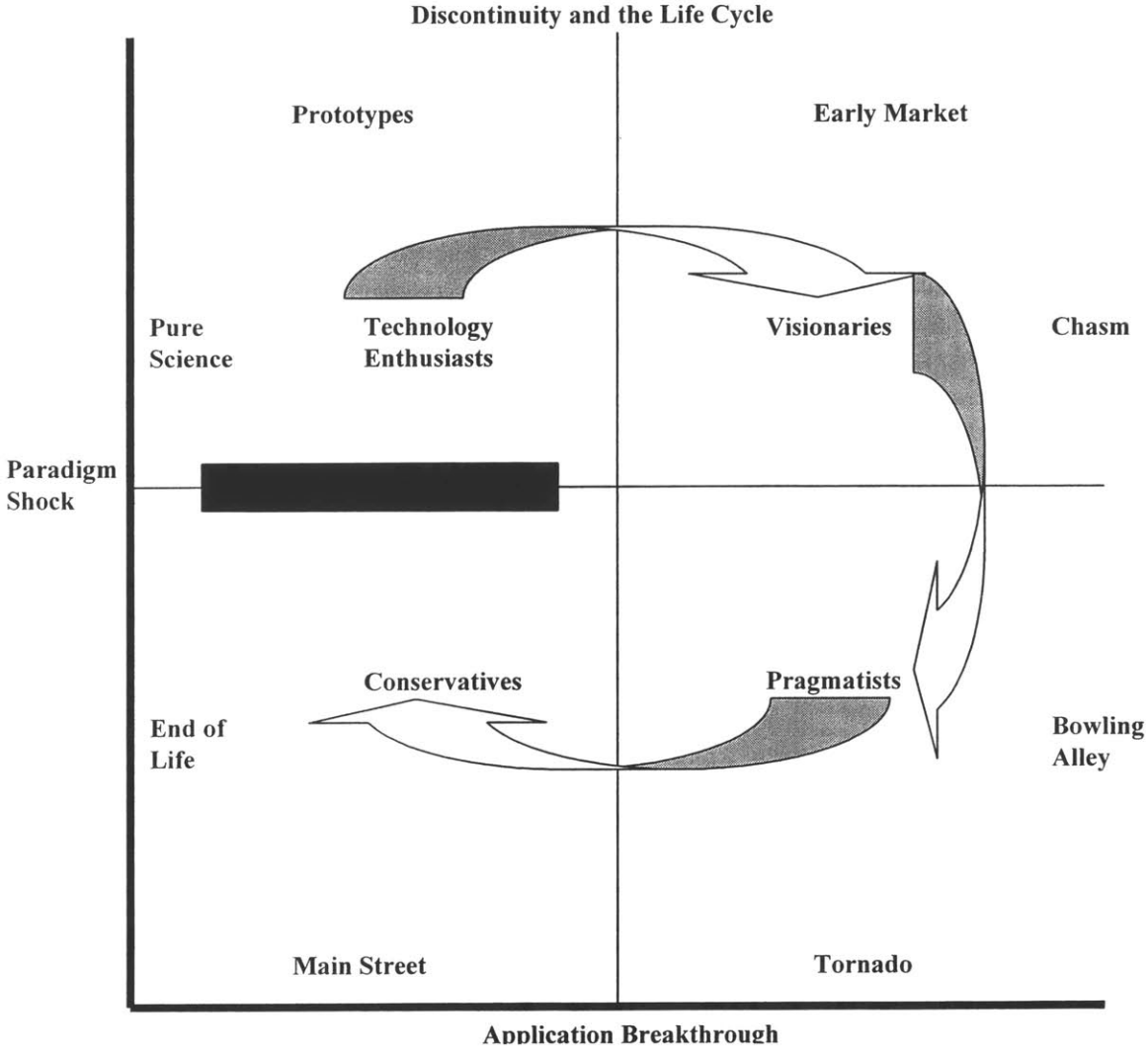
Customer Category	**Innovators**	**Early Adopters**	**"The Chasm"**	**Early Majority**	**Late Majority**	**Laggards**
"Name"	**Technology Enthusiasts**	**Visionaries**		**Pragmatists**	**Conservatives**	**Skeptics**
Customer Characteristics	customs, military, space, bleeding edge	Low volume, visionary technology lovers	The Chasm is the 'area' between the second customer type and the third. They are quite different and must be sold to differently. Third customers require references, but do not find the second customers trustworthy.	practical producers but looking for an edge over rivals	Conservative, major producers	require technology to be 'invisible'
Service Needs	put up with any problem	put up with some quirks		Require high service	require stellar service	require stellar service, if service not unnecessary
Usage of Technology (their market)	ultra-small niche markets	small niche markets, Production Runs/ Tests		mid to high volume	high volume	High volume
Volume	ultra-small	Small to lower medium		Medium to major	Major	Major
Customer Examples for Semiconductors	various research outfits, Honeywell, US Gov't	Sampling at IBM, HP, Motorolla		Small production runs at IBM, AMD	Intel	

[30] Rogers examines horticulture products, antibiotics and weed spray, while Moore focuses on computers and other high-tech equipment.

Different Customer types are often located within the same company. For instance, research divisions of Intel or IBM may act as a first or second customer while the manufacturing division acts like a fourth customer.

A. General Agreement between Different Models

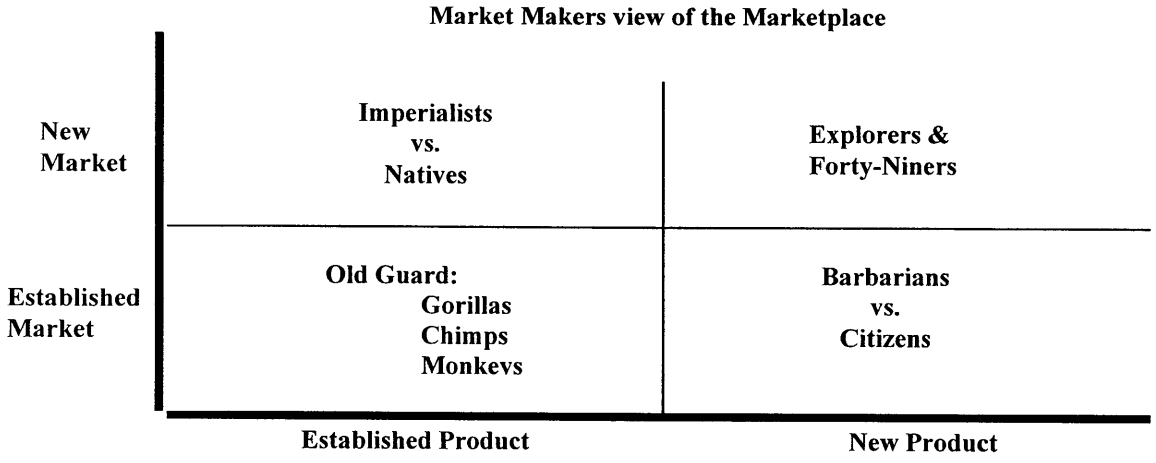
Geoffrey Moore provides a diagram that helps to talk about the market life cycle and 'discontinuities':



Notice how well the 'Paradigm Shock' Axis can map onto Christensen's idea of a disruptive technology, because what is a disruptive technology disrupting, if not for the current Paradigm? In fact, Moore suggests that 'discontinuous technologies' (as he calls them) indeed must go through this very process. Christensen's idea about making light forays into the market, searching for the initial foothold maps very well onto Moore's ideas about Visionaries and the subsequent Bowling Alley. When Christensen suggests that disruptive technologies with margins lower than established products need an

independent organization to find success, this also maps very well onto Moore's ideas about 'Margin Management' for 'Main Street' markets (and therefore Main Street suppliers). The wall between 'Main Street' and 'Prototypes' can also map onto the Christensen's belief that established companies will have a difficult time developing and marketing truly disruptive innovations.

Moore provides another diagram that also maps well to Christensen's thought. Here, firms with disruptive technologies typically begin by pursuing a New Market with their New Product, presumably an 'Explorer'. Then, when the Performance of the product improves enough, the disruptive technology enters into the Established Market and the new firm is a 'Barbarian', attacking the current 'Citizens' (companies) in that space. Moore, like Christensen, uses two vivid examples: mainframes and minicomputers, minicomputers and PCs. Eventually, if the 'Barbarians' win, they disrupt the 'Old Guard' and become the new paradigm. It would seem that Moore and Christensen are tightly linked.



B. An overview of my understanding of his process:

1) Seed a new technology to Technology Enthusiasts
2) Make the Visionaries satisfied customers
3) Survive the chasm between Visionaries and Pragmatists
4) "The Bowling Alley." Leverage your initial strength in the first niche like a 'bowling pin' to knock down nearby niches. Repeat. Become the market leader and 'standard' with the Pragmatists
5) "The Tornado." Once a 'critical mass'' of niches are cornered, the market will very suddenly adopt the product and make it the preferred standard. Commoditize the product and Just Ship; ignore end users because you are the bottleneck – providing supply is key.
6) Gain volume and experience with the Pragmatists, improving price and reliability

7) "Main Street." Hyper-tornado growth subsides. Operational excellence and customer intimacy are most important. Improve the product until the needs of Conservatives are met. Reorganize operations for +1 marketing.
8) Leave the Skeptics to discover the technology at their own pace.

It is important to note that his thoughts apply to the category of the product, not one particular offering. So, when one is applying the process or reading his work, one must always remember that he is talking about a class of products and not necessarily the product one company is offering or thinking of offering.

C. My full understanding of what Moore is saying:

1) Seed a new technology to Technology Enthusiasts
   a) Use Technology Enthusiasts as references to the Visionaries
   b) Product Leadership is most important.
2) Make the Visionaries satisfied customers
   a) Do not try to lead the Visionaries. Just follow them.
   b) Support and systems integration are essential to capture customers. Integrators and service vendors have the bulk of the market power.
   c) What happens to the product/organization?
      i) Increasingly encumbered by commitments to change the product for customers.
      ii) Service resources to change the product are depleted.
3) Survive the chasm between Visionaries and Pragmatists
   a) Pragmatists do not accept Visionaries as very good references – these groups have very different personalities.
   b) Change your product and marketing strategies.
   c) Piece together a whole product by partnering with other vendors. Hopefully, you control the 'core' product in the offering. Partner to become the market leading technology and to have a whole product.
4) "The Bowling Alley." Become the market leader and 'standard' with the Pragmatists
   a) Leverage your initial strength in the first niche like a 'bowling pin' to knock down nearby niches. Repeat.
   b) How?
      i) Need product leadership and customer intimacy.
      ii) Focus on the economic buyer and the end user; approach infrastructure buyers later
         (1) Reasons economic buyers purchase products:
            (a) Product solves a previously unsolvable and costly problem.
            (b) The problem is 'built-in' to the current industry paradigm.
            (c) The product eliminates the problem's root cause(s) and is a whole product – not just a partial solution.
            (d) Methodically demonstrate your extensive knowledge of their space to overcome their natural Pragmatist resistance.
      iii) Emphasize ROI as the compelling reason to buy.
      iv) Pursue one particular niche and differentiate on this point.

v) Partner with a value-added distribution channel to ensure customized solution delivery.
vi) Use value-based pricing to maximize profit margins.
vii) Avoid competition to gain niche market share.
viii) Position your product within vertical market segments.

c) How do you pick niches?
   i) Pick ones about your own size in terms of revenue – pick segments that are SMALL enough - not large enough - to serve your strategic need.
   ii) Pick niches with compelling reasons to buy.
   iii) Pick niches not currently well served by any competitor.
   iv) Pick niches that can be leveraged into other, similar and strategic niches.
d) Your niche-based customers become your friends, sponsors, protectors and allies during this period. They perceive you as the market leader because you are – in their niches!
e) The lead technology provider has the market power and needs to make sure that all of the partners make money early on. This is essential to attract good partners and to develop the market properly.
f) Organization?
   i) Business knowledge: need intimate customer understanding.
   ii) Need application-specific engineering for the market segment.
   iii) Recruiting: need to recruit very good people.
   iv) Revenues within set targets.
g) What not to do:
   i) Try to rush the "bowling alley' process; you must become very close to your niche customers.
   ii) Settle down in your first few niches when a tornado is possible.
   iii) Become seduced by recurrent service revenues and never simplifying the product.
   iv) Try to execute 'bowling alleys' in consumer markets

5) "The Tornado." Commoditize the product and Just Ship; ignore end users because you are the bottleneck – providing supply is key.
   a) Once a 'critical mass'' of niches are cornered, the market will very suddenly adopt the product and make it the preferred standard.
   b) Pragmatists buy what other Pragmatists buy; this becomes the dominant design and the dominant firm(s). They do not need to be courted or convinced – they just need to be supplied.
   c) Product leadership and operational excellence are most important.
   d) How?
      i) Ignore the economic buyer and the end user; focus exclusively on the infrastructure buyer.
      ii) Ignore ROI on investment. Focus on timely deployment of a reliable infrastructure.
      iii) Commoditize the whole product for general-purpose use. Drive price points ever lower to maximize market share.
      iv) Distribute through low-cost, high-volume channels to ensure maximum market exposure. Supply all channels.

v) Use competition-based pricing to maximize market share.
vi) Attack competition to gain mass-market share.
vii) Position your products horizontally as global infrastructure.

e) What not to do:
   i) Try to control the tornado. Do not act to control the supply of the technology.
   ii) Introduce discontinuity during a tornado. Only introduce if you are not winning the tornado and think you can win a future tornado with this discontinuity.
   iii) Keeping service designed in.
   iv) Bet on preventing a tornado.
   v) Remain hyper-competitive is sales, marketing or engineering. Instead, focus on capturing strategic customers and their satisfaction.

f) Design your partners out, increase product integration and margins. Service vendors lose market power.

g) Organization?
   i) Systems expertise.
   ii) Sales Management
   iii) Process Driven
   iv) New hire Orientation
   v) Cash Flow Management: accounts receivable grow very fast.

h) Competing with different market shares:
   i) The "Gorilla" has the largest market share. Just ship and capture the distribution channel. Keep updating the product to maintain product leadership and keep your competitors playing catch-up.
   ii) "Monkeys" have the smallest market shares. Ignore research and development + marketing ; clone the Gorilla product. Consider niche 'Bowling Alley' marketing.
   iii) "Chimps" have medium market shares. The market has decided on the "Gorilla" – do not try to beat it. Adopt a 'Bowling Alley' strategy to differentiate your product; you will lose sales at first, but capture some valuable niche markets for "Main Street". This will work against the Gorilla's later +1 Marketing strategy.

6) Gain volume and experience with the Pragmatists, improving price and reliability
7) "Main Street." Hyper-tornado growth subsides. Improve the product until the needs of Conservatives are met. Reorganize operations for +1 marketing.
   a) Operational excellence and customer intimacy are most important.
   b) How?
      i) Sell to the end user.
      ii) Focus on the end user's experience of the product, seeking to gratify their individual needs.
      iii) Differentiate the commoditized whole product with +1 campaigns targeted at specific niches.
      iv) Continue to distribute through the same channels, but now focus on merchandising to communicate +1 marketing messages.
         (1) How? ...Make an offer of value. Learn from results. Correct mistakes. Make another offer.

v) Celebrate +1 value propositions to gain margins above the low-cost clone.
vi) Compete against your own low-cost offering to gain margin share.
vii) Position yourself in niche markets, based on the individual preferences of the end users.

c) Mature products should be aware of disruptive innovations.
d) Product vendors lose market power to the distribution channel. Need to find new ways to the customer.
e) Organization?
   i) Convenience engineering
   ii) Marketing communications
   iii) Staff development
   iv) Margin management
f) Competing with different market shares:
   i) Gorillas provide both low-cost and +1 marketed premium offerings.
   ii) Monkeys provide low-cost clone offerings.
   iii) Chimps provide +1 marketed premium offerings.

8) Leave the Skeptics to discover the technology at their own pace.

APPENDIX III - Real Options Strategies

In a vacuum, any investment in highly variable situations seems highly risky, with potential for both high losses and high gains. When faced with this state of affairs, it is easy to 'freeze' and effectively not make a real decision or to 'shrink back' into doing what the company already does very well for their current customers. However, this often proves to be the worst action that can be taken. What is to be done about this situation? It seems that any decision is a dangerous decision.

Careful real options approaches effectively let companies participate in the technology, without placing the company in a position to completely fail. Fundamentally, companies can find and create ways in which they 'test the waters' for a new market or technology before they 'jump in head-first'; companies can move in increments. In other words, 'investments can be made as a series of deliberately staged and sequenced options.'[xcvi] Each stage allows the owner to gain a little more information about the technology and/or the market. Each stage provides a bit more technology or market information that can be used in some other product. The new information can then be used to make more informed decisions, effectively increasing the success rate and profitability.

Real options are where uncertain markets or technologies meet with financial constructs such as Net Present Value and Discounted Cash Flow. Occasionally, Net Present Value techniques show that a project is not profitable, where real options will show that it is profitable.[xcvii] What real options thought recognizes is that many projects have hidden decision points inside of them and that the decisions made at these points can make or break the project.

For instance, the decision to build or not to build a new plant will depend heavily upon the expected price of the product. This price probably has a distribution associated with it, say a 33% chance each that the product will sell for 25$, 35$ or 45$. If the product costs 35$ to make, there is no expected profit under Net Present Value and the plant will not be built. Under real options, however, one recognizes that the firm does not have to produce if the price is 25$ or 35$, thus increasing the value of the plant and increasing the chance of building it. Real options basically says, 'spend a little money now, giving yourself capabilities, information or resources which you can use in the future to make a lot more money.' Unless the money is spent today, the company will not be properly positioned in the future when the market or the technology is more ready and revealed. Real options are often what companies are using (consciously or unconsciously) when they pursue research and development.[xcviii]

Strangely, real options appear more valuable if the project shows greater variability in outcomes. This is particularly interesting because traditional thought inside large companies typically shies away from projects that have great variability in outcomes; people get fired for making incorrect choices. In real options, the general thought is that 'downsides' can be controlled and limited, so that great variability can be actively skewed towards favorable outcomes. Happily, once the realization sets in that returns can be skewed upward, innovative technologies and products that have very variable outcomes can show themselves to be profitable.

Often times, however, there is no good way to decide on values to use or probabilities to assign when using a real options framework. In these cases, most companies rely entirely upon the 'feelings' and 'intrinsic experience' of their people. This method has both good and bad points – good if their people are smart, experienced and lucky and bad if they are foolish, inexperienced or are not lucky. It can often make decision-makers (often numbers oriented) nervous to make million-dollar investments into inexact and indefinable 'feelings'.

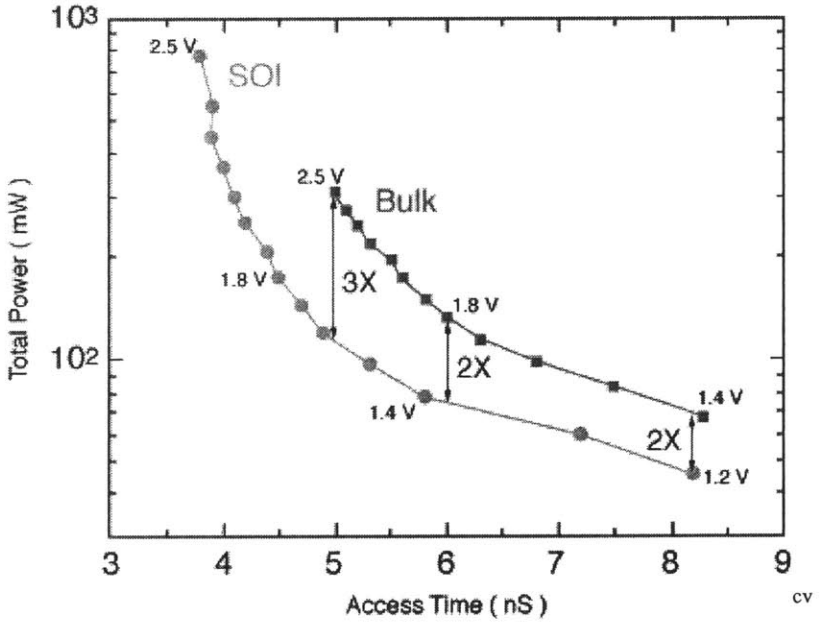
One way of dealing with this uncertainty (or to turn up new ideas) is to use STAR analysis, developed at Wharton's Snider Entrepreneurial Research Center.[xcix] Their STAR© methodology guides the user through a series of questions that helps in defining and reasoning through such hard-to-define situations.

APPENDIX IV: SOI Differences

A. SOI lowers:

- leakage
- latch-up
- signal threshold
- processing steps (up to 30%)[c],[ci]
- damage to Si surface
- susceptibility to cosmic rays[cii]
- plasma-induced charging damage
- necessary doses for sources and drains
- power requirements (up to 80%)[ciii]
- overall cost of tooling??
- re-entry flow??
- material/ chemical costs???
- power supply or battery sizes
- switching speed (due to lower capacitance)
- voltages (due to lower capacitance)
- need to move to next generation (equivalent scaling)
- parasitic capacitance (insulating layer replaces latticed Si)
- chip size (Can be reduced by as much as 50%)[civ] (due to better isolation)
- need to cool chips/ size & expense of heat sinks – fans, coolers??

IBM demonstrates the Power-Reducing capabilities of SOI on a 4Mb SRAM :



cv

B. SOI raises:

- chip speed
- power into substrate
- allowable operating temperature[cvi]
- drain current (floating body charging brings more carriers and dynamically lowers Vt) [cvii]
- allowable chip operating temperature (350° C, ~100° C higher than bulk[cviii])
- battery life
- "soft error" upset immunity

- packing density[cix]: transistors/area, circuit area[cx], chips/wafer[cxi]
  - 'A problem with bulk semiconductor logic circuits is that a relatively large amount of surface area is needed for the electrical isolation of the various FETs which is undesirable for the current industry goals for size reduction.' [cxii]

C. SOI involves complications:

- Cost of the wafers is higher
- Wafer volumes available are 'too small' to really supply the market
- stress-induced silicon defects
- pinholes in the buried oxide
- self heating, lower thermal conductance[cxiii], poor heat removal (SiO_2 has a much lower thermal conductivity than latticed Si: ~1.4 W/m°C versus ~150 W/m°C) [cxiv]
- high occurrence of lattice defects resulting from extremely high Ion Doses
- long annealing times are required to heal the lattice damage: reduces throughput and makes the SOI film thickness difficult to control[cxv]
- changing threshold voltage causes variable delay
- complex channel hot electron degradation
- design inexperience[31]: Product managers are "very conservative," said Ted Houston, a researcher at Texas Instruments Inc. "Before they will take a chance on a new material, a lot must be proven."[cxvi]
  - "there is an enormous economic design investment in modem VLSI integrated circuit (IC) products. Typically, standard *SOI* does not behave the same way as bulk CMOS because of the dielectric isolation, and bulk CMOS designs are thus generally not compatible with, or readily transferable to an *SOI* architecture. Product groups must decide whether to re-design circuits for *SOI* CMOS, even when the circuit functions adequately using bulk CMOS, especially since the fabrication facilities will not try to run any new technology without a baseline." [cxvii]
- floating body effects: gates surrounded by isolation regions
  - As they are dynamically or statically charged, LaPotin showed, the body voltage changes the threshold voltage, which in turn impacts performance and may cause a variable delay.
    LaPotin also noted that floating bodies cause pattern-dependent delays, which could cause problems in static timing analysis with respect to sensitization of inputs. Putting things in perspective, however, he noted that SOI might impact delay by 10 percent, which is less than the impact caused by many other factors. [cxviii]

[31] Design experience is essential to make use of SOI because semiconductor processes are highly linked to design: 'Examples of process-intensive products include semiconductors, foods, chemicals, and paper. For these products, the production process places strict constraints on the properties of the product, so that the product design cannot be separated, even at the concept phase, from the production process design.' Eppinger, Steven and Ulrich, Karl. Product Design and Development. New York: McGraw-Hill Companies Inc., 2000.

- 'cause pattern-dependent delays, which could cause problems in static timing analysis with respect to sensitization of inputs'
- 'charge trapping and interface state generation can occur at the gate oxide silicon interface and the buried oxide silicon interface'[cxix]
- there are a number of companies which are not supporting SOI yet or are actively 'denouncing' it publicly
- Other substrates (Bulk, SiGe, GaAs) keep getting better and cheaper
- Other substrates performance are better at smaller nodes

D. **Future SOI uses/ advantages – Technical Viewpoint**

The potential for many new technologies are unforeseen in advance. It is only through research and development that the technology is studied, characterized and put to its' most effective use. The invention of the semiconductor is a perfect example: no one could have predicted all of the uses and products that the semiconductor has made possible. The list below illustrates this thought along with some of SOIs' potential future uses:

- 'The future of the technology is open-ended, beginning with the obvious promises of improved power and performance, but including more subtle advantages and reaching to new, as yet unimagined structures in silicon.'[cxx] -Ron Wilson, EETimes
- 'In the near future, customers are likely to find the introduction of SOI to be almost transparent. The differences between SOI and bulk CMOS will be hidden inside ASIC libraries, with the ASIC vendor stepping in to do some custom work when something really needs to be different above the circuit level. But as SOI matures, the IBMers predicted, changes will start to surface even for logic designers. New tools will emerge, new techniques will be preferred, and, eventually, some rather revolutionary possibilities will exist.'[cxxi]
- pass-gate instead of conventional logic[cxxii]
- very large programmable logic arrays
- System-on-a-Chip (SoC)
  - ...IBM "researchers from the Semiconductor Research and Development Center (Hopewell Junction) will describe the process methodology and initial results of using 0.1-micron Silicon On Insulator logic technology to produce an 8-nanosecond 0.31-micron2 embedded-DRAM cell on pattern SOI wafer for SoC applications. One key issue facing pattern SOIs, which are made by blocking out specific areas of standard p-type silicon wafers, is whether defect-free bulk regions can be created in small areas.
    Early results indicate that eDRAM yield and retention characteristics are comparable to bulk SOI with initial retention fails occurring at 128 milliseconds. The researchers said this work paves the way for integrating eDRAM in an SOI-based technology and makes SoC applications in SOI feasible." [cxxiii]
- on-chip DRAM:
  - "In embedded DRAM, if you use a thick SOI layer you may have good signal and thermal isolation from logic,"[cxxiv]
  - 'Further in the future, IBM is intent on moving its trench-capacitor DRAM technology to SOI.'[cxxv]

- dynamic-threshold MOSFET structures
  - "The floating-body effect allows a more flexible design effort"[cxxvi]
  - 'big gains in device performance are possible by dynamically controlling the body voltage — and hence the threshold voltage — of transistors. This change by itself will result in library elements with significantly better performance than would be possible even with conventional fixed-threshold MOSFETs on an SOI wafer.'[cxxvii]
  - "We have been doing first-generation SOI designs, using basically CMOS design work moved to new libraries. Now we are entering the second generation, where we move from conventional MOSFETs to dynamic-threshold MOSFET structures."[cxxviii]
  - "To create the 1T cell, the team stripped the DRAM of its capacitor and exploited the floating body effect of SOI, long considered a drawback of the technology, Fazan said. The resulting 0.04 micron2 cell is half the size of a standard one-transistor, one-capacitor (1T-1C) cell, and bypasses the scaling problems of sub-100-nanometer technology DRAMs that were predicted by the International Technology Roadmap for Semiconductors (ITRS). By removing the capacitor, Fazan said, DRAM scaling could be equivalent to transistor scaling."[cxxix]
  - "Jean-Pierre Colinge, a professor at the department of electrical and computer engineering at the University of California at Davis, outlined a new "π" gate MOSFET he has built that use what he called a "virtual" back gate to form something like a four gate device.
    Researchers are pressing to develop practical multiple-gate MOSFETs that boost current while keeping the drain's electric fields from encroaching on the channel region. The more the gate surrounds the channel region, the better the shielding. While quadruple gates are difficult to fabricate, the "π" gate, which has two side gates buried 10 nanometers into the oxide, performs nearly as well as a "real" quadruple gate, Colinge said.
    "A triple-gate is easy, but etched a little bit into the oxide for the two side gates, and the extensions give you extra field lines from the drain to give you a virtual fourth gate," he told EE Times." [cxxx]
- 3-D SOI/ multistory ICs/ stacking
  - SOI is an essential enabling technology for 3-D structures.[32]
  - 3D SOI chips are already fabricated in the lab:
    - 'The 3-D, 4-bit multiplier had half the interconnect length, slightly less than half the normalized power per device and nearly 75% smaller footprint of comparable 2-D CMOS circuits."[cxxxi]
- SOI analog circuitry
  - takes full advantage of the availability of variable-threshold transistors
  - some techniques were already used on the SRAM cache for PowerPC chips.
- "Due to the isolation between circuits: elimination of guard rings, easier handling of RF on a mixed-signal die, and, startlingly, much better techniques for dealing with electrostatic discharge resistance."[cxxxii]
- 'Old tools find new life'

[32] 3D SOI decreases interconnect lengths from microns to less than tenths of microns, increasing speed and decreasing resistance/ capacitance, while reducing circuit footprint

- SOI is worth a lot to a chipmaker if it can delay next-generation capital expenditures by one or two years… SOI not be state-of-the-art, but it competes!
- IBM, AMD, less-advanced fabrication plants (China, India, etc.) need not purchase more expensive lithographic tools to achieve performance boosts normally gained by shrinking line widths.
- Semiconductor tooling is very long-lived. Most of the world chip-market is still making 0.35um and 0.25 um chips. Why scrap these tools if SOI can make them competitive again? All they need are designs, processes and SOI equipment to compete with products at smaller geometries without SOI.

Taken out logically, many of these advances can lead to dramatic cost or performance enhancement over traditional architectures. For instance, if the claim that SOI transistors need 50% less space[cxxxiii] than normal transistors is true, then the chips per wafer will double, which could lead to some new and very interesting industry dynamics.

Another logical progression concerns the fact that SOI chips use less power and can run at higher temperatures. Seeing that many SOI chips go into servers and that many servers typically make up 'server farms', it may be in the future that 'server farms' require less cooling. As a result, future 'server farms' could possible purchase and run smaller and less expensive cooling equipment or locate in hotter areas with cheaper land costs. As Richard Doherty, an analyst for Envisioneering Group in Seaford, N.Y., said, "Server rooms emit a lot of heat. For every 100 W of heat produced by CPUs you need 100 W of air conditioning to cool the heat down. So if your processor is more powerful but emits 100 W, enterprises need money for utility bills."[cxxxiv] Indeed, IBM is pursuing SOI, partially because of the energy savings: 'IBM's thin client server lines driven by a processor to be launched later this month that an IBM spokesperson said would consume 1/10 the wattage compared to competing low-power processors.'[cxxxv]

A third logical progression centers on SOI's performance benefits. SOI chips on a feature node one behind normal chips on the cutting-edge feature node perform similarly. Chipmakers can potentially switch to an SOI product rather than upgrade their capital equipment to handle the next node.

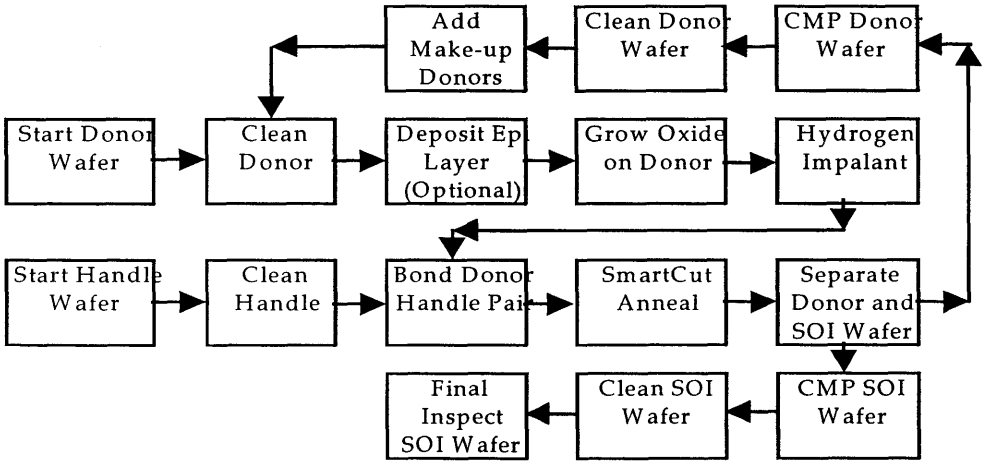
APPENDIX V: SOI Processes

A. SOI PROCESSES – Wafer Bonding

1. SMARTCUT (UNIBOND)

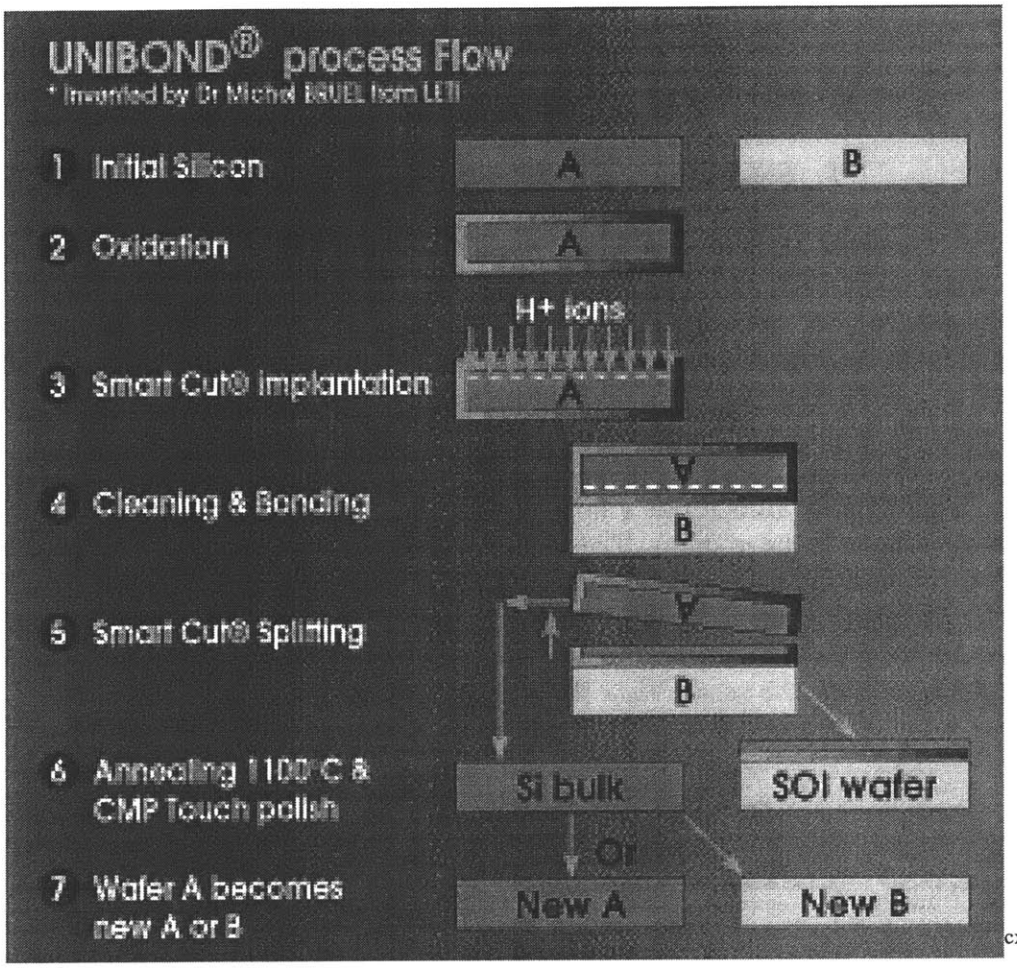
Presently, this is the leading process to make a SOI wafer. It was invented by and is owned by SOITEC, a French company associated with LETI. In this process, ~$6e^6$ hydrogen ions/cm^2 are implanted though a surface oxide and into the wafer. The energy depends on the desired thickness of surface silicon. In general, energies below 80keV are used for advanced devices like microprocessors and energies significantly above 80keV are used for high power bipolar devices or for MEMS devices.

This "donor wafer" is annealed to form a plane of 'hydrogen bubbles' and bonded to a 'handle wafer' (this forms a single wafer, 2X normal thickness, with an oxide and hydrogen layer in the middle). The 'donor wafer' is then cleaved along the hydrogen plane, forming a slightly thicker SOI wafer and a slightly thinner donor wafer. The surface silicon thickness currently ranges from 1000 Å to 1.5 μm, and the buried oxide layer from 1000 Å to 3 μm. Donor wafers are currently 'recycled' three times before they can no longer be used. View the process diagram:



[33]

[33] Diagram generated from reading process descriptions.

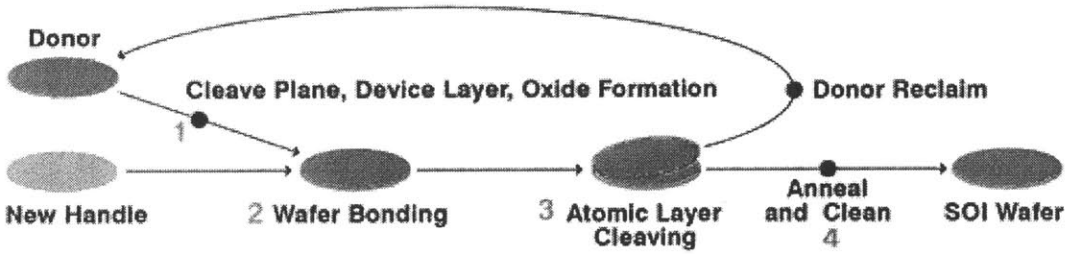


[cxxxvi]

2. Ion Immersion

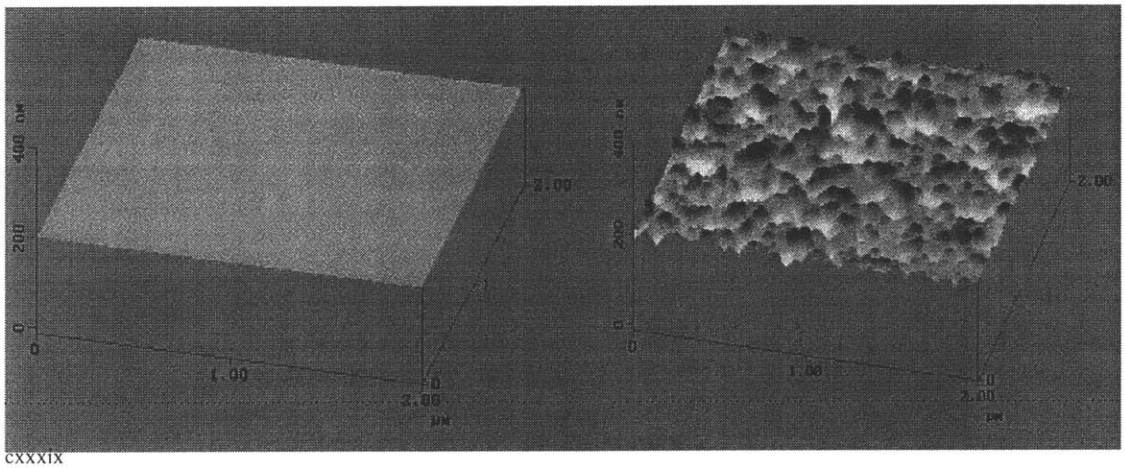
Donor wafers are placed into a plasma chamber and are rapidly charged. The correct voltage attracts the positively charged Hydrogen ions and the ions are implanted to the appropriate depth. This donor wafer is then permanently bonded to a 'handle' wafer. One unfortunate side effect of this process is that there is significant reverse current (electron flow) from the wafer to the plasma source – which causes a number of other problems.

The donor wafer's Hydrogen molecules 'clump' together and form a plane of 'bubbles'. The donor wafer is brought to near-room temperature and cleaved along this plane of Hydrogen bubbles, leaving behind a very smooth Si surface (near the 1-Angstrom level, 10-100 times smoother than competing separation methods), a Si layer 300 Angstroms to 2 microns thick and a BOX layer 1000Angstroms to 1 micron thick[cxxxvii]. View the process diagram:



cxxxviii

This process requires 40% fewer steps than competing wafer bonding processes and that no additional polishing, edge smoothing or damage removal steps are required, reducing complexity and producing cost savings between 50 and 70%. Note the smoothness of the as-cleaved surface on the left side of the picture below:


cxxxix

At the time of the writing of this thesis, there is some uncertainty around the intellectual property rights for the ion immersion process.

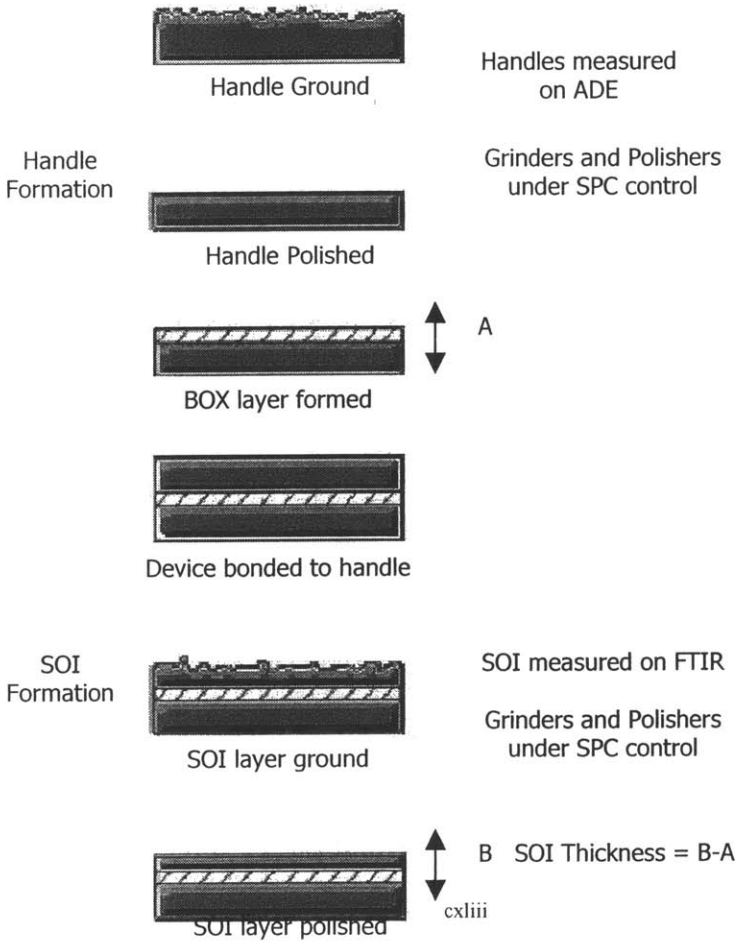
3. Epitaxial Layer Transfer

SOI-Epi wafers are made from highly selective etching and hydrogen annealing with no polishing. The SOI layer is formed by the epitaxial method and CVD to avoid defects resulting from crystal-originated pits or particles. The insulating layer is formed in a portion of the epitaxial grown silicon layer using thermal oxidation. The wafer is then bonded to a handle wafer and split at the SiO_2 – Bulk SOI interface using a water-jet[cxl], forming a SOI wafer and a thin bulk wafer. The new SOI wafer is smoothed using Hydrogen Annealing completed and the bulk wafer is recycled for another cycle of Epi growth, bond and split. [cxli]

The wafer's layer uniformity can be controlled within 1.6nm, and a wide variety of SOI and insulating thicknesses can be created. They have also demonstrated low inclusion densities, even in thin-film SOI. The wafers are available up to 300 mm in diameter.[cxlii]

4. Bonding and Grind Back SOI

This is similar to SMARTCUT or ion immersion, but without an implantation step. This process is workable, but uses more raw materials than the two processes just mentioned.



[cxliii]

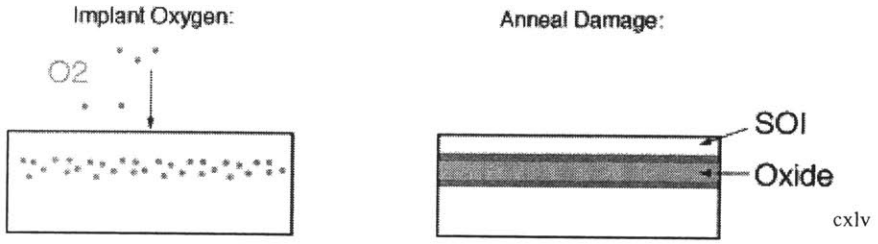
5. Bonding and Etch Back SOI

This process is extremely similar to Bond and Grind, but they use and chemical etch instead of the grind. There are no known companies marketing this process.

B. SOI PROCESSES – SIMOX (Separation by the IMplantation of OXygen)

1. Full-Dose SIMOX

Full-Dose SIMOX consists of a high-dose Oxygen implant (~$3e^{18}$), during which the wafer is kept at ~600°C, and a six-hour[cxliv] high temperature anneal. Although keeping the wafer at a high temperature helps, high-dosage implants create many disruptions and lattice disturbances that must be corrected before further wafer processing. The high-temperature anneal attempts to heal the lattice, but often has not resulted in adequate quality in years past. View the general process below:



cxlv

2. ITOX (Internal Thermal OXidation)[cxlvi]

ITOX consists of a low-dose implant, a high temperature anneal and high temperature oxidation. ITOX was a major advance because the low-dose implant ($3e^{17}$ to $4.5e^{17}$ cm^{-2})[cxlvii] was faster and created less lattice disruptions and caused less damage than in the full-dose process. In addition, the high temperature anneal was shortened in time (because there was less lattice damage). The low-dose, however, was not enough to produce the necessary BOX layer. High temperature oxidation takes advantage of Oxygen's natural proclivity to migrate out of the Silicon lattice and towards damaged or surface regions and results in a uniform, continuous BOX layer (more uniform and more continuous than full-dose SIMOX). ITOX significantly increased the productivity of the process and at the same time greatly improved SOI wafer quality. ITOX has proceeded through several cycles of improvement, where the BOX layer became thinner and thinner.

IBM's newest process is called Advantox MLD or Modified Low Dose; the process is very similar to ITOX. The process begins with a high-dose introduction of O+ ions, but not actually enough to form a SiO_2 layer. The wafer is then removed from the implanter and annealed at high temperature, in an Oxygen-rich atmosphere; during this annealing, additional Oxygen molecules migrate toward the region of highest damage (the average depth of the new ions) and the surface. After annealing, however, the SiO_2 layer is still not formed yet. The wafer then receives a medium-dose introduction of O+ ions, at which point the SiO_2 layer begins to form. Another annealing step completes the SiO_2 layer formation. Altogether, this process requires significantly less time in some pieces of capital equipment.

C. SOI PROCESSES – Other

1. BOX Layer Formation by Oxygen Precipitation at Implantation Damage of Light Ions[cxlviii]

While technically not a 'SIMOX' process, this is extremely similar to ITOX. Japanese researchers at NEC recently invented this unique procedure that is, essentially, the same as ITOX, except that H+ or He+ ions are implanted into the wafer rather than O+ ions. These 'light ions' are easier to accelerate and could be easier to generate than O+ ions. The wafer is then annealed to repair implant damage and goes through high-temperature oxidation. Oxygen molecules diffuse into the wafer during annealing and concentrate within the layer of light-ion concentration; obviously, to create a satisfactory BOX layer, the time within this oxidation process must be longer because there are no Oxygen atoms already present within the lattice.

2. Si-28 SOI

Silicon-28 (isotopically pure) wafers were identified earlier as a technology to evaluate. Here we see an interesting combination of an isotopically pure active silicon layer and the electrical isolation of the SOI layer.

APPENDIX VI: A Warning about Acquisitions

Acquisitions can fail in one of two ways: market/technological failure or poor execution/strategic thought. The first of these types of failure may not have been preventable; acquisitions often times are not ultimately satisfactory either because the technology gets replaced, the technology does not work, the market never arrives in the expected size or the market chooses another solution. The second of these types of failure is more interesting because it is more preventable.

A common source of preventable failure is accepting a bankers' analysis without conducting independent strategic thought. To acquire, without well-thought out reasoning or a plan, will usually result in a case of buyers' remorse, long after the people who 'did the deal' are long gone. Michael Lewis, an investment banker turned popular author, wrote:

> There are those who would have you think that a great deal of thought and wisdom is invested in each take-over. Not so. Wall Street's take-over salesmen...spend far more time plotting strategy than they do wondering if they should do the deals. They basically assume that anything that enables them to get rich must also be good for the world.[cxlix]

The second preventable failure is unwittingly destroying the value of an acquired company. Clayton Christensen strongly notes that acquisitions must be performed differently, based upon whether the company's true value lies in their processes and values or their resources. If the value lies in the processes and values, he suggests allowing the acquisition to stand more or less alone. If, on the other hand, the value lies in the resources, he suggests that integration make more sense.[cl]

Keeping these different sources of failure in mind, any potential acquisition/ partnership requires thorough due diligence and private, strategic meditation before companies take action. This process is absolutely necessary to ensure a successful arrangement.

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