High Mobility Strained Si/SiGe Heterostructure MOSFETs: Channel Engineering and Virtual Substrate Optimization

by

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B.S. Materials Science and Engineering
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Submitted to the Department of Materials Science and Engineering
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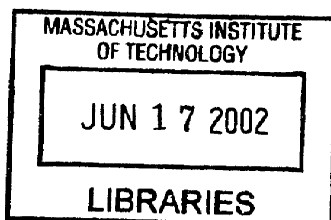
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ABSTRACT

High quality relaxed silicon-germanium graded buffers are an important platform for monolithic integration of high speed heterostructure field-effect transistors and III-V-based optoelectronics onto silicon substrates. In this thesis, dislocation dynamics in compositionally graded SiGe layers are explored and mobility enhancements in strained Si/SiGe metal-oxide-semiconductor field-effect transistors (MOSFETs) are evaluated. These results demonstrate the dramatic increases in microelectronics performance and functionality that can be obtained through use of the relaxed SiGe integration platform.

By extending and modifying a model for dislocation glide kinetics in graded buffers to SiGe/Si, a complete picture of strain relaxation in SiGe graded buffers emerges. To investigate dislocation glide kinetics in these structures, a series of identical samples graded to 30% Ge have been grown at temperatures between 650°C and 900°C on (001)-, (001) offcut 6° towards an in-plane <110>-, and (001) offcut 6° towards an in-plane <100>-oriented Si substrates. The evolution of field threading dislocation density (TDD) with growth temperature in the on-axis samples indicates that dislocation nucleation and glide kinetics together control dislocation density in graded buffers. The TDD of samples grown on offcut substrates exhibits a more complicated temperature dependence, due to their reduced tendency towards dislocation pile-up formation at low temperature and dislocation reduction reactions at high temperature. Finally, by evaluating field threading dislocation density and dislocation pile-up density in a wide variety of SiGe graded buffers, a correlation between dislocation pile-up formation and increases in field threading dislocation density emerges.

Record mobility strained Si p-MOSFETs have been fabricated on relaxed 40% Ge virtual substrates. Hole mobility enhancements saturate at virtual substrate compositions of 40% Ge and above, with mobility enhancements over twice that of co-processed bulk Si devices. In contrast, hole mobility in strained Si p-MOSFETs displays no strong dependence on strained layer thickness. These results indicate that strain is the primary variable in determining hole mobility in strained Si p-MOSFETs and that symmetric electron and hole mobility enhancements in strained Si MOSFETs can be obtained for virtual substrate compositions beyond 35% Ge.

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The effect of alloy scattering on carrier mobility in tensile strained SiGe surface channel MOSFETs is measured directly for the first time. Electron mobility is degraded much more severely than hole mobility in these heterostructures, in agreement with theoretical predictions.

Dual channel heterostructures, which consist of the combination of buried compressively strained $Si_{1-y}Ge_y$ buried channels and tensile strained Si surface channels, grown on relaxed $Si_{1-x}Ge_x$ virtual substrates, are explored in detail for the first time. Hole mobilities exceeding 700 cm^2/V-s have been achieved by combining tensile strained Si surface channels and compressively strained 80% Ge buried channels grown on relaxed 50% Ge virtual substrates. This layer sequence exhibits nearly symmetric electron and hole mobilities, both enhanced relative to bulk Si. Though channel composition plays a more important role than strain in determining hole mobility in dual channel heterostructures, significant hole mobility enhancements can be obtained even in low-Ge-content buried channels, despite the effects of alloy scattering. Finally, the best high-field hole mobility enhancements are obtained for structures with thin Si surface layers, whereby the hole is forced into the high mobility strained $Si_{1-y}Ge_y$ buried channel. Overall, dual channel heterostructures display excellent promise for high mobility n- and p-MOSFETs and demonstrate the incredible performance improvements available through heterostructure MOSFET channel engineering.

Thesis Supervisor: Eugene A. Fitzgerald
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represents a different technology node for SiGe-based CMOS, where increased performance is balanced with increased integration complexity. The strained Si on relaxed $Si_{0.8}Ge_{0.2}$ curve has been adapted from Currie *et al.*[50] while the Ge dual channel heterostructure curve has been adapted from Lee *et al.*[105]

List of Tables

Acknowledgements

Wow, this part is fun. It's not just that graduate school, and its numerous frustrations, is nearly complete (though that helps). Anyone who knows me understands that I found graduate school immensely difficult at times. So I can only hope that I've been as good a friend and colleague to the people listed here as they've been to me, since I wouldn't be here without them.

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Chapter 1.   Introduction and Background

1.1. Motivation

The rapid increase in silicon-based CMOS speed and functionality, and the concomitant drop in cost per device over the past several decades, has been the result of aggressive scaling of chip components to ever smaller dimensions. This scaling results in improved metal-oxide-semiconductor field-effect transistor (MOSFET) performance and increased integration density and functionality. Consequently, this has allowed complementary MOSFET (CMOS) manufacturing to reach such economies of scale that there are now over 60 million transistors for every person on earth.[1] However, through a convergence of various physical and economic factors, device scaling will eventually halt, putting an end to the incredible pace of CMOS performance advancements. As scaling approaches its inevitable end, interest in alternate high performance materials and technologies is intensifying. One approach to overcoming the limits of device scaling is to replace silicon microelectronics with a completely different technology. Another approach is to increase the performance and functionality of the silicon platform through integration of new materials onto Si substrates, while retaining compatibility with mainstream silicon device fabrication modules. Since the former approach is far less technologically mature than mainstream Si technology, and since there is immense economic pressure to utilize the existing multi-billion dollar Si fab infrastructure, for the foreseeable future the traditional Si scaling roadmap will be extended by integrating new high performance materials on the Si platform.

Before discussing the advantages over Si of alternate materials, it is important to emphasize the reasons for the ascension of Si to its current dominant status in the microelectronics industry. The importance of silicon's high quality native oxide (which

enables high quality MOS gate formation) and mechanical stability (which enables growth of large area substrates) cannot be overstated—without these attributes, modern microelectronics as we know it would not exist. However, Si has some inherently poor material properties that limit its device applications. First and foremost, Si has an indirect bandgap, which precludes efficient light emission. When compared to other common semiconductors, Si also has relatively low carrier mobilities, which is one factor which limits MOSFET speed. Similarly, hole mobility in bulk Si is over two times lower than electron mobility, which forces circuit designers to make *p*-MOSFETs larger than *n*-MOSFETs to obtain the same current drive. This takes up valuable chip real estate and decreases overall circuit speed. Integrating other semiconductor materials onto Si substrates offers the promise of overcoming these limitations while maintaining the inherent economic advantages of the Si platform.

There are two approaches to integration of dissimilar materials on the Si platform: hybrid and monolithic integration. These approaches are illustrated schematically in Figure 1.1 below.
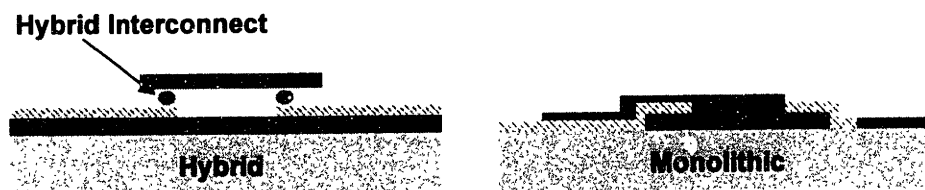
Figure 1.1 Schematic of hybrid versus monolithic integration techniques. The hybrid scheme (pictured on the left) involves integration of single components while the monolithic scheme (pictured on the right) utilizes film growth and/or wafer bonding and patterning to enable very-large-scale integration of dissimilar materials onto a common substrate.

The hybrid approach generally involves bonding or soldering of discrete components onto Si chips, while the monolithic approach involves integration of dissimilar materials onto the wafer surface through either wafer bonding or thin film deposition. Since hybrid

integration involves picking and placing of individual components, it is inherently more costly and less reliable than monolithic integration. Furthermore, in practice hybrid integration is impossible for very large scale integrated (VLSI) systems, since the sheer number of discrete components is overwhelming. In contrast, monolithically integrated films are by definition self-aligned and compatible with standard VLSI processing techniques.

Figure 1.2 illustrates lattice constant versus bandgap for common semiconductor materials. Of particular interest for this work are the SiGe and AlGaAs alloys.
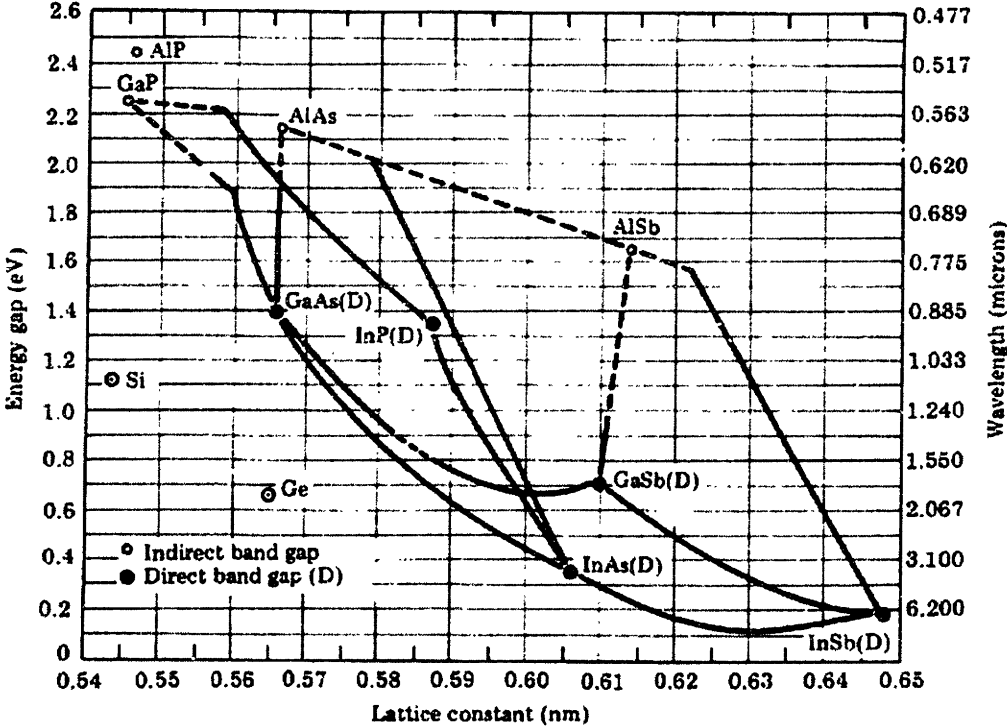
Figure 1.2 Bandgap versus lattice constant for common semiconductor materials. Figure adapted from Mayer and Lau.[2]

As will be described below, the main barrier to monolithic integration of these materials on Si is the large lattice mismatch between the device material and the Si substrate.

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1.2.   The Relaxed SiGe Integration Platform

The silicon-germanium (SiGe) materials system possesses several attractive

properties that make it a natural choice for extending the performance of the Si

microelectronics platform.[3,4] High mobility strained Si and SiGe layers offer the

potential for greatly increased MOSFET performance over bulk Si at the same gate

length, while maintaining compatibility with mainstream CMOS processing. Ge-rich

alloys are nearly lattice-matched to GaAs and AlAs, enabling integration of high quality

III-V light emitting devices with SiGe-based CMOS. SiGe layers display excellent etch-

stop properties,[5,6] making them attractive for microelectromechanical systems (MEMS)

fabrication. Moreover, as the binary phase diagram in Figure 1.3 indicates, silicon and

germanium are completely miscible over the entire composition range.
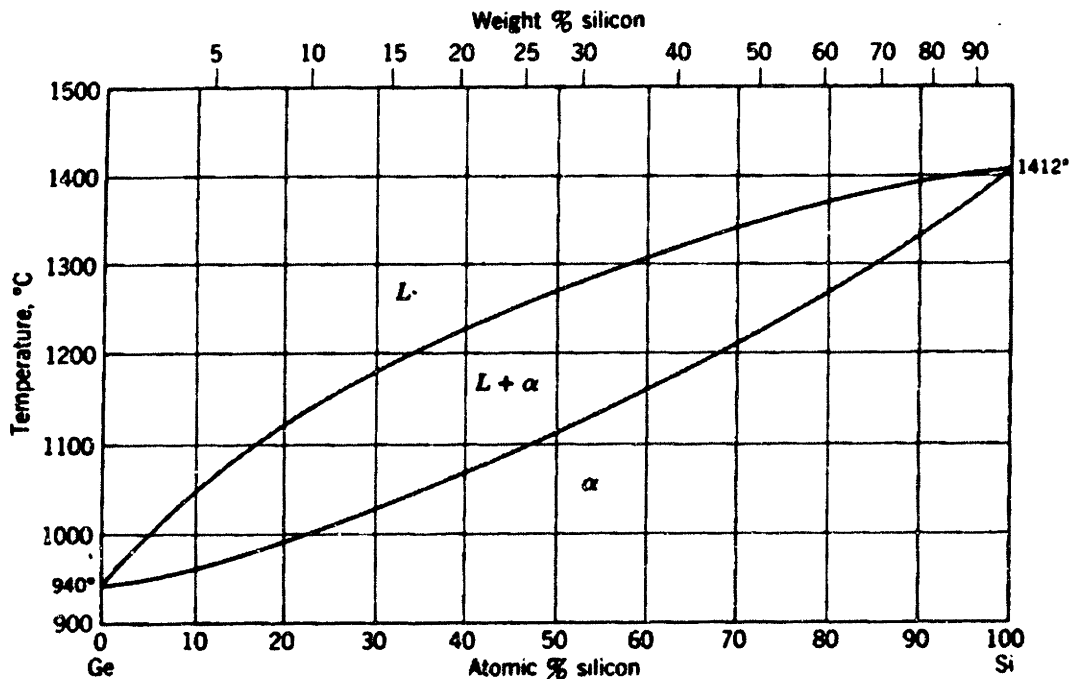
**Figure 1.3 The Si-Ge Binary Phase Diagram, adapted from Gandhi.[7] Si and Ge are
completely miscible, enabling SiGe films of arbitrary composition to be grown
without phase segregation.**

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While this makes bulk growth of compositionally uniform SiGe crystals difficult, it does mean that SiGe films grown on Si are immune to phase segregation. Finally, through the compositional grading technique discussed below, high quality SiGe layers of any composition can be grown upon Si substrates.

1.3. Lattice Mismatch and Critical Thickness

Accessing the improved functionality offered by silicon-germanium alloys requires relaxed films with a low defect density.[8] However, because of the lattice mismatch between silicon (a = 5.431 Å) and germanium (a = 5.658 Å), direct deposition of SiGe onto a silicon substrate will not fulfill these requirements simultaneously. At small film thickness, the energy required for dislocations to be present and relieve mismatch strain is less than the strain energy accumulated in the film. As a result, the SiGe layer grows pseudomorphically, with an in-plane lattice constant equal to that of the Si substrate. At large film thickness, the strain energy in the film exceeds the energy necessary for dislocations to be present, leading to dislocation formation.[9] This situation is depicted in Figure 1.4 below.
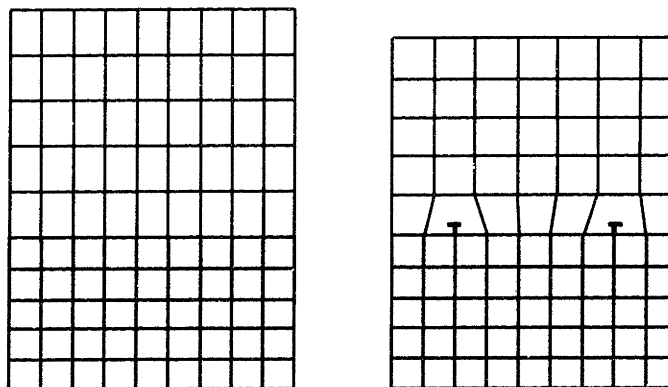
Figure 1.4 Schematic of pseudmorphic growth and the onset of dislocation formation in lattice-mismatched heteroepitaxy. Initially, the in-plane film lattice constant is constrained to that of the substrate, as shown on the left. Above a critical thickness, dislocation formation becomes energetically favorable and the film relaxes, as shown on the right.

The thickness at which it becomes thermodynamically favorable to nucleate misfit dislocations is termed the critical thickness. It is an *equilibrium* parameter; metastable structures that are dislocation-free well past the critical thickness can be grown at reduced temperatures (where dislocation nucleation is kinetically suppressed). The equilibrium critical thickness, h_c, for a lattice-mismatched layer is given by

$$h_c = \frac{D\left(1 - \nu\cos^2\alpha\right)\left(b/b_{\text{eff}}\right)\left[\ln\left(h_c/b\right) + 1\right]}{2Yf}$$

where D is the average shear modulus at the interface, ν is Poisson's ratio, α is the angle between the dislocation line direction and Burgers vector b, b_{eff} is the interfacial component of the Burgers vector, h is the film thickness, Y is the Young's modulus of the film, and f is the mismatch between film and substrate.[10]

The lattice constant of a relaxed SiGe layer is given very nearly by Vegard's Law[11,12]

$$a_{\text{SiGe}} = a_{\text{Si}}(1 - x) + a_{\text{Ge}}(x)$$

for a given Ge atomic fraction (x). The lattice constants for Si and Ge are 5.431 Å and 5.658 Å, respectively. By interpolating elastic constants, calculating mismatch for $\text{Si}_{1-x}\text{Ge}_x$ layers grown on Si substrates, and assuming $b_{\text{eff}} = a/2$ (discussed below), the equilibrium critical thickness for $\text{Si}_{1-x}\text{Ge}_x$ layers grown on Si can be computed, as given in Figure 1.5 below. Note that for large Ge content (>15% Ge) the equilibrium critical thickness is on the order of only hundreds of angstroms (Å).
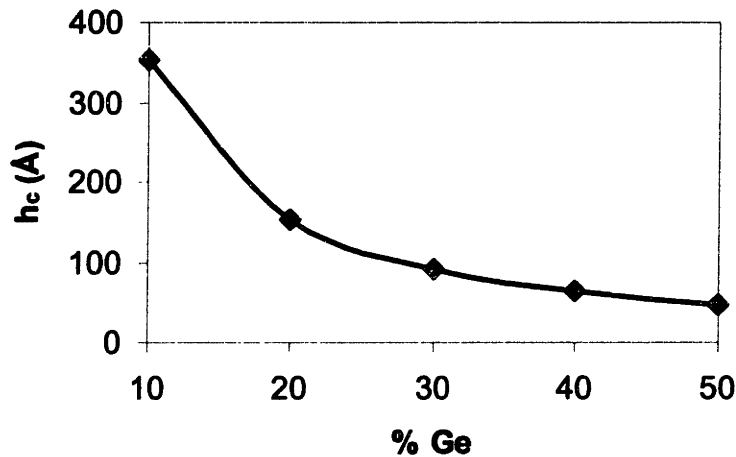
Figure 1.5 Critical thickness (h_c) of $Si_{1-x}Ge_x$ alloys on Si (001) versus Ge content (x). Critical thickness drops rapidly with increasing lattice mismatch.

The exact mechanisms of dislocation nucleation are not well understood.[10]

Theoretical calculations indicate that there is a large barrier to homogeneous dislocation nucleation, so the dominant dislocation nucleation paths in lattice-mismatched epitaxy are likely heterogeneous. A detailed discussion of possible dislocation nucleation mechanisms in mismatched epitaxy has been presented by Fitzgerald.[10]

In lattice-mismatched epitaxial systems, dislocations that glide along the heterointerface to relieve mismatch strain are termed misfit dislocations. However, since these dislocations cannot terminate in the crystal and must glide long distances to reach the wafer edge, they eventually bend upward and thread their way through the film to reach the film surface. These threading dislocations are in general deleterious for device applications; they scatter carriers, serve as non-radiative recombination centers in direct bandgap semiconductors, and are fast diffusion paths for dopants. Direct deposition of relaxed, highly lattice-mismatched layers (e.g. Ge on Si) results in large threading

dislocation densities ($\sim 10^9$ - 10^{11} cm^{-2}) at the film surface that are too high for most practical applications.

1.4.   Active Slip Systems in SiGe/Si Heteroepitaxy

The glissile slip system in diamond cubic semiconductors, such as Si, is {111}<110>, and a total of 24 unique slip systems (12 unique <110> Burgers vectors times 2 unique {111} planes per Burgers vector) are possible. However, for SiGe/Si(001) heteroepitaxy, not all of these slip systems will be active. For eight of these slip systems, Burgers vector and line direction are parallel, resulting in pure screw dislocations and no strain relief. Of the remaining 16 slip systems, only eight relieve compressive strain. These eight active slip systems are detailed in Table 1.1 below.

Table 1.1 Active slip systems for SiGe/Si(001) heteroepitaxy.

Glide Plane	Burgers Vector
$(\bar{1}\bar{1}1)$	$\frac{1}{2}a[\bar{1}0\bar{1}]$
$(\bar{1}\bar{1}1)$	$\frac{1}{2}a[10\bar{1}]$
$(\bar{1}11)$	$\frac{1}{2}a[10\bar{1}]$
$(\bar{1}11)$	$\frac{1}{2}a[011]$
$(\bar{1}\bar{1}\bar{1})$	$\frac{1}{2}a[10\bar{1}]$
$(\bar{1}\bar{1}\bar{1})$	$\frac{1}{2}a[01\bar{1}]$
$(\bar{1}\bar{1}1)$	$\frac{1}{2}a[101]$
$(\bar{1}\bar{1}1)$	$\frac{1}{2}a[011]$

When SiGe layers are deposited on Si substrates offcut from (001), the imbalance in resolved shear stress on active slip systems causes an imbalance in Burgers vector populations. This effect has implications on dislocation reduction reactions, discussed further in Section 4.2.2.

1.5. Comparing Dislocation Morphology in Low- and High-Mismatch Systems

In low-mismatch SiGe layers grown on Si(001), the majority of dislocations that nucleate are of the 60° variety (so named because of the angle between Burgers vector and line direction) with an in-plane Burgers vector (b_{eff}) equal to $\frac{a}{2}$. These are mixed dislocations, with edge, screw, and tilt (*i.e.*, a misfit dislocation whose Burgers vector is parallel to the growth direction) components, and they can glide on {111} planes. However, non-edge components of 60° dislocations are in essence wasted, since they do not contribute to strain relief. In contrast, in highly mismatched SiGe layers, the majority of dislocations that nucleate are sessile (90°) pure edge dislocations.

Qualitatively, in low-mismatch SiGe/Si layers, relatively few dislocations nucleate and they glide long lengths to relieve mismatch strain. Consequently, the threading dislocation density of the epilayer is relatively low, making it suitable for device applications. By contrast, in highly mismatched SiGe/Si layers, a high density of sessile 90° dislocations nucleates at the interface. The threading dislocation density in these films is very high, making them unsuitable for device applications. Moreover, highly mismatched SiGe films deposited on Si grow by the Stranski-Krastanov mechanism (unless grown at impractically low temperatures), which is unsuitable for planar device applications. This difference between low- and high-mismatch dislocation morphology is depicted in Figure 1.6 below. Compositionally graded buffers, discussed in the next section, enable the growth of high quality, highly mismatched films by dividing the large lattice mismatch over a series of low-mismatch interfaces.

Low Lattice Mismatch   **High Lattice Mismatch**
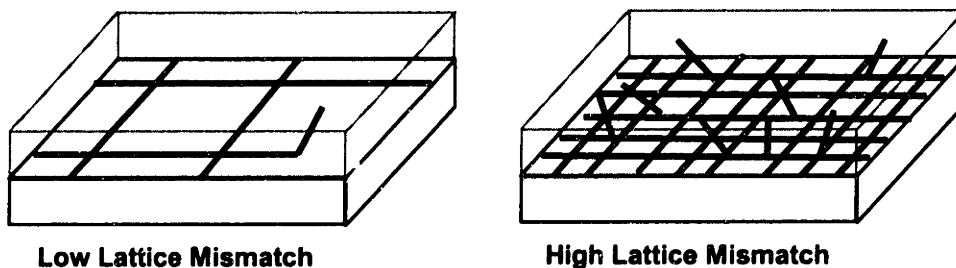
Figure 1.6 Illustration of dislocation morphology in low mismatch versus high mismatch systems. In low lattice mismatch films, relatively few mobile dislocations relieve mismatch strain. Under high lattice mismatch, a high density of mostly sessile dislocations nucleates at the film/substrate interface.

1.6. Compositionally Graded Buffers

Though several methods have been proposed to circumvent the problem of lattice mismatch, the only method that leads to consistent growth of low-defect-density relaxed SiGe layers on Si over an entire wafer involves the use of compositional grading, first introduced by Fitzgerald et al. in 1991.[13,14] A schematic of a compositionally graded buffer, along with an actual transmission electron micrograph of a graded SiGe region, is given in Figure 1.7 below.

(a)   (b)
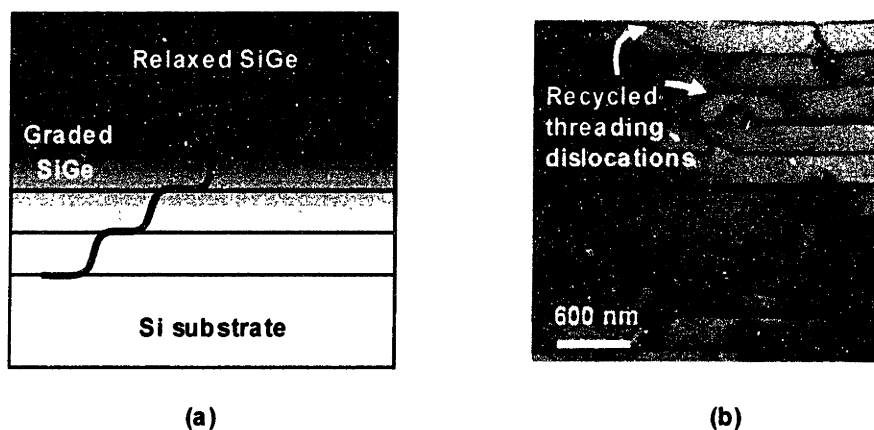
Figure 1.7 (a) Compositionally graded SiGe buffer schematic. A graded buffer consists of a series of step-graded, low mismatch interfaces. Each layer is relaxed to its intermediate lattice constant, and threading dislocations are recycled throughout the graded region. (b) Cross-sectional transmission electron micrograph of a compositionally graded SiGe region, showing threading dislocations being recycled as misfit dislocations throughout the graded region. Image courtesy of Thomas Langdo.

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In addition to its application to SiGe/Si, this technique has also been used to grow high quality InGaAs/GaAs[15] and InGaP/GaP[16] layers. Compositionally graded buffers introduce the lattice mismatch between the final SiGe layer and the Si substrate gradually. Each step in the grade is a low-mismatch interface, which ensures that a low density of dislocations is needed to relax the resulting lattice mismatch. Moreover, the misfit dislocations that glide to relax strain in a previously grown layer will thread their way to the film surface, where they can be recycled as strain relieving misfit dislocations in subsequently grown layers.[17] The low density of misfit dislocations at each interface minimizes detrimental dislocation-dislocation interactions. Finally, the small lattice mismatch at each layer minimizes dislocation nucleation. The final SiGe uniform composition cap layer has a relatively low density of threading dislocations and is fully relaxed, forming a "virtual substrate" for further deposition of device layers.

Because the final threading dislocation density of a compositionally graded SiGe layer should be set by dislocation glide kinetics at each interface, it will thus be independent of final Ge content.[18] Since dislocation glide velocities have an exponential dependence on temperature, growth temperature is the primary experimental variable that controls strain relaxation at each heterointerface. Before outlining a model based on dislocation glide, we should note that this concept stands in stark contrast to the previously held theory of strain relaxation kinetics in graded buffers. Based upon early efforts to grow SiGe films on Si,[19] a nucleation-limited model for relaxation in graded buffers was presented, in which dislocation density increased exponentially with growth temperature and linearly with thickness.[20,21,22] However, as will be outlined in the following sections, this prediction repeatedly has stood in stark contrast to experimental

data. A detailed critical analysis of the nucleation-limited model for strain relaxation in graded buffers has been presented by Kim.[23]

1.6.1. *Evolution of Threading Dislocation Glide Density in Compositionally Graded Layers*

Given that threading dislocation density in compositionally graded buffers is controlled by dislocation glide velocities, these two variables can be linked. In diamond cubic semiconductors, the empirical relation for dislocation glide velocity is[24,25,26]

$$v = v_0 \left(\frac{\tau_{eff}}{\tau_0} \right)^m \exp\left(\frac{-E_{glide}}{kT} \right)$$

where v_0 is a constant for a given material, τ_{eff} is the effective stress driving dislocation motion, τ_0 is a constant, m is typically between 1 and 2, E_{glide} is the activation energy for dislocation glide, and T is the growth temperature.

Assuming plastic relaxation is isotropic in all <110> directions, the plastic relaxation rate of a diamond-cubic thin film can be related to the dislocation glide velocity by:

$$\dot{\delta} = \frac{\rho b v}{2}$$

where ρ is the dislocation density and b is the Burgers vector. Combining these two equations yields

$$\rho = A \exp\left(\frac{E_{glide}}{kT} \right),$$

where A is a temperature-independent constant.[16] Thus, assuming that relaxation is glide-limited (*i.e.*, that impediments to dislocation flow do not force the nucleation of more

threading dislocations), a plot of $\ln(\rho)$ versus $1/T$ in graded buffers should be linear with slope equal to $k \times E_{glide}$.

A more complex version of this model relates the effective stress and relaxation rate described above to growth parameters, yielding the following expression for threading dislocation density in a graded buffer:[18]

$$\rho = \frac{2R_g R_{gr} \exp\left(\dfrac{E_{glide}}{kT}\right)}{bBY^m \varepsilon_{eff}^m}$$

where R_g is the film growth rate, R_{gr} is the strain grading rate, B is a constant, Y is the Young's modulus of the material, and ε_{eff} is the effective stress driving dislocation motion. Note that this equation begins with a slightly different but equivalent expression for dislocation glide velocity than the expression given above. The above equation provides valuable insight into the various experimental dependencies of threading dislocation density. The experimenter has control over only four variables: growth rate, grading rate, effective stress, and growth temperature. Practically speaking, growth rates and grading rates cannot be varied by orders of magnitude, so their effect on threading dislocation density is slight. Effective stress is coupled to grading rate, and its practical limit is set by dislocation nucleation. Unlike dislocation glide, dislocation nucleation displays an exponential dependence on strain:

$$\dot{\rho}_{nuc} \propto \exp\left(\frac{-E_{nucleation}}{C\varepsilon T}\right)$$

where $\dot{\rho}_{nuc}$ is the nucleation rate (number of threads per unit time), $E_{nucleation}$ is the activation energy for dislocation nucleation and C is a constant.[8] Thus, increases in strain will result in a small increase in dislocation glide velocity and large increase in

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dislocation nucleation. The derivation of this relation and its significance will be discussed further in Section 4.2.1. Ultimately, since threading dislocation density displays an exponential dependence on growth temperature, the final threading dislocation density in a compositionally graded buffer is mainly controlled by growth temperature.

Until recently, this model was never directly tested in SiGe, though the body of empirical evidence supported the major conclusion of this glide kinetics model: that high growth temperatures result in the lowest threading dislocation density (see, for example, Rosenblad et al.[27]). However, the hypothesis that the final threading dislocation density in a graded buffer should be independent of the final strain relieved was not born out by experiment.[8,18] Figure 1.8 is a plot of threading dislocation density versus final Ge composition for a series of samples grown at identical temperatures (750°C) and grading rates (10% Ge/μm).[18,28,29] The increase of threading dislocation density with overall mismatch accommodated was caused by the presence of impediments to dislocation glide, which in the SiGe materials system are dislocation pile-ups.[29] The formation of these pile-ups is outlined in the following section.

Threading Dislocation Density (cm^{-2})

1E+8

1E+7

1E+6

1E+5

30 40 50 60 70 80 90 100

% Ge
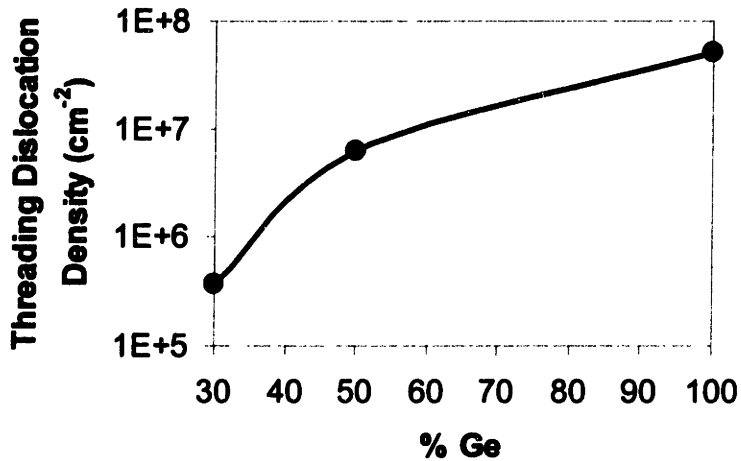
Figure 1.8 Overall threading dislocation density (a sum of the density of threading dislocations in the field and trapped in dislocation pile-ups) versus final Ge content for SiGe graded buffers grown at 750°C. Dislocation pile-ups cause an increase in overall threading dislocation density.

1.6.2. *Barriers to Dislocation Glide in SiGe and III-V Materials*

At any point during compositionally graded buffer growth, the film surface

morphology reflects overall strain fields present in the deposited material. Graded

buffers feature a diffuse array of misfit dislocations at each mismatched interface. These

dislocations glide along <110> directions and thus, for SiGe/Si(001) heteroepitaxy form

an orthogonal pattern. The film surface reflects the cumulative strain fields of misfit

dislocations distributed throughout the graded buffer and thus mimics the orthogonal

pattern of the misfit dislocation array, leading to the commonly observed "crosshatch"

pattern. An atomic force microscopy image of the surface of a compositionally graded

buffer displaying this crosshatch pattern is given in Figure 1.9 below.
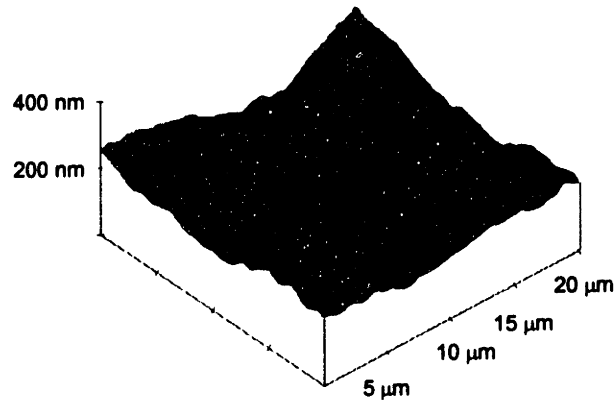
Figure 1.9 Atomic force microscopy image of the surface of a SiGe compositionally graded buffer showing the characteristic crosshatch surface morphology. In this case, the buffer has been graded to 50% Ge at a grading rate of 10% Ge/μm (2000 Å steps of 2% Ge).

Typical RMS roughness for SiGe compositionally graded buffers is on the order of 10 nm for 50 × 50 μm scan areas. Also, note that the frequency of the crosshatch pattern (~ 0.5/μm) does not reproduce misfit dislocation spacing, which is on the order of tens to hundreds of nm.

Deep troughs in the crosshatch pattern indicate regions of high strain concentration in the film and typically lie over bunches of misfit dislocations activated by a heterogeneous nucleation source.[8] Since the strain fields above misfit dislocations decay radially, these thin regions above misfit dislocations contain heavily concentrated strain fields and have been shown to trap gliding threading dislocations.[30] This increases already elevated local strain, further arresting adjacent threading dislocation glide and reducing local growth rates, leading to an escalation in dislocation blocking.[29] As a result, threading dislocation pile-ups, groups of immobile threading dislocations pinned in a deep crosshatch trough, form. A plan-view optical micrograph of a typical dislocation pile-up is given in Figure 1.10, where the pile-up was revealed using a selective etch.
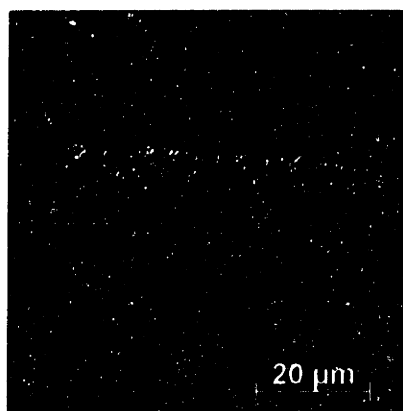
Figure 1.10 Plan-view optical micrograph of a selectively etched SiGe surface revealing widely spaced dislocations in the field and a large threading dislocation pile-up. Dislocations trapped in pile-ups cannot relieve mismatch strain, forcing nucleation of additional dislocations in the field and causing an escalation in overall dislocation density.

Threading dislocations trapped in dislocation pile-ups can no longer contribute to strain relief, which forces nucleation of additional dislocations away from the pile-up (termed field dislocations) to continue strain relief. This increases overall threading dislocation density, leading to the trend depicted in Figure 1.8. Dislocation pile-ups are general features of compositionally graded buffers and are not specific to the SiGe materials system.

In the $In_xGa_{1-x}P/GaP$ system, another type of defect, termed the branch defect, was found to be the primary impediment to dislocation flow.[16] The temperature dependence of the nucleation and strength of these defects was mapped out, and a new growth sequence was used to minimize their effect. These types of defects also possibly occur in InGaAs/GaAs.[31] A detailed discussion of branch defect control is found in Kim *et al.*[16,23] The removal of impediments to dislocation flow in $In_xGa_{1-x}P/GaP$ led to the recovery of pure glide-limited strain relaxation, as evidenced by samples graded to 10% In grown between 650°C and 800°C. In this case, threading dislocation density was set only by the exponential change in dislocation glide velocity with temperature, verified by the

calculation of the activation energy for dislocation glide from a plot of field threading

dislocation density versus growth temperature for a series of $In_{0.1}Ga_{0.9}P/In_xGa_{1-x}P/GaP$

samples.

1.6.3. *Controlling Threading Dislocation Pile-Ups in Compositionally Graded SiGe Layers*

One way to reduce dislocation pile-up density is simply to increase growth

temperature. High growth temperatures lead to high dislocation glide velocities, making

arrest of gliding threading dislocations less likely. This approach generally delays the

onset of pile-up formation and minimizes their occurrence.

Dislocation pile-up formation can also be controlled by switching to substrates offcut

from (001).[29] Offcut substrates interrupt the orthogonal crosshatch pattern, since the

intersection of {111} planes with the sample surface is no longer orthogonal. Figure 1.11

presents a schematic of the crosshatch pattern that results from growth of compositionally

graded SiGe layers grown on (001)-oriented Si substrates, (001)-oriented Si substrates

offcut 6° towards an in-plane <110>, and (001)-oriented substrates offcut 6° towards an
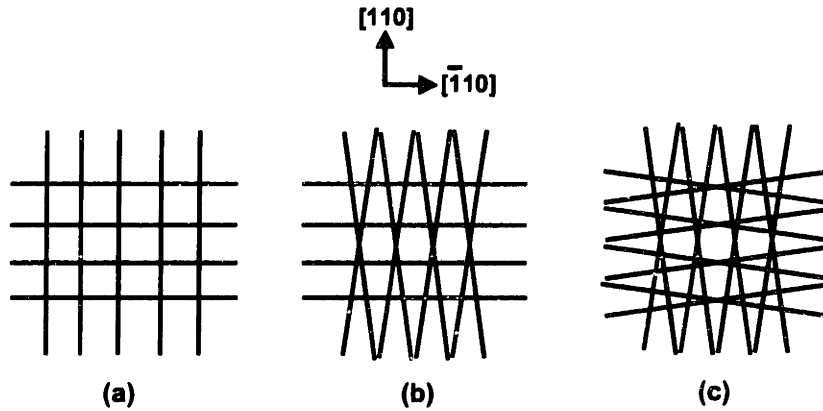
in-plane <100>.

Figure 1.11 Schematic of cross-hatch morphology for SiGe graded buffers grown on (a) (001) Si substrates, (b) (001) Si substrates offcut 6° towards an in-plane <110>, and (c) (001) Si substrates offcut 6° towards an in-plane <100>. For graded buffers deposited on offcut substrates, the probability that long parallel lines of misfit dislocations can form is reduced, leading to reduced dislocation pile-up density.

In these cases, the substrate offcut reduces the probability that a group of misfit dislocations will be grouped together in long parallel bundles and produce the strain effects discussed previously. Thus, growth on offcut substrates results in lower surface roughness and reduced dislocation pile-up density. Furthermore, offcut substrates suppress antiphase boundary formation in III-V material growth, and are thus necessary for high quality GaAs growth on Ge/SiGe/Si virtual substrates.

Another way to control dislocation pile-up formation is through an intermediate chemical-mechanical planarization (CMP) step.[28] CMP removes the crosshatch pattern and frees trapped threading dislocations. An intermediate planarization step (at 50% Ge) was shown to significantly reduce both the density of threading dislocations trapped in pile-ups and the field threading dislocation density in Ge/Si$_{1-x}$Ge$_x$/Si, yielding a final threading dislocation density in the relaxed Ge layer of 2×10^6 cm^{-2}. In fact, the threading dislocations liberated via CMP were free to undergo reduction reactions,

resulting in an overall reduction of threading dislocation density between 50% Ge and 100% Ge.

With control of dislocation pile-up density (and hence overall threading dislocation density) achieved over the entire composition range, the glide kinetics model can now be tested in SiGe. This will be outlined in Chapter 4. Furthermore, with high quality SiGe material available over the entire composition range, a wide range of new devices are possible. These are outlined in Section 1.7 and Chapter 2.

1.7. Device Integration on Relaxed SiGe Virtual Substrates

With the control over defect density obtained by using compositionally graded SiGe buffers, a variety of novel devices can now be integrated onto Si substrates. High quality Ge photodetectors have been integrated onto Ge/SiGe/Si compositionally graded buffers grown with an intermediate CMP step.[32] These photodetectors display dark currents near theoretical limits, indicating that the residual threading dislocation density is not limiting device quality. Coupled with advances in controlling the GaAs/Ge interface to eliminate antiphase boundaries,[33,34] Ge/SiGe/Si virtual substrates have also been used to integrate a variety of GaAs-based devices. GaAs solar cells, displaying record minority carrier lifetimes, have been realized on these virtual substrates.[35] In fact, minority carrier lifetimes in these devices approach values seen in bulk GaAs, further proof that residual threading dislocation density is not affecting efficiency of minority carrier devices. GaAs/AlGaAs optical links have also been successfully integrated onto these virtual substrates.[36] Finally, the first working lasers (AlGaAs/GaAs) on Ge/SiGe/Si virtual

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substrates have recently been realized.[37] This is a particularly noteworthy achievement since lasers are the most defect-sensitive minority carrier devices.

While defect densities are no longer affecting device efficiency, residual threading dislocations are still expected to decrease device reliability. Thus, the main challenge for continued integration success using Ge/SiGe/Si virtual substrates lies in still further reducing threading dislocation densities. A detailed understanding of dislocation glide and reduction kinetics and pile-up formation could enable further improvements in compositionally graded SiGe buffer material quality. This will be discussed further in Chapter 4.

Chapter 2. High Mobility Strained Si and SiGe Field-Effect Transistors on Relaxed SiGe Virtual Substrates

Using the relaxed SiGe platform, a variety of technologically relevant strained Si and SiGe-based heterostructures are possible. Tensile strained Si films can be produced by depositing thin Si layers on relaxed $Si_{1-x}Ge_x$ virtual substrates. Compressively strained $Si_{1-y}Ge_y$ layers can be grown on Si or on relaxed $Si_{1-x}Ge_x$ $(x < y)$ virtual substrates. The application of these layers to high mobility FETs is described in this chapter.

2.1.   Overview of Metal-Oxide-Semiconductor Field-Effect Transistor Technology

Before discussing SiGe/Si heterostructure field effect transistors, a brief review of metal-oxide-semiconductor field-effect transistor (MOSFET) device operation and performance metrics relevant to this work is warranted. A detailed description of MOSFET physics is presented by Sze.[38]

Figure 2.1 presents a schematic of a bulk Si n-MOSFET. Typically, the gate oxide is formed by thermal oxidation, and the doped source and drain regions are formed by ion implantation. Essentially, a MOSFET operates by using an applied gate voltage to modulate carrier motion between the source and drain. In other words, the gate voltage controls the minority carrier concentration in the channel under the gate. In standby, conventional MOSFETs in CMOS-based circuits operate in enhancement mode, meaning that there are few minority carriers in the gate channel. This ensures that few carriers flow between the source and drain in standby, leading to low power consumption.
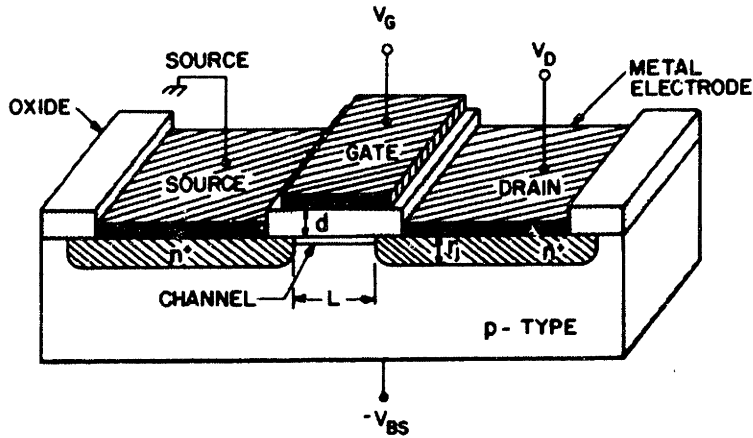
Figure 2.1 Cross-section of a typical metal-oxide-semiconductor field-effect transistor. Figure adapted from Sze.[38]

Beyond a threshold (gate) voltage, enough minority carriers are pulled into the channel to

induce inversion. Thus, under an applied bias between the source and drain, charge flows

between these two points. The relation between applied gate and drain voltages and drain

current for the linear regime ($V_D << V_G$) in a long-channel MOSFET is:

$$I_D = \frac{W}{L}\mu_{eff}C_{ox}\left(V_G - V_T\right)V_D$$

where W is the gate width, L is the gate length, μ_{eff} is the effective mobility of carriers in

the gate region, C_{ox} is the gate capacitance (per unit area), V_G and V_D are (respectively)

the applied gate and drain voltages, and V_T is the threshold voltage. Note that while this

equation neglects several important effects seen both in long- and short-channel

MOSFETs, it illustrates the key dependencies.

The first derivative of drain current with respect to gate voltage is known as the

transconductance and is given by:

$$g_m = \frac{W}{L}\mu_{eff}C_{ox}V_D$$

in the linear regime. Again, this is a simplified equation, but it reflects the key relation between transconductance and effective mobility. Essentially, transconductance represents the ability of the gate to modulate drain current, which is directly related to device speed. In this equation, the key materials parameter is the effective mobility, which is described in detail below.

Mobility describes the velocity of carriers in an electric field; low-field carrier velocity is simply the product of applied electric field and carrier mobility. Drift mobility is given by the familiar relation

$$\mu = \frac{e\tau}{m^*}$$

where e is the carrier charge, τ is the mean scattering time, and m^* is the carrier effective mass. From this relation, carrier mobility can be increased by reducing effective mass or by increasing scattering times. SiGe-based heterostructure FETs take advantage of both of these effects.

Mobility is often extracted by Hall effect measurements, but the so-called Hall mobility in this case differs from true drift mobility by a scattering factor. The precise value of the scattering factor is often unknown, which complicates interpretation of Hall mobility measurements. The actual value of drift mobility in a MOSFET (termed effective mobility), which is extracted from measured MOSFET output characteristics, takes into account the change in scattering time with the electric field experienced by carriers in an inversion layer (commonly called the effective vertical field). Effective vertical field[39,40] is computed through the relation

$$E_{eff} = \frac{Q_b + \eta Q_{inv}}{\varepsilon_s}$$

where Q_b is the bulk depletion charge in the semiconductor, η is a dimensionless fitting

parameter (η = 1/3 for holes and 1/2 for electrons), Q_{inv} is the inversion layer charge, and

ε_s is the dielectric constant of the substrate.

2.1.1. *Universal Mobility Curves for Si MOSFETs*

The relationship between effective mobility and effective vertical field in bulk Si

MOSFETs follows a universal relation regardless of substrate doping.[41] A schematic of

the universal mobility curve for both electrons and holes is given in Figure 2.2 below.
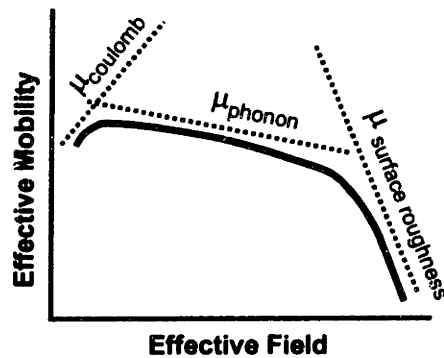
Figure 2.2 Universal electron and hole mobility relations for bulk Si MOSFETs. At low fields, carrier mobility is limited mainly by Coulomb scattering. At moderate vertical fields, carrier mobility is limited by phonon scattering. At high vertical fields, surface roughness scattering limits carrier mobility.

At low vertical fields, where the density of carriers in the inversion layer is low, carrier

mobility is controlled by Coulomb scattering, which becomes screened out at high

vertical fields (where there is a high density of carriers in the inversion layer). At

moderate vertical fields, carrier mobility is controlled by phonon scattering. Finally, at

high vertical fields, carrier mobility is degraded by surface roughness scattering. The

evolution of effective mobility versus effective vertical field is a key performance metric

for SiGe-based heterostructure MOSFETs. These curves, sometimes also normalized as

mobility enhancements over bulk Si, are first-order representations of performance enhancements in these devices.

Carrier mobility is of fundamental importance in MOSFET design, since it determines the die size needed to extract a given drive current from a MOSFET. Since hole mobility in bulk Si is much lower than electron mobility, p-MOSFETs must be made larger than n-MOSFETs to obtain the same drive current, consuming valuable chip real estate. Moreover, the mismatch between n- and p-MOSFET size increases overall circuit capacitance, decreasing the operating speed of logic elements. Symmetric carrier mobilities would offer more design latitude to VLSI circuit designers and significantly increase overall chip speed.

In modern short-channel MOSFETs, the relation between carrier mobility and device performance is not necessarily as straightforward. In this case, the high lateral electric fields employed lead to velocity saturation. Thus, there has been debate in the literature over whether low-field mobility enhancements translate into enhanced high-field performance. This is an important question, since modern digital CMOS circuits operate in the high-field regime, and it will be considered in more detail in Section 2.2.9.

2.1.2. Buried Channel MOSFETs

For certain heterostructures, band alignments promote confinement of electrons and/or holes within a single quantum well, opening up the possibility of buried channel MOSFETs. This class of devices is attractive because interface scattering is greatly reduced (since the upper interface of the channel is crystalline and coherent), so high-field mobility increases dramatically. However, the trade-off in buried channel devices is the reduction of overall gate capacitance, since the low dielectric constant semiconductor

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material is in series with the higher dielectric constant gate oxide. The assessment of buried channel MOSFET performance must therefore account for this effect. Returning to the transconductance relation given earlier, the capacitance term in this equation technically must now also account for the separation of the inversion layer charge centroid from the Si/SiO$_2$ interface. Thus, the C_{ox} term in this relation can be replaced by a general capacitance term that accounts for the total capacitance of the oxide and semiconductor in series. Transconductance is then more properly expressed as

$$g_m = \frac{W}{L} \mu_{eff} \left(C_{ox}^{-1} + C_s^{-1} \right)^{-1} V_D$$

where C_s is the semiconductor contribution to total capacitance. Semiconductor capacitance plays an important role in assessing the performance advantages of buried channel devices.

Doping profiles also present an important design issue for buried channel devices. With a buried quantum well, channel mobility can be increased significantly by using modulation doping.[42] In this technique, a thin layer, ideally single monolayer, of heavily doped material is placed either above or below the channel. Though the dopant atoms are physically separated from the quantum well, carriers will occupy this layer. Thus, the channel is free of dopant atoms, which eliminates ionized impurity scattering in these heterostructures. However, since carriers are present in the channel at zero gate bias, modulation doped transistors have high offstate currents. Modulation doped transistors are thus unsuitable for most digital applications, where standby power consumption must be minimized. Furthermore, modulation doping in general increases growth complexity and is difficult to accomplish in CVD. For these reasons, SiGe heterostructures that require modulation doping are in general incompatible with mainstream Si CMOS

technology. However, such devices are useful in analog circuit applications, in which low noise and high speed performance are the critical design criteria.

2.2. Strained Si and SiGe Heterostructure FETs

Relaxed silicon-germanium may be used as a template for integration of high mobility strained layer MOSFETs onto Si substrates. In the following sections, the electronic properties of SiGe alloys are discussed. Subsequently, the effects of strain on the valence and conduction bands are outlined and band alignments in strained SiGe-based heterostructures are presented. A review of strained Si and SiGe *p*-MOSFETs and strained Si *n*-MOSFETs is then presented, followed by a discussion of optimal heterostructures for SiGe-based CMOS applications.

2.2.1. *Electronic Properties of SiGe Alloys*

The bandgaps of relaxed[43] and compressively strained[44] SiGe alloys are depicted in Figure 2.3 below.
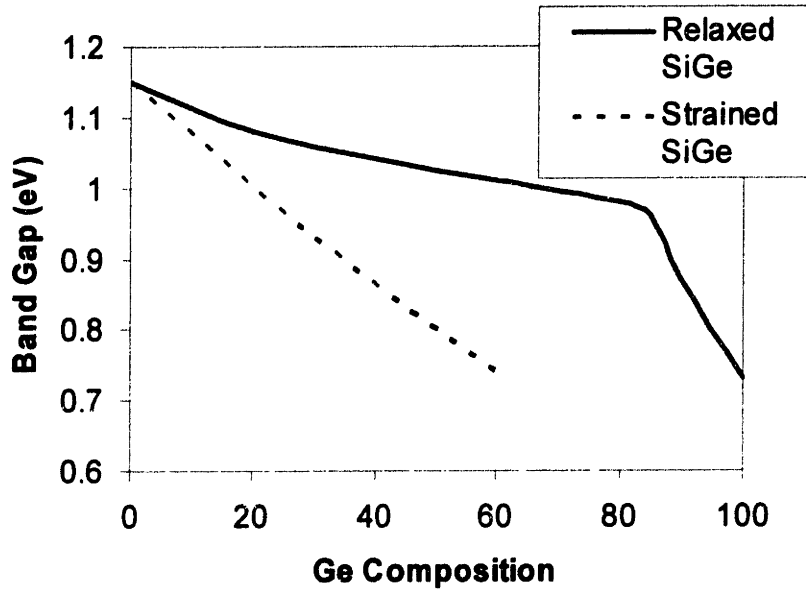
Figure 2.3 Bandgap of relaxed and compressively strained SiGe alloys versus Ge composition. In both cases, bandgap drops as Ge composition increases.

Generally, bandgap decreases as Ge content increases. The rapid drop in the bandgap of

relaxed alloys beyond 85% Ge indicates the change in conduction band structure from a

Δ-minimum to an L-minimum.

Electron and hole mobilities in bulk Si and Ge are given in Table 2.1 below, along

with values for other common semiconductor materials.

Table 2.1 Average electron and hole mobilities of common semiconductor materials.

Material	Electron Mobility $(cm^2/V\text{-}s)$	Hole Mobility $(cm^2/V\text{-}s)$
Si	1900	500
Ge	3800	1820
GaAs	8800	400
InP	4600	150

Measurements of bulk, often polycrystalline, SiGe crystals indicate that electron and hole

mobilities in SiGe alloys are generally suppressed compared to pure Ge or Si.[45,46,47,48]

Strain can decrease scattering rates and carrier effective mass and thus has a dramatic influence on carrier mobility, as described below.

2.2.2. Effect of Strain on the Valence Band

Figure 2.4 shows the valence band structure of unstrained Si and Si under biaxial tensile strain.[49] The valence band of Si is composed of the heavy hole, light hole, and spin-orbit subbands. In unstrained Si, the heavy hole and light hole subbands are degenerate at the Γ point, while the spin-orbit subband is located only 0.044 eV below these two subbands. As a result, holes in unstrained Si experience a high rate of intervalley scattering, which is the primary limitation on hole mobility in bulk Si. When Si is subjected to a biaxial tensile strain, the energy of the heavy hole and spin-orbit subbands is lowered relative to the light hole subband, leading to reduced intervalley scattering. Theoretical predictions indicate that the elimination of intervalley scattering does not occur until relatively high strain levels, beyond that of strained Si on virtual substrate compositions of 40% Ge (~ 1.6% strain).[50]
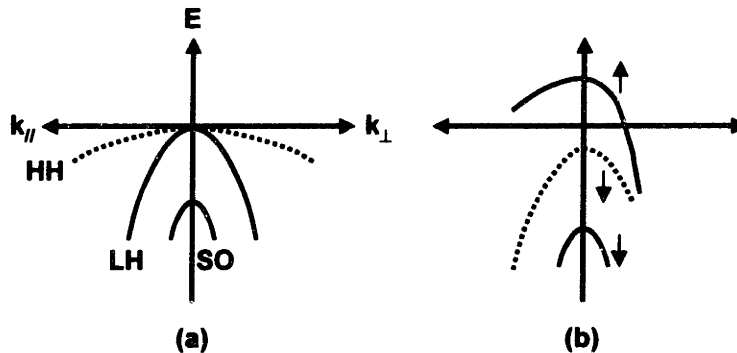
Figure 2.4 Valence band structure of (a) unstrained Si and (b) Si under biaxial tensile strain. Tensile strain lowers the energy of the heavy hole and spin-orbit subbands relative to the light hole subband and modifies the shape of the valence subbands.

Tensile strain also modifies the shape of the valence subbands, lowering the in-plane and out-of-plane effective mass of holes.[49] In fact, in strained Si the designations "heavy hole" and "light hole" are merely used for identification purposes, since the subband deformation is strain-dependent and anisotropic. Because tensile strain continues to lower the effective mass of holes beyond virtual substrate composition of 40% Ge, hole mobility enhancements never completely saturate with strain.

Of course, since Si has a smaller lattice constant than SiGe alloys, compressively strained Si is not possible in the SiGe materials system. However, compressively strained $Si_{1-y}Ge_y$ alloys can be grown on Si or on relaxed $Si_{1-x}Ge_x$ virtual substrates (for x $< y$). For relaxed $Si_{1-y}Ge_y$ alloys below about 85% Ge, the valence band structure still qualitatively resembles that of Si, and the effects of biaxial compressive strain are similar to those of biaxial tensile strain. However, in this case, compressive strain lowers the energy of the light hole and spin-orbit subbands relative to the heavy hole subband, leading to reduced intervalley scattering. As described above, the "light hole" and "heavy hole" designations are used only for identification purposes, since strain modifies the shape of the valence subbands. The net result of compressive strain in SiGe alloys is a reduction in hole effective mass and suppression of intervalley scattering, leading to enhanced carrier mobility.

2.2.3.   Effect of Strain on the Conduction Band

Figure 2.5 presents a schematic of the conduction band structure of unstrained Si and Si under biaxial tensile strain. The conduction band minimum is located at the Δ-point, and is composed of six-fold degenerate lobes along <100> directions. Biaxial tensile strain splits this six-fold degeneracy, lowering the energy of the two perpendicular (Δ_2)

valleys relative to the four in-plane (Δ_4) valleys. This energy splitting suppresses intervalley scattering between the Δ_2 and Δ_4 valleys and leads to increased electron mobility. Monte Carlo calculations predict that intervalley scattering is completely suppressed for virtual substrate compositions greater than 20% Ge,[51] which is in good agreement with experiment.[52,53]
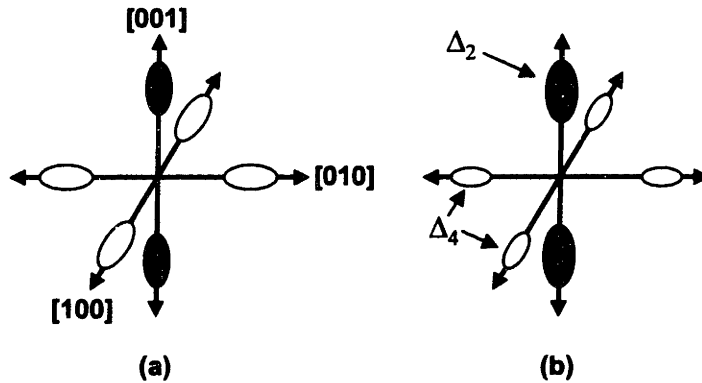
Figure 2.5 Conduction band structure of (a) unstrained Si and (b) Si under biaxial tensile strain.

Electrons in unstrained Si occupy all six conduction band lobes and thus experience a combination of the longitudinal ($m_l = 0.98m_0$) and transverse ($m_t = 0.19m_0$) effective mass. The in-plane electron effective mass in unstrained Si is given by

$$m^* = \left[\frac{1}{3}\left(\frac{1}{m_l}\right) + \frac{2}{m_t}\right]^{-1}$$

and is equal to $0.26m_0$. Tensile strain does not alter the shape of the conduction band subbands in Si, so strain does not directly alter electron effective mass.[54] However, for in-plane transport, electrons in Δ_2 valleys experience only the smaller transverse effective mass, leading to increased carrier mobility. Thus both the reduction in intervalley scattering and reduced in-plane effective mass are responsible for increased electron mobility in strained Si.

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Again, since Si has a smaller lattice constant than SiGe alloys, compressively strained Si cannot be produced in the SiGe materials system. Theoretical calculations indicate that compressively strained $Si_{1-y}Ge_y$ alloys grown on relaxed $Si_{1-x}Ge_x$ virtual substrates (for $x < y$) exhibit only moderate mobility enhancements over their unstrained counterparts.[55] Moreover, the band alignments in compressively strained $Si_{1-y}Ge_y$ on relaxed $Si_{1-x}Ge_x$ result in a negligible conduction band offset between these two layers (discussed in the next section), making electron confinement in the device layers difficult to achieve.

2.2.4.   *Compressively Strained SiGe: Type I Band Alignment*

When compressively strained $Si_{1-y}Ge_y$ layers are deposited on Si or on relaxed $Si_{1-x}Ge_x$ $(x < y)$ virtual substrates, the difference in bandgap between the strained and relaxed layers is primarily accommodated by a valence band offset,[56] as illustrated in Figure 2.6 below. This Type I band offset leads to a quantum well for holes, making these heterostructures suitable for buried or surface channel devices. For a compressively strained $Si_{1-y}Ge_y$ layer on a relaxed $Si_{1-x}Ge_x$ $(x < y)$ virtual substrate, the average valence band offset in eV is given by[57]

$$\Delta E_v = (0.47 - 0.06x)(y - x) .$$
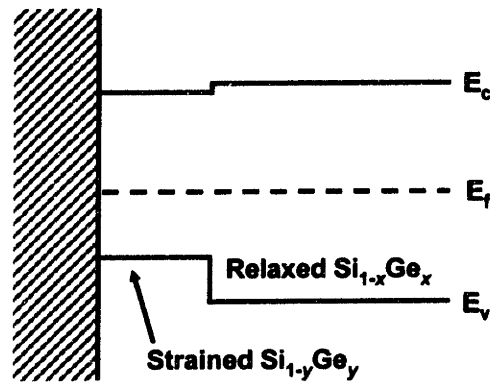
Figure 2.6 Band alignments for strained $Si_{1-y}Ge_y$/relaxed $Si_{1-x}Ge_x$ $(x < y)$, illustrating the Type I band offset that emerges for compressively strained $Si_{1-y}Ge_y$ alloys on $Si_{1-x}Ge_x$.

The conduction band offset for this configuration is negligible.

2.2.5. Pseudomorphic SiGe p-Channel FETs

The valence band offset between compressively strained SiGe and Si offers the possibility of realizing high mobility fully pseudomorphic enhancement mode p-MOSFETs on Si substrates.[58,59] These structures are typically capped with thin Si layers to ensure a high quality MOS interface.[60] While such structures are attractive because of their simplicity, the mobility enhancements possible in a fully pseudomorphic technology are relatively modest, especially at high vertical fields where parallel conduction through the Si cap layer occurs.[60,61,62,63,64] In contrast, compressively strained layers of higher Ge content $(y > 0.5)$ grown on relaxed $Si_{1-x}Ge_x$ virtual substrates offer better potential for high mobility p-MOSFETs, since the effective mass of holes in these channels is much smaller.

2.2.6. SiGe p-Channel FETs on Relaxed SiGe Virtual Substrates

Buried, compressively strained, $Si_{1-y}Ge_y$ quantum wells grown on relaxed $Si_{1-x}Ge_x$ $(x < y)$ virtual substrates have been used to create high mobility two-dimensional hole gases.

By incorporating modulation doping, peak room temperature hole mobility values of 700 cm^2/V-s, 1050 cm^2/V-s, and 1860 cm^2/V-s for strained 70% Ge,[65] 80% Ge,[66] and 100% Ge[67] quantum wells (respectively) have been obtained. These layers are typically deposited on virtual substrates such that the difference between channel and substrate composition is 30-40% Ge. Because of this large compressive strain, these layers must be grown at reduced temperatures (< 500°C) to suppress strain-induced channel undulations.

The impact of alloy scattering on hole mobility has been a controversial issue in SiGe-based p-MOSFETs,[55,68,69] fueled in part by the paucity of reliable experimental data. Generally, alloy scattering-limited mobility in $Si_{1-y}Ge_y$ is described by

$$\mu_{alloy} \propto \left(U_{alloy} \cdot y(1-y) \right)$$

where U_{alloy} is the alloy scattering potential. The exact value of alloy scattering-limited mobility depends on carrier effective masses, which are a function of strain and composition. Regardless of the alloy scattering potential, this equation predicts alloy scattering to be most severe for $0.3 \leq y \leq 0.7$. The value of alloy scattering potential used in literature varies widely, ranging from 0.2 eV to 1 eV,[68] leading to a wide range of theoretical predictions regarding the importance of alloy scattering on hole mobility in strained SiGe quantum wells. Fischetti and Laux[55] have argued that alloy scattering in $Si_{1-y}Ge_y$ layers completely cancels performance gains realized from the suppression of intervalley scattering. On the other hand, Kearney and Horrell[68] have argued that alloy scattering is not the dominant room temperature scattering mechanism in SiGe quantum wells. The differences in theoretical predictions can be attributed to several experimental and theoretical shortcomings. First, much of the mobility data used for theoretical

predictions has come from limited measurements on polycrystalline $Si_{1-y}Ge_y$ samples ($y <$ 0.2).[70,71] Second, room temperature experimental measurements in SiGe quantum wells are subject to the influence of other scattering mechanisms, making alloy scattering difficult to isolate.[68] Similarly, the uncertainty in Hall scattering factors in SiGe quantum wells complicates the extraction of true drift mobility. Third, most experimental data is focused on pseudomorphic SiGe layers grown on Si substrates, where strain and channel composition cannot be decoupled, further complicating the issue. Finally, the presence of parasitic hole channels complicates isolation of buried channel mobility, particularly since the out-of-plane effective mass of holes in these layers is very low.

To assess the performance potential of SiGe quantum wells, Hackbarth et al.[72] compared hole mobility in modulation doped $Si_{1-y}Ge_y$ quantum wells grown on relaxed $Si_{1-x}Ge_x$ virtual substrates ($y - x = 0.3$ or 0.4). A hole mobility of 1880 cm^2/V-s was obtained for pure Ge channels on 60% Ge virtual substrates. Hole mobility was significantly lower for SiGe alloy channels, but peak hole mobility in 80% Ge channels was still roughly twice that of bulk Si. In a theoretical study, Bufler and Meinerzhagen[71] calculated hole mobility for the full range of strained $Si_{1-y}Ge_y$ alloys on relaxed $Si_{1-x}Ge_x$ virtual substrates (for all y and x). They concluded that the highest hole mobility enhancements would be obtained for strained Ge channels, though large enhancements (> 3 times bulk Si) are obtainable for channel compositions beyond 60% Ge, and also that channel composition played a more important role than strain in determining hole mobility. This data clearly indicates that strained Ge channels offer the highest hole mobility, but they require higher Ge content virtual substrates. Such layers are more difficult to integrate into heterostructures optimized for both high electron and hole

mobility, as will be discussed in detail in Chapter 6. Lower Ge composition strained SiGe alloy channels (70-80% Ge) still offer high hole mobility but do not require high-Ge-content virtual substrates.

Because pure Ge displays the highest hole mobility in the SiGe materials system, efforts at creating two-dimensional hole gases have focused on using strained Ge channels.[73] By using modulation doped Ge quantum wells grown on relaxed SiGe virtual substrates, (using either Si[74,75,76,77] or Ge[78] substrates), high transconductance p-MODFETs can be created. These devices show excellent promise for analog applications, where utility is governed largely by device switching speed. However, since these devices do not employ MOS gates, they operate under only a limited range of gate voltages. Furthermore, most modulation doped devices operate in depletion mode, complicating integration of these layers into conventional CMOS circuits. Ideally, high-Ge-content quantum wells would be combined with Si/SiO_2 gates to create high mobility p-MOSFETs compatible with mainstream Si CMOS technology.

2.2.7.   Tensile Strained Si: Type II Band Alignment

A schematic of band alignments in strained Si on relaxed $Si_{1-x}Ge_x$ is given in Figure 2.7. As this figure indicates, strained Si on relaxed $Si_{1-x}Ge_x$ forms a Type II band offset, leading to a potential well that confines electrons.[79] Thus, both surface and buried channel n-MOSFETs can be realized in this system. The magnitude of the conduction band offset (in eV) is given by[44]

$$\Delta E_c = 0.6x$$

for strained Si on relaxed $Si_{1-x}Ge_x$ ($x < 0.6$). Thus, for virtual substrate compositions of 20-30% Ge, the band offset between strained Si and relaxed $Si_{1-x}Ge_x$ is 120-180 meV.

The band offset of strained Si on relaxed SiGe leads to a potential *barrier* for holes, the magnitude of which is given by

$$\Delta E_v = (0.74 - 0.53x)x$$

for strained Si on relaxed $Si_{1-x}Ge_x$ ($x < 0.6$).[44] As a consequence of this barrier, holes will not populate the strained Si until the vertical field is sufficient to overcome the band offset, and only surface channel strained Si p-MOSFETs are possible. In principle, since MOSFET devices operate under such a bias, the offset has little consequence. However, since the out-of-plane effective mass of holes is relatively low,[49] holes can also populate the relaxed SiGe virtual substrate, forming a low mobility parasitic channel and degrading device performance.
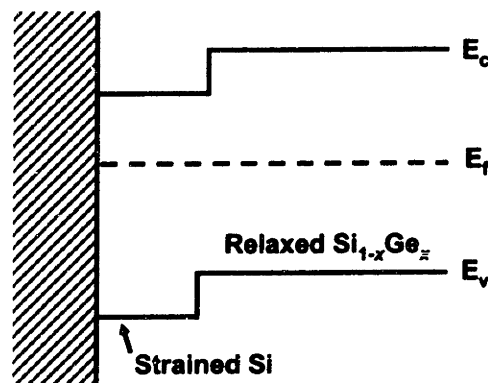
Figure 2.7 Band alignments for strained Si on relaxed $Si_{1-x}Ge_x$ illustrating the Type II band offset for these heterostructures.

2.2.8. Strained Si p-MOSFETs

The first verification of enhanced hole mobility in tensile strained Si was made by Nayak *et al.*, where a 50% enhancement in hole mobility over bulk Si was attained.[80] Since then, several other researchers have fabricated surface channel strained Si p-MOSFETs on relaxed SiGe virtual substrates.[52,81,82,83] Peak hole mobility enhancements of 60% have been obtained by Currie *et al.*[52] and Rim *et al.*[81] For virtual substrate

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compositions below 30% Ge, hole mobility enhancements increase roughly linearly with strain.[52,81] While the general trend of increasing mobility with strain was verified, the authors only investigated virtual substrate compositions below 30% Ge and did not observe the predicted saturation in mobility enhancements with strain.

Hole mobility enhancements in strained Si display a strong dependence on effective vertical field. An example of hole mobility enhancement versus effective vertical field is given in Figure 2.8 below for a strained Si p-MOSFET on a relaxed $Si_{0.7}Ge_{0.3}$ virtual substrate.[52]
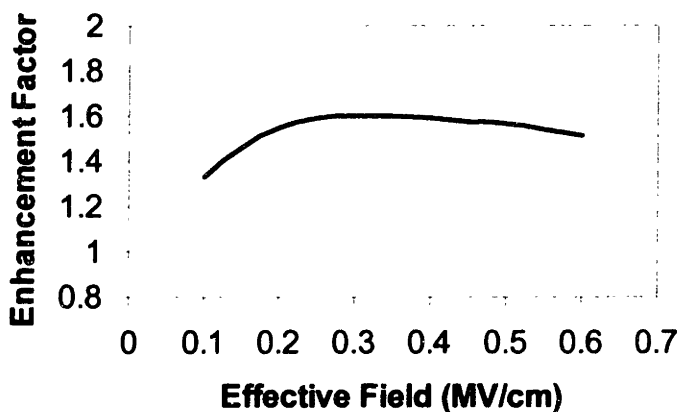
Figure 2.8 Hole mobility enhancement versus effective vertical field for a typical strained Si p-MOSFET.[52] At low vertical fields, hole mobility is suppressed by parallel conduction through the relaxed SiGe virtual substrate. Hole mobility enhancements also decrease at high-fields, possibly from intervalley scattering.

At low vertical fields, mobility enhancements are relatively low, likely because of parallel conduction through the low mobility relaxed SiGe virtual substrate.

Enhancements increase with increasing vertical field, but then drop slightly at high-fields.

Maiti *et al.* have postulated that since the average kinetic energy of holes is very high at high vertical fields, holes can scatter from the light hole to heavy hole band, reducing hole mobility enhancements at high vertical fields.[83]

To lessen the influence of hole population in the virtual substrate at low vertical fields, the abrupt relaxed SiGe/strained Si interface can be replaced with a graded interface.[81] The band alignments for this configuration are given in Figure 2.9. This gradeback structure eliminates the abrupt band offsets and promotes hole population in the strained Si layer at low vertical fields. However, the gradeback layer effectively reduces the critical thickness of the surface channel and hastens misfit dislocation introduction. Also, since high vertical fields effectively pull holes into the surface layer, the gradeback layer does not influence high-field mobility enhancements.[4] Thus, an abrupt interface heterostructure is actually preferable for digital devices that operate at high vertical fields.
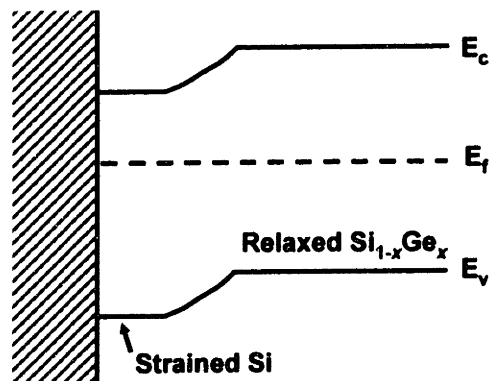
Figure 2.9 Band alignments for strained Si on relaxed SiGe using a gradeback layer at the interface. The gradeback smoothes the valence band discontinuity, allowing holes to populate the high mobility strained Si layer at low vertical fields.

Detailed studies of the effects of channel thickness and strain on mobility enhancements in surface channel strained Si p-MOSFETs, as well as further exploration of the dependence of mobility enhancements on effective vertical field and the influence of alloy scattering on hole and electron mobility in tensile strained SiGe channels, will be presented in Chapter 5.

2.2.9.   *Strained Si n-MOSFETs*

Surface and buried channel strained Si *n*-MOSFETs on relaxed SiGe virtual

substrates have been fabricated by several researchers.[52,84,85,86,87] Since electron mobility

is much higher than hole mobility in Si, early efforts aimed at realizing high mobility

strained Si quantum wells focused on electron channel devices. For this reason, there

exists an evolution of low temperature electron mobility records in strained Si

heterostructures that nicely illustrates improvements in material quality brought about by

the introduction of compositionally graded buffers. Figure 2.10 presents a plot of record

low-temperature (4K unless otherwise noted) electron mobility in strained Si versus time.

Note that all of these heterostructures are modulation doped, buried channel

configurations, optimized for high mobility at low temperature.
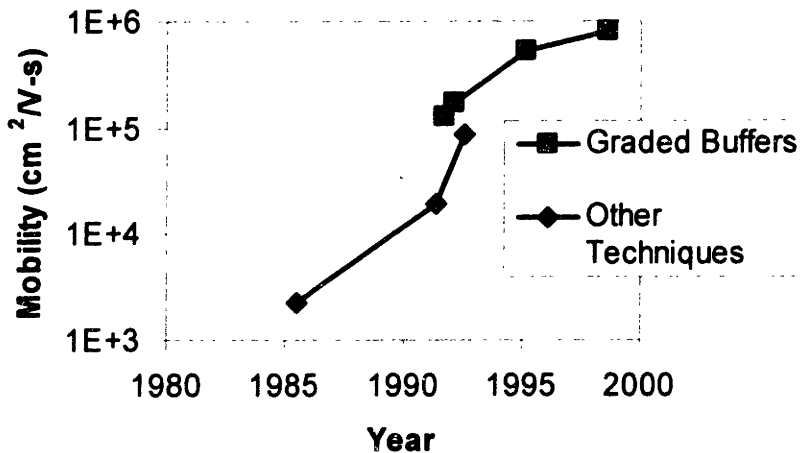
Figure 2.10 Evolution of record low temperature electron mobility in strained Si versus time. The introduction of the graded buffer technique resulted in a rapid increase in electron mobility. In chronological order, the record for electron mobility in strained Si grown without graded buffers was held by Abstreiter *et al.*,[79] Ismail *et al.*,[88] and Nelson *et al.*,[89] while the record for electron mobility in strained Si grown on graded buffers was held by Mii *et al.*,[90] Schäffler *et al.*,[91] Ismail *et al.*,[92] and Sugii *et al.*[93] Figure adapted from Schäffler.[69]

Early measurements of electron mobility in strained Si heterostructures were disappointing because of poor material quality; in fact, peak electron mobility in strained Si was actually below that of bulk Si until 1991.[90,94] With the advent of graded buffer technology,[13] electron mobility enhancement over bulk Si was demonstrated for the first time in 1991 by Mii *et al.*[90] Since that time, other researchers have incrementally improved on these numbers by improving interface quality and adjusting doping profiles. The current record low-temperature electron mobility is 800,000 cm^2/V-s.[93]

The first strained Si modulation doped field-effect transistors fabricated on SiGe graded buffers were realized by Konig[95] while enhancement mode strained Si surface channel *n*-MOSFETs were first fabricated by Welser *et al.*[84] To date, mobility enhancements in surface channel MOSFETs of roughly 80% over bulk Si have been obtained by several researchers.[52,84,87] Since modulation doped devices are incompatible with mainstream Si CMOS technology, this discussion will focus on enhancement mode MOSFETs in which carriers are supplied by conventional source/drain implants.

In strained Si surface channel MOSFETs, mobility enhancements increase roughly linearly with strain up to about 20% Ge, saturating at roughly 80% enhancement.[52,53] For strained Si on virtual substrates greater 20% Ge, the subband splitting is large enough to completely suppress intervalley scattering. These experimental results are in good agreement with theory.[51] For surface channel strained Si *n*-MOSFETs, mobility enhancement is not a function of vertical effective field.[52] However, because of the potential for parasitic channels in buried channel strained Si *n*-MOSFETs, mobility enhancements in these devices are a strong function of vertical field.[84] At low fields, carriers are confined to the buried channel and experience decreased Coulomb scattering;

therefore low-field mobility in buried channel MOSFETs exceeds that of surface channel MOSFETs. However, at the high fields used for CMOS, carriers are pulled towards the gate interface, decreasing mobility enhancements. Moreover, because buried channel structures typically minimize the thickness of the Si surface channel (to avoid population of this parasitic channel), carriers pulled towards the surface actually sample the low mobility relaxed SiGe layers, thus resulting in lower high-field mobility than their surface channel counterparts. For this reason, surface channel strained Si n-MOSFETs are preferable for high-field CMOS applications.

Because of the large out-of-plane (longitudinal) mass of electrons in strained Si,[96] carriers can be confined over a wide range of channel thicknesses. Currie et al.[52] have shown that electron mobility enhancements in surface channel strained Si n-MOSFETs drop rapidly for channel thicknesses below roughly 50 Å, since thinner channels are unable to confine electrons. For channels between roughly 50 Å and 180 Å thickness, electron mobility enhancements are constant at 80% over bulk Si. Electron mobility enhancements drop slightly beyond 180 Å, possibly because of misfit dislocation scattering at the strained Si/relaxed $Si_{0.8}Ge_{0.2}$ interface.

High-field Transport in Strained Si n-MOSFETs

As discussed in Section 2.1, the effects of increased low-field carrier mobility were unclear in deep submicron FETs, where velocity saturation effects could potentially negate gains in carrier mobility. The saturation velocity of electrons in strained Si is only slightly higher than in bulk Si;[54,97] therefore, to first order, enhanced electron mobility in strained Si could have minimal impact on high-field state-of-the-art MOSFET performance (though recent studies have demonstrated that the injection velocity of

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carriers from the source to the inversion layer under the gate under quasi-equilibrium conditions, *not* the saturation velocity, represents the upper bound to MOSFET speed[98,99]). Recently, Rim *et al.*[87,100] demonstrated a 75% increase in electron mobility and a 40% increase in drive current over bulk Si for 0.1 micron devices measured at vertical fields greater than 1 MV/cm. Enhanced current drive in strained Si *n*-MOSFETs for vertical fields up to 1.5 MV/cm has also recently been observed in 70 nm devices fabricated in a state-of-the-art industrial facility.[101] These results clearly indicate that the demonstrated low-field mobility enhancements of these devices (and by extension of other SiGe-based heterostructure MOSFETs) will translate into enhanced CMOS circuit performance.

The significance of low-field mobility enhancements in determining high-field device performance was further underscored in a study by Lochtefeld *et al.*[102] In this study, both long- and short-channel bulk Si *n*-MOSFETs were subject to an applied uniaxial tensile stress, obtained by using a bending apparatus. The researchers measured the shift in mobility as a function of strain for both sets of devices. Though gains in mobility with strain were lower for short-channel devices than for long-channel devices, a direct increase in high-field electron velocity with strain was observed. Again, these results underscore the positive impact of high mobility, even under high lateral electric fields.

2.2.10. *SiGe Heterostructure FETs for CMOS Applications*

Because strained Si provides both electron and hole mobility enhancements over bulk Si, surface channel strained Si devices are candidates for SiGe-based CMOS applications. However, hole mobility in conventional strained Si *p*-MOSFETs is still roughly four times lower than electron mobility. A promising route towards integration of high hole

mobility devices on Si substrates involves the use of buried compressively strained $Si_{1-y}Ge_y$ layers and surface strained Si layers, grown on relaxed $Si_{1-x}Ge_x$ virtual substrates ($x < y$), hereafter referred to as dual channel heterostructures.[103] A schematic of the layer sequence and band alignments in these heterostructures is given in Figure 2.11.
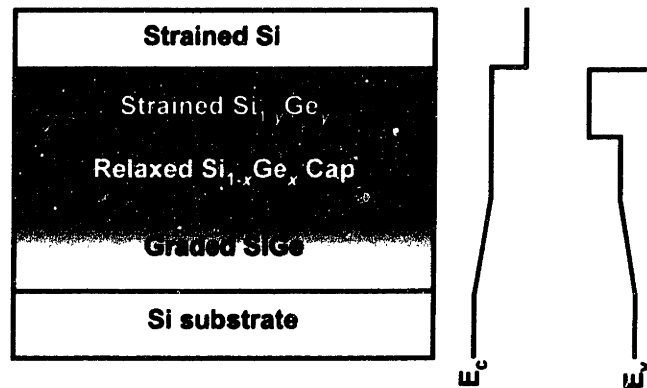
Figure 2.11 Schematic layer sequence and band alignments for dual channel heterostructures. Strained layer thicknesses have been exaggerated for clarity. The buried compressively strained $Si_{1-y}Ge_y$ channel is a quantum well for holes while the surface strained Si channel is a quantum well for electrons. The conduction band offset between the relaxed $Si_{1-x}Ge_x$ and the strained $Si_{1-y}Ge_y$ is negligible.

Dual channel heterostructures allow simultaneous integration of hole and electron channel devices within the same layer sequence,[104] while the strained Si surface channel enables formation of a high quality MOS gate interface. Since the hole in conventional strained Si/relaxed $Si_{1-x}Ge_x$ surface channel MOSFETs remains light in the direction normal to the channel,[49] the hole wavefunction in the normal direction is large and holes sample the low mobility relaxed $Si_{1-x}Ge_x$ virtual substrate. By inserting a compressively strained $Si_{1-y}Ge_y$ layer below a thin strained Si layer, holes are prevented from occupying the low mobility relaxed $Si_{1-x}Ge_x$. Furthermore, the high mobility of compressively strained Ge-rich hole channels has been well documented,[66,67,73,105] so holes sampling both strained layers should see a dramatic mobility boost. With high enough band offsets between the buried and surface channel and a thick enough buried channel, holes can be

largely confined in the high mobility buried channel. The extent to which devices based upon dual channel heterostructures behave as true buried channel devices thus depends on channel thickness and composition, both of which control band offsets that define the buried channel. Finally, dual channel heterostructures require no modulation doping— high mobility hole and electron channels are formed simply by the confinement resulting from band alignments in each layer.

Recently, Höck *et al.* have shown that through the combination of a buried compressively strained $Si_{0.17}Ge_{0.83}$ channel and a surface tensile strained Si channel, room temperature hole mobilities of over 700 cm^2/V-s are possible.[106] They also demonstrated that hole mobility in these devices closely matches electron mobility over a limited range of effective vertical fields. This concept has recently been applied to pure Ge channels deposited on 70% Ge virtual substrates, where peak hole mobilities over 1000 cm^2/V-s have been obtained, despite the presence of a highly defective Si surface channel.[107]

Detailed studies of dual channel heterostructure *n*- and *p*-MOSFETs will be presented in Chapter 6.

2.3. Scope and Organization of Thesis

This thesis examines dislocation dynamics in compositionally graded SiGe layers and evaluates strained Si and SiGe-based MOSFETs for next-generation CMOS applications. Chapter 3 describes SiGe growth, characterization, and MOSFET fabrication. Chapter 4 presents a detailed description of dislocation glide, blocking, and reduction kinetics in compositionally graded SiGe layers. A complete description of the mechanisms controlling threading dislocation density in these films is outlined. Chapter 5 contains detailed experimental results regarding hole mobility enhancements in strained Si *p*-

MOSFETs and alloy scattering in tensile-strained SiGe surface channel MOSFETs. Coupled with recent work on strained Si n-MOSFETs, a complete description of mobility enhancements as a function of strain, channel thickness, and channel composition in surface channel strained Si and SiGe MOSFETs emerges. Chapter 6 describes hole and electron mobility enhancements in dual channel heterostructure MOSFETs. In particular, hole mobility enhancements in these heterostructures are explored as a function of strain, channel thickness, and buried channel composition. These devices display enormous potential for symmetric mobility SiGe-based heterostructure MOSFETs. Finally, Chapter 7 concludes with a research summary and suggestions for future work.

Chapter 3.   SiGe Growth and Device Fabrication

3.1. Ultrahigh Vacuum Chemical Vapor Deposition

The SiGe virtual substrates used in this thesis were grown by ultrahigh vacuum chemical vapor deposition (UHVCVD). A schematic of the UHVCVD system employed in this study is given in Figure 3.1 below.
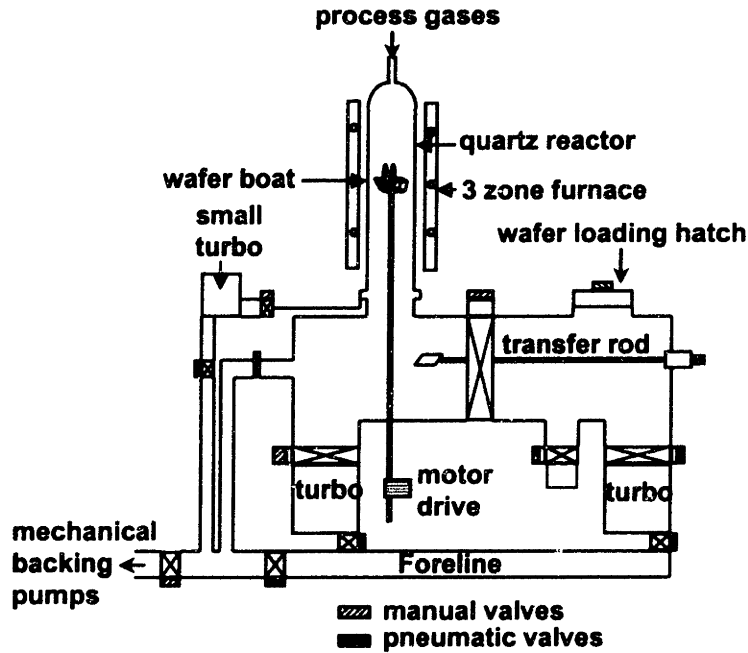
Figure 3.1 Schematic of the UHVCVD system used in this work.

The UHVCVD technique was developed in the mid-1980s for deposition of thin epitaxial silicon films at reduced growth temperatures.[108] As the partial pressures of water and oxygen are reduced, SiO_2 is unstable at increasingly lower temperatures,[109,110] enabling growth of high quality epitaxial layers at relatively low growth temperatures ($< 550°C$).

In practice, the ultimate utility of the UHVCVD system used in this study is its ability to grow high quality compositionally graded buffers at high temperatures ($750°C - 900°C$) and device heterostructures at low temperatures ($400°C - 650°C$).

The UHVCVD system used in this study employs SiH_4 and GeH_4 source gases. Dopants are supplied via 1% B_2H_6 in H_2 and 1% PH_3 in H_2 gases, which can be further diluted with either H_2 or Ar via two dilution stages. The UHVCVD is a hot-walled, load-locked system with a quartz growth chamber. The growth chamber holds up to ten 4" Si wafers at once, and wafer diameters up to 6" can be accommodated if proper quartzware is used. The UHVCVD has a base pressure of less than 1×10^{-9} torr at 750°C, achieved through the use of a novel differential pumping scheme between two o-rings at the quartz tube base. Growth temperatures vary from 400°C to 900°C; the upper limit is set by devitrification of the quartz tube and cooling of the o-rings at the tube base, while the lower limit is set by thermally activated decomposition of source gases. Typical growth pressures vary between 3mT and 25mT, and can be regulated by partially closing a gate valve over the reactor turbo pump, decreasing its pumping efficiency.

The UHVCVD system used in this study has been extensively calibrated over several years, so composition and growth rate are known over the entire range of growth temperatures. A general discussion of SiGe growth by chemical vapor deposition was presented by Greve.[111] In general, composition and growth rate are determined by the kinetics of source gas decomposition.[112] Much of the compositional calibration in the UHVCVD system used in this study displays a straightforward dependence on the ratio of GeH_4 to SiH_4 flow, as depicted in Figure 3.2 below. At high growth temperatures, where both SiH_4 and GeH_4 crack efficiently, composition varies roughly linearly with GeH_4 flow rate. At low growth temperatures, SiH_4 does not decompose as efficiently as GeH_4, so proportionally less GeH_4 is required to obtain the same composition.
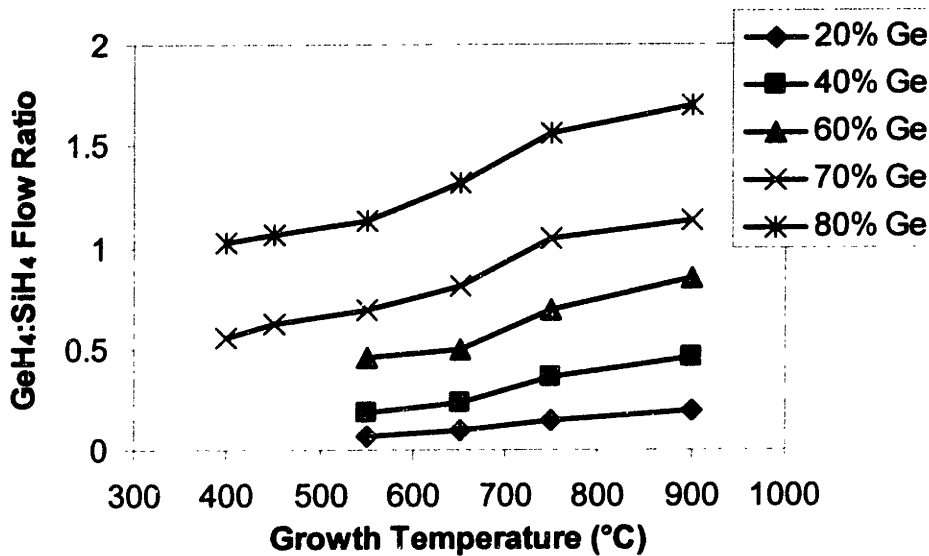
Figure 3.2 Experimentally determined ratio of GeH₄:SiH₄ flow necessary to obtain a given Ge composition as a function of growth temperature for the UHVCVD system used in this study.

Growth rates in general are more difficult to represent since they vary widely with growth temperature, pressure, and composition of gas phase reactants. However, some simple trends in growth rate are observed. For example, Figure 3.3 shows the growth rate of homoepitaxial Si, homoepitaxial $Si_{0.5}Ge_{0.5}$, and homoepitaxial Ge as a function of growth temperature. Generally, growth rate is relatively insensitive to temperature variation at high growth temperatures (where transport of reactants to the substrate surface limits growth rate), and falls off exponentially at low growth temperatures as decomposition of source gases becomes the rate limiting step in crystal growth. Note that for pure Si, the growth rate becomes impractically slow (< 0.1 Å/s) for growth temperatures below 550°C due to inefficient SiH_4 decomposition. By contrast, Ge growth rates are relatively high (> 1 Å/s) and roughly constant between 400°C and 650°C, indicating that mass transport, not source gas decomposition, limits growth rates. For $Si_{0.5}Ge_{0.5}$ alloys, overall

growth rates below 650°C are higher than for pure Si, since GeH_4 catalyzes SiH_4 decomposition.[19,113]
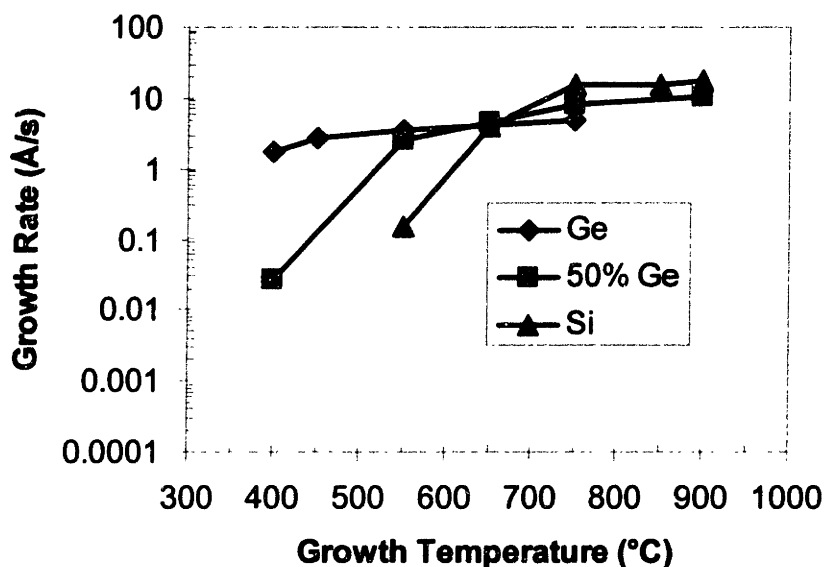
Figure 3.3 Growth rates of Si, $Si_{0.5}Ge_{0.5}$ and Ge as a function of growth temperature in the UHVCVD used in this study. Growth rates fall rapidly at low temperature, where cracking of source gases becomes the rate-limiting step in crystal growth.

At very low growth temperatures (< 550°C), where hydrogen desorption from the substrate surface becomes the rate limiting step, growth rates become even more difficult to calibrate. At low temperatures, growth rate also displays a strong dependence on the Ge content at the wafer surface, since hydrogen desorption kinetics are dependent on substrate Ge composition. For example, Figure 3.4 displays the growth rate of undoped Ge as a function of substrate Ge content at 400°C, where growth rate increases by over a factor of four between 50% Ge and pure Ge.
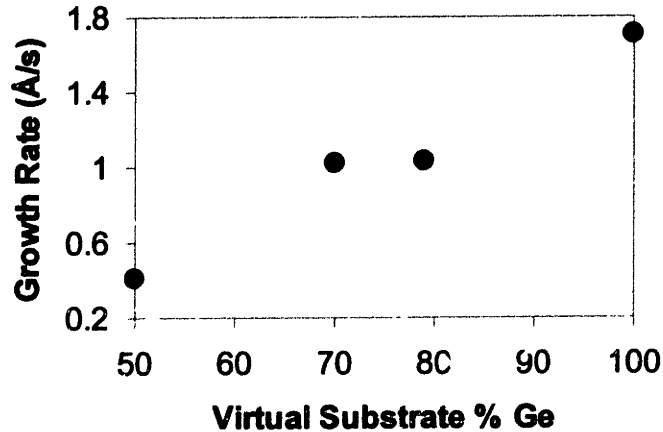
Figure 3.4 Growth rate of undoped Ge at 400°C as a function of virtual substrate Ge composition for the UHVCVD system used in this study. Growth rate increases rapidly as the crystal surface becomes more Ge-rich.

Further complicating calibration, Ge segregates towards the surface during UHVCVD growth above 515°C,[114] which "smears out" abrupt interfaces slightly and thus results in increased initial growth rates. These considerations necessitate extensive growth rate calibration at low growth temperatures.

Prior to growth, Si wafers are typically subjected to a 10 minute piranha clean (3:1 $H_2SO_4:H_2O_2$) followed by a 1 minute HF dip (10:1 $H_2O:HF$), which yields a clean hydrogen-terminated surface. For regrowth on SiGe virtual substrates after intermediate CMP step, an analogous procedure is employed. However, following CMP, wafers are subjected to two piranha cleans instead of one (to remove residual slurry contamination), with cleaning time reduced accordingly to avoid over-etching the SiGe layers. Wafers are then immediately loaded into the UHVCVD load-lock, which is pumped down for at least two hours, and typically overnight. Prior to growth, wafers are held at roughly 200°C for 30 minutes to desorb organics. Finally, immediately prior to growth, wafers are subjected to a high-temperature desorption step (typically 900°C) to remove native

oxide. A 1 μm homoepitaxial buffer layer is then deposited to bury any residual

impurities. Growth of SiGe layers proceeds after homoepitaxial buffer growth.

3.1.1.   Material Characterization

Effective growth of high quality compositionally graded SiGe layers requires multiple

characterization techniques to measure defect density, composition, strain, and surface

morphology. This section describes the techniques commonly employed in this thesis.

Transmission Electron Microscopy

Transmission electron microscopy (TEM) involves passing a high energy beam of

electrons through a thinned sample, either in cross-section or plan-view, to produce a

high-resolution image. TEM is useful for determining film morphology and thickness. A

typical low-magnification cross-sectional TEM image of a SiGe graded buffer is shown

in Figure 3.5 below.
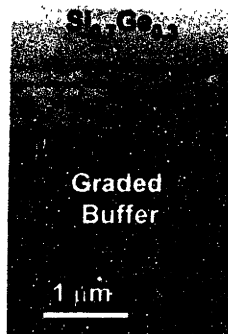
**Figure 3.5 Cross-sectional TEM of a compositionally graded SiGe buffer graded to
a final composition of 30% Ge.**

Under certain contrast conditions, TEM can also identify local strain fields, which

facilitates correlation of dislocation dynamics and surface morphology (see, for example,

Kim et al.[16]). Since dislocations may be directly imaged using this technique, TEM can

also be used to unambiguously measure dislocation densities under the correct contrast

condition. However, when using TEM to arrive at dislocation densities, one must be aware of the limits inherent in the technique. Because the sampling area in TEM is very small, in practice cross-sectional TEM has a threading dislocation detection lower limit of roughly 10^8 cm^{-2} while plan-view TEM has a threading dislocation detection lower limit of roughly 10^6 cm^{-2}. Unfortunately, the field of mismatched epitaxy is clouded by numerous claims of defect-free material made on the basis of cross-sectional TEM analysis. Furthermore, since dislocation pile-ups are spaced very far apart, TEM is unsuitable for accurately measuring dislocation pile-up densities. In general, then, TEM measurements of dislocation densities in low defect density material should always be confirmed with other wide-area techniques.

Etch-Pit Density Measurements

Selective etching is a useful technique for conducting large-area measurements of threading and misfit dislocation densities in SiGe films. An example of an optical micrograph in which selective etching was used to reveal dislocations was given in Figure 1.10. For SiGe alloys, standard dislocation etches utilized are either chromic acid- or iodine-based etches. The standard chromic acid etch, composed of 4 parts 0.3 molar aqueous CrO_3 to 5 parts concentrated HF, is commonly known as the Schimmel etch[115] and is useful for revealing dislocations in SiGe layers for Ge compositions less than 70%.[116] Occasionally, when the Schimmel etch failed to reveal threading dislocations, a more concentrated version of this etch was utilized.[117] The iodine etch,[118] a 5:10:11 mixture of HF, HNO_3, and CH_3COOH combined with 30 mg I_2 per 260 mL solution, is used for revealing dislocations in SiGe alloys above 70% Ge. Etch pits (in the case of threading dislocations) or etch lines (in the case of misfit dislocations) are readily

identifiable using Nomarski optical microscopy. Since the sampling area in optical microscopy is large, etch-pit density is a particularly important technique for measuring low defect densities and identifying dislocation pile-ups. However, selective etching can give anomalous results, particularly when dislocation densities are high and closely spaced etch pits cannot be resolved. Etch-pit density measurements can also be hampered by the extreme sensitivity of etch selectivity to film doping, background impurity concentration, and etch chemistry. Thus, detailed correlation of etch-pit density measurements with other techniques, such as plan-view TEM, is necessary for accurate determination of dislocation densities.

Throughout this thesis, both field threading dislocation densities and dislocation pile-up densities are commonly given. The accuracy of these measurements depends both on the sampling area and dislocation density. Through extensive measurements on a variety of samples, we have determined standard error for dislocation density measurements. Field threading dislocation densities are accurate to within 5% when above 10^6 cm^{-2}, and to within 10% when below this value. In contrast, because dislocation pile-ups are widely spaced, the error incurred when calculating their density is relatively large. For dislocation pile-up densities above 10^6 cm^{-2}, measurements are accurate to within 10%. For very low pile-up densities ($< 10^5$ cm^{-2}), measurements are only accurate to within 50%.

Atomic Force Microscopy

Tapping mode atomic force microscopy (AFM) maps the electrostatic deflection of a sharp stylus in close proximity to a sample surface, producing very high resolution three-dimensional images of surface morphology. For compositionally graded buffers, AFM is

useful for quantifying surface roughness resulting from the crosshatch morphology, as depicted in Figure 1.9. Since threading dislocations intersecting the sample surface leave small cusps at the surface, AFM can also be used to measure threading dislocation densities.[119] However, because practical scan areas in AFM are limited, this technique is only applicable when the threading dislocation is high. As with the other techniques described above, threading dislocation density measurements obtained by AFM should be compared with those obtained by other techniques.

RMS roughness values are commonly used in this work to quantify differences in surface morphology between different samples. As with dislocation density measurements, the accuracy of RMS roughness values depends on the sampling area, especially since crosshatch is a periodic phenomenon. For small scan areas (10 μm × 10 μm or less), we estimate that RMS roughness values are accurate to within 25%. For large scan areas (25 μm × 25 μm or more), we estimate that RMS roughness values are accurate to within 10%. These estimates are based upon measurements on a wide variety of graded buffer samples.

Triple-Axis X-ray Diffraction

Triple-axis x-ray diffraction (TAXRD) is a high resolution x-ray diffraction technique capable of accurately resolving strain and composition in compositionally graded buffers. In TAXRD, the x-ray beam is conditioned by crystals before and after diffracting off the sample surface, producing a highly monochromatic beam and filtering out intensity resulting from sample bow.[120] Simple double-axis $\theta/2\theta$ scans, where the crystal located between the sample and detector is removed to increase intensity and decrease scan time, are a quick and convenient method for determining SiGe film composition, and are most

accurate when the film is fully relaxed. An example of a $\theta/2\theta$ scan obtained from a

compositionally graded SiGe buffer layer is given in Figure 3.6 below.
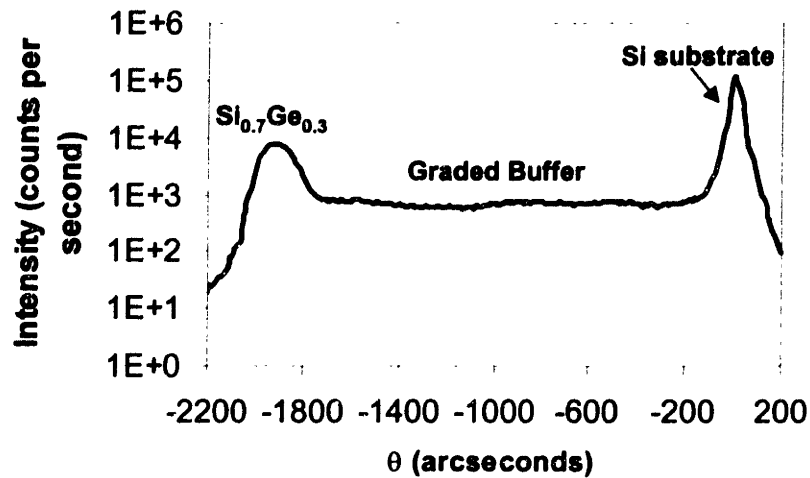
Figure 3.6 Example of an (004) $\theta/2\theta$ scan obtained from a compositionally graded SiGe buffer graded to a final Ge composition of 30%.

Triple-axis reciprocal space maps, in which a series of $\theta/2\theta$ scans are taken at various θ

values, are useful for determining strain and composition and are in general more

accurate than $\theta/2\theta$ scans. An example of a reciprocal space map obtained from a

compositionally graded SiGe buffer layer is given in Figure 3.7 below.
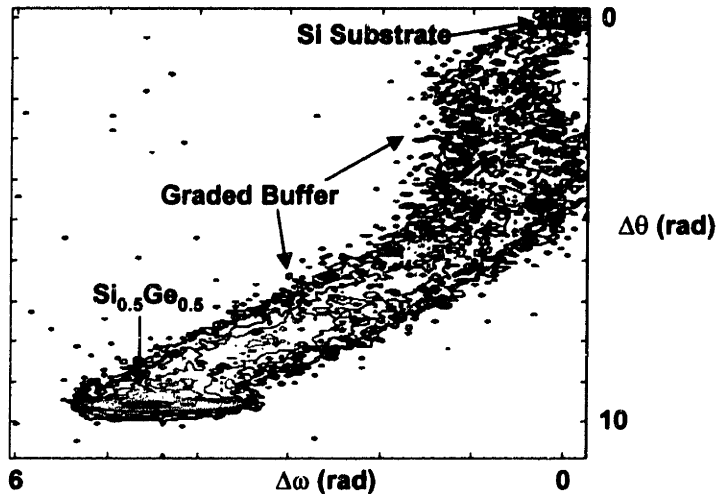
Figure 3.7 Example of an (004) reciprocal space map obtained from a compositionally graded SiGe buffer graded to a final Ge composition of 50%.

Depending on the sample, one or both of these techniques are used for determining strain and composition. Generally, we have found that composition measurements are accurate to within 1% Ge and strain measurements are accurate to within 10^{-4}. A detailed discussion of analysis of compositionally graded SiGe layers by TAXRD is given in Appendix A.

Other Characterization Techniques

Spreading resistance profiling was generally used to determine doping levels in SiGe graded buffers.[121] This method involves beveling a wafer and measuring resistivity along the bevel. With a known bevel angle, a depth profile of resistivity (and thus doping) can be obtained. To determine residual impurity concentrations in SiGe graded buffers, secondary ion mass spectrometry (SIMS) was commonly employed.[122] SIMS involves sputtering away the sample at a known rate and measuring the composition of the resulting ion flux, which produces a depth profile of film composition. Finally, to determine Ge composition at the surface of device heterostructures, a combination of vapor phase decomposition (VPD) and spectroscopy techniques was used.[123] In VPD, the

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first few atomic layers of the film surface are etched in hydrofluoric acid vapor and collected in solution. The solution is then analyzed by spectroscopy, which gives a very sensitive measurement of surface composition.

3.2.   Short Flow MOSFET Process

Device fabrication itself provides an indirect means of analyzing material quality and represents the ultimate measure of the utility of SiGe-based technology. In this thesis, metal-oxide-semiconductor field-effect transistors (MOSFETs) were fabricated by a short flow process.[104] Electrical measurements of completed devices were used to extract effective mobility versus effective vertical field and to assess the potential of various SiGe heterostructures.

3.2.1.   Motivation for the Short Flow MOSFET

As described in Section 2.1, extraction of effective carrier mobilities is important for accurate assessment of SiGe device performance. However, a typical MOSFET process involves a minimum of four lithography steps and takes several months to complete in a university lab. At MIT, a novel short flow process, requiring only one lithography step and capable of completion in less than two weeks, has been developed to quickly explore different SiGe heterostructure MOSFET variants.[104] The short flow MOSFET process yields long-channel devices, but the high vertical fields present in the inversion layer of these devices simulate conditions in short-channel MOSFETs. Thus, effective mobility, which represents the most important performance metric for SiGe heterostructure devices, can be extracted at vertical fields approaching those used in state-of-the-art CMOS devices. However, no other important device performance metrics (e.g. subthreshold slope, leakage currents) can be meaningfully extracted. Nevertheless, the

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importance of the short flow MOSFET process cannot be overstated, since it enables

rapid evaluation of SiGe heterostructure MOSFETs. For this thesis, over 150 different

wafers, involving over 60 different SiGe heterostructures, were subject to the short flow

process. A typical MOSFET fabrication process would not allow such rapid turn-around

and would severely limit the scope of this work. Based on measurements from short flow

MOSFETs, the most promising heterostructures may then be subjected to advanced

MOSFET fabrication processes to obtain more detailed device performance metrics.

3.2.2.   MOSFET Fabrication Process

The short flow MOSFET process was used to rapidly fabricate ring transistors at

MIT's Microsystems Technology Laboratory (MTL). A complete description of the MIT

short flow MOSFET process, complete with MTL machine names, is given in Appendix

Deposit gate stack   **Pattern gate stack**   **BOE undercut**

**Implant source/drain/gate
& RTA**   **E-beam metallization**
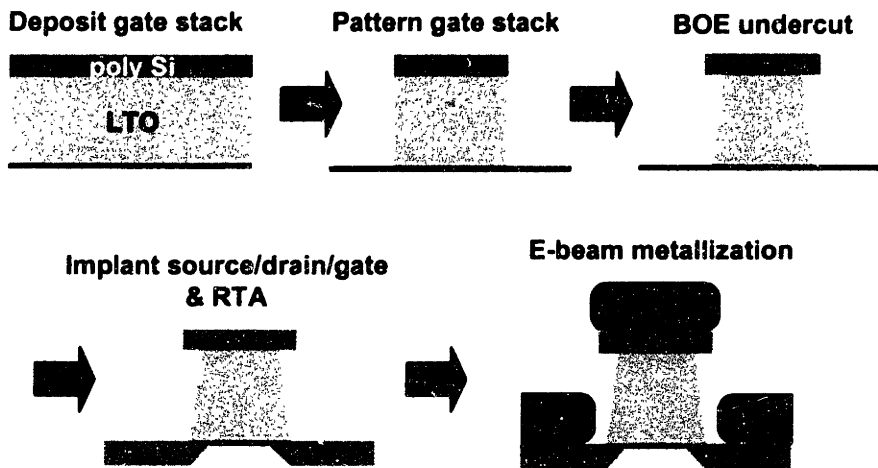
B, while a schematic of the short flow process is given in Figure 3.8 below.

**Figure 3.8 Short flow MOSFET process schematic. Since the geometry of metal
deposition results in an electrically isolated source, gate, and drain, transistors can
be fabricated in a single lithography step.**

The first step in the short flow MOSFET process is gate stack formation. First, wafers

are subjected to a modified RCA clean, designed to minimize etching of thin strained Si

surface layers. A standard RCA clean is composed of a 10 minute SC-1 step (5:1:1 $H_2O:H_2O_2:NH_4OH$ held at 80°C), a 15 second 50:1 $H_2O:HF$ dip, and a 15 minute SC-2 step (6:1:1 $H_2O:H_2O_2:HCL$ held at 80°C). The SC-1 clean removes organic contaminants from the surface while the SC-2 clean removes metal contaminants. However, the SC-1 step etches Si, and is thus unsuitable for cleaning thin strained Si layers. Therefore, in the short flow process, the SC-1 step has been replaced by a 10 minute piranha clean (3:1 $H_2SO_4: H_2O_2$), which serves a similar function without severely etching silicon. For SiGe heterostructures with very thin Si surface layers, cleaning times are also reduced (to a 5 minute piranha clean and a 2.5 minute SC-2 clean) to further protect the surface. Following the modified RCA clean, wafers are immediately loaded into a low-temperature oxidation (LTO) tube, where 3000 Å of SiO_2 is deposited at 400°C. Previous measurements of MIT LTO confirm that the interface state density is comparable to thermally grown SiO_2.[104] While the modified RCA clean is designed to minimize material removal, the combination of a modified RCA clean and LTO deposition (in which the first few Si layers are thermally oxidized) removes about 20 Å of Si. Following LTO deposition, 500 Å of undoped poly-Si is deposited via LPCVD at 560°C to complete the gate stack.

The next step in the short flow MOSFET process involves clearing the backside poly-Si and LTO to facilitate a good backside electrical contact. Wafer frontsides are coated with 1 μm photoresist, and the backside poly-Si is dry-etched in an HBr/Cl_2 plasma. Wafers are then subject to a 30 second buffered oxide etch (BOE) to remove the backside LTO. Finally, photoresist is removed either by ashing or a 10 minute etch in piranha solution.

Next, the source, drain, and gate regions are defined in the only lithography step in the process. Wafers are coated in 1 μm positive photoresist and exposed through the MOBIL mask developed at MIT, which has ring transistors with gate lengths between 50 μm and 500 μm. Following development, the frontside poly-Si is dry-etched in an HBr/Cl$_2$ plasma and the frontside LTO is dry-etched in a CHF$_3$/O$_2$ plasma. The LTO etch is timed to leave roughly 250 Å of LTO remaining, which prevents etching-induced surface damage. Next, wafers are ashed to remove the photoresist. Finally, wafers are subjected to a 30 second BOE etch to remove the remaining LTO over the source and drain and slightly undercut the gate region, forming a T-gate geometry. This undercut is necessary for the metal deposition step.

Wafers are next subjected to a blanket ion implantation step, performed by an outside vendor, in which the source, drain, and gate poly-Si are implanted simultaneously. For p-MOSFETs (n-MOSFETs), the implantation species is BF$_2$ (As), implanted at 35 keV with a dose of 1 × 10^{12} ions/cm^{-2}. Four identical implants are performed, each at a 90° rotation, to prevent shadowing effects resulting from the ring geometry. Upon reintroduction to the clean room, wafers are subject to a brief piranha clean and annealed in N$_2$ for 30 minutes at 600°C.

Finally, device metallization is performed. First, the wafers are subjected to a brief pre-metallization clean, consisting of a 1 minute piranha clean and a 20 second 50:1 H$_2$O:HF dip. Normal incidence electron beam evaporation is then used to deposit 500 Å Ti and 1000 Å Al. The extreme geometry of the T-gates, coupled with normal incidence evaporation, ensures that metal lines break between the raised gates and the source/drain regions, isolating these regions without use of another patterning step. Next, 5000 Å of

Al is deposited via electron beam evaporation on the backs of the wafers, and wafers are sintered in an H_2/N_2 atmosphere at 400°C for 30 minutes to create good electrical contacts and reduce interface state density.

3.2.3. Carrier Mobility Extraction

A top view of the final short flow ring transistor structure is given in Figure 3.9 below.
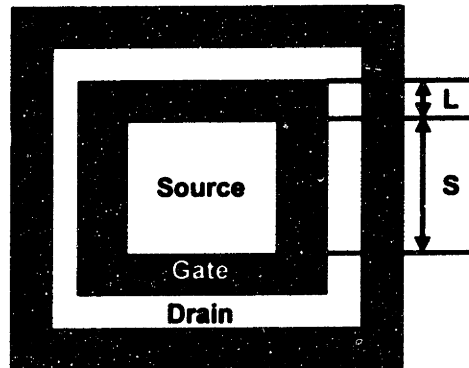
Figure 3.9 Top view of short flow MOSFET ring transistor with relevant device dimensions indicated.

Typically, transistors with a gate length of 200 μm were measured. The other relevant dimensions of this transistor, including the geometry factor, G, necessary for carrier mobility extraction, are given in Table 3.1 below.

Table 3.1 Relevant dimensions of MOSFETs characterized in this work.

L (μm)	200
S (μm)	250
A_{gate} (μm^2)	360,000
G	.138

As described in section 2.1, effective mobility is extracted from measurements of drain current in the linear regime, given by

$$I_D = \frac{W}{L} \mu_{eff} C_{ox} (V_{GS} - V_T) V_{DS}$$

where *W/L* is replaced by the inverse of the geometry factor cited in Table 3.1.[104] With the appropriate substitution, effective mobility is expressed as

$$\mu_{eff} = \frac{GI_D}{C_{ox}V_{DS}(V_{GS} - V_T)}$$

where C_{ox} is the oxide capacitance, V_T is the threshold voltage, and V_{GS} is the applied gate-source voltage. For all device measurements, V_{DS} was fixed at 0.1 V.

Effective vertical field[39,40] is given by

$$E_{eff} = \frac{Q_b + \eta Q_{inv}}{\varepsilon_s}$$

where Q_b is the bulk depletion charge in the semiconductor, η is a dimensionless fitting parameter ($\eta = 1/3$ for holes and $1/2$ for electrons), Q_{inv} is the inversion layer charge, and ε_s is the dielectric constant of the substrate. Because of uncertainties in substrate doping, bulk charge cannot be expressed via the typical $N_a x_{d,max}$ approximation. Instead, bulk charge was approximated by considering the electrostatics of the oxide/semiconductor interface.[4] For electric displacement continuity at this interface,

$$E_{ox}\varepsilon_{ox} = E_s\varepsilon_s$$

where E_{ox} is the gate oxide electric field, E_s is the field at the semiconductor surface, and ε_{ox} and ε_s are the oxide and semiconductor dielectric constants, respectively. From Gauss' Law,

$$E_s = \frac{Q_{inv} + Q_b}{\varepsilon_s}.$$

Combining the above three equations yields

$$E_{eff} = \frac{E_{ox}\varepsilon_{ox} - Q_{inv}(1 - \eta)}{\varepsilon_s}.$$

Finally, Q_{inv} is taken as $C_{ox}(V_{GS} - V_T)$, and E_{ox} was assumed to equal V_{GS}/t_{ox} where t_{ox} is the oxide thickness. The latter formula is only valid for $V_{DS} \ll V_{GS}$. Combining these assumptions yields the computed effective vertical field:

$$E_{eff} = \frac{C_{ox}(V_T + \eta(V_{GS} - V_T))}{\varepsilon_s}.$$

From these formulas, effective mobility versus effective vertical field curves for bulk Si and SiGe heterostructure based MOSFETs were compared to universal curves. Mobility measurements are accurate to within 10% at low vertical fields (< 0.3 MV/cm), and the accuracy of these measurements increases with increasing vertical field.[124,125] For SiGe heterostructure MOSFETs, mobility enhancement (the ratio of effective mobility in a SiGe heterostructure device to a coprocessed bulk Si MOSFET at the same effective vertical field) is often given to normalize mobility values and facilitate comparison between various heterostructures.

Chapter 4.   Dislocation Dynamics in Compositionally Graded SiGe

As described in Section 1.5, the model for strain relaxation in graded buffers begins with the assumption that the final threading dislocation density (TDD) in a compositionally graded SiGe buffer is controlled by dislocation glide kinetics. This glide kinetics model predicts that the evolution of threading dislocation density with growth temperature can be related to the activation energy for dislocation glide[16] and that, assuming constant growth and grading rates, the final threading dislocation density should be independent of final Ge composition. However, as discussed earlier, the former conclusion had not been tested in SiGe/Si and the latter conclusion was not supported by early experimental evidence. With control over dislocation pile-ups in SiGe, the dislocation glide kinetics theory that was successfully implemented in InGaP/GaP[16] can now be applied to SiGe/Si. Since the SiGe materials system does not suffer from decomposition or branch defect formation, it should prove to be an ideal test of the glide kinetics model. In this chapter, the glide kinetics model is extended to the $Si_{1-x}Ge_x$/Si system and the influence of pile-up formation on threading dislocation density in $Si_{1-x}Ge_x$/Si is explored.

4.1.   Overview of Compositionally Graded SiGe Buffer Growth and Characterization

Two sets of samples, labeled glide kinetics and reduction, were grown in this study. The glide kinetics series was grown to explore the kinetics of strain relaxation in compositionally graded SiGe/Si. The reduction set was grown to calculate dislocation reduction rates in compositionally graded SiGe/Si. All samples were grown in the hot-wall UHVCVD system described in Section 3.1, on Si(001), Si(001) offcut 6° towards a <110>, and Si(001) offcut 6° towards a <100>. Growth temperatures varied between

650°C and 900°C, while typical growth pressures and growth rates were 25 mTorr and 10 Å/s, respectively.

The glide kinetics series was intended to consist of identical growths conducted at different temperatures and deposited on different substrate offcuts. Samples used in the dislocation glide kinetics portion of this study consisted of n-type compositionally graded layers, graded at 10% Ge/μm (2000 Å jumps of 2% Ge) to 30% Ge. A uniform composition cap was then deposited, consisting of 1.5 μm of undoped $Si_{0.7}Ge_{0.3}$, followed by 1000 Å p^+-doped $Si_{0.7}Ge_{0.3}$. All portions of this growth were conducted at the same temperature. The built-in p-i-n structure was intended to facilitate electron beam induced current (EBIC) measurements; spreading resistance measurements revealed that the buffer was typically doped $\sim 10^{18}$ cm^{-3} while the final portion of the uniform composition cap was doped $\sim 10^{19}$ cm^{-3}. A spreading resistance profile in the 900°C sample showed that the doping level in the p-type cap was too low. As a result, this sample was regrown with an additional 1 μm p-type $Si_{0.7}Ge_{0.3}$ cap layer and a thin strained silicon layer deposited at 650°C (to aid etch pit density measurements). All defect measurements were done on the regrown samples. This redeposition process should not significantly change the threading dislocation density of these samples.

The dislocation reduction growths began with a compositionally graded buffer graded to 15% Ge at 650°C and 25 mT. The growth temperature was then raised to 900°C, and the compositional grading to 30% Ge was completed. A 3 μm-thick uniform composition $Si_{0.7}Ge_{0.3}$ cap was then deposited at 900°C and 25 mT.

Cross-sectional and plan-view transmission electron microscopy (TEM), using JEOL 2000FX and JEOL 200CX microscopes, was performed to examine microstructure.

Triple axis x-ray diffraction (TAXRD), using a Bede D^3 diffractometer with a Rigaku rotating anode source, was used to measure composition and strain relaxation. Surface morphology was characterized by tapping mode atomic force microscopy (AFM) using a Digital Instruments Dimension 3000 Nanoscope IIIa system. Defect densities were measured with etch pit density (EPD), using standard chromic acid-based etchants and a Zeiss Axioplan optical microscope in differential interference contrast (DIC) mode. Field dislocation densities (ρ_{field}) were calculated by counting the number of etch pits per unit area that were located away from pile-ups. Pile-up densities ($\rho_{pile-up}$) were calculated by counting the number of etch pits per unit length of pile-up (ρ_{thread}) at high magnification and multiplying that number by the linear density of pile-ups (ρ_{linear}), measured at low magnification:

$$\rho_{pile-up} = \rho_{linear} \times \rho_{thread} \, .$$

4.2.   Strain Relaxation Kinetics in Compositionally Graded SiGe

Figure 4.1 is a plot of field dislocation density (ρ_{field}) versus growth temperature for the three different substrate types in the glide kinetics series. A clear increase in ρ_{field} as growth temperature is reduced emerges for the on-axis samples, while the samples deposited on offcut substrates exhibit more complicated behavior.
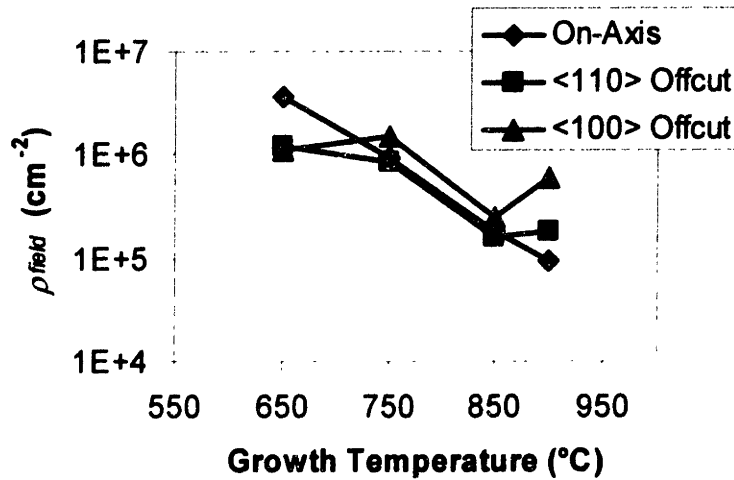
Figure 4.1 Field threading dislocation versus growth temperature for the three different substrate offcuts investigated. Generally, field threading dislocation density decreases with increasing growth temperature.

Figure 4.2 is a plot of the total density of threading dislocations trapped in pile-ups ($\rho_{pile-up}$) in glide kinetics samples versus growth temperature. Note that $\rho_{pile-up}$ also generally decreases with increasing growth temperature but that, with only one exception, $\rho_{pile-up}$ is always at least 4-5 times lower than ρ_{field}.
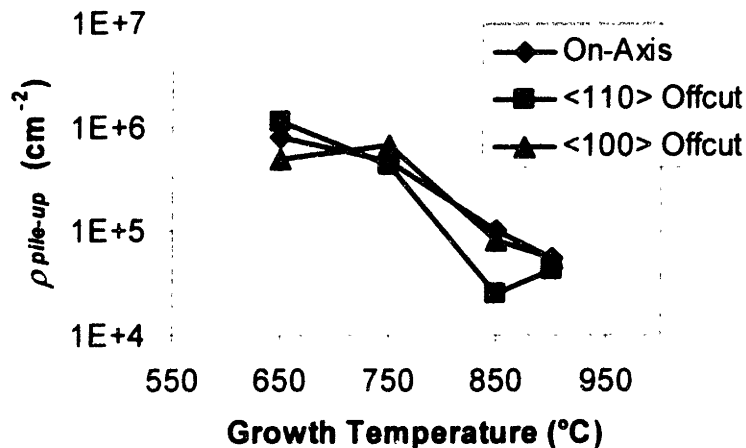
Figure 4.2 Total density of threading dislocations trapped in pile-ups versus growth temperature for the three different substrate offcuts investigated. Dislocation pile-up density decreases with increasing growth temperature.

The glide kinetics series was grown to examine, in the case of $Si_{0.7}Ge_{0.3}/Si_{1-x}Ge_x/Si$, a kinetic model for strain relaxation in compositionally graded buffers developed by Kim *et al.*[16] The basis of this model is the assumption that, in the absence of dislocation blocking, the overall TDD (ρ) of a graded buffer is set by the dislocation glide velocity and hence can be related to the activation energy for dislocation glide for a given material:

$$\rho = A \exp\left(\frac{E_{glide}}{kT} \right),$$

where A is a temperature-independent constant, E_{glide} is the activation energy for dislocation glide, and T is the growth temperature. Thus, assuming that relaxation is glide-limited (*i.e.*, that impediments to dislocation flow are not forcing the nucleation of more threading dislocations), a plot of $\ln(\rho)$ versus $1/T$ should be linear with slope equal to $k \times E_{glide}$. Such a plot is shown in Figure 4.3, where the calculated activation energy for dislocation glide in the on-axis $Si_{0.7}Ge_{0.3}$ samples is 1.4 eV. The evolution of TDD with growth temperature for samples deposited on offcut substrates is more complex and cannot be fitted to a single activation energy. The discussion will therefore begin by examining the on-axis glide kinetics samples and build towards an explanation of TDD evolution with growth temperature in offcut samples.
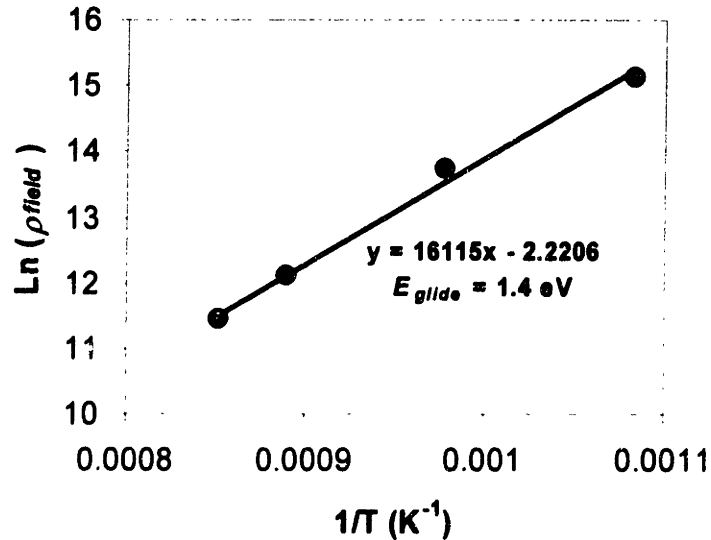
Figure 4.3 Fit of ρ_{field} **versus** $1/T$ **to obtain** E_{glide} **for on-axis glide kinetics samples. The extracted value of the activation energy for dislocation glide in this series is 1.4 eV.**

Accepted values for E_{glide} are 2.25 eV for Si and 1.65 eV for Ge.[25] Note that both of these values are significantly higher than the value for $Si_{0.7}Ge_{0.3}$ calculated from the glide kinetics series. The accepted values for dislocation glide in Si have also been confirmed by numerous *ex situ*[24,126,127] and *in situ*[128] annealing studies of dislocation motion in single $Si_{1-x}Ge_x$/Si layers ($x < 0.35$). Furthermore, the n-type doping in the graded region cannot account for the measured difference in the activation energy for dislocation glide.[129,130] This implies that strain relaxation in the on-axis glide kinetics samples is not controlled solely by dislocation glide. Possible sources of deviation from ideal glide-limited relaxation will be examined below.

4.2.1. Extracting Dislocation Glide Activation Energies in Samples Grown on On-Axis Substrates

One possible deviation from ideal glide-limited relaxation could arise from changes in dislocation mobility with surface morphology. In compositionally graded layers, the

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surface morphology and defect density are linked, since deep crosshatch can lead to

dislocation pile-up formation.[29] A similar mechanism could be responsible for the

apparent low activation energy for dislocation glide in on-axis glide kinetics samples.

Figure 4.4 is a plot of RMS roughness (R_q) versus growth temperature for all glide

kinetics samples, for both 10×10 µm and 25×25 µm scan areas.
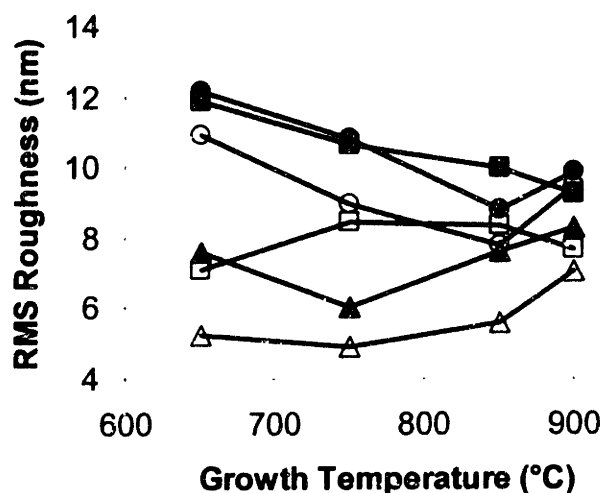
Figure 4.4 RMS roughness versus growth temperature for glide kinetics samples deposited on on-axis substrates (circles), substrates offcut towards a <110> (squares), and substrates offcut towards a <100> (triangles). Closed symbols are for 25 × 25 µm scans, and open symbols are for 10 × 10 µm scans.

While there are relatively small changes in RMS roughness (~ 3 nm) over the

temperature range investigated, dislocation motion becomes more sluggish at low

temperature. Therefore, the same surface roughness at low growth temperatures can

arrest dislocation glide more easily. A key assumption in the dislocation glide kinetics

model is that the low strain rates employed during graded buffer growth act to suppress

dislocation nucleation. However, accumulated strain during grading at low temperature

can result in dislocation nucleation in the graded region. Dislocation glide displays a

roughly linear or parabolic dependence on strain:

$$v \propto \varepsilon^m \, exp\left(\frac{-E_{glide}}{kT}\right),$$

where v is the dislocation glide velocity, ε is the strain, and m is a dimensionless

exponent that can vary between 1 and 2 depending on the choice of fitting constants.[24]

Unlike dislocation glide rates, heterogeneous dislocation nucleation rates in general

cannot be precisely calculated. However, Fitzgerald et al.[8] proposed that the functional

dependence of heterogeneous dislocation nucleation is identical to that of homogeneous

dislocation nucleation. Since dislocation nucleation is exponentially sensitive to strain:

$$\dot{\rho}_{nuc} \propto exp\left(\frac{-E_{nucleation}}{C\varepsilon T}\right),$$

where $\dot{\rho}_{nuc}$ is the nucleation rate, $E_{nucleation}$ is the activation energy for dislocation

nucleation and C is a constant, increases in strain with a decrease in growth temperature

will result in a small increase in dislocation velocity and large increase in dislocation

nucleation.[8] Thus, the measured value of E_{glide} for glide kinetics samples may reflect

both dislocation nucleation and glide kinetics.

To test this hypothesis, TAXRD was used to measure residual strain in on-axis glide

kinetics samples. Figure 4.5 is a plot of as-grown strain versus growth temperature for

these samples. As-grown strain is defined as residual strain minus thermal strain

resulting from cooling from growth temperature to room temperature.
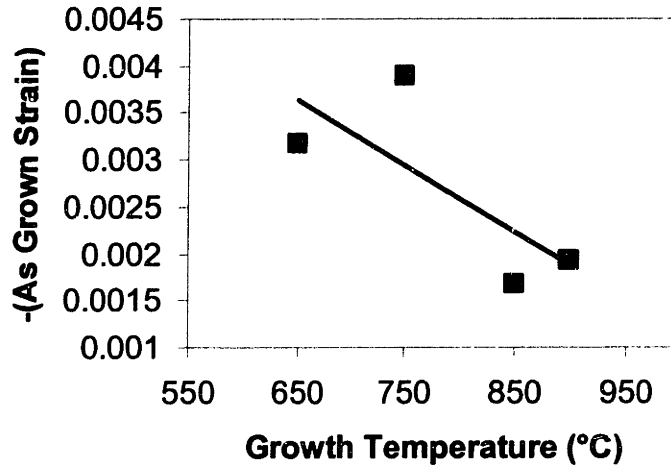
Figure 4.5 As-grown strain versus growth temperature for glide kinetics samples. As-grown strain drops with increasing growth temperature, possibly indicating that strain is accumulating during graded buffer growth at low temperature.

In general, as-grown strain increases as growth temperature is reduced. Each glide

kinetics sample was capped with a 1.5 μm uniform composition layer, making direct

measurement of accumulated strain in the graded region prior to deposition of the cap

layer impossible. Furthermore, separating the influence of glide and nucleation in a

graded buffer is a difficult task, since such a model would require detailed knowledge of

the nucleation mechanism. However, from the TAXRD measurements, it is possible to

fit on-axis glide kinetics trends to an empirical model that takes into account changes in

strain with growth temperature. Figure 4.6 compares the evolution of field TDD with

growth temperature in on-axis glide kinetics samples with the expected ideal glide-

limited dependence.
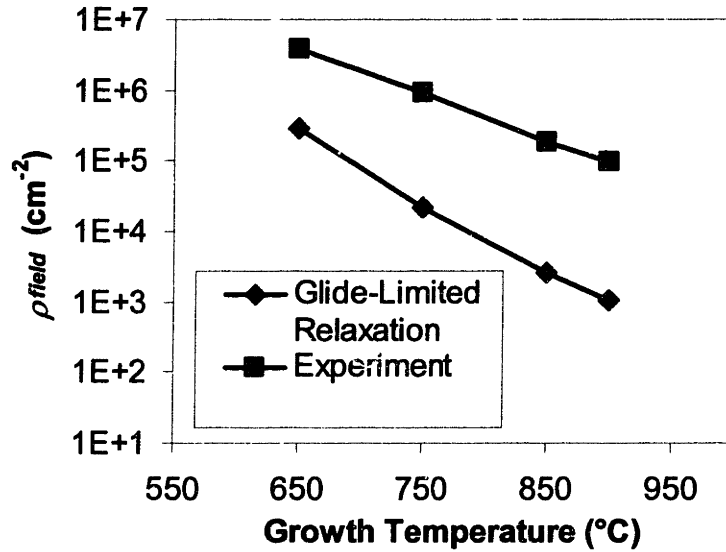
Figure 4.6 Experimental and theoretical variation (taking E_{glide} to be 2.25 eV) of field threading dislocation density for on-axis glide kinetics samples. The gap between the theoretical variation and experimental measurements reflects the influence of dislocation nucleation processes on field threading dislocation density.

In this figure, the intercept of the glide-limited threading dislocation density line is

arbitrary, since this value is dependent on experimental parameters; we can only specify

that its slope is set by dislocation glide kinetics. However, by definition, this line cannot

be above experimental data since it represents the lowest dislocation density obtainable.

Figure 4.7 is a plot of the strain (normalized to the strain value at 650°C) needed to bring

on-axis glide kinetics samples' TDD into accordance with the expected variation (E_{glide} =

2.25 eV) using an empirical fit:

$$\rho \alpha \frac{1}{\varepsilon^m(T)} exp\left(\frac{E_{Glide}}{kT}\right),$$

where we have set m equal to 2.[18] In this figure, we have expressed all strain values as

$\varepsilon(T)/\varepsilon(650\,°C)$ since, as described above, we cannot specify a unique glide-limited

threading dislocation density. The above equation was derived by relating the rate of

strain relief in a graded buffer to growth conditions and solving for the threading

dislocation density required to relieve this strain.[18] Again, this is an empirical fit that does not specifically account for the effects of dislocation nucleation (which would require another fitting parameter); however, as seen in Figure 4.7, this equation generally supports TAXRD measurements.
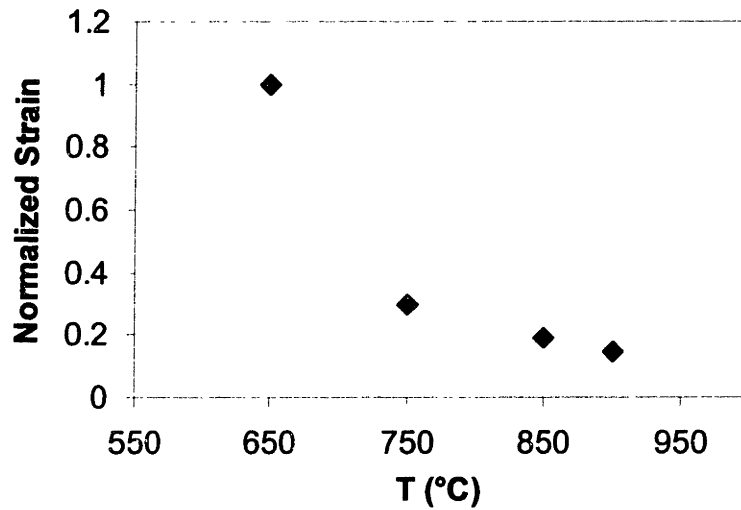
Figure 4.7 Calculated variation of strain with growth temperature needed to account for the difference between theory and experiment. Strain needs to decrease with increasing growth temperature to account for this difference, a hypothesis supported by TAXRD measurements.

4.2.2.   Extension to Samples Grown on Offcut Substrates

The final mechanisms influencing the field TDD of glide kinetics samples are dislocation reduction reactions. The two mechanisms for dislocation reduction in a compositionally graded buffer are dislocation annihilation and dislocation fusion.[131] For a compositionally graded buffer, dislocation reduction reactions are driven by dislocation glide.

For the glide kinetics series, on-axis samples grown at 900°C have a lower field TDD than offcut samples. This trend can be understood by considering the effect of substrate

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offcut on active slip systems. When SiGe layers are deposited on on-axis Si substrates, the resolved shear stress on the eight active slip systems is equal for all <110> directions. However, substrate offcut breaks this degeneracy, resulting in higher resolved shear stresses in some slip systems and lower resolved shear stresses in others.[132] For SiGe films deposited on Si(001) offcut 6° towards an in-plane <110>, the eight-fold degeneracy in resolved shear stress is broken into two four-fold degenerate slip systems. For SiGe films deposited on Si(001) offcut 6° towards an in-plane <100>, the eight-fold degeneracy in resolved shear stress is broken into four two-fold degenerate slip systems. This imbalance leads to a net Burgers vector content in the film, which has been shown both theoretically[133,134] and experimentally[135] to lead to saturation in dislocation reduction reactions. This trend is evidenced by the increase in field TDD for offcut glide kinetics samples at 900°C. The net Burgers vector content becomes greater for the <110> offcut and is greatest for the <100> offcut, which is reflected by the respective increase in field TDD for these samples.

The dislocation reduction set was grown to test the strength of dislocation reduction reactions in graded SiGe. These samples consisted of a grade to 15% Ge at 650°C and continued grading to 30% Ge at 900°C, deposited on the three substrate types described above. The low temperature portion of this growth seeded the buffer with an excess concentration of threading dislocations, which were free to annihilate or fuse during the high temperature portion of the grade. For the on-axis reduction sample, the measured field TDD is 1.1×10^6 cm^{-2}. This TDD is roughly four times lower than that which results from grading to 30% Ge at 650°C exclusively, but about an order of magnitude higher than that which results from grading to 30% Ge at 900°C exclusively. This result

indicates that dislocation reduction reactions occurred but could not fully erase the excess concentration of threading dislocations in this sample. In contrast, offcut samples grown by this two step grade process exhibited little or no net drop in threading dislocation density when compared to the field TDD resulting from grading to 30% Ge at 650°C exclusively. The reduction sample deposited on the <110> offcut substrate had a field TDD of 1.2×10^6 cm^{-2} (compared to 1.2×10^6 cm^{-2} for the 650°C grade). Furthermore, the reduction sample deposited on the <100> offcut substrate exhibited a *rise* in field TDD when compared to the 650°C grade, to 3.2×10^6 cm^{-2} (compared to 1.1×10^6 cm^{-2} for the 650°C grade). These results indicate that, as predicted, dislocation reduction reactions are not occurring as efficiently in the offcut reduction samples.

4.3.   Exploring the Link Between Field Dislocations and Dislocation Pile-Ups

When examining threading dislocation densities of various graded SiGe samples, an increase in field TDD with overall accommodated mismatch occurs. Since the field TDD is set by the growth temperature and grading rate, we would expect a constant field threading dislocation density over the entire range of Ge composition. While an increase in pile-up density is expected, the presence of dislocation pile-ups should not influence field threading dislocation density. By definition, threading dislocations trapped in pile-ups cannot contribute to strain relief. Thus, when a field dislocation becomes trapped in a pile-up, another must nucleate in the field to compensate, resulting in zero net change in field TDD.

However, a close look at the variation of field and pile-up TDD in glide kinetics samples indicates that they both follow the same general trends. Furthermore, Figure 4.8

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plots field threading dislocation density versus pile-up density for a variety of graded $Si_{1-x}Ge_x$ samples $(0.3 \le x \ge 1)$ grown at temperatures between 550°C and 900°C. The correlation between field TDD and pile-up TDD can be seen on this plot.
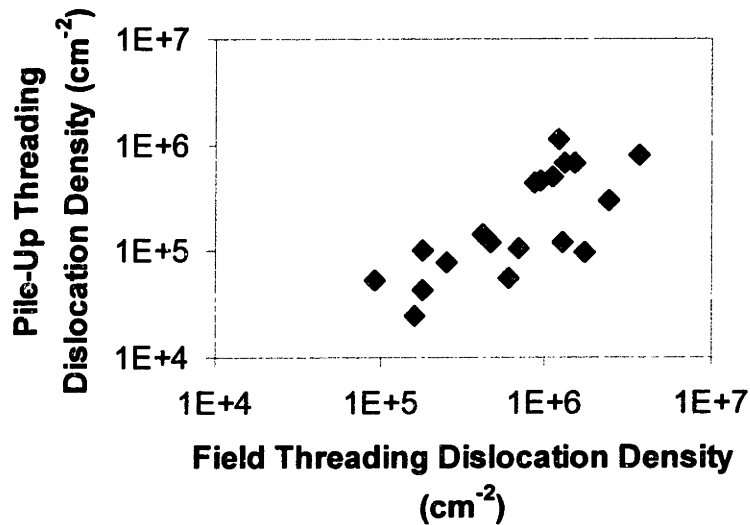
Figure 4.8 Field threading dislocation density versus pile-up density for selected SiGe samples. Field threading dislocation density and pile-up density increase concomitantly.

Figure 4.9 is a plot of threading dislocation densities versus Ge content, again for a wide variety of growth conditions. The increase in field TDD between 30% Ge and 50% Ge is mirrored by the increase in pile-up TDD in this composition range.

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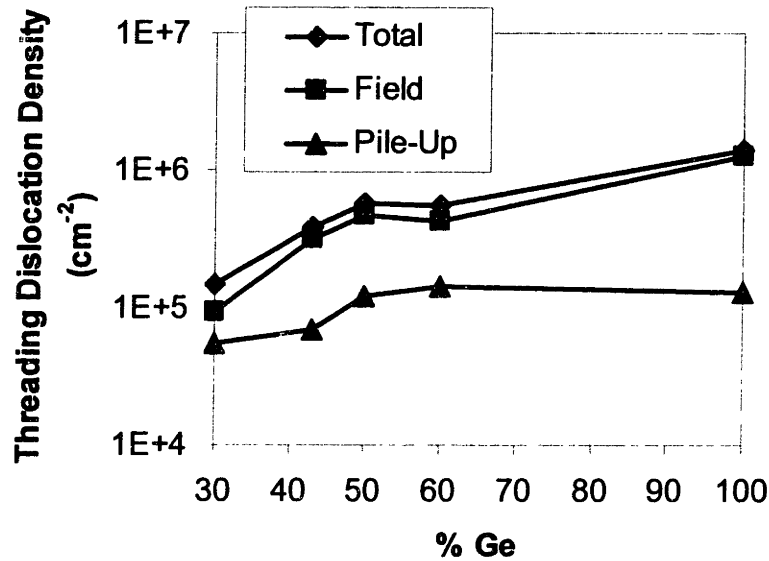
Figure 4.9 Defect density versus Ge content for selected SiGe samples. Both field threading dislocation density and dislocation pile-up density increase beyond 30% Ge.

The link between dislocation pile-up formation and increases in field TDD has been discussed previously.[8] The authors theorized that the same interaction between surface morphology and strain fields that causes pile-up formation can also be a source of extrinsic drag on field threading dislocations. The relationship between field and pile-up TDD could also arise from the influence of dislocation pile-ups on adjacent gliding threading dislocations. Figure 4.10 depicts an idealized surface of a compositionally graded layer. In this illustration, dislocation pile-ups form cell walls that restrict threading dislocation motion.
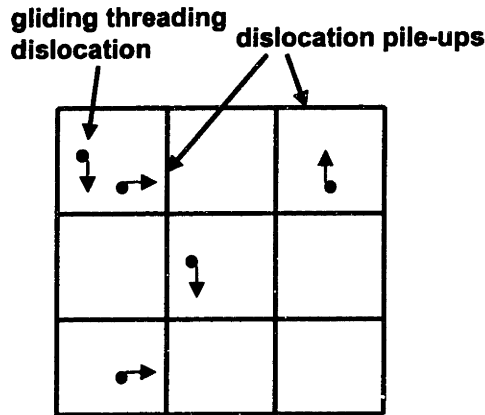
Figure 4.10 Plan-view of cellular structure emerging from dislocation pile-up formation. Dislocation pile-ups form boundaries that restrict gliding threading dislocation motion.

While a gliding threading dislocation can move within its cell, its movement could be restricted as it nears a pile-up. In the language of surface morphology, the stress fields of the threading dislocations in the pile-up add to create an even larger area of reduced effective strain. Thus, threading dislocation velocities in one cell drop, reflecting the drop in effective stress. In the regime where mean glide lengths are lower than mean pile-up spacing, we expect that field TDD would be independent of pile-up density. However, low dislocation velocities require low growth temperatures, the regime where dislocation pile-up formation is most severe. We would thus expect that pile-up formation will in general be accompanied by a rise in field TDD.

Returning to the glide kinetics samples, the increase in field TDD accompanied by pile-up formation explains the field threading dislocation densities obtained at low temperature in this series. At 650°C, both pile-up TDD and surface roughness are generally higher in the on-axis sample than for the offcut samples. Both of these characteristics lead to a high-field threading dislocation density in the on-axis glide kinetics sample grown at this temperature when compared to offcut samples.

Dislocation pile-up formation in compositionally graded buffers arises from both intrinsic and extrinsic factors. As discussed in section 1.5.2, deep troughs in the cross-hatch pattern can intercept gliding threading dislocations, leading to pile-up formation. However, pile-ups can also form from heterogeneous mechanisms. This is of particular importance in the hot-wall UHVCVD system used in this study, where material evolving from the walls of the growth chamber increases particulate density. This mechanism is highly dependent on the thermal history and composition of past growths; however, its magnitude can be estimated by comparing samples grown in clean and heavily coated quartz tubes. These heterogeneous nucleation sources can significantly increase field and pile-up TDD, as demonstrated by two undoped 60% Ge graded buffers grown at identical grading rates and growth temperatures. The first sample was grown on a heavily coated quartz tube ($\sim$ 150 μm total SiGe thickness on the chamber walls) and had an overall TDD of 2.0×10^6 cm^{-2} and a field TDD of 1.3×10^6 cm^{-2}. The second sample was grown in a nearly clean quartz tube and had an overall TDD of 5.7×10^5 cm^{-2} and a field TDD of 4.2×10^5 cm^{-2}. Etch-pit density photos clearly show dislocation pile-ups extending from particles in the former sample, as shown in Figure 4.11 below. These results indicate that process conditions can heavily influence both field and pile-up TDD, further reinforcing the link between pile-up TDD and field TDD.
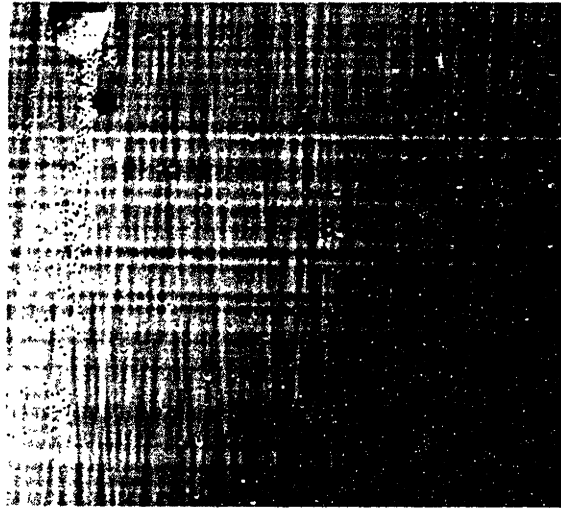
Figure 4.11 Etch-pit density photograph of a 60% Ge layer with a dislocation pile-up emerging from a particulate source.

4.4. Application to Ge/SiGe/Si Virtual Substrates

With threading dislocation densities near 10^5 cm^{-2} for virtual substrate compositions up to 50% Ge, the primary challenge in SiGe defect engineering lies in reducing threading dislocation densities in Ge/SiGe/Si virtual substrates. Between 50% Ge and pure Ge, threading dislocation density rises by roughly an order of magnitude. To better understand dislocation dynamics in the upper graded regions of these structures, several variations on Ge/SiGe/Si virtual substrate growth were investigated.

The lowest threading dislocation densities for Ge/SiGe/Si virtual substrates, roughly 10^6 cm^{-2}, have been obtained by using the growth sequence depicted in Figure 4.12 below.
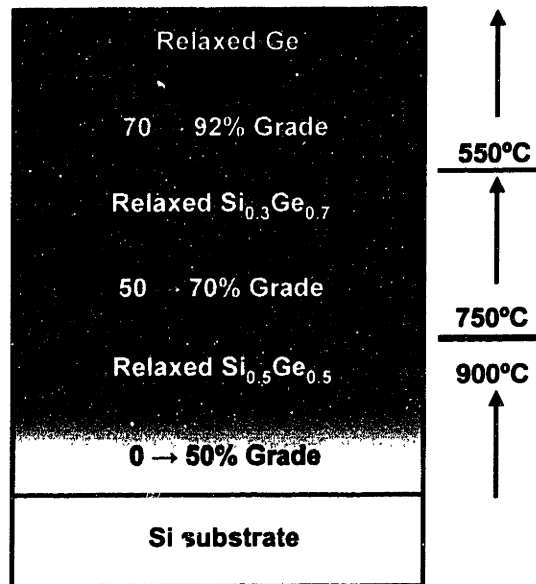
Figure 4.12 Optimized relaxed buffer sequence for Ge virtual substrates. Generally, layers are grown at the highest possible temperature. Maximum growth temperatures are limited mainly by gas-phase nucleation. The jump in composition between 92% Ge and Ge locks in compressive strain, which prevents cracking of the epilayer induced by thermal stress upon cooldown.

The initial grade to 50% Ge is conducted at 900°C. At 50% Ge, virtual substrates are CMPed, which controls dislocation pile-up formation.[28] After regrowth of the 50% Ge at 900°C (to bury the CMP interface), grading proceeds at 750°C up to 70% Ge. At 70% Ge, growth temperature is once again reduced, and the final portion of the grade is conducted at 550°C. The jump in composition between the 92% Ge layer and the Ge cap results in residual compressive strain upon cooling to room temperature, preventing the Ge layer from cracking.[28] All layers are graded at 10% Ge/µm (2000 Å jumps of 2% Ge).

Variations on this optimized grading sequence were explored to examine dislocation dynamics in these structures. First, the grading rate between 70% Ge and 92% Ge was doubled (to 1500 Å jumps of 3% Ge), which increased overall threading dislocation density to 2.5×10^6 cm^{-2}. Next, the growth temperature in this region was increased to

650°C while holding the grading rate at 10% Ge/μm (the Ge cap was still grown at 550°C), which resulted in an overall threading dislocation density of 1×10^6 cm^{-2}.

These experiments demonstrate the relative insensitivity of varying grading sequences in the high Ge content regions during Ge virtual substrate growth and indicate that the rise in threading dislocation density between 50% Ge and 100% Ge can likely be attributed to another factor. The jump in composition between 92% Ge and 100% Ge appears to be the cause of the escalation of defect density in this regime; dislocation nucleation at this interface likely obscures any changes in glide kinetics in underlying layers.

Chapter 5.   Surface Channel Strained Si p-MOSFETs

As discussed in Section 2.2.8, strained Si n-MOSFETs have been studied extensively by several researchers, and electron mobility enhancements of 80% over bulk Si are readily attainable.[52,84] These enhancements have been confirmed even at high vertical fields, indicating that strained Si n-MOSFETs have excellent potential for extending the Si roadmap.[87,101] Strained Si p-MOSFETs also display significant mobility enhancements over bulk Si, but this class of devices has not been studied as extensively. Detailed studies of channel mobility in surface channel strained Si p-MOSFETs will be necessary to fully gauge the impact of strained Si devices on CMOS technology. Furthermore, there exists the theoretical possibility of symmetric electron and hole mobility enhancements, or even of hole mobility enhancements exceeding electron mobility enhancements. This would offer the ability to significantly reduce p-MOSFET device sizes by adopting strained Si technology. In this section, the effects of virtual substrate composition and channel thickness on hole mobility enhancements in surface channel strained Si p-MOSFETs are explored, and carrier mobility degradation in SiGe alloy channels is measured for the first time. Finally, strategies for increasing hole mobility beyond that of strained Si are discussed.

5.1.   Overview of Strained Si MOSFET Growth and Device Fabrication

All films were grown in the UHVCVD system described in Section 3.1. Growth began with the relaxed compositionally graded SiGe buffers, grown at 900°C and 25 mT, that comprised the virtual substrates for device layers. All compositionally graded layers were graded at 10% Ge/μm (2% jumps of 2000 Å) and capped with 1.5 μm uniform composition layers. From previous experience[18,136] and measurements done in this study,

these virtual substrates have threading dislocation densities of 1-2 × 10^5 cm^{-2}, regardless of final composition. Following virtual substrate growth, deposition of device layers proceeded at 650°C and 3 mT. All structures were doped ~ 10^{16} cm^{-3} with either phosphorus (for p-MOSFETs) or boron (for n-MOSFETs) up to the strained device layers. Ring transistors were then fabricated by the short flow MOSFET process. The highest temperature step in device processing for this study is the implant activation anneal, done at 600°C for 30 minutes. Effective mobility versus effective vertical field for these devices was extracted by the procedure outlined in Section 3.2.3.

5.2. Effect of Strain on Hole Mobility Enhancements

Effective hole mobility versus effective vertical field is shown in Figure 5.1 for virtual substrate compositions between 35% and 50% Ge. In these structures, strained Si thickness was held constant at 100 Å (as-grown; processing removes about 20 Å of strained Si).
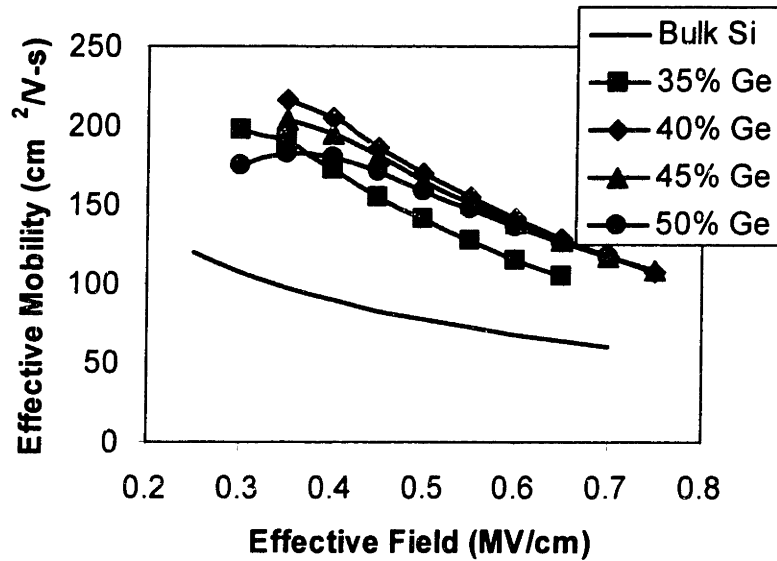
Figure 5.1 Effective hole mobility versus effective vertical field for strained Si *p*-MOSFETs grown on virtual substrate compositions between 35% Ge and 50% Ge. Low-field hole mobility increases between 35% Ge and 40% Ge, but falls slightly beyond this point.

Mobility enhancements over bulk Si, taken at three different effective vertical fields, are given in Figure 5.2 as a function of virtual substrate composition. Additional experimental data for virtual substrate compositions up to 30% Ge,[52] and the theoretical variation[50] of mobility enhancement with strain, are plotted alongside this data.
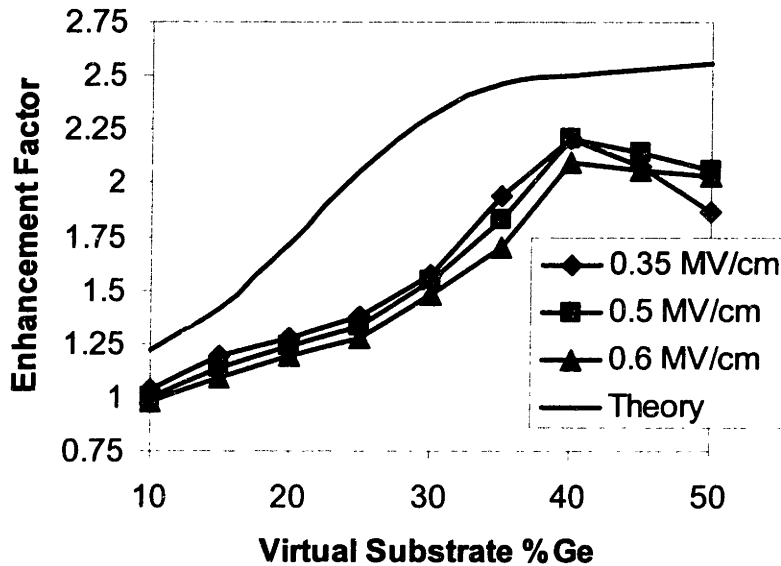
Figure 5.2 Hole mobility enhancement versus virtual substrate composition for strained Si p-MOSFETs, taken at the three vertical fields indicated. Theoretical data is from Oberhuber et al.[50] while experimental data for virtual substrate compositions between 10% Ge and 30% Ge is from Currie et al.[52] The experimental data supports the theoretical conclusion that enhancements saturate at 40% Ge.

As predicted by Oberhuber et al., mobility enhancement saturates at virtual substrate compositions of 40% Ge, with a slight drop-off at higher compositions. Since selective chromic acid-based etching[115] reveals a steadily increasing misfit dislocation density in as-grown samples as substrate Ge content increases, this drop-off could possibly be attributed to scattering from misfit dislocations. Moreover, AFM scans on these samples reveal no changes in small- or large-scale surface roughness of these samples as a function of strain. However, the drop in mobility enhancement at high virtual substrate Ge compositions could also arise from the increasing band offset between the strained Si and the SiGe virtual substrate, since larger band offsets increase the hole population in the low mobility SiGe virtual substrate. The rate of the decrease in hole mobility enhancements with increasing composition (past 40% Ge) is greatest at low vertical fields

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and least at high vertical fields, consistent with both of the proposed mechanisms listed above. Neither of these mechanisms affect high-field mobility, where holes are pulled away from the strained Si/relaxed SiGe interface. To our knowledge, the enhancement factor of 2.2, recorded at a vertical field of 0.5 MV/cm, is the largest ever reported for a strained Si p-MOSFET. Interestingly, for strained Si grown on 35% virtual substrates, we can obtain an 80% mobility enhancement for both electrons and holes. This point of symmetric enhancements is important because it would allow circuit designers to scale both strained Si n-MOSFET and p-MOSFET areas relative to bulk Si by the same amount to obtain the desired current drive.

As described in Section 2.2.7, several researchers have shown that hole mobility enhancements in strained Si display a strong dependence on effective vertical field, a trend that also emerges in these samples. Hole mobility enhancements are relatively low at low vertical fields, likely because of parallel conduction through the SiGe virtual substrate. Enhancements increase with increasing vertical field up to roughly 0.4 MV/cm, but then drop slightly at high-fields. The drop in hole mobility enhancements at high vertical fields has been explained in the following manner. At high vertical fields, the average kinetic energy of holes is very high, allowing them to scatter from the light hole to heavy hole band.[83] This postulate is supported by considering the evolution of hole mobility enhancements in strained Si p-MOSFETs as a function of vertical field and strain. Figure 5.3 is a plot of mobility enhancement versus effective vertical field for strained Si p-MOSFETs on virtual substrate compositions between 35% Ge and 50% Ge.
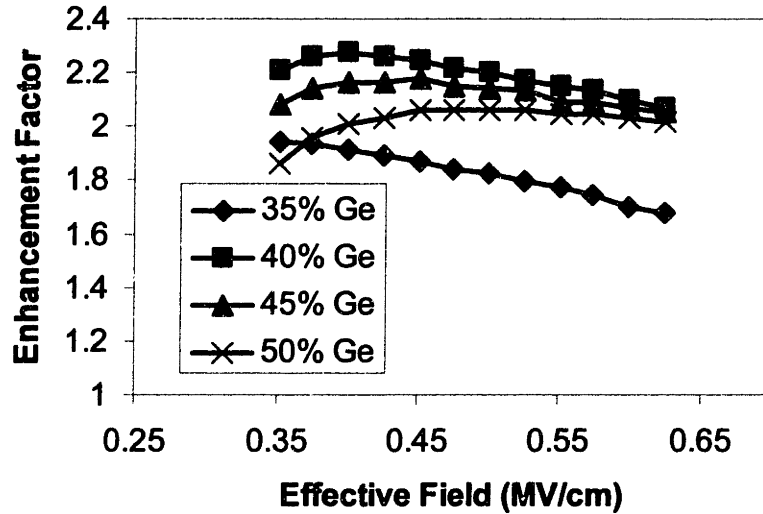
Figure 5.3 Hole mobility enhancement versus effective vertical field for strained Si *p*-MOSFETs on different SiGe virtual substrate compositions. The rate of decrease of hole mobility enhancements with increasing effective field drops as strain increases.

The severity in the drop-off of mobility enhancements at high vertical fields decreases with strain, possibly indicating that the increased subband splitting at high strain levels helps to suppress intervalley scattering at high vertical fields. Interestingly, however, the change in kinetic energy of holes over the field range investigated is slight. Though the situation should be analogous in strained Si *n*-MOSFETs beyond virtual substrate compositions of 20% Ge (where intervalley scattering is completely suppressed), mobility enhancements in these devices are relatively independent of effective field and strain.[52] However, Rim *et al.* have shown that high-field electron mobility in strained Si *n*-MOSFETs is higher than can be predicted by phonon-limited mobility, possibly indicating that strained Si *n*-MOSFETs are resistant to this scattering mechanism.[101] Thus, direct comparison between strained Si *n*-MOSFETs and *p*-MOSFETs may not be possible.

Figure 5.4 shows that the vertical field at which the maximum hole mobility enhancement occurs increases as virtual substrate Ge composition (strain) increases. This reflects the trade-off between hole population in the virtual substrate and high-field surface roughness scattering. As the band offset between the strained Si surface channel and the virtual substrate increases, a higher gate bias is needed to pull holes into the high mobility surface channel. Thus, the maximum hole mobility enhancement occurs at higher vertical fields.
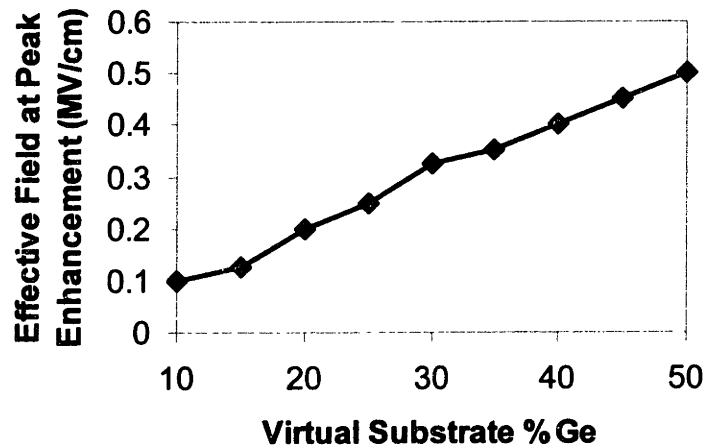
Figure 5.4 Vertical field at which peak hole mobility enhancement occurs in strained Si p-MOSFETs versus virtual substrate Ge composition. As strain increases, maximum enhancements occur at increasing vertical fields. Experimental data for virtual substrate compositions between 10% Ge and 30% Ge is from Currie et al.[52]

5.3. Effect of Channel Thickness on Hole Mobility Enhancements

Effective hole mobility versus effective vertical field for p-MOSFETs for different strained Si thicknesses, all grown on 30% Ge virtual substrates, is given in Figure 5.5. Though eight different channel thicknesses were measured, only three are shown for

clarity. The thicknesses indicated are for as-grown samples; processing removes roughly 20 Å of strained Si.
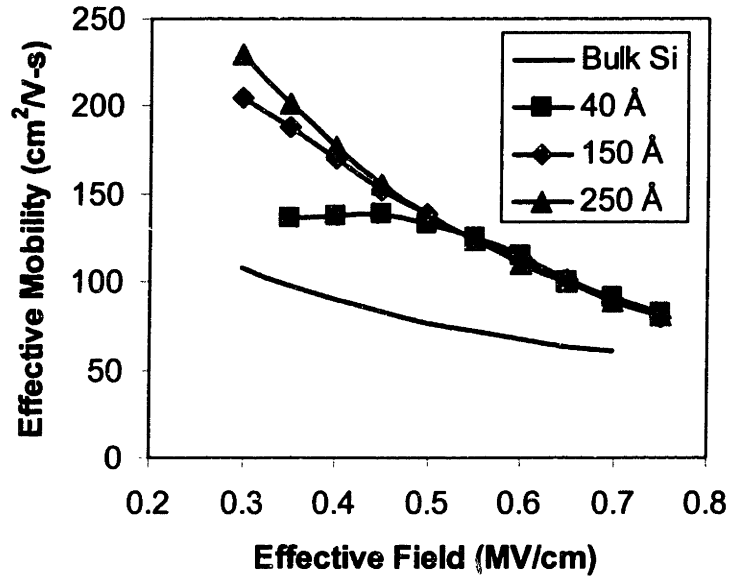
Figure 5.5 Effective hole mobility versus effective vertical field for strained Si p-MOSFETs on 30% Ge virtual substrates with varying surface channel thicknesses.

At low vertical fields, thin strained Si layers have the lowest effective mobility, the result of significant hole population in the low mobility SiGe virtual substrate. At high-fields, hole mobility is independent of channel thickness, even for the thinnest channels. This trend is further supported by Figure 5.6, which is a plot of hole mobility enhancement factors, measured at vertical fields of 0.3 and 0.6 MV/cm, versus channel thickness for these samples.
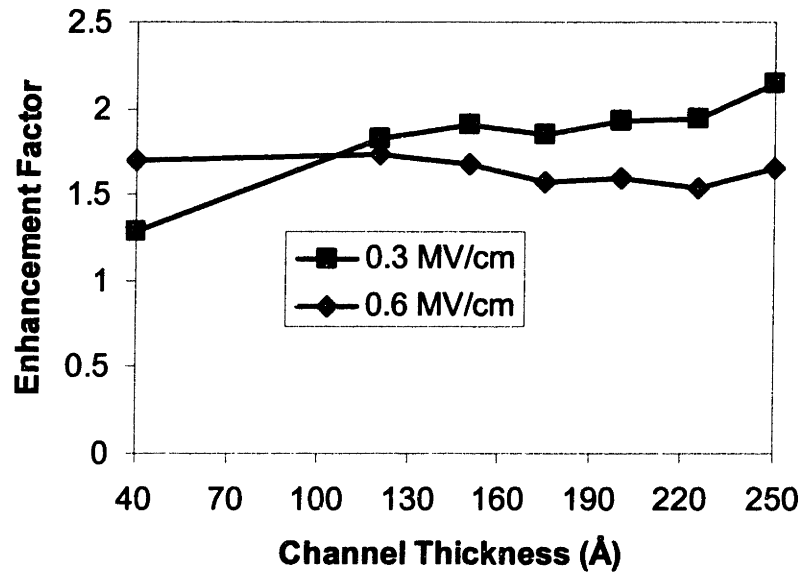
Figure 5.6 Hole mobility enhancement factor versus channel thickness in strained Si p-MOSFETs for two different effective vertical fields. At low vertical fields, thin channels exhibit the lowest hole mobility; however, hole mobility is independent of channel thickness at high vertical fields.

At low vertical fields, thin channels have almost no enhancement over bulk Si because of the parallel hole channel in the SiGe virtual substrate. However, at higher vertical fields, hole mobility enhancements are independent of channel thickness, indicating that the applied gate bias is sufficient to pull holes into the strained Si surface channel.

The thickest strained Si layers are almost three times the equilibrium critical thickness; therefore one would expect that the misfit dislocations at the strained Si/relaxed SiGe interface may decrease the mobility of carriers in the channel. However, since most holes are pulled away from this interface at high-fields, scattering from misfit dislocations is diminished for such thick channels. Even though selective etching revealed an increase in misfit dislocation density with channel thickness in as-grown samples, the misfit dislocation density ($< 10^3$ cm^{-1}) was always low enough to result in negligible strain relaxation.

The vertical field at which maximum hole mobility enhancement occurs is also a function of channel thickness, as shown in Figure 5.7 for a series of strained Si p-MOSFETs grown on relaxed $Si_{0.7}Ge_{0.3}$ virtual substrates.
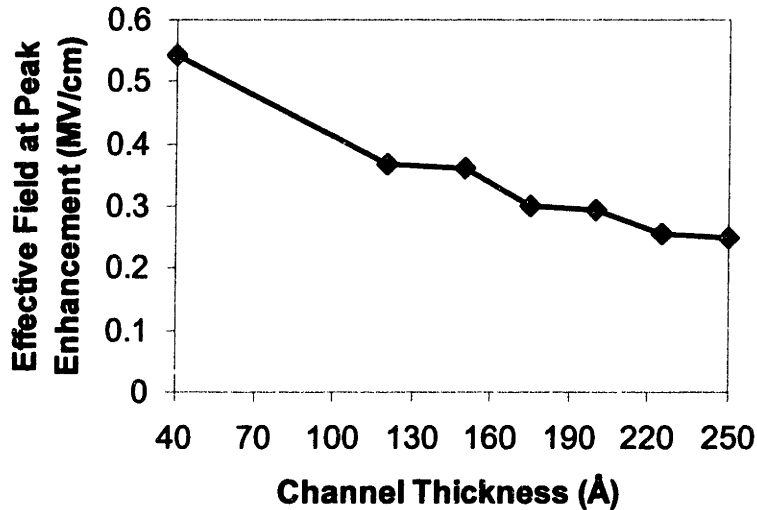
Figure 5.7 Effective vertical field at which hole peak mobility enhancement occurs in strained Si p-MOSFETs on 30% Ge virtual substrates versus channel thickness. As channel thickness increases, peak mobility enhancements occur at lower vertical fields.

For thin channels, the maximum in enhancement occurs at high vertical fields. Note, however, that this does not imply that thin channels are necessarily superior to thick channels. Mobility enhancements at low vertical fields are actually lower for thin channels, as discussed above. Rather, this reflects the trade-off between hole population in the low mobility relaxed SiGe virtual substrate (most severe at low fields) and surface roughness scattering (most severe at high-fields). Thin channels have reduced low-field mobility enhancements because a significant fraction of the hole wavefunction is not confined to the strained Si surface channel, so the maximum enhancements occur at high vertical fields.

5.4. Alloy Scattering in Strained SiGe Surface Channels

To study the effects of alloy scattering on electron and hole mobility in tensile strained SiGe, a series of n- and p-MOSFETs were fabricated featuring $Si_{1-y}Ge_y$ surface channels under constant strain on relaxed $Si_{1-x}Ge_x$ virtual substrates ($x - y = 25\%$ Ge). All heterostructures were capped with ~20 Å Si (as-grown) to preserve the Si/SiO_2 interface. Essentially, these heterostructures are intended to be analogous to conventional strained Si surface channel MOSFETs, with channel and virtual substrate composition shifted accordingly to keep strain constant. These heterostructures were designed to allow direct measurement of carrier mobility degradation in tensile strained $Si_{1-y}Ge_y$ quantum wells. Since there is a negligible conduction band offset between strained $Si_{1-y}Ge_y$ layers and strained Si, we cannot confine electrons in tensile strained $Si_{1-y}Ge_y$ alloy channels and still maintain the high quality Si/SiO_2 interface. Thus, to ensure that the strained Si surface layer would not impact mobility measurements, the thickness of this layer was minimized.

Figure 5.8 is a plot of effective electron mobility versus effective vertical field for $Si_{1-y}Ge_y$ n-MOSFETs with different alloy channel composition (y) under a constant 1% tensile strain.
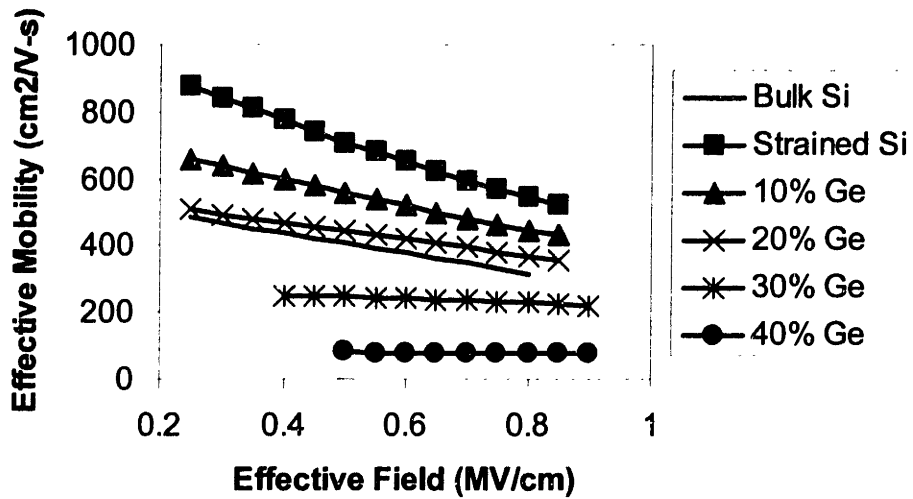
Figure 5.8. Effective electron mobility versus effective vertical field for SiGe tensile strained alloy channel *n*-MOSFETs. Electron mobility drops sharply as alloy channel Ge composition increases.

This figure clearly indicates that electron mobility is impacted by alloy scattering—

severe mobility degradation occurs for all Ge compositions. Also, the slopes of the

curves of effective mobility versus effective field for alloy channel devices are different

than for strained Si or bulk Si. We can gain insight into the physical origins behind this

difference by plotting the above figure on a logarithmic scale, shown in Figure 5.9 below.
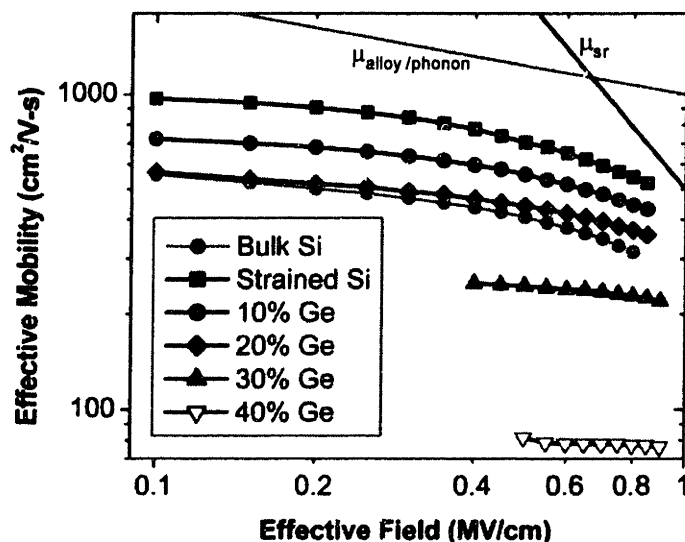
Figure 5.9. Effective electron mobility versus effective vertical field for SiGe tensile strained alloy channel n-MOSFETs, presented on a logarithmic scale. The dependence of effective mobility on surface roughness scattering (labeled μ_{sr}) and phonon/alloy scattering (labeled $\mu_{alloy/phonon}$) is also illustrated.

Electron mobility in both bulk Si and strained Si devices is limited by phonon scattering at moderate fields (~ 0.4 MV/cm), with a dependence of $E_{eff}^{-0.3}$.[41] At high fields, electron mobility in these devices is limited by surface roughness scattering, with a dependence of E_{eff}^{-2}.[41] Electron mobility in alloy scattering samples appears to display a similar dependence on effective field; however, both alloy scattering and phonon scattering appear to display a similar dependence on E_{eff}. The importance of alloy scattering in limiting electron mobility in these samples can be seen in the steadily increasing vertical field at which surface roughness scattering limits mobility. For the 10% Ge and 20% Ge alloy channel samples, the decrease in mobility at high fields (> 0.7 MV/cm) is less rapid than for bulk Si or strained Si, indicating that mobility is still partly limited by an $E_{eff}^{-0.3}$ dependence. For 30% Ge and 40% Ge alloy channel samples,

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mobility over the entire vertical field range is limited by an $E_{eff}^{-0.3}$ dependence. The

increasing influence of the $E_{eff}^{-0.3}$ dependence in alloy channel samples indicates that this

dependence must at least partly be attributed to alloy scattering. Moreover, the increased

dependence on alloy scattering in these samples accounts for the difference in slope

between alloy scattering samples and strained Si—since mobility in alloy scattering

samples is limited mainly by alloy scattering, the more rapid mobility degradation due to

surface roughness scattering is not apparent.

Figure 5.10 is a plot of electron mobility enhancement, taken at a vertical field of 0.5

MV/cm, versus alloy channel composition. Electron mobility enhancements fall below 1

for SiGe channel compositions beyond 20% Ge.
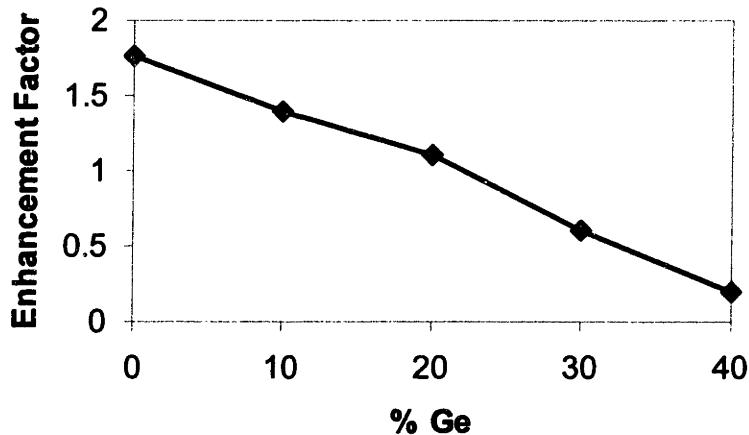
Figure 5.10. Electron mobility enhancement factor measured at 0.5 MV/cm in SiGe tensile strained alloy channel n-MOSFETs versus channel alloy composition. Electron mobility enhancements drop sharply as Ge composition increases.

The situation for strained $Si_{1-y}Ge_y$ surface channel p-MOSFETs is markedly different.

Figure 5.11 is a plot of effective hole mobility versus effective vertical field for $Si_{1-y}Ge_y$

p-MOSFETs with different alloy channel compositions (y), under a constant 1% tensile

strain. Because of a problem with the electron beam metallization system, the 10% and

20% Ge alloy channel *p*-MOSFETs were not co-processed with the rest of the samples, so measurements were taken on similar samples processed earlier. The only significant difference between these sets of samples was the use of rapid thermal annealing for implant activation (850°C for 1 s) instead of the 600°C anneal used in later samples. As described previously,[4,52] the actual annealing temperature in the rapid thermal annealing system was much higher than the setpoint—in fact, optical pyrometry measurements indicated that these anneals were actually done at 990°C.
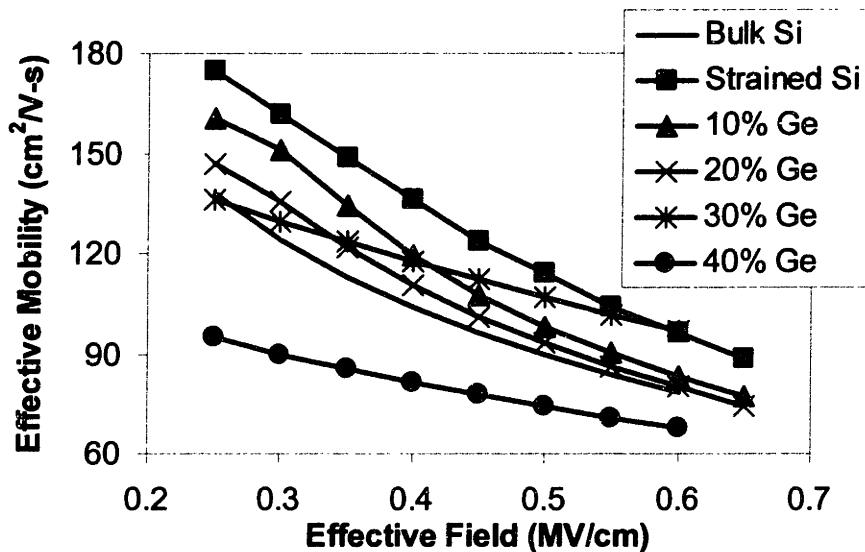
Figure 5.11. Effective hole mobility versus effective vertical field for SiGe tensile strained alloy channel *p*-MOSFETs. Low-field hole mobility drops slightly for all alloy compositions investigated compared to strained Si.

At low vertical fields, hole mobility clearly drops as Ge composition increases. In fact, low-field mobility in the 30% Ge strained alloy channel is roughly equal to bulk Si. However, overall mobility degradation in alloy channel *p*-MOSFETs is much milder than in alloy channel *n*-MOSFETs. Also, the slope of the 10% Ge and 20% Ge alloy channel *p*-MOSFETs appears different than the other samples. Again, this difference can be explained plotting the above figure on a logarithmic scale, shown in Figure 5.12 below.
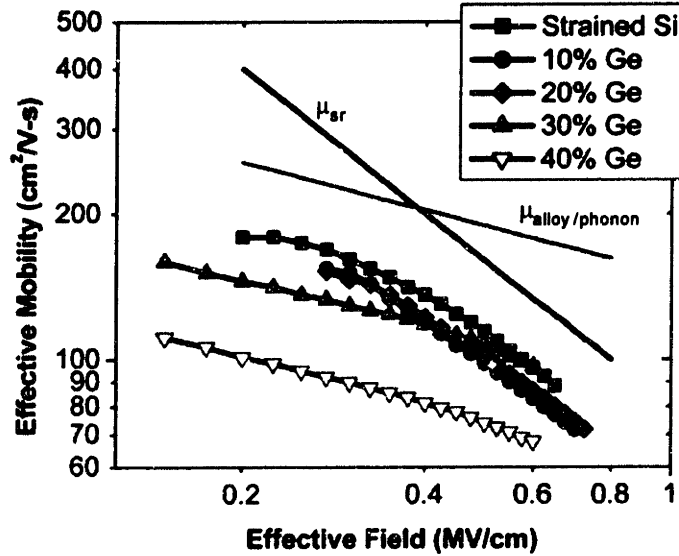
Figure 5.12. Effective hole mobility versus effective vertical field for SiGe tensile strained alloy channel *p*-MOSFETs, presented on a logarithmic scale. The dependence of effective mobility on surface roughness scattering (labeled μ_{sr}) and phonon/alloy scattering (labeled $\mu_{alloy/phonon}$) is also illustrated.

For clarity, the bulk Si mobility curve has been eliminated from this plot.

Hole mobility in the strained Si device and 10% Ge and 20% Ge alloy scattering samples is limited mainly by surface roughness scattering, with a dependence of E_{eff}^{-1}.[41]

In contrast, hole mobility in the 30% Ge and 40% Ge alloy scattering samples follows a dependence of $E_{eff}^{-1/3}$ over almost the entire field range, which is either attributable to phonon scattering[41] or alloy scattering.[106] Given that the strained Si *p*-MOSFET only displays a dependence on phonon scattering over a very narrow field range, we conclude that the $E_{eff}^{-1/3}$ dependence of mobility in the 30% Ge and 40% Ge alloy channel *p*-MOSFETs can be attributed to alloy scattering. Interestingly, the 10% Ge and 20% Ge alloy channel *p*-MOSFETs only show this dependence at low vertical fields, and high-field mobility in these samples is limited by surface roughness scattering. We attribute this difference to the effects of rapid thermal annealing on surface roughness in these

samples. As was the case for alloy channel n-MOSFETs, the different slope of alloy

channel p-MOSFETs compared to strained Si p-MOSFETs is due to the increased

influence of alloy scattering (and correspondingly decreased influence of surface

roughness scattering) in alloy channel samples.

Figure 5.13 is a plot of mobility enhancement, taken at a vertical field of 0.3 MV/cm,

versus alloy channel composition. We have chosen to measure low-field hole mobility

enhancements to isolate the effects of alloy scattering in the 10% Ge and 20% Ge

samples. Hole mobility enhancements fall slowly between 0% Ge and 20% Ge, but

degrade rapidly past 20% Ge.
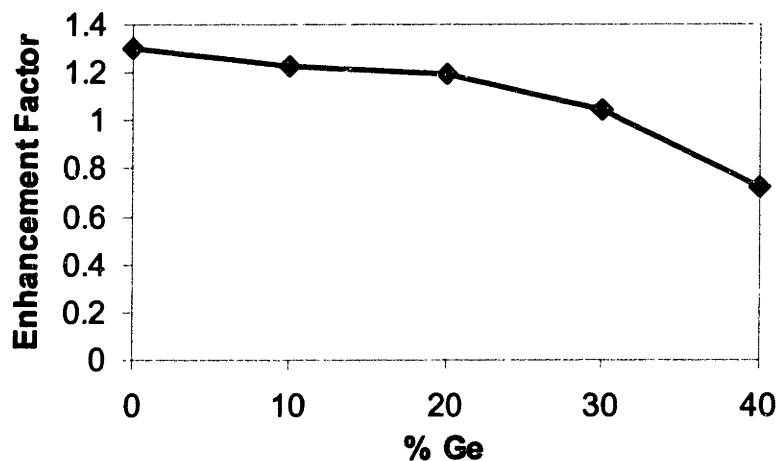
Figure 5.13. Hole mobility enhancement factor (measured at 0.3 MV/cm) in SiGe tensile strained alloy channel p-MOSFETs versus channel composition. Hole mobility enhancements drop slightly for alloy channels up to 30% Ge, and sharply thereafter.

5.4.1.   Comparing Electron and Hole Mobility Degradation in Strained SiGe Alloy Channels

By taking the ratio of alloy channel mobility to strained Si mobility at a given vertical

field, mobility degradation in n-MOSFETs and p-MOSFETs can be directly compared,

despite the different enhancement factors for electrons and holes under 1% tensile strain.

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Figure 5.14 is such a plot, where mobility degradation (relative to strained Si) is plotted

versus channel composition. In this graph, electron mobility enhancements over bulk Si

were measured at a vertical field of 0.5 MV/cm while hole mobility enhancements over

bulk Si were measured at a vertical field of 0.3 MV/cm (to ensure that the effects of alloy

scattering were isolated in the 10% Ge and 20% Ge alloy channel p-MOSFETs).
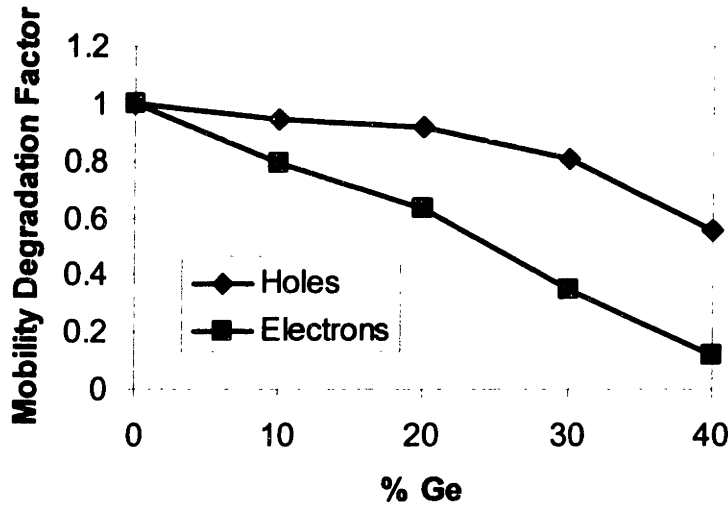
Figure 5.14 Comparison of electron and hole mobility degradation in SiGe tensile strained alloy channel MOSFETs (relative to strained Si) versus channel alloy composition. Mobilities were measured at 0.3 MV/cm (holes) and 0.5 MV/cm (electrons). Electron mobility is degraded much more severely by alloy scattering than hole mobility.

These results are the first direct experimental verification that alloy scattering in tensile

strained SiGe surface channels affects electrons more severely than holes, which had

been argued in a theoretical study by Kearney and Horrell.[68] Currie et al. had also

observed that mobility enhancements in strained Si p-MOSFETs were less severely

degraded than those in strained Si n-MOSFETs when these devices were subject to

1000°C anneals for increasing times, indicating that Ge interdiffusion degrades electron

mobility more severely than hole mobility.[52]

5.4.2. Evolution of Interface Quality with Alloy Channel Content

To directly measure the impact of alloy scattering in tensile strained $Si_{1-y}Ge_y$ surface

channel MOSFETs, the strained Si surface layer in these alloy channel samples had to be

very thin. However, this resulted in a degraded MOS interface, particularly as alloy

channel Ge composition increased, because of the high concentration of Ge atoms at the

Si/SiO_2 interface. The impact of interface degradation can clearly be seen in

Capacitance-Voltage (C-V) curves for alloy channel n-MOSFETs, which are given in

Figure 5.15 below. The C-V curves of p-MOSFETs display a similar degradation. Full-

width at half-maximum (FWHM) of these curves remains low up to 20% Ge, but

increases rapidly past this point.
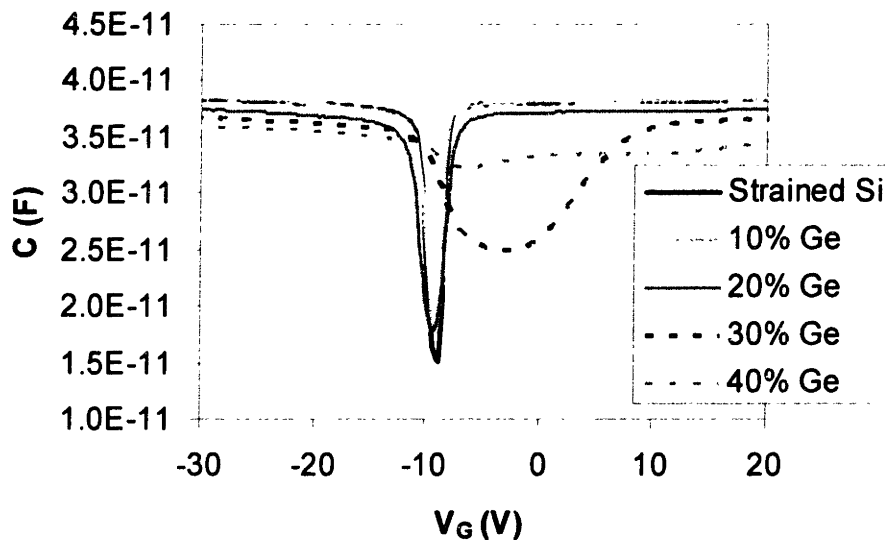
Figure 5.15 Capacitance-Voltage curves taken on alloy channel n-MOSFETs. The increasing full-width at half-maximum as channel composition increases results from increasing interface state density.

To verify that Ge atoms at the interface were responsible for the degraded C-V curves

shown above, VPD analysis[123] of alloy channel n-MOSFET structures was undertaken.

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To enable analysis of full wafers without destroying completed MOSFETs, separate wafers were subjected to a modified short flow MOSFET process, which consisted of a modified RCA clean, a standard LTO deposition at 400°C, an anneal in N_2 at 600°C, and a BOE strip of the LTO layer. This modified process mimics the material removal and thermal budget of the short flow process, but can be completed in one day and does not require completed device wafers to be destroyed. Additionally, following a modified RCA clean, another set of alloy channel n-MOSFET structures subject only to a modified RCA clean were also subjected to VPD analysis to determine the as-grown Ge content at the surface of alloy channel device structures. The results of the VPD analysis are summarized in Table 5.1 below. Generally, wafers subject to the modified short flow MOSFET process have two to four times the surface density of Ge atoms than as-grown samples. Both as-grown and as-processed wafers display a similar trend, where interface Ge composition increases rapidly as channel alloy composition increases.

Table 5.1 Concentration of Ge atoms at the surface of as-grown and processed alloy channel n-MOSFET heterostructures. In both cases, Ge concentration at the sample surface increases with increasing alloy channel content.

Sample	As-grown surface Ge content ($\times 10^{10}$ cm^2)	As-processed surface Ge content ($\times 10^{10}$ cm^2)
Strained Si	20	35
10% Ge	570	1100
20% Ge	1100	1700
30% Ge	4200	5700
40% Ge	8000	27000

Figure 5.16 is a plot of surface Ge composition in structures subjected to the modified short flow MOSFET process versus the FWHM of C-V curves. Since interface state density is proportional to the FWHM of C-V curves,[137] this figure indicates that interface state density increases severely for alloy channel compositions beyond 20% Ge.

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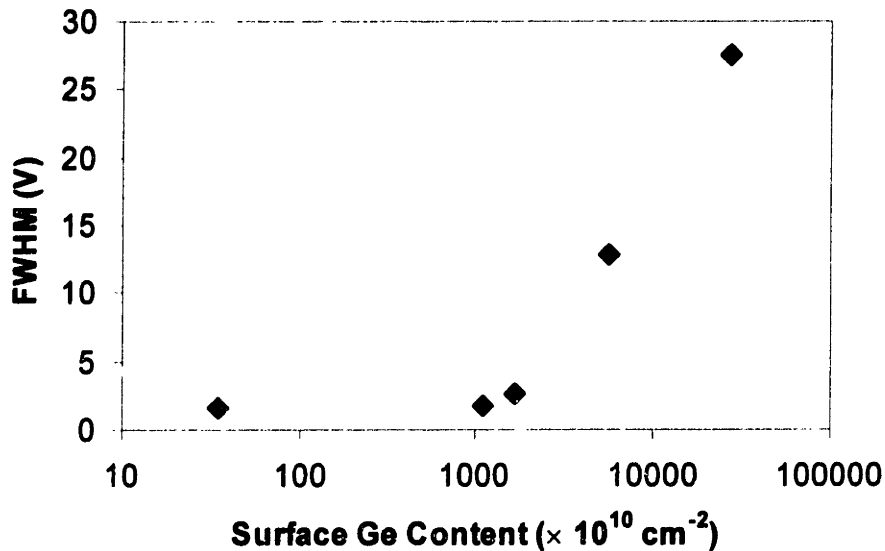
Figure 5.16 Full-width at half-maximum (FWHM) of Capacitance-Voltage curves for alloy channel n-MOSFETs versus surface concentration of Ge atoms in these heterostructures. FWHM increases rapidly beyond roughly 10^{13} Ge atoms cm^{-2}, indicating that this concentration is sufficient to degrade interface state density.

High interface state densities will in general increase Coulomb scattering rates and thus degrade carrier mobility, especially at low vertical fields where the inversion layer charge is much lower than the interface state charge. Overall, this can mask the contribution of alloy scattering to mobility degradation in these samples. With precise values of interface state density of these samples (which is unfortunately difficult to calculate accurately), this effect could be quantified. To avoid the inaccuracies associated with a high interface state density, mobility enhancements in Figure 5.10 and Figure 5.14 were taken at relatively high vertical fields.

The as-grown surface Ge concentration in these heterostructures likely reflects both Ge evolution from the walls of the growth chamber and Ge intermixing. The latter has been shown to occur in UHVCVD at growth temperatures above 515°C.[114] The increasing Ge concentration at the sample surface as alloy channel composition increases

in as-grown samples is understandable, since the compositional gradient between the Si surface layer and buried alloy channel (which drives intermixing) is largest for high Ge composition alloy channels. The relatively low thermal budget of the short flow MOSFET process further degrades the Si/SiO_2 interface.

5.5. Strategies for Increased Carrier Confinement

The strain and thickness variation experiments outlined in Sections 5.2 and 5.3 clearly indicate that strain, not thickness, is the key variable in determining channel mobility in strained Si p-MOSFETs. While hole mobility enhancements obtained in these heterostructures are relatively high, hole mobility in the best strained Si p-MOSFETs is still roughly four times lower than electron mobility for a given vertical field. This disparity can be reduced by using a dual channel heterostructure,[103] consisting of a strained Si surface layer and a buried compressively strained $Si_{1-y}Ge_y$ channel deposited on a relaxed $Si_{1-x}Ge_x$ virtual substrate ($x < y$), described in section 2.2.10. In this case, the buried $Si_{1-y}Ge_y$ layer can be seen to increase hole mobility through a variety of mechanisms. At low gate bias, with a large valence band offset between the strained Si surface channel and strained $Si_{1-y}Ge_y$ buried channel, the buried channel can effectively confine holes. With proper choice of buried channel composition, this layer can have a very high hole mobility, and thus this heterostructure is simultaneously suitable for buried channel p-MOSFETs and surface channel n-MOSFETs. At the high vertical fields used in state-of-the-art CMOS, however, holes are pulled towards the strained Si/SiO_2 interface. Thus, these heterostructures are not strictly buried channel devices. However, since the out-of-plane effective mass of holes is low,[49] holes sample both the buried Si_1.

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$_y$Ge$_y$ layer and strained Si surface layer, and overall hole mobility can be increased considerably.

Initially, we investigated the p-MOSFET performance of two of these dual channel heterostructures, both grown on chemical-mechanical planarized (CMPed) 30% Ge virtual substrates. The first structure was composed of a 110 Å buried $Si_{0.5}Ge_{0.5}$ channel and an 85 Å Si surface channel. The second structure was composed of an 85 Å buried $Si_{0.4}Ge_{0.6}$ channel and an 85 Å Si surface channel. A control sample, composed of 85 Å strained Si on a CMPed 30% Ge virtual substrate, was also grown. For this experiment, all device layers were grown at 550°C to suppress channel undulations in the buried compressive layer. The effective hole mobility versus effective vertical field for the different dual channel configurations is given in Figure 5.17.
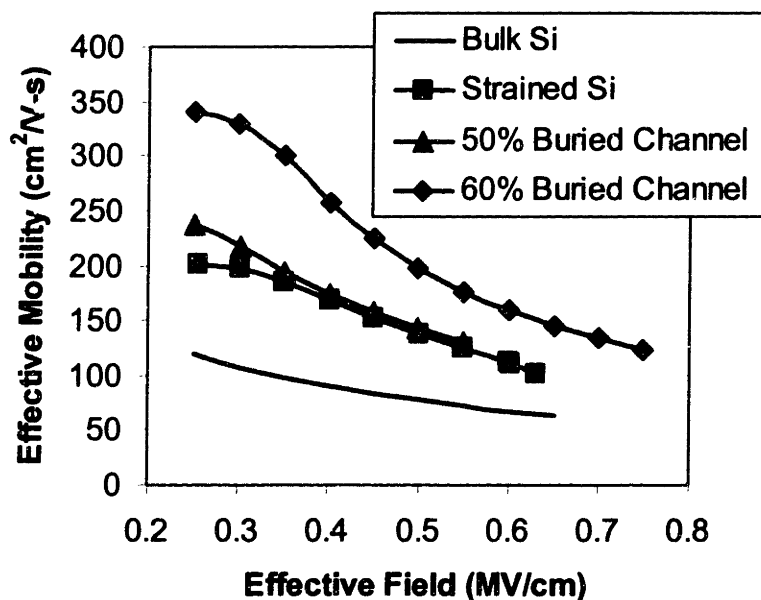
Figure 5.17 Effective hole mobility versus effective vertical field for two different dual channel heterostructures grown on 30% Ge virtual substrates. A control strained Si p-MOSFET is also shown. The heterostructure with the 60% Ge buried channel displays significant hole mobility enhancement over strained Si over the entire field range investigated.

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The sample with the 50% Ge channel displays identical mobility to strained Si at high vertical fields, indicating that the band offset between the 50% Ge buried channel and the strained Si surface channel is insufficient to confine holes in the buried layer and/or that the mobility boost attained by the portion of the wavefunction in the 50% Ge layer is not enough to significantly increase hole mobility over that of strained Si. However, the sample with the 60% Ge channel exhibits high mobility over the entire field range, with a peak hole mobility enhancement factor of 3.1 at a vertical field of 0.35 MV/cm, indicating that holes must be substantially occupying the buried high mobility 60% Ge channel. This enhancement occurs despite the presence of moderate strain-induced undulations in the buried 60% Ge channel. At high vertical fields, more of the wavefunction may begin to occupy the strained Si, but the enhancement is still very high over the entire field range. These results show remarkable promise for creating symmetric mobility SiGe heterostructure *p*- and *n*-MOSFETs and beckon us towards high Ge content buried channels. A more thorough investigation of hole mobility enhancements as a function of composition, strain, and channel thickness in these dual channel heterostructures will be presented in Chapter 6.

Chapter 6.   Dual Channel Heterostructure MOSFETs

As discussed in section 5.5, inserting a compressively strained $Si_{1-y}Ge_y$ layer between a $Si_{1-x}Ge_x$ virtual substrate and a strained Si surface layer can increase hole mobility considerably. Moreover, because of the negligible conduction band offset between the strained Si and strained $Si_{1-y}Ge_y$ layers, electron mobility should be unaffected by the presence of the buried channel.[104] These dual channel heterostructures offer the promise of nearly symmetric electron and hole mobility, both enhanced relative to bulk Si. In this chapter, we explore the effects of alloy scattering, strain, and layer thickness on hole mobility in dual channel heterostructure p-MOSFETs and compare electron and hole mobility enhancements in dual channel heterostructures to those attainable in strained Si MOSFETs.

6.1. Overview of Dual Channel Heterostructure p-MOSFET Growth

All films were grown in the UHVCVD system described in Section 3.1. Growth began with relaxed compositionally graded SiGe buffers, grown at 900°C and 25 mT, that comprised the virtual substrates for device layers. All compositionally graded layers were graded at 10% Ge/μm (2% jumps of 2000 Å) and capped with 1.5 μm uniform composition layers. From previous experience[18,136] and measurements done in this study, these virtual substrates have threading dislocation densities of 1-2 × 10^5 cm^{-2}, regardless of final composition. Deposition of device layers followed virtual substrate growth. One set of structures (with 60% Ge buried channels) continued with device layers deposited at 550°C exclusively. As noted in Section 5.5, these 60% Ge buried channels were slightly undulated. Another set of structures (with buried channel composition between 70% Ge and 80% Ge) proceeded with deposition of the buried $Si_{1-y}Ge_y$ channel

at 400°C. All channels grown at 400°C were planar. Because of the extremely low growth rate of Si using pure SiH_4 at 400°C, the subsequent strained Si surface layers for this set were deposited using a two step process. First, SiH_4 flow was initiated at 400°C and the growth temperature was raised to 450°C while still flowing SiH_4. This step allows enough silicon to deposit at low temperature to help stabilize the compressive layer against strain-induced undulations. Finally, the temperature was again raised under continued SiH_4 flow, and a thin strained Si surface channel was deposited at 550°C. Because the furnace ramp-up time can vary by several minutes, this process results in highly variable strained Si thicknesses (± 20%). All p-MOSFET (n-MOSFET) structures were doped ~ 10^{16} cm^{-3} with phosphorus (boron) up to the strained layers, and all device layers were 85 Å thick (as-grown) unless otherwise noted. Ring transistors were then fabricated by the short flow process. Effective mobility versus effective vertical field for these devices was then extracted by the procedure outlined in section 3.2.3.

6.2. Effect of Channel Composition on Hole Mobility Enhancements

First, we consider the effect of buried channel composition on hole mobility in dual channel heterostructures. By independently varying virtual substrate and buried channel Ge content, we can decouple the effects of strain and alloy scattering on hole mobility, a scattering mechanism whose significance has been widely debated.[55,68,69] Thus, dual channel heterostructures can provide insight into fundamental hole transport phenomena in strained layers. Figure 6.1 is a plot of effective hole mobility versus effective vertical field for dual channel heterostructures under constant strain; the difference between buried channel composition and virtual substrate composition is 30% Ge. The 70% and

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80% channels were grown at 400°C, while the 60% channel was grown at 550°C. For

comparison, the effective mobility of a strained Si p-MOSFET on a 30% Ge virtual

substrate (the strained Si thickness in this device is 150 Å) is also given on this plot.
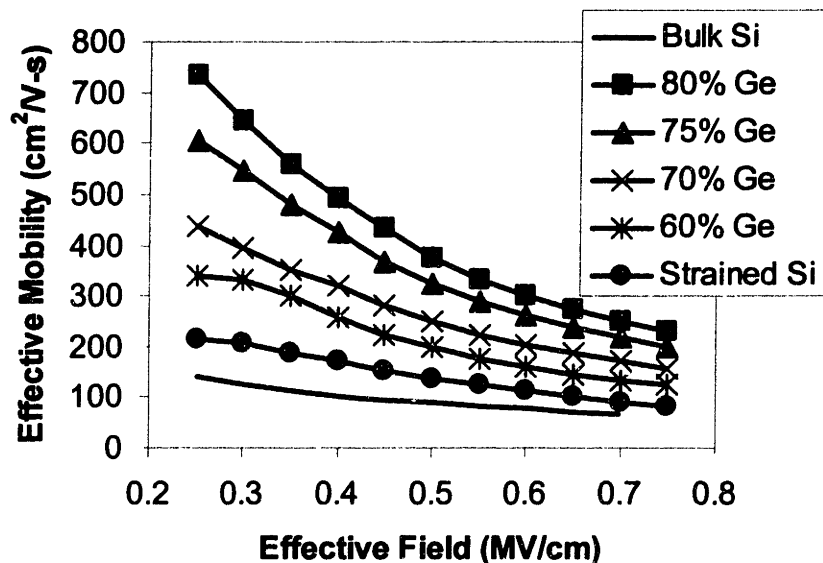
**Figure 6.1 Effective hole mobility versus effective vertical field for dual channel
heterostructures under constant strain ($y - x$ = 30% Ge) compared to a strained Si
p-MOSFET. All channel thicknesses in dual channel heterostructures are 85 Å.
Hole mobility in dual channel heterostructures increases with buried channel Ge
composition.**

All of these dual channel heterostructures display significant improvements in hole

mobility over conventional strained Si p-MOSFETs. In particular, the heterostructure

with an 80% Ge channel displays enormous improvements in hole mobility over the

entire field range.

The impact of channel composition on hole mobility is illustrated further in Figure

6.2, which is a plot of mobility enhancement factor over bulk Si, taken at a constant

vertical field of 0.3 MV/cm, versus buried channel Ge content for different

Si/compressively strained $Si_{1-y}Ge_y$/relaxed $Si_{1-x}Ge_x$ structures ($y - x$ = 0.3). For this

figure, we have chosen to use low-field mobility enhancements since holes will begin to

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occupy the Si surface layer at high-fields. The 50% Ge and 60% Ge channels were grown at 550°C, the 70% Ge and 80% Ge channels were grown at 400°C, and the 30% Ge data has been adapted from Bouillon et al.[138] All buried channels in this figure are under a constant strain level, with the exception of the 50% Ge point which was grown on a 30% Ge virtual substrate. While this channel actually is under a slightly lower strain level, the variation of mobility with strain in this layer should be mild for this channel composition.
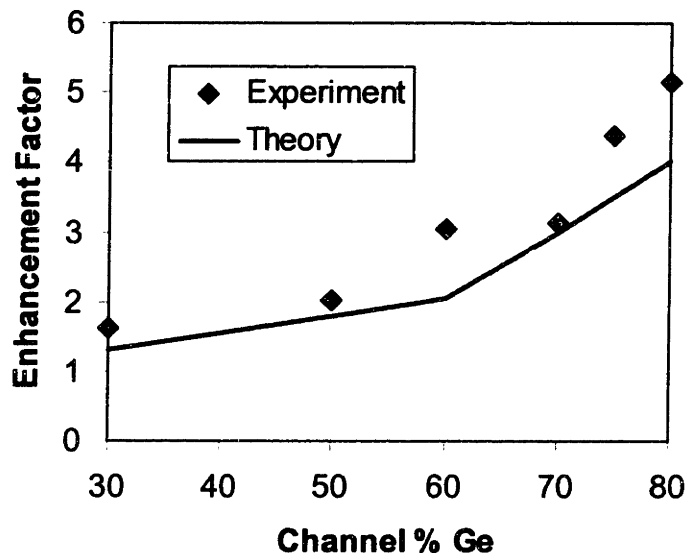
Figure 6.2 Hole mobility enhancement factors over bulk Si (taken at vertical fields of 0.3 MV/cm) for different strained $Si_{1-y}Ge_y$ channel compositions. All channels except the 50% Ge point were grown on relaxed virtual substrates such that $y - x =$ 0.3; the 50% Ge point was grown on a 30% Ge relaxed virtual substrate. The 30% Ge point was taken from Bouillon et al.[138] Hole mobility enhancements are large even where alloy scattering is expected to be most severe.

From this figure, we can see that high hole mobility clearly requires high Ge content channels (> 60% Ge). However, this figure also demonstrates that alloy scattering does not preclude high hole mobility in alloy channels, since the $y \cdot (1 - y)$ dependence of alloy scattering would imply that hole mobility should be greatly degraded around these

channel compositions. The variation of hole mobility enhancements with channel composition shown in this figure also follows the same general trend presented in a theoretical study by Bufler and Meinerzhagen.[71]

6.3. Effect of Strain on Hole Mobility Enhancements

Next, we consider the effects of strain on hole mobility enhancements by examining dual channel heterostructures with 80% Ge buried channels on virtual substrates between 30% Ge and 50% Ge. In these heterostructures, buried channel thickness varied roughly in line with the critical thickness for each of these layers; the 80% Ge channel thicknesses were 65 Å, 85 Å, and 105 Å on the 30%, 40%, and 50% Ge virtual substrates, respectively. All buried channels were grown at 400°C to avoid strain-induced undulations, and cross-sectional TEM analysis revealed that all device layers were planar. Because of the inherent variability involved in producing the strained Si surface layers when growing at 400°C, surface channel thickness in these devices varied between 65 Å and 105 Å. Figure 6.3 is a plot of effective hole mobility versus effective vertical field for this series of 80% Ge channels grown on different Ge composition virtual substrates.
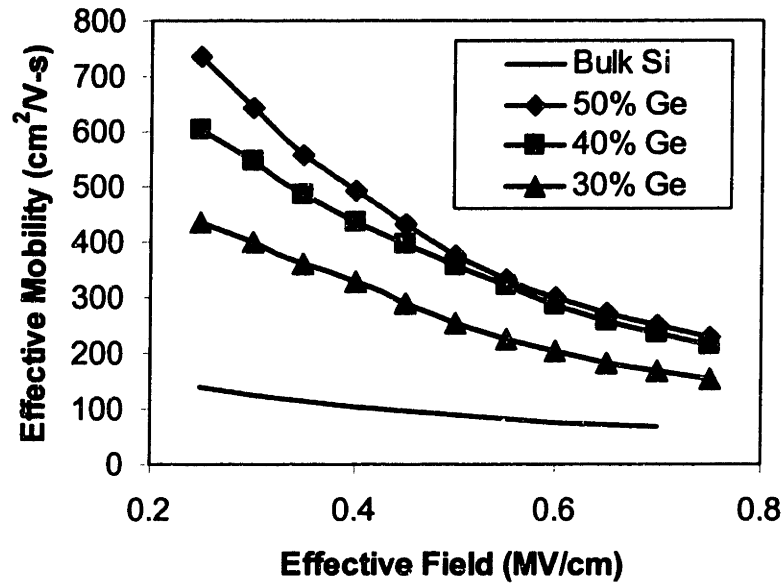
Figure 6.3 **Effective hole mobility versus effective vertical field for dual channel heterostructures with 80% Ge buried channels on various composition $Si_{1-x}Ge_x$ virtual substrates. Buried channel thickness is inversely proportional to strain. Hole mobility decreases as strain increases, indicating that channel thickness plays a more important role than strain in determining hole mobility enhancements in dual channel heterostructures.**

Low-field mobility, in which holes primarily occupy the buried channel, decreases as strain in the buried channel increases. This trend runs opposite the expected behavior in these samples, and is likely due to the decreasing buried channel thickness with strain. Thus, combined with the data from Section 6.2, we conclude that hole mobility enhancements in dual channel heterostructures are mainly controlled by channel thickness and composition, with strain as a secondary variable. Theoretical studies by Bufler and Meinerzhagen[71] have also supported the notion that hole mobility in strained $Si_{1-y}Ge_y$ quantum wells is more sensitive to channel composition than to strain.

6.4. High Electron and Hole Mobility in Dual Channel Heterostructures

Figure 6.4 is a plot of hole mobility enhancement factors versus effective vertical field for the dual channel structure consisting of an 80% Ge buried channel grown on 50% Ge virtual substrate at 400°C (discussed in the previous section).
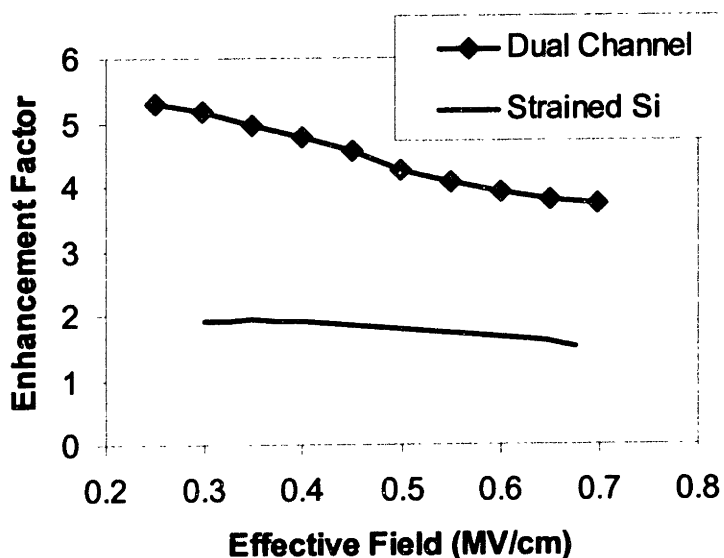
Figure 6.4 Hole mobility enhancement over bulk Si versus effective vertical field for a dual channel heterostructure featuring an 80% Ge buried channel on a relaxed 50% Ge virtual substrate. A strained Si p-MOSFET is also shown for comparison. Hole mobility enhancements in the dual channel heterostructure are above 3.65 over the entire effective field range.

This dual channel structure exhibits a peak hole mobility enhancement factor of 5.15 over bulk Si, obtained at a vertical field of 0.3 MV/cm. The hole mobility enhancement factor in this sample is also maintained above 3.65 over the entire investigated vertical field range, far higher than can be obtained in conventional strained Si p-MOSFETs.

Effective electron mobility exhibited in dual channel heterostructures is identical to that exhibited in strained Si on relaxed $Si_{1-x}Ge_x$ ($x > 0.2$) surface channel MOSFETs. For example, Figure 6.5 plots effective electron mobility versus effective vertical field for

the dual channel heterostructure discussed above, as well as another dual channel

heterostructure n-MOSFET (85 Å Si/85 Å $Si_{0.4}Ge_{0.6}$ on relaxed $Si_{0.7}Ge_{0.3}$) and a strained

Si n-MOSFET (100 Å Si on relaxed $Si_{0.75}Ge_{0.25}$).
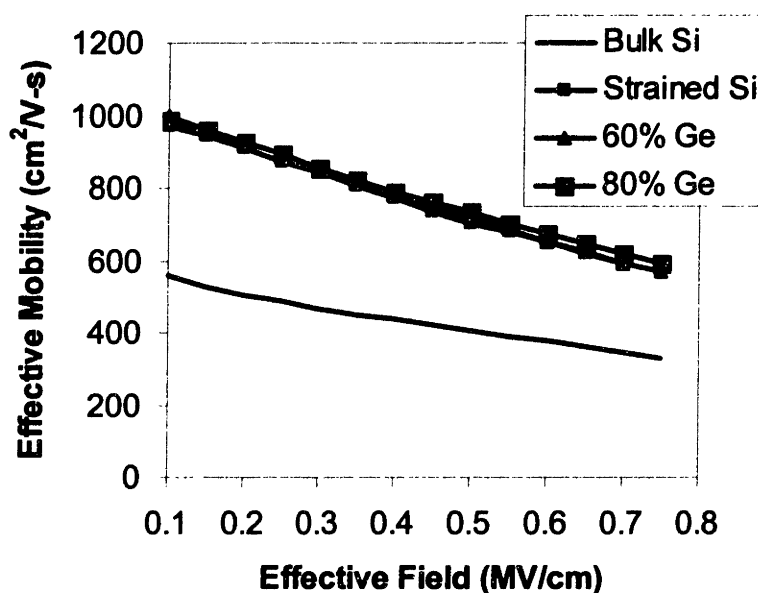
Figure 6.5 Effective electron mobility versus effective vertical field for two dual channel heterostructures and to strained Si. Electron mobility in dual channel heterostructures is identical to that of strained Si.

As expected, the presence of the buried $Si_{1-y}Ge_y$ layer in dual channel heterostructures

does not adversely impact electron moblility. Figure 6.6 is a plot of the ratio of electron

mobility to hole mobility for the dual channel heterostructure shown in Figure 6.4 versus

effective vertical field, compared to both bulk Si and strained Si/relaxed $Si_{0.75}Ge_{0.25}$

MOSFETs.
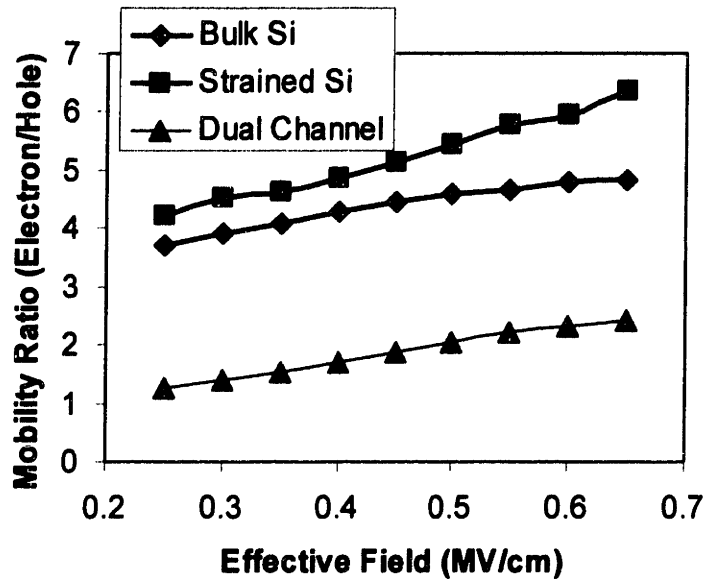
Figure 6.6 Ratio of electron mobility to hole mobility in the dual channel heterostructure shown in Figure 6.4 compared to both bulk Si and strained Si. In bulk Si, carrier mobilities are low and highly asymmetric. In strained Si, carrier mobilities are enhanced, but are still asymmetric. In dual channel heterostructures, carrier mobilities are nearly symmetric and both are enhanced relative to bulk Si.

Note that electron and hole mobility in bulk Si and strained Si MOSFETs are highly asymmetric, though in strained Si both electron and hole mobility are enhanced over bulk Si. As this figure indicates, by using a dual channel configuration we can achieve nearly symmetric carrier mobilities, both of which are enhanced relative to bulk Si. However, as discussed in Section 2.1.2, transconductance and drive currents in dual channel heterostructure p-MOSFETs will not be enhanced as much as mobility, since the hole wavefunction in these devices is separated spatially from the Si/SiO_2 interface. The exact penalty this causes in current drive enhancement is thus far unknown; this data could be obtained through quantum-mechanical modeling or through measurements on more advanced devices. Regardless, we note that since both strained layers in dual channel heterostructures are populated, these devices cannot be thought of as strictly buried channel. Furthermore, the enormous gains in hole mobility should far outweigh the loss

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in current drive due to the increased contribution of semiconductor capacitance to overall gate capacitance.

6.4.1. Retaining High-Field Hole Mobility Enhancements in Dual Channel Heterostructures

Finally, we investigate the effects of varying buried and surface channel thickness in dual channel heterostructures. Figure 6.7 is a plot of hole mobility enhancement over bulk Si versus vertical field for a series of strained $Si/Si_{0.4}Ge_{0.6}$ structures grown on relaxed 30% Ge virtual substrates at 550°C. In this plot, thin layers are 40 Å while thick layers are 85 Å.
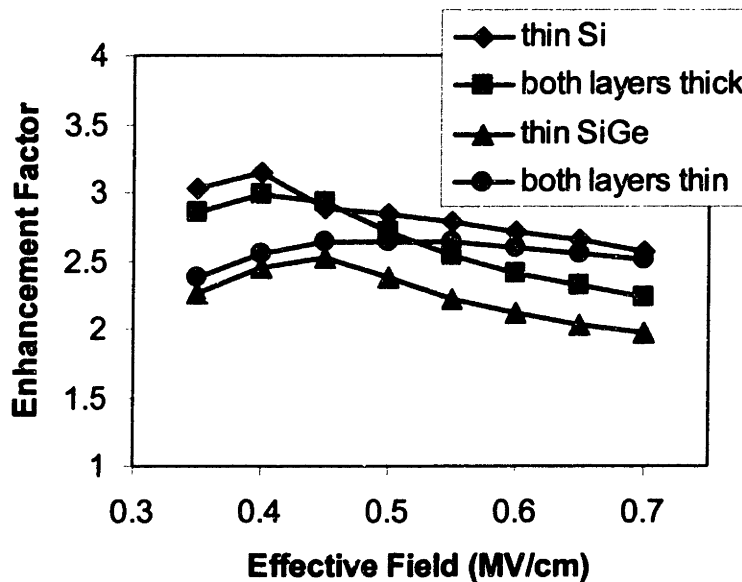
Figure 6.7 Hole mobility enhancement factors versus effective vertical field for different channel thicknesses in dual channel $Si/Si_{0.4}Ge_{0.6}$ heterostructures on relaxed $Si_{0.7}Ge_{0.3}$ virtual substrates. Thin channels are 40 Å while thick channels are 85 Å. Hole mobility enhancements are maintained at high vertical fields by minimizing the strained Si surface channel thickness.

These plots clearly illustrate the advantage of having a thin strained Si surface layer. The sample with an 85 Å $Si_{0.4}Ge_{0.6}$ channel and a 40 Å strained Si cap displays the highest mobility enhancement over the entire range of vertical fields investigated. In this case,

the strained Si layer is too thin to allow significant hole population, forcing holes to occupy the high mobility buried channel. The strained Si surface layer should have even less influence for higher Ge content channels, where the large band offset between the buried compressive $Si_{1-y}Ge_y$ and surface Si effectively confines holes within the buried layer. Thus, the extent to which dual channel heterostructures are buried or surface channel devices can be modulated by varying channel thicknesses. Moreover, recent research indicates that strained Si layers of roughly 50 Å are sufficient for high mobility Si n-type MOSFETs,[52] so a reduction of strained Si thickness should not degrade n-MOSFET performance in devices fabricated on the same layer structure.

Chapter 7.   Conclusions and Future Work

7.1.   Summary of Experimental Work

For the first time, a model for dislocation dynamics in compositionally graded buffers has been extended to SiGe. The effects of dislocation glide, blocking, and reduction kinetics in relaxed SiGe have been explored, leading to a unified picture of strain relaxation in these films. In general, dislocation glide kinetics control strain relaxation in compositionally graded SiGe buffers. However, final threading dislocation density may also be influenced by dislocation nucleation and reduction reactions, the strength of which can vary with substrate offcut. In general, while use of offcut substrates will lead to lower dislocation pile-up densities, dislocation reduction reactions will also be suppressed in films grown on these substrates. Finally, we have shown that dislocation pile-up formation will be accompanied by a rise in field threading dislocation density. Taken together, this data clearly indicates that high growth temperatures are the key experimental variable in producing high quality SiGe virtual substrates.

Record mobility strained Si p-MOSFETs have been fabricated on relaxed $Si_{0.6}Ge_{0.4}$ virtual substrates. For the first time, a saturation in hole mobility enhancements under high strain levels in strained Si p-MOSFETs has been observed. Furthermore, strain was proven to be the key variable in determining mobility enhancements in these devices, while channel thickness does not significantly influence high-field hole mobility. Earlier work on strained Si n-MOSFETs has led to similar conclusions.[52] A summary of electron and hole mobility enhancements as a function of strain is presented in Figure 7.1 below.
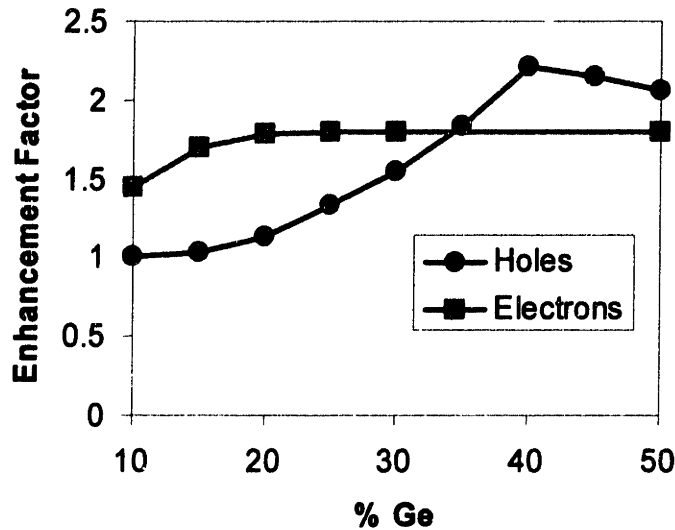
Figure 7.1 Electron and hole mobility enhancements in strained Si surface channel MOSFETs, taken at vertical fields of 0.6 MV/cm. Electron mobility enhancements saturate at 20% Ge, while hole mobility enhancements saturate at 40% Ge. Symmetric enhancements are obtained for strained Si MOSFETs on $Si_{0.65}Ge_{0.35}$ virtual substrates. Experimental data for strained Si n-MOSFETs and p-MOSFETs between 10% Ge and 30% Ge was obtained from Currie et al.[52] Electron mobility enhancements in strained Si n-MOSFETs on $Si_{0.5}Ge_{0.5}$ virtual substrates were obtained from measurements on dual channel heterostructures.

For strained Si MOSFETs on relaxed 35% Ge virtual substrates, symmetric mobility enhancements of 80% over bulk Si are obtained. Beyond 35% Ge, hole mobility enhancements actually exceed electron mobility enhancements, which could potentially decrease the mismatch in device size between n- and p-MOSFETs. Taken as a whole, strained Si MOSFETs display excellent potential for next-generation CMOS devices.

The effects of alloy scattering on tensile strained SiGe surface channels and compressively strained SiGe buried channels were explored. For tensile strained SiGe alloy channels, electron mobility is degraded much more severely than hole mobility. In compressively strained SiGe buried channels, high hole mobility enhancements are obtained for channel compositions beyond 60% Ge, where the large band offsets between the $Si_{1-y}Ge_y$ channel and strained Si surface channel, coupled with the low effective mass

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of holes in the $Si_{1-y}Ge_y$ layer, leads to high hole mobility. Though the highest hole mobility compressively strained SiGe heterostructures have utilized pure Ge channels,[107] lower Ge content channels are much simpler to integrate while still offering enormous improvements in hole mobility over bulk Si.

The useful design space for dual channel heterostructures has been explored. In general, buried channel composition and thickness play the most important role in determining hole mobility, while strain is a secondary variable (unlike in strained Si). These observations have been supported by theoretical predictions.[71] Peak hole mobility enhancements of 5.15 over bulk Si have been obtained in p-MOSFETs by combining tensile strained Si surface channels and compressively strained 80% Ge buried channels grown on relaxed 50% Ge virtual substrates. This dual channel heterostructure also displays nearly symmetric electron and hole mobility over a wide range of effective fields. These results indicate that dual channel heterostructures display enormous potential for realizing symmetric mobility CMOS, with both electron and hole mobility enhanced over bulk Si, possibly liberating modern microelectronics from the burden of poor p-MOSFET performance.

7.2.   Areas for Further Work and Future Prospects

While control over defect density in SiGe graded buffers has been realized over the entire composition range, defect density still rises slightly beyond 50% Ge. Detailed studies of graded layers in this composition range will be necessary for further optimization of Ge virtual substrate growth sequences. In particular, further studies should explore the influence of grading rate, growth temperature, and nucleation in the compressive Ge cap layer. Furthermore, our understanding of dislocation dynamics in

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graded buffers could be aided greatly by *in situ* characterization studies. *In situ* X-ray diffraction studies could yield valuable information regarding the kinetics of dislocation nucleation and strain relaxation in graded buffers, while *in situ* electron microscopy studies could be extended from single mismatched layers to more complex graded structures. Finally, further improvements in material quality should be possible by suppressing the nucleation sources always present in this study. Simply switching to a cold-wall deposition system located in a clean room should reduce dislocation pile-up density significantly. Indeed, recent reports of very low dislocation densities in graded SiGe alloys grown in a cold-wall plasma-enhanced CVD system are very encouraging.[27]

One of the major remaining challenges in SiGe virtual substrates involves integration strategies for strained Si/SiGe MOSFETs with III-V devices. Currently, Ge virtual substrates require thick buffer layers. To realize the full advantages of monolithic integration, all device layers should be nearly coplanar, which could be accomplished by growth in recessed patterns or novel wafer bonding schemes. Similarly, with the drive towards adoption of silicon-on-insulator (SOI) technology into CMOS processes, these integrated heterostructures will likely need to be incorporated onto insulating substrates. Considering the potential for enormous increases in functionality using SiGe virtual substrates (where light emission, detection, and signal processing could be incorporated onto one chip), process integration is one of the key remaining challenges in this area.

Strained Si surface channel MOSFETs are at the crossroads of experiment and commercialization, and many of the remaining questions deal with suitable processing sequences for state-of-the-art CMOS circuits. In particular, detailed assessment of strained Si device fabrication, encompassing thermal budget and reliability evaluation,

needs to be undertaken before strained Si can make an impact in the marketplace. Process sequences will also have to be designed that minimize strained Si removal, particularly since higher strain levels (and hence thinner channels) provide significant hole mobility enhancements. While these questions are probably best answered in commercial Si fabs, several fundamental issues are amenable to university-based experiments. The impact of misfit dislocation scattering on carrier mobility in strained Si MOSFETs remains a mystery. Similarly, the impact of Ge atoms on the Si/SiO_2 interface should be explored further. Finally, the physics of high-field mobility enhancements, particularly in strained Si p-MOSFETs, should be studied further.

While dual channel heterostructures are promising candidates for advanced SiGe-based CMOS applications, much about these heterostructures remains unknown. First-order device qualification via fabrication of thermally oxidized MOSFETs with thin gate oxides could provide valuable information regarding high-field mobility enhancements, drive current enhancements, and thermal budget evaluation. Detailed C-V studies on these devices, coupled with quantum-mechanical-based device modeling, could determine carrier population as a function of applied gate bias, channel thickness, and buried channel composition, enabling further optimization of these heterostructures. Device modeling studies indicate that subthreshold characteristics are degraded in both n-MOSFETs and p-MOSFETs based on dual channel heterostructures,[139] so an acceptable trade-off between drive current enhancements and subthreshold characteristics needs to be determined. In general, the key question remaining to be answered in these devices is: will the tremendous increases in hole mobility translate into increased overall device and circuit performance? While the high mobilities in these heterostructures demonstrated in

Chapter 6 are an important first step, individual device performance needs to be placed into the context of overall circuit design issues (such as cost versus performance). Furthermore, mobility enhancements in dual channel heterostructures need to be correlated with drive current enhancements in state-of-the-art MOSFETs. Finally, in a fashion similar to surface channel strained Si MOSFETs, process optimization studies should be undertaken in state-of-the-art MOSFETs based on these heterostructures in order to determine the unique processing requirements for this class of devices.

The ultimate extension of high mobility dual channel p-MOSFETs would of course incorporate both strained Ge and Si channels. Lee et al. have fabricated these heterostructures on 70% Ge virtual substrates, with hole mobility enhancements of eight times that of bulk Si.[107] However, the strained Si surface channel in these devices had a high density of threading dislocations, which would be deleterious to n-MOSFET performance. For this application, a 50% Ge virtual substrate would be an acceptable trade-off between strain in the two channels. In this case, the critical thickness for each layer on this substrate would be about 50 Å, which is of sufficient thickness for MOSFETs. In this work, we have attempted to fabricate such a heterostructure by depositing the Ge channel at 400°C. A cross-sectional TEM image of this heterostructure is given in Figure 7.2 below.

Figure 7.2 Cross section TEM image of a dual channel heterostructure incorporating a buried strained Ge channel and a strained Si surface channel on a relaxed 50% Ge virtual substrate. The buried Ge layer is extremely thin and has undulated severely.

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Unfortunately, the buried Ge channel was too thin (~ 30 Å) to sufficiently confine holes

in this heterostructure. Also, despite the low growth temperature, this layer undulated

severely, further degrading hole mobility. Figure 7.3 is a plot of effective hole mobility

versus effective vertical field for this heterostructure. Despite the thin, islanded Ge layer,

hole mobility in this heterostructure is still significantly enhanced over strained Si,

illustrating the potential of this class of heterostructure for producing high mobility p-

MOSFETs.
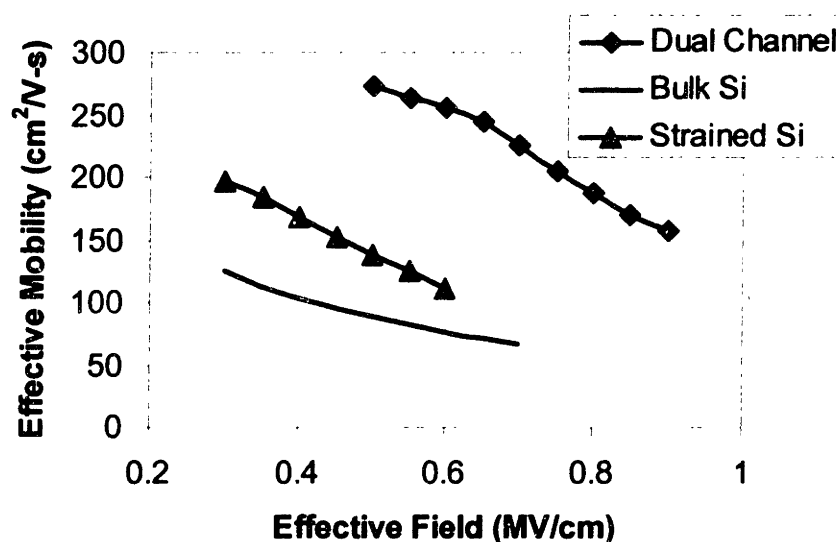
Figure 7.3 Effective hole mobility versus effective vertical field for a dual channel heterostructure consisting of a buried undulated Ge channel and a strained Si surface channel on a relaxed 50% Ge virtual substrate, compared to strained Si and bulk Si p-MOSFETs. Despite having a very thin, undulated strained Ge layer, hole mobility in this dual channel heterostructure is still significantly higher than in strained Si.

The difficulties in creating dual channel heterostructure MOSFETs with pure Ge

channels help to illustrate the challenges inherent in adopting more complex

heterostructures into MOSFET processes. In general, as Ge composition of the buried

channel increases, graded buffer thickness must increase, growth temperature must

decrease, and high quality strained Si layers are more difficult to incorporate. These

considerations may warrant gradual adoption of SiGe heterostructure MOSFET

technology, with increasing Ge content leading to increased performance. This concept

is illustrated dramatically in Figure 7.4 below, which compares effective hole mobility

versus effective vertical field for bulk Si, strained Si (on 20% Ge virtual substrates and

40% Ge virtual substrates), and dual channel heterostructures (under constant strain such

that the difference between buried channel and virtual substrate composition is 30% Ge).
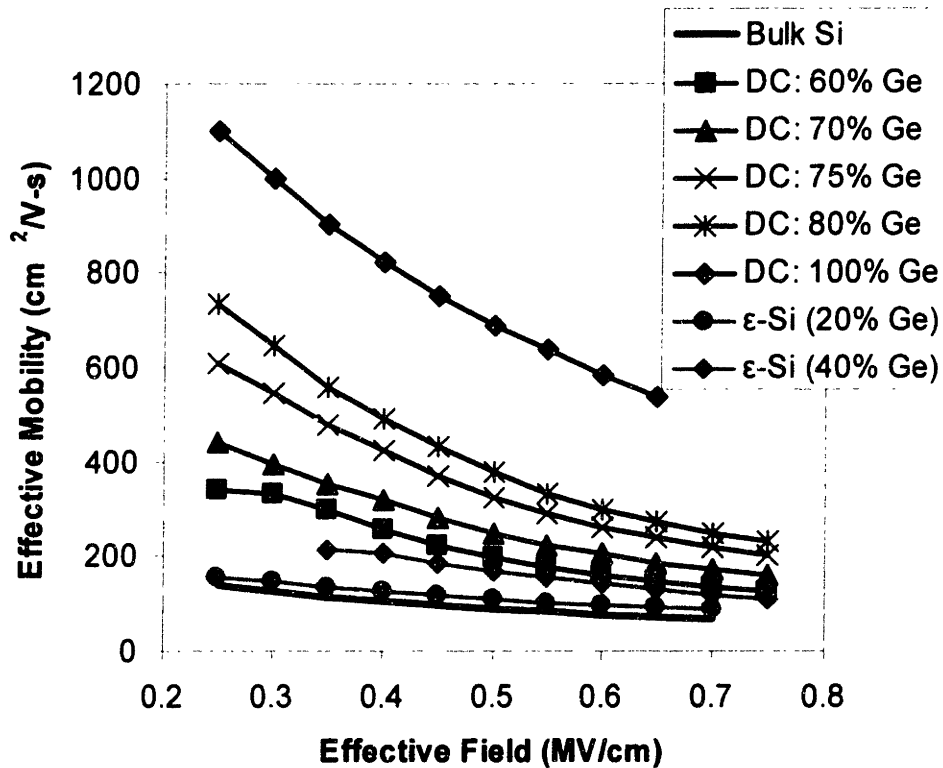
Figure 7.4 Comparison of effective hole mobility versus effective vertical field for strained Si (denoted ε-Si) and dual channel heterostructure (denoted DC; buried channel composition has been indicated) MOSFETs. Each curve represents a different technology node for SiGe-based CMOS, where increased performance is balanced with increased integration complexity. The strained Si on relaxed $Si_{0.8}Ge_{0.2}$ curve has been adapted from Currie et al.[52] while the Ge dual channel heterostructure curve has been adapted from Lee et al.[107]

Strained Si p-MOSFETs display moderate enhancements in hole mobility over bulk Si,

and are relatively simple to incorporate into CMOS processes. Dual channel

heterostructures display large hole mobility enhancements (and identical mobility to strained Si surface channel n-MOSFETs), and hole mobility increases with buried channel Ge content. However, as Ge content increases, these layers become more difficult to grow and incorporate into CMOS processes. Essentially, this is analogous to traditional CMOS scaling, where each technology node (gate length) brought increased performance but required extensive research and development. Now, with Ge content as the new scaling parameter, each step in Ge composition will greatly increase performance but will also require thorough optimization of growth and process parameters. SiGe-based heterostructure MOSFETs not only offer the potential for greatly increased MOSFET performance, but also emerge as the new scaling platform as traditional device scaling comes to an end.

Appendix A. Analysis of Graded Buffers by Triple-Axis X-Ray Diffraction

Triple-axis x-ray diffraction is a valuable tool for determining composition and strain in SiGe graded buffers. Generally, for low-Ge-content buffers grown on on-axis substrates, a combination of (004) and (224) glancing incidence and glancing exit $\theta/2\theta$ scans are sufficient for accurate determination of composition. Depending on the resolution required, these scans may either be done in double-axis or triple-axis mode. However, for films with large net tilt (generally, high-Ge-content films grown on offcut substrates), triple-axis reciprocal space maps must be utilized. The necessary equations for analysis of graded buffers through these methods are presented below;[140] detailed discussions of epitaxial thin film analysis by x-ray diffraction are given by van der Sluis,[141] Fewster,[142] and Swaminathan and Macrander.[143]

Symmetric $\theta/2\theta$ rocking curves, where the angle of incidence of the x-ray beam equals the angle of reflection, provide accurate measurement of the perpendicular lattice parameter in an epitaxial film. In an (004) scan (our choice for symmetric scans), $a_\perp$, the perpendicular film lattice constant, is calculated directly from Bragg's Law:

$$a_\perp = \frac{2 \cdot \lambda}{\sin(\theta_B + \Delta\theta_{sym})},$$

where θ_B is the substrate Bragg angle, λ is the x-ray wavelength, and $\Delta\theta_{sym}$ is the angular difference between the substrate and film peak in the rocking curve. This equation often appears in an equivalent form, using the substrate lattice parameter (a_s) in the calculation:

$$a_\perp = [\frac{\sin(\theta_B)}{\sin(\theta_B + \Delta\theta_{sym})} - 1] \cdot a_s + a_s$$

which is valid for all scan types. If the degree of relaxation of a film is known beforehand, a single symmetric $\theta/2\theta$ rocking curve is sufficient to fully characterize the film. However, the opposite is usually the case—the x-ray diffraction is done to determine the degree of relaxation. To gain any information about the in-plane lattice constant, $a_{\parallel}$ (and therefore strain and relaxation), asymmetric scans are necessary.

In principle, further information can be derived solely from two asymmetric scans, one glancing exit and the other glancing incidence. In this case, the angular separation between the substrate and film peak in each geometry is denoted by $\Delta\omega_{ge}$ and $\Delta\omega_{gi}$, respectively. Traditionally, a tetragonal film lattice with no tilt is assumed, and an asymmetric $\theta/2\theta$ rocking curve is used to calculate both $a_{\perp}$ and $a_{\parallel}$:

$$a_{\perp} = a_s \cdot \frac{\sin\theta_{B,asym}}{\sin(\theta_{B,asym} + \Delta\theta)} \cdot \frac{\cos\phi}{\cos(\phi + \Delta\phi)}$$

$$a_{\parallel} = a_s \cdot \frac{\sin\theta_{B,asym}}{\sin(\theta_{B,asym} + \Delta\theta)} \cdot \frac{\sin\phi}{\sin(\phi + \Delta\phi)},$$

where $\theta_{B,asym}$ is the Bragg angle for the asymmetric plane, ϕ is the angle between the asymmetric and symmetric planes in a cubic lattice, $\Delta\phi = (\Delta\omega_{ge} - \Delta\omega_{gi})/2$, and $\Delta\theta = (\Delta\omega_{ge} + \Delta\omega_{gi})/2$. We have typically chosen to use the (224) reflection for asymmetric scans since they usually provide sufficient intensity and peak separations in diamond cubic crystal structures for our purposes.

Tilt in a film is defined as the number of degrees consecutive (004) planes differ from being parallel. The above two equations can be modified for tilt by taking all four scans for a set of planes in either of the glancing geometries (e.g. (224), $(2\bar{2}4)$, $(\bar{2}\bar{2}4)$, and

($\bar{2}\bar{2}4$)) and averaging the separation distances between substrate and film peak in each of the scans.

The above formulation provides a quick means of evaluating composition and strain in SiGe graded buffers, particularly in nearly fully relaxed films with little tilt. However, for partially relaxed films or films with large net tilt (> 0.25°), we have found that triple-axis reciprocal space maps are necessary to accurately determine relaxation and composition. In these scans, a series of $\theta/2\theta$ rocking curves are taken with the sample at different angular positions (*i.e.*, at different θ values), and the results are plotted as two-dimensional contour plots (ω vs. θ). In reciprocal space maps, the angular position of the sample is renamed ω to distinguish this axis from the $\theta/2\theta$ scanning direction.

In films with no tilt, a single (224) reciprocal space map provides complete x-ray diffraction data; an additional (004) map is necessary for films with tilt present. Reciprocal lattice wavevectors, $k_{||}$ and $k_{\perp}$, are calculated from (224) scans by

$$k_{||} = \frac{2}{\lambda}\sin(\theta_{B,224} + \Delta\theta_{224})\cdot\cos(\frac{\pi}{2} - (\phi - \Delta\omega_{224} + \Delta\omega_{004}))$$

$$k_{\perp} = \frac{2}{\lambda}\sin(\theta_{B,224} + \Delta\theta_{224})\cdot\sin(\frac{\pi}{2} - (\phi - \Delta\omega_{224} + \Delta\omega_{004}))$$

for the glancing incidence geometry and

$$k_{||} = \frac{2}{\lambda}\sin(\theta_{B,224} + \Delta\theta_{224})\cdot\cos(\frac{\pi}{2} - (\phi + \Delta\omega_{224} - \Delta\omega_{004}))$$

$$k_{\perp} = \frac{2}{\lambda}\sin(\theta_{B,224} + \Delta\theta_{224})\cdot\sin(\frac{\pi}{2} - (\phi + \Delta\omega_{224} - \Delta\omega_{004}))$$

for the glancing exit geometry. In all cases, $\theta_{B,224}$ is the substrate Bragg angle, $\Delta\theta_{224}$ is the angular separation between substrate and film (224) peaks (negative for compressive

films, positive for tensile films), ϕ is the angle between (224) and (004) planes (35.264°),

$\Delta\omega_{224}$ is the separation between substrate and film peaks for the (224) scan, and $\Delta\omega_{004}$ is

the separation between substrate and film peaks for the (004) map (which is zero in a film

with no tilt). All terms involving Δ are referenced to the substrate; i.e., Δ = film-

substrate.

From the above equations, calculation of lattice parameters and relaxation is

straightforward:

$$a_{\parallel} = 2\sqrt{2} / k_{\parallel}$$

$$a_{\perp} = 4 / k_{\perp},$$

and

$$a_r = \frac{(a_{\perp} + (v \cdot a_{\parallel}))}{1 + v}$$

$$composition = \frac{a_r - a_s}{a_f - a_s}$$

$$strain = \frac{a_{\parallel} - a_r}{a_r}$$

$$misfit = \frac{a_s - a_r}{a_r}$$

$$\%relaxation = [1 - \frac{|strain|}{|misfit|}] \cdot 100,$$

where a_r is the lattice parameter of a fully relaxed film of the composition measured, v is

Poisson's ration, and a_f is the lattice parameter of pure film with 100% alloy composition.

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Appendix B. Short Flow MOSFET Fabrication Sequence

The following section outlines the MTL machines and recipes used in short flow

MOSFET fabrication. Both MIT's Integrated Circuits Laboratory (ICL) and Technology

Research Laboratory (TRL) were used in this process. In cases where more than one

machine could be utilized for a given step, the preferred machine is italicized.

Process Module	Machine	Description
Gate Stack Deposition	ICL RCA	Modified RCA Clean (5-10 min. piranha clean, 15 s 50:1 H$_2$O:HF dip, 2.5-15 min. SC-2 clean)
Gate Stack Deposition	ICL tubeA7	Deposition of 3000 Å LTO (recipe 462, 400°C; average deposition rate ~ 100 Å/min.)
Gate Stack Deposition	ICL tubeA6	Deposition of 500 Å poly-Si (recipe 705, 560°C; average deposition rate ~16 Å/min.)
Backside Clear	ICL HMDS	Coat wafers with HMDS; standard recipe
Backside Clear	ICL coater6	Coat wafer fronts with 1 μm positive resist and post-bake; standard recipe
Backside Clear*	ICL oxide	Remove backside native oxide with 5 s BOE dip
Backside Clear	ICL AME5000	Remove backside poly-Si with poly_std etch
Backside Clear	ICL oxide	Remove backside LTO with 30 s BOE dip
Backside Clear	ICL pre-metal or *ICL asher*	Remove photoresist with either standard asher recipe or 10 min. piranha clean
Frontside Patterning	ICL HMDS	Coat wafers with HMDS; standard recipe
Frontside Patterning	ICL coater6	Coat wafer fronts with 1 μm positive resist; standard recipe
Frontside Patterning	ICL stepper2 or *TRL EV1*	Expose photoresist through MOBIL mask
Frontside Patterning	ICL developer or *TRL photowet-1*	Develop photoresist
Frontside Patterning	ICL coater6 or *TRL postbake*	Post-bake photoresist
Frontside Patterning*	ICL oxide	Remove frontside native oxide in exposed regions with 5 s BOE dip
Frontside Patterning	ICL AME5000	Etch frontside poly-Si in exposed regions with poly_std etch
Frontside Patterning	ICL AME5000	Etch frontside LTO in exposed regions with Matt_LTO etch, leaving ~250 Å LTO remaining

Frontside Patterning	ICL UV1280	Use ellipsometry to verify pre- and post-etch LTO thicknesses and calibrate LTO etch rates
Frontside Patterning	*ICL asher* or TRL asher	Remove photoresist with standard asher recipe
Frontside Patterning	*ICL oxide* or TRL acid-hood	Remove remaining LTO and undercut gates with 30 s BOE dip
Implant	Outside vendor	BF_2 or As, 35 keV, 1×10^{12} ions/cm^{-2}; 4 identical implants at 90° rotation
Implant	TRL tubeA2	Post-implant clean; 2×60 s piranha clean
Implant	TRL tubeA2	30 min. anneal at 600°C in N_2 ambient
Metallization	ICL pre-metal	Pre-metal clean; 60s piranha clean, 20 s 50:1 H_2O:HF dip
Metallization	ICL e-beam	Deposit 500 Å Ti + 1000 Å Al on wafer fronts
Metallization*	ICL e-beam	Deposit 5000 Å Al on wafer backsides

* Optional

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