InGaAs/GaAsSb Type-II Heterojunction Vertical Tunnel-FETs

By

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Abstract

The supply voltage (V_{DD}) scaling of conventional CMOS technology is approaching its limit due to the physical limit of 60 mV/dec subthreshold swing (SS) at room temperature and the requirement for controlled leakage current. In order to continue V_{DD} scaling for low power applications, novel device structures with steep SS have been proposed. Tunnel-FETs (TFETs) are among the most attractive device structure due to their compatibility with conventional CMOS technology and the potential for outstanding V_{DD} scalability. Heterostructure vertical TFETs with enhanced gate modulation promise significantly improved electrostatic control and drive current relative to lateral tunneling designs. In this thesis, vertical TFETs based on InGaAs/GaAsSb heterostructure are investigated in terms of design, fabrication and electrical characterization.

$In_{0.53}Ga_{0.47}As$/ $GaAs_{0.5}Sb_{0.5}$ heterostructure vertical TFETs are fabricated with an air-bridge structure, designed to prevent parasitic tunneling path in the device, with a two-step highly selective undercut process. Electrical measurement of the devices with various gate areas demonstrates area-dependent tunneling current. The $In_{0.53}Ga_{0.47}As$/ $GaAs_{0.5}Sb_{0.5}$ vertical TFETs with HfO_2 high-k gate dielectric (EOT ~ 1.3 nm) exhibit minimum sub-threshold swings of 140 and 58 mV/dec at 300 and 150 K respectively, with an ON-current density of 0.5 $\mu A/\mu m^2$ at V_{DD} = 0.5 V at 300 K. A physical model of TFET operation in the ON-state is proposed based on temperature dependent measurements, which reveal a current barrier due to an ungated region near the drain. Simulations illustrate that the gate-to-drain distance must be scaled to eliminate this barrier. In diode-mode operation, outstanding backward diode performance is demonstrated in this system for the first time, with gate-tunable curvature coefficient of 30 V^{-1} near V_{DS} = 0 V. These results indicate the potential of vertical TFETs in hybrid IC applications.

Acknowledgements

In the past two years, it is really hard to count how many people have helped me accomplish the goals in this thesis. The group of intelligent gave me strong motivation and kind advice during my hard times. The things I learned and achievements I attained are impossible without their support and help.

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Chapter 1. Background and Motivation

This chapter introduces the physical background, motivation and design of the InGaAs/GaAsSb based type-II heterostructure tunnel-FETs (TFETs). First, the need for low power FET devices with further voltage scaling will be introduced; second, emerging candidates for future ultra-low-power applications will be demonstrated and previous work on TFETs will be discussed. Then, the motivation for InGaAs/GaAsSb based TFETs structure will be illustrated. Finally, a design for InGaAs/GaAsSb based type-II heterostructure TFET is proposed.

1.1 Scaling and Power Consumption

The downscaling of the complementary-metal-oxide-semiconductor (CMOS) technology has been following Moore's law for decades. Especially, the critical dimension of the recent CMOS technology is approaching sub-10 nm according to the International Technology Roadmap for Semiconductor (ITRS) [1]. On the other hand, the scaling rule also calls for a proper scaling of the operating voltage (V_{DD}) of the logic circuit, so that the power consumption can be minimized according to the well-known expression for the power in digital circuits [2]:

$$P = \alpha C V_{DD}^2 f + V_{DD} \cdot I_{leak}$$

where α is the active factor, C is the total capacitance, f is the switching frequency, and I_{leak} is the leakage current in the OFF-state, or OFF-current. By lowering V_{DD}, not only the active portion ($\alpha C V_{DD}^2 f$) but also the subthreshold portion ($V_{DD} \cdot I_{leak}$) can be effectively reduced. However, the scaling of V_{DD} is reaching its limit (Fig. 1.1.1). This is mainly due to the constraints from the speed, subthreshold power and the physical limit of 60 mV/dec sub-

threshold swing (*SS*), and the 60 mV/dec *SS* limit arises from the thermionic injection behavior at the source [2]:

$$SS = \frac{dV_G}{d\Psi_S}\frac{d\Psi_S}{d(\log I_D)} \geq \frac{kT}{q}\ln 10 = 60 \text{ mV/dec} \quad \text{at } 300 \text{ K}$$

As shown in Fig. 1.1.2, in order to satisfy the demand of high-speed applications, large ON-current at $V_{GS} = V_{DD}$ is desired which leads to substantially large overdrive voltage ($V_{GT} = V_{GS} - V_{TH}$). On the other hand, due to the physical limit of 60 mV/dec in the subthreshold region, it becomes difficult to achieve low subthreshold power dissipation (i.e., low OFF-current). As illustrated in Fig. 1.1.3 [3], with the advancement of the CMOS technology, the subthreshold power dissipation starts to dominate, indicating that V_{TH} cannot further scale in a power-aware digital circuit design. Therefore, the scalability of V_{DD} is limited in the conventional CMOS technology with 60 mV/dec subthreshold swing.

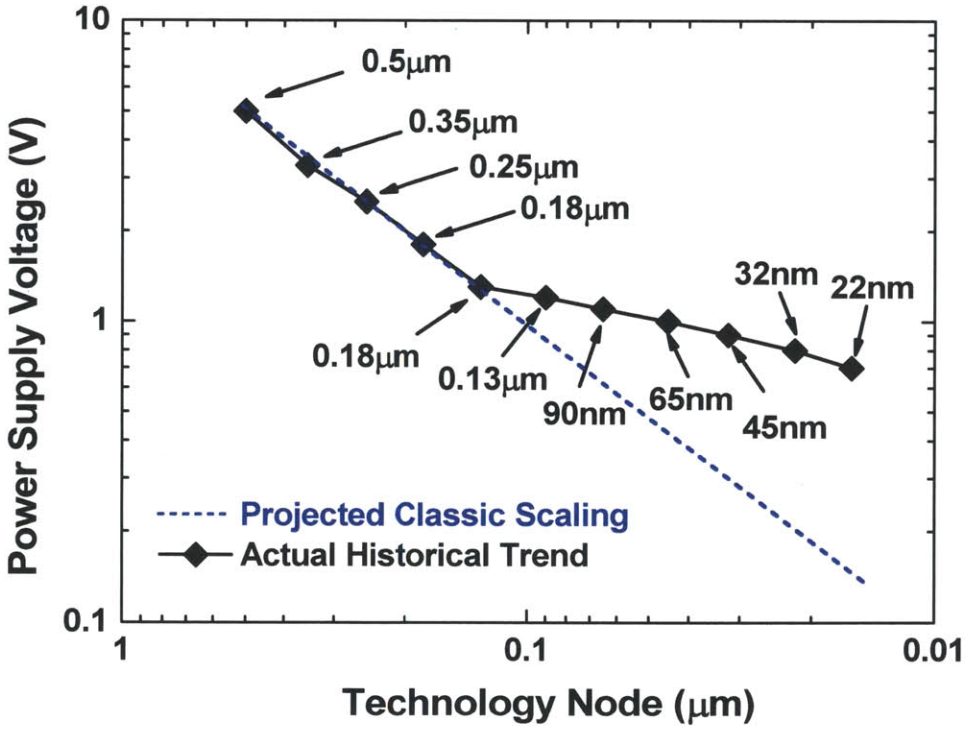


Fig 1.1.1 Power supply voltage (V_{DD}) for digital circuits [1]. V_{DD} scaling is becoming much slower and approaching its limit with the rapid downscaling of conventional CMOS technology.

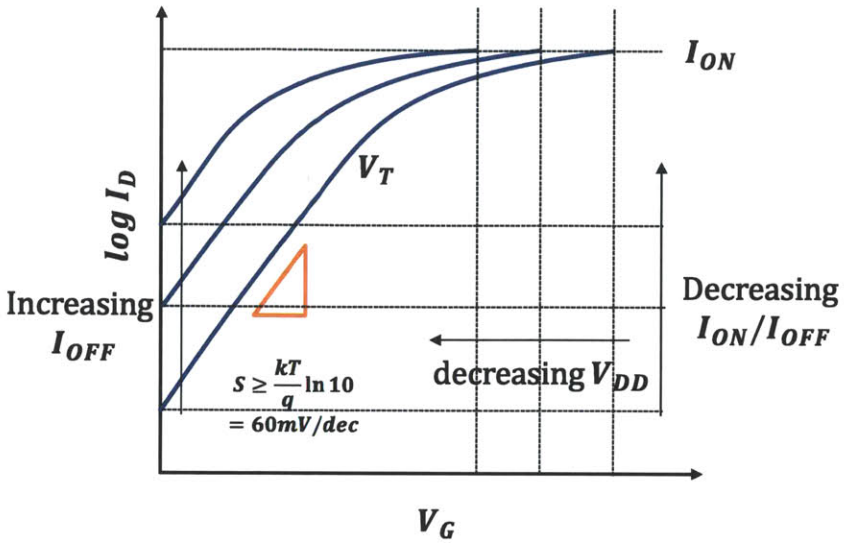


Fig 1.1.2 Schematic view of the transfer characteristic behavior of a conventional MOSFET with scaling V_{DD}. To maintain the performance of the MOSFET, the ON-current (or V_{DD}-V_{TH}) is kept the same, leading to exponentially increased OFF-current due to the physical limit of 60 mV/dec subthreshold swing. Hence, the ON/OFF ratio of the device dramatically decreases.

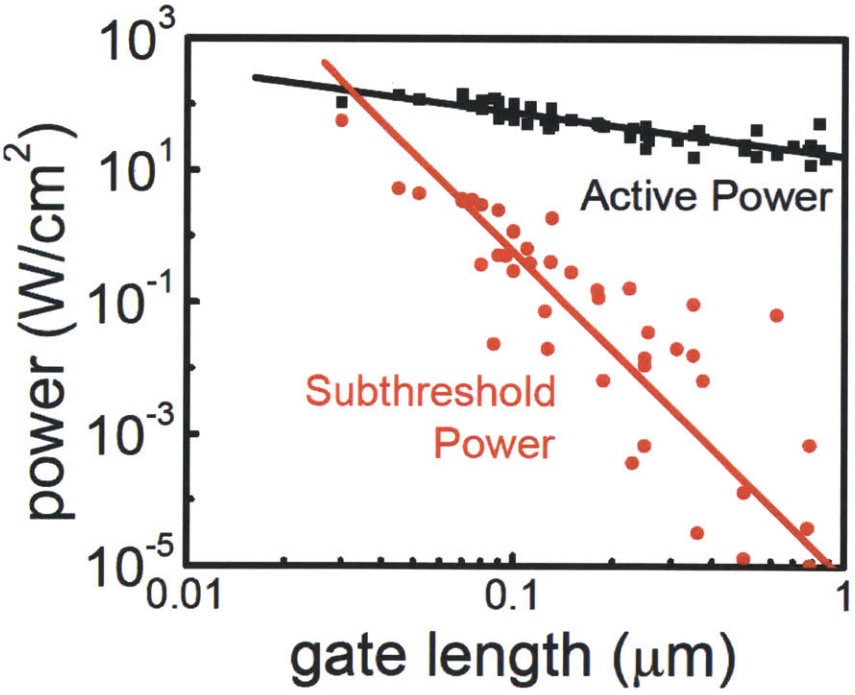


Fig 1.1.3 Active (black) and subthreshold (red) power dissipation for a digital IC with evolving CMOS technology [3]. The subthreshold power dissipation is increasing much faster than the active power dissipation, mainly due to the exponentially increased OFF-current as V_{DD} downscales. The subthreshold power dissipation becomes dominant in the power-aware design of digital ICs.

1.2 Emerging Devices for Low Power Application

As the subthreshold power dissipation skyrocketed due to the continuing scaling of V_{DD}, novel types of transistors with the potential for *SS* below 60 mV/dec have been studied. Especially, impact-ionization MOSFET (I-MOS) [4]-[11] and tunnel-FET (TFET) [12] are popular due to the similarity of their device structures to conventional MOSFETs and CMOS technology compatibility (Fig 1.2.1). The device operation of the I-MOS and TFET is illustrated in Fig 1.2.2. By utilizing the sharp turn on of the avalanche breakdown, the I-MOS device contains an intrinsic region where the electric field concentrates as the gate voltage increases. Thus, the avalanche breakdown takes place as the field exceeds the critical value and hence results in sub-60 mV/dec *SS*. The TFET, on the other hand, harnesses the sharp turn on of the tunneling process, which does not depend on the 60 mV/dec tail of the conduction band density of states. As seen in Fig 1.2.2 (b), the conduction band in the channel region is pushed down with increasing gate bias, and the tunneling takes place when the conduction band minimum in the channel region is aligned with the valence band maximum in the source, and the tunneled carriers are extracted by the drain.

1.3 Review of previous work on TFETs

In recent years, I-MOS research has decreased because the supply voltage cannot be scaled, due to the large field required for the avalanche breakdown [8]. On the other hand, a number of research studies have explored the potential of TFETs in achieving sub-60 mV/dec *SS* [13]-[36]. Experimental demonstrations of sub 60 mV per decade SS have been difficult to achieve. Another issue that hinders the TFET from practical application is its unacceptably low drive current due to the poor tunneling efficiency. In order to improve the drive current, TFET

structures with enhanced gate modulation and tunneling area have been proposed by Hu *et al.* [16], Kao *et al.* [33] and Asra *et al.* [27] on Si/SiGe system, as well as by Li *et al.* [32] and Zhou *et al.* [34] [36], on III-V material systems.

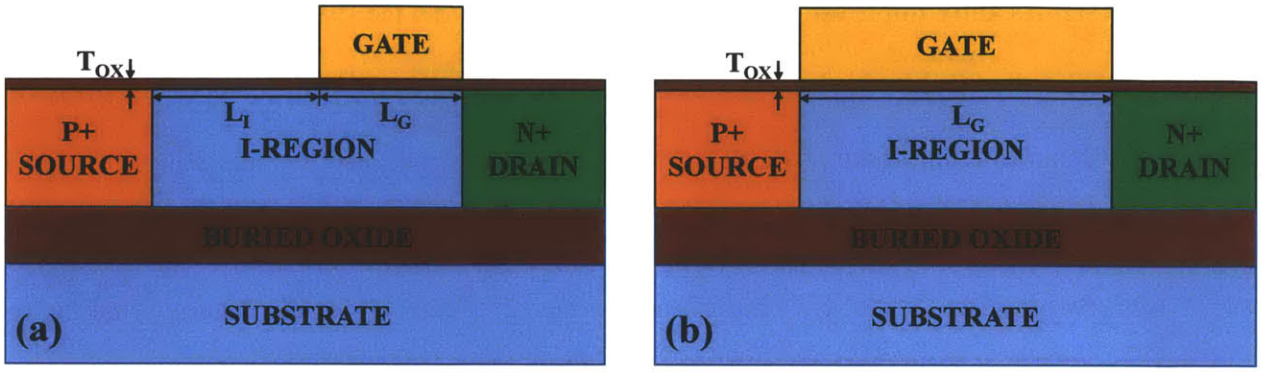


Fig 1.2.1 Schematic cross-sectional view of (a) I-MOS and (b) TFET. Both devices use p-i-n asymmetric doping scheme, but the different gate alignment to the junction result in different carrier transport mechanism.

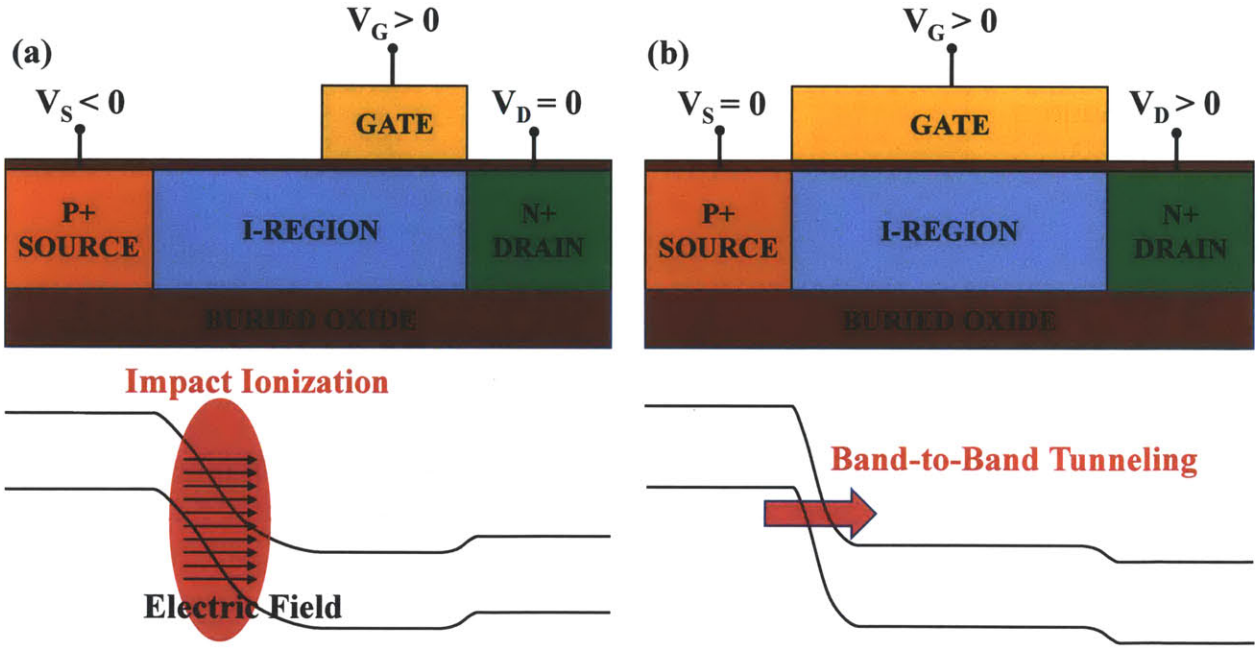


Fig 1.2.2 The operations of (a) I-MOS and (b) TFET. Due to the different gate alignment and bias conditions, the carrier generation mechanisms are complete different: the I-MOS concentrates electric field in the ungated i-region, and trigger avalanche breakdown; the TFET harnesses the band overlap within a narrow region and result in band-to-band tunneling.

The green transistor (gFET) structure is shown in Fig 1.3.1 (a) [16]. The implanted pocket provides additional bending on the source side of the lateral band profile, as well as an increased tunneling area. Simulations predict that the gFET yields at least 10x boost in the ON-current and significantly improved *SS* below 60 mV/dec. The device structure shown in Fig 1.3.1 (b) [33] makes the pocket big enough such that the tunneling direction becomes primarily vertical. In this way, the effective tunneling area is enhanced because the tunneling junction is dominated by the gate, which is much weaker in the case of conventional TFET structure. The structure shown in Fig 1.3.1 (c) [27] buries the source completely under the channel, making the tunneling direction aligned to the gate electric field. Hence, the tunneling junction is completely controlled by the gate and tunneling is significantly enhanced.

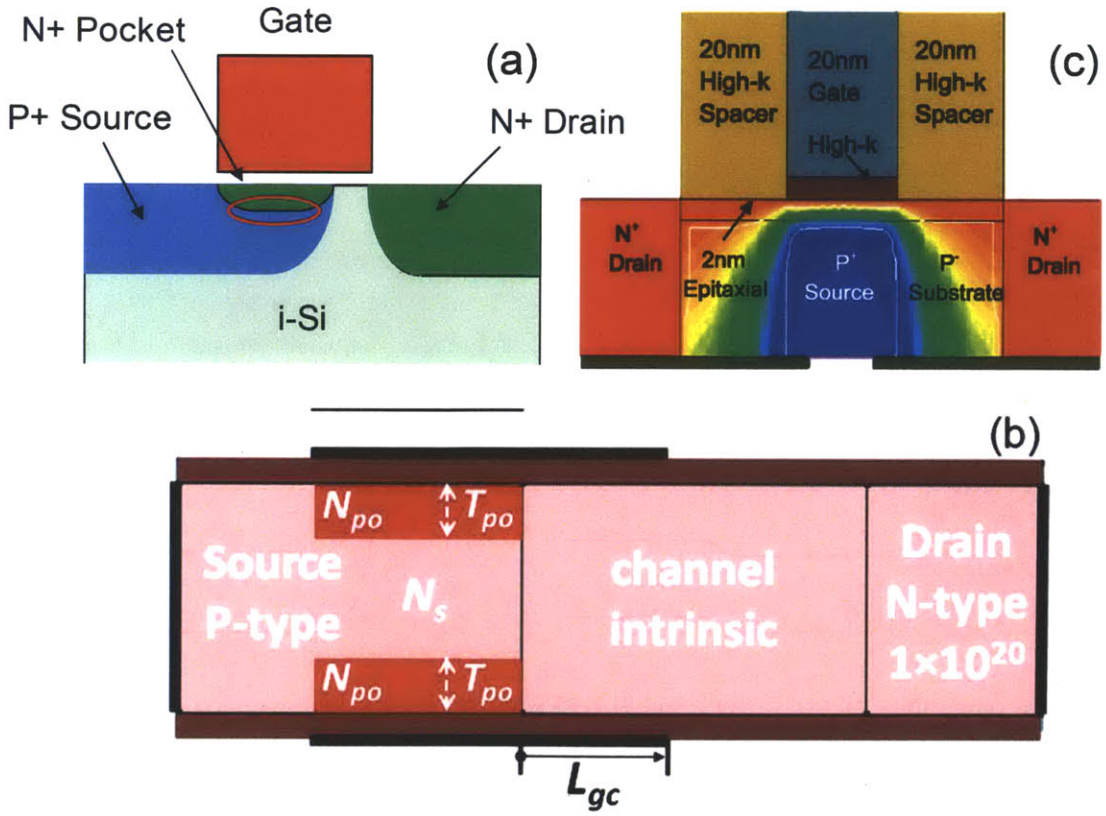


Fig 1.3.1 The schematic view of different TFET structures with pockets for gate modulation enhancement: (a) gFET [16]; (b) double-gate TFET with n-type pockets [33]; (c) buried p+ source [27].

By taking advantage of well-established III-V heterostructure epitaxial growth, the gate enhanced TFET structures are realized more easily than in Si/Ge. Another advantage of designing TFETs with III-V heterostructure is the numerous possible band alignments between the two materials, especially when ternary or quaternary alloys are involved. The III-V heterostructure TFET usually consists of two materials, one with high electron affinity (HEA) and one with low electron affinity (LEA), such that the electrons in the valence band of the LEA material can tunnel into the conduction band of the HEA material. As shown in Fig 1.3.2 (a) [32], the InAs/AlGaSb type-II heterostructure is used as device layers. The isolation between the source/drain and the ungated region is done by layer recess and air-bridge structure. Another vertical TFET structure is shown in 1.3.2 (b) and (c) with InAs/InP material system [34] and InAs/GaSb system [36]. This device structure completely cuts off any possible leakage source from the substrate, which is superior for leakage sensitive device design. Still, it is very challenging to fabricate, especially with ultra-thin InAs layer.

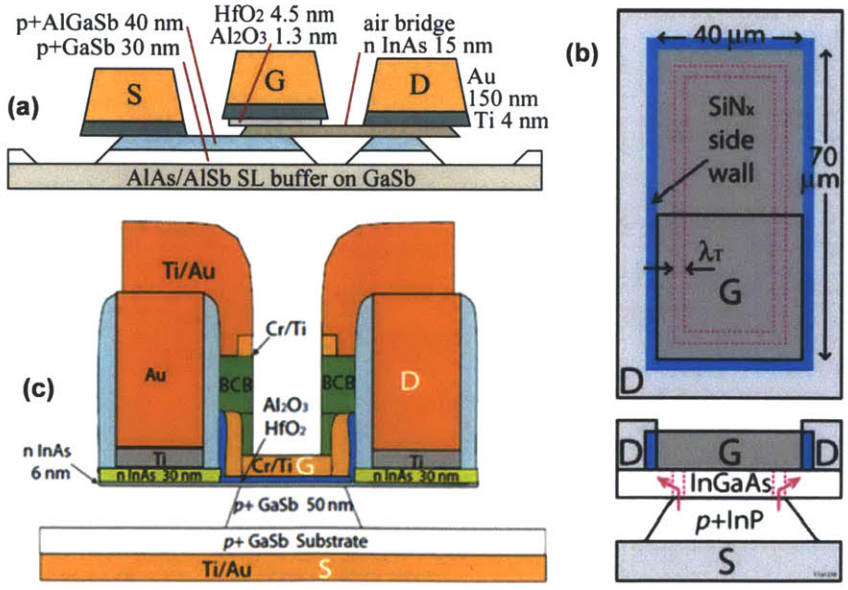


Fig 1.3.2 The schematic view of different III-V heterostructure vertical TFETs with enhanced gate modulation: (a) InAs/AlGaSb TFET with air-bridge structure [32]; (b) InGaAs/InP TFET with completely isolated S/D structure [34]; (c) InAs/GaSb TFET with completely isolated S/D structure [36].

1.4 InGaAs/GaAsSb Material System

As mentioned in Section 1.3, ternary compound semiconductors play an important role in designing the band alignment and tunneling properties of vertical TFETs with enhanced gate modulation. Especially, arsenide-antimonide based heterostructures are desirable because of their type-II band alignment with tunable effective bandgap [28]. The band diagrams of the device operation are plotted in Fig 1.4.1, where the effective bandgap, $E_{g\text{-}eff}$, is defined as the energy difference between the conduction band minimum (CB_{min}) of the HEA material and the valence band maximum (VB_{max}) of the LEA material. As shown in Fig 1.4.2 [37], the CB_{min} of InGaAs and decreases in energy as the In composition increases, while the VB_{max} of GaAsSb bows down between 50% and 100% Sb composition. Therefore, the effective bandgap, $E_{g\text{-}eff}$, from -150 meV to 270 meV can be achieved with different alloy composition (without quantum mechanics correction). Furthermore, if the material system consists of lattice mismatched layers and strain is taken into account, additional degrees of freedom are provided in the design of the epitaxial layers for the vertical TFETs.

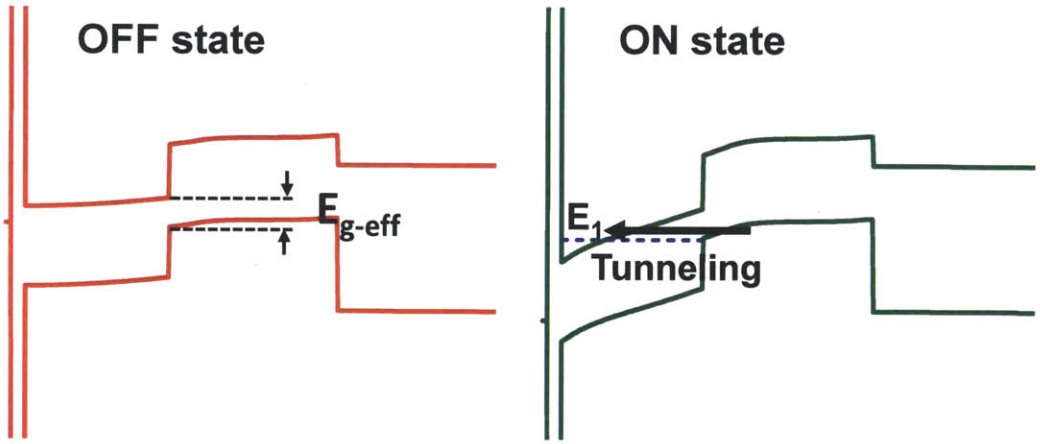


Fig 1.4.1 Energy band diagram of the device operation status, where the effective bandgap of the heterostructure is defined as $E_{g\text{-}eff}$. In OFF-state, the valence band of the low electron affinity (LEA) material does not overlap with the conduction band of the high electron affinity (HEA) material, so that tunneling does not happen; in ON-state, the bands overlap and tunneling takes place.

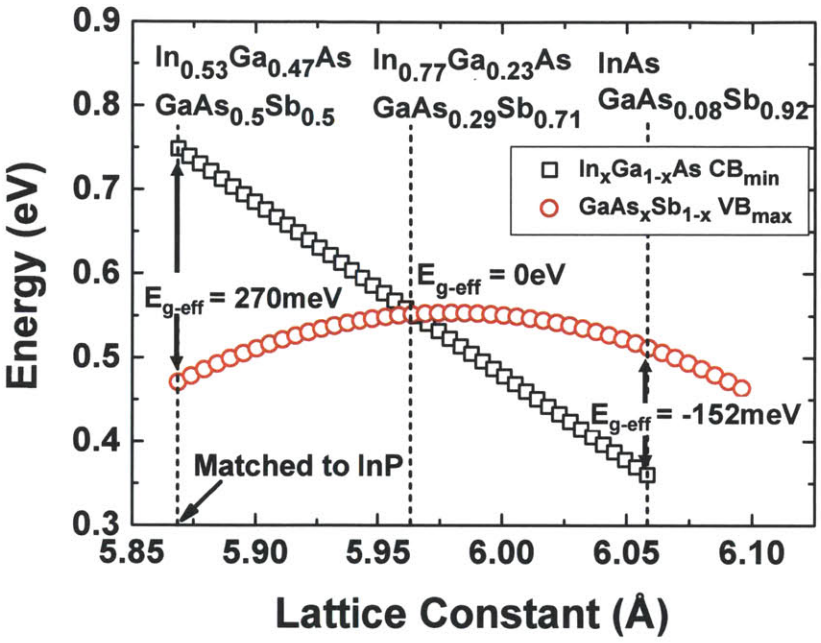


Fig 1.4.2 The CB_{min} of InGaAs and the VB_{max} of GaAsSb (referred to VB_{max} of InAs) for different lattice constants. The $E_{g\text{-}eff}$ is tunnable from -152 meV to 270 meV by varying alloy composition [37]

1.5 Ultra-thin $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ Vertical Tunnel-FET Design

In this thesis, $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ lattice matched to InP is used as the device heterostructure, which has an expected $E_{g\text{-}eff}$ of ~270meV. The 3-D schematic view of the $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ vertical TFET is drawn in Fig 1.5.1, where an air-bridge structure similar to [32] is used to prevent direct tunneling from source to drain under the drain contact. As shown in the schematics in Fig 1.5.2, both the air-bridge and the source recess have to be self-aligned to the gate and hence eliminate parasitic tunneling paths through the ungated region. Also, the dimensions of the device features and the layer thicknesses are important to achieve superior performance. The quantum-well (QW) structures are desired as QW-to-QW tunneling is expected to produce step-like turn on when the subbands of the QWs overlap [22]. Therefore, 15 nm ultra-thin layers are designed to have quantum confinement on the carriers and achieve QW-

to-QW tunneling behavior. On the other hand, the undercut of the GaAsSb layer under the gate (L_{UG}) (Fig 1.5.3 (a)) is critical to OFF-current suppression. Fig 1.5.3 (b) shows the Non-Equilibrium Green's Function (NEGF) simulation result (courtesy of M. Luisier) on InAs/GaSb TFET with various gate lengths (L_G) and L_{UG}, suggesting that the OFF-current is dominated by L_{UG} rather than L_G. Taking advantage of the isotropic undercut etching, a self-aligned air-bridge structure will suffice to provide L_{UG} large enough to prevent severe leakage current.

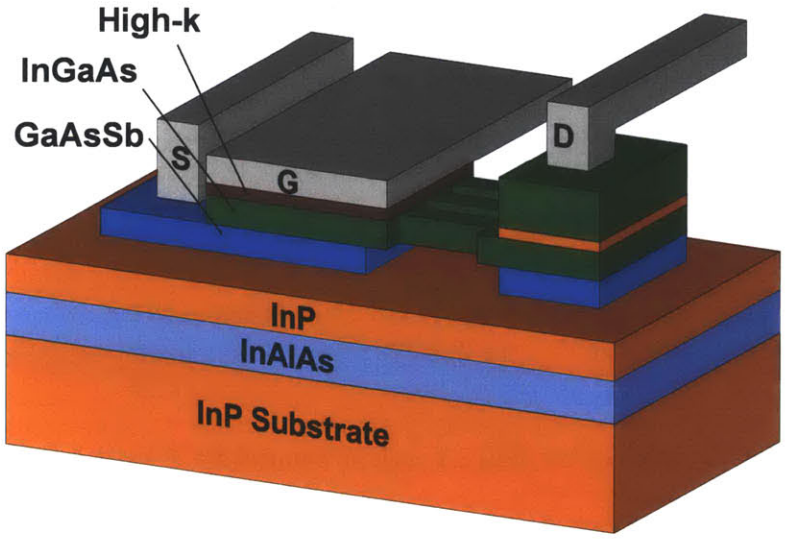


Fig 1.5.1 The 3-D schematic view of the InGaAs/GaAsSb vertical TFET on semi-insulating InP substrate. QW-to-QW tunneling with ultrathin layers provides step-like tunneling turn on; air-bridge structure is used to prevent direct S-D tunneling.

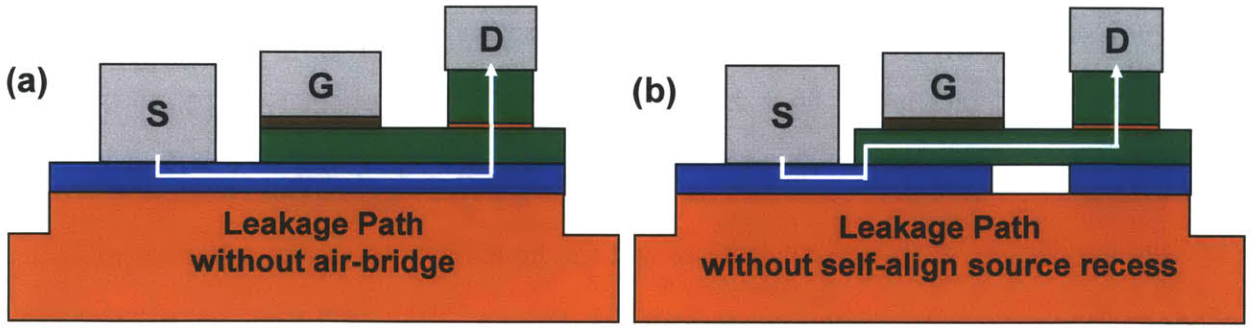


Fig 1.5.2 Possible leakage paths in vertical TFET structures. Self-aligned source recess and air-bridge structure are used in this study to suppress these leakage paths.

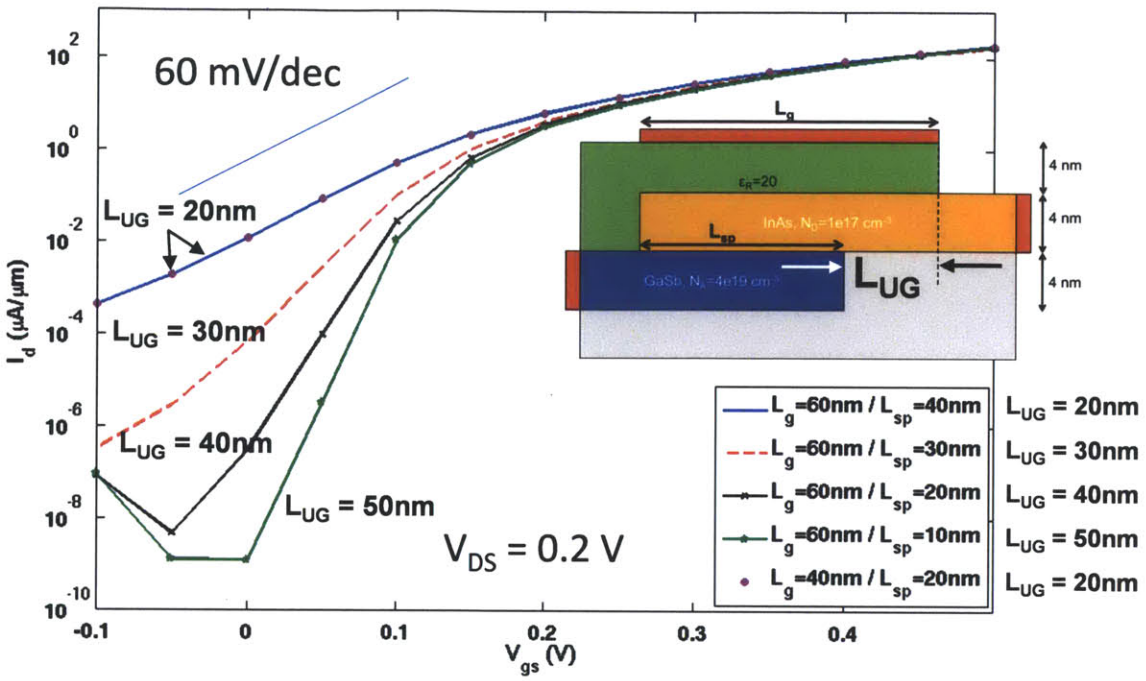


Fig 1.5.3 Non-Equilibrium Green's Function (NEGF) simulation result (courtesy of M. Luisier) on InAs/GaSb TFET with various gate lengths (L_G) and L_{UG}, suggesting that the OFF-current is dominated by L_{UG} rather than L_G.

1.6 Thesis Organization

This thesis investigates $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ vertical TFETs in detail, including fabrication technology, temperature dependent electrical measurement, as well as device modeling. In Chapter 2, the fabrication detail will be illustrated, the SEM images of the air-bridge structure and the TEM images of the fabricated device will be shown, which provide useful information on the further optimization of the device design and fabrication. Chapter 3 details the device measurement result with both room temperature and low temperature characteristics, and a physical model will be proposed for ON-state operation of the device. Low temperature measurement result is consistent with the proposed model, and suggests modification of the device structure for performance improvement. Also, diode-mode operation

of the TFETs are also demonstrated in the last part of Chapter 3. Finally, Chapter 4 summarizes this thesis and highlights some of the key results as well as the challenges in device optimization.

Chapter 2. $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ Vertical Tunnel-FET Fabrication Technology

This chapter introduces the epitaxial structure lattice matched to an InP substrate and the fabrication technology of the $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ vertical TFET, including the critical step of air-bridge fabrication and the overall process flow. The SEM images of the air-bridge test structure confirm the high selectivity between InGaAs and GaAsSb using ammonium hydroxide based solution etchant. The cross-sectional TEM (XTEM) images show the precise epitaxial and device structure, which reveal the growth defects and fabrication technology issues.

2.1 Fabrication of the Air-bridge Structure

As discussed in Chapter 1.5, the air-bridge structure is necessary to prevent possible parasitic tunneling path directly under the drain, and the undercut distance L_{UG} is critical to suppress the OFF-current. Hence, it is important to fabricate the air-bridge structure with highly selective wet etch. Also, due to the ultrathin InGaAs on GaAsSb, the dimension of the air-bridge cannot be arbitrary, in order to prevent damage of the InGaAs and maintain structural integrity. In this section, the fabrication technology of the air-bridge test structure and the results are demonstrated on the actual epitaxial substrate with various air-bridge dimensions.

The epitaxial structure for both the test structure and the actual devices is shown in Fig 2.1.1. The device layers are 15 nm n-$In_{0.53}Ga_{0.47}As$/p+-$GaAs_{0.5}Sb_{0.5}$, and the 30 nm n+-$In_{0.53}Ga_{0.47}As$ provides excellent Ohmic contact for the drain. The epitaxial wafers used in this work were obtained from IQE, Inc. The 500 nm InAlAs virtual substrate is necessary for eliminating the growth defects (mainly threading dislocations) that would otherwise originate at the beginning of the epitaxial growth. Fig 2.1.2 shows the TEM image of the threading

dislocations starting at the InAlAs/InP substrate interface and eliminated during the InAlAs growth.

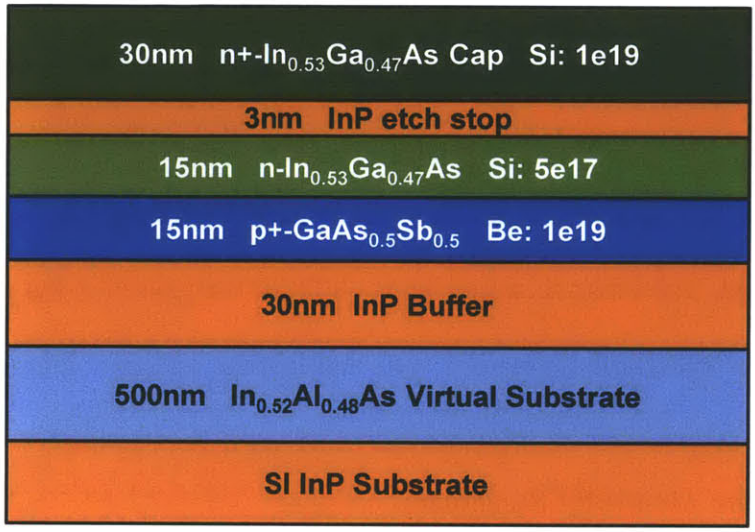


Fig 2.1.1 Epitaxial structure for the air-bridge test structures and actual devices. The device layers are 15 nm n-$In_{0.53}Ga_{0.47}As$/p+-$GaAs_{0.5}Sb_{0.5}$, and the 30 nm n+- $In_{0.53}Ga_{0.47}As$ provides excellent Ohmic contact for the drain.

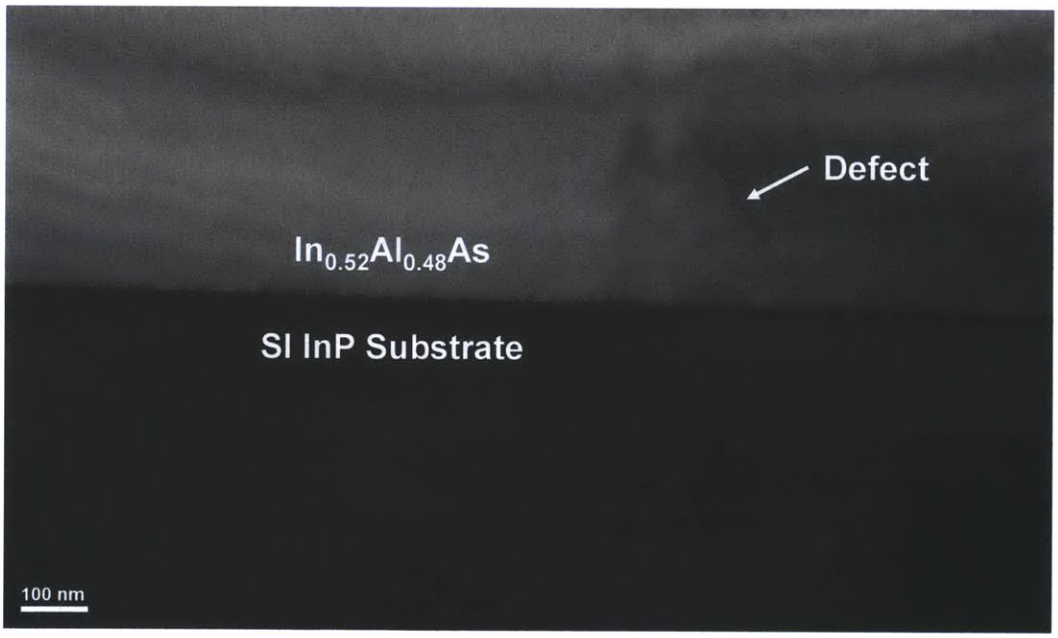


Fig 2.1.2 TEM image of the $In_{0.52}Al_{0.48}As$ virtual substrate on semi-insulating InP substrate. The 500 nm $In_{0.52}Al_{0.48}As$ can eliminate most of the growth defects originated at the $In_{0.52}Al_{0.48}As$/InP interface.

The air-bridge test structures were first fabricated on InAs/GaSb substrates, as schematically shown in Fig 2.1.3. The air-bridge patterns are defined with 4% hydrogen silsesquioxane (HSQ) negative tone e-beam resist using the Elionix ELS-125 125 kV e-beam lithography system. The dimensions of the air-bridge test structures are illustrated in Fig 2.1.3. The top-down view of the air-bridge test structures as developed are shown in Fig 2.1.4 with various dimensions, and subsequent BCl_3/Ar based ICP-RIE is carried out to transfer the pattern to the substrate. The gas flows for BCl_3 and Ar are 9 sccm and 2 sccm respectively. This ratio is important for obtaining a smooth etched surface since more Ar may result in a roughened surface while less Ar cannot remove the polymer formed by BCl_3 and results in micromasking. The bias power and ICP power need to be calibrated for anisotropic etch without roughening the etched surface (detailed calibration courtesy of Xin Zhao). Fig 2.1.5 shows the top-down view and 45 degree view of the etched air-bridge test structures, where the dimension of the air-bridge does not change much after dry etch and the etched area is clean and smooth after calibration. Finally, GaSb is selectively etched in 10:1 DI:NH_4OH [38], suspending InAs to form the air-bridge structure (Fig 2.1.5 (e)).

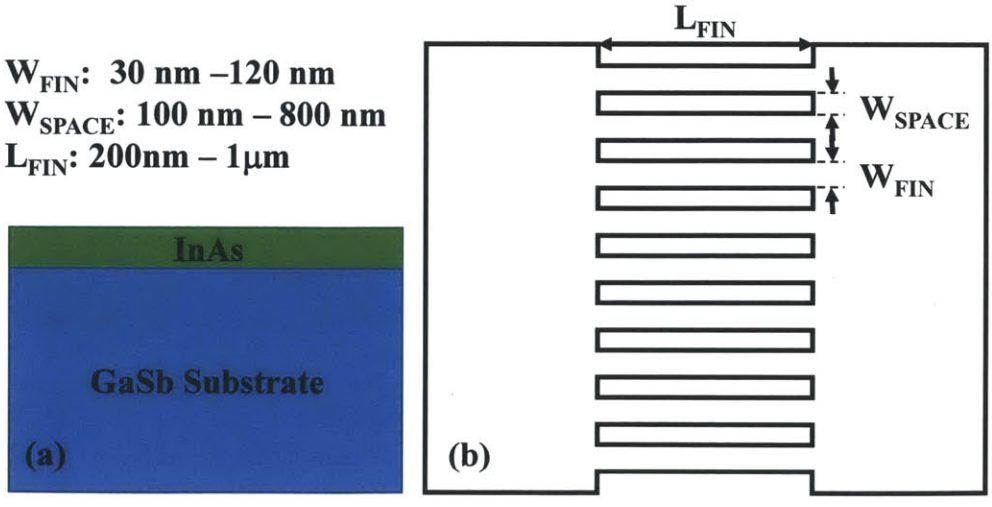
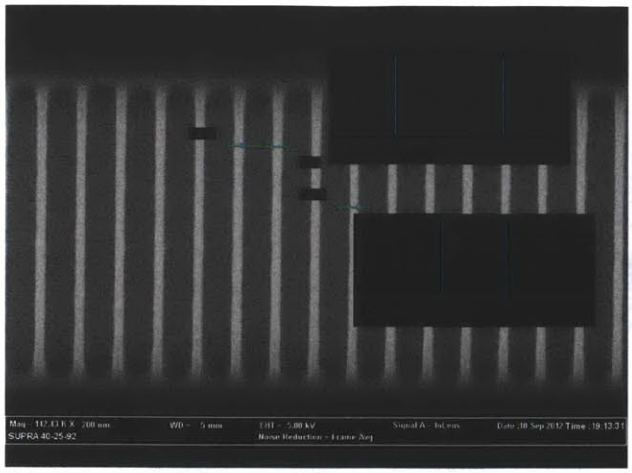
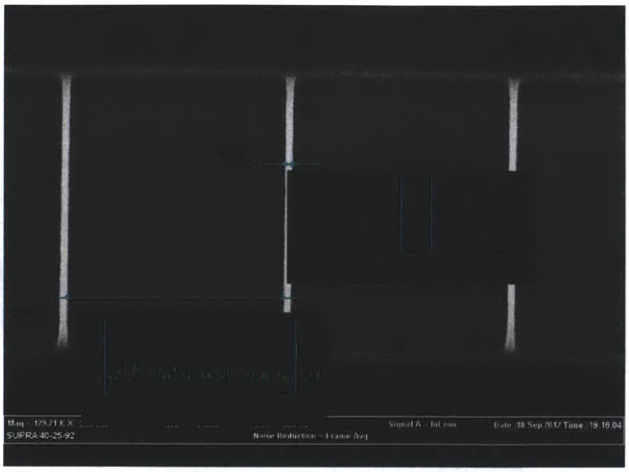


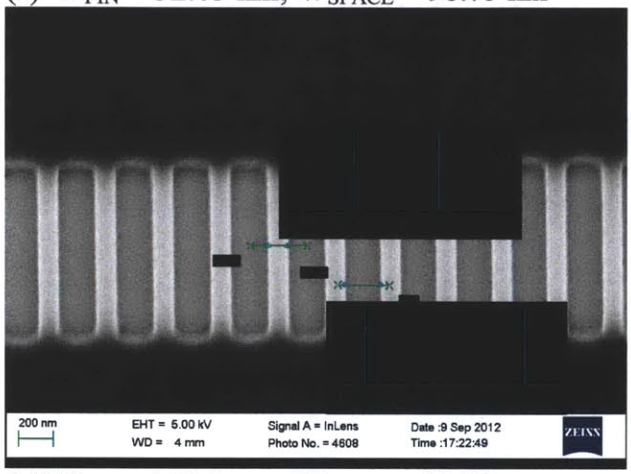
Fig 2.1.3 (a) Epitaxial structure of the InAs/GaSb substrate for air-bridge test structure fabrication. (b) The top-down schematic of the air-bridge test structure; various air-bridge dimensions are fabricated.



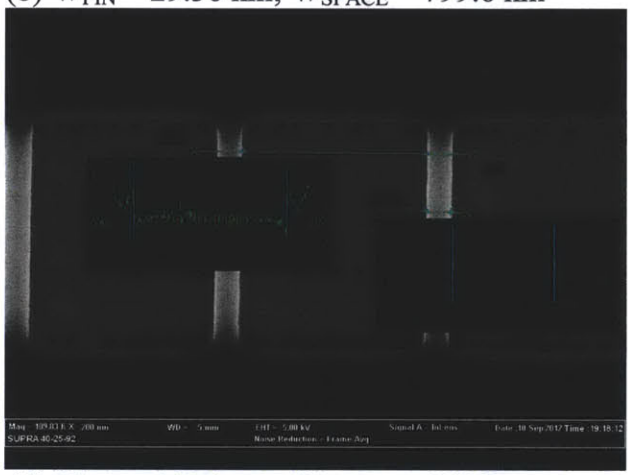
(a) W_{FIN} = 32.03 nm; W_{SPACE} = 98.75 nm



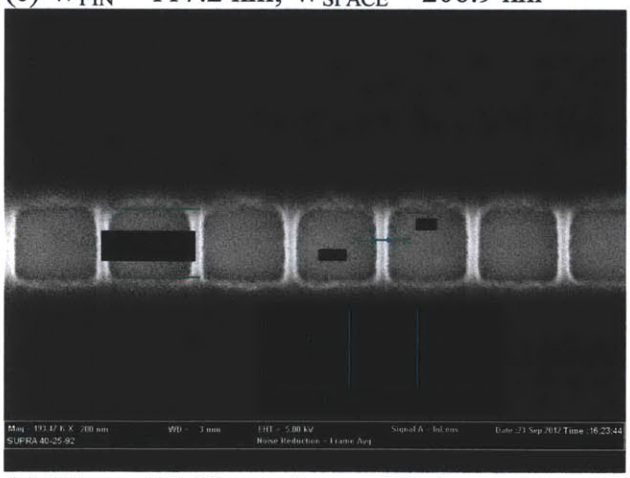
(b) W_{FIN} = 29.36 nm; W_{SPACE} = 799.6 nm



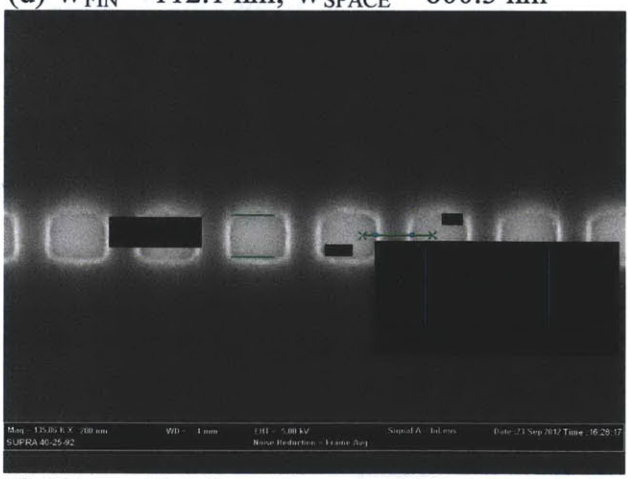
(c) W_{FIN} = 117.2 nm; W_{SPACE} = 206.9 nm



(d) W_{FIN} = 112.1 nm; W_{SPACE} = 800.3 nm



(e) W_{FIN} = 37.86 nm; L_{FIN} = 171.1 nm



(f) W_{FIN} = 131.5 nm; L_{FIN} = 148.8 nm

Fig 2.1.4 SEM micrographs of HSQ air-bridge structures as developed (a) W_{FIN} = 30 nm, W_{SPACE} = 100 nm, L_{FIN} = 1 μm; (b) W_{FIN} = 30 nm, W_{SPACE} = 800 nm, L_{FIN} = 1 μm; (c) W_{FIN} = 120 nm, W_{SPACE} = 200 nm, L_{FIN} = 1 μm; (d) W_{FIN} = 120 nm, W_{SPACE} = 800 nm, L_{FIN} = 1 μm; (e) W_{FIN} = 30 nm, W_{SPACE} = 200 nm, L_{FIN} = 200 nm; (f) W_{FIN} = 120 nm, W_{SPACE} = 200 nm, L_{FIN} = 200 nm. The measured dimensions are labeled under the images.

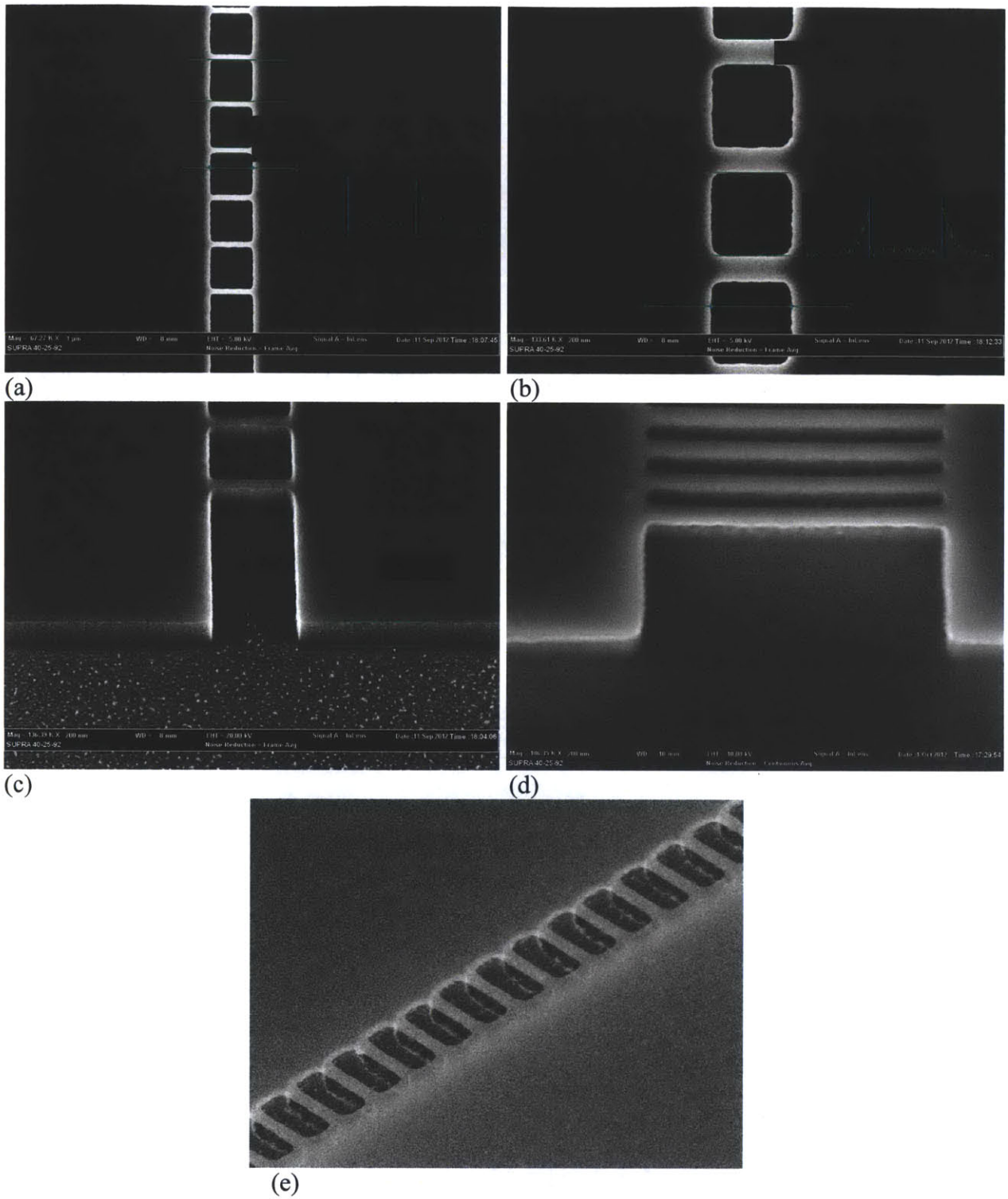


Fig 2.1.5 Top-view air-bridge structures as etched (a) W_{FIN} = 30 nm, W_{SPACE} = 400 nm, L_{FIN} = 400 nm; (b) W_{FIN} = 120 nm, W_{SPACE} = 400 nm, L_{FIN} = 400 nm. The dimensions are consistent with HSQ defined dimensions. 45° tilted view air-bridge structure as etched (c) un-optimized etch recipe; (d) optimized etch recipe. The micromasking is improved in the optimized etch recipe. (e) 45° tilted view of the air-bridge structure after undercut.

The air-bridge test structures are fabricated on the device substrate as illustrated previously. Different from the InAs/GaSb substrate, the actual device substrate has only a 15 nm-thick GaAsSb layer, which may make it difficult for the etchant to diffuse under the InGaAs layer; and NH_4OH is no longer an effective selective etchant for GaAsSb. Therefore, a two-step etching scheme is proposed for the device substrate with first, NH_4OH/H_2O_2 (1:100) solution and second, tri-methyl-ammonium-hydroxide (TMAH) solution (25% wt.). Due to the non-volatile $InCl_x$-containing residue from the ICP-RIE step, it is difficult to get a uniform undercut etch starting with TMAH. The NH_4OH/H_2O_2 solution can effectively remove the $InCl_x$-containing residue and is selective between InGaAs and GaAsSb. After the initial etching with NH_4OH/H_2O_2, TMAH provides higher selectivity for GaAsSb to accomplish the subsequent undercut process. Fig. 2.1.6 shows the air-bridge test structure fabricated on the device substrate with two-step undercut process.

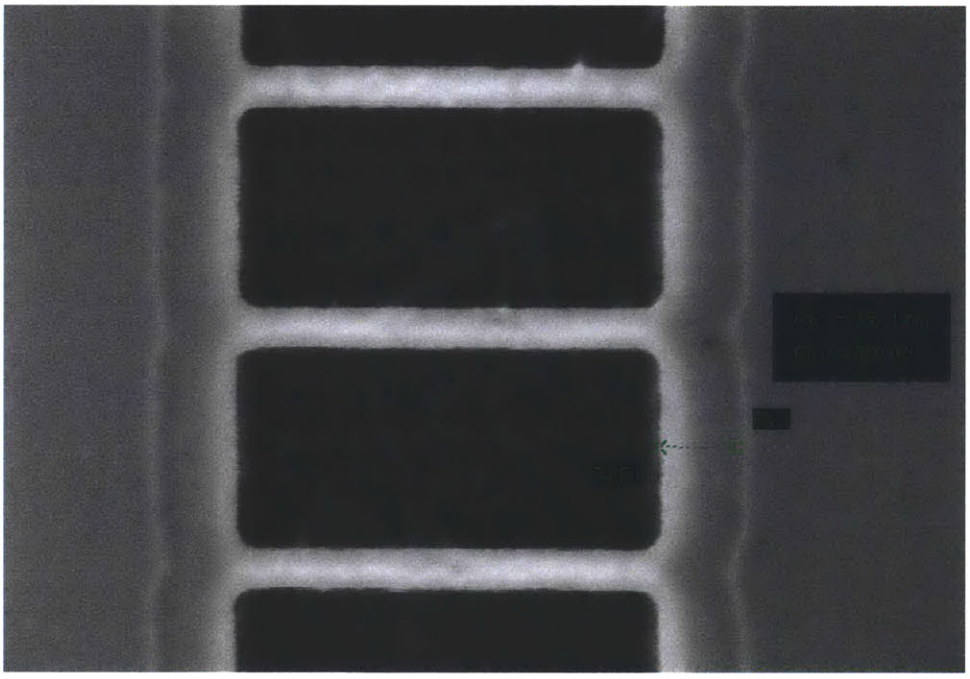


Fig 2.1.6 Top-view SEM image of the air-bridge test structure on the device substrate. Two-step undercut process is used to selectively etch the GaAsSb under InGaAs. The edge of the etched GaAsSb can be clearly seen from the image.

2.2 $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ Vertical Tunnel-FET Fabrication

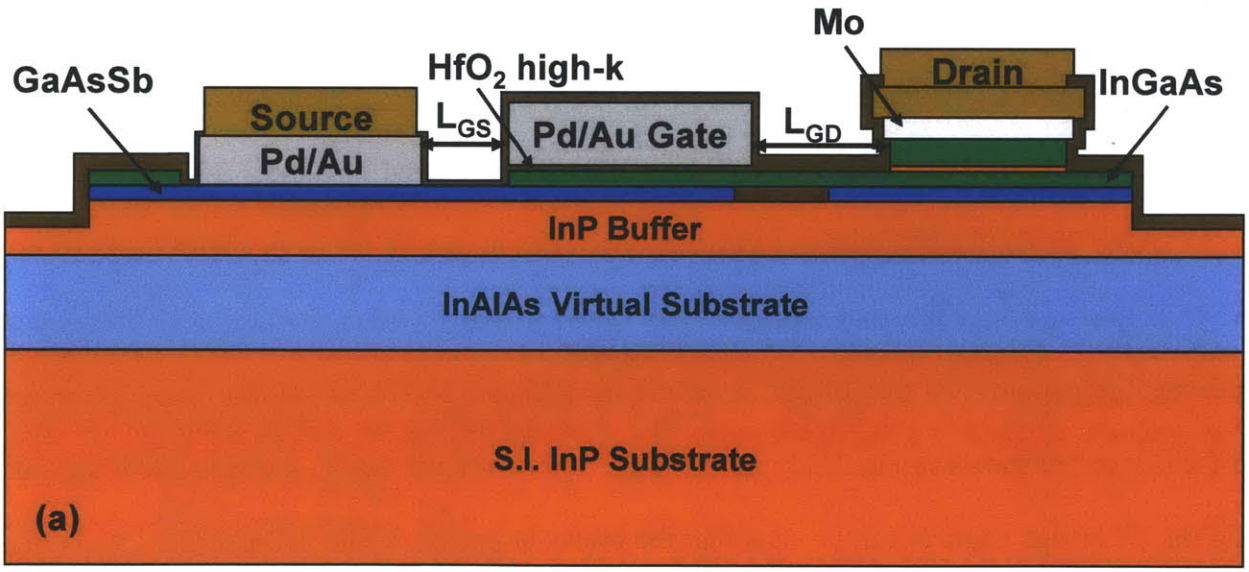
The fabrication of the $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ vertical T-FET is on the same substrate illustrated in the previous section, and a process flow is given in Fig 2.2.1. The cross-sectional and top-down view of the finished device structure is shown in Fig 2.2.2, and the detailed process flow of the fabricated is provided in the Appendix. Molybdenum is first sputtered on n+- $In_{0.53}Ga_{0.47}As$ as the drain contact, then the n+- $In_{0.53}Ga_{0.47}As$ cap is recessed with 1:10 H_2O_2:citric acid solution. 5 nm ALD HfO_2 gate dielectric is deposited and Pd/Au gate metal is formed by e-beam evaporation and liftoff. Air-bridge structure is then fabricated self-aligned to the gate, and passivated with ALD Al_2O_3. InGaAs is recessed self-aligned to the gate for isolation of the source contact. Finally, CVD inter-layer dielectric (ILD) is deposited, via holes are opened, metal contacts and pads are formed. The dimensions of the device include the gate length L_G, gate width W_G, gate-to-drain distance L_{GD}, gate-to-source distance L_{GS}, as defined in Fig 2.2.2; as well as the air-bridge dimensions W_{FIN}, L_{FIN} and W_{SPACE} defined in the previous section. The detailed dimensions of the fabricated devices are listed in Table 2.2.1.

After the device fabrication, cross-sectional TEM images of the device with L_G = 3.8 μm, W_G = 22 μm, L_{GS} = 0.8 μm, and L_{FIN} = 300 nm were performed by Evans Analytical Group, with specimen preparation via the lift-out technique using focused-ion-beam (FIB). Selected images of the device are shown in Fig 2.2.3, including the source contact region, the area under the gate, and the air-bridge edge. It can be seen that the epitaxial growth of the InGaAs/GaAsSb is high quality with only a few monolayers of intermixing, and the high-k dielectric is uniform across the gated area. The measured thickness of the HfO_2 is 5.3 nm, with EOT ~ 1.3 nm from dielectric constant calibration [39]. Also, the Pd/Au source contact has clearly diffused into the GaAsSb

layer, and even InP in some regions. Although it is designed as non-alloyed contact, CVD process with 300°C substrate temperature has driven Pd into the GaAsSb.

- **Mo drain contact**
- **Mesa etch**
- **Gate Recess & Passivation**
- **ALD HfO_2 deposition**
- **Gate metal formation**
- **Air-bridge formation**
- **Al_2O_3 Passivation**
- **Source exposure and source metal deposition**
- **Inter-layer dielectric**
- **Via open and metal**
- **Probe pad**

Fig 2.2.1 Process flow of the $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ vertical TFET.



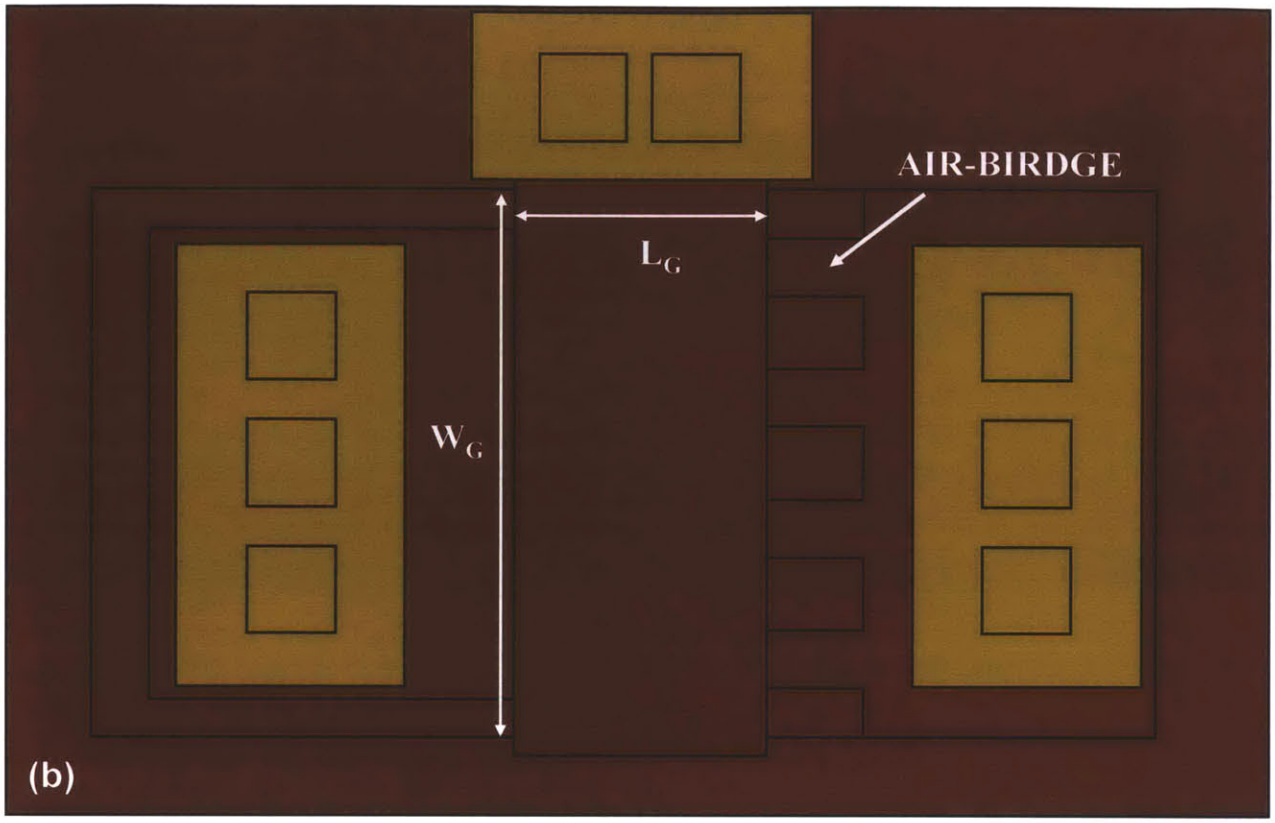


Fig 2.2.2 Cross-sectional and top-down schematic view of a finished device. The dimensions of the device are labeled.

Geometric Parameter	Symbol	Value
Gate Length	L_G	500nm – 3.8μm
Gate Width	W_G	14μm, 22μm
Gate to Source Distance	L_{GS}	500nm – 1.1μm
Gate to Drain Distance	L_{GD}	1.3μm, 1.6μm
Air-bridge Length	L_{FIN}	300nm, 600nm
Air-bridge Width	W_{FIN}	150nm
Air-bridge Spacing	W_{SPACE}	200nm

Table 2.2.1 Geometric parameters of the device

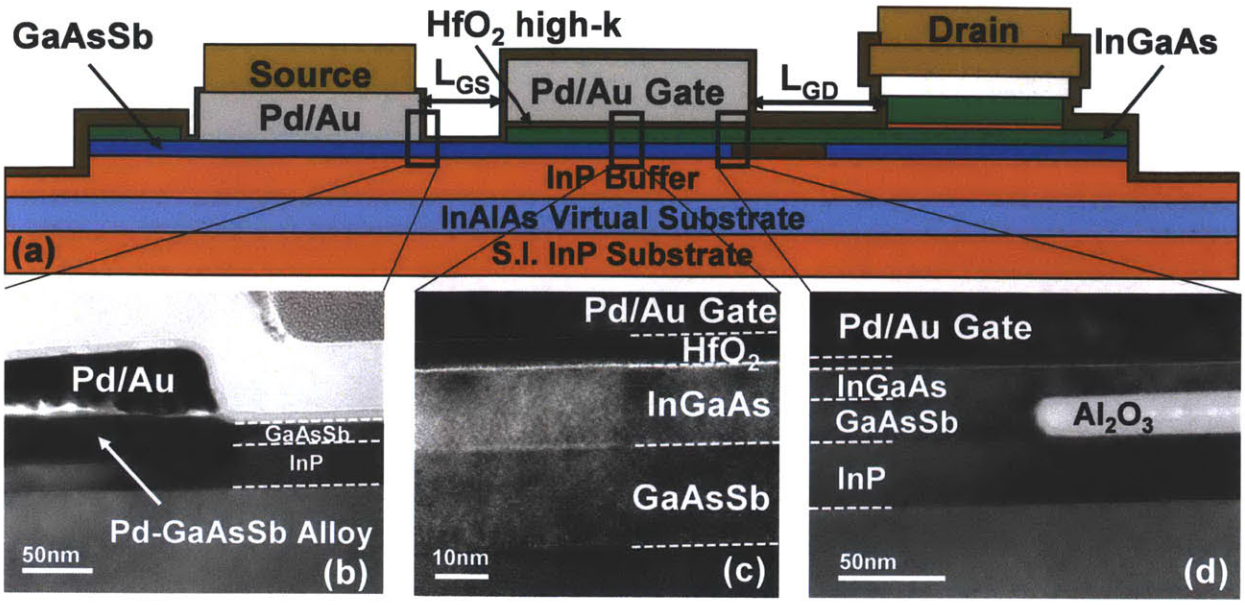


Fig 2.2.3 Cross-sectional TEM images of the device with L_G = 3.8 μm, W_G = 22 μm, L_{GS} = 0.8 μm, and L_{FIN} = 300 nm: (a) simplified cross-sectional schematic view; (b) XTEM image at source contact region. Pd has diffused through the 15 nm GaAsSb layer. (c) HR-XTEM image under the gate. High epitaxial quality and uniform ALD layer are shown. (d) XTEM image at the edge of the air-bridge. Highly selective undercut is achieved using two-step process.

Chapter 3. $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ Vertical Tunnel-FET Device Analysis

This chapter contains the analysis of the electrical performance of the $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ vertical TFETs. Room temperature characterization shows the overall performance of the fabricated device, while the temperature dependent measurement results reveal the underlying physics. A physical model of TFET operation in the ON-state is then proposed based on temperature dependent measurements, and the simulation result give some guidelines for TFET structure improvement. Moreover, the diode-mode operation is demonstrated, which is an indicator of the potential of vertical TFETs in hybrid IC applications.

3.1 Room Temperature Performance

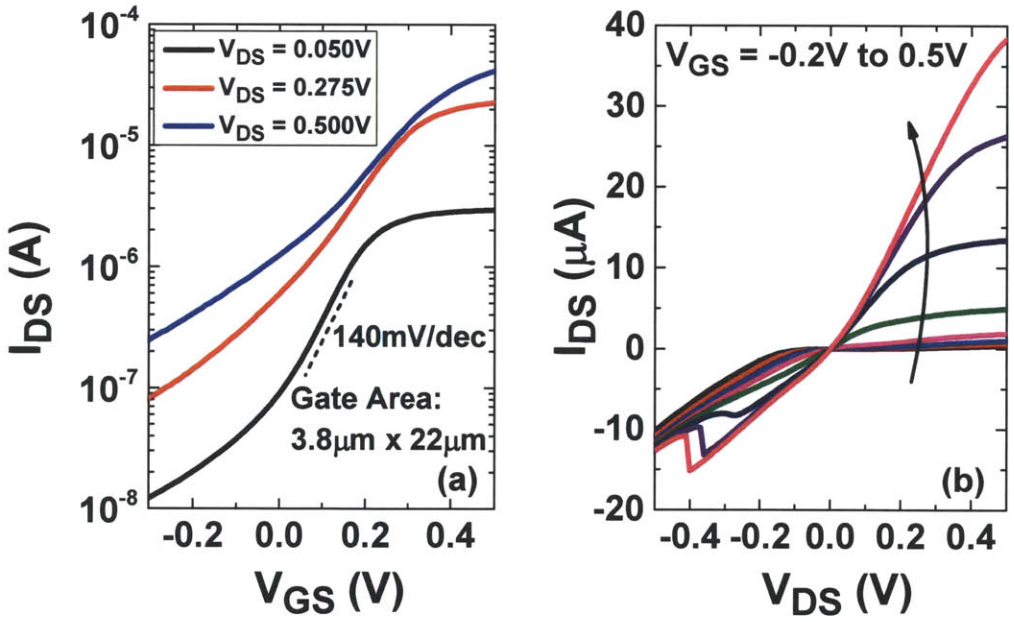


Fig 3.1.1 (a) Transfer and (b) output characteristics of the fabricated TFET with gate dimension of 3.8 × 22 μm^2. NDR can be clearly seen in the forward bias region in (b), indicating the tunneling nature of the device operation.

The transfer and output characteristics of the TFET with gate dimension of 3.8 × 22 μm^2 are plotted in Fig 3.1.1. The minimum (point) sub-threshold swing (SS_{min}) at low V_{DS} is 140 mV/dec. and the effective SS (SS_{eff}) is 220 mV/dec. (I_{DS} from 20 nA to 2 μA). The drive currents

achieved at V_{DS} = 50 mV and V_{DS} = 0.5 V are 2.93 μA and 41.4 μA respectively. It is seen that the I_{DS}-V_{GS} curve starts flatten out when $V_{GS} < 0$, which is mainly due to the leakage current in OFF state. Consequently, although SS could start dropping at lower current region, it is completely overwhelmed by the leakage current. On the other hand, the output characteristics show good saturation for positive V_{DS}, which is desirable in applications that require large output resistance (e.g., amplifier). Also, the V_{GS} dependent negative-differential-resistance (NDR) is clearly seen in the negative V_{DS} region. This is a solid evidence of the tunneling nature of the device operation, where the tunneling turns off with larger negative V_{DS} as the drain bias pulls up the band in the InGaAs layer (Fig 3.1.2).

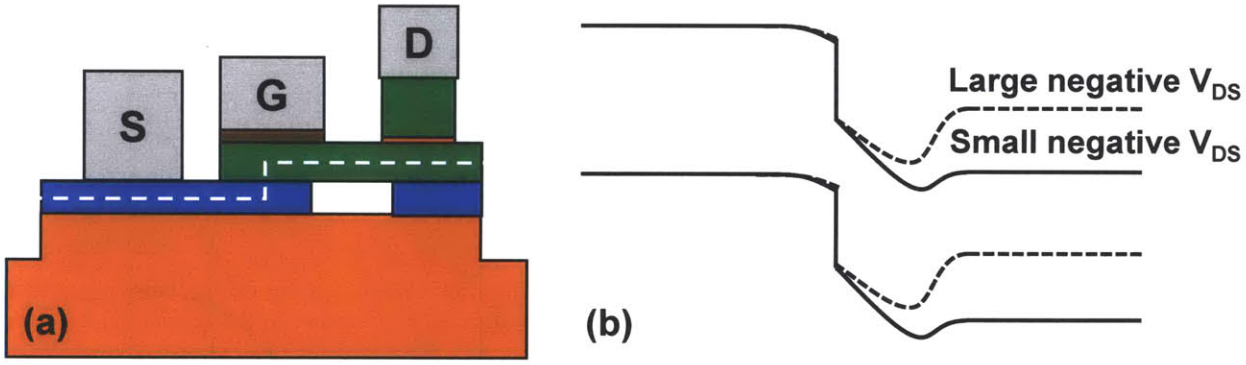


Fig 3.1.2 Band diagram (b) along the dashed line in (a). The tunneling junction is turned off when large V_{DS} is applied as the band is pulled up and the conduction band of InGaAs does not overlap with the valence band of GaAsSb.

3.2 Extraction of Basic Parameters from Devices and Test Structures

The capacitance-voltage (CV) characteristics of on-chip MOSFET-like test structures (inset of Fig 3.1.3) are shown in Fig 3.1.3. In order to eliminate the parasitic capacitance, two-FET method with L_{g1} = 16.8 μm and L_{g2} = 10.4 μm is adopted. Two test structures with exactly same parasitic capacitance (identical geometric parameters except for gate length) are measured, so that the difference in the gate area accounts for the difference in capacitance. A capacitance

equivalent thickness of ~2 nm is obtained at V_G - V_{FB} = 0.5 V and minimum D_{it} of 2 × 10^{12} $cm^{-2}eV^{-1}$ is extracted near the mid-gap (V_{GS} ~ 0.2 V) using the high-low method [40]. The extracted CET is larger than the expected EOT in Chapter 2, which is mainly due to the strong quantization in the ultrathin InGaAs pushing the carriers away from the surface [2]. On the other hand, the frequency dispersion at high V_{GS} is mainly due to D_{it} near and in the InGaAs conduction band. This is where the Fermi level spans in the sub-threshold regime, resulting in relatively large SS, which can be improved by reducing D_{it} via further optimization of the gate stack.

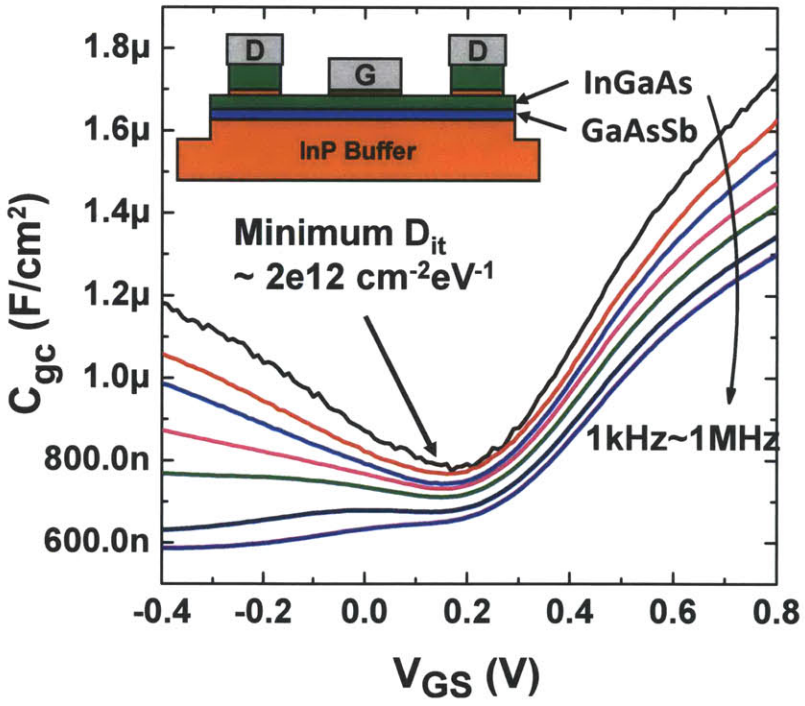


Fig 3.2.1 Multifrequency split-CV characteristics of the MOSFET-like test structure (inset). Two-FET method with L_{g1} = 16.8 µm and L_{g2} = 10.4 µm is applied. A minimum mid-gap D_{it} of 2 × 10^{12} $cm^{-2}eV^{-1}$ is extracted using the high-low method. The frequency dispersion at high V_{GS} is mainly due to high D_{it} near and in the conduction band, resulting in relatively large SS.

As seen from Chapter 2.2, Pd has spiked through GaAsSb during the CVD SiO_2 process and voids are formed during the diffusion. This may result in large contact resistance and affect

the device performance. Also, it is well known that the hole mobility in GaAsSb is relatively low (typically < 100 $cm^2 \cdot V^{-1} \cdot s^{-1}$), which could induce large series resistance. Therefore, it is important to extract the contact resistance of Pd/Au on GaAsSb and the sheet resistance of GaAsSb to estimate the impact of the parasitic resistance on the device. Using the transmission-line-model (TLM) test structure [40], the contact resistance and the sheet resistance of GaAsSb are extracted to be 4.6×10^{-4} $\Omega \cdot cm^2$ and 5.8×10^3 $\Omega/\square$ respectively. With the dimension of the contact and L_{GS}, the series resistance on the source side can be estimated as:

$$R_S^S = \frac{R_C^S}{A_C^S} + R_S^S \cdot N_\square^S \approx 532\ \Omega$$

On the drain side, the contact resistance is below 10^{-5} $\Omega \cdot cm^2$ [41] and the sheet resistance of n-type InGaAs with 5×10^{17} cm^{-3} doping concentration can be estimated as 4.2×10^3 $\Omega/\square$. So that with the dimension of the contact and air-bridge, the series resistance on the drain side is estimated as:

$$R_S^D = \frac{R_C^D}{A_C^D} + R_S^D \cdot N_\square^D \approx 397\ \Omega$$

So that the estimated series resistance of the device is

$$R_S^{total} = R_S^S + R_S^D \approx 930\ \Omega$$

Fortunately, from Fig 3.1.1 (b), the total resistance in ON-state is extracted as 1.75×10^4 Ω, which is much larger than the estimated series resistance. From another perspective, the total resistance of the device in ON state consists of R_S^{total} and R_C ("tunneling resistance" or channel resistance). Since R_C should be proportional to the tunneling area, and $R_{total} = R_S^{total} + R_C$ is also proportional to tunneling area (as will be discussed in Section 3.3), R_S^{total} is negligible compared with R_C. In other words, the InGaAs/GaAsSb tunneling junction resistance still dominates the

total resistance of the device in ON-state, which can be reduced by using the heterostructure with smaller $E_{g\text{-}eff}$.

3.3 Areal Tunneling Behavior

As discussed in Chapter 1, vertical TFETs with enhanced gate modulation are attractive due to their uniform gate modulation in the gated area. Therefore, the drive current of the device should be proportional to the gate area, which is predicted by the TCAD simulation study in [35]. Fig 3.3.1 (a) plots the I_{DS}-V_{GS} curves at V_{DS} = 0.275 V for four different device sizes normalized to the gate area, showing appropriate scaling behavior with gate area. I_{DS} is also plotted at V_{GS}= 0.5 V over a wide range of gate areas in Fig 3.3.1 (b) to confirm the areal tunneling behavior. However, the drive current does not scale appropriately with gate area for the devices with small gate length (e.g. L_G = 0.5 μm). This is mainly because the drain side corner is a preferential tunneling point, as illustrated in Fig 3.3.2. So that the corner tunneling current is dominant for the devices with small gate area.

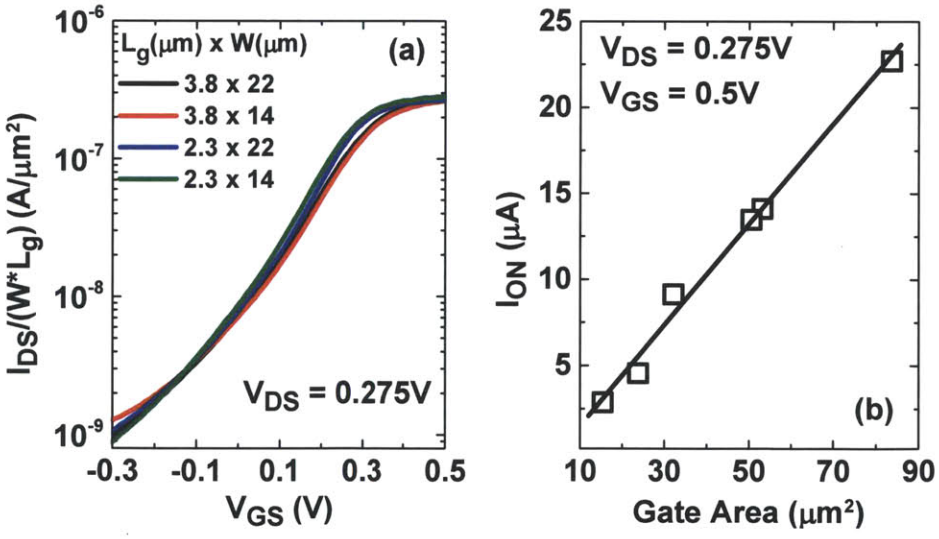


Fig 3.3.1 (a) I_{DS}-V_{GS} curves at V_{DS} = 0.275 V for four devices with different gate dimensions normalized to the gate area; (b) Drive current at V_{GS} = 0.5 V versus gate area indicates areal tunneling current in the vertical TFET.

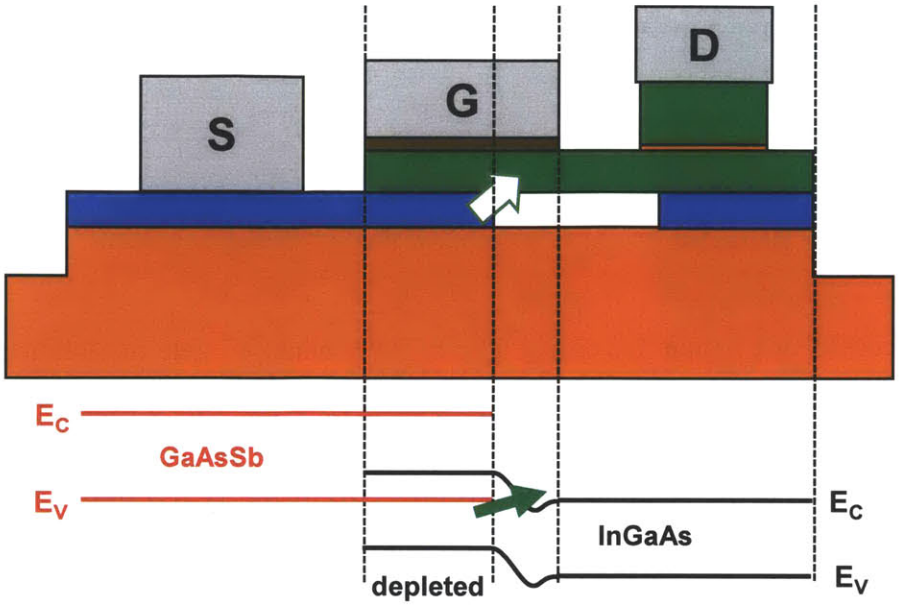


Fig 3.3.2 The drain side corner of the device is a preferential tunneling point. The band diagram of the channel region shows the elevated bands in the depletion region, making the corner turn on first.

3.4 Temperature Dependent Study and Device Optimization

In order to have deeper understanding of the physics and limitations of the device structure, a temperature dependent study was carried out from 300 K down to 150 K. Since band-to-band tunneling efficiency does not have temperature dependence, it is easy to separate the thermal injection limited current and tunneling limited current by varying the temperature. Fig 3.4.1 shows the I_{DS}-V_{GS} curves from 150 to 300 K at V_{DS} = 0.05 V. It is clearly seen that the OFF current is one of the major factors limiting the SS. When the temperature decreases to 150 K, the region with lower point SS is revealed. This high OFF-current floor may originate from the leakage through the 30 nm-thick InP buffer layer. Especially as the Pd/Au source contact spiked through the 15 nm GaAsSb, the carriers are easily injected into the InP buffer layer and can be extracted from the drain. One way to eliminate this parasitic current path is to undercut the InP

layer under the drain, which is similar in the method of isolating source and drain with the air-bridge structure.

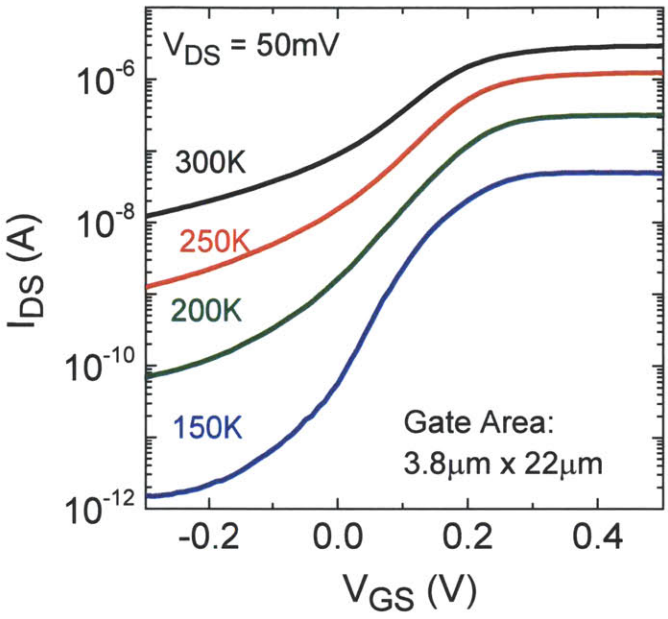


Fig 3.4.1 I_{DS}-V_{GS} curves of the TFET from 150 to 300 K at low V_{DS}. The OFF state leakage current is dramatically decreased at 150 K .

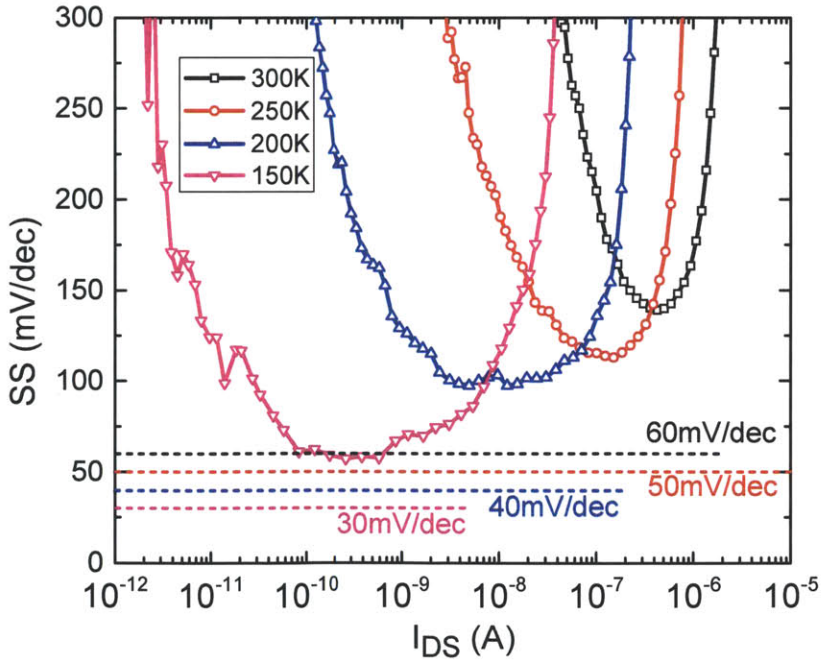


Fig 3.4.2 Subthreshold swing (*SS*) versus drive current from 150 to 300 K. *SS* ~ 60 mV/dec over more than one order of magnitude in I_{DS}, and SS_{eff}= 80 mV/dec is achieved at 150 K.

The SS versus I_{DS} is plotted in Fig 3.4.2 at various temperatures, showing a significantly improved SS_{min} = 58 mV/dec and SS_{eff} = 80 mV/dec. (I_{DS} from 10 pA to 10 nA) at 150 K, due to the suppressed leakage. The SS-I_{DS} curve at 150 K exhibits two segments which converge at 1nA. This is typical TFET behavior where the segment at lower current level is modulated by the tunneling barrier and the segment at higher current is modulated by the available states for tunneling [25].

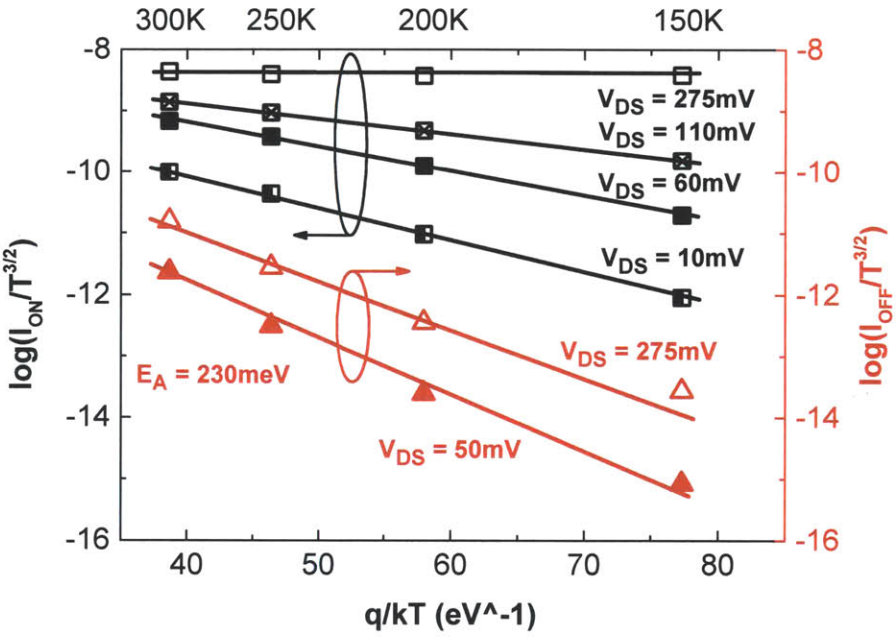


Fig 3.4.3 ON-current (V_{GS} = 0.5 V) and OFF-current (V_{GS} = -0.3 V) at various V_{DS} versus inverse thermal energy. The linear relation in semi-log scale implies an energy barrier in the current path, and the slopes are related to the barrier height.

It can be observed from Fig 3.4.1 that the ON current of the device degrades as the temperature decreases. There are two probable reasons: increase of tunneling barrier and decreased thermionic emission over a barrier in the current path. In order to analyze the underlying physics, the ON currents at V_{GS} = 0.5 V of the device with different drain biases are extracted, and the Arrhenius plot ($\ln(I_{ON}/T^{3/2})$ vs. 1/kT) is shown in Fig 3.4.3, where $T^{3/2}$ accounts for the bandgap widening at lower temperature. It is seen from the plot that the ON

current shows thermal behavior at lower drain biases as $\ln(I_{ON}/T^{3/2})$ is linear versus 1/kT. This linear behavior implies that there exists a barrier in the current path, with the slopes related to the barrier height.

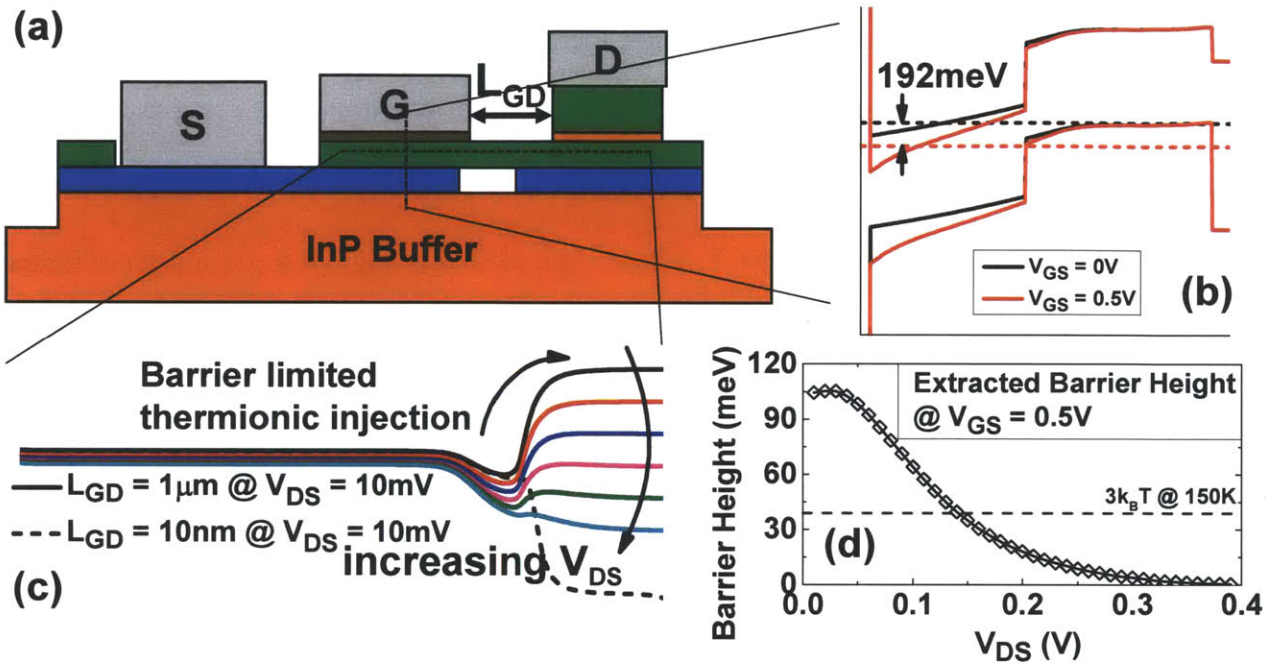


Fig 3.4.4 A physical model for the InGaAs/GaAsSb vertical TFET in the ON-state. (a) A simplified schematic view; (b) Simulated band diagram along the tunneling direction. Application of V_{GS} = 0.5 V changes the InGaAs first subband energy by 192 meV (neglecting D_{it}); (c) InGaAs conduction band diagram parallel to the gate simulated at V_{GS} = 0.5 V with varying V_{DS}. The barrier from the channel to the ungated InGaAs region dominates the drive current at low V_{DS}. (d) Extracted channel-drain barrier height, from the activation energies as in Fig. 3.4.3.

Based on the above observation, self-consistent Poisson-Schrodinger calculation of the band diagram (courtesy of James Teherani using nextnano3 [42]) and TCAD simulations [43] are performed to investigate and model the barrier in the current path. Fig 3.4.4 shows the simulation results, modeling and characterization of this barrier located in the drain side ungated region. The band diagram normal to the gate plotted in Fig 3.4.4 (b) is calculated self-consistently under quasi-equilibrium assumption. It can be seen that the gate introduces

approximately 192 meV modulation to the first subband of InGaAs, where the majority of electrons populate. In fact, due to the presence of severe D_{it}, the actual modulation is smaller than 192 meV. Fig 3.4.4 (c) shows the band diagram parallel to the gate simulated with TCAD tool. The device dimension used in the simulation is extracted from the cross-sectional TEM images. It can be seen that with small V_{DS} bias, there forms a barrier in the ungated region near the drain, which electrons must overcome to reach the drain. When the drain bias increases, the barrier diminishes and finally disappears. The barrier heights at V_{GS} = 0.5 V associated with the slope in the Arrhenius plot at different V_{DS} biases are plotted in Fig 3.4.4 (d) and the reference line of $3k_BT$ at 150 K is marked as well. So that when V_{DS} > 0.14 V, the barrier height the electrons encounter is smaller than $3k_BT$. The output characteristics of the device at 150 K are plotted in Fig 3.4.5, where the curves corresponding to V_{GS} = 0.4 V and V_{GS} = 0.5 V start to separate at V_{DS} = 0.14 V (circled point). By assuming that the limiting factor for the drive current is the tunneling when the barrier height is smaller than $3k_BT$, the output characteristics are consistent with the extracted barrier height in Fig 3.4.4(d). The fundamental problem in the device structure is that the ungated drain extension region is lightly doped, so that there are not enough carriers to raise the Fermi level and hence a barrier forms in this region. This is similar to the MOSFET structure with long lightly doped drain (LDD) region, when the electrons start to accumulate in the channel and cannot easily reach the heavily doped drain. In order to eliminate this barrier, the lightly doped region must be shortened. The simulation result with L_{GD} = 10 nm is shown in Fig 3.4.4 (c), where the conduction band is effectively lowered by populating excessive electrons in the lightly doped region, and the barrier is eliminated. However, due to the design of the air-bridge structure, it is unrealistic to scale L_{GD} to such a small value. So that the improved device structure would be more similar to the structure in [36], which undercuts of the

GaAsSb under the entire drain region. Additionally, as mentioned previously, it is important to isolate the drain from the InP buffer layer, and this structure can achieve this goal inherently as well.

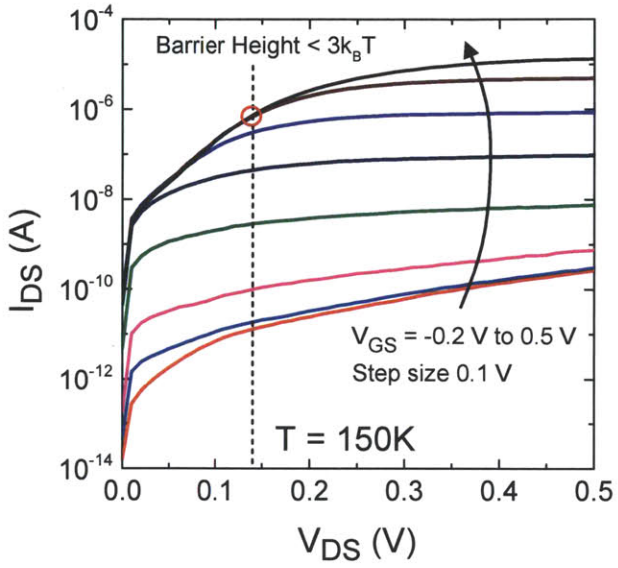


Fig 3.4.5 Measured I_{DS}-V_{DS} curves for different V_{GS} at 150 K. Output curves corresponds to V_{GS} = 0.4 V and V_{GS} = 0.5 V start to separate at V_{DS} = 0.14 V, where the barrier height becomes smaller than $3k_BT$.

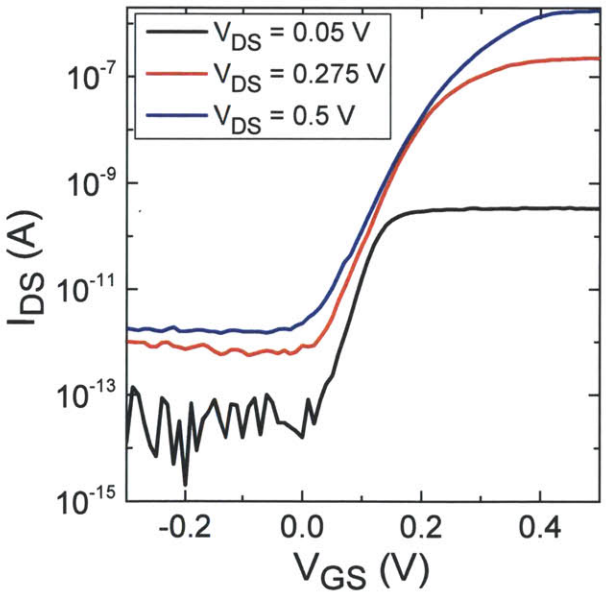


Fig 3.4.6 I_{DS}-V_{GS} curves for different V_{DS} at 77 K. The ON currents are further suppressed by the existence of the barrier, but the value is much larger than extrapolated from the Arrhenius plot. This may be due to the parasitic tunneling path that is not limited by this barrier.

In a separate set of measurements, the devices were also cooled to 77K. According to the model, we are expecting a severely limited current when V_{DS} is small. Indeed, as seen from the transfer characteristics at 77 K in Fig 3.4.6, the ON current at V_{DS} = 50 mV has further decreased. However, from the Arrhenius plot we can extrapolate approximately 2.52×10^{-11} A ON current at V_{DS} = 50 mV, which is about only 1/10 of the measured current. This may be mainly due to the parasitic tunneling path that is not limited by the barrier (e.g. the preferential corner tunneling current). So that when the major tunneling current is extremely limited, the parasitic current becomes dominant.

3.5 Diode-mode Operation

Aside from the FET operation as discussed in previous sections, the InGaAs/GaAsSb vertical TFETs can also be operated as a backward/Esaki diode with different bias conditions. From the device structure of the vertical TFET, it is inherently a PN junction, which can rectify the current going from drain to source. In this sense, by applying a fixed offset voltage between the drain and the gate, when the signal is applied to the drain, the signal also goes to the gate, which modulates the bands of InGaAs in the channel. In this way, the device operates like a diode, which is called the diode-mode operation of a TFET for the rest of this thesis.

One of the important figures of merit (FoMs) of a backward diode is the curvature coefficient [44], γ, where $\gamma = (dI^2/dV^2)/(dI/dV)$. The optimum value for γ should be as large as possible. It reflects the small signal rectifying capability of the device and thus the current and voltage sensitivity [44]. Although large value of γ can be obtained by biasing the diode, the real applications of the diodes as microwave detectors require zero-bias to avoid the noise from the DC bias. Therefore, it is important to have the right design to achieve desirable γ. From the

previous study on the Sb-heterostructure backward diodes [45], the optimal γ is achieved when NDR starts to become evident in the forward bias region, which indicates the tunneling action near the origin. On the other hand, for TFET, it is easy to tune the device to show the sign of NDR by applying gate bias. Different from biasing the diode, the input signal is separated from the noise of the DC bias, which is much easier to isolate and filter. Fig 3.5.1 demonstrates the diode-mode measurements performed with fixed V_{GD} bias, which shows exceptional tunable backward diode behavior with varied V_{GD}. The optimal γ measured at zero-bias is as high as 30 V^{-1} with appropriate V_{GD}. The gate voltage enables tuning of the band alignment at the tunnel junction, and the vertical TFET structure enables better gate control over the entire junction. This demonstration exhibits the potential of the vertical TFET for future hybrid integrated circuit applications.

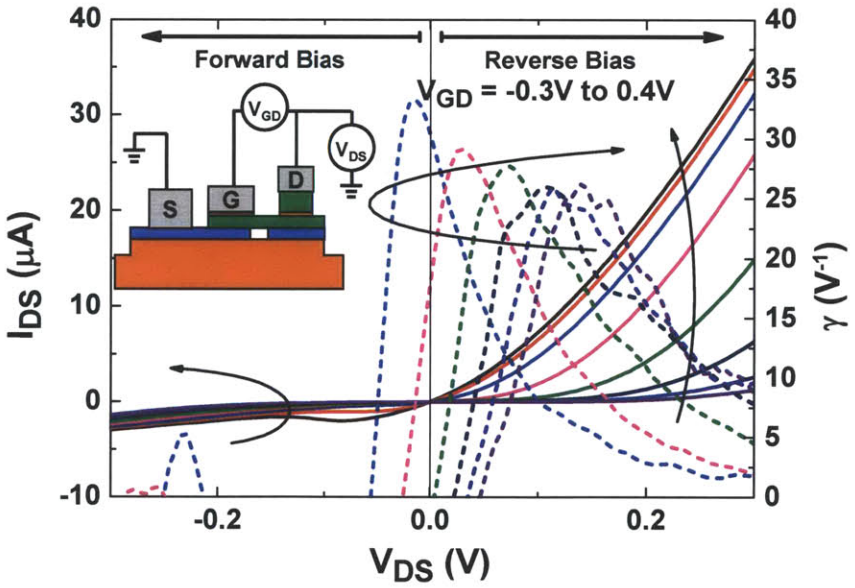


Fig 3.5.1 I_{DS}-V_{DS} characteristics of the device under fixed V_{GD} bias demonstrate backward diode behavior with tunable curvature coefficient (γ) at different V_{GD}. An excellent peak γ of 30 V^{-1} is achieved, suggesting the potential of the vertical TFET as a microwave detector in future hybrid integrated circuit applications.

Chapter 4. Conclusions and Future Work

This work demonstrates the design, fabrication and electrical characterization of the $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ vertical Tunnel-FET. The design of the air-bridge structure eliminates some of the parasitic tunneling paths in the device, and it is successfully fabricated with two-step undercut process. The device I-V characteristics show NDR in the output curves, which is the evidence of tunneling behavior in device operation. A minimum point SS of 140 mV/dec and effective SS of 220 mV/dec are obtained in this device. On-chip C-V measurement and temperature dependent study indicate that the severe D_{it} in the conduction band of InGaAs and the leakage current through the InP buffer layer have the major impact on the SS. Also, the temperature dependent study reveals a barrier at the drain side of the ungated region, which significantly impacts the drive current, and a revised design with L_{GD} = 10 nm is suggested to eliminate the barrier. Finally, the diode-mode operation of the TFET is proposed and demonstrated. The inherent PN junction in the TFET allows the device to operate as a tunable backward diode, where the gate bias can tune the band alignment at the junction at zero-bias and give optimum γ value. This demonstration indicates the versatility of the vertical TFET in IC applications and point out another direction for the development of TFETs.

Contributions of this work are:

- Designed and fabricated the $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ vertical Tunnel-FET with air-bridge structure.
- Demonstrated appropriate areal scaling property in this kind of TFET structure.
- Temperature dependent study and simulated device band diagrams are performed and a model associated with the results is proposed (partially courtesy of James Teherani).

- Demonstrated diode-mode operation, exceptional curvature coefficient is achieved with appropriate gate bias.

As analyzed in the fabricated device, the optimization of the device structure and material combination are important for the performance improvement. Also, a deep investigation on the diode-mode operation of the TFETs can give better insights on the device physics and the application of TFETs. Therefore, future work will be directed in optimizing the device structure to eliminate the substrate leakage and the barrier in the ungated region, and improve D_{it} to achieve better electrostatic control from the gate. The proposed device structure is shown in Fig 4.1, where the drain of the device is completely suspended from the substrate. Then, more sophisticated measurement and test structures will be designed to study the diode-mode operation of the TFETs. A proposed measurement scheme for the TFETs as a microwave detector is illustrated in Fig 4.2 [44].

Summary of suggested future work includes:

- Development of a different alloyed contact for GaAsSb.
- Development of a new gate dielectric technology to minimize D_{it}
- Fabrication of the TFET structure as shown in Fig 4.1
- Optimization of heterostructure, doping and device dimensions for improved performance
- RF measurements on the TFETs as microwave detector, study the underlying device physics

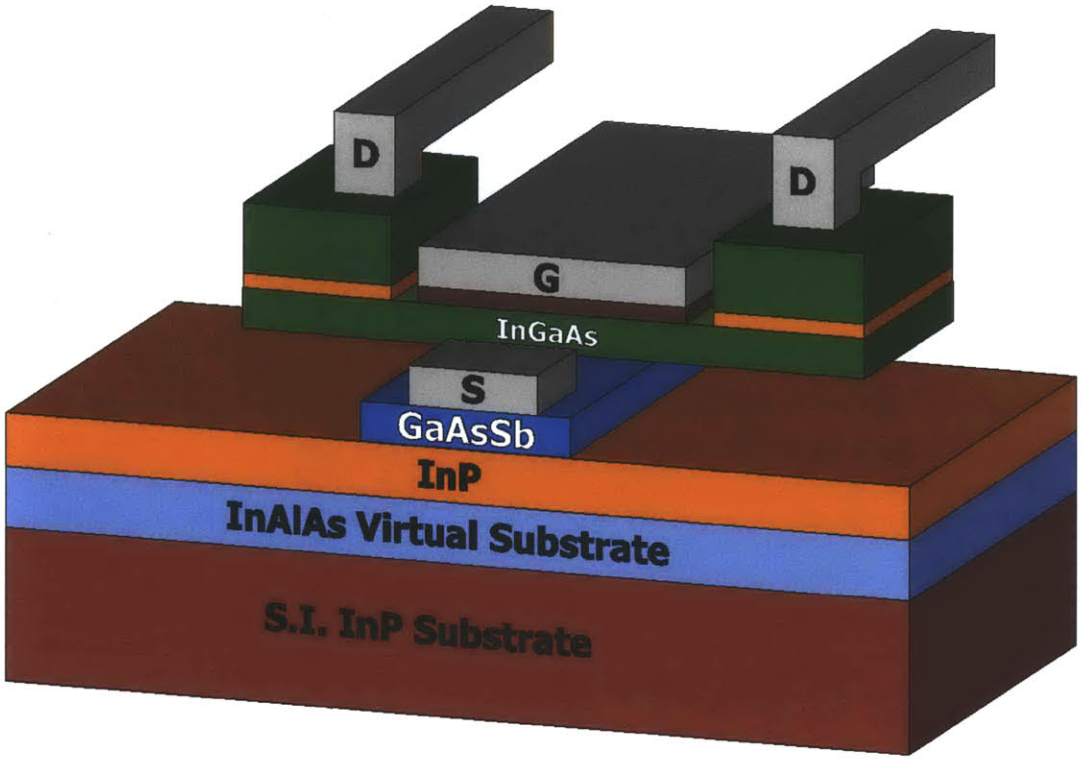


Fig 4.1 Improved TFET structure with completely suspended drain and self-aligned gate. The substrate leakage and the barrier at the drain side ungated region can be eliminated.

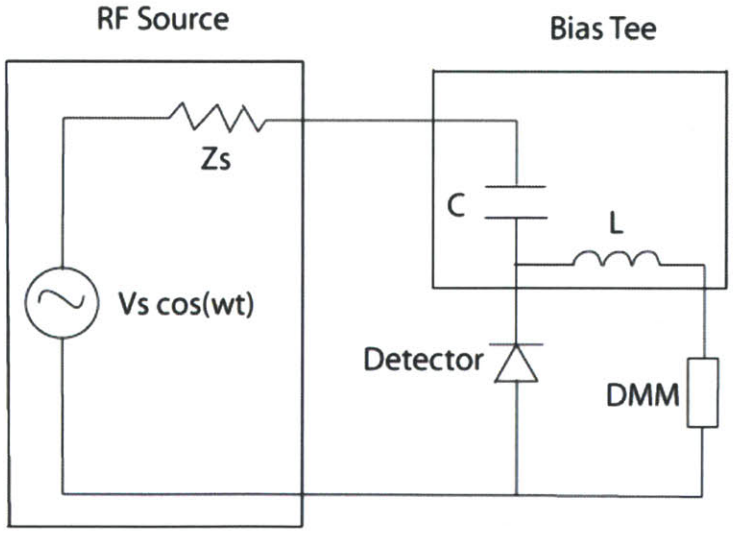


Fig 4.2 Schematic view of the RF measurement setup for microwave detector sensitivity measurement [44].

Appendix. Process Flow for $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ Vertical Tunnel-FET Fabrication

The procedures outlined below are for the fabrication of $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ vertical Tunnel-FET. The machines utilized in the fabrication are located in the Microsystems Technology Laboratories at MIT unless otherwise noted.

Step #	Process Step	Process Details	Machine Name
1	Surface Cleaning	30 sec 4:1 HCl	Acidhood/TRL
2	Sputter Mo	Recipe: yut_Mo_20nm	AJA-TRL/TRL
3	PMMA Spin	A8, 3000 RPM, 60 sec, Bake 180 C, 3 min	coater/TRL
4	E-beam Lithography	TFET_L1, 10 nA, 0.28 us Dose: 1244 $\mu C/cm^2$	Elionix /EBL
5	Develop	MIBK:IPA 1:3, 90 sec	photo-wet-r/TRL
6	Ashing	800W, 3 min	asher-TRL/TRL
7	Ti/Au Deposition	5 nm/30 nm	eBeamFP/TRL
8	Liftoff	Acetone 20 min, Ultrasonic Power 2	photo-wet-Au/TRL
9	Mo Etch	Recipe: XZMO.rcp 90 sec	Plasmaquest/TRL
10	InGaAs cap recess	Recipe: 59, 120 C, 15 sec, 20 nm	SAMCO/TRL
11	InGaAs cap recess 2	Citric Acid:H_2O_2 10:1 20 sec	Acidhood/TRL
12	InP thinning	Digital Etch (Ash 800W 3 min + H_2SO_4:H_2O_2 1:1 30 sec) × 2	Asher-TRL/TRL Acidhood/TRL
13	HSQ Spin	6%, 3500 RPM, 60 sec, Bake 180C, 2 min	coater/TRL
14	E-beam Lithography	TFET_L2, 10 nA, 0.22us Dose: 2200 $\mu C/cm^2$	Elionix /EBL
15	Develop	TMAH 25%, 90 sec	Acidhood/TRL
16	Mesa Etch	Recipe: 59, 120 C, 45 sec, 50 nm	SAMCO/TRL

17	HSQ Strip	BOE 7 sec	Acidhood/TRL
18	Surface Passivation	Ash 800W 3 min, H_2SO_4:H_2O_2 1:1 30 sec	Asher-TRL/TRL Acidhood/TRL
19	ALD	HfO_2, 50 cycle, 250 C	ALD/ICL
19	PMMA Spin	A6, 3000 RPM, 60 sec, Bake 180 C, 3 min	coater/TRL
20	E-beam Lithography	TFET_L3, 10 nA, 0.3 us Dose: 1330 $\mu C/cm^2$	Elionix /EBL
21	Develop	MIBK:IPA 1:3, 90 sec	photo-wet-r/TRL
22	Ashing	800 W, 3 min	asher-TRL/TRL
23	Pd/Au deposition	30 nm/40 nm	eBeamAu/TRL
24	Liftoff	Acetone 20 min, Ultrasonic Power 2	photo-wet-Au/TRL
25	ALD	Al_2O_3, 40 cycle, 250 C	ALD/ICL
26	ZEP Spin	2500 RPM, 60 sec, Bake 190 C, 3 min	coater/TRL
27	E-beam Lithography	TFET_L4, 500 pA, 0.2 us Dose: 400 $\mu C/cm^2$	Elionix /EBL
28	Develop	Xylenes, 60 sec	photo-wet-r/TRL
29	Air-bridge Etch	Recipe: 59, 40 C, 75 sec	SAMCO/TRL
30	ZEP Strip	NMP, 60 C, 1 hr & Ash 800 W, 10 min	photo-wet-r/TRL Asher-TRL/TRL
31	Air-bridge Undercut	1:100 NH_4OH:H_2O_2, 3 min; TMAH 5 min	Acidhood/TRL
32	ALD	Al_2O_3, 40 cycle, 250 C	ALD/ICL
33	PMMA Spin	A6, 3000 RPM, 60 sec, Bake 180 C, 3 min	coater/TRL
34	E-beam Lithography	TFET_L5, 10 nA, 0.28 us Dose: 1244 $\mu C/cm^2$	Elionix /EBL
35	Develop	MIBK:IPA 1:3, 90 sec	photo-wet-r/TRL

36	Source Recess	Recipe: 59, 120 C, 38 sec, ~ 8 nm	SAMCO/TRL
37	Source Recess 2	Citric Acid:H_2O_2 2:1 30 sec	Acidhood/TRL
38	PMMA Strip	Acetone 20 min	photo-wet-Au/TRL
39	PMMA Spin	A6, 3000 RPM, 60 sec, Bake 180 C, 3 min	coater/TRL
40	E-beam Lithography	TFET_L6, 10 nA, 0.28 us Dose: 1244 $\mu C/cm^2$	Elionix /EBL
41	Develop	MIBK:IPA 1:3, 90 sec	photo-wet-r/TRL
42	Ashing	800 W, 3 min	asher-TRL/TRL
43	Surface Clean	HCl:H_2O_2 1:10, 30 sec	Acidhood/TRL
44	Pd/Au deposition	30 nm/30 nm	eBeamAu/TRL
45	Liftoff	Acetone 20 min, Ultrasonic Power 2	photo-wet-Au/TRL
46	Resist Ashing	1000 W, 10 min	Asher-TRL/TRL
47	ALD	Al_2O_3, 40 cycle, 250 C	ALD/ICL
48	ILD Deposition	HFSiO, 2 min 15 sec, 50 nm	STS-CVD/TRL
49	PMMA Spin	A8, 3000 RPM, 60 sec, Bake 180 C, 3 min	coater/TRL
50	E-beam Lithography	TFET_L7, 10 nA, 0.28 us Dose: 1244 $\mu C/cm^2$	Elionix /EBL
51	Develop	MIBK:IPA 1:3, 90 sec	photo-wet-r/TRL
52	Via Etch	Recipe: XZSIO.rcp, 220 sec, 70 nm	Plasmaquest/TRL
53	Via Etch 2	Recipe: 59, 120 C, 60 sec	SAMCO/TRL
54	PMMA Strip	Acetone 20 min	photo-wet-Au/TRL
55	Resist Ashing	1000 W, 10 min	Asher-TRL/TRL
56	PMMA Spin	A6, 3000 RPM, 60 sec, Bake 180 C, 3 min	coater/TRL

57	E-beam Lithography	TFET_L8, 10 nA, 0.28 us Dose: 1244 $\mu C/cm^2$	Elionix /EBL
58	Develop	MIBK:IPA 1:3, 90 sec	photo-wet-r/TRL
59	Ashing	800W, 3 min	asher-TRL/TRL
60	Ti/Au Deposition	10 nm/100 nm	eBeamFP/TRL
61	Liftoff	Acetone 20 min, Ultrasonic Power 2	photo-wet-Au/TRL
62	AZ5214 Spin	4000 RPM, 60 sec, Bake 80 C, 3 min	coater/TRL
63	Photolithography	Hard 9 sec, Image Reversal Bake: 110 C, 3 min, Flood 90 sec	MA6/TRL
64	Develop	AZ442, 60 sec or until clear	photo-wet-r/TRL
65	Ashing	800 W, 5 min	asher-TRL/TRL
66	Ti/Au Deposition	10 nm/150 nm	eBeamFP/TRL
67	Liftoff	Acetone 20 min, Ultrasonic Power 2	photo-wet-Au/TRL

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