Efficient, Low-distortion Switch-mode Power Amplifier for Amplitude Modulation

by

Christopher Buenrostro

S.B., Electrical Engineering and Computer Science

Massachusetts Institute of Technology, 2010.

Submitted to the Department of Electrical Engineering and Computer Science

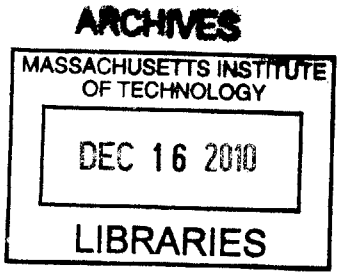
in Partial Fulfillment of the Requirements for the Degree of

Master of Engineering in Electrical Engineering and Computer Science

at the Massachusetts Institute of Technology

September 28, 2010

[FEBRUARY 2011]



Author _____

Department of Electrical Engineering and Computer Science
September 28, 2010

Certified by _____

James K. Roberge
Professor of Electrical Engineering
Thesis Supervisor

Accepted by _____

Dr. Christopher J. Terman
Chairman, Masters of Engineering Thesis Committee

Efficient, Low-distortion Switch-mode Power Amplifier for Amplitude Modulation

by

Christopher Buenrostro

Submitted to the

Department of Electrical Engineering and Computer Science

September 28, 2010

in Partial Fulfillment of the Requirements for the Degree of

Master of Engineering in Electrical Engineering and Computer Science

ABSTRACT

Amplitude modulation systems are used in many areas of engineering, especially communication based disciplines. Typical systems have low-level signals which encode the desired information to be transmitted. These low-level signals are usually not of adequate power to transmit the desired information across a target medium, thus requiring modulation and power amplification. In general, two goals of power amplifier design are low-distortion and high-efficiency. To meet these goals, a unique switch-mode power amplifier intended for amplitude modulation which utilizes spectral content at the carrier frequency is designed, simulated, and built. Theoretical predictions of total harmonic distortion (THD) and efficiency are made, and the constructed prototype results are measured. The THD for a 1 kHz modulating tone is predicted to be 0.9% and measured to be 4.15% worst case. The amplifier output stage efficiency is predicted to be 95.8% and measured to be 95.4% worst case.

Thesis Supervisor: James K. Roberge
Title: Professor of Electrical Engineering

Contents

List of Figures

List of Tables

Acknowledgments

For their teaching and academic guidance, my Professors at MIT deserve my most sincere gratitude. Of particular influence were and continue to be Professor Joel Dawson, Professor Paul Gray, Professor Jim Roberge, Professor Alan Oppenheim, Professor David Perreault, Professor Anantha Chandrakasan, Professor Nicholas Makris, Professor James Kirtley, and Dr. Kent Lundberg.

For their extra effort and help during my academic career at MIT, Anne Hunter and Arnold Henderson all receive my extreme thanks and will be forever remembered as vital to my completion of this work. If it weren't for their efforts, the chance to complete this thesis would never have formed.

For their support and encouragement no matter what the circumstances, my parents, Cindy and Gilbert, and my grandparents receive more thanks than can be expressed by words. Without their unconditional love and guidance, I would not have been capable of achieving my dream of completing a graduate degree from MIT. In addition to my parents, I would like to thank Elizabeth Kowalski for her love and patience during the completion of this thesis. Beyond just moral support, Elizabeth helped tremendously in technical editing, for which I am forever grateful. Also, Sean Schoenmakers receives my special thanks for sticking through the good and the bad of undergraduate life at MIT with me both when I needed him and when I did not.

I would also like to thank the authors whose work provided the foundations for this thesis. I am only able to achieve because these men and women have worked so hard.

Chapter 1

Introduction

Amplitude modulation (AM) is a common communication technique generally used for transmitting a target signal through a medium more conducive to frequencies higher than those in the target itself. The most basic form of amplitude modulation is termed double-sideband (DSB) modulation which focuses primarily on producing an output signal of the general form

$$y(t) = [1 + x(t)] \sin(2\pi f_c t)$$

where $-1 \leq x(t) \leq 1$ and f_c is the carrier frequency. Amplitude modulation system power requirements/levels vary depending on the particular application. If low-power signals are the only interest, many highly linear techniques exist which are not necessarily efficient. However, in high-power applications efficiency becomes increasingly important as practical concerns, e.g. thermal and power supply lifetime, increase the design constraints. High-power amplitude modulation applications at a fixed carrier frequency are the primary focus of this thesis.

A typical high-power amplitude modulation system will contain a low-power target (control) signal to be modulated. There are generally two primary goals of this low-power to high-power amplification system: linearity and efficiency. Consequently, power amplifier metrics are based, for the most part, on relating these two factors. In this thesis, total harmonic distortion (THD) and time-averaged input power relative to time-averaged output power (standard definition of efficiency) are of primary interest.

Most modern power amplifiers fundamentally fall in to one of two categories: linear or switch-mode (though these categories need not limit one's view on the "power amplifier world"' as countless hybrid systems exist which have characteristics of both). Generally speaking, linear amplifiers have

historically tended towards high linearity (as the name would suggest) but low efficiency. Conversely, switch-mode power amplifiers historically have tended towards high efficiency but low linearity. As a consequence electrical engineers have devoted great resources over many decades to eliminating the trade off between linearity and efficiency in both linear and switch-mode power amplifiers. In this thesis, switch-mode amplifiers are of primary interest.

Given the desire to make a high-power amplitude modulation system at a fixed carrier frequency using a switch-mode power amplifier, the popular Class-D modulating amplifier is a viable option. The Class-D modulating amplifier, as referenced in this thesis, is defined to be a switch-mode, modulating amplifier using pulse-width modulation (PWM) with switching frequency well above the highest frequency of the signal to be modulated. The modulating information is acquired by low-pass (or band-pass) filtering the switch-mode output. A potential drawback to this common technique is high switching rates leading to lower efficiency (techniques exist, e.g. soft-switching, that attempt to address this problem but are not considered in this thesis). Furthermore, the final amplitude modulated signal may need to be sufficiently band-limited around the carrier as to not interfere with other spectral bands. In this thesis, the primary goal is exploration of a modulation technique referred to here as pulse-blanked pulse-width modulation (PBPWM) that allows for slower switching (lower switching losses) than a comparable Class-D amplifier while providing adequate fidelity.

To evaluate the PBPWM technique, theoretical analysis is performed, simulations are conducted, and design/construction of a prototype amplifier are implemented. One intent of this thesis is to keep the content free of frequency range and application constraints to provide a generally useful analysis, but building a prototype system requires concrete specifications. Thus, measurement equipment limitations and other constraints (including time) led to design and construction of a prototype operating at a 50kHz carrier frequency with a 1kHz modulating tone delivering 60 Watts into a 5 Ohm load set to resonate at the carrier by using a 120nF capacitor and 88uH inductor (in a series connection). Likewise the design target efficiency is 80% and target THD is approximately 1%, both specifications chosen to "ground" the design and provide comparison for other potential implementations (basis for these specifications is provided in Chapter 2).

This thesis is organized as follows. In Chapter 2, the relevant background material for amplitude modulation and power amplifiers is presented. A theoretical analysis of the PBPWM technique is then performed. Simulation procedures and results are then presented. Analog considerations and expected non-ideal characteristics (though still approached theoretically) are then analyzed. In Chapter 3, the practical design and implementation of a system constructed to meet the above

mentioned design criterion is presented. The "paper" design is shown first and the physical prototype second. In Chapter 4, measured waveforms from the prototype along with efficiency results are presented along with analysis of the results. Measurement equipment, techniques, and conditioning are then discussed to help support result validity. In Chapter 5, a summary and final analysis of the topics, procedures, and results are presented along with future work to be completed.

Chapter 2

Background, Theory, and Simulations

2.1 Chapter Structure

This chapter is organized as follows. First, an overview of amplitude modulation is presented. Second, a brief overview of power amplifiers relevant to this thesis is given. Third, the pulse-blanked pulse-width modulation (PBPWM) waveform is defined and spectral analysis is performed. Fourth, simulation results of a test PBPWM waveform are presented and discussed.

2.2 Amplitude Modulation Overview

As stated in the introduction chapter, amplitude modulation (AM) can be viewed as a multiplication of a carrier wave with a modulating waveform written as

$$y(t) = [1 + x(t)] \sin(2\pi f_c t)$$

where x(t) is limited to ± 1 and f_c is the carrier frequency [1]. The input x(t) is limited in magnitude to avoid a condition known as overmodulation, which is a condition typically to be avoided [1].

A plot of the frequency content, specifically the magnitude of the Fourier Transform, gives insight into the spectral characteristics of AM systems. Since multiplication in time translates to convolution in frequency, the process shown in Figure 2.1 illustrates ideal amplitude modulation [2]. The ideal frequency magnitude in Figure 2.1 is important as it is the goal to which variants of double-sideband

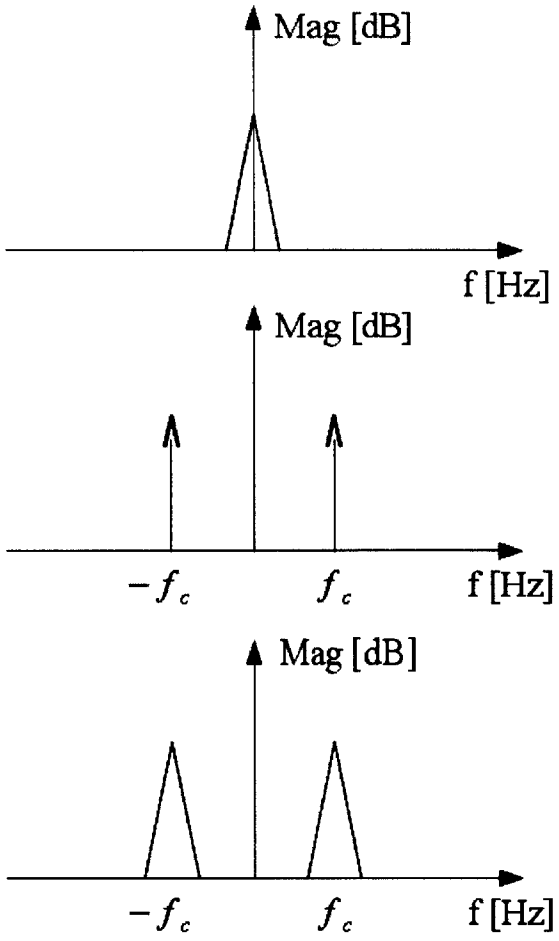


Figure 2.1: Ideal amplitude modulation

(DSB) modulation techniques tether.

Real systems will inevitably exhibit nonlinearities which will cause a practical system to stray from the target case. Analytically, this variance from the target can be generally written as

$$y(t) = [1 + x(t)]\, g\left(\sin\left(2\pi f_c t\right)\right)$$

where g() is a nonlinear function. Assuming the function g() has a convergent power series expansion (for simplicity the McLaurin series is used), the first few terms give

$$\begin{aligned} y(t) &= [1 + x(t)]\left[a_0 + a_1 \sin\left(2\pi f_c t\right) + a_2 \sin^2\left(2\pi f_c t\right) + a_3 \sin^3\left(2\pi f_c t\right) + ...\right] \\ &\approx [1 + x(t)]\left[a_0 + a_1 \sin\left(2\pi f_c t\right) + a_2 \sin^2\left(2\pi f_c t\right) + a_3 \sin^3\left(2\pi f_c t\right)\right] \end{aligned}$$

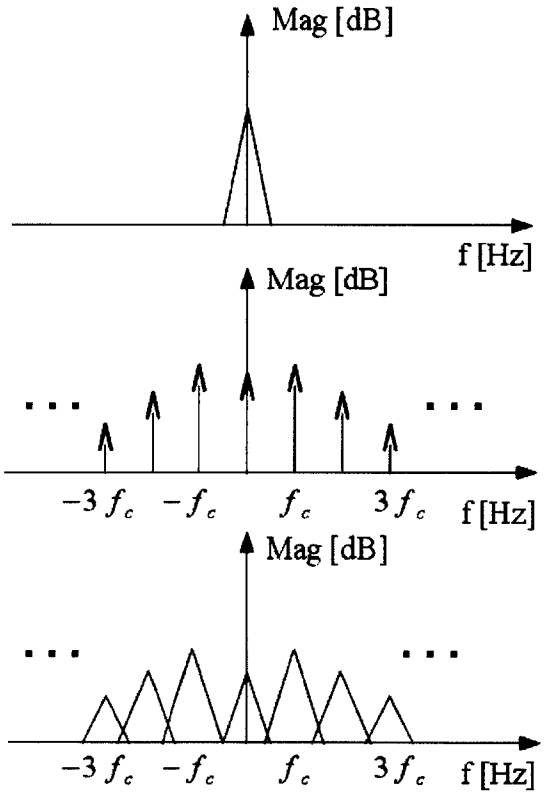


Figure 2.2: Nonlinear Modulation

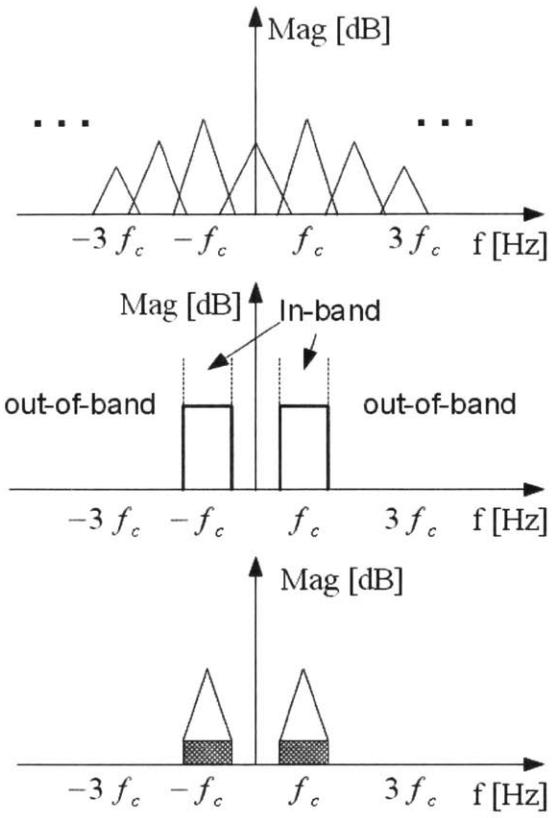


Figure 2.3: In-band distortion after ideal filtering.

Using DeMoivre's formula or equivalently noting $\sin^2\theta = \frac{1}{2}(1-\cos 2\theta)$ and $\sin^3\theta = \sin^2\theta\sin\theta = \frac{1}{2}(1-\cos 2\theta)\sin\theta$, it is apparent that spectral content will exist (in general) at the harmonics of the carrier frequency f_c [4]. A qualitative sketch of the above phenomenon is shown in Figure 2.2. It is emphasized that Figure 2.2 is not to be interpreted quantitatively and is merely used for illustration.

If the spectrum in Figure 2.1 is the target (as it is in this thesis), there are two types of distortion introduced in nonlinear modulation as seen in Figure 2.2: in-band and out-of-band. Of the two bands, out-of-band distortion can potentially be filtered out through the use of a bandpass network while in-band distortion typically cannot. An illustration of the distortion bands is shown in Figure 2.3.

2.3 Power Amplifier Overview

In general, power amplifier designs tend to have (at least) two goals: linearity and efficiency. Unfortunately, increasing one tends to decrease the other. Engineering effort over many decades has been focused on achieving high levels of both linearity and efficiency, culminating in two broad classifications of amplifiers: linear and switch-mode (again, many hybrids exist)[7],[8],[10], and [9].

The primary distinction between the two amplifier types is transistor operation regimes. For illustration, it is assumed the power MOSFET is the transistor type used in a given amplifier. Given this assumption, a linear amplifier would operate its MOSFETs in the triode (or linear) regime for some if not all of an output cycle. Operation in the triode regime requires simultaneous current through and voltage across the drain and source of the MOSFET, thus causing power dissipation in the transistor at any given instant. Conversely, switch-mode amplifiers (ideally) operate MOSFETs in the cutoff (zero drain current) and saturation (zero drain to source voltage) regimes at any given instant, thus giving zero instantaneous power and a theoretical efficiency of 100%.

The highest theoretical efficiency for a linear amplifier, specifically the Class B power amplifier, is $\approx 78.5\%$, but this efficiency is unrealizable in practice [7]. Switch-mode power amplifiers, on the other hand, are realizeable in practice well above 78.5% [7]. The linear amplifier efficiency bound sets the target prototype efficiency of 80% used in this thesis.

For modulation applications, many variants of switch-mode amplifiers exist and are in common use. The particular amplifier architecture used for comparison in this thesis is the Class-D switch-mode power amplifier. The output of this amplifier is typically low-pass filtered to acquire the modulating signal. The higher the switching frequency the greater the power loss (in general) of the amplifier. An amplitude modulation system such as the one designed in this thesis can be implemented using a conventional Class-D amplifier with the appropriate switching frequency by simply considering the baseband bandwidth to be the carrier plus the modulating bandwidth.

To setup a comparison, it is noted that the PBPWM technique will be shown to have no even harmonics of the switching waveform as well as no harmonics of multiple three, therefore giving a spectrum with distortion starting at the fifth harmonic. Thus, a comparable Class-D power amplifier would require a switch-frequency no lower than five times the carrier frequency (assuming low baseband distortion when sampling at five times the carrier, which has been proven possible [12]). Now, the PBPWM technique discussed in this thesis will be shown to require the capability of switching at six times the carrier frequency but only imposes the switching losses of a system which operates at two times the carrier frequency. As a result, PBPWM, when compared to a conventional Class-D amplifier, will require the ability to switch slightly faster but have one-third the losses. Determination of the theoretical and practical loss of linearity given this efficiency boost is a primary goal of this thesis.

2.4 Spectral Analysis

The goal in this section is to derive the time function and spectral content of the PBPWM waveform content around the carrier frequency. From these results, the theoretical THD for a given single-tone can be calculated to any accuracy desired. This number sets a bound on the expected performance for the PBPWM technique.

This section is difficult to present in an intuitive manner without jumping to the end right at the start. Therefore, the best way to proceed (in this author's opinion) is to do just that, i.e. start at the end. Thus, the following section goes as follows. First, the PBPWM waveform is presented. Second, the PBPWM waveform is decomposed into a product of a non-modulated carrier containing no harmonics of multiple three and a standard PWM waveform. Third, the non-modulated carrier and PWM waveforms are analyzed individually. Fourth, the two waveforms are brought back together and the result analyzed. Fifth, the theoretical THD for a single-tone modulating waveform is derived and numerically approximated.

Before proceeding, the Fourier series expansion for a time waveform [4] is defined as

$$f(x) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos(nx) + b_n \sin(nx) \tag{2.1}$$

$$a_n = \frac{1}{\pi} \int_0^{2\pi} f(x) \cos(nx)\, dx \tag{2.2}$$

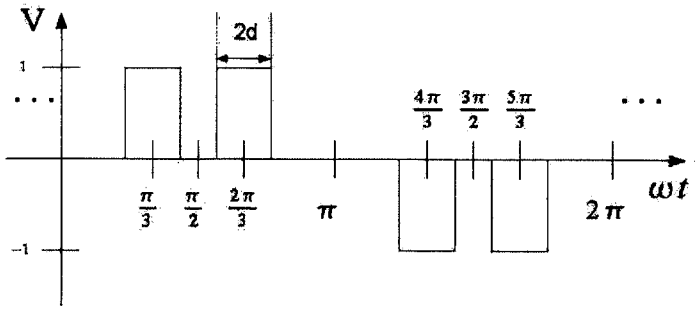
$$b_n = \frac{1}{\pi} \int_0^{2\pi} f(x) \sin(nx)\, dx \tag{2.3}$$

where it is assumed that the fundamental period of the waveform is 2π.

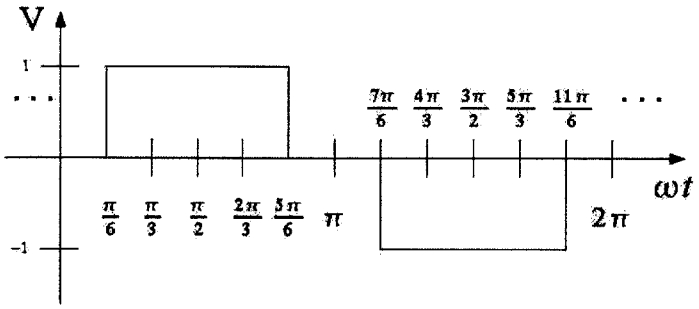
2.4.1 PBPWM Waveform

The PBPWM waveform is shown in Figure 2.4. The arrows in Figure 2.4(a) indicate the pulses are width modulated. Each non-zero pulse occurs around a multiple of $\frac{\pi}{3}$. There are two blanked pulses, occurring at zero and π radians, giving six pulses per 2π period with the pattern: blank, positive, positive, blank, negative, negative. The duty cycle definition is illustrated in Figure 2.4(a). A duty cycle of $d = 1$ is equivalent to $\frac{\pi}{6}$, so the absolute radian value for a given duty cycle is $d\frac{\pi}{6}$ from the pulse center. Figure 2.4(b) illustrates the waveform at maximum duty cycle, $d = 1$.

As a starting point, the case of a fixed but arbitrary duty cycle is examined since it is both odd and has half-wave symmetry, meaning many of the Fourier series coefficients are zero as discussed



(a) PBPWM waveform with duty cycle definition.



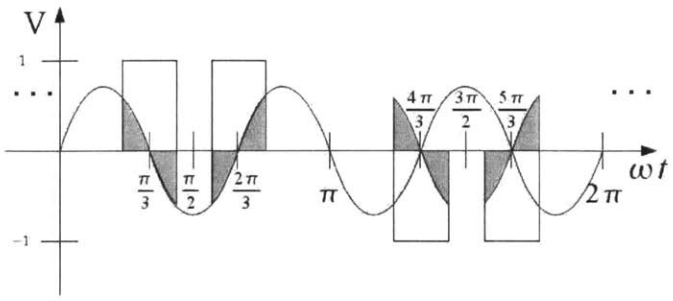
(b) PBPWM waveform with maximum duty cycle, d=1.

Figure 2.4: PBPWM waveforms.

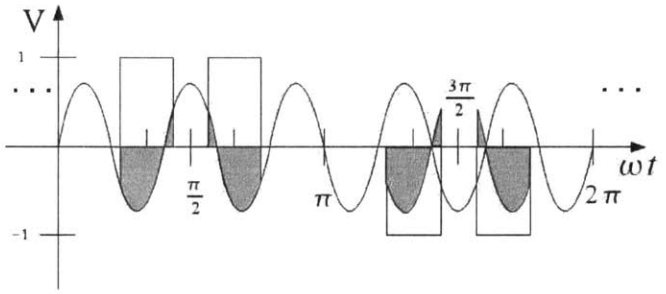
in the following sections [6]. This case provides a good intuition for further analysis. It will later be argued that the requirement of fixed duty cycles can be dropped without introducing harmonics.

Proving PBPWM Waveform Has No Third Harmonic: Graphical Approach

The illustrations in Figure 2.5 serve as graphical tool used in waveforms that are instantaneously zero or one to qualitatively determine the Fourier series expansion coefficient magnitudes [8]. In Figure 2.5(a) a sine wave of three times the carrier frequency is superimposed on the original waveform, and a similar waveform of five times the carrier frequency is superimposed in Figure 2.5(b). The shaded area above zero represents positive contribution to the first Fourier series coefficient for the sine wave terms. The shaded area below zero represents negative contribution to the corresponding first Fourier coefficient for the sine wave terms. The sum of the areas over one entire fundamental cycle gives the first Fourier coefficient for the sine wave terms. While this method can be used to give a quantitative solution with proper graph scaling, the method is used here in a more qualitative manner leaving the analytic, closed-form Fourier coefficient equation to give the quantitative solution. It is worth mentioning that in general the same approach can be used for the cosine terms of the Fourier series expansion, but this approach is not useful here as the cosine terms are known



(a) Third harmonic contribution.



(b) Fifth harmonic contribution.

Figure 2.5: Graphical determination of fixed duty cycle PBPWM waveform Fourier series sine wave components.

to be zero due to odd symmetry of the waveform.

Examination of Figure 2.5 reveals the absence of the third sine term harmonic but non-zero fifth term harmonic. To give further importance to Figure 2.5(a), it is illustrative to imagine if the two blanked pulses were present at zero and 2π, the third harmonic along with all harmonics of multiple three would be present. As such, the absence of these pulses is very important in this waveform.

Proving PBPWM Waveform Has No Third Harmonic: Analytic Approach

Since the waveform has both odd and half-wave symmetry, the Fourier series expansion will contain no cosine terms or even sine terms [6]. Consequently, only the odd sine terms in the Fourier expansion need to be analyzed. The sine terms of the Fourier series expansion are given by

$$
\begin{aligned}
b_n &= \frac{4}{\pi}\int_{\frac{\pi}{3}-d\frac{\pi}{6}}^{\frac{\pi}{3}+d\frac{\pi}{6}} \sin(nx)\,dx \qquad (2.4)\\
&= -\frac{4}{n\pi}\left[\cos(nx)\,|_{\frac{\pi}{3}-d\frac{\pi}{6}}^{\frac{\pi}{3}+d\frac{\pi}{6}}\right]\\
&= -\frac{4}{n\pi}\left[\cos\left(n(\frac{\pi}{3}+d\frac{\pi}{6})\right)-\cos\left(n(\frac{\pi}{3}-d\frac{\pi}{6})\right)\right]\\
&= -\frac{4}{n\pi}\left[\cos\left(n\frac{\pi}{3}+nd\frac{\pi}{6}\right)-\cos\left(n\frac{\pi}{3}-nd\frac{\pi}{6}\right)\right]\\
&= -\frac{4}{n\pi}\left[-2\sin\left(n\frac{\pi}{3}\right)\sin\left(nd\frac{\pi}{6}\right)\right]\\
&= \frac{8}{n\pi}\left[\sin\left(n\frac{\pi}{3}\right)\sin\left(nd\frac{\pi}{6}\right)\right] \text{ for n odd}
\end{aligned}
$$

The first line in the above derivation contains a factor of four due to each pulse contributing equally to the final coefficient value. This factor is a consequence of the odd and half-wave symmetric property of the waveform.

For $n = 3m$ where m is an integer, i.e. n is a multiple of three, Equation 2.5 gives

$$
\begin{aligned}
b_{n=3m} &= \frac{8}{3m\pi}\left[\sin\left(3m\frac{\pi}{3}\right)\sin\left(3md\frac{\pi}{6}\right)\right] \qquad (2.5)\\
&= \frac{8}{3m\pi}\left[\sin(m\pi)\sin\left(md\frac{\pi}{2}\right)\right]\\
&= 0 \text{ for m 1,3,5, etc...}
\end{aligned}
$$

Therefore, it is clear (hopefully) that the remaining odd harmonics are non-zero (except for d=0 of course). It has now been established both graphically and analytically that the PBPWM waveform will contain only odd harmonics which are not multiples of three.

2.4.2 Decomposition

The PBPWM waveform for arbitrary duty cycles can be decomposed into the multiplication of two waveforms as shown in Figure 2.6. At this point, **the requirement of fixed duty cycle per period is dropped**. The two waveforms in Figure 2.6 are now examined separately, but it is emphasized that the modulated waveform is six times the frequency of the non-modulated waveform. In addition, the non-modulated waveform is of the same frequency as the original PBPWM waveform. In the following, any reference to the carrier frequency is in reference to the frequency of the non-modulated waveform in Figure 2.6 and, equivalently, the original PBPWM waveform fundamental frequency.

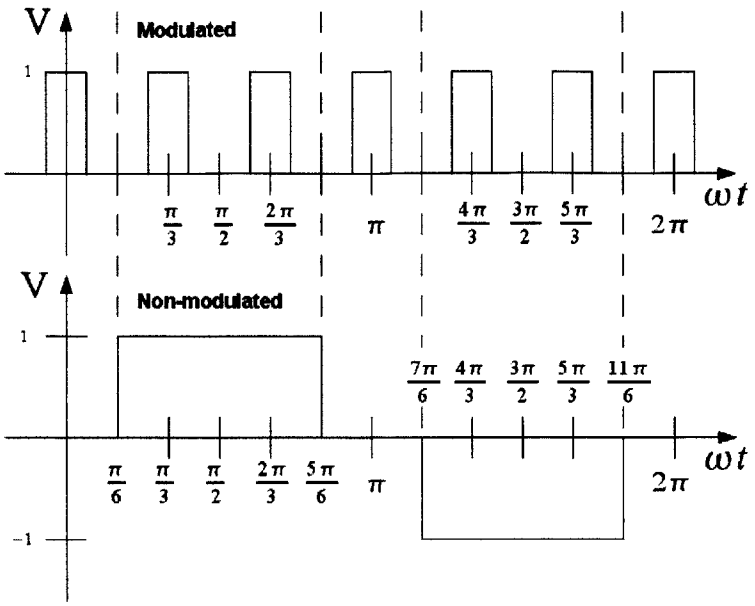


Figure 2.6: Decomposition of PBPWM waveform into the product of a PWM waveform (top) and a non-modulated carrier wave (bottom).

Non-modulated Carrier Waveform

The non-modulated waveform in Figure 2.6 is recognized as being the same waveform appearing in Figure 2.4(b) and contains no harmonics of multiple three as already proven in Equation 2.6 and also shown in [8]. Plugging d=1 in to Equation 2.5, the following solution is obtained for the non-zero Fourier series sine wave terms

$$b_n = \frac{8}{n\pi}\left[\sin\left(n\frac{\pi}{3}\right)\sin\left(n\frac{\pi}{6}\right)\right] \text{ for n odd} \tag{2.6}$$

with the first few terms calculated as

$$
\begin{aligned}
b_1 &= \frac{2\sqrt{3}}{\pi} V_{DC} \\
b_5 &= -\left(\frac{1}{5}\right) \frac{2\sqrt{3}}{\pi} V_{DC} \\
b_7 &= -\left(\frac{1}{7}\right) \frac{2\sqrt{3}}{\pi} V_{DC} \\
b_{11} &= \left(\frac{1}{11}\right) \frac{2\sqrt{3}}{\pi} V_{DC} \\
b_{13} &= \left(\frac{1}{13}\right) \frac{2\sqrt{3}}{\pi} V_{DC} \\
b_{17} &= -\left(\frac{1}{17}\right) \frac{2\sqrt{3}}{\pi} V_{DC} \\
b_{19} &= -\left(\frac{1}{19}\right) \frac{2\sqrt{3}}{\pi} V_{DC}.
\end{aligned}
$$

Pulse-width Modulation

Qualitative Solution

The exact shape and magnitude of the PWM spectral content are not vital for determining which convolved components will lie around the carrier. All that is required for this analysis is the existence of energy around DC, six times the carrier, and all integer multiples of six times the carrier, which is reasonable to assume (and is validated shortly). Thus, the qualitative spectral plot in Figure 2.7 is drawn without consideration for the actual shape of the information other than it is centered around harmonics of six times the carrier frequency. Again, the point in this section is exact knowledge of the spectrum is not required for graphical analysis.

Quantitative Solution

While the exact solution is not required for identifying contribution from convolution, the spectral content of the PWM waveform will be required when recombining the modulated and non-modulated waveforms of Figure 2.6 to obtain an analytic time equation, so the corresponding PWM spectral content is now presented.

Up to this point, there has been no mention of how the PWM waveform is generated from the input modulating signal. Typically, a base waveform of period equal to the PWM waveform period is compared with the modulating signal, and a binary output waveform is generated based on this comparison. Three common base waveform which lead to tractable closed-form solutions to the final PWM signal are leading edge sawtooth waves, trailing-edge sawtooth waves, and triangle waves

[12]. The details of the spectral analysis differentiating the base waveforms are not shown here, but ultimately a triangle wave is chosen for the base waveform since it is easy to implement and has zero baseband distortion. The resulting relevant equation is (along with simplification)

$$\begin{aligned} y(t) &= x(t) + \\ &\sum_{k=1}^{\infty} (-1)^k \left(\frac{2}{k\pi}\right) \left[\sin\left(2\pi k 6 f_c t + k\pi \frac{x(t)+1}{2}\right) - \sin\left(2\pi k 6 f_c t - k\pi \frac{x(t)+1}{2}\right)\right] \\ &= x(t) + \sum_{k=1}^{\infty} (-1)^k \left(\frac{2}{k\pi}\right) \left[2\cos(2\pi k 6 f_c t) \sin\left(\frac{k\pi}{2}(x(t)+1)\right)\right] \\ &= x(t) + \sum_{k=1}^{\infty} \left[(-1)^k \left(\frac{4}{k\pi}\right) \sin\left(\frac{k\pi}{2} x(t) + \frac{k\pi}{2}\right)\right] \cos(2\pi k 6 f_c t) \end{aligned} \tag{2.7}$$

where $x(t)$ is the input modulating signal ranging from the values -1 to 1, $y(t)$ is the output PWM waveform, and $6f_c$ is the switching frequency of the triangle wave (note the higher switch frequency is to account for the relationship between the modulated and non-modulated waveforms). This important result reveals there is no distortion in the baseband modulating signal $x(t)$ and all harmonics of the switching frequency contain phase modulated (distorted) versions of the baseband signal.

It will prove useful to define the following

$$a_k \triangleq \left[(-1)^k \left(\frac{4}{k\pi}\right) \sin\left(\frac{k\pi}{2} x(t) + \frac{k\pi}{2}\right)\right] \tag{2.8}$$

which allows the harmonics of the switching frequency in the above equation to be rewritten as $y_k(t) = a_k \cos(2\pi(k6f_c)t)$. The trigonometric relationships

$$\begin{aligned} \sin(\theta + \pi) &= -\sin(\theta) \\ \sin\left(\theta + \frac{\pi}{2}\right) &= \cos(\theta) \\ \sin\left(\theta - \frac{\pi}{2}\right) &= -\cos(\theta) \\ \sin(\theta - \pi) &= -\sin(\theta) \\ \cos(\theta + \pi) &= -\cos(\theta) \\ \cos\left(\theta + \frac{\pi}{2}\right) &= -\sin(\theta) \\ \cos\left(\theta - \frac{\pi}{2}\right) &= \sin(\theta) \\ \cos(\theta - \pi) &= -\cos(\theta) \end{aligned}$$

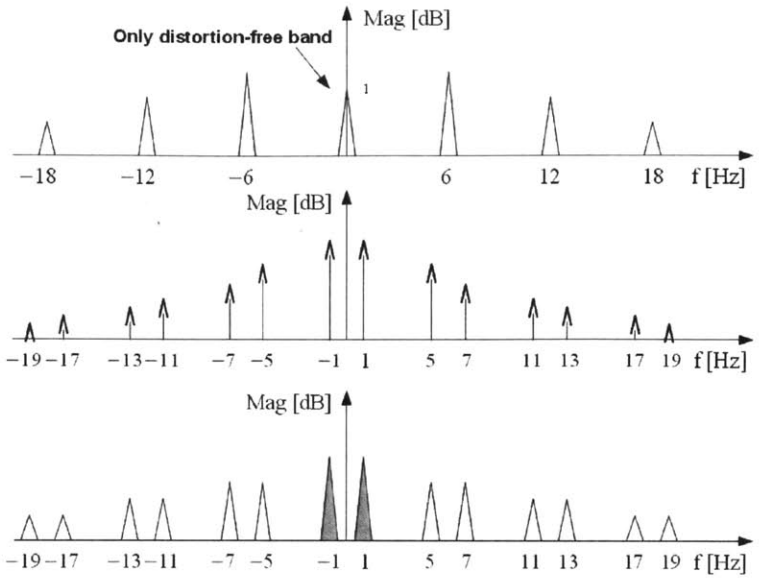


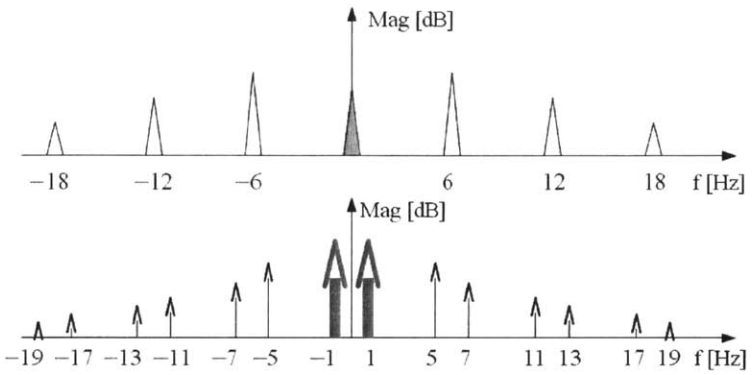
Figure 2.7: Frequency spectrum magnitude for the PWM waveform (top), non-modulated waveform (middle), and convolution of the two (bottom).

give the first few terms in a_k as

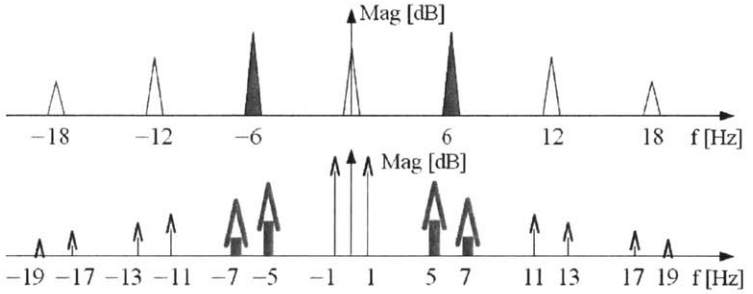
$$\begin{aligned} a_1(t) &= -\left(\frac{4}{\pi}\right)\cos\left(\frac{\pi}{2}x(t)\right) \\ a_2(t) &= -\left(\frac{2}{\pi}\right)\sin\left(\pi x(t)\right) \\ a_3(t) &= \left(\frac{4}{3\pi}\right)\cos\left(\frac{3\pi}{2}x(t)\right) \\ a_4(t) &= \left(\frac{1}{\pi}\right)\sin\left(2\pi x(t)\right) \\ a_5(t) &= \left(\frac{4}{5\pi}\right)\cos\left(\frac{5\pi}{2}x(t)\right) \end{aligned} \tag{2.9}$$

2.4.3 Recombination

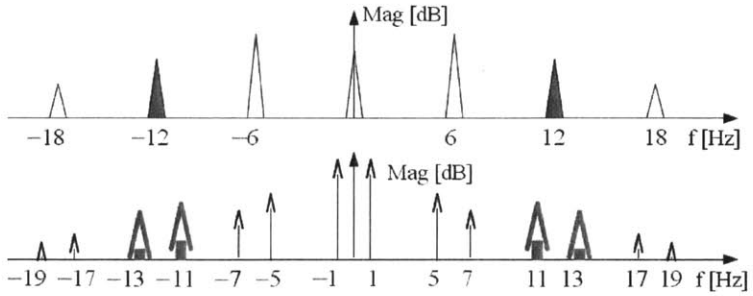
The magnitude of the frequency spectrum of the modulated and non-modulated waveforms along with the resulting convolution of the two is illustrated in Figure 2.7. Only the spectral content produced around the carrier frequency is of interest. Therefore, instead of trying to solve for $p(t)$ directly, the components that, when convolved together, produce a result falling on the carrier frequency are first identified, greatly simplifying analytic analysis. Figure 2.8(b) and Figure 2.8(c) highlight these components in the spectral domain. Figure 2.7 shows the only distortion-free contribution to the final output waveform from the convolution process, which is the target (ideal) component signal



(a) Non-distorted contribution to the final target signal.



(b) Distorted contribution to the final target signal from the 5th and 7th carrier harmonics.



(c) Distorted contribution to the final target signal from the 11th and 13th carrier harmonics.

component. The final convolution of the modulated and non-modulated waveforms is defined as $p(t)$ and is given as

$$\begin{aligned} p(t) &= y(t) \times b(t) \\ &= \left[x(t) + \sum_{k=1}^{\infty} a_k \cos(2\pi k 6 f_c t) \right] \times \left[\sum_{n=1}^{\infty} b_n \sin(2\pi n f_c t) \right] \end{aligned} \tag{2.10}$$

The above figures indicate frequency components of interest. Figure 2.8(a) shows the DC component of the PWM waveform and fundamental component of the non-modulated waveform group together. Figure 2.8(b) shows the fundamental component of the PWM waveform and both the fifth and seventh harmonics of the non-modulated waveform group together. Figure 2.8(c) shows the second carrier harmonic of the PWM waveform and both the 11th and 13th harmonics of the non-modulated waveform group together. Putting this grouping in analytic form gives

$$\begin{aligned} p(t) &= x(t) b_1 \sin(2\pi f_c t) \\ &\quad + a_1 \cos(2\pi 6 f_c t) b_5 \sin(2\pi 5 f_c t) + a_1 \cos(2\pi 6 f_c t) b_7 \sin(2\pi 7 f_c t) + \ldots \\ &= x(t) b_1 \sin(2\pi f_c t) \\ &\quad + a_1 b_5 \left(\frac{1}{2}\right) [\sin(2\pi 11 f_c t) - \sin(2\pi f_c t)] \\ &\quad + a_1 b_7 \left(\frac{1}{2}\right) [\sin(2\pi 13 f_c t) - \sin(-2\pi f_c t)] + \ldots \\ &= x(t) b_1 \sin(2\pi f_c t) + \frac{a_1}{2} (b_7 - b_5) [\sin(2\pi f_c t)] + \ldots \end{aligned} \tag{2.11}$$

The same formulation will follow for other harmonics. The final result gives

$$p(t) = \left[x(t) b_1 + \frac{a_1}{2} (b_7 - b_5) + \frac{a_2}{2} (b_{13} - b_{11}) + \frac{a_3}{2} (b_{19} - b_{17}) + \ldots \right] \sin(2\pi f_c t) + \ldots \tag{2.12}$$

Doing the math in intermediate steps gives

$$
\begin{aligned}
b_7 - b_5 &= \frac{2\sqrt{3}}{\pi} V_{DC} \left[-\frac{1}{7} + \frac{1}{5} \right] \\
&= \left(\frac{2}{35} \right) \left(\frac{2\sqrt{3}}{\pi} V_{DC} \right) \\
b_{13} - b_{11} &= \frac{2\sqrt{3}}{\pi} V_{DC} \left[\frac{1}{13} - \frac{1}{11} \right] \\
&= -\left(\frac{2}{143} \right) \left(\frac{2\sqrt{3}}{\pi} V_{DC} \right) \\
b_{19} - b_{17} &= \left(\frac{2}{323} \right) \left(\frac{2\sqrt{3}}{\pi} V_{DC} \right) \\
b_{25} - b_{23} &= -\left(\frac{2}{575} \right) \left(\frac{2\sqrt{3}}{\pi} V_{DC} \right) \\
b_{31} - b_{29} &= \left(\frac{2}{899} \right) \left(\frac{2\sqrt{3}}{\pi} V_{DC} \right)
\end{aligned}
$$

The first few components of the baseband contribution now give

$$
\begin{aligned}
x(t)\, b_1 &= \frac{2\sqrt{3}}{\pi} V_{DC} x(t) \qquad (2.13) \\
\frac{a_1}{2} (b_7 - b_5) &= \left[-\left(\frac{4}{\pi} \right) \cos\left(\frac{\pi}{2} x(t) \right) \right] \times \left[\frac{2\sqrt{3}}{35\pi} V_{DC} \right] \\
&= \frac{8\sqrt{3}}{35\pi^2} V_{DC} \cos\left(\frac{\pi}{2} x(t) \right) \\
\frac{a_2}{2} (b_{13} - b_{11}) &= \left[-\frac{2}{\pi} \sin(\pi x(t)) \right] \left[-\frac{2\sqrt{3}}{143\pi} V_{DC} \right] \\
&= \frac{4\sqrt{3}}{143\pi^2} V_{DC} \sin(\pi x(t)) \\
\frac{a_3}{2} (b_{19} - b_{17}) &= \left[\left(\frac{4}{3\pi} \right) \cos\left(\frac{3\pi}{2} x(t) \right) \right] \left[\left(\frac{2\sqrt{3}}{323\pi} V_{DC} \right) \right] \\
&= \frac{8\sqrt{3}}{969\pi^2} V_{DC} \cos\left(\frac{3\pi}{2} x(t) \right)
\end{aligned}
$$

from which it is noted that the first distortion term is approximately -28.7 dB below the fundamental, the second distortion term is approximately -47.0 dB below the fundamental, and the third distortion term is approximately -57.8 dB below the fundamental.

2.4.4 Calculating Single-tone THD

In this section, a single-tone input of $\sin(2\pi f_0 t)$ is assumed. To calculate THD of this tone, the following generating functions are used

$$\cos(z\sin\theta) = J_0(z) + 2\sum_{k=1}^{\infty} J_{2k}(z)\cos(2k\theta) \tag{2.14}$$

$$\sin(z\sin\theta) = 2\sum_{k=0}^{\infty} J_{2k+1}(z)\sin((2k+1)\theta) \tag{2.15}$$

where J_n are the nth order Bessel functions of the first kind of integer order [13]. These functions fall off rather quickly after the first few terms, so an approximation can be made without much loss in accuracy by taking the 3rd term and below. This approximation gives

$$\begin{aligned}\cos\left(\frac{\pi}{2}\sin(2\pi f_0 t)\right) &= J_0\left(\frac{\pi}{2}\right) + 2\sum_{k=1}^{\infty} J_{2k}\left(\frac{\pi}{2}\right)\cos(2\pi(2kf_0)t) \qquad (2.16)\\ &= .472 + .499\cos(2\pi(2f_0)t) + 0.028\cos(2\pi(4f_0)t) + ...\\ \sin(\pi\sin(2\pi f_0 t)) &= 2\sum_{k=0}^{\infty} J_{2k+1}(\pi)\cos(2\pi((2k+1)f_0)t) \qquad (2.17)\\ &= .570\sin(2\pi f_0 t) + 0.667\sin(2\pi(3f_0)t)\\ &\quad +0.104\sin(2\pi(5f_0)t) + 0.007\sin(2\pi(7f_0)t) + ...\end{aligned}$$

Ignoring the contribution from DC, the base tone, and higher order terms (all considered small) as well as noting the symmetry of the Bessel coefficients, the THD can be calculated approximately as

$$THD \approx \frac{\sqrt{\sum_{k=0}^{\infty}\left[\frac{8\sqrt{3}}{35\pi^2}2J_{2k}(\frac{\pi}{2})\right]^2 + \sum_{k=1}^{\infty}\left[\frac{4\sqrt{3}}{143\pi^2}2J_{2k+1}(\pi)\right]^2}}{\frac{2\sqrt{3}}{\pi}}. \tag{2.18}$$

For a pure tone, Equation 2.18 comes out to be about roughly 0.0086, which gives about 0.9% THD. It should be noted that Equation 2.18 reveals THD level is independent of tone frequency. However, a key assumption made in order to arrive at Equation 2.18 is modulated components from higher carrier harmonics are negligible. As the modulating tone becomes exceedingly large relative to the carrier, this assumption clearly breaks down. In practice, though, the modulating tone will most likely be well below the carrier frequency.

2.4.5 Resonant Load

As discussed in the next section, the THD deviation from a non-ideal bandpass filter depends on filter Q and the ratio of the modulating signal fundamental frequency to the carrier waveform, e.g. the effects are different for a 1kHZ tone modulated on a 50kHz carrier than for a 15kHz tone modulated on a 50kHz carrier.

The previous analysis alluded to an ideal bandpass filter to filter out harmonic components. In actuality, the filter will not be ideal, having both magnitude and phase variation over frequency. Thus, the effects of practical bandpass filtering using a simple resonant load need to be addressed. It is noted that more complicated analog filtering can be done at the amplifier output stage to produce a filter closer to ideal, but any filtering at the output of the amplifier must be done by components capable of handling high power. Any component parasitics will consequently have increased power loss and lower the overall amplifier efficiency. Additionally, inductors which carry potentially high currents must be used rather than simple resistive elements to maintain efficiency, which may increase design complexity.

The primary relationship of interest regarding the resonant network is filter Q-factor relative to the desired modulating signal bandwidth. A high filter Q will increase attenuation of carrier frequency harmonics but attenuate the modulating signal relative to the carrier and potentially introduce phase and magnitude errors. Conversely, a low filter Q will have less effect on the modulating signal relative to the carrier but gives less attenuation of carrier harmonics. As stated in Chapter 1, the prototype in this thesis uses a resonant load for filtering with a 5 Ω resistor, 88 μH inductor, and 120 nF capacitor. The resulting frequency response of this network will be studied in Chapter 3, but the end result will be that the effect of resonance on 50 kHz carrier modulated by a 1kHz tone should be negligible for the given network Q.

2.4.6 Simulation Procedure and Results

A simulation of the waveform was done to verify theoretical predictions before prototyping. While there is surely a more clever way to implement the simulations, the appropriate time functions were used to simulate the ideal, nonlinear comparison action of the triangle wave to a sample input. The test case used was a single tone for which the theoretical THD has already been calculated.

For the simulation, a triangle waveform was produced, a reference waveform was then produced, the two were compared, and the final output was either blanked or had its polarity flipped. The important parameter for this simulation is the the number of sample points in the base triangle

wave. This number should be no less than 1000 (determined empirically) which gives about 10 bits of resolution when comparing to the reference waveform. Furthermore, this number of sample points is what sets the available resolution of the output duty cycle. If this number is too low, the output spectrum will be colored by harmonic distortion, especially noticeable for 100 points per triangle or less, which is the equivalent affect seen by low bit resolution in any digital-to-analog converter. The duty cycle resolution requirement also ensures a relatively high sampling frequency relative to both the carrier frequency and the modulating tone frequency. Therefore, aliasing effects are negligible. In addition, the large oversampling factor means low-pass filtering and decimation can be used to reduce final Fast-Fourier Transform computation.

The results of this computation are shown in Figure 2.8 and Figure 2.9. The test tone used was 2.5 kHz with a 50 kHz carrier. From Figure 2.8, it is seen that the second harmonic is at about -36 dBc and the third is at about -54 dBc. This simulation results in a THD of approximately 1.6%. Figure 2.9 shows a zoomed-out view of the frequency spectrum, illustrating the carrier harmonic content. It is important to note that there are no even harmonics nor harmonics of multiple three present as expected. In addition, a resonance filter was created using the bilinear transformation applied to a resonant filter prototype with its transfer function equal to that of the resonant filter built in this thesis. The resulting attenuation for the first few carrier harmonics is shown in Figure 2.10.

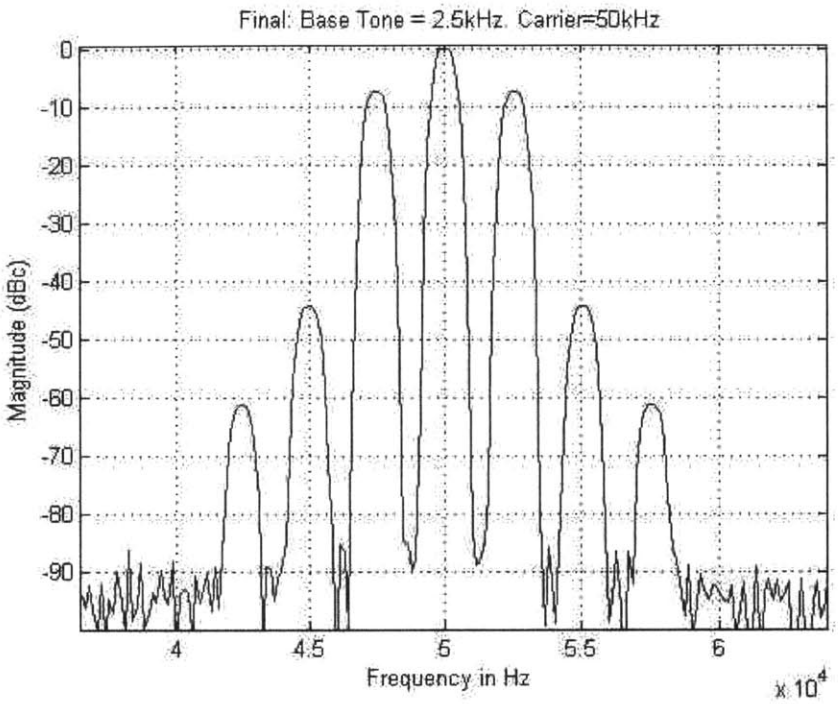


Figure 2.8: Simulation results zoomed in around the carrier frequency. Data processed using flattop window.

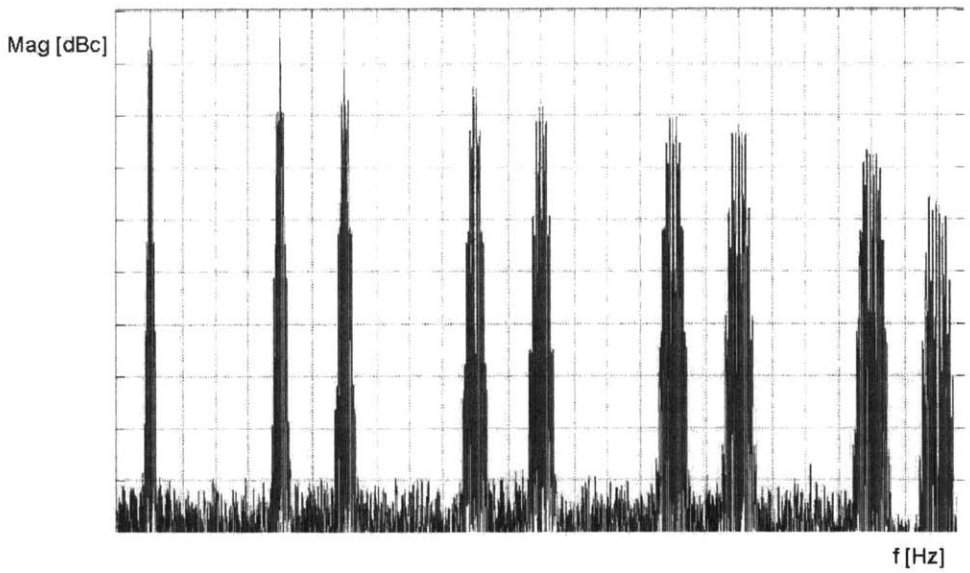


Figure 2.9: Simulation results as viewed over many carrier harmonics. Note the absence of even harmonics and harmonics of multiple three.

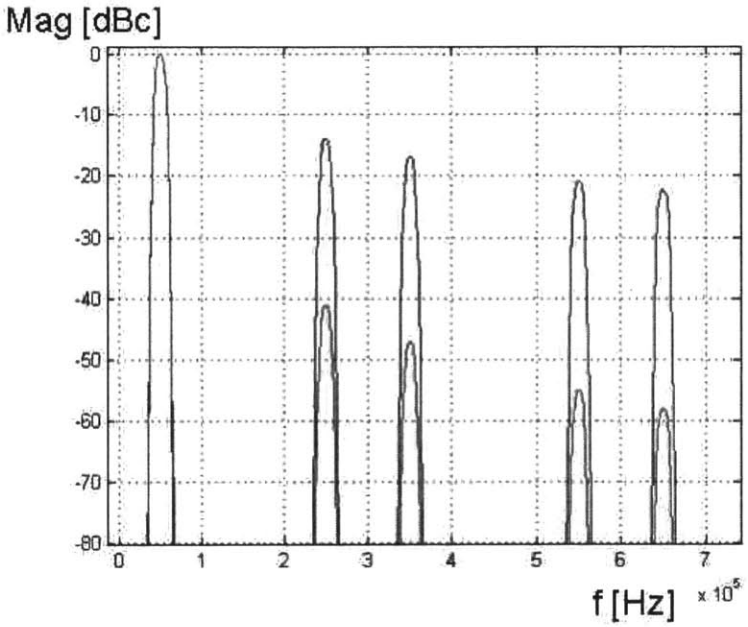


Figure 2.10: Illustration of resonant filtering effects on carrier harmonics. The highest waveform is the simulation result without accounting for the resonant filter, and the lower waveform is the simulation result after accounting for the resonant filter.

Chapter 3

Design and Prototype

In this chapter, the paper design and prototype construction of the developed PBPWM power amplifier are presented. First, the paper design is shown. This design is organized into three sections: control board design, load analysis, and power board design. As depicted in block diagram form in Figure 3.1, the control board design covers development of an integrator, choice of a comparator, and design of digital logic circuitry used to generate the PBPWM waveform. Corresponding power loss from the control board is then determined. The load analysis covers measurement of a series connected load inductor, resistor, and capacitor. Corresponding parasitics of each component are then presented and discussed. The power board design covers the choice of output stage topology, power switches, and power switch drivers. The expected power loss (including thermal analysis) is then presented. In each section, justification for design decisions is given. Second, the final board schematics and prototype construction are presented.

Before beginning, it is noted that the power loss of the control board is only briefly discussed and not emphasized in this thesis; this de-emphasis is for the following reasons. First, control board power loss does not scale with output current draw and, consequently, has less effect on efficiency as output power increases, e.g. one Watt of control board loss is a large portion of a two Watt power draw but not a large portion of a 100 Watt power draw. Second, low-power digital logic is relatively easy to find (not used in this thesis because it was not necessary). Third, operational amplifiers designed to operate on (low) single-supply voltages are readily available, greatly reducing power consumption (at increased design effort). Fourth, the square-wave and blanking signals can be generated from a number of much lower power sources than the microcontroller used, namely the TMS320F28027. Therefore, efficiency is ignored during control board development for faster design and prototyping under the assumption that control board power loss can be recovered with relative

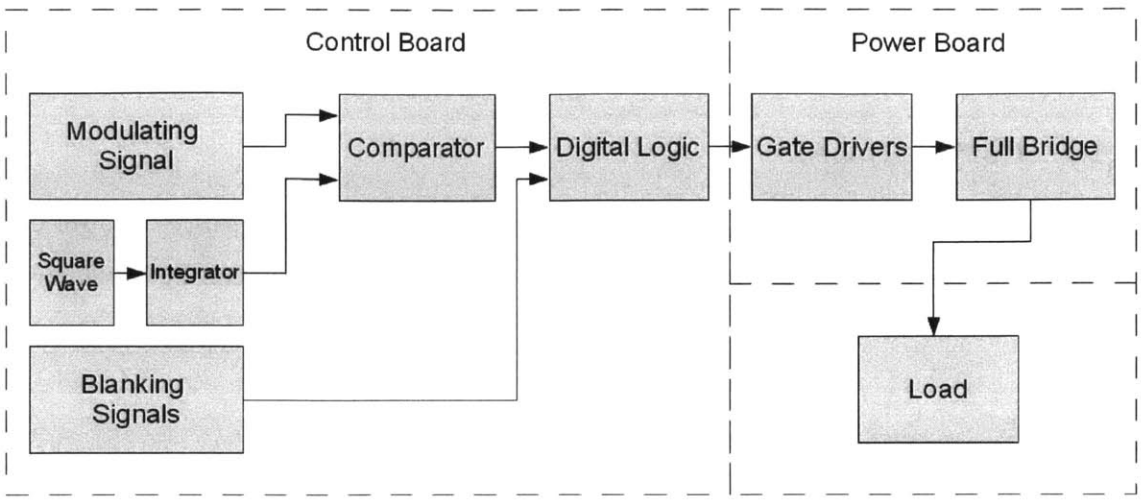


Figure 3.1: System block diagram.

ease through different component choices and increased design time.

In Table 3.1, the selection of chips used in this design is summarized for ease of reference. Reasoning behind chip selection will be given in this chapter as relevant chip functionality is discussed.

Table 3.1: Key Components

Part	Description
LF356	JFET input Single Op-amp
LM311	Comparator
M74HC08	Digital Inverter Gates
M74HC14	Digital AND Gates
IR2011	High and Low Side Gate Drivers
IRLM0030	MOSFETs

3.1 Paper Design

PBPWM generation is illustrated in Figure 3.1 and explained as follows. First, a square-wave of six times the final carrier frequency is generated by a microcontroller. Second, a triangle-wave is generated by integrating the square-wave. Third, the triangle-wave is compared with the modulating signal to form the PWM waveform. Fourth, the PWM waveform is processed by digital logic circuitry in conjunction with two "blanking" waveforms also generated by the microcontroller. Fifth, the output waveforms from the digital logic circuitry are sent to two half-bridge drivers which then control the operation of the power switches. Sixth, the power switches turn on and off in the PBPWM pattern to deliver the power amplified PBPWM waveform across the load (which then

resonates at the carrier to filter the waveform). In the following paper design, the control board is discussed first, the load is discussed second, and the power board is discussed third.

3.1.1 Control Board

This section covers the integrator, the comparator, and the digital logic circuitry. Control board losses are discussed during the section conclusion. Square-wave and pulse-blanking waveform generation are not discussed explicitly and are assumed easily generated from a microcontroller.

Integrator

The integrator and input signal integrity dramatically influence the overall amplifier system fidelity. This statement can be crassly reworded as "garbage in gives garbage out." For this thesis, the signal-to-noise ratio is not the primary metric of interest, so analysis will be done only to show sufficiently low noise to allow for proper THD measurement, i.e. not have the noise so high it swamps the expected output harmonics. However, even if the final noise is too high, oversampling and averaging of the output may recover a substantial portion of the signal [2]. To adequately measure 1% THD from a full-scale input (or 40 dB below full-scale), a required signal-to-noise ratio (SNR) of 60 dB (approximately 10-bits) from the integrator block is adequate.

In this section, the following topic ordering is used: stability analysis, choosing the op-amp, choosing the time constants, noise analysis, additional error sources, and component selection. Before proceeding, it is noted that the expected square wave input to the integrator from the microcontroller is unipolar, meaning a large DC bias will exist. Therefore, a decoupling capacitor is required at the input, which is chosen to be 1 μF for this design. In the following analysis, the DC blocking capacitor is, by design, large enough in value (has low enough impedance) that it can be ignored for stability calculations.

First, stability analysis is discussed. Due to the non-zero input bias current of any given operational amplifier, a resistor must be placed in parallel with the feedback capacitor or the output will rail. This topology is referred to as a leaky integrator and can be generically classified as an active low-pass filter. The inverting topology used for the leaky integrator is shown in Figure 3.2, where $R_F >> R_G$ by design. The inverting topology stability analysis and notation presented follow that found in [14]. The feedback impedance is denoted as Z_F, the impedance from the signal input to the op-amp inverting input is denoted as Z_G, and the op-amp open-loop gain is denoted as $a(s)$. The inverting topology can be broken into parts to give

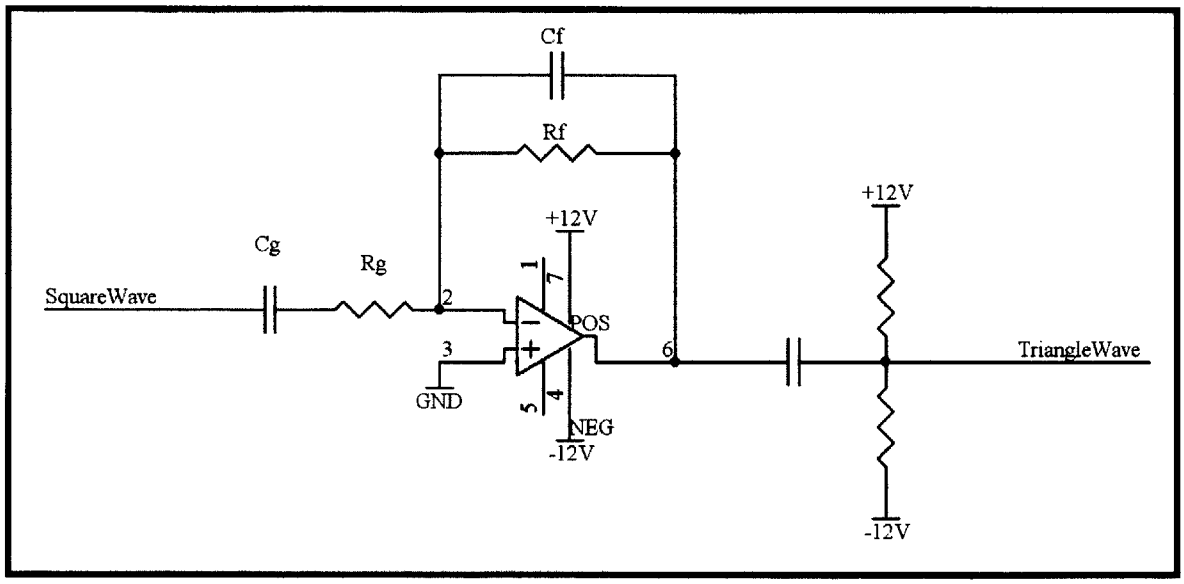


Figure 3.2: Implemented leaky integrator using inverting topology.

$$\begin{aligned} A &= -a(s)\frac{Z_F}{Z_G + Z_F} \\ \beta &= -\frac{Z_G}{Z_F} \\ L &= A\beta \\ &= a(s)\frac{Z_G}{Z_G + Z_F} \end{aligned}$$

where A is the direct gain, β is the feedback factor, and L is the loop gain.

For the leaky integrator, the impedances are

$$\begin{aligned} Z_F &= R_F || \frac{1}{sC_F} \\ &= \frac{R_F}{R_F C_F s + 1} \\ Z_G &= \frac{1}{C_G s} + R_G \\ &= \frac{R_G C_G s + 1}{C_G s} \end{aligned}$$

where the DC blocking capacitor at the input is ignored. Plugging parameters in to equation 3.1 gives

$$
\begin{aligned}
A &= -a(s)\frac{R_F}{R_F R_G C_F s + R_G + R_F} \\
&= -a(s)\frac{1}{R_G C_F s + 1} \\
\beta &= -\frac{R_G}{R_F}(R_F C_F s + 1) \\
L &= a(s)\frac{R_G}{R_F}\frac{R_F C_F s + 1}{R_G C_F s + 1}
\end{aligned}
$$

where $R_F >> R_G$ is used. Defining $R_F C_F$ to be τ_F and $R_G C_F$ to be τ_G, the following can be written as

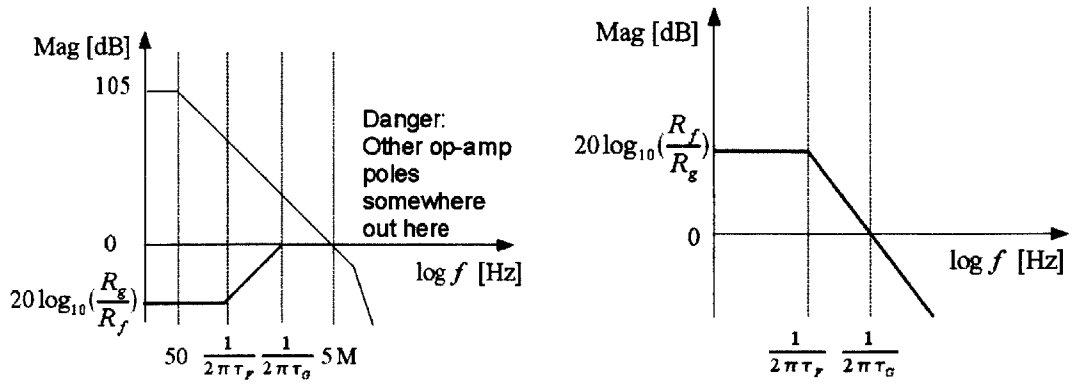
$$
\begin{aligned}
A &\approx -a(s)\frac{1}{\tau_G s + 1} \\
\beta &= -\frac{R_G}{R_F}(\tau_F s + 1) \\
L &= a(s)\frac{R_G}{R_F}\left(\frac{\tau_F s + 1}{\tau_G s + 1}\right).
\end{aligned}
$$

It is noted that $\tau_F >> \tau_G$ or, equivalently, $\frac{1}{\tau_F} << \frac{1}{\tau_G}$. The closed-loop transfer function can now be calculated as

$$
\begin{aligned}
\frac{V_{out}}{V_{in}} &= \frac{A}{1 + A\beta} \\
&\approx \frac{1}{\beta} \\
&\approx -\frac{R_F}{R_G}\left(\frac{1}{\tau_F s + 1}\right)
\end{aligned}
$$

where the second equation assumes $|A\beta| >> 1$ which is typically a safe assumption [15].

Figure 3.3 shows the resulting Fourier Transform magnitude plots for both the closed-loop and open-loop transfer functions (the op-amp open-loop transfer function shown in the figure is that of the LF356 for illustrative purposes). The open-loop transfer function magnitude at the top of Figure 3.3 illustrates why a unity-gain stable operational amplifiers is required for stability. The only affect the external components can have on crossover is to push this frequency higher where other operational amplifier poles certainly lie (recipe for instability). Therefore, it is important to keep τ_G smaller than the crossover frequency for stability (though this requirement is not terribly restrictive for this design). Fortunately, unity-gain stable operational amplifiers are rather abundant, and a



(a) Open-loop Transfer Function Magnitude Plot.

(b) Closed-loop Transfer Function Magnitude Plot.

Figure 3.3: Transfer function magnitude plots. Note the DC blocking capacitor C_g is ignored in these plots.

simple dominant-pole compensated op-amp will be used as discussed below.

Now, the specific op-amp which fits design needs is determined. Besides unity-gain stability, the next op-amp requirement is low-noise. The input stage of an op-amp has a great impact on its imperfections and, consequently, its ability to maintain signal integrity and low noise. To help aid component selection, a survey and comparison of operational amplifier input stages can be found in [16]. An operational amplifier with junction field-effect transistors (JFET) inputs is determined to be a strong choice for low input current noise performance. Furthermore, to provide an acceptable signal-to-noise ratio (SNR) as requisite for final THD measurements, the output voltage swing must be large (this statement is quantified in the next section). A large output voltage swing requires the op-amp be capable of using wide supply voltages . Finally, the op-amp must have a bandwidth of at least 3 MHz to allow for acceptable reproduction of the 300 kHz triangle wave, which, when combined with the requirement for large output voltage swing, requires a relatively large slew rate.

Given these design requirements, the LF356 is chosen. This op-amp is unity-gain stable, has JFET inputs allowing for low input current bias and low input current noise, allows for a large voltage supply range, has a gain-bandwidth product of 5 MHz, and has a relatively large slew rate of 12 Volts per microsecond. It is worth mentioning that the LF357 has a larger gain-bandwidth product than the LF356, meaning a potentially sharper triangle wave can be generated, but is not unity gain stable.

It is briefly noted that op-amp loading considerations were not of great importance since the integrator is followed by a comparator which provides negligible resistive and capacitive loading. In other designs, resistive loading would place requirements on the op-amp output drive current

capability, and capacitive loading would place requirements on the acceptable output resistance of the op-amp since the load capacitance and op-amp output resistance form an additional pole in the open-loop transfer function (potentially causing instability).

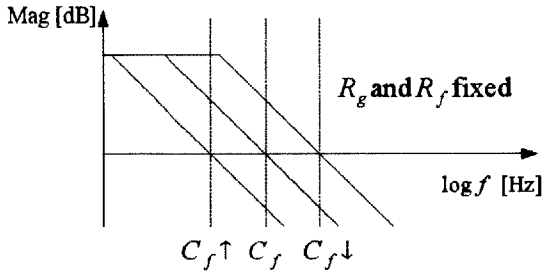
Next, time constants of the integrator are determined. Before starting with numerical calculation, Figure 3.4 is presented to give a qualitative feel for the effects of component variation. This figure is primarily of use when tweaking prototype values to fine tune the design. Now, the slew rate of the LF356 is 12 Volts per microsecond. The frequency of the input square wave is 300kHz (six times the carrier), which gives a period of $3.33\mu S$. The triangle wave peak-to-peak voltage swing is generated over half this period, which is $1.66\mu S$. Therefore, the maximum allowable peak-to-peak voltage is 12×1.66 which is approximately 19.92 Volts. To err on the safe side, the peak-to-peak voltage of the triangle wave is set at 18 Volts. The time based relationship between the square wave and triangle wave is

$$\begin{aligned} V_{tr,pp} &= \frac{1}{R_G C_F} \int_0^{\frac{T}{2}} \frac{V_{sq,pp}}{2} dt \\ &= \left(\frac{V_{sq,pp}}{2R_G C_F}\right)\left(\frac{T}{2}\right) \\ &= \left(\frac{V_{sq,pp}}{2R_G C_F}\right)\left(\frac{1}{2}\right)\left(\frac{1}{6f_c}\right) \\ &= \frac{V_{sq,pp}}{24 R_G C_F f_c} \end{aligned}$$

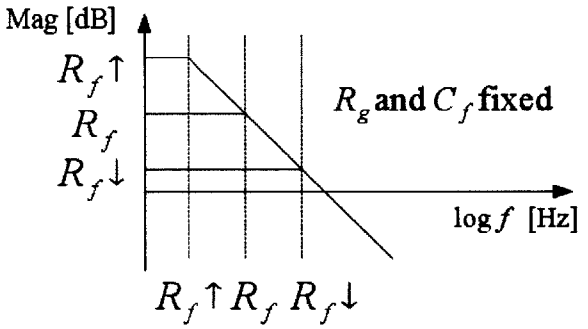
where $V_{tr,pp}$ is the triangle wave peak-to-peak voltage, $V_{sq,pp}$ is the square wave peak-to-peak voltage, T is the time period of the square wave, and f_c is the carrier frequency (50kHz). It is noted that $6f_C$ is used for the triangle wave frequency as explained in the introduction. Since the capacitor will be more limiting in component values, the required resistance for a given capacitance is solved. Plugging in for the expected triangle wave peak-to-peak and square wave peak-to-peak gives

$$R_G \leq \frac{1}{C_f} \frac{3.3}{24 \times 18 \times 50 \times 10^3}$$

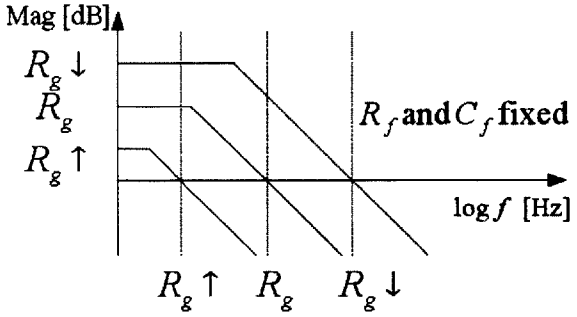
In order to avoid any phase shift in the fundamental frequency of the triangle wave (300kHz), $\frac{1}{\tau_F}$ is set at least a decade behind 300kHz, which gives



(a) Effects of changing C_f.



(b) Effects of changing R_f.



(c) Effects of changing R_g.

Figure 3.4: Qualitative effects of discrete component changes on integrator closed-loop transfer function magnitude.

$$\frac{1}{2\pi R_F C_F} \leq 30\text{kHz}$$

which can be rearranged to give

$$R_F \geq \frac{1}{2\pi \times 30 \times 10^3 \times C_F}.$$

The midband gain of the noise magnitude transfer function will be shown to be proportional to $\frac{R_F}{R_G}$. Therefore, to keep noise gain down to a minimum it is desirable to have R_G as high as allowable and R_F as low as possible. This relationship suggests R_F and R_G be chosen so as to stay as close to equality as possible in the above constraints. It is also noted that the input resistance for the leaky integrator is given by R_G, and the microcontroller used specifies a maximum output current of 20mA. Since the voltage output from the microcontroller will be 3.3V, the input resistance from the integrator stage should not go below 1 kΩ. Plugging in 100 pF for C_F gives 1.5 kΩ for R_G and 333 kΩ for R_F (the final value selections are summarized in Table 3.2). The chosen component vales are reasonable since 100pF is well enough above expected parasitic values and resistances are not excessively high or low [17].

Table 3.2: Leaky Integrator Component Values

Component	Value
R_F	333kΩ
R_G	1.5kΩ
C_F	100pF

Now, noise analysis is presented. The analysis and notation below follows [19]. First, the closed-loop noise gain is determined. Second, the op-amp noise is calculated. Third, the input current noise is calculated. Fourth, the resistor and capacitor noise voltages are calculated. Fifth, all noise sources are added together using root sum of the squares (RSS) to give the overall topology noise [18], [19]. Table 3.3 lists the variables used and their associated meaning.

Op-amp noise is now analyzed. The noise gain is determined by grounding the signal input node and placing a voltage source at the non-inverting terminal of the op-amp. From this perspective, the op-amp is configured as a non-inverting topology. Analysis of the non-inverting configuration gives the same open-loop response as the inverting analysis done before, but the non-inverting closed-loop gain becomes

Table 3.3: Noise Analysis Variable Mapping [19]

Variable	Meaning	Units
f_H	Upper Cutoff Frequency	Hertz
K_n	Equivalent Noise Bandwidth	Unitless
BW_n	Effective Noise Bandwidth	Hertz
e_{nBB}	Broadband Voltage Noise	Volts RMS
e_{BB}	Power Spectral Density for Broad-band Noise	Volts per $\sqrt{\text{Hertz}}$
e_{atf}	Power Spectral Density for a particular Frequency in 1/f Region	Volts per $\sqrt{\text{Hertz}}$
e_{fnorm}	Normalizing Noise At 1 Hertz	Volts RMS
e_{nf}	Total Noise from 1/f Region	Volts RMS
e_{nv}	Total Input Referred Voltage Noise	Volts RMS
e_{nr}	Effective Resistor Noise	Volts RMS
e_{nrvf}	Effective Total Noise Before Gain	Volts RMS
e_{nrms}	Noise referred to output	Volts RMS
e_{npp}	Noise referred to output	Volts peak-to-peak

$$\begin{aligned} 1+\frac{Z_f}{Z_G} &= 1+\left(\frac{R_F}{1+R_FC_Fs}\right)\left(\frac{C_Gs}{R_GC_Gs+1}\right) \\ &= \frac{(1+R_FC_Fs)(1+R_GC_Gs)+R_FC_FR_GC_Gs^2}{(1+R_FC_Fs)(1+R_GC_Gs)} \\ &= \frac{R_FC_FR_GC_Gs^2+(R_FC_F+R_GC_G+R_FC_G)s+1}{(1+R_FC_Fs)(1+R_GC_Gs)} \end{aligned}$$

where by design $R_FC_G >> R_FC_F + R_GC_G$, giving

$$1+\frac{Z_f}{Z_G} \approx \frac{R_FC_FR_GC_Gs^2+R_FC_Gs+1}{(1+R_FC_Fs)(1+R_GC_Gs)}$$

It is worth noting that since the open-loop function is identical for either topology, stability is independent of input location [14]. The closed-loop noise gain is shown in Figure 3.5.

The closed-loop poles appear at $s=-\frac{1}{R_FC_F}$ and $s=-\frac{1}{R_GC_G}$ while the zeros appear at

$$s = \frac{-R_FC_G \pm \sqrt{(R_FC_G)^2-4R_FC_FR_GC_G}}{2R_FC_FR_GC_G} \tag{3.1}$$

For the chosen component values, the poles are at 4.78 kHz and 106 Hz while the zeros are at 0.48 Hz and 1.00 MHz. Now, to determine the exact noise given in this topology, integration of the power spectral density over the entire frequency range of interest (approximately 1.57 times 5 MHz

for this design) is required. While simulation in SPICE is another option for measuring the noise contribution, a few simple hand calculations will suffice which do not contain integrals explicitly. The analysis presented here uses an assumption that will be justified at the end of the section, namely that the closed-loop noise gain shown in Figure 3.5 can be substituted by $\left(\frac{R_F}{R_G}\right)\frac{1}{R_F C_F s+1}$ and 1/f noise can be ignored without introducing substantial inaccuracy. This substitution should not be unreasonable for frequencies near and below $\frac{1}{2\pi R_F C_F}$ since $R_F >> R_G$ by design. Using this alternative closed-loop noise gain, the high frequency cutoff is given as

$$\begin{aligned} f_H &= \frac{1}{2\pi R_F C_F} \\ &= 4.78 \text{ kHz.} \end{aligned}$$

The effective noise bandwidth is then given by

$$\begin{aligned} BW_n &= f_H K_n \\ BW_n &= \left(4.78 \times 10^3\right)(1.57) \\ BW_n &\approx 7.5 \text{ kHz.} \end{aligned}$$

where K_n accounts for the effective noise bandwidth [14]. The broadband noise for the LF356 can then be calculated as

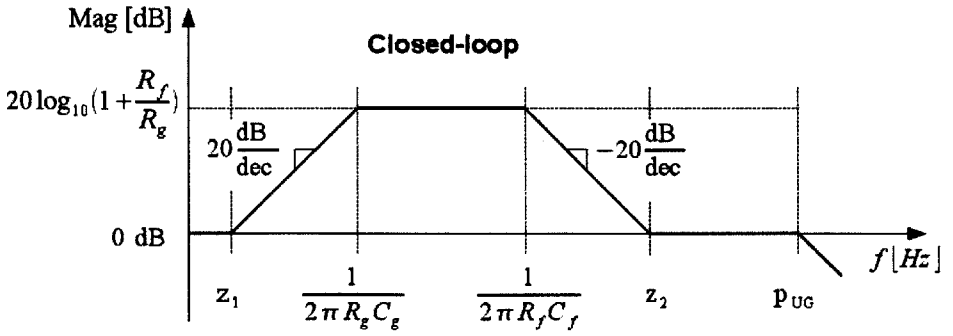


Figure 3.5: Closed-loop noise transfer function magnitude. The zeros are determined in Equation 3.1. P_{UG} is the unity-gain pole as determined by the operational amplifier (for the LF356, P_{UG} is 5 MHz).

$$
\begin{aligned}
e_{nBB} &= e_{BB}\sqrt{BW_n} \\
&= \left(12\frac{\text{nV}}{\sqrt{\text{Hz}}}\right)\sqrt{7.5\text{ kHz}} \\
&\approx 1\ \mu\text{Vrms}
\end{aligned}
$$

Since the 1/f noise is ignored, the total noise energy from noise voltage sources is

$$
e_{nv} \approx 1\ \mu\text{Vrms.}
$$

The input current noise is determined next. Using the closed-loop bandwidth determined above gives

$$
\begin{aligned}
i_{nBB} &= i_{BB}\sqrt{BW_n} \\
&= \left(10\frac{\text{fA}}{\sqrt{\text{Hz}}}\right)\sqrt{7.5\text{ kHz}} \\
&\approx 866\text{ fArms.}
\end{aligned}
$$

Input current 1/f noise can be ignored for JFET input op-amps [19]. The equivalent resistance is the parallel combination of the feedback and input impedances, which is approximately the input resistance in this design. The equivalent input current noise voltage is then given as

$$
\begin{aligned}
e_{ni} &= i_{nBB}R_{eq} \\
&\approx (866\text{ fArms})\,1.5\text{ k}\Omega \\
&\approx 1.30\text{ nVrms}
\end{aligned}
$$

which is small compared to the voltage noise source and will be ignored for the remainder of this analysis.

Resistor and capacitor thermal noise are now analyzed. The feedback path noise adds directly to the noise referred to the output without seeing the closed-loop noise transfer function. The feedback capacitor noise is given as $\sqrt{\frac{kT}{C}}$. For a 100 pF capacitor at room temperature, the noise

is approximately 4.5 μVrms. Thus the capacitor produces the same noise as a 9.1 GΩ resistor. The parallel combination of the feedback resistor, the equivalent resistor noise source for the capacitor, and the input resistor R_G gives the equivalent resistance, R_{eq}. The value of R_{eq} will be dominated by the input resistor, which gives a resistor thermal noise of

$$\begin{aligned} e_{nr} &= \sqrt{4kTR_{eq}\Delta f} \\ &= \sqrt{4\,(1.38\times 10^{-23})\,(273+25)\,(1.5\text{ k}\Omega)\,(7.5\text{ kHz})} \\ &\approx 430\text{ nVrms.} \end{aligned}$$

The total noise can now be determined. Considering all of the noise contributions gives

$$\begin{aligned} e_{nrvf} &= \sqrt{e_{nv}^2 + e_{nr}^2} \\ &\approx 1.1\mu\text{Vrms.} \end{aligned}$$

Multiplying by noise gain gives (why the feedback resistor should be small)

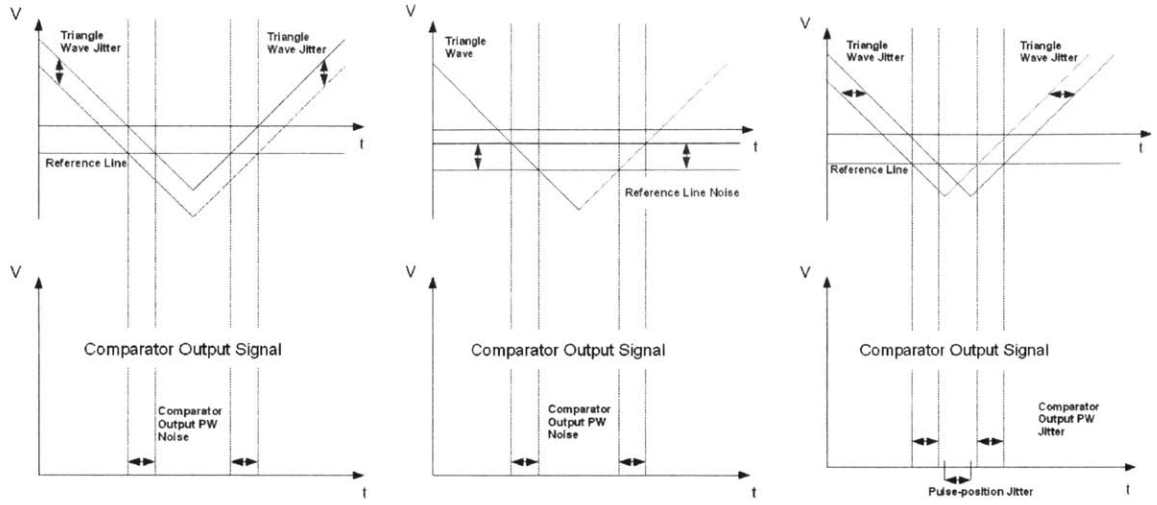
$$\begin{aligned} e_{nrms} &= e_{nrvf} \times 223 \\ &\approx 245\ \mu\text{Vrms} \end{aligned}$$

as the noise referred to the output. The feedback resistor and capacitor add a direct (non-gained) component to the output noise, but this addition is much smaller than the gained component and is ignored. Thus, the peak-to-peak voltage is approximated as

$$\begin{aligned} e_{npp} &= e_{nrms} \times 6 \\ &\approx 1.47\text{ mVpp} \end{aligned}$$

where the statistical analysis behind this approximation is given in [14].

As stated earlier, 60 dB of SNR is required for proper THD measurement. Given 18 Vpp for the triangle wave, a noise of 1.47 mVpp gives about -78.5 dB (13.2 bits) SNR at full-scale. For ease of



(a) Integrator output noise effects. (b) Reference line noise effects. (c) Input square-wave jitter effects.

Figure 3.6: Comparator output noise.

demonstration, ± 12 Volt supply rails are used for the op-amp which provide more than sufficient voltage swing.

Justification for the initial calculation assumption is now given. Though there will be some double counting in the following arguments, this double counting actually overestimates the noise contribution proclaimed negligible and thus further supports that the argument the noise contribution discussed can be ignored. If the op-amp were configured as a buffer with unity-gain, the first closed-loop pole would occur at crossover. The unity-gain noise power spectral density is equivalent to that of the leaky integrator minus the gain area above unity. For the unity-gain buffer, we get $f_H = 5\text{MHz}$, which gives $BW_n \approx 7.85\text{MHz}$. The effective broadband noise will then be given by $e_{nBB} \approx 34\mu\text{Vrms}$. The 1/f noise still remains negligible due to the blocking capacitor C_G (more specifically, the low-frequency pole-zero pair introduced in the Figure 3.5). In addition, 1/f noise also exists for frequencies in the high-gain region, though the power spectral density magnitude of the 1/f noise is less than the constant 12 nV per root Hertz from the white noise. The effective broadband noise is higher than those calculated for the leaky integrator before noise gain scaling, but this new noise value is then multiplied by unity instead of 233. The result gives a total noise value that is at least two orders of magnitude below the total noise calculated from the previous section analysis. Thus the single pole approximation originally stated is valid.

Next, other noise and error sources are discussed. In addition to op-amp noise, operational amplifiers can introduce error through open-loop gain nonlinearity, poor common-mode rejection ratio, and poor power supply rejection ratio just to name a few factors [20]. While these factors

are not examined in detail in this thesis, they are to be kept in mind when analyzing results and measurements. An important source of noise to mention goes along with the "garbage in gives garbage out" mantra at the start of this section. The noise source alluded to is square-wave jitter from the microcontroller. Since the signal-to-noise ratio is not considered in this thesis, this topic is only mentioned and illustrated in Figure 3.6(a), Figure 3.6(b), and Figure 3.6(c). Figure 3.6(a) illustrates how noise on the integrator output translates to noise on the PWM signal. The reference line, i.e. input modulating signal, and input square-wave to the integrator are assumed noise-free for the illustration. Figure 3.6(b) illustrates how noise on the reference line translates to noise on the PWM signal. The integrator output and input square-wave to the integrator are assumed noise-free for the illustration. Figure 3.6(c) illustrates how noise on the integrator input square wave translates to noise on the PWM signal. The reference line, i.e. input modulating signal, and integrator output are assumed noise-free for the illustration. It is noted that square-wave noise is the most detrimental source when comparing the above figures since the result potentially affects both comparator output pulse position and pulse-width.

Finally, passive component selection is briefly discussed. Since the design in this thesis need not necessarily be robust, i.e. account for temperature variations and component tolerances, X7R ceramic capacitors and thick-film resistors were used. In a more robust design, for example, plastic film capacitors composed of polystyrene or Teflon would be used instead of ceramic capacitors. For a more detailed analysis on component selection, a good reference is [17].

Comparator

The comparator chosen is the LM311. The pull-up resistor chosen for the open-collector output of the LM311 is set at 200 Ω to allow for fast pull-up action (if power were considered this value of pull-up resistance may not be acceptable). The 200 Ω resistor connected to a 5 Volt supply requires the comparator to sink approximately 25mA of current during pull-down, which is within the capabilities of the LM311. The propagation delay of the comparator is the primary parameter of interest and is determined from the data sheet to be approximately 200nS for design conditions of this thesis, which is acceptable. The voltage supply accepts the same ± 12 Volts used in the LF356 for the integrator as well as accepting ± 30 Volts of differential signal at the input. The power consumption for the LM311 is far from ideal for the design since it is on the order of the output MOSFET dissipation, but the control logic power consumption is not considered important in this design. The device is available in a DIP package for easy prototyping. The output offset voltage is not critically important since the output will be digital, thus only having to be below the appropriate

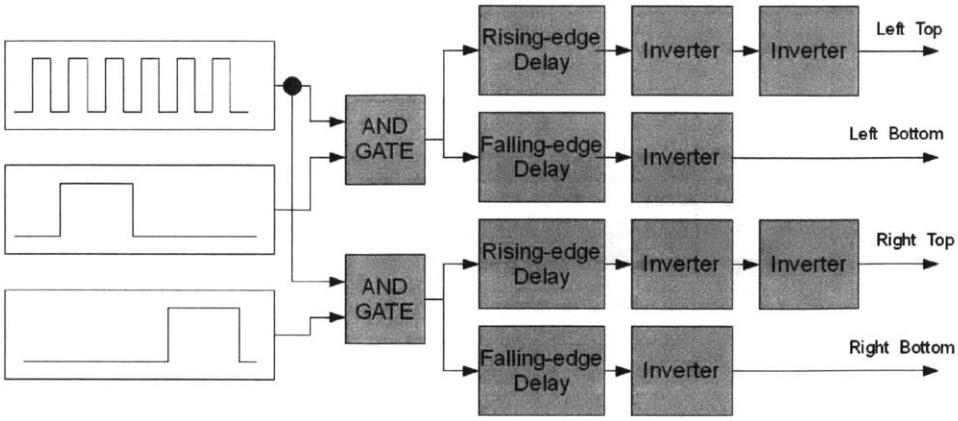


Figure 3.7: Digital logic circuitry. Signals on the left are: (top) PWM, (middle) left blanking, (bottom) right blanking. Inverters are Schmitt Trigger type. Output goes to gate driver ICs.

logic level set by the digital circuitry of the next stage. The primary references used to help choose the comparator were [21],[22],[23], and [24].

Digital Logic Circuitry

The digital logic circuitry consists of two (separate) 2-input *AND* gates, dead-time generation circuitry, and six Schmitt-trigger inverters. The signal flow is shown in Figure 3.7 and explained as follows. First, the PWM waveform generated by the comparator is sent as an input to two separate *AND* gates. Each *AND* gate receives the PWM waveform along with one of the two blanking signals generated by the microcontroller. These blanking signals repeat at the carrier frequency (one-sixth the square-wave frequency) and are phase-shifted relative to the square-wave. The process is shown in Figure 3.7. It is important to note the phase-shift of the blanking signals relative to the square-wave must take into account the phase delay introduced by the integrator and comparator. If pulse phase delay is not taken into account, there is a high-potential that pulse waveforms may be blanked in the middle of signal generation. Blanking a pulse at the wrong time will severely distort the output and cause extra switching loss. Second, the output of each *AND* gate is passed through a simple asymmetric delay generator (discussed below) to create a rising-edge and falling-edge deadtime for preventing shoot through [8]. Third, inverter gates buffer the appropriately delayed inputs and pass two signals for the left half-bridge driver (the PBPWM signal and its inverse) and two signals to the right half-bridge driver. The resulting waveforms is shown in Figure 3.8. It is important to note that each half-bridge only sees switch transitions during one-half of a given carrier period (this statement is illustrated later in the chapter during discussion of the design topology). The remainder of this

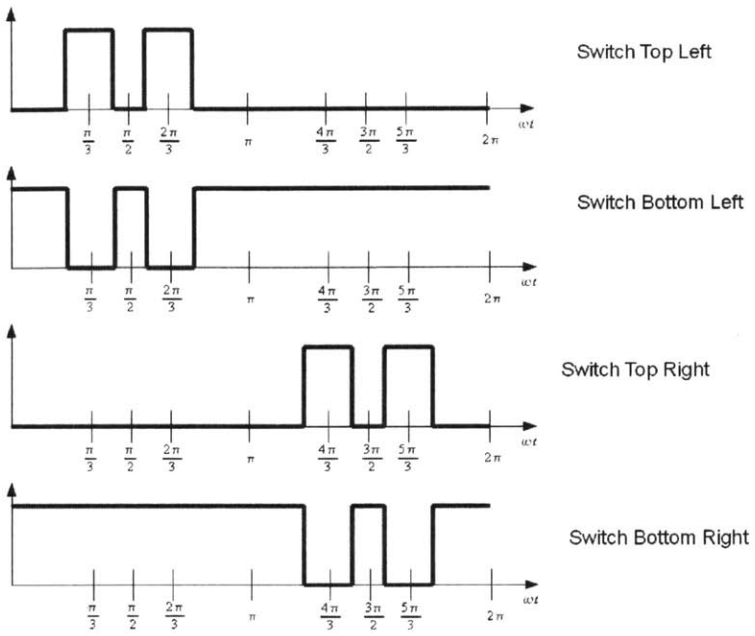


Figure 3.8: Signals sent to switch-drivers. The amplitudes of these signals are normalized in this figure such that a high level represents the switch being closed and a low signal represents the switch being open.

section contains discussion of delay effects (from dead-time, propagation delay, and rise/fall times), dead-time generation, inverter IC selection, and *AND* gate IC selection.

The effects of delay are now discussed. Propagation delays and rise/fall times of the given logic gates in addition to corresponding delays from other circuitry in the amplifier, e.g. gate drivers, determine the maximum allowable frequency of operation for the amplifier along with the maximum and minimum allowable duty cycles.

Dead-time generation is now discussed. The signals sent to either the left half-bridge or the right half-bridge are the exact inverses of each other with some delay between them. The dead-time generation circuitry is placed after the *AND* gates but before the inverters and is shown in Figure 3.9. The parallel combination of the diodes and the resistors allows for fast rise and slow fall or slow rise and fast fall (depending on the signal analyzed). The two separate paths allow for independent dead-times for the rising edge and the falling edge of a given transition.

The inverter gates are now discussed. The STMicroelectronics M74HC14 is used for the inverter logic. The M74HC14 has six Schmitt-trigger inverters which is the number required for the pulse-blanking logic. The propagation delays are approximately 12nS and balanced, which is adequate for the desired switching speeds. The rise and fall times are matches at 7nS. As shown in the data sheet, the input stage and output CMOS pair are both protected by voltage suppressing diodes (easing

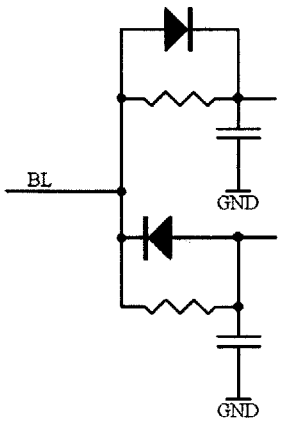


Figure 3.9: Rising-edge and falling-edge delay circuitry. The left side of the figure is the input, which consists of the PWM waveform logically "anded" with one of the blanking signals. The top diode-resistor network output gives a fast rise and slow fall. The bottom diode-resistor network output gives a slow rise and fast fall. The Schmitt Inverter output is then delayed by the corresponding RC time constant.

possible chip destruction from static discharge during prototyping).

The *AND* gates are now discussed. The STMicroelectronics M74HC08 was used for the *AND* gate logic. The M74HC08 contains six 2-input CMOS *AND* gates, which is two more than needed for the prototype but was chosen for accessibility. The propagation delay is approximately 7nS and balanced, which is adequate for the desired switching speeds. The rise and fall time of the gates are approximately 7nS and balanced as well. As shown in the data sheet, the input stage and output CMOS pair are both protected by voltage suppressing diodes (again aiding prototyping).

Control Board Losses

This section is intended to be brief. The primary mechanisms for power dissipation in the control board are quiescent current draw from each IC package, power draw from the comparator pull-up resistor, power lost to charging and discharging capacitances, and power lost to leakage currents. Furthermore, the power loss from the microcontroller used to generate the square-wave and pulse-blanking signals also adds additional loss. In addition, voltage regulators supplying the rails would also add power loss, though this loss can be minimal if switching regulators are used. To give a number for total power loss of the control board designed in this thesis, the current draw from the control board voltage rails was measured to be approximately 40 mA in the worst case. The rails are ± 12 Volts, giving approximately one Watt of power draw. This current draw includes an LED which sinks approximately 10 mA.

3.1.2 Load

In this section, the ideal load is stated and described, the devices and techniques used to measure component parasitics is given, the resulting (measured) component values are presented, and the resulting frequency response of the load including parasitics is illustrated.

Ideal Load

The design in this thesis is intended for a specific (measurable) load. As a result, the design does not directly address questions of load component tolerances as the aim of the prototype built in this thesis is to verify a theoretical result rather than design a general purpose amplifier. This section describes the characterization and measurement of load parameters. The general specifications for the load were given in the introduction to this thesis, but the actual measured parameters are required for design. The test load was chosen to give easily measurable values using the test equipment available.

A 120 nF capacitor, a 88 μH inductor, and a 5 Ω resistor were chosen for the following reasons. The resonant frequency of 50 kHz is relatively easy to measure with the data acquisition unit used (described in Chapter 4). The Q of the load was chosen not to be too high as to make tuning difficult or have too strong of a filtering effect on the modulated signal while not being so broad that passive components were hard to choose. The load resistance gave a reasonable maximum current (3 Amperes peak) given the rail voltage chosen (16 Volts DC). It is noted that an impedance transformer can be used to modify the load resistance to a different value if desired.

Measuring Resonance and Total Load Resistance

Three devices were used to characterize the load components: an LCR meter, a function generator, and a digital multi-meter (DMM). All measurement equipment used is discussed in more detail in Chapter 4. The LCR meter used only measures parameters at either 120 Hz, 1 kHz, or 10 kHz. Unfortunately, the inductor parasitic resistance as measured from the LCR meter was somewhat questionable, and this inductor ESR measurement was at 10 kHz, not resonance. To adequately model the load, parameter measurements around the frequency range of interest, namely resonance, are highly desired. While a vector network analyzer or impedance analyzer would greatly ease the process (unfortunately neither is cheap), these measurement devices were not accessible. To verify frequency response and determine overall resistance at resonance, an ad-hoc method was constructed that relies on the assumption that parameters do not change characteristics dramatically with increased power levels (as would be the assumption on an impedance analyzer that uses low

power levels). The method used is described in the next paragraph.

The function generator was used to measure the resonant frequency of the load and resistance at this resonant frequency. The following was done. First, the load was attached to the function generator and frequency set to 1kHz at 10Vpp output. Second, the output voltage across the entire load and the voltage across the resistor were monitored. The voltage across the resistor is assumed to give an accurate measure of the current through the load (ignoring resistor parasitics). Third, the frequency is swept and both voltage waveforms are monitored. When resonance is reached, the output voltage measured across the load is at a minimum. This minimum occurs because the load impedance is minimal at resonance, causing maximum current draw and largest voltage drop across the function generator output impedance. Another sign of resonance will be both voltage waveforms are in phase since the load should be purely real (resistive) at resonance. Fourth, while being driven at the resonant frequency, the RMS values of the total voltage across the load and RMS current through the load are measured. The current is obtained by dividing the voltage across the resistor by the resistance value measured using the DMM. The ratio of the RMS voltage across the load and RMS current through the load gives the total resistance.

The method described relies on staying within the acceptable current output range of the function generator and measurable voltage range of the DMM. To explain, if the expected impedance is too large, the current draw will be too low to get a reasonable measurement across the resistor. If the expected impedance is too low, the output impedance will drop too much of the voltage, not to mention that the any output short-circuit protection will most likely kick-in and obfuscate readings. Capacitance and inductance can also be measured using this technique assuming the operating frequency is far enough from resonance that the magnitude of the impedance of the load is dominated by the passive element (assuming the function generator can adequately drive a mostly reactive load).

Results and Admittance Plots

Using the LCR meter, the following results appearing in Table 3.4 were obtained.

Using the function generator, resonance was measured to be approximately 49.6 kHz. Using the DMM to measure voltage across and current through the load at resonance, the resistance was measured to be approximately 5.801 Ω. Therefore, a slight discrepancy exists between the total resistance as measured by the LCR meter and the function generator/DMM. However, the LCR meter measures parameters at 10kHz, meaning a change is expected for the operating frequency. Furthermore, this author's confidence is low in the inductor ESR reading as the LCR meter was

Table 3.4: Key parameters for integrator design

Component	Parameter	Value
Inductor	Inductance	88μH
	ESR	0.3Ω
Capacitor	Capacitance	114nF
	ESR	0.26Ω
Resistor	Resistance	5.051Ω
	ESL	Too Low to Measure

not consistently locking on during the reading. The result obtained using the function generator method was verified with other test loads with high part tolerance as validation of the method and found to be very accurate with specified part values, so the ESR of the entire load, including the load resistors, was determined to be 5.8 Ω.

Two additional notes are made. First, the capacitor ESR reading from the LCR meter comes close to that expected ESR from the manufacturer quoted worst-case dissipation factor and operating frequency, and the temperature derating does not cause dramatically different expected ESR and capacitance values from that measured at the low-power levels. Second, the inductor ESR is somewhat tricky to know at high-power levels since many more effects come in to play including core loss, proximity effects, skin effect, and Eddy current losses to name a few [9]. Therefore, the inductor ESR readings from both methods used above should be interpreted with the knowledge that high-power level interactions may cause the inductor ESR to stray during operation.

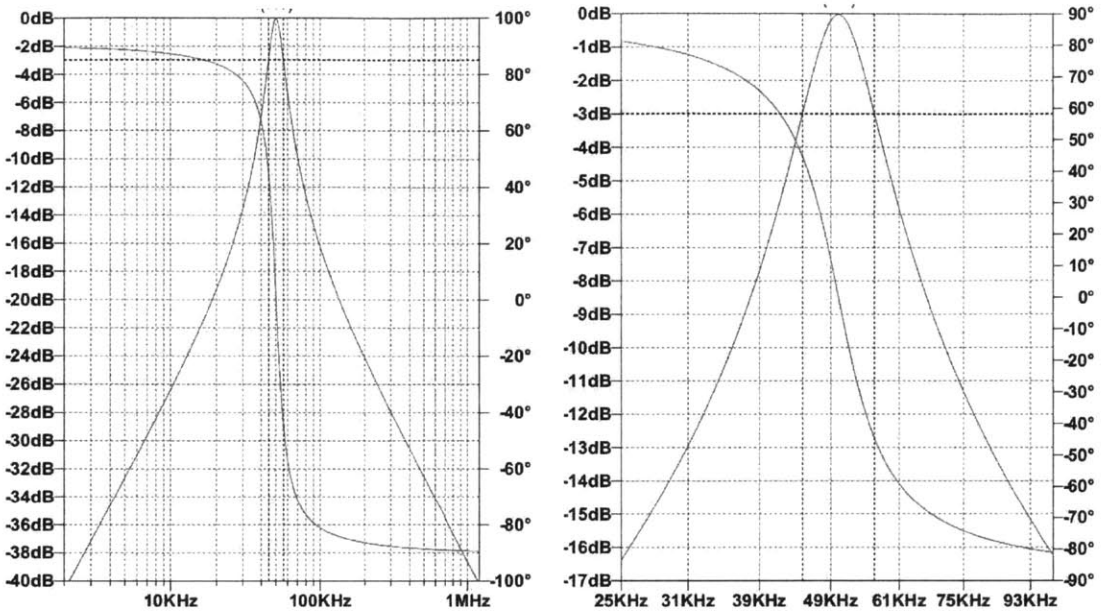
The admittance of the load given the above designated component values is shown in Figure 3.10.

3.1.3 Power Board

In this section the output topology is presented first, the switches are presented second, the switch drive circuitry is presented third, and the power board losses are presented fourth.

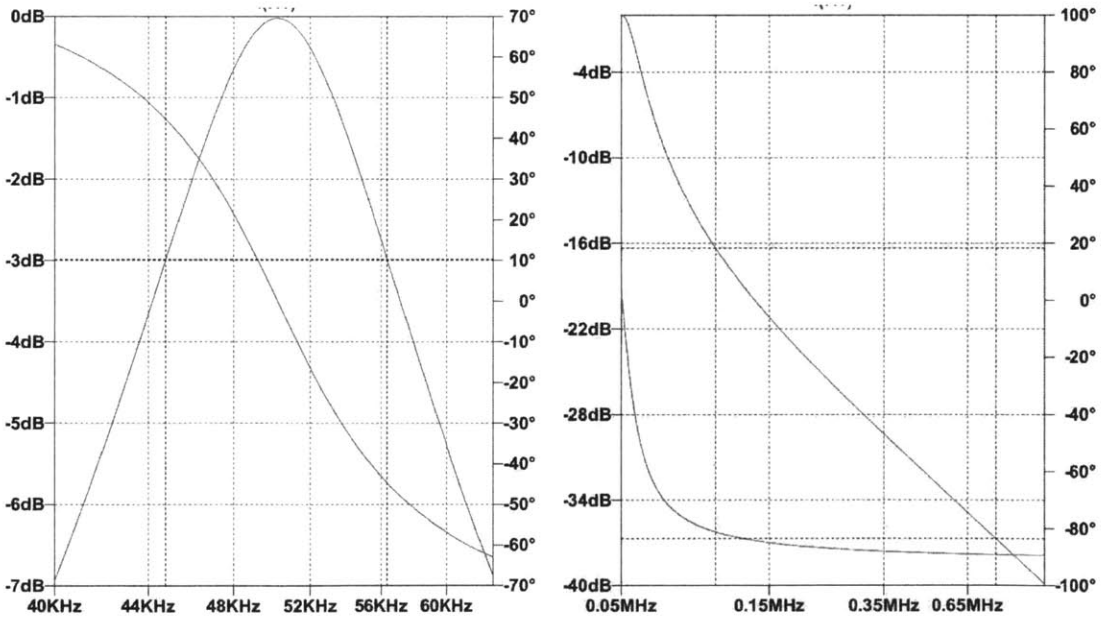
Topology Choice

The full-bridge configuration as shown in Figure 3.11 is used. This configuration allows three voltage levels across the differential drive output as compared to a single half-bridge which only allows two discrete voltages [9]. The full-bridge topology is really two half-bridge configurations with their respective output attached to either side of the load, thus creating a differential output drive to the load itself. While various drive sequences are available, the drive waveform in Figure 3.11 is used. This waveform gives an asymmetry in the nominal on time for the top and bottom switches. At



(a) Load admittance broad view.

(b) Load admittance close view.



(c) Load admittance very close view.

(d) Load admittance from the carrier to 75kHz.

Figure 3.10: The magnitude of the admittance is measured in decibels relative to the maximum admittance (at resonance) with corresponding values on the left side of the vertical axis. The phase of the admittance is the measured in degrees relative to the phase at resonance (when the admittance is purely resistive) with corresponding values on the right side of the vertical axis. The frequency values appear on the bottom of the horizontal axis. The dashed, bold line at the top of the graph is the -3 dB magnitude reference.

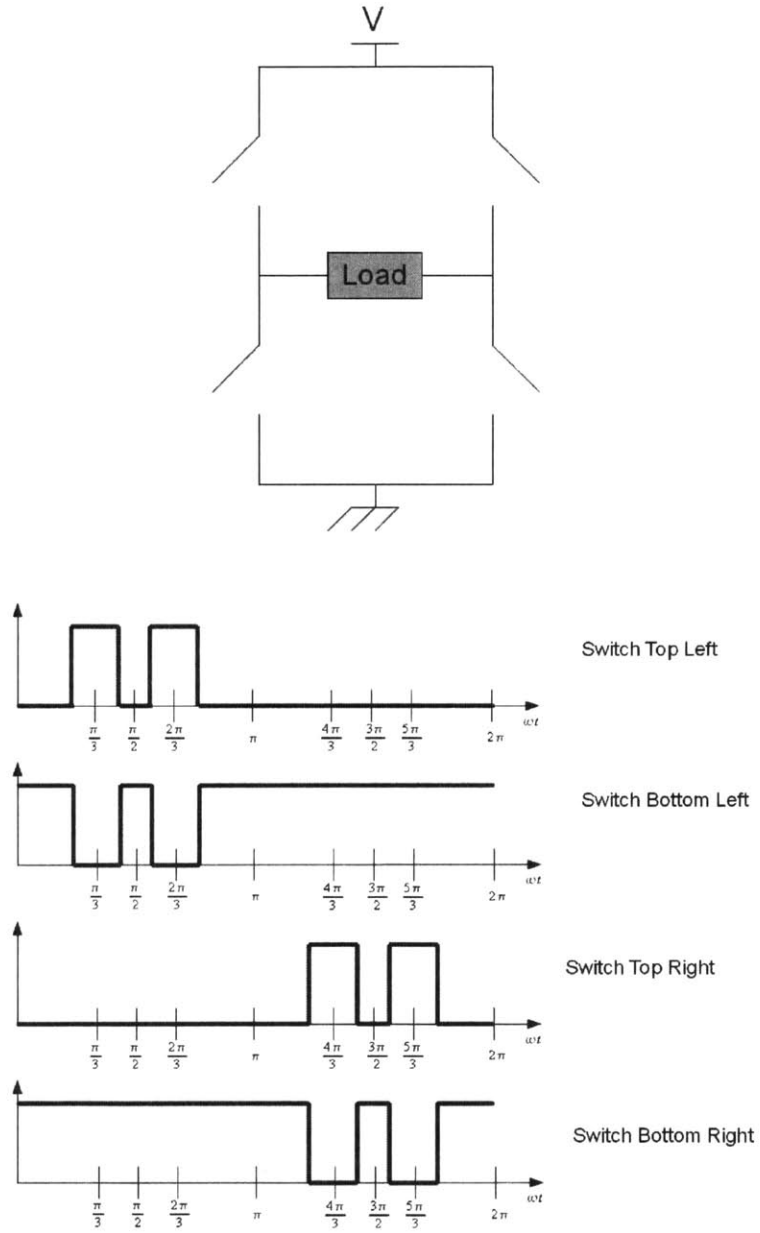


Figure 3.11: Full-bridge switch scheme. Control waveforms are shown. High level voltages correspond to the switch being closed (conducting current), and low voltages correspond to the switch being open (not conducting current).

maximum duty cycle, the top switches are on for one-third of the carrier period while the bottom switches are on for two-thirds of the carrier period. As a result there will be greater conduction loss in the bottom switches than the top switches. Furthermore, only the bottom diodes will conduct during a given switch transition if the drive frequency is at load resonance. If the drive frequency is far enough away from resonance, there will be a phase shift between the drive voltage and current draw such that the polarity of the current during a switch transition could actually change. The phase shift requirement would have to be ± 30 degrees. How far away from resonance this shift will occur depends on the load Q. Further consideration of drive far from resonance is not considered in this thesis.

Switch Selection

While many options exist for power semiconductor switches (e.g. power MOSFETs power BJTs, SCRs, IGBTs, etc.), switching frequency and required power output generally guide semiconductor switch choice [29]. In general power bipolar junction transistors are typically too slow for fast switching without external circuitry to prevent saturation (removing stored charge from saturation is the primary reason BJTs are so slow), though designs using power BJTs have been published up to at least 400kHz. IGBTs are typically outperformed by For the switching frequency range and power levels used in this thesis, a MOSFET is a strong choice [29]. Also, it is noted that the on-resistance has a positive temperature coefficient (which makes the switch attractive for paralleling applications). Given the voltage levels, Schottky diodes can also be used to ease the power loss in the MOSFETs from body-diode conduction.

Since a full-bridge topology is used, the choice of n or p-type FETs must be made. The primary trade off in a full-bridge (or half-bridge) topology regarding MOSFET channel type is required drive circuitry versus switch performance [26]. A p-channel MOSFET on the high-side can be easily driven just as the low-side n-channel. However, p-channel MOSFETs operate with holes as the majority carrier which have lower mobility than electrons, meaning that the on-resistance of the p-channel MOSFETs is inherently higher (generally 2 or 3 times higher [31],[32]). Thus n-channel MOSFETs are chosen for both top and bottom switches.

The IRLM0030 power MOSFET was chosen for the power switch in this design. The IRLM0030 comes in an SOT-23 package which has a thermal resistance of 100 degrees Celsius per Watt. The reason for choosing such a high thermal resistance was for validation of design efficiency results since any error in power dissipation will be easily felt by touch. In practice, assuming space was not tantamount to other parameters, an SOIC-8 package or other comparable part would potentially be a

wiser choice as it is more forgiving if heat is generated in the switch due to power loss (larger packages or packages with exposed metal such as the D2PAK have much lower thermal resistance [30]). The IRLM0030 has a small gate charge requirement for turn-on as well, meaning that fast switch transitions are possible with the proper drive circuitry (discussed shortly), can handle the expected current draw, and has a large enough reverse-breakdown voltage for the design requirements.

Gate Drive

First, the required current capability of the gate driver is calculated. Given the choice of the IRLM0030 n-channel MOSFET, calculating the required gate driver current capability requires three parameters: the total gate charge required for a transition, the gate-to-source voltage applied for a transition, and the desired time to transition [25]. The resulting calculation gives

$$\begin{aligned} I &= \frac{Q_G}{t} \\ &= \frac{6 \text{ nC}}{50 \text{ nS}} \\ &= 120mA \end{aligned}$$

where the gate charge was determined from the MOSFET data sheet given the gate-to-source voltage of 12 Volts. This calculation ignores explicit load capacitor knowledge but is typically still accurate for MOSFETs of interest [25]. The determined current requirement must be increased above this factor since the current drive will be neither linear nor constant [25]. Therefore, a peak current capability of 200 mA should be more than sufficient.

Next, the full-bridge topology with two n-channel MOSFETs per half-bridge necessitates high-side n-channel drive capability. This requirement demands a floating voltage supply for the top n-channel MOSFETs of the full-bridge. Four standard choices used to meet the high-side MOSFET requirement include charge pumps, galvanic isolators (transformers), digital opto-couplers, and bootstrapped capacitors [26]. The bootstrap capacitor method is chosen for this design. This method is the most common employed due to low cost, meaning many integrated-circuit implementations are readily available.

The IR2011 gate driver is chosen as the gate driver IC for driving each separate half-bridge of the full-bridge (the full-bridge requires two IR2011 ICs). The IR2011 delivers 1 Ampere of current for both source and sink action with a rated propagation delay of approximately 80 nS (these specifications are under specific testing conditions, of course). Choosing a gate driver with the

ability to deliver more current than necessary may come at increased monetary cost but allows for more drive flexibility when fine-tuning the prototype to address parasitic-induced EMI. The IR2011 requires two inputs which control the top and bottom MOSFETs independently, which will be driven by the signals generated by the digital logic circuitry in this design. The IR2011 requires an external bootstrap diode and bootstrap capacitor. Choosing these components can be aided by the discussion in [27]. The diode chosen is the Vishay S1G-E3 (1A, 400V rectifier), and the capacitor value of 1 μF is used.

External gate resistors may be required during prototyping to address variations in parasitic inductance [25]. Determining the initial value used for the external gate resistors is done as follows. First, the gate driver output resistance is determined from the data sheet (if the information is not directly stated, it can be measured on the lab bench). Second, the MOSFET gate resistance is determined from the data sheet. Third, the expected equivalent gate capacitance for the driven MOSFET is determined by taking the total required gate charge divided by the final gate-to-source voltage. Fourth, given the desired rise (or fall) time of the gate transition, the standard step response of a voltage source driving an RC load is used. This process gives

$$V_{GS} = V_F e^{-\frac{t}{R_{EQ}C_{EQ}}}$$

where V_{GS} is the gate-to-source voltage, V_F is the final gate voltage, R_{EQ} is the sum of the driver output resistance, the input gate resistance, and the external gate resistor, and C_{EQ} is the equivalent gate capacitance. The rise time is typically defined as the time it takes the gate-to-source voltage to rise from 10% of the final value to 90% of the final value. Plugging in two time values with known voltage levels gives

$$\begin{aligned} .9 &= e^{-\frac{t_{final}}{R_{EQ}C_{EQ}}} \\ .1 &= e^{-\frac{t_0}{R_{EQ}C_{EQ}}} \end{aligned}$$

where t_final is the time at 90% voltage, t_0 is the time at 10% voltage, and the final voltage has been divided out. The rise time, t_r, is then defined as t_{final} plus t_0. Dividing the two equations and rearranging gives

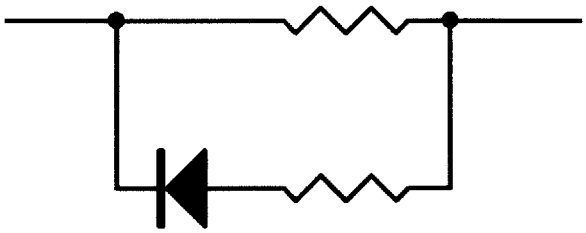


Figure 3.12: External gate drive delay circuitry. The left side of the circuit is connected to the switch driver, and the right side is connected to the switch. Typically the resistor in series with the diode is smaller than the other resistor to allow for faster turn-off than turn-on.

$$\begin{aligned} R_{EQ} &= \frac{t_r}{C_{EQ} \ln 9} \\ &\approx \frac{t_r}{2.2 C_{EQ}} \end{aligned}$$

from which the external gate resistance is determined to be $R_X \approx \frac{t_r}{2.2 C_{EQ}} - R_{GD} - R_{IG}$ where R_{GD} is the gate driver output resistance and R_{IG} is the internal gate resistance of the MOSFET.

The required external resistance starting value for this design is now determined. The data sheet for the IR2011 does not explicitly state the output resistance of the driver, but the number can be estimated given stated parameters and associated operating conditions. The resulting resistances are 17 Ω for sourcing and 10 Ω for sinking. The value of the gate-to-source voltage is set at 12 Volts since this voltage is a common number for designs as determined from looking at common gate driver ICs. The input resistance of the IRLM0030 is 2.3 Ω as stated explicitly in the data sheet. The equivalent gate capacitance is given as $\frac{6n}{12} \approx 500$ pF. The desired rise time is 50 ns, which gives a required external gate resistance of 33 Ω using the lower sink resistance as a worst-case.

The value set by the analysis above does not account for parasitic inductance and thus is only a starting value. Furthermore, the required rise and fall times may be different to achieve acceptable EMI performance, so standard practice is to use the circuit shown in Figure 3.12. The diode direction typically faces away from the gate because faster discharge times relative to charge times are usually desired. In addition, the top driver will most likely see a larger parasitic inductance than the bottom switch because the current has to travel through traces and through the lower MOSFET as opposed to the bottom MOSFET which has the ground plane as the return path. Therefore, the top MOSFET will typically have to be turned on a little slower than the bottom switch.

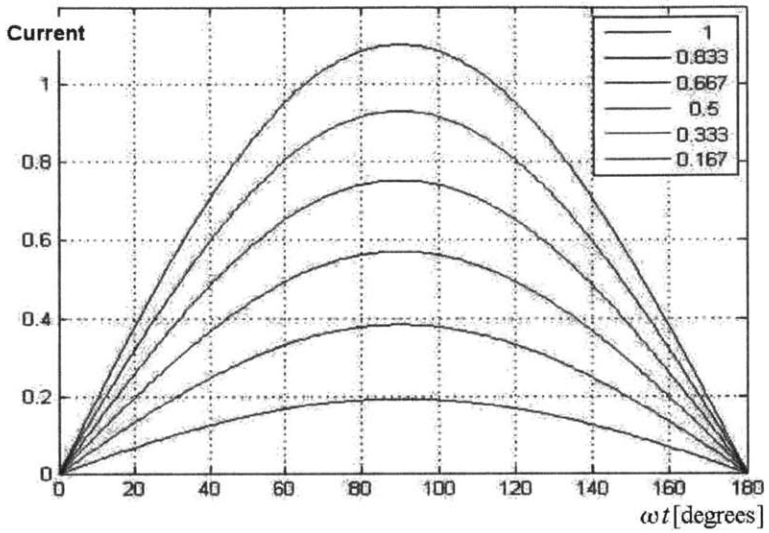
Loss Calculations

This section is organized as follows. First, the operation conditions are determined. Second, the expected MOSFET losses are calculated. Third, the gate driver losses are calculated. Fourth, the total losses are calculated and summarized.

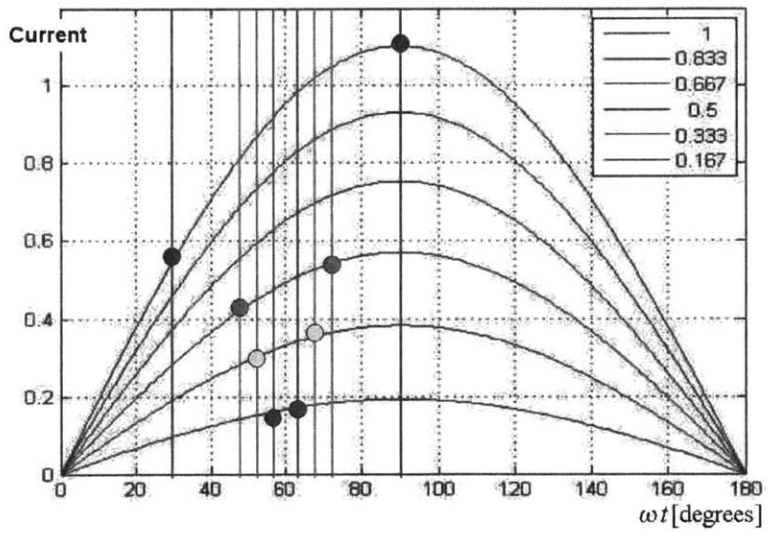
To start, the operating conditions are discussed. The maximum voltage seen across a switch is 16 Volts, which is the full-bridge supply voltage. The effective switching frequency is 100 kHz (two times the carrier frequency). Specification of the current during switching transitions is a bit more complicated since the current draw at transitions varies with nominal duty cycle. To determine the expected current, the duty cycle was varied and corresponding current was determined through simulation. Variation of the duty cycle is in a static sense, i.e. the duty cycle is set, current is determined, and then a new duty cycle is set. The resulting simulation for current levels is shown in Figure 3.13. The top illustration in Figure 3.13 shows half of a carrier cycle with varying duty cycles going from large at the top to small at the bottom of the graph. The bottom illustration in Figure 3.13 shows the current values when the actual transition occurs for various duty cycles with large duty cycles intersecting the top waveform and low duty cycles intersecting the bottom waveform. As the duty cycle falls, the two corresponding points on the plot converge and their average level falls as well. Thus the worst case current draw during a switching transition occurs at large duty cycles, which follows intuition. A point worth noting is that the worst case current draw does not occur at a duty cycle of unity but at just below unity since unity duty cycle implies the transition at peak current draw never occurs. This discrepancy was discussed in the section on digital circuitry of this chapter but will be ignored for worst case analysis presented in this section.

To get a concrete number for the worst case current draw, it is noted that the PBPWM waveform will be filtered by the resonant load. When the drive frequency of the PBPWM is at the resonant frequency of the load, the carrier frequency will dominate. The amplitude of this component is approximately 1.1 times the voltage rail as shown in Chapter 2 when discussing the Fourier coefficients of the PBPWM waveform with duty cycle equal to one. This relationship gives 17.6 Volts. At resonance, the inductor and capacitor reactance cancel leaving the impedance set by the resistance. The maximum current amplitude is then determined to be $\frac{17.6V}{5.8\Omega} \approx 3$ Amperes. Allotting for 1% of the cycle period to be in the transition phase would give 30 ns, so a safer bet is to assume the rise and fall time are equal and around 50nS.

Next, the expected MOSFET losses are determined. Three primary loss considerations are taken into account: conduction loss, dynamic losses, and body diode loss. One other loss mechanism



(a) Fundamental harmonic of load current with varying nominal duty cycles.



(b) Expected current at switch transitions for various nominal duty cycles. Note there are two intersections per duty cycle grouped by dot shading in the graph. Verticle lines at dot intersection occur at the corresponding duty cycle.

Figure 3.13: Determination of current at various duty cycles. Load current is normalized to a 1 Ω resistive load. Waveforms shown are for half of a carrier cycle. Maximum amplitude is 1.1 following analysis of the Fourier coefficient values discussed in Chapter 2 for the PBPWM waveform.

Table 3.5: Summary of Key Operating Conditions

Parameter	Value	Units
Rail Voltage	16	Volts
Peak Voltage (max output)	17.6	Volts
Peak Current (max output)	3	Amperes
RMS Current (max output)	2.1	Amperes
Rise Time	50	nano-seconds
Fall Time	50	nano-seconds

assumed negligible but listed for completeness is output capacitance loss (Coss loss) [33]. A thermal review will be given at the end of this section to account for expected temperature rise.

The conduction loss occurs because a switch has non-zero resistance while conducting. The standard design approximation is to assume the RMS current is delivered during the on-time of the switch action [34]. For a given time period, the switch is on for the duty cycle times the cycle period. Thus the conduction loss is given as

$$P_c = I_{RMS}^2 R_{on} D$$

The given worst case current draw is 2.1 Arms, the specified on-resistance for our gate drive is 27 mΩ, and the top switches will be on for one-third of a cycle (worst case) while the bottom switches will be on for two-thirds of a cycle (worst case). This relationship gives

$$\begin{aligned} P_{\mathrm{cT}} &= (2.1)^2 \times \left(27 \times 10^{-3}\right) \left(\frac{1}{3}\right) \\ &\approx 40 \text{ [mWatts]} \\ P_{\mathrm{cB}} &= (2.1)^2 \times \left(27 \times 10^{-3}\right) \left(\frac{2}{3}\right) \\ &\approx 80 \text{ [mWatts]}. \end{aligned}$$

Dynamic losses are now discussed. There are two primary losses associated with dynamic losses: switching transition losses and body-diode reverse recovery losses [34]. These are calculated in the following.

The switching transition loss approximation typically used assumes a linear rise and fall of voltage and current such that both current and voltage reach their maximum or minimum value at the same time [33]. The power lost is then taken as the time average of the product of voltage and current over

these intervals and then multiplied by the switch frequency. This relationship gives the following formula

$$P_s = \left(\frac{1}{2}VI_{on}t_{on} + \frac{1}{2}VI_{off}t_{off}\right)f_s$$

where V is the rail voltage, I_{on} and I_{off} are the current during the turn on and turn off transitions, t_{on} and t_{off} are the on and off time, and f_s is the switching frequency. For this design, V is 16 Volts and the rise and fall times are each 50 ns. For a given switch, there are two turn-on transitions and two turn-off transitions for the PBPWM waveform. For the worst case of large duty cycles, each switch will see one on and one off transition at the lower switching current and one on and one off transition at the higher switching current. Assuming the worst case is $0.5 \times I_{max}$ for the lower current and I_{max} for the higher current gives

$$\begin{aligned} P_s &\approx \left(I_{on}\left(t_{on}+t_{off}\right) + I_{off}\left(t_{on}+t_{off}\right)\right)\frac{1}{2}16f_c \\ &\approx \left(I_{on}+I_{off}\right)\frac{1}{2}2\times 50\times 10^{-9}16f_c \\ &\approx (1.5I_{max})\times 50\times 10^{-9}\times 16\times 50\times 10^{3} \\ &\approx 180 \text{ [mWatts]} \end{aligned}$$

The body diode gives a loss of

$$P_{bd} = 2\times\left(\frac{1}{2}V_F Q_{rr} f_{sw}\right) + V_F I_{pk} T_{on} f_s$$

as derived in [34]. Given the topology, only one of the bottom body diodes will conduct during a given dead time. This conduction will occur four times per carrier period, which means the effective switching frequency is 200kHz. Using the data sheet, this relationship gives approx 5.2mW loss. The on time is approx 4 times 10nS (worst case) and the carrier period is 20uS. The forward voltage is 1 Volt and the current is worst case 3 A, so this number is 6mW (more or less can be considered negligible).

A thermal review is now presented. Up to this point, the worst case loss for a 16 Volt drive into 5.8 Ω is estimated to be 266 mWatts for the lower switches and 220 mWatts for the top switches.

However, the design has assumed room temperature and has not yet considered temperature rise from power dissipated. Thus, an iterative step is necessary to confirm the conservative estimation above are not grossly inaccurate at higher temperature operation.

The expected temperature increase given a thermal resistance of 100 degrees Celsius per Watt and the calculated power dissipation of 266 mWatts gives 27 degrees Celsius rise above ambient for the bottom switches (only the bottom switches are considered since this situation is a worst case scenario). This relationship translates to a 25% increase in the on-resistance according to the data sheet. The appropriate MOSFET parameters affected by increased temperature are now examined. All figure references in the remainder of this paragraph are to the IRLM0030 data sheet. The gate voltage used in this design in 12 Volts, so figures 1, 2, and 3 in the data sheet can be ignored. Figure 4 indicates the on-resistance will rise to 1.2 times the room temperature value, giving approximately 32 mOhms. Figures 4 through 7 are not relavant. Figure 8 is not considered due to the switching frequency, maximum drain-to-source voltage, and maximum current of this design. Figure 9 indicates the maximum operating current of 3 Amperes peak is still within the capabilities of the transistor. Figure 11 can be ignored since the nominal duty cycle can be considered $D = 0.50$ at a repeated rate disregards the single pulse test case. Figures 12 and 13 are just restatements of the on-resistance change and are already taken into account. Figure 15 indicates expected voltage transients on the gate-to-source voltage are still acceptable.

Therefore, the only considerations necessary given the expected temperature increase are the increase in power dissipation due to higher conduction loss via higher on-resistance. This relationship gives a 20% increase in conduction loss equating to an extra 20 mW for the bottom switches. This result demonstrates the power loss will not change considerably with the higher conduction loss, and the design calculations do not need to be completely redone. To account for this power increase, an additional 20 mWatts is added to the bottom switches, and an additional 10 mWatts is added to the top switches.

The change in voltage breakdown given increased temperature is considered next. Since the rise is 27 degrees Celsius, the voltage breakdown depredation is 0.8 Volts equating to 29.2 Volts for breakdown. Therefore operation at 16 Volts is still very safe. The change in maximum power dissipation also shows that 0.8 Watts is the limit for the expected temperature increase, so the power rating is also good. For later measurement purposes, it is noted that the case temperature should be anywhere between 5 and 10 degrees below the junction temperature, so switch junction temperature determination should take this relationship in to account [35].

Now, the expected gate driver losses are determined. The gate drive losses come from four major

sources: the bootstrap diode, the bootstrap capacitor, the gate charge required for MOSFET turn-on, and losses associated with the gate driver IC, e.g. shoot-through in the internal IC package [26]. The dominant component will be the MOSFET gate charge which must be sourced to and sunk from the gate for each turn-on and turn-off, respectively, of the MOSFET. The formula used for this calculation is

$$P_{gd} = 2 \times \left(\frac{1}{2} Q_G V_{GS} f_s\right) \tag{3.2}$$

as shown in [34].

For gate charge of V_{GS} of 12, and f_s of 100kHz (neglecting temperature effects and distribution of loss, i.e. loss to certain resistors, and neglecting inductive effects of trace parasitics), we get approximately 7.2 mWatts of dissipation per switch. Also, it is noted that since the MOSFET gate charge is temperature independent, there does not need to be a readjustment of the switching frequency analysis. Since the majority of the gate-drive power is dissipated in the external gate resistors, these numbers do not need to be included in the power MOSFET loss calculations. Therefore, the total power loss contribution from the gate drive operation is 28.8 mWatts. The gate charge loss goes in to the aggregate loss calculation, but the gate charge does not limit the speed if a large enough gate driver current is available. Maximum allowable current is limited for EMI constraints, but this limitation falls with lower parasitic inductance.

Finally, the total losses are determined and summarized. For the top switches, expected conduction loss is 50 mWatts, expected switching loss is 180 mWatts, and expected body diode loss is zero Watts. For the bottom switches, expected conduction loss is 100 mWatts, expected switching loss is 180 mWatts, and expected body diode loss is 4 mWatts. For the gate drivers, the expected loss due to driving gate charge is 7.2 mWatts per switch, or 14.4 mWatts per gate driver IC. Again, the loss to the gate charging is dissipated primarily in the external gate resistor. The total losses for the output stage consisting of the gate drivers and the MOSFETs is approximately 1.06 Watts (before accounting for bypass capacitor losses). The expected output power to the load is $2.1^2 \times 5.8$ which is approximately 25.6 Watts. Thus, the expected worst-case efficiency is approximately 95.8% (again this number does not account for bypass capcitor losses). The losses are summarized in Table 3.6.

Table 3.6: Summary of MOSFET Power Loss

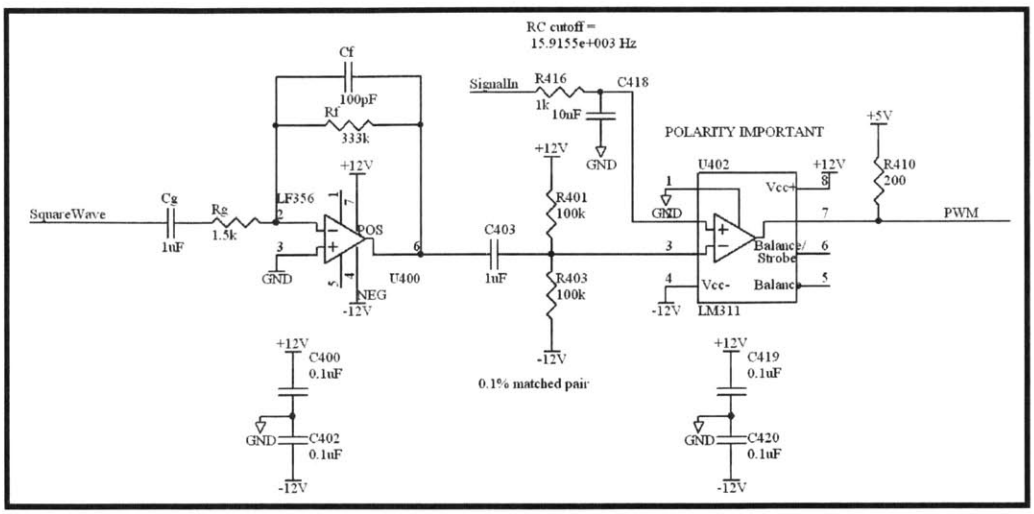
Location	Loss Type	Amount (mWatts)	% of Total Loss
Top MOSFET	Conduction	50	21.7
	Switching	180	78.3
	Body Diode	0	0
	Total	230	
Bottom MOSFET	Conduction	100	35.0
	Switching	180	62.9
	Body Diode	6	2.1
	Total	286	
Single Gate driver	Gate Charging	14.4	
	Bootstrap Capacitor Charging	0	
	Bootstrap Diode Conduction and Reverse Recovery	0	

3.2 Board Schematics and Prototype Construction

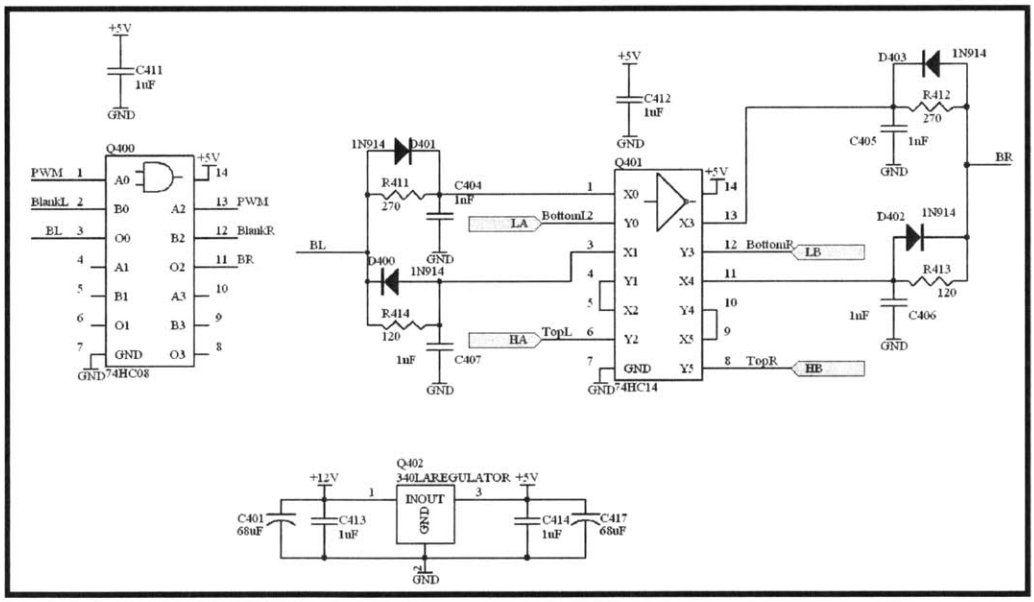
In this section, the final schematics and prototype layout are presented and discussed. The control board is presented first and the power board second. The control board connects to a TMS320F28027 microcontroller evaluation board through Sullen-pin connectors on the bottom of the control board PCB, which is also where the modulating signal input is connected. The control board and power board connect through Sullen-pin connectors as will. This connection between the control and power boards was made for prototyping ease but also allowed for good separation between low and high power areas. The control board was laid out for separation between the analog and digital circuitry in an attempt to minimize ground noise. The power board contains only digital signals (though the signals are still really analog since the group of all possible pulse-width values forms a continuum and not a set of discrete values).

Control Board

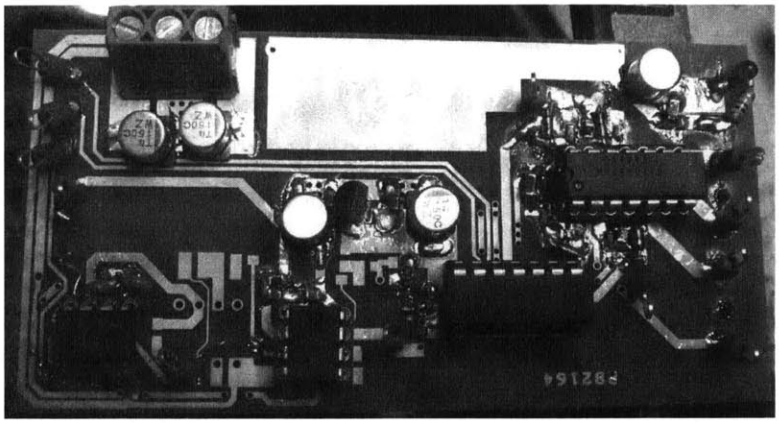
The final schematic for the control board appears in Figure 3.14. The square-wave input and blanking signals were generated using a TMS320F28027 evaluation board and are labeled "Square-waveTMS", "BlankL", and "BlankR". U400 is the LF356 integrator, U402 is the LM311 comparator, Q400 is the digital and gate IC, Q401 is the digital inverter gate package. All capacitors are ceramic surface mount. The components surrounding Q401 form the dead time generation circuitry. The diodes are standard 1N914 fast diodes that allow for setting the rising-edge and falling-edge dead time separately. Q402 is a linear regulator used to provide the 5 Volt supply for the digital logic circuitry. C403, R401, and R403 form the DC bias offset removal from the integrator.



(a) Integrator and comparator.



(b) Digital logic and deadtime circuitry.



(c) Picture of populated board.

Figure 3.14: Control board schematic and populated board picture.

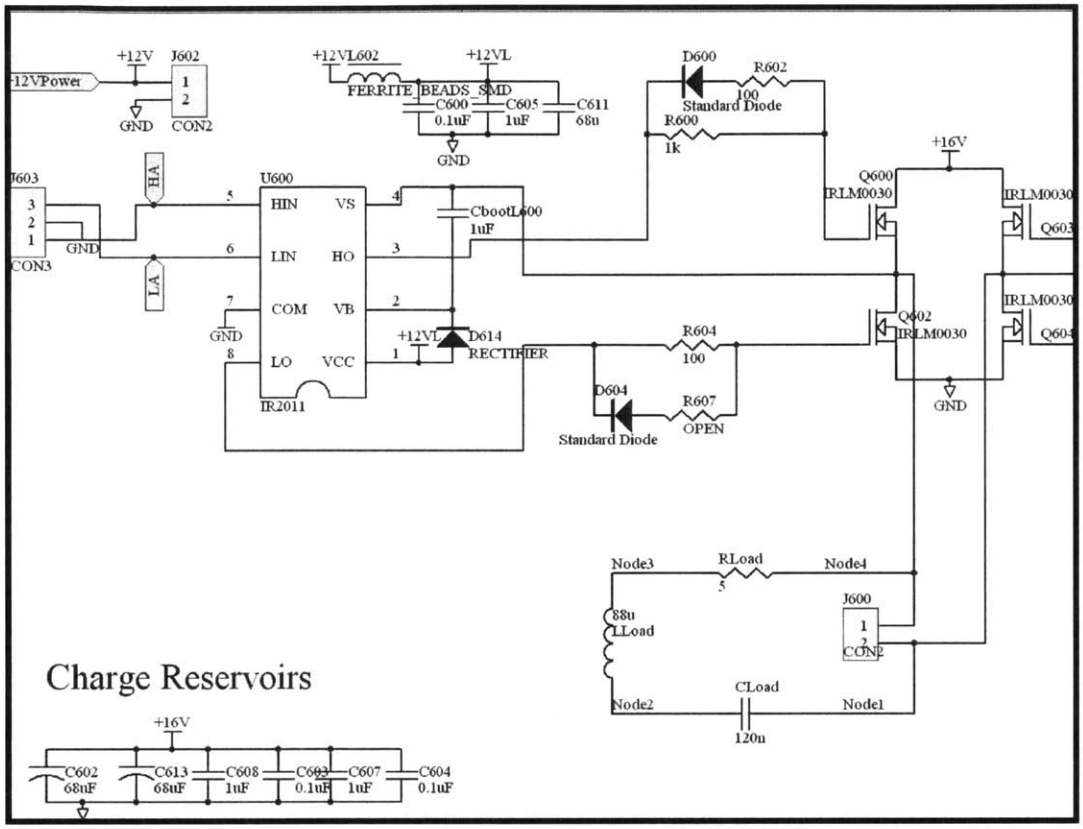
The final PCB control board is shown in Figure 3.14. The $\pm 12V$ power supply is connected in the top left. The TMS320F28027 microcontroller signals and input modulating signal come in under the board on the far left. The integrator is in the bottom left corner. The comparator is to the right of the integrator. Above the comparator is the 5 Volt regulator. To the right of the integrator is the digital and gate IC. Above the and gate IC is the inverter gate IC. The top right is the power connection for the gate drivers on the power board (underneath the control board). The gate drive signals are underneath the far right of the board.

Power Board

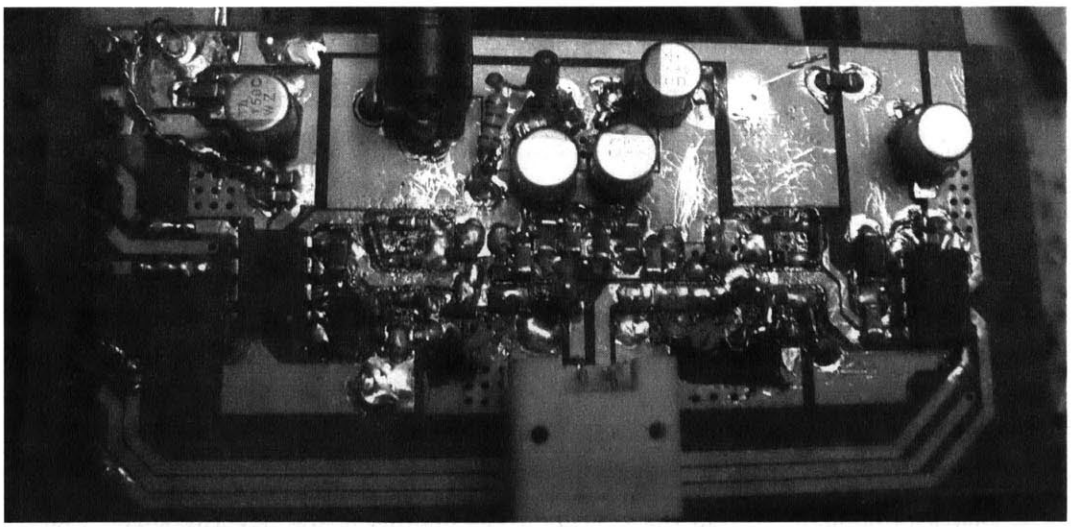
In Figure 3.15 only half of the power board circuit is shown since the circuit is symmetric. U600 is the gate driver IC and Q600, Q601, Q602, and Q603 are the output MOSFETs. CbootL600 is the 1 μF bootstrap capacitor that acts as the floating supply for the high-side drive. D614 is the ultra-fast bootstrap rectifier.

The far left of the board connects to the control board. The positive 12 Volt power supply for the gate drivers is delivered from the top left connection to the control board. Small ferrite beads are placed between the control board supply and the gate driver supply connection. The IR2011 gate drivers are the only two 8-pin DIP ICs on the board. The MOSFET switches are located in the center of the board very close to the charge reservoir capacitors. The top of the board is the main power input of 16 Volts. Note that this supply is a different than the gate driver 12 Volt supply from the control board. The bottom connector is a standard BNC jack that connects to the load.

Regarding parasitics, the layout of the power board is **absolutely critical**. The charge reservoir capacitors must be placed as close as possible to the drains of the top MOSFETs. Furthermore, a large number of vias are placed at the ground connection of these charge reservoir capacitors and at the source connection of the bottom MOSFETs. This number of vias is used to ensure minimal inductance between the top and bottom of the full-bridge as to dramatically reduce EMI. Furthermore, the source of the top MOSFET and the drain of the lower MOSFET are placed as close as possible with as much copper connecting the two as possible. Again, this layout is absolutely critical to reduce EMI from parasitic inductance. The goal of taking care in full-bridge layout is that lead inductance from the SOT-23 is the limiting factor. For the SOT-23 package, a reasonable number to assume is 1 nH of inductance. The formulas used to calculate via inductance and capacitance are



(a) One-half of power board schematic.



(b) Picture of populated board.

Figure 3.15: Power board schematic and populated board picture. Note only half of power board schematic is shown due to symmetry of the circuit.

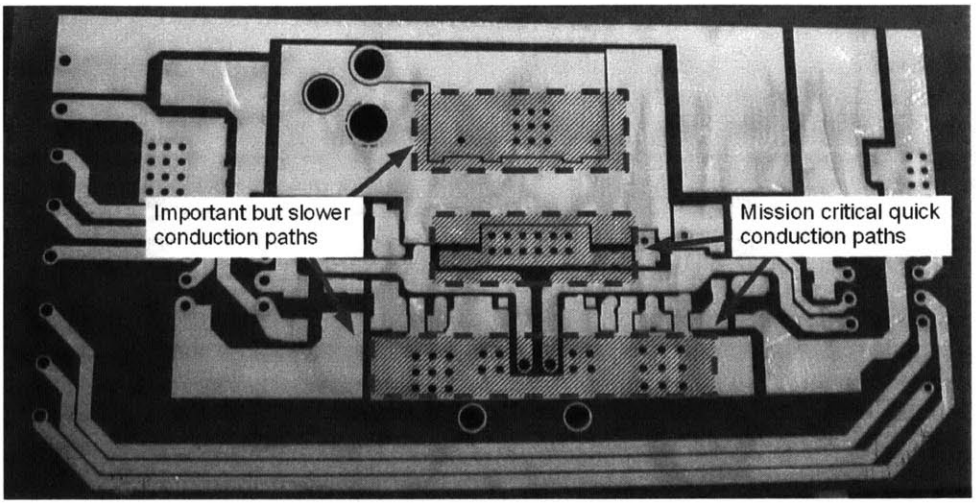


Figure 3.16: Board Design Parasitics

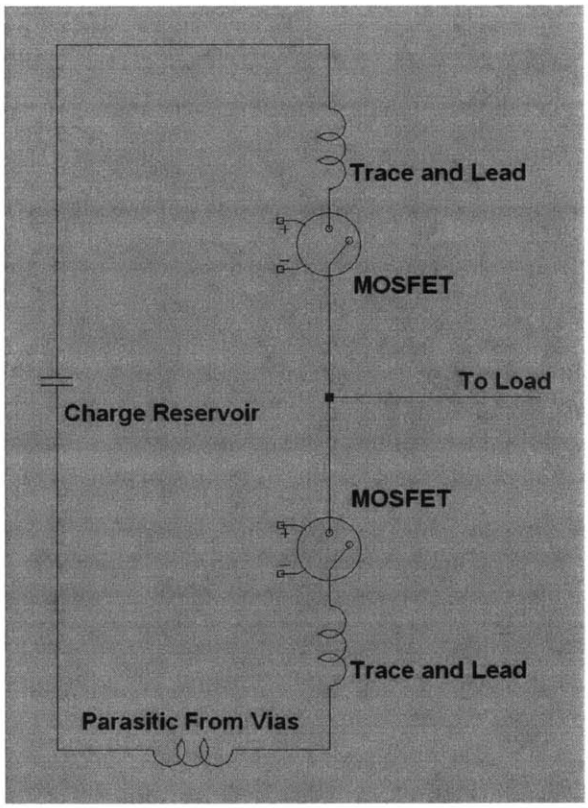


Figure 3.17: Vital Parasitics to Consider

$$L = 2T\left[\ln\frac{4T}{d} + 1\right] \text{ nH}$$
$$C = \frac{0.55\epsilon_r TD}{H - D}2T \text{ pF}$$

where H is the diameter of clearance hole, D is the diameter of the pad surrounding the via, d is the diameter of the via, T is the thickness of the PCB, and ϵ_r is the dielectric constant [28]. The formulas above assume dimensions given in centimeters. If variable definitions are unclear, please see [28]. For the given vias used, the inductance is approximately 1 nH per via. To put this number in perspective, a 10 Ampere transition in 10 ns causes across the via causes a voltage of approximately 1 Volt, which, when considering a 24 Volt rail, may be substantial for the design. Therefore, numerous vias in parallel were used to reduce the combined via inductance, thus making the MOSFET SOT-23 lead inductance the dominant parasitic. As an additional note on vias, there is not a real penalty (at least known to this author) for having more vias than not except in excessive cases where via total exceeds, say, 25 vias per square-inch which is where PCB manufacturers may start charging additional fees per via for tool wear. A final point regarding parasitic inductance is that the parasitic connection to the load is not crucial since there is a large inductor in the load that will appear in series with any other inductive values, thus dominating final inductance.

Modifications to the paper design are now discussed. The specific areas of change are the integrator component values, the dead-time resistor and capacitor values, and the gate resistance values. In the integrator, the input resistor was modified to be 1 kΩ instead of 1.5 kΩ since the microcontroller output voltage was slightly less than 3.3 Volts. In the dead-time circuitry of the digital logic section, resistors were initially set to be 470 Ω, and capacitors were set to be 1 nF. These component values allowed for extra dead-time above paper design to ensure shoot-through would not occur. The values were then scaled back to reach a compromise between undesirable dead-time and shoot-through prevention. As stated earlier in this section, the top gates required extra dead-time on the rising edge due to the increased inductance. The final values used were 270 Ω resistors for the top gate delay and 120 Ω resistors for the bottom gate delay. Both top and bottom delay capacitors were set to 1 nF. For the gate resistor values, the bottom gates worked well with 100 Ω, which is relatively close to the predicted 33 Ω, for both rise and fall action. The top MOSFETs worked well with 100 Ω for the falling edge but required adjustment for the rising edge to achieve acceptable EMI and were set at 1 kΩ, which is reflected in Figure3.15. This need for adjustment to the rise time agrees with expectation of higher parasitic inductance for the top MOSFET conduction paths.

Chapter 4

Measurements and Measurement Techniques

In this chapter, experimental measurements are presented first so as to "get to the point." Next, measurement method explanation and validation is given for procedural justification. The more detailed chapter organization is as follows. First, experimental measurements are shown including time waveform measurements, spectral measurements, and efficiency measurements. Second, measurement techniques are explained including efficiency determination, analog signal conditioning, and digital signal processing. Table 4.1 lists the measurement equipment and function generator used to gather data.

Table 4.1: Measurement Equipment and Function Generator Listing

Manufacturer	Model Number	Function
Agilent	34410A	Digital Mult-meter (DMM)
Tektronix	TDS2024B	Digital Oscilloscope
Tektronix	2445A	Analog Oscilloscope
National Instruments	NI USB-6251	Data Acquisition Module (DAQ)
Agilent	33220A	Function Generator

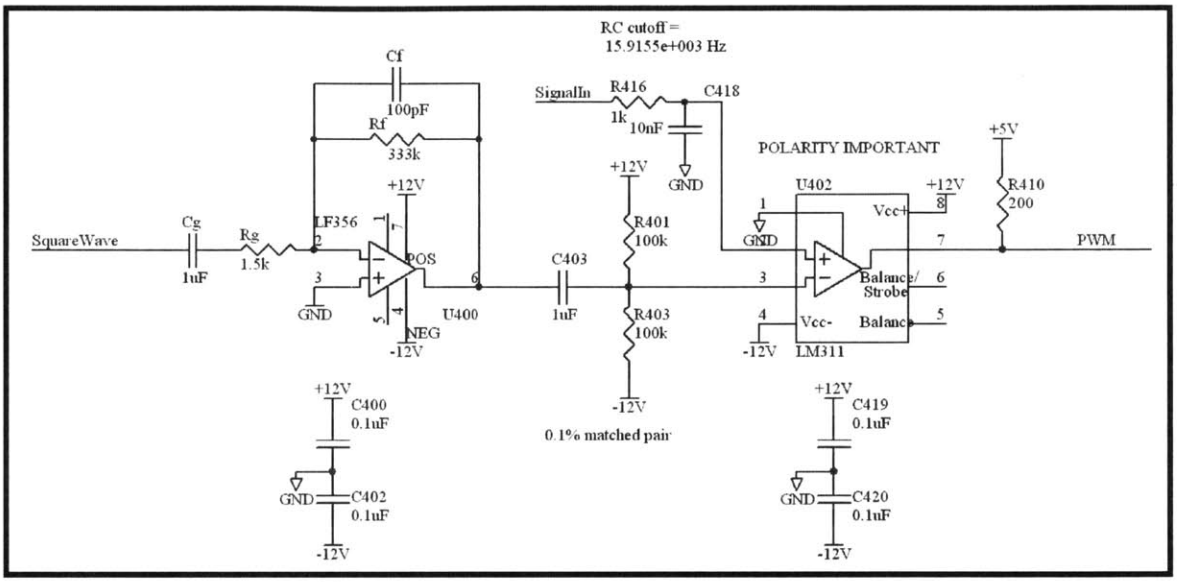
4.1 Measurements

4.1.1 Time Waveforms

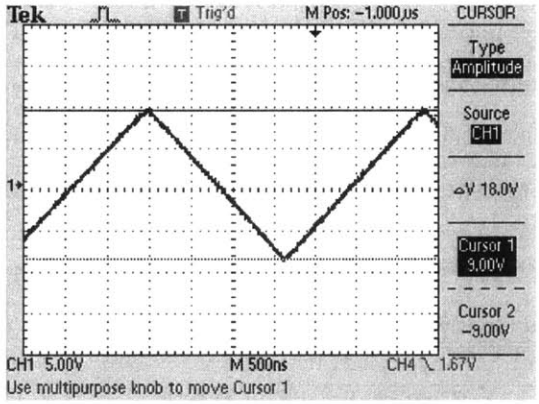
In this section, the control board waveforms are presented first and power board waveforms second. The control board is separated into two sections: modulation and digital logic. Each section contains

a relevant schematic for reference and has detailed descriptions of the figures.

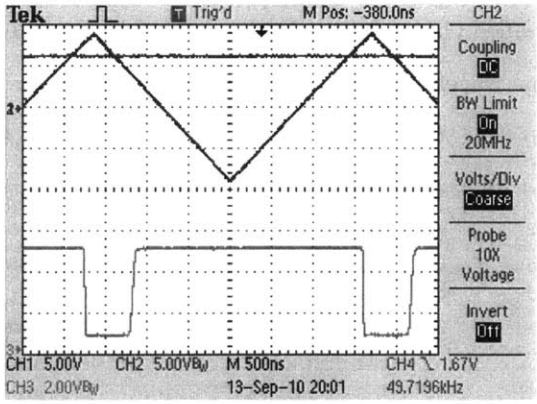
Control Board



(a) Control board integrator and comparator schematic.



(b) Triangle wave measuring 18 Volts peak-to-peak. The period is approximately 3.3 μS.



(c) Comparator operation example. The modulating input and triangle wave are superimposed at top of the graph. The bottom waveform is the comparator output. Modulating input is a DC Voltage of 6.3 Volts.

Figure 4.1: Control board waveforms related to PWM creation

The modulation section of the control board and relevant waveforms are shown in Figure 4.1. Figure 4.1(a) gives the corresponding schematic for control board waveforms related to PWM generation. The triangle wave is displayed in Figure 4.1(b). After trimming the DC offset, the DC Voltage of the triangle wave was measured by the Agilent DMM to be approximately 300 μV. The expected signal amplitude is 18 Volts peak-to-peak which is verified in Figure 4.1(b). An example of comparator operation, equivalently PWM generation, is shown in Figure 4.1(c). The important

feature to note is the asymmetry in the rise and fall times of the waveform. This difference in time occurs because pull-up resistance is much larger than pull-down resistance (output resistance of the LM311). Furthermore, this difference can potentially be a source of error if the difference is large since unintended asymmetry may be introduced to the PWM waveform and should be kept in mind. Another feature to note is the propagation delay from input signal intersection to comparator output, which is approximately 50 ns (difficult to see in Figure 4.1(c) but verified during prototyping) for both rise and fall action. However, this propagation delay should not introduce distortion since the delays appear well matched.

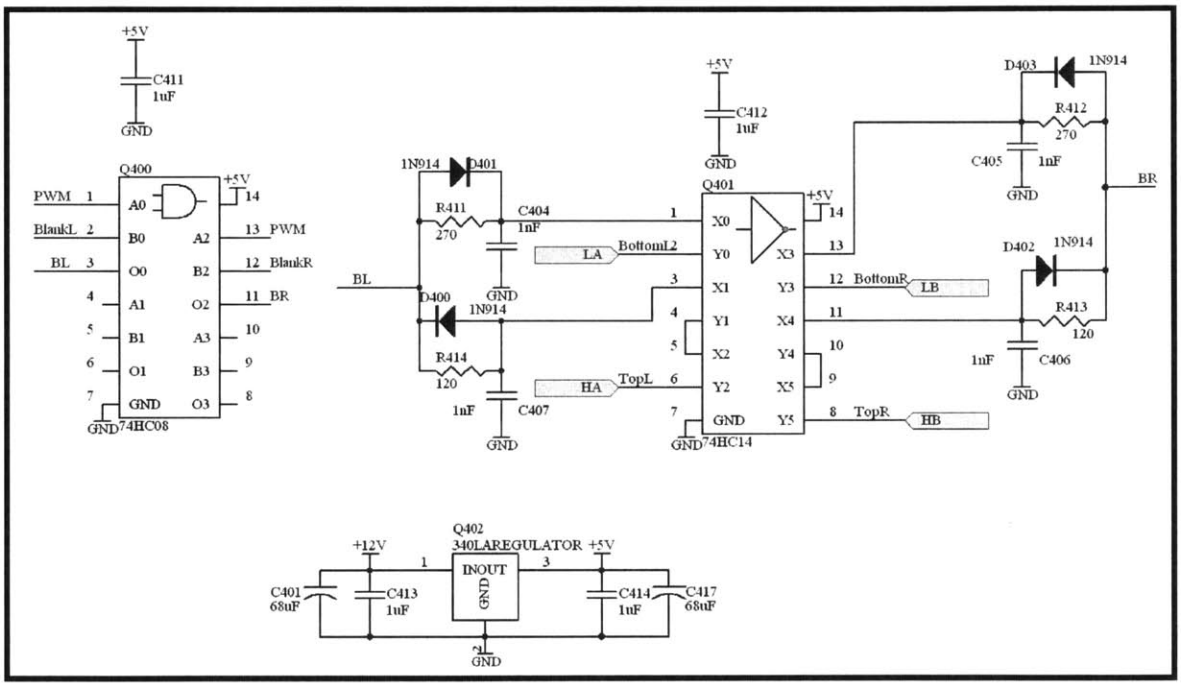
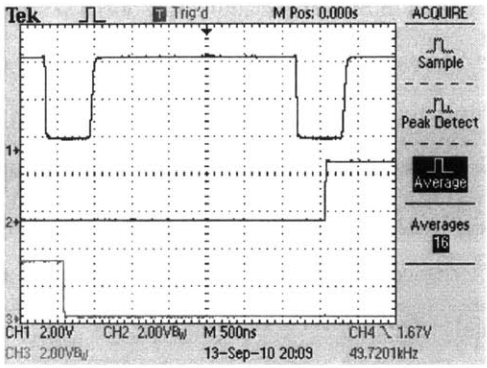
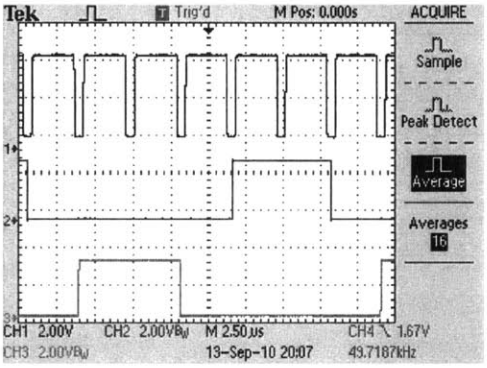


Figure 4.2: Control board digital logic.

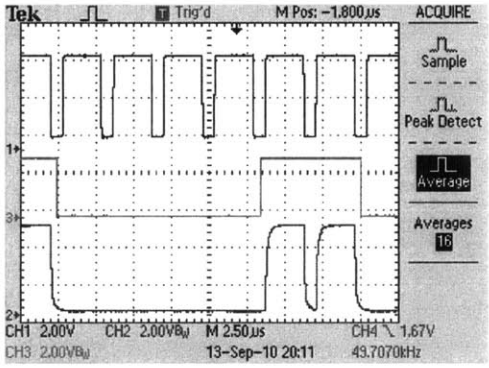
The digital logic section of the control board and corresponding waveforms are shown in Figure 4.2 and Figure 4.3. In Figure 4.2, the digital logic section schematic is shown. Figure 4.3(b) shows the blanking signals aligned with the PWM waveform. Figure 4.3(a) validates phase alignment of the blanking signals and PWM waveform. Figure 4.3(c) illustrates the inputs and outputs of the left-side *AND* gate. Figure 4.3(d) shows the left-side inverter output. Figure 4.3(e) illustrates the right side inverter output waveform. For both sides, the rising edge delay is 100 ns, and the falling edge delay is 200 ns. The reason for the difference in edge delays pertains to different inductive paths for each edge as discussed at the end of Chapter 3.



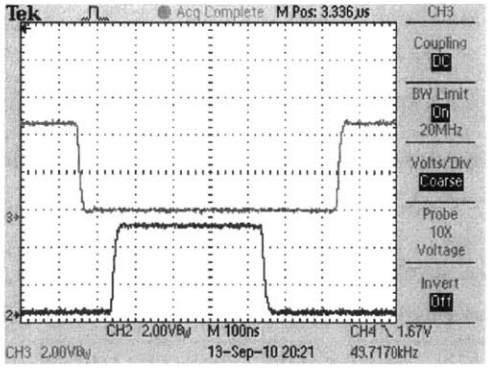
(a) Important phase alignment. The top waveform is the PWM signal. The middle waveform is the left blanking signal. The bottom waveform is the right blanking signal. This alignment is crucial to ensure blanking does not occur during an intended PWM high signal.



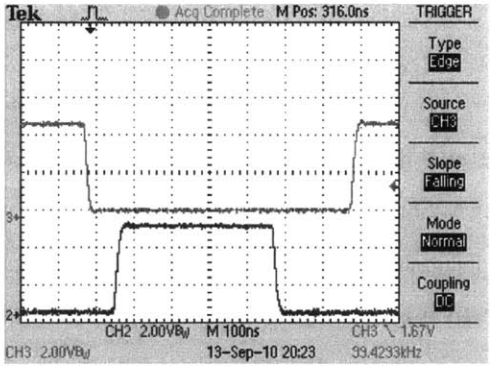
(b) Broader view of PWM Waveform and blanking signals. The top waveform is the PWM signal. The middle waveform is the left blanking signal. The bottom waveform is the right blanking signal.



(c) Left *AND* gate input and output signals. Top signal is the PWM, middle waveform is the left blanking signal, and bottom waveform is the left AND gate output.



(d) Left side dead-time. Top waveform is the high-side input to the left half-bridge gate driver. The rising edge delay is 100nS. The falling edge delay is 200nS.

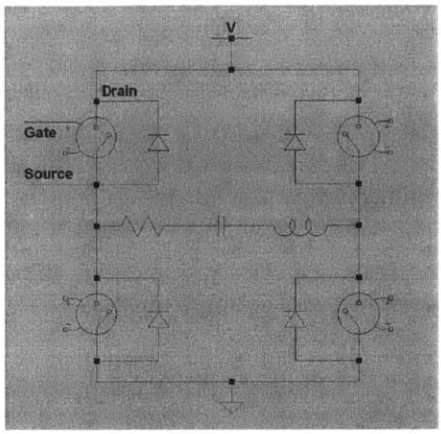


(e) Right side dead-time. Top waveform is the high-side input to the right half-bridge gate driver. The rising edge delay is 100nS. The falling edge delay is 200nS.

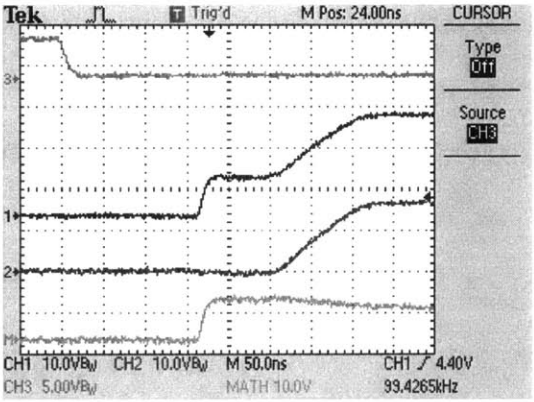
Figure 4.3: PWM waveform and blanking pulses of the digital logic section.

Power Board

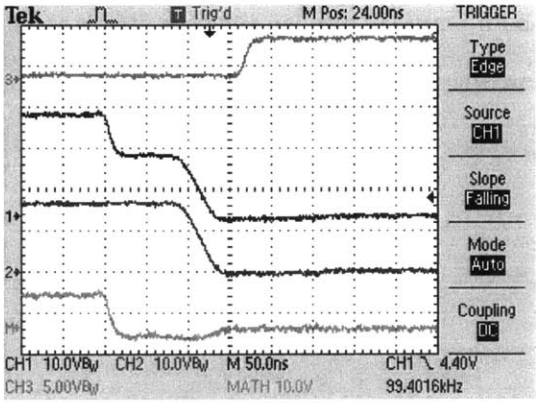
The input modulating signal used for all illustrations in this section was 6.4 Volts DC, which is 80% of the 8 Volt maximum allowed for modulation, and was chosen in order to give large system stress. Figure 4.4(a) gives a simplified schematic for this section (better for illustration than the true schematic). Figure 4.4(d) shows the fall times for both the left and right MOSFETs are verified to be approximately 50 nS and the rise times are approximately 150 nS, which accounts for the slower turn-on preventing EMI as discussed in Chapter 3. The graphs in Figure 4.4(d) and Figure 4.4(e) show low-side MOSFET performance, verifying adequate dead-time between lower gate turn-on (turn-off) and the drain voltage rise from the top switch transition. An important feature to note in both Figure 4.4(e) and Figure 4.4(d) is the negligible Miller charging period resulting from body diode conduction [9].



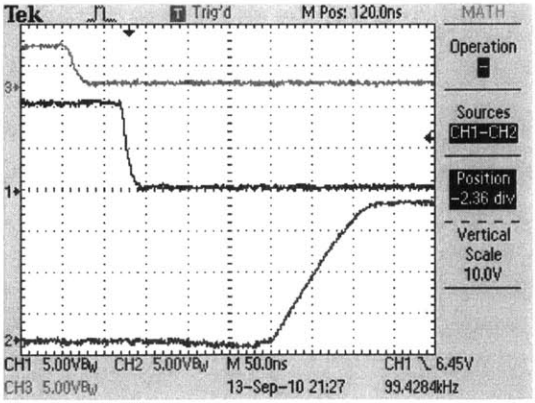
(a) Full-bridge with load for reference.



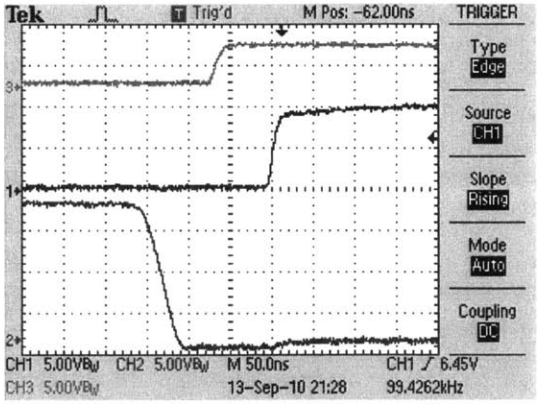
(b) Top left MOSFET open-to-closed transition. The top waveform is the control input signal, second from the top is the MOSFET gate voltage, third waveform from the top is the source voltage, and bottom waveform is the gate-to-source voltage.



(c) Top left MOSFET closed-to-open transition. The top waveform is the control input signal, second from the top is the MOSFET gate voltage, third waveform from the top is the source voltage, and bottom waveform is the gate-to-source voltage.



(d) Bottom left MOSFET closed-to-open transition. Top waveform is the control input, middle waveform is the gate voltage, and bottom waveform is the drain.

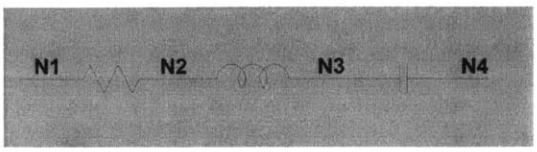


(e) Bottom left MOSFET open-to-closed transition. Top waveform is the control input, middle waveform is the gate voltage, and bottom waveform is the drain.

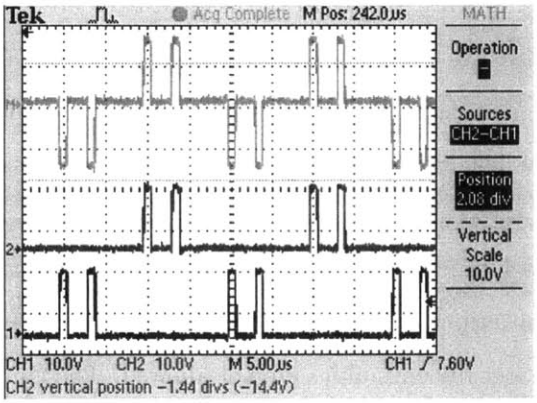
Figure 4.4: Left half-bridge MOSFET transitions.

Load Waveforms

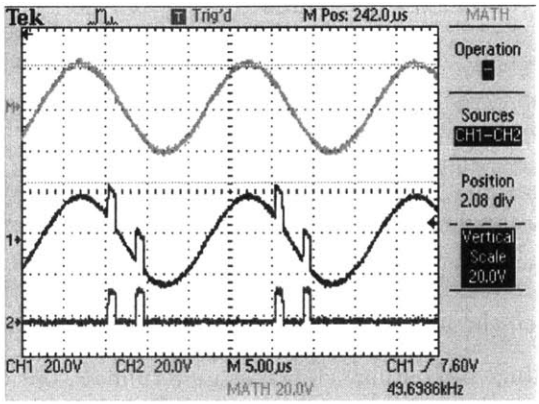
The reference nodes used for discussion of the load waveforms are defined in Figure 4.5(a). The waveforms presented are differential load voltage, capacitor voltage, resistor voltage, and the inductor voltage. The load voltage is shown in Figure 4.5(c) (this waveform is exactly what was desired from the start of this thesis). A DC voltage of -1 Volt was used for illustration. Voltages corresponding to the load capacitor are shown in Figure 4.5(b). The differential voltage across the capacitor must be continuous as required by $I_C = C\frac{dV_C}{dt}$. Voltages corresponding to the load resistor are shown in Figure 4.5(d). The voltage at $N1$ is attached directly to the full-bridge output and, as evident in Figure 4.5(d), does not vary significantly from load current. Small variation in $N1$ are due to on-resistance of the corresponding MOSFETs. The The differential voltage across the load resistor is proportional to the current through the load and is discussed in the next paragraph. Voltages corresponding to the load inductor are shown in Figure 4.5(e). The load current is visible on both nodes since the nodes are not attached to the differential output of the full-bridge. The inductor allows voltage discontinuities across its terminals, but current discontinuities are not allowed. The current through the inductor does satisfy the continuity constraint as discussed in the next paragraph.



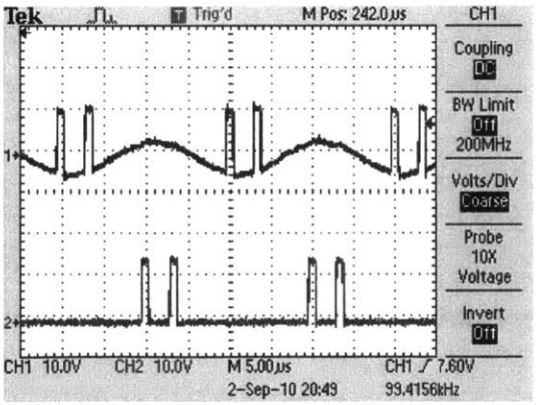
(a) Node definitions



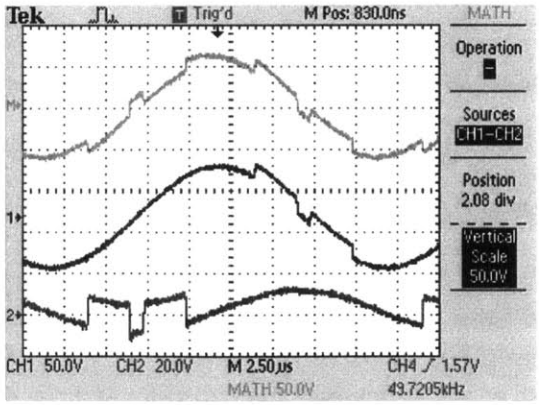
(b) Voltage across the entire load. The top waveform is $N1$, the middle waveform is $N4$, and the bottom waveform is $N1$ minus $N4$.



(c) Voltage across the capacitor. The top waveform is $N3$ minus $N4$, the middle waveform is $N3$, and the bottom waveform is $N4$. Note the voltage across the capacitor does not have any discontinuities as expected.



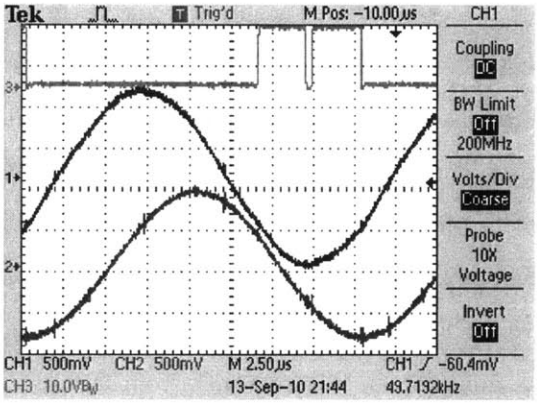
(d) Voltage across the resistor. The top waveform is N2 and the bottom waveform is $N1$.



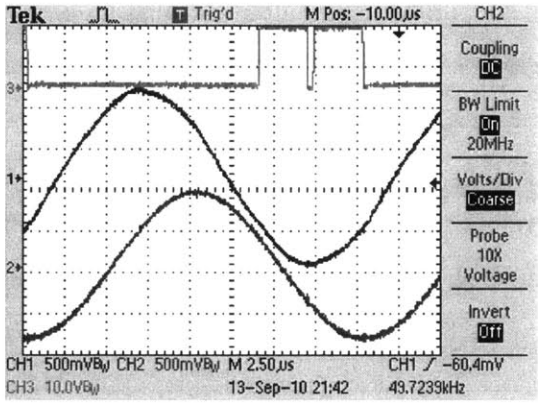
(e) Voltage across the inductor. The top waveform is $N3$ minus $N2$, the middle waveform is $N3$, and the bottom waveform is $N2$.

Figure 4.5: Load voltage waveforms.

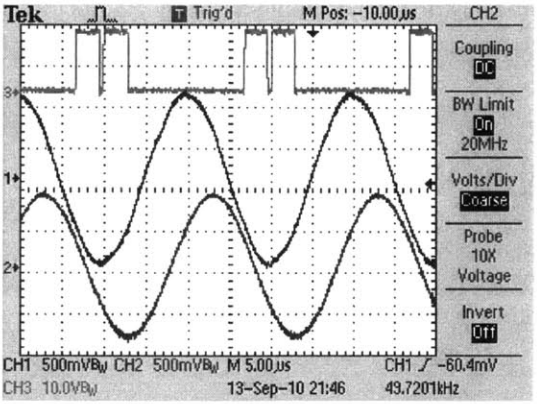
The load current draw is shown in Figure 4.6. The input modulating voltage is set to 7.5 Volts DC, giving a current output of approximately 10.3 Amperes peak-to-peak. The graphed current waveforms in Figure 4.6 are **not** calculated from the oscilloscope math function. The measurement procedure is explained later in this chapter where the referenced anti-alias filter is also presented. In Figure 4.6(d), an example of the final double-sideband, amplitude modulated current waveform is shown. Note the odd shading on the lower waveform occurs from aliasing on the digital oscilloscope, but the envelope is clearly visible.



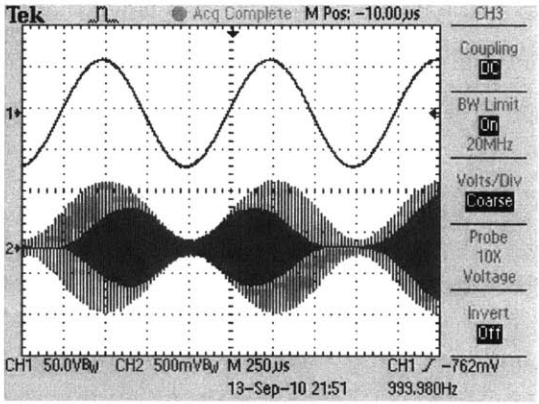
(a) The load current with 20 MHz bandwidth limit off. The top waveform is $N1$ for timing reference. The middle waveform is the differential voltage across the load resistor before anti-aliasing. The bottom waveform is the differential voltage across the load resistor after anti-aliasing.



(b) The load current with 20 MHz bandwidth limit on. The top waveform is $N1$ for timing reference. The middle waveform is the differential voltage across the load resistor before anti-aliasing. The bottom waveform is the differential voltage across the load resistor after anti-aliasing.



(c) A wider view of load current with 20 MHz bandwidth limit on. The top waveform is $N1$ for timing reference. The middle waveform is the differential voltage across the load resistor before anti-aliasing. The bottom waveform is the differential voltage across the load resistor after anti-aliasing.



(d) Amplitude modulated current waveform example. The top waveform is the modulating tone. The bottom waveform is the modulated carrier.

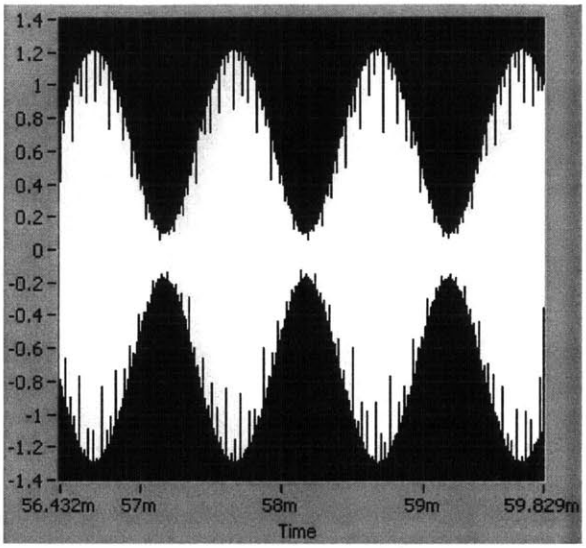
Figure 4.6: Load current waveforms.

4.1.2 Spectral Measurements

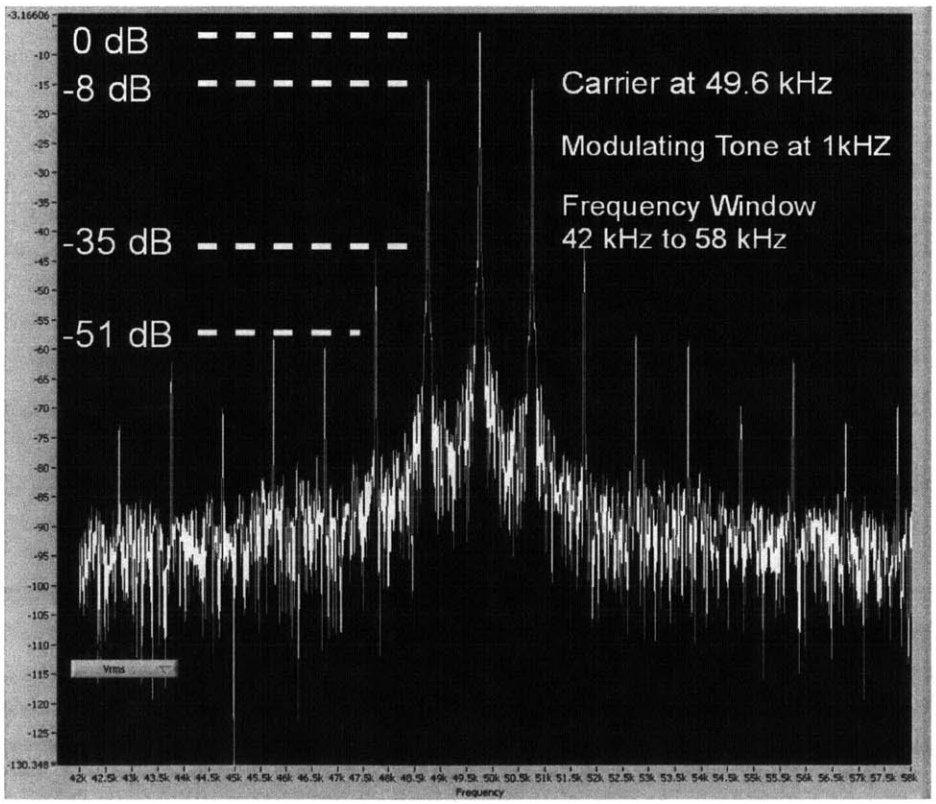
Spectral measurements were taken under two input conditions: zero DC bias with 80% of maximum modulation depth and zero DC bias with 20% of maximum modulation depth. The modulating sinusoid frequency was 1kHz. The waveforms recorded are not scaled for correct absolute readings of the waveforms, though this lack of proper scaling is acceptable since THD measurements only require accurate readings of relative magnitudes. Figure 4.1.2 and Figure 4.8 waveforms were acquired from the NI-USB6251 DAQ after anti-alias filtering. Figure 4.9 results were acquired from the Tektronix digital oscilloscope FFT module **before** anti-aliasing (a flattop window was used in the FFT module).

The time waveform of the zero DC bias with 80% of maximum modulation depth is shown in Figure 4.7(a). Figure 4.7(b) illustrates the Fourier Transform magnitude plot corresponding to Figure 4.7(a). The THD determined from the frequency from this graph is approximately 4.15% as measured by summing the first eight harmonics. Figure 4.8(a) illustrates the time waveform of the zero DC bias with 20% of maximum modulation depth. Figure 4.8(b) illustrates the corresponding Fourier Transform magnitude plot. The THD determined from the frequency from this graph is approximately 4.11% as measured by summing the first eight harmonics.

To provide a further verification of DAQ measurements, Figure 4.9 was generated from the oscilloscope. Figure 4.9(a) shows the spectral content around the carrier for a 1 kHz tone at 80% of maximum modulation depth. It is noted that the first distortion harmonic amplitude coincides with that from the DAQ measurement, thus giving confidence in the results. Figure 4.9(b) shows spectral content acquired from the digital oscilloscope for a 6.4 Volt DC bias (no modulating sinusoid).

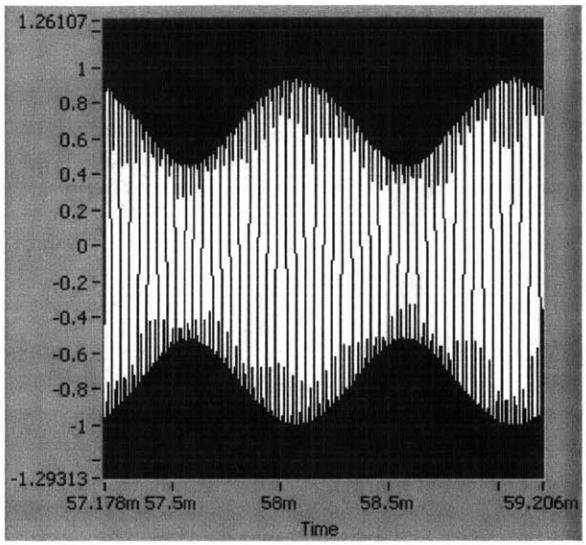


(a) Time waveform. Note the amplitude scale is arbitrary.

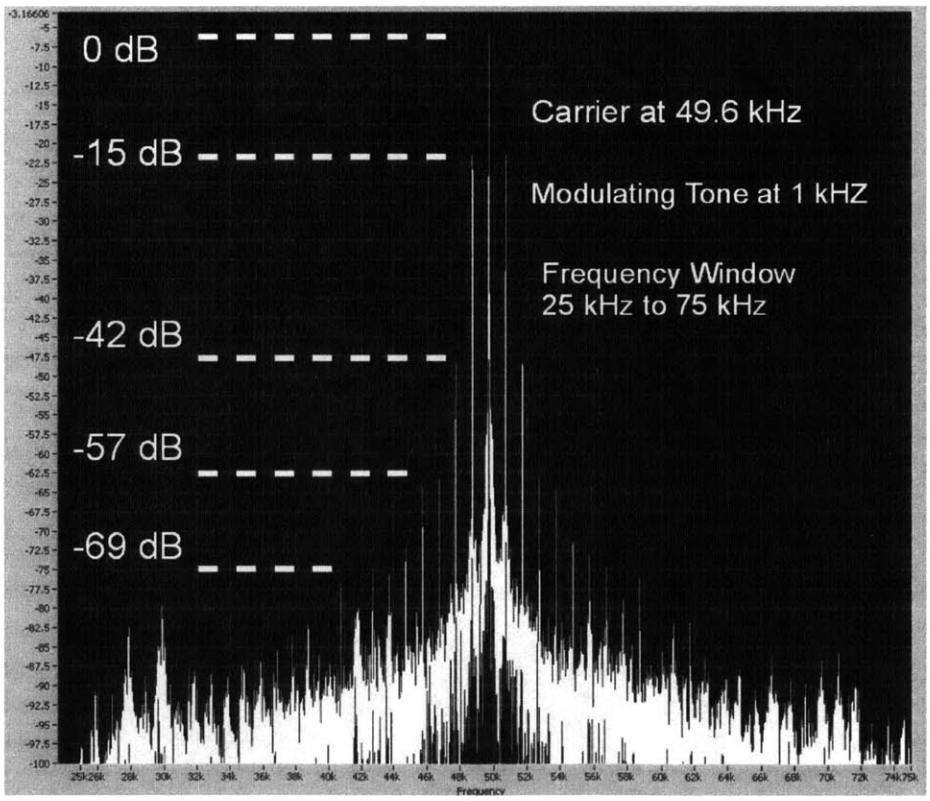


(b) Fourier Transform magnitude.

Figure 4.7: Measurements from NI-USB6251 with 1 kHz modulating input at zero DC bias with modulation at 80% of maximum modulation depth.

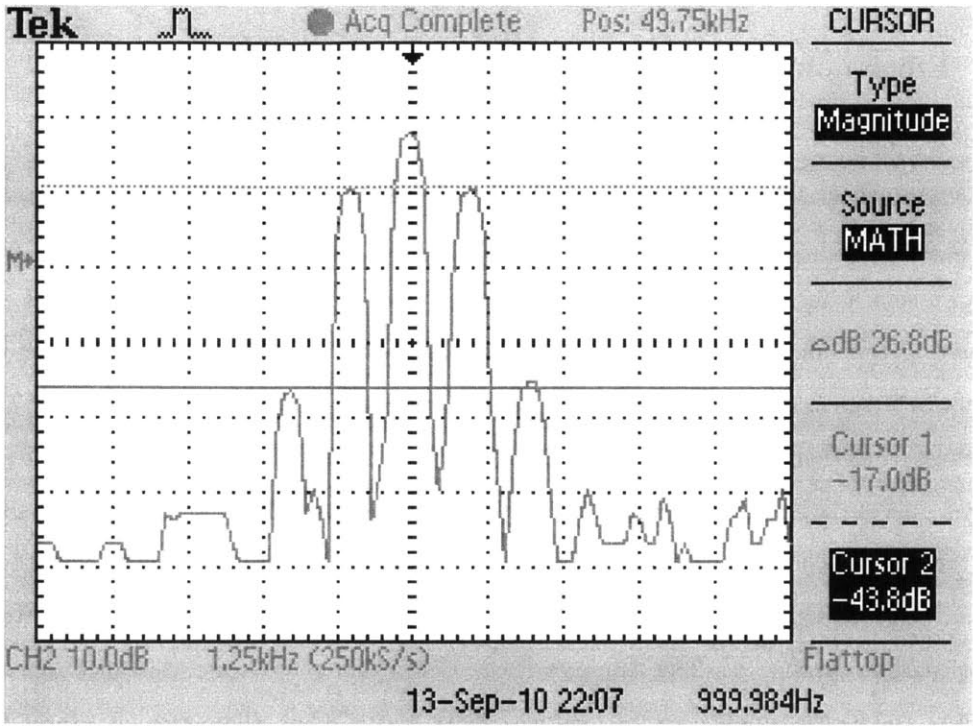


(a) Time waveform. Note the amplitude scale is arbitrary.

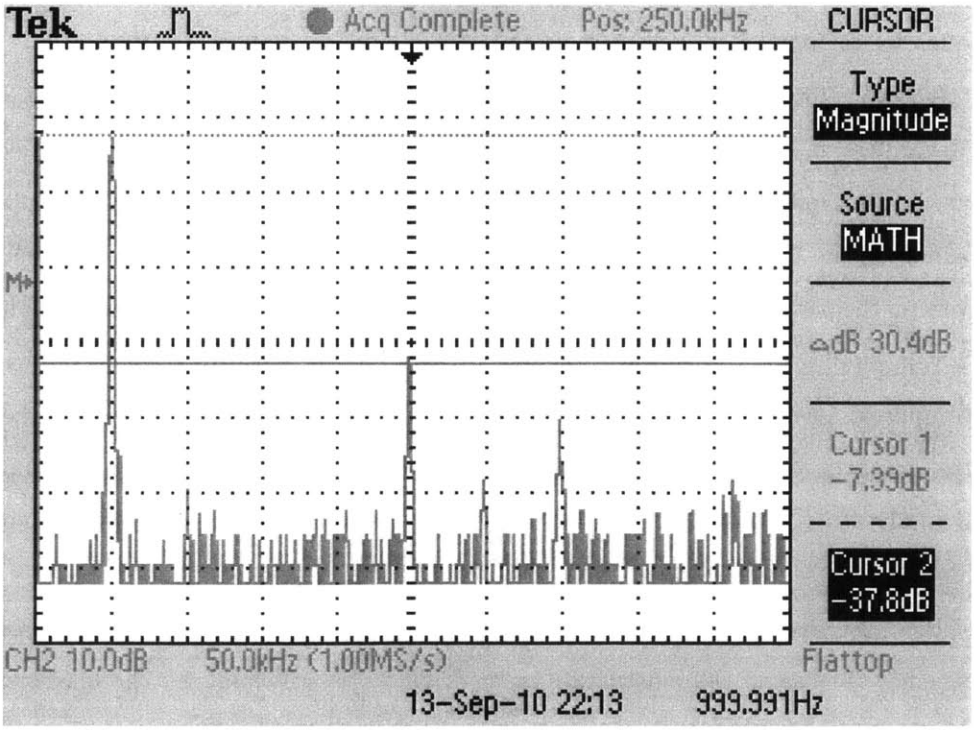


(b) Fourier Transform magnitude.

Figure 4.8: Measurements from NI-USB6251 with 1 kHz modulating input at zero DC bias with modulation at 20% of maximum modulation depth.



(a) Fourier Transform magnitude of load current (close view).



(b) Fourier Transform magnitude of load current (broad view). The even harmonics, third harmonic, and ninth harmonic are below the noise as expected.

Figure 4.9: Measurements from Tektronix digital oscilloscope with 1 kHz modulating input at zero DC bias with modulation at 80% of maximum modulation depth.

4.1.3 Efficiency Results

Before proceeding, two points are emphasized. First, the input signal used to test efficiency does not contain a modulating tone. This choice of test signal is made to ensure maximum power output and maximum system stress since tone modulation with a given maximum envelope level will not source as much current as an equivalent continuous carrier wave of the same level. Second, the input DC signal used to test efficiency must be below the maximum allowed modulation level such that four distinct switch transitions occur per cycle per switch. For example, a duty cycle of unity inherently only has two transitions per half-bridge per cycle, which is not a true test of the worst-case efficiency.

Now, a 16 Volt DC source sets the rail of the full-bridge stage. The input modulation signal used was 7.5 Volts DC. The measured DC current from the power supply contained negligible (if any) ripple and was 1.55 Amperes. This current draw gave a time average power input of 24.8 Watts. The measured output current was 2.02 Amperes RMS. Given that the output resistance was measured to be 5.8 Ω, the power supplied to the load was 23.43 Watts. Thus, the power lost was 1.13 Watts. The measured overall efficiency of the output stage was 95.4%. The expected efficiency from the paper design for the output stage was 95.8%.

As stated in the introduction to Chapter 3, the control board efficiency is not emphasized in this design. Regardless, measurements of the worst-case current draw were taken. The resulting current draw from the $\pm$12 Volt supplies was approximately 40 mA. The resulting current gives a power draw of approximately one Watt. It is important to note that the control board power draw includes the gate-drivers on the power board since the voltage supplied to the gate drivers comes from the control board 12 Volt supply. Additionally, a light indicator (LED) was added to the control board which consumed approximately 10mA of current from the 12 Volt supply. Therefore, taking into account the control circuitry and gate drivers, the overall power dissipation is 2.13 Watts at 23.43 Watts delivered to the load. Thus, efficiency including the control board is approximately 90.9%, well above the target efficiency of 80%.

To further test the amplifier, the full-bridge rail voltage was raised to see effects on output stage efficiency. The same DC modulating input of 7.5 Volts was applied. The final test voltage was 24 Volts and gave an efficiency of approximately 94.7%. The temperature steadily increased with increased power draw as to be expected. The final temperature as measured by an infra-red thermometer was approximately 20 degrees Celsius above ambient. The theoretical limit to this design is around 120 Watts of power given specifications from the MOSFETs datasheet.

4.2 Measurement Techniques

4.2.1 Efficiency Measurement Methods

Verifying efficiency was not as straightforward as the results section makes it appear (at least not for this author). A number of attempts were made before arriving at the accurate measurement (verified with multiple test cases). In this section the methods are described.

The first method used to qualitatively measure efficiency was simple touch. The load resistance was attached to a large heat sink (of unknown thermal resistance) and became extremely hot after a few minutes of running near maximum power output of the amplifier. The MOSFETs, to the contrary, were still at room temperature as determined by probing with the finger. While the mere touch is obviously not going to give a numeric calculation, it is rather convincing that high efficiency has been attained.

Three more methods were attempted for quantitatively measuring efficiency. The first method attempted involved temperature measurement. To determine the MOSFET case temperature, a thermocouple was used first, a packaged IC second, and an infra-red thermometer third. While these temperature measurements did verify the MOSFETs were heating, calculation of efficiency from these measurements gave non-sensible results. The problem with the temperature measurement method includes, amongst other factors, the difficulty in measuring junction temperature from the outer case. An approximation can be made from this temperature reading, but this approximation is not quantitatively that useful [35]. The second method attempted involved current and voltage multiplication using an Analog Devices MLT04G multiplier IC. To perform this multiplication, the voltage across the load resistor was divided down and connected to an input of the MLT04G. Next, the voltage across the entire load was taken directly from the full-bridge differential output, divided down, and sent to the other multiplier input. The time-average of the output signal was measured using the DMM and scaled accordingly for the multiplication. Unfortunately, this method proved to be highly variable and gave unbelievable results. The third method attempted involved RMS load current measurement. The current was determined by using the DMM to read the RMS voltage across the measured load resistor. The RMS current was then squared and multiplied by the total load resistance as determined using the function generator method described in Chapter 3. It is emphasized that the total load resistance **is not** just the load resistor value. The final method gave consistent results across many test cases that was also believable given paper design predictions and (qualitative) temperature measurements from simple touch.

4.2.2 Signal Conditioning and Processing

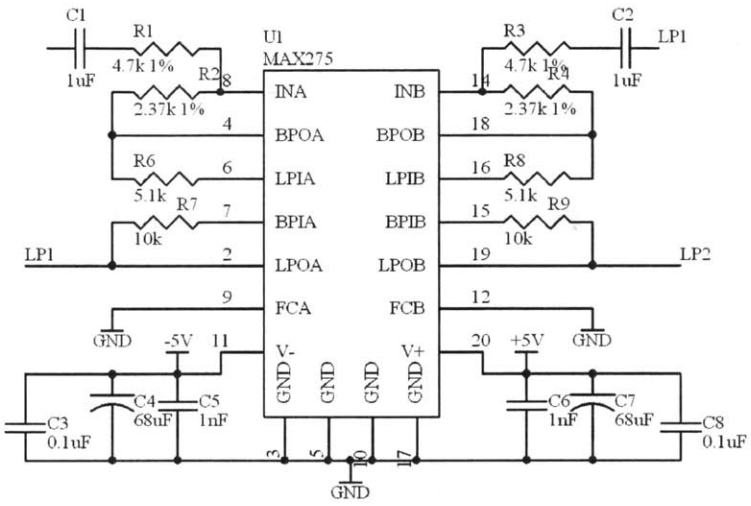
In this section, the steps taken to properly sample the final current waveforms are briefly described.

Anti-alias Filter

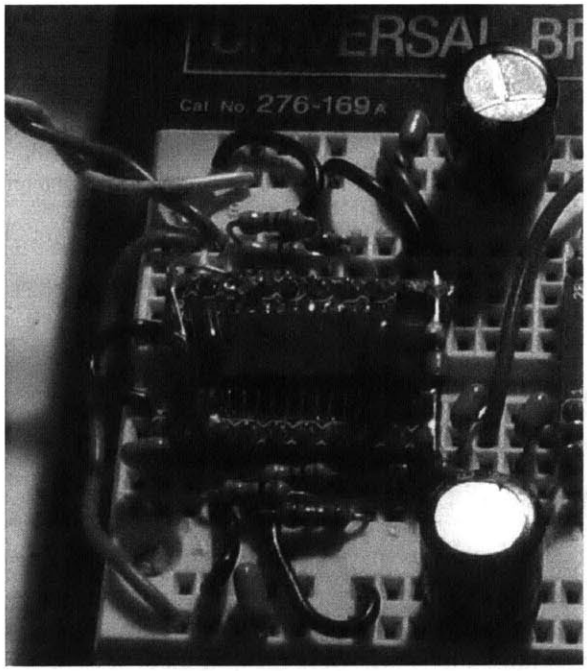
An Analog Devices AMP03 unity-gain differential amplifier was used to convert the differential signal across the load resistor to a single-ended voltage. Two hand-matched, 237 kΩ resistors were used to attenuate the common-mode voltage to an acceptable level for the differential amplifier (though in retrospect a simple voltage divider across the load resistance would have been far simpler). The AMP03 output was then sent to a low-pass, anti-alias filter implemented using a Maxim MAX275 which allows easy implementation of two bi-quad filters. Each of the two filters was designed and measured to have a bandwidth of 150 kHz (maximum allowed by the IC), a Q of approximately 0.707, and a linear gain of 1.1. The two filters sections were ganged together to form a 4th-order filter, giving a verified 24 decibels of attenuation per octave above 150 kHz. Figure 4.10 shows the anti-alias filter used. Figure 4.10(a) shows a schematic of the filter circuitry used along with the corresponding resistor values. Figure 4.10(b) shows an image of the breadboarded circuit.

Digital Signal Processing

The acquired data was sampled at a rate of 1.25 MHz from the NI-USB6251. Since the anti-alias filters cutoff at approximately one-eighth the sampling rate, the acquired signal was decimated by a factor of four in order to slightly lessen the computational requirements of the Fourier Transform as well as get back one bit of SNR [2]. A flattop window was used to process the acquired data.



(a) Anti-alias filter schematic.



(b) Anti-alias filter breadboard prototype.

Figure 4.10: Anti-alias circuitry.

Chapter 5

Summary and Conclusion

The goals of this thesis were to to determine the theoretical bound on total harmonic distortion (THD) of an amplitude modulation technique referred to as pulse-blanked pulse-width modulation (PBPWM) and to build a switch-mode power amplifier with efficiency superior to the theoretical limitation of linear power amplifiers. Both goals were achieved.

In this thesis, prediction of single-tone THD was derived from theoretical analysis, believed to be novel, resulting in an estimate of 0.9%. To verify this theoretical THD prediction, simulations were conducted showing closely matching results of 1.6%. A prototype system was designed and built to test the capability of a practical amplifier realization, giving a final measured THD of approximately 4.15%. The output stage efficiency of the designed prototype was targeted to be above 80% in order to outperform the theoretical limitation of a linear amplifier. The predicted efficiency of the output stage was 95.8% (worst-case), and the measured efficiency of the prototype output stage was 95.4% (worst-case), almost exactly as projected. The overall amplifier efficiency, including control circuitry, was measured to be approximately 90.9%.

A potential reason for the THD discrepancy between theoretical prediction and simulation is the duty cycle quantization inherent in discrete characterization of the waveforms. The simulation used in this thesis required a large number of data points for adequate results, which limited the final duty cycle resolution allowed for reasonable computation time. This limitation effectively adds quantization noise to the output spectrum that can potentially become correlated with the input modulating signal if the duty cycle resolution is too low (this fact was determined empirically). Whether low resolution accounts for the resulting discrepancy between theory and simulation is unknown.

A few potential reasons for THD discrepancy between theoretical prediction and prototype mea-

surements include the following. First, real-world components have non-linearities that are difficult to take into account individually and even more difficult to take into account in aggregate (magnetic components fall into this category). Second, while measurement equipment was verified with test loads, sophisticated test equipment was unavailable. As such, the discrepancy could follow from measurement techniques, though extensive effort was made to remove this possibility. Third, implementation practicalities such as required dead-time between switch transitions and unmatched propagation delays causing unintended pulse-width modification can contribute to measured THD.

Future work on this thesis includes: first, thorough analysis of the noise floor along with measurements of the prototype noise, which potentially requires more sophisticated test and measurement equipment; second, exploration of demodulation and corresponding fidelity; third, closed-loop design and analysis to further reduce THD; fourth, design of efficient control circuitry; fifth, utilization of switch stress asymmetry inherent in the prototype design along with examination of soft-switching techniques allowing for even higher efficiency and lower EMI induced distortion. With the listed improvements, PBPWM is a practical power amplification technique capable of driving a resonant load with remarkable linearity **and** efficiency.

Bibliography

[1] H. Black, *Modulation Theory*. D. Van Nostrand Company,Inc., 1953.

[2] A. Oppenheim and A. Willsky, *Signals and Systems*, 2nd Edition. Prentice Hall, 1997.

[3] A. Carlson, *Communication Systems: An Introduction to Signals and Noise in Electrical Communication*, Third Edition. McGraw-Hill, 1986.

[4] E. Saff, A. Snider, and L. Trefethen, *Fundamentals Of Complex Analysis For Mathematics, Science, Engineering*, 2nd Edition. Prentice Hall, 1993.

[5] A. Oppenheim and R. Schafer, *Discrete-Time Signal Processing*. Prentice Hall, 1989.

[6] G. Paskusz and B. Bussell. *Linear Circuit Analysis*. Prentice-Hall, Inc., 1963, Ch 9.7, Ch 12.

[7] T. Lee, *The Design of CMOS Radio-frequency Integrated Circuits*, 2nd Edition. Cambridge University Press, 2004.

[8] J. Kassakian, M. Schlecht, and G. Verghese, *Principles of Power Electronics*. Addison-Wesley Publishing Company, 1992.

[9] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd Edition. Kluwer Academic Publishers, 2001.

[10] N. Mohan, T. Undeland, and W. Robbins, *Power Electronics - Converters, Applications, and Design*, 2nd Edition. John Wiley & Sons, Inc., 1995.

[11] FeedbackLinearizationOfRFPowerAmplifiers

[12] Z. Song and D. Sarwate, "Frequency Spectrum of pulse-width modulated signals," *Signal Processing*, vol. 83, issue 10, pages 2227 - 2258, October 2003, Elsevier North-Holland, Inc. ISSN 0165-1684.

[13] M. Abramowitz and I. Stegun, *Handbook of Mathematical Functions With Formulas, Graphs, and Mathematical Tables*, Tenth Printing, page 361. U.S. National Bureau of Standards, 1972.

[14] Anonymous, "Feedback, Op Amps, and Compensation," *AN9415.3, Intersil*, November 1996.

[15] R. Stata, "Operational Integrators," *AN-357, Analog Devices*, Reprint from Analog Dialogue 1967.

[16] Anonymous, "Operational Amplifier Inputs," *Application Note 717, Maxim*, November 30, 2000.

[17] R. Mancini, "Chapter 16 Active Filter Design Techniques," *SLOA088 - Excerpt from SLOD006A, Texas Instruments*, pages 50 and 52.

[18] A. Kay, "Analysis and Measurement of Intrinsic Noise in Op Amp Circuits Part II: Introduction to Op Amp Noise," *EN-Genius Network: analogZONE* [Online], www.analogzone.com/avt_1023.pdf.

[19] A. Kay, "Analysis and Measurement Of Intrinsic Noise In Op Amp Circuits Part III: Resistor Noise And Sample Calculations," *EN-Genius Network: analogZONE* [Online], www.analogzone.com/avt_1204.pdf.

[20] J. Roberge, *Operational Amplifiers: Theory and Practice*. John Wiley & Sons, Inc., 1975.

[21] Anonymous, "Selecting the Right Comparator," *Application Note 886, Maxim*, December 13, 2001.

[22] W. Kester, "Comparators," *MT-083 Tutorial, Analog Devices*, October, 2008.

[23] J. Bryant, "Using Op Amps as Comparators,", *AN-849, Analog Devices*, 2006.

[24] Anonymous, "Adding Extra Hysteresis to Comparators," *AN3616, Maxim*.

[25] J. Dunn, "Matching MOSFET Drivers to MOSFETs," *AN799, Microchip Technology Inc.*, 2004.

[26] L. Balogh, "Design And Application Guide For High Speed MOSFET Gate Drive Circuits," *SLUP169, Texas Instruments*.

[27] A. Merello, "Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality," *Application Note AN-1123, International Rectifier*.

[28] Anonymous, "RF Design Guidelines: PCB Layout and Circuit Optimization," *AN1200.04 0, Semtech Advanced Communications & Sensing.*

[29] C. Blake and C. Bull, "IGBT or MOSFET: Choose Wisely," *Technical Papers, International Rectifier.*

[30] J. Zhang, "Choosing The Right Power MOSFET Package," *Technical Papers, International Rectifier.*

[31] Anonymous, "How P-Channel MOSFETs Can Simplify Your Circuit," *AN-940, International Rectifier.*

[32] Anonymous, "P-Channel MOSFETs, the Best Choice for High-side Switching," *AN-804, Vishay Siliconix.*

[33] Anonymous, "A More Realistic Characterization of Power MOSFET Output Capacitance Coss," *AN-1001, International Rectifier.*

[34] S. Mappus, "Optimizing MOSFET Gate Drive Voltage," *EN-Genius Network: analogZONE* [Online], www.analogzone.com/pwrt1208.pdf.

[35] D. Jauregui, "Estimating Tj of SO-8 Power MOSFETs," *Desing Tip 99-2, International Rectifier.*

[36] J. Klein, "Synchronous Buck MOSFET loss calculations with EXCEL model," *AN-6005, Fairchild Semiconductor.*