A Hybrid Switched-Capacitor/Inductor Converter for Small Conversion Ratios

by

Norah Elena Nakibuuka

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Author _____
Department of Electrical Engineering and Computer Science
May 24th 2013

Certified by _____
David J. Perreault
Associate Professor, Department of Electrical Engineering and Computer Science
Thesis Supervisor May 24th, 2013

Certified by _____
Shea Petricek
Intersil Corporation
Thesis Co-Supervisor May 24th, 2013

Accepted by _____
Prof. Dennis Freeman
Chairman, Masters of Engineering Thesis Committee

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Abstract

A hybrid three-switch DC-DC step-up power converter for on chip applications is proposed. It is shown that the hybrid-three switch step-up converter can offer advantages such as reduced size of magnetic components, reduced MOSFET voltage stresses, improved closed loop control and can offer high efficiency compared to a standard boost converter of the same IC package size. These improvements are made possible by adding a flying capacitor that reduces the voltage stresses on the switches and decreases the inductor size by reducing the volt-second across the inductor. The converter is implemented as an integrated circuit built in a 0.25μm 5V CMOS process. Experimental verification shows the gains.

Thesis Supervisor: David J. Perreault
Title: Associate Professor, Department of Electrical Engineering and Computer Science

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1. Introduction

Conventional boost converters have been used almost exclusively to provide DC-DC conversion for integrated switching regulators. However, existing boost converters have some constraints including 1: Large inductor size, 2. High voltage stresses on MOSFETs, and 3. Right-half-plane zero that easily causes instability. Further, the efficiency of the conventional boost converter can be improved. Large inductor size is a barrier to integration, especially for SOC (System on a Chip) applications. Increasing the switching frequency reduces the inductor size, but results in higher switching losses that reduce overall converter efficiency.

For applications that require small conversion ratios such that the output voltage need not be greater than twice the input voltage, the converter proposed in this thesis can: 1. Reduce the required inductor size, 2. Reduce the voltage stresses on the switches, 3. Reduce the average inductor current, 4. Provide improved closed loop control, 5. Maintain or offer improved efficiency over that of the traditional boost converter by reducing inductor losses. This topology may be used to generate a 5V rail from low voltages such as a single lithium-ion cell.

1.1 Research Background

1.1.1 Current switched capacitor/inductor DC-DC converters

As applications that require power converters move more and more towards

miniaturization, it becomes important to integrate the power stage components of the

converter. Various methods are currently adopted to realize dc-dc conversion for such

integrated solutions. These include topologies that utilize magnetic components, and

are discussed in [1]-[9]. Other power converters such as switched capacitor circuits

require no magnetics and are discussed in [11]-[17].

Switched capacitor circuits contain primarily semiconductor switches and

capacitors. They are used to convert or invert dc voltages. The capacitors in the switched

capacitor stages are charged when they are connected across the input. The switched

capacitor circuits are attractive as they require no magnetic components and therefore

are small and can be used for integration ([12], [14], [21]). Moreover, high efficiency can

be realized. However, when using switched capacitor circuits, it is difficult to realize

output regulation with a wide range of input variations, as discussed in [20]. Moreover,

good output regulation is achieved at the expense of high efficiency.

Due to the limitations of the switched capacitor circuits, these circuits are often

integrated with a regulation stage to allow for output voltage regulation. An example of

a two stage architecture that utilizes a switched capacitor stage and a buck converter

stage for regulation is discussed in [1]. Another circuit integrates a switched capacitor

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circuit within a boost converter and is discussed in [18]. Similarly, a two stage

architecture that uses a switched capacitor voltage divider as the first stage and a

regulation stage is discussed in [2].

1.1.2 Proposed class of circuits

While the converters discussed in the section above have various merits, we

would like to investigate circuits that improve on performance of the conventional

converters. To have commercial value, we must produce a circuit having some

improved combination of size, cost and efficiency. The class of circuits proposed consists

of a three switch plus inductor unit and is shown in Figure 1.1.
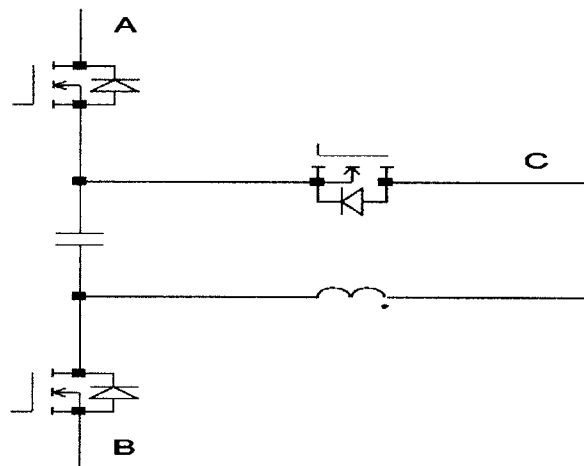
Figure 1.1: Three switch plus inductor unit of the proposed class of circuits.

A flying capacitor is added to act as a floating voltage source. The unit has six different

variants: the step up, step down and inverting configurations. Each configuration has a

constraint on the output. This work focuses on one of the step up configurations whose operation is detailed in the next chapter.

1.2 Thesis Objectives, Contributions and Organization

The goal of this thesis is to analyze and design a hybrid switched capacitor/inductor step-up power converter in order to understand the value and limitation of this class of circuits. An experimental prototype is built with the following specifications:

- Input voltage: 2.5-4.2V

- Output voltage: 3.3-5V

- Switching frequency: 1MHz

- Output current: 3A

Chapter 2 introduces the hybrid 3-switch step-up power converter that is analyzed in this thesis. The operating principles of the circuit are discussed, and its merits over the conventional boost converter are illustrated by showing the circuit's inductance benefit, reduced voltage stresses and average inductor benefit. This chapter also illustrates the simulated converter performance.

Chapter 3 discusses the power loss mechanisms of the proposed power converter. A detailed model of the loss contribution of each of the converter components

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is presented. Lastly, the efficiency results obtained from the power loss model are compared with those from experimental verification to determine the model's accuracy.

Chapter 4 details the methods used to select and size the power stage components. The flying capacitor and the switch on resistance are of special interest.

Chapter 5 discusses the design and layout of the power stage components, control circuit and the PCB board used for experimental verification.

Chapter 6 provides experimental verification of the IC implementation of the proposed converter. Important characteristics such as power loss, efficiency, response to load steps, startup and shutdown waveforms are evaluated at different conditions. The gains provided by the IC implementation are shown.

Finally, Chapter 7 summarizes the contribution of the thesis, and also suggests areas for future work.

2. Proposed Hybrid 3-switch Step-Up Power Converter

The previous chapter discussed the limitations of existing hybrid switched capacitor/inductor power converters. Chapter 2 discusses the proposed architecture of the hybrid step up power converter. To have commercial value, the circuit must have some improved combination of size, cost and efficiency. In addition, the circuit must not be so complex that it becomes impractical for widespread use. Section 2.1 discusses the proposed architecture, followed by the operating principles in Sections 2.2. The proposed circuit is compared with the conventional boost converter in Section 2.3 and the simulated performance of the proposed converter is discussed in Section 2.4.

2.1 Power Stage Architecture

The power stage is shown in Figure 2.1 and it consists of three switches Q_1, Q_2 and Q_3. An external flying capacitor C_{fly} is added that acts as a floating voltage source and is balanced so that it holds the input voltage. Finally, a low pass filter consisting of an inductor and output capacitor is connected to the high frequency phase node. A key feature to note is that the architecture looks like that of the conventional buck converter, with a third switch and flying capacitor added to provide a boosting benefit. This architecture offers the simplicity to be used in a commercial application.

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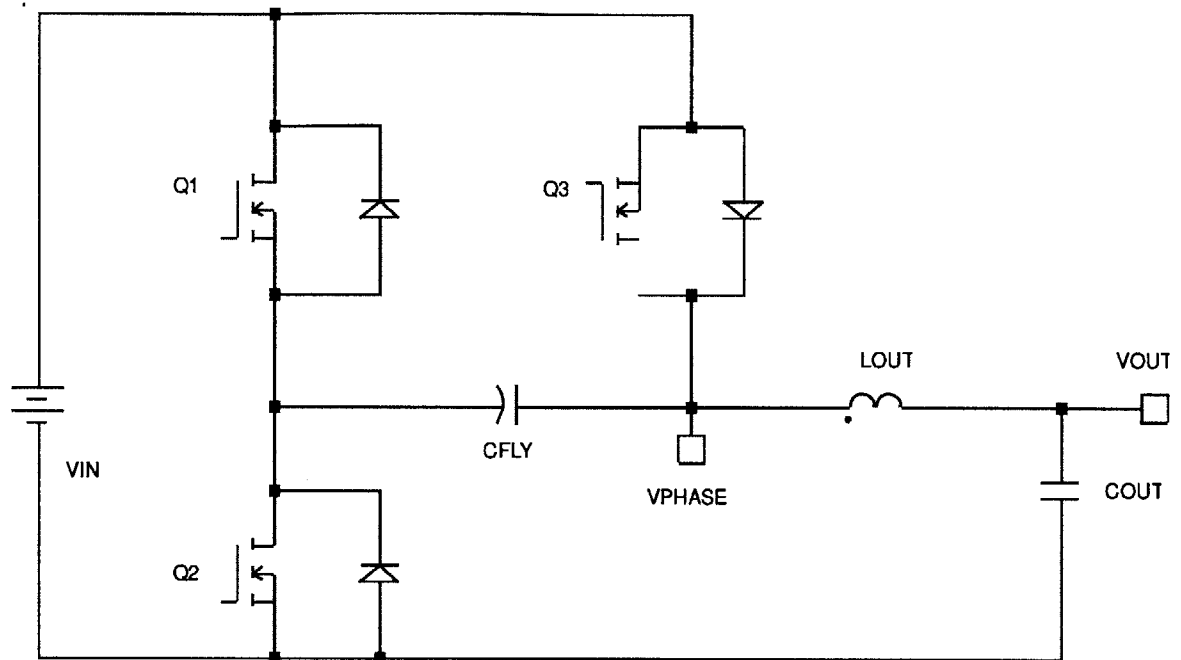
Figure 2.1: Schematic of the 3-switch hybrid step-up power converter, consisting of three switches Q_1, Q_2 and Q_3, a flying capacitor C_{fly}, and an output filter consisting of an inductor L_{out} and output capacitor C_{out}.

The size of the flying capacitor must be chosen so that it is large enough to hold the input voltage but at the same time should not increase the size of the desired application. Chapter 4 discusses the sizing of the flying capacitor in more detail.

2.2 Operating Principles

The operation of the proposed circuit is as follows:

DT-T: Switches Q_2 and Q_3 are turned on while Q_1 remains off. The flying capacitor is charged and the input voltage appears across it. The voltage across the inductor is

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reversed and the inductor current ramps down. Figure 2.3 shows the charging phase of

the flying capacitor.

0-DT: Switch Q_1 is turned on while Q_2 and Q_3 are off. The flying capacitor is discharged.

A positive voltage appears across the inductor and the inductor current ramps up.

Figure 2.4 shows the discharging phase of the flying capacitor, and Figure 2.2 below

illustrates the timing diagram when the duty ratio is less than 0.5.
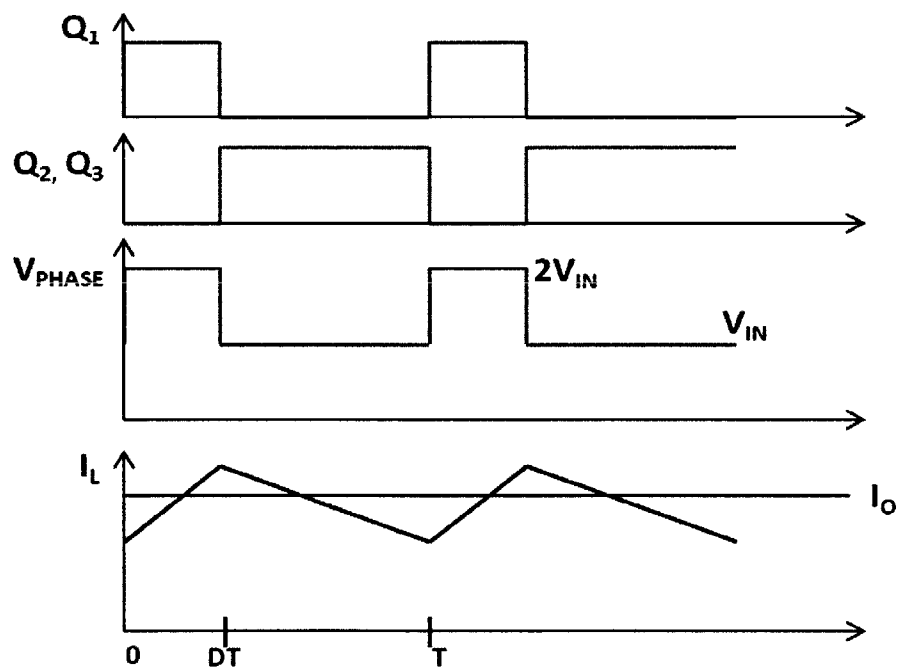
Figure 2.2: Timing diagram for D<0.5.
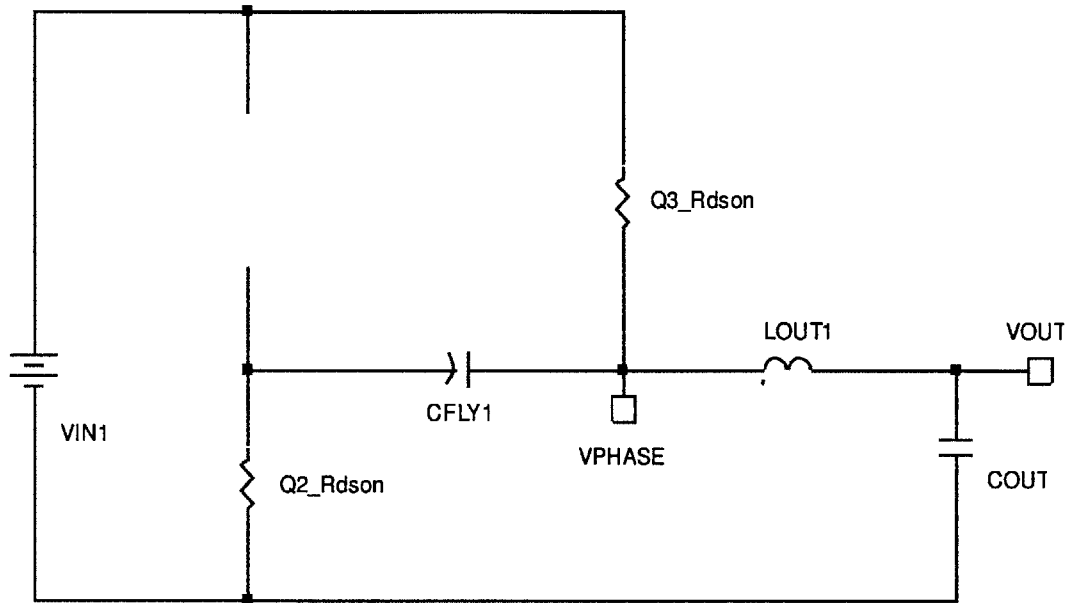
Figure 2.3: Charging phase of the flying capacitor.
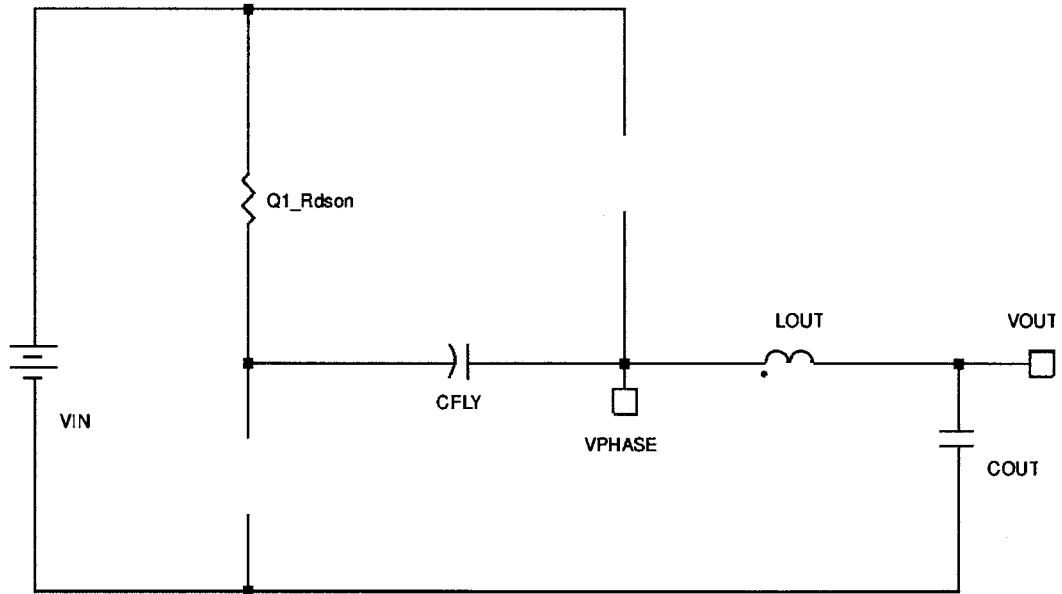
Figure 2.4: Discharging phase of the flying capacitor.

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During one complete cycle, the phase node moves between V_{in} and $2V_{in}$. From inductor

volt-second balance, it follows that:

$$(2V_{in}-V_{out})D+(1-D)(V_{in}-V_{out})=0 \qquad (2.1)$$

$$\frac{V_{out}}{V_{in}}=1+D \qquad (2.2)$$

where V_{in} is the input voltage, V_{out} is the output voltage, and DT is the on-time of switch

Q_1. The inductor current ramps up during time 0-DT, which results in an inductor ripple

current given by

$$\Delta_{IL_{pk\_pk}}=\frac{(2V_{in}-V_{out})D}{f_{sw}L} \qquad (2.3)$$

where f_{sw} is the switching frequency and L is the value of the output inductor. Using

state equations, the small signal gain of the converter is derived and has a transfer

function given by

$$\frac{V_{out}}{V_{in}}=\frac{-1}{s^2LC+\frac{sL}{R}+1} \qquad (2.4)$$

where C is the output capacitor and R is the load. This converter has two left half-plane

poles, and no zeros. Given the operating principle explained above, it can be seen that

since the phase node moves between the input voltage and twice the input voltage, the

output voltage can only rise to twice the input voltage. Hence, the proposed circuit can

only be used in applications that require boost conversion ratios of up to two.

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2.3 Comparison with a conventional boost converter

Compared with the conventional boost converter, the proposed circuit offers

advantages such as reduced inductor size, lower voltage stresses on the switches, and

reduced average inductor current. Each of these gains is explained in detail in the

following subsections.

2.3.1 Inductance Benefit

The hybrid three switch step up converter is attractive for small boost conversion

ratios as it eliminates the use of bulky magnetic components. The sizes of the inductors

required in the hybrid three switch and conventional boost converter are as follows:

$$L_{3switch} = \frac{(2V_{in}-V_{out})(\frac{V_{out}}{V_{in}}-1)}{\Delta_{IL_{pk\_pk}}f_{sw}} \tag{2.5}$$

$$L_{traditional\_boost} = \frac{V_{in}(\frac{V_{out}-V_{in}}{V_{out}})}{\Delta_{IL_{pk\_pk}}f_{sw}} \tag{2.6}$$

When the switching frequency and ripple current are kept constant, a comparison of the

inductor size needed in the hybrid versus the conventional boost converter is illustrated

in Figure 2.5. As shown in the figure, the hybrid always utilizes a smaller inductor for

conversion ratios greater than 1.2.

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(a) Inductance Comparison   (b) Inductance Benefit
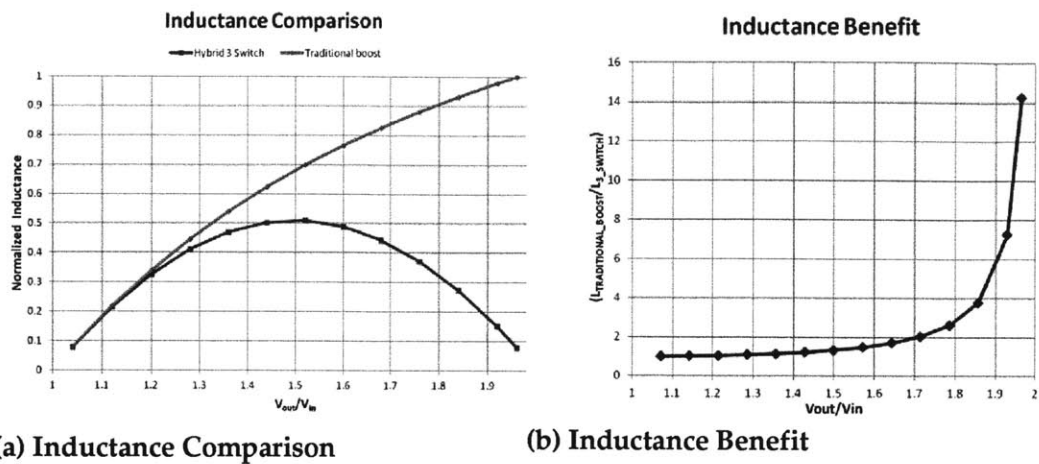
Figure 2.5: Comparison of the inductor size used in a conventional boost converter versus the hybrid 3-switch with switching frequency and ripple current kept constant.

In a simulated test case when the output power is 12W, the proposed circuit

attains a forty percent reduction in inductor size when compared with the conventional

boost converter. Table 2.1 illustrates the inductor benefit offered by the proposed circuit.

The results in the table were obtained from running a SIMetrix/SIMPLIS simulation.

	Conventional boost converter	Proposed circuit
Inductor size	1μH	600nH

Table 2.1: Inductor size comparison. The operating conditions are Vin =2.8V, Vout =4V, fsw = 1MHz Iout =3A.

2.3.2 Voltage Stresses on Devices

The three switches in the hybrid three switch converter only need to be sized to

handle the input voltage. During the phase when the inductor current ramps up, the

voltages on the MOSFET's are as follows:

$$V_{dsQ1}=0 \tag{2.7}$$

$$V_{dsQ2}=V_{in} \tag{2.8}$$

$$V_{dsQ3}=(V_{in}+V_{Cfly}-V_{in})=V_{in} \tag{2.9}$$

where V_{dsQ1}, V_{dsQ2}, and V_{dsQ3} are the drain to source voltages across Q_1, Q_2 and Q_3

respectively. As the inductor current ramps down and the flying capacitor is charged,

the voltages seen across the devices are:

$$V_{dsQ1}=V_{in} \tag{2.10}$$

$$V_{dsQ2}=0 \tag{2.11}$$

$$V_{dsQ3}=0 \tag{2.12}$$

where V_{Cfly} is the voltage across the flying capacitor and is balanced to equal the input

voltage.

Hence, all the switches need only be sized to handle the input voltage as

compared to the conventional boost converter where the switches must handle the full

output voltage.

2.3.3 Average Inductor Current Benefit

In the hybrid three switch converter, the inductor carries the load current,

whereas the inductor in the conventional boost carries a multiple of the load current, as

seen in the equations 2.13 and 2.14.

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$$I_{L3switch} = I_o \tag{2.13}$$

$$I_{L_{traditional\_boost}} = \left(\frac{V_{out}}{V_{in}}\right) I_o \tag{2.14}$$

where I_o is the load current. This allows for the inductor in the hybrid converter to be sized for lower peak currents. Figure 2.1 below illustrates the average inductor current benefit of the proposed circuit versus the conventional boost converter.

Inductor Average Current
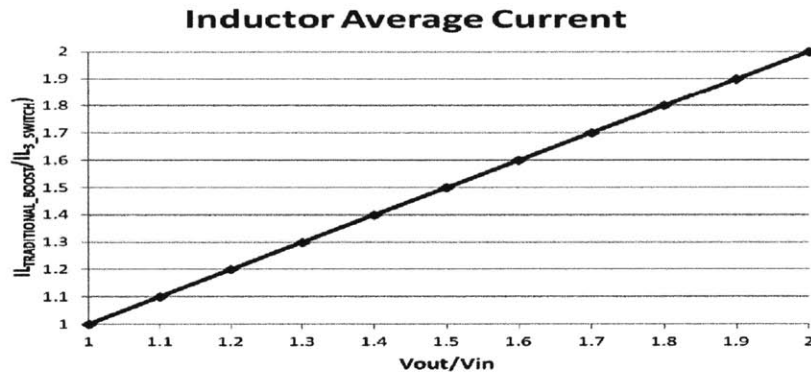
Figure 2.1: The conventional boost converter carries more average current than the hybrid 3-switch by a factor of the conversion ratio.

2.4 Simulated Converter Performance

The SIMetrix/SIMPLIS simulator was used to optimize the performance of the proposed circuit before an experimental prototype was built. A piecewise linear model for the flying capacitor used in the simulator was obtained by taking laboratory measurements of the capacitance at various voltages and then calculating the stored charge. The on-resistance of the switches used in the simulator was chosen to minimize conduction losses, as will be discussed in Chapter 3.

2.4.1 Converter Waveforms

Figure 2.6 below shows the switch, inductor and flying capacitor current waveforms when the load current is 3A. Switch Q_1 carries the inductor current during its on time, whereas the load current is split between switches Q_2 and Q_3 during their on time. The flying capacitor carries high frequency currents, and hence its E_{SR} should be low to reduce conduction losses.
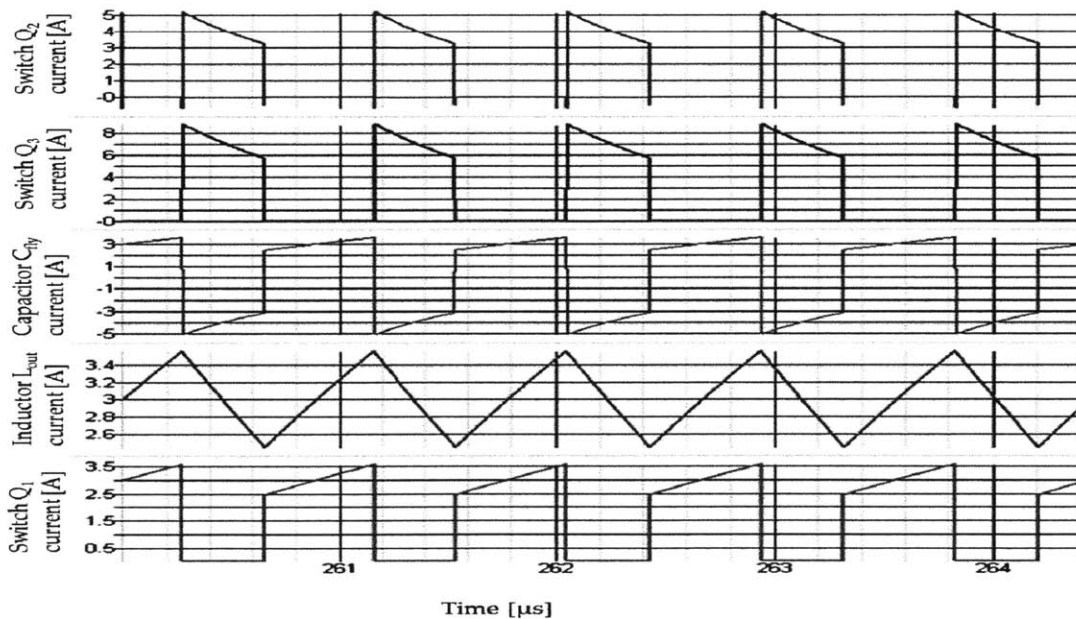
Figure 2.6: Converter waveforms obtained from a SIMetrix/SIMPLIS simulator when the load current is 3A. The flying capacitor carries high frequency current.

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3. Power Loss Modeling

For circuit evaluation, much emphasis was placed on fully understanding the actual power conversion losses and limitations. The converter performance is highly dependent on the loss mechanism of each of the components used. When operating the converter in the 10W power range, I_{rms} ^2R losses are high and must be minimized. A power loss model was built in excel to calculate the losses due to the output inductor (Section 3.1), flying capacitor (Section 3.2), and switches (Section 3.3). Section 3.4 illustrates the accuracy of the modeled results.

3.1 Output Inductor

The main loss mechanism for the inductor was the conduction loss. Figure 3.1 below shows the inductor current waveform in steady state. The I_{rms} values of the currents were calculated by taking the integral of the square of current over one switching cycle and then simplifying the resulting equations using Mathcad.

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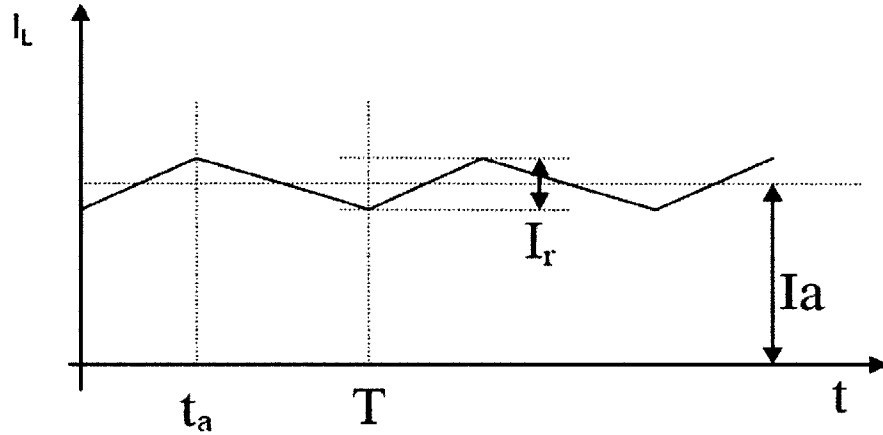
Figure 3.1: Inductor current in steady state.

The ripple current I_r was calculated as follows:

$$I_r = \left(\frac{2V_{in}\text{-}V_{out}}{L}\right)\left(\frac{V_{out}}{V_{in}} - 1\right) \times \frac{1}{f_{sw}} \qquad (3.1)$$

The I_{rms} current in the inductor is calculated as follows:

$$I_{rms} = \sqrt{\left(I_a{}^2 + \frac{I_r{}^2}{12}\right)} \qquad (3.2)$$

The conduction loss in the inductor is calculated as follows:

$$P_{conduction} = I_{rms}{}^2 \times L_{DCR} \qquad (3.3)$$

3.2 Flying capacitor

Figure 3.2 shows the waveform for the current through the flying capacitor.

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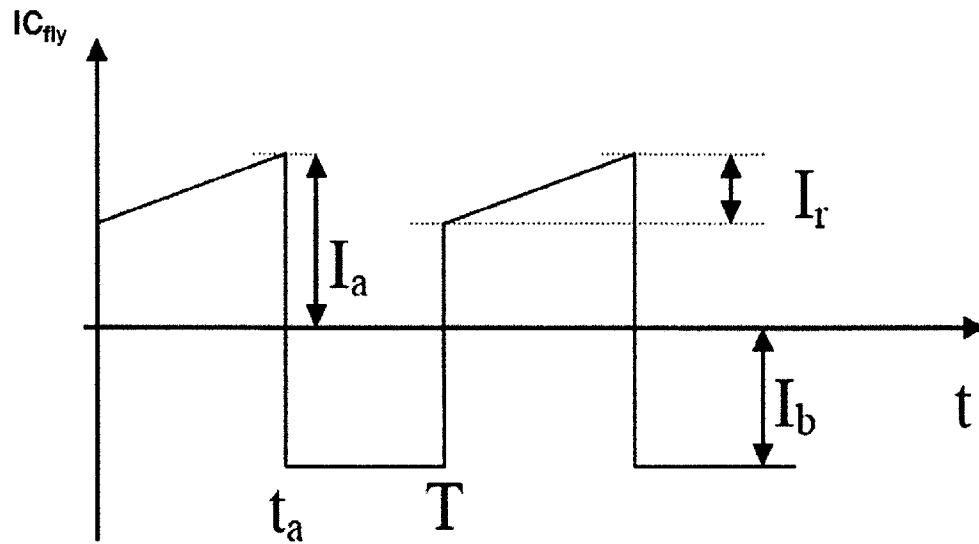
Figure 3.2: The current through the flying capacitor C_fly in steady state.

The I_{rms} current through the flying capacitor is estimated as follows:

$$I_{rms}=\sqrt{\left(I_b{}^2(1\text{-}k)+k(I_a{}^2-I_aI_r+\frac{I_r{}^2}{3})\right)} \tag{3.4}$$

Using capacitor charge balance, the current I_b is obtained as:

$$I_b=\frac{-k\left(I_a\text{-}\frac{I_r}{2}\right)}{1\text{-}k} \tag{3.5}$$

where

$$k=\frac{t_a}{T} \tag{3.6}$$

The conduction loss was then calculated by:

$$P_{conduction}=I_{rms}{}^2\times C_{fly\_ESR} \tag{3.7}$$

Similarly, the output capacitor conduction loss is given by:

$$P_{conduction}=I_{rms}{}^2\times C_{OUT\_ESR} \tag{3.8}$$

3.3 Switches

The main loss mechanism for the switches Q_1, Q_2, and Q_3 were the conduction

loss, switching loss, body diode deadtime loss and output capacitance loss.

3.3.1 Switch Q_1

Figure 3.3 below shows the current through switch Q_1 in steady state. The switch

turns on when the flying capacitor is discharging. During this phase, Q_1 carries the

inductor current. The I_{rms} current was derived as follows:

$$I_{rms}=\sqrt{\left(k(I_a^2+\frac{I_r^2}{3}-I_aI_r)\right)}$$
(3.9)

The conduction loss was then calculated by:

$$P_{conduction}=I_{rms}^2 \times R_{dson}$$
(3.10)

The switching losses were calculated by:

$$P_{switching}=0.5*V_{in}^2I_{Q1}(t_{rise}+t_{fall})f_{sw}$$
(3.11)

The average current I_{Q1} was calculated by:

$$I_{Q1}=\left(I_a-\frac{I_r}{2}\right)$$
(3.12)
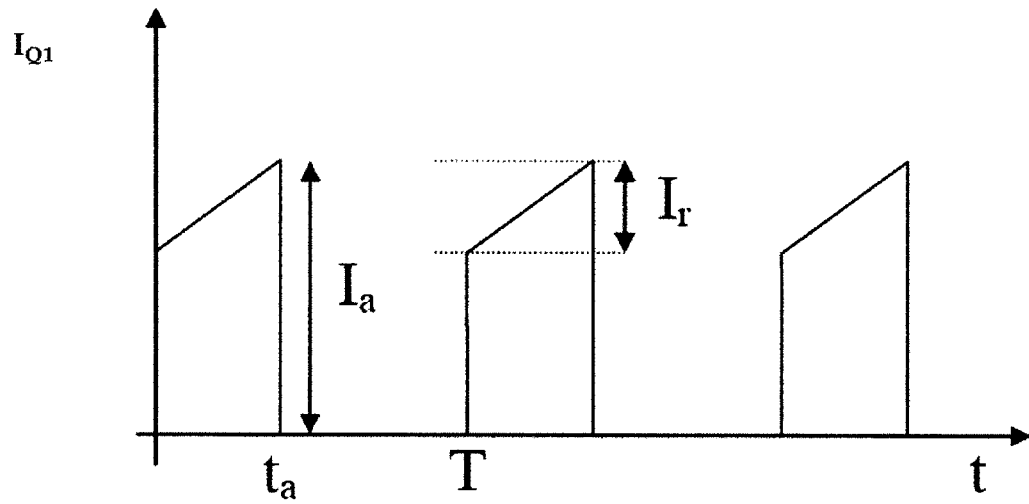
Figure 3.3: The current through switch Q1 in steady state.

Finally, the output capacitance loss was calculated as follows:

$$P_{loss\_cap} = C_{oss} \times V_{in}^2 f_{sw} \times 0.5 \tag{3.13}$$

The loss due to driving Q1 is determined by:

$$P_{driver} = V_{gs1} f_{sw} Q_g \tag{3.14}$$

where Q_g is the gate charge.

3.3.2 Switch Q_2

Figure 3.4 below shows the current through switch Q2 in steady state. The main losses in this switch were conduction loss, switching loss, body diode dead time loss, and output capacitance loss.
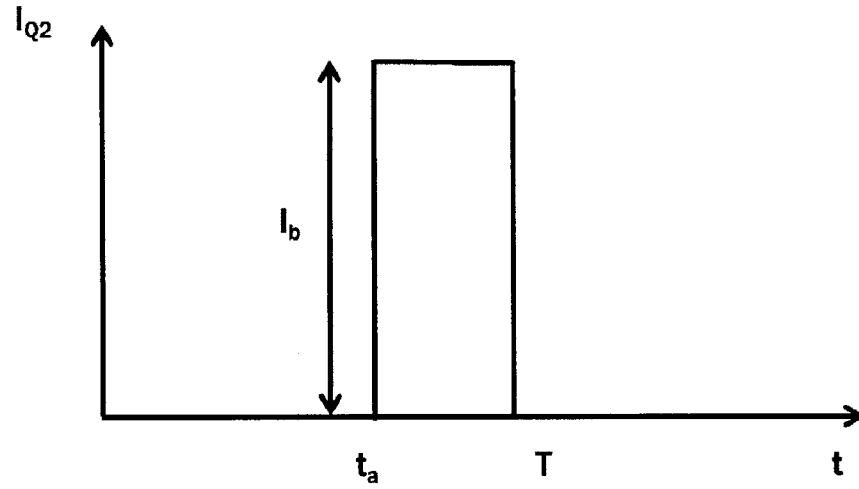
Figure 3.4: The current through switch Q₂ in steady state.

The I_{rms} current through this switch was calculated by:

$$I_{rms} = I_b \sqrt{1 - \frac{t_a}{T}}$$

(3.15)

$$I_{Q2} = I_{rms}$$

(3.16)

Then the body diode deadtime loss was calculated as follows:

$$P_{deadtime} = V_d\, f_{sw}(I_b T_d + I_b T_d)$$

(3.17)

The conduction loss was determined as follows:

$$P_{conduction} = I_{rms}^2 \times R_{dson}$$

(3.18)

The output capacitance loss was calculated by:

$$P_{loss\_cap} = C_{oss} \times V_{in}^2 f_{sw} \times 0.5$$

(3.19)

The switching loss was calculated as follows:

$$P_{switching} = 0.5 * V_{in}^2 I_{Q2}(t_{rise} + t_{fall}) f_{sw}$$

(3.20)

The loss due to driving Q_2 is determined by:

$$P_{driver} = V_{gs2} f_{sw} Q_g \tag{3.21}$$

3.3.3 Switch Q_3

Figure 3.5 below shows the current through switch Q_3 in steady state.
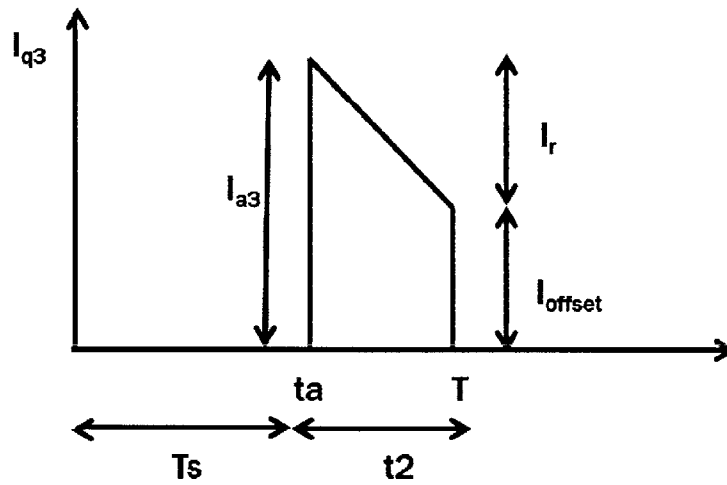
Figure 3.5: The current through switch Q_3 in steady state.

The I_{rms} current was calculated as follows:

$$I_{rms} = \sqrt{\left((I_{offset}^2 + I_{offset} \times I_r + \frac{I_r^2}{3}) \frac{t_2}{T_s} \right)} \tag{3.22}$$

Then the switch conduction loss was determined as follows:

$$P_{conduction} = I_{rms}^2 \times R_{dson} \tag{3.23}$$

The switching loss was then calculated as:

$$P_{switching} = 0.5 * V_{in}^2 I_{Q3} (t_{rise} + t_{fall}) f_{sw} \tag{3.24}$$

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Finally, the output capacitance loss was determined as follows:

$$P_{loss\_cap} = C_{oss} \times V_{in}^2 f_{sw} \times 0.5 \tag{3.25}$$

In addition, there is loss due to driving the gate of Q_3. The driver loss is given by:

$$P_{driver} = V_{gs3} f_{sw} Q_g \tag{3.26}$$

3.4 Modeled power loss results

Figure 3.6 illustrates the predicted power loss distribution by component at an output power of 8.25W. These results were obtained from the excel power loss model. Table 3.1 shows the percent contribution to the loss by each component. At this operating condition, switch Q_3 contributes to the majority of the losses (36.9%), followed by Q_2 (26.9%), and L_{out} (16.1%). The gate driver has the least amount of loss.

3.4.1 Accuracy of modeled results

Figure 3.7 compares the predicted power loss to experimental results. The model is more accurate at lighter loads than it is at full loads. As shown in the figure, the modeled efficiency at full load is slightly higher than the measured result. At such large loads, $I_{rms}^2 R$ losses due to the parasitics on the PCB board are more difficult to predict, which could explain the discrepancy in measured and modeled efficiency at full load.

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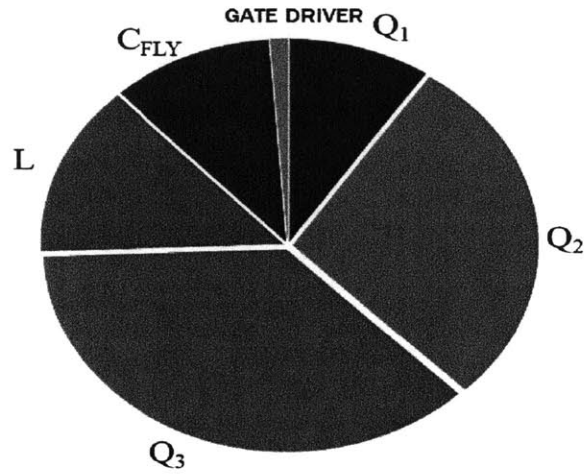
Figure 3.6: Predicted power loss distribution by component when the output power is 8.25W.

Component	Power Loss [W]	% of total power loss
Q_1	0.078	9.4
Q_2	0.223	26.9
Q_3	0.304	36.9
L_{OUT}	0.113	16.1
C_{fly}	0.089	10.7

Table 3.1: Component loss distributions predicted by the loss model.

Modeled vs. Measured Efficiency at V_{out} = 5V
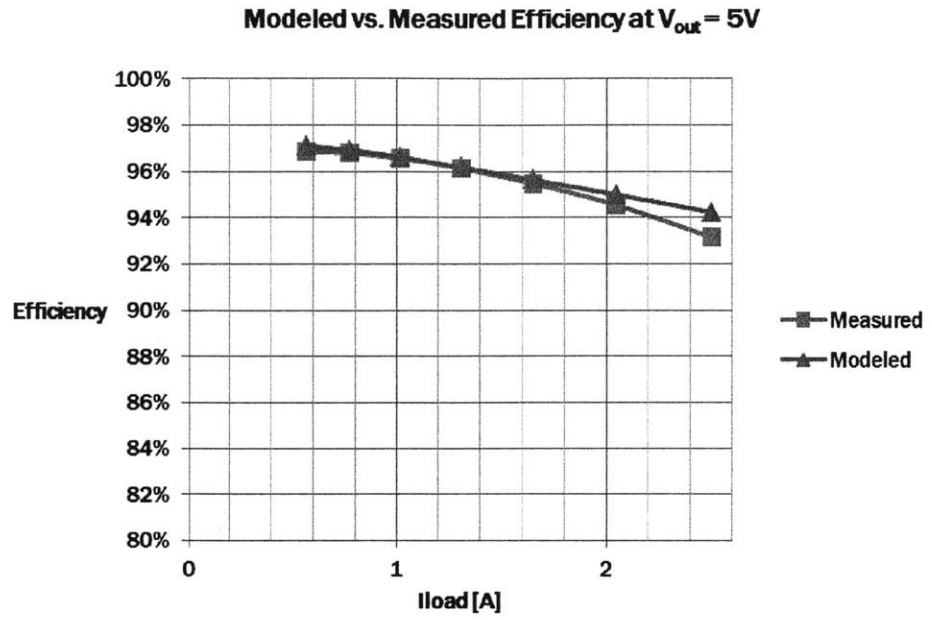
Figure 3.7: Modeled versus measured efficiency.

4. Device Selection and Sizing of Power Stage Components

In order to achieve high performance, care must be taken when selecting the components used in the power converter. The on-chip devices are sized to achieve the maximum power for a given die area with minimum loss. The off-chip components are sized to minimize loss and size for a given PCB area, as well as to achieve high performance at a given switching frequency. Section 4.1.1 details the sizing of switch on-resistance, and Section 4.1.2 discusses how the flying capacitor should be sized.

4.1 Device Selection and Sizing

4.1.1 Switch on-resistance

The experimental prototype of the 3-switch hybrid step-up power converter was designed to carry a 3A load current. The switches used were 5V/5V V_{gs}/V_{ds} isolated nmos devices. Detailed calculations were performed to determine the I_{rms} current that each of the three switches carries. Thereafter, a simulation was run to better estimate the ratios of I_{rms} current in the three switches. It was found that the switches Q_1 and Q_2 carry about the same current, whereas Q_3 carries twice the amount of current as the other two switches. Hence, the switch that carries the largest root mean square current is designed to have the smallest on-resistance, and vice versa. Once the switch current was determined, the switch on resistance was determined by the following equations:

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$$R_{sp} = R_{dson} \times Area \tag{4.1}$$

$$I_{rmsQ1} \sim I_{rmsQ2} \tag{4.2}$$

$$I_{srmsQ3} \sim 2I_{rmsQ1} \tag{4.3}$$

$$I_{rms} \sim \frac{1}{R_{dson}} \tag{4.4}$$

$$R_{dsonQ1} = R_{dsonQ2} \tag{4.5}$$

$$R_{dsonQ3} = \frac{1}{2} R_{dsonQ1} \tag{4.6}$$

Table 4.1 below summarizes the designed values of the switch on-resistance for the

experimental prototype of the 3-switch step- up power converter.

	Irms	Rdson	Area
Q_1	I_{rms1}	$40m\Omega$	$0.22mm^2$
Q_2	I_{rms1}	$40m\Omega$	$0.22mm^2$
Q_3	$2I_{rms1}$	$20m\Omega$	$0.44mm^2$
Total			$0.88mm^2$

Table 4.1: Designed values for switch on-resistance and area.

As shown in the table, the total area ocuupied by the switches is $0.88mm^2$ for an Rsp of

$\sim4*2.2\ m\Omega*mm^2$.

4.1.2 Size of the flying capacitor

The flying capacitor should be sized so that it is large enough to hold the input

voltage. However, it must not be too large so as not to have a practical application. At

the same time, the capacitor ESR should be small enough so as to minimize conduction

losses. During the phase when the capacitor charges, the on time of switches Q_2 and Q_3

must be long enough so that the capacitor is charged to the input voltage. If R_{eq} is the

resistor combination of the on-resistance of switches Q_2 and Q_3, then the on time of these

two switches should be in the neighborhood of the $R_{eq}C_{fly}$ time constant. Figure 4.1 below

shows the schematic of the converter during the charging phase of the capacitor.
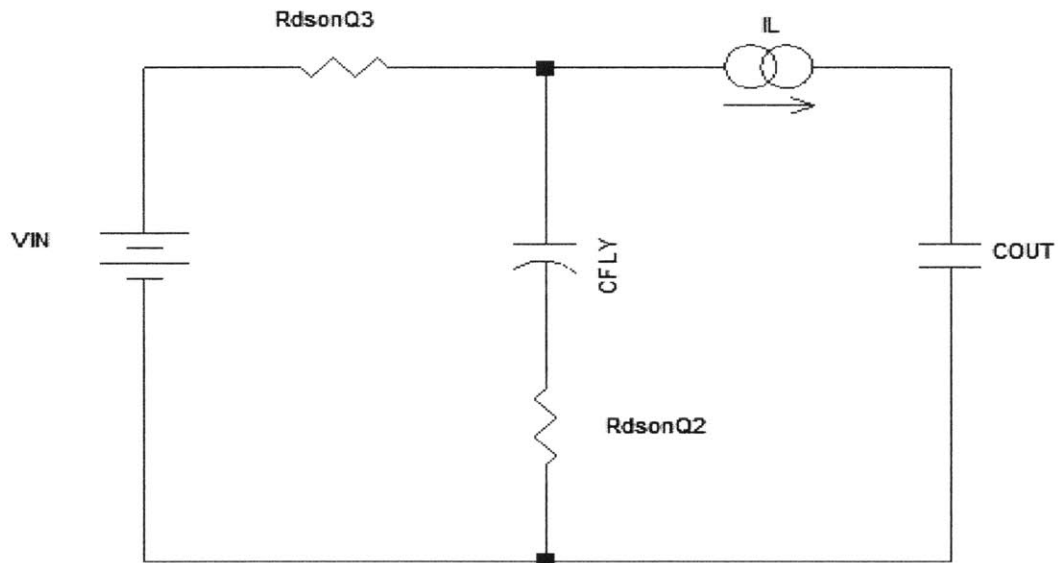
Figure 4.1: A schematic showing the charging phase of the flying capacitor. The on
time of switches Q_2 and Q_3 should be in the neighborhood of the RC time constant of
R_{dsonQ3} and R_{dsonQ2}.

Unfortunately, the actual capacitance values often differ from those stated in the

capacitor datasheet. In addition to allowing for enough charging time for the flying

capacitor, the size of the capacitor required for the experimental prototype was

determined by using the AP Instruments network analyzer and experimentally

measuring the capacitance at different bias voltages. The test chip application used a

single 10μF flying capacitor.

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5. Design and Layout

Chapters 1- 3 discussed the theory, architecture, and power loss model of the

proposed hybrid power converter. Chapter 4 then presented ways to select the

components used in the power stage. This chapter presents the design and layout of the

experimental prototype. Section 5.1 explains the layout of the power stage, followed by a

discussion of the control circuitry layout in Section 5.2.

5.1 Power Stage

5.1.1 Test Chip Layout

Figure 6.1 illustrates the pin out of the test chip and the schematic of the converter is also

shown for reference.

Figure 5.1: Left is the 3 switch hybrid test chip. To the right is the converter schematic.

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The test chip of the 3 switch hybrid step-up power converter was designed in a 0.25μm

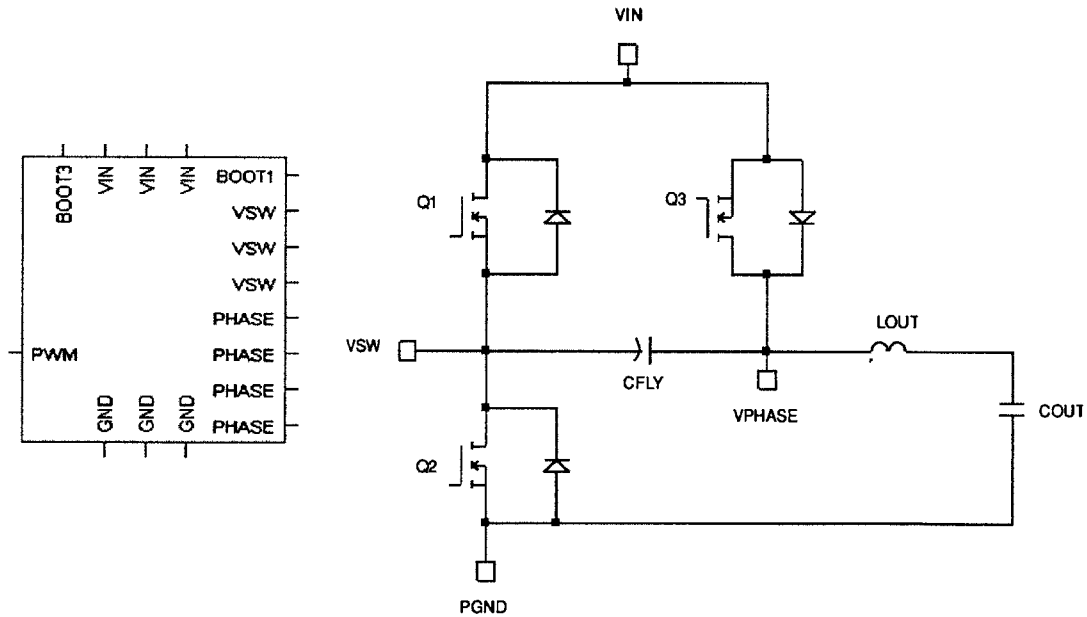5V CMOS process. Design help from Intersil Corporation was utilized. The test chip

package consists of 7 pins namely BOOT1, VIN, VSW, PHASE, GND, PWM and BOOT3.

The description of the pins is detailed in Table 5.1.

NAME	I/0	DESCRIPTION
BOOT1	I	Bootstrapped supply to the Q_1 gate for PWM enabling. A boot capacitor is connected between this pin and VSW.
BOOT3	I	Bootstrapped supply to the Q_3 gate for PWM enabling. A boot capacitor is connected between this node and VIN.
VIN	I	Power input to the device. This pin is bypassed to ground in the board layout.
VSW	O	This pin connects to the switch node of the controller. It connects the Q_1 source to the Q_2 drain.
VPHASE	O	Connects to the phase node of the converter. Connect the flying capacitor between this pin and VSW. The inductor is also connected to this pin.
PWM	-	This pin supplies the control for the switches. It is connected to an external controller for closed loop control. It can also be connected to a signal generator for open loop control.
GND	-	Ground connection to the device.

Table 5.1: A description of the pin functions of the test chip.

5.1.2 Power Stage Board Layout

The evaluation board for the test chip was designed and laid out by utilizing the

Cadence Allegro PCB design software. Figure 5.2 shows a photograph of the PCB board.

Majority of the power stage components were placed on the top side of the board using

a tight layout. Care was taken to minimize stray inductance due to the PCB traces. For

instance, components such as the input and boot capacitors were placed as close to the

IC as possible. In addition, the V_{in}, V_{out} and G_{nd} traces were wide and placed on multiple

layers to minimize PCB losses. Multiple layers were used for the G_{nd} plane to improve

thermal performance. The sensitive analog pins of the controller were placed far from

the converter. As shown in Figure 5.3, the converter was implemented using very small

components. All capacitors and resistors used were of the 0603 package size, apart from

the large electrolytic input capacitor that was placed in parallel with a smaller ceramic

input capacitor. Moreover, a single 10µF ceramic capacitor was used as the flying

capacitor and a small 0.56µH output inductor achieved minimal ripple current.
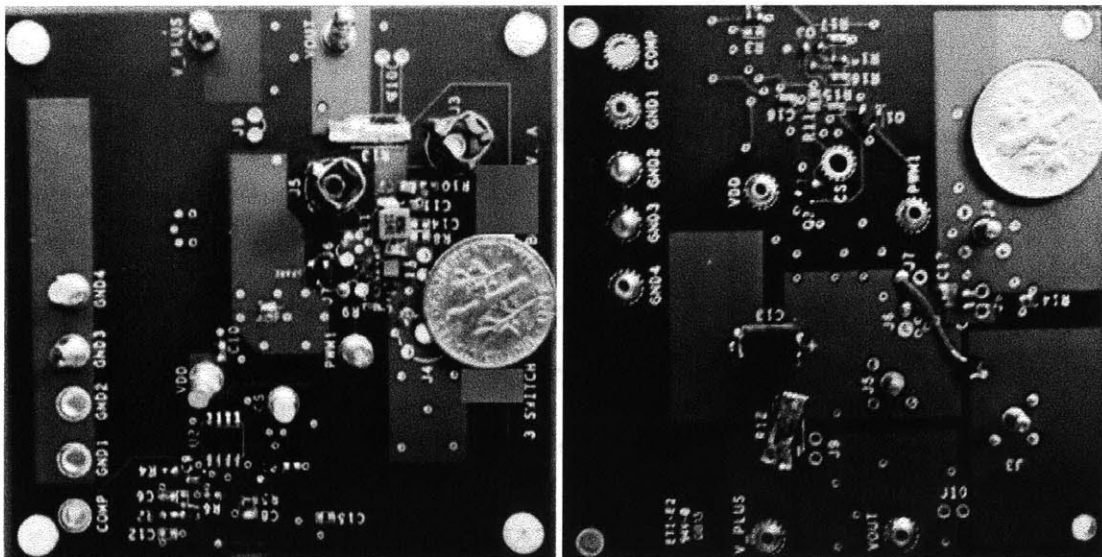
(a) Photograph of top side of the converter evaluation board with dime shown for scale.

(b) Photograph of bottom side of the converter evaluation board with dime shown for scale.

Figure 5.2: Photograph of top and bottom sides of the converter evaluation board.
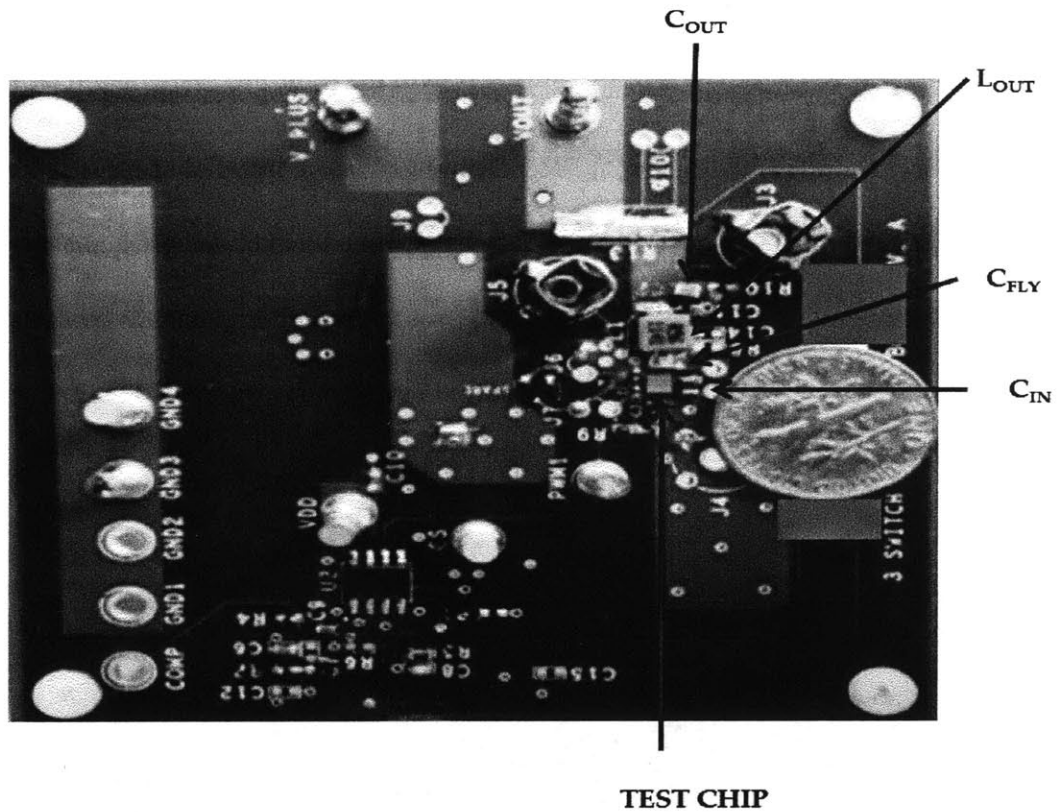
Figure 5.3: Photograph of the converter with power stage components labeled.

5.1.3 Power Stage Components

Table 5.2 shows the component values for the power stage. Ceramic capacitors are used for the flying capacitor due to their relatively low E_{sr}.

Component	Value	Package	Manufacturer
L_{OUT}	0.56μH	4020	Wurth Elektronik
C_{FLY}	10μF	0603	TDK
C_{IN}	22μF	0603	TDK
	220μF		Sanyo
C_{OUT}	22μF	0603	TDK

Table 5.2: Component values for the power stage.

5.2 Control Circuitry

The ISL6840 current mode controller provided the PWM input to the test chip and completed the feedback loop. This converter has a maximum duty cycle of 100%, which enabled its use for a wide range of conversion ratios. The control circuitry was placed on both the bottom and top sides of the board.
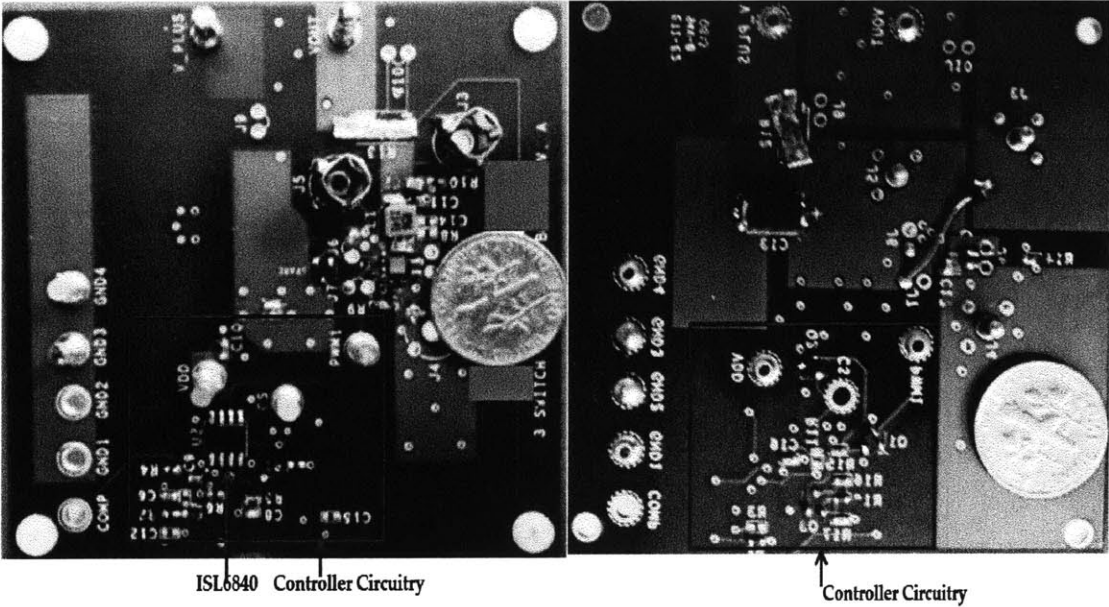
(a) Front of evaluation board with control circuitry boxed out.

(b) Back of evaluation board with control circuitry boxed out.

Figure 5.4: Photograph of the evaluation board with control circuits boxed out.

Figure 5.5 shows a layout schematic of the components of the PCB board used to evaluate the test chip. The values of the various components are displayed on the schematic.
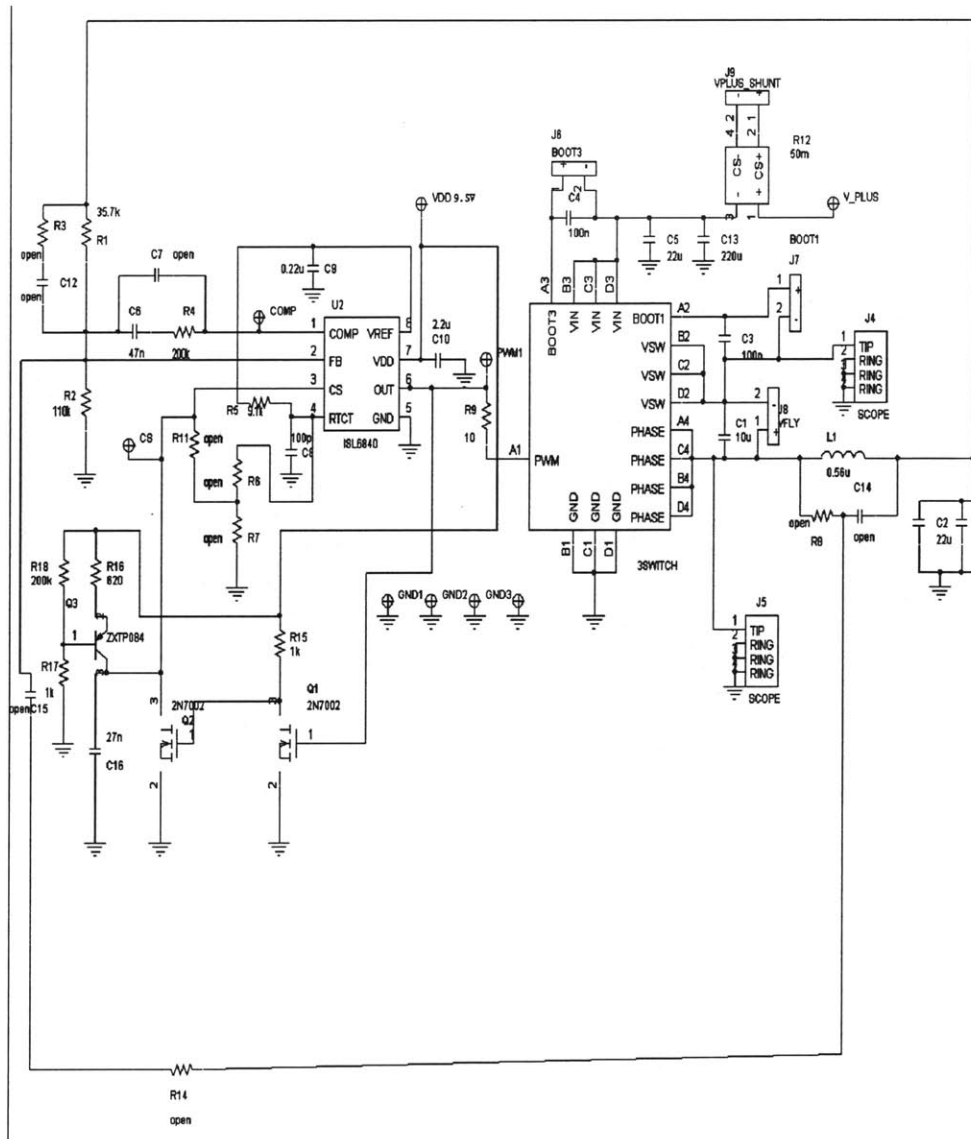

Figure 5.5: Layout schematic of the PCB board components.

6. Experimental Results

This chapter presents experimental results obtained by taking data on the test

chip of the proposed hybrid 3 switch step-up power converter. The chapter begins with

an overview of the measurement setup that was used when taking the data in Section

6.1. Section 6.2 discusses the test chip converter waveforms, followed by the power stage

efficiency (Section 6.3) and transient performance (Section 6.4). Finally, the chapter

concludes by showing experimental results of the efficiency gains obtained by the 3

switch hybrid test chip.

6.1 Measurement Setup

Figure 6.1 shows the measurement setup used when taking efficiency

measurements. A 220μF electrolytic capacitor and a 22 μF ceramic capacitor were placed

at the input of the test chip to stabilize the input voltage. The 22μF capacitor was placed

as close as possible to the input of the chip. The input voltage is provided by an Agilent

E3631A dc power supply. To measure the input voltage, an Agilent 34401A digital

multimeter in voltage mode was connected across the 22 μF input capacitor. The input

current was measured by connecting an Agilent 34401A digital multimeter in current

mode between the power supply and the input to the evaluation board. A similar setup

of two multimeters in voltage mode and current mode were used to measure the output

voltage and the output current respectively. A BK Precision electronic load was

connected to the current measuring multimeter to supply a variable load.
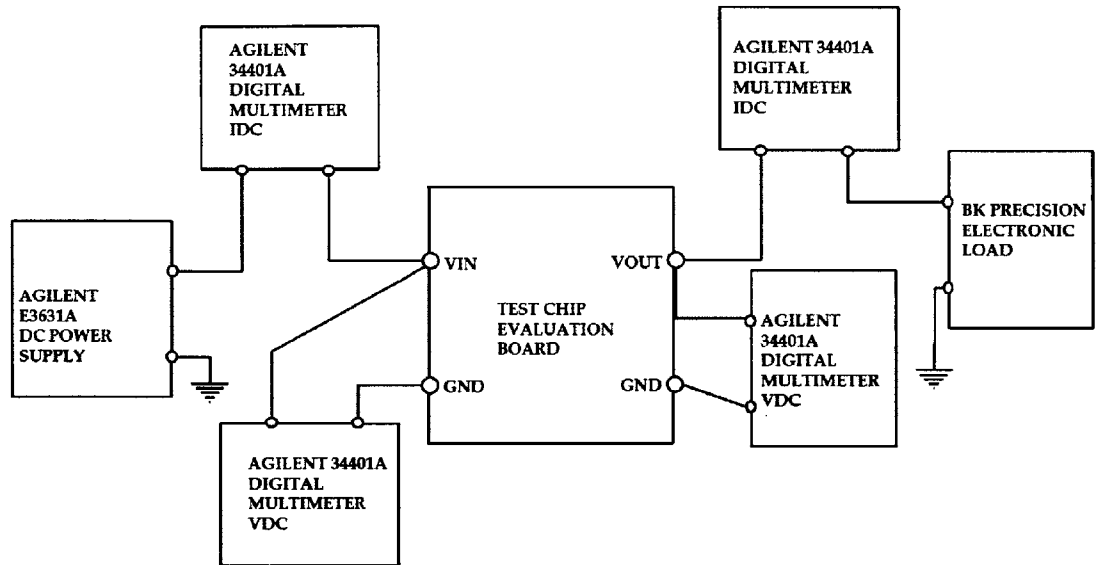
Figure 6.1: Measurement setup used to obtain efficiency measurements.

Care was taken to minimize losses caused by parasitics on the evaluation board

by minimizing the use of probe wires. The converter voltage waveforms were obtained

using the Lecroy WavePro 960 oscilloscope with 4 channels.

6.2 Converter Waveforms

6.2.1 Steady State Waveforms

Figure 6.2 shows the steady state voltage waveforms of the flying capacitor

voltage, the phase node voltage, switch node voltage and inductor current. As seen in

Figure 6.2: Steady state waveforms showing the flying capacitor voltage V_{fly}, phase node voltage V_{phase}, switch voltage V_{sw}, and inductor current I_L. The results in the top graph were obtained at no load, whereas those in the bottom graph were obtained at a 2.5A load.

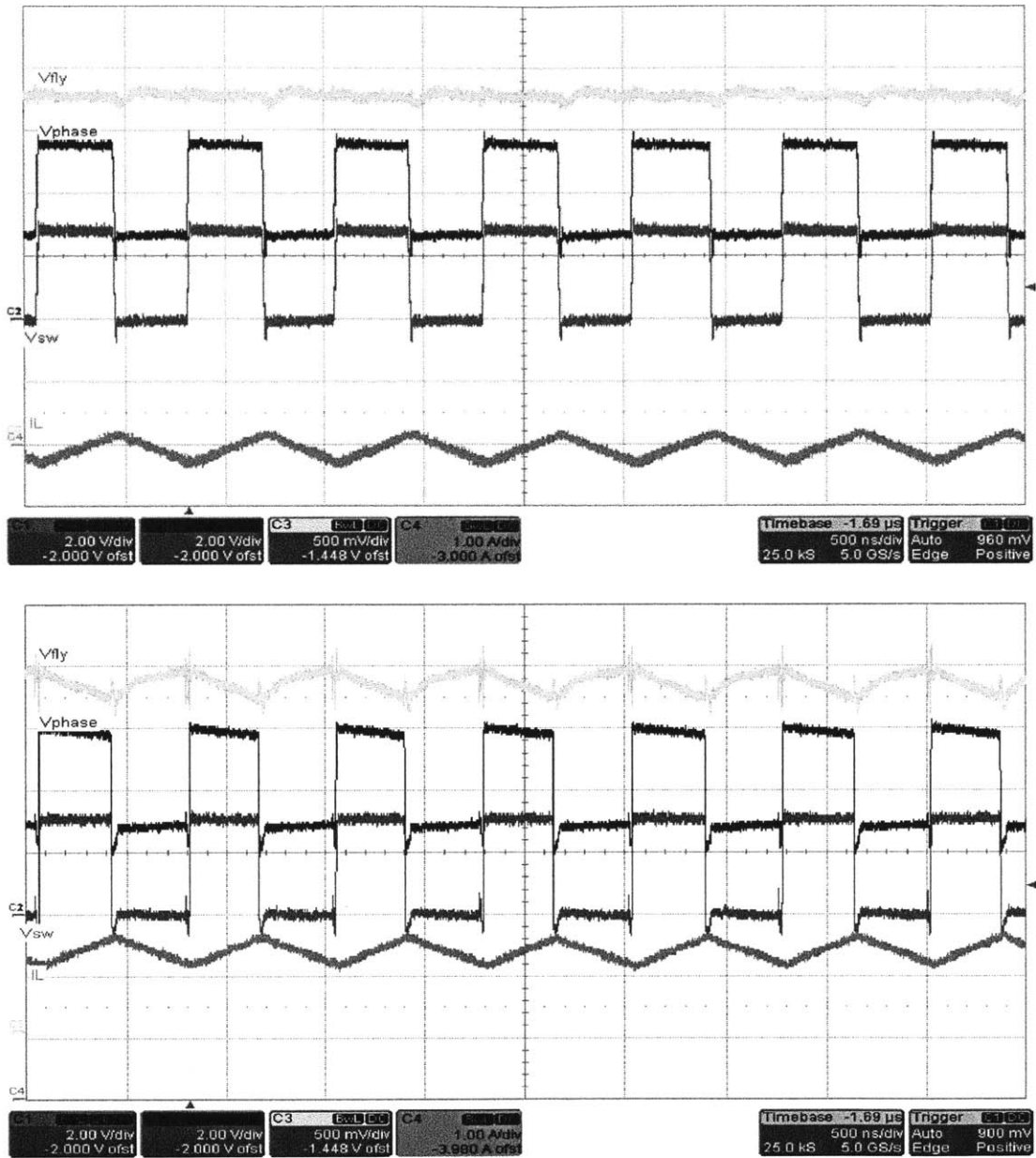in the two graphs, at no load, there is hardly any ripple in the flying capacitor voltage. As the load current increases as shown in the bottom graph of Figure 6.2, the current through the flying capacitor increases and results in a higher ΔV across the capacitor. Moreover, the higher load current causes the phase node to dip as more current is forced out of the node. The downward dip in the phase node voltage can be reduced by either using a larger size of the flying capacitor, or utilizing a capacitor with a higher voltage rating.

6.2.2 Startup waveform

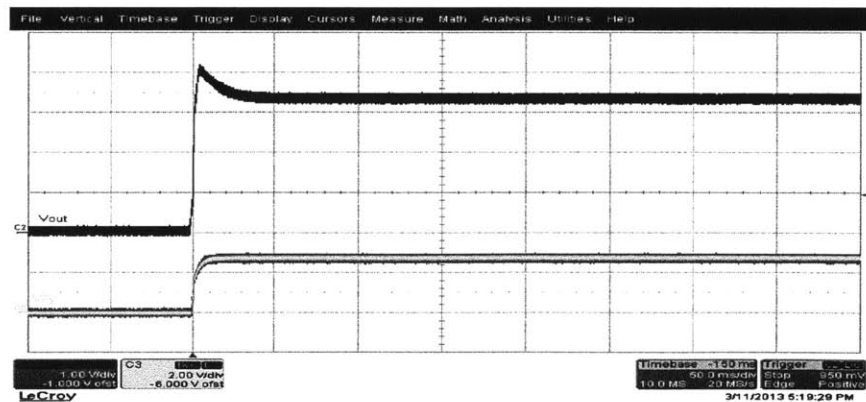Figure 6.3 below shows the output voltage and flying capacitor voltage waveforms at start up.

Figure 6.3: Startup waveforms showing the output voltage and flying capacitor voltage at startup.

6.3 Closed Loop Efficiency

All efficiency and power loss measurements were obtained at a switching

frequency of 1.25MHz. Table 6.1 below shows key component values used when taking

the efficiency data.

Component	Value	Package	Manufacturer
L_{out}	0.56μH	4020	Wurth Elektronik
L_{DCR}	16mΩ	-	-
C_{fly}	10μF	0603	TDK

Table 6.1: Key Component values for efficiency and power loss measurements.

As shown in Figure 6.6, losses increase with an increase in load current due to the rise in

the I_{rms}^2R conduction losses. As Figure 6.4 illustrates, the 3 switch hybrid step-up power

converter exhibits high efficiency even at light loads. Moreover, the converter has a peak

efficiency of 97.7%. The converter's efficiency decreases following a reduction in input

voltage due to the higher conversion ratio at low input voltages.
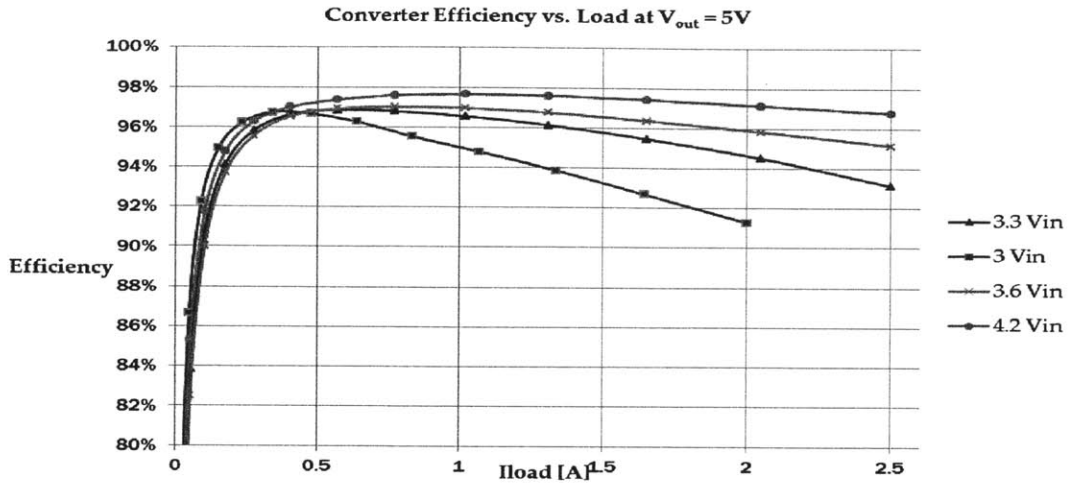
Figure 6.4: Efficiency measurements at V_{out} = 5V.
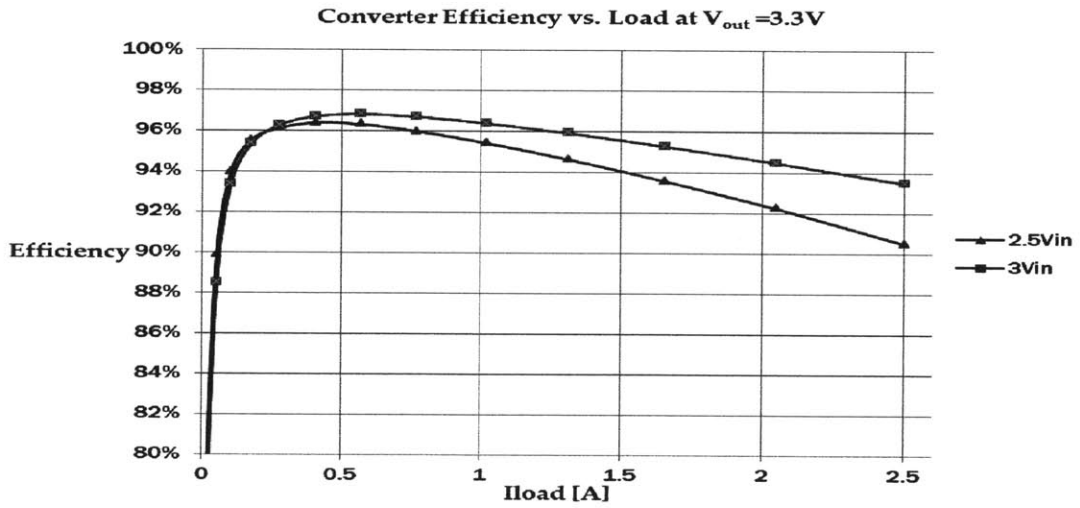
Figure 6.5: Efficiency measurements at V_{out} = 3.3V.

Converter Power Loss vs. Load at V_out =5V
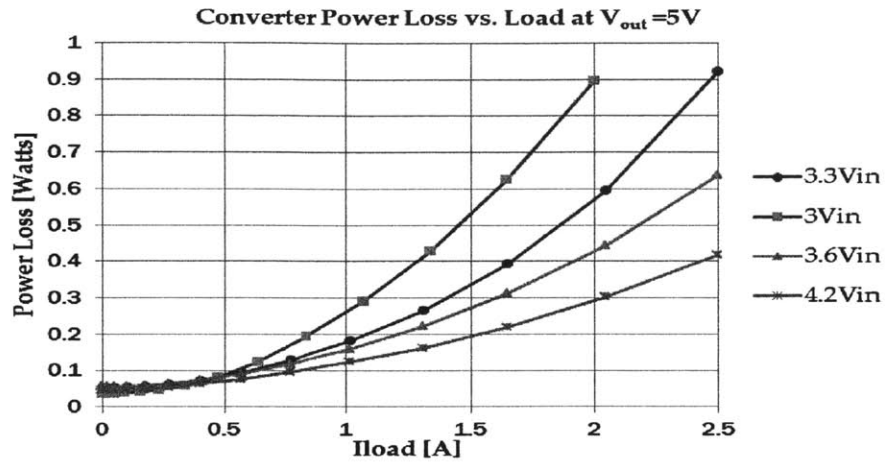
Figure 6.6: Power loss measurements at V_out = 5V.

Converter Power Loss vs. Load at V_out = 3V
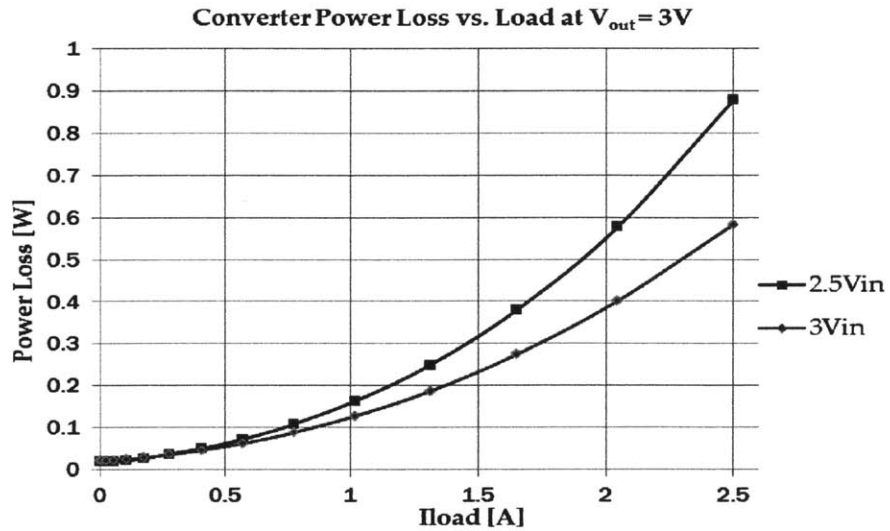
Figure 6.7: Power loss measurements at V_out = 3.3V.

We investigated the effect of the number of flying capacitors used on the power loss of

the converter. This relation is shown in Figure 6.8. Adding a second flying capacitor in

parallel with the first has no noticeable effect on light load power loss. As the load

current increased, the power loss reduced by less than 9 % at full load.

Effect of Number of Flying Capacitors on Power Loss at V_{out}=5V

Figure 6.8: Effect of number of flying capacitors used on power loss.

6.4 Transient Performance

6.4.1 Load step and step down

Figure 6.9 and 6.10 show the transient performance of the converter when the

load is changed from low to high and vice versa.

Figure 6.9: Load step up waveform.

Figure 6.10: Load step down waveform.
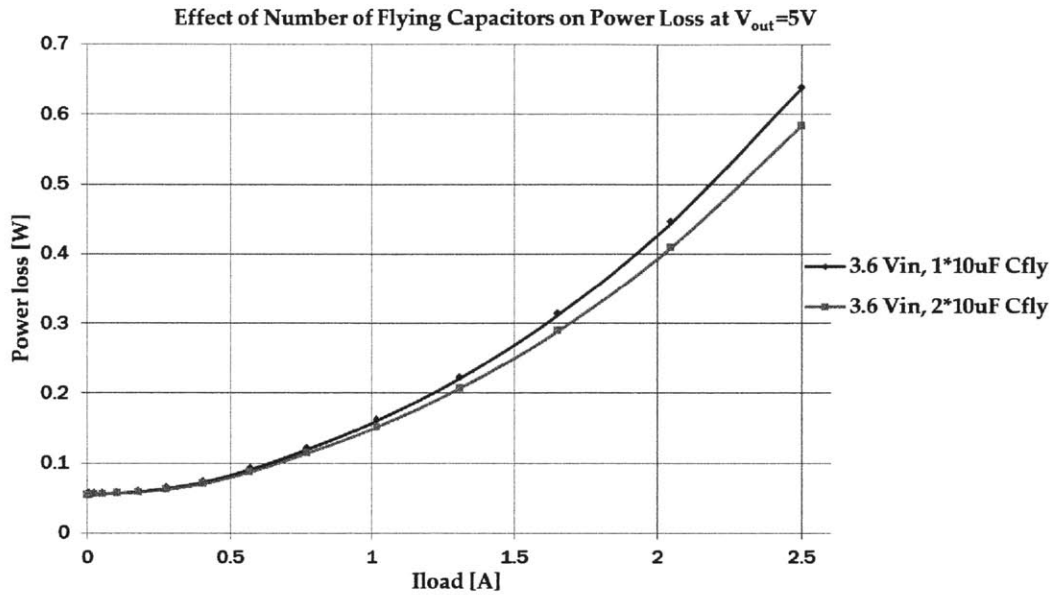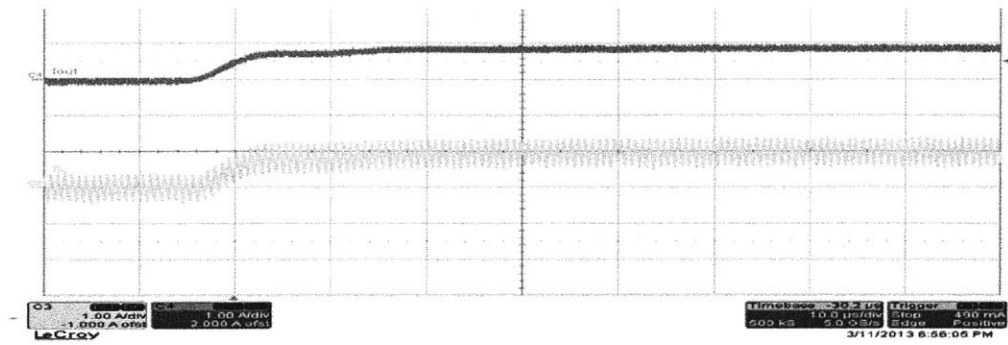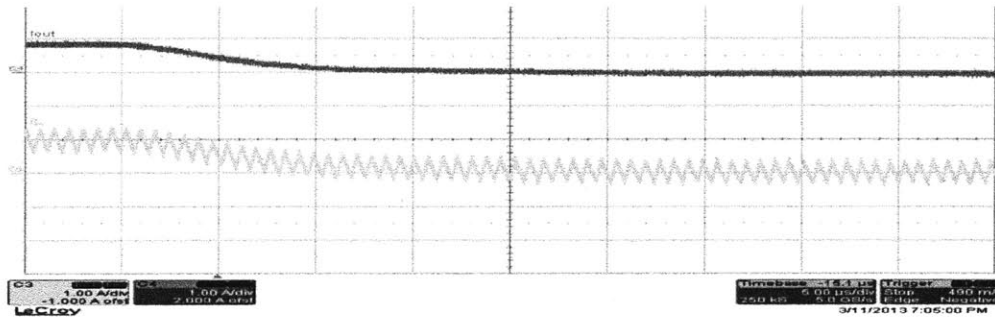
7. Summary and Conclusions

This chapter provides a summary of the thesis. Ideas for areas of improvement and future work are discussed in Section 7.2.

7.1 Thesis Summary and Contributions

This thesis presents a switched capacitor/inductor step-up power converter for small conversion ratios. The circuit offers some gains compared with the conventional boost converter. These benefits include reduced inductor size, reduced switch voltage stress and improved closed loop control while maintaining the efficiency of a boost converter of a similar IC package size. Adding a flying capacitor between the three switches reduces the voltage stress on the switches. Moreover, adding the flying capacitor reduces the required inductor size by reducing the volt-second across the inductor. A power loss model for the converter is constructed to better understand the loss mechanisms of the circuit as discussed in Chapter 3.

After an understanding of the operation and loss mechanisms, an experimental prototype of the power converter is implemented as an integrated circuit and is built in a 0.25μm 5V CMOS process. The converter has a peak efficiency of 97.7%. Moreover, it displays high efficiency at light load even without using light load efficiency enhancements schemes. A side by side comparison with the conventional boost converter shows the efficiency gains of the converter at high voltages.

7.2 Future Work

This work has detailed the analysis of a switched capacitor/inductor step-up power converter and demonstrated its gains through experimental verification. Further improvements on the converter can be realized by enhancing the efficiency further. For instance, techniques such as low load enhancements may be applied to the converter to increase its efficiency. The proposed converter of this thesis belongs to a class of circuits that comprises of a three switch plus inductor unit that can be arranged to form step-up, step-down and inverting configurations. Further work will investigate the step-down and inverting configurations of the class of circuits.

Appendix A: Efficiency Comparison with a Conventional Boost Converter

Earlier work showed a side by side efficiency comparison of the three switch hybrid step-up converter and the conventional boost converter. An experimental prototype of the hybrid three switch converter was constructed to demonstrate its gains over the conventional boost converter. It was built using the ISL85400 buck converter IC made by Intersil Corp. The third switch, Q_3 was implemented using a B340B shottky diode manufactured by Diodes Incorporated that has a forward voltage drop of 0.6V. Similarly, the boost converter was implemented using the ISL86401 boost converter IC made by Intersil Corp. The ISL85400 and ISL86401 IC's have the same switch on resistance for the high side and low side MOSFET's ($450m\Omega$ and $250m\Omega$ respectively). These two IC's were used to ensure that a side by side comparison of the hybrid three switch and conventional boost converter was achieved.

The efficiency of the two converters was observed with the inductor ripple current kept constant, and the results are compared in Figure A.1. It is observed that the hybrid converter has higher efficiency than the conventional boost converter.

Efficiency comparison of conventional boost and 3-switch
hybrid step-up converter
V_{out} =36V, V_{in} =24V
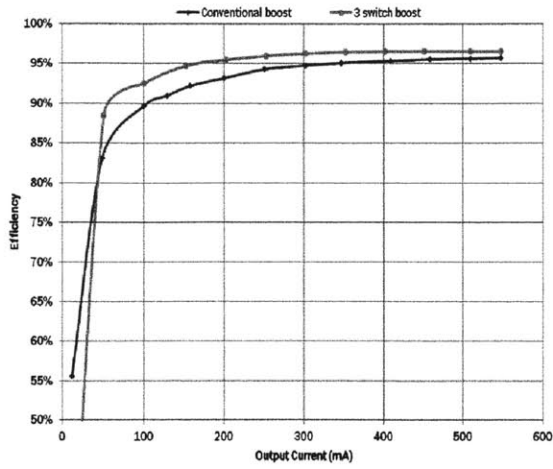
Power loss comparison of conventional boost and 3-switch
hybrid step-up converter
V_{out} =36V, V_{in} =24V
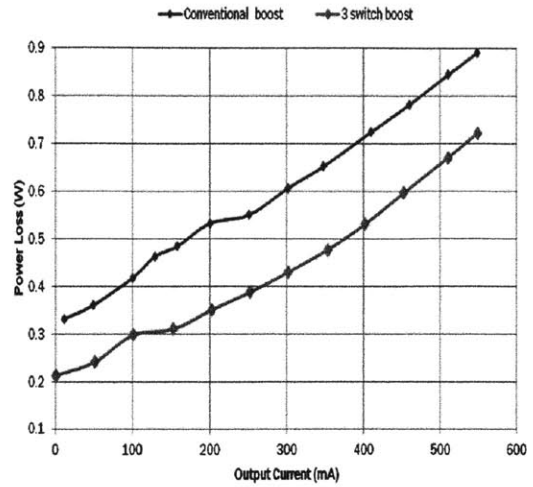
Figure A.1: Power loss comparison of the conventional boost converter and the 3 switch hybrid step-up power converter

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Appendix B: Inductor Conduction Loss Comparison

In Figure B.1, the inductor and switching frequency were kept constant and the conduction loss in the hybrid three switch and conventional boost converter were compared. When the converters operate at the same frequency, the inductor in the conventional boost carries higher average current, as well as higher ripple current, which results in higher losses.

Comparison of Inductor Conduction Loss
$V_{out} = 3.3V, f_{sw} = 1.25\,MHz$

Figure B.1: Comparison of inductor conduction loss of the proposed converter and the conventional boost converter.

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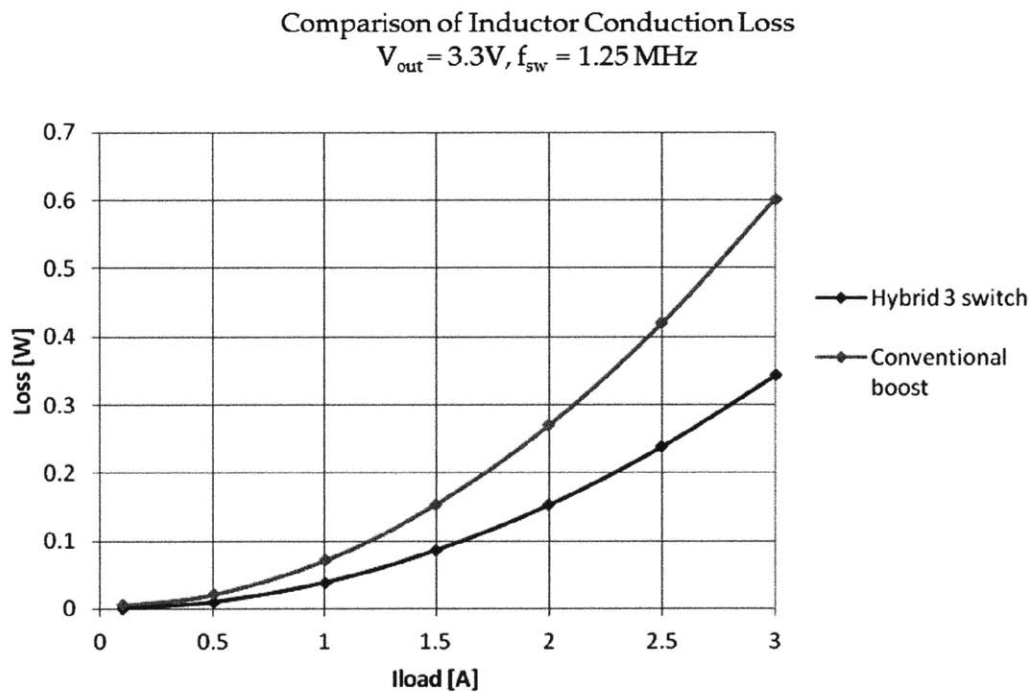[1]   J. Robert C.N. Pillawa-Podgurski, David M. Giuliano and David J. Perreault, "Merged Two-Stage power converter architecture with soft charging switched-capacitor energy transfer," in Power Electronics Specialists Conference, 2008. PESC 2008. IEEE.

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