A Merged Two-Stage Converter for LED Lighting Applications

by

John Ranson

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Abstract

Light Emitting Diodes (LEDs) are a very promising technology for developing more efficient lighting. For high-efficiency applications, a switching current regulator is necessary to control the power drawn by an LED string. This thesis investigates a merged two-stage LED driver for lighting applications, with a switched capacitor (SC) voltage preregulator and a HF resonant-transition inverted buck current regulator. The design, analysis and implementation of the HF stage are developed in detail, and a full merged two-stage system is implimented based on a SC stage pulled heavily from the work of Seungbum Lim.

Thesis Supervisor: David J. Perreault
Title: Professor

Acknowledgments

First and foremost, I would like to thank Prof. David Perrault, who has been an excellent, supportive advisor, and who made this project happen. I also give thanks to Seungbum Lim for putting an amazing amount of work into the design of the switched capacitor circuit. The whole ARPA-E project team deserves recognition; their work is foundation of this project. Finally, I must thank my lovely wife, Bertha Tang, for putting up with me through grad school and pushing me forward when I needed it.

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Chapter 1

Introduction

In the push toward energy efficient lighting, the trend has been toward replacing incandescent bulbs with more efficient technologies. As of 2009, CFLs were the dominant replacement for incandescents, having 16% of the standard screwbase lightbulb market[3]. CFLs suffer from a number of problems, such as limited dimmability, slow start times, poor low temperature operation, poor lifetime with frequent on-off cycles, substantial mercury content, and fragility. These problems motivate finding an improved alternative. LEDs are a promising replacement for incandescents and CFLs. They are potentially more efficient than CFLs, they turn on instantly even at low temperature, their lifespan is unaffected by usage pattern, they contain no mercury, and they're highly resistant to shock.

A downside to LEDs is that they are DC current controlled devices, and cannot be directly powered from voltage sources such as standard line power. Switched-mode LED drivers provide an efficient means to convert power from a voltage source into a controlled form usable by LEDs. However, existing LED driver designs operate at low frequency and consequently require large capacitors and magnetic devices. These large devices make it more difficult, from a size and cost perspective, to use LED modules as replacements for existing incandescent or compact-fluoroescent lightbulbs. This motivates this work to improve the state of art in LED drivers.

Chapter 2

Background

2.1 LEDs

White LEDs can produce light with extremely high luminous efficacy. To date, the highest achieved efficacy for a white LED is 254 lumens per watt[4], well over 10 times the efficacy of incandescent lighting. For comparison, ceramic metal halide lighting, the most efficient alternative commercially available white lighting technology, generally has a lamp efficacy of 80-125 lumens per watt. Fluorescent lighting tops out at about 100 lumens per watt[5]. Hence, there is significant potential for LEDs to outperform existing technologies in luminaire applications.

The current in an LED is ideally exponentially related to the product of the forward voltage and the reciprocal of the absolute temperature. Typically, in operation, the LED voltage remains near a fixed value, V_F, for a large range of currents. Increasing junction temperature decreases V_F for a given current[18]. With this behavior, applying a fixed voltage across an LED create a positive feedback loop between junction temperature and current, leading to thermal runaway and potentially destroying the device. This necessitates controlling LED current instead of LED voltage.

In most off-line luminaire applications, LEDs are connected in series to have a string voltage of 20V-40V[8]. The primary reason for doing this is reducing the voltage step-down necessary to power the string from line voltage. However, there are two other advantages to this arrangement. LEDs tends to lose luminous efficacy

with increasing current. For the same light output, it is less efficient to power a single LED at high current than several LEDs at lower current. Futhermore, because individual LEDs have non-uniform light distribution, using multiple LEDs enables better light distribution without a lossy diffuser.

2.2 Gallium Nitride Active Devices

Gallium Nitride (GaN) is a 3-5 semiconductor that is the subject of active research. By a number of metrics, it has substantially greater potential than silicon for high power applications. It has large bandgap, high saturation velocity, large breakdown field, high electron mobility, high thermal conductivity, good sheet carrier concentration. Together, these characteristics are allowing the development of devices that can switch high voltages and high currents with fast transients while operating at high temperature[13].

The major downside of present-day power devices based on Gallium Nitride is an effect known as dynamic on-state resistance. The on-state resistance in GaN HEMT is a function of the previously applied drain voltage. The resistance increases when a large drain voltage is applied to the device, and decays back to the DC value when the voltage is removed. The time constants for this decay vary on the submicrosecond to minute range[10]. Unfortunately, in any switching application where voltage is reapplied to the device at smaller intervals than the time constant, the on resistance never returns to its DC value.

Research being done by the groups of Prof. Tomas Palacios and Prof. Jesus del Alamo to create GaN devices optimized for switching converters. Ideally, these devices will have small dynamic on resistance, high breakdown voltages, and will operating in enhancement mode. These devices are not yet available, but satisfactory commercial devices exist.

2.3 Advanced Magnetics

Several research teams at MIT, Dartmouth, U. Penn, and Georgia Tech are working on creating very small inductors for operation for high frequency power applications. Two approaches are being taken: creating small air-core or magnetic core toroids using IC fabrication techniques, and creating "racetrack" inductors using thin-film magnetic nanomaterials. These devices further shrink the potential size of converters operating in the 5-30MHz range, and while not yet available, the topology in this thesis was picked to allow these new technologies to be exploited when they are fully realized.

2.4 Problems with current designs.

The state of the art in commercial LED drivers for lighting applications suffers from several problems, including high cost, low power density, low power efficiency, and low power factor[15]. A number of factors play into these problems. A survey of designs from literature is found in Appendix E.

2.4.1 Operating Frequency

Switching circuit losses can be divided into three parts: semiconductor device losses, passive device losses, and control losses. There are two major sources of semiconductor device loss in switching power converters. Conduction loss is the power loss due to current flowing through the devices. Switching loss is the power loss that occurs when a switch turns on or off. Power is dissipated in a switching event when a device experiences simultaneous high voltage and high current due to finite switching speed, or when a parasitic capacitance is discharged through the switch resistance. Under some conditions, other sources of loss, such as device leakage, may also be significant.

Passive device losses can come from a variety of sources. Again, all devices seem some parasitic resistance that causes conduction loss. The skin effect can cause significant losses where ripple current is high. Eddy losses and hysteresis losses in magnetic

materials increase with frequency and field strength. Dissipation in the dielectric and leakage can cause loss in capacitors. In general, each passive device creates some DC loss, and presents some Q to the component frequencies of the carried current.

Current designs for off-line LED drivers operate at relatively low frequencies, e.g. 50- 100kHz. Operating at low frequency reduces switching loss and magnetics loss significantly, allowing optimization to reduce conduction loss. Unfortunately, operating a low frequency means that the reactive elements in the power converter and filter have to be large-valued, and hence physically large. For example, two LED drivers found in commercially available lightbulbs have switching frequencies in the range of 50-100kHz, power densities of $3.66W/in^3$ and $4.76W/in^3$, with efficiencies of 65% and 88%. A 25W converter with this power density would take 5-$7in^3$ for the power circuitry alone.

2.4.2 Flicker

Light flicker can be a big problem in LEDs. 60Hz and 120Hz flicker, while beyond the flicker fusion threshold of our conscious vision, still affect the mechanisms of our eyes, changing pupil dialation and causing headaches, eyestrain and nausea in sensitive people. LEDs respond very quickly to input power changes, so any 60Hz or 120Hz ripple in current shows up as flicker at the output. Many current designs use input-side boost power factor correction (PFC) circuits, which inherently eliminate this problem by placing large energy storage on the intermediate voltage. While effective, this solution pays a large penalty in size, complexity and cost.

Chapter 3

Design

3.1 Target Specifications

There were two related design goals in this project. The first goal was to make an high frequency (HF) (3 - 30MHz) switching DC LED driver that could operate from 100V, drive tens of Watts into a 30-40V load, and achieve greater than 90% efficiency. The second goal was to take this design and leverage it in a system that runs from ac line voltage, to create an ac-line LED driver that has a power factor greater than 0.9 and an efficiency of approximately 90%. These specs are summarized in Table 3.1.

Table 3.1: Target Specifications

Parameter	DC Specification	AC Specification
Input Voltage Range	50V-100V	$120\text{VAC}_{RMS} \pm 10\%$
Target Output Voltage	30-40V	
Operating Frequency	>5MHz	
Output Power	Around 25W Peak	Around 10W
Power Factor	-	> 0.9
Efficiency	>90%	

3.2 Design Considerations

3.2.1 High Frequency Operation

Passives in switching circuits generally scale down in size as the frequency of operation increases. At higher switching frequencies, smaller-valued capacitors and inductors can be used to achieve the same impedances. This allows reduction in the size of the main passives and also any necessary input filter. HF operation generally also allows a much faster control loop, giving faster transient response. Using advanced magnetics provides another reason for HF operation. In many cases, their optimal operating points are in the range of 5-30MHz.

Zero Voltage Switching

High frequency operation comes with the downside that the design must keep switching losses at a minimum. Switching loss can be broken down into overlap loss, where active devices carry simultaneous high voltage and current, and capacitive discharge loss, where capacitances are discharged through a switch on turn-on. Zero voltage switching (ZVS) mitigates both of these problems. In this paradigm, the active devices only turn on or off when they have zero, or near-zero voltage maintained across them. Even if they're switching substantial current, the overlap loss is low, because the V term is small in the IV product. Reducing the turn-on voltage causes a square-law reduction in capacitive discharge loss, because the loss is $\frac{1}{2}CV^2$ per cycle. It should be mentioned that ZVS is a means to reduced loss, not an end, and losses such as those due to non-zero voltage at turn-on may be traded for decreased losses elsewhere.

3.2.2 Preregulation

Limits of resonant operation

In order to achieve ZVS at device turn on, soft-switched converters often rely on resonant behavior for part of the switching cycle to make the switch voltages fall

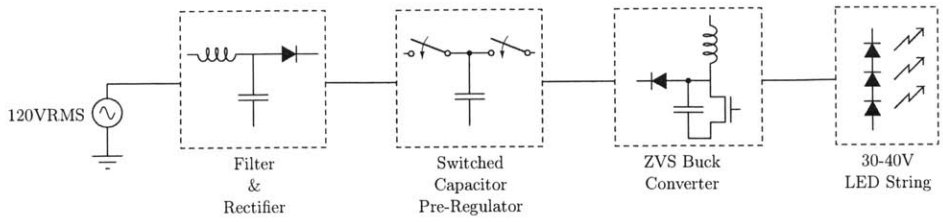


Figure 3-1: Complete system architecture

to zero before switch turn-on events. Generally, this places a limiting relationship between the characteristic impedance of the passive network and the amount of power that is drawn by the load. In the case of a converter operating from high voltage but delivering low power, the characteristic impedance $Z_o = \sqrt{\frac{L}{C}}$ is large. However given operation at high frequency, $\omega_0 = \frac{1}{\sqrt{LC}}$ has to be larger than the operating frequency. Taken together, these constraints generally require a large-valued L and small-valued C. However, at high frequency, most magnetic materials are very lossy, so it's unreasonable to use values much larger than $1\mu H$, if we're aiming for a compact design. Assuming an resonably small switch capacitance of 100pF, we can expect an approximate $Z_o = 100\Omega$, which would draw a substantial amount of power from line voltages.

With this in mind, for AC operation above 100V, we chose a two stage design, where a low frequency switched capacitor preregulator stage transforms the input voltage to a lower intermediate level, from which the HF stage is operated. This relaxes the requirement of high characteristic impedance for the second HF stage. This has the further advantages of reducing the voltage stress on the HF stage switching devices and reducing the difficulty of achieving ZVS in our chosen topology. We picked a switched capacitor design because it requires no magnetics, needs only moderate capacitances, achieves high power density, and when used simply as a transformer, it achieves very high efficiency. The complete system architecture is shown in Figure 3-1.

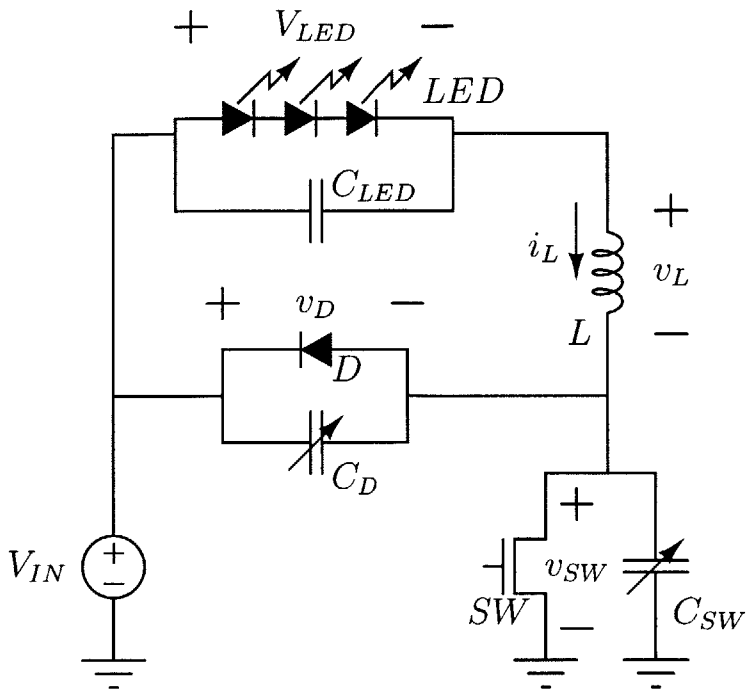


Figure 3-2: Basic HF stage circuit topology

3.3 Resonant transition, critical conduction mode, inverted buck converter

The topology chosen for the HF stage is shown in Figure 3-2, with the circuit operating waveforms shown in Figure 3-3. It is topologically equivalent to a buck converter, with the switch referenced to ground and the load referenced to the supply. By inverted, it is meant that the converter is designed with "common positives", such that the switch is referenced to ground. The inductor current falls to zero on every cycle, and except during resonant switching transitions, one of the diode or switch is always conducting. Not considering differences in control and some design aspects, for a good portion of the operating range the topology acts much like a Quasi-Square-Wave ZVS buck converter[19] with a low ratio of switching to resonant frequency.

This topology was chosen for several reasons. Unlike a standard buck, the gate drive is ground referenced, greatly simplifying HF operation. It has a minimal component count. Correct operation is possible using the intrinisic capacitances of the

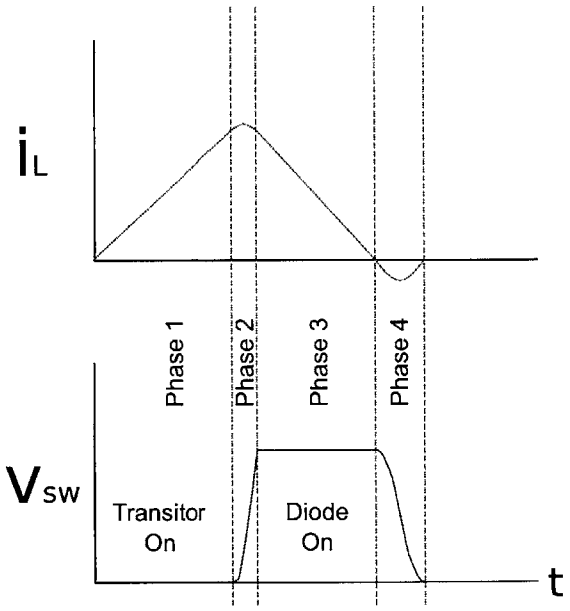


Figure 3-3: Simplified inductor current and transistor drain voltage

active devices and a single inductor. For given input and output voltages, power is essentially linear with on time.

3.3.1 Phases of Operation

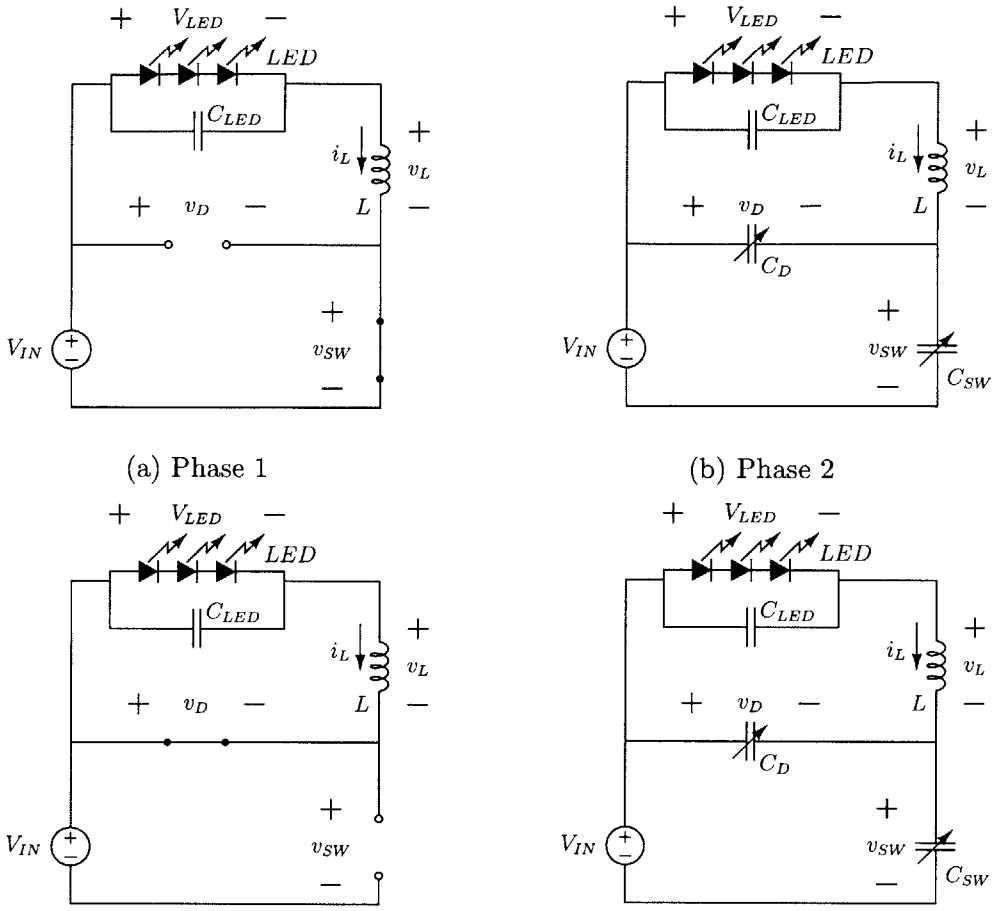
There are four phases to the operation of the converter, depending on the direction of current flow and the state of the active devices. Figure 3-4 shows simplified circuits for each phase. Figure 3-3 shows the current during these periods.

Phase 1

At the beginning of phase one, v_{SW} is near 0V and i_L is zero or slightly negative. Switch SW turns on and i_L ramps up linearly.

Phase 2

After T_{on}, switch SW turns off. i_L immediately starts charging C_{SW} and C_D. Since C_{SW} is large when v_{SW} is small, v_{SW} increase slowly as the switch turns off, achieving ZVS on turn-off. Through the remainder of this phase, i_L charges up the capacitors



(a) Phase 1

(b) Phase 2

(c) Phase 3

(d) Phase 4

Figure 3-4: Simplified circuits for each phase of operation

until v_{SW} exceeds V_{IN}.

Phase 3

Once v_{SW} exceeds V_{IN}, diode D turns on, and i_L linearly ramps down to 0A.

Phase 4

In the final phase, diode D turns off as i_L goes negative. i_L now discharges C_{SW} and C_D. Generally both C_{SW} and C_D are nonlinear capacitors that decrease in capacitance as their bias voltages increase. If C_D is sufficiently large and nonlinear, it injects enough charge into L when $v_L > 0$ to ring v_{SW} to 0V in preparation for

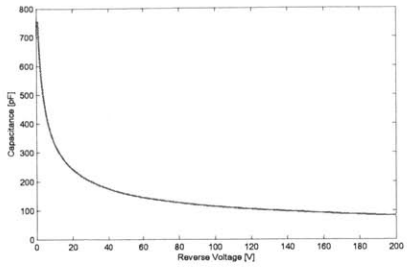


Figure 3-5: Example diode capacitance curve. (Cree C2D20120D)

a zero-voltage turn on of the switch and the start of phase 1. Even if the diode capacitance is insufficiently nonlinear to achieve zero voltage switching, switching at the minimum voltage point conserves significant energy relative to hard switching. Figure 3-5 shows the capacitance curve of a Cree C2D20120D SiC diode, which can be used to this end. It exhibits standard abrupt-junction diode capacitance behavior.

3.3.2 Current and Power

As can be seen in Figure 3-3, the peak current is roughly proportional to the transistor on-time. This is because there is a fixed voltage, $(V_{IN} - V_{LED})$, across the inductor during the switch on state. Ignoring the effect of phases 2 and 4, the peak current should be $t_{on}(V_{IN} - V_{LED})/L$. Because the current waveform approximates a triangle wave, it can be said that the average current is is 1/2 of the peak current, or $(V_{IN} - V_{LED})/(2L)$. Because the LED voltage is constant, the output power becomes $(V_{IN} - V_{LED})(V_{LED})/(2L)$. This relationship is approximately true when the on-time is large relative to the times spent in the resonant phases. At smaller on-times, the power delivered becomes highly affected by the nature of the nonlinear capacitances, and is best calculated from simulation.

3.3.3 Operating Frequency

With the selected control technique, the converter operates with variable switching frequency. The period of operation can be estimated, again ignoring phases 2 and 4, by looking at the time it takes to ramp down the current during phase 3. It can

be shown that this time is equal to $t_{on}(V_{IN} - V_{LED})/V_{LED}$. Adding this to the on-time, we find that the total cycle time is approximately $t_{on}V_{IN}/V_{LED}$. In high input voltage and high power operation, where we don't achieve ZVS, we can improve this approximation. In high power operation, the current at the beginning of phase 2 is high. The time it takes to charge the non-linear capacitors will be correspondingly small. Hence, we can ignore Phase 2 at the price of an error that decreases with power. The amount of time spent in Phase 4 is on half of a period of the nonlinear LC circuit. This is independent of on-time, and can be calculated numerically based solely on V_{IN}, V_{LED}, L, C_{SW} and C_{DI}. This is demonstrated in the MATLAB code in Appendix C.1.3. By adding these terms together, we get a reasonable approximation of the period, valid for high voltage, high power operation.

3.3.4 Achieving ZVS

The main design challenge for this converter is achieving ZVS on turn-on. The input voltage, the LED voltage, and $C_{SW}(v)$, the switch capacitance function, together set the requirement on $C_{DI}(v)$, the diode capacitance function needed in order to achieve zero voltage turn-on of the switch. Equation 3.1, derived from energy conservation in the inductor as the voltage swings, shows this relation. Equation 3.2 is a simpler restatement of this criteria. So long as this contraint is met, the converter will operate in ZVS. For linear capacitors C_{SW} and C_{DI}, this reduces to $V_{IN} < 2V_{LED}$, independent of the actual capacitance values.

$$\int_{0V}^{V_{IN}} \left(C_{SW}(v_{SW}) + C_{DI}(V_{IN} - v_{SW})\right) \left(v_{SW} - (V_{IN} - V_{LED})\right) dv_{SW} > 0 \tag{3.1}$$

$$\int_{0V}^{V_{IN}} C_{SW}(v_{SW}) \left(V_{IN} - V_{LED} - v_{SW}\right) dv_{SW} < \int_{0V}^{V_{IN}} C_{DI}(v_{DI}) \left(V_{LED} - v_{DI}\right) dv_{DI} \tag{3.2}$$

ZVS Exploiting Buck Diode Reverse Recovery

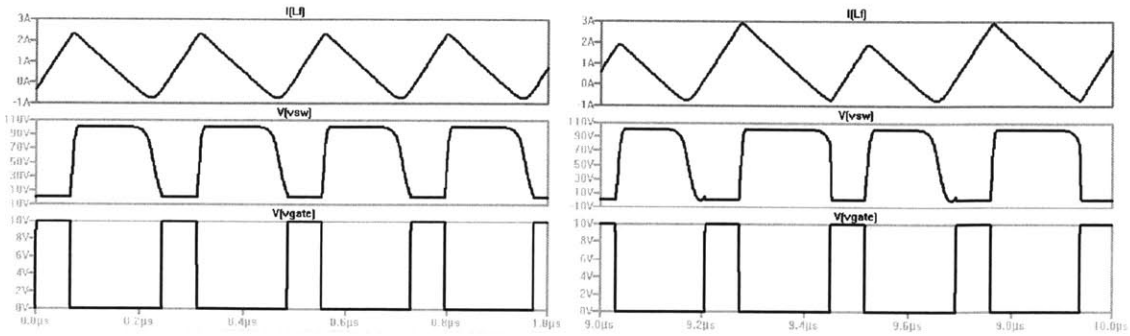
An alternative method of achieving zero voltage switching during turn-on uses the reverse recovery charge of the buck diode. At the end of Phase 3 of the converter cycle, the buck diode turns off. As the diode turns off, it injects its reverse recovery charge (Q_{RR}), into the inductor. This charge adds energy to the inductor, and increases the magnitude of swing of the switch voltage toward ground. If the following constraint is met, the converter switch will achieve ZVS turn-on.

$$\int_{0V}^{V_{IN}} C_{SW}(v_{SW})\,(V_{IN} - V_{LED} - v_{SW})\,dv_{SW} < Q_{RR} \times (V_{IN} - V_{LED}) + \int_{0V}^{V_{IN}} C_{DI}(v_{DI})\,(V_{LED} - v_{DI})\,dv_{DI} \tag{3.3}$$

Challenges with utilizing reverse recovery include variations in Q_{RR} with temperature, current and $\frac{di}{dt}$ (determined by voltage), and the fact that reverse recovery characteristics may not be well controlled in many devices. Reverse recovery may be use in tandem with nonlinear capacitance to achieve ZVS over a wider range than either could alone.

Non-ideal Input Voltages

Most designs will not have perfectly tuned capacitances that balance Equation 3.1. When the input voltage is too high, the drain voltage does not ring completely down to zero volts after the diode turns off. In this circumstance, the best behavior is to turn the transistor on when the voltage is at a minimum. Even though the device is still hard switched, ignoring nonlinearities, the amount of energy lost per transition is reduced by the square of the ratio of the switching voltage to the input voltage. Thus, when the input is too high for true zero-voltage turn-on soft switching of the transistor, we can still achieve relatively low loss. Conversely, when the input voltage is low, the transistor will switch on with zero drain voltage, but the switch



(a) Correct behavior (b) Two cycle oscillation

Figure 3-6: Simulations showing inconsistent converter behavior with identical fixed duty cycle drives.

carries negative current for a short time. Depending on the nature of the controls, this may mean that the intrinsic diode of the transistor turns on for a short while before the transistor gate is turned on, and there may be loss implications from this. Furthermore, because the transitor turns on with negative current, there no longer is a close relationship between the transistor on-time and the peak current through the inductor.

3.3.5 Control

The power drawn by the HF stage is controlled by the transistor on-time and the intermediate voltage. The control architecture of this circuit went through three design iterations, each of which gave some very useful information about the circuit behavior.

Duty Cycle Control

In the original design, the gate drive signal of the HF stage was generated off board by a signal generator. The signal generator produced a square wave that was hand tuned to have the right duty-ratio for each input voltage. However, just applying the correct duty ratio was insufficient for reliable operation. The converter can fall into a two-cycle oscillation which can damage the converter at high power. The behavior was reproduced in simulation, as shown in Figure 3-6, and the origin was diagnosed.

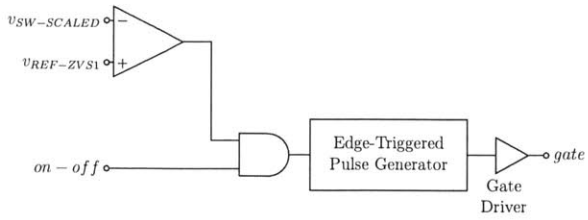


Figure 3-7: On-time control basic implementation.

In the first cycle, the transistor on-time is lengthened because the "intrinsic diode" turns on before the transistor gate is driven. This leads to an increase in inductor current, lengthens the time that the buck diode remains on, and leads to hard switching at the beginning of the second cycle when the gate drive goes high. Because the second cycle is hard switched, the following transistor on-time is short, lowering the inductor current and shortening the buck diode on-time. With short buck diode on-time, the transistor voltage falls early, and the following transistor on-time is lengthened, recreating the conditions of the first cycle. While fine tuning allowed the circuit to operate with some instability, small perturbations led to high-voltage hard-switching and transistor failure.

On Time Control

To address this issue, a new control technique was used in a second version of the design. The second design utilized edge-triggered on-time control. By turning on the gate at the falling edge of the transistor voltage, the controls ensured consistent on-time and reliable soft-switching. Figure 3-7 shows the basic implementation of this idea. However, in this design, the on time was set by a pulse generator controlled by a microcontroller. With this arrangement, the controls are very slow to react to transients at the intermediate voltage. If the input voltage rises quickly, the control delay can cause catastrophic overcurrent conditions in the transistor.

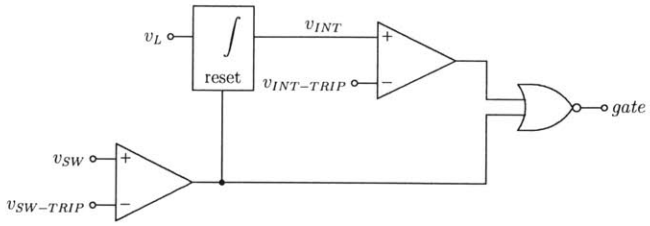


Figure 3-8: Estimator-based peak current control block diagram

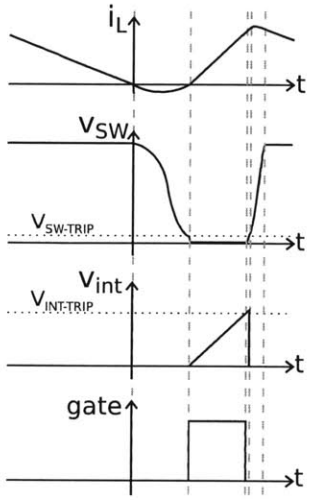


Figure 3-9: Estimator-based peak current control operating waveforms

Estimator-Based Peak Current Control

The final control design was based around the concept of controlling the peak current through the transistor, hence protecting it from transients, while retaining the stability of the edge-triggered on-time control. Since directly measuring the peak current at frequencies on the order of 10MHz is tricky and likely to be inefficient, the solution came in the form of an estimator. While the transistor is on, the inductor current is an integral of the supply voltage less the LED voltage. We can estimate this integral and switch the transistor off based on the estimate reaching a threshold value. The concept is shown in Figure 3-8, with operating waveforms in Figure 3-9.

There are a two major requirements on this design. First, the system must be fast. Integrator bandwidth and propagation delay limit the accuracy of the peak current control and the efficacy of the overcurrent protection. For best results, all of the delays

should be well less than the integrator on-time, ensuring that the controls can respond to a transient within a cycle and prevent an over-current condition. Second, the delay from the input comparator to the NOR gate must be less than the delay from the same comparator through the integrator reset and the integrator comparator. This prevents the gate drive from having glitches at turn-off. This requirement is trivial in the basic configuration in Figure 3-8, but if ancillary logic is added, it must meet this delay requirement. More details about the implementation of this design can be found in Section5.3.1.

3.4 2:1 Switched Capacitor

The switched capacitor design was not core to my research work, but is shown for completeness. Seungbum Lim designed a switched capacitor circuit that is reconfigurable amongst 2:1, 1:1, and 1:2 conversion modes. For reliability, power factor and controllability reasons, a simple 2:1 down converting switched capacitor was found to be preferable for ac line-interfaced circuits or for dc-dc circuits not requiring a very wide input range. The design utilized here, heavily based on Lim's work[14], is shown in Figure 3-10. It uses two interleaved energy storage elements to provide uninterrupted current from the input to the output. A detailed circuit diagram with part numbers and component values is shown as part of the merged 2-stage schematic in Appendix A.2.

Because the HF stage operates at high frequency and draws fairly constant current, it can be modeled as a current source for longer time scales associated with the SC circuit operation. This is actually essential for high efficiency operation of the SC stage through "soft charging" or "adiabatic" charging of the SC stage capacitors. It's our goal to have the SC stage run at low frequency. At low frequency, in a normal SC design where the load has a hold-up capacitor, the floating capacitors are charged and discharged through an RC process with the parasitic resistances of the circuit. This is an inherently lossy process that occurs every cycle, dissipating $C\Delta V^2$ per cycle, where ΔV is the ripple across a given capacitor[16]. By omitting the output

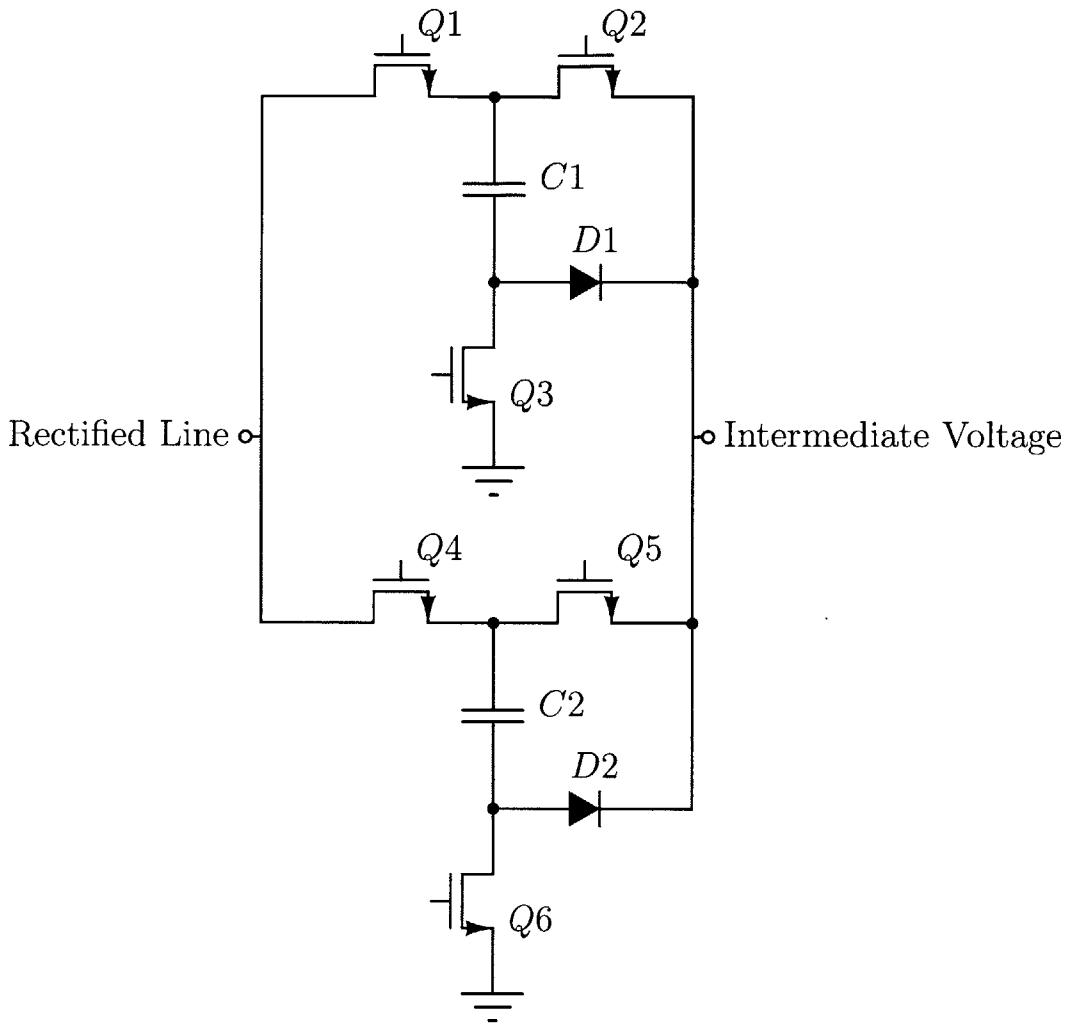
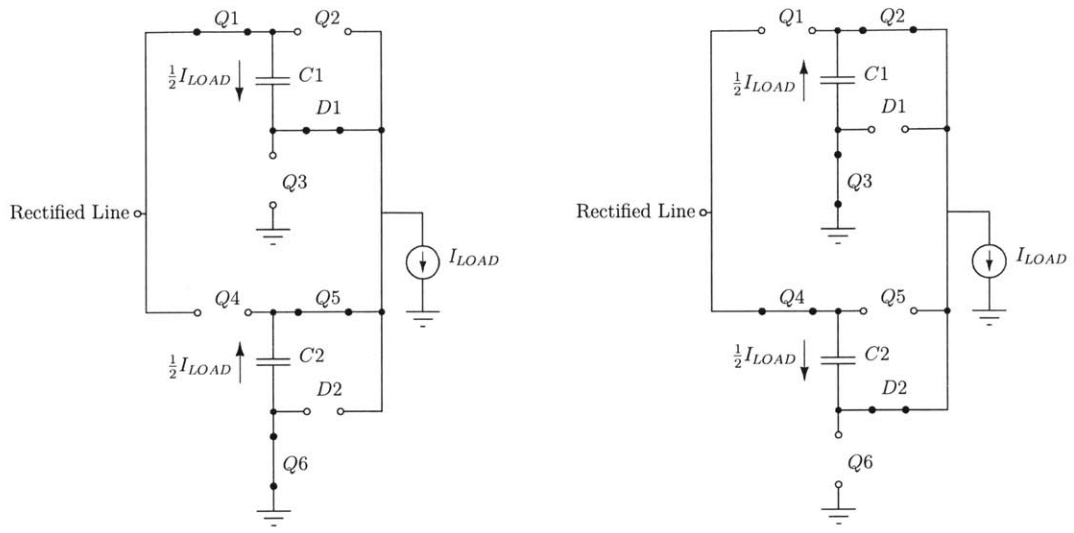


Figure 3-10: Switched capacitor basic circuit. A detailed circuit diagram with part numbers and component values is shown as part of the merged 2-stage schematic in Appendix A.2.

hold-up capacitor and using a current source load, the floating capacitors are now charged with a constant current. While the voltage ripple remains the same, the loss is reduced to I^2R, where I is the charging current and R is the parasitic series resistance for a given capacitor. Figure 3-11 shows diagrams of the switched capacitor circuit demonstrating its charging and discharging behavior.



(a) Phase 1

(b) Phase 2

Figure 3-11: Simplified diagrams of the charging and discharging behavior of the SC circuit. I_{LOAD} represents the current drawn by the HF stage

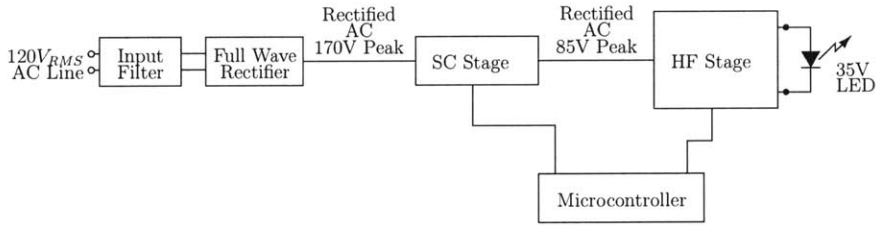


Figure 3-12: Merged 2-Stage block diagram

3.5 Merged 2-Stage Converter

By combining the HF buck with the switched capacitor circuit, we have a circuit that has the potential to operate from rectified AC line with high power factor and high efficiency. The block level design can be seen in Figure 3-12.

3.5.1 Control for Power Factor and Peak Power

Our initial attempt to control the power factor of the converter involved bursting the HF stage on and off at low frequency. For a number of reasons discussed in the results section, this method was scrapped. The method used in the final merged

2-stage prototype used only feed-forward on-time modulation to achieve good power factor. Assuming square wave current being drawn from the input, it's possible to achieve a > 0.9 power factor by only drawing power from AC when the input voltage is above 100V, 59% of the peak voltage, assuming $120V_{RMS}$ sinusoidal line voltage. This is true because the current waveform has near complete third harmonic cancellation, switching at 36° instead of the ideal 30°, with a theoretical power factor of 0.937. Further improving on this, if the converter draws current proportional to the input voltage over the operating voltages, it can achieve a theoretical power factor of 0.946. Both of these cases are shown in Figure 3-13.

The HF stage draws power essentially proportional to the peak current into the LEDs, because the LEDs present a mostly constant voltage load and the peak current is roughly proportional to the average current. By controlling the peak current, we have a knob to control the power drawn by the entire converter. Within the operating range of input voltage, 100V-170V, peak current control can produce output current that is proportional to the line voltage or the square of the line voltage. When reflected back to the line, these output currents create input currents that are respectively constant, or proportional to the line voltage. Since it was achievable, the second option, shown with currents in solid lines in Figure 3-13, was chosen for its higher power factor and lower potential EMI.

3.5.2 Input Filter

In general, this circuit has minimal filtering needs. Because the HF portion operates at around 10MHz, it takes a small capacitance and small inductance to filter out the ripple current. Because the SC circuit is interleaved and the charging is adiabatic, it generates almost no noise at its switching frequency.

3.5.3 LED Output Capacitor

This circuit does not intrinsically prevent the 120Hz current ripple from going through the LEDs. However, the output capacitor forms a current divider with the small signal

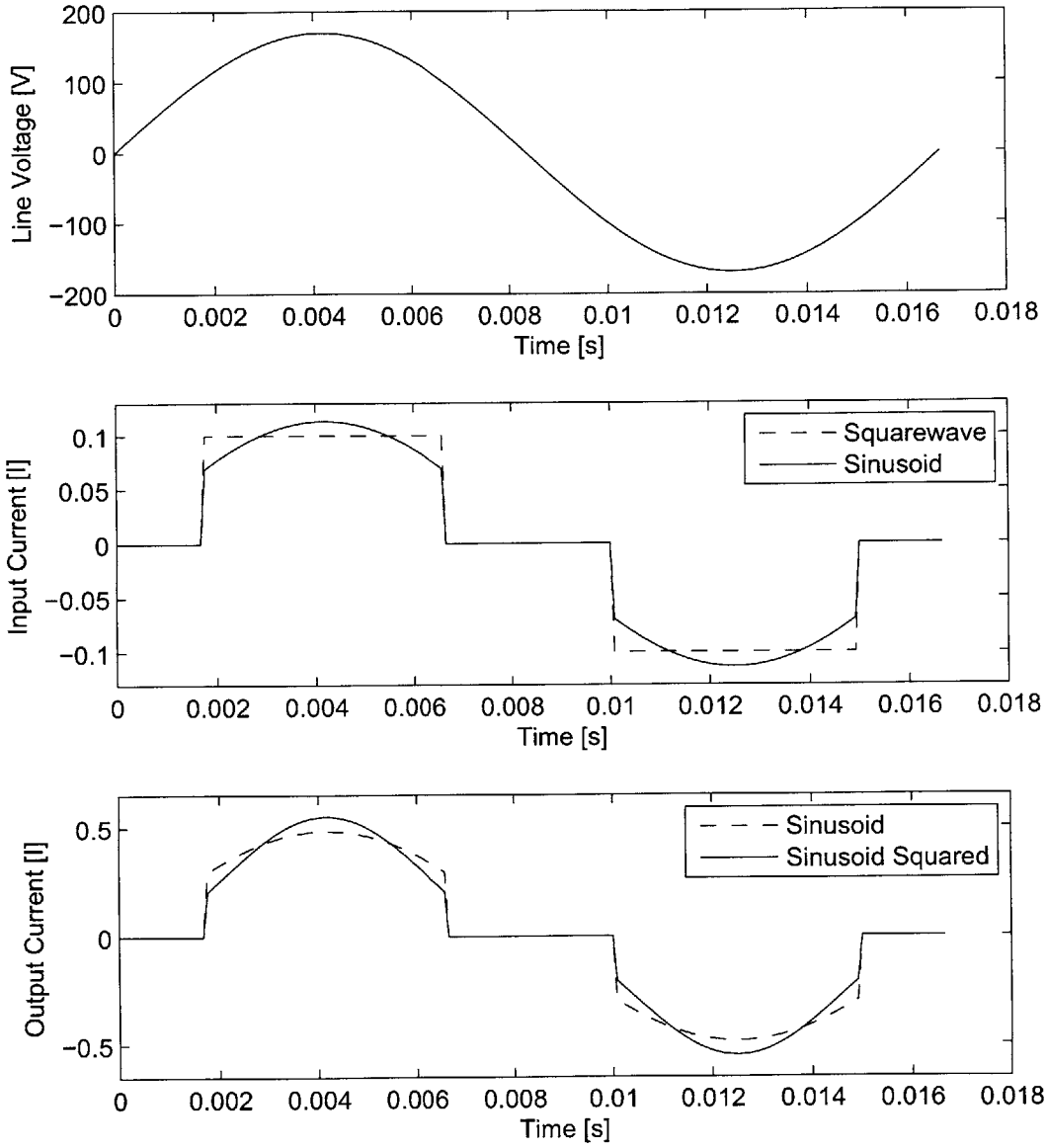


Figure 3-13: Current shaping options for power factor correction.

resistance of the LEDs. By making the capacitor across the LEDs sufficiently large, it is possible to reduce the current ripple and the prevent output flicker. The design pursued here thus addresses the twice-line-frequency ripple inherent in single-phase ac-dc conversion is thus handled by a bulk capacitor placed across the LED string.

Chapter 4

Simulation and Optimization

One critical portion of this project was simulation of the HF stage of the converter. Two approaches were taken to simulation. The first was a closed loop SPICE simulation of the circuit, using LTSpice. The other method, created to allow iterative optimization, was parameterized matlab modeling.

4.1 LTSpice Simulation

LTSpice provided the initial verification that the circuit concept was sound. The nonlinear capacitance of the transistor was modeled with a variable current source, bypassing instability in the LTSpice variable capacitor model. While the LTSpice simulation was used for initial testing, no significant attempt was made to make the simulation exactly match the experimental data. This was, by and large, due to a number of complicating factors, largely dynamic Rds-on but also buck diode leakage, and parasitic capacitance loss. Appendex D shows a sample SPICE deck and a set of waveforms generated with it.

4.2 MATLAB Simulation

Matlab was used to provide an optimization platform for the other groups designing transistors and inductors for use in the converter. The converter behavior was divided

into five phases, the four previously described, as well as a short time period during incomplete ZVS when the transistor turns on and the capacitances are quickly discharged. The basic simulation was done by treating the elements as lossless, except for the portion of the cycle where the capacitances were being discharged. For ease of simulation, switching behavior was set by the on-time parameter, defined as the period where the switch was on and the switch current as positive. All of the code used can be found in Appendix C;

4.2.1 Nonlinear Capacitances

MATLAB functions are used to model the nonlinear capacitances of the circuit. Each function takes the device voltage as an input and produces the small-signal capacitance at the voltage as its output. For example, the STPS10170C has a capacitance function that calculates the following (in pF): $\frac{476.4}{(1+Vr/0.7437)^{0.5216}} + 6.313$. For simulation, the diode capacitance, switch capacitance, and parasitic inductor capacitance are lumped together into a single function that gives the total node capacitance for any switch voltage. This is possible because each capacitance has one end connected to a small signal ground.

4.2.2 Fixed voltage step forward Euler (FVSFE)

Operating with high speed was the first priority of the MATLAB simulation code because the simulation is repeated in loops for device and magnetics optimization. When the voltages and currents in the circuit change simultaneously, some numerical method must be used to solve the circuit behavior. Fixed time step forward Euler is very simple to implement and fairly fast. However, the overall timescale of the resonances of the converter vary strongly with capacitance shape and inductor size. This made a fixed time step forward Euler not ideal. Variable time steps can be very efficient, but guaranteeing accuracy is difficult. The solution used in this thesis is a variant of forward Euler with a fixed voltage step. This works well for this design because the portions of the waveform that require numerical methods change

monotonically and relatively smoothly. The steps used in this method follow:

1. Calculate $\frac{\delta v_{sw,n}}{\delta t}$ at the present operating point.
2. Estimate the time step $\Delta t_n = \Delta v_{sw} \frac{1}{\frac{\delta v_{sw,n}}{\delta t}}$.
3. Calculate $\frac{\delta i_n}{\delta t}$ for the relevant current path at the present operating point.
4. Calculate the current step $\Delta i_n = \frac{\delta i_n}{\delta t} \Delta t_n$
5. $v_{sw,(n+1)} = v_{sw,n} + \Delta v_{sw}$, $i_{n+1} = i_n + \Delta i_n$ and $t_{n+1} = t_n + \Delta t_n$
6. If not at an end condition, repeat.

4.2.3 Simulating the Phases

Phase 1

In phase 1, the switch voltage is assumed to be constant. The simulator first calculates the derivative of the inductor current. If the current starts negative, it calculates the time to reach zero from the current derivative. It then multiplies current derivative by the on-time to find current when the transistor turns off. The current calculated is a linear ramp from the starting current to the ending current, and the time spent in this stage is the sum of the negative current portion and the fixed on-time.

Phase 2

For phase 2, FVSFE is used to calculate the inductor current and switch voltage waveforms in the LV resonator as the v_{SW} rises from 0V to V_{IN}.

Phase 3

In phase 3, the switch voltage is assumed to be constant. The simulator calculates the derivative of the inductor current. The diode on-time is then calculated from the starting current and the derivative. The current calculated is a linear ramp from the starting current to zero.

Phase 4

In phase 4, FVSFE is used to calculate the inductor current and switch voltage waveforms in the LC resonator as the voltage rings down. The ends conditions are either reaching 0V, or reaching 0 voltage derivate. The second happens if V_{IN} is high and the converter does not achieve ZVS.

Capacitor Discharge

If the converter does not achieve ZVS, a phase is added for simulating the capacitor discharge. FVSFE is used to calculate the current and voltage waveforms in the RC circuit as the device capacitances are discharged through the switch resistance.

Top Level Simulation

The top level simulation code starts with Phase 3, because the starting conditions in Phase 3 are always the same, $v_{SW} = V_{IN}$, and $i_L = 0$. It then proceeds through each phase in sequence until it generates a full cycle simulation. The end conditions of the previous stage become the starting conditions of the next stage.

4.2.4 Loss Calculations

The losses were calculated by integrating, over that cycle, the power loss if lossy elements were carrying the same current as the lossless design. Because the timestep is variable, care has to to be taken to properly calculate the actual power. The is especially true with the resistances, where the current is trapezoidal, but power being integated is quadratic between the simulation points. Added to all of this was the simulated loss from the capacitor discharge on turn-on.

4.2.5 Optimization

Using this code, a mechanism was provided for quickly optimizing power loss by simulating a number of different inductors, transistors and diodes. This was used

largely by the magnetics team to design inductors optimized around the EPC1012 GaN transistor that was available to us.

Chapter 5

Experimental Design and Results

5.1 HF Stage

The converter design went through a number of iterations, shown in Table 5.1. The first three iterations were critical for understanding the basic converter behavior and selecting suitable components for the topology. The EPC1012 GaN on Si transistor was used as an active device, because it was a good fit for the converter and the closest commercial equivalent to the devices we expected from Prof. Tomas Palacios' team at MIT.

For the buck diode, I initially used a diode-connected Microsemi ARF521 vertical FET in parallel with a Cree C2D20120D SiC diode. The SiC device provided a

Table 5.1: Converter Iterations

Iter.	Inductor	Transistor	Diode	Gate Control
1	4x 422nH 132-18SMJB	EPC1012	ARF521 // C2D20120D	External Signal Generator
2	4x 422nH 132-18SMJB	EPC1012	ARF521 // DFLS1150	Edge-Triggered 74AHC123 Pulse Generator
2.1	4x 422nH 132-18SMJB	EPC1012	ARF521 // 5x DFLS1150	Edge-Triggered 74AHC123 Pulse Generator
2.2	4x 422nH 132-18SMJB	EPC1012	ARF521 // STPS10170C	Edge-Triggered 74AHC123 Pulse Generator
3	2x 422nH 132-18SMJB	EPC1012	STPS10170C	Edge-Triggered Analog Pulse Generator

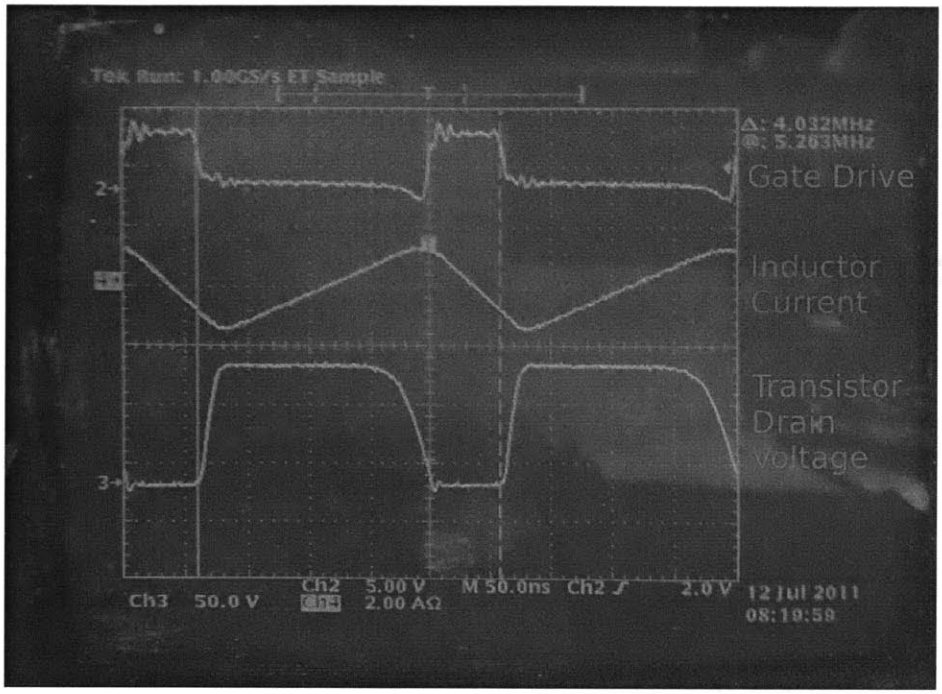


Figure 5-1: Converter using ARF521 to achieve ZVS at 100V in, 35V out

fast high-voltage diode while the FET provided a strongly nonlinear capacitance that enabled zero voltage switching with 100V in and a 30-35V load. The converter operated with ZVS across the entire input voltage range. Figure 5-1 demonstrates ZVS at the worst case input voltage of 100V. Unfortunately, the converter easily fell into the aforementioned two-cycle oscillation, and the peak efficiency was only 74% at 50V in.

Based on the suspicion of high conduction loss in the SiC diode, Iteration 2 used a small Si schottky in place of the SiC diode, and also corrected the control issue by adding a logic-chip based on-time control. Unfortunately, this converter showed similarly bad efficiency, peaking at 67%. Through a series of iterative changes, two issues were uncovered. The buck diode, despite having a forward current rating well above the average current actually carried, was experiencing much higher loss than anticipated. Using several diodes and eventually a larger diode, shown in iterations 2.1 and 2.2, fixed this problem. (This characteristic of high loss at nominal current levels in schottky rectifiers utilized at HF and VHF has been observed in other contexts as

well[17].) Also, the ARF521, despite enabling ZVS, was reducing overall efficiency, owing to large conduction losses in its nonlinear capacitance. Interation 3 incoporates all of the previous fixes, plus the removal of the ARF521. This design was settled on for the remainder of the project. It was followed by two more iterations that differed only in how the on-time was generated, but were functionally the same.

5.2 Results

Table 5.2 shows the performance of iteration 3 of the HF stage. The full schematics, BOM, PCB layout and board photograph for this version of the circuit are shown in Appendix A.1. The the peak efficiency reached 94%. Figures 5-2 - 5-4 show the waveforms of the iteration 3 converter at a various operating points. Without the nonlinear capacitance from the ARF521, the converter no longer achieves ZVS across the entire input range. Nonetheless, the energy dissipated from the capacitors is significantly reduced compared to hard switching. Figures 5-5 - 5-7 show the power and efficiency of the various iterations, showing the evolution of the designs. Table 5.2 summarizes the results of the converter operation.

Table 5.2: HF Stage Results (Iteration 3, 25-28ns on-time)

Parameter	Specification	Measured
Input Voltage Range	50V-100V	50.1V - 100V
Target Output Voltage	30-40V	30.7V - 34.4V
Operating Frequency	>5MHz	7.8MHz - 10.4MHz
Peak Output Power	Around 25W	21.5W
Efficiency	>90%	94.0% Peak >90%, $62V \leq V_{IN} \leq 100V$

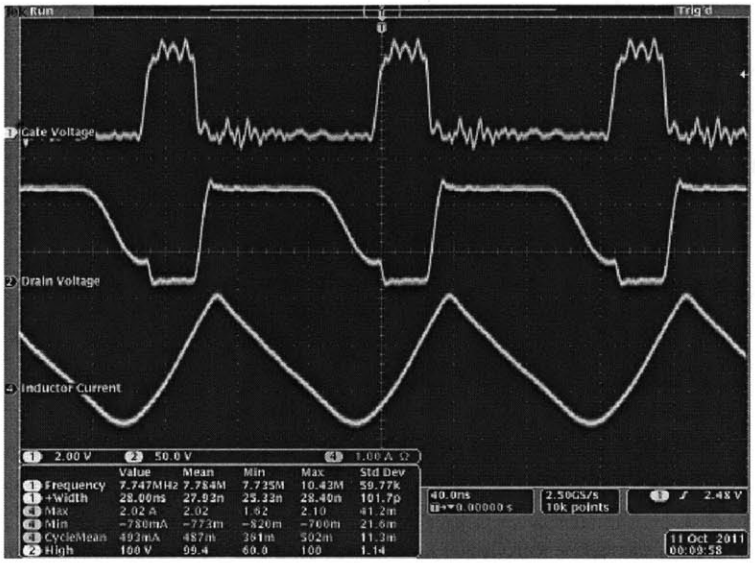


Figure 5-2: Iteration 3 waveforms showing low but nonzero turn-on voltage at 100V in, 35V out

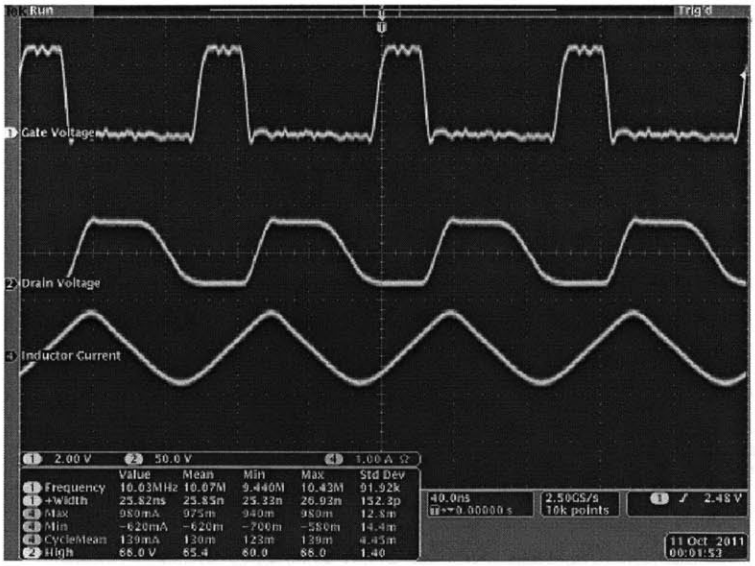


Figure 5-3: Iteration 3 waveforms showing perfectly tuned ZVS at 66V in, 35V out

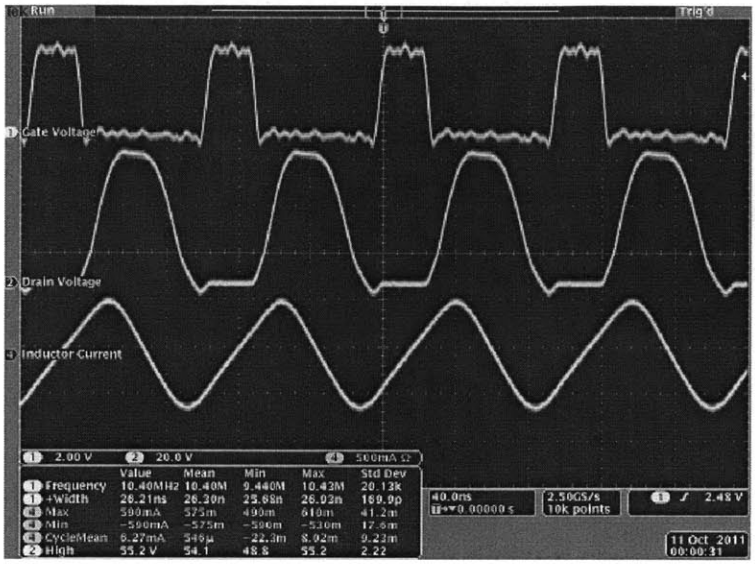


Figure 5-4: Iteration 3 waveforms showing ZVS with intrinsic diode clamping at 55V in, 35V out

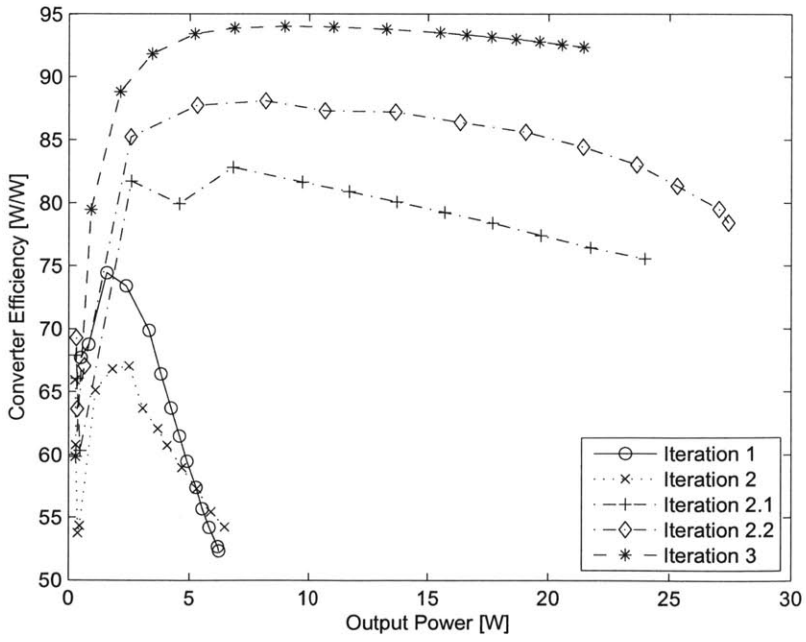


Figure 5-5: HF stage prototype efficiency versus power

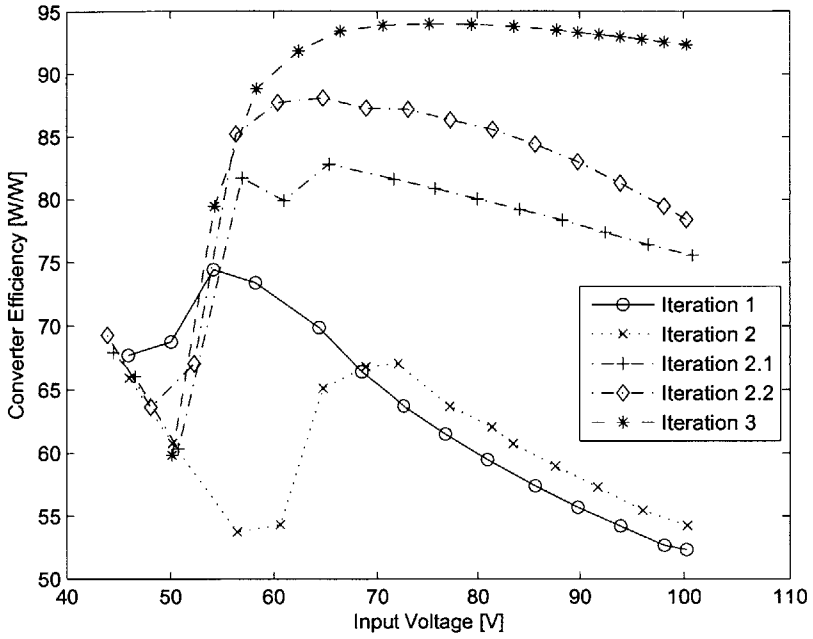


Figure 5-6: HF stage prototype efficiency versus voltage

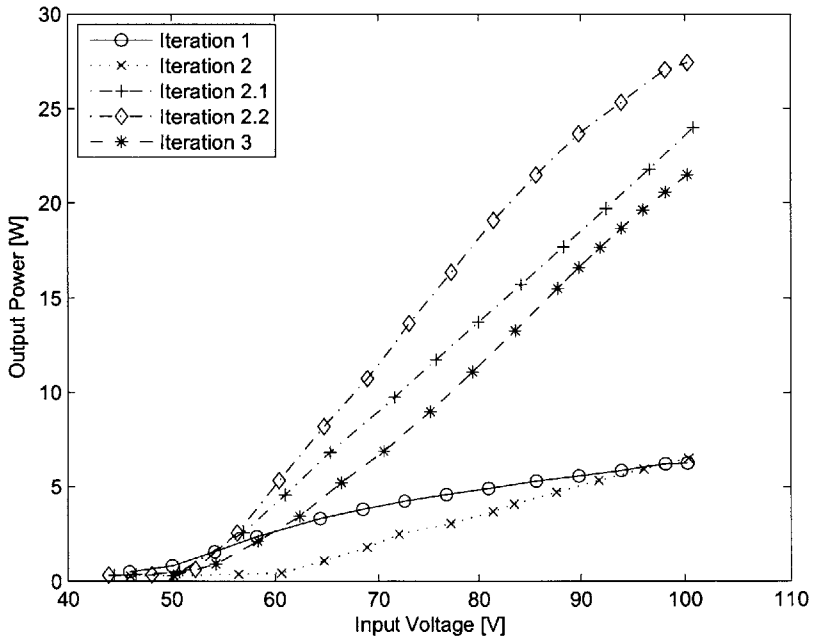


Figure 5-7: HF stage prototype power versus voltage

5.3 Merged 2 Stage

Our first attempt to to feed the HF stage from the switched capacitor preregulator to operate from ac was not reliable. We chained an Iteration 5 HF PCB (Iteration 3 with digitally controlled on-time) with the switched capacitor board designed by Seungbum Lim. This presented several problems. The total power was controlled by a microprocessor modulating the on-time of the switch and modulating the HF converter on and off. Modulating the converter on and off added low frequency components to the input current, requiring a large filter. Furthermore, the SC stage had 3 modes, 2:1, 1:1, and 1:2, and switched between them dynamically to provide a consistent 50-100V to the HF stage. At mode transitions, the boards would explode. The suspected reason for this was the limited bandwidth with which the controls responded to input transients. It was possible for many HF stage switching transitions to occur before the microcontroller responded to a rising input transition. In this time, the converter could draw current well beyond its capacity, fail, and take the switched capacitor stage with it.

To mitigate this problem, a new merged two stage board was designed specifically for ac use. It used the 2:1 switched capacitor converter incorporating EPC2012 devices and the design was based on the Iteration 3 power circuit. The controls implemented the edge-triggered peak current control. The whole system was controlled by a microcontroller. The components and design parameters are shown in Table 5.3. The full schematics, BOM, PCB layout and board photograph for this version of the circuit are shown in Appendix A.2.

5.3.1 Estimator Based Peak Current Control Implementation

The discrete implementation of the estimator-based peak current control is shown in Figure 5-8. In this implementation, an RC circuit is used to approximate the integrator at the frequencies of interest. There are two major additional sources of error in this implementation. First, the RC "integrator" integrates the difference

Table 5.3: Merged 2 Stage Components and Parameters

Subsystem	Component / Parameter	Value
SC Stage	Transistors	EPC EPC1012/EPC2012
	Energy Transfer Capacitors	1uF Ceramic
	Switching Frequency	51.2kHz
HF Stage	Transistor	EPC EPC1012/EPC2012
	Inductor	2x 422nH Coilcraft 132-18SMJB
	Diode	ST STPS10170C
Rectifier	Full Bridge	Fairchild MB6S
Input Filter	Filter Capacitor	22pF Ceramic
	Damping Leg	220pF / 442Ω
	Common Mode Choke	Bourns PM3700-40-RC
	X Capacitor	None Installed
	Y Capacitors	22pF Ceramic

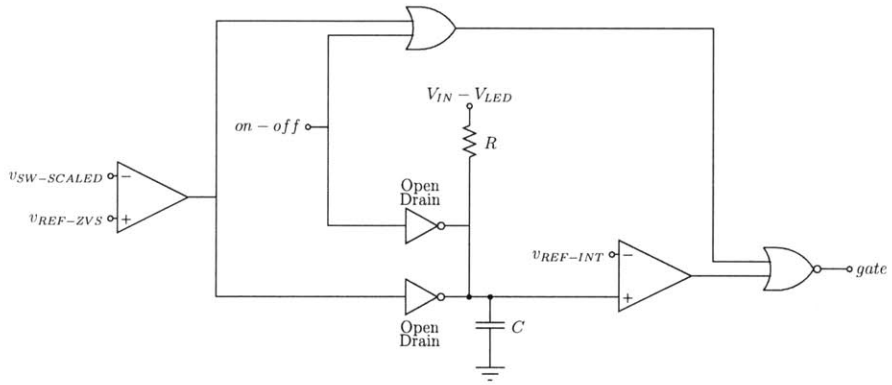


Figure 5-8: Discrete implementation of estimator-based peak current control.

between $V_{IN} - V_{LED}$ and its own output voltage. When $V_{IN} - V_{LED}$ is small, this error can be substantial. Second, during reset, the open-drain inverters carry the integrator current and consequently have a non-zero reset voltage, causing reduced on-times.

The converter input power was characterized across input voltage and HF stage peak power command, as shown in Figure 5-9. From this data, the optimal peak current command for each input voltage was calculated to give input power proportional to the square of the line voltage for power factor correction. This was programmed into a table in the microcontroller and used for feed forward control.

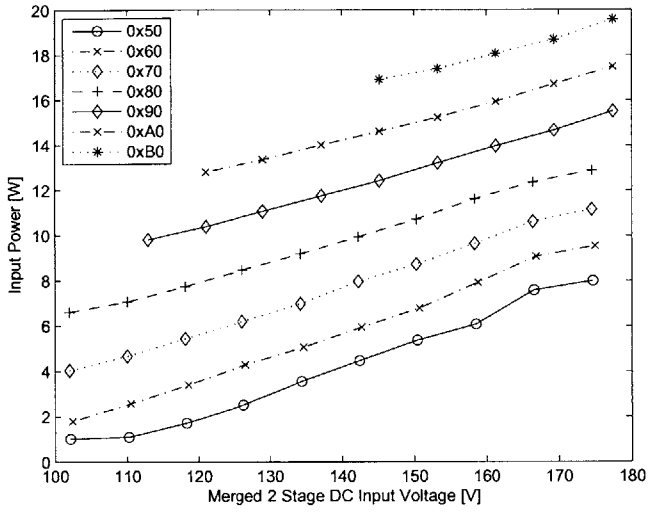


Figure 5-9: Characterization of the input power of the merged two stage converter across line voltage and peak current command

Table 5.4: Merged 2 Stage Results

Parameter	Target	Measured
Input Voltage Range	$120\text{Vac}_{RMS} \pm 10\%$	Up to 137Vac_{RMS}
Target Output Voltage	30-40V	34.9V-35.1V
Output Power	No Spec	8.4W @ 120Vac_{RMS}
Efficiency	>90% @ 120Vac_{RMS}	88.2% @ 120Vac_{RMS}
Power Factor	>0.9 @ 120Vac_{RMS}	0.93 @ 120Vac_{RMS}

5.3.2 Results

After the feed forward table was calibrated, the converter was tested again at dc to ensure that the power factor correction ought to work. Figure 5-10 shows that with a dc input, the feed forward controlled converter draws close to ideal square law power from its input over its operating range.

The merged two stage converter then operated successfully off 120Vac. The converter put 8.4W of average power into a 35V load with an efficiency of 88.2% and a 0.934 power factor. The input voltage and current can be seen in Figure 5-11. Evident in the current waveform is noise. The frequency of this noise is well below the switching frequency of either stage, and appears to be either an input filter resonance or noise from quantization error and latency in the HF controls. Table 5.4

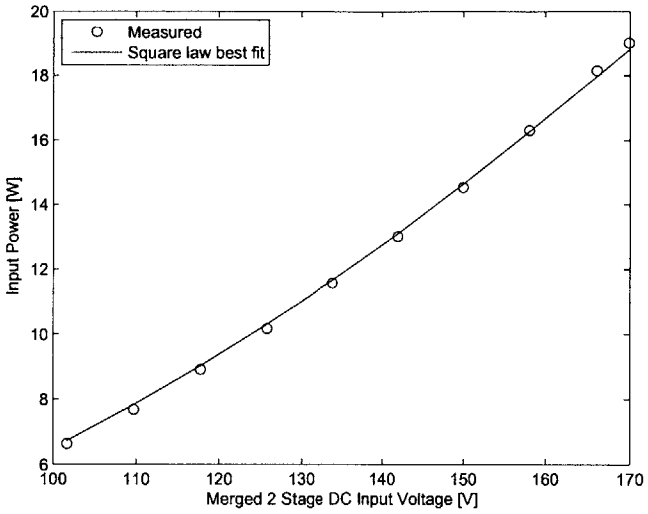


Figure 5-10: Characterization of the input power of the merged two stage converter operating from a DC input under feed forward control

summarizes the results of the converter operation.

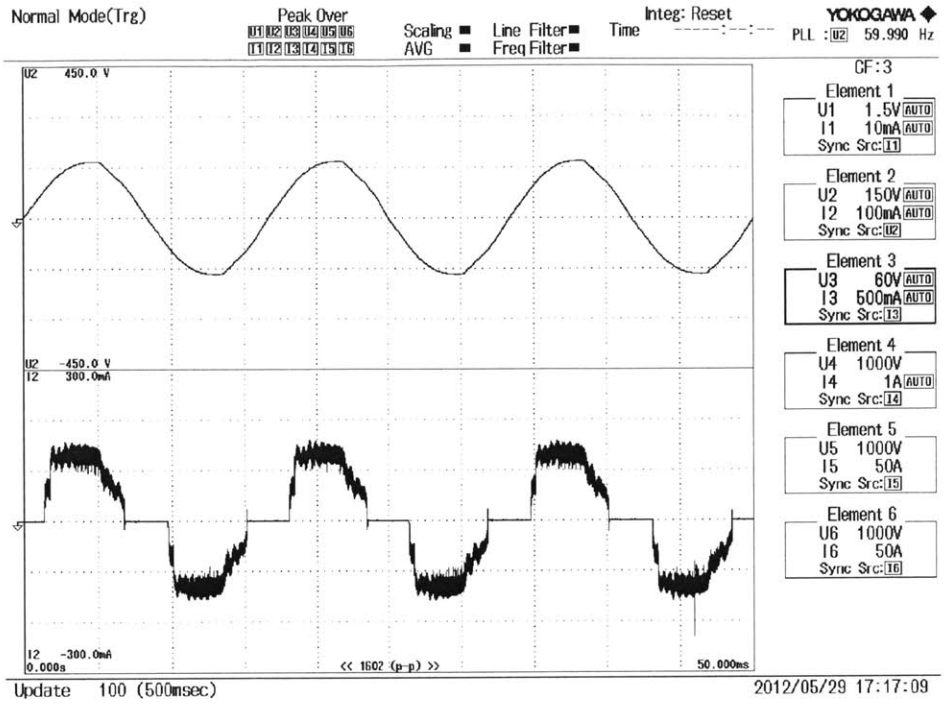


Figure 5-11: Merged 2-Stage ac operation showing high power factor operating from 120V line putting 8.4W into a 35V load.

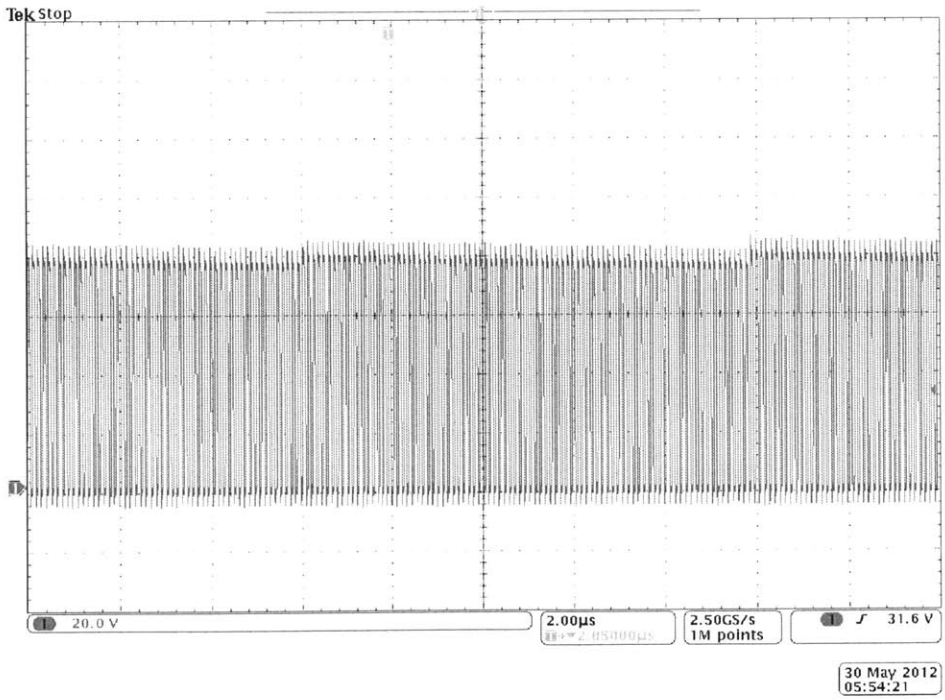


Figure 5-12: Envelope modulation of HF drain voltage caused by SC operation in the merged two stage.

Chapter 6

Future Work

6.1 Integrated Control and Driver IC

Already in progress is the design of an integrated circuit that pulls together all of the controls necessary for the HF portion of the converter. At its base is the design shown in Figure 6-1. This is a refined implementation of the estimator based peak current control. Two comparators are provided. This allows switching on based on a constant low voltage, when ZVS is possible, or switching on referenced to V_{IN} or $V_{IN} - 2V_{LED}$, when the input voltage will not allow ZVS. The integrator is uses a current mirror to reduce the non-linearity from the changing voltage across the sense resistor.

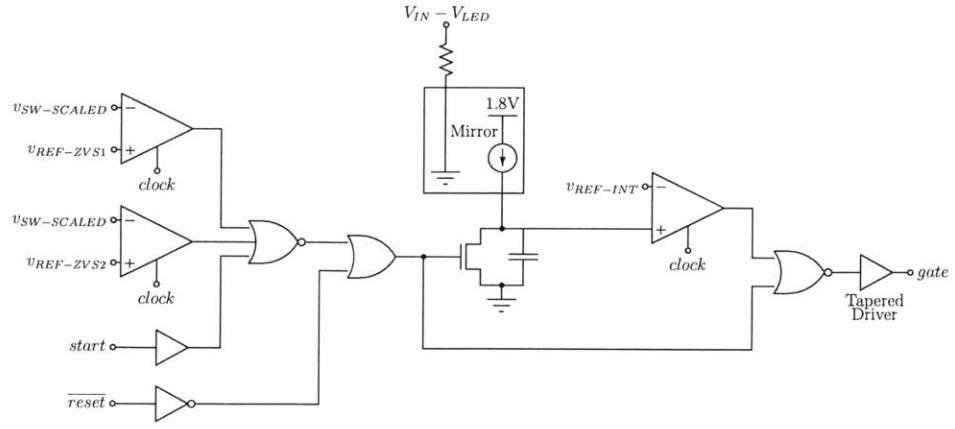


Figure 6-1: HF control block IC implementation

6.2 Integration of Experimental Devices

When miniaturized inductors and optimized GaN transitors become available, very tight integration of the HF stage will be possible. Using a small interposer board to integrate a flip-chipped control IC, the transistor, the inductor, and necessary capacitors and passive should make a converter of unparalleled size.

6.3 Characterization and optimization

As it stands, there is a significant amount of further characterization and optimization that can be put into this topology. A number of loss mechanisms in the circuit are poorly characterized: dynamic on-state resistance, HF schottky loss, schottky leakage, etc. Furthermore, all of this work has been done with a limited selection of parts. For the best balance of size and efficiency, co-optimization of the HEMT, inductor, and diode is necessary. And the ability to optimize is not limited to the HF stage. The exact interplay of the HF and SC stages needs to be well understood, allowing optimal design of each stage to fit in the overall system.

6.4 Extending ZVS

Testing the HF portion of the converter with a variety of sources of nonlinear capacitances (or reverse recovery charge) in order to obtain ZVS could be invaluable for decreasing the switching loss. Beyond standard active device capacitances, piezoelectic materials may provide useful nonlinear capacitances. Furthermore GaN may itself present a new type of highly-nonlinear capacitance that can be exploited. These devices are being fabricated by Prof. Tomas Palacios group at MIT, and are an exciting prospect for other power circuits as well.

6.5 Control and Drive Improvements

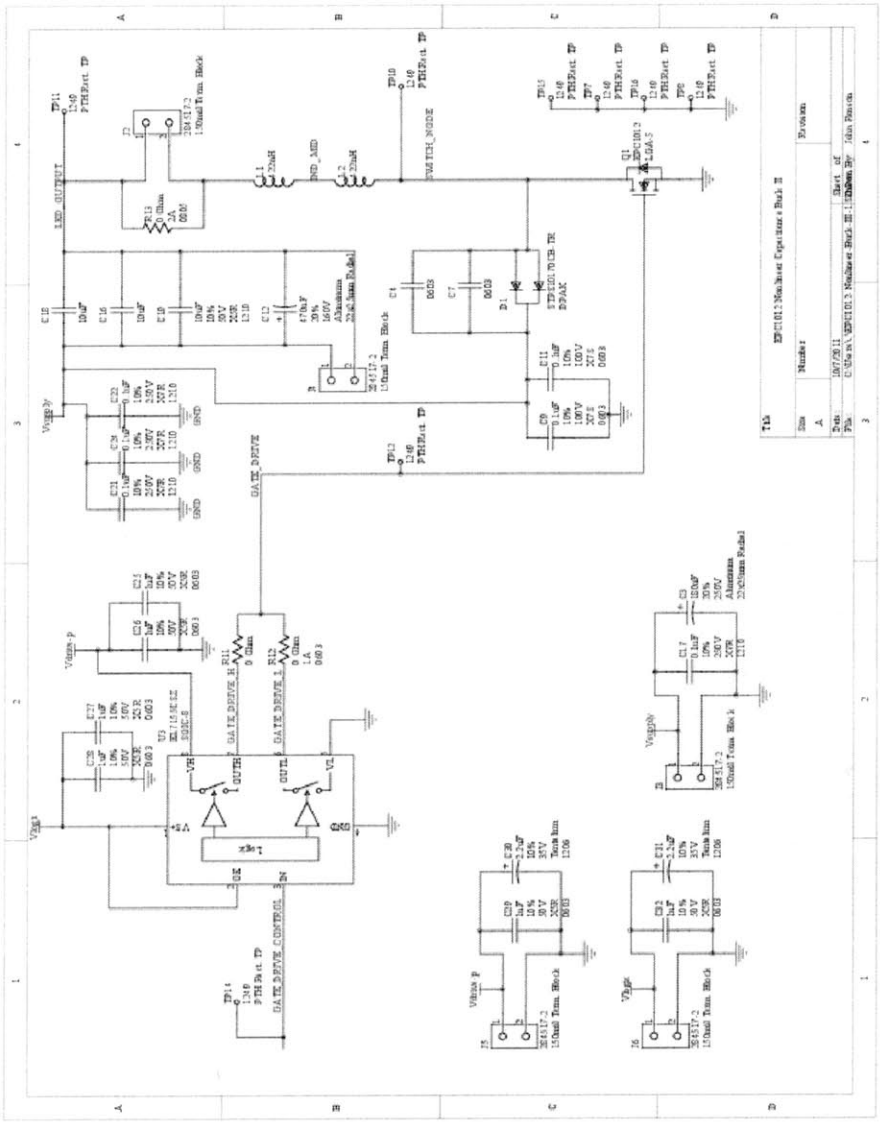
Much work remains in controlling this converter topology. The switched capacitor stage has six controlled switches, four of which are not ground referenced. Our current design uses isolated supplies, but they are highly inefficient. Bootstrapping, or some other efficient means of generating the high side drive is necessary. Also, the control scheme for the system is almost entirely feed forward, and should be revisited and made more robust.

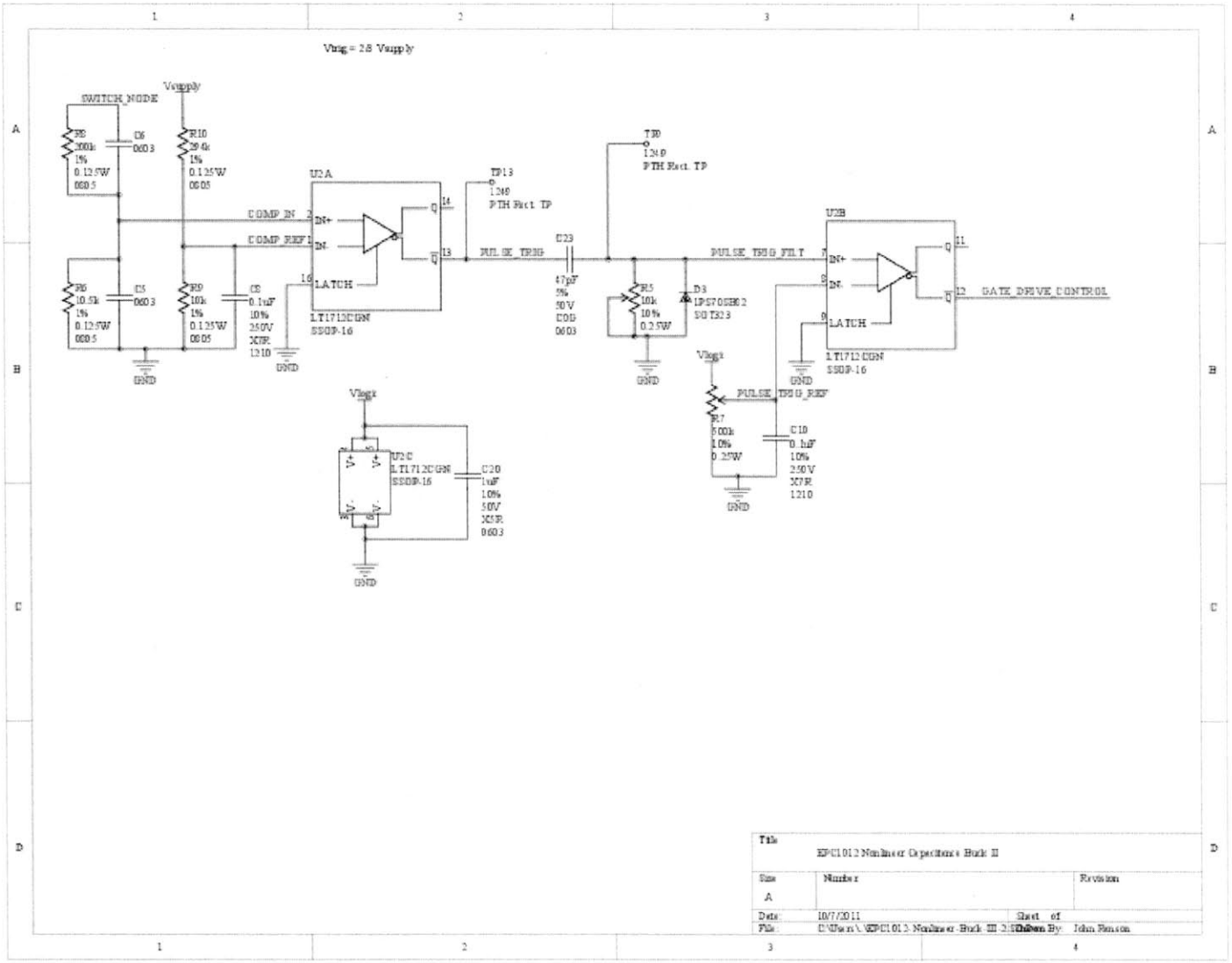
Appendix A

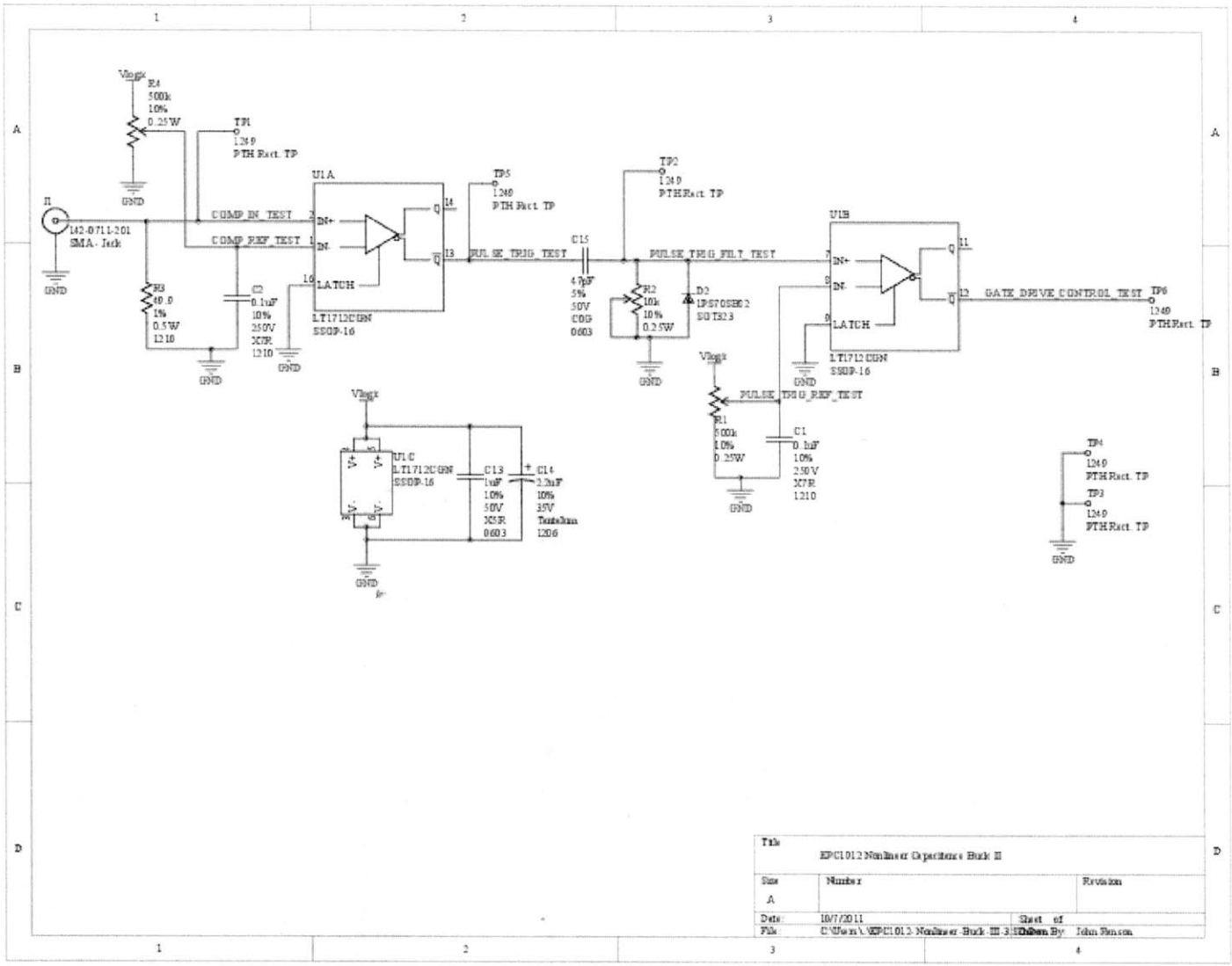
Schematics & PCB Prints

A.1 Iteration 3 - HF Stage

A.1.1 Schematic




Vtrig = 2.8 Vsupply
SWITCH_NODE
Vsupply
R8
300k
1%
0.125W
0805
C6
0603
R10
29.4k
1%
0.125W
0805
U2:A
COMP_IN-
COMP_REF-
LATCH
LT1712CGN
SSOP-16
TP13
1240
PTH Elect. TP
PULSE_TRIG
C23
47pF
5%
50V
C0G
0603
TP0
1240
PTH Elect. TP
R5
10k
10%
0.25W
D3
IPS70SH02
SOT323
PULSE_TRIG_FILT
U2:B
GATE_DRIVE_CONTROL
R6
10.5k
1%
0.125W
0805
C5
0603
R9
10k
1%
0.125W
0805
C8
0.1uF
10%
250V
X7R
1210
GND
Vlogic
U2:C
C20
1uF
10%
50V
X5R
0603
R7
500k
10%
0.25W
PULSE_TRIG_REF
C10
0.1uF
10%
250V
X7R
1210
Title
EPC1012 Nonlinear Capacitance Buck II
Size
A
Number
Revision
Date:
10/7/2011
Sheet of
File:
Drawn By:
John Hanson


Vlogic
R4
500k
10%
0.25W
TP1
1240
PTH Rect. TP
GND
J1
142-0711-201
SMA - Jack
COMP_IN_TEST
COMP_REF_TEST
R3
49.9
1%
0.5W
1210
C2
0.1uF
10%
250V
X7R
1210
U1A
IN+
IN-
LATCH
Q
LT1712CGN
SSOP-16
TP5
1240
PTH Rect. TP
PULSE_TRIG_TEST
C15
47pF
5%
50V
COG
0603
TP2
1240
PTH Rect. TP
PULSE_TRIG_FILT_TEST
R2
10k
10%
0.25W
D2
IPS70SH02
SOT323
U1B
GATE_DRIVE_CONTROL_TEST
TP6
1240
PTH Rect. TP
PULSE_TRIG_REF_TEST
R1
500k
10%
0.25W
C1
0.1uF
10%
250V
X7R
1210
U1C
C13
1uF
10%
50V
X5R
0603
C14
2.2uF
10%
35V
Tantalum
1206
TP4
1240
PTH Rect. TP
TP3
1240
PTH Rect. TP
Title
EPC1012 Nonlinear Capacitance Buck II
Size
A
Number
Revision
Date:
10/7/2011
Sheet of
File:
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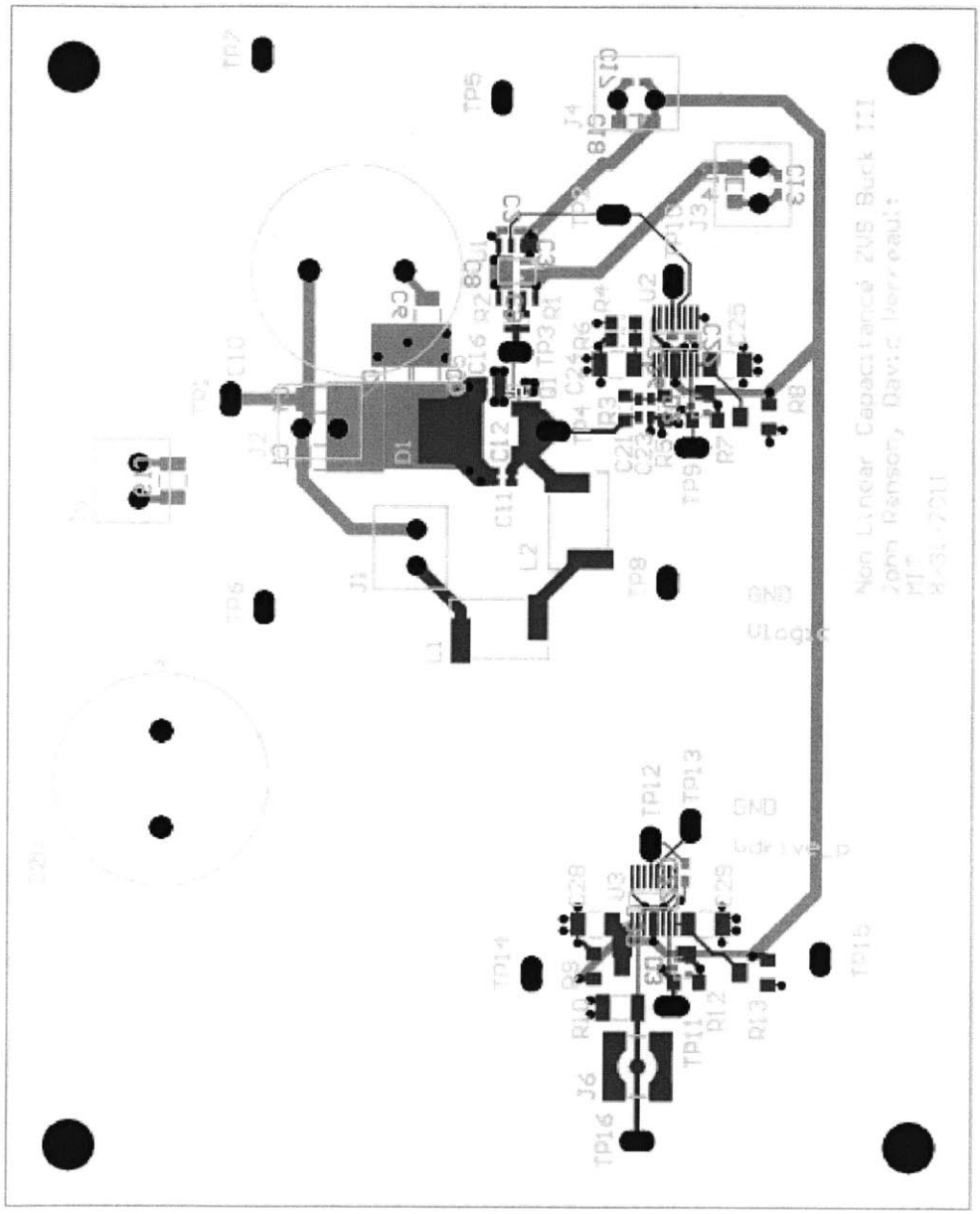
Drawn By:
John Benson

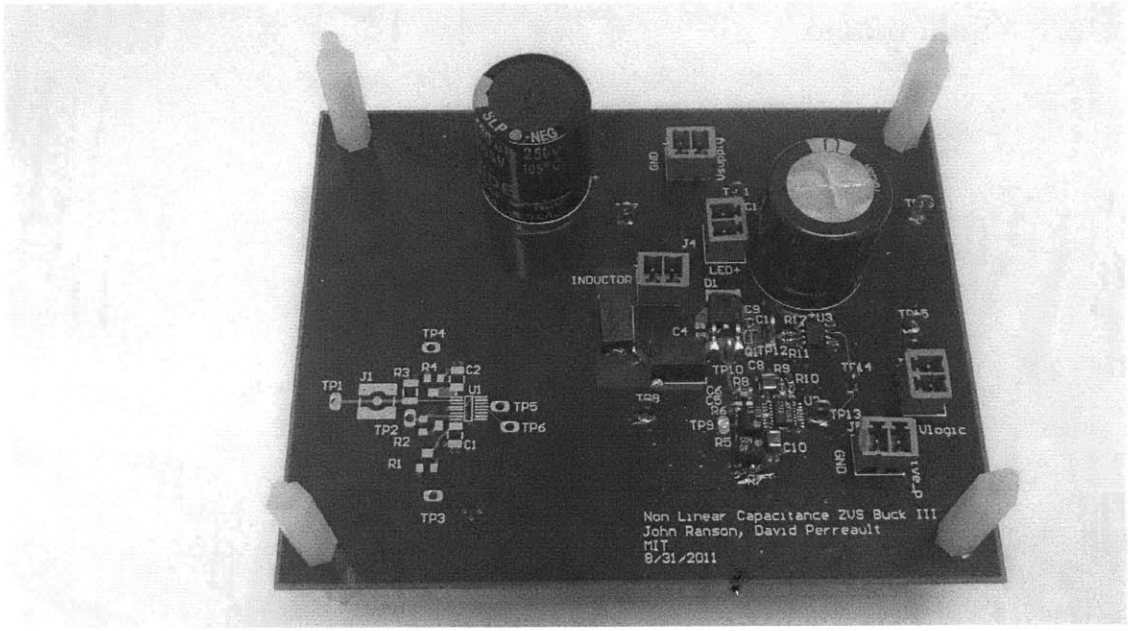
A.1.2 Bill of Materials

Quantity	Designater	Manufacturer	Part Number	Description	Supplier	Supplier PN
8	C1, C2, C8, C10, C17, C21, C22, C24	Taiyo Yuden	GMK325B7104KN-T	Capacitor - 0.1uF - 250V - X7R - 1210	Digikey	587-1360-1-ND
1	C3	Cornell Dubilier	SLP181M250A1P3	Capacitor - 180uF - 250V - Aluminum - 22mm Radial	Digikey	338-1471-ND
4	C4, C5, C6, C7	NONE	TBD-0603			
2	C9, C11	TDK	C1608X7S2A104K	Capacitor - 0.1uF - 100V - X7S - 0603	Digikey	445-5201-1-ND
1	C12	Nippon Chemi-Con	EKMQ161VSN471MP25S	Capacitor - 470uF - 160V - Aluminum - 22mm Radial	Digikey	565-2936-ND
8	C13, C20, C25, C26, C27, C28, C29, C32	Taiyo Yuden	UMK107BJ105KA-T	Capacitor - 1uF - 50V - X5R - 0603	Digikey	587-2400-1-ND
3	C14, C30, C31	AVX	TPSA225K035R1500	Capacitor - 2.2uF - 35V - Tantalum - 1206	Digikey	478-3105-1-ND
2	C15, C23	Murata	GQM1885C1H470JB01D	Capacitor - 47pF - 50V - C0G - HF/Low ESR - 0603	Digikey	490-3579-1-ND
3	C16, C18, C19	Taiyo Yuden	UMK325BJ106KM-T	Capacitor - 10uF - 50V - X5R - 1210	Digikey	587-2247-1-ND
1	D1	ST Microelectronics	STPS10170CB-TR	Diode - Schottky - 170V - 2x5A - DPAK	Digikey	497-6075-1-ND
2	D2, D3	NXP	1PS70SB82	Diode - Schottky - 15V - 30mA - SOT323	Digikey	568-6780-1-ND
1	J1	Emerson	142-0711-201	Connector - SMA Jack - SMT	Digikey	J819-ND
5	J2, J3, J4, J5, J6	Tyco Electronics	284517-2	Terminal Block - Two Piece - 150mil - 1x2	Digikey	A98410-ND
2	L1, L2	Coilcraft	132-18SMGLB	Coilcraft Maxispring Inductor - 422nH	Coilcraft	132-18SMGLB
1	Q1	EPC	EPC1012	EPC EPC1012	Digikey	917-1008-1-ND
3	R1, R4, R7	Copal	SM-43TW504	Potentiometer - 500k Ohm - J-hook SMT	Digikey	SM-43TW504CT-ND
2	R2, R5	Copal	SM-43TW103	Potentiometer - 10k Ohm - J-hook SMT	Digikey	SM-43TW103CT-ND
1	R3	Panasonic	ERJ14NF49R9U	Resistor - 49.9 Ohm - 1% - 1210	Digikey	P49.9AACT-ND
1	R6	Panasonic	ERJ6ENF1052V	Resistor - 10.5k Ohm - 1% - 0805	Digikey	P10.5KCCT-ND
1	R8	Panasonic	ERJ6ENF2003V	Resistor - 200k Ohm - 1% - 0805	Digikey	P200KCCT-ND
1	R9	Panasonic	ERJ6ENF1002V	Resistor - 10k Ohm - 1% - 0805	Digikey	P10.0KCCT-ND
1	R10	Panasonic	ERJ6ENF2943V	Resistor - 294k Ohm - 1% - 0805	Digikey	P294KCCT-ND
2	R11, R12	Panasonic	ERJ3GEY0R00V	Resistor - 0 Ohm - 0603	Digikey	P0.0GCT-ND
1	R13	Panasonic	ERJ6GEY0R00V	Resistor - 0 Ohm - 0805	Digikey	P0.0ACT-ND
16	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16	Keystone Electronics	1249	Test Point - TH	Digikey	1249K-ND
2	U1, U2	Linear	LT1712CGN	Comparator - Dual - 4.5ns - +/-5V	Digikey	LT1712CGN#PBF-ND
1	U3	Intersil	EL7156CSZ	Gate Driver - 40MHz - 3.5A - Low Side	Digikey	EL7156CSZ-ND

A.1.3 PCB Layout

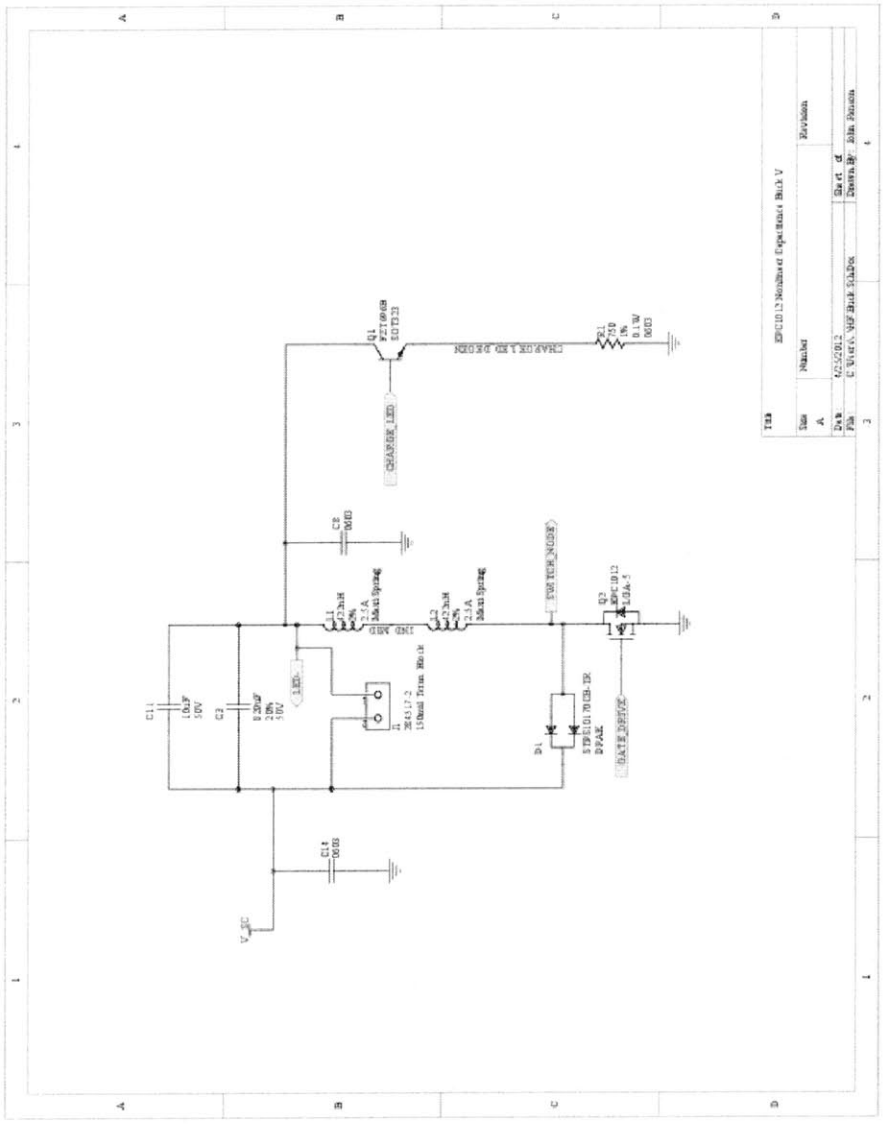


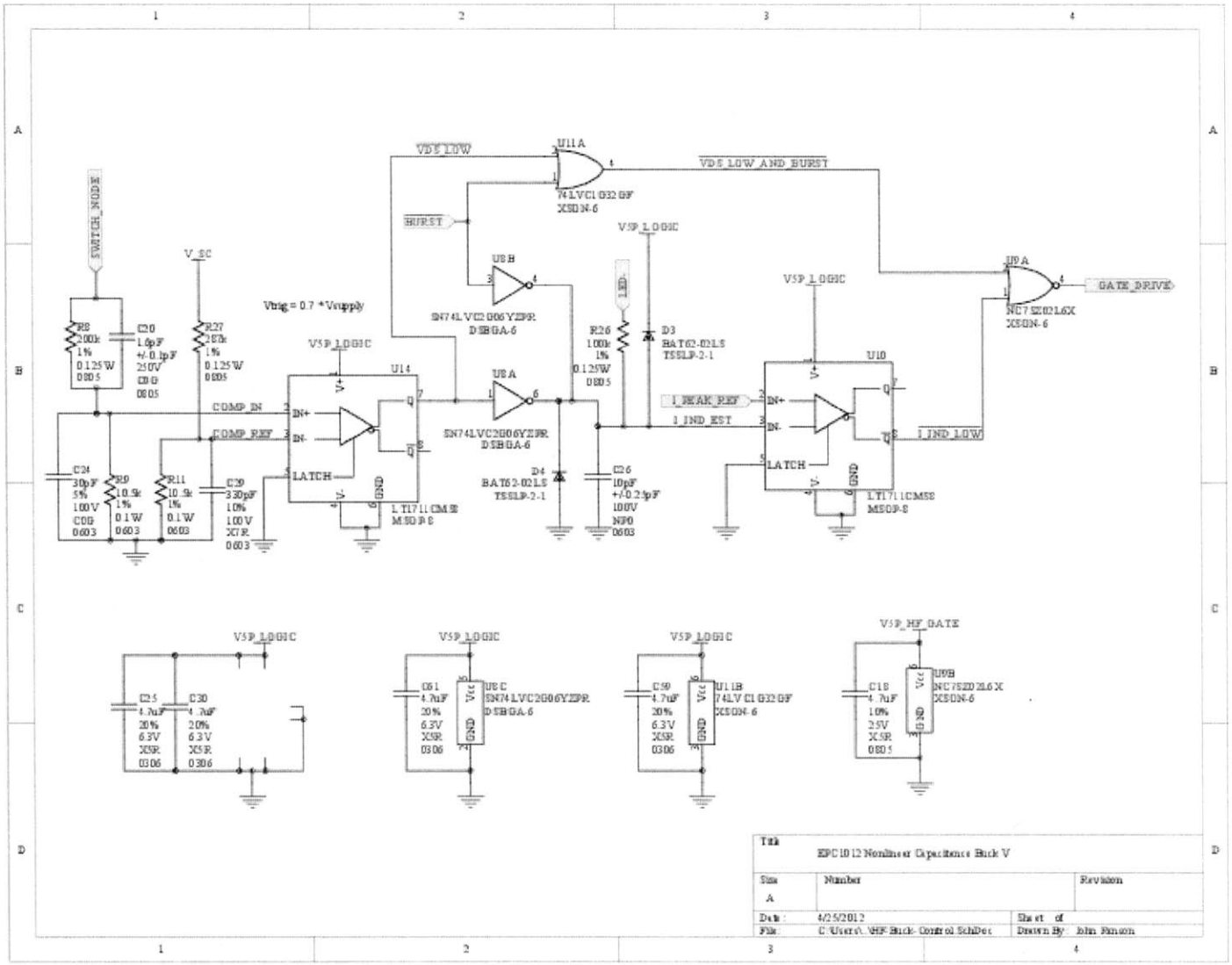
A.1.4 PCB Picture



A.2 Merged 2 Stage

A.2.1 Schematic




VDS_LOW
U11A
74LVC1G32GF
DCSON-6
VDS_LOW_AND_BURST
BURST
V5P_LOGIC
U8B
SN74LVC2G06YZPR
DSBGA-6
SWITCH_NODE
V_SC
R8
200k
1%
0.125W
0805
C20
1.6pF
+/-0.1pF
25V
C0G
0805
R27
187k
1%
0.125W
0805
Vtrig = 0.7 *Vsupply
U14
COMP_IN
COMP_REF
LATCH
GND
LTL711CMSE
MSOP-8
C24
30pF
5%
100V
C0G
0603
R9
10.5k
1%
0.1W
0603
R11
10.5k
1%
0.1W
0603
C29
330pF
10%
100V
X7R
0603
U8A
SN74LVC2G06YZPR
DSBGA-6
D4
BAT62-02LS
TSSLP-2-1
C26
10pF
+/-0.25pF
100V
NP0
0603
R26
100k
1%
0.125W
0805
LED
D3
BAT62-02LS
TSSLP-2-1
U9A
NC7SZ02L6X
DCSON-6
GATE_DRIVE
U10
I_PEAK_REF
I_IND_EST
I_IND_LOW
LTL711CMSE
MSOP-8
C25
4.7uF
20%
6.3V
X5R
0306
C30
4.7uF
20%
6.3V
X5R
0306
C61
4.7uF
20%
6.3V
X5R
0306
U8C
SN74LVC2G06YZPR
DSBGA-6
C50
4.7uF
20%
6.3V
X5R
0306
U11B
74LVC1G32GF
DCSON-6
V5P_HF_GATE
C18
4.7uF
10%
25V
X5R
0805
U9B
NC7SZ02L6X
DCSON-6
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EPC1012 Nonlinear Capacitance Buck V
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Number
Revision
Date:
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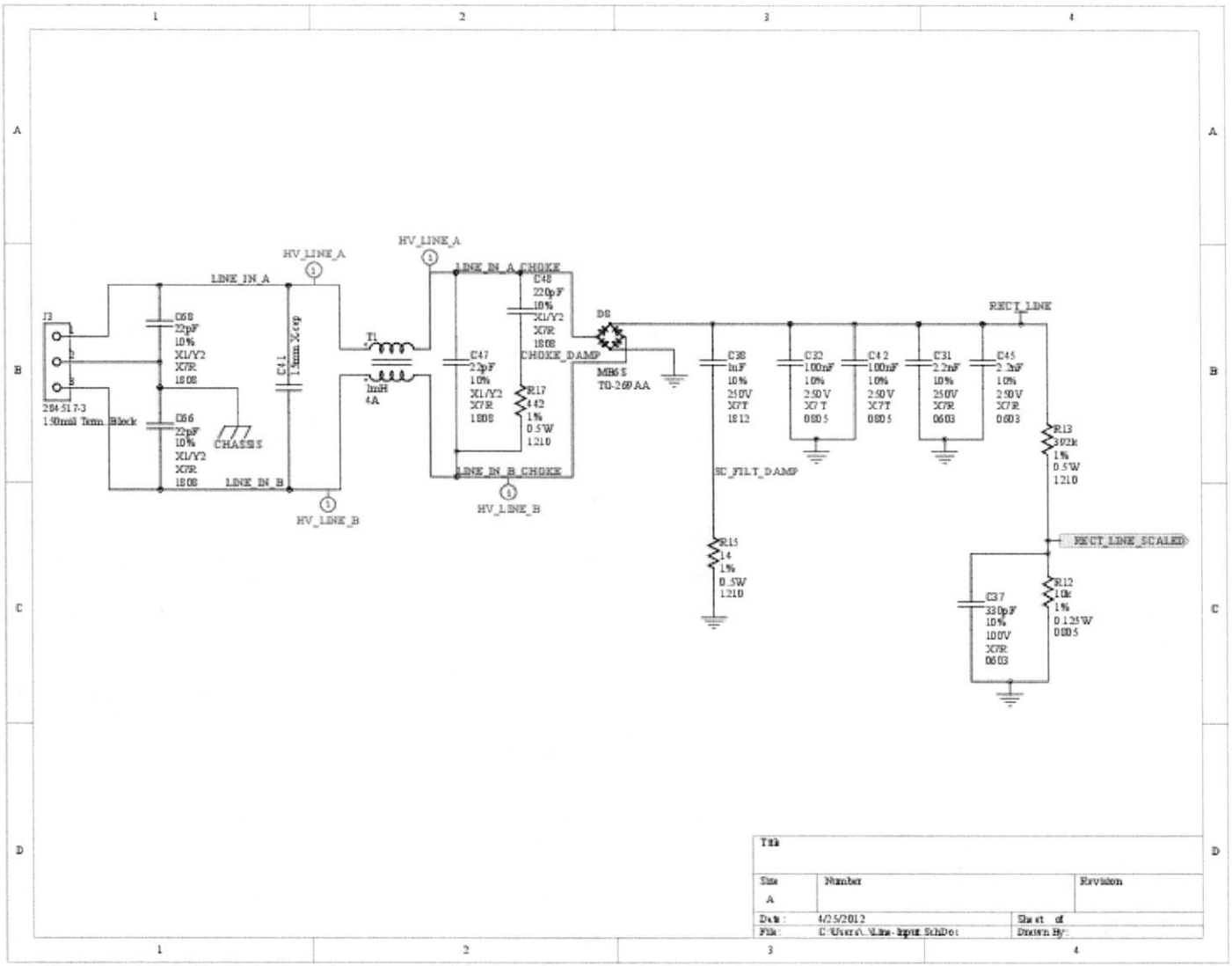
Drawn By:
John Rinson


HV_LINE_A
LINE_IN_A
HV_LINE_A
LINE_IN_A_CHOKE
C48
220pF
10%
X1/Y2
X7R
1808
CHOKE_DAMP
D8
MBRS
TO-269AA
RECT_LINE
J3
284517-3
150mil Term. Block
C68
22pF
10%
X1/Y2
X7R
1808
C66
22pF
10%
X1/Y2
X7R
1808
CHASSIS
C41
1.5mm X-cap
LINE_IN_B
HV_LINE_B
T1
1mH
4A
C47
2.2pF
10%
X1/Y2
X7R
1808
R17
442
1%
0.5W
1210
LINE_IN_B_CHOKE
HV_LINE_B
C38
1nF
10%
250V
X7T
1812
SC_FILT_DAMP
R15
14
1%
0.5W
1210
C32
100nF
10%
250V
X7T
0805
C42
100nF
10%
250V
X7T
0805
C31
2.2nF
10%
250V
X7R
0603
C45
2.2nF
10%
250V
X7R
0603
R13
392k
1%
0.5W
1210
RECT_LINE_SCALED
C37
330pF
10%
100V
X7R
0603
R12
10k
1%
0.125W
0805
Title
Size
A
Number
Revision
Date:
4/25/2012
Sheet of
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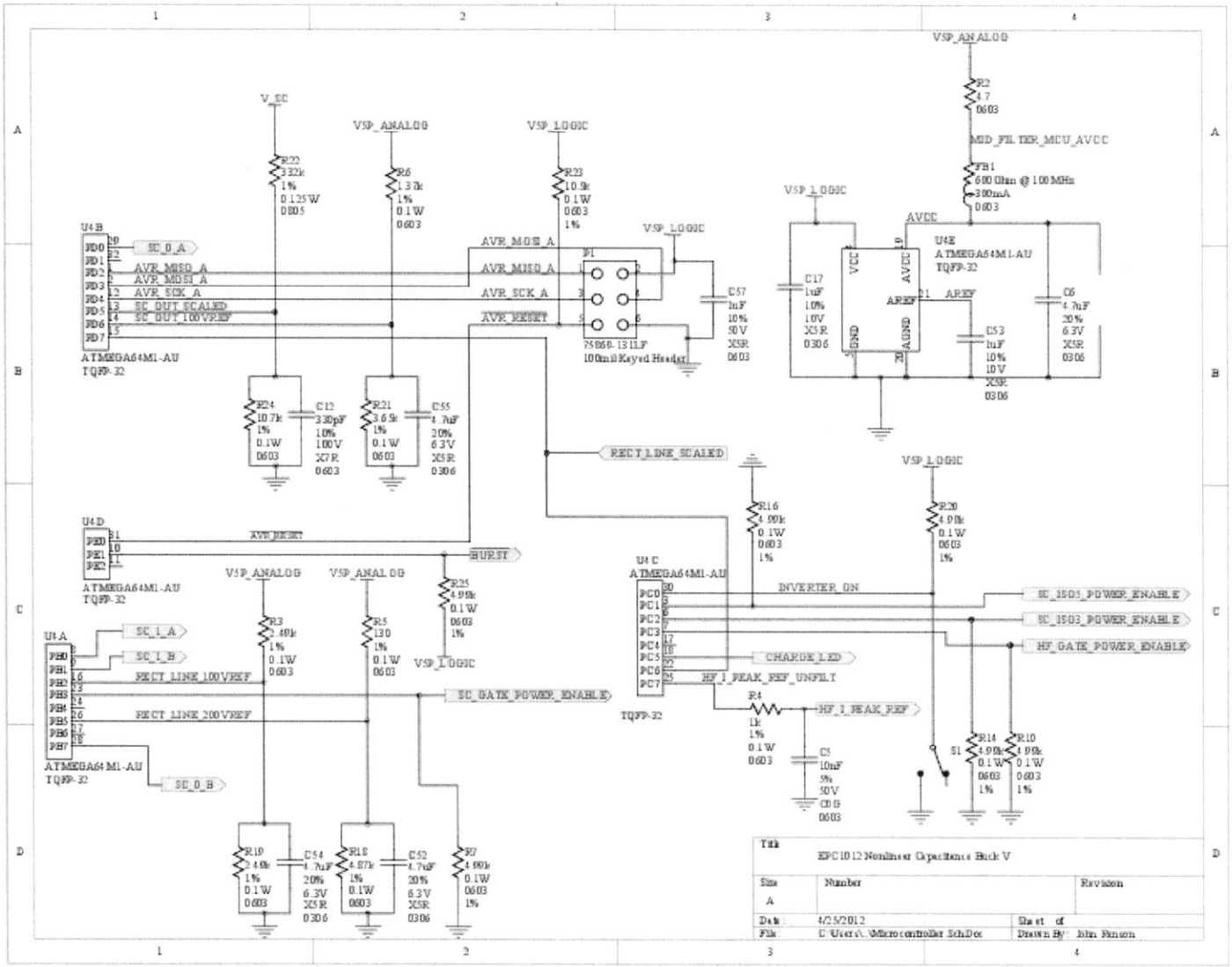
V_SC
VSP_ANALOG
VSP_LOGIC
AVCC
MSD_FILTER_MCU_AVCC
FB1
600 Ohm @ 100 MHz
300mA
0603
R2
4.7
0603
R22
332k
1%
0.125W
0805
R6
1.37k
1%
0.1W
0603
R23
10.5k
0.1W
0603
1%
U4B
ATMEGA64M1-AU
TQFP-32
SC_0_A
AVR_MISO_A
AVR_MOSI_A
AVR_SCK_A
SC_OUT_SCALED
SC_OUT_100VREF
AVR_RESET
JP1
75869-13 1LF
100mil Keyed Header
C57
1nF
10%
50V
X5R
0603
U4E
ATMEGA64M1-AU
TQFP-32
C17
1uF
10%
10V
X5R
0306
C53
1nF
10%
10V
X5R
0306
C6
4.7uF
20%
6.3V
X5R
0306
AREF
R24
10.7k
1%
0.1W
0603
C12
330pF
10%
100V
X7R
0603
R21
8.65k
1%
0.1W
0603
C55
4.7uF
20%
6.3V
X5R
0306
RECT_LINE_SCALED
U4D
ATMEGA64M1-AU
TQFP-32
AVR_RESET
BURST
R16
4.99k
0.1W
0603
1%
R20
4.99k
0.1W
0603
1%
U4C
ATMEGA64M1-AU
TQFP-32
INVERTER_ON
SC_1503_POWER_ENABLE
SC_1503_POWER_ENABLE
HF_GATE_POWER_ENABLE
CHARGE_LED
HF_1_PEAK_REF_UNFILT
R4
1k
1%
0.1W
0603
HF_1_PEAK_REF
C5
10nF
5%
50V
C0G
0603
S1
R14
4.99k
0.1W
0603
1%
R10
4.99k
0.1W
0603
1%
U4A
ATMEGA64M1-AU
TQFP-32
SC_1_A
SC_1_B
RECT_LINE_100VREF
SC_GATE_POWER_ENABLE
RECT_LINE_200VREF
SC_0_B
R3
2.49k
1%
0.1W
0603
R5
130
1%
0.1W
0603
R25
4.99k
0.1W
0603
1%
R19
2.49k
1%
0.1W
0603
C54
4.7uF
20%
6.3V
X5R
0306
R18
4.87k
1%
0.1W
0603
C52
4.7uF
20%
6.3V
X5R
0306
R7
4.99k
0.1W
0603
1%
Title
EPC1012 Nonlinear Capacitance Buck V
Size
A
Number
Revision
Date:
4/25/2012
Sheet of
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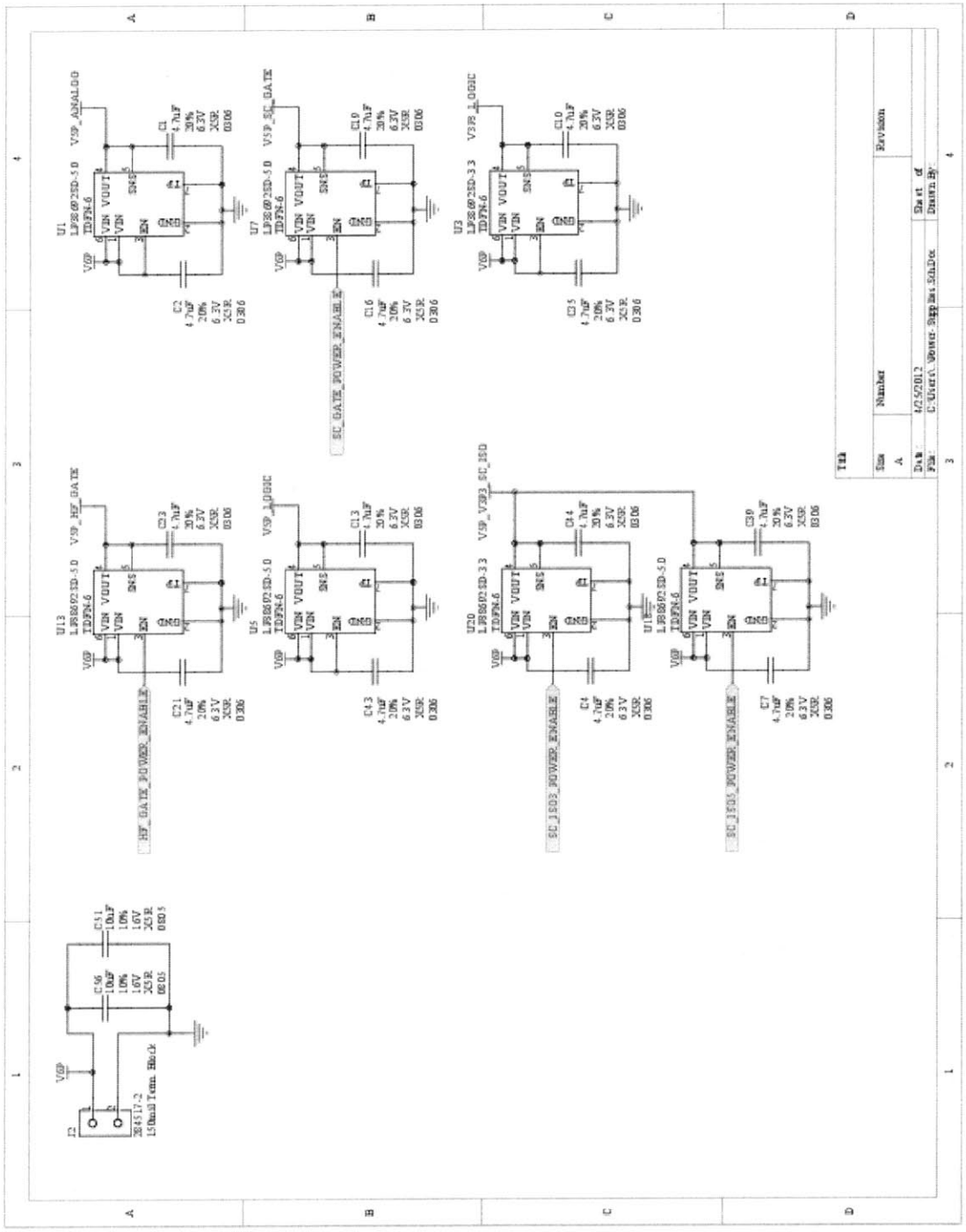
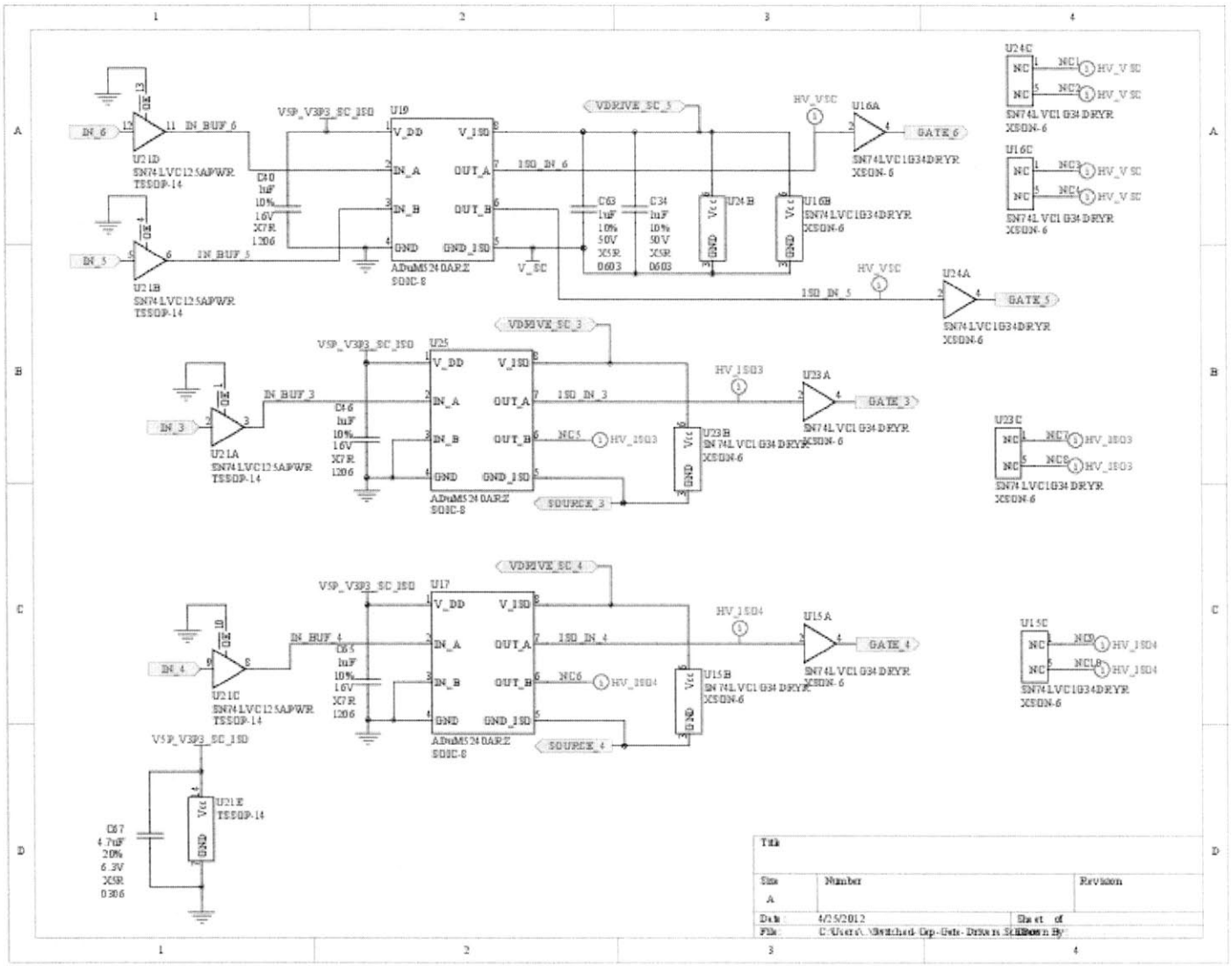
Drawn By:
John Hanson




IN_6
IN_BUF_6
U21D
SN74LVC125APWR
TSSOP-14
VSP_V3P3_SC_ISO
U19
ADuM5240ARZ
SOIC-8
V_DD
V_ISO
IN_A
OUT_A
IN_B
OUT_B
GND
GND_ISO
ISO_IN_6
VDRIVE_SC_5
HV_VSC
U16A
SN74LVC1G34DRYR
XSON-6
GATE_6
C40
1uF
10%
16V
X7R
1206
C63
1uF
10%
50V
X5R
0603
C34
1uF
10%
50V
X5R
0603
U24B
U16B
U24C
U16C
NC
HV_VSC
IN_5
IN_BUF_5
U21B
ISO_IN_5
U24A
GATE_5
VDRIVE_SC_3
U25
IN_3
IN_BUF_3
U21A
C46
ISO_IN_3
HV_ISO3
U23A
GATE_3
U23B
U23C
NC5
NC7
NC8
SOURCE_3
VDRIVE_SC_4
U17
IN_4
IN_BUF_4
U21C
C65
ISO_IN_4
HV_ISO4
U15A
GATE_4
U15B
U15C
NC6
NC10
NC9
SOURCE_4
U21E
C67
4.7uF
20%
6.3V
X5R
0306
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Size
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Number
Revision
Date:
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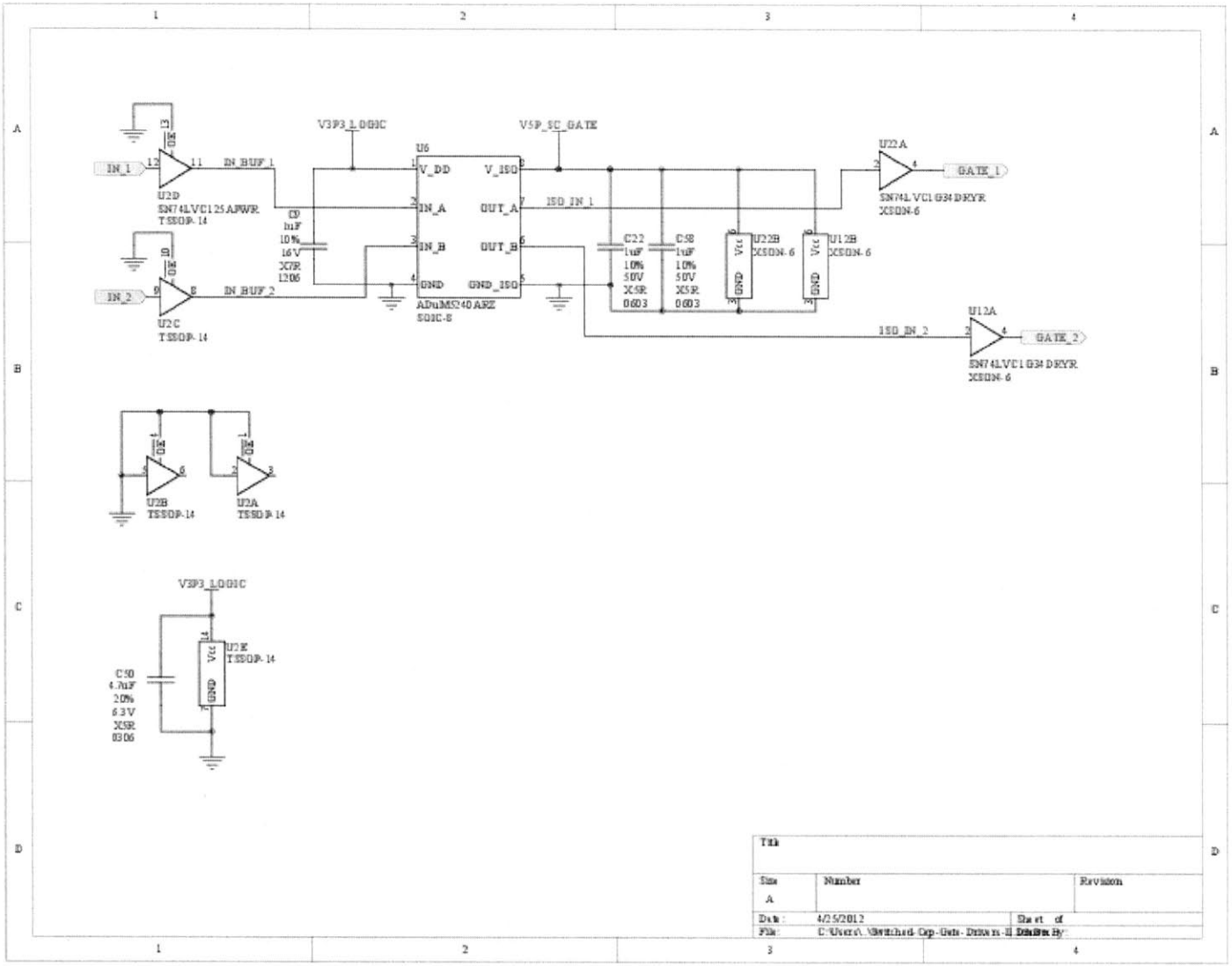
IN_1
IN_BUF_1
U2D
SN74LVC125APWR
TSSOP-14
V3P3_LOGIC
V5P_SC_GATE
U6
V_DD
V_ISO
IN_A
OUT_A
ISO_IN_1
IN_B
OUT_B
GND
GND_ISO
ADuM5240ARZ
SOIC-8
C9
1nF
10%
16V
X7R
1206
C22
1uF
10%
50V
X5R
0603
C58
1uF
10%
50V
X5R
0603
U22A
SN74LVC1G34DBVR
SOT23-5
GATE_1
U22B
SC70N-6
U12B
SC70N-6
IN_2
IN_BUF_2
U2C
TSSOP-14
ISO_IN_2
U12A
SN74LVC1G34DBVR
SOT23-5
GATE_2
U2B
TSSOP-14
U2A
TSSOP-14
V3P3_LOGIC
U2E
TSSOP-14
C50
4.7uF
20%
6.3V
X5R
0306
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Size
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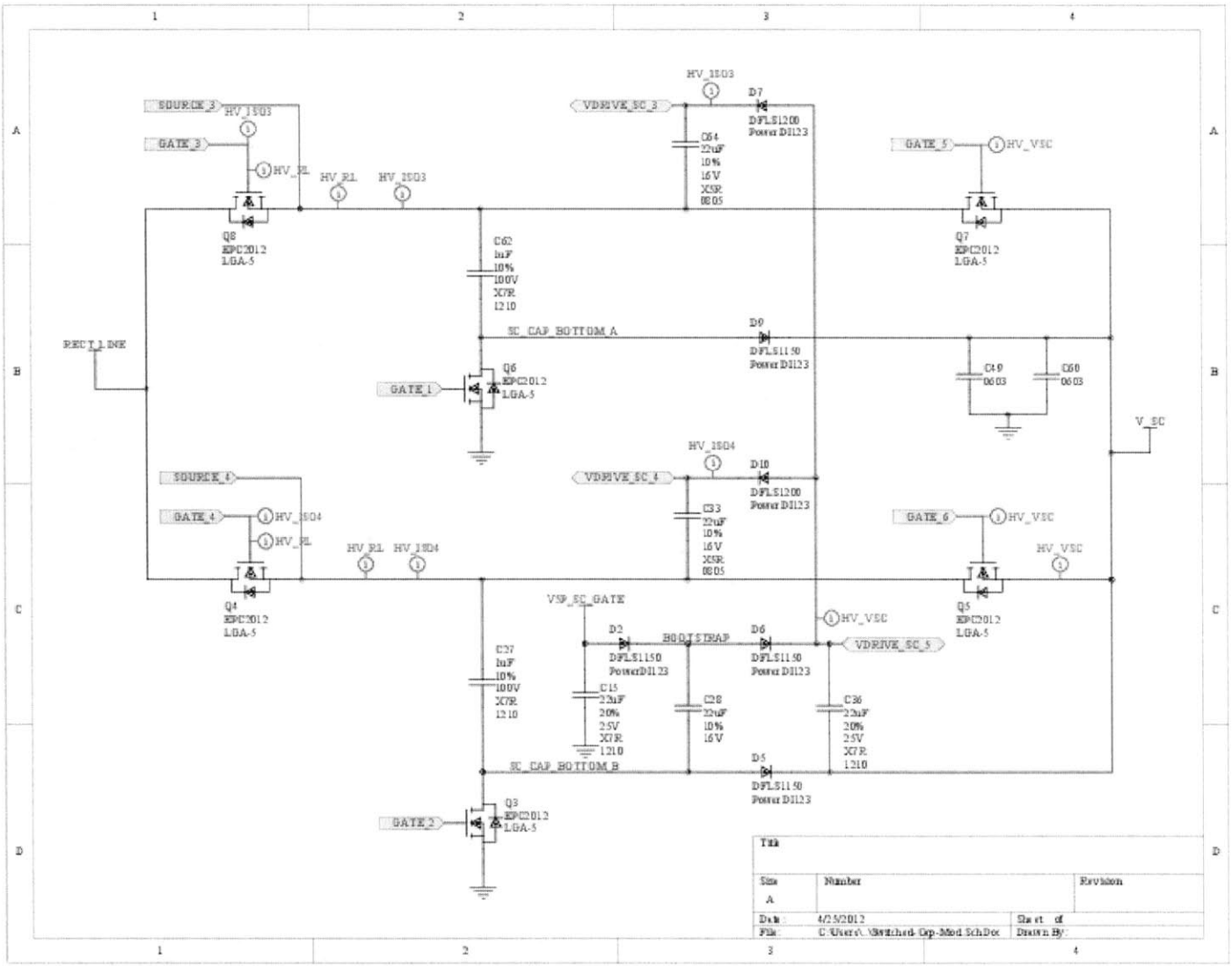
SOURCE_3
GATE_3
HV_1S03
HV_RL
HV_RL
HV_1S03
Q8
EPC2012
LGA-5
C62
1uF
10%
100V
X7R
1210
RECT_LINE
SC_CAP_BOTTOM_A
Q6
EPC2012
LGA-5
GATE_1
VDRIVE_SC_3
HV_1S03
D7
DFLS1200
PowerDI123
C64
22uF
10%
16V
X5R
0805
GATE_5
HV_VSC
Q7
EPC2012
LGA-5
D9
DFLS1150
PowerDI123
C49
0603
C60
0603
V_SC
SOURCE_4
GATE_4
HV_1S04
HV_RL
HV_RL
HV_1S04
Q4
EPC2012
LGA-5
VDRIVE_SC_4
HV_1S04
D10
DFLS1200
PowerDI123
C33
22uF
10%
16V
X5R
0805
GATE_6
HV_VSC
HV_VSC
Q5
EPC2012
LGA-5
VSP_SC_GATE
D2
DFLS1150
PowerDI123
BOOTSTRAP
D6
DFLS1150
PowerDI123
HV_VSC
VDRIVE_SC_5
C27
1uF
10%
100V
X7R
1210
C15
22nF
20%
25V
X7R
1210
C28
22uF
10%
16V
C36
22nF
20%
25V
X7R
1210
SC_CAP_BOTTOM_B
D5
DFLS1150
PowerDI123
Q3
EPC2012
LGA-5
GATE_2
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Revision
Date:
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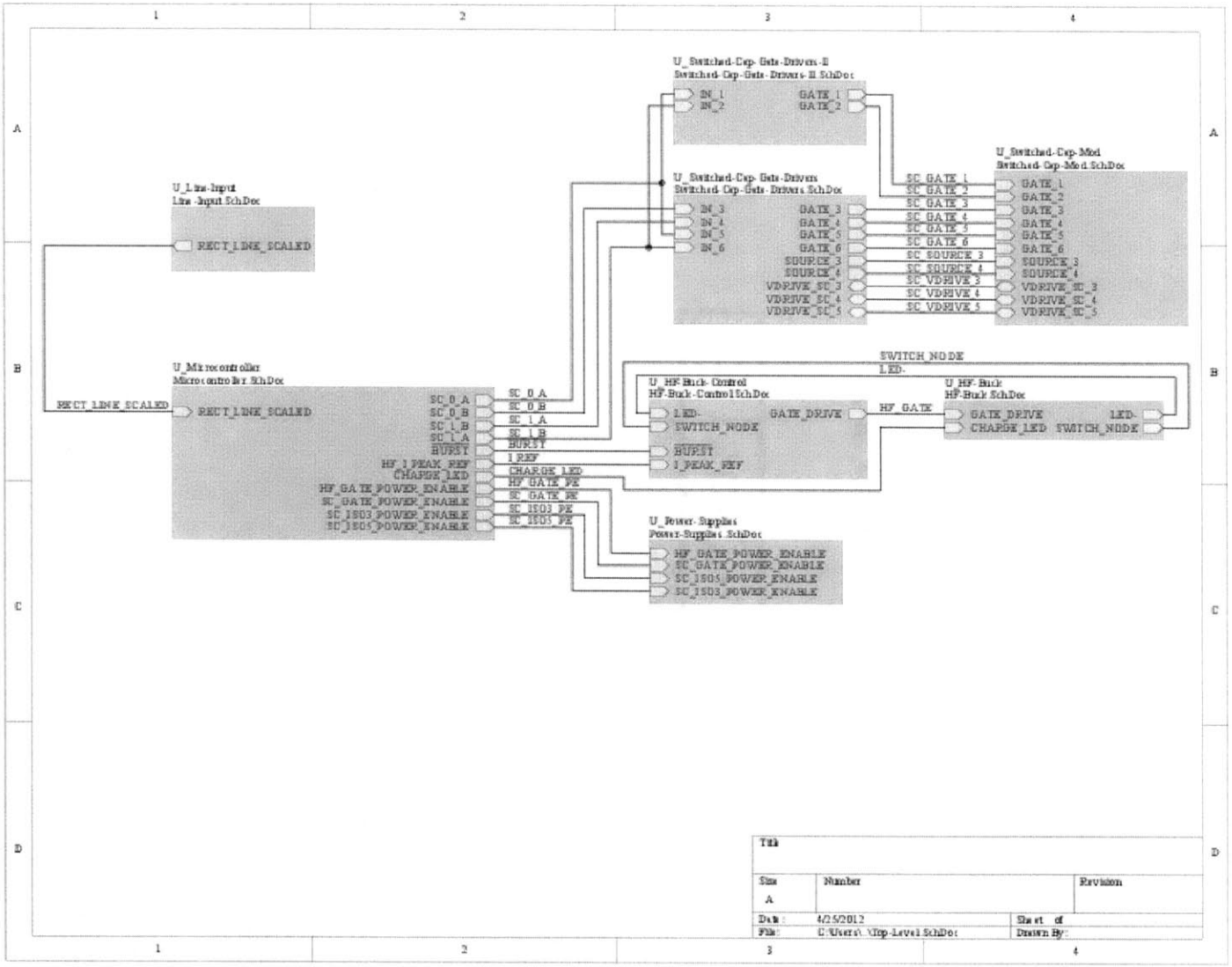
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Switched-Cap-Gate-Drivers-2.SchDoc
IN_1
IN_2
GATE_1
GATE_2
U_Switched-Cap-Gate-Drivers
Switched-Cap-Gate-Drivers.SchDoc
IN_3
IN_4
IN_5
IN_6
GATE_3
GATE_4
GATE_5
GATE_6
SOURCE_3
SOURCE_4
VDRIVE_SC_3
VDRIVE_SC_4
VDRIVE_SC_5
U_Switched-Cap-Mod
Switched-Cap-Mod.SchDoc
SC_GATE_1
SC_GATE_2
SC_GATE_3
SC_GATE_4
SC_GATE_5
SC_GATE_6
SC_SOURCE_3
SC_SOURCE_4
SC_VDRIVE_3
SC_VDRIVE_4
SC_VDRIVE_5
U_Line-Input
Line-Input.SchDoc
RECT_LINE_SCALED
U_Microcontroller
Microcontroller.SchDoc
SC_0_A
SC_0_B
SC_1_A
SC_1_B
BURST
I_REF
CHARGE_LED
HF_GATE_PE
SC_GATE_PE
SC_1S03_PE
SC_1S05_PE
HF_GATE_POWER_ENABLE
SC_GATE_POWER_ENABLE
SC_1S03_POWER_ENABLE
SC_1S05_POWER_ENABLE
SWITCH_NODE
LED-
U_HF-Buck-Control
HF-Buck-Control.SchDoc
GATE_DRIVE
HF_GATE
U_HF-Buck
HF-Buck.SchDoc
CHARGE_LED
U_Power-Supplies
Power-Supplies.SchDoc
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Revision
Date:
4/25/2012
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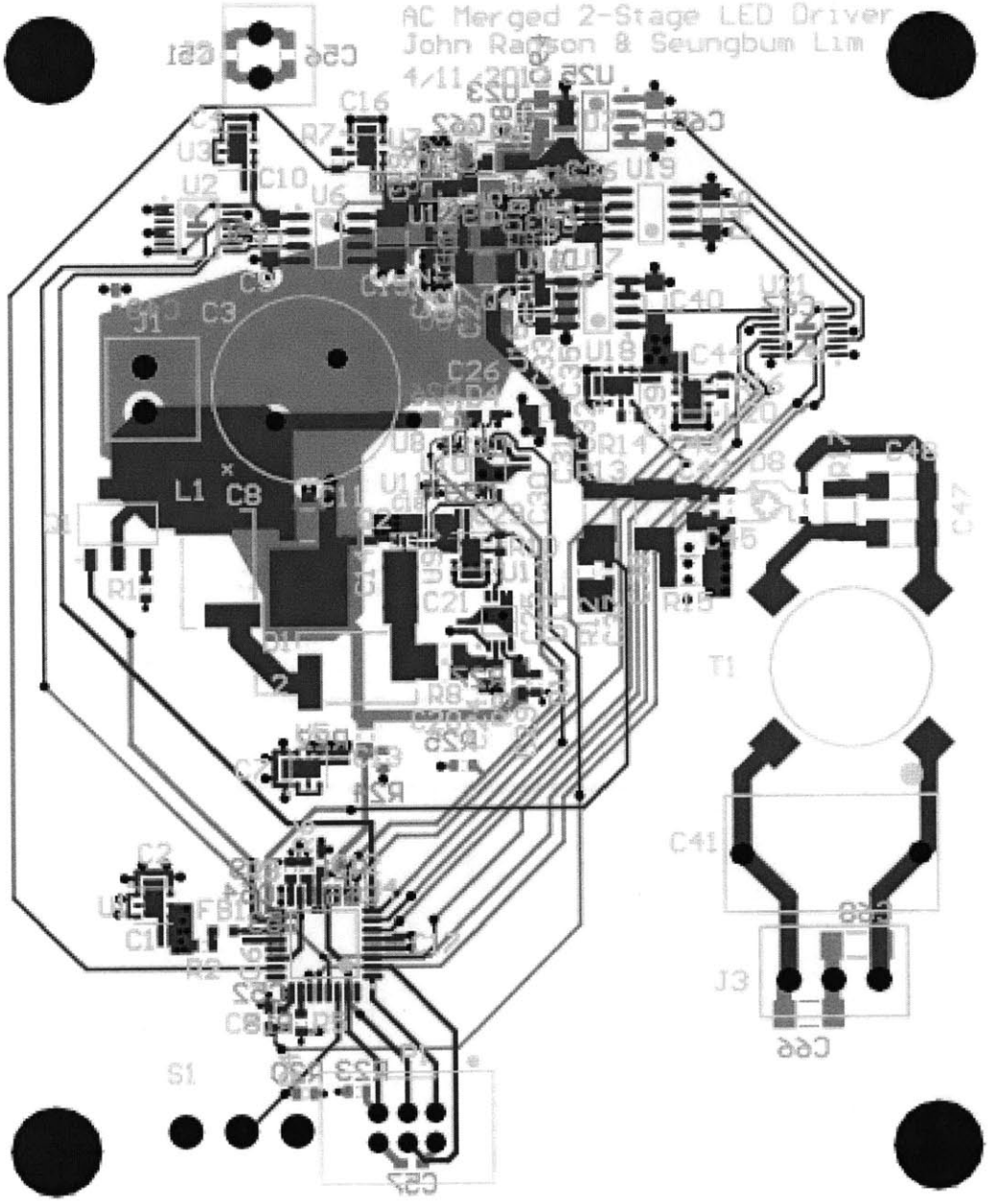
Drawn By:

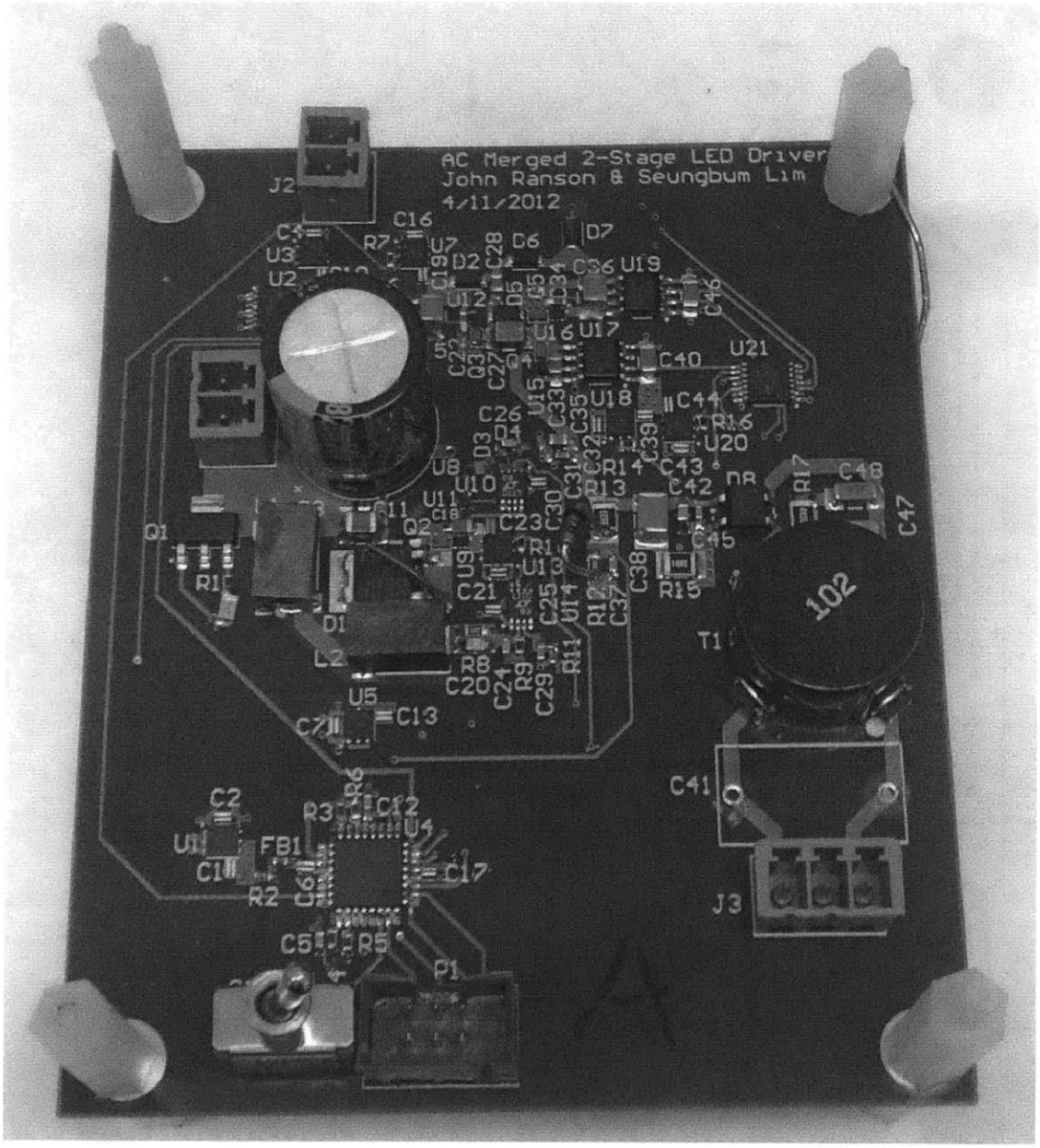
A.2.2 Bill of Materials

Quantity	Designator	Manufacturer	Part Number	Description	Supplier	Supplier PN
1	R1	Panasonic	ERJ3EKF75R0V	Resistor - 75.0 Ohm - 1% - 0603	Digikey	P75.0HCT-ND
1	R17	Panasonic	ERJ1HNF4420U	Resistor - 442 Ohm - 1% - 1210	Digikey	P442AACT-ND
1	R13	Panasonic	ERJ1HNF3923U	Resistor - 392k Ohm - 1% - 1210	Digikey	P392KAACT-ND
1	R22	Panasonic	ERJ6ENF3323V	Resistor - 332k Ohm - 1% - 0805	Digikey	P332KCCT-ND
1	R27	Panasonic	ERJ6ENF2873V	Resistor - 287k Ohm - 1% - 0805	Digikey	P287KCCT-ND
1	R8	Panasonic	ERJ6ENF2003V	Resistor - 200k Ohm - 1% - 0805	Digikey	P200KCCT-ND
1	R5	Panasonic	ERJ3EKF1300V	Resistor - 130 Ohm - 1% - 0603	Digikey	P130HCT-ND
1	R26	Panasonic	ERJ6ENF1003V	Resistor - 100k Ohm - 1% - 0805	Digikey	P100KCCT-ND
1	R15	Panasonic	ERJ1HNF14R0U	Resistor - 14 Ohm - 1% - 1210	Digikey	P14.0AACT-ND
1	R24	Panasonic	ERJ3EKF10R7V	Resistor - 10.7k Ohm - 1% - 0603	Digikey	P10.7KHCT-ND
3	R9, R11, R23	Panasonic	ERJ3EKF1052V	Resistor - 10.5k Ohm - 1% - 0603	Digikey	P10.5KHCT-ND
1	R12	Panasonic	ERJ6ENF1002V	Resistor - 10k Ohm - 1% - 0805	Digikey	P10.0KCCT-ND
6	R7, R10, R14, R16, R20, R25	Panasonic	ERJ3EKF4991V	Resistor - 4.99k Ohm - 1% - 0603	Digikey	P4.99KHCT-ND
1	R18	Panasonic	ERJ3EKF4871V	Resistor - 4.87k Ohm - 1% - 0603	Digikey	P4.87KHCT-ND
1	R2	Panasonic	ERJ8RQF4R7V	Resistor - 4.7 Ohm - 1% - 0603	Digikey	P4.7AJCT-ND
1	R21	Panasonic	ERJ3EKF3651V	Resistor - 3.65k Ohm - 1% - 0603	Digikey	P3.65KHCT-ND
2	R3, R19	Panasonic	ERJ3EKF2491V	Resistor - 2.49k Ohm - 1% - 0603	Digikey	P2.49KHCT-ND
1	R6	Panasonic	ERJ3EKF1371V	Resistor - 1.37k Ohm - 1% - 0603	Digikey	P1.37KHCT-ND
1	R4	Panasonic	ERJ3EKF1001V	Resistor - 1k Ohm - 1% - 0603	Digikey	P1.00KHCT-ND
1	D8	Vishay	MB6S	Diode - Bridge - 600V - 0.5A - TO-269AA	Digikey	MB6S-E3/80GICT-ND
2	U15, U14	Linear	LT1711CMS8	Comparator - 4.5ns - +/- 6V	Digikey	LT1711CMS8#PBF
5	U1, U5, U7, U13, U18	Texas Instruments	LP38692SD-5.0	LDO Regulator - 5V - 1A	Digikey	LP38692SD-5.0/CT-ND
2	U3, U20	Texas Instruments	LP38692SD-3.3	LDO Regulator - 3.3V - 1A	Digikey	LP38692SD-3.3/CT-ND
1	Q1	Diodes Inc	FZT696B	BJT - NPN - 250V - 0.5A	Digikey	FZT696BCT-ND
1	S1	E-Switch	100SP1T1B4M2QE	Switch - Toggle - SPDT	Digikey	EG2353-ND
2	D7, D10	Diodes Inc	DFLS1200	Diode - Schottky - 200V - 1A - PowerDI 123	Digikey	DFLS1200CT-ND
4	D2, D5, D6, D9	Diodes Inc	DFLS1150	Diode - Schottky - 150V - 1A - PowerDI 123	Digikey	DFLS1150CT-ND
2	D3, D4	Infineon	BAT62-02LS	Diode - RF Schottky - 40V - 20mA - TSSLP-2	Digikey	BAT 62-02LS E6327CT-ND
1	U4	Atmel	ATMEGA64M1-AU	Microcontroller - 8-bit AVR - 64KB Flash - 16MHz	Digikey	ATMEGA64M1-AU-ND
4	U6, U17, U19, U25	Analog Devices	ADuM5240ARZ	Isolator & Power Supply	Digikey	ADUM5240ARZ-ND
1	J3	Tyco Electronics	284517-3	Terminal Block - Two Piece - 150mil - 1x3	Digikey	A98411-ND
2	J1, J2	Tyco Electronics	284517-2	Terminal Block - Two Piece - 150mil - 1x2	Digikey	A98410-ND
6	C3, C4, C5, C6, C7, C8	EPC	EPC2012	HEMT - GaN - 200V - 3A	Digikey	917-1017-1-ND
1	Q2	EPC	EPC1012	HEMT - GaN - 200V - 3A	Digikey	917-1005-1-ND
1	P1	FCI	75869-1311LF	Header - Keyed - 100mil - 2x2	Digikey	609-2945-ND
24	C1, C2, C4, C6, C7, C10, C13, C16, C19, C21, C23, C25, C30, C35, C39, C43, C44, C50, C52, C54, C55, C59, C61, C67	Taiyo Yuden	UMK107BJ475MV-T	Capacitor - 4.7uF - 6.3V - X5R - 0306	Digikey	587-3128-1-ND
1	C18	Taiyo Yuden	TMK212BJ475KD-T	Capacitor - 4.7uF - 25V - X5R - 0805	Digikey	587-2992-1-ND
2	C51, C52	Taiyo Yuden	EMK212ABJ106KD-T	Capacitor - 10uF - 16V - X5R - 0805	Digikey	587-2983-1-ND
2	C15, C38	Taiyo Yuden	TMK325B7226MM-TR	Capacitor - 22uF - 25V - X7R - 1210	Digikey	587-2784-1-ND
5	C22, C34, C57, C58, C63	Taiyo Yuden	UMK107BJ105KA-T	Capacitor - 1uF - 50V - X5R - 0603	Digikey	587-2400-1-ND
1	C11	Taiyo Yuden	UMK325BJ106KM-T	Capacitor - 10uF - 50V - X5R - 1210	Digikey	587-2247-1-ND
4	C9, C40, C46, C65	Taiyo Yuden	EMK316B7105KF-T	Capacitor - 1uF - 16V - X7R - 1206	Digikey	587-1945-1-ND
1	FB1	Taiyo Yuden	BK1608HW601-T	Ferrite Bead - 0603 - 600 Ohm @ 100MHz	Digikey	587-1879-1-ND
2	C17, C53	Taiyo Yuden	LWK107B7105KA-T	Capacitor - 1uF - 10V - X5R - 0306	Digikey	587-1783-1-ND
2	C27, C62	Taiyo Yuden	HMK325B7105KN-T	Capacitor - 1uF - 100V - X7R - 1210	Digikey	587-1365-1-ND
1	U11	NXP	74LVC1G32GF	OR Gate - 2.4ns - 1.65V - 5.5V	Digikey	568-9331-1-ND
1	U9	Fairchild	NC7SZ02L6X	NOR Gate - 2.4ns - 1.65V - 5.5V	Mouser	512-NC7SZ02L6X
1	D1	ST Microelectronics	STPS10170CB-TR	Diode - Schottky - 170V - 2x5A - DPAK	Digikey	497-6075-1-ND
1	C3	Nichicon	UHE1H821MHD6	Capacitor - 820uF - 50V - Aluminum - 16mm Radial	Digikey	493-1625-ND
1	C20	Murata	GQM2195C2E1R6BB12D	Capacitor - 1.6pF - 250V - C0G - 0805	Digikey	490-3293-1-ND
2	C31, C45	Murata	GRM188R72E222KW07D	Capacitor - 2.2nF - 250V - X7R - 0603	Digikey	490-3530-1-ND
1	C48	Murata	GA342DR7GF221KW02L	Capacitor - 220pF - X1/Y2 - X7R - 1808	Digikey	490-3473-1-ND
3	C47, C66, C68	Murata	GA342D1XGF225JY02L	Capacitor - 2.2pF - X1/Y2 - X7R - 1808	Digikey	490-3463-1-ND
3	C12, C29, C37	Murata	GRM188R72A331KA01D	Capacitor - 330pF - 100V - X7R - 0603	Digikey	490-1464-1-ND
1	C24	Murata	GRM1885C2A300JA01D	Capacitor - 30pF - 100V - C0G - 0603	Digikey	490-1339-1-ND
1	C28	TDK	C4532X7J2E105K	Capacitor - 1uF - 250V - X7T - 1812	Digikey	445-7769-1-ND
2	C32, C42	TDK	C2012X7J2E104K	Capacitor - 100nF - 250V - X7T - 0805	Digikey	445-7749-1-ND
1	C5	TDK	C1608C0G1H103J	Capacitor - 10nF - 50V - C0G - 0603	Digikey	445-7404-1-ND
3	C36, C33, C64	TDK	C2012X5R1C226K	Capacitor - 22uF - 16V - X5R - 0805	Digikey	445-6797-1-ND
1	C26	TDK	C1608C0G1H100C	Capacitor - 10pF - 100V - NP0 - 0603	Digikey	445-5048-1-ND
6	U12, U15, U16, U22, U23, U24	Texas Instruments	SN74LVC1G34DRYR	Buffer - 2.9ns - 1.65 - 5.5V	Digikey	296-29051-1-ND
1	U8	Texas Instruments	SN74LVC2G06YZPR	Inverter - Dual - Open Drain - 2.4ns - 1.65 - 5.5V	Digikey	296-17987-1-ND
2	U2, U21	Texas Instruments	SN74LVC125APWR	Buffer - Quad - 3-state - 1.65V - 3.6V	Digikey	296-1222-1-ND
2	L1, L2	Coilcraft	132-18SMSKLB	Coilcraft Maxispring Inductor - 422nH	Coilcraft	132-18SMSKLB
1	T1	Bourns	PM2706-4T-RC	Common Mode Choke - 1mH - 3.9uH	Newark	63K2822
1	C41	NONE	TBD-X2AP150M			
4	C8, C14, C49, C60	NONE	TBD-06C3			

A.2.3 PCB Layout



A.2.4 PCB Picture



Appendix B

Gate Drive IC testing

This project presented a unusual set of requirements for the gate driver. Because the gate drive was triggered on the falling edge of the drain-source waveform, the driver delay has to be very small. Given that ZVS isn't fully achieved, the rise and fall time of the driver has to be very small. Finally, the GaN devices require a 6V maximum gate drive with minimal ringing that might damage the gate or cause spurious switching. I tested a variety of gate drivers and logic ICs in two configurations, driving a 100pF capacitor and hard switching on an EPC1012 HEMT at 30V, shown in figure B-1. The inputs to the drivers were driven with low frequency 5V square wave, and input, output and drain voltage (where applicable) were measured using 500MHz scope probes on a 500MHz scope.

The results of this test, shown in table B.1, were useful but not entirely conclusive. The rise and fall times reported are the 10-90%, measured to the first instance

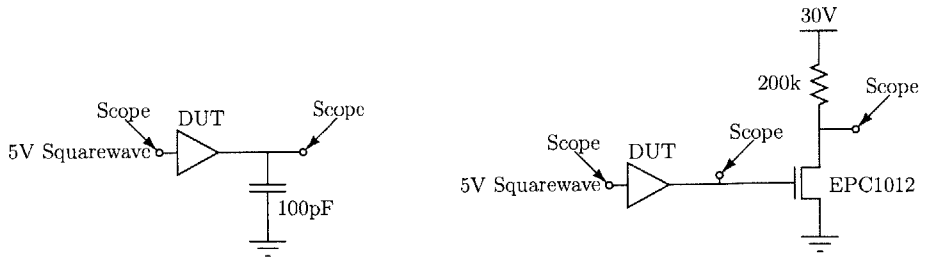


Figure B-1: Gate Drive Testing Circuits

Table B.1: Gate Drive Test Results

Part Config	100pF Capacitor [ns]				EPC1012 Transistor [ns]				Ringing Amount
	t_r	t_f	t_{pd-h}	t_{pd-l}	t_r	t_f	t_{pd-h}	t_{pd-l}	
EL7155	3.4	13.5	3.2	14.3	5.2	14.8	3.7	14.9	None
IDT74FCT807CTQG									BAD
ISL5510IRZ	2	10.5	2	10.8	3.4	10.5	2.9	11.3	Small
LT1711 Driving 6 Parallel NC7SZ02	1	5.5	1.1	5.6	0.9	5.6	1.6	5.5	Big*
MAX5048 Inverting	4	16.6	1.5	20.6	4.6	17.3	2	21	Big
MAX5048 Non-Inverting	4	18.7	1.6	15.9	4.6	21.4	1.9	17.2	Big
NC7SZ04L6X Tapered 1 - 2 - 6	1	3.7	1	4.2	0.8	3.8	1.5	4.2	Big*
NC7SZ04L6X Tapered 1 - 3	1.3	3	1.5	2.8	2.4	2.9	2.1	3.2	Big*
NC7SZ04L6X Tapered 1 - 4	1	3	1.2	2.7	0.9	3	1.7	2.7	Big*
NC7SZ04L6X	2.3	2.3	3.3	3	5.2	2.3	5.4	4.3	Big*

of reaching the target voltage. The propagation delays reported are midpoint to midpoint. The NC7 logic family were clearly the fastest. All drivers, save the Intersil EL7155, showed some amount of ringing. However, with the NC7 logic family components, the ringing visible in the gate voltage matched the ringing visible in the drain voltage. This suggests that the ringing for these parts may due to ground bounce in the scope instead of actual ringing of the gate voltage. These devices, especially when paralleled, had sub-nanosecond rise and fall times. This would indicate that multiple amperes were being drawn in pulses of less than a nanosecond. It would be unreasonable to expect a 500MHz scope to accurately measure these data. Figures B-2 through B-4 demonstrate a variety of waveforms from driving the EPC1012 devices, showing the issues mentioned.

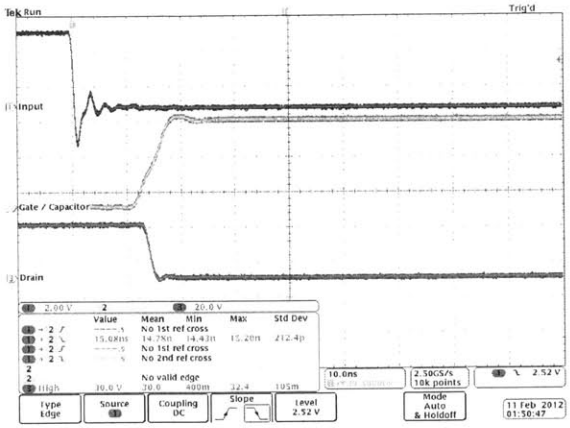


Figure B-2: EL7155 switching on (hard) without ringing

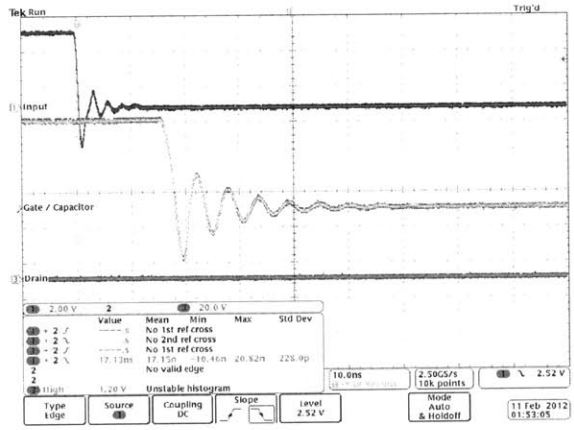


Figure B-3: MAX5048 switching off (soft) with significant ringing

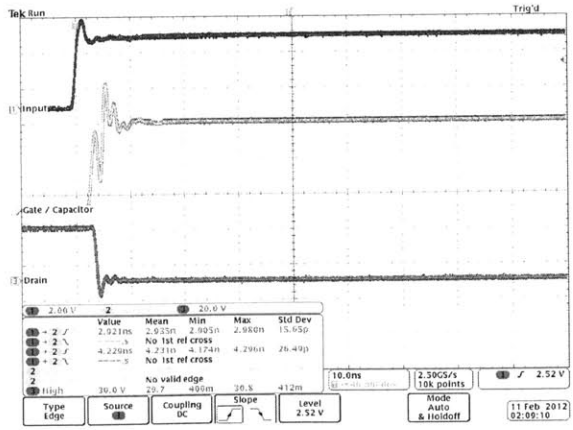


Figure B-4: NC7SZ04L6X 1-3 taper switching on (hard) with potential measurement ground bounce

Appendix C

MATLAB Code

C.1 Single Cycle Simulation

C.1.1 Function SimulateWaveforms

```
function [ Vswitch_V, Iswitch_A, Vdiode_V, Idiode_A, Vind_V,
    Iind_A, T_s ] = ...
SimulateWaveforms( Vin_V, Vled_V, Ton_s, L_H, Coss_F, Cj_F,
    Cind_F, Rsw_Ohm)
%SimulateWaveforms Simulate a complete single cycle of the
    circuit
%
%   Inputs
%   Vin_V - scalar - Input supply voltage [Volts]
%   Vled_V - scalar - LED string voltage [Volts]
%   Ton_s - scalar - on time [nanoseconds]
%   L_H - scalar - Inductor inductance [nanoHenries]
%   Coss_F - function - Incremental transistor output
    capacitance versus
%   drain source voltage [Volts to Farads]
%   Cj_F - function - Incremental diode capacitance versus
```

```
    reverse voltage
%   [Volts to Farads]
%   Cind_F - scalar - Inductor capacitance to ground [Farads]
%   Rsw_Ohm - scalar - Transistor on resistance [Ohms]
%
%   Outputs
%   V_switch_V - vector - switch drain voltage [Volts]
%   V_diode_V - vector - diode reverse voltage [Volts]
%   I_ind_A - matrix - inductor current - first column is
    inductive
%   current, second column is capacitive current from Cind [
    Amperes]
%   I_diode_A - matrix - inductor current - first column is
    forward
%   current, second column is capacitive current from Cj [
    Amperes]
%   I_switch_A - matrix - switch current - first column is on
    -state
%   current, second column is capacitive current from Coss [
    Amperes]
%   T_s - vector - time [seconds]
%   Vzvs - scalar - voltage at which switching is occuring [
    Volts]

Cnode_F = @(V) ((Coss_F(V)+Cj_F(Vin_V-V)+Cind_F));


[ Vring_V, Iring_A, Tring_s ] = SimulateRing( Vin_V, Vled_V,
    Cnode_F, L_H, 0);
```

```
[ Vdisc_V, IdiscR_A, Idisc_A, Tdisc_s ] =SimulateDisc( Vin_V,
    Vled_V, Cnode_F, L_H, Rsw_Ohm, Vring_V(end), Iring_A(end)
    , Tring_s(end));

[ Von_V, Ion_A, Ton_s ] = SimulateOn( Vin_V, Vled_V, Ton_s,
   L_H, Idisc_A(end), Tdisc_s(end));

[ Vrise_V, Irise_A, Trise_s ] = SimulateRise( Vin_V, Vled_V,
   Cnode_F, L_H, Ion_A(end), Ton_s(end));

[ Voff_V, Ioff_A, Toff_s ] = SimulateOff( Vin_V, Vled_V, L_H,
    Irise_A(end), Trise_s(end));



Vswitch_V = [Vring_V; Vdisc_V(2:end); Von_V; Vrise_V(2:end);
   Voff_V];
Vdiode_V = Vin_V-Vswitch_V;
Vind_V = Vin_V-Vled_V-Vswitch_V;



ICind_A = -Cind_F./(Cnode_F(Vswitch_V)).*[Iring_A; Idisc_A(2:
   end); 0 ; 0 ; Irise_A(2:end); 0 ;0];
ICswitch_A = Coss_F(Vswitch_V)./(Cnode_F(Vswitch_V)).*[
   Iring_A; Idisc_A(2:end); 0 ; 0 ; Irise_A(2:end); 0 ; 0];
ICdiode_A = Cj_F(Vdiode_V)./(Cnode_F(Vswitch_V)).*[Iring_A;
   Idisc_A(2:end); 0 ; 0 ; Irise_A(2:end); 0 ; 0];

T_s = [Tring_s; Tdisc_s(2:end); Ton_s; Trise_s(2:end); Toff_s
   ];
```

```
Iind_A = [Iring_A' Idisc_A(2:end)' Ion_A' Irise_A(2:end)'
    Ioff_A' ; ICind_A'];
Iswitch_A = [zeros(size(Iring_A')) IdiscR_A(2:end)' Ion_A'
    zeros(size([Irise_A(2:end)' Ioff_A'])) ; ICswitch_A'];
Idiode_A = [zeros(size([Iring_A' Idisc_A(2:end)' Ion_A'
    Irise_A(2:end)'])) Ioff_A' ; ICdiode_A'];

end
```

C.1.2 Function SimulateOff

```
function [ V_V, I_A, T_s ] = SimulateOff( Vin_V, Vled_V, L_H
    , i0_A, t0_s)
%SimulateOff Simulate the circuit as the current falls back
    to zero volts
%when the switch is off

%   Inputs
%   Vin_V - scalar - Input supply voltage [Volts]
%   Vled_V - scalar - LED string voltage [Volts]
%   L_H - scalar - Inductor inductance [Henries]
%   t0_s - scalar - Simulation starting time [seconds]
%   i0_A - scalar - Simulation starting inductor current [
    Amperes]
%
%   Outputs
%   V_V - scalar - drain voltage [Volts]
%   I_A - scalar - inductor current [Amperes]
%   T_s - scalar - time [seconds]
```

```
I_A = [i0_A; 0];
T_s = [t0_s+1e-12 ; t0_s+i0_A*L_H/Vled_V];
V_V = [Vin_V; Vin_V];

end
```

C.1.3 Function SimulateRing

```
function [ V_V, I_A, T_s ] = SimulateRing( Vin_V, Vled_V,
    Cnode_F, L_H, t0_s)
%SimulateRing Simulate the circuit as the voltage rings down
    from Vin
%as the inductor current goes negative
%
%   Inputs
%   Vin_V - scalar - Input supply voltage [Volts]
%   Vled_V - scalar - LED string voltage [Volts]
%   Cnode_F - function - Incremental total capacitance on the
    drain node
%   [Volts to Farads]
%   L_H - scalar - Inductor inductance [Henries]
%   t0_s - scalar - Simulation starting time [seconds]
%
%   Outputs
%   V_V - vector - drain voltage [Volts]
%   I_A - vector - inductor current [Amperes]
%   T_s - vector - time [seconds]


tsteps = 1000;
```

```
VledP_V = Vin_V-Vled_V;

dv_V = Vin_V/tsteps;

V_V = (Vin_V:-dv_V:0)';
I_A = zeros(tsteps+1,1);
T_s = zeros(tsteps+1,1);
T_s(1) = t0_s;

dt_s=sqrt(L_H*Cnode_F(Vin_V))*acos(1-dv_V/Vled_V);
iter = 1;

while ( dt_s >= 0 && iter <= tsteps)


    di_A = - dt_s * (V_V(iter) - VledP_V)/L_H;

    I_A(iter+1) = I_A(iter) + di_A;
    T_s(iter+1) = T_s(iter) + dt_s;
    iter = iter + 1;
    dt_s = - dv_V/(I_A(iter) / Cnode_F(V_V(iter)));
end

if (dt_s < 0)
    iter = iter -1;
    V_V=V_V(1:iter);
    I_A=I_A(1:iter);
    T_s=T_s(1:iter);
end
```

```
end
```

C.1.4 Function SimulateDisc

```
function [ V_V, IR_A, I_A, T_s ] = SimulateDisc( Vin_V,
    Vled_V, Cnode_F, L_H, Rsw_Ohm, v0_V, i0_A, t0_s)
%SimulateRise Simulate the circuit as the voltage rises after
    switch turn
%off
%
%   Inputs
%   Vin_V - scalar - Input supply voltage [Volts]
%   Vled_V - scalar - LED string voltage [Volts]
%   Cnode_F - function - Incremental total capacitance on the
    drain node
%   [Volts to Farads]
%   L_H - scalar - Inductor inductance [Henries]
%   Rsw_Ohm - scalar - Transistor on resistance [Ohms]
%   v0_V - scalar - Simulation starting drain voltage [Volts]
%   i0_A - scalar - Simulation starting inductor current [
    Amperes]
%   t0_s - scalar - Simulation starting time [seconds]
%
%   Outputs
%   V_V - vector - drain voltage [Volts]
%   IR_A - vector - switch conducted current [Amperes]
%   I_A - vector - inductor current [Amperes]
%   T_s - vector - time [seconds]

tsteps = 100;
```

```
VledP_V = Vin_V-Vled_V;

dv_V = v0_V/tsteps;

V_V = (v0_V:-dv_V:0)';
I_A = zeros(tsteps+1,1);
IR_A = zeros(tsteps+1,1);
T_s = zeros(tsteps+1,1);

iter = 1;

I_A(1) = i0_A;
T_s(1) = t0_s;
IR_A(1) = v0_V/Rsw_Ohm;

while ( iter <= tsteps)
    IR_A(iter);
    I_A(iter);
    dt_s = dv_V/( (IR_A(iter) - I_A(iter)) / Cnode_F(V_V(iter
       )));

    di_A = - dt_s * (V_V(iter) - VledP_V)/L_H;

    IR_A(iter+1) = V_V(iter+1)/Rsw_Ohm;
    I_A(iter+1) = I_A(iter) + di_A;
    T_s(iter+1) = T_s(iter) + dt_s;
    iter = iter + 1;
end
```

```
end
```

C.1.5 Function SimulateOn

```
function [ V_V, I_A, T_s ] = SimulateOn( Vin_V, Vled_V,
    Ton_s, L_H, i0_A, t0_s)
%SimulateOn Simulate the circuit as the inductor current
    rises while the
%switch is on
%
%   Inputs
%   Vin_V - scalar - Input supply voltage [Volts]
%   Vled_V - scalar - LED string voltage [Volts]
%   L_H - scalar - Inductor inductance [Henries]
%   Ton_s - scalar - on time [seconds]
%   t0_s - scalar - Simulation starting time [seconds]
%   i0_A - scalar - Simulation starting inductor current [
    Amperes]
%
%   Outputs
%   V_V - scalar - drain voltage [Volts]
%   I_A - scalar - inductor current [Amperes]
%   T_s - scalar - time [seconds]

VledP_V = Vin_V-Vled_V;

T_s = [t0_s+1e-12 ; t0_s + Ton_s - i0_A*L_H/(VledP_V)];
I_A = [i0_A ; Ton_s*(VledP_V)/L_H];
V_V = [0; 0];

end
```

C.1.6 Function SimulateRise

```
function [ V_V, I_A, T_s ] = SimulateRise( Vin_V, Vled_V,
   Cnode_F, L_H, i0_A, t0_s)
%SimulateRise Simulate the circuit as the voltage rises after
    switch turn
%off
%
%   Inputs
%   Vin_V - scalar - Input supply voltage [Volts]
%   Vled_V - scalar - LED string voltage [Volts]
%   Cnode_F - function - Incremental total capacitance on the
    drain node
%   [Volts to Farads]
%   L_H - scalar - Inductor inductance [Henries]
%   i0_A - scalar - Simulation starting inductor current [
   Amperes]
%   t0_s - scalar - Simulation starting time [seconds]



%
%   Outputs
%   V_V - vector - drain voltage [Volts]
%   I_A - vector - inductor current [Amperes]
%   T_s - vector - time [seconds]

tsteps = 1000;

VledP_V = Vin_V-Vled_V;
```

```
dv_V = Vin_V/tsteps;

V_V = (0:dv_V:Vin_V)';
I_A = zeros(tsteps+1,1);
T_s = zeros(tsteps+1,1);

iter = 1;

I_A(1) = i0_A;
T_s(1) = t0_s;

while ( iter <= tsteps)

    dt_s = dv_V/(I_A(iter) / Cnode_F(V_V(iter)));

    di_A = - dt_s * (V_V(iter) - VledP_V)/L_H;

    I_A(iter+1) = I_A(iter) + di_A;
    T_s(iter+1) = T_s(iter) + dt_s;
    iter = iter + 1;
end

end
```

C.2 Power and Loss Estimation

C.2.1 Function PowerCalcs

```
function [ PDiode_W, PSwitch_W, Pout_W ] = PowerCalcs(
   Iswitch_A, Idiode_A, Iind_A, T_s, DiodeDrop_V,
   DiodeCRes_Ohm, TranRon_Ohm, TranCRes_Ohm, Vled_V )
```

```
%POWERCALCS Power snapshot given circuit waveforms
%
%   Inputs
%   I_switch_A - matrix - switch current - first column is on
    -state
%   current, second column is capacitive current from Coss [
    Amperes]
%   I_diode_A - matrix - inductor current - first column is
    forward
%   current, second column is capacitive current from Cj [
    Amperes]
%   I_ind_A - matrix - inductor current - first column is
    inductive
%   current, second column is capacitive current from Cind [
    Amperes]
%   T_s - vector - time [seconds]
%   DiodeDrop_V - scalar - diode voltage drop [Volts]
%   DiodeCRes_Ohm - scalar - resistance in series with the
    diode capacitance [Ohms]
%   TranRon_Ohm - scalar - FET on resistance [Ohms]
%   TranCRes_Ohm - scalar - resistance in series with the FET
    capacitance [Ohms]
%   Vled_V - scalar - LED string voltage [Volts]
%
%   Outputs
%   PDiode_W - scalar - power loss in the diode
%   PSwitch_W - scalar - power loss in the transistor
%   Pout_W - scalar - power delivered to the led
```

```
DT_s=T_s(2:end) - T_s(1:end-1);

PswitchCap_W = ((Iswitch_A(2:end,2).^2)*DT_s*TranCRes_Ohm)/
    T_s(end);
PswitchCond_W = (((Iswitch_A(1:end-1,1)).^2+(Iswitch_A(2:end
    ,1)).*(Iswitch_A(1:end-1,1))'+(Iswitch_A(2:end,1)).^2)
    /3*DT_s*TranRon_Ohm)/T_s(end);
PDiodeDrop_W = ((Idiode_A(2:end,1))'+(Idiode_A(1:end-1,1))')*
    DT_s*DiodeDrop_V/2/T_s(end);
PDiodeCap_W = ((Iswitch_A(2:end,2).^2)*DT_s*DiodeCRes_Ohm)/
    T_s(end);

Pout_W = ((Iind_A(2:end,1))'+(Iind_A(1:end-1,1))')*DT_s*
    Vled_V/2/T_s(end)

PSwitch_W = PswitchCap_W + PswitchCond_W
PDiode_W = PDiodeDrop_W + PDiodeCap_W


end
```

C.2.2 EstLosses

```
function [ PDiode_W, PSwitch_W ] = EstLosses( Iswitch_A,
    Idiode_A, T_s, DiodeDrop_V, DiodeCRes_Ohm, TranRon_Ohm,
    TranCRes_Ohm )
%ESTLOSSES Find the losses in the devices given the current
    waveforms
%
%   Inputs
```

```
%   I_switch_A - matrix - switch current - first column is on
    -state
%   current, second column is capacitive current from Coss [
    Amperes]
%   I_diode_A - matrix - inductor current - first column is
    forward
%   current, second column is capacitive current from Cj [
    Amperes]
%   T_s - vector - time [seconds]
%   DiodeDrop_V - scalar - diode voltage drop [Volts]
%   DiodeCRes_Ohm - scalar - resistance in series with the
    diode capacitance [Ohms]
%   TranRon_Ohm - scalar - FET on resistance [Ohms]
%   TranCRes_Ohm - scalar - resistance in series with the FET
    capacitance [Ohms]
%
%   Outputs
%   PDiode_W - scalar - power loss in the diode
%   PSwitch_W - scalar - power loss in the transistor



DT_s=T_s(2:end) - T_s(1:end-1);


PswitchCap_W = ((Iswitch_A(2:end,2).^2)*DT_s*TranCRes_Ohm)/
    T_s(end);
PswitchCond_W = (((Iswitch_A(1:end-1,1)).^2+(Iswitch_A(2:end
    ,1)).*(Iswitch_A(1:end-1,1))'+(Iswitch_A(2:end,1)).^2)
    /3*DT_s*TranRon_Ohm)/T_s(end);
PDiodeDrop_W = ((Idiode_A(2:end,1))'+(Idiode_A(1:end-1,1))')*
```

```
    DT_s*DiodeDrop_V/2/T_s(end);
PDiodeCap_W = ((Iswitch_A(2:end,2).^2)*DT_s*DiodeCRes_Ohm)/
    T_s(end);

PSwitch_W = PswitchCap_W + PswitchCond_W
PDiode_W = PDiodeDrop_W + PDiodeCap_W


end
```

C.3 Inductor Sizing

C.3.1 Function FindInductor

```
function [ L_H, Ton_s, T_s ] = FindInductor( Vin_V, Vled_V,
    Power_W, Freq_Hz, Coss_F, Cj_F, Cind_F)
%FindInductor - This function gives you the inductance, diode
     scaling
%factor, and switch on-time necessary for the provided
    operating conditions
%
%   Inputs
%   Vin_V - scalar - Input supply voltage [Volts]
%   Vled_V - scalar - LED string voltage [Volts]
%   Power_W - scalar - LED power delivery goal [Watts]
%   Freq_Hz - scalar - Operating frequency goal [Hz]
%   Cj_F - function - Incremental diode capacitance versus
    reverse voltage
%   [Volts to Farads]
%   Coss_F - function - Incremental transistor output
    capacitance versus
```

```
%   drain source voltage [Volts to Farads]
%   Cind_F - scalar - Inductor capacitance to ground [Farads]
%
%   Output
%   L_H - scalar - required inductor value [Henries]
%   T_s - scalar - cycle time [seconds]
%   Ton_s - scalar - on time [seconds]

Cnode_F = @(V) ((Coss_F(V)+Cj_F(Vin_V-V)+Cind_F));

tRingScaled_s_rootH = RingTime( Vin_V, Vled_V, Cnode_F);

QSum_C = reimann(Cnode_F,0,Vin_V,100);

L_H=800e-9;

Tgoal_s=1/Freq_Hz;
Igoal_A=Power_W/Vled_V;
Qtot_C=Igoal_A*Tgoal_s;

while 1==1
    Ton_s=sqrt(Qtot_C/(Vin_V^2/(2*L_H*Vled_V)-Vin_V/(2*L_H)))
        ;
    Ipk_A=Ton_s*(Vin_V-Vled_V)/L_H;
    Toff_s=Ipk_A*L_H/Vled_V;
    Trise_s=QSum_C/Ipk_A;
    Tring_s=sqrt(L_H)*tRingScaled_s_rootH;
    T_s = Ton_s+Toff_s+Trise_s+Tring_s;
    scaleT = T_s/Tgoal_s;
    if (0.995 < scaleT && scaleT < 1.05)
```

```
        break;
    else
        L_H=L_H/scaleT;
    end
end


end
```

C.4 Miscellaneous

C.4.1 Function EPC1012_Coss

```
function [ Coss ] = EPC1012_Coss( Vds )
%This function shows the voltage/capacitance relationship for
    an EPC1012

Coss = 25.09e-12*exp(-((Vds+6.828)/4.976).^2) ...
     + 47.32e-12*exp(-((Vds-0.0558)/12.49).^2) ...
     + 138.4e-12*exp(-((Vds+199.8)/391.6).^2);
end
```

C.4.2 Function STPC10170C_Cj

```
function [ Cj ] = STPS10170C_Cj( Vr )
%This function shows the voltage/capacitance relationship for
    an C2D20120D

Cj =  476.4e-12./(1+Vr/0.7437).^0.5216+6.313e-12;


end
```

C.4.3 Function reimann

```
function [ s ] = reimann( myfunction, a, b, n )
%reimann Calculates a reimann sum
%   This function calculates the reimann sum of myfunction
    over the range
%   [a, b] using n midpoints.

delta = (b-a)/n;
x = (a+delta/2):delta:(b-delta/2);
s = delta .* sum(myfunction(x));

end
```

Appendix D

SPICE

D.1 SPICE Circuits

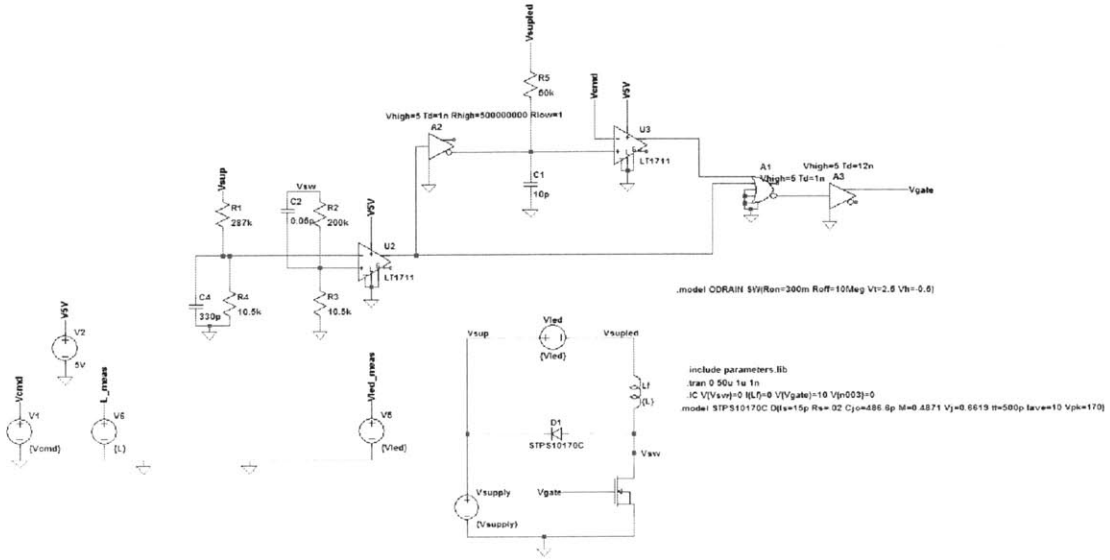


Figure D-1: Top level circuit for spice simulation

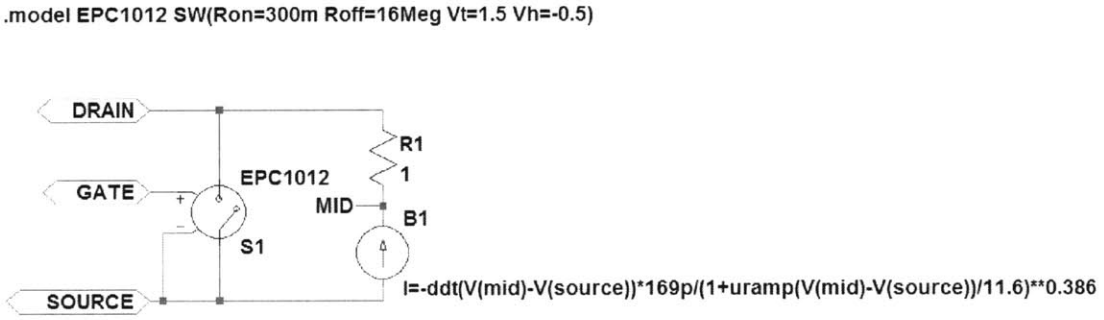


Figure D-2: STPS10170C transistor model

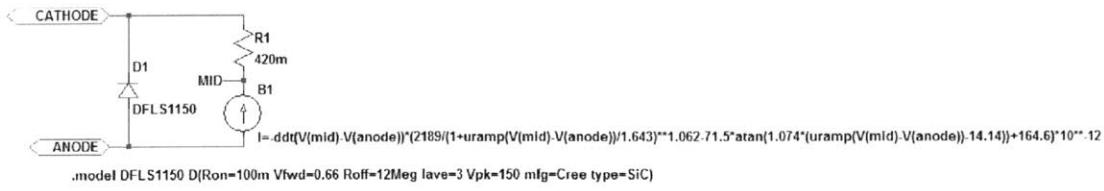


Figure D-3: EPC1012 diode model

D.2 SPICE Code

D.2.1 Parameters File

```
.params Ton=66n

.params Vsupply=100V
.params Vled=36V


*.params Vsupply=100V
*.params Vled=30V
*.params Cj=11n
*.params Mj=0.8
*.params Vj=1.177

.params L=1.678u
```

D.2.2 Measurement File

```
.MEASURE TRAN OUTPUTPWR AVG I(Vled)*V(Vled_meas)
.MEASURE TRAN INPUTPWR AVG -I(Vsupply)*V(Vsup)
.MEASURE TRAN EFFICIENCY PARAM OUTPUTPWR/INPUTPWR

.MEASURE TRAN SWITCHLOSS AVG V(Vsw)*Ix(X2:DRAIN)
.MEASURE TRAN DIODELOSS AVG (V(Vsup)-V(Vsw))*Ix(X1:CATHODE)

.MEASURE TRAN L AVG V(L_meas)
.MEASURE TRAN Ton AVG V(Ton_meas)
.MEASURE TRAN Vled AVG V(Vled_meas)
.MEASURE TRAN Vsupply AVG V(Vsup)
```

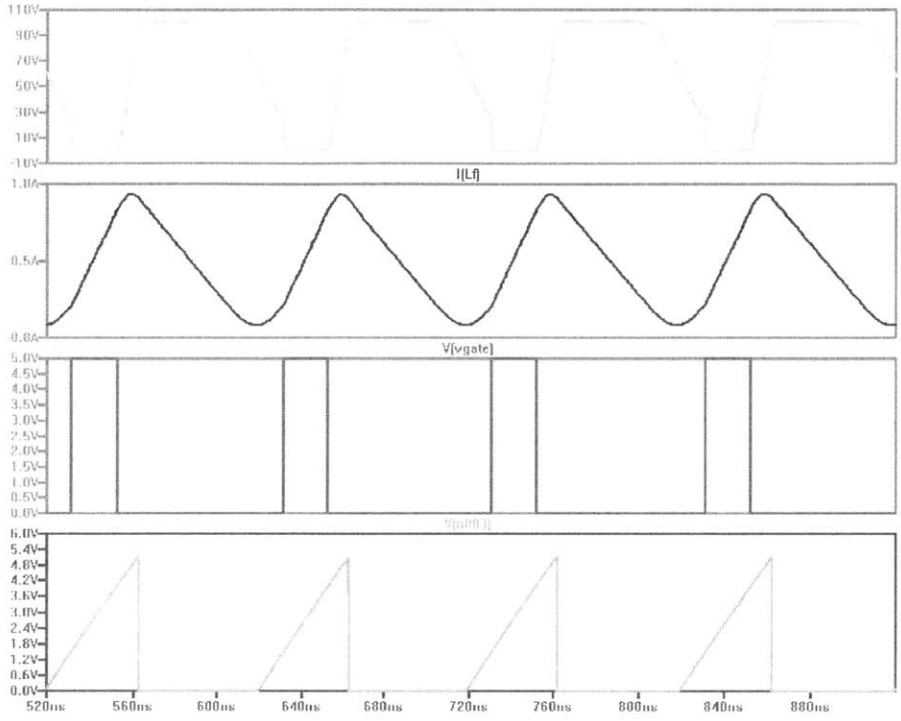


Figure D-4: Spice output waveforms including switch voltage, inductor Current, gate drive and integrator voltage

D.3 SPICE Output

Appendix E

Survey of existing LED Drivers in literature

Table E.1: A survey of the performance of various architectures in literature

Architecture	Power	Eff.	P.F.	Flicker	Inductors	Capacitors	FETs	LED Volt.
Boost PFC, Floating Buck[2]	11.593W	93.4%	0.97	Low	4.5mH, 3x20mH	47uF@200V	4	3x181-187
Flyback PFC, Inverted Buck[6]	31.2W	80.2%	0.925	Low	5mH, 570uH	68uF@70V	2	32V
Quadratic Buck-Boost[1]	70W	84.5%	0.98	Low	1.2mH, 7mH	80uF, 40uF	1	170V
Switched Resistive[12]	9W	80%	0.95	High	None	None	2	Unknown
Modified Boost[11]	18W	84.5%	0.963	High	10mH	None	1	360V
Flyback PFC[9]	13W	90%	0.95-0.99	High	1.1mH	1mF	1	27V
Inverter Buck[7]	5W	82-85%	0.92-0.098	High	5.5mH	1uF	1	Unknown
Flyback PFC, Bidirectional[20]	33.6W	87%	Unknown	Low	1.1mH, 80uH, 30uH	20uF	2	48V

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