Ultra Low-Power Wireless Sensor Demonstration System: Design of a Wireless Base Station

by

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Abstract

For the completion of the MIT Ultra Low-Power Wireless Sensor Project, a demonstration system was created in order to test and showcase the MIT designed integrated circuits. This thesis focuses on all of the analog front-end circuitry designed and built in order to communicate information over a wireless radio frequency channel.

An RF base station capable of receiving and demodulating a 2.5 Mbps GFSK modulated signal in the DECT band was built with existing commercially available components. The station digitizes the demodulated data signal and passes it along with a RSSI signal to a communications board. The communications board performs the remaining digital signal processing and clock recovery. A low-rate back channel was also necessary in order to communicate sensor control information from the base station to the sensor board. The base station's transmitter and sensor's receiver were built around an existing DECT chipset.

The demonstration system was completed by interfacing the base station with a notebook computer that interactively displayed sensor information as well as allowed sensor parameters to be altered in real time.

Thesis Supervisor: Charles G. Sodini, Ph.D.
Title: Professor of Electrical Engineering

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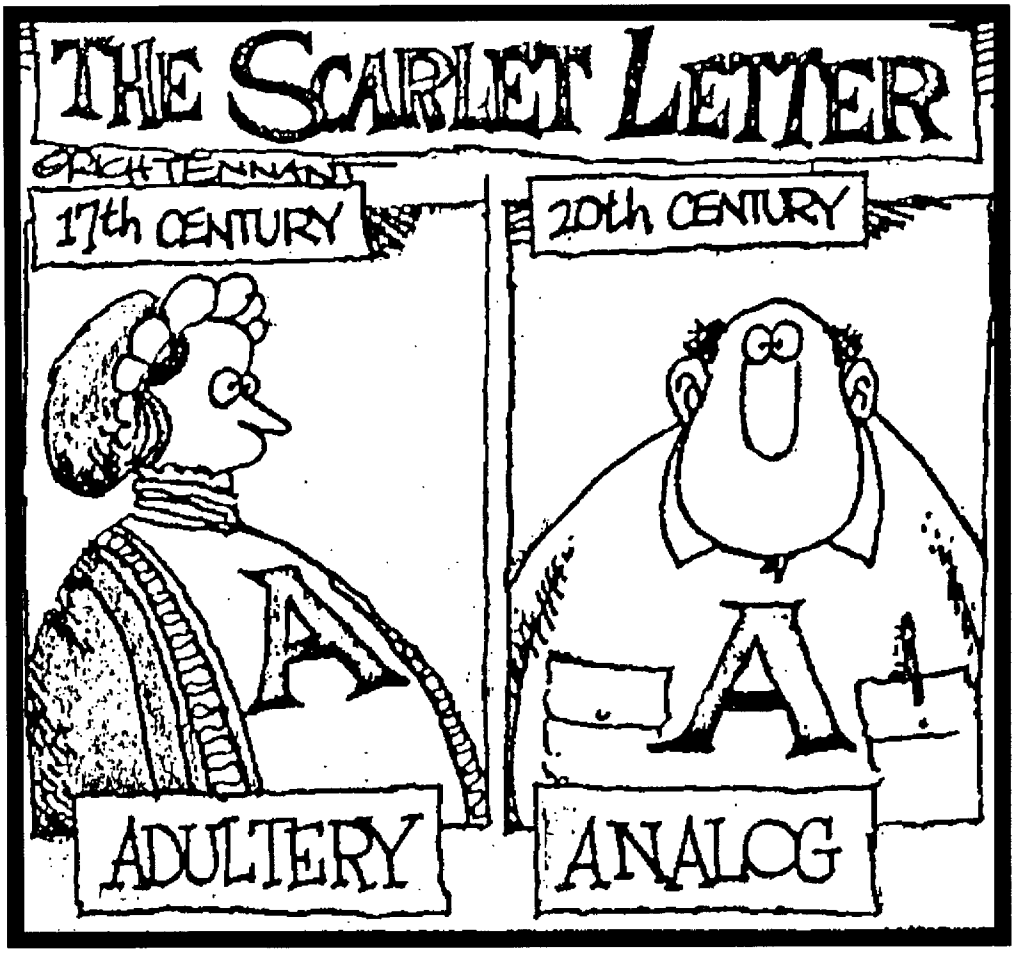
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Chapter 1

Introduction

Due to the recent emergence of portable battery–powered devices marketed for wireless communications, there has been a large amount of active research targeting the reduction of power dissipation, device size, and system cost. These goals inevitably require advancements in the levels of integration within these systems [1]. At the Massachusetts Institute of Technology, these design goals are being addressed by the Ultra Low–Power Wireless Sensor project. The wireless sensor project is a collaborative research effort whose goal is to investigate and develop new techniques aimed at low–power circuits. A wireless sensor system incorporating video was chosen as a design example because it presents an application very conducive for research. The system incorporates a variety of circuit elements: imager, data conversion, digital signal processing, RF transmission, and power supply conversion. Each element offers design hurdles not only individually but also when interfacing with one another. The choice of video transmission allows for varying data rates as well as resolutions; thus allowing another parameter that must be considered when optimizing designs.

Figure 1-1 presents a simplified block diagram of the sensor platform. For the image sensor, a 256 x 256 CMOS passive–pixel imager was developed [2]. In comparison with a CCD imager, the CMOS imager consumes less power and allows a random access architecture. For the data acquisition block, a low–power reconfigurable analog–to–digital converter was designed. The converter caters to a wide range of resolutions and speeds (6–16 bits, 1 kHz–10 MHz) while optimizing power dissipa-

tion by reconfiguring its topology and parameters [3]. A low power Direct Cosine Transform (DCT) compressor and Quadratic Residue Generator (QRG) encryption chip were developed to perform necessary DSP functions [4]. The data stream is then formatted for transmission in an FPGA and passed to a PLL based RF transmitter. At the heart of the transmitter is a high data rate fractional–N synthesizer that incorporates digital compensation to overcome the conflicting requirements of high data rate and low noise [5]. The synthesizer controls the steering line of a low power 1.8 GHz voltage–controlled oscillator [6]; the oscillator in turn completes a feedback loop by feeding a frequency signal back to the synthesizer. The two chips, along with a power amplifier, complete the RF transmission engine. The final circuitry designed for the project were high efficiency, low–voltage DC–DC converters that provide the differing power supplies lines to all the chips [7].

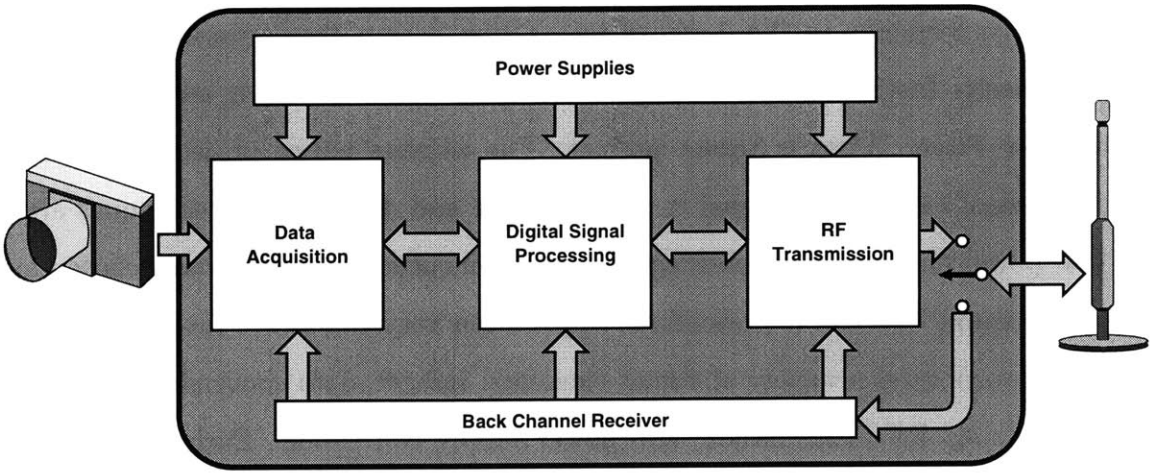


Figure 1-1: Wireless sensor platform.

While each block can be tested and verified individually, a demonstration of the complete system's capabilities necessitates the development of a base station. Since a sensor is allowed to communicate only with the station via an RF channel, the base station provides the central point of computation for the system. The base station receives and processes each sensor's data and transmits the control information needed to direct the sensor's future actions. Consequently, a low data rate receiver on the sensor side is also necessary.

1.1 Base Station Receiver Specifications

A block diagram of the base station is shown in Fig. 1-2. The base station employs time–division duplexing of a channel in the DECT frequency band (1.88–1.90 GHz); the carrier is nominally at 1.890 GHz. This allows both the uplink and downlink paths to occupy the same channel. The sensor–to–base link is a 2.5 Mbps Gaussian Frequency Shift Keyed (GFSK) signal occupying a 3.325 MHz channel [5, 8]. The base station demodulates the signal and then digitizes it. The receiver is designed to at least meet the DECT standard of -82 dBm of receiver sensitivity with a bit error rate of 10^{-3} [9]. The base station board presents the digitized data and a *received signal strength indicator* (RSSI) signal to a communications board. The communications board handles all of the digital signal processing and communications protocol.

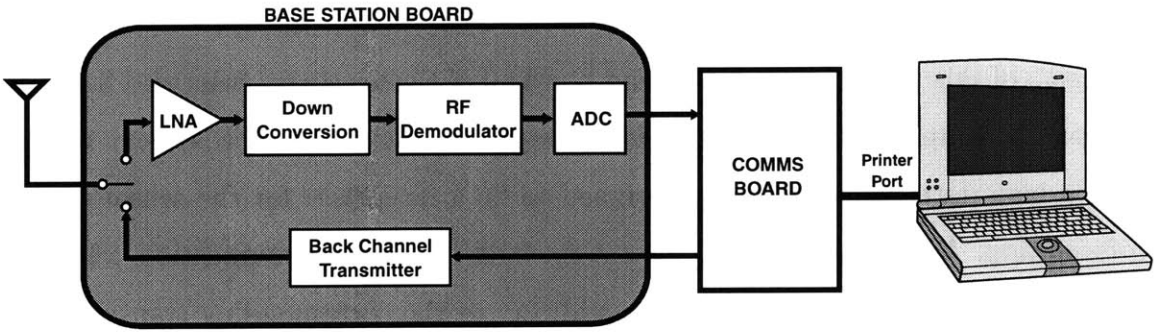


Figure 1-2: Base station block diagram.

1.2 Back Channel Specifications

The back channel is used to transfer the majority of decision–making processes away from the sensor and to the base station. This allows the sensor's power consumption to be further optimized. The command packet contains data for the following instructions:

- What data the sensor should return in response to the command.
- What resolution the next image should be.

- What type of image compression should be used.
- What seed to feed the QRG encryption chip.
- How many subsequent command packets the sensor is allowed to ignore (i.e. how long to power down).

While occupying the same frequency band as the sensor–to–base link, the data rate requirements on the back channel are more relaxed. A minimum burst rate of 100 kbps is desired. However, to reduce the on–time of the sensor's receiver and thus lower power consumption, the base–to–camera burst rate should be as high as possible without further increasing the system's complexity.

1.3 Project Approach

The goal of this project is to design and build all of the necessary front end hardware needed to complete the demonstration system. In particular, the system requires that a high data rate receiver be designed to be a receptacle for the sensor's image information. Also, in order to implement the back channel communication, a low rate receiver is developed for the sensor in addition to the corresponding transmitter on the base station.

The project begins with a review of the various schemes currently employed in RF transceivers. The benefits and drawbacks of each architecture are studied and scrutinized to see which would be the most viable given the constraints of time and ease of implementation. It is decided that the base station receiver would demodulate the signal on the board in the analog domain, as opposed to digitizing the frequency modulated signal and then performing demodulation in a DSP unit or in software. The chosen architecture is a dual–IF receiver utilizing quadrature detection.

To meet the stated objectives, it is decided that all of the circuitry will be composed entirely of existing, commercially available components. This decision was based upon time issues and ease of design. The back channel's target frequency band and data rate allows for the integration of readily available DECT chipsets. However,

for the base station receiver, the decision to use *off-the-shelf* components forces some constraints on the design process. Key elements, such as SAW filters, are only commercially available in set bandwidths at certain center frequencies. Thus compromises are made between an optimum solution and a viable one.

Simulations are performed on system metrics such as noise figure and intermodulation with receiver chains consisting of readily accessible parts. Once a design is deemed satisfactory, an RF printed circuit board is laid out and constructed. The base station board consists of a high rate receiver and a back channel transmitter. The second board built contains the MIT designed low–power transmitter [10] as well as the back channel receiver integrated onto it. Once populated, the boards are tested to verify functionality and performance.

1.4 Thesis Overview

The remaining chapters of this thesis present further analysis and details of the project. For readers unfamiliar with introductory RF concepts and terminologies, Appendix A provides a brief review of concepts and definitions used through the remainder of this thesis. Chapter 2 presents preliminary research and analysis that lead to the design work in the chapters following it. Chapters 3 and 4 document the design of the base station receiver and back channel circuitry, respectively. Measured results for each board are presented in Chapter 5. Chapter 6 summarizes the project and suggests areas of future work.

Appendices B and C provide complete schematics, board layout details, and a bill of materials for both the base station and sensor board. Appendix D and E provide ancillary information regarding the programming of both the frequency synthesizer and AD6411 DECT chipset; material in these sections are reprinted from each components data sheets.

Chapter 2

Receiver Analysis

This chapter presents an analysis of the receiver architectures considered for the base station. Each scheme is presented and compared to determine the most appropriate choice for this project. This is followed by a discussion addressing the different types of demodulators available. The chapter concludes with details explaining why a dual–IF conversion receiver with quadrature detection was chosen as the the architecture to be implemented. However, the chapter begins with a presentation of the GFSK modulation employed in the wireless sensors.

2.1 Gaussian Frequency Shift Keying

The PLL–based transmitter in the wireless sensor employs Gaussian Frequency Shift Keying (GFSK) as a frequency modulation scheme. This modulation method is similar to Gaussian Minimum Shift Keying (GMSK) or more generally Minimum Shift Keying (MSK); the difference in definitions is due to differing modulation index requirements. (Modulation index is defined as the ratio of the frequency deviation of the modulated signal to the frequency of the modulating signal.) While MSK requires by definition a modulation index of precisely 0.5, GFSK allows a tolerance. For this project, the modulation index was designed to be 0.5 ± 0.05.

Gaussian Frequency Shift Keying utilizes a premodulation filter to manipulate the output spectrum. As seen in Figure 2-1, the digital baseband signal is passed through

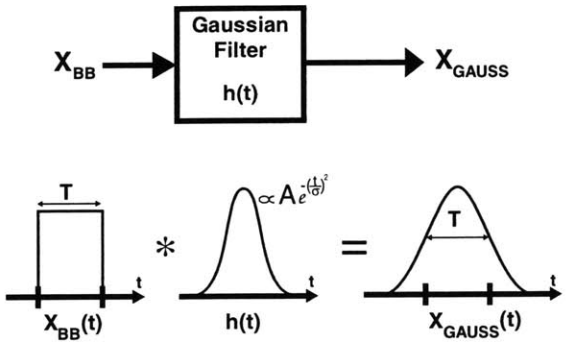


Figure 2-1: Effect of Gaussian filter on bit pulse in the time domain. By convolving the bit stream with a Gaussian filter, the resulting pulse stream can be made less abrupt.

a Gaussian transmit filter in order to remove the hard edges; this premodulated signal is then used to feed the modulator. As a visual example, GMSK and MSK will be compared (we can easily extend the example to GFSK since it was previously noted that GMSK and GFSK are similar in terms of functionality). Figure 2-2 shows that by convolving the bit stream with a filter, phase transitions in the frequency modulated signal are smoothened and the resulting RF output spectrum is much more spectrally efficient compared to traditional MSK. The power in the sidelobes is decreased considerably due to the prefiltering. As the Gaussian filter becomes

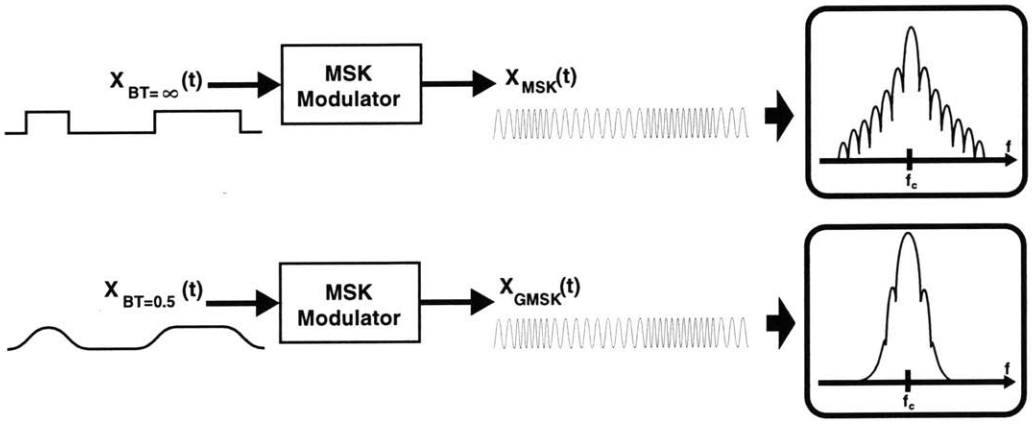


Figure 2-2: Comparison of GMSK to unfiltered MSK. The upper figure shows a traditional MSK system (BT$\rightarrow \infty$) and its corresponding output spectrum. In comparison, the GMSK system (BT$\rightarrow$ 0.5) in the lower figure shows a much more spectrally efficient output.

wider in the time domain, the output spectrum decays faster. However, this channel narrowing doesn't come without consequences. As the channel bandwidth decreases, the modulating pulse widens in the time domain and thus causes an increase in intersymbol interference (ISI). [For information on ISI, please refer to Appendix A.3.] Hence a compromise needs to be found between spectral efficiency and intersymbol interference.

In GMSK and GFSK signaling, modulation is parameterized by the normalized 3 dB–down bandwidth of the Gaussian premodulation filter, BT ($1/T$ = data rate). As BT is lowered, the transmit filter's impulse response becomes wider and will thus increase spectral efficiency at the output of the modulator. However, as explained above, if BT is decreased too much, ISI becomes a limiting factor. Table 2.1 presents the occupied bandwidth of a GMSK modulated channel normalized to the date rate given a percentage of total signal power and value of BT [8].

The low power transmitter designed for this project adhered to the DECT standard specification as a benchmark and accordingly employs a BT of 0.5. Given a transmit data rate of 2.5 Mbps and a BT of 0.5, Table 2.1 reveals a channel bandwidth of 3.325 MHz. This information is transmitted within the DECT frequency band; the nominal carrier is near the fourth DECT channel at a carrier frequency of 1.890000 GHz [9].

	Percentage of Signal Power			
BT	90.0%	99.0%	99.9%	99.99%
0.20	0.52	0.79	0.99	1.22
0.25	0.57	0.86	1.09	1.37
0.50	0.69	1.04	1.33	2.08
∞ (MKS)	0.78	1.20	2.76	6.00

Table 2.1: Normalized Channel Bandwidth Containing a Percentage of Signal Power versus BT. For a 2.5 Mbps signal with a BT of 0.5, 99.9% of the signal power is within a channel of bandwidth: $(1.33) \cdot (2.5\text{Mbps}) = 3.325$ MHz.

2.2 Receiver Architectures

The first step in the design process requires choosing an appropriate receiver architecture for the base station. Developing new architectures has even been the focus of much research recently [11, 12]. While various schemes were considered for this project, the following three architectures were seen as viable solutions: single–IF conversion, dual–IF conversion, and direct conversion.

2.2.1 Single–IF Conversion

Due to bandwidth limitations and unattainable filtering requirements at high carrier frequencies, wireless receivers translate the interested channel to a much lower frequency. Adequate filtering and demodulation can then be readily implemented. Figure 2-3 shows the block diagram of a single–IF conversion receiver that utilizes frequency translation. The RF front end performs the translation by using a mixer or analog multiplier. The fundamental concept of frequency mixing is shown by the following relationship:

$$(A\cos\omega_{RF}t)\cdot(B\cos\omega_{LO}t) = \frac{AB}{2}\left[\cos(\omega_{RF}-\omega_{LO})t + \cos(\omega_{RF}+\omega_{LO})t\right] \qquad (2.1)$$

where ω_{LO} is the frequency of the local oscillator. By low pass filtering Eq. (2.1), the later term is removed and the output is the desired channel moved to the new frequency, $\omega_{RF}-\omega_{LO}$, called the *intermediate frequency* (IF).

While the single–IF conversion receiver is a simple solution, it has one major flaw. After discussing frequency translation and IF, the topic of where to set the

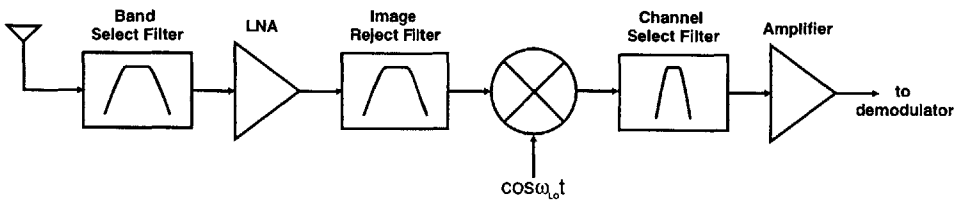


Figure 2-3: Block diagram of a single–IF conversion receiver.

intermediate frequency reveals an unfortunate trade off between channel selectivity and image rejection.

Image Issue

When choosing the IF for a system, the image signal that will also be translated to the IF must be considered. To understand what the image is, we refer back to Eq. (2.1). Since analog multiplication doesn't discriminate polarity differences, $cos(\omega_{RF} - \omega_{LO})t$ is equivalent to $cos(\omega_{LO} - \omega_{RF})t$. In other words, frequency bands located symmetrically about ω_{LO} will be translated to the same IF frequency. For example, if $f_{RF} = 200$ MHz and $f_{LO} = 150$ MHz, then not only will the desired signal band get downconverted to 50 MHz, but so will any RF content at 100 MHz. The equivalent band at 100 MHz is referred to as the *image* of the desired signal. In practical applications, the designer has no control of the power levels at the image frequency since it will generally be outside the frequency band controlled by a given standard. Thus it is imperative that the system utilize sufficient image rejection techniques.

Returning to the question of where to set the IF, we see the basic trade off in Figure 2-4. Since the image is located at twice the IF frequency from the channel of interest, good rejection by way of an image reject filter requires the selection of a high IF. This situation is shown in the upper example. A high IF, however, results in a much higher Q requirement on the channel select filter. Conversely, a low IF facilitates rejection of local interferers, but the image band will experience less suppression. Since filter Q and loss are generally conflicting parameters, trying to place a sharper image–reject filter in the receive chain will result in greater signal loss and consequently increase the system noise figure. In order to decouple image rejection and channel selectivity, a dual–IF conversion architecture that takes advantage of an additional stage of mixing is used.

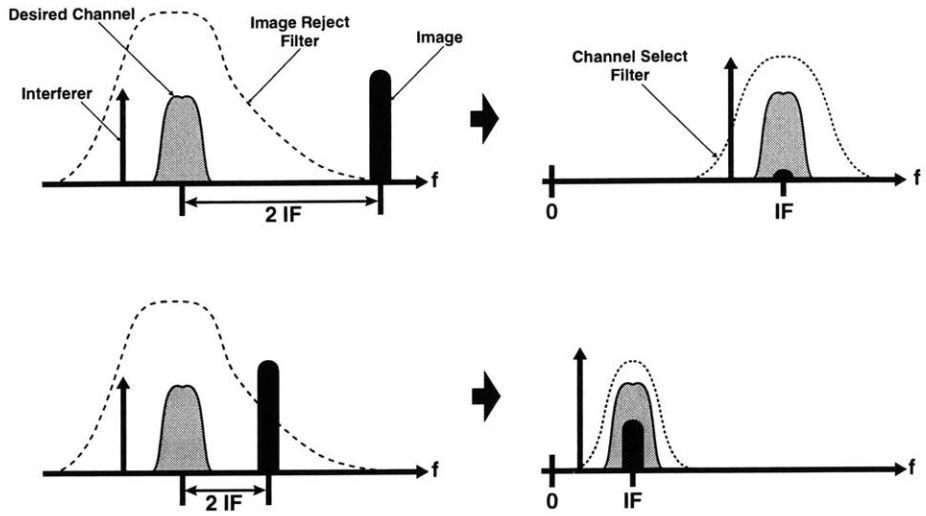


Figure 2-4: Image rejection versus channel selectivity. The upper figure is characteristic of a high IF; the lower figure shows the effects of a low IF [13].

2.2.2 Dual–IF Conversion

As seen in Figure 2-5, a dual–IF conversion receiver is essentially identical to a single–IF receiver with an additional mixing stage. This architecture allows the designer to resolve the image rejection versus channel selectivity trade off by addressing each goal independently. Image rejection is achieved by setting the first IF high enough to allow low–loss, modest Q filters to be placed in the receiver front end. Thus adequate image rejection is performed with minimal noise figure degradation. Channel filtering is actually performed at each IF. At the first IF, usually a *surface acoustic wave* (SAW) filter is used to provide filtering. At the second IF, the lower frequency permits the use of either active or passive filters composed of discrete inductors and capacitors. By filtering in stages, the Q requirement on any single filter is lowered from that

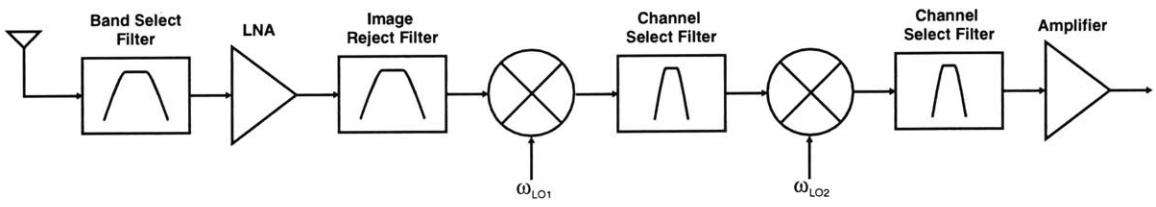


Figure 2-5: Block diagram of a dual–IF conversion receiver.

required in a single–IF receiver.

Until recently, the described benefits of a dual–IF conversion had made it the most ubiquitous solution to RF reception. However with the higher levels of integration and lowering power requirements, the drawbacks of dual–IF have caused designers to seek alternatives. Due to the extra mixer stage as well as periphery amplifiers and filters, a dual–IF architecture does not lend itself well to optimum power consumption. From an integration viewpoint, system complexity is rather high. Besides the sheer number of parts, certain crucial components such as ceramic and SAW filters cannot be integrated into a silicon process. (Ceramic and SAW filters are both mechanical devices that rely on piezoelectric materials; unfortunately, common IC silicon neither exhibits any piezoelectric activity nor is compatible with materials that are used to make the filters.) While there have been advancements in on–chip matching networks and integrated transformers [14, 15], is has not been enough to consider a dual–conversion architecture for a fully integrated solution.

2.2.3 Direct Conversion

Instead of mixing the RF spectrum to an intermediate frequency, a direct conversion or zero–IF receiver translates the spectrum directly down to baseband. However, simply mixing an FM signal with an LO at the carrier frequency is not sufficient for down conversion, As seen in Figure 2-6, since the frequency content in the channel's two halves are not the same, mixing results in signal corruption because both halves get placed on top of each other in the baseband. In order to recover the signal, quadrature downconversion as shown in Figure 2-7 is used. By multiplying the

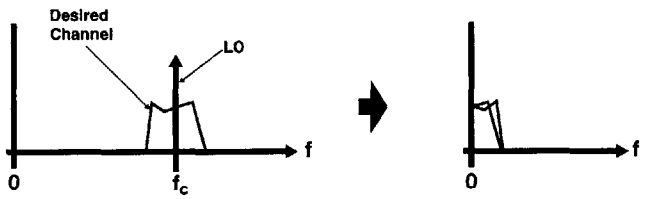


Figure 2-6: Downconversion in a zero–IF receiver using a single LO.

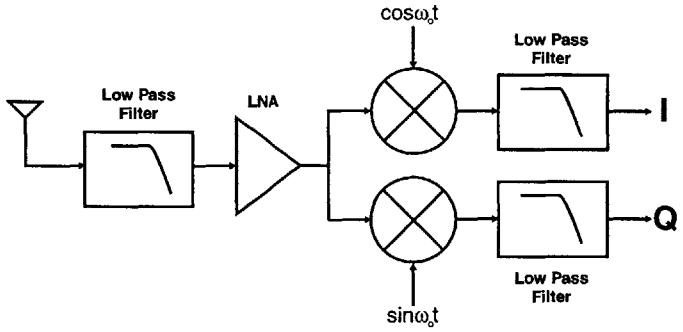


Figure 2-7: Direct conversion receiver employing quadrature downconversion.

channel with both a sine and cosine signal, information is preserved and can be recovered from the quadrature I and Q signals.

With the spectrum being mixed down to DC, there is no image problem and thus there is no need for image reject filters or extra mixing steps. Also, expensive external components such as SAW filters are replaced with integrated low–pass filters. Due to the benefits of a low part counts, small size, and high integration, direct conversion techniques have been increasingly employed in low power applications such as pagers.

However, direct conversion receivers suffer from a number of issues that are not applicable to the previous two receiver examples. The most serious drawback is due to self–mixing and consequent parasitic DC offsets. Since the spectrum resides at DC, parasitic offset voltages directly corrupt the channel. While systematic offset voltages can be easily removed, offsets due to self–mixing are time varying and present a much more challenging task. Self–mixing within downconverters occurs because of the finite isolation between the local oscillator and signal path. Any appreciable LO leakage signal that gets to the input of a mixer will mix with the LO and produce an offset voltage that interferes with the downconverted channel. The same deterioration will be caused by a strong interferer leaking from the signal path to the mixer's LO input. Due to the large amount of gain concentrated in the front end, the parasitic offset can be large enough to saturate following circuitry and thus further hinder any hope of recovering the signal.

Other issues to designing a direct conversion receiver include I/Q mismatch, even–

order distortion, and flicker noise. I/Q mismatch stems from errors in the phase shift and gain matching needed to perform quadrature downconversion. Even–order distortion is due to low frequency components being generated when two closely spaced interferers pass through a second–order system. Since the desired channel resides at baseband, the second–order terms will directly corrupt the signal. Flicker noise is appreciable at low frequencies in circuits fabricated with MOSFETs, thus requiring high front end gain in order to amplify the desired signal. This high gain in turn exacerbates self–mixing.

2.3 Demodulation

Once the choice of receiver architecture is set, the next crucial step is to decide what type of demodulation scheme will be employed. There are many ways to recover information from an FM signal. Taking into account the frequency modulation used in this project and the sought after receiver performance, the following three methods were considered: digitizing at the second IF and demodulating in the digital domain; using a phase–locked loop detector; using a quadrature detector.

2.3.1 Digitizing the IF

As digital speeds continue to increase and digital signal processing becomes ever efficient, more and more of the receive path has been encroached upon by the digital domain. One approach has been to digitize the analog signal at the first IF and then perform the mixing and filtering via DSP. The difficulty in this approach is the high performance requirements of the analog–to–digital converters needed at high IF values. At such sample rates, the ADCs consume a lot of power. Also, since the signal levels are on the order of a few hundred microvolts at the first IF, the ADC must have very small noise specifications. Combined with high linearity and dynamic range, it is difficult to design an ADC capable of meeting all of the specifications without consuming a large amount of power. These reasons tend to make this approach prohibitive in portable systems. An alternative is to use sub–sampling techniques

to relax the bandwidth requirements. However, this approach suffers greatly from noise aliasing. It has been found that sub–sampling by a factor of (j) will cause the downconverted noise power to increase by a factor of $2j$, and the effects of the sampling clock's phase noise will be amplified by j^2 [16].

Another, less aggressive approach applicable to a dual conversion system is to digitize at the second IF. The demodulation is then carried out in the digital domain. The key issue with this approach is that an automatic gain–control (AGC) loop must be designed in order to maintain optimum signal strength into the ADC. Otherwise, either saturation will occur in response to changing power levels or the sensitivity of the system will be very poor. Both conditions place greater requirements on the ADC's dynamic range.

2.3.2 Phase–Locked Loop

A common technique to recover data from a frequency modulated signal in the analog domain is to incorporate a phase–locked loop (PLL). Figure 2-8 shows a block diagram of a PLL based demodulator. The FM signal is driven into a phase/frequency detector (PFD) which compares the FM signal with the VCO signal. The PFD responds to the differences in the two signals by directing the charge pump to produce a series of control pulses. The pulses are then filtered and smoothened by the loop filter and then applied to the steering line of the VCO. The entire feedback system forces the VCO output to match the incoming FM signal; the demodulated signal is recovered by looking at the steering line voltage needed to force the phase/frequency lock.

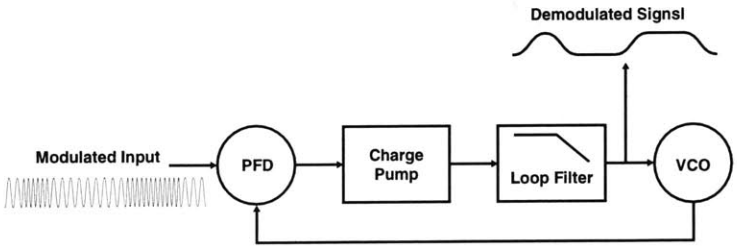


Figure 2-8: Phase–locked loop based FM demodulator

As with any feedback system, stability is an important issue with all PLLs. While the PLL does provide the benefits of locking onto a frequency and resisting some drift, practical issues such as startup transients, large drifts, and large initial frequency deviations can cause the PLL to either not lock or lock to the wrong frequency. In a time duplexed system such as the one used in this project, the PLL would not be continually locked; this requires either a large time set aside to ensure locking or more commonly a precharge interval to precondition the PLL to the intended in coming carrier.

2.3.3 Quadrature Detection

A popular alternative to the coherent PLL–based demodulator is the quadrature (phase–shift) detector. Quadrature detection is easily implemented in integrated circuits at low costs, making it a common solution on many commercially available chipsets. As diagrammed in Figure 2-9, the system uses a frequency dependent phase shift network to produce a phase shifted replica of the input signal. Therefore, if we allow the input to be represented by $A\cos(\omega_{BB}t + \theta_0)$, the output of the phase shift network is,

$$B\cos\left(\omega_{BB}t + \theta_0 + \phi[\omega_{BB}]\right) \tag{2.2}$$

where $\phi[\omega_{BB}]$ indicates that the added phase shift is solely a function of the incoming frequency, ω_{BB}. By multiplying the two signals and ignoring the constants, we get

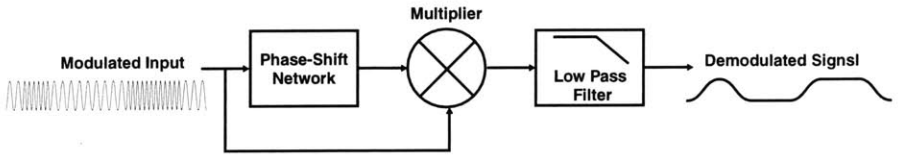


Figure 2-9: Quadrature detection block diagram.

the following output terms,

$$\cos\left\{2(\omega_{BB}t + \theta_0) + \phi[\omega_{BB}]\right\} + \cos\left\{\phi[\omega_{BB}]\right\} \tag{2.3}$$

By filtering out the high frequency term with a low pass filter, only the later term in Eq. (2.3) remains. The system output is thus a function of the incoming frequency and the phase shift network. By letting the phase shift network have the phase characteristics presented in Figure 2-10, the output will be zero at the carrier frequency and swing negative or positive in response to any frequency variation. This phase shift characteristic is easily created by an RLC tank circuit.

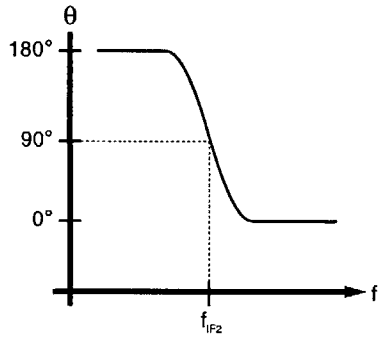


Figure 2-10: Desired phase shift network transfer characteristic.

2.4 Choice of Receiver Architecture

Even with all of the challenges inherent to direct conversion architectures, it is still a much sought after solution to wireless reception because of its substantial gain in power consumption and integration. However for this project, a dual–IF architecture is preferable. Since the base station's key objective is high performance, as opposed to low cost, size, or power consumption, the benefits of direct conversion are lost. Similarly, any benefits in size or power dissipation gained by employing a single–IF receiver are irrelevant when compared to the performance gains attributed to a dual conversion architecture.

For demodulation, the quadrature detector was chosen over a PLL implementation. Digitizing–IF was considered too complex given the time constraints of this project. The factors behind choosing quadrature detection over the PLL solution were simplicity for near equal performance. As can be seen by the plot in Figure 2-11, for a DECT standard BER requirement of 10^{-3}, non–coherent detection required an E_b/N_0 of only 1.5 dB higher than that required by coherent FSK detection [17, 18]. The lower complexity may thus be justified.

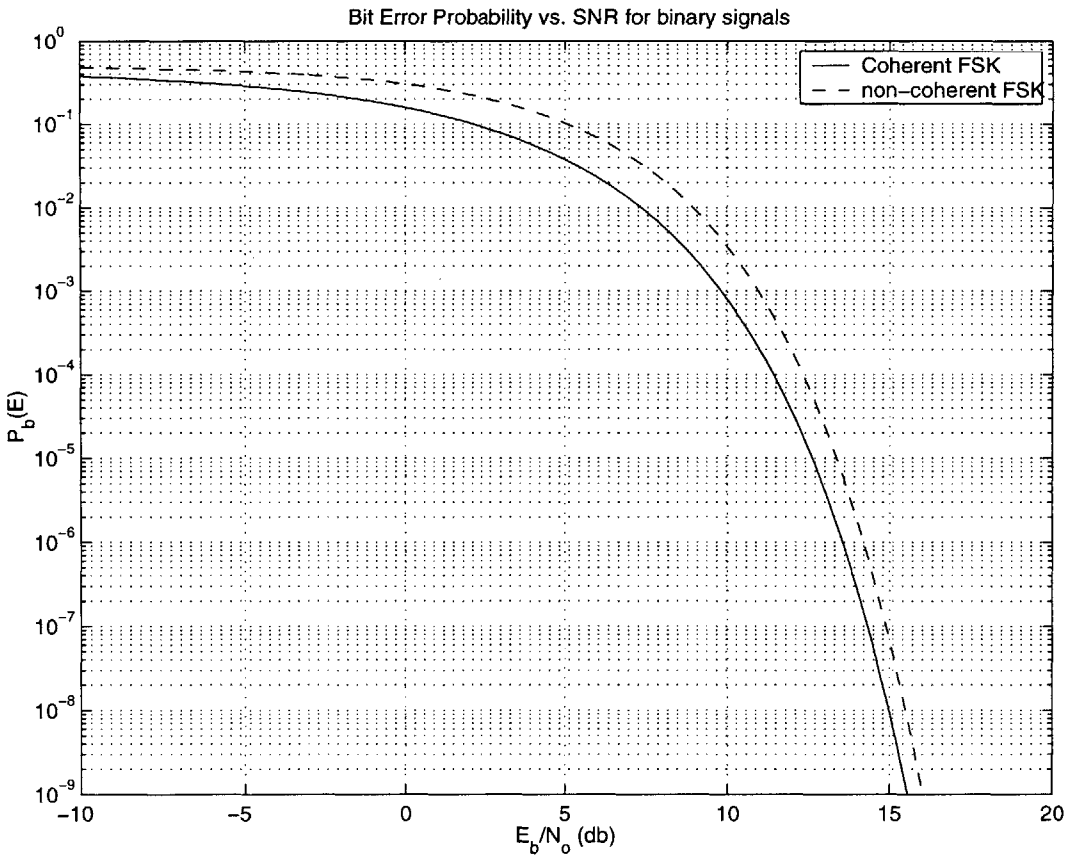


Figure 2-11: Bit error probability versus SNR for coherent and non–coherent FSK [19].

Chapter 3

Base Station Receiver Design

In the previous chapter, it was decided that the base station receiver will be a dual–IF architecture utilizing a quadrature detector for demodulation. This chapter presents details regarding the design and implementation of the receiver. The process begins with an exercise in frequency planning and builds toward a hardware solution. Along the way, details will be provided on issues challenging an optimum design. Finally, the design process gives way to the design of an RF printed circuit board.

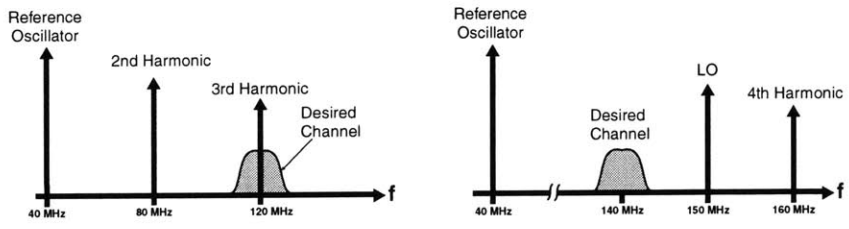
3.1 Frequency Planning

A most crucial first step in the design of a wireless system is the frequency planning. Based on research compiled on existing standards, great care has been taken in order to minimize the effects of noise, images, and other spurious signals. As an example, a common frequency plan used in the DECT standard is presented.

3.1.1 Example: DECT

DECT has allocated 10 channels in the 1.88 – 1.90 GHz band. Each channel's center frequency is spaced exactly 1.728 MHz from the next, at frequencies of 1.881792 GHz, 1.883520 GHz, ... , 1.897344 GHz [9]. The carrier frequencies were set as such because each is an integer multiple of a DECT channel's required bandwidth; thus

the frequency band is fully occupied. The usual first IF in a DECT system is at 110.592 MHz. Since this IF value is also an integer multiple of the channel spacing, all of the LO frequencies needed for channel selection are also multiples of 1.728 MHz and are easily obtained with a simple PLL synthesizer incorporating digital dividers. By setting the second IF to either 20.736 MHz or 13.824 MHz (again both multiples of 1.728 MHz), then the second LO signal can be obtained from the same synthesizer without additional reference sources or prescalars. Such frequency planning not only facilitates a low power solution by minimizing hardware, it also helps prevent spurious signals due to harmonics from falling directly into a band of interest. For example, digital signals such as a synthesizer's reference oscillator or an analog–to–digital converter's sampling clock are commonly the largest signals on a board; it is not uncommon for high–order harmonics of these digital signals to be larger than the desired signal. If these signals aren't accounted for, their harmonics can fall directly into a desired channel, or the harmonics could mix with other signals and produce the same destructive effect (Fig. 3-1). In DECT the frequency planning allows a 10.369 MHz crystal to be divided down to provide the necessary 1.728 MHz reference frequency without it's harmonics falling into either IF.



(a) (b)

Figure 3-1: Signal degradation due to spurious signals. Figure (a) shows an example of a reference oscillator harmonic falling into the channel of interest. Figure (b) shows an example of a 160 MHz harmonic that becomes an image signal and will be translated along with the channel to the intermediate frequency.

3.1.2 Implementing the DECT Model

For this project, the frequency planning of the base station receiver had to make many concessions. Since from the onset this project required the use of existing commercially available components, the frequency management was greatly influenced by what products had already been manufactured. Generally, when a standard is being developed, the availability of components is secondary; once the standard is adopted, companies will design new components in response. However, with custom integrated chip design beyond the scope of this project, the first step became finding which stages of the receiver chain presented the least degree of freedom. Since the frequency band used in this project is normally allocated for DECT, it was desirable to adopt the frequency planning commonly used by DECT. Unfortunately this approach is met by two key barriers.

Limited SAW Filter Availability

One of the most crucial components in the system is the SAW filter located at the first IF. This filter provides the first stage of channel filtering in the signal path. It is critical for suppression of out–of–band signals because the SAW filter is commonly followed by the second mixer in a dual–IF system. Unlike the first mixer stage where linearity is of lesser importance, corruption due to intermodulation is more likely at the second IF because signal levels are greater.

Many companies have produced SAW filters at 110.592 MHz targeted for a DECT channel bandwidth of 1.728 MHz. However, this bandwidth is too small for this project. A bandwidth of at least 3.325 MHz is required. After an exhaustive search, no suitable SAW filters were found at any of the common DECT IF frequencies. A custom made SAW filter would be needed if the DECT frequency scheme was to be used.

Reference Spurs

By trying to adopt the DECT frequency plan, the issue of reference spurs presents a problem. Reference spurs in the LO signal are caused by the reference frequency modulating the VCO. This undesired modulation is due to the non-ideal characteristics of the charge pump used in a PLL based synthesizer. Due to finite switching times and mismatched charge injection, as well as the addition of noise, the actual spectral output of the VCO will appear as in Figure 3-2. Since the magnitude of the spurs is found to be inversely proportional to the reference frequency [13], using a reference frequency of 1.728 MHz will result in unacceptably large spurs close to the channel edges.

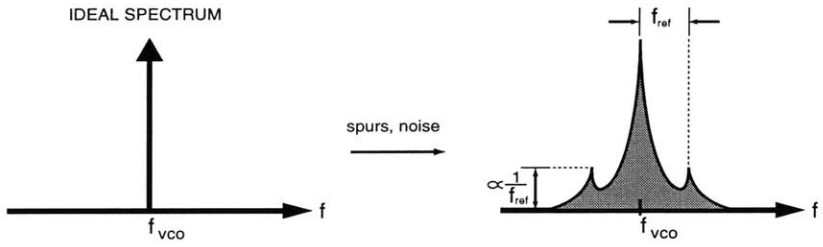


Figure 3-2: Effects of reference spurs and phase noise on the spectral output of a VCO.

3.1.3 Approach to Frequency Planning

Even if a suitable SAW was obtained, the issue of reference spurs would still present a problem. Therefore a new solution is needed. Since finding a suitable SAW filter is so crucial and limited in assortment, it is given the highest priority in the frequency planning. Thus the first IF is pinned down by component availability and not performance issues. Once the first IF is set, a suitable frequency synthesizer and reference frequency capable of producing the first LO are sought. However, while searching for these components, it is done with an eye on what second IF values could be supported with the same circuitry. Another condition affecting the choice of second IF is the filtering available. A low–loss, high Q integrated filter is desired over a passive, discrete filter that would require tuning.

After compiling data sheets on numerous components, various combinations were evaluated in terms of their system metrics. In particular, system noise figures and third–order input intercept points were calculated in order to determine the system's sensitivity and spurious–free dynamic range (Appendix A). Addressing SAW filters first, SAWTEK was the only manufacturer that provided filters of varying bandwidths; one series is centered at 140 MHz while the other is at 70 MHz. A 140 MHz SAW filter was selected because the higher IF allowed greater image suppression. With the first IF set, a synthesizer was found that is able to support both the LO needed to mix the RF channel down to 140 MHz as well as to allow the second IF to be 21.25 MHz. This choice of a second IF was selected because bandpass filters centered at 21.4 MHz are readily available.

After many iterations, the frequency setup shown in Figures 3-3 & 3-4 was developed. Although the solution is less than optimum, it is adequate for the performance

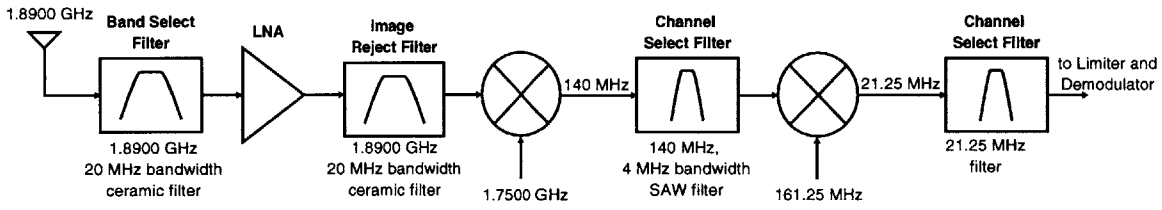


Figure 3-3: System block diagram highlighting frequency planning.

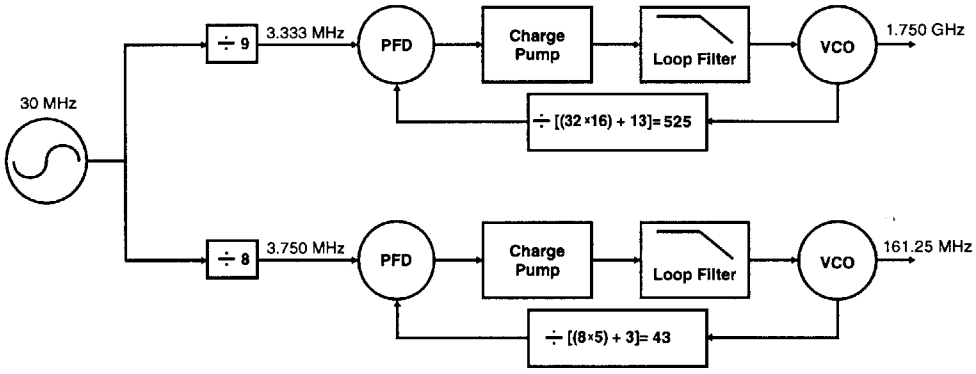


Figure 3-4: Block diagram of dual frequency synthesizer.

specifications desired. Based on the components available for each block (Appendix B), the system exhibits a system noise figure of 6.87 dB and third–order input intercept point of -9.03 dBm; from these numbers, the sensitivity is calculated to be -91.03 dBm while the spurious–free dynamic range equals 60.04 dB.

3.2 Implementation Highlights

This section provides details regarding design issues that presented themselves while transferring the block diagram representation to a circuit realization. Mundane details are left out in order to present the material in a clear, concise fashion. Information regarding component values and such can be obtained by examining the detailed schematics provided in Appendix B.

3.2.1 Choice of Ceramic Filter

Two ceramic filters were placed in the receive path. The first provides band filtering and image suppression; the second, placed between the low noise amplifier and the first mixer, provides further image suppression as well as attenuation of any harmonics that result from the amplifier. Since the project uses the DECT frequency band, ceramic filters marketed for DECT were readily available. The decision to use these filters also dictated that the first oscillator LO_{RF} should be placed lower than the carrier frequency (*low–side injection*). The explanation is that the ceramic filters are constructed assuming a translation to the DECT IF frequency of 110.592 MHz via low–side injection. Accordingly, the transfer function of the ceramic filters (Fig. 3-5) features maximum attenuation at approximately 1.670 GHz. This frequency is the location of the image in a common DECT system. Since the first IF in the base station is at 140 MHz, the image frequency is at 1.610 GHz and some of the benefits are lost. However low–side injection still provides better image suppression than high–side injection.

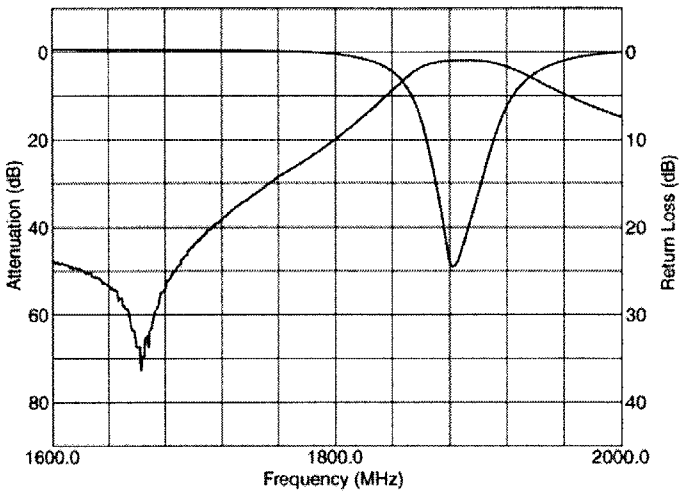


Figure 3-5: Transfer function of ceramic filter: Murata DFC21R89P020 HHE.

3.2.2 Channel Filtering at the Second IF

At the second IF, a high Q filter is desired to reject any near–by interferers. However, placing a passive filter composed of discrete components at the output port of the wide–band second mixer presents a problem. Given that passive filters function by varying their impedance, they are highly reflective to out of band signals. Since mixers produce both the difference and sum of frequency components, $\omega_{LO2} \pm \omega_{IF1}$, the filter will pass the difference term while reflecting the sum component back to the mixer. This term will mix with the second harmonic of the LO and produce a spurious signal at $\omega' = 2\omega_{LO2} - (\omega_{LO2} + \omega_{IF1}) = \omega_{IF2}$. This secondary signal is at the same frequency as the second IF.

Two solutions are available: insert resistive pads or use a constant impedance filter. By placing a 10 dB resistive pad between the mixer output and the filter, the reflected component will be attenuated by 20 dB before it re–enters the mixer. This solution is detrimental because it not only decrease the desired signal's level, it also contributes wide–band noise to the system and further degrades the noise figure. The other alternative is to use a constant-impedance filter. As it's name indicates, the filter provides a constant 50Ω load impedance to the mixer over a wide frequency

band. The drawback to these types of filters is that they're not available with high Q values. The band-pass filter used in this project decays with a slope of only 20 dB per decade of frequency.

Under some instances, the low–order response of the constant–impedance filter may be acceptable. However, the base station suffers from the sub-optimum frequency planning and requires additional filtering. The frequency synthesizer uses a 30 MHz digital reference oscillator that produce a harmonic at 180 MHz. Since the reference oscillator's peak–to–peak voltage swing of 5V is by far the largest on the board, the harmonics are rather large compared to the RF signals. It was found that this 180 MHz harmonic was able to leak directly into the second mixer's input port, thus bypassing the SAW filter. The signal then mixed with the 161.25 MHz LO signal and produced a spurious signal at 18.75 MHz. Since the second IF is at 21.25 MHz, the close proximity of the spurious signal caused the sensitivity of the system to be reduce to approximately -45 dBm.

In order to reduce the effects of the spur as well as further filter the channel, a third–order, elliptical bandpass filter centered at 21.25 MHz was designed. The filter, shown in Figure 3-6, was made tunable by incorporating two variable inductors into the design. The inductors allowed the null points in the frequency response to be tuned to the desired frequencies. Inductor L12 controls the lower frequency point while L11 tunes the upper point. As seen by simulation (Fig. 3-7), L12 can be varied so that the lower null occurs precisely at 18.75 MHz; once set, L11 is varied to set the filter's 3–dB down bandwidth equal to the channel width.

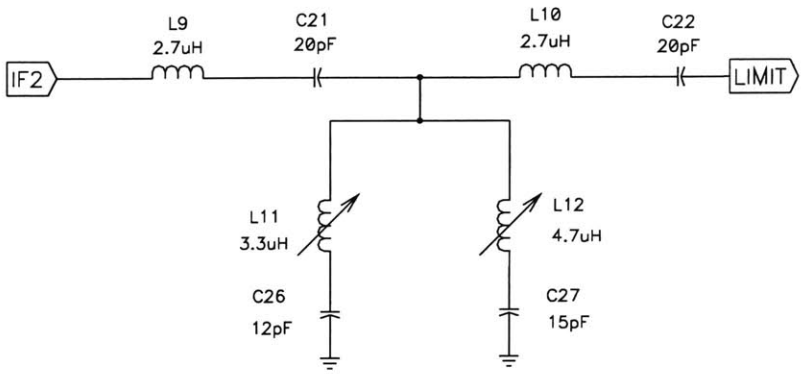


Figure 3-6: Third–order, tunable elliptical bandpass filter.

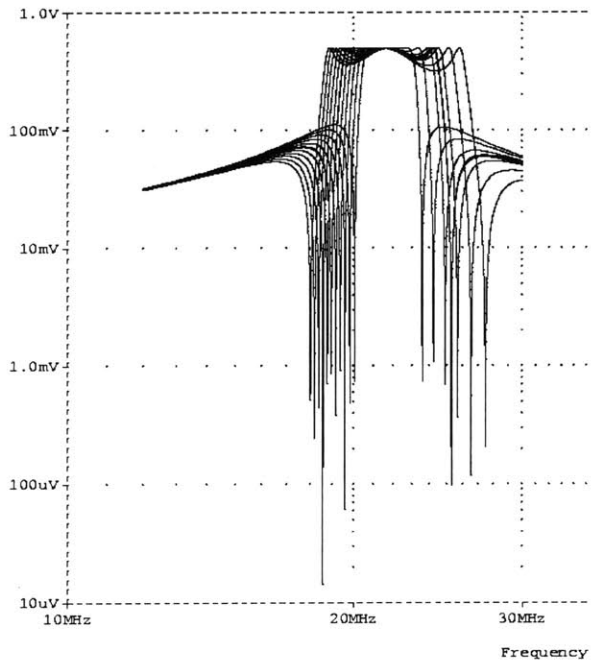


Figure 3-7: Simulation of elliptical filter tunability. Each variable inductor is varied ± 0.5 μH with the other at its nominal value.

3.2.3 Demodulator Design

The demodulator consists of a logarithmic limiting amplifier and a quadrature detector. Both sub–circuits were designed using two Motorola MC13155 Wideband FM IF chips (Fig. 3-8). The first chip functions solely as a limiter, while the second adds additional limiting gain and a detector.

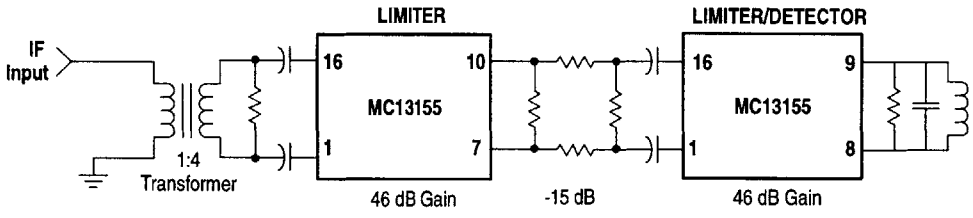


Figure 3-8: Block diagram of Limiter and Demodulator using two MC13155 chips.

Limiting is needed because the mixer in the quadrature demodulator requires large, sharp edges to perform well. Also, good channel filtering is required preceding the limiter stage. This is because the limiters utilize a logarithmic limiting function. Due to this non-linear response, the effect of the 18.75 MHz spur described in the previous section became highly corruptive at low input signal levels. By observing the output spectrum of the limiter, the gain experienced by the spur became larger as the input signal was decreased.

A single chip is specified as having 46 dB of power gain and an RSSI dynamic range of 35 dB; by cascading two chips, the effective gain is increased to 77 dB. The loss in effective gain is because 15 dB of interstage loss is placed in order to linearize the cascaded RSSI response. Figure 3-9 shows a typical cascaded RSSI response with and without interstage attenuation.

As described in Chapter 2, the quadrature detector requires a phase–shift network that varies from 180° to 0°, with a 90° phase–shift at the carrier frequency. Such a network is realized with a parallel RLC tank capacitively coupled to the input. In Figure 3-10(a), the coupling capacitor introduces a constant 90° phase shift to create the quadrature signal while the resonant tank provides instantaneous phase shifts in response to frequency changes. Figure 3-10(b) shows an equivalent differential

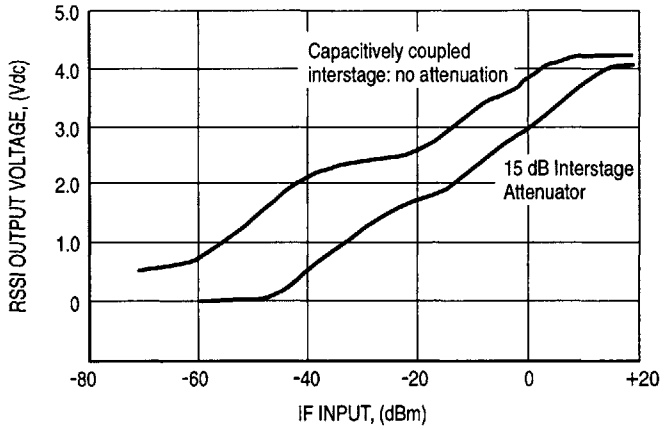


Figure 3-9: RSSI output voltage versus IF2 input power for two cascaded MC13155 chips.

network.

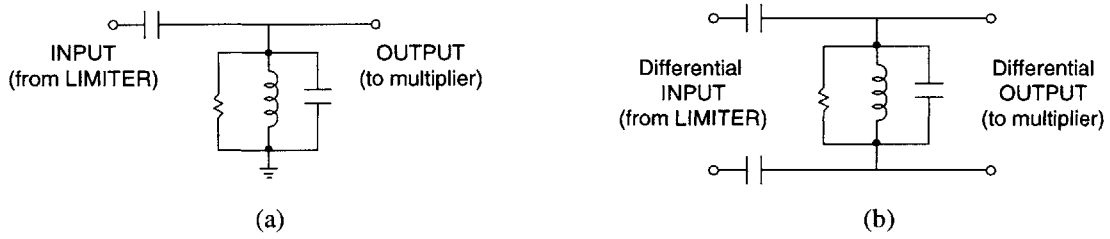


Figure 3-10: Phase–shift networks suitable for quadrature detection. Figure (a) is used in single–ended applications; figure (b) is used to for differential signals.

Since the circuitry in the MC13155 is fully differential, a differential resonant tank is used. Using half–circuit techniques, analysis of the differential circuit is equivalent to the single-ended case. The performance of the tank is determined by its Q. When designing the tank circuit, care has to be taken to account for the MC13155's internal resistance and capacitance. Setting the loaded Q of the tank to 5, and accounting for an internal capacitance of 3 pF and 3.2 kΩ of internal resistance shunted across the tank, the circuit shown in Figure 3-11 was designed. The phase response from simulation is shown in Figure 3-12.

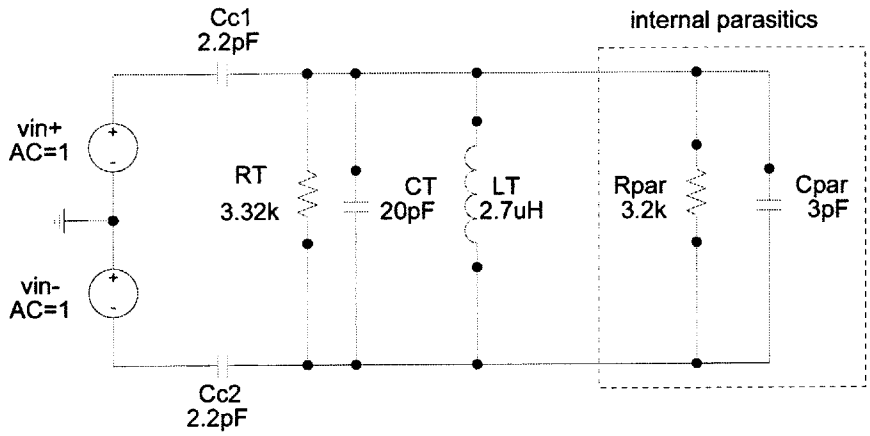


Figure 3-11: Differential phase–shift circuit used in the quadrature detector.

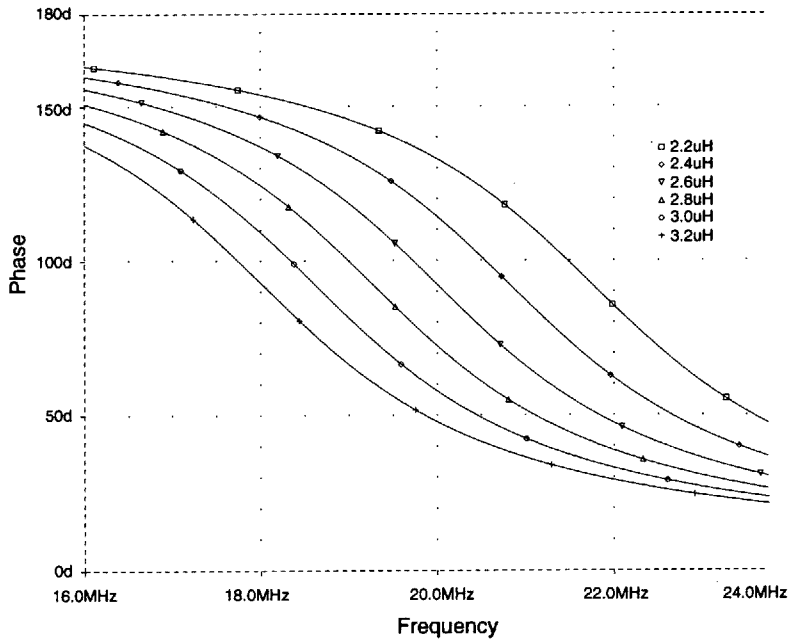


Figure 3-12: Phase response of differential phase–shift network. The resonant tank inductor, L_T, is varied over its tuning range in steps of 0.2μH.

3.2.4 Baseband Processing

The differential output of the demodulator is lowpass filtered and combined together using an operational amplifier circuit. Since the demodulator's output is DC coupled to the baseband section, an op–amp with a large common–mode input voltage range (CMVR) is warranted. Also, it is preferable that the op–amp run off a single 5V supply since everything else on the base station is powered off a single 5V rail. National Semiconductor's LM6152 Dual Rail–to–Rail I/O operation amplifier chip is found to be suitable. Capable of running off a single supply, the CMVR and output swing both approach rail–to–rail performance. Referring to the base-band circuitry reprinted in Figure 3-13, the stage also provides gain and performs level shifting. The level shifting is necessary to force the output DC level to 1.6V; this is the mean of the input voltage range for the subsequent analog–to–digital converter. The second op–amp in the LM6152 package is used to provide an amplified data signal for the off–board clock recovery circuitry.

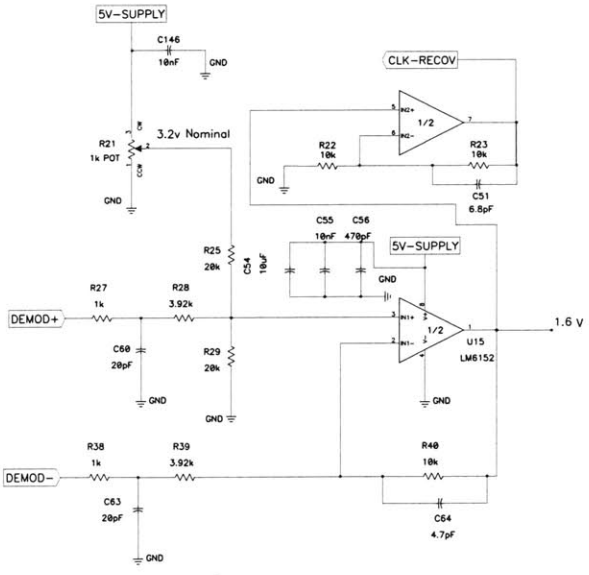


Figure 3-13: Baseband circuitry performing subtraction and level shifting.

The 8–bit analog–to–digital converter that follows the level shifter stage quantizes the analog signal. The sample clock signal is provided off board by the communications (COMMS) board. The choice to do clock recovery in the digital domain allows

the sample rate to be altered easily. Currently, the analog signal is sampled once per symbol; if over-sampling is desired, the sampling signal can be quickly reconfigured on the COMMS board. Another benefit is that noise and spurious signals due to harmonics are minimized by placing the majority of digital processing off board. The last stage of the receive path is a digital buffer that is used to drive the ribbon cable connecting the base station board to the COMMS board. LEDs are also included to assist in trimming the offset voltage in the level shifter stage. By driving the board with an unmodulated carrier signal, potentiometer R21 is varied until the LEDs indicate a logic level of $(10000000)_2$.

3.3 Receiver Printed Circuit Board Design

The design of the printed circuit board involves maximizing performance while minimizing size. Issues such as transmission line impedance, proper grounding, and noise reduction are considered during the layout process. When supplied, care is taken to follow the manufacturer's recommended layout. The following sections conclude this chapter by providing some of the key layout points.

3.3.1 Dimensions and Layers

The board designed for the base station is a four layer board. A cross–sectional view of the layers is shown in Figure 3-14. A total thickness of 62 mils was chosen because it not only facilitated reasonable transmission line widths, it was relatively sturdy; going down in size resulted in a very flimsy board while going up required very wide traces. The dielectric used was FR4 fiberglass with a relative permittivity of 4.8. Layer 1 was used primarily for analog signals. In order to reduce parasitic inductances and possible oscillations due to long ground loops, layer 2 was used entirely as a ground plane layer. Layer 3 was predominately a power plane supplying 5 V to all of the chips. Layer 4 was reserved for digital traces and power traces for the back channel transmitter. The board was designed as a 6" x 6" square with the antenna on one side and the COMMS interface on the other. This simplified the enclosure design to

a simple rectangular box with easily accessible ports.

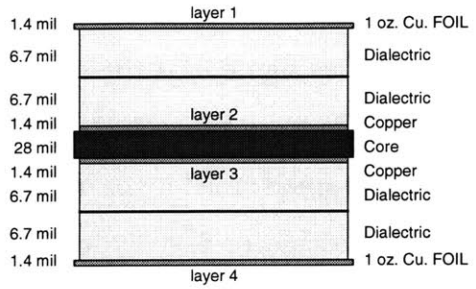


Figure 3-14: Cross–sectional view of printed circuit board.

3.3.2 Microstrip Line Impedance

At 1.89 GHz, transmission line effects become quite destructive on the scales of a printed circuit board. Impedance mismatches between a transmission line and connected load will cause reflected and standing waves to be present. In order to minimize signal corruption and maximize power transfer, transmission lines are carefully designed. Since most components were designed to be driven from as well as drive a 50 Ω impedance, a 50 Ω micro-strip line was developed. Using the dimensions given in Figure 3-14, the micro-strip calculator written by Dan McMahill [20] calculated that for a characteristic impedance of 50 Ω, a trace width of 22.7 mils is needed. As a check of the software, the 22.7 mil result was input into the following definitions derived in [21]:

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \cdot \frac{1}{\sqrt{1 + 12\frac{d}{W}}} \tag{3.1}$$

$$Z_0 = \begin{cases} \frac{60}{\sqrt{\epsilon_{eff}}} \cdot \ln\left(\frac{8d}{W} + \frac{W}{4d}\right) & \text{for } \frac{W}{d} \leq 1 \\ \frac{120\pi}{\sqrt{\epsilon_{eff}} \cdot \left(\frac{W}{d} + 1.393 + 0.667 \cdot \ln\left(\frac{W}{d} + 1.444\right)\right)} & \text{for } \frac{W}{d} \geq 1 \end{cases} \tag{3.2}$$

where ϵ_r is the relative permittivity of the dielectric, W is the width of the strip line, and d is equal to the distance from the metal trace to the ground plane. The result of setting $W = 22.7$mils was a characteristic impedance of 51.8 Ω. Note that the formulas given are not the only derivations available for a microstrip line; many other analytic and computational formulations of varying complexity exist.

3.3.3 Preventing Spurious Signals due to 30 MHz Harmonics

As previously discussed, the 6th harmonic of the reference oscillator was mixing with the second LO to produce a spurious signal near the second IF. Three steps are taken in order to minimize this effect. The trace between the SAW filter and second mixer is minimized in order to provide a minimal area for the harmonic to couple into. Second, instead of powering the reference oscillator directly from the third layer power plane, the plane is cut and an isolated trace is used. This effectively provides increased filtering on the supply line. Third, plated vias connected to ground were placed as guards around the synthesizer in an effort to provide the harmonics a low impedance paths to ground.

3.3.4 Increasing Isolation

In order to increase isolation between the SAW input and output port, a slot was placed in the board across the device by removing copper from all other layers. Also, the inductors which made up the matching networks were placed perpendicular to one another in order to minimize any mutual inductance. A similar slot was used to split up the ground plane beneath the analog–to–digital converter. One side carried the ground currents from the analog circuitry, while the other portion handled the much larger current spikes due to the digital circuits.

Chapter 4

Back Channel Design

This chapter presents the development of the back channel circuitry. Due to the low data rate requirements, the Analog Devices' AD6411 DECT chipset is used as a small, low–power solution. This chapter presents the AD6411 and its integration into the system. The chapter concludes with details regarding the board layout.

4.1 Analog Devices' AD6411 Chipset

Analog Devices' AD6411 DECT chipset provides most of the necessary receive and transmit circuitry to implement a low power digital wireless transceiver. As shown in Figure 4-1, for the receive chain the chip provides an RF mixer, integrated IF limiter and demodulator, and data slicer. The transmit circuitry consists of a VCO, frequency doubler, and buffer amplifier. With the addition of external filters, a power amplifier, and passive components, a complete transceiver is achieved. For the back channel, one AD6411 chip is designed for receive only purposes while another chip is configured for data transmission only.

The receiver functions by mixing the channel down to the first IF of 110.592 MHz. Demodulation is then performed with a hybrid IF strip/PLL demodulator; the PLL loop encloses the second mixing stage. The second LO is controlled by the PLL to force the instantaneous signal frequency at the second IF to match the reference frequency of 13.824 MHz. For example, if the signal frequency is greater than

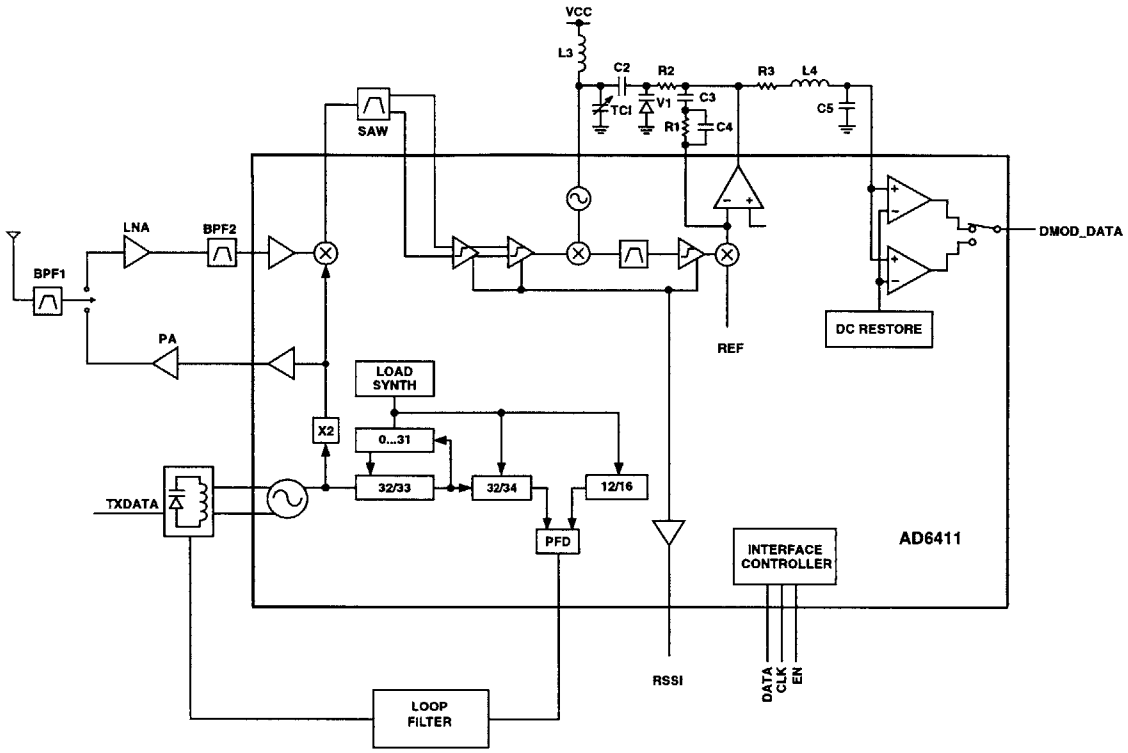


Figure 4-1: Block diagram of AD6411 DECT RF transceiver.

110.592 MHz, the PLL will cause the second LO signal to increase until the translated signal matches the reference frequency. Similarly, if the data signal is less than 110.592 MHz, the second LO will decrease until the mixed signal matches the 13.824 MHz reference signal. The data is recovered by looking at the second LO's control line. The signal can be sent out of the chip in analog form, or it can be bit sliced by using the integrated comparator and DC restoration circuitry.

For transmission, the VCO is directly modulated by the data stream. Prior to transmission, the synthesizer is used to achieve the correct carrier frequency. The VCO operates at half the final output frequency; an on–chip doubler translates the frequency to its correct carrier value. The synthesizer's charge pump is then placed in a high impedance mode and the VCO is modulated by the bit stream. The frequency drift is small enough for the required application, but it prevents the chip from being placed in a continuous transmit mode.

All programming and control of the chip is provided via a three-wire serial inter-

face. The interface consists of a 16–bit shift register and two latches for IC configuration and mode control. Additional lines need to be supplied to control external signals such as the power amplifier and LNA power down lines.

4.2 Circuit Implementation

This section provides details of some of the important design elements that came up while designing the back channel. Complete schematics of the back channel are available in Appendix B and C.

4.2.1 Reference Oscillator

A 13.824 MHz reference oscillator is needed for the frequency synthesizer. This signal provides the necessary reference for the synthesizer to produce all of the DECT channel frequencies. The schematic of the reference oscillator is provide in Figure 4-2. The design uses a digital crystal oscillator topology with a following low pass filter to suppress higher order harmonics. The filter also attenuates the signal to levels acceptable for the AD6411. A variable capacitor, C79, is added to trim the output to the desired frequency

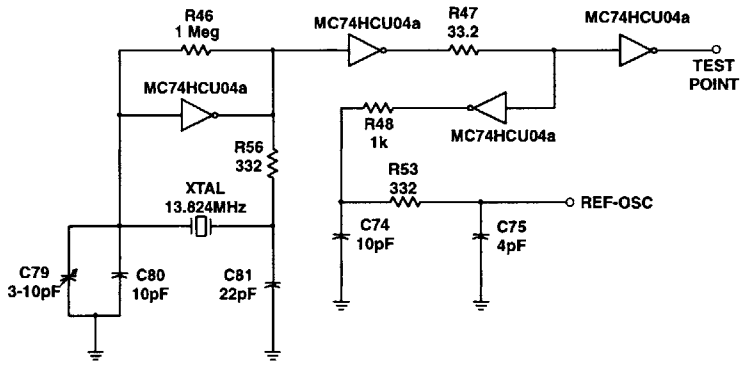


Figure 4-2: 13.824 MHz reference oscillator.

4.2.2 Balanced Resonant Tank Design

A balanced oscillator configuration is used to provide the synthesizer's VCO. A balanced topology has the advantages of rejection of common–mode interferers and noise. The external resonant tank is shown in Figure 4-3. Since the VCO operates at half its final value, the design is relaxed compared to designing a 1.89 GHz oscillator. Also, since the receive and transmit functions require the VCO to be in different bands, additional capacitance is added to the tank circuitry for the back channel receiver; this is achieved by switching the diode on.

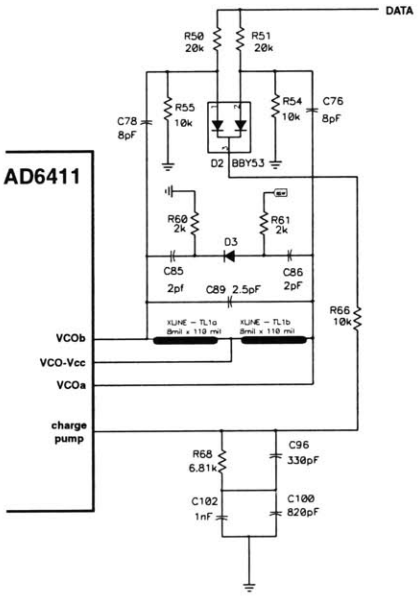


Figure 4-3: Balanced resonant tank circuitry.

4.2.3 Power Amplifier

The power amplifier used in the base station transmitter was designed to achieve an output power of approximately +24 dBm into the antenna. An attenuator pad is placed between the AD6411 output buffer and the power amplifier to reduce the input signal to acceptable levels; otherwise the power amplifier will be damaged. As a very optimistic estimate, the range of the transmitter can be calculated using the

Friis free-space transmission formula [18]:

$$\frac{W_r}{W_t} = G_t G_r \left(\frac{\lambda}{4\pi d}\right)^2 \tag{4.1}$$

where W_t and W_r are the transmitted and received power, G_t and G_r are the antenna gains, and d is the distance between the antennas. Assuming lossless antennas ($G_t = G_r = 1$) and a receiver sensitivity of -89 dBm, a range of 5.6 km is calculated. This estimate is highly optimistic because it assumes ideal conditions that are not practical. For indoor applications, power generally rolls off by a power of 4; the Friis transmission formula can then be modified to,

$$\frac{W_r}{W_t} = G_t G_r \left(\frac{\lambda}{4\pi d}\right)^4 \tag{4.2}$$

resulting in a transmission range of about 8.5 meters.

4.3 Printed Circuit Board Design

The layout of the back channel circuitry involved the same goals as the layout of the base station receiver. Care was taken to reduce overall size, parasitics, and impedance mismatches. In order to minimize size and parasitics, 0603 sized passives were used when possible. The layout of the AD6411 section followed the layout used in the Analog Devices demonstration board. Additional board information such as stripline design and isolation techniques can be found in the board layout section in the previous chapter.

4.3.1 Layers and Form Factor

Both back channel circuits were laid out on 4 layer, 1/16 inch boards. The top layer was used primarily for analog signals while digital signals were placed on the bottom, 4th layer. Layer 2 was used as a ground plane in order to minimize inductances in the ground loops. Layer 3 was used for routing and for supplying power to the AD6411.

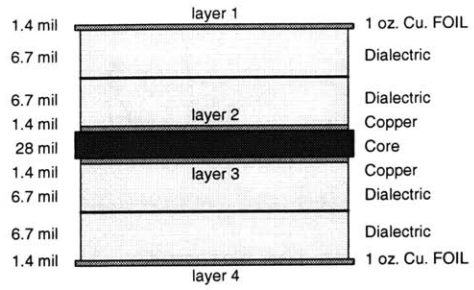


Figure 4-4: Cross–sectional view of back channel printed circuit boards.

The cross sectional profile of both boards is shown in Figure 4-4

4.3.2 Power Management

The base station board runs off a single +5 V external supply, However, the AD6411 and power amplifier requires +3.3 V. Low dropout regulators are added to the base station board to furnish this supply value. Separate regulators are used in order to further isolate the power amplifier from the AD6411's frequency synthesizer; this is due to the issue of *load pulling.* An example of load pulling occurs when the oscillator's output signal inadvertently shifts due to changing load conditions. In this particular system, since the transmit VCO is being modulated in an open–loop configuration, it is highly sensitive to changing load conditions. Since in mobile applications the power amplifier is turned off and on to minimize power consumption, an amplifier with high reverse isolation is required to buffer the VCO from the changing input impedance of the power amplifier. Another source of error is due to the poor power supply rejection of most RF oscillators. Since the power amplifier sources a large amount of current when turned on, the supply voltage may change significantly due to the supply's finite output resistance. By using separate regulators in addition to the on–chip regulation provided by the AD5411, the frequency synthesizer is well isolated from these supply variations.

Chapter 5

Results

Measured results of all three circuits — base station receiver, base station transmitter, sensor receiver — are presented in this chapter. Sections 5.1 and 5.2 address the base station receiver while the remainder focus on the back channel. Each set of tests is preceded by a brief introduction containing information needed to setup each board.

5.1 Base Station Testing

The base station is tested using a DECT capable signal generator. Unfortunately, the maximum allowable bit rate of this generator is 1.3 Mbps. When feasible, the sensor camera was used to provide a 2.5 Mbps signal.

5.1.1 Tuning the Elliptical Filter

The 21.25 MHz elliptical bandpass filter was tuned by setting the jumpers to SMA and connecting the filter's ports to a network analyzer. By varying L12 in Figure 5-1, the lower frequency notch is placed precisely at 18.75 MHz, the location of the spur discussed in Chapter 3. L11 is then tuned to set the 3-dB bandwidth of the filter to about 4 MHz (Fig 5-2). The notches at 18.75 MHz and 24.85 MHz result in a 3-dB bandwidth of 4.00 MHz at a center frequency of 21.25 MHz. The rejection is -21.75 dBm at the lower notch and -38 dBm at the higher notch; the filter rejection is -15

dBm for low frequencies and -26 dBm for higher frequencies.

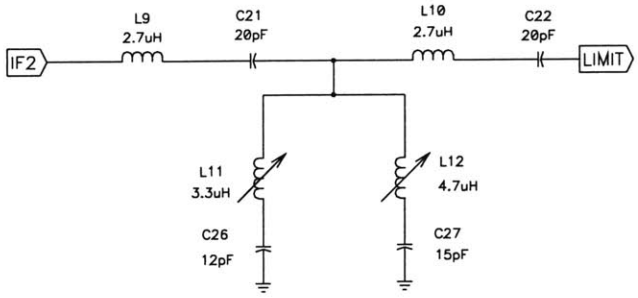


Figure 5-1: Third–order, tunable elliptical bandpass filter.

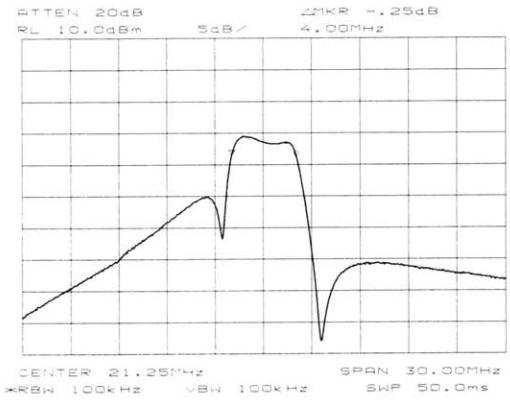


Figure 5-2: Measured frequency response of elliptical bandpass filter.

5.1.2 Tuning Quadrature Tank Circuitry

The inductor in the quadrature detector must be tuned prior to use. This is accomplished by inputing an unmodulated carrier signal into the antenna port and by watching the differential output of the detector. The inductor is varied until the DC level of both outputs match each other. Ideally the common DC value should be half way between the power supply values, but this will not necessarily be true.

5.1.3 Setting Baseband Reference Voltage

Since the input range of the analog–to–digital converter in the baseband circuitry is centered at 1.6 V, R21 needs to varied until the DC level into the ADC is 1.6 V.

To set this resistance, an unmodulated carrier signal is applied and allowed to travel through the tuned demodulator and to the ADC. Resistor R21 is then varied until the ADC produces a digital $(10000000)_2$, as seen by monitoring the LEDs attached at the output of the ADC. Once set, the ADC is specified as providing a full scale input range of 2 V (1.6 ± 1.0 V).

5.2 Base Station Receiver Results

5.2.1 Third–Order Intermodulation

A measurement of the third–order input intercept point was performed by applying an RF carrier signal at 1890 MHz and an equal interferer signal at 1891 MHz. The input power of both signals was swept while measuring the fundamental and intermodulation components at the output of the elliptical filter. A plot of the measurements is given in Figure 5-3. By curve fitting the data and extrapolating the lines, an IIP_3 value of 7.31 dBm was found. This is much higher than the calculated value of -9.03 dBm because the calculated value doesn't take into account any filtering placed in the receive chain. In particular, the SAW filter and the elliptical channel filter reduce the intermodulation terms significantly.

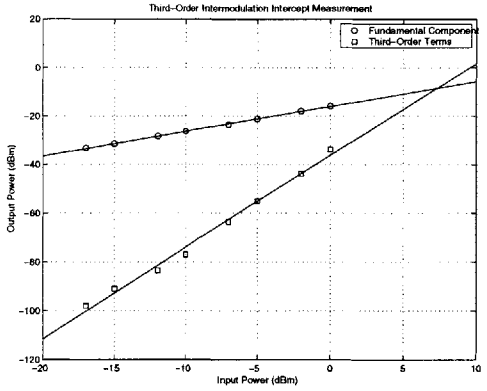


Figure 5-3: Third–order input intercept measurement. Input signals were spaced 1 MHz apart; measurements were taken at the output of the elliptical channel filter.

5.2.2 Limiter Output

The effects of noise and spurious signals at the second IF can be seen in Figure 5-4. Figure (a) shows the output spectrum for a modulated input signal with an input power of -20 dBm. The remaining figures include a plot of this signal as a reference. As seen in figures (b) and (c), decreasing the input power to -40 dBm and -60 dBm results in little or no amount of increased noise. However, figure (d) shows that at -80 dBm, the signal still limits but the contributions due to spurious signals begin to cover up the desired channel. At these low values of input power, the noise overtakes the desired signal and the information becomes unrecoverable.

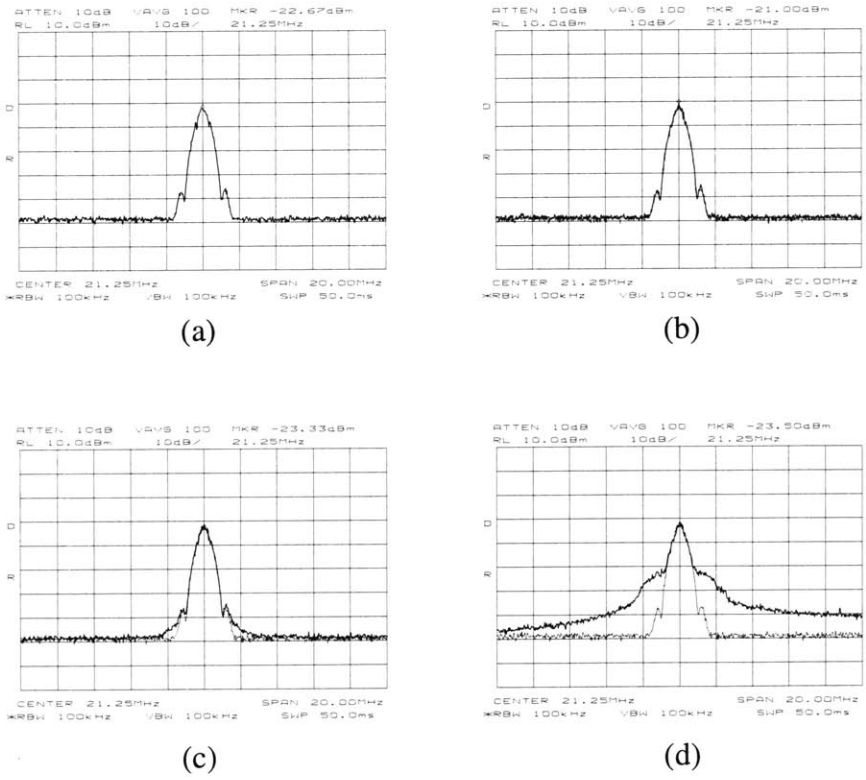


Figure 5-4: Effects of spurious signals entering the limiter. Figure (a) shows the output spectrum for a -20 dBm input signal. The input power for the remaining figures: (b)= -40 dBm, (c)= -60dBm,(d)= -80 dBm. Figure (a) is superimposed on the remaining figures to provide a reference.

5.2.3 Eye Diagrams

Eye diagrams at the demodulator's output are shown in Figures (5-5) – (5-7). For large input levels, the eye expectedly displays a large amount of overshoot. While this signal is still recoverable, +10 dBm is greater than the measured third–order intercept point of +7.31 dBm, and in a field setting this signal would be accompanied with large amounts of non-linear distortion and adjacent–channel interference. At low input levels the eye begins to *close*. As discussed in the previous section, this is not directly due to the input level bring too low to be limited, but rather because the spurious signals witness a greater amount of gain in the limiter when the input is low.

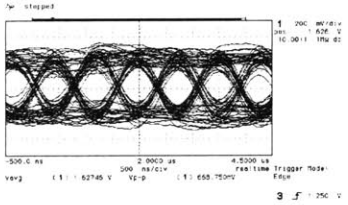


Figure 5-5: Eye diagram: +10 dBm input power at antenna.

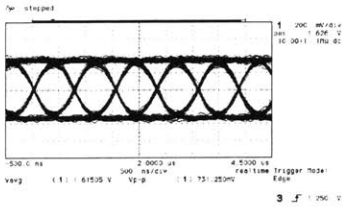


Figure 5-6: Eye diagram: -50 dBm input power at antenna.

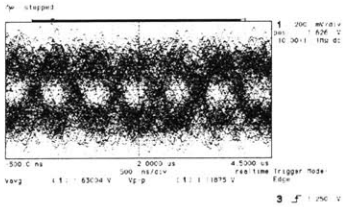


Figure 5-7: Eye diagram: -70 dBm input power at antenna.

5.2.4 Bit Error Rates and Sensitivity

Bit error rate and sensitivity measurements were made using the wireless camera hardwired to the receiver. The camera was positioned to transmit an image while the received input power was varied by using RF attenuators. Bit error rate values were calculated by reading in one million bits and using error correction to determine the number of incorrect bits. The input power was determined by monitoring the RSSI signal and comparing the values to measured data displayed in Figure 5-8. A plot of the measured BER values are shown in Figure 5-9. Figure 5-10 shows three cases of the BER test. Since the imaging algorithms use the preamble to properly display an image, turning off error correction causes errors in the preamble to ripple throughout the data block and produce image streaking. Thus the true BER of the transmission is much less than that seen visually in the screen captures. To see the difference, bit errors lengths of three or more are filtered out of the scatter plot and a more representative plot is shown on the bottom row.

From the plot, a 10^{-3} BER occurs at approximately -71 dBm. This sensitivity is less than expected; two major factors are the low RF mixer gain and insertion loss of the elliptical filter. The RF mixer's gain was 6 db less than that measured in the first version of the base station board. Solutions include replacing the part as well as checking the matching networks on the mixer's ports. The elliptical filter was not in the first version of the base station board and its insertion loss was not included in the initial calculation of the sensitivity. The loss may be reduced by increasing the gain of the amplifier driving the filter.

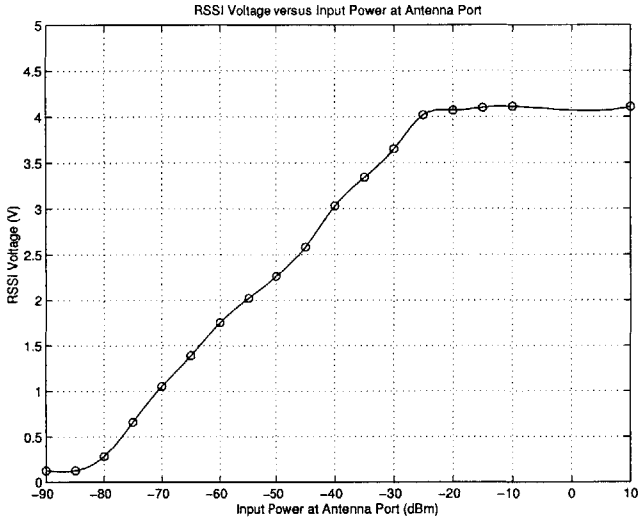


Figure 5-8: Measured RSSI voltage versus input power.

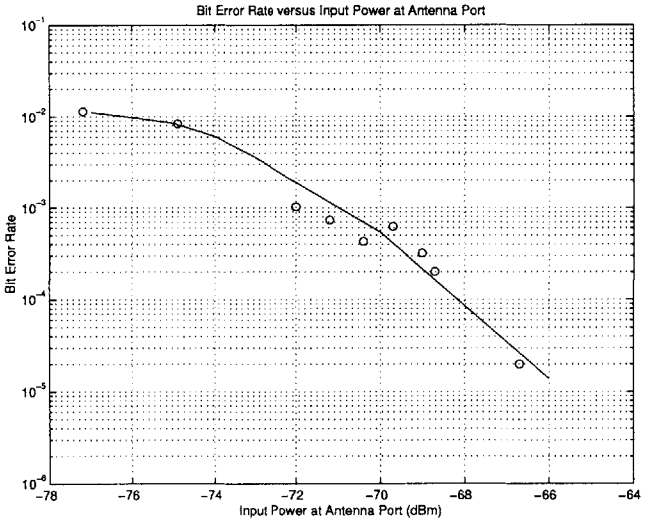


Figure 5-9: Bit error rate versus input power.

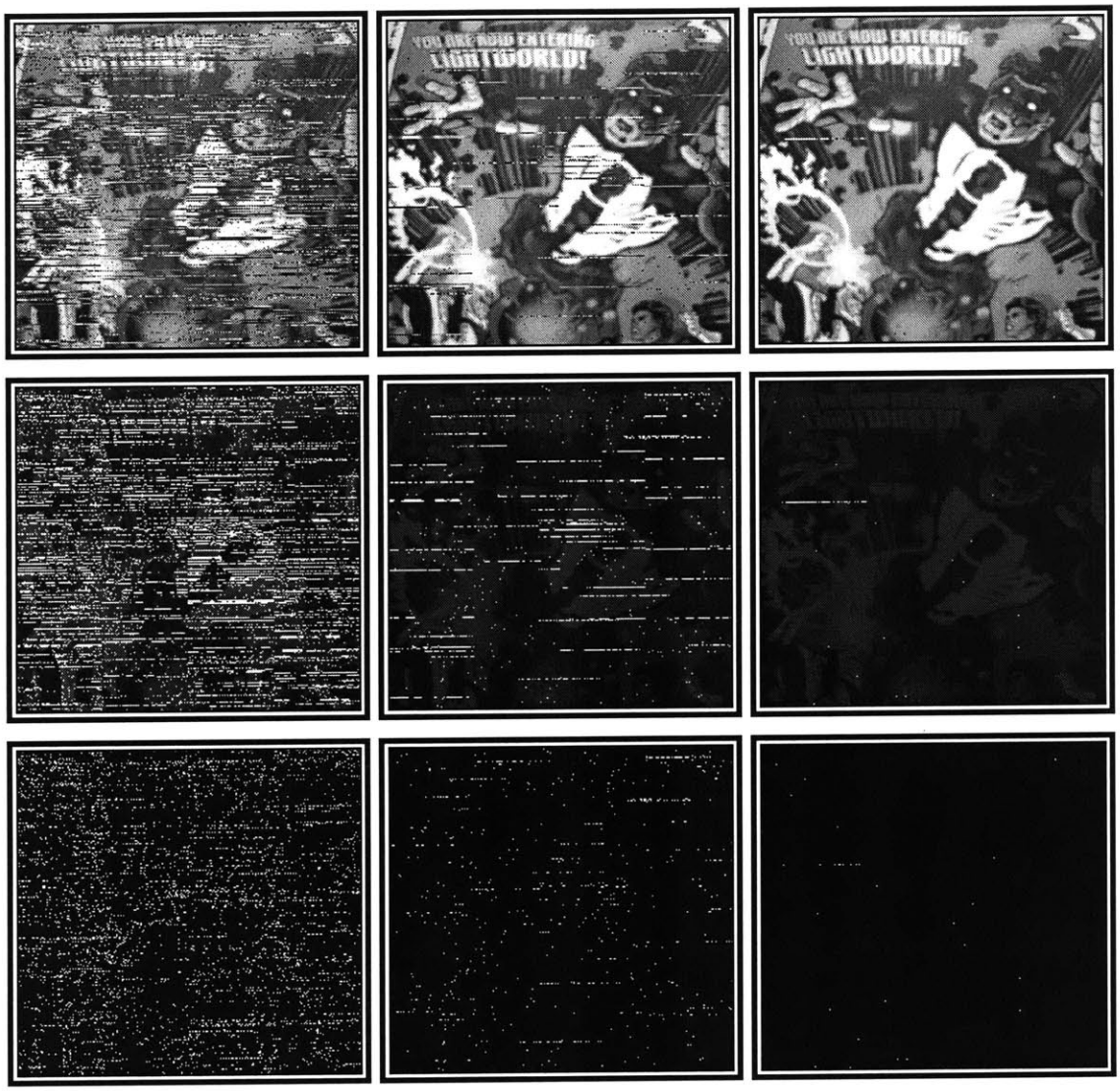


Figure 5-10: Screenshots of BER test. The top row shows screen grabs at three different power levels (left to right: -75 dBm, -70 dBm, -67 dBm). Beneath each screenshot is a scatter plot showing the location of each error bit. The error free image superimposed on each plot serves to provide a reference between a scatter plot and its screenshot. The bottom row shows the scatter plots filtered of long bit error lengths due to an error in the preamble.

5.2.5 Effects of Frequency Drift

Measurements of the effects of carrier drift were taken to determine how much error or drift could be accepted. Since the quadrature detector doesn't *lock* onto the carrier like a PLL, there's no stability or locking time concerns; rather frequency offsets cause varying output DC values and non-optimum output swings. Measurements of these effects are shown in Figure 5-11. The peak–to–peak variation indicates that the quadrature detector coil needs to be slightly varied for maximum peak–to–peak output voltage at the carrier frequency. The changing DC value limits the effectiveness of analog–to–digital converter. The ADC's input range is centered at 1.6 V; for large frequency drifts or errors, a dynamic DC offset system incorporating feedback would need to be implemented in order to properly center the demodulated signal.

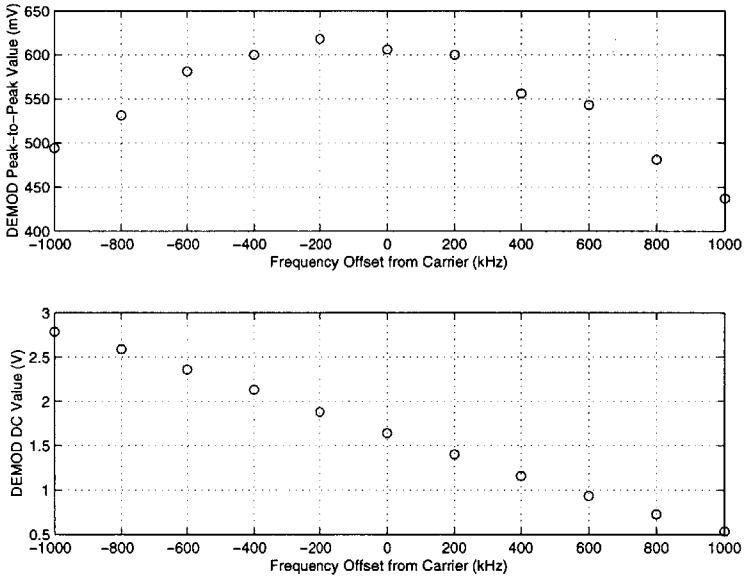


Figure 5-11: Effects of frequency drift on the demodulated output signal.

5.3 Back Channel Testing

5.3.1 Test Setup

Similar to the base station receiver, the back channel circuitry was tested independently with a DECT capable signal generator. The testing was performed in the 4th DECT channel at a carrier frequency of 1890.432 MHz. Programming of the AD6411 is provided in Appendix E.

The reference oscillator on both back channel circuits needs to be trimmed in order to obtained the desired amount of accuracy. This is performed by connecting the spectrum analyzer to the reference clock test point and then trimming the variable capacitor (C104 on the transmitter, C79 on the receiver) until the spectrum is at exactly 13.824 MHz.

If the on–chip data slicer is to be used, its reference voltage needs to be trimmed. This is accomplished by applying a continuously modulated signal of $\{1, 0, 1, 0, \ldots\}$ and monitoring the data slicer's output. By varying C101 in the receiver, the data slicer's output duty cycle should be made approximately 50%.

5.3.2 Back Channel Transmitter Results

Synthesizer Characterization

The AD6411's VCO is the most crucial element in the chipset. In order to assist future revisions or further use of the chipset, measurements of the transmit VCO's range and switching dynamics were made. Figure 5-12 shows the measured tuning curve of the VCO. The average tuning sensitivity K_{VCO} was measured to be 16.868 MHz/V.

Switching dynamics were tested by forcing the VCO to switch from DECT channels 9 to 0 and then back. The results of these measurements are shown in Figures 5-13 & 5-14. The rise time, including the settling time to within 1%, was measured to be 32.7μs; the fall time measurement was 35.4 μs.

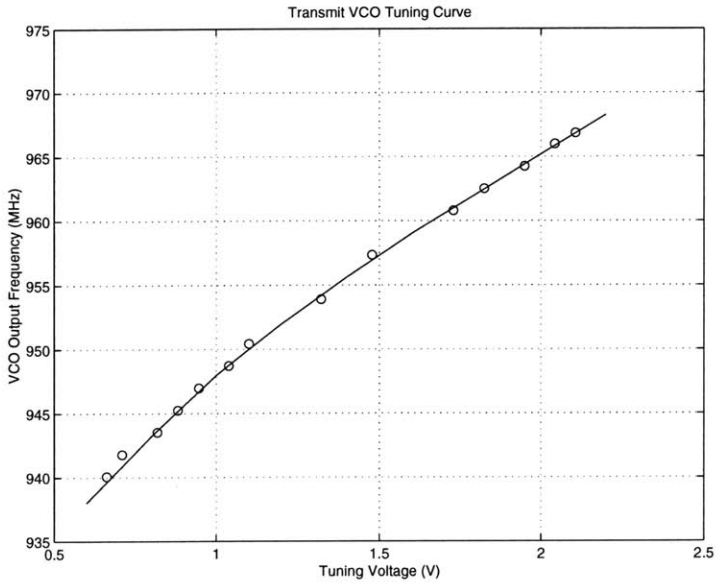


Figure 5-12: Transmit VCO tuning curve.

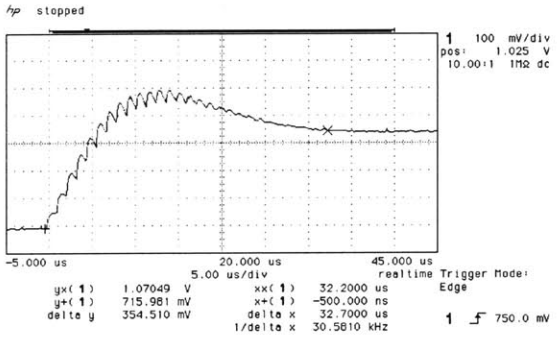


Figure 5-13: Transmit VCO rise time: channel 9 to 0.

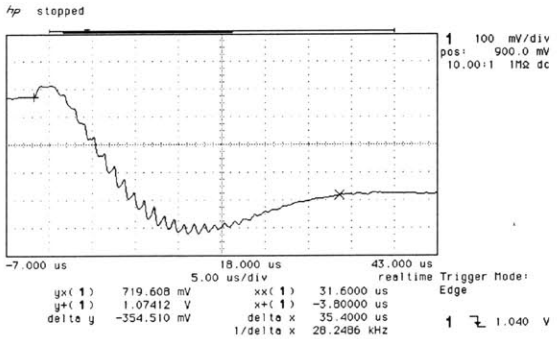


Figure 5-14: Transmit VCO fall time: channel 0 to 9.

Since the VCO is directly modulated in the transmit mode, the PLL charge pump is placed into a high impedance state. This causes the VCO output to drift since it is now operating in an open loop configuration. A measurement of frequency drift showed that on average the VCO output changed by 675 kHz over a 20 second period. Assuming a constant rate of change, this translates into a drift of about 32.9 kHz per second.

Output Spectrum

The output spectrum of the back channel transmitter modulated by a 1.3 Mbps pseudo–random bit stream is shown in Figure 5-15. The spectrum can be manipulated by either altering the transmit filter or by changing the modulation index by varying R61. Is was found that when the RF switch was placed in receive mode, the output of the power amplifier was at 24.50 dBm. However, when the switch was placed in transmit mode, the output power dropped to 15.42 dBm. In order to obtain the desired maximum signal, the amplifier–to–switch interface needs to be optimized.

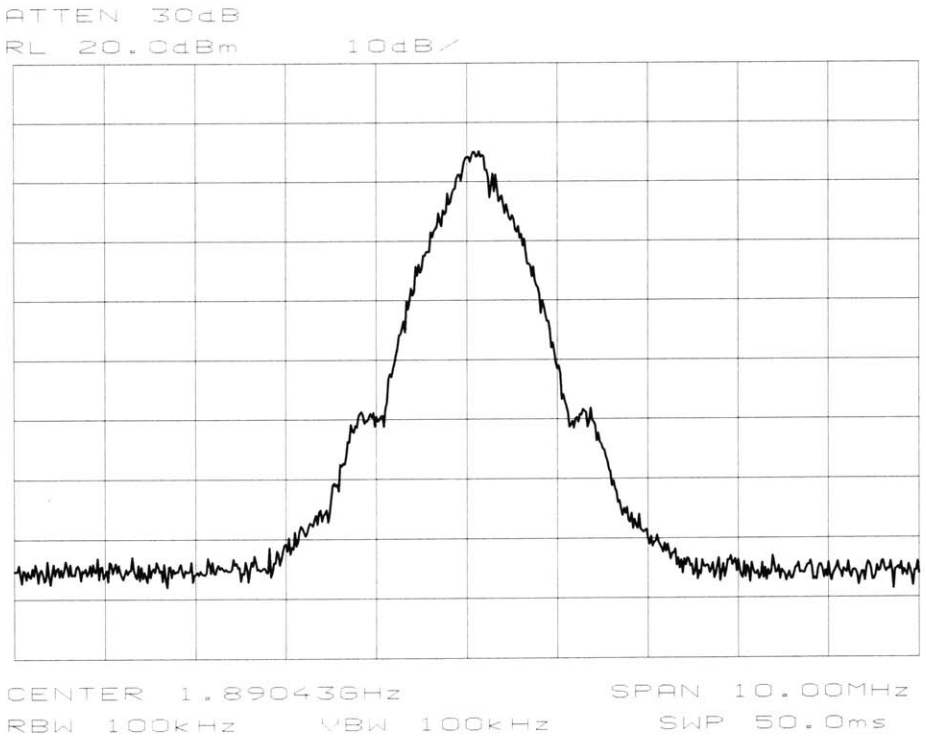


Figure 5-15: Back channel transmitter output spectrum.

5.3.3 Back Channel Receiver Results

RSSI Measurements

The back channel was tested similarly to the base station receiver. Received signal strength measurements were taken in order to assist in the system integration. Measurements were taken by varying the power levels of an unmodulated carrier at the antenna port. The results are provide in Figure 5-16.

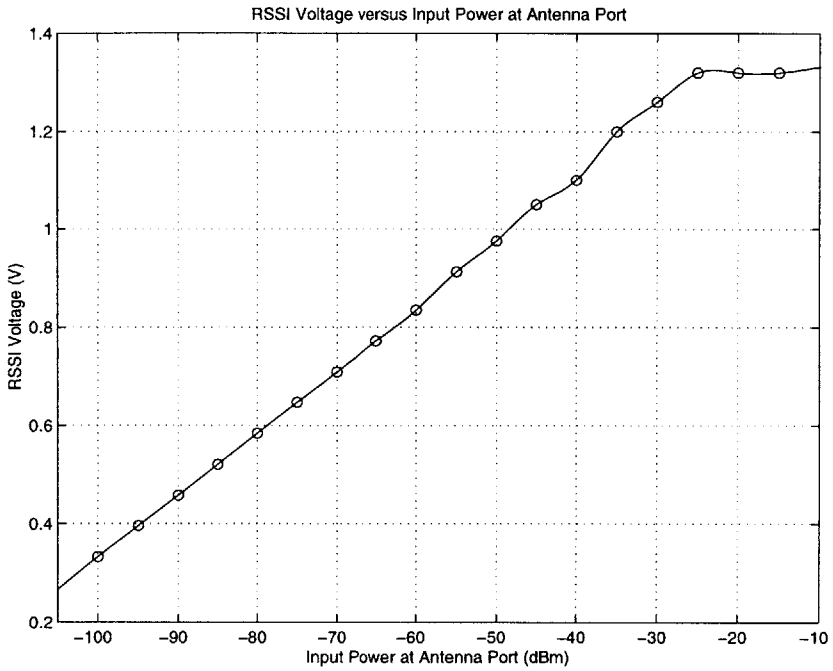


Figure 5-16: Back channel receiver RSSI voltage versus input power.

Eye Diagrams

Eye diagrams for bit rates of 500 kbps and 1.3 Mbps are shown. The upper trace is the analog demodulated eye diagram while the lower trace is the output of the data slicer. The diagrams show an open eye down to input levels of -95 dBm.

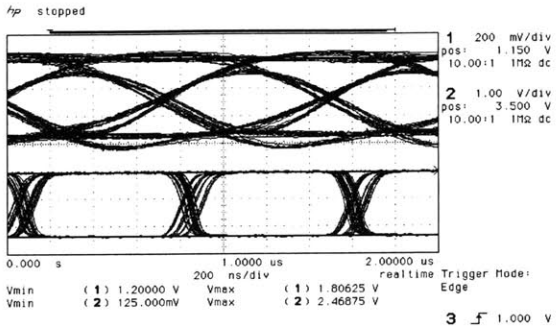


Figure 5-17: Eye diagram: -5 dBm, 1.3 Mbps.

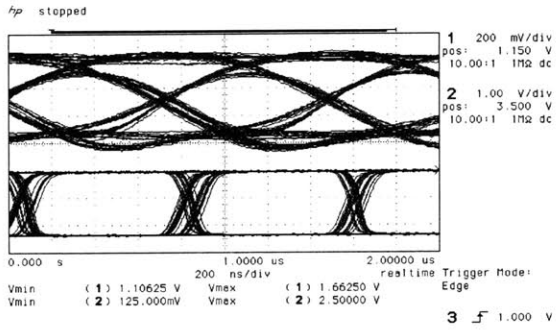


Figure 5-18: Eye diagram: -40 dBm, 1.3 Mbps.

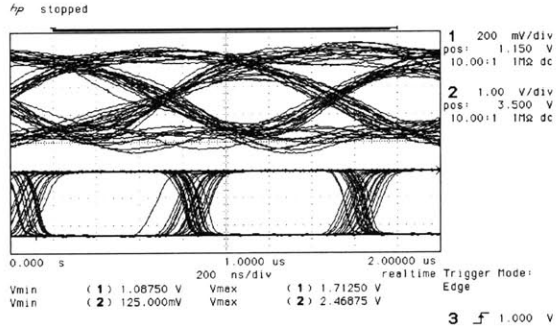


Figure 5-19: Eye diagram: -80 dBm, 1.3 Mbps.

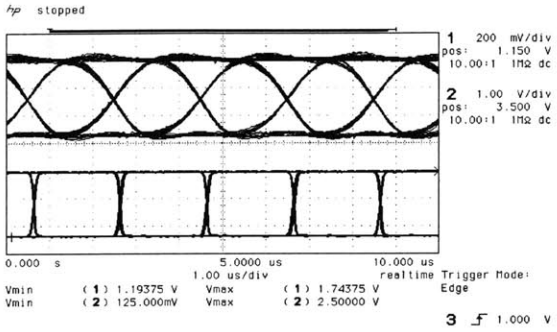


Figure 5-20: Eye diagram: -5 dBm, 500 kbps.

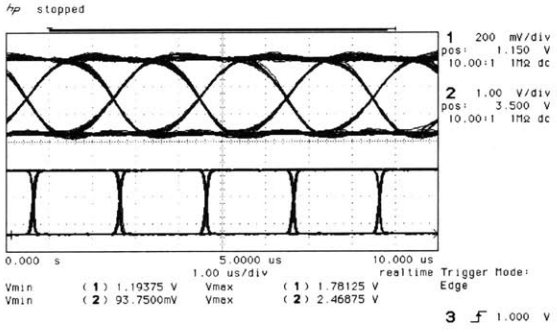


Figure 5-21: Eye diagram: -40 dBm, 500 kbps.

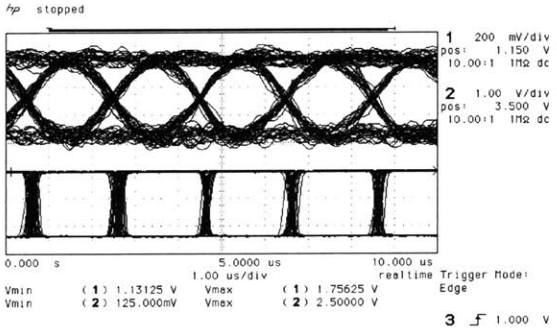


Figure 5-22: Eye diagram: -80 dBm, 500 kbps.

Power Consumption

Since the back channel receiver is placed on the mobile sensor board, it is desirable that power consumption be small. The following table gives power measurements of the receiver under different operating conditions. Note that the actual system power consumption will be less due to duty ratio-ing.

Receiver Conditions	**Power Consumption**
Rx on, LNA on	416 mW
Rx on, LNA off	284 mW
All off except regulators	53 mW

Table 5.1: Back channel receiver power consumption.

Chapter 6

Conclusions

This thesis has presented the analog hardware necessary to implement a demonstration system for MIT's ultra low–power wireless sensors. This chapter recapitulates the project and provides future improvements.

6.1 Summary

In order to demonstrate the low–power wireless sensors developed at MIT, a demonstration unit was needed. The demonstration unit required a base station receiver to obtain and recover the information transmitted by the sensors. A back channel link consisting of a base station transmitter and mobile sensor receiver were also needed for the communication of control information. The objective of this project was to design and build all of the front–end hardware of the system. Due to time for design and ease of implementation, all of the circuitry was built with discrete, commercially available components

The base station receiver achieved a sensitivity of -71 dBm with a bit error rate of 10^{-3}. The spurious–free dynamic range was measured to be 63 dB. Once integrated with the DSP and baseband processing units, the receiver demonstrated the capability of reliably recovering the sensor's transmitted data. The back channel circuitry also achieved its desired performance. While a bit rate of only 100 kbps is required, the back channel is capable of up to at least 1.3 Mbps transfer. The entire system —

sensor, front–end hardware, baseband processing, user interface — has been built and is functional.

6.2 Improvements

The following improvements, while not necessary, will help to further optimize the hardware designed in this project. In order to further enhance the receiver sensitivity, unexpected loss in the receive chain needs to be investigated and corrected. As previously explained, the RF mixer provided less gain that previously shown. Also, the insertion loss of the elliptical filter can be negated be increasing the gain of the preceding amplifier.

The detriments of frequency error or drift can be corrected by using an active DC offset system in the base band circuitry. By looking at the demodulated data stream, a digital-to-analog converter could be used to alter the DC voltage being added to the demodulated signal. The feedback loop would attempt to force the signal entering the ADC to have a DC value of 1.6 V.

The power amplifier in the back channel transmitter suffers from a sub–optimum loading circuitry. The output power level drops from 24.5 dBm to 15.4 dBm when the RF switch is switched from receive to transmit. In order to maintain the higher level, the load needs to be redesigned. However, the issue may be moot since it the sensor side transmitter, not the back channel transmitter, that is limiting the range of the system.

While not a design goal or requirement, another improvement would be to reduce the power consumption of the base station. When receiving, the circuit consumes a total of 1.6 W. Areas of power reduction include a lower power LNA as well as alternate biasing circuits for the IF amplifiers. Currently the amplifiers are biased via a current mirror; current mirrors were chosen oven a simple resistor because of stability considerations involved with low power supply lines. However, this choice results in twice the required device current being sourced from the supply (half goes into the device, the other half lost in the mirror). Possible solutions include alternate

current supply circuits as well as trying a resistor and testing for stability.

6.3 Future Work

Future work could include optimizing the circuitry for the desired response without being constrained by available off–the–self components. Different architectures could be studied and implemented. While integrating the base station into a single chip may not be feasible or even useful, the sensor back channel receiver could be redesigned into a single chip solution. This would allow the entire sensor board to be integrated and made tiny. This is ultimately the desired end product.

Appendix A

Fundamental Concepts

Before one blindly rushes in and attempts to design RF circuits that meet a set of prescribed specifications, a designer must be knowledgeable of the many concepts and terminologies employed in RF electronics. While many of the concepts are rooted in fundamental signal and systems analysis, they require the novice to extend beyond the traditional linear time-invariant (LTI) models usually employed in introductory courses. Another challenge is the rapid convergence of many disciplines that must be utilized in order to address a radio frequency project from a system viewpoint. In addition to signal theory and circuit design techniques, the designer must also have a solid understanding of topics as diverse as electrodynamics and signal propagation to stochastics and communication theory. Combined with IC or board layout issues, RF electronics presents a uniquely multidisciplinary problem that is overwhelming, yet at the same time intellectually challenging and ultimately stimulating.

This appendix presents a number of important concepts that are necessary to comprehend before one dives into designing any RF circuitry. This review begins with an introductory discussion on non–linear systems and then progresses to a brief section on noise. Next, the cause and detrimental effects of intersymbol interference are explored. The chapter concludes with a discussion of system metrics such as bit error rate, sensitivity, and dynamic range. Along the way, a number of important parameters are introduced and defined where appropriate. While an in depth treatise on all these fields is well beyond the scope of this thesis, cross–references with

additional analysis have been included for the reader to refer to.

A.1 Nonlinearity

Loosely stated, a linear system is one in which the system's output exhibits the property of superposition: the system response can be expressed as a linear combination of responses to the individual stimuli. In other words, if:

$$f[x_1(t)] = y_1(t), \quad f[x_2(t)] = y_2(t); \tag{A.1}$$

then by superposition we require for any constants α and β that:

$$f[\alpha x_1(t) + \beta x_2(t)] = \alpha y_1(t) + \beta y_2(t) \tag{A.2}$$

Any system f which fails the preceding requirement is categorized as being nonlinear. While most elements can be approximated by a linear transfer function over some small region, higher order terms must be factored in to account for some phenomena that are witnessed and possibly utilized. For the following discussions, we will limit our system to a memoryless, time-variant system whose response is approximated as:

$$f[x(t)] \approx \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \tag{A.3}$$

A.1.1 Harmonics

If the input to the system in Eq. (A.3) is a pure sinusoidal wave of amplitude A and angular frequency ω, then by direct substitution,

$$f[x(t)] = \alpha_0 + \alpha_1 A\cos\omega t + \alpha_2 A^2\cos^2\omega t + \alpha_3 A^3\cos^3\omega t \tag{A.4}$$

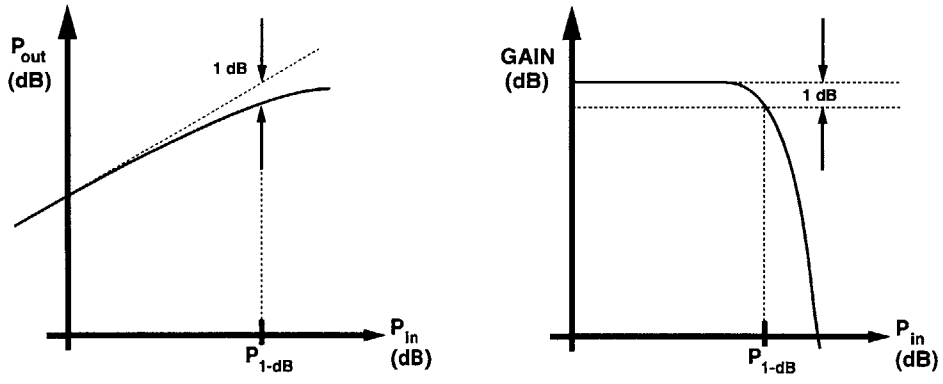
$$= \alpha_0 + \alpha_1 A\cos\omega t + \frac{\alpha_2 A^2}{2}(1+\cos 2\omega t) + \frac{\alpha_3 A^3}{4}(3\cos\omega t + \cos 3\omega t) \tag{A.5}$$

$$= \left(\alpha_0 + \frac{\alpha_2 A^2}{2}\right) + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos\omega t + \frac{\alpha_2 A^2}{2}\cos 2\omega t + \frac{\alpha_3 A^3}{4}\cos 3\omega t \tag{A.6}$$

By examining Eq. (A.6), we see that unlike a linear system whose output differs from a sinusoidal excitation solely in amplitude and phase, a nonlinear system can add an additional DC term to the existing output bias as well as produce new frequency components that are integer multiples of the input frequency. Also of note is that the odd harmonics are a result of only the odd-order terms in Eq. (A.3); similarly, the even harmonics are due to the even-order terms. Thus, ideally, a fully differential system ($\alpha_i \to 0$, for all even i) will produce no even-order harmonics.

A.1.2 Gain Compression

Assuming that the output harmonics are negligible for small input levels, the small-signal gain of the system from Eq. (A.6) becomes simply α_1. However, as the input amplitude begins to increase, the system gain begins to vary due to the emergence of harmonics. If only the first-order term is considered, then the gain of the system becomes $\alpha_1 + 3\alpha_3 A^2/4$. Since most circuits exhibit lowering gain in response to very high input levels, it can be assumed that $\alpha_3 < 0$. Figure A-1 shows a typical circuit's power transfer characteristic. For low input levels, the gain remains constant; at higher levels, however, we see that the gain begins to decrease and the output power veers away from its expected value. The input level at which the small-signal gain



(a) (b)

Figure A-1: Illustration of gain compression. Figure (a) shows output power versus input power. Figure (b) shows an alternative view with gain on the vertical axis and input power on the horizontal axis.

has dropped by 1 dB is parameterized as the *1–dB compression point* ($P_{1\ dB}$). This compression is one factor contributing to the ceiling of the system's dynamic range.

A.1.3 Intermodulation

Intermodulation causes the presence of spectral components in the output that are not harmonics of the input signals. This can occur when two signals of differing frequencies are applied to a nonlinear system. To see this effect mathematically, assume the input to Eq. (A.6) is $x(t) = A_1 \cos\omega_1 t + A_2 \cos\omega_2 t$; also assume the two frequencies are close enough in value such that the frequency variations in the system coefficients can be ignored. Direct substitution into the system results in,

$$\begin{aligned} f[x(t)] &= \alpha_0 + \alpha_1(A_1 \cos\omega_1 t + A_2 \cos\omega_2) + \alpha_2(A_1 \cos\omega_1 t + A_2 \cos\omega_2)^2 \\ &\quad +\alpha_3(A_1 \cos\omega_1 t + A_2 \cos\omega_2)^3 \end{aligned} \tag{A.7}$$

By expanding the right side of the equation, we see that in addition to fundamental and harmonic terms, we get the following intermodulation terms:

$$\alpha_2 A_1 A_2 \cos(\omega_1 + \omega_2) + \alpha_2 A_1 A_2 \cos(\omega_1 - \omega_2) \tag{A.8}$$

$$\frac{3\alpha_3 A_1^2 A_2}{4} \cos(2\omega_1 + \omega_2) + \frac{3\alpha_3 A_1^2 A_2}{4} \cos(2\omega_1 - \omega_2) \tag{A.9}$$

$$\frac{3\alpha_3 A_1 A_2^2}{4} \cos(2\omega_2 + \omega_1) + \frac{3\alpha_3 A_1 A_2^2}{4} \cos(2\omega_2 - \omega_1) \tag{A.10}$$

Equation (A.8) displays the second-order terms that form the basis for mixers. Letting $\omega_1 < \omega_2$ and defining $\Delta\omega = \omega_2 - \omega_1$, then the latter third-order terms in Eqs. (A.9)&(A.10) become:

$$\frac{3\alpha_3 A_1^2 A_2}{4} \cos(\omega_1 - \Delta\omega) + \frac{3\alpha_3 A_1 A_2^2}{4} \cos(\omega_2 + \Delta\omega) \tag{A.11}$$

The equations now reveal that these two intermodulation products occur in close proximity to the fundamental harmonics and are thus difficult to filter out. Signal deterioration due to intermodulation can be parameterized by plotting the desired

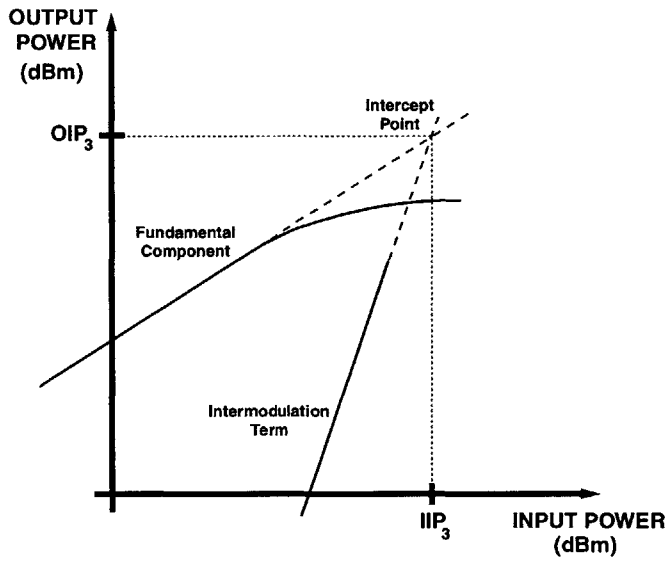


Figure A-2: Graphical definition of third–order input intercept point.

signal power and third-order product's power levels versus RF input levels. Figure A-2 displays the general appearance of such a plot. From Eqs. (A.9)&(A.10) we see that the third-order intermodulation terms are proportional to A^3 while the fundamental increases linearly with A. On a logarithmic plot, this translates into an IM_3 slope of three times larger than the fundamental. If the lines are extrapolated out to a common intercept, one can determine the mathematical input level at which the desired signal and the intermodulation products are equal; this input level is defined as the *third–order input intercept point* (IIP_3). Note that as one tries to approach the extrapolated IIP_3, gain compression due to previously ignored higher–order terms contribute to lower the actual gain of the circuit. (In many circuits the IIP_3 value is beyond the maximum operating levels specified by a manufacturer.) Thus the IIP_3 value is considered a low–level measure of linearity while the 1–dB compression point conveys an actual upper-level boundary.

The most common case of RF signal corruption attributed to intermodulation is displayed in Figure A-3 [13]. When nearby interferers accompany a weak desired signal through a nonlinear system (such as an amplifier), the third order intermodulation products of the two interferers will fall into the desired channel. Due to

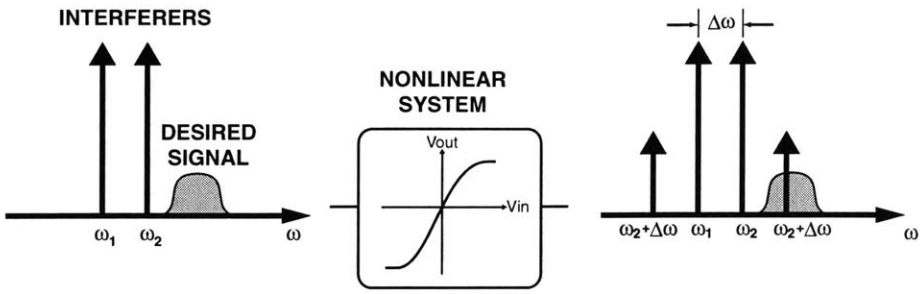


Figure A-3: Signal corruption due to intermodulation.

the prevalence of adjacent channel interferers that can undergo this phenomena, the third–order intercept point has become an important measure of linearity.

A.1.4 Cascaded IIP_3 Calculation

Given the IIP_3 of each block in a RF chain, it is desirable to know what the equivalent cascaded value is. Qualitatively, one would expect the equivalent IIP_3 to decrease with high gain early in the chain. High gain in the first stage translates into larger input levels for the second stage, which in turn will produce larger intermodulation terms. When referenced to the input, this results in a lowering of the equivalent IIP_3 level. Thus the linearity of elements later in a chain becomes much more critical than the earlier elements because their individual IIP_3 values are effectively scaled down by the preceding gain. If we let the n-th stage's IIP_3 level in volts be equal to $A_{IIP_3,n}$ and the small–signal gain be equal to G_n, then it is found that the cascaded system third–order input intercept point adheres to the following approximate relationship:

$$\frac{1}{A^2_{IIP_3,total}} \approx \frac{1}{A^2_{IIP_3,1}} + \frac{G_1^2}{A^2_{IIP_3,2}} + \frac{G_1^2 G_2^2}{A^2_{IIP_3,3}} + \cdots \tag{A.12}$$

A.2 Noise

An important performance metric of a wireless system is the smallest amplitude signal a receiver can process and recover reliably. A key source of error in this goal is random *noise*. The exact definition of noise varies from author to author. While some consider

signals such as power supply hum or cross-coupling of signals as noise, these forms of unwanted signals can theoretically be removed through careful design and layout. Noise, as referred to throughout this thesis, includes only those undesirable signals uncorrelated to the signal of interest that are fundamental in nature and cannot be wholly eliminated.

Whether external (atmospheric noise) or internal (thermal) to the system, noise analysis is a critical aspect of modern wireless communications systems. The field of noise, and more generally stochastics, is a long studied and well documented area of research. For our purposes, a formal introduction will be deferred to any of a number of classical texts. Rather, this section will address the issues and definitions relevant for a discrete RF design. In particular, a few generators of noise will be presented as well as the concept of *noise figure.*

A.2.1 Sources of Noise

The most common source of noise in all circuits is thermal noise. Thermal noise (or Johnson noise) results from the random Brownian motion of charged particles through a resistance. Being fundamental to the system, thermal noise can be reduced but cannot be entirely removed. In RF circuits, thermal noise is attributed to resistors, to base and emitter resistances in bipolar devices, and to channel resistance in a MOSFET. Shot noise is another common source of noise in active devices that results from the discrete, quantum nature of current. Shot noise results from the random flow of electrons across an energy barrier in a conductor. The effect of each electron's energy transition is to induce a current impulse that contributes to the shot noise. Another important type of noise is flicker noise. Flicker noise is found in all active devices as well as some passive elements. While not fully understood fundamentally, flicker noise in transistors is attributed to the random trappings of electrons at the oxide–silicon interface for MOSFETS; for bipoloar devices, the trappings occur within the emitter-base depletion layer and at the oxide isolation areas. Unlike the previous two examples of noise, flicker noise exhibits a noise density that is inversely proportional to frequency (and is sometimes referred to as $1/f$ noise). A fourth type

of noise is burst noise (or popcorn noise). Again little is known about this source of noise; it is conjectured that it is to some extent due to metal imperfections within the lattice. A unique feature of this type of noise is that it exhibits a multi–modal, non-Gaussian amplitude distribution that causes particles to randomly jump between discrete values.

Among the four, thermal noise is proportional to temperature but is unaffected by current. Thus thermal noise may be reduced by lowering device temperatures. Shot noise, in comparison, is independent of temperature and always associated with direct–current flow. Both types of noise, however, do exhibit similar, *white* spectral densities that are constants as a function of frequency. Flicker noise can be seen in carbon composite resistors, however it only exists if there is a direct–current flow through the device. Thus carbon resistors may be used in low frequency, low noise applications if it only carries an alternating current. If bias currents must flow through a resistor, metal film resistors are the optimum choice since they do not produce flicker noise.

For a much more in depth analysis of the various noise sources in analog circuits, see the following references: [22, 23, 24]

A.2.2 Noise Factor and Noise Figure

The noise performance of front–end RF blocks are generally characterized with a *noise factor*(F) or *noise figure*(NF). Noise figure is calculated by converting the noise factor into decibels: $10\log_{10}$(noise factor). The IEEE definition for noise factor can be stated as [25]:

$$\text{noise factor (F)} = \frac{\text{available output noise power}}{\text{available output noise due to the source}} \tag{A.13}$$

By algebraic manipulation, Eq. (A.13) can be rearranged into the following common form,

$$\text{noise factor} = \frac{SNR_{in}}{SNR_{out}} \tag{A.14}$$

Noise factor is a measure of how much the signal–to–noise ratio (SNR) degrades due to noise added by the device. The importance of noise figure is that it limits how small a received signal can be and still be recovered reliably. One salient point must be pointed out: in a practical system, since noise factor is always greater than 1, the output signal–to–noise ratio is always less that the signal–to–noise ratio at the input. However, this is generally not the case in actual receivers. The contradiction stems from the definition of noise factor. In practice, receivers employ filters to reduce the input noise power; since the formulation of noise factor uses the same bandwidth in determining both SNR values, noise factor will not reflect the filtering. Noise factor also doesn't take into account noise additions due to spurious signals or image noise.

A.2.3 Cascade Noise Figure Calculation

Similar to determining an overall IIP_3 for a system, it is likewise beneficial to determine the overall noise figure for a chain of cascaded blocks. A formulation of system noise factor is given by the Friis equation:

$$F_{total} = 1 + (F_1 - 1) + \frac{F_2 - 1}{A_{p1}} + \cdots + \frac{F_m - 1}{A_{p1} \cdots A_{p(m-1)}} \tag{A.15}$$

where F_i is the noise factor of the *i-th* stage calculated with respect to the source impedance driving that stage, and $A_{p(i)}$ is the *available power gain.* Available power gain is defined as the ratio of the output power into a conjugate–matched load to the source power available to a conjugate–matched circuit. Qualitatively, the Friis equation reveals that the noise factor, and consequently the noise figure, of an individual element is scaled down by the gain preceding it. This makes sense because the noise performance in the first stage ripples down the chain and is amplified by the following stages' gains. The noise contributed by latter stages is less significant when compared to this first term; hence when referenced back to the input the noise figure of the latter stages is scaled down. If a stage exhibits loss (perhaps a filter or passive mixer), then the gain is less than 1 and the following noise figure is amplified by the loss. The key point is that the system noise figure relies heavily on the first

few elements in the signal chain.

A.3 Intersymbol Interference

Another source of signal corruption is due to intersymbol interference (ISI) in a bandwidth limited system. This effect is due to the fact that a signal can not be both time and bandwidth limited. In a digital transmission system, ISI causes a temporal spreading of the data pulses. Large amounts of ISI lead to an overlapping of the individual pulses such that the receiver cannot accurately discern between changes in state. Figure A-4 presents examples of both slight and severe ISI. The first system shows a swift step response that indicates that it has adequate bandwidth. A pulse train applied to the first system is able to pass through without much ISI. The eye diagram gives a visual indication of how the band-limited stream looks and interacts over time. In the second system we see that the rise time is slow relative to the period of a bit; the resulting output waveform shows a large amount of overlap and distor-

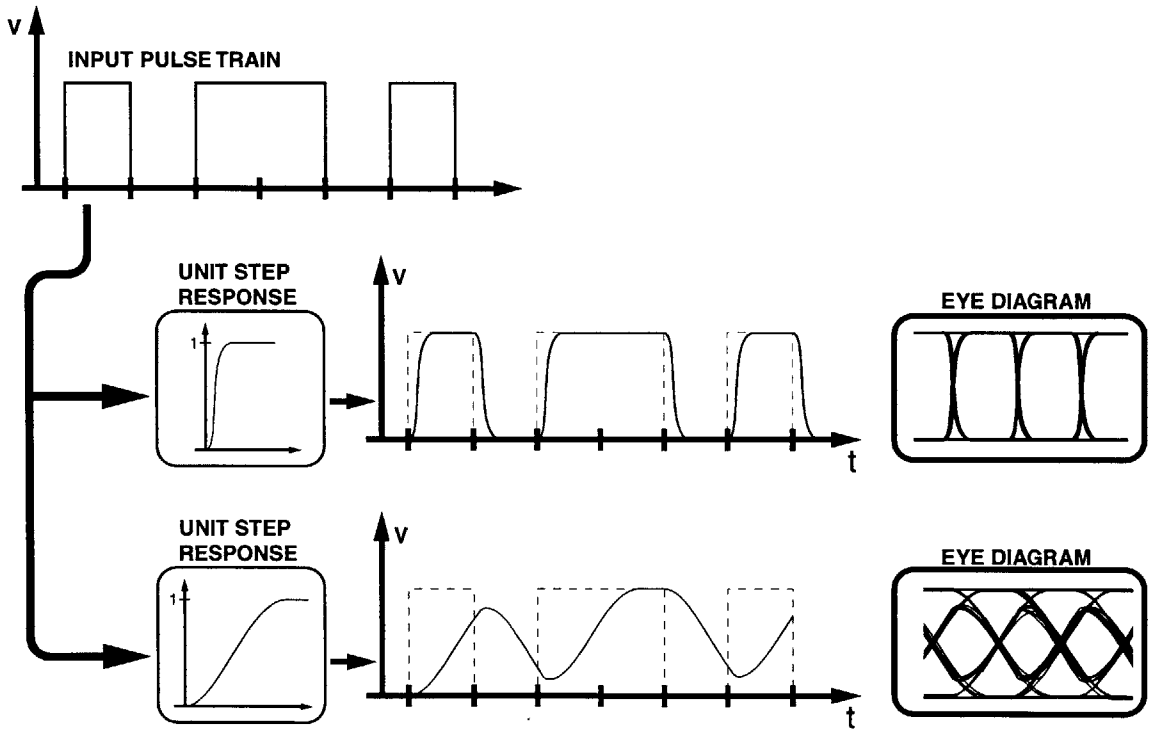


Figure A-4: Effects of intersymbol interference.

tion. The eye diagram reveals not only a *closing eye* but also *pseudo-levels* caused by the slowly decaying pulse tails. Both will result in a much lower probability of accurate data recovery.

In RF systems, ISI is such a problem that a number of techniques have been developed to reduce it. Pulse shaping, or Nyquist signaling, can be employed in the transmitter to minimize the effects of pulse tails, while receivers commonly employ adaptive *equalization* schemes to compensate for ISI. Further information on handling ISI as well as other forms of signal deterioration can be found in [26, 19].

A.4 System Metrics

A.4.1 Bit Error Rate

In a digital wireless communications system, we are interested in the SNR of the detector output in response to noise and other types of unwanted signals. By maximizing the signal quality, other variables such as transmitter power and signal range can be optimized without compromising communication accuracy. The quality of a digital modulation scheme can be quantified via a *bit error rate* (BER). Bit error rate is defined as the average number of erroneous bits divided by the total number of bits transmitted, received, or processed over some stipulated period. In a receiver, the BER relays information regarding the detector and its decision making ability in the presence of noise. Via probability theory, BER can be calculated solely as a function of signal-to-noise ratio or more commonly as a function of signal energy to noise spectral density ratio [26, 19].

A.4.2 Sensitivity

The sensitivity of a communications receiver is defined as the minimum signal level that can be detected with a given signal-to-noise ratio. In the previous section it was mentioned that BER and SNR are closely related; sensitivity in a digital system can thus be redefined as the minimum signal level that can be detected for a given BER.

A quantitative expression for sensitivity can be obtained by rearranging the equation for noise figure. Realizing that SNR_{in} is equal to the ratio of input signal power (P_{sig}) to the source resistance noise power (P_{RS}), Eq. (A.14) can be rearranged into:

$$P_{sig} = P_{RS} \cdot NF \cdot SNR_{out} \tag{A.16}$$

Since the total signal power is distributed over the channel, both sides of Eq. (A.16) must be integrated over the channel. Letting the channel bandwidth in Hertz be equal to (B) and converting values to decibels, we obtain the following:

$$P_{sig,min} = P_{RS}|_{dBm/Hz} + NF|_{dB} + SNR_{min}|_{dB} + 10\log(B) \tag{A.17}$$

where $P_{sig,min}$ is the minimum input power commensurate with the allowable SNR_{min}. Finally, assuming conjugate matching at the input and room temperature conditions, $P_{RS} = kT$, and Eq. (A.17) simplifies to,

$$P_{sig,min}\ (S) = \underbrace{-174\ dBm/Hz + NF|_{dB} + 10\log(B)}_{noise\ floor} + SNR_{min}|_{dB} \tag{A.18}$$

The *noise floor* signifies the total integrated noise of the system. In this form, Eq. (A.18) can be readily used to determine the maximum noise figure a system can have for a given sensitivity and BER.

A.4.3 Spurious–Free Dynamic Range

The minimum detectable signal (sensitivity) was determined in the previous section to be dependent on the input thermal noise and the noise added to the signal by the receiver, as indicated by the noise figure. On the other end, distortion due to intermodulation and compression limit how large a signal can be. What exactly constitutes *too much* distortion varies. One approach defines the upper limit as the input level such that the third–order intermodulation products in a two–tone test are equal to the noise floor. This definition is referred to as the *spurious–free dynamic*

range (SFDR) [13]. Qualitatively, the SFDR reveals how large interferers may be and still allow the receiver to recover information with suitable signal quality

Based on the definition given, the intermodulation levels equal the noise floor when:

$$P_{in,max} = \frac{2P_{IIP_3} + noise\ floor}{3} \tag{A.19}$$

where noise floor is defined as indicated in Eq. (A.18). By combining Eqs. (A.18) & (A.19), the SFDR is found to be,

$$\begin{aligned} SFDR &= P_{in,max} - P_{sig,min} && \text{(A.20)} \\ &= \left(\frac{2P_{IIP_3} + noise\ floor}{3}\right) - (noise\ floor + SNR_{min}) && \text{(A.21)} \\ &= \frac{2}{3}(P_{IIP_3} - noise\ floor) - SNR_{min} && \text{(A.22)} \end{aligned}$$

Appendix B

LPE–Base: Schematics, Board Layout, & Parts List

- Schematics: Figures B-1 – B-9
- Board Layout: Figures B-10 – B-13
- Parts List: Table B.1

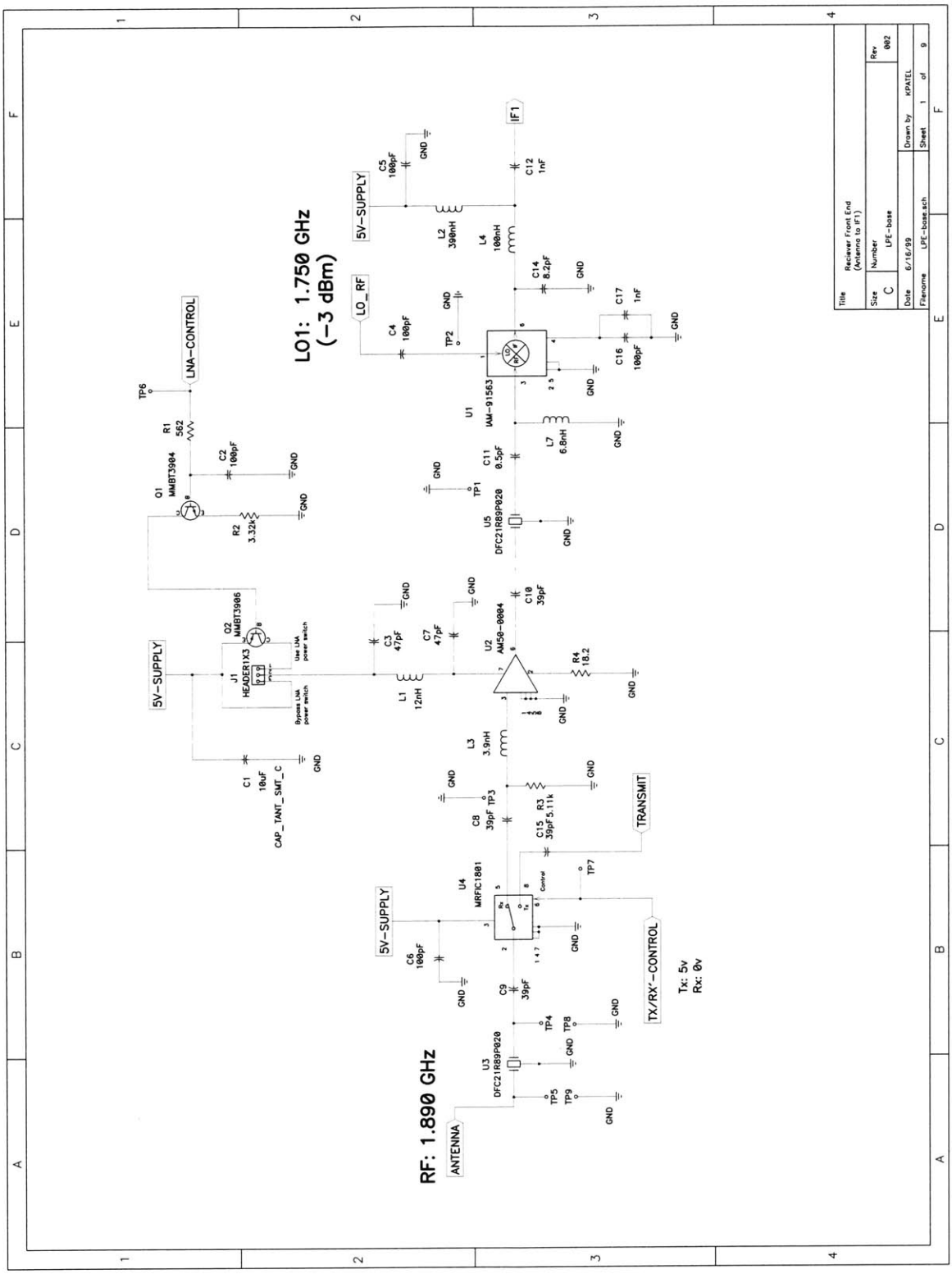


Figure B-1: LPE–Base Schematic: Receiver Front End (Antenna to IF1).

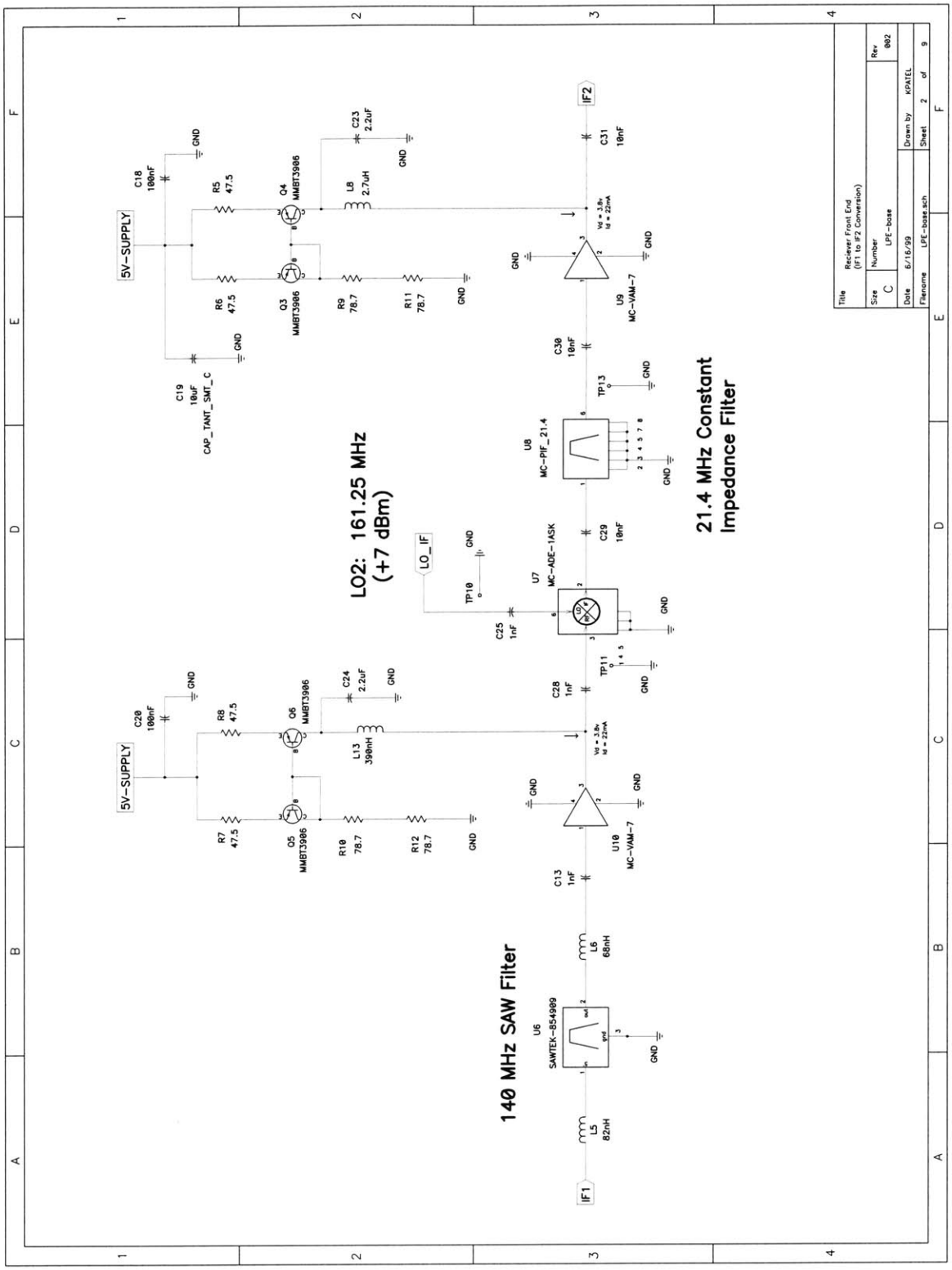


Figure B-2: LPE–Base Schematic: Receiver Front End (IF1 to IF2 Conversion).

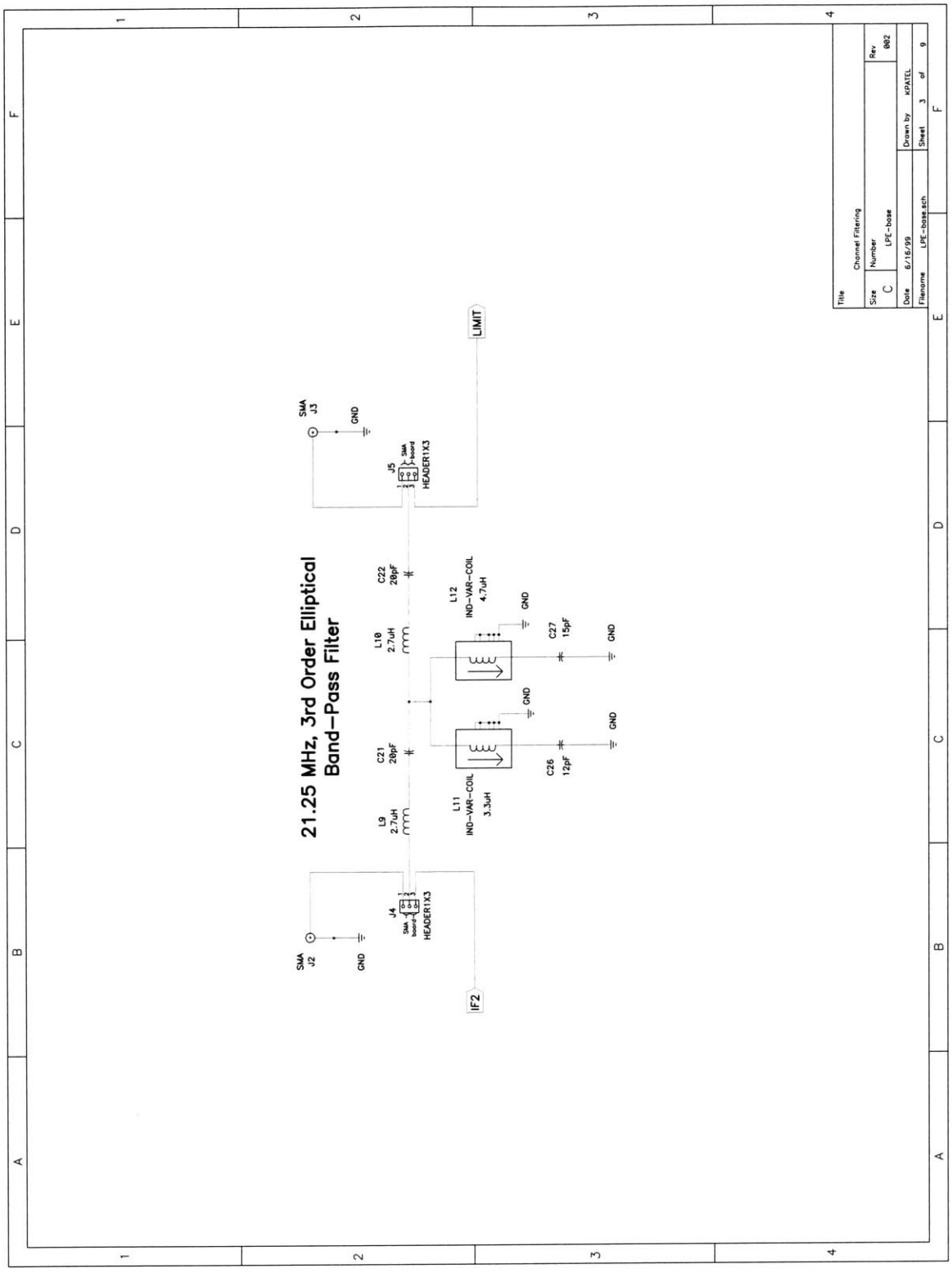


Figure B-3: LPE–Base Schematic: Channel Filtering.

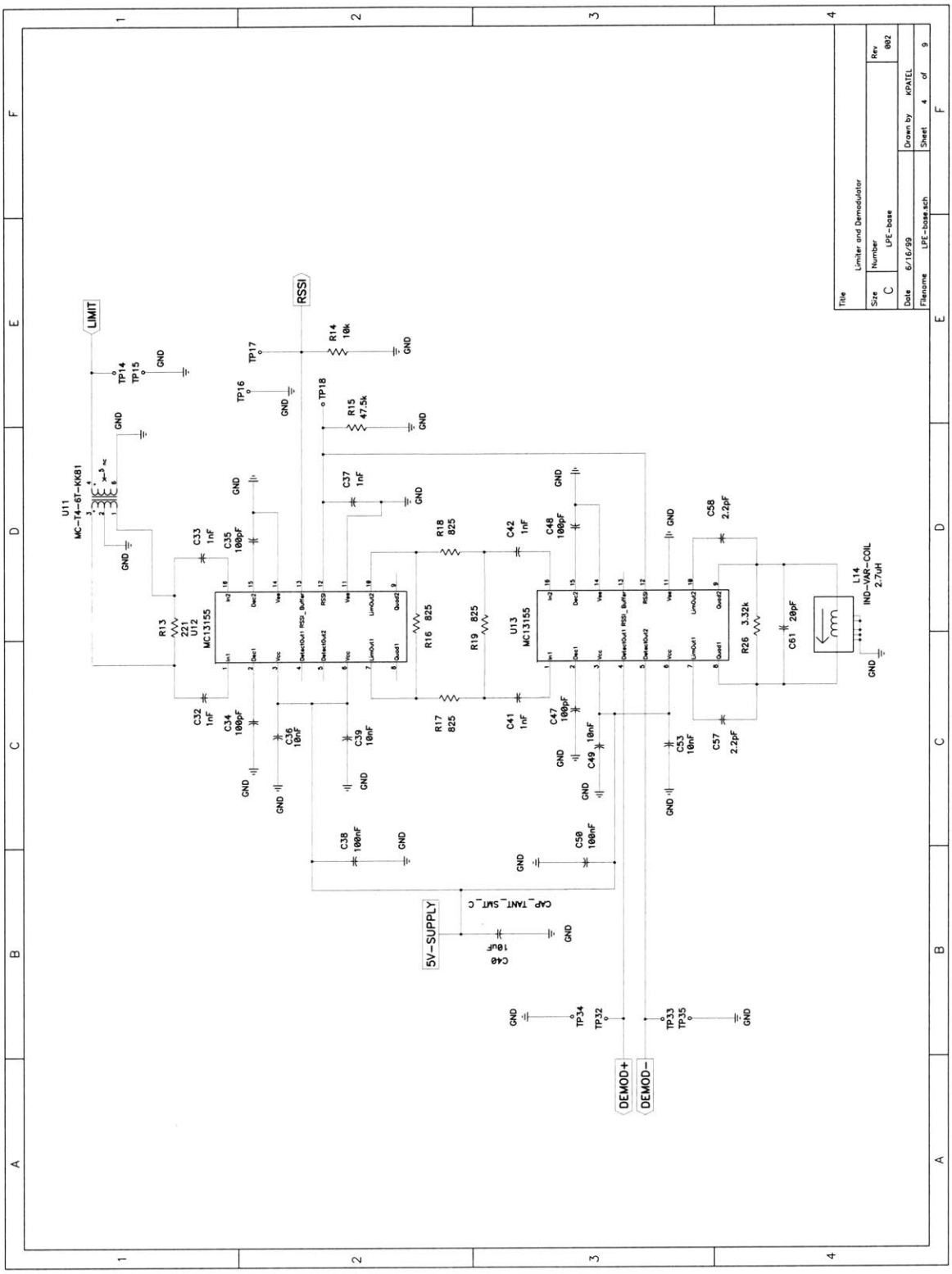


Figure B-4: LPE–Base Schematic: Limiter and Demodulator.

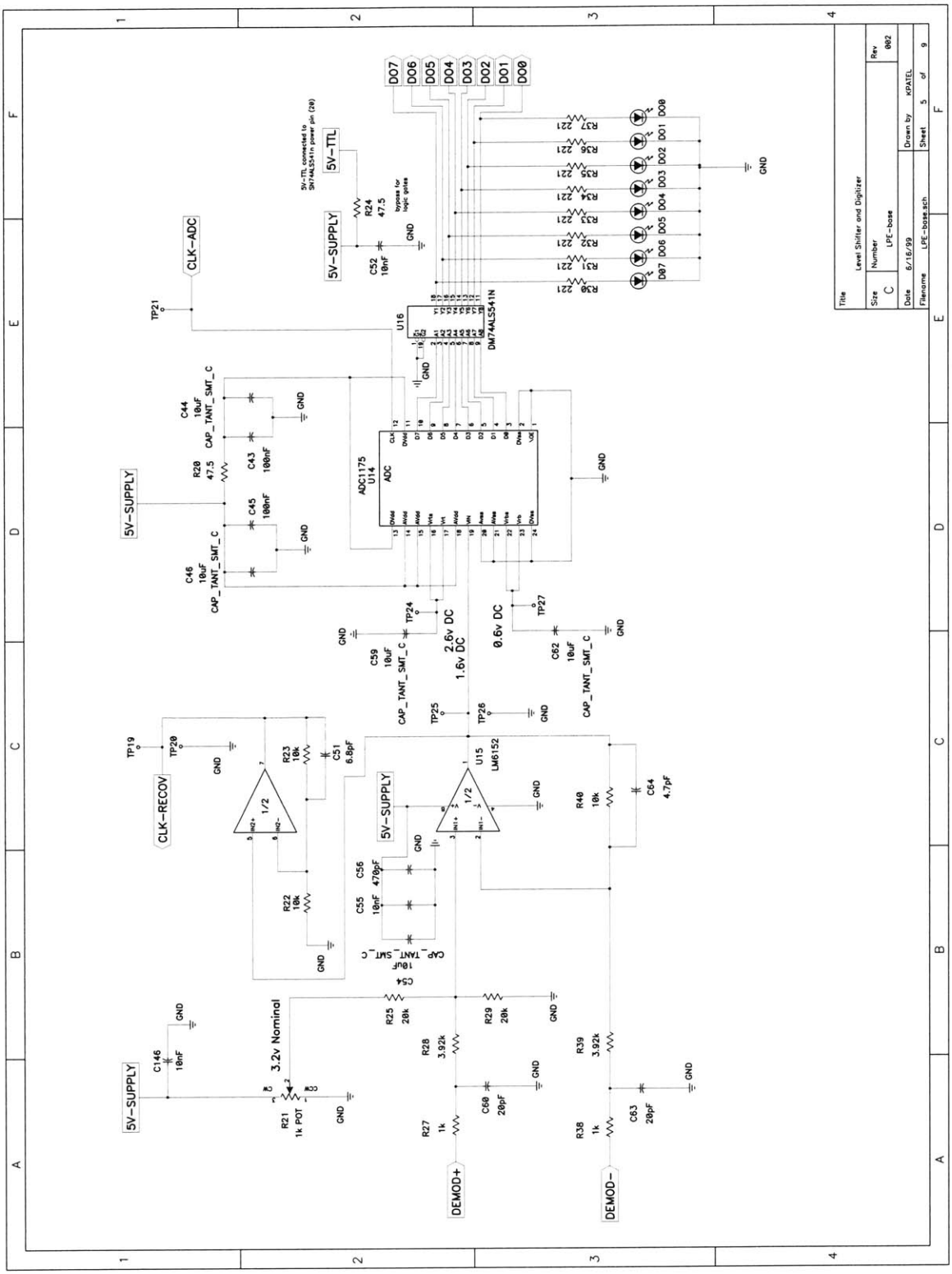


Figure B-5: LPE–Base Schematic: Level Shifter and Digitizer.

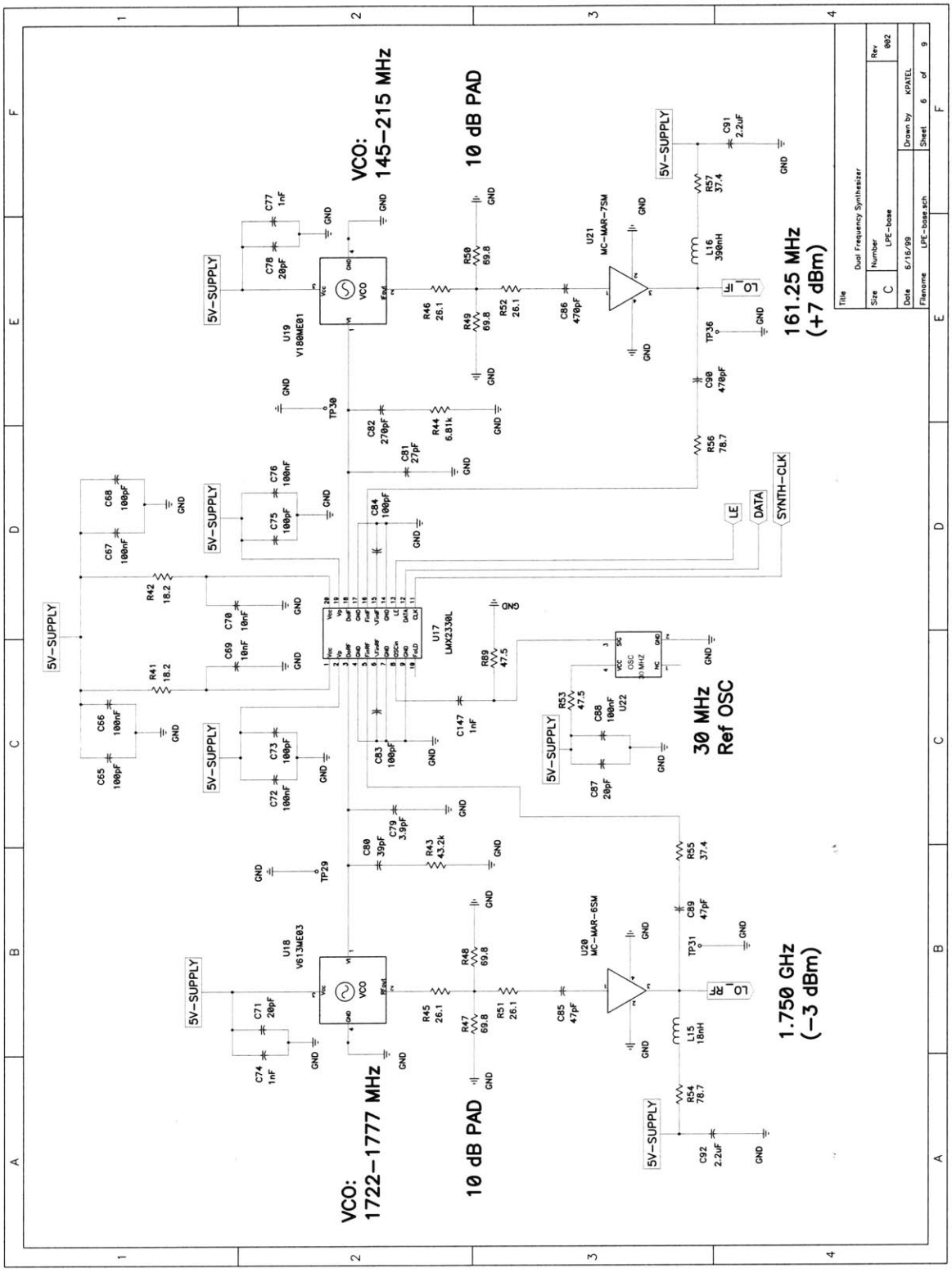


Figure B-6: LPE–Base Schematic: Dual Frequency Synthesizer.

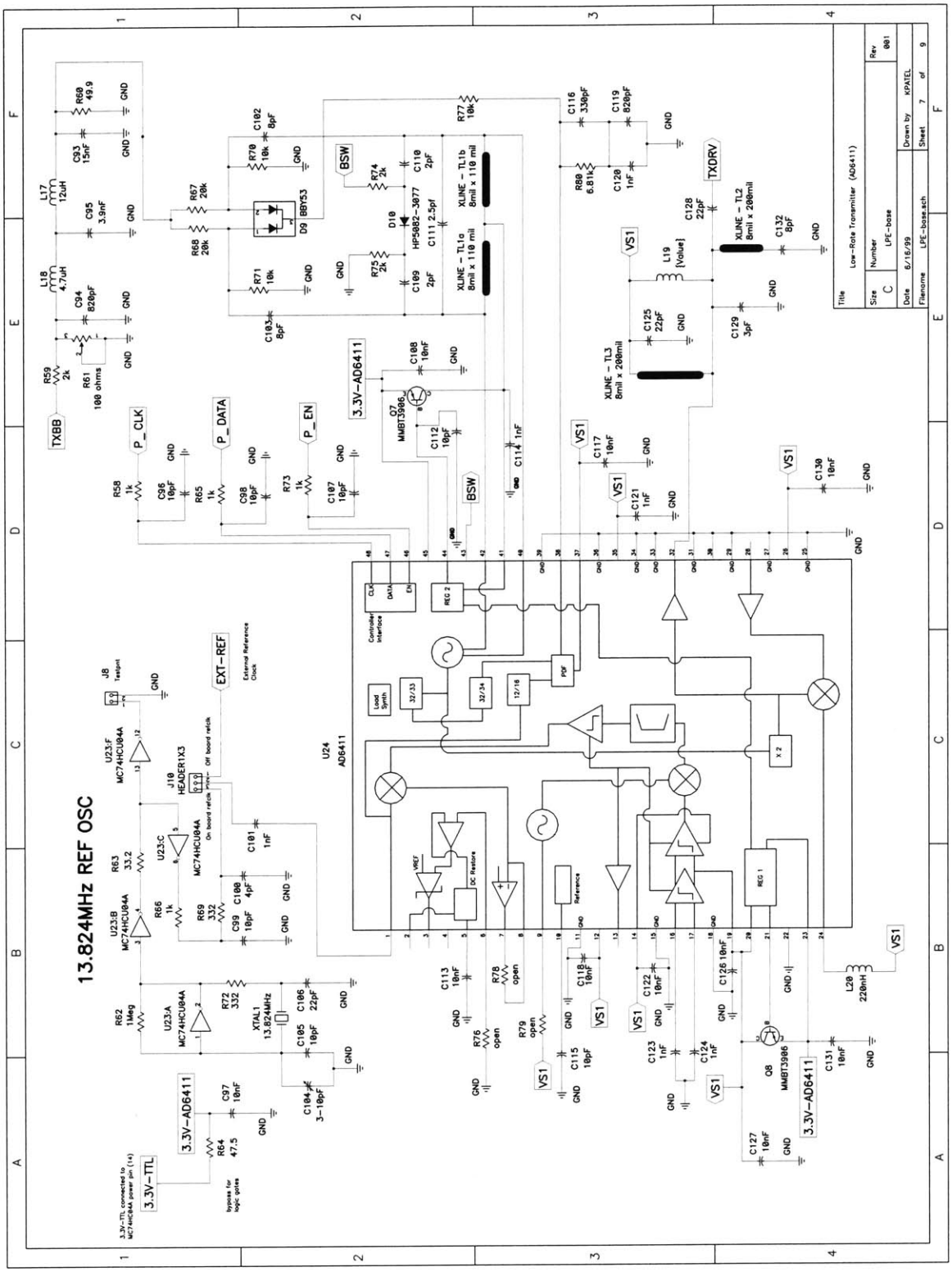


Figure B-7: LPE–Base Schematic: Low–Rate Transmitter (AD6411).

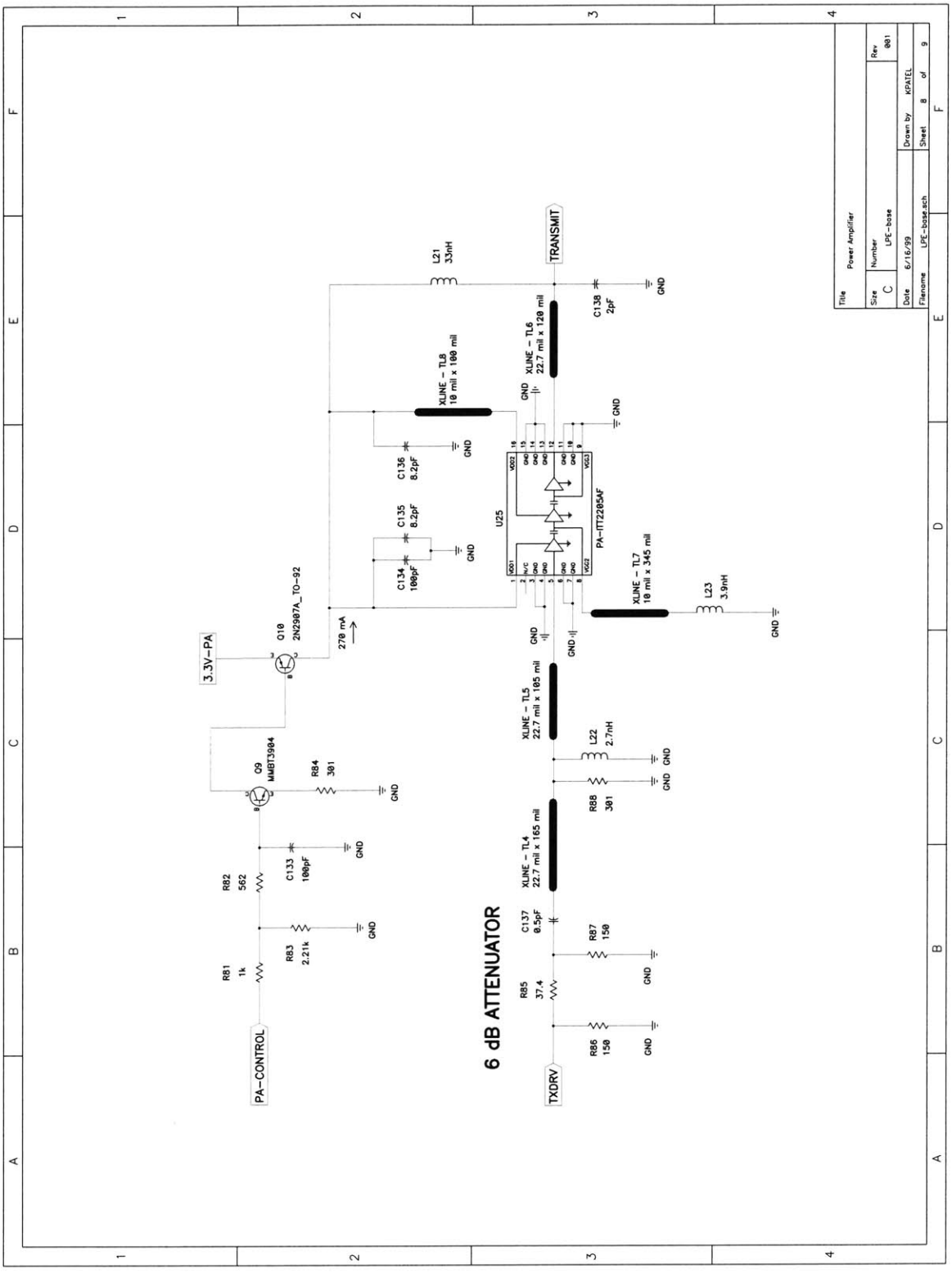


Figure B-8: LPE–Base Schematic: Power Amplifier.

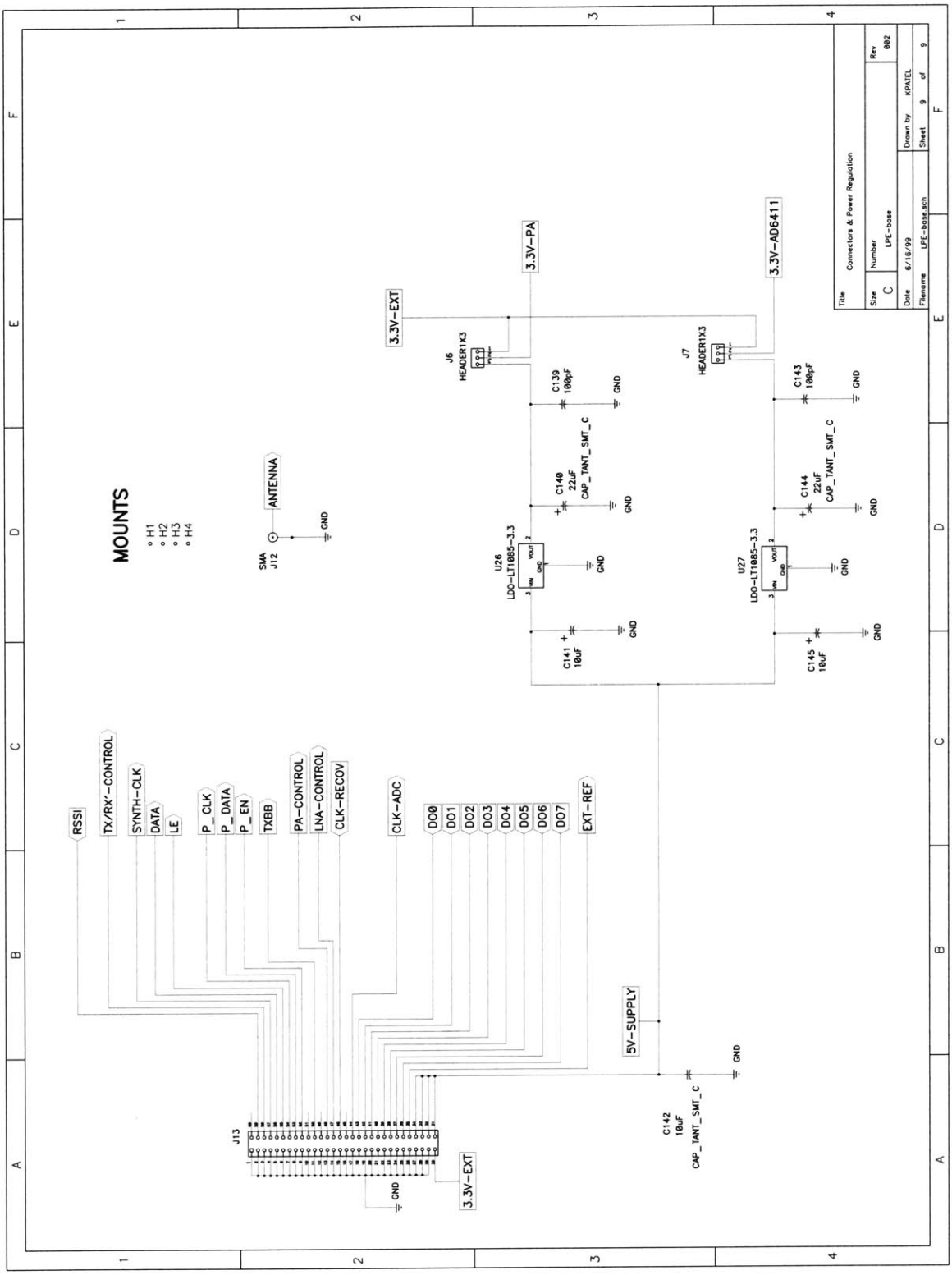


Figure B-9: LPE–Base Schematic: Connectors and Power Regulation.

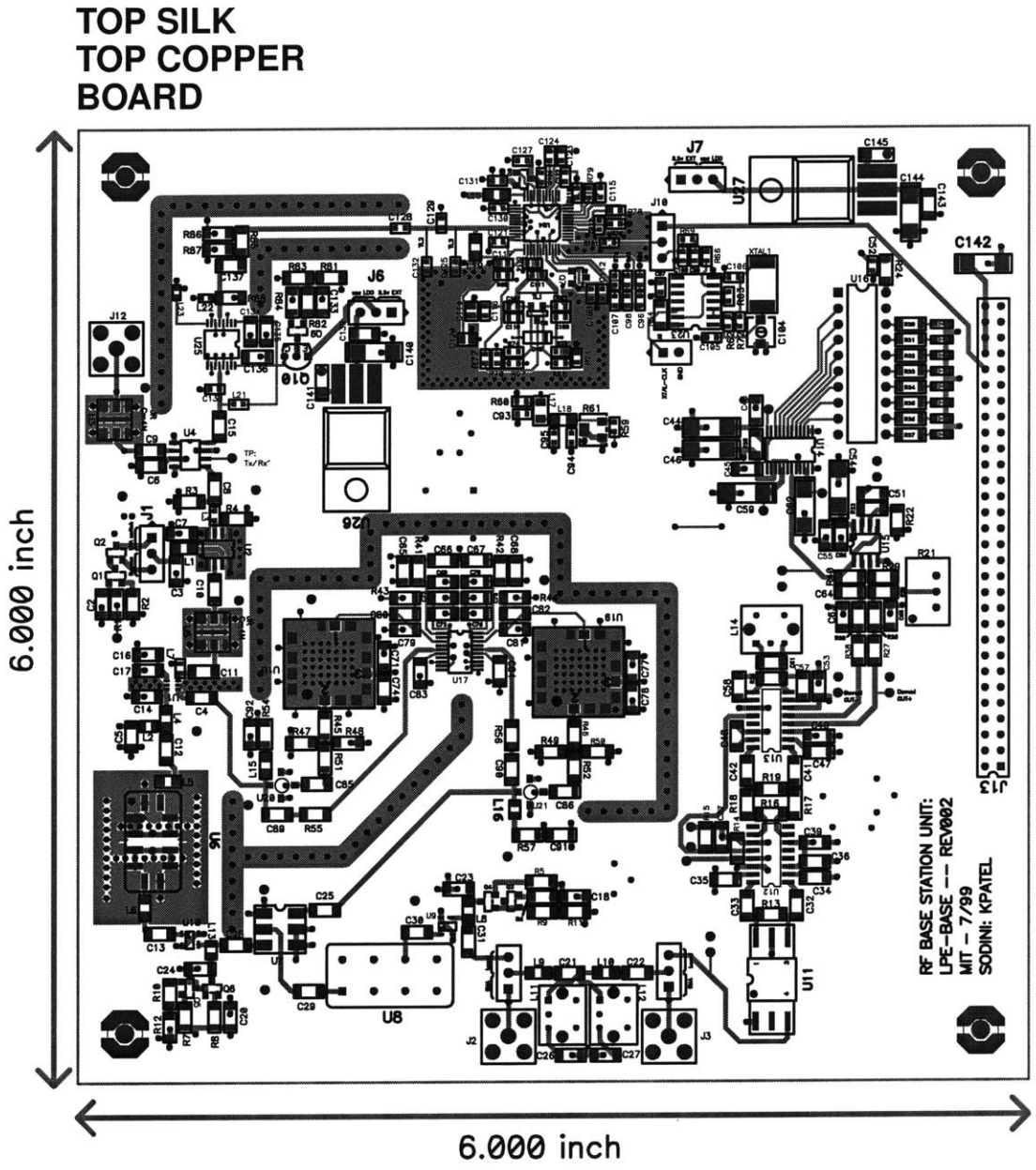


Figure B-10: LPE–Base Layout: Layer 1.

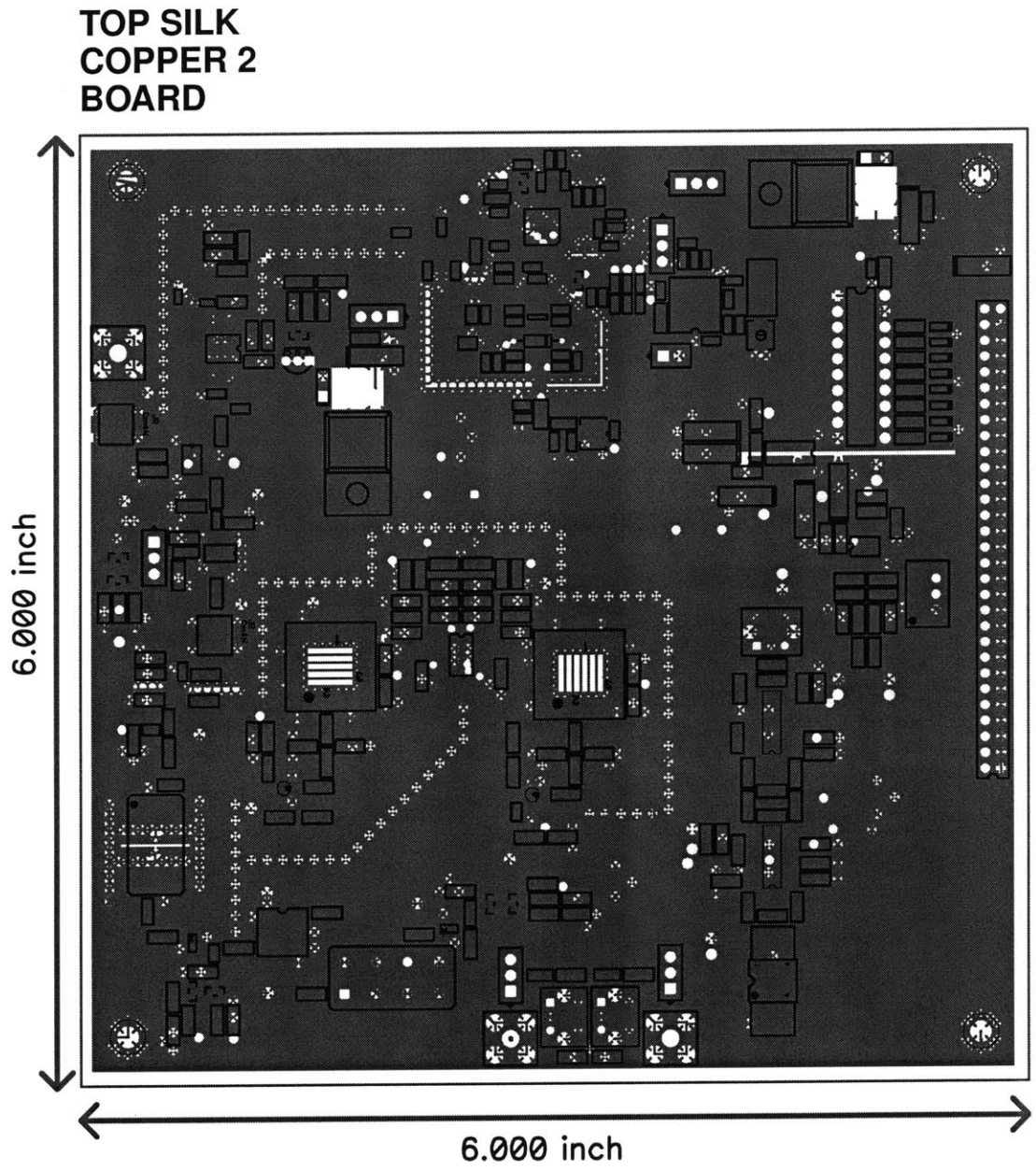


Figure B-11: LPE–Base Layout: Layer 2.

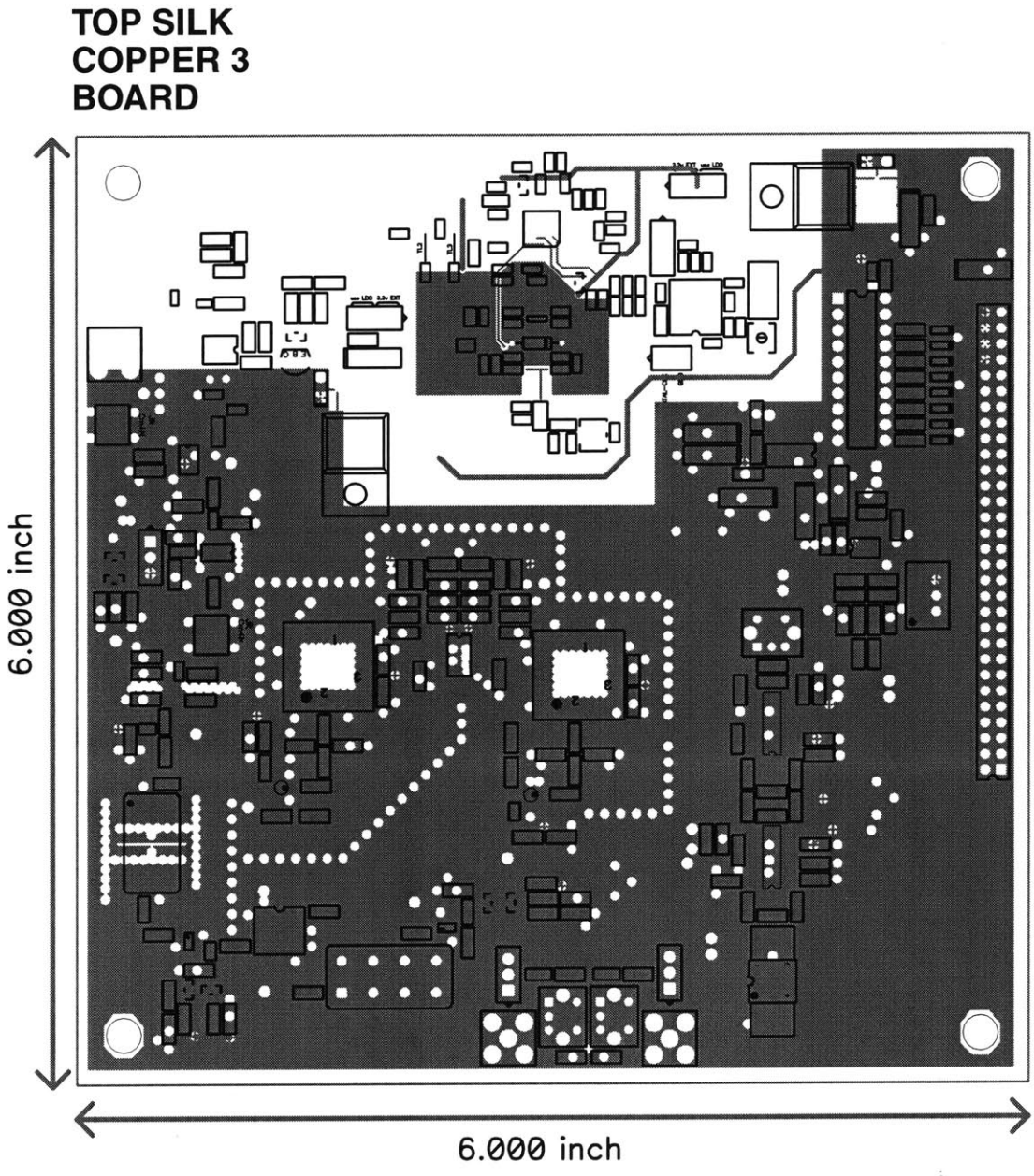


Figure B-12: LPE–Base Layout: Layer 3.

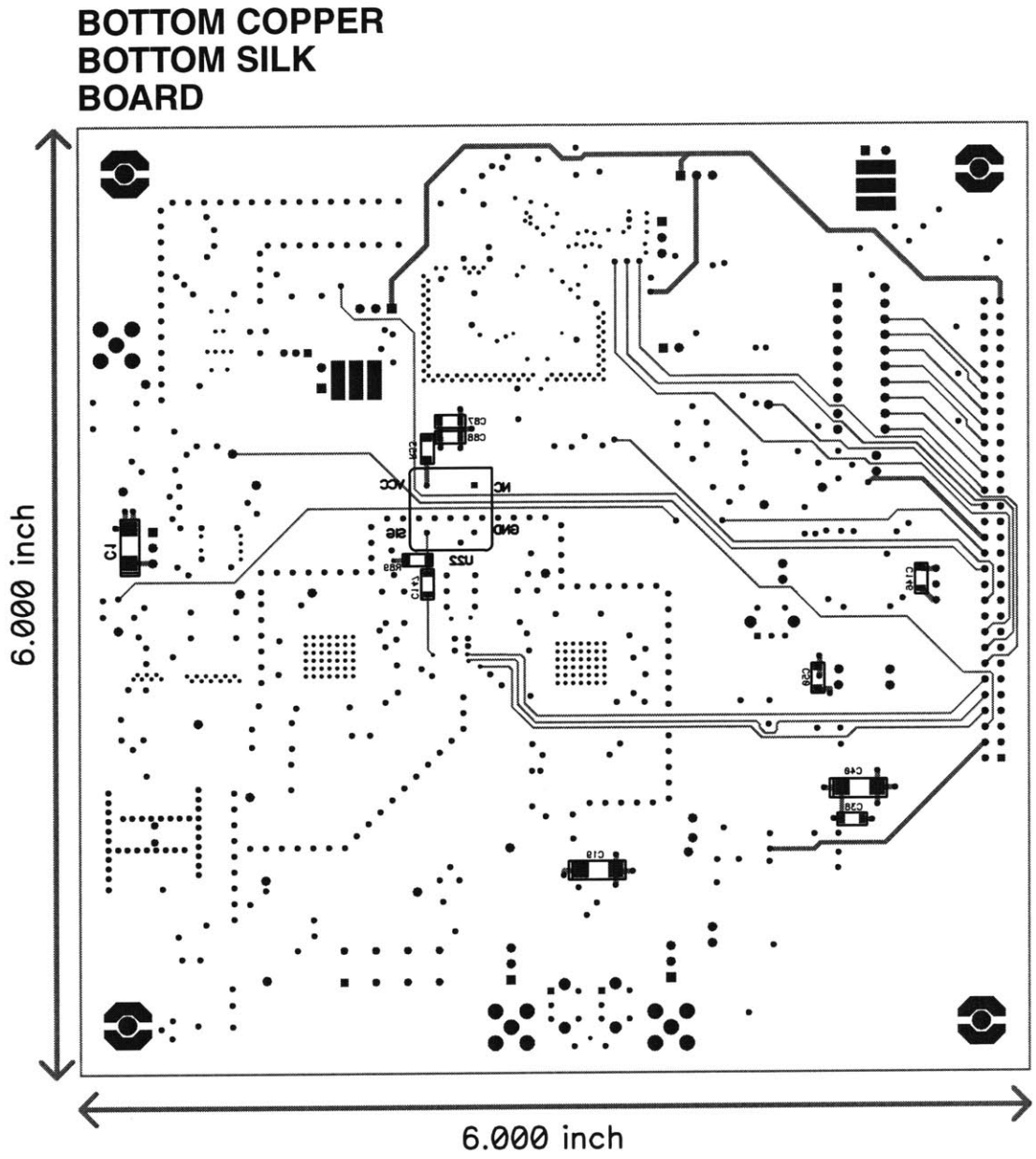


Figure B-13: LPE–Base Layout: Layer 4.

Table B.1: Bill of Materials: LPE–Base

BILL OF MATERIALS: LPE–BASE				
Quantity	**Ref Des**	**Part Number**	**Description**	**Company**
1	U1	HP IAM–91563	RF mixer	Hewlett Packard
1	U2	AM50–0004	LNA	MACOM
2	U3,U5	DFC21R89P020 HHE	ceramic filter	Murata
1	U4	MRFIC1801	Tx/Rx switch	Motorola
1	U6	SAWTEK–854909	SAW filter	Sawtek
1	U7	ADE–1ASK	IF mixer	Mini–Circuits
1	U8	PIF_ 21.4	constant Z filter	Mini–Circuits
2	U9,U10	VAM–7	amplifier	Mini–Circuits
1	U11	T4–6T–KK81	4:1 transformer	Mini–Circuits
2	U12,U13	MC13155D	FM limiter/demod	Motorola
1	U14	ADC1175 CIMTC	ADC	National Semi.
1	U15	LM6152 AC	I/O op-amp	National Semi.
1	U16	DM74ALS541N	octal buffer	Digi–Key
1	U17	LMX2330L TM	dual freq synth	National Semi.
1	U18	V613ME03	VCO–RF	Z–Comm
1	U19	V180ME01	VCO–IF	Z–Comm
1	U20	MAR–6SM	amplifier	Mini–Circuits
1	U21	MAR–7SM	amplifier	Mini–Circuits
1	U22	520–TCH3000	30 MHz oscillator	Mouser
1	U23	MC74HCU04a	hex unbuf. inv.	Motorola (Arrow)
1	U24	AD6411	DECT IC	Analog Devices
1	U25	ITT2205AF	power amplifier	GaAsTEK
2	U26,U27	LT1085CT–3.3	3.3V LDO	Digi–Key
1	XTAL1	CRYSTAL [CX–1–SM]	13.824 MHz crystal	Statek
8	D1,D2,D3,D4,D5, D6,D7,D8	P524 CT–ND	LED: red	Digi–Key
1	D9	BBY53	dual varactor	Siemens
1	D10	HP 5082–3077	switching diode	HP (Arrow)
2	Q1,Q9	MMBT3904 DICT–ND	NPN transistor	Digi–Key
7	Q2,Q3,Q4,Q5,Q6, Q7,Q8	MMBT3906 DICT–ND	PNP transistor	Digi–Key
1	Q9	PN2907A–ND	PNP (through hole)	Digi–Key
1	J12	ARFX1232	right angle SMA	Digi–Key
2	J2,J3	PE4117	top connect SMA	Pasternack
1	J13	MHD60K	60 pin header	Digi–Key

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Quantity	Ref Des	Part Number	Description	Company
1	L22	PCD1269 CT-ND [0402]	2.7nH inductor (10%)	Digi-Key
1	L23	PCD1271 CT-ND [0402]	3.9nH inductor (10%)	Digi-Key
1	L1	PCD1185 CT-ND [0805]	12nH inductor (5%)	Digi-Key
1	L15	PCD1163 CT-ND [0805]	18nH inductor (10%)	Digi-Key
1	L6	PCD1170 CT-ND [0805]	68nH inductor (5%)	Digi-Key
1	L5	PCD1171 CT-ND [0805]	82nH inductor (5%)	Digi-Key
1	L4	PCD1172 CT-ND [0805]	100nH inductor (5%)	Digi-Key
1	L20	PCD1176 CT-ND [0805]	220nH inductor (5%)	Digi-Key
3	L8,L9,L10	PCD1192 CT-ND [0805]	2.7μH inductor (10%)	Digi-Key
1	L18	PCD1195 CT-ND [0805]	4.7μH inductor (10%)	Digi-Key
1	L17	PCD1241 CT-ND [1008]	12μH inductor (5%)	Digi-Key
3	L2,L13,L16	TKS2393 CT-ND [0805]	390nH inductor (5%)	Digi-Key
1	L3	0603CS-3N9X_BC [0603]	3.9nH inductor (5%)	Coilcraft
1	L7	0603CS-6N8X_BC [0603]	6.8nH inductor (5%)	Coilcraft
1	L21	0603CS-33NX_BC [0603]	33nH inductor (5%)	Coilcraft
1	L14	7M3-272 [slot seven]	2.7μH variable inductor	Coilcraft
1	L11	7M3-332 [slot seven]	3.3μH variable inductor	Coilcraft
1	L12	7M3-472 [slot seven]	4.7μH variable inductor	Coilcraft
3	R76,R78,R79	[smt 0603]	open circuits	
1	R21	3299W-102-ND	1kΩ POT: top adjust	Digi-Key
1	R61	3214W-101ECT-ND	100Ω POT: top adjust	Digi-Key
1	R63	P33.2H CT-ND [0603]	33.2Ω resistor (1%, $\frac{1}{16}$W)	Digi-Key
1	R60	P49.9H CT-ND [0603]	49.9Ω resistor (1%, $\frac{1}{16}$W)	Digi-Key
2	R69,R72	P332H CT-ND [0603]	332Ω resistor (1%, $\frac{1}{16}$W)	Digi-Key
4	R58,R65,R66,R73	P1.00KH CT-ND [0603]	1.00kΩ resistor (1%, $\frac{1}{16}$W)	Digi-Key
3	R59,R74,R75	P2.00KH CT-ND [0603]	2.00kΩ resistor (1%, $\frac{1}{16}$W)	Digi-Key
1	R80	P6.81KH CT-ND [0603]	6.81kΩ resistor (1%, $\frac{1}{16}$W)	Digi-Key
3	R70,R71,R77	P10.0KH CT-ND [0603]	10.0kΩ resistor (1%, $\frac{1}{16}$W)	Digi-Key
2	R67,R68	P20.0KH CT-ND [0603]	20.0kΩ resistor (1%, $\frac{1}{16}$W)	Digi-Key
1	R62	P1.00MH CT-ND [0603]	1.00MΩ resistor (1%, $\frac{1}{16}$W)	Digi-Key
3	R4,R41,R42	P18.2F CT-ND [1206]	18.2Ω resistor (1%, $\frac{1}{8}$W)	Digi-Key
4	R45,R46,R51,R52	P26.1F CT-ND [1206]	26.1Ω resistor (1%, $\frac{1}{8}$W)	Digi-Key
3	R55.R57,R85	P37.4F CT-ND [1206]	37.4Ω resistor (1%, $\frac{1}{8}$W)	Digi-Key
9	R5,R6,R7,R8,R20, R24,R53,R64,R89	P47.5F CT-ND [1206]	47.5Ω resistor (1%, $\frac{1}{8}$W)	Digi-Key
4	R47,R48,R49,R50	P69.8F CT-ND [1206]	69.8Ω resistor (1%, $\frac{1}{8}$W)	Digi-Key

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Quantity	Ref Des	Part Number	Description	Company
6	R9,R10,R11,R12, R54,R56	P78.7F CT-ND [1206]	78.7Ω resistor (1%, $\frac{1}{8}$W)	Digi-Key
2	R86,R87	P150F CT-ND [1206]	150Ω resistor (1%, $\frac{1}{8}$W)	Digi-Key
9	R13,R30,R31,R32, R33,R34,R35,R36, R37	P221F CT-ND [1206]	221Ω resistor (1%, $\frac{1}{8}$W)	Digi-Key
2	R84,R88	P301F CT-ND [1206]	301Ω resistor (1%, $\frac{1}{8}$W)	Digi-Key
2	R1,R82	P562F CT-ND [1206]	562Ω resistor (1%, $\frac{1}{8}$W)	Digi-Key
4	R16,R17,R18,R19	P825F CT-ND [1206]	825Ω resistor (1%, $\frac{1}{8}$W)	Digi-Key
3	R27,R38,R81	P1.00KF CT-ND [1206]	1.00kΩ resistor (1%, $\frac{1}{8}$W)	Digi-Key
1	R83	P2.21KF CT-ND [1206]	2.21kΩ resistor (1%, $\frac{1}{8}$W)	Digi-Key
2	R2,R26	P3.32KF CT-ND [1206]	3.32kΩ resistor (1%, $\frac{1}{8}$W)	Digi-Key
2	R28,R39	P3.92KF CT-ND [1206]	3.92kΩ resistor (1%, $\frac{1}{8}$W)	Digi-Key
1	R3	P5.11KF CT-ND [1206]	5.11kΩ resistor (1%, $\frac{1}{8}$W)	Digi-Key
1	R44	P6.81KF CT-ND [1206]	6.81kΩ resistor (1%, $\frac{1}{8}$W)	Digi-Key
4	R14,R22,R23,R40	P10.0KF CT-ND [1206]	10.0kΩ resistor (1%, $\frac{1}{8}$W)	Digi-Key
2	R25,R29	P20.0KF CT-ND [1206]	20.0kΩ resistor (1%, $\frac{1}{8}$W)	Digi-Key
1	R43	P43.2KF CT-ND [1206]	43.2kΩ resistor (1%, $\frac{1}{8}$W)	Digi-Key
1	R15	P47.5KF CT-ND [1206]	47.5kΩ resistor (1%, $\frac{1}{8}$W)	Digi-Key
1	C104	SG2002 CT-ND	3-10pF trimmer cap.	Digi-Key
2	C141,C145	P2026-ND	10μF tantalum cap. (10V)(10%)	Digi-Key
9	C1,C19,C40,C44, C46,C54,C59, C62,C142	PCT2106 CT-ND [size-C]	10μF tantalum cap. (10V)(20%)	Digi-Key
2	C140,C144	PCT1226 CT-ND [size-C]	22μF tantalum cap. (6.3V)(20%)	Digi-Key
1	C111a	PCC0R5CV CT-ND [0603]	0.5pF ceramic cap. (±0.25pF)	Digi-Key
4	C109,C110, C111b,C138	PCC020CV CT-ND [0603]	2pF ceramic cap. (±0.25pF)	Digi-Key
1	C129	PCC030CV CT-ND [0603]	3pF ceramic cap. (±0.25pF)	Digi-Key
1	C100	PCC040CV CT-ND [0603]	4pF ceramic cap. (±0.25pF)	Digi-Key
3	C102,C103,C132	PCC080CV CT-ND [0603]	8pF ceramic cap. (±0.50pF)	Digi-Key
7	C96,C98,C99, C105,C107,C112, C115	PCC100CV CT-ND [0603]	10pF ceramic cap. (±1pF)	Digi-Key
3	C106,C125,C128	PCC220ACV CT-ND [0603]	22pF ceramic cap. (5%)	Digi-Key
1	C116	PCC331ACV CT-ND [0603]	330pF ceramic cap. (5%)	Digi-Key

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Quantity	Ref Des	Part Number	Description	Company
1	C94	PCC821BV CT-ND [0603]	820pF ceramic cap. (10%)	Digi-Key
5	C101,C114,C121, C123,C124	PCC102BV CT-ND [0603]	1.0nF ceramic cap. (10%)	Digi-Key
1	C95	PCC392BV CT-ND [0603]	3.9nF ceramic cap. (10%)	Digi-Key
11	C52,C97,C108, C113,C117,C118, C122,C126,C127 C130,C131	PCC103BV CT-ND [0603]	10nF ceramic cap. (10%)	Digi-Key
1	C93	PCC153BV CT-ND [0603]	15nF ceramic cap. (10%)	Digi-Key
1	C119	PCC821CG CT-ND [0805]	820pF ceramic cap. (5%)	Digi-Key
1	C120	PCC102CG CT-ND [0805]	1.0nF ceramic cap. (5%)	Digi-Key
2	C11,C137	PCC0R5C CT-ND [1206]	0.5pF ceramic cap. (±0.25pF)	Digi-Key
2	C57,C58	PCC2R2C CT-ND [1206]	2.2pF ceramic cap. (±0.25pF)	Digi-Key
1	C79	PCC3R9C CT-ND [1206]	3.9pF ceramic cap. (±0.25pF)	Digi-Key
1	C64	PCC4R7C CT-ND [1206]	4.7pF ceramic cap. (±0.25pF)	Digi-Key
1	C51	PCC6R8C CT-ND [1206]	6.8pF ceramic cap. (±0.50pF)	Digi-Key
3	C14,C135,C136	PCC8R2C CT-ND [1206]	8.2pF ceramic cap. (±0.50pF)	Digi-Key
1	C26	PCC120C CT-ND [1206]	12pF ceramic cap. (5%)	Digi-Key
1	C27	PCC150C CT-ND [1206]	15pF ceramic cap. (5%)	Digi-Key
8	C21,C22,C60,C61, C63,C71,C78,C87	PCC200C CT-ND [1206]	20pF ceramic cap. (5%)	Digi-Key
1	C81	PCC270C CT-ND [1206]	27pF ceramic cap. (5%)	Digi-Key
5	C8,C9,C10,C15, C80	PCC390C CT-ND [1206]	39pF ceramic cap. (5%)	Digi-Key
4	C3,C7,C85,C89	PCC470C CT-ND [1206]	47pF ceramic cap. (5%)	Digi-Key
19	C2,C4,C5,C6,C16, C34,C35,C47,C48, C65,C68,C73,C75, C83,C84,C133, C134,C139,C143	PCC101C CT-ND [1206]	100pF ceramic cap. (5%)	Digi-Key
1	C82	PCC271B CT-ND [1206]	270pF ceramic cap. (10%)	Digi-Key
3	C56,C86,C90	PCC471B CT-ND [1206]	470pF ceramic cap. (10%)	Digi-Key
13	C12,C13,C17,C25, C28,C32,C33,C37, C41,C42,C74,C77, C147	PCC102B CT-ND [1206]	1.0nF ceramic cap. (10%)	Digi-Key

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Quantity	**Ref Des**	**Part Number**	**Description**	**Company**
11	C29,C30,C31,C36, C39,C49,C53,C55, C69,C70,C146	PCC103B CT-ND [1206]	10nF ceramic cap. (10%)	Digi-Key
11	C18,C20,C38,C43, C45,C50,C66,C67, C72,C76,C88	PCC104B CT-ND [1206]	100nF ceramic cap. (10%)	Digi-Key
4	C23,C24,C91,C92	PCC1868 CT-ND [1206]	2.2μF ceramic cap. (10%)	Digi-Key

Appendix C

LPE–Mobile: Schematics, Board Layout, & Parts List

- Schematics: Figures C-1 – C-6
- Board Layout: Figures C-7 – C-10
- Parts List: Table C.1

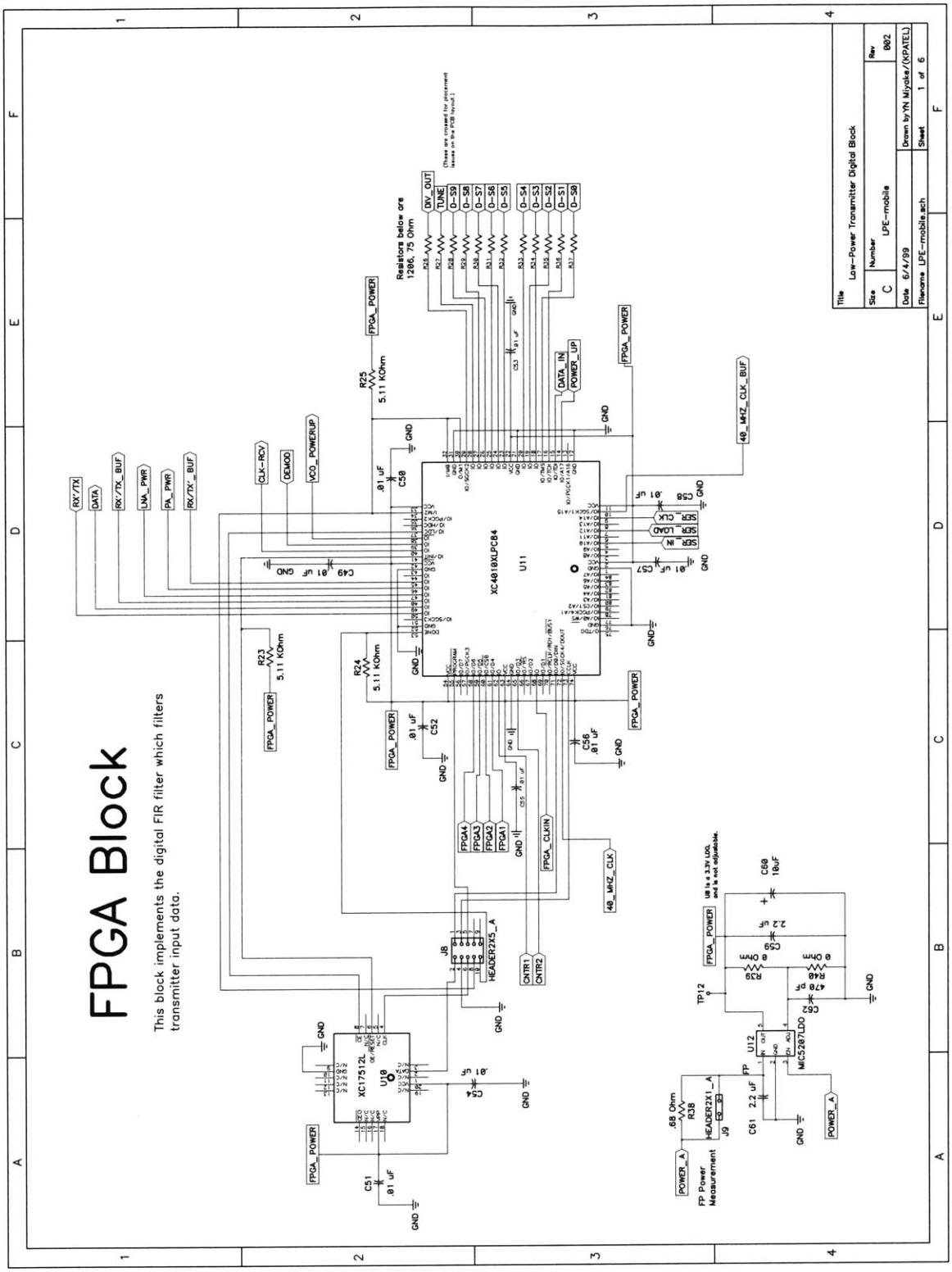

Figure C-1: LPE–Mobile Schematic: Transmitter Synthesizer Chip Block.

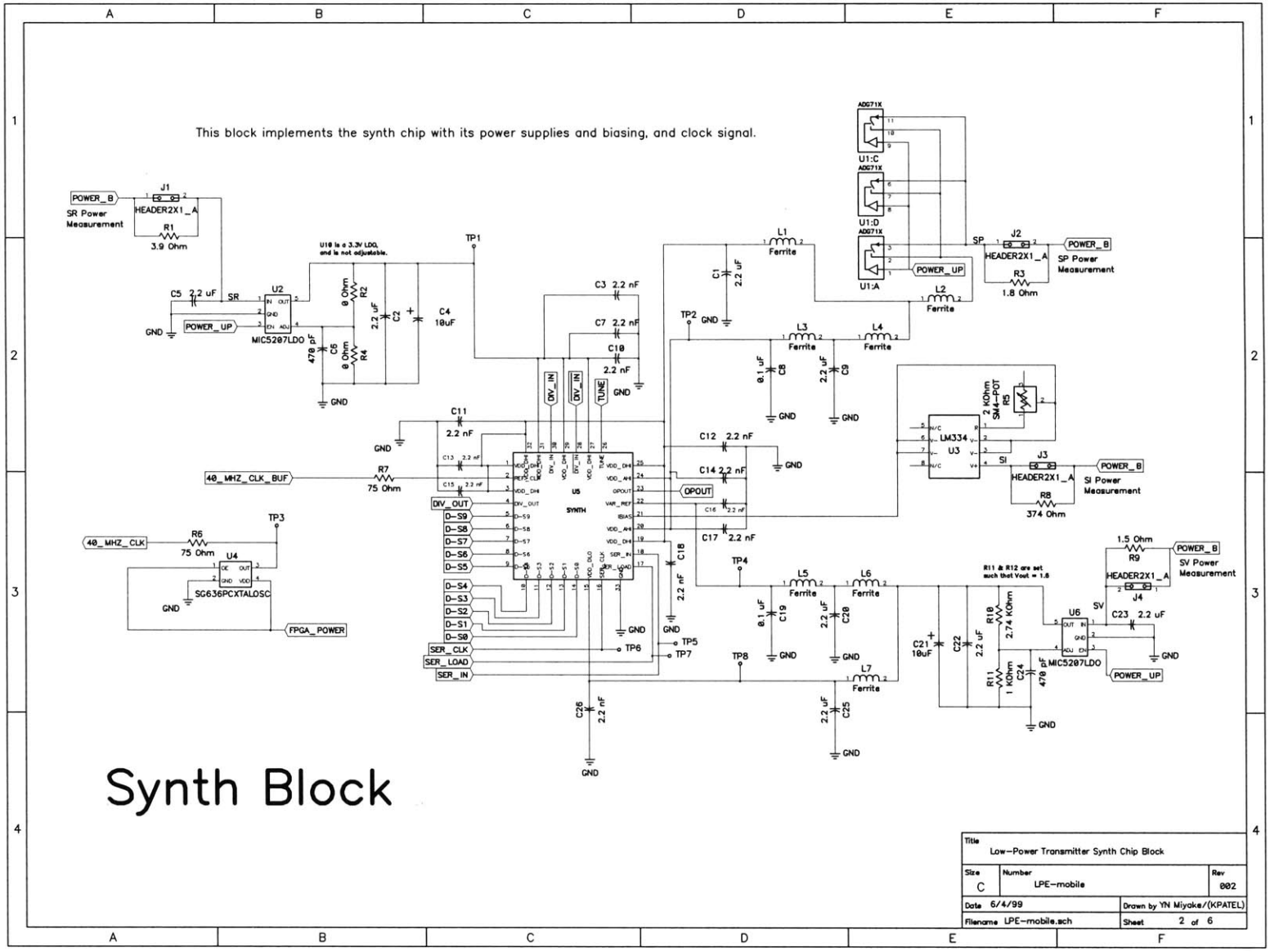

Figure C-2: LPE-Mobile Schematic: Low-Power VCO Block.

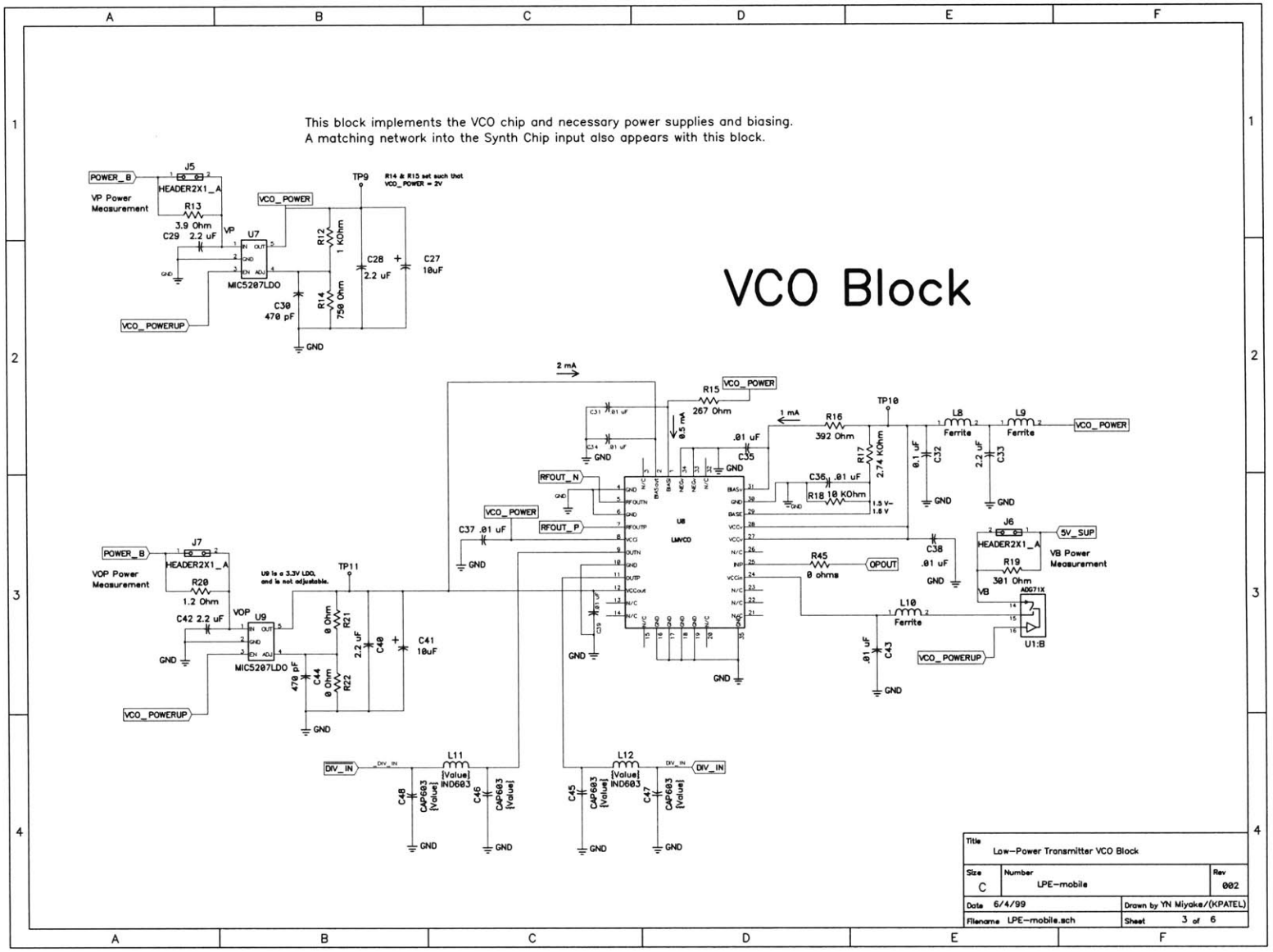

Figure C-3: LPE-Mobile Schematic: Digital FPGA Block.

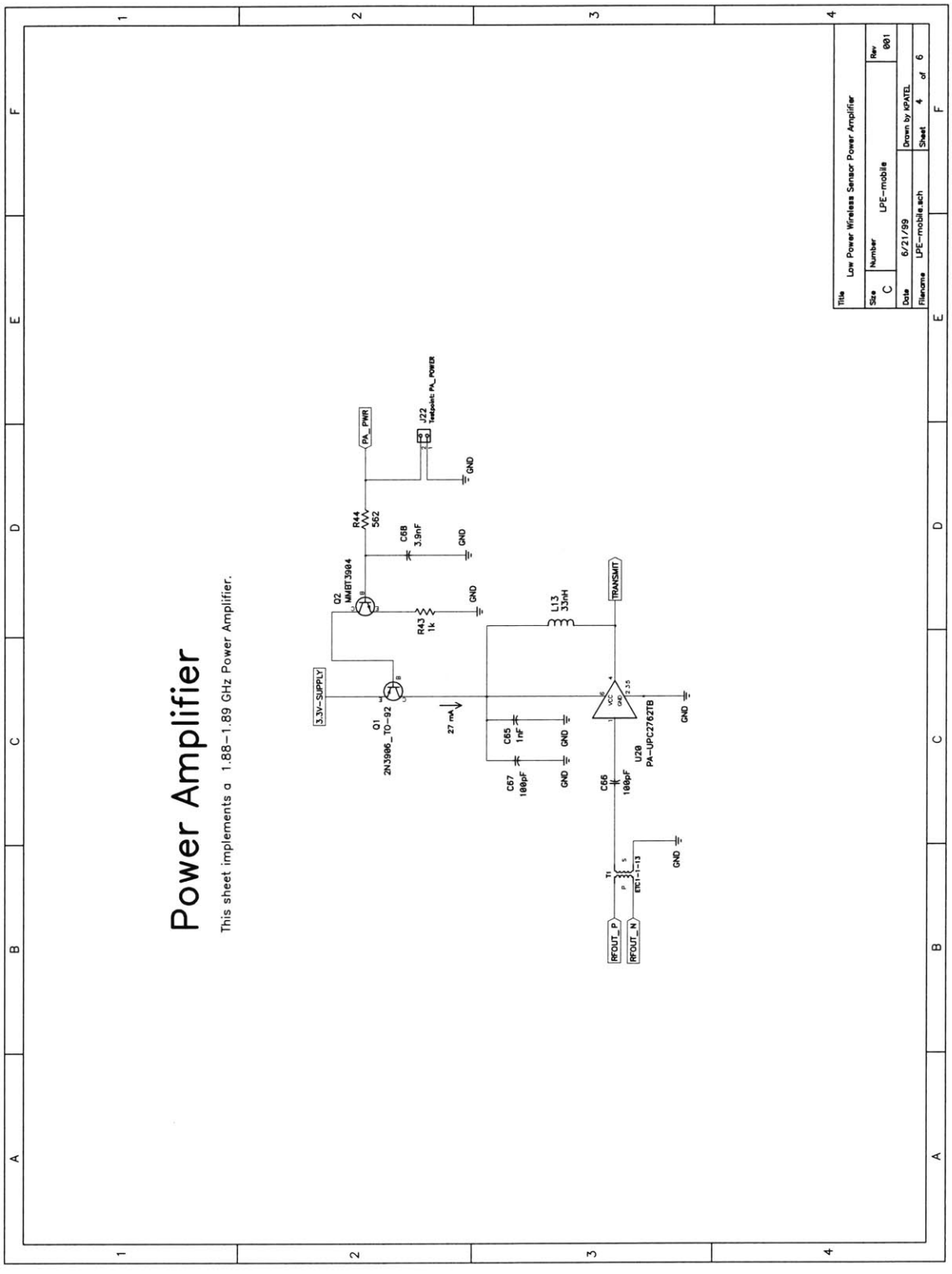

Figure C-4: LPE–Mobile Schematic: Power Amplifier.

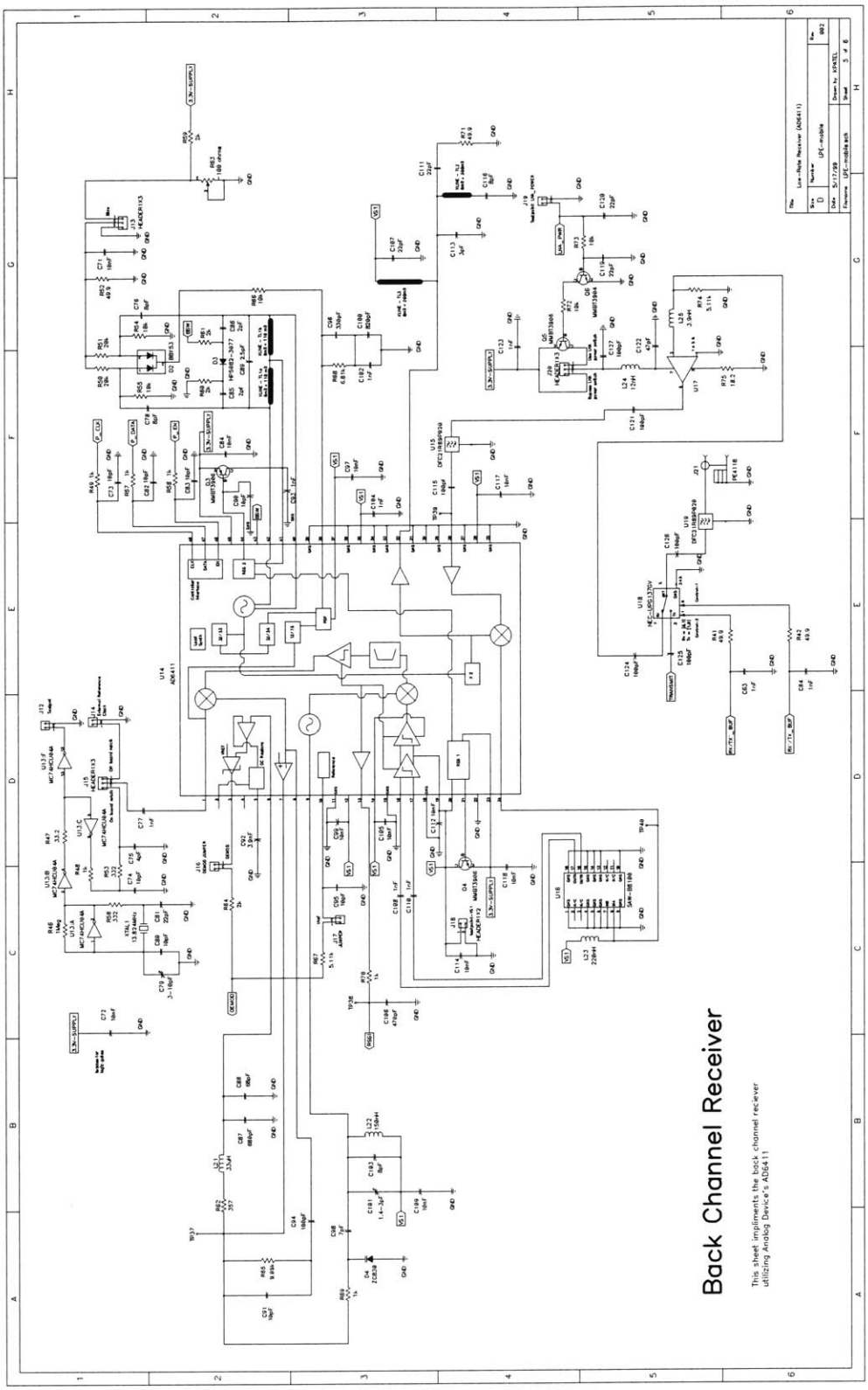

Figure C-5: LPE–Mobile Schematic: Low Data Rate Receiver (AD6411).

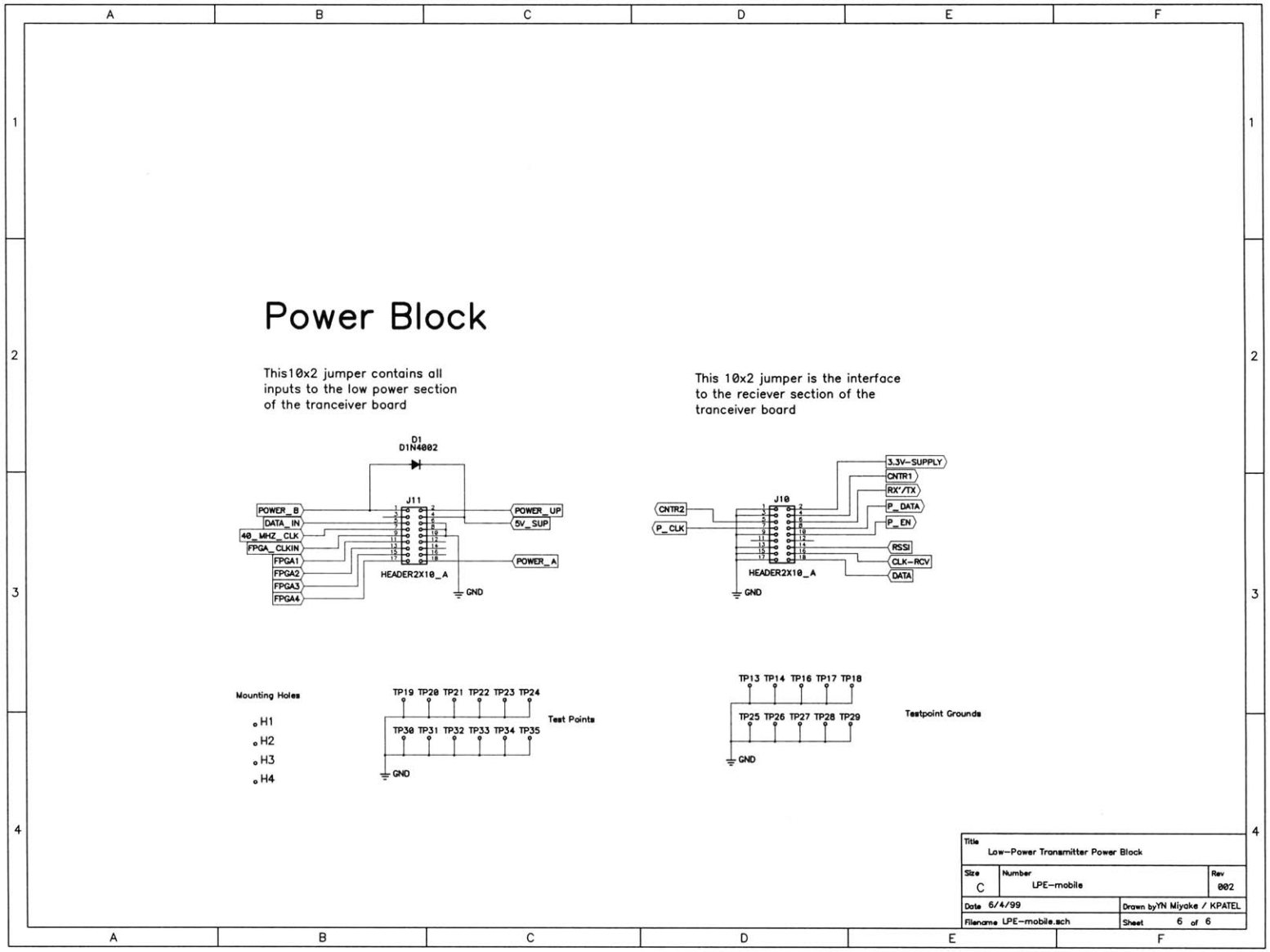

Figure C-6: LPE-Mobile Schematic: Power Block.

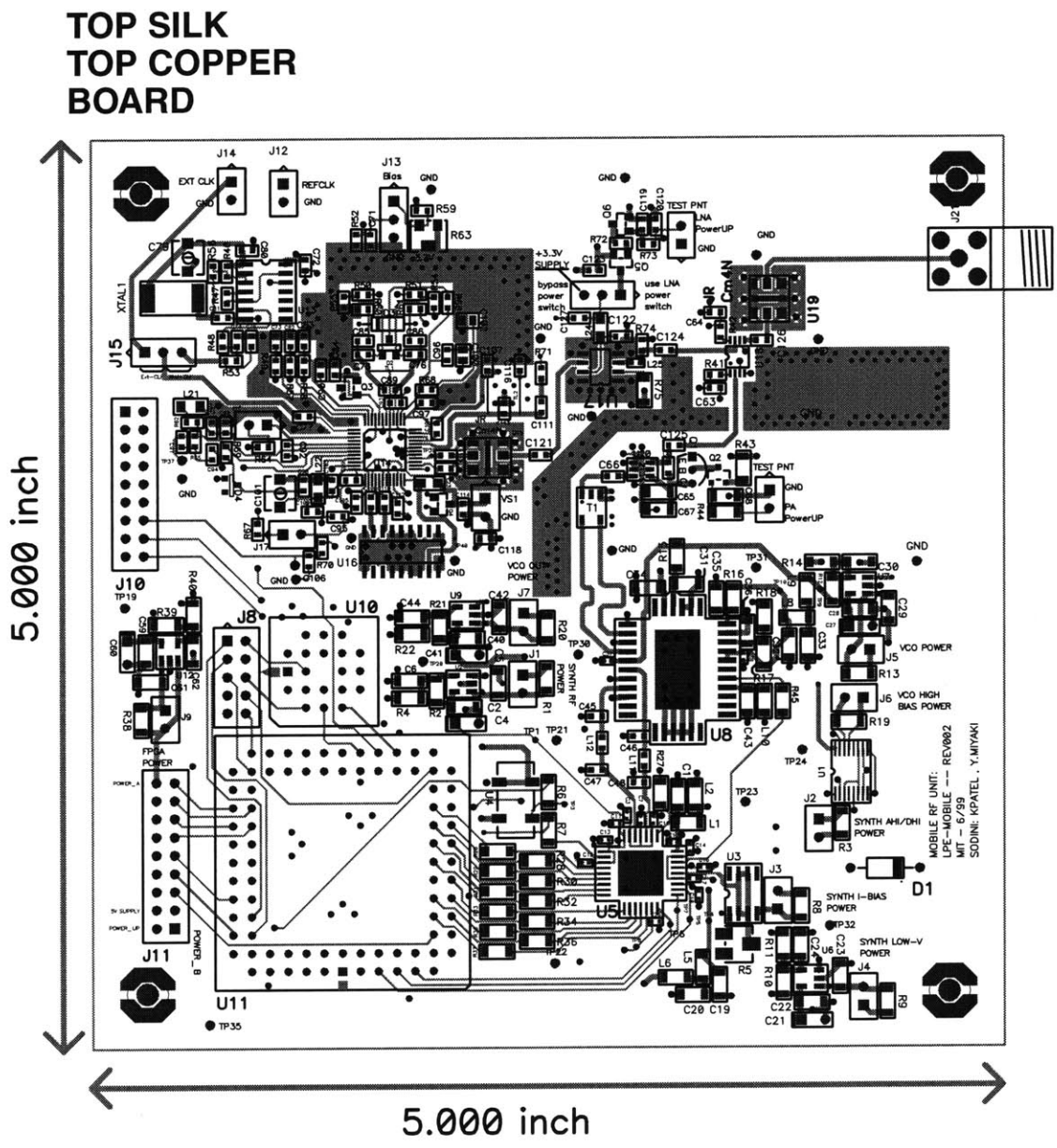

Figure C-7: LPE–Mobile Layout: Layer 1.

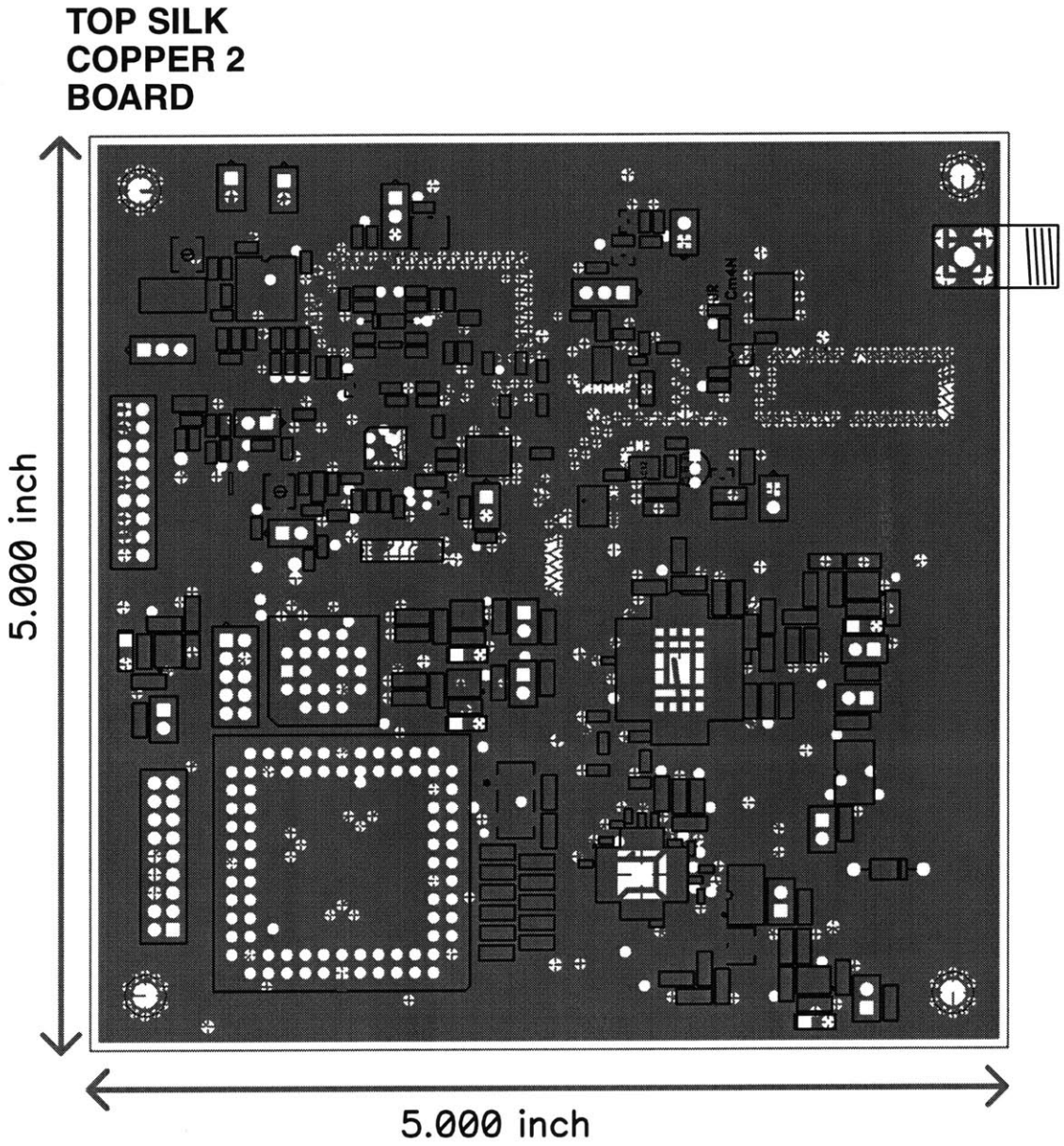

Figure C-8: LPE–Mobile Layout: Layer 2.

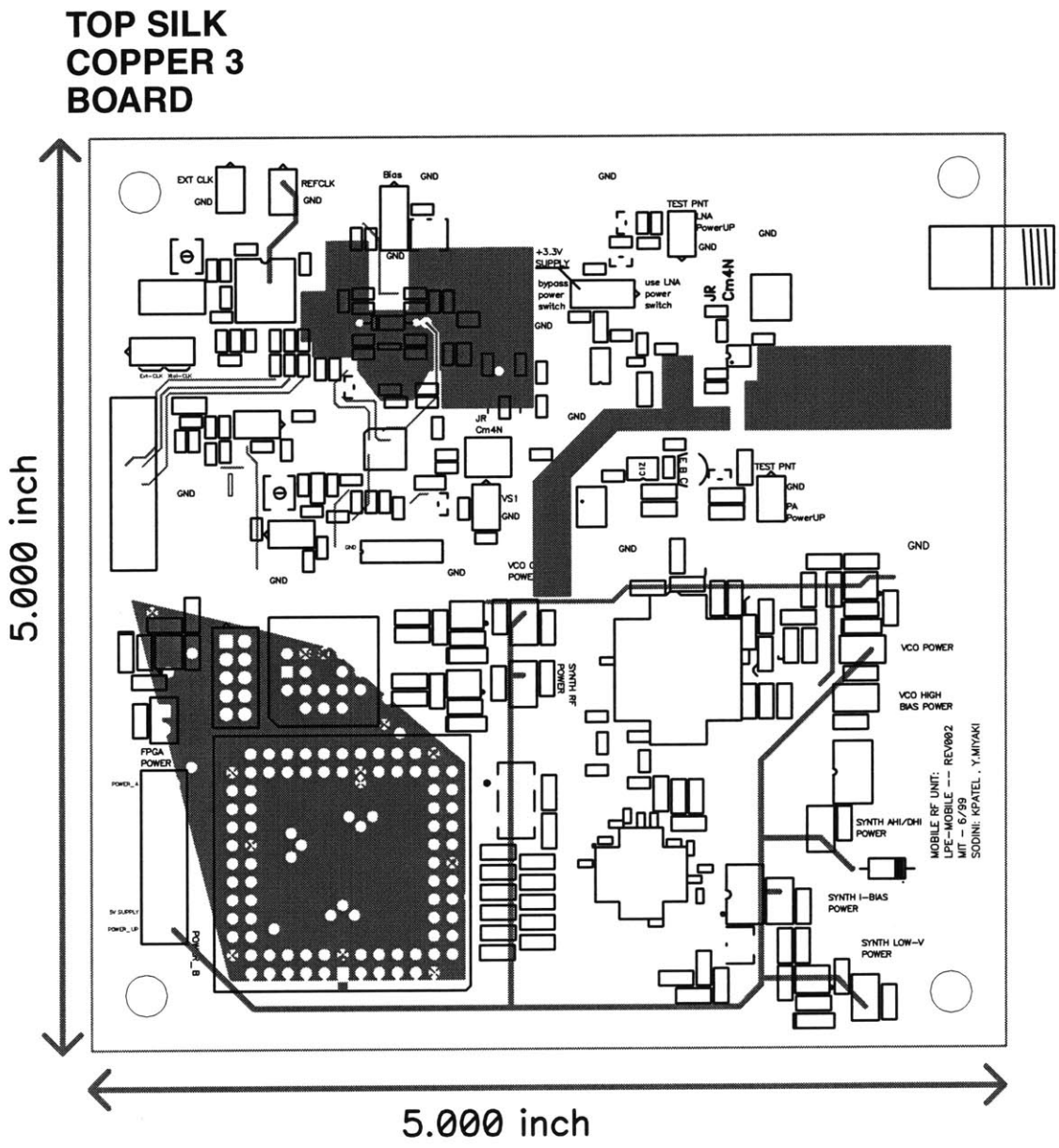

Figure C-9: LPE–Mobile Layout: Layer 3.

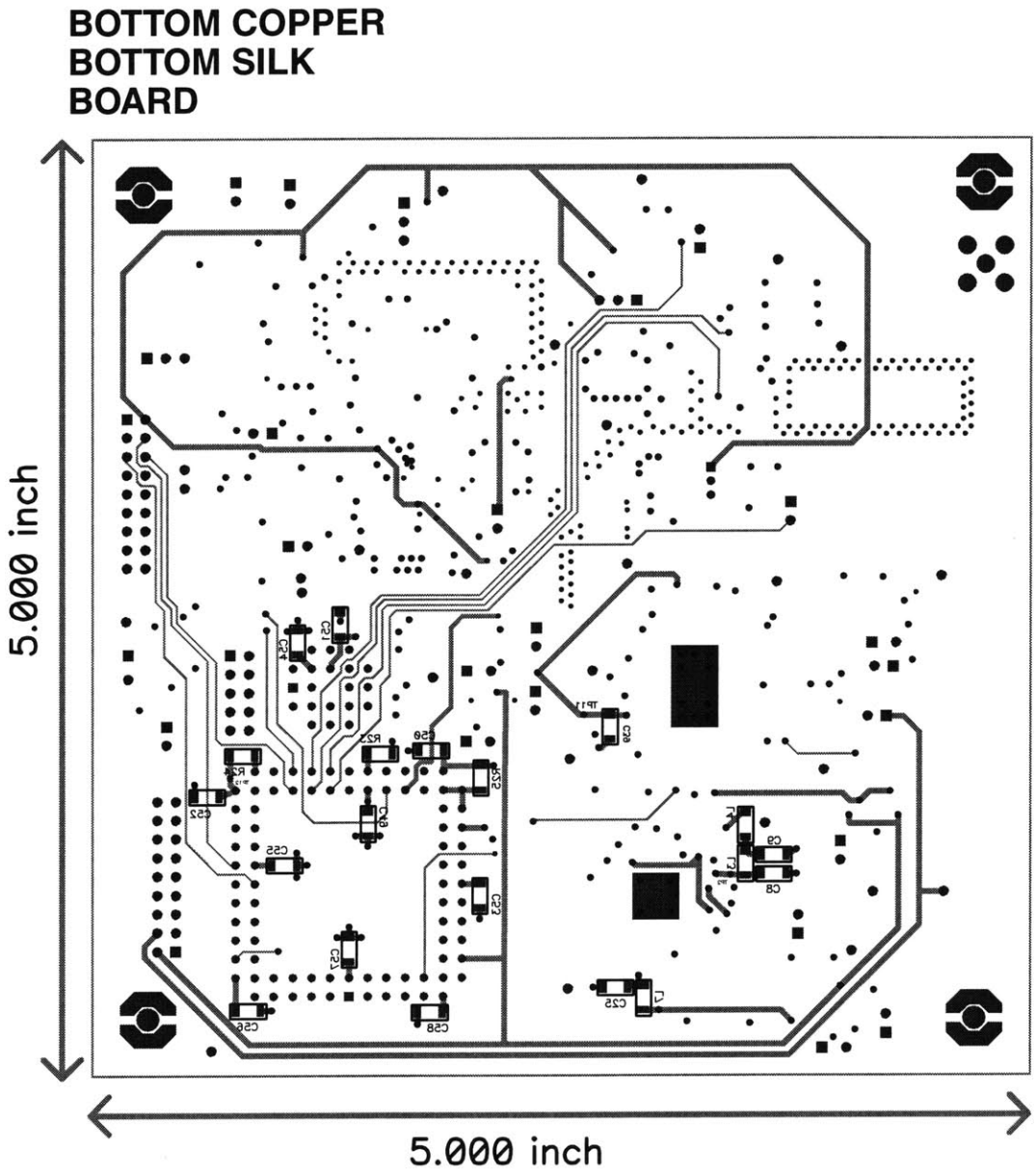

Figure C-10: LPE–Mobile Layout: Layer 4.

Table C.1: Bill of Materials: LPE-Mobile

BILL OF MATERIALS: LPE-Mobile				
Quantity	**Ref Des**	**Part Number**	**Description**	**Company**
1	U1	ADG712	quad switches	Analog Devices
5	U2,U6,U7,U9,U12	MIC5207LDO	LDO	MIT-MTL
1	U3	LM334M	current source	National Semi.
1	U4	SE2851 CT-ND	40 MHz oscillator	Digi-Key
1	U5	SYNTH	freq. synth	MIT-MTL
1	U8	LMVCO	1.89 GHz VCO	MIT-MTL
1	U10	XC175121	ROM case	Mini-Circuits
1	U11	XC4010XLPC84	FPGA case	Mini-Circuits
1	U13	MC74HCU04AD	hex unbuf. inv.	Motorola (Arrow)
1	U14	AD6411	DECT IC	Analog Devices
2	U15,U19	DFC21R89P020	ceramic filter	Murata
1	U16	B8100	SAW filter	Siemens
1	U17	AM50-0004	LNA	MACOM
1	U18	UPG137GV	Tx/Rx switch	NEC (Mouser)
1	U20	UPC2762T	power amplifier	NEC (Mouser)
1	XTAL1	CRYSTAL [CX-1-SM]	13.824 MHz crystal	Statek
1	D1	D1N4002	rectifying diode	Digi-Key
1	D2	BBY53	dual varactor	Siemens
1	D3	HP 5082-3077	switching diode	HP (Arrow)
1	D4	ZC830 ACT-ND	varactor	Digi-Key
1	T1	ETC-1-13	1:1 transformer	MACOM
1	Q1	2N3904-ND	PNP (through hole)	Digi-Key
2	Q2,Q6	MMBT3904 DICT-ND	NPN transisto	Digi-Key
3	Q3,Q4,Q5,	MMBT3906 DICT-ND	PNP transistor	Digi-Key
1	J21	ARFX1232	right angle SMA	Digi-Key
2	J10,J11	MHD20K-ND	20 pin header	Digi-Key
1	L25	PCD1271 CT-ND [0402]	3.9nH inductor (10%)	Digi-Key
1	L24	PCD1185 CT-ND [0805]	12nH inductor (5%)	Digi-Key
1	L22	PCD1174 CT-ND [0805]	150nH inductor (5%)	Digi-Key
1	L23	PCD1176 CT-ND [0805]	220nH inductor (5%)	Digi-Key
1	L21	PCD1246 CT-ND [1008]	33μH inductor (5%)	Digi-Key
10	L1,L2,L3,L4,L5, L6,L7,L8,L9,L10	240-1019-1 ND [1206]	ferrite	Digi-Key
2	L13	0603CS-33NX_BC [0603]	33nH inductor (5%)	Coilcraft

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Quantity	Ref Des	Part Number	Description	Company
7	R2,R4,R21,R22, R39,R40,R45	[SMT 1206]	0Ω short	
1	R63	3214W-101ECT-ND	100Ω POT: top adjust	Digi-Key
1	R5	SM4W202-ND	2kΩ POT: top adjust	Digi-Key
1	R47	P33.2H CT-ND [0603]	33.2Ω resistor (1%, $\frac{1}{16}$W)	Digi-Key
4	R41,R42,R52,R71	P49.9H CT-ND [0603]	49.9Ω resistor (1%, $\frac{1}{16}$W)	Digi-Key
2	R53,R56	P332H CT-ND [0603]	332Ω resistor (1%, $\frac{1}{16}$W)	Digi-Key
1	R62	P357H CT-ND [0603]	357Ω resistor (1%, $\frac{1}{16}$W)	Digi-Key
6	R48,R49,R57,R58, R69,R70	P1.00KH CT-ND [0603]	1.00kΩ resistor (1%, $\frac{1}{16}$W)	Digi-Key
2	R59,R60,R61,R64	P2.00KH CT-ND [0603]	2.00kΩ resistor (1%, $\frac{1}{16}$W)	Digi-Key
2	R67,R74	P5.11KH CT-ND [0603]	5.11kΩ resistor (1%, $\frac{1}{16}$W)	Digi-Key
1	R68	6.81KH CT-ND [0603]	6.81kΩ resistor (1%, $\frac{1}{16}$W)	Digi-Key
1	R65	9.09KH CT-ND [0603]	9.09kΩ resistor (1%, $\frac{1}{16}$W)	Digi-Key
5	R54,R55,R66,R72, R73	P10.0KH CT-ND [0603]	10.0kΩ resistor (1%, $\frac{1}{16}$W)	Digi-Key
2	R50,R51	P20.0KH CT-ND [0603]	20.0kΩ resistor (1%, $\frac{1}{16}$W)	Digi-Key
1	R46	P1.00MH CT-ND [0603]	1.00MΩ resistor (1%, $\frac{1}{16}$W)	Digi-Key
1	R38	P0.68R CT-ND [1206]	0.68Ω resistor (5%, $\frac{1}{8}$W)	Digi-Key
1	R20	P1.2R CT-ND [1206]	1.2Ω resistor (5%, $\frac{1}{8}$W)	Digi-Key
1	R9	P1.5R CT-ND [1206]	1.5Ω resistor (5%, $\frac{1}{8}$W)	Digi-Key
1	R3	P1.8R CT-ND [1206]	1.8Ω resistor (5%, $\frac{1}{8}$W)	Digi-Key
2	R1,R13	P3.9R CT-ND [1206]	3.9Ω resistor (5%, $\frac{1}{8}$W)	Digi-Key
1	R75	P18.2F CT-ND [1206]	18.2Ω resistor (1%, $\frac{1}{8}$W)	Digi-Key
14	R6,R7,R26,R27, R28,R29,R30,R31, R32,R33,R34,R35, R36,R37	P75.0F CT-ND [1206]	75.0Ω resistor (1%, $\frac{1}{8}$W)	Digi-Key
1	R15	P267F CT-ND [1206]	267Ω resistor (1%, $\frac{1}{8}$W)	Digi-Key
1	R19	P301F CT-ND [1206]	301Ω resistor (1%, $\frac{1}{8}$W)	Digi-Key
1	R8	P374F CT-ND [1206]	374Ω resistor (1%, $\frac{1}{8}$W)	Digi-Key
1	R16	P392F CT-ND [1206]	392Ω resistor (1%, $\frac{1}{8}$W)	Digi-Key
1	R44	P562F CT-ND [1206]	562Ω resistor (1%, $\frac{1}{8}$W)	Digi-Key
1	R14	P750F CT-ND [1206]	750Ω resistor (1%, $\frac{1}{8}$W)	Digi-Key
3	R11,R12,R43	P1.00KF CT-ND [1206]	1.00kΩ resistor (1%, $\frac{1}{8}$W)	Digi-Key

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Quantity	Ref Des	Part Number	Description	Company
2	R10,R17	P2.74KF CT-ND [1206]	2.74kΩ resistor (1%, $\frac{1}{8}$W)	Digi-Key
3	R23,R24,R25	P5.11KF CT-ND [1206]	5.11kΩ resistor (1%, $\frac{1}{8}$W)	Digi-Key
1	R18	P10.0KF CT-ND [1206]	10.0kΩ resistor (1%, $\frac{1}{8}$W)	Digi-Key
1	C101	SG2000 CT-ND	1.4-3.0pF trimmer cap.	Digi-Key
1	C79	SG2002 CT-ND	3-10pF trimmer cap.	Digi-Key
5	C4,C21,C27,C41, C60	P2026-ND	10μF tantalum cap. (10V)(10%)	Digi-Key
12	C3,C7,C10,C11, C12,C13,C14,C15, C16,C17,C18,C26	PCC1725 CT-ND [0402]	2.2nF ceramic cap. (10%)	Digi-Key
2	C37,C38	PCC103BQ CT-ND [0402]	0.01μF ceramic cap. (10%)	Digi-Key
1	C89a	PCC0R5CV CT-ND [0603]	0.5pF ceramic cap. (±0.25pF)	Digi-Key
3	C85,C86,C89b	PCC020CV CT-ND [0603]	2pF ceramic cap. (±0.25pF)	Digi-Key
1	C113	PCC030CV CT-ND [0603]	3pF ceramic cap. (±0.25pF)	Digi-Key
1	C75	PCC040CV CT-ND [0603]	4pF ceramic cap. (±0.25pF)	Digi-Key
1	C98	PCC070CV CT-ND [0603]	7pF ceramic cap. (±0.50pF)	Digi-Key
4	C76,C78,C103, C116	PCC080CV CT-ND [0603]	8pF ceramic cap. (±0.50pF)	Digi-Key
8	C73,C74,C80,C82 C83,C90,C91,C95	PCC100CV CT-ND [0603]	10pF ceramic cap. (±1.0pF)	Digi-Key
5	C81,C107,C111, C119, C120	PCC220ACV CT-ND [0603]	22pF ceramic cap. (5%)	Digi-Key
1	C122	PCC470ACV CT-ND [0603]	47pF ceramic cap. (5%)	Digi-Key
1	C88	PCC680ACV CT-ND [0603]	68pF ceramic cap. (5%)	Digi-Key
8	C66,C94,C115, C121,C124,C125, C126,C127	PCC101ACV CT-ND [0603]	100pF ceramic cap. (5%)	Digi-Key
1	C96	PCC331ACV CT-ND [0603]	330pF ceramic cap. (5%)	Digi-Key
1	C106	PCC471BV CT-ND [0603]	470pF ceramic cap. (10%)	Digi-Key
1	C87	PCC681BV CT-ND [0603]	680pF ceramic cap. (10%)	Digi-Key
8	C63,C64,C77,C93, C104,C108,C110, C123	PCC102BV CT-ND [0603]	1.0nF ceramic cap. (10%)	Digi-Key
1	C92	PCC392BV CT-ND [0603]	3.9nF ceramic cap. (10%)	Digi-Key

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Quantity	Ref Des	Part Number	Description	Company
11	C71,C72,C84,C97, C99,C105,C109, C112,C114,C117, C118	PCC103BV CT-ND [0603]	10nF ceramic cap. (10%)	Digi-Key
1	C100	PCC821CG CT-ND [0805]	820pF ceramic cap. (5%)	Digi-Key
1	C102	PCC102CG CT-ND [0805]	1.0nF ceramic cap. (5%)	Digi-Key
1	C67	PCC101C CT-ND [1206]	100pF ceramic cap. (5%)	Digi-Key
5	C6,C24,C30,C44, C62	PCC471C CT-ND [1206]	470pF ceramic cap. (10%)	Digi-Key
1	C65	PCC102B CT-ND [1206]	1.0nF ceramic cap. (10%)	Digi-Key
1	C68	PCC392B CT-ND [1206]	3.9nF ceramic cap. (10%)	Digi-Key
16	C31,C34,C35,C36 C39,C43,C49,C50, C51,C52,C53,C54, C55,C56,C57,C58	PCC103B CT-ND [1206]	10nF ceramic cap. (10%)	Digi-Key
3	C8,C19,C32	PCC104B CT-ND [1206]	100nF ceramic cap. (10%)	Digi-Key
15	C1,C2,C5,C9,C20, C22,C23,C25,C28, C29,C33,C40,C42, C59,C61	PCC1868 CT-ND [1206]	2.2μF ceramic cap. (10%)	Digi-Key

Appendix D

Programming the LMX2330L Dual Frequency Synthesizer

Functional Description

The National Semiconductor 2.5 GHz LMX2330L PLLatinum^{TM} Low Power Dual Frequency Synthesizer employs a digital phase–locked loop technique incorporating dual modulus prescalars to produce the tuning voltages for two external VCOs.

Nominal Programming Words

With a 30 MHz reference frequency, the data sequence shown below sets LO_{RF} to 1.7500 GHz and LO_{IF} to 161.25 MHz:

RF(R)=9 : $(01001000000000000100110)_2$

IF(R)=8: $(01001000000000000100000)_2$

RF(N)=525: $(00000000100000000110111)_2$

IF(N)=43: $(00000000001010000001101)_2$

Pulse Swallow Function

The frequency to programming relationship is governed by the following equation:

$$f_{VCO} = \left[(P \cdot B) + A\right] \cdot \frac{f_{osc}}{R}$$

f_{VCO}: Output frequency of external VCO

P: Prescalar modulus (for RF, P= 32 or 64; for IF, P= 8 or 16)

B: Preset divide ratio of 11–bit programmable counter (3 to 2047)

A: Preset divide ratio of 7–bit swallow counter

$$(0 \leq A \leq 127\{RF\}; 0 \leq A \leq 15\{IF\}; A \leq B)$$

f_{osc}: Output frequency of external reference oscillator

R: Preset divide ratio of 15–bit programmable reference counter (3 to 32767)

Control Bits

The three wire programming is performed via a 22–bit shift register that transfers data to two 15–bit R counters and to the 15–bit and 18–bit N counters. The DATA stream is clocked in on the rising edge of the CLOCK signal, MSB first, and then stored to the appropriate counter latches on the rising edge of LE. The last two bits are Control Bits that choose which of the 4 latches the data should be transfered into when LE is pulsed high.

Control Bits		DATA Location
C2	C1	
0	0	IF R Counter
0	1	IF N Counter
1	0	RF R Counter
1	1	RF N Counter

Table D.1: Latch Selection via Control Bits

Programmable Reference Dividers (R Counter)

If the Control Bits {C2,C1} are 00 or 10, then the data is transferred from the 22–bit register to the 15–bit R counter. Serial data format follows.

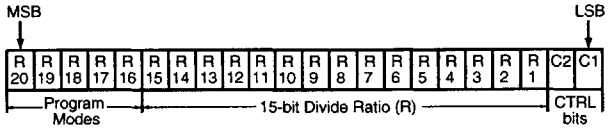

Figure D-1: Reference divider (R) serial format.

Divide Ratio	R 15	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Notes:
Divide ratios less than 3 are prohibited.
Divide ratio: 3 to 32767
R1 to R15: These bits select the divide ratio of the programmable reference divider.
Data is shifted in MSB first.

Table D.2: 15–Bit Programmable Reference Divider Ratio (R counter)

Programmable Dividers (N Counter)

The N counter consists of the 7–bit swallow counter (A counter) and the 11–bit programmable counter (B counter). If the Control Bits {C2,C1} are 01 or 11, then the data is transferred from the 22–bit register into an 11–bit latch (B counter) and either a 7–bit or 4–bit latch (A counter). [For the IF N counter, bits 7, 6, and 5 are DON'T CARE bits.] Serial format of the N counter is shown below.

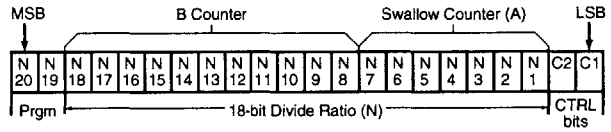

Figure D-2: Divider (N) serial format.

RF

Divide Ratio A	N 7	N 6	N 5	N 4	N 3	N 2	N 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

Notes: Divide ratio: 0 to 127
B ≥ A

IF

Divide Ratio A	N 7	N 6	N 5	N 4	N 3	N 2	N 1
0	X	X	X	0	0	0	0
1	X	X	X	0	0	0	1
.	.	.	.	.	.	.	.
15	X	X	X	1	1	1	1

X = DON'T CARE condition

Table D.3: 7–Bit Swallow Counter Divide Ratio (A counter)

Divide Ratio B	N 18	N 17	N 16	N 15	N 14	N 13	N 12	N 11	N 10	N 9	N 8
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.	.	.	.
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio: 3 to 2047 (Divide ratios less than 3 are prohibited)
B ≥ A

Table D.4: 11–Bit Programmable Counter Divide Ratio (B counter)

Programmable Modes

Modes of operation can be programmed with bits R16–R20, including phase detector polarity and charge pump TRI-STATE. The following two truth tables provide information for the modes.

C1	C2	R16	R17	R18	R19	R20
0	0	IF Phase Detector Polarity	IF I_{CPo}	IF D_o TRI-STATE	IF LD	IF F_o
0	1	RF Phase Detector Polarity	RF I_{CPo}	RF D_o TRI-STATE	RF LD	RF F_o

C1	C2	N19	N20
1	0	IF Prescaler	Pwdn IF
1	1	RF Prescaler	Pwdn RF

Table D.5: Synthesizer Programmable Modes

	Phase Detector Polarity (Note 1)	D_o TRI-STATE	I_{CPo} (Note 2)	IF Prescaler	2330L RF Prescaler	2331L/32L RF Prescaler	Power Down
0	Negative	Normal Operation	LOW	8/9	32/33	64/65	Pwrd Up
1	Positive	TRI-STATE	HIGH	16/17	64/65	128/129	Pwrd Dn

Note 1: PHASE DETECTOR POLARITY
Depending upon VCO characteristics, R16 bit should be set accordingly:
When VCO characteristics are positive, R16 should be set HIGH;
When VCO characteristics are negative, R16 should be set LOW.

Note 2: The I_{CPo} LOW current state = 1/4 x I_{CPo} HIGH current.

Table D.6: Mode Select Truth Table

Serial Data Input Timing

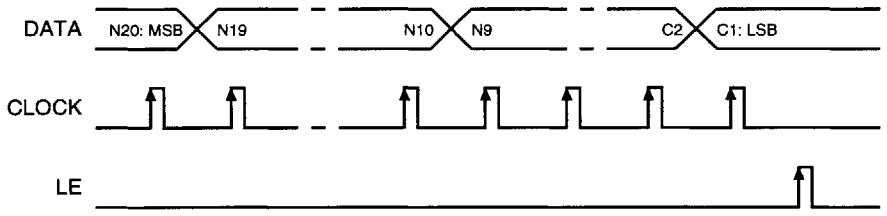

Figure D-3: LMX2330L three-wire serial programming timing diagram.

- 5V CMOS logic levels needed
- Data shifted into register MSB first on rising edge of CLOCK.
- Date is loaded to appropriate counter latch on rising edge of LE

DATA set up time:	50 ns
DATA hold time:	10 ns
ENABLE pulse width:	50 ns
CLOCK low to ENABLE high:	50 ns
CLOCK high/low pulse width:	50 ns

Appendix E

Programming the AD6411 DECT RF Transceiver

Functional Description

Analog Device's AD6411 DECT RF Transceiver provides a single integrated chip solution to implementing a digital wireless transceiver that is fully compliant with the Digital Enhanced Cordless Telecommunications (DECT) standard.

The receiver implements a dual–IF receiver that uses a PLL to demodulate the data. The transmit function is performed by directly modulating a VCO operating at half the transmit frequency. An on–chip frequency doubler translates the signal to its proper DECT channel.

Nominal Programming Words

The programming sequences shown below are for communication in the fourth DECT channel (1.890432 GHz):

Receive

Setup A, analog out:	$(0110111001100110)_2$
Setup A, digital out:	$(0110111001110110)_2$
Pre-Rx B, 4th ch:	$(0001100011101011)_2$
Active-Rx B, 4th ch:	$(0001101111101011)_2$

Transmit

Setup A,	$(0110111001100110)_2$
Pre-Tx B, 4th ch:	$(1001100001111111)_2$
Active-Tx B, 4th ch:	$(1001100001011111)_2$

Power Down

Standby, regs on	$(1xxxxx0000000111)_2$
All off:	$(1xxxxx0000000101)_2$

Initial Setup

A one–time setup word must be loaded in and is selected by setting the LSB to 0. The register format as well as bit definitions follow:

D15	D14	D13	D12	D11	D10	D9	D8
X	RSB	TSB	SSB	RXM1	RXM0	TXM	BSWS

D7	D6	D5	D4	D3	D2	D1	D0
CF0	CT1	CT0	DSD	SFM	PDS	RD	0

Figure E-1: One-time setup register.

RSB: Receive Control Line Sense Bit

RSB	Function
0	Receive Section POWER UP Active HIGH
1	Receive Section POWER UP Active LOW

TSB: Transmit Control Line Sense Bit

TSB	Function
0	Transmit Section POWER UP Active HIGH
1	Transmit Section POWER UP Active LOW

SSB: Synthesizer Control Line Sense Bit

SSB	Function
0	Synthesizer POWER UP Active LOW
1	Synthesizer POWER UP Active HIGH

RXM1, RXM0: Divider Power Mode In Active Receive Slot

RXM1	RXM0	Function
0	0	Dividers Powered Down, VCO Flywheeled in Active Receive Mode
0	1	Dividers Powered Up, VCO Flywheeled in Active Receive Mode
1	0	Dividers Powered Up, VCO Locked to Synthesizer in Active Receive Mode
1	1	Dividers Powered Up, VCO Locked to Synthesizer in Active Receive Mode

TXM: Divider Power Mode In Active Transmit Slot

TXM	Function
0	Dividers Powered Down, VCO Flywheeled in Active Mode
1	Dividers Powered Up, VCO Flywheeled in Active Mode

BSWS: Band Switch Sense (Control with External Lines)

BSWS	Function
0	Band Switch Output High in Receive Slot, PIN Diode ON
1	Band Switch Output Low in Receive Slot, PIN Diode ON

CF0: Configuration Bit 0

CF0	Function
0	Use Serial Interface for Mode Control
1	Use External Control Lines for Mode Control

CT1, CT0: Charge Pump Test Bits

CT1	CT0	Function
0	0	Three-State Output
0	1	Force Pump UP Current (Nom 1 mA)
1	0	Force Pump DOWN Current (Nom 1 mA)
1	1	Normal Operation (Driven from PFD)

DSD: Disable Data Slicer

DSD	Function
0	Disable On-Chip Data Slicer. Analog Output at Pin DEMOD_DATA
1	Enable On-Chip Data Slicer. Digital Output at Pin DEMOD_DATA

DSD bit is configured at power-up depending on whether an external data slicer is being used in the system. Data slicer is disabled when the IF strip is powered down irrespective of the status of bit DSD.

SFM: S-Field Mode

SFM	Function
0	Normal Demodulation Mode
1	S-Field Sampling Mode

PDS: Phase Detector Sense

PDS	Function
0	PFD Pumps UP when Fvco > Fref
1	PFD Pumps UP when Fref > Fvco

RD: Reference Divide Ratio

RD	Function
0	Reference Frequency = 10.368 MHz
1	Reference Frequency = 13.824 MHz

Table E.1: One–Time Setup Register Bit Definitions

Operating Mode

The operating mode register is loaded when the LSB is 1. The register, as diagramed in Figure E-2, allows any circuit block to be independently powered on or off.

D15	D14	D13	D12	D11	D10	D9	D8
M0	A4	A3	A2	A1	A0	IF/RSSI	RXMixer

D7	D6	D5	D4	D3	D2	D1	D0
DMOD	DIV	CP	TX BUF	UHF VCO	BSW	REGS	1

Figure E-2: Operating mode control register.

Data Bits (D9 . . . D0) Operating Mode Register	Function	Comments
00 0000 0101	All Off Mode	All Circuits Off
00 0000 0111	Stand-By Mode	Regulators On
00 0111 1111	Prior to TX Slot	VCO, TX Buffer, Dividers, Charge Pump, Regulators Active, VREF (1.4 V) Active
00 0101 1111	Active TX Slot	VCO, TX Buffer, Dividers, Regulator Circuits Active, VREF (1.4 V) Active
00 1110 1011	Prior to RX Slot	VCO, Dividers, Charge Pump, Regulators, Demodulator Precharge Circuits Active, VREF (1.4 V) Active
11 1100 1011	Active RX Slot	RX Mixer, VCO , Dividers, Regulators, Demodulator, Receive Strip Circuits Active, VREF (1.4 V) Active

Table E.2: Bit Status for Different Operating Modes

CHANNEL SELECTION/FREQUENCY CONTROL

The M0 and A4–A0 bits in the operating mode register control the channel selection for the AD6411 synthesizer. The M0 bit selects the M Counter division ratio.

M0: M Counter Divide Ratio

M0	Function
0	M Divide Ratio 32
1	M Divide Ratio 34

The A4 through A0 bits control the A counter division ratio, and control the channel selection. Refer to the section of this data sheet on Synthesizer Programming for a mapping of channel frequency to synthesizer divider words.

A4–A0: A Counter Division Ratio

"A"	A4	A3	A2	A1	A0
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
–	–	–	–	–	–
30	1	1	1	1	0
31	1	1	1	1	1

Table E.3: Channel Selection Control Bits

Transmit

DECT Channel	A Counter	M Counter	Frequency/MHz
9	1	34	1881.792
8	2	34	1883.520
7	3	34	1885.248
6	4	34	1886.976
5	5	34	1888.704
4	6	34	1890.432
3	7	34	1892.160
2	8	34	1893.888
1	9	34	1893.888
0	10	34	1897.344

Receive (Local Oscillator Frequency)

Main values are shown for a 110.592 MHz IF frequency. Values in parentheses are for the 112.32 MHz.

DECT Channel	A Counter	M Counter	Frequency/MHz
9	1 (0)	32	1771.200 (1769.472)
8	2 (1)	32	1772.928 (1771.200)
7	3 (2)	32	1774.656 (1772.928)
6	4 (3)	32	1776.384 (1774.656)
5	5 (4)	32	1778.112 (1776.384)
4	6 (5)	32	1779.840 (1778.112)
3	7 (6)	32	1781.568 (1779.840)
2	8 (7)	32	1783.296 (1781.568)
1	9 (8)	32	1785.024 (1783.296)
0	10 (9)	32	1786.752 (1785.024)

Table E.4: DECT Channel Programming

Timing Diagram

The three line serial interface for the AD6411 is similar to that of the LMX2330L (Fig D-3). The DATA is clocked in on the rising edge of CLOCK. The 16–bit word is transfered from the register to the appropriate latch on the rising edge of EN.

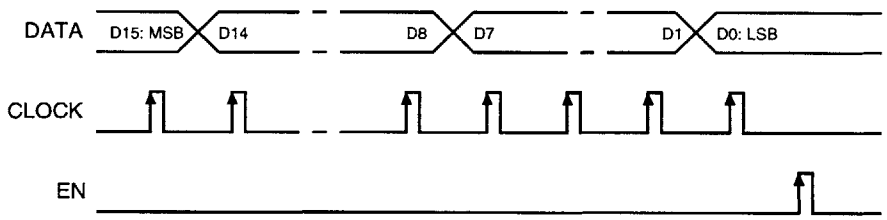

Figure E-3: AD6411 three-wire serial programming timing diagram.

- 3.3V CMOS logic levels needed.
- Data shifted into register MSB first on rising edge of CLOCK.
- Data is loaded to appropriate counter latch on rising edge of LE.

Maximum serial CLOCK frequency:	13.824 MHz
DATA set up time:	8 ns
DATA hold time:	8 ns
ENABLE set up to CLOCK high:	10 ns
CLOCK low to ENABLE high:	5 ns

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