

# Field Emission from Silicon

by

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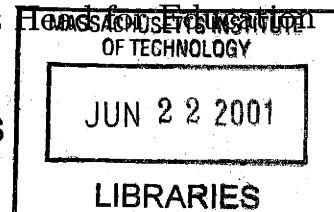
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## Abstract

A field emitter serves as a cold source of electrons. It has practical applications in various fields such as field emission flat panel displays, multiple electron-beam lithography, ion propulsion/micro-thrusters, radio frequency source, information storage technology, and electronic cooling. Silicon is an attractive material for building electron field emitters. To understand the physics of electron field emission from silicon and to push technologies of making quality field emitter arrays present both opportunities and challenges. This work focuses on an experimental study of electron field emission phenomena from silicon field emitter arrays.

We demonstrate electron field emission from both the conduction band and the valence band of silicon simultaneously. A two-band field emission model is presented to explain the experimental data. Theoretical predictions for valence band emission were made in the past; however there was no direct observation until now. Experimental evidence of current saturation in field emission existed in the literature. We also report the observation of current saturation in n-type silicon field emitter arrays. A simple model is presented to account for the results.

We report successfully fabricating  $1\mu m$  gate-aperture silicon field emitter arrays with a turn-on voltage as low as 14 V. The gate leakage current is observed to be less than 0.01% of the total emission current. Devices show excellent emission uniformity for different sized arrays. The low turn-on voltage is attributed to the small emitter tip radius. It was achieved by isotropic etching of silicon and low temperature oxidation sharpening of the emitter tips. Field emitters with a tip radius of about  $10nm$  can be routinely obtained. Optimization of the oxidation sharpening process further reduced the tip radius to be around  $1nm$ . The results were confirmed by Transmission Electron Microscopy (TEM). Device characterization showed agreement with Fowler-Nordheim theory. Analytical and numerical models were introduced to account for the experimental results. We also demonstrate the successful fabrication of the high aspect ratio silicon tip field emitter arrays. Silicon emitters as high as  $5 - 6\mu m$  with an aspect ratio larger than  $10 : 1$  was achieved in our facilities. Furthermore we have also successfully fabricated and tested the fully gated high aspect ratio field emitter arrays. The experimental current-voltage data agree well with the Fowler-Nordheim

theory.

A Maxwell Stress Microscope, which is capable of imaging sample topography and the surface potential simultaneously is set up and tested for the purpose of further study of the properties of the surfaces of the silicon field emitters.

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To my father and my mother.

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# Chapter 1

## Introduction

### 1.1 Background and motivation

Electron sources are increasingly important tools for scientific research and device technology. They are used in a broad range of applications which include television monitors, scanning electron microscopes, flat panel displays, and spacecraft neutralizer. Electron beams can be obtained from solids using several mechanisms, the most common being photo electron emission, thermionic electron emission, and field electron emission.

Field electron emission is the phenomenon that electrons are extracted from inside a solid into vacuum when an intense external electric field is applied near the solid surface. Typically, the electron sources are arrays of micro-structures called field emission arrays (FEAs).

Thermionic electron emission is most widely used in electron guns in Cathode Ray Tubes (CRTs). A filament is heated such that electrons escape from inside the filament into vacuum. In contrast, a field emitter electron source does not need heating.

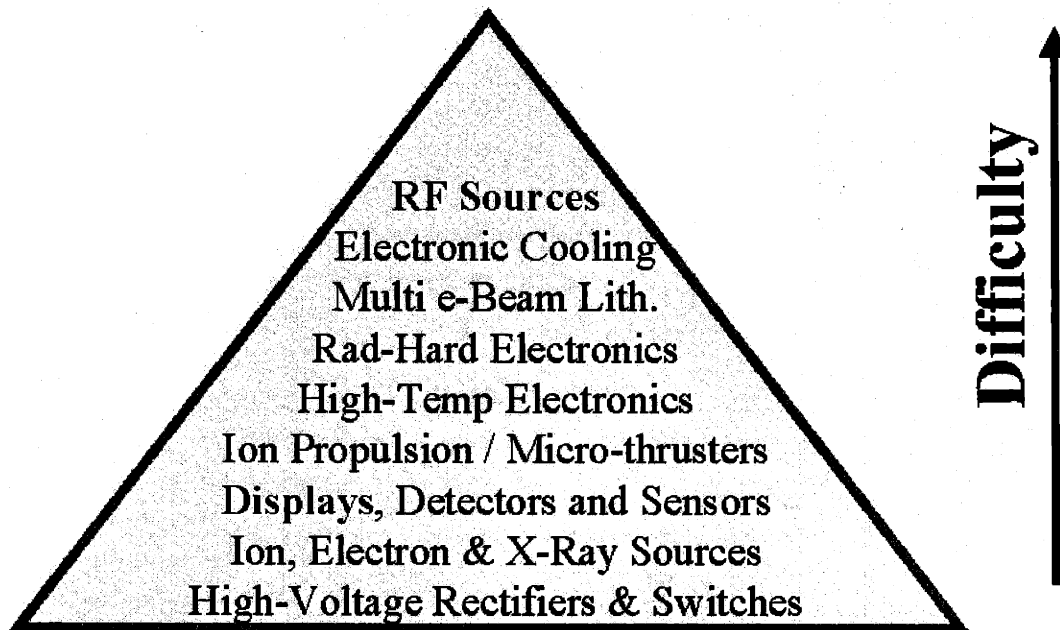


Figure 1-1: Applications of gated electron field emitters.

Electron field emitters have applications in various fields as listed in figure 1-1 [2, 3, 11, 12, 13, 14, 15, 16, 17, 18, 20].

The prevailing application of electron field emitters is the field emission display (FED) technology, which is the motivation of this work in the first place.

Silicon is a promising material for building field emission arrays, because its conductivity could be modulated by changing its doping or the surface potential, and it has rather advanced and mature microfabrication technology. Thus experimental exploration of electron field emission from silicon is of interest for both the fundamental physics and the practical applications. This work will address some of the physical and technological issues in field emission from silicon.

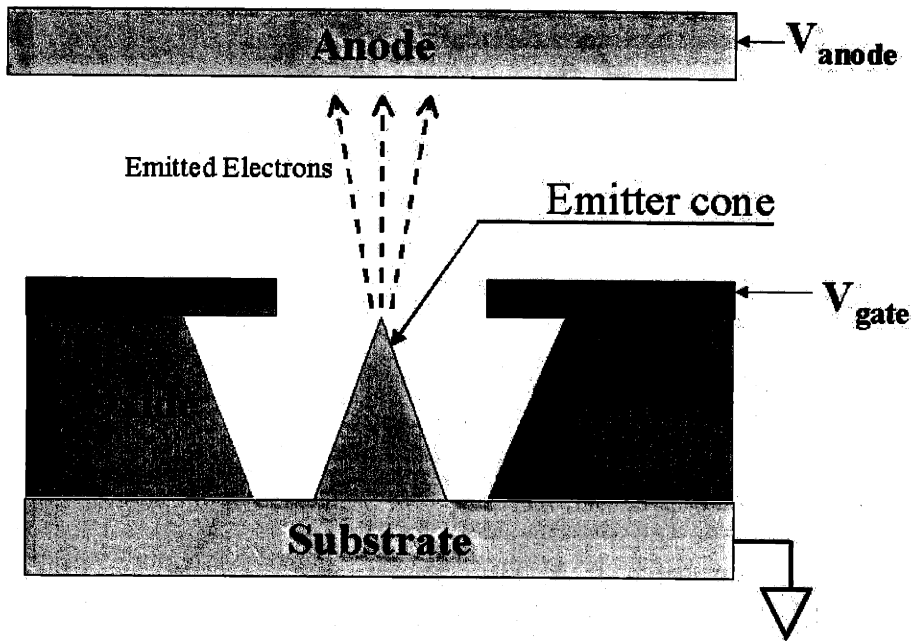


Figure 1-2: Schematic of the working principle of a field emitter.

## 1.2 Field emission arrays and flat panel display technology

### 1.2.1 The working principle of field emission arrays (FEAs)

The field emitter microstructure shown in figure 1-2 consists of a conical tip with a small radius that is located within a circular conducting gate aperture. The gate electrode is separated from the emitter substrate by an insulator, usually silicon dioxide ( $SiO_2$ ). When a sufficient large voltage (greater than the field emission turn-on voltage) is applied to the gate, electrons are extracted from the tip and are accelerated towards the anode by the large applied anode voltage. It is essentially a three terminal device in which the anode current is controlled by the applied gate voltage.

In practice there are also other types of emitter structures such as the ridge type field emitter and the thin film field emitter, which are described in Appendix F. The cone



shape emitter is the most widely used emitter structure in applications because it has the largest field enhancement effect (refer to section 2.8).

### 1.2.2 Field emission displays (FEDs)

There are genuine needs to develop a high efficiency, low cost and lightweight display technology. This is driven by the need to make displays more integrated with communication and computing. Field emission display proves to be a good candidate for this application.

Figure 1-3 is a schematic of a field emission display. A typical field emission display consists of two plates: the base plate and the face plate. The distance between the base plate and the face plate is only about  $200\mu m$  to  $1000\mu m$ . These two plates are separated by dielectric spacers in a vacuum envelope. The base plate consists of a two-dimensional array matrix of addressable FEAs arranged in rows and columns. The emitter cones are connected to the rows and the gates are connected to the columns. The matrix addressable FEAs are mini-electron guns which are proximity focused on the base plate.

The face plate consists of indium-tin-oxide (ITO) covered glass with a two dimensional array of phosphor dots corresponding to individual FEAs on the base plate. The phosphor dot and the corresponding FEA together form a pixel of the display. The emitted electrons from the FEA are accelerated to the face plate by the screen voltage. The electrons gain energy and generate hole-electron pairs in the phosphor. The hole-electron pairs form excitons and transfer their energy to activator ions which are dopants for the phosphor host lattice. Visible light is generated by the phosphor when the excited activator ions relax to the ground state. Typically the activator ions are rare earth elements (f-shell electron system) which have narrow band emission or transition metals (d-shell electron system) which have broad band emission.

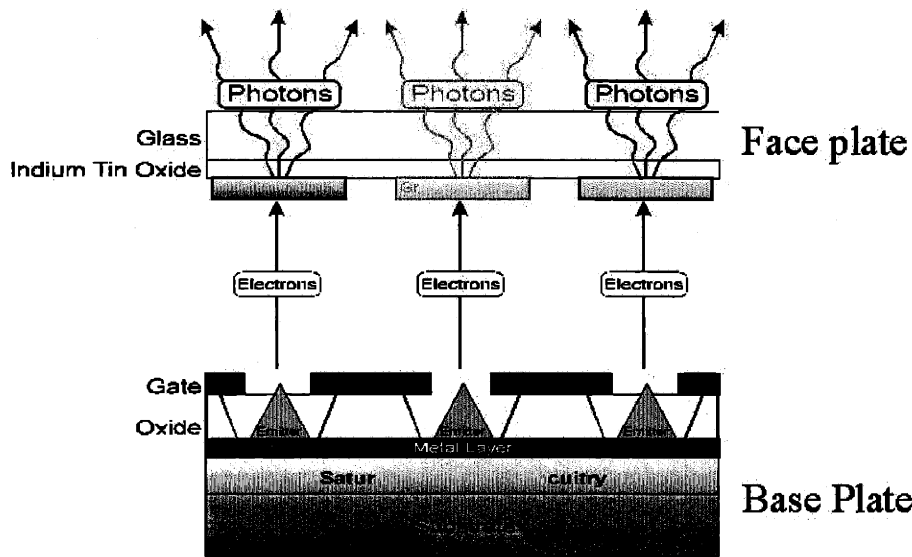


Figure 1-3: Schematic of a field emission display (FED)

A pixel is activated by the application of a row select voltage to the row connected to the pixel, and a data voltage to the column connected to the pixel, resulting in sufficient voltage difference between the gate and emitter tips, greater than the turn-on voltage for field emission. All non-activated pixels do not have sufficient voltage difference (less than threshold voltage) between their gates and emitter tips for field emission, hence the non-selected pixels remain dark.

The ability of matrix addressing and control of individual FEAs eliminates the need for bulky electron beam deflection mechanisms found in CRTs. Additionally, driving the display in a matrix addressable fashion can enable “smart” display design. A “smart” architecture, where each pixel has an embedded memory and is only addressed when necessary, can reduce the power consumption and increase the lifetime [9].

### Comparison to Cathode Ray Tube (CRT) display

A field emission display is essentially a “flat” and “thin” CRT (Cathode Ray Tube) display. Figure 1-4 shows the comparison between a CRT and a field emission display.

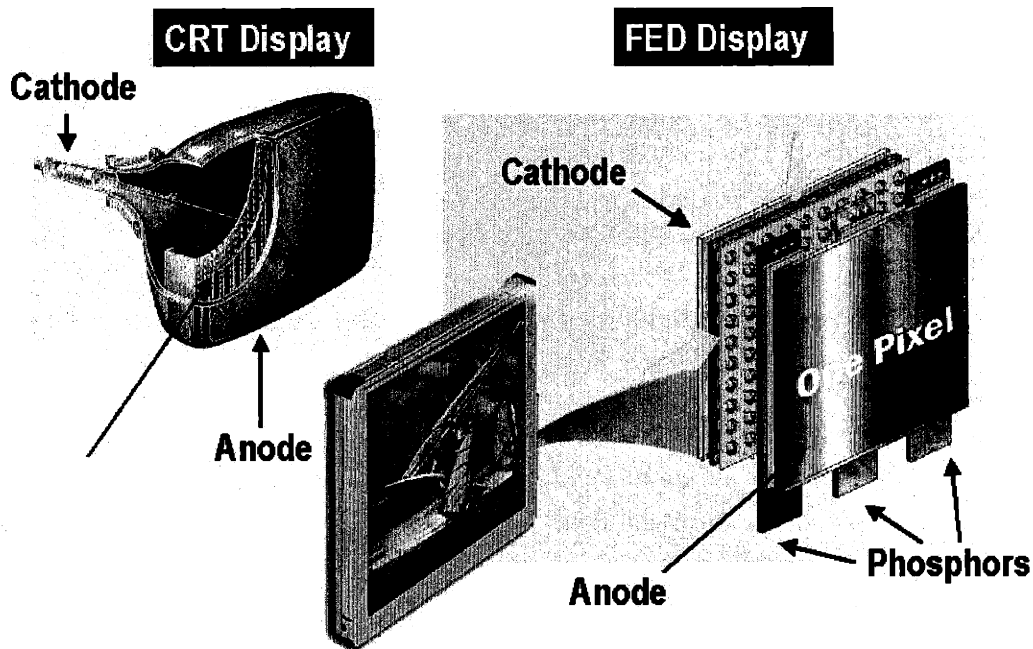


Figure 1-4: Comparison between CRT and FED. In a FED there are many microscopic electron guns—field emitters, in contrast to the case in a CRT where there is only one electron gun. The emitter array provide redundancy in case some emitters in the array are not functional. Courtesy:PixTech.

Like the CRT, the field emission display is based on cathodoluminescence.

The CRT is a large vacuum envelope with a single electron gun—the thermionic electron emission source. The source is heated so that the electrons gain enough energy to overcome the energy barrier at the surface. Then electrons are accelerated to the phosphor screen. A single electron beam is rastered over the entire screen by magnetically deflecting the beam. However, CRTs are bulky, heavy, and have high power consumption. The deflecting mechanism determines that CRTs can not be made with a thin profile. Furthermore, the sequential drive mechanism does not translate the very high spot brightness obtained from cathodoluminescence into high average screen brightness.

Arrays of field emitters, on the other hand, could provide an electron source in proximity to the phosphor screen. In CRT there is only one electron gun rastered over the entire screen. In FED, instead of only one electron gun, there are many many mi-

croscopic electron guns:field emitters. An array of these electron guns, a field emitter array, corresponds to one pixel on the screen. The emitter array provides redundancy in case some emitters in the array are not functional. The field emission display has all the advantages of a CRT such as: high brightness, high luminous efficiency, high dynamic range in brightness (nonlinear voltage response), flat profile, wide viewing angle, and high spatial resolution. It also combines the positive attributes of flat panel display technologies, such as: a thin profile, matrix addressing, higher screen brightness, light weight, and low power.

This research work will focus on the field emitter array part (the base plate) of the flat panel field emission display structure.

## **1.3 Statement of the problem**

### **1.3.1 Understanding field emission from semiconductors**

Most studies of field emission have concentrated on metal emitters. There were a lot of experimental data of metal field emitters and the data agreed well with Fowler-Nordheim theory [18, 38] which we will discuss in detail in the next chapter. However, field emission from semiconductors has not been studied as much, partly due to the difficulties with fabrication.

Along with the phenomenal growth and development of integrated circuit (IC) technology starting from the 70's, the processing technologies of semiconductor materials have since improved dramatically. The mature and uniform semiconductor processing and fabrication technologies, especially in the case of silicon, have made it possible to fabricate high quality semiconductor field emitters. Field emission research in semiconductor emitters has since attracted a lot of attention and has been very active in the past ten years. However, the majority of the reported work in semiconductor

field emission has focused on the fabrication technology rather than the device physics. The theory of field emission from semiconductors was developed during the 50's and 60's, largely by Stratton [61, 62]. However, many predictions of the theory, such as the valence band electron emission, are not confirmed [46, 61, 62, 137]. Furthermore, experimental data showed deviations from Fowler-Nordheim theory. Current saturation in p-type semiconductor has been observed [124, 125, 126, 127, 128, 130], but the mechanism is not fully understood. Current saturation in n-type semiconductors has been predicted [123, 129], but not fully observed.

In this work we will try to address some of these issues experimentally, further expanding the knowledge and understanding of field emission from semiconductors.

### **1.3.2 Advance the silicon field emitter technology**

Improving the quality and performance of microelectronic devices has challenged both physicists and electrical engineers for decades. It will continue to do so. One of the goals in our research is to advance the fabrication technology for field emission arrays.

Silicon is a promising material for field emission applications for several reasons:

- The conductivity of silicon can be easily changed by different levels of doping;
- The mature silicon processing technologies provided necessary conditions for building high quality silicon field emitter arrays;
- It is easier to integrate a silicon field emitter with the also silicon-based Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFET) driver circuitry [65, 66]. Figure 1-5 shows the schematic of the integration of the field emitter with field effect transistor circuitry.
- Certain silicon processing techniques such as oxidation sharpening [76, 77] makes it easier to produce very sharp emitter tips, an essential element for

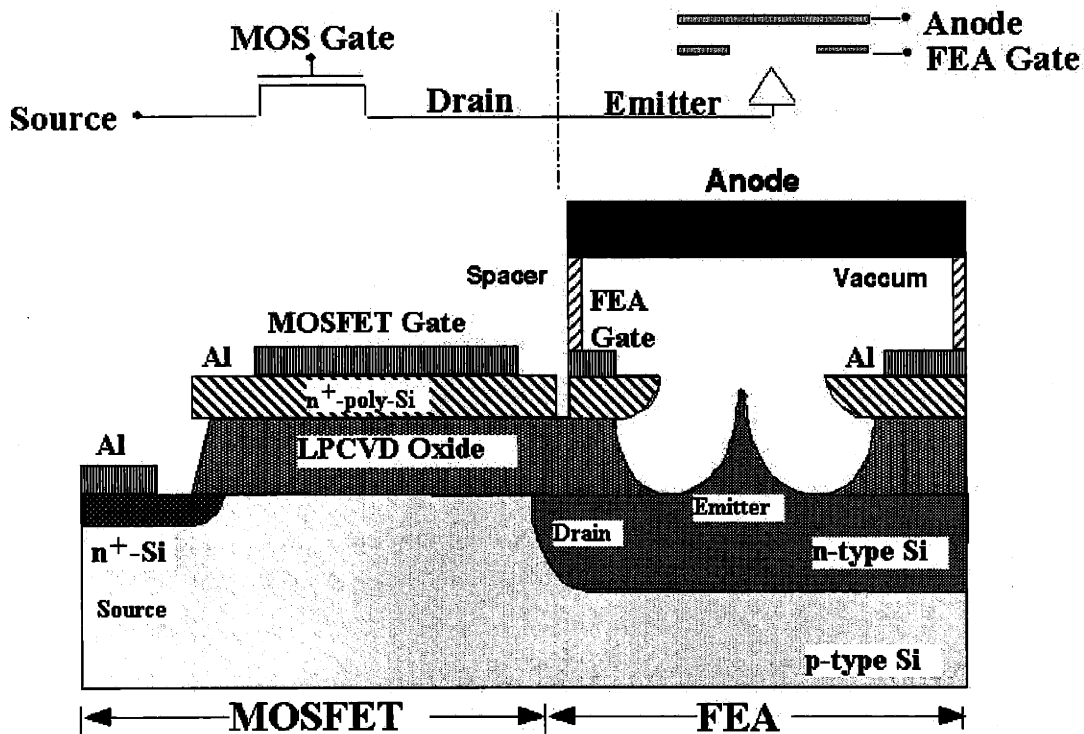


Figure 1-5: Schematic of a field emission display (FED) integrated with field effect transistor (FET). The transistor is biased as a constant current source. It supplies electrons to the field emitter thereby stabilizing emission current density and uniformity.

field emitters to operate at low voltages.

### Device performance criteria for FEAs

The device performance criteria for FEAs are: (1) low turn-on voltage, i.e., low operating voltage, (2) high current density and high transconductance, and (3) uniformity. We will elaborate on these points below.

**Low operation voltage** Low operation voltage will improve the overall performance of the field emission display in the following ways:

- Lower operating voltage reduces the energy stored in a field emission microstructure. The gated emitter structure resembles a capacitor. The energy stored is

$$E = \frac{1}{2}C_g V_g^2$$

where  $C_g$  is the capacitance and  $V_g$  is the gate voltage. The lower operating voltage will thus increase the burnout resistance due to less energy stored in the structure. This will greatly increase the life-time of the emitters.

- Lower operating voltage reduces the power dissipation in the addressing electronics. The power dissipated in the addressing electronics is calculated as

$$P = C_L V_g^2 f$$

where  $C_L$  is the load capacitance,  $f$  is the switching frequency. Decreasing operation voltage  $V_g$  will decrease energy dissipated in the system, thus increase the overall power efficiency of the display.

- Low operating voltage makes it easier to integrate FEAs with MOSFETs. This will enable the fabrication of CMOS logic, memory, and FEAs on a single silicon wafer. An advantage of such a technology is the integration of small displays with other electronic circuits to form a “system-on-a-chip”.

**High current density and high transconductance** The high current density and high transconductance will affect the performance of field emission displays in the following ways:

- The brightness of the display is directly proportional to the number of electrons hitting the phosphor screen, i.e., the current density of the emission current.
- The high frequency performance of the FEA is improved if it has high transconductance. The frequency at which a field emission electron source can operate

is limited by the unity current gain cutoff frequency defined by:

$$f_{cutoff} = \frac{g_m}{2\pi C_g}$$

where  $g_m$  is the transconductance:

$$g_m = \frac{dI}{dV_g}$$

with  $I$  the emission current.  $g_m$  measures the rate of change of emission current as a function of gate voltage  $V_g$ .  $C_g$  is the gate capacitance mentioned before. It is apparent that a high transconductance increases the cutoff frequency of the device.

Good uniformity is very important for the overall performance of the field emission displays in the sense that we want every field emitter array to work in exactly the same way. This is essential for the spatial uniformity of the whole display. Also good uniformity will lead to a high mass production yield of field emission displays.

## 1.4 Objectives of this work

Based on the discussion above, this thesis work has two objectives:

- Extend our knowledge and understanding of the physics of electron field emission from semiconductors.
- Develop high performance silicon field emitter arrays for potential applications of field emission devices and advance the semiconductor FEA device design and fabrication.



## 1.5 Organization of the thesis

In chapter 2, the theory of field emission from metals and from semiconductors will be described. In chapters 3 and 4, the low- and high-aspect ratio silicon field emitter arrays fabrication, characterization, and device results will be described. Analytical and numerical simulation models are presented to explain the experimental results. Discussions of the breakdown mechanism of silicon field emitter arrays will also be presented. In chapter 5, current saturation and valence band field emission of silicon field emitter arrays will be reported. In chapter 6, the principle and the setup of the Scanning Maxwell Microscope will be described. Chapter 7 summarizes the thesis and gives recommendations for future work. Appendices provide fundamental physical data of materials, detailed derivation of formulae, and more information on device fabrication process flow.

# Chapter 2

## Theory of electron field emission

### 2.1 Work function of solids

Inside a metal, the behavior of electrons could be approximately described by the free electron gas model. The electrons move freely inside the metal. Electrons are unable to come out of the metal surface freely because there is a potential barrier at the surface. This surface barrier is called the work function. It represents the difference in energy between the highest normally occupied electron energy level inside the metal and the state of an electron at rest outside the surface. The phenomenon of electron emission occurs when electrons overcome this surface barrier and come outside of the surface.

The work function plays a decisive role in all electron emission phenomena. The work function of a metal depends both on its bulk properties and on the characteristics of its surface. The energy difference involved in the definition of the work function can be divided into two parts:

1. the energy of the highest filled level in the metal relative to the mean electro-

static potential inside the metal, and

2. the difference between this interior potential and the potential outside.

The former has nothing to do with conditions at the surface and thus involves only the bulk properties of the metal; the latter involves the surface and is influenced by surface structure [22].

Before 1960's, the electron theory of metals has always been primarily concerned with properties of the metal interior. These bulk properties are of great fundamental interest and the translational invariance prevailing inside the metal provided important elements of simplicity into calculations. The theory of bulk metal properties gives a quantitatively accurate description of wide classes of metals [21]. However, the theory of metal surfaces had lagged far behind at that time. This has been primarily due to the additional difficulties introduced by the rapid decrease of electron density near the surface and by the loss of translational symmetry.

In metals, the positive charges are fixed in space, and they can not move. However, electrons can move freely. So the positive charge density is constant up to the surface and zero beyond the surface. It is a step function. The electron density equals the positive density in the deep interior, but falls gradually rather than suddenly to zero as the surface is crossed. The result is a double layer, with an excess of negative charge just outside the surface and an excess of positive charge just inside. Figure 2-1 shows a schematic of this charge density configuration [32].

This double layer produces an electrostatic potential which results in a positive energy barrier that makes it difficult for electrons inside to escape from the surface. However, the work function does not only come from this double layer "dipole" potential. Inside the metal, according to the theory of the interacting electron gas [23, 24], the exchange and correlation energy will lower the potential in the interior of the metal. Outside the surface, the combined potential of the exchange and correlation forces should be taken over by the classical image potential [25, 26] that an electron experiences

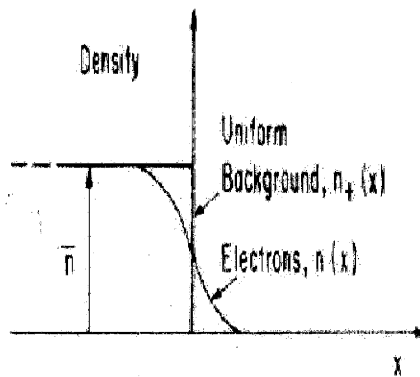


Figure 2-1: Schematic of the charge density distribution at a metal surface. A double layer is formed by an excess of negative charge just outside the surface and an excess of positive charge just inside.

outside of the surface. In the intermediate region the potential connects smoothly across the surface [25, 26]. Bardeen made an important contribution to the theory of metal surfaces in 1936 by performing an approximately self-consistent calculation for the metal sodium [25]. The wave functions of the conducting electrons of the sodium crystal are, except in the immediate vicinity of the ions, very nearly the same as those of perfectly free electrons [25]. By taking the exchange and correlation energy and the surface “dipole” layer potential energy into the free electron gas model, Bardeen self-consistently calculated the work function of sodium to be about  $2.35\text{eV}$ , which agree well with the experimental value of  $2.46\text{eV}$ . However, after Bardeen’s work, there was almost no progress in the theory of metal surfaces for thirty years. During the middle 1960’s the development of the density functional theory by Kohn et al. greatly advanced the treatment of electron systems, especially in “inhomogeneous” electron gas systems [27, 28, 29, 31]. Based on this theory, Lang and Kohn [32] developed a self-consistent scheme for calculating the work function for metals, taking into consideration the exchange and correlation energy, surface double layer “dipole” potential, and the image potential. They developed their method based on the “jellium model”: a model of metals in which the positive ionic charges inside the metal are replaced by a uniform charge background of positive charge density [23]. Their results of the calculated work function quantitatively agreed with the experimental

results of many metals. This method laid down the foundation of calculating work functions and has been constantly improved and modified by authors subsequently [33]. For a detailed derivation of the self-consistent method, please refer to [32] for a insightful description.

## 2.2 Methods of electron emission from surface

Any process of electron emission involves getting electrons to overcome the work function. This section describes the methods of electron emission from a surface.

Electrons could be removed from solids by:

1. providing them with sufficient kinetic energy to surmount the potential barrier at the surface of the solid, or
2. reducing the height of or thinning the barrier, so that the electrons can penetrate the barrier and escape by virtue of their wave characteristics: tunneling [34].

Sufficient kinetic energy may be given to electrons by the application of heat, resulting in thermionic emission, or by the absorption of light quanta of sufficient energy to cause photo-electric emission. Reduction and thinning of the barrier could be brought about by the application of high electric fields to the surface, leading to field emission. Finally, electron emission from solids can also be caused by the incidence of energetic particles, such as electrons, positive ions, metastable atoms, and neutral atoms.

Figure 2-2 is a schematic of the electron energy versus position inside a metal. It is convenient to consider a metal as a box within which the potential energy of an electron is lower than that of an electron outside by an amount  $\delta$ , as illustrated. Here,  $\delta$  is the distance between the bottom of the metal conduction band and the vacuum level. In the box, at absolute zero temperature, the electrons have kinetic energies

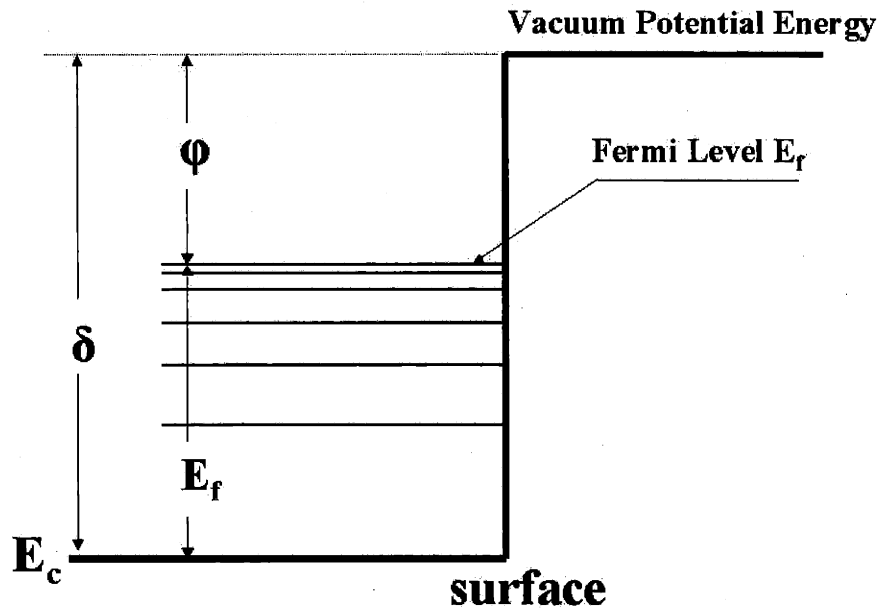


Figure 2-2: Schematic of the electron energy diagram in a metal.  $E_f$  is the Fermi level of the electron inside the metal;  $\varphi$  is the work function of the metal. The work function is the work necessary to remove an electron from the metal.

which are distributed up to the Fermi level  $E_f$ . The distance between the Fermi level  $E_f$  and the vacuum potential level is the work function  $\varphi$ , which is the work necessary to remove an electron from the metal.

In the following text we will briefly describe thermionic electron emission and photo electron emission. We will later focus our discussion on electron field emission; we will consider first the electron field emission from a metal, and then the electron field emission from semiconductors.

## 2.3 Thermionic electron emission

At zero temperature the electron distribution function has the form of a step function:

$$n(E) = \begin{cases} 1 & E < E_f \\ 0 & E > E_f \end{cases} \quad (2.1)$$

At finite temperature, the step distribution function becomes smoother as electrons can be excited to occupy energy levels higher than the Fermi level. The energy distribution function is given by the Fermi-Dirac distribution function [30]

$$n(E) = \frac{1}{e^{\frac{E-E_f}{k_B T}} + 1} \quad (2.2)$$

where  $n(E)$  is the probability of occupation (average number of electrons) of a state with energy  $E$ ,  $E_f$  is the Fermi level mentioned above and illustrated in figure 2-2,  $k_B = 1.38 \times 10^{-23} J/K$  is the Boltzmann constant, and  $T$  is the absolute temperature. It is convenient to assume that without the presence of an external electric field, i.e., the vacuum level remains flat at the surface, and only electrons with energy levels higher than the vacuum level are able to jump over the barrier into the vacuum. This is understandable because the tunneling probability of a electron through an infinitely wide barrier is zero.

When the temperature  $T$  is very low, the density of electrons that have energy higher than the vacuum level is extremely small, and therefore the electron emission from the material is undetectable. When the material is heated, more electrons will be thermally excited to occupy energy levels higher than the vacuum level. Thus thermionic electron emission occurs. Figure 2-3 is a schematic of the thermionic electron emission.

Richardson and Dushman [35, 36, 37] investigated electron emission from metals at high temperatures and developed a thermodynamical theory from which they related the current density  $J$  to the absolute temperature  $T$  of the metal. They showed that:

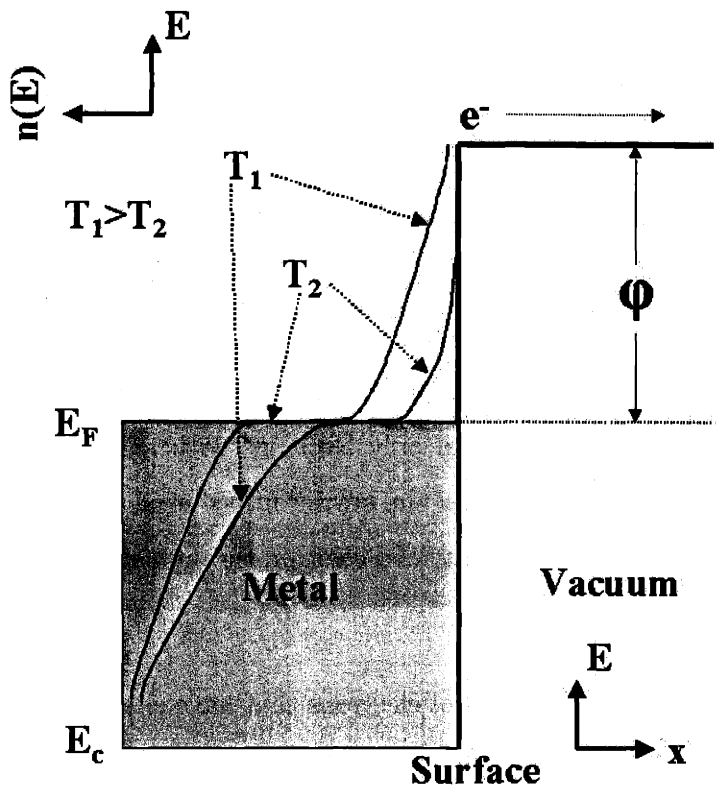


Figure 2-3: Schematic of thermionic electron emission. At higher temperature  $T_1$  there are more electrons that occupy energy levels higher than the vacuum level, thus resulting in a greater degree of thermionic electron emission.



$$J = AT^2 \exp(-\varphi/k_B T) \quad (2.3)$$

where  $\varphi$  is the work function.  $A$  is a constant having the following form

$$A = \frac{4\pi m e k_B^2}{h^3} \approx 120 \frac{\text{Amps}}{\text{cm}^2 \text{K}^2} \quad (2.4)$$

where  $h = 6.63 \times 10^{-34} \text{J} \cdot \text{s}$  is the Planck's constant,  $m$  is the electron mass,  $e$  is the electron charge.

Nordheim [39, 41, 42] obtained a similar formula by considering the possibility that an electron can be reflected back into the metal after escaping from the metal:

$$J = A(1 - r)T^2 \exp(-\varphi/k_B T) \quad (2.5)$$

where  $r$  is the probability that electrons which have sufficient energy to get over the barrier are reflected back.

Owing to the predominance of the exponential term, it is not easy to distinguish experimentally between the difference forms of the equations 2.3 and 2.5.

## 2.4 Photo electron emission

It was observed long ago that the incidence of ultra-violet light upon a metal caused the emission of electrons. Einstein [43] suggested that light could be regarded as being made up of quanta, each of energy  $h\nu$  where  $\nu$  is the frequency of the light wave. Moreover, it is assumed that the quanta transferred their energy *in toto* to the electrons in the metal. Therefore, if the photon imparts enough energy to the

electron, sufficient to overcome the barrier at the surface, the electron can escape from the material. Hence, if  $h\nu < \varphi$ , the electron will not escape from the material; if  $h\nu > \varphi$ , an electron at the Fermi level could escape with energy

$$E_1 = h\nu - \varphi \quad (2.6)$$

This equation has been verified by Millikan [44].

The electron emission current density of photo emission is mainly decided by the intensity of the incoming light, i.e., the number of photons incident on the surface provided that the frequency of the light wave is greater than  $\varphi/h$ . Other factors affecting the emission include the absorption coefficient.

Figure 2-4 is a schematic of the photo electron emission process.

## 2.5 Schottky Emission

Under applied electric fields the work function is effectively reduced to,

$$\varphi' = \varphi - e^{\frac{3}{2}} F^{\frac{1}{2}} \quad (2.7)$$

where  $F$  is the electric field. This is also called the "Schottky Lowering" in the literature. Thus if  $I_0$  is the emission from zero field at a temperature  $T$ , i.e.,  $I_0 = AT^2 \exp(-\varphi/k_B T)$ , then  $I_F$ , the current for a field  $F$ , is

$$I_F = I_0 e^{\left(\frac{e^{\frac{3}{2}} F^{\frac{1}{2}}}{k_B T}\right)} \quad (2.8)$$

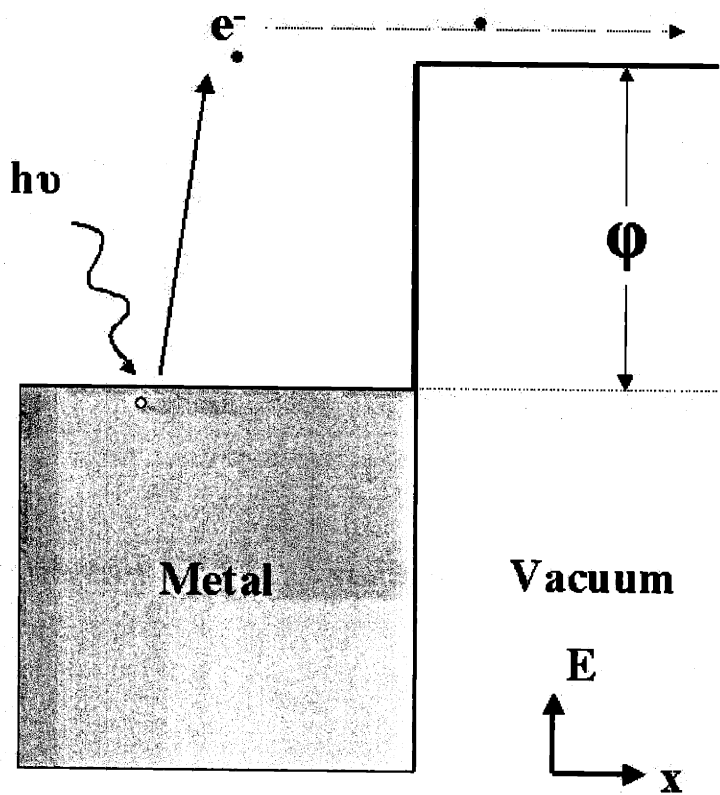


Figure 2-4: Schematic of the photo electron emission. An electron absorbs energy quanta  $h\nu$  from the incident photon, gaining enough energy to overcome the surface barrier and escape from the barrier.

This relation which was derived by Schottky [48] has been shown to be valid over a wide range of temperatures and for fields up to  $10^6 V/cm$  [49]. But calculation of the Schottky emission at room temperature for metals shows that Schottky emission is negligible even when fields as high as  $10^6 V/cm$  are applied. Under this situation, electrons do not have to surmount the reduced potential barrier of height  $\varphi$ , but can by virtue of their wave properties tunnel through the potential barrier. This is known as the tunneling effect and is the onset of the field emission which will be discussed in detail in the following section.

The origin of Schottky Lowering comes from the image potential that an electron experiences near a conducting surface. We will discuss image potentials in section 2.6.2 within the framework of the theory of field emission. There, we can get a clearer picture of how Schottky Lowering occurs.

Figure 2-5 is a schematic of Schottky Emission.

## 2.6 Electron emission from a metal and the Fowler-Nordheim theory

Electron field emission from a solid can be characterized as having two continuous processes:

1. Electron flux to the surface of the emitters, determined and limited by the electron supply,
2. Electron tunneling through the surface potential barrier, determined by the tunneling transmission coefficient.

These processes are illustrated in Figure 2-6. After the electrons come out of the solid's surface and go into the vacuum, they could be accelerated, focused, bunched

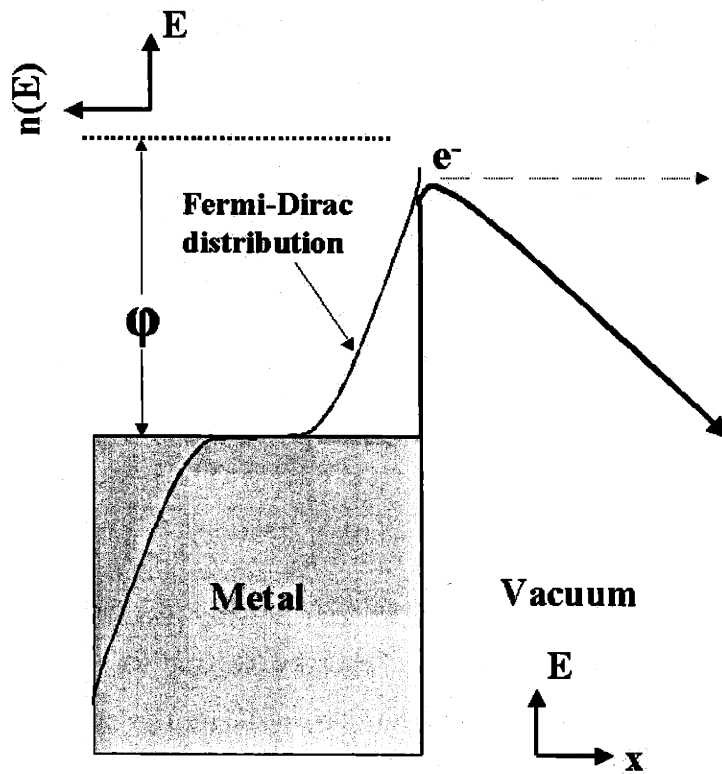


Figure 2-5: Schematic of Schottky Emission.

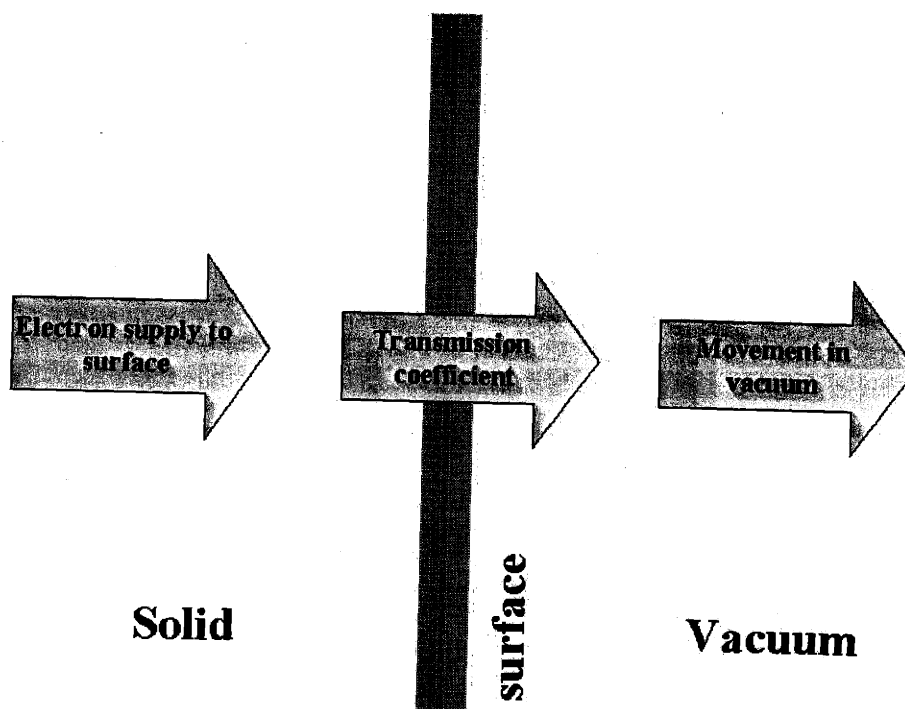


Figure 2-6: The field emission of electrons from a solid can be broken down into electrons incident on the surface, transmission through the surface barrier and the movement of the electrons in the vacuum.

or manipulated, based on the application of interest.

The field emission process is treated by considering a one-dimensional potential barrier. This potential barrier was originally proposed by Schottky [48] and was used by Nordheim [39, 45] in his modification of the original Fowler-Nordheim theory.

From figure 2-2 we can see that at room temperature, the potential barrier at the surface of the metal has a infinite width, thus preventing electrons from coming out of the surface. When an external electrical field is applied, the vacuum level is bent and the barrier width is no longer infinite. Figure 2-5 and figure 2-9 show the schematic of the bending of the vacuum level in the presence of an external electric field. Electron field emission occurs when the vacuum level bending is so much that the barrier width is small enough for the electrons inside the metal to tunnel through the barrier. Typically, a barrier width of about  $20\text{\AA}$  will result in

appreciable tunneling probability.

### 2.6.1 An intuitive argument from the uncertainty principle

Tunneling is a purely quantum-mechanical phenomenon with no classical analogue. It can be reconciled with macroscopic intuition by the Heisenberg uncertainty principle [46]. A knowledge of the momentum of an electron within an uncertainty  $\Delta p$  implies a corresponding uncertainty  $\Delta x$  in its position, given by

$$\Delta p \cdot \Delta x \cong \hbar/2 \quad (2.9)$$

where  $\hbar = h/2\pi$ ,  $h$  being Planck's constant. If we consider electrons near the Fermi level, the pertinent uncertainty in momentum is that corresponding to the barrier height  $\varphi$ ,  $(2m\varphi)^{\frac{1}{2}}$ . The corresponding uncertainty in position, according to equation 2.9, is

$$\Delta x \cong \hbar/2(2m\varphi)^{\frac{1}{2}}. \quad (2.10)$$

With the presence of an external electric field, the barrier width is given by

$$x = \varphi/Fe. \quad (2.11)$$

If the uncertainty in position (equation 2.10) is of the order of the barrier width (equation 2.11) there will be a good chance of finding an electron on either side of it. This can be expressed by requiring that

$$\varphi/Fe \cong \hbar/2(2m\varphi)^{\frac{1}{2}} \quad (2.12)$$

or that

$$2\left(\frac{2m}{\hbar^2}\right)^{\frac{1}{2}} \frac{\varphi^{\frac{3}{2}}}{Fe} \approx 1.$$

So the field required to extract electrons out from the metal is estimated as

$$F \approx \frac{2(2m)^{\frac{1}{2}}\varphi^{\frac{3}{2}}}{e\hbar} \quad (2.13)$$

A direct calculation of equation 2.13 gives rise to a field of  $8.34 \times 10^8 V/cm$ , assuming  $\varphi = 4.05eV$  for the case of the conduction band electron of silicon. This value is approximately 40 times larger than the actually needed field for field emission.

### 2.6.2 Image potential - modification of the simple triangular potential barrier model

An electron ( $-e$ ) outside a conducting plane experiences an image charge ( $+e$ ) force, because the electron induces positive charges on the surface of the conducting plane [63]. As it moves around, the electron experiences a potential created by its image charge. Figure 2-7 shows the schematic of the image charge.

The electrostatic force the electron experiences in front of a conducting plane is equal to the electrostatic force between the electron and the image charge. Taking the positive  $x$  direction to be the direction pointing from the plane to the electron, the electric force the electron experiences is equal to



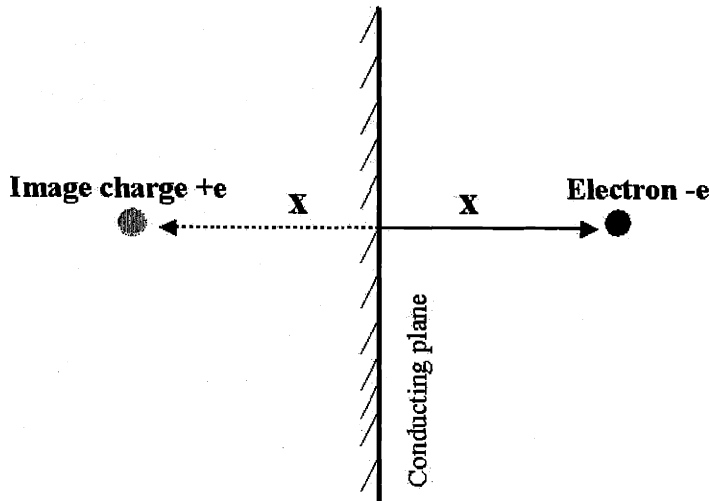


Figure 2-7: Schematic of the concept of the image charge of an electron sitting in front of a conducting plane. The image charge has the opposite sign of the electron, and the distance between the image charge and the plane is equal to the distance between the electron and the plane.

$$F = -\frac{e^2}{(2x)^2} = -\frac{e^2}{4x^2}. \quad (2.14)$$

Assuming that the potential approaches to zero when the electron is infinitely far away from the conducting plane, i.e.,  $V_{image}(+\infty) = 0$ . Then the potential  $V_{image}(x)$  is given by

$$V_{image}(x) = -\int_{\infty}^x -\frac{e^2}{4x^2} = -\frac{e^2}{4x}. \quad (2.15)$$

We also use equation 2.15 to describe the image potential that an electron experiences when it is outside of the surface of a field emitter [26, 46].

Equation 2.15 holds, of course, only so long as  $x$  is large. The potential diverges at  $x = 0$  and this result is not physical.  $x$  must be large enough so that the surface of the metal can be treated as an ideal equipotential plane. When  $x$  becomes comparable to the inter-atomic distance in the metal, the electron density deficiency produced by

repulsion of the electrons in the metal away from the test charge will be spread out over a depth comparable with  $x$  itself, and the force on the test charge will be less than that given by the image potential [22]. If the test charge is placed inside the metal, its potential will be primarily determined by the exchange and correlation energy of the interacting electron gas and the dipole potential of the double layer and will have a constant value,  $\delta$ , as depicted in figure 2-2. In the middle transition region, the potential varies smoothly between its value inside the metal and its value outside the metal over a distance that is comparable to the inter-atomic distance [22, 39]. In the later sections (2.6.4) we can see that the details of the form of the image potential near  $x = 0$  have a negligible effect on the results of the kinetic formulation of electron field emission from a metal. For a more detailed theoretical consideration and treatment of the image potential near a metal surface, please refer to [25, 26, 32, 33, 39].

### Schottky lowering

One of the direct consequences of the image potential is the so-called Schottky Lowering effect [39, 48, 49]. Figure 2-8 shows a schematic of the effect. Figure 2-8 (a) shows the potential energy without the image potential nor the external electric field. The barrier height is the work function  $\varphi$ . Figure 2-8 (b) shows the potential energy with an external electric field, but without an image potential. The barrier height is also  $\varphi$ , but narrower. Figure 2-8 (c) shows the potential energy with an image potential, but without the external electric field. The steep potential discontinuity at the surface is rounded, but the barrier height remains at  $\varphi$ . Figure 2-8 (d) shows the potential energy with both image potential and external field. In this case, the potential barrier at the surface is actually decreased and is narrower. This effect is called Schottky Lowering. The simple calculation can give the lowering to be

$$\Delta\varphi = -\sqrt{e^3 F} \quad (2.16)$$

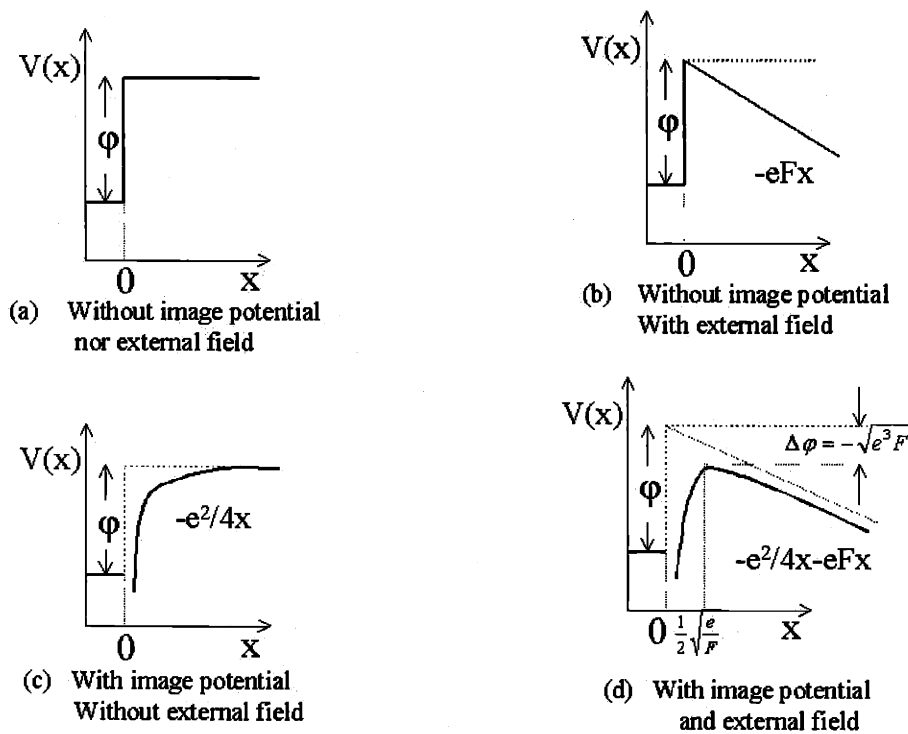


Figure 2-8: Schematic of Schottky Lowering. (a) Without image potential nor external electric field. The barrier height is the work function  $\phi$ . (b) With external electric field, but without image potential. The barrier height is also  $\phi$ . (c) With image potential but without the external electric field. The steep potential discontinuity at the surface is rounded, but the barrier height remains at  $\phi$ . (d) With both image potential and external field, the potential barrier at the surface is decreased by  $\Delta\phi = -\sqrt{e^3 F}$ .

at the position

$$x = \frac{1}{2} \sqrt{\frac{e}{F}} \quad (2.17)$$

Schottky lowering is the source of the so-called Schottky emission briefly described in section 2.5. When the external electric field is small, the work function (surface barrier) of the metal surface is effectively lowered, resulting in equation 2.7. The net effect is increased thermionic electron emission, resulting in equation 2.8. In the presence of a strong external electric field, field emission predominates.

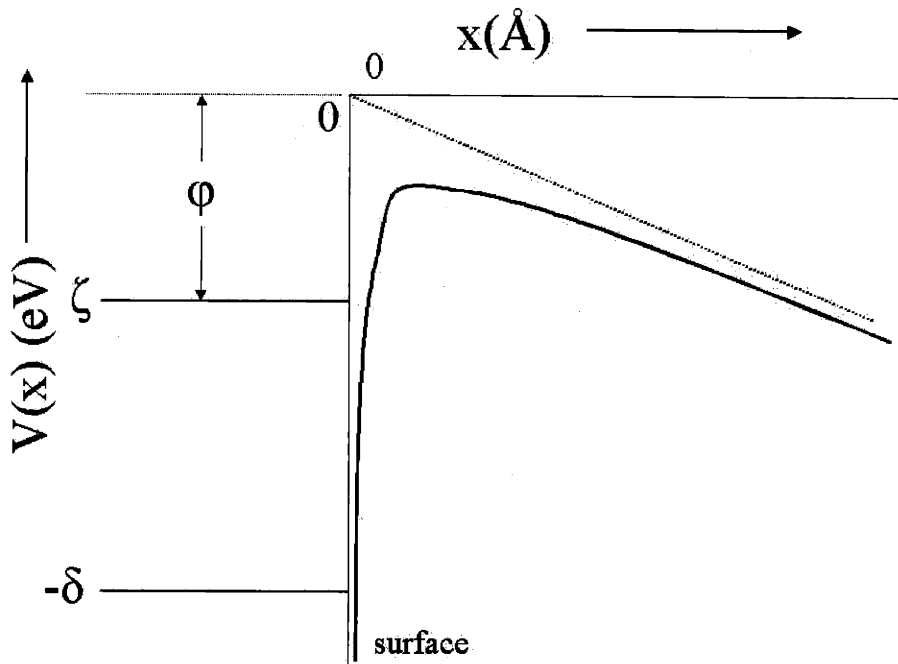


Figure 2-9: Schematic of the potential barrier near a metal surface with the presence of an external electric field.  $-\delta$  is the constant potential inside the metal,  $\zeta$  is the electron Fermi level,  $\varphi$  is the work function. The energy zero point is set to be the vacuum energy level at the surface. The dashed line represents the potential energy of the external field, and the solid curve is the total potential energy including the image potential. The positive directions of  $x$  and  $V(x)$  are shown as the arrows indicate.

### 2.6.3 Formulation of the surface potential barrier

Figure 2-9 illustrates the profile of the potential energy an electron experiences in the case of electron field emission.

Based on the discussion above, there are three contributions to the surface potential barrier:

1. Within the metal the potential energy has some constant value  $-\delta$  relative to zero (here the zero point is the vacuum energy level). This energy is lower than the Fermi Level  $\zeta$  in metals.
2. An external electric field  $F$  is applied to narrow the potential barrier, allowing

the electrons to tunnel out of the metal. The origin will be chosen to be on the metal surface and the positive  $x$ -axis perpendicular to the surface and out of the metal. This field gives a contribution of  $-eFx$  to the potential barrier. It is presumed that the free charges cause this field to be neutralized within the metal and so it applies only outside, i.e., for metals, there is no field penetration. The zero point is chosen so that this contribution to the potential is zero when the applied field is zero.

3. The image potential  $-\frac{e^2}{4x}$  as obtained in section 2.6.2. The potential energy is chosen to be zero when the electron is far from the metal. This energy also applies only to electrons outside the metal.

These three contributions give

$$V(x) = \begin{cases} -\delta & \text{where } x < 0 \\ -eFx - \frac{e^2}{4x} & \text{where } x > 0 \end{cases} \quad (2.18)$$

for the effective potential barrier.

It is noticed that equation 2.18 is not continuous at  $x = 0$ . As it is discussed in section 2.6.2, the potential inside the metal should smoothly connect with the potential outside the metal. However, for our subsequent discussion and derivation, this potential is not expected to have significance at the point  $x = 0$ . In the following section it will be demonstrated that the electron field emission current density is dependent on an integral of the square root of the potential at the Fermi Level over a range of  $x$  that excludes  $x = 0$ . For simplicity, equation 2.18 is retained as the expression of the surface potential barrier.

The main features of field emission can be understood from the shape of the potential outside the metal only. The maximum value of the potential is found by differentiation to be at the point

$$x_0 = \frac{1}{2} \sqrt{\frac{e}{F}} \quad (2.19)$$

and the corresponding maximum value of  $V(x)$  is

$$V_{max} = -\sqrt{e^3 F} \quad (2.20)$$

Under practical conditions this maximum remains above the Fermi energy  $\zeta$ .

It is observed that equation 2.20 is exactly equal to the Schottky lowering of the work function under an external field, as described in equation 2.7.

#### 2.6.4 Fowler-Nordheim tunneling theory

In their theory of field emission, Fowler and Nordheim assumed: (i) the “free” electron gas model for the conduction electrons, and (ii) the effective potential model of the metal presented in equation 2.18, and made an additional physical assumption that the electrons inside the metal remain essentially at equilibrium, in spite of the electrons that are escaping from the metal. Under this set of assumptions, the current of electrons is found by integrating over all electron energies, the equilibrium flux of electrons incident on the surface times the probability that an electron penetrates the barrier.

The total energy of an electron under the surface potential energy is found, by noting that  $p_x$ ,  $p_y$ , and  $p_z$  are the momentum components of the electron in  $x$ ,  $y$ , and  $z$  directions

$$\epsilon = \frac{p_x^2}{2m} + \frac{p_y^2}{2m} + \frac{p_z^2}{2m} + V(x). \quad (2.21)$$

Then this integral can conveniently be written in terms of the  $x$ -part of the energy  $W$ , defined by

$$\left. \begin{aligned} W &= \varepsilon - \frac{p_y^2}{2m} - \frac{p_z^2}{2m} \\ &= \frac{p_x^2}{2m} + V(x) \end{aligned} \right\} \quad (2.22)$$

All energies will be measured from the same reference as the effective potential  $V(x)$ . Then, if  $N(W)dW$  is the number of electrons with the  $x$ -part of their energy within  $dW$  incident on the surface per second per unit area, and  $D(W)$  is the probability of transmission through of the barrier, the product  $P(W)dW$  gives the number of electrons within  $dW$  that emerge from the metal per second per unit area

$$P(W)dW = D(W)N(W)dW \quad (2.23)$$

and  $j$ , the electric current per unit area, is

$$j = e \int_{-\delta}^{\infty} P(W)dW. \quad (2.24)$$

The function  $N(W)$  is called the supply function and  $D(W)$  is called the transmission coefficient.

The supply function can be calculated (refer to appendix D for a detailed derivation) to be

$$N(W) = \frac{4\pi mkT}{h^3} \ln(1 + e^{-\frac{W-\zeta}{kT}}). \quad (2.25)$$

The transmission coefficient is calculated using the WKB approximation [55, 56, 57] (refer to appendix D for a detailed derivation):

$$D(W) = e^{-\frac{4\sqrt{2m}|W|^3}{3\hbar e F}} v(y) \quad (2.26)$$

where

$$v(y) = 2^{-\frac{1}{2}} \sqrt{1 + \sqrt{1 - y^2}} E(k) - (1 - \sqrt{1 - y^2}) K(k) \quad (2.27)$$

$$K(k) = \int_0^{\pi/2} \frac{d\varphi}{\sqrt{1 - k^2 \sin^2 \varphi}} \quad (2.28)$$

$$E(k) = \int_0^{\pi/2} \sqrt{1 - k^2 \sin^2 \varphi} d\varphi \quad (2.29)$$

$$k^2 = \frac{2\sqrt{1 - y^2}}{1 + \sqrt{1 - y^2}} \quad (2.30)$$

and

$$y = \frac{\sqrt{e^3 F}}{|W|}. \quad (2.31)$$

The number of electrons within  $dW$  that emerge from the metal per second per unit area is found by combining equation 2.25 and equation 2.26 according to equation 2.23:

$$P(W)dW = \frac{4\pi mkT}{h^3} e^{-\frac{4\sqrt{2m}|W|^3}{3\hbar e F}} v\left(\frac{\sqrt{e^3 F}}{|W|}\right) \ln\left(1 + e^{-\frac{W-\zeta}{kT}}\right) dW \quad (2.32)$$

It is difficult to obtain an analytical expression of integral 2.24 with the integrand



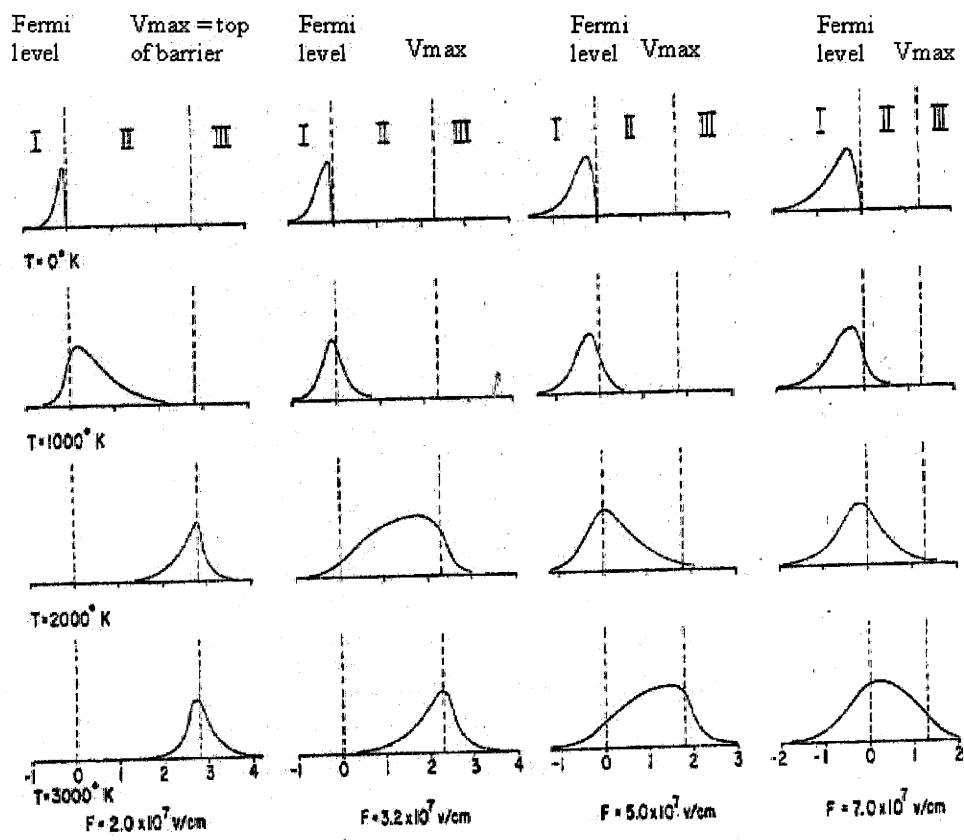


Figure 2-10: Theoretical energy distributions for emitted electrons at the indicated fields and temperatures, for  $\phi = 4.5eV$ , with amplitudes arbitrarily normalized to a common maximum. Energy is in  $eV$  relative to the top of Fermi Level at 0. The left dotted line is the location of the Fermi Level and right dotted line is the location of the maximum of the potential barrier. This figure is quoted from reference [58].

$P(W)$  having the form of equation 2.32. Approximations have been made to obtain results of interest [59, 60]. Dolan and Dyke studied equation 2.32 numerically and calculated  $P(W)$  for various temperatures and field strengths [58]. Figure 2-10 is quoted from their paper [58]. In their simulation, the work function was assumed to be  $\phi = 4.5eV$ , the value for clean tungsten.

From this figure it is observed that at low temperature, the energy distribution of the emitted electron  $P(W)$  narrowly peaks near the Fermi Level over the range of electric fields at which field emission occurs. This means that at low temperature the field emitted electrons have energies approximately around the Fermi Level  $W = \zeta$ . For

a hand-waving argument, this result could be intuitively understood in the following way. At low temperature, there are few electrons above the Fermi Level. Electrons that are capable of participating in field emission almost all come from below the Fermi Level. In this scenario, the transmission coefficient  $D(W, F)$  is a maximum when  $W = \zeta$ . Because, at low temperature, the electron supply function  $N(W)$  is a slow varying function of  $W$  (equation 2.39 and reference [58]) and the transmission coefficient  $D(W, F)$  is a sensitive function of  $W$  (due to the exponential dependence on  $W$ ), the product of these two functions always peaks near the Fermi Level and decreases quite fast below the Fermi Level.

When the temperature is very high, there are an appreciable number of electrons above the Fermi Level. At the same time, the transmission coefficient for these electrons is much larger than that for the electrons near the Fermi Level (again due to the exponential dependence of  $D(W, F)$  on  $W$ .) Then the energy distribution of emitted electrons could no longer peak near the Fermi Level.

In Fowler-Nordheim theory only the low temperature limit is considered. It is permissible then to approximate the exponent in the transmission coefficient by the first two terms in a power series expansion at the Fermi Level  $W = \zeta$ . One finds directly that

$$-\frac{4\sqrt{2m}|W|^3}{3\hbar eF}v\left(\frac{\sqrt{e^3F}}{|W|}\right) \approx -c + \frac{W - \zeta}{d} \quad (2.33)$$

where

$$c = \frac{4\sqrt{2m}\varphi^3}{3\hbar eF}v\left(\frac{\sqrt{e^3F}}{\varphi}\right) \quad (2.34)$$

$$d = \frac{\hbar eF}{2\sqrt{2m}\varphi t\left(\frac{\sqrt{e^3F}}{\varphi}\right)} \quad (2.35)$$

$$t(y) = v(y) - \frac{2}{3}y \frac{dv(y)}{dy} \quad (2.36)$$

and  $\varphi = -\zeta$  is the work function. Numerical values of the function  $t(y)$  are given in Table D.1 – it is seen that it is a slowly varying function, ranging only between 1.00 and 1.11. If numerical values of  $m$ ,  $e$ ,  $h$ , are inserted here and if  $\varphi$  is expressed in e-volts and  $F$  in volts/cm, then  $c$  and  $d$  are given by

$$c = \frac{6.83 \times 10^7 \varphi^{\frac{3}{2}}}{F} v\left(3.79 \times 10^{-4} \frac{F^{\frac{1}{2}}}{\varphi}\right) \quad (2.37)$$

$$d = \frac{9.76 \times 10^{-9} F}{\varphi^{\frac{1}{2}} t\left(3.79 \times 10^{-4} \frac{F^{\frac{1}{2}}}{\varphi}\right)} \quad \text{e-volts.} \quad (2.38)$$

In calculating the numerical values here and below, Dumond and Cohen's [52] recommendations for the values of the atomic constants have been followed.

For low enough temperatures, it is seen that

$$\left. \begin{aligned} kT \ln(1 + e^{-\frac{W-\zeta}{kT}}) &= 0 && \text{when } W > \zeta \\ &= \zeta - W && \text{when } W < \zeta \end{aligned} \right\} \quad (2.39)$$

If equation 2.33 and equation 2.39 are substituted into equation 2.32, the result is

$$\left. \begin{aligned} P(W) &= 0 && \text{when } W > \zeta \\ &= \frac{4\pi m}{h^3} e^{-c + \frac{W-\zeta}{d}} (\zeta - W) && \text{when } W < \zeta \end{aligned} \right\} \quad (2.40)$$

and this is the low temperature limit of the distribution of the emitted electrons. By differentiation, one finds easily that the peak of  $P(W)$  occurs at the energy  $W = \zeta - d$  and has the value

$$P_{max} = \frac{4\pi m d}{h^3} e^{-(c+1)} \quad (2.41)$$

From a numerical discussion of the function one finds that the width of the peak at half this maximum value is  $2.44d$  [53].

The total electric current flowing is found by integrating the distribution given by equation 2.40 over all energies according to equation 2.24. Ordinarily the lowest energy  $-\delta$  is far below the Fermi energy  $\zeta$  so the lower limit of the integral may be taken at  $-\infty$ . The results are as follows:

$$\left. \begin{aligned} j &= e \int_{-\infty}^{\zeta} \frac{4\pi m}{h^3} e^{-c + \frac{W-\zeta}{d}} (\zeta - W) dW \\ &= \frac{4\pi m e d^2}{h^3} e^{-c} \end{aligned} \right\} \quad (2.42)$$

Substituting  $d$  (2.35) and  $c$  (2.34) into the above equation, the current density is finally obtained:

$$j = \frac{e^3 F^2}{8\pi h \phi t^2 \left(\frac{\sqrt{e^3 F}}{\phi}\right)} e^{-\frac{4\sqrt{2m}\phi^{\frac{3}{2}}}{3heF} v\left(\frac{\sqrt{e^3 F}}{\phi}\right)}. \quad (2.43)$$

If  $\phi$  in e-volts and  $F$  in volts/cm are inserted in to equation 2.43 the result is

$$j = \frac{1.54 \times 10^{-6} F^2}{\phi t^2 (3.79 \times 10^{-4} \frac{F^{\frac{1}{2}}}{\phi})} e^{-6.87 \times 10^7 \frac{\phi^{\frac{3}{2}}}{F} v(3.79 \times 10^{-4} \frac{F^{\frac{1}{2}}}{\phi})} \quad \text{amp/cm}^2. \quad (2.44)$$

Equation 2.43 and equation 2.44 are the Fowler-Nordheim field emission formulae. Some numerical values of the logarithm of the current density for various fields and work functions are given in Table D.2. A more extensive set of values has been calculated by Dolan [54] using equation 2.44 but with  $t$  set equal to unity. This simplification is often made because  $t^{-2}$  varies only between 1.00 and 0.81, contributing

between 0 and  $-0.09$  to  $10 \ln(J)$ .

Based on the above observations of the properties of the functions  $t^2(y)$  and  $v(y)$ , Spindt et al. [18] proposed a close approximation of these two functions:

$$t^2(y) = 1.1 \quad (2.45)$$

$$v(y) = 0.95 - y^2 \quad (2.46)$$

where

$$y = 3.79 \times 10^{-4} \frac{F^{\frac{1}{2}}}{\varphi}. \quad (2.47)$$

In actual experiments, the current density  $j$  and electric field near the emitter surface  $F$  are not directly measurable. What is measurable are the applied gate voltage and the extracted current, i.e., the  $I - V$  curve. Because the electric field is not uniform across the whole emitter surface, the total emission current from a tip could be obtained by integrating equation 2.44 over the entire emitter surface. By considering the axial symmetry (which is almost always true for cone shape emitter structures), Dvorson et al. [93] derived that

$$I = \alpha' \pi R_{TIP}^2 j(F_A) \quad (2.48)$$

where  $R_{TIP}$  is the radius of curvature of the tip,  $F_A$  is the electric field at the apex of the emitter tip, and  $j(F_A)$  is the current density at the apex of the emitter tip.  $\alpha'$  is a proportionality factor that has a weak dependence on tip radius and gate voltage but this weak dependence is negligible in most cases [93].

The effective emitting area  $\alpha'\pi R_{TIP}^2$  indicates that there is a proportionality constant between the tip current and the tip apex current density. The proportionality constant (effective emitter area) is

$$\alpha = \alpha'\pi R_{TIP}^2. \quad (2.49)$$

Electrostatics can be used to show that there is also a similar proportionality constant  $\beta$  relating the field to the applied gate voltage, as shown in section 2.8.

So, two linear relationships are obtained:

$$I = \alpha j \quad (2.50)$$

$$F = \beta V \quad (2.51)$$

where  $I$  is the total current observed,  $\alpha$  is the effective emitting area and  $\beta$  is defined as the field factor. field factor  $\beta$  will be discussed in detail in section 2.8.

Substituting equations 2.45, 2.46, 2.50, and 2.51 into equation 2.44, it is finally obtained that

$$I = a_{FN} V^2 e^{-b_{FN}/V} \quad (2.52)$$

where

$$a_{FN} = \frac{\alpha A \beta^2}{1.1 \varphi} e^{\frac{B(1.44 \times 10^{-7})}{\varphi^{1/2}}} \quad (2.53)$$

$$b_{FN} = \frac{0.95B\varphi^{\frac{3}{2}}}{\beta} \quad (2.54)$$

$$A = 1.54 \times 10^{-6} \quad (2.55)$$

$$B = 6.87 \times 10^7. \quad (2.56)$$

It is observed that  $a_{FN}$  and  $b_{FN}$  are constants and are only dependent on the emitter's work function  $\varphi$  and geometric dimensions and are not dependent on the external field  $F$ .

Typically, in analyzing experimental data, a diagram of  $\ln(I/V^2)$  vs  $1/V$  is plotted. This corresponds to the following form of the Fowler-Nordheim formula:

$$\ln(I/V^2) = \ln(a_{FN}) - b_{FN} \frac{1}{V} \quad (2.57)$$

The diagram should produce a straight line. From the interception of the plot with the  $y$  axis and the slope of the straight line, important information of about the device reflected in parameters  $a_{FN}$  and  $b_{FN}$  could be calculated. Figure 2-11 shows a typical Fowler-Nordheim plot.

For a good description on Fowler-Nordheim theory readers could refer to reference [40].

## 2.7 Electron emission from a semiconductor

The theory of electron field emission from a semiconductor is almost parallel to the theory of electron field emission from a metal (Fowler-Nordheim theory). For semiconductors, the electron supply comes from two bands: the conduction band and the valence band, which are separated by a bandgap  $E_g$ . For conduction band electrons, the surface barrier height is the electron affinity  $\chi$ , while for the valence band the

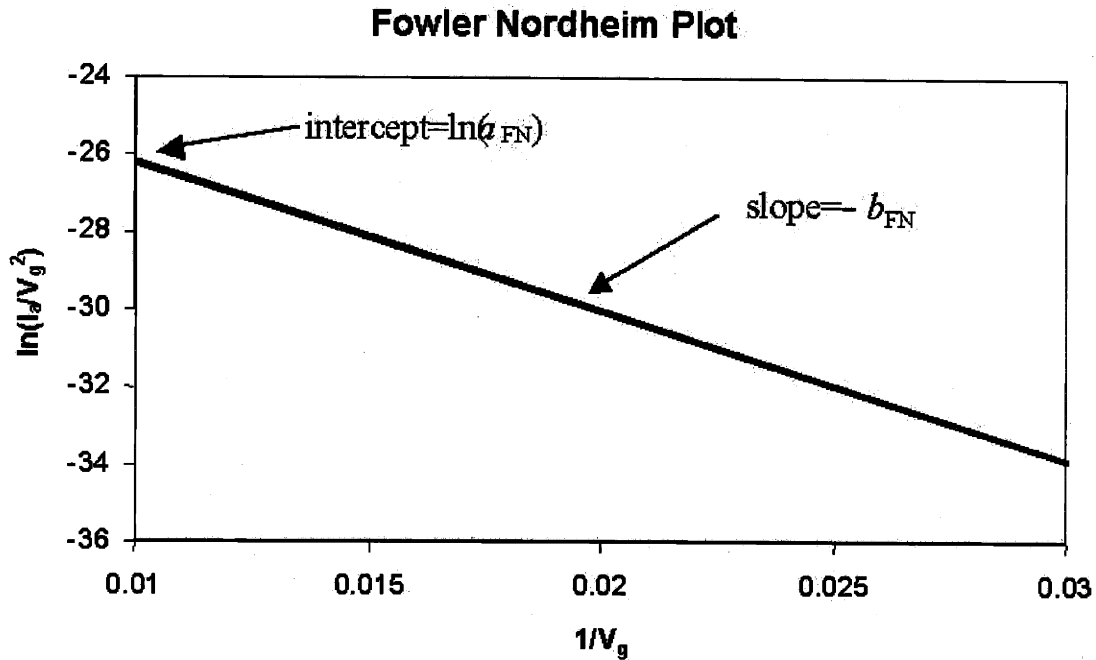


Figure 2-11: A typical Fowler-Nordheim plot. From the intercept of the plot with the  $y$  axis and the slope of the straight line, important information of about the device reflected in parameters  $a_{FN}$  and  $b_{FN}$  could be calculated.

surface barrier height is  $\chi + E_g$ . But the theory does not simply replace  $\varphi$  in equation 2.43 and equation 2.44 with these two parameters. Special effects such as field penetration inside the semiconductor surface have to be taken into consideration. In the following sections, field emission from semiconductors will be discussed in more detail.

### 2.7.1 Field emission from a semiconductor valence band

Although there has been scarce reports on the observation of electron field emission from the valence band of a semiconductor, the theory of valence band electron emission is much simpler and very much in parallel with the metal field emission theory.

The valence band of a semiconductor is a full band. An intrinsic semiconductor usually is an insulator at low temperature because there are almost no electrons in



the conduction band. The electrons in the valence band are not conductive because there is no empty states in the band. However, the non-conducting property of the valence band electrons does not prevent electron field emission from the valence band. When the external electric field is high enough, the electrons from the top of the valence band can tunnel through the barrier and come into the vacuum. Since each emitted electron leaves a positive hole (an empty state), there will be enough conduction to balance the emission current.

The derivation of the current density emitted from the valence band could go parallel to the derivation of the current density in the metal case. However, in the semiconductor valence band case, the energy distribution of the emitted electrons  $P(W)$  no longer peaks near the Fermi Level (or the chemical potential) which usually lies within the energy band gap. The reason is that there are no electrons at the Fermi Level, i.e., the electron supply function  $N(W)$  at the Fermi Level is zero. The highest energy level that electrons can occupy in the valence band is the top of the valence band  $\chi + E_g$ . For valence band electrons, the transmission coefficient  $D(W, F)$  is a maximum when  $W = \chi + E_g$  and decreases exponentially when  $W$  goes below the top of the valence band. Correspondingly, equation 2.32  $P(W)$  needs to be expanded at  $W = \chi + E_g$ . So, for the valence band field emission, it is like a metal electron field emission with an effective work function of  $E_g + \chi$ . For a detailed derivation, please refer to reference [61, 62].

Another difference between the semiconductor valence band electron emission and the metal field emission is the value of the image potential. Because of the dielectric properties of semiconductors the image potential has the form [63]:

$$V_{image}(x) = -\frac{\epsilon_s - 1}{\epsilon_s + 1} \frac{e^2}{4x} \quad (2.58)$$

where  $\epsilon_s$  is the dielectric constant of the semiconductor. This new form of the image potential will result in a new parameter  $y$  in equation 2.31:

$$y = \left( \frac{\epsilon_s - 1}{\epsilon_s + 1} \right)^{\frac{1}{2}} \frac{\sqrt{e^3 F}}{|W|}. \quad (2.59)$$

For the case of silicon,  $\epsilon_s = 11.9$  (Appendix B), it is calculated that  $\frac{\epsilon_s - 1}{\epsilon_s + 1} \approx 0.845$  and  $\left( \frac{\epsilon_s - 1}{\epsilon_s + 1} \right)^{\frac{1}{2}} \approx 0.92$ .

It is worth noting here that the external electrical field does penetrate the semiconductor surface, as will be described in the following section. The valence band will be bent near the surface. However, in contrast to the conduction band, an electron accumulation layer will not be formed, because in the fully occupied valence band there are no empty electronic states available to hold more electrons, while in the almost vacant conduction band there is plenty of available states.

## 2.7.2 Field penetration

If the external electric field does not penetrate into the inside of a semiconductor, the physical picture of field emission from a semiconductor will look like figure 2-12. Conduction band and valence band electrons will participate in field emission in almost the same way, except that they have different barrier heights  $\chi$  and  $\chi + E_g$ .

However, semiconductors are not metals, and the electric field will penetrate into the semiconductor surface and reach the inside of the solid. The field will bend both the conduction band and the valence band downward, as shown in figure 2-13. The field essentially has no effect on the valence band, although the field also bends it, because at the semiconductor surface the distance between the top of the valence band and the vacuum level (the barrier height) still remains unchanged at  $\chi + E_g$ . However, for the conduction band the situation is different. The Fermi level  $\mu$  is usually close to the conduction band (n-type semiconductor) and it must remain constant throughout the semiconductor. So the bottom of the conduction band will generally dip below  $\mu$ , the Fermi level. When this happens, a "pool" of electrons will collect in this depression.

No field penetration

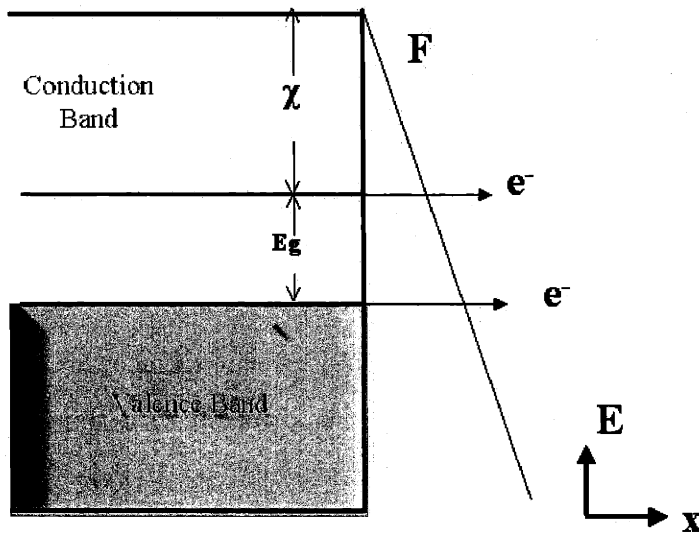


Figure 2-12: Physical picture of field emission from a semiconductor without field penetration. Conduction band and valence band electrons will participate in the field emission in almost the same way, except that they have different barrier heights  $\chi$  and  $\chi + E_g$ , respectively.

With field penetration

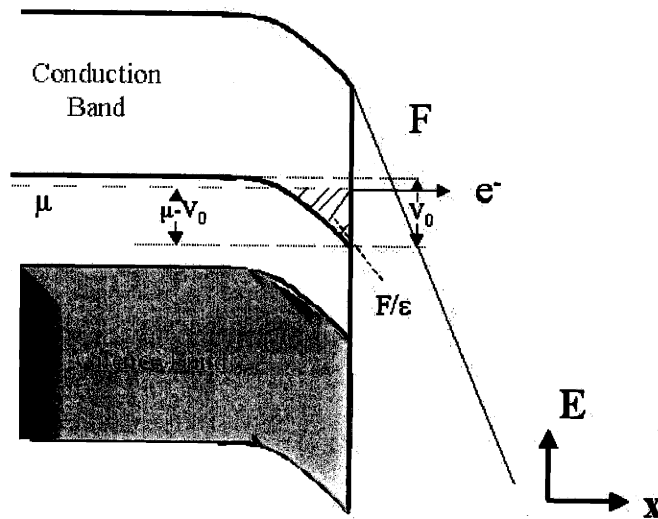


Figure 2-13: Field penetration causes the conduction band to bend underneath the Fermi Level, creating a pool of electron near the surface. This carrier pool causes the effective barrier height to decrease.

If the field is high enough, this “pool” of electrons could become degenerate. It is apparent that the highest filled level of this “pool” must coincide with the Fermi level. In this situation the effective work function of the conduction band electron is decreased to

$$\varphi_{effective} = \chi - (\mu - V_0) \quad (2.60)$$

where  $V_0$  denotes the amount of conduction band bending.

### 2.7.3 The surface electron accumulation layer

We call the “pool” of electrons accumulated in the surface described in the above section an electron accumulation layer. It is necessary to evaluate the value of  $\mu - V_0$ ,

since it determines the proper work function we need to use in the Fowler-Nordheim equation for field emission of conduction band electrons. In figure 2-13  $V_0 = V(0)$ . Gomer [46] gave a simple and insightful derivation of this value by assuming a local free electron gas model and  $\mu - V_0$  is calculated to be (refer to appendix E for a detailed derivation):

$$\mu - V_0 = \nu F^{\frac{4}{5}} \quad (2.61)$$

where

$$\nu = 4.5 \times 10^{-7} \epsilon_s^{-\frac{2}{5}} \quad (2.62)$$

$\epsilon_s$  is the dielectric constant of the semiconductor,  $F$  is in  $V/cm$ , and the energies are in  $eV$ . So the quantity  $\nu F^{\frac{4}{5}}$  needs to be subtracted from  $\chi$  to get the new barrier height in a semiconductor in using the Fowler-Nordheim equation.

#### 2.7.4 Field emission from the semiconductor conduction band

R. Stratton did seminal work in formulating the theory of field emission from a semiconductor [61, 62]. From the above discussion it is seen that there is an accumulation layer of electrons formed at the surface of the semiconductor. This layer of electrons makes the semiconductor behave like a metal. For a metal surface, the image potential should take the form of equation 2.15 instead of the form of equation 2.58. However, in this case, the semiconductor is not a real metal. It still takes a longer time for a semiconductor than metal to adjust itself to compensate for the influence of an external test charge. Stratton stated in reference [61] that

A semiconductor would be expected to behave as a dielectric if the dielec-

tric relaxation time  $\epsilon_s/4\pi\sigma$  is sufficiently large. (Here  $\sigma$  is the conductivity near the surface where charges are displaced.) This case will be assumed in the rest of the paper since in any case the factor  $\frac{\epsilon_s-1}{\epsilon_s+1}$  is not very different from unity for the  $\epsilon_s$  values of typical semiconductors.

Since the effect of the dielectric constant  $\epsilon_s$  on the final formulation of the emission current is minimal, the image potential of the form of equation 2.15 could be used throughout the derivation.

In summary, the only difference in deriving the Fowler-Nordheim formula for a semiconductor conduction band from deriving the Fowler-Nordheim formula for a metal are

1. the image potential is changed from  $-\frac{e^2}{4x}$  to  $-\frac{\epsilon_s-1}{\epsilon_s+1}\frac{e^2}{4x}$
2. the effective work function is changed from  $\chi$  to  $\chi - \nu F^{\frac{4}{5}}$ .

Based on the above assumptions, by substituting the proper values into equation 2.43, the current density from a semiconductor's conduction band is obtained to be

$$j = \frac{e^3}{8\pi h} \frac{F^2}{(\chi - \nu F^{\frac{4}{5}})t^2(y)} e^{-\frac{4\sqrt{2m}}{3\hbar e} \frac{(\chi - \nu F^{\frac{4}{5}})^{\frac{3}{2}}}{F}} v(y) \quad (2.63)$$

where

$$y = \left(\frac{\epsilon_s - 1}{\epsilon_s + 1}\right)^{\frac{1}{2}} \frac{\sqrt{e^3 F}}{\chi - \nu F^{\frac{4}{5}}} \quad (2.64)$$

by considering the modified image potential (refer to equations 2.58 and 2.59).

For a detailed and comprehensive theory of field emission from semiconductors, please refer to references [61, 62].

### 2.7.5 Theoretically predicted regimes of operation of semiconductor field emission

From the theory discussed above, we can clearly see that theoretically there are two sources of electron supply for field emission from a semiconductor. This is the distinctive difference between field emission from a metal and field emission from a semiconductor. In a semiconductor, we are expected to observe two regions of field emission that should obey Fowler-Nordheim formula: conduction band emission and valence band emission. In between, since the electron supply for the conduction band is limited by the finite dopant concentration, we may expect to see current saturation. Figure 2-14 shows a schematic of this physical picture. For valence band emission, the slope in a  $\ln(I/V^2)$  vs.  $1/V$  plot is proportional to  $(E_g + \chi)^{3/2}$ , while for conduction band emission the slope is proportional to  $\chi^{3/2}$ , where  $E_g$  is the energy band gap and  $\chi$  is the electron affinity of the semiconductor. The ratio of these two slopes has a theoretical value of  $(\frac{E_g + \chi}{\chi})^{3/2}$ . In the case of silicon, where  $E_g = 1.12eV$  and  $\chi = 4.05eV$ , the ratio has a value of 1.44. In this discussion, we ignored the effects of surface states and emission from surface states. In section 3.2.2 we will see that at the onset of the turn-on of the field emission, the effect of surface states is minimal.

In chapter 5 we will discuss the experimental observation and theoretical analysis of current saturation and valence band field emission from silicon.

## 2.8 Field enhancement of a field emitter

The Fowler-Nordheim formula describes the fundamental process and equation that field emission follows. In order to achieve field emission, either from a metal or from a semiconductor, it requires a huge electric field, typically  $\sim 2 - 6 \times 10^7 V/cm$ . For a planar surface, even at sub-micron spacing, a large voltage would be required to achieve these fields to turn on the field emission. Take a parallel plate as an example.

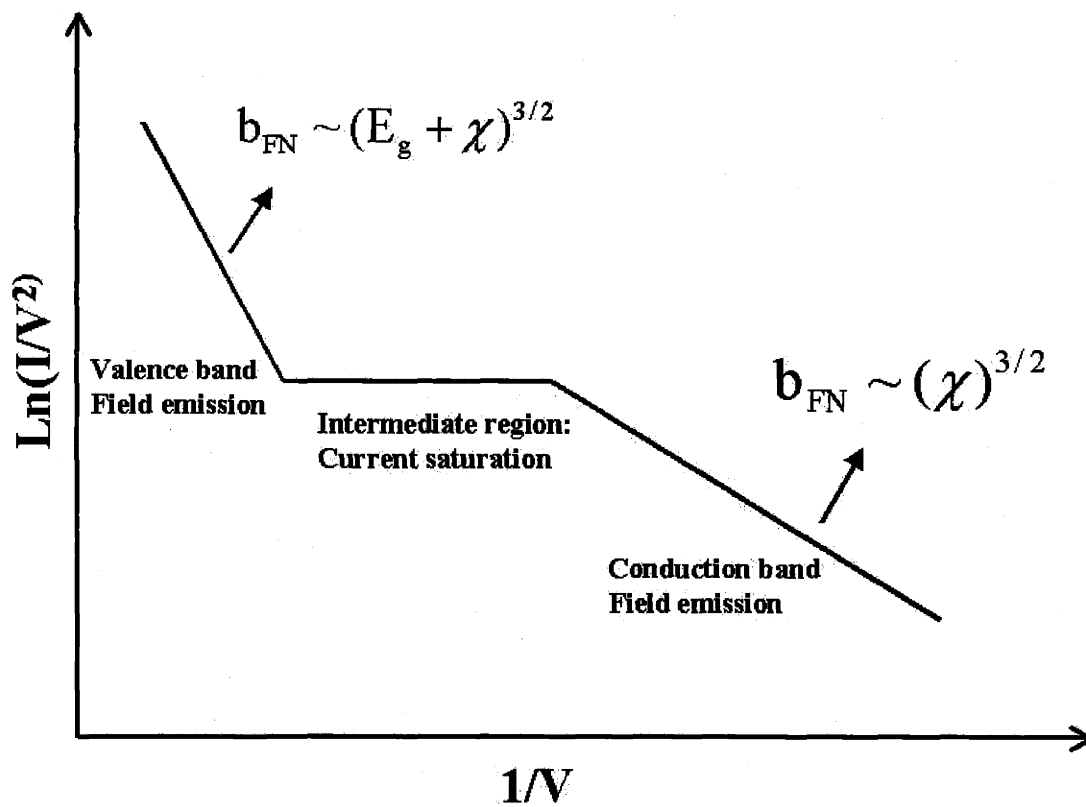


Figure 2-14: Schematic of the two band emission picture. The ratio of the two slopes of the Fowler-Nordheim plot has a theoretical value of  $(\frac{E_g + \chi}{\chi})^{3/2}$ . In case of the silicon, the value is 1.44.



For a spacing of  $50nm$ ,  $250V$  would be required to achieve a surface electric field of  $5 \times 10^7 V/cm$ . This example shows that in order to achieve a high electric field at low voltage, we need to use special physical structures, such as sharp tips to enhance the surface electric field. In the following section 2.8.1, we will present the “ball in a sphere” model to calculate the field enhancement of a typical conical emitter structure.

### 2.8.1 “Ball in a sphere” model

A good model for describing geometry effects in a field emitter cone structure is the “ball in a sphere” model. Figure 2-15 is a schematic of this model. The apex of the emitter cone is not strictly speaking a spherical ball. However it is a good model for describing the effect of tip geometry because mathematically the field at the tip is related to the “curvature” of the tip. The curvature of the tip apex is best represented by the “smallest” radius circle that could be drawn. This circle coincides with the tip circumference. In practice, a circle with the best fit to the tip circumference is drawn. The radius of this fitting circle is the radius of curvature of the tip. In figure 2-15 the interior ball is analogous to the cone tip and the outer sphere is the gate.  $r$  is the radius of curvature of the emitter tip and  $2d$  is the diameter of the gate aperture. In the text below, we sometimes use tip radius to denote the tip radius of curvature for the sake of simplicity.

Typically, the emitter is grounded, i.e., bias at  $0V$  and a voltage  $V_g$  is applied to the gate. A solution to Laplace’s equation in spherical coordinates [63] gives the electric field at the ball’s surface to be

$$\begin{aligned} F &= -V_g \left( \frac{1}{r} + \frac{1}{d-r} \right) \\ &= -\beta V_g \end{aligned} \tag{2.65}$$

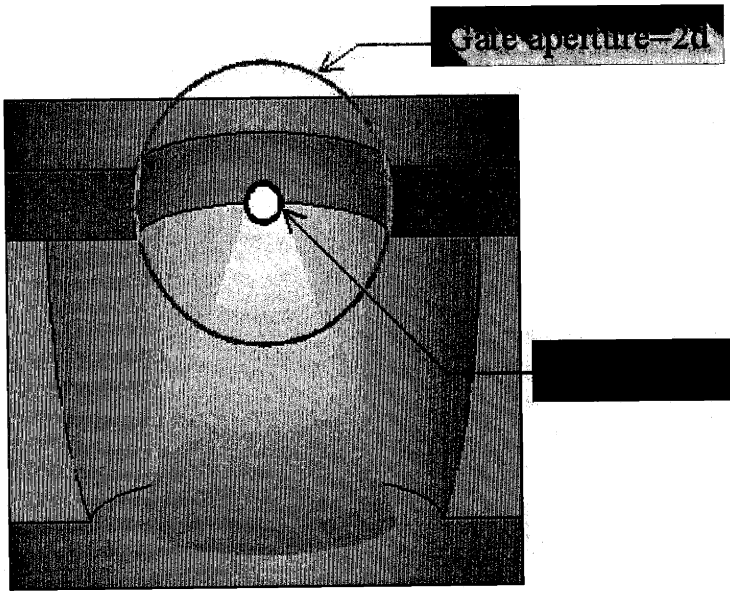


Figure 2-15: Schematic of the “ball in a sphere” model. The interior ball is analogous to the cone tip and the outer sphere is the gate.  $r$  is the radius of curvature of the emitter tip and  $2d$  is the diameter of the gate aperture. In experiments, the emitter is grounded, i.e., bias at  $0V$  and the gate is applied a voltage  $V_g$ .

as shown in figure 2-16. The minus sign equation 2.65 indicates that the direction of the electric field is originating from the gate and ending at the emitter surface.  $\beta$  is the aforementioned field factor defined by

$$\beta = |F/V_g| = \left(\frac{1}{r} + \frac{1}{d-r}\right). \quad (2.66)$$

It is obvious that the field factor is only a function of the emitter’s geometry. In the case of  $d \gg r$ , which is typical in our fabrication, the electric field is independent of gate aperture and is inversely proportional to the radius of curvature of the emitter tip. For example, in the case of  $r = 2nm$ , a gate voltage as low as  $10V$  would be sufficient to achieve the previously mentioned electric field of  $5 \times 10^7 V/cm$ .

For reference, in appendix F another emitter structure, the “coaxial cylinder”, is considered for the field enhancement.

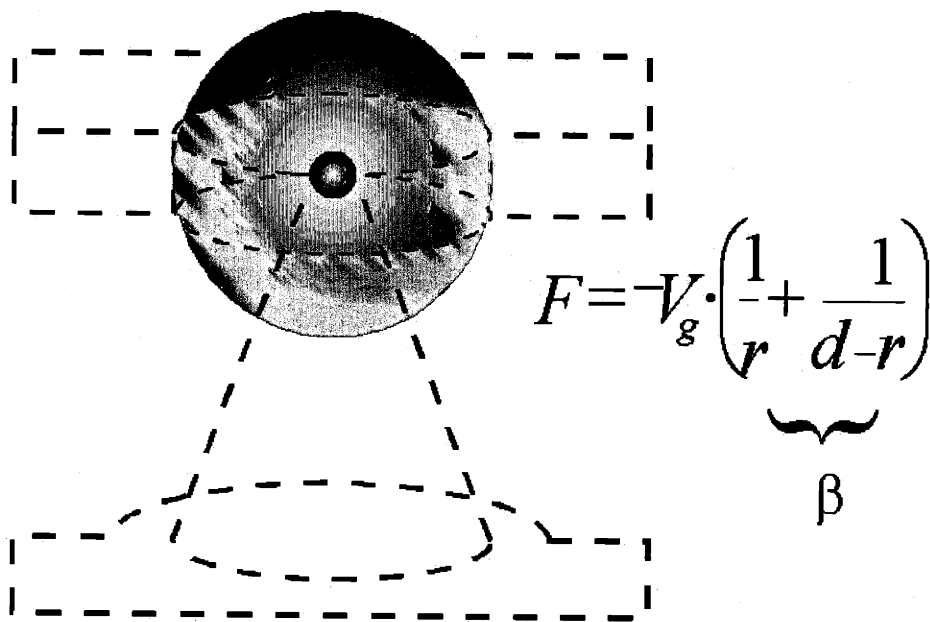


Figure 2-16: "Ball in a sphere" model. A solution to Laplace's equation in spherical coordinates gives the electric field at the ball's surface to be  $F = -\beta V_g = -V_g \left( \frac{1}{r} + \frac{1}{d-r} \right)$  and  $\beta = |F/V_g| = \left( \frac{1}{r} + \frac{1}{d-r} \right)$  is the field factor.

## Chapter 3

### Silicon field emission array

In the last chapter we briefly reviewed the field emission theory for metals and for semiconductors. In this chapter we will present the fabrication and the characterization of the silicon emitter arrays.

There are two most widely used approaches of fabricating cone field emitter arrays:

- the Spindt approach and
- the chemical mechanical polishing (CMP-FED) approach.

In the mid 1960's, Capp Spindt at S. R. I. described a process for producing self-aligned gated emitter arrays, commonly referred to as the "Spindt emitter array" [18]. The Spindt technique employs the use of high resolution lithography and plasma etching to create micron or sub-micron sized holes in a metal/dielectric sandwich. A directional molybdenum evaporation process then deposits a film to a thickness greater than the hole diameter. Under ideal conditions the hole closes during the deposition process and the tips are formed in the cavities. A subsequent lift-off process removes the unwanted material above the tip and leaves a formation of molybdenum cones which are self-aligned to the holes in the original metal/dielectric sandwich.

Figure 3-1 illustrated the schematic of the above process flow.

The Spindt approach has long been the standard procedure of producing gated field emitter arrays. However, the process is difficult to scale to larger display sizes and pixel densities [88]. The molybdenum evaporation process requires a highly directional source; therefore collimation is often used. Scaling of a collimated molybdenum evaporation process over large areas in a manufacturing environment will be an expensive and formidable engineering challenge.

The CMP-FED approach was developed at Micron Display Technology to address the issue of scalability and application to high-volume manufacturing not addressed by the Spindt approach [78]. The CMP-FED uses a combination of deposition, chemical mechanical polishing and wet chemical etching to produce self-aligned extraction grids (gates) around each tip. In the CMP-FED process, the formation of the emitter tip and the formation of gate are separate steps, which allows for greater control of critical tip parameters. This is in contrast to the Spindt approach where the cone tip is determined by the metal deposition process.

We pursue our research by fabricating cone shape silicon field emitter arrays with a polycrystalline silicon gate using the chemical mechanical polishing approach described by Micron Display Technology [78]. The goal of this thesis work is to experimentally study the field emission phenomenon from a semiconductor. We choose silicon because it is one of the most widely used semiconductors at present, and there is a mature technological base in fabricating silicon-based microelectronic devices. We hope to fabricate silicon field emitter arrays with low operation voltage, high current density, high transconductance and high current uniformity. These are the major factors determining the performance of field emitter arrays. Furthermore we hope to be able to understand more deeply the physics of field emission from silicon and hope to observe field emission from the valence band of silicon as described in the last chapter.

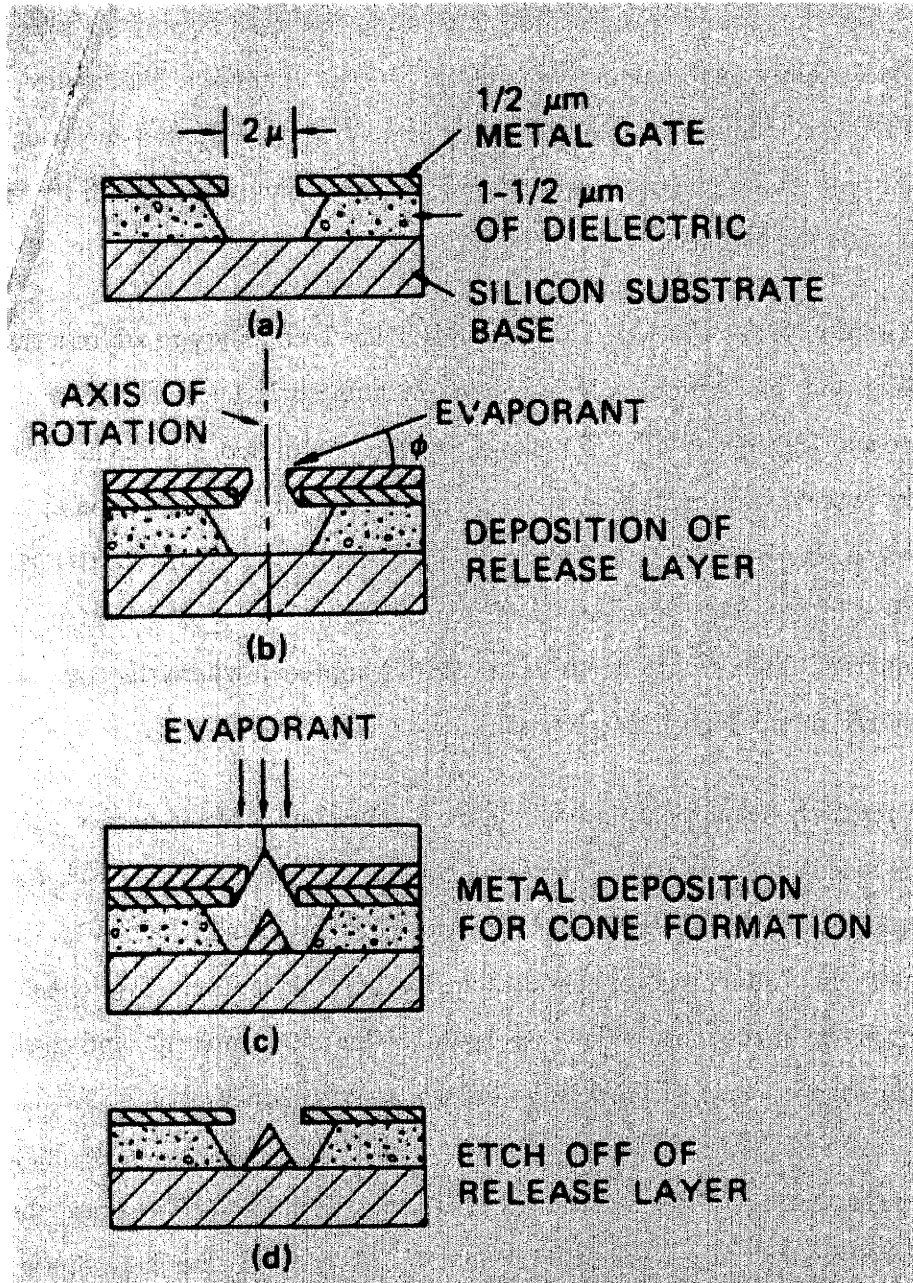


Figure 3-1: Schematic of the fabrication process of the Spindt type emitter arrays. This figure is quoted from reference [18].

In this chapter the fabrication and characterization of silicon field emitter arrays are presented. In chapter 4 the fabrication and characterization of high aspect ratio field emitter arrays will be presented. In chapter 5 the observation of current saturation and field emission from the silicon valence band will be presented and discussed.

## 3.1 Fabrication process

We fabricated field emission arrays with  $\sim 1\mu m$  gate aperture on 4-inch (100) n-type silicon substrates with dopant concentration of about  $10^{16}cm^{-3}$ . The process consists of three main steps: cone/tip formation, gate aperture formation, tip exposure.

The fabrication process is described below.

### 3.1.1 Cone/tip formation

#### Thermal oxidation

First, a layer of 250 nm  $SiO_2$  was thermally grown on the substrate by wet oxidation at  $1000^\circ C$  [74, 75]. After the formation of the oxide layer, a layer of photoresist [67] was spin-coated. The wafer was patterned in an optical stepper [68]. The photoresist was then developed and arrays of circular photoresist dots were defined on the surface of the silicon wafers. Using these arrays of photoresist dots as etching masks, the silicon dioxide layer was then anisotropically (directionally) etched in a  $CF_4$  &  $CHF_3$  plasma [69, 74]. The circular dots array pattern of the photoresist was thus transferred to the silicon dioxide. Figure 3-2 is a schematic description of this pattern transfer process.

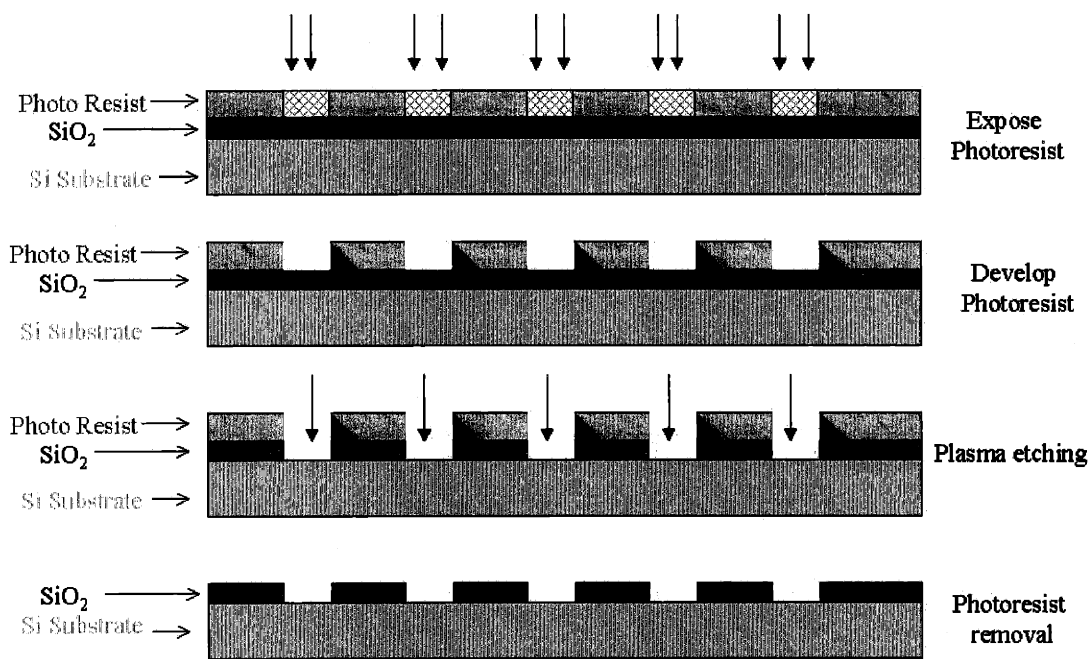


Figure 3-2: The process of definition of  $SiO_2$  disks. The wafer was spin-coated with  $1\mu m$  of photoresist. The photoresist was patterned by a clear field mask in a stepper. The exposed photoresist was then developed away, opening the window for the etching of  $SiO_2$  in  $CF_4$  &  $CHF_3$  plasma. After the  $SiO_2$  was etched, the photoresist is removed in an  $O_2$  plasma. The pattern which was initially defined by the mask was transferred to the  $SiO_2$  layer. The final outcome of this step were arrays of circular  $SiO_2$  disks.



### Isotropic etching of silicon

The oxide layer was patterned to obtain an array of  $1\ \mu\text{m}$  diameter  $\text{SiO}_2$  disks. Using these  $\text{SiO}_2$  disks as hard masks the underlying silicon was isotropically etched in an  $\text{SF}_6$  &  $\text{He}$  plasma to form tips [71]. Figure 3-3 shows a single emitter after isotropic etching of the underlying silicon.

### Oxidation sharpening of the silicon cones

The silicon tips were oxidized in dry oxygen at  $950^\circ\text{C}$  for 15 hours [76, 77]. The time duration of the sharpening process was obtained by device simulation using SUPREM-IV [70]. Figure 3-4 shows the result of the simulation. The neck was consumed by oxidation, resulting in a sharp tip. If the sharpening process exceeds the time period necessary to consume the neck, the tip remains sharp; however, the aspect ratio of the cone decreases. The  $\text{SiO}_2$  disks were then removed in hydrofluoric acid solution [72]. Figure 3-5 shows the SEM picture of an array of sharpened tips after the oxide is stripped. Figure 3-6 is an atomic force microscope (AFM) picture of an array of sharpened tips. Figure 3-7 shows a single silicon tip. The radius of curvature of the apex is measured to be about  $9.2\text{nm}$  by drawing a circle to best fit the shape of the apex.

The tip radius of curvature is very uniform across a large area of the wafer. This is due to the uniformity of the neck formed during plasma etching and the self-limiting nature of the oxidation-sharpening step.

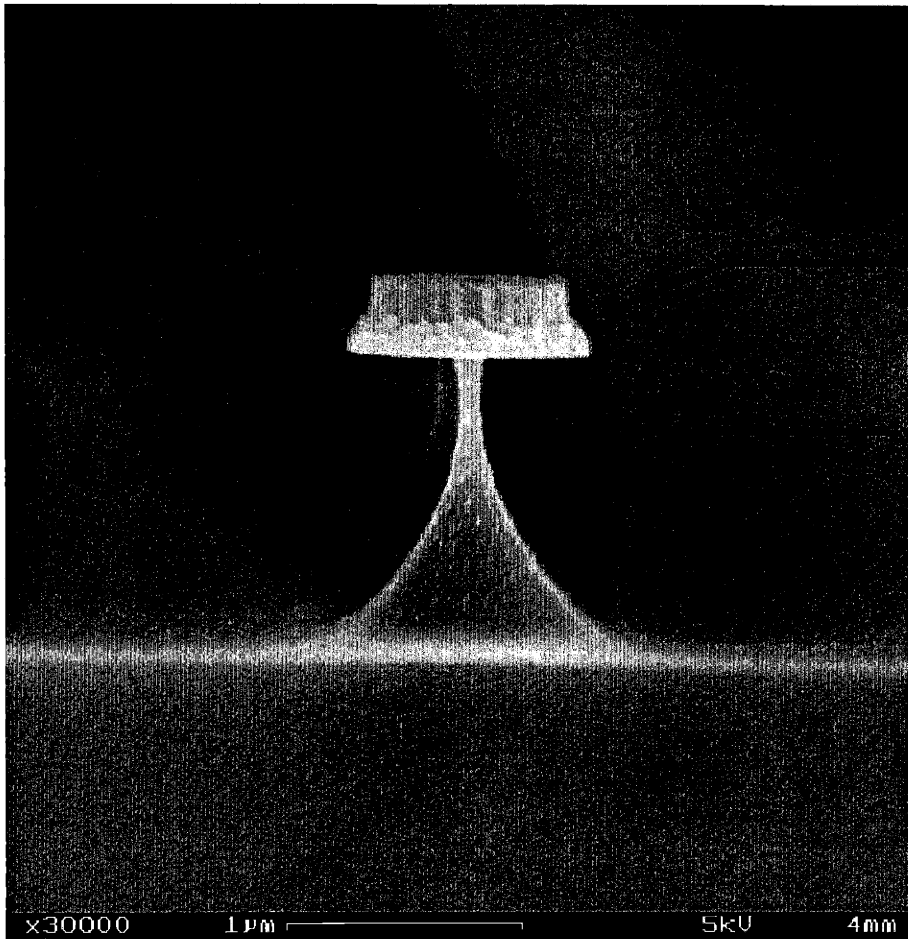


Figure 3-3: The structure after isotropic silicon etching in an  $SF_6$  &  $He$  plasma environment. Notice the residual silicon necks not consumed by the etching. We can easily distinguish the  $SiO_2$  cap and the underlying  $Si$  cones. The oxide cap has a diameter of about  $1\mu m$ .

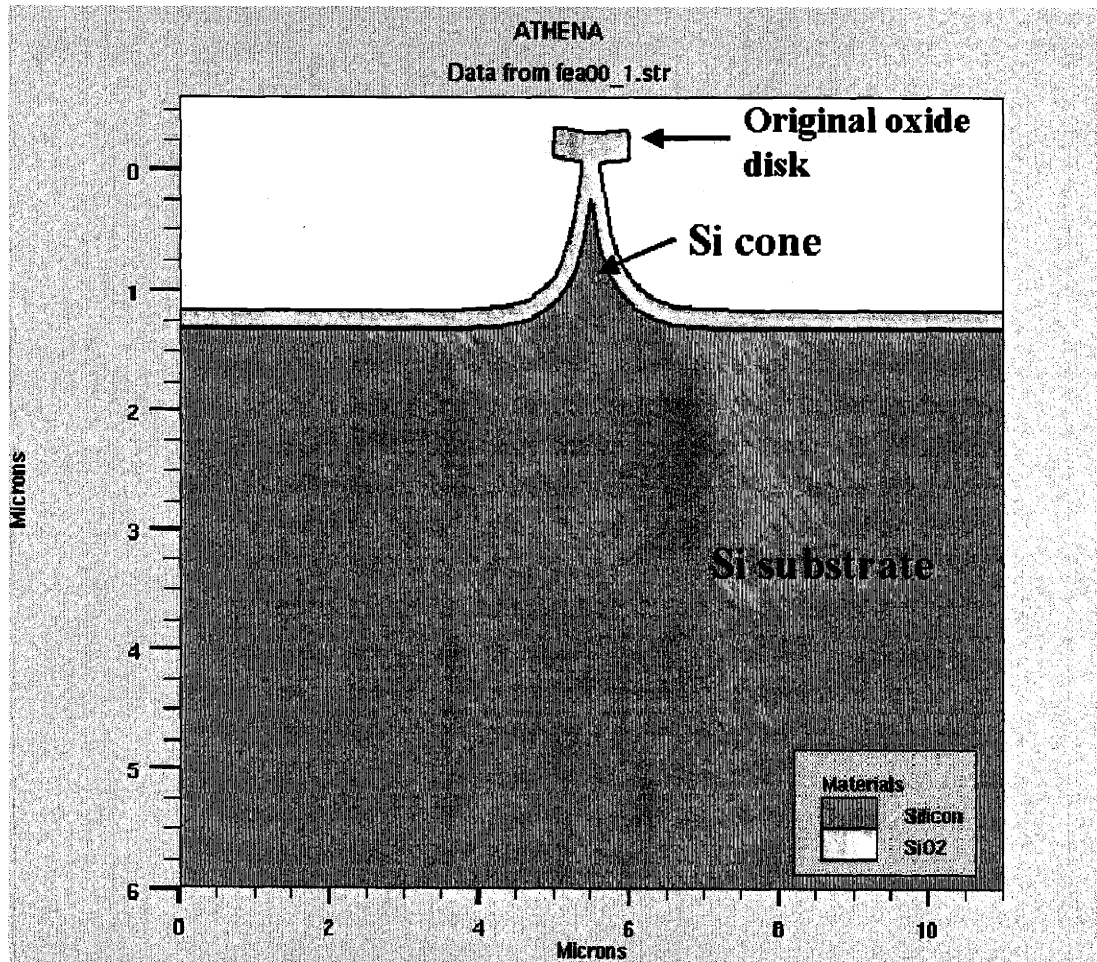


Figure 3-4: Simulation result of oxidation sharpening of silicon tips. The previous neck was consumed and the tip becomes sharp. The oxide cap is about  $1\mu m$  wide. The simulation is done using SUPREM IV.

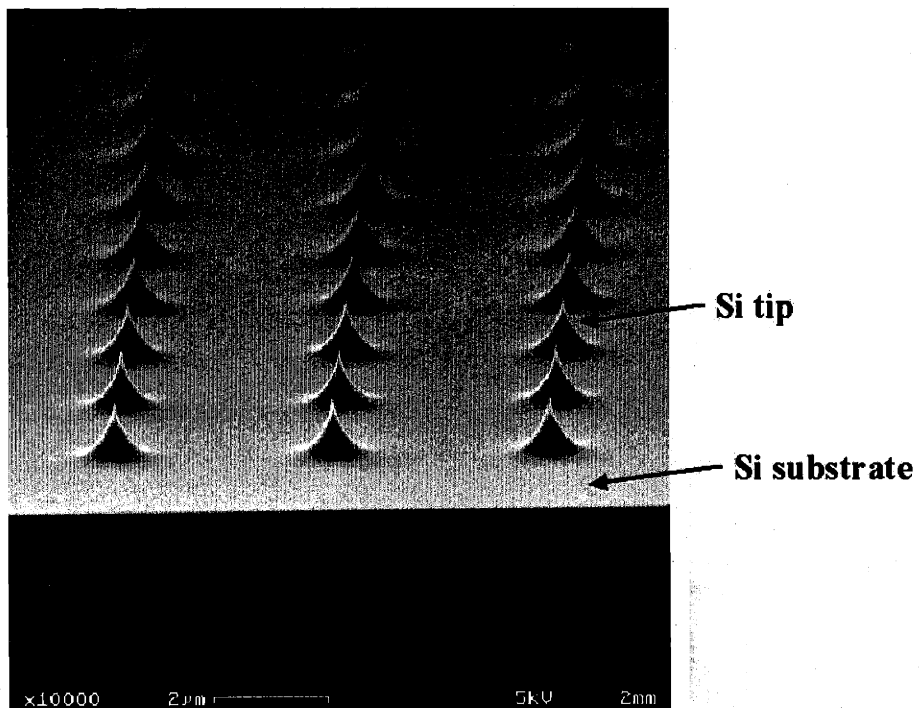


Figure 3-5: The silicon tip array after the oxide is stripped. This is a  $4\mu\text{m}$  pitch array. The distance between neighboring tips is  $4\mu\text{m}$ . The  $x$  and  $y$  direction spacings are the same.

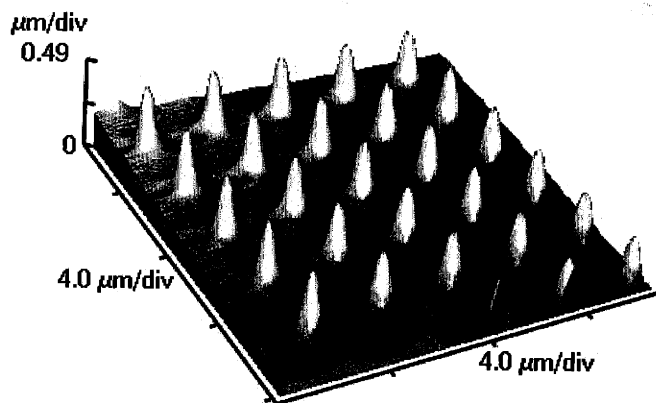


Figure 3-6: AFM picture of a silicon tip array after the oxide is stripped. This is a  $3\mu\text{m}$  pitch array. The distance between neighboring tips is  $3\mu\text{m}$ .

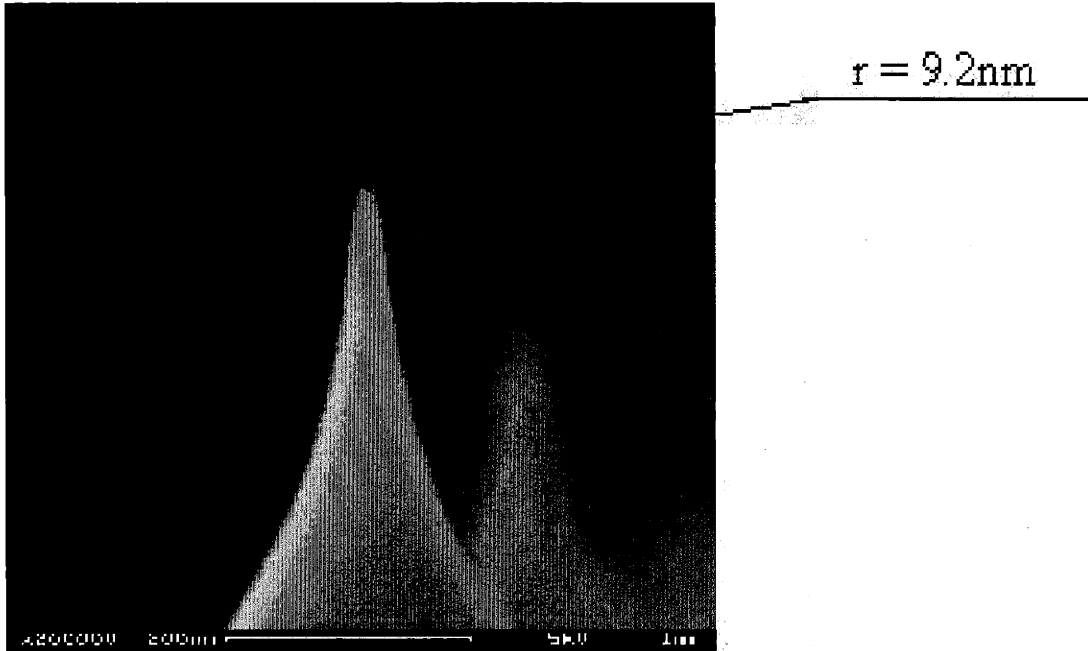


Figure 3-7: A close look at the apex area of a single silicon tip. The radius of curvature of the apex is measured to be about  $9.2nm$

### 3.1.2 Gate aperture formation

#### LPCVD of the gate insulator and the gate

A conformal, approximately  $0.7\mu m - 0.8\mu m$  thick, low-pressure chemical vapor deposited (LPCVD) [74] layer of  $SiO_2$  was next added. The oxide was densified at  $950^\circ C$  in  $O_2$  for 20 minutes and  $N_2$  for 20 minutes. Previous tests on densified oxide show that the breakdown voltage is similar to thermal oxides after  $O_2$  densification at high temperature. The gate electrode was next deposited. It is a conformal layer of approximate  $0.3\mu m$  LPCVD polycrystalline silicon. The polycrystalline silicon layer was subsequently doped with phosphorus to increase its conductivity. The dopant was diffused at  $925^\circ C$  in  $POCl_3$  for 100 minutes. The measured sheet resistance of the doped polycrystalline layer is about  $88\Omega/\square$ . Figure 3-8 shows the simulation of these two steps of low-pressure chemical vapor deposition. After these two steps, a blunt bump is formed above every single emitter.

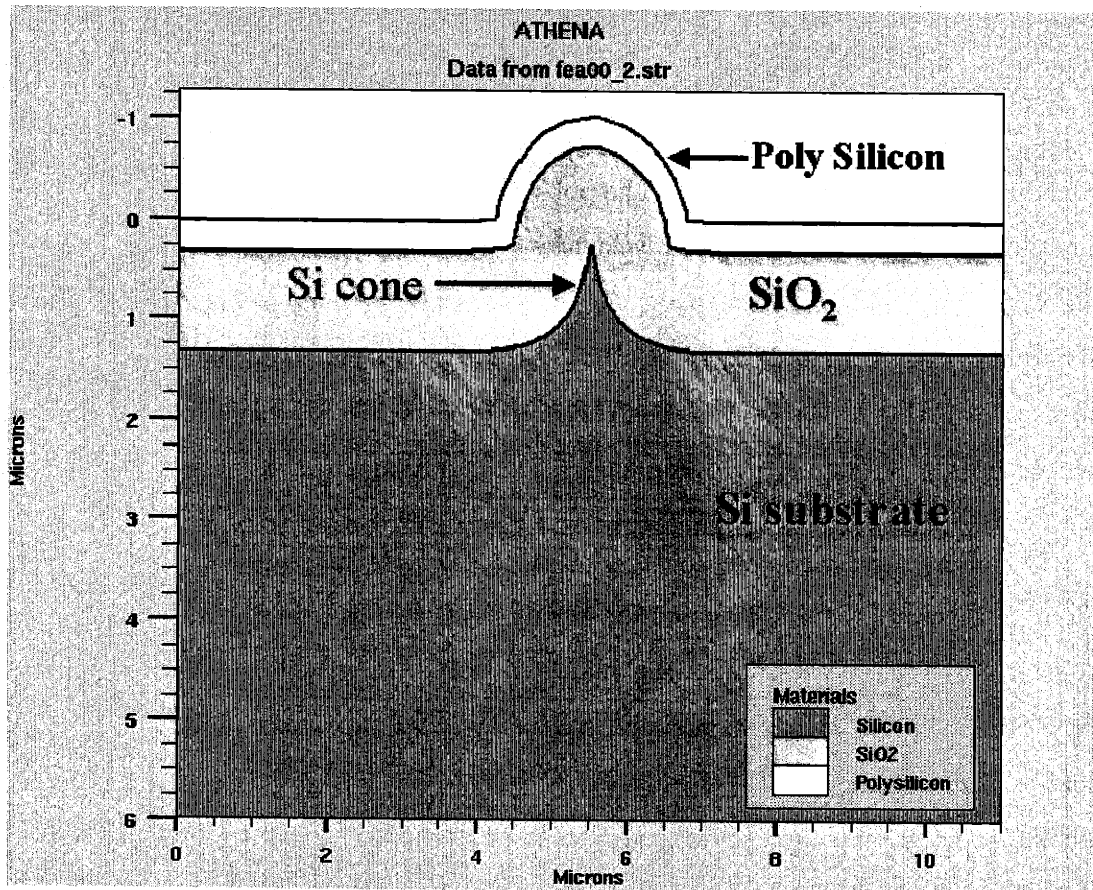


Figure 3-8: Simulation result after two steps of low-pressure chemical vapor deposition (LPCVD): the first is a LPCVD layer of  $SiO_2$ , the second is a LPCVD layer of polycrystalline silicon. The thickness of the  $SiO_2$  layer is about  $700nm$  and the thickness of the polycrystalline silicon layer is about  $300nm$ . After the polycrystalline silicon is doped with phosphorus it becomes conducting gate material.

## Chemical mechanical polishing

A timed chemical mechanical polishing (CMP) [78, 81, 82, 83] step process was used to remove the bumps thus revealing the gate aperture.

Figure 3-9 shows a schematic of the CMP and its operation principle. A wafer is placed underneath a polishing head, held against gravity by applying vacuum to the polishing head. The polishing head brings the wafer, whose front side is facing down, in contact with the polishing pad. The polishing head and the pad rotate in the same direction but at different angular velocities, thus creating relative motion between the wafer front side and the pad. A slurry containing microscopic particles with diameters ranging from  $130nm$  to  $160nm$  flows between the pad and the polishing head. The slurry permeates between the wafer front side and the surface of the pad, hence accomplishing the polishing task. This polishing process is very similar to sandpaper polishing, but in a much more delicate and controlled way.

Figure 3-10 shows the simulation of the device structure after the chemical mechanical polishing process. The bumps are removed and the underlying silicon dioxide is exposed. This window of exposed silicon dioxide defines the gate aperture of the final field emitter structure. This chemical mechanical polishing is actually a self-aligned etching process, which does not need a mask nor photolithography step to etch away the materials.

The chemical mechanical polishing exploits the fact that the polishing rate of the bumps is faster than that of the flat surfaces due to increased mechanical pressure. As seen in figure 3-8, the emitter array structure prior to polishing has two distinct surfaces. There is a flat "shoulder" which accounts for a majority of the surface area to be polished and the topography created by the emitter tips which accounts for a minority of the surface area. The removal rate of this topography is higher than for the flat "shoulder". The process is expected to be self-limiting: once polishing has locally reached the shoulder the removal rate nearly stops in comparison to any to-



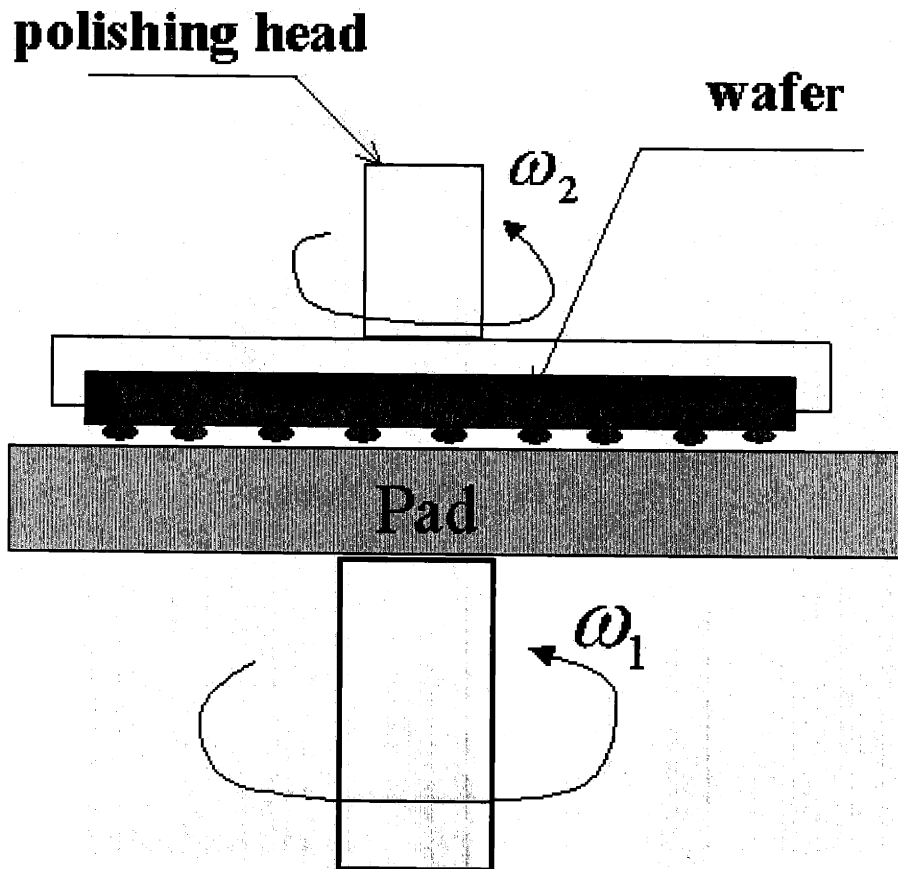


Figure 3-9: Chemical mechanical polishing (CMP) and its operating principle. The wafer is held against gravity by applying vacuum to the polishing head. The polishing is accomplished by the relative motion between the pad and the polishing head, resulting from the different angular velocities they rotate at.

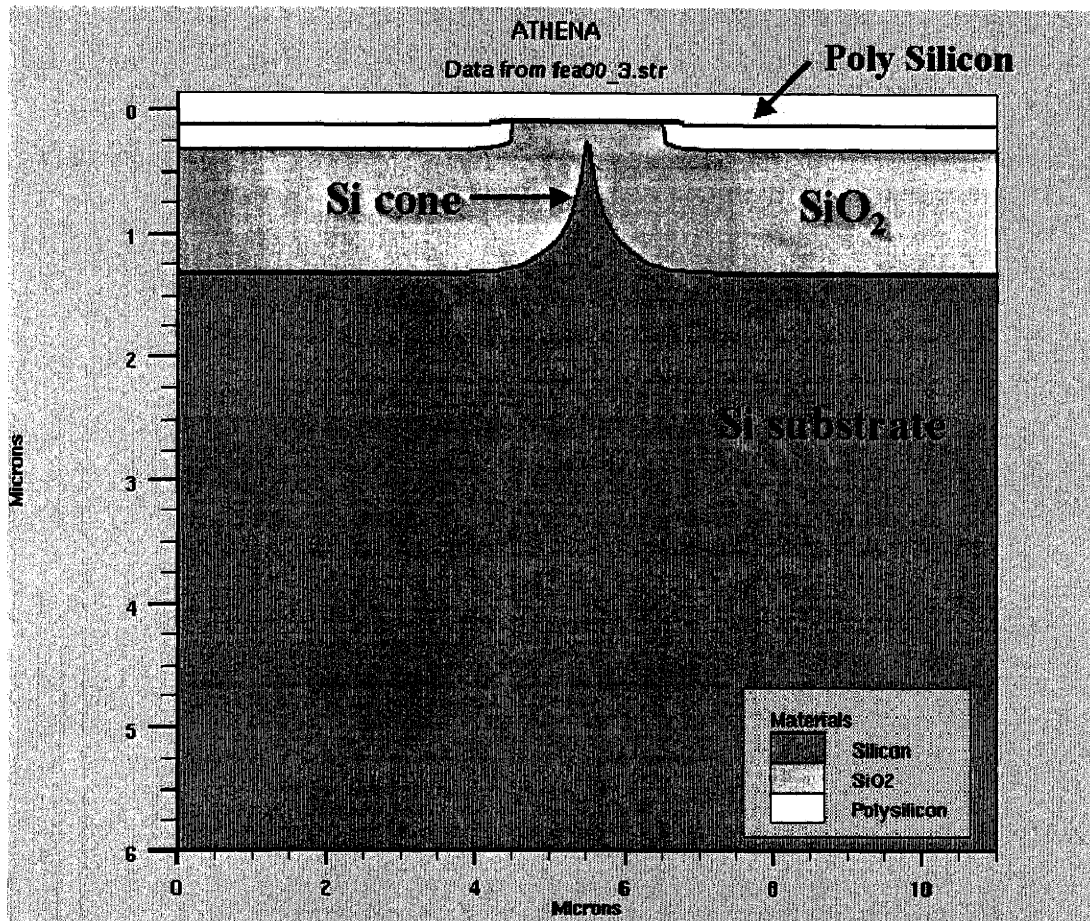


Figure 3-10: Simulation of the device structure after the chemical mechanical polishing. The gap in the polycrystalline silicon layer defines the gate aperture of the final field emitter structure.

pography remaining which continue to polish at an accelerated rate. This is expected to provide the large process window necessary in a manufacturing environment and reduces the demands on the equipment. However, because the polishing rate of doped polycrystalline silicon is quite large even for the the flat surface, a careful timed etch is still employed in this processing step.

### 3.1.3 Tip exposure

Standard photolithography was used to define the gate leads and pads, and the polycrystalline silicon was etched in  $SF_6$  plasma to complete the gate definition. The sacrificial oxide layer was then etched in a HF solution to expose the silicon tip. Figure 3-11 shows the simulation of the oxide etching. Figure 3-12 shows the SEM picture of a cross-section of the final structure of a single gated field emitter showing the silicon substrate, the silicon dioxide dielectric layer, the polycrystalline silicon gate, and the silicon tip. Figure 3-13 shows an SEM picture of the four  $4\mu m$  pitch gated field emitter arrays with polycrystalline silicon electrodes in a single die. The array sizes are  $10 \times 10$ ,  $20 \times 20$ ,  $30 \times 30$ , and  $60 \times 60$ . Figure 3-14 is the top view of an array of field emitters with  $4\mu m$  pitch and figure 3-15 shows the top view of a single gated silicon field emitter. It can be observed that the gate apertures are very uniform. This is due to the conformal films deposited by LPCVD.

## 3.2 Device Characterization

The characterization was done for  $4\mu m$  pitch silicon field emitter arrays with array sizes of  $10 \times 10$ ,  $20 \times 20$ ,  $30 \times 30$  and  $60 \times 60$  on a single die. Device characterization was performed in ultra high vacuum environment at pressure of about  $5 \times 10^{-10}$  Torr without bake out or field forming.

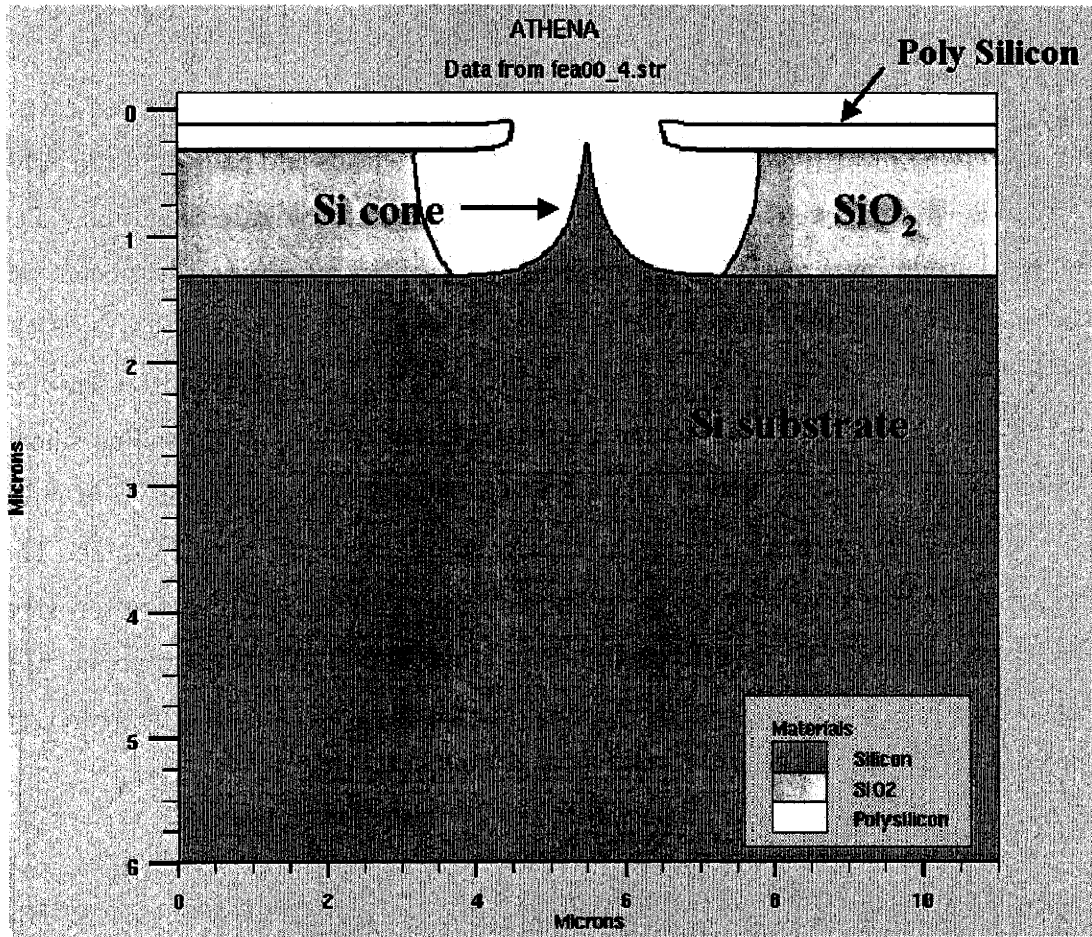


Figure 3-11: Simulation of the oxide etching. The gate aperture is revealed.

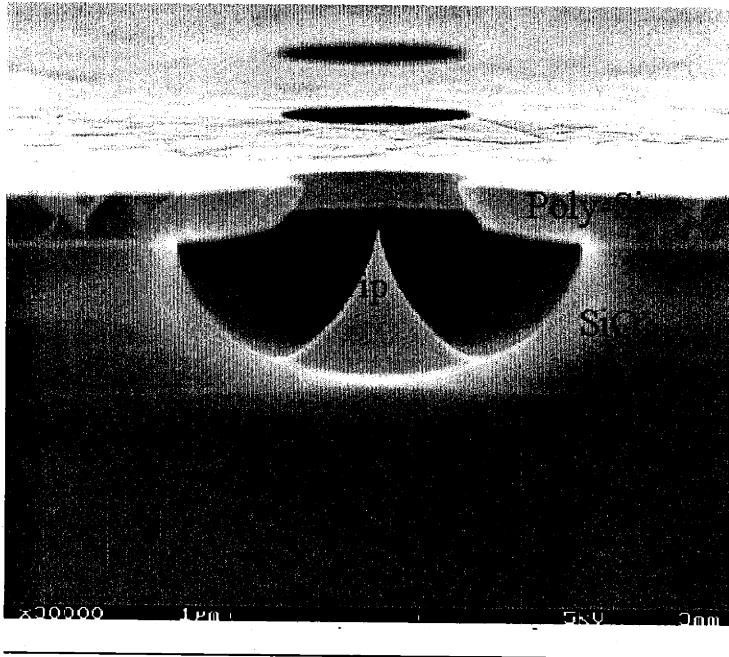


Figure 3-12: The final structure of a single gated field emitter.

### 3.2.1 Characterization setup

Figure 3-16 is a photograph of the actual test station while figure 3-17 shows a schematic of the configuration of the test system. The polycrystalline gate of each emitter array is probed on-wafer using a very sharp tungsten probe. The anode is a slab of Pt-coated silicon wafer; it is biased at a high gate voltage  $V_a$ . Both the gate and the anode are each connected to a *Keithley 237* source measure unit (SMU) which sources the voltage and measures the current. The backside of the wafer is in contact with the metal sample holder, which is in turn connected to a *Keithley 6517* multimeter, which is grounded and measures the emitter current. A high resolution camera placed above the wafer stage outside the main test chamber magnifies the images of the surface of the wafer.

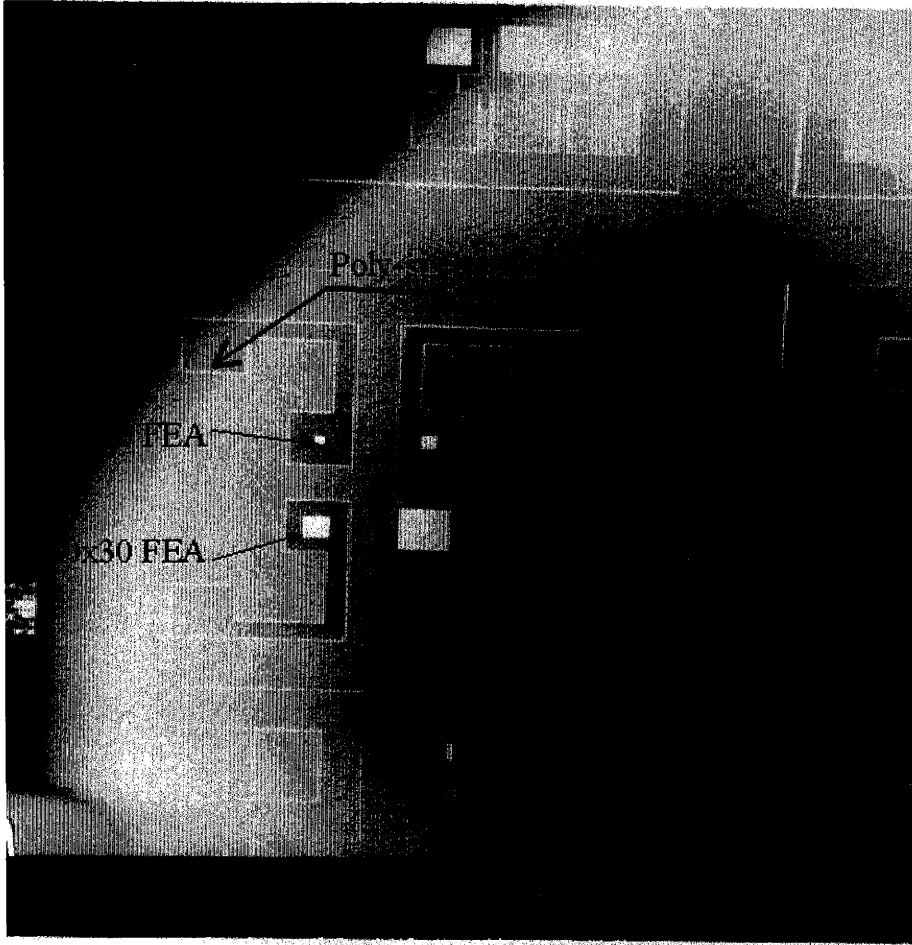


Figure 3-13: An SEM picture of the four  $4\mu\text{m}$  pitch gate field emitter arrays.

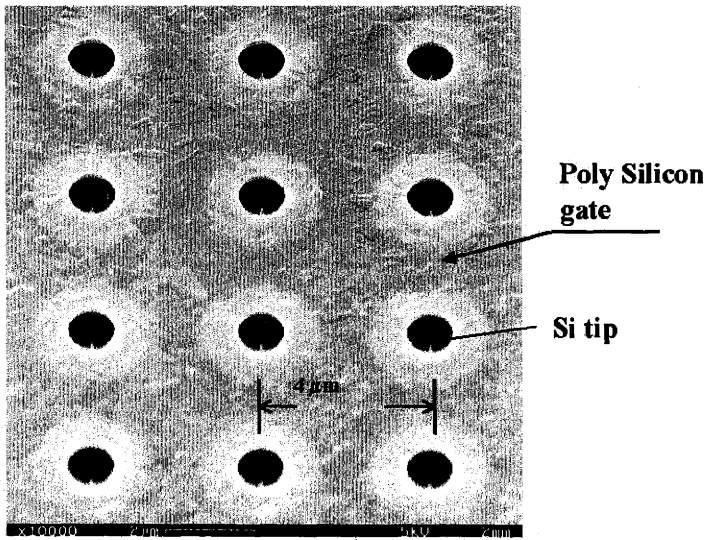


Figure 3-14: The top view of an array of field emitters with  $4\mu m$  pitch. In normal triode operation, an anode structure, typically another silicon wafer, is placed above the array. Electrons are emitted from the silicon tip (emitter), shown in this SEM, when a voltage is applied to the poly silicon gate, also shown in this SEM. The emitted electrons are collected by the anode, not shown in this SEM.

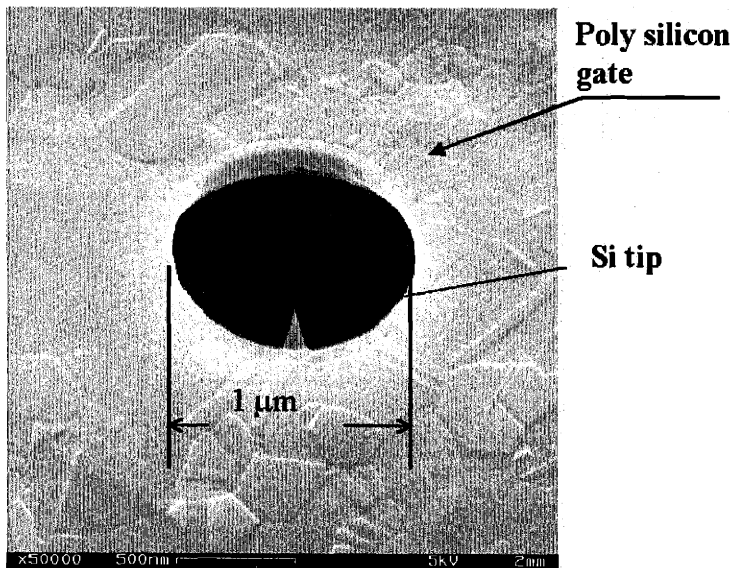


Figure 3-15: Top view of a single gated silicon field emitter.

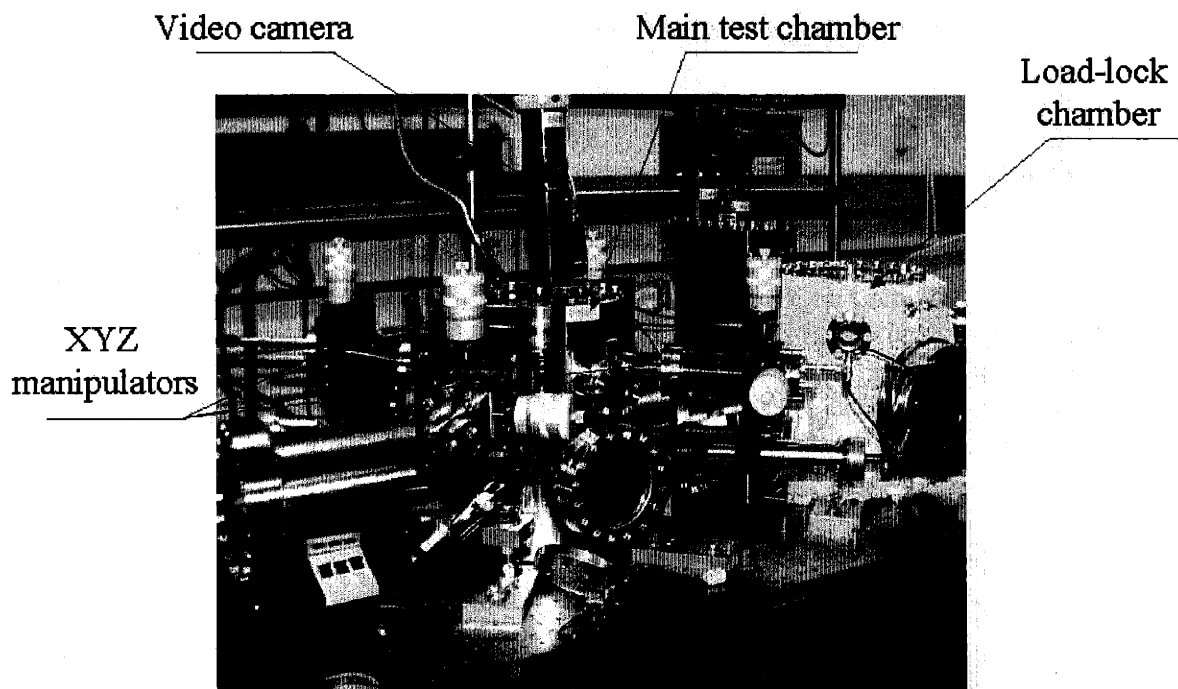


Figure 3-16: The picture of the ultra high vacuum characterization station. The chamber on the left is the main test chamber, the chamber on the right is the loadlock chamber. Pre-testing bake-out of the wafer is sometimes carried out in the loadlock chamber before the wafer is transferred to the main test chamber.



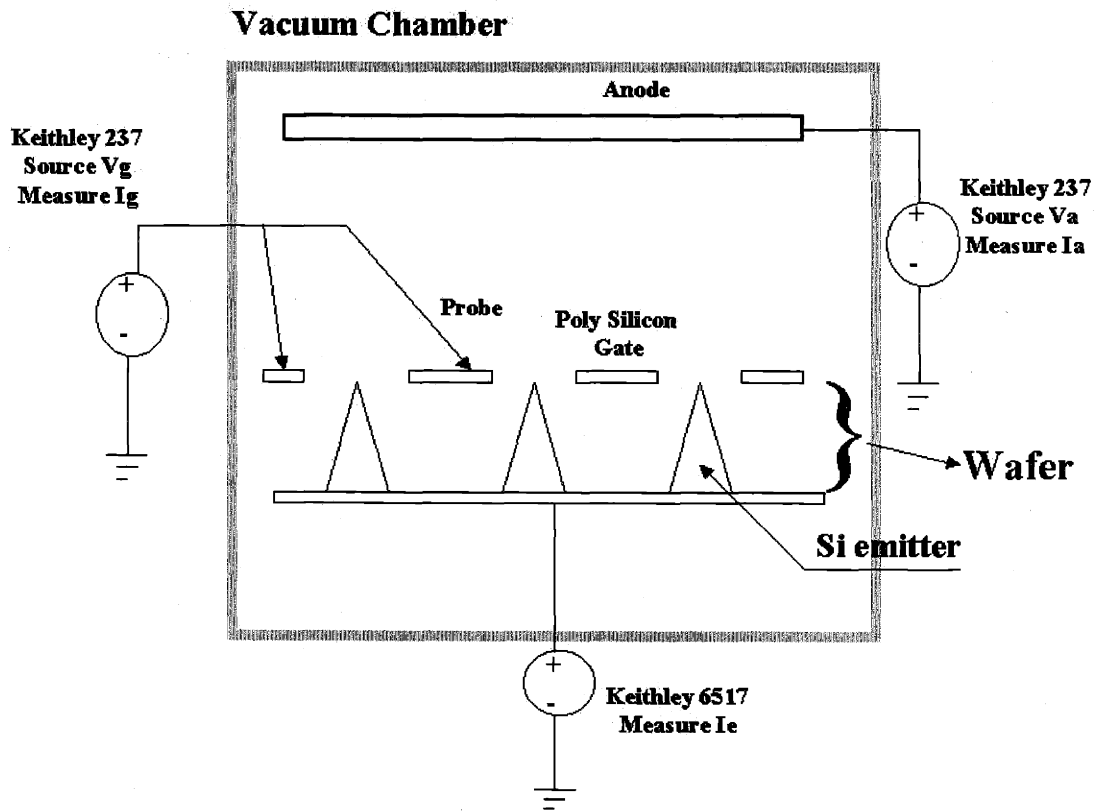


Figure 3-17: The schematic of the main testing chamber and the electronics setup. A high resolution camera (not in the figure) is placed above the test stage outside the main test chamber to take magnified images of the surface of the wafer. The anode is a slab of Pt coated silicon wafer that is held by metal clamp and can be moved by one of the XYZ manipulators in figure 3-16.

### 3.2.2 Transfer IV Characterization

Emitter current  $I_e$ , anode current  $I_a$ , and gate current  $I_g$  were monitored. The anode was a Pt-coated silicon wafer or a phosphor screen. The anode voltage  $V_a$  was fixed at 1000V and the anode-substrate distance was fixed at about 1cm. The gate voltage was sourced and the currents were recorded by three individual *Keithley* 237 SMUs. The gate voltage was ramped from 0V to a predefined value. The data was acquired using *Labview* from National Instruments. The probe station and the computer communicate and transport data through a *GPIB* cable and card.

Typically, the I-V curve and Fowler-Nordheim plot of  $\ln(I/V^2)$  vs.  $1/V$  as in figure 2-11 are analyzed for the examined devices.

## 3.3 Device analysis

The device analysis showed that the I-V characteristics agree with Fowler-Nordheim theory. The devices also demonstrated excellent properties required of field emission device applications. We will discuss them in the following text.

### 3.3.1 Agreement with Fowler-Nordheim theory

Figure 3-18 and Figure 3-19 are the I-V curves and the corresponding Fowler-Nordheim plot of a  $60 \times 60$  field emitter array. In the text below we will analyze the experimental data in more detail. Let's repeat the Fowler-Nordheim equation 2.52 here

$$I = a_{FN} V^2 e^{-b_{FN}/V} \quad (3.1)$$

where

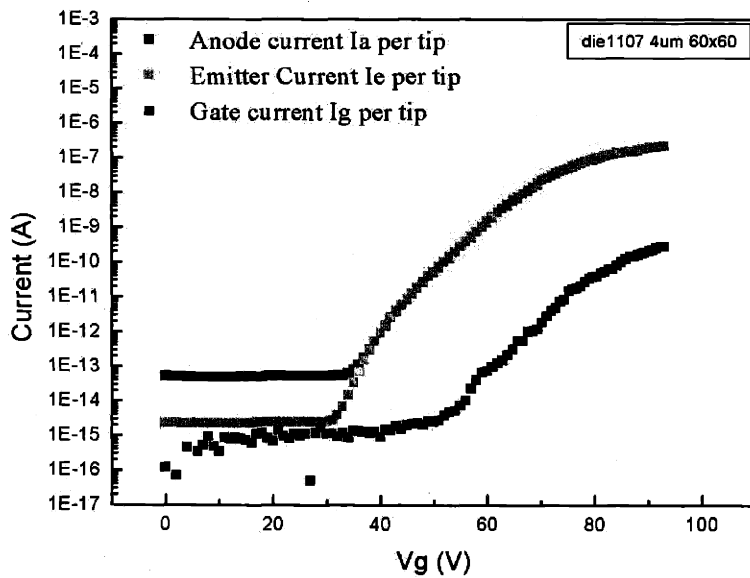


Figure 3-18: A typical I-V curve of a field emitter array. Anode current  $I_a$ , emitter current  $I_e$ , and gate current  $I_g$  are all plotted. The  $x$  axis is on a linear scale while the  $y$  axis is on a logarithmic scale.

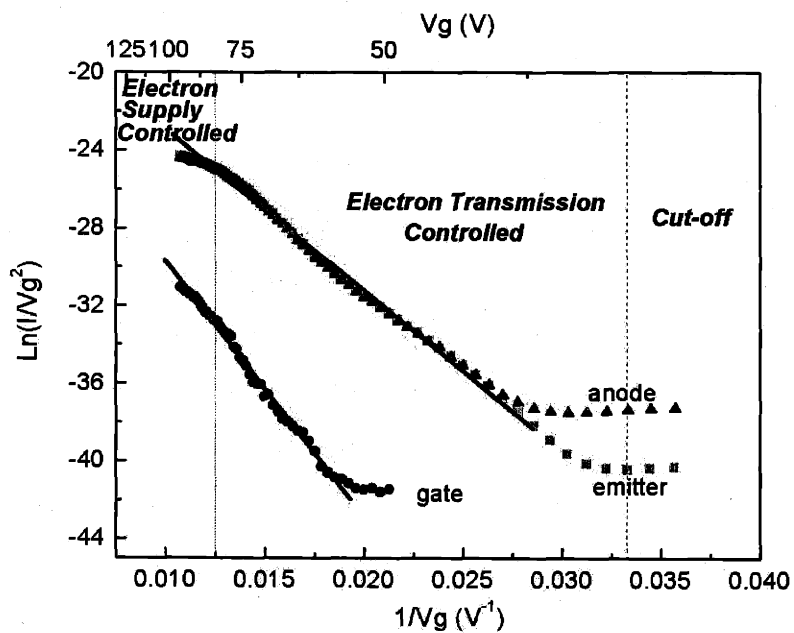


Figure 3-19: The Fowler-Nordheim plot of the data in figure 3-18.

$$\begin{aligned}
a_{FN} &= \frac{\alpha A \beta^2}{1.1 \varphi} e^{\frac{B(1.44 \times 10^{-7})}{\varphi^{\frac{1}{2}}}} \\
b_{FN} &= \frac{0.95 B \varphi^{\frac{3}{2}}}{\beta} \\
A &= 1.54 \times 10^{-6} \\
B &= 6.87 \times 10^7
\end{aligned}$$

$\alpha$  is the effective emitter area,  $\varphi$  is the workfunction, and  $\beta$  is the field factor.

Figure 2-13 shows the energy diagram of a semiconductor under an external electric field. For silicon, in the absence of field penetration, the barrier height for the conduction band electrons is the electron affinity  $\chi$ , which is 4.05 eV (Appendix B.1). The energy gap  $E_g$  of silicon is 1.12 eV. For silicon, the electrons in the valence band are also the source of emission electron. The theory has been discussed in chapter 2 and we will discuss the experimental results of valence band electron field emission from silicon in chapter 5. In this chapter we will limit our discussion to conduction band electron field emission. From the discussion of semiconductor emission in section 2.7, it is known that the field penetration plays a role in field emission effects of semiconductors. The conduction band minimum dips below the Fermi level because of field penetration, effectively reducing the barrier height (refer to figure 2-13 too). However, for conduction band electron field emission, the voltage applied is not very high, the electric field at the surface of the emitter is moderate, rendering the effect of the lowering insignificant across the range of testing. For example, from equation 3.3 below, it is learned that the electric fields of conduction band emission are of the order of  $2 \times 10^7 \text{V/cm}$ . According to equation 2.61, the decrease in barrier height is of the order of  $\nu F^{\frac{4}{5}}$  where  $\nu = 4.5 \times 10^{-7} \epsilon^{-\frac{2}{5}}$  and  $\epsilon = 11.9$  is the dielectric constant of silicon. Substituting  $F = 2 \times 10^7 \text{V/cm}$  into this formula, the reduction in barrier height is approximately 0.11 eV, which is very small compared to the electron affinity of silicon. It is worthy of noting that the surface states of silicon could act as capture

sites for electrons, thus creating an internal barrier, as suggested by Stratton [61]. For a typical surface state density of  $\sigma = 1.2 \times 10^{13}/\text{cm}^2$  [61, 130], an external electric field of

$$F = \frac{\sigma}{\epsilon_0} = \frac{1.2 \times 10^{13} \times 1.6 \times 10^{-19} \text{C}/\text{cm}^2}{8.85 \times 10^{-14} \text{F}/\text{cm}} = 2.17 \times 10^7 \text{V}/\text{cm} \quad (3.2)$$

is needed to overcome the surface states. This value is very close to the turn-on electric field  $1.92 \times 10^7 \text{V}/\text{cm}$  of our device, as we will see below. Upon the turn-on of our device, the surface states had been overcome. So, for simplicity, we ignore these secondary effects in our discussion here.

From Figure 3-18 it is observed that the device turned on at about 30V, with the turn-on voltage defined as the voltage at which the emission current exceeds the noise floor of about 10pA. The anode current  $I_a$  and emitter current  $I_e$  almost overlap on top of each other. In the 30-80 V range, we see a steady exponential increase of current. After that the curve levels off. From figure 3-19 it is observed that there is a linear fit of the data, indicating good agreement with Fowler-Nordheim theory. Using the slope of the FN plot ( $b_{FN}$ ) and  $\chi = 4.05$  eV, an effective field factor,  $\beta$ , was calculated to be  $6.4 \times 10^5 \text{cm}_{-1}$ . At a gate voltage of 30 V this gives an electrostatic field of

$$F = \beta V_g = 6.4 \times 10^5 \text{cm}^{-1} \times 30 \text{V} = 1.92 \times 10^7 \text{V}/\text{cm}. \quad (3.3)$$

It is also observed that the Fowler-Nordheim plots of the emitter (anode) and gate currents have different slopes as shown in figure 3-19. There are three possible sources for the gate leakage current at high anode voltages. These are

- vacuum emission of electrons from the tip to the gate;

- leakage along the oxide surface between the gate and emitter electrodes and
- Fowler-Nordheim emission of electrons from the substrate to the polycrystalline silicon gate through the silicon dioxide [119].

The difference in slopes between the Fowler-Nordheim plots of gate and emitter (anode) currents suggest that the third source may be dominant.

### Modeling using “ball in sphere” model

Using the “ball in a sphere” model in section 2.8.1 and according to equation 2.66  $\beta = 1/r$  where  $r$  is the tip radius of curvature, we extracted a tip radius of curvature of about  $15.6nm$  which is, to a certain extent, in agreement with the SEM measurement of  $9.2nm$ .

### Modeling by using numerical simulation

The “ball in sphere” model provides an analytical expression of the field factor  $\beta$ . It is an intuitive but very simplified electrostatic model. In this section, we will try to determine the field factor  $\beta$  using numerical simulation method. It is a non-analytical but a more sophisticated method intended to solve the problem by taking into consideration the actual structure of the field emitter. By assuming axial symmetry for the device structure (which is true for a majority of the cone shape emitters), the simulation can be considered in a 2-D space, which can significantly reduce computation complexity.

In this section the numerical simulation is carried out in a 2-D space for axially symmetric cone shape silicon field emitters in MATLAB’s Partial Differential Equation Toolbox (PDE Toolbox). Due to the axially symmetric nature of the problem, only half of the emitter structure needs to be defined in this case. Figure 3-20 shows a

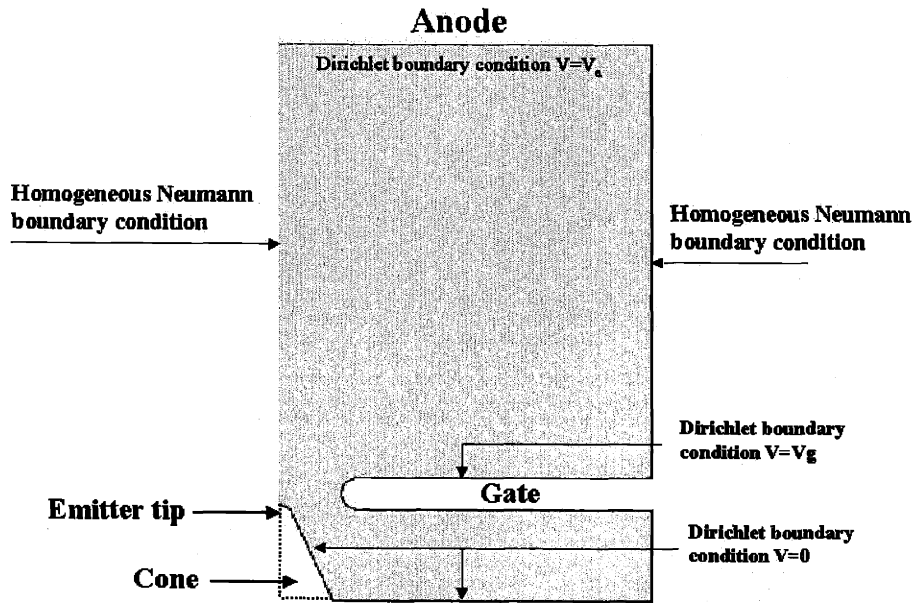


Figure 3-20: Problem space with boundary conditions.

layout of the problem space with labels added to indicate boundary conditions. The model is made up of a half cone and a half gate aperture. The problem space is defined to ten times the gate aperture in the  $z$  direction and three times the gate aperture in the  $r$  direction. This choice was proposed by David Pflug [89] because it gave a stable emitter tip electric field, independent of the  $z$  or  $r$  dimensions.

The top edge in the problem space is selected as a boundary with a Dirichlet boundary condition of  $V = V_a$ , representing that the potential at the anode is  $V_a$ . The left edge is set to a homogeneous Neumann boundary condition and represents the  $z$ -axis in the cylindrical coordinate system. The right edge is also defined to be a homogeneous Neumann boundary condition. At these two edges, there are no normal components of the electric field. This is a direct result from the axial symmetry of the problem. The bottom edge of the problem space and surface of the emitter tip is assigned a Dirichlet boundary condition of  $V = 0$ , representing that it is connected to the ground. The surface of the gate is assigned to a Dirichlet boundary condition of  $V = V_g$ , representing the applied gate voltage. Figure 3-21 shows a finite element

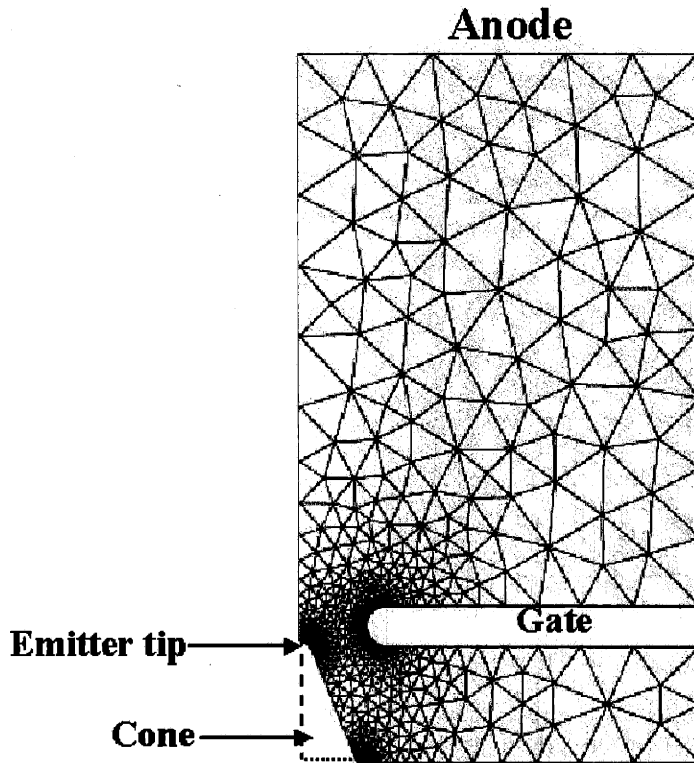


Figure 3-21: Finite element method (FEM) mesh of the problem space.

method (FEM) mesh of the problem space. In this mesh the edge of the emitter is modeled by straight line. The mesh is automatically generated by the MatLab's PED toolbox. The routine needs an input of the fineness of the mesh and it will generate corresponding mesh accordingly. Basically It uses a Delaunay triangulation algorithm. Details of the algorithm can be accessed in reference [95, 96]. The mesh size is determined from the shape of the geometry. At the places of interest such as the tip area the mesh triangle is much finer.

For the structure shown in figure 3-12, the field factor  $\beta$  was calculated as a function of the tip radius  $r$  using the above numerical method. The result is shown as the scatter data points in figure 3-23. Fitting of the data gave an excellent power law dependence of  $\beta$  on  $r$  as shown by the red line:



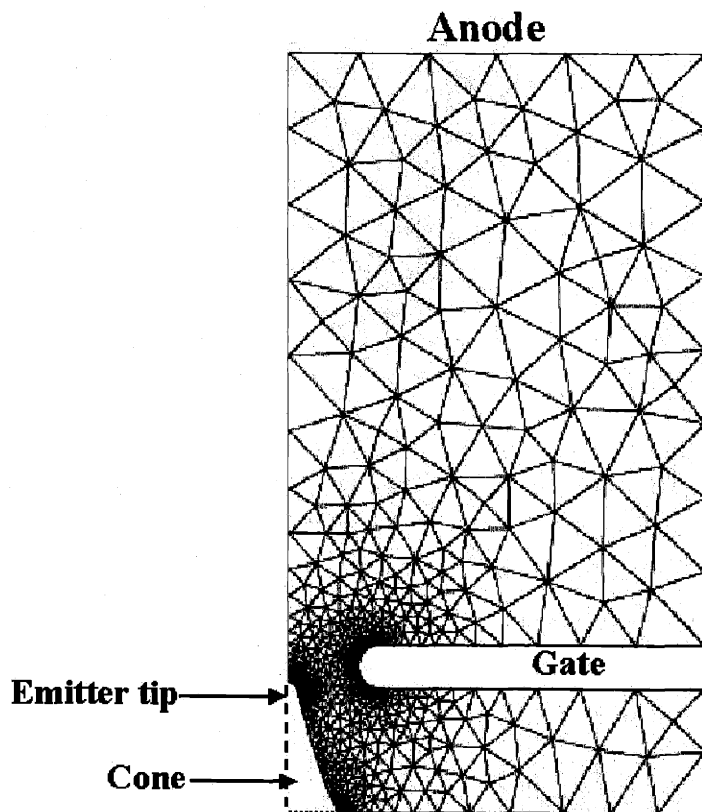


Figure 3-22: Another finite element method mesh of the problem space, taking the curve nature of the emitter base into consideration.

$$\beta = \frac{22.73 \times 10^5}{r^{0.69266}} \text{cm}^{-1} \quad (3.4)$$

where  $r$  is in units of  $nm$ . Considering the curved nature of the emitter base shape as illustrated in figure 3-12, another “parabolic” cone shape can be used for the numerical model. The model is illustrated in figure 3-22. For the same radius of curvature  $r = 5nm$ , the “straight edge” model gives  $\beta = 7.50 \times 10^5 V/cm$ , while the “parabolic” model gives  $\beta = 7.58 \times 10^5 V/cm$ . The difference is about 1.06%. This difference is about the same magnitude of the numerical simulation error of about 0.92% when using fine and very fine meshing parameters. This result shows that the two models have negligible differences. This result also shows that the tip radius of curvature is the most important factor determining the field factor, while the emitter base shape has minimal effect. Based on this observation the “straight edge” model is used all along.

Equation 3.4 differs significantly from the “ball in sphere” model which can be written as

$$\beta = \frac{10^7}{r} \text{cm}^{-1} \quad (3.5)$$

if  $r$  is in units of  $nm$ . The blue line in figure 3-23 is the “ball in sphere” model’s  $1/r$  dependence.

According to equation 3.4, the experimentally observed  $\beta = 6.4 \times 10^5 \text{cm}^{-1}$  corresponds to a tip radius of  $r = 6.23nm$ , in good agreement with the SEM measurement of  $9.2nm$ .

Dvorson et al. [93, 94] developed a “bowling pin” model to analyze the conical field emitter and analytically derived a dependence of  $\beta$  on  $r$ :  $\beta \sim \frac{1}{r^{0.8}}$ . By assuming a tip radius of  $r = 8.6nm$ , the “bowling pin” model agrees with the experimental

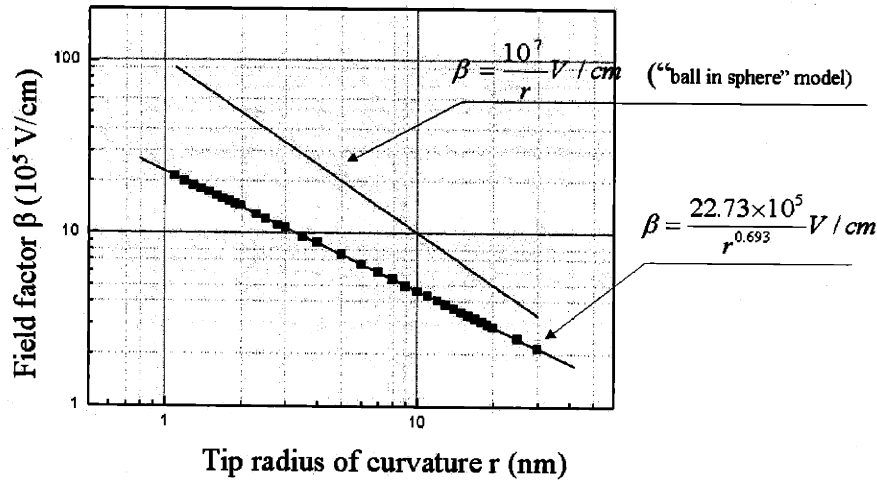


Figure 3-23: Dependence of field factor  $\beta$  on the tip radius  $r$ . The blue line is the “ball in sphere” model’s  $1/r$  dependence. In the calculation, the following parameters are used: tip height= $855nm$ , oxide thickness= $822nm$ , gate thickness= $283nm$ , and gate aperture= $1000nm$ .

data well. Yang et al. fitted the experimental data by applying a full 3-dimensional electrostatic simulation CAD tool using a boundary element method [92, 101]. By assuming a tip radius of  $8.2nm$ , a good match was obtained between our device data and their simulation. His model does not require the device structure to have any symmetry, but the model is very much computationally expensive.

Based on the discussion above, it appears, qualitatively, that the real curve of dependence of  $\beta$  on  $r$  lies in between the two lines in figure 3-23. The “ball in sphere” model serves as an upper bound, because in this model, all the electric flux lines originating from the “sphere” gate terminate at the inner “ball”, resulting in maximum field enhancement. The other line in figure 3.4 serves as the nominal lower bound because in this model the gate dielectric in the real device is replaced by vacuum (refer to figure 3-20), resulting in the “loss” of electric flux lines in the parallel capacitor, leading to reduced field enhancement.

Table 3.1 summarizes the results for this particular device.

Table 3.1: Summary of physical parameters of field emitter array shown in figure 3-18 (wafer1\_die1107\_4 $\mu m$ \_60  $\times$  60)

$\alpha$	$\beta$	$r_{SEM}$	$r_{ball\ in\ sphere}$	$r_{2D}$	$r_{bowlingpin}$	$r_{3D-CAD}$
$2.52 \times 10^{-14} cm^2$	$6.4 \times 10^5 cm^{-1}$	9.2nm	15.6nm	6.23nm	8.6nm	8.2nm

### 3.3.2 Low turn-on voltage

Figure 3-24 shows the emitter and gate currents per tip of a 60  $\times$  60 field emitter array. The vertical axis is the emitter current per emitter on a log scale. The horizontal axis is gate voltage on a linear scale. The emitter array turns on at a gate voltage of about 20 volts, with the turn-on voltage defined as the voltage at which the emission current exceeds the noise floor ( $\approx 2 \times 10^{-15}$  A/tip).

On another wafer we are able to observe even lower turn-on voltages. Figure 3-25 shows the I-V curve of an 30  $\times$  30 device with a gate aperture of about 0.75 $\mu m$ . The height of the emitters on this wafer is about 0.5 $\mu m$ . A turn on voltage of about 16V is observed in this device. In another array in the same die a turn-on voltage of 14V is also observed.

The Fowler-Nordheim plot of the data shown in figure 3-25 is shown in figure 3-26. The experimentally obtained field enhancement factor was  $\beta = 21.925 \times 10^5 V/cm$ . Using the “ball in sphere” model, the tip radius is calculated to be  $r = 4.56nm$ .

The device of figure 3-25 was also numerically simulated using the model presented in section 3.3.1. Based on the dimensions of the structure, a dependence of  $\beta$  on  $r$  was calculated to be:

$$\beta = \frac{23.86 \times 10^5}{r^{0.69129}} cm^{-1} \quad (3.6)$$

### Emitter and Gate Current per Tip vs. Gate Voltage

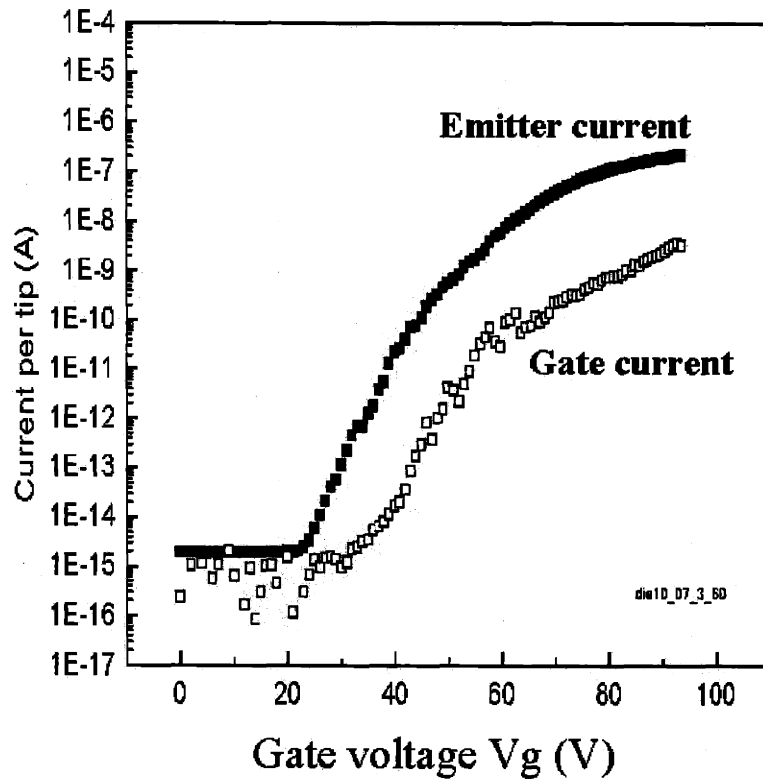


Figure 3-24: The emitter and gate currents per tip of a  $60 \times 60$  field emitter array. The vertical axis represents emitter current per emitter on a log scale in units of Amps. The horizontal axis represents the gate voltage on a linear scale in units of Volts. The emitter array turns on at a gate voltage of about 20 volts, with the turn-on voltage defined as the voltage at which the emission current exceeds the noise floor ( $\approx 2 \times 10^{-15}$  A/tip).

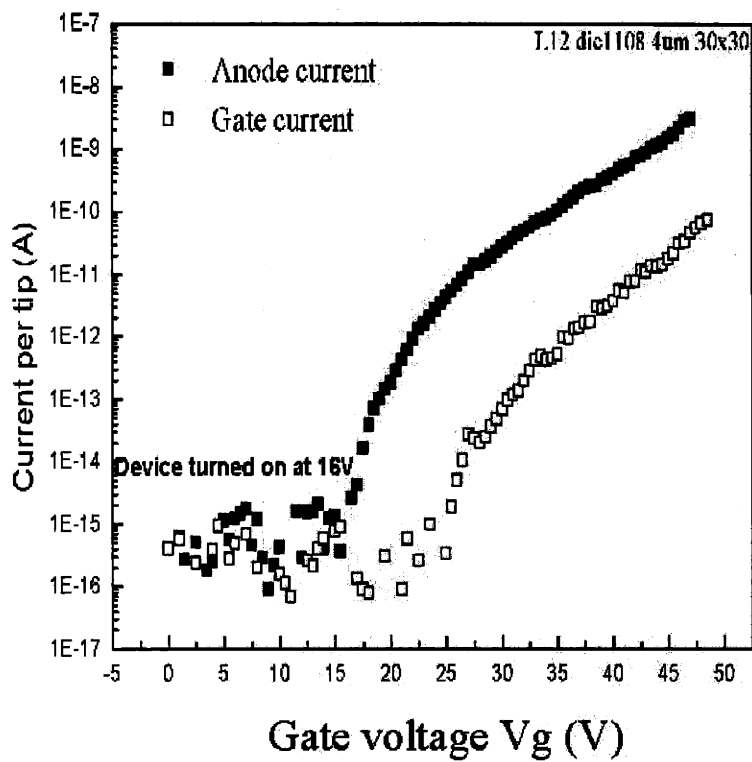


Figure 3-25: The I-V characteristics shows a very low turn-on voltage of about 16V. In this device the height of the emitter is about  $0.5\mu m$  and the gate aperture is about  $0.75\mu m$ .

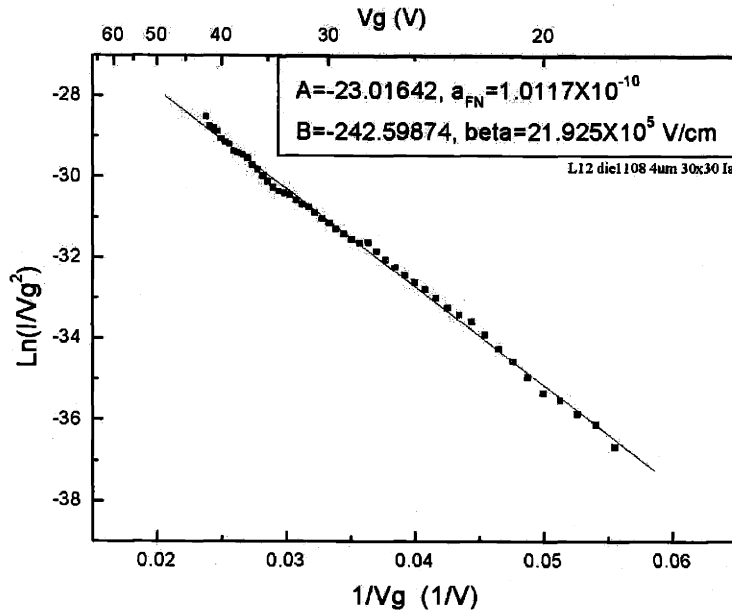


Figure 3-26: Fowler-Nordheim plot of the data in figure 3-25.  $\beta = 21.925 \times 10^5 \text{ V/cm}$ .

Table 3.2: Summary of physical parameters of field emitter array shown in figure 3-25 (L12.die1108.4 $\mu\text{m}$ .30  $\times$  30)

$\alpha$	$\beta$	$r_{SEM}$	$r_{ballinsphere}$	$r_{2D}$
$4.463 \times 10^{-19} \text{ cm}^2$	$21.93 \times 10^5 \text{ cm}^{-1}$	not measured	4.56nm	1.13nm

where  $r$  has units of  $nm$ . Figure 3-27 compares this dependence with the “ball in sphere” model’s  $1/r$  dependence.

Equation 3.4 and equation 3.6 are very similar although the two devices corresponding to these two equations have different dimensions. This observation indicates that for device structures similar to figure 3-12 the field factor depends primarily on the tip radius  $r$ .

According to equation 3.6, the experimentally observed  $\beta = 21.925 \times 10^5 \text{ V/cm}$  corresponds to a tip radius of  $r = 1.13 \text{ nm}$ . Table 3.2 summarizes the results for this particular device.

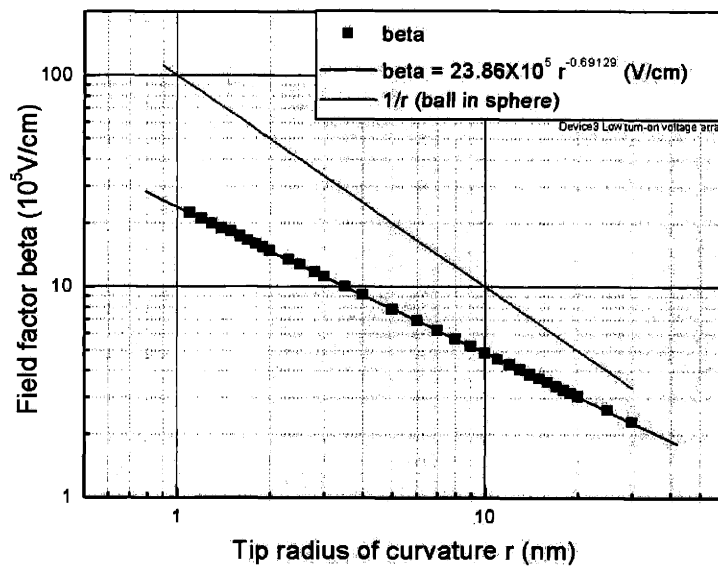


Figure 3-27: Dependence of the field factor  $\beta$  on the tip radius  $r$  for the device in figure 3-25. The blue line is the “ball in sphere” model’s  $1/r$  dependence. In the calculation, the following parameters are used: tip height= $462nm$ , oxide thickness= $477nm$ , gate thickness= $110nm$ , and gate aperture= $750nm$ .



We attribute the extraordinary low turn-on voltages to the small radius curvature of the emitter tip we were able to achieve. From field enhancement's "ball in a sphere" model (section 2.8.1) and equation 2.65, or from equation 3.4 and equation 3.6, it is learned that the field factor  $\beta$  is strongly dependent on the radius of curvature of the emitter tip. Especially when the gate aperture is large, the value of the gate aperture's effect on  $\beta$  is minimal. The gate apertures in our devices are quite large compared to the small aperture devices [89]. So the tip radius plays a dominant role in field enhancement.

SUPREM-IV simulation of oxidation sharpening process only gave us an approximate period of time that is needed for the oxidation. However, the results of the oxidation sharpening process need to be monitored frequently in order to guarantee good results. After one step of oxidation sharpening, the tips were observed in an in-lab SEM that is compatible with the CMOS processing in ICL. A rough measurement of the tip sharpness was obtained and if the tip was not sharp enough, another round of oxidation was conducted for a new period of time. Sometimes this process was repeated several times to get a satisfactory result. Then the fabrication proceeded to the next step.

Through a carefully controlled oxidation sharpening process as described as above, we have been able to achieve extremely sharp emitter tips with a radius of curvature in the vicinity of  $1nm$ . Figure 3-28 and Figure 3-29 are two *Transmission Electron Microscope* (TEM) [89] pictures of one of the emitter tips. Figure 3-28 is at a magnification of  $100K$  and Figure 3-29 is at magnification of  $400K$ . In figure 3-29 the atomic lattice structure of  $Si\{111\}$  planes with a spacing of  $3.13\text{\AA}$  can be observed. The observed radius of curvature of the very tip is about  $1nm$ .

The values of the tip radius we achieved agree with the literature on oxidation sharpening. David Pflug achieved a similar tip radius in  $70nm$  gate aperture silicon field emitter arrays [89]. Koga et al. achieved less than  $5nm$  tip radius in silicon field emitters using an oxidation sharpening and lift-off technique [104]. Marcus et al.

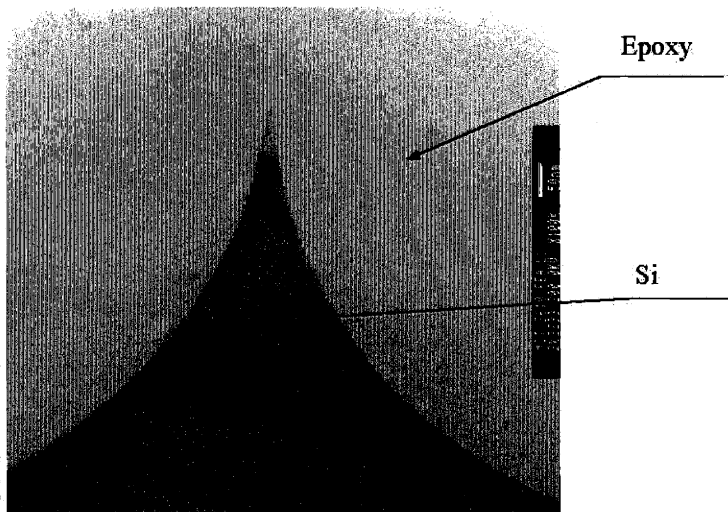


Figure 3-28: TEM picture of an emitter tip. The magnification is  $100K$ .

[76, 77] experimented with dry oxidation sharpening of silicon tips also at a temperature of  $950^{\circ}C$ , as we did. They were able to achieve a tip radius of curvature of  $< 1nm$ . Figure 3-31 is quoted from reference [76], showing a TEM picture of their tip apex after oxidation sharpening. We believe that these atomically sharp emitter tips played a major role in the making of the low turn-on voltages observed. The striking similarity between figure 3-29 and figure 3-31 suggests that the dry oxidation sharpening contributes to the uniformity of silicon emitter tips.

Approximately 80 data values of the tip radius of our emitter tips were collected from TEM images taken from a JEOL 2010 Microscope. The data were compiled to the histogram picture shown in figure 3-30. The data fit with the lognormal distribution [99, 100]. The fitting gave an expected value of  $1.75nm$  for the tip radius and a shape parameter (standard deviation) [99] of  $0.74nm$ . This observation agrees with the value of the tip radius of  $1.13nm$  shown in table 3.2 as calculated from the 2-D numerical model for the device in figure 3-25. David Pflug [89] fabricated silicon tips with a base dimension of about  $100nm$  and obtained a similar lognormal distribution of tip radii with an expected value of  $4.5nm$  and a shape factor of  $0.498nm$ .

Due to the nature of their fabrication process, Spindt type emitters typically have

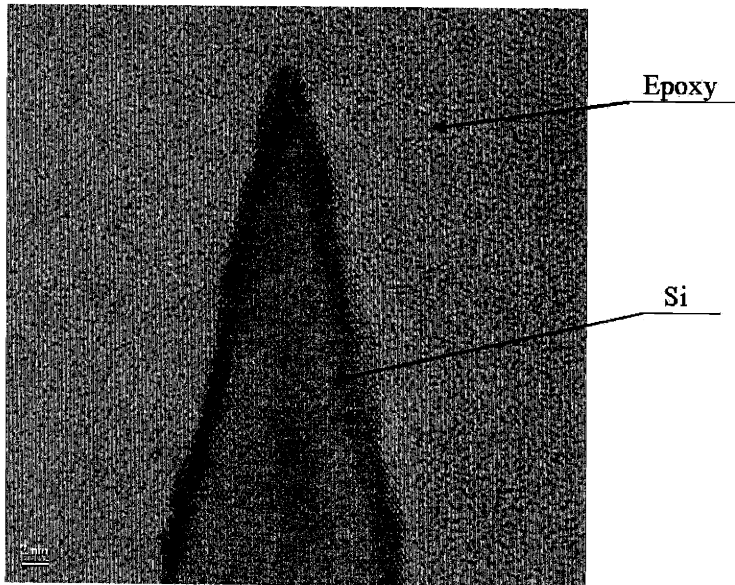


Figure 3-29: TEM picture of an emitter tip. The magnification is  $400K$ . The atomic lattice structure of  $Si\{111\}$  planes with a spacing of  $3.13\text{\AA}$  is seen. The radius of curvature of the very tip is around  $1nm$ .

larger tip radii of curvature. Spindt et al. [19] fabricated  $1\mu m$  gate apertures,  $0.75\mu m$  tip height metal field emitters using molybdenum. The emitter tip radius is about  $40nm$ . Adler et al. [66] fabricated gated arrays of molybdenum-coated polycrystalline silicon tips with  $10\mu m$  pitch size. The tip radius is about  $30nm$ . Hyung et al. [122] fabricated gated silicon field emitter arrays on n-type silicon substrates using a “lift-off” technique, which is similar to the one used in Spindt type emitters. The tip radius of curvature is about  $24nm$  [122]. However, David Pflug was able to achieve a tip radius as low as 6 to  $7nm$  in  $100nm$  gate aperture molybdenum emitter arrays fabricated using interferometric lithography [98].

### 3.3.3 High current density, very good current uniformity, low leakage current, and high transconductance

Figure 3-32 shows the data of the emitter and gate currents as a function of the gate voltage for  $4\mu m$  pitch field emitter arrays within a certain die. The data are for four

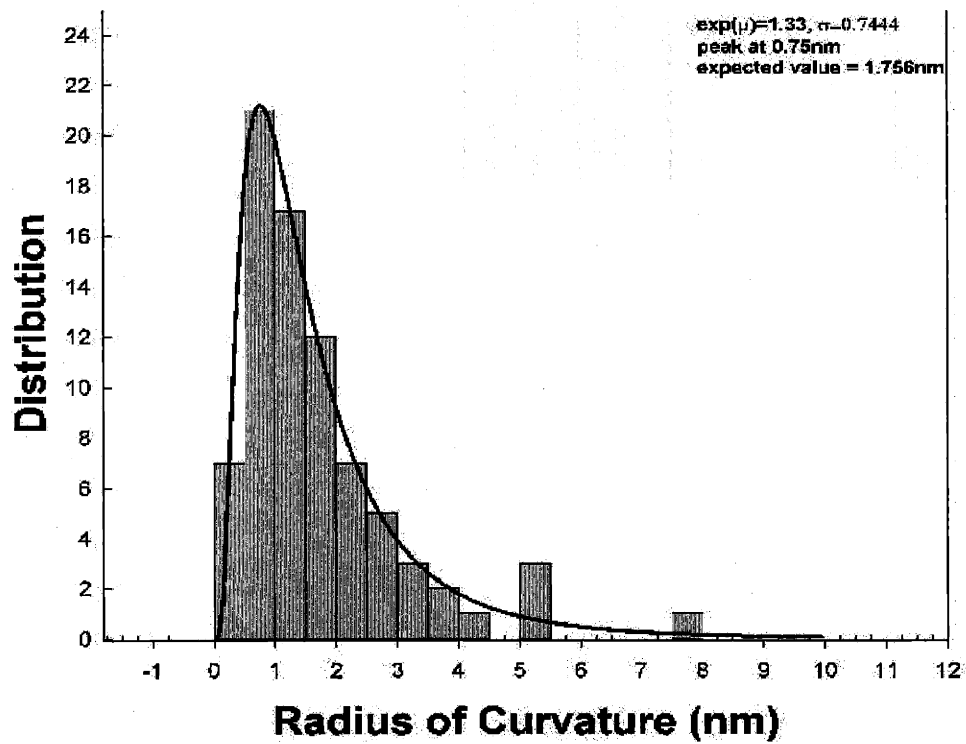


Figure 3-30: The lognormal distribution of the tip radii of the silicon emitters. The data from about 80 tips is shown by the bars of the histogram, and the curve line is the fit to a log-normal distribution.

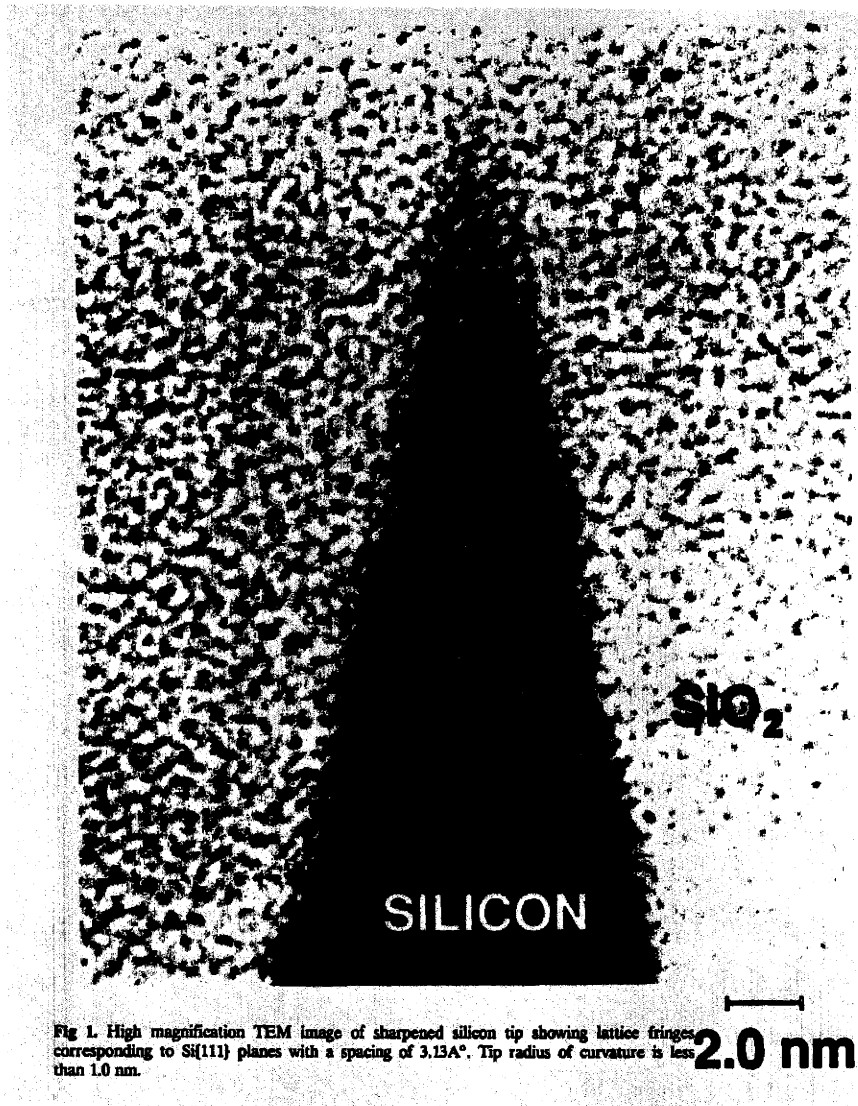


Figure 3-31: TEM of Marcus et al.'s oxidation sharpened silicon tip. The radius of curvature of the tip apex is less than 1nm. This figure is taken from reference [76].

individual field emitter arrays:  $10 \times 10$ ,  $20 \times 20$ ,  $30 \times 30$ , and  $60 \times 60$ . The field emitter arrays are all from the same die in the same wafer. The turn-on voltage for the four devices are all about 30V for this die. At a voltage of about 90 volts, the  $60 \times 60$  arrays have a current of about 1mA, corresponding to a nominal areal current density of  $1.8A/cm^2$ .

Figure 3-33 shows the currents per emitter of the same die as in figure 3-32. It is observed that the average emitter currents are the same for the four array sizes ranging from 100 tips to 3600 tips, indicating high electron emission uniformity. To the best of our knowledge, such uniformity of emission has not been reported before.

We attribute the very good uniformity to two factors:

- highly uniform tip radius as compared to tips defined by lift-off [121] and
- highly uniform aperture diameter due to the conformal, uniform low pressure chemical vapor deposited silicon dioxide and polycrystalline Si layers.

The excellent uniformity could lead to significant reductions in the array size required per pixel in FED applications and improved yield.

Furthermore, the gate leakage current of every field emitter array is about 3 to 4 orders of magnitude smaller than the corresponding emitter currents. These gate leakage currents are extremely small and negligible. Small gate leakage is very important to the efficiency of field emitter arrays. Furthermore, a gate voltage swing of 10 volts can modulate the emitter current by about 3 orders of magnitude, indicating a large transconductance. High current density and high transconductance are important factors for assessing the performance of field emission devices and applications.

The high current density and high transconductance can also be attributed to the sharpness of the tip. Sharp tip induces a higher field at relatively lower voltages. Also

## Emitter & Gate Currents vs. Gate Voltage

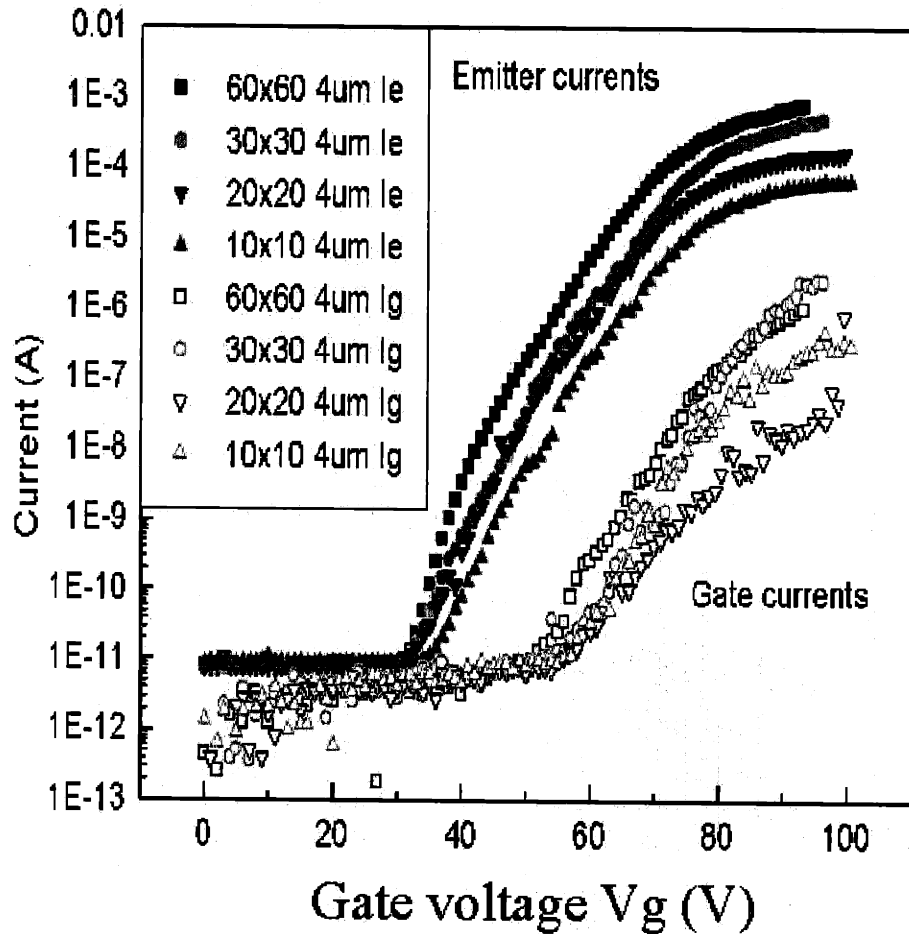


Figure 3-32: The emitter and gate currents as a function of the gate voltage for 4 $\mu$ m pitch field emitter arrays within a given die. The data represent four individual field emitter arrays: 10  $\times$  10, 20  $\times$  20, 30  $\times$  30, and 60  $\times$  60.  $I_e$  and  $I_g$  represent emitter current and gate current respectively.

## Emitter and Gate Currents per Tip vs. Gate Voltage

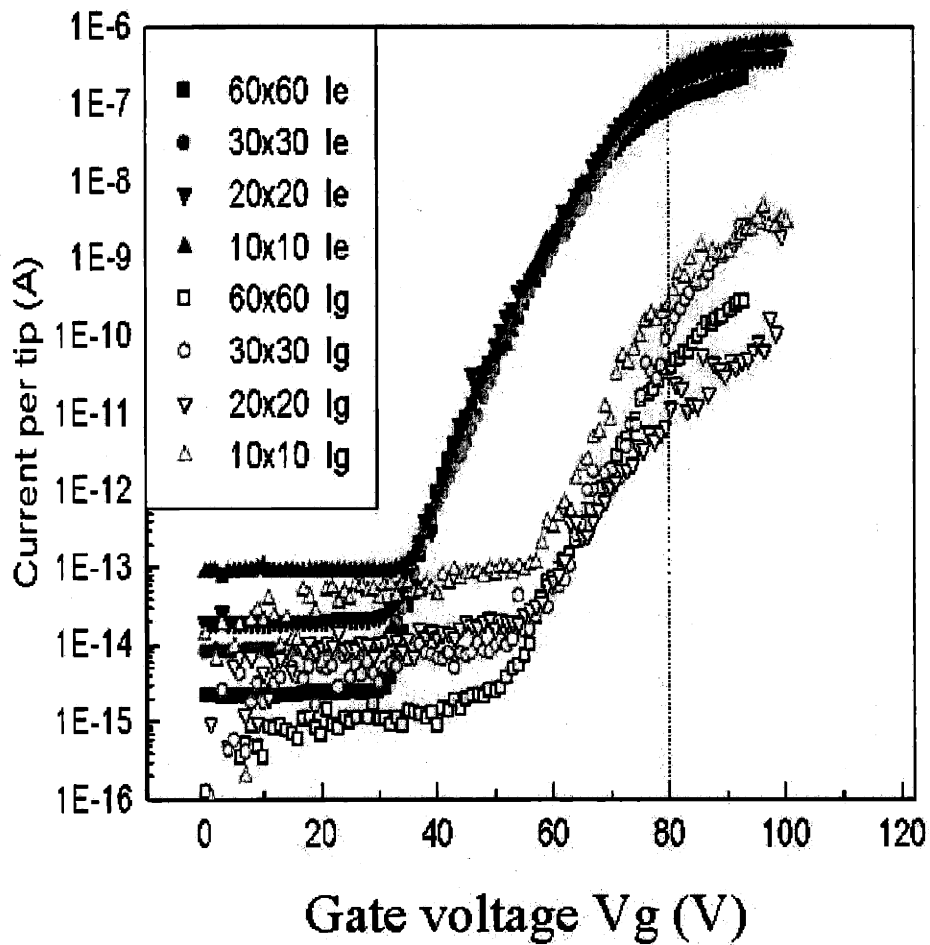


Figure 3-33: Normalized currents per emitter of the same die as figure 3-32. The average emitter currents are the same for the four array sizes ranging from 100 tips to 3600 tips, indicating high emission uniformity.



from equation 2.52 and equation 2.66 of the “ball in a sphere” model, an expression for  $b_{FN}$  in terms of the tip radius could be obtained:

$$b_{FN} \sim 0.95B\varphi^{\frac{3}{2}}r. \quad (3.7)$$

When  $r$  is smaller,  $b_{FN}$  is smaller, and thus the current increases faster with an increase of the gate voltage  $V_g$  due to the exponential factor  $e^{-\frac{b_{FN}}{V}}$  in the Fowler-Nordheim formula 2.52.

From equation 3.7,  $r$  can be calculated according to the following formula:

$$r_{FN} = \frac{b_{FN}}{0.95B\varphi^{\frac{3}{2}}} \quad (3.8)$$

Apply operator  $\ln$  to both sides of the equation and after that take a differentiation on both sides and finally it reads:

$$\frac{\Delta r_{FN}}{r_{FN}} = -\frac{3}{2} \frac{\Delta\varphi}{\varphi} \quad (3.9)$$

If we take into consideration the lowering  $\Delta\varphi$  of the barrier height  $\varphi$  due to field penetration, we can estimate the variation of the calculated tip radius of curvature according to equation 3.9. It was calculated previously that at a field of  $2 \times 10^7 V/cm$  the lowering of the barrier is approximately  $\Delta\varphi = 0.11eV$  (refer to section 3.3.1). Substitute this value and  $\varphi = 4.05eV$  for silicon’s electron affinity into equation 3.9, from which it is estimated that an approximately 4% variation will be incurred to the calculated  $r_{FN}$ . This is a very modest variation. It is insignificant when compared to the difference between the SEM measurement and the calculated tip radius of curvature. This estimate further justifies our decision to ignore the effect of barrier lowering in the beginning of section 3.3.1.

The low gate leakage current could be attributed to the high quality LPCVD oxide deposited as the dielectric insulator and the highly symmetric emitter structure. High quality densified LPCVD oxide (as good as thermally grown oxide) could significantly reduce the tunneling current through the oxide. Furthermore, the highly symmetric circular gate and cone geometry reduces the chance that an electron leaving the emitter goes to the gate instead of the anode.

### 3.3.4 Low angular spread, current stability and one-pixel display prototype

By placing a high voltage phosphor screen directly above the FEAs we were able to observe an illuminated spot on the screen. Figure 3-34 shows the digital picture of such a "single pixel field emission display". At a gate voltage of 50 V, an anode voltage of 5000 V and a screen-substrate distance of 1 cm, a  $60 \times 60$   $4\mu\text{m}$  pitch field emitter array generates a spot with the size of about 2 mm in diameter. The calculated half angle of the angular spread of the emitted electron beam ( $\theta/2$ ) is about 12.6 degrees, which is very low. The low angular spread of the electron beam might relax the requirement of an integrated focusing electrode, whose function is to expel the emitted spreading electron beams and keep them focused [91].

## 3.4 Discussions of results

Silicon field emitter arrays with a gate aperture of around  $1\mu\text{m}$  and a small tip radius are successfully fabricated by using two Integrated Circuit (IC) fabrication technologies: oxidation sharpening and chemical mechanical polishing. The characterization of these devices were performed in an UHV environment, without pre-testing treatment such as field forming or bake out. At relatively low voltage, the field emission data agree with Fowler-Nordheim theory very well. The devices also demonstrated

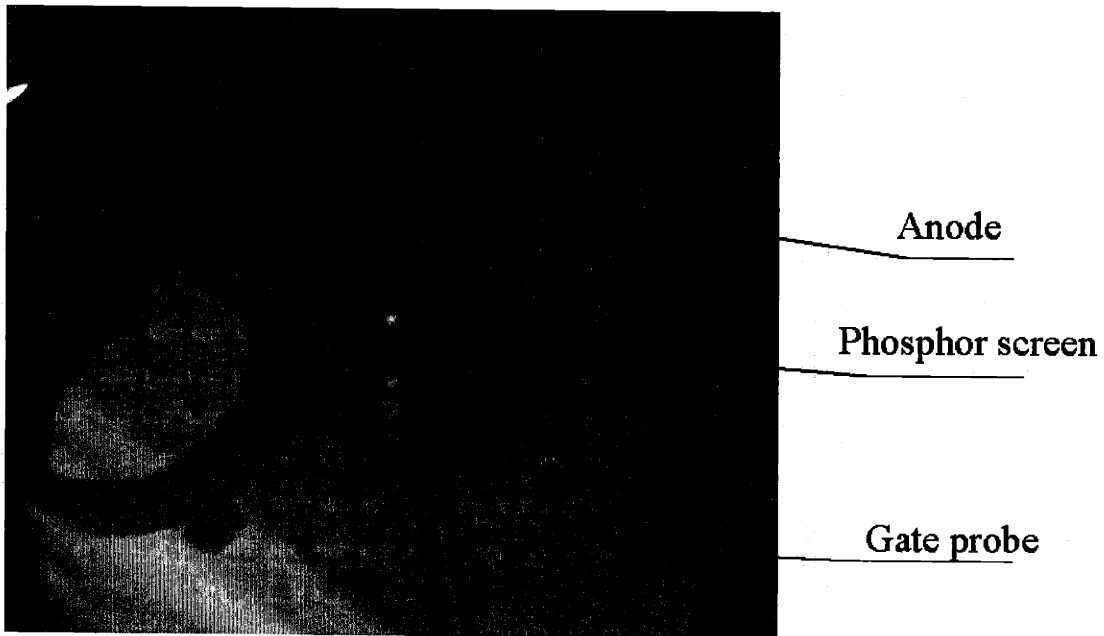


Figure 3-34: “Single pixel field emission display”. The image is taken after 20 days of stable operation of the  $60 \times 60$  emitter array.  $V_g = 50V$ ,  $V_a = 5000V$  with screen-substrate distance of  $1cm$ . The diameter of the illuminated spot is about  $2nm$ . The calculated half angle of the angular spread of the emitted electron beam ( $\theta/2$ ) is about 12.6 degrees. From the figure one can observe that anode is a slab of Pt coated silicon wafer fixed on a metal clamp and is held in place by one of the XYZ manipulators shown in figure 3-16.

low turn-on voltage, high current density, high transconductance, negligible gate leakage current, and are very uniform. A tip radius of about  $1nm$  was achieved. These properties are very important factors for enhancing the performance, increase the reliability, and prolonging the lifetime of field emission based devices.

**Turn-on voltage** Turn-on voltages between  $20V$  to  $30V$  were routinely observed. One field emitter arrays with gate aperture of  $0.8\mu m$  exhibited an extraordinarily low turn-on voltage of  $14V$ . It is even comparable to the devices that are observed with much smaller gate apertures [89, 120]. David Pflug [89] fabricated  $70nm$  gate aperture silicon field emitter arrays that turn on at  $8.5V$ . Hunt et al. [120] fabricated gold gate silicon field emitter arrays with  $400$  to  $500nm$  gate apertures and the devices turned on around  $12V$ . Koga et al. fabricated silicon emitter arrays with gate aperture of  $0.6\mu m$  using oxidation sharpening and lift-off techniques. Their devices turned on at  $8V$  [104]. David Pflug also fabricated gated molybdenum field emitter arrays with gate apertures of about  $100nm$  that turned on at about  $12V$  [89, 98]. Hisahi et al. fabricated silicon emitter arrays with  $90nm$  gate aperture, which turned on at  $17V$  [102]. Hunt et al. [20] also fabricated silicon field emitter arrays with  $20\mu m$  pitch size using an n-type substrate of dopant concentration of  $10^{16}cm^{-3}$ , which is the same as the dopant concentration of our field emitters. They achieved a tip radius of about  $1nm$  [77] by low temperature oxidation sharpening. The device turned on around  $5V$ . However, their device had a diode structure, not a triode structure. There was no extraction gate around the emitter tip. An anode plate was placed directly above the emitter tips and the cathode-anode distance is  $920nm$ . Adler et al. [66] fabricated gated arrays of polycrystalline silicon tips with a  $10\mu m$  pitch size. The dimensions of the device are comparable to our devices and they turned on between  $20V$  to  $30V$ . But their polycrystalline silicon tips were coated with molybdenum. Lee et al. [122] fabricated gated silicon field emitter arrays on an n-type silicon substrate using a "lift-off" technique. The gate aperture was  $1.6\mu m$ , the height of the tip is about  $1\mu m$ . The device was baked out at  $250^{\circ}C$  for 10 hours and it turned on at  $38V$ .

Table 3.3: Comparison of turn-on voltages of different groups.

Group	Tip material	Structure	Aperture	$V_{turn-on}$
Author	Si	3-terminal	$0.8 - 1.0\mu m$	14V
Pflug et al.	Si	3-terminal	70nm	8.5V
Hisahi et al.	Si	3-terminal	90nm	17V
Pflug et al.	Molybdenum	3-terminal	100nm	12V
Hunt et al.	Si	3-terminal	$0.4 - 0.5\mu m$	12V
Kogal et al.	Si	3-terminal	$0.6\mu m$	8V
Hunt et al.	Si	2-terminal	no aperture	5V
Adler et al.	Poly-Si with Mo coating	3-terminal	$1\mu m$	20 - 30V
Hyung et al.	Si	3-terminal	$1.6\mu m$	38V

Table 3.3 summarizes the comparison above. The turn-on voltages of our devices are much smaller than those of metal emitter arrays with similar dimensions, which typically have turn-on voltages of about 50 to 60V before treatment like field forming [18]. Field forming is a process often used to sharpen the metal emitter tips [79], thus enhancing the performance of field emission. The enhancement is achieved by heating the cathode while the tips are under high electric field stress. The tip is reformed and sharpened in this way, resulting in an increased local electric field on the tip surface for a given applied voltage. The field increase can lower the turn-on voltage and cause a shift of the voltage-current characteristic. Spindt et al. compared the emission results before and after field forming and found that the emission current with 35V applied to the tips has been increased five to six orders of magnitude by the forming process [19, 80].

**Current density** Current density is a very important device performance parameter. The current density is directly related to the packing density of the tips in the emitter array, and the transconductance is proportional to the total number of tips in the array. Thus emitter-tip packing density is also an important consideration for many applications. For our  $3\mu m$  pitch arrays, the tip density is about  $1.15 \times 10^7/cm^2$ . From figure 3-32 it is observed that at a gate voltage of about 90V, the  $60 \times 60$  arrays

have a current of about  $1mA$ , or  $0.27\mu A$  per tip. This emission current corresponds to a nominal areal current density of  $1.8A/cm^2$ . David Pflug [89] 's  $70nm$  gate aperture silicon field emitter arrays achieved an areal current density of about  $10mA/cm^2$  at a gate voltage of  $13V$ . For Hyung et al.'s device mentioned above [122], an anode current of  $0.1\mu A$  per tip is observed at gate voltage of  $80V$ , close to the value observed in our device. Gray, Shaw, and Temple et al. fabricated "tip on post" silicon field emitter structures with tip height of about  $4\mu m$  and gate aperture of about  $3.5 - 4\mu m$ , for the purpose of microwave amplifier applications [105]. At a gate bias of about  $120V$  emission current of about  $2\mu A$  per tip was achieved, which was in the acceptable range for RF amplification in the GHz frequency range [105]. Spindt et al. [19] fabricated  $1\mu m$  gate aperture,  $0.75\mu m$  tip height metal field emitters using molybdenum. By using directional reactive ion etching (RIE) instead of the isotropic wet etching in the molybdenum process, a packing density of  $1.6 \times 10^7 tips/cm^2$  is achieved (compared to the packing density of  $6.4 \times 10^5/cm^2$  if using wet etching). This packing density is of the same order of magnitude as the arrays we fabricated. The molybdenum tip underwent a  $450^\circ C$  bake out for outgassing before testing. At a voltage of  $130V$ , the average tip loading could be about  $40\mu A$  per tip. A peak emission level of areal current density of  $1000A/cm^2$  is achieved at  $212V$ . This huge areal current density is due to the almost unlimited supply of electrons in a metal. In silicon field emitters, due to the limited electron concentration ( $10^{16}cm^{-3}$  in our device), current saturation occurs at intermediate voltages. Current saturation will be discussed in detail in chapter 5.

**Leakage current** Low gate leakage current is an important property reflecting the efficiency of the device and is also very important in enhancing the lifetime of the emitter arrays. In our devices, the gate leakage current is extremely small, about 0.01% to 0.1% of the total emission current. This is comparable with the literature. Spindt et al. [19] reported that gate leakage current was about 0.008% of the total emission current in their  $1\mu m$  gate aperture,  $0.75\mu m$  tip height molybdenum emitter.

In Adler et al.'s device mentioned above [66], the gate leakage current was about 1 to 5% of the total emission current. In Hyung et al.'s device [122] mentioned above, the gate leakage current was about 0.3% of the anode current.

For a good review of field emitter array development please refer to Dorata Temple's article (reference [16]).

### **New materials for field emission applications**

New materials are always being explored for field emission applications. Spindt [19] experimented with titanium carbide ( $TiC$ ) for field emitter materials and found that its performance was as good as molybdenum tips before field forming, but was not as good as molybdenum after the field forming. Kang et al. reported a sub-V turn-on voltage of about 0.7V for gated diamond emitters fabricated using a self-aligned-gate-molding technique [107].

Recently, a lot of attention have been paid to Carbon Nanotubes (CNT): a whole new class of materials that could be of great importance for a lot of application fields, including field emission devices [108]. A carbon nanotube is a tubular form of carbon with a diameter ranging from 0.3 to 1nm. The length can be from a few nanometers to several microns. A carbon nanotube is a good field emission electron source. Large emission current density from  $10mA/cm^2$  to  $4A/cm^2$  have been reported [109, 113]. The emission has shown structure pattern (like the "ring" pattern) on phosphor anode screens. It is believed that the nanotube tips are responsible for the field emission [112]. Experimental results showed that the turn-on electric field need for CNT fielded emission is about  $1.7 \times 10^4 V/cm$  [109, 110]. It is worth noting that these turn-on fields were the average field for the parallel plate capacitor typically seen in the two-terminal diode CNT field emission structures. They were not the local fields on the the cap of the carbon nanotubes. Gröning et al, measured a work function of about 5.3eV for carbon nanotubes using an energy resolved field emission method [110, 111]. This

result means that the local surface electric field required for field emission from CNT is still in the order of  $10^7 V/cm$ . The observed nominal low turn-on field is believed to be caused by the field enhancement effect due to the very small radius of curvature of the nanotube cap [110]. Up to the present, most field emission work in CNTs are done in a diode setup. Instead of using an integrated gate, an anode is placed directly above the CNT for electron extraction. The operating voltages are still in the range of hundreds to thousands of volts [109, 113]. It is still a technological challenge for researchers to bring an integrated gate to CNT field emitters.

### 3.4.1 Summary

Figure 3-19 showed that beyond 80V the Fowler-Nordheim plot starts to level off, indicating that the emission current starts to saturate. These results suggested three regions of operation: cut-off, electron transmission controlled, and electron supply controlled regions. In the cut-off region, the device has not been turned on yet. In the electron transmission controlled region, the experimental data agree well with Fowler-Nordheim theory. In the electron supply controlled region, current saturation starts to occur. We will discuss the current saturation and the behavior of field emission beyond current saturation in detail in chapter 5.



## Chapter 4

# High aspect ratio silicon field emitter arrays and the breakdown mechanism of field emitter arrays

Our main purpose of fabricating high aspect ratio field emitters is to increase the maximum current density. This goal can be achieved by increasing maximum voltage of operation and increase the breakdown voltage. Tall and high aspect ratio emitter implies that thick gate dielectric ( $SiO_2$ ) will be needed. It is expected to increase the breakdown threshold voltage of  $SiO_2$  so that we can test the device in higher voltages, and thereby enable further exploration of the performance and physics of the silicon field emitter arrays. Specifically, it is expected to make it easier to observe valence band field emission if the field emitter arrays can sustain higher gate voltages (refer to chapter 5).

On the other hand, high aspect ratio field emitter arrays have a lot of other applications. It is the basis of the integration of vertical transistors with field emitters [90]. It is also the basis for field emitter arrays with focusing electrodes [91]. When built along with a cantilever they can be used as probing tips for Scanning Tunneling

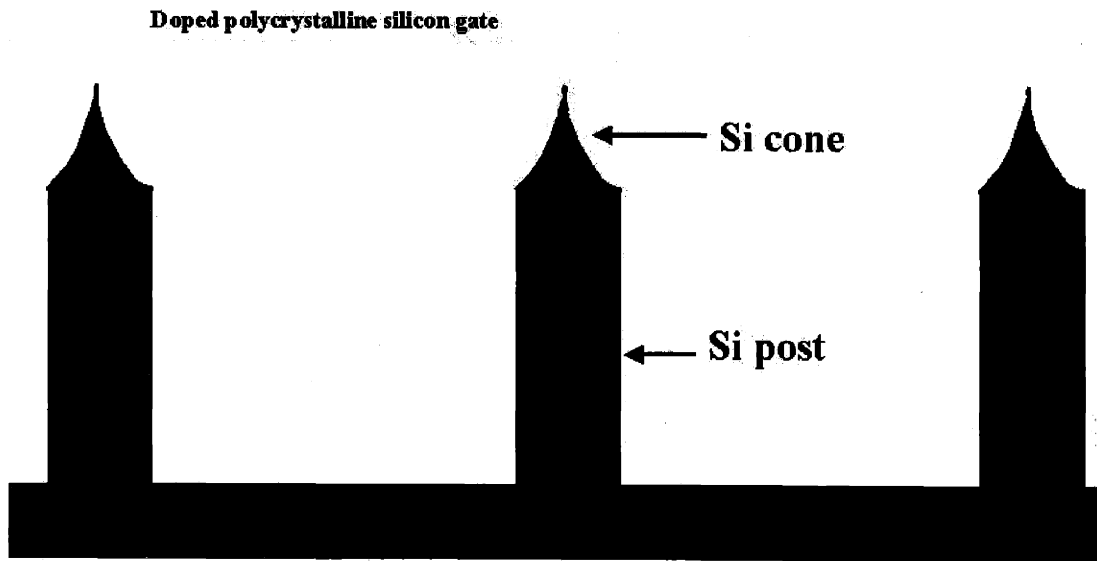


Figure 4-1: Schematic of the cross section of the final structure of the device. In the device area, the polycrystalline gate is actually “dangling” because the oxide in the device area has all been etched away. The gate is supported by the oxide sandwiched between the polycrystalline silicon and the substrate in the outer gate electrode area.

Microscope (STM) and Atomic Force Microscope (AFM) applications. The idea has also been proposed as the writing head of atomic scale information storage devices [145].

So, for the above reasons, the high aspect ratio silicon field emitter arrays are fabricated and tested in our lab.

## 4.1 Fabrication of high aspect ratio silicon field emitter arrays

The final device structure we want to achieve is depicted schematically in figure 4-1.

The first few steps of the fabrication of high aspect ratio emitters are the same as described in section 3.1 up to the isotropic etching of silicon substrate using an  $SiO_2$

hard mask, as shown in figure 3-3.

Figure 4-2 describes the formation of a tall silicon pillar with a silicon cone tip similar to the devices described in previous chapter. After the isotropic etching, a thin layer of  $SiO_2$  is grown by another dry oxidation step. This thin layer of oxide on the substrate is etched away using directional plasma etching [69]. The thick  $SiO_2$  cap serves as a self-aligning mask, so that the thin oxide layer at the surface of the silicon cone underneath the cap is not etched away. Figure 4-2 (a) is a schematic drawing of the cone at the end of this "oxide masking" process. After this step, reactive ion etching of silicon was performed as shown in figure 4-2 (b), resulting structure shown in figure 4-2 (c). A pillar of silicon with a silicon cone on top of it is formed. Figure 4-2 (d) is an SEM picture of this structure.

Afterwards, the oxide cap was stripped in BOE (Buffered Oxide Echant), as well as the thick oxide layer on the surface of the cone. Then the whole structure went through another dry oxidation sharpening step. This time the purpose was to sharpen the tip as shown in figure 4-3.

Figure 4-4 demonstrated the pillar and the sharpened silicon tip. In the case shown in the SEM picture, the pillar is about  $5\mu m$  tall and has a  $0.5\mu m$  base diameter with a tip to tip pitch size of  $4\mu m$ . The aspect ratio of this emitter is about 10 : 1.

In the next step, a thick layer of  $SiO_2$  was deposited in a PECVD (Plasma Enhanced Chemical Vapor Deposition) system [73]. The thickness of the deposited oxide was chosen to exceed the height of the emitter. The oxide was densified in  $N_2$  at  $1000^\circ C$  for 30 minutes. The densification process shrank the thickness of the oxide by about 2% – 5%. Figure 4-5 is a schematic of the structure after the oxide deposition. Figure 4-6 shows SEM pictures of the actual device after the PECVD oxide deposition. There are huge oxide domes formed after this step, due to the conformal nature of the chemical vapor deposition process and the tall emitter tips.

Then the structure was planarized to achieve a flat surface using CMP. Figure 4-7 is

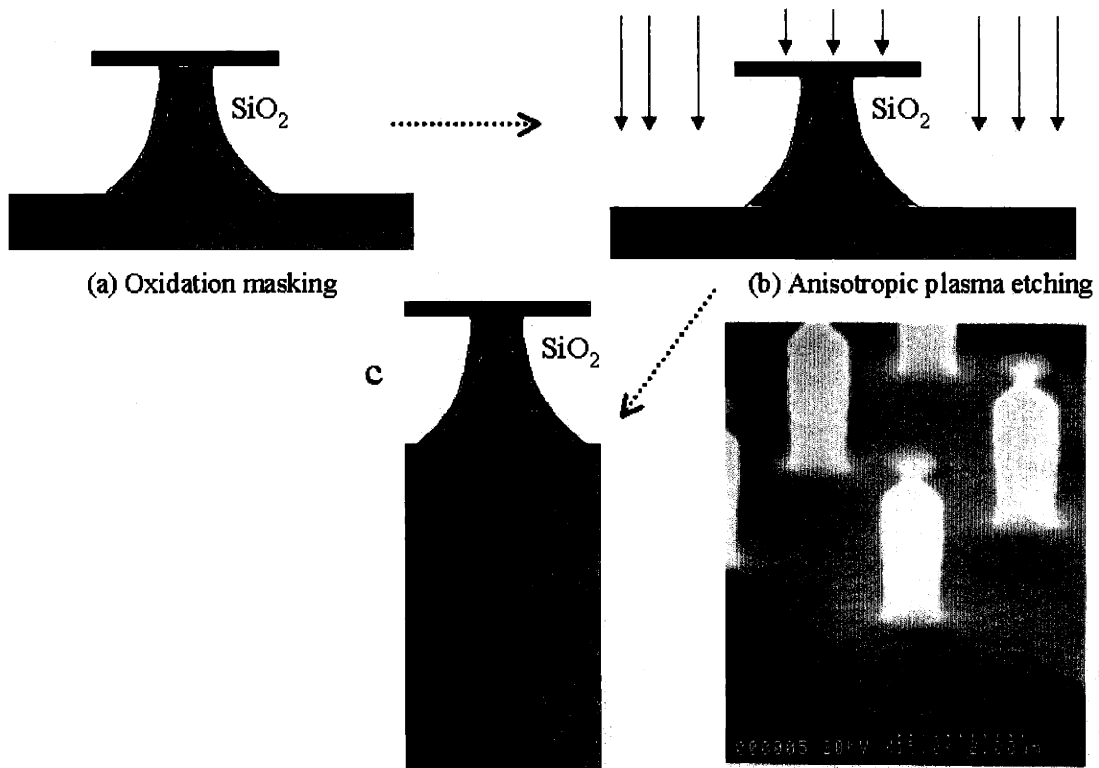


Figure 4-2: Formation of silicon pillar with silicon cone on top of it. (a) “oxidation masking” process; (b) directional plasma etching of silicon substrate using the oxide cap as the hard mask; (c) the resulting pillar structure; (d) an SEM picture of the resulting pillar structure. We notice that the plasma etching of silicon has significantly etched away the oxide cap.

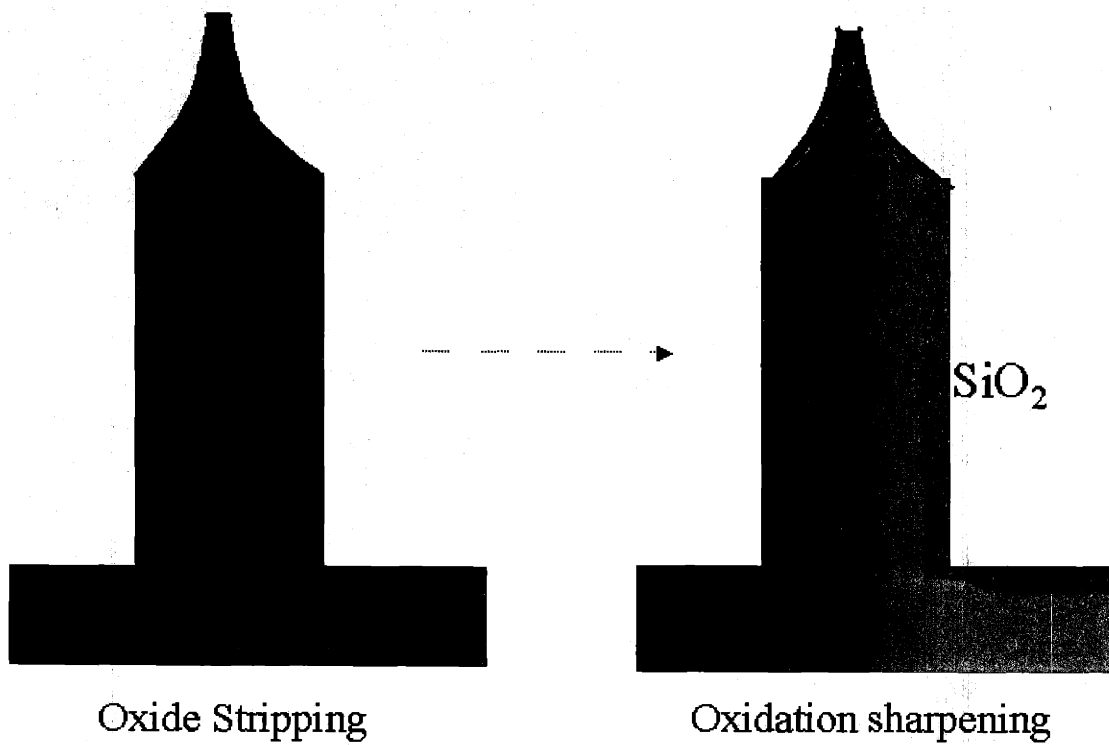


Figure 4-3: The oxide cap as well as the thin oxide layer on the surface of the cone were stripped in hydrofluoric acid solution. The whole structure went through a dry oxidation sharpening process. This time the purpose of the oxidation is to sharpen the tip.

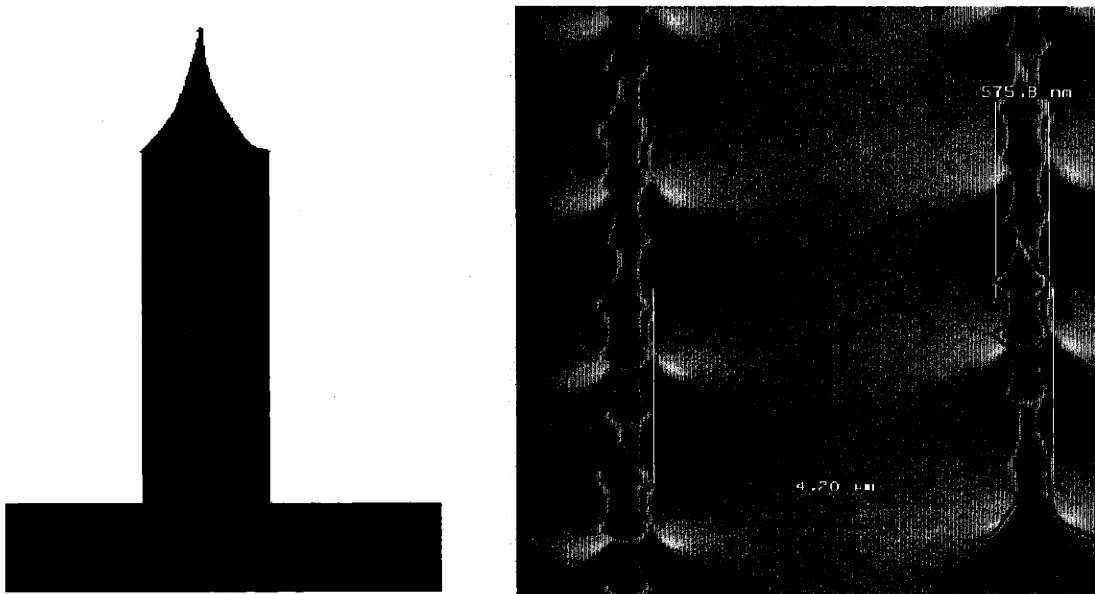


Figure 4-4: The figure on the left is a schematic of a sharpened silicon tip. The figure on the right is the SEM of a real emitter. The pillar is about  $5\mu m$  tall and the base diameter is about  $0.5\mu m$ . The tip to tip pitch size is  $4\mu m$ . The aspect ratio of this emitter is about 10 : 1. The scalloping of the edge wall of the emitter was caused by intermittent etching and passivation of the silicon. It is a machine-specific result.

a schematic after the CMP and Figure 4-8 is a SEM picture of the wafer surface after the CMP process.

The next step is a very critical step in the fabrication. The wafer is time etched in BOE to etch back the oxide so as to expose the silicon cone. The height of the exposed portion should be around  $700nm$ , thus making the surface of the wafer look similar to figure 3-5. Due to the fact that BOE has a high etch rate (about  $1000\text{\AA}/\text{min}$ ) for thermal oxide and it has an even faster etch rate for CVD deposited oxide (about  $2000\text{\AA}/\text{min}$ ), very careful timed etching is required to perform this step successfully. Before the etch, the thickness of the oxide is precisely determined. Furthermore, the etch rate of the BOE solution needs to be characterized on control wafers with thick CVD oxide, deposited and densified under the same conditions of the device wafer. Figure 4-9 shows the structure after the timed etch process. The left schematic shows the cross-section and the right SEM picture shows the surface of the device wafer after the etch.

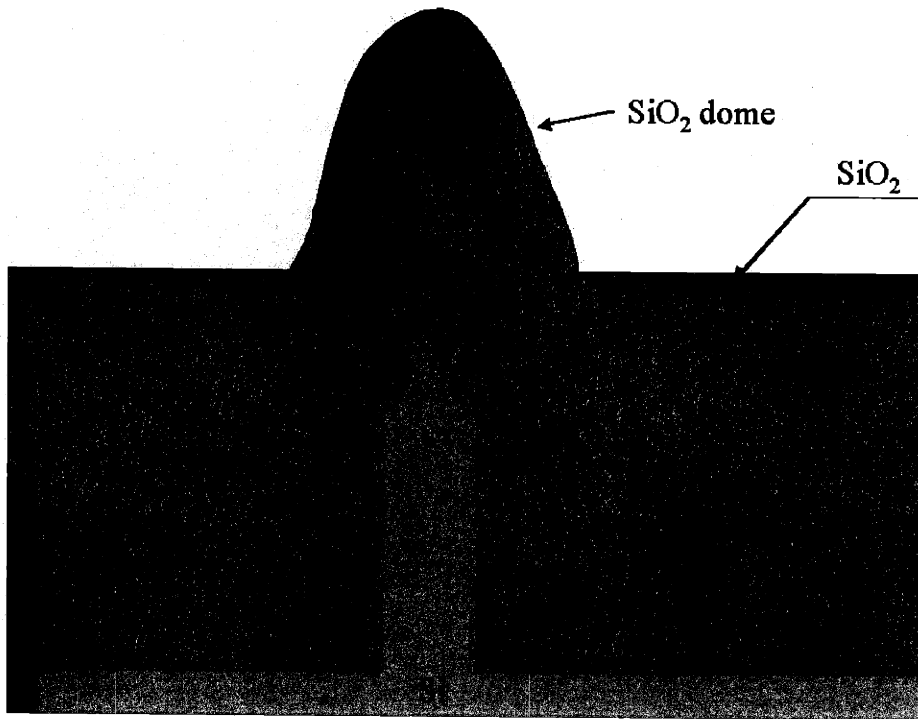


Figure 4-5: The deposition (PECVD) of oxide, the dielectric. There are huge domes formed after this step, due to the conformal nature of the chemical vapor deposition process and the tallness of the emitter tip.

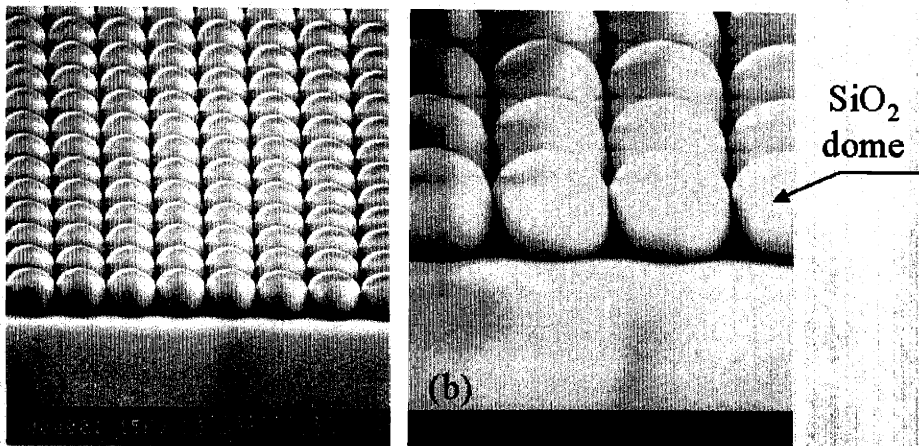


Figure 4-6: SEM pictures of the device after the conformal PECVD deposition process. These two pictures were taken from a  $60^\circ C$  tilted view.

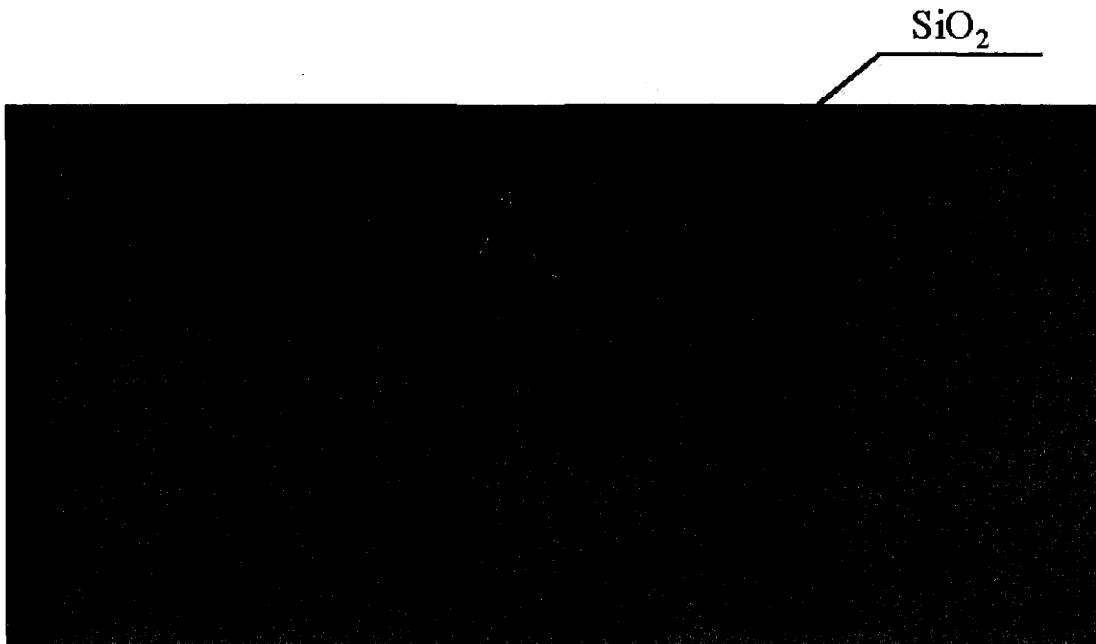


Figure 4-7: Schematic of the device cross-section after the CMP. The purpose of this step is to remove the *SiO*<sub>2</sub> domes.

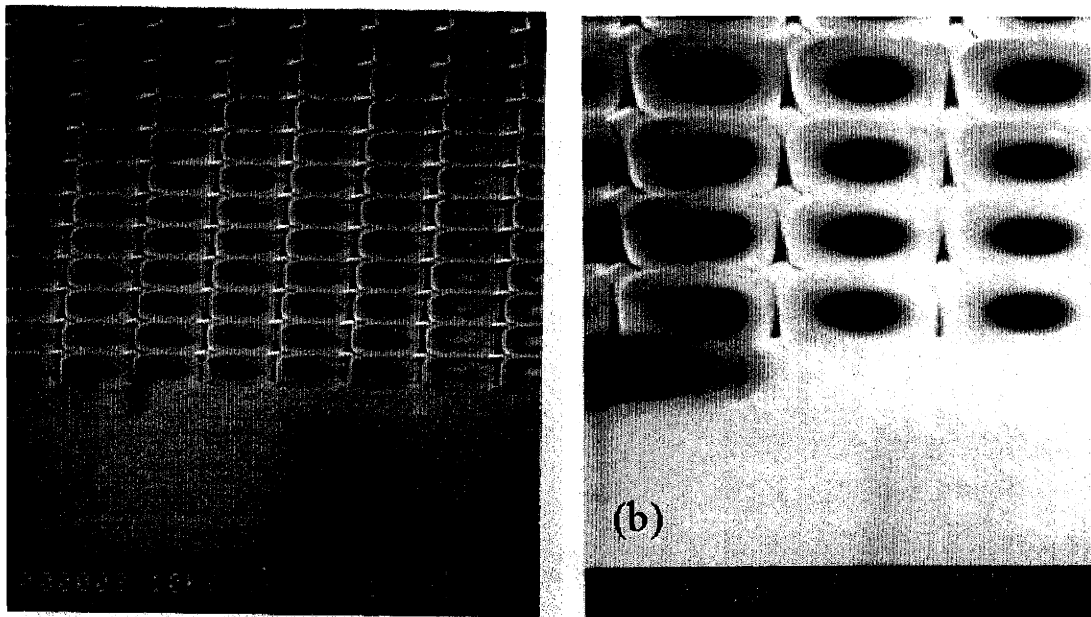


Figure 4-8: SEM pictures of the device surface after the CMP. These two pictures were taken from a 60° tilted view.



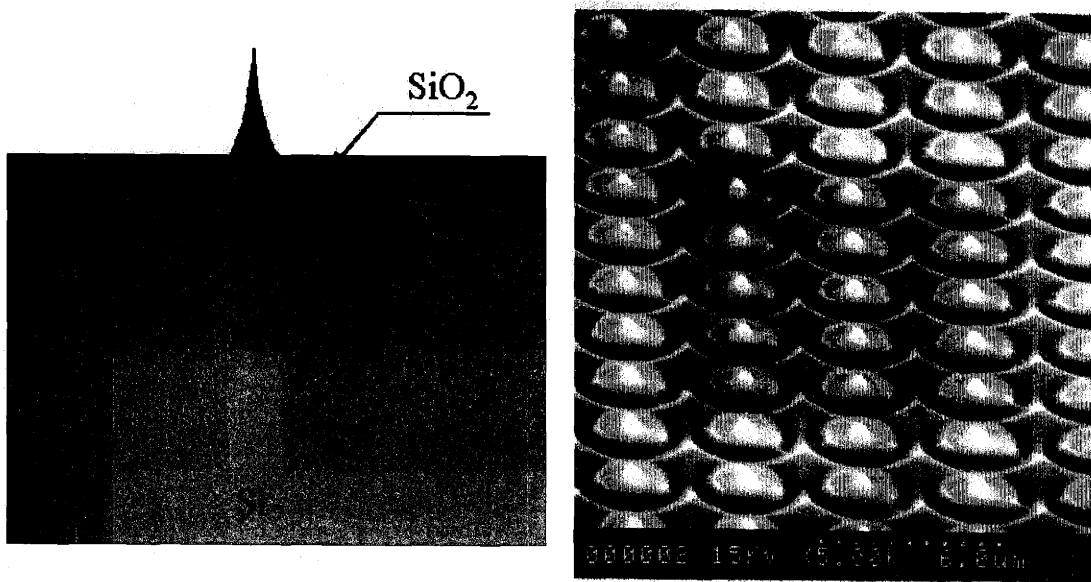


Figure 4-9: The timed etch-back of the oxide. The left schematic shows the cross-section and the right SEM picture shows the surface of the device wafer after the etch. The exposed portion of the tip is around  $700nm$ .

What follows is the second PECVD deposition of the oxide. This time the deposited thickness is about  $700nm$ , to cover the height of the exposed emitter tip. Again the deposited oxide is densified in  $N_2$  at  $1000^\circ C$  for 30 minutes. Figure 4-10 shows the schematic of the cross section after this step. The size of the domes is reduced compared to the domes in figure 4-6. Figure 4-11 are SEM pictures of the device surface. The SEM on the left is a plane view and the SEM on the right is a tilted view.

After the oxide deposition the next step was the deposition of the gate electrode material: polycrystalline silicon. A layer of about  $3000\text{\AA}$  polycrystalline silicon was deposited on top of the CVD oxide layer. The layer was subsequently doped with phosphorus to increase its conductivity. The doping is achieved by high temperature ( $925^\circ C$ ) diffusion [74]. Figure 4-12 shows the schematic of the cross section of the device after the polycrystalline silicon was deposited. Figure 4-13 are SEM pictures of the surface of the device after the deposition. The left one is a tilted view and the right one is a top-down view. The rough grains of the polycrystalline silicon are

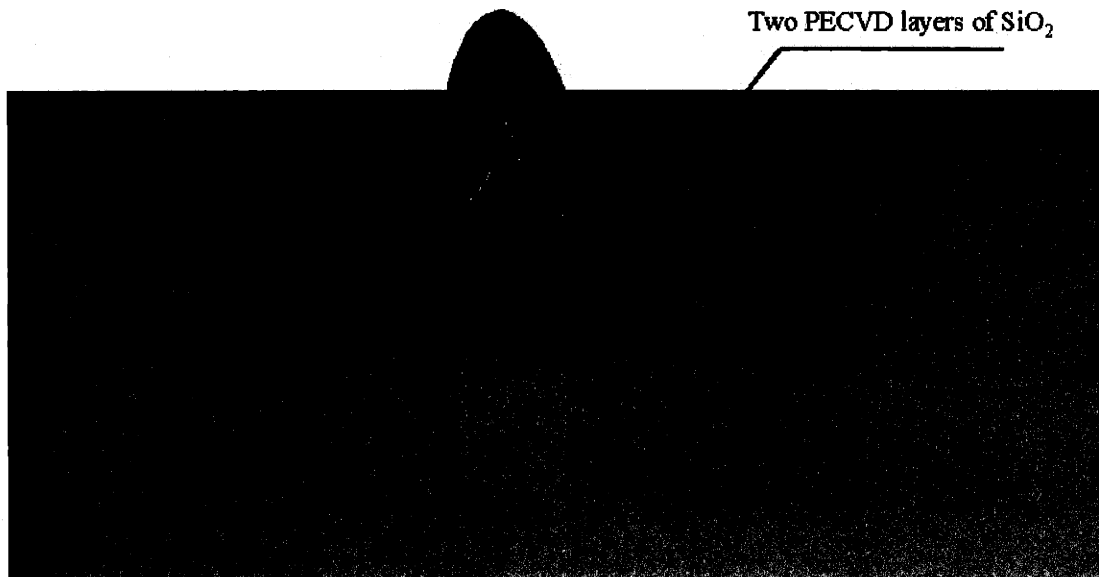


Figure 4-10: Schematic of the cross section of the device after the second PECVD oxide deposition and densification. The surface bump is much smaller this time.

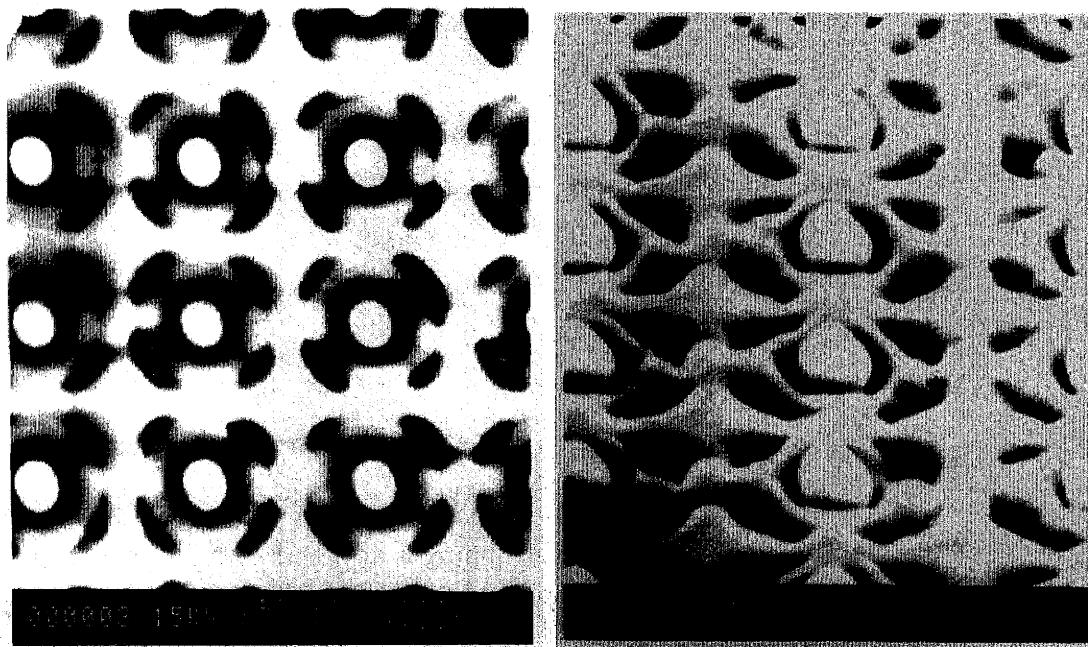


Figure 4-11: SEM pictures of the device surface after the second PECVD oxide deposition and densification. The left SEM is a top-down view and the right SEM is a tilted view.

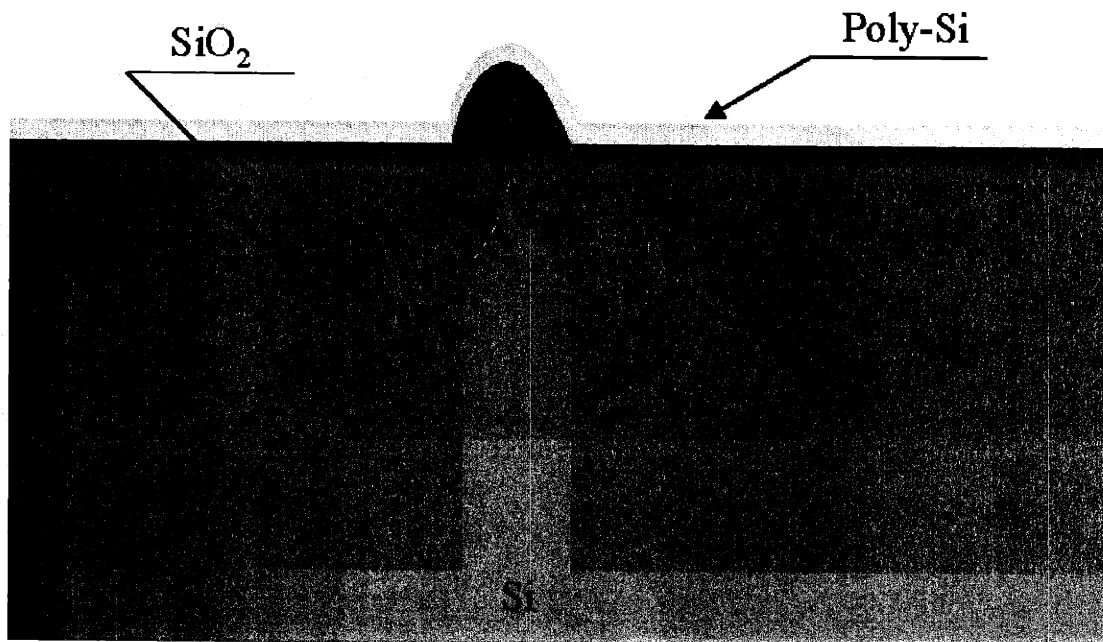


Figure 4-12: Schematic of the cross section of the device after the polycrystalline silicon is deposited.

easily observed.

Then the wafer underwent the second chemical mechanical polishing. This time the purpose was to remove the bumps and to open the gate aperture. The CMP machine polishes polycrystalline silicon very fast even when there are no bumps present on the surface. So, the planar portion of the wafer should not serve as the polishing stopping layer, as it might be the case for the oxide polishing. A very careful timed polishing is needed in order not to over polish the wafer and subsequently damage the emitter tip. Figure 4-14 shows a schematic of the cross section of the device after the second chemical mechanical polishing. Figure 4-15 are SEM pictures of the surface of the polished wafer, revealing the gate aperture.

After the gate aperture is revealed, the gate was patterned to form the gate electrode. The surface of the wafer after this step will be similar to figure 3-13. After the gate patterning, the device is immersed in hydrofluoric acid solution for a long time to etch away all the oxide around the pillar emitter and expose the silicon tip. A  $3\mu\text{m}$

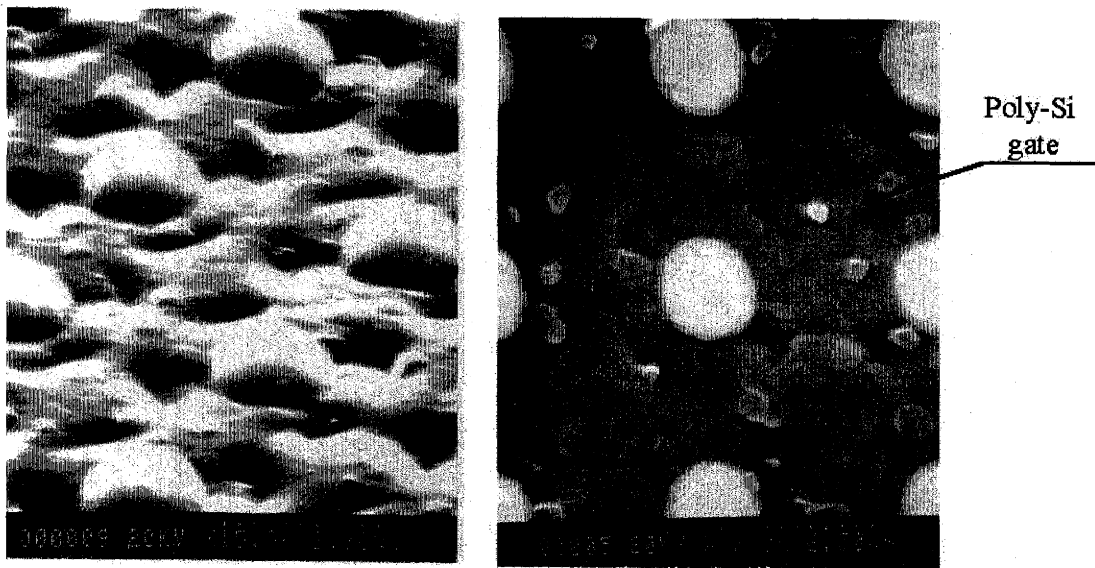


Figure 4-13: SEM pictures of the surface of the device after the polycrystalline silicon deposition. The left SEM is a tilted view and the right SEM is a top-down view. One can easily see the rough grains of the polycrystalline silicon.

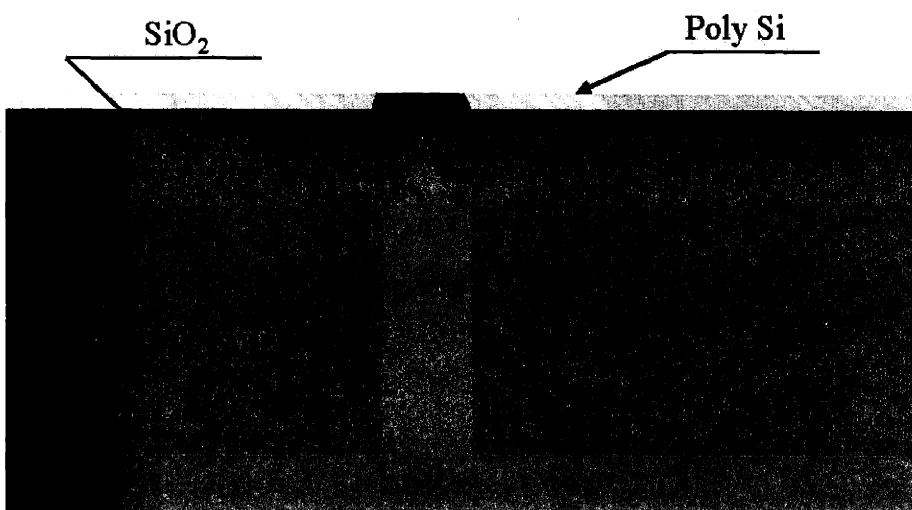


Figure 4-14: Schematic of the cross section of the device after the second chemical mechanical polishing.

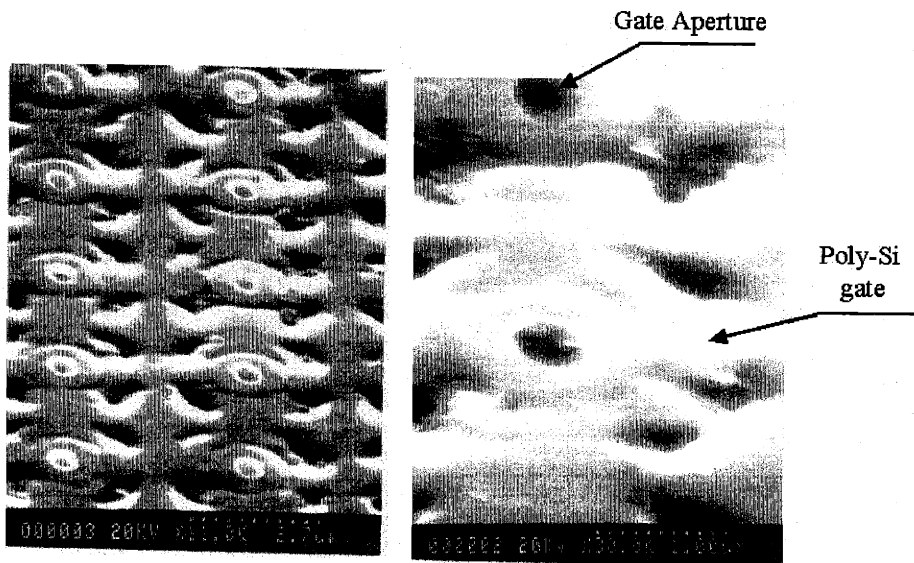


Figure 4-15: SEM pictures of the surface of the polished wafer. One can see that the gate aperture is revealed. The SEM on the right is a larger magnification (30K) picture compared to the SEM on the left (11K).

tall emitter needs about 30 minutes to etch away all the oxide. Figure 4-16 shows the SEMs of the wafer surface after the gate patterning and the oxide etch. The SEM on the left shows the tip within the gate aperture. The diameter of the gate aperture is about  $0.8\mu m$  to  $1\mu m$ . The lower magnification SEM on the right shows the edge of the polycrystalline gate electrode and the device area (far side). A severe undercut of oxide is observed due to the extended period of time of oxide etching in hydrofluoric acid solution. Figure 4-1 shows the schematic cross section of the device. In the device area the polycrystalline gate is actually “dangling” because the oxide in the device area has all been etched away. The gate is still supported by the oxide sandwiched between the polycrystalline silicon and the substrate in the outer gate electrode area.

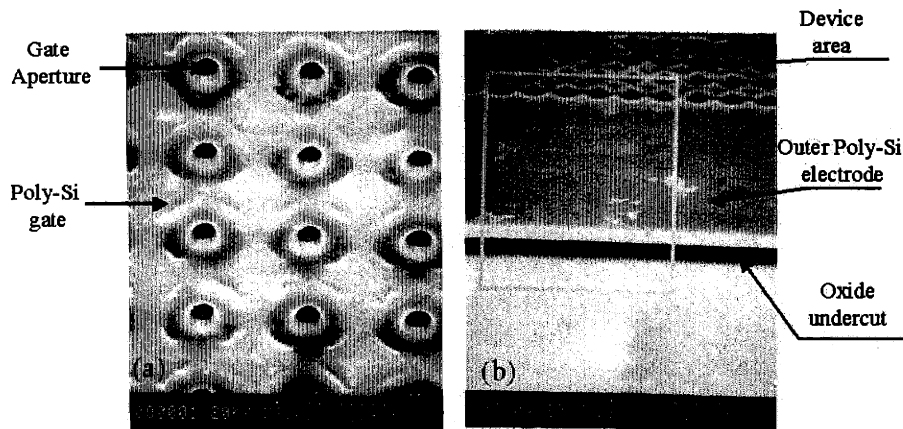


Figure 4-16: SEM pictures of the wafer surface after the gate patterning and the oxide etch. The gate aperture is about  $0.8\mu m$  to  $1\mu m$ .

## 4.2 Characterization of high aspect ratio field emitter arrays

The device characterized has a pillar emitter height of  $2.3\mu m$ .

### 4.2.1 Agreement with Fowler-Nordheim formula

Figure 4-17 and figure 4-18 are the I-V curve and the corresponding Fowler-Nordheim plot of a  $4\mu m$  pitch  $10 \times 10$  field emitter array. The data follow the Fowler-Nordheim equation well. It appears that the slope of Fowler-Nordheim plot of the gate current and the slope of the Fowler-Nordheim plot of the anode current are the same. This observation, together with the observation in figure 4-17 that the gate leakage current is significant compared to anode and emitter current (in this case the gate current is even larger than the anode current), suggests that the gate leakage current comes mainly from the emission current. Although there are several steps in the process that need optimization, the acquired data showed that the current fabrication flow is a first pass success.

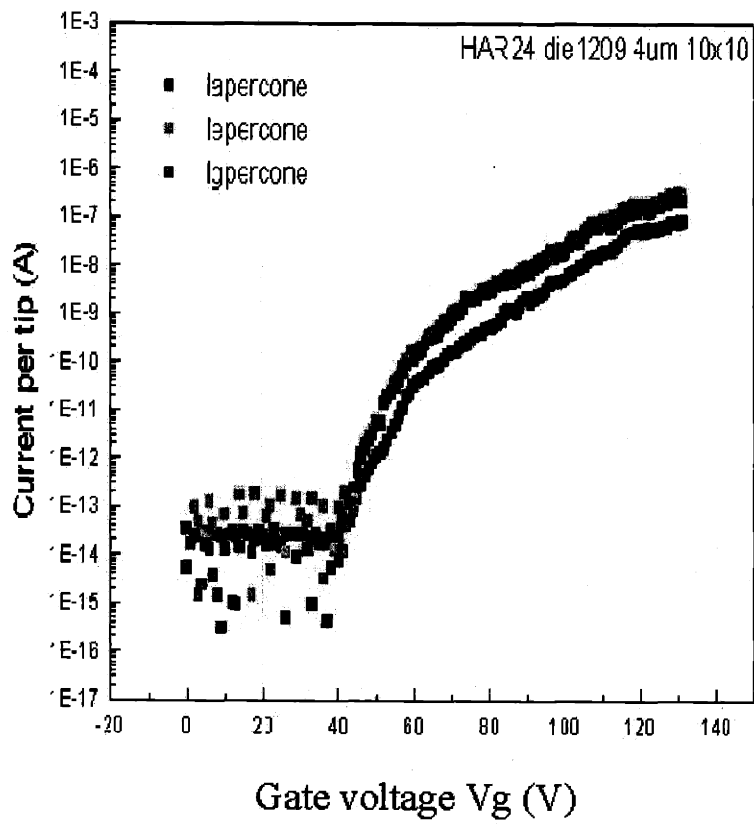


Figure 4-17: I-V characteristics of a high aspect ratio  $4\mu m$  pitch  $10 \times 10$  field emitter array. Anode current  $I_a$ , gate current  $I_g$ , and emitter current  $I_e$  are plotted together vs.  $V_g$ .

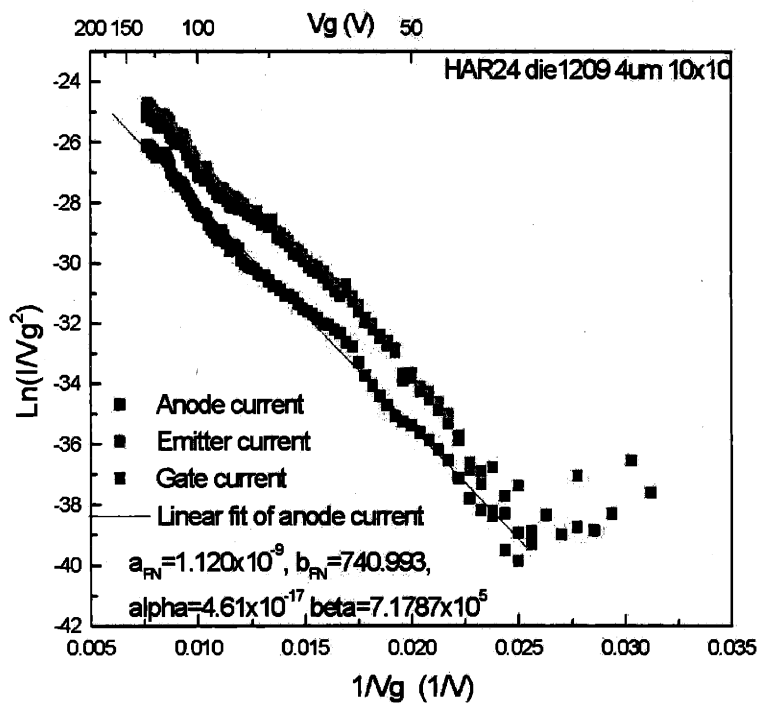


Figure 4-18: Fowler-Nordheim plots corresponding to the same data as in figure 4-17. The data agree with the Fowler-Nordheim formula well.



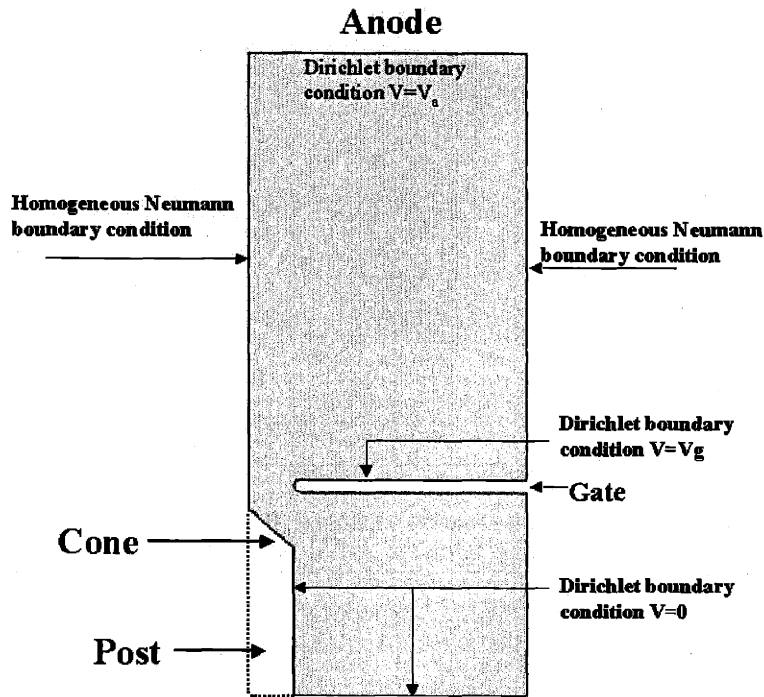


Figure 4-19: Problem space with boundary conditions for the high aspect ratio field emitter.

The field factor is calculated to be  $\beta = 7.18 \times 10^5 \text{cm}^{-1}$ . A tip radius of  $r = 13.9 \text{nm}$  is obtained by applying the “ball in sphere” model.

The high aspect ratio device was also numerically simulated using the method described in section 3.3.1. Figure 4-19 shows the layout of the problem space and the boundary conditions.

Based on the dimensions of the device, a dependence of the field factor  $\beta$  on tip radius  $r$  was derived to be:

$$\beta = \frac{10.93 \times 10^5}{r^{0.56729}} V/\text{cm} \quad (4.1)$$

where  $r$  has units of  $\text{nm}$ . Figure 4-20 compares this dependence with the “ball in sphere” model’s  $1/r$  dependence.

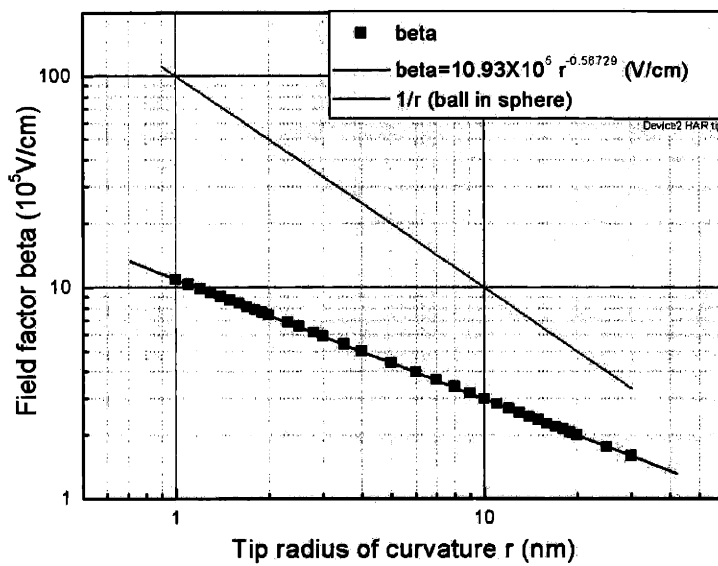


Figure 4-20: Dependence of field factor  $\beta$  on the tip radius  $r$  for the device structure shown in figure 4-1. The blue line is the “ball in sphere” model’s  $1/r$  dependence. In the calculation, the following parameters are used: tip height= $460nm$ , pillar height= $1840nm$ , oxide thickness= $2534nm$ , gate thickness= $150nm$ , and gate aperture= $1000nm$ .

Table 4.1: Summary of physical parameters of the field emitter array shown in figure 4-17 and 4-18 (HAR\_die1209\_4 $\mu$ m\_10  $\times$  10)

$a_{FN}$	$b_{FN}$	$\alpha$	$\beta$	$r_{ballinsphere}$	$r_{2D}$
$1.12 \times 10^{-9}$	740.993	$4.61 \times 10^{-17} cm^2$	$7.18 \times 10^5 cm^{-1}$	13.9nm	2.10nm

Comparing equation 4.1 with equation 3.4 and equation 3.6, it is found that the power dependence of  $\beta$  on  $r$  for high aspect ratio field emitters is significantly different from that of the regular field emitters. The field factor is suppressed for the high aspect ratio emitters compared to the ordinary emitters with the same tip radius and gate apertures. A qualitative argument for this suppression would be that some electric flux lines terminate on the pillar instead of the tip, resulting in a reduced field enhancement.

Based on equation 4.1, the experimentally observed  $\beta = 7.18 \times 10^5 cm^{-1}$  corresponds to a tip radius of  $r = 2.10nm$ .

Table 4.1 summarize the results for this particular device.

#### 4.2.2 Current uniformity and comparison with ordinary emitter structures

Figure 4-21 shows anode currents as a function of the gate voltage for four 4 $\mu$ m pitch field emission arrays with different sizes within a certain die. The data are for four field emitter arrays: 10  $\times$  10, 20  $\times$  20, 30  $\times$  30, and 60  $\times$  60. The turn-on voltages for the four devices ranged from 28 to 40 volts.

Figure 4-22 shows the normalized anode currents per emitter for devices from the same die as in figure 4-21. The normalized currents per tip for the four different size emitter arrays overlap to some extent, with each other, indicating a certain degree of emission uniformity. However, the uniformity is not as good as the one demonstrated

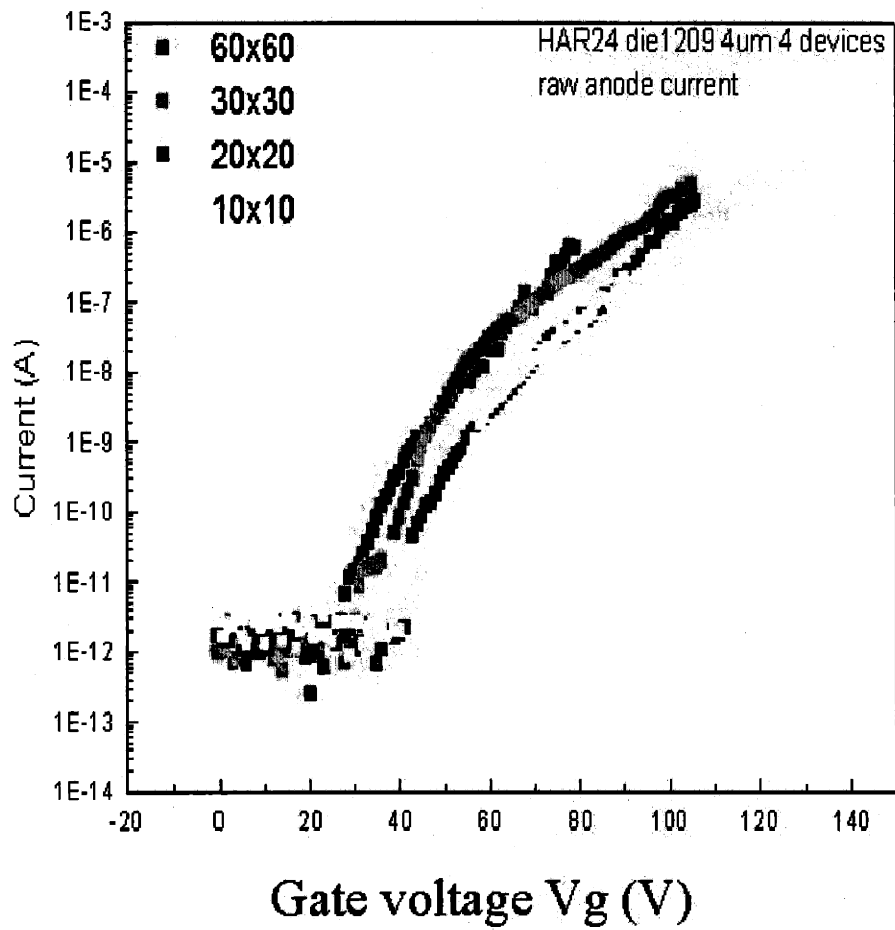


Figure 4-21: The anode currents plotted as a function of the gate voltage for 4 $\mu$ m pitch field emitter arrays within die1209.

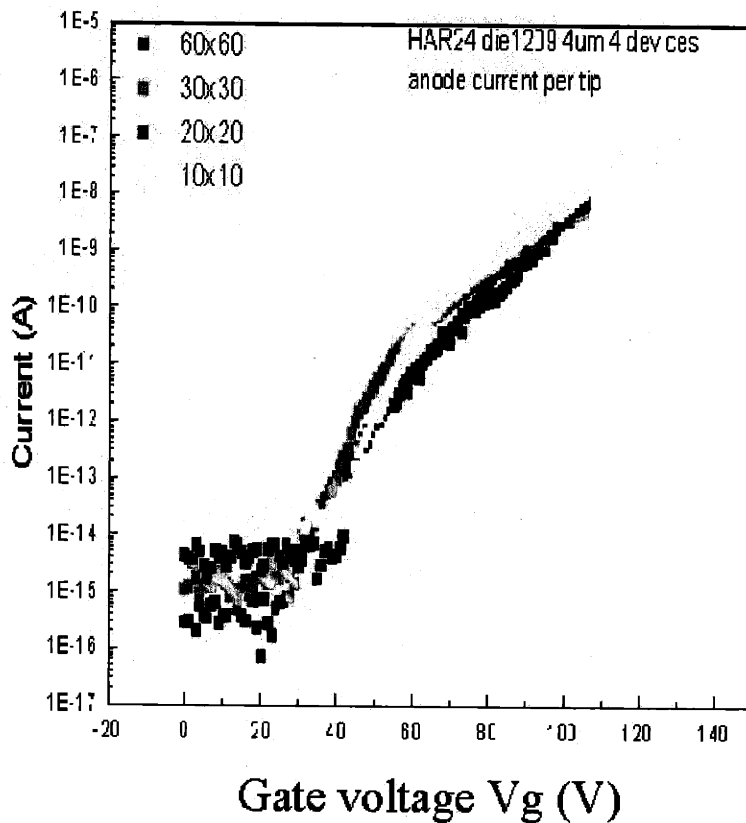


Figure 4-22: The normalized anode currents per emitter of the same die as in figure 4-21.

in figure 3-33 in the ordinary field emitter arrays.

From figure 4-17, 4-18, 4-21, and 4-22, it is observed that the high aspect ratio field emission arrays are not as good as regular emission arrays described in section 3.1. The turn-on voltage, current density, current uniformity of the high aspect ratio FEAs are not as good as those of the “regular” field emission arrays. We would like to argue that the following reasons may account for the differences:

- The exploratory fabrication process is not optimized. Two steps of aggressive chemical mechanical polishing might result in local non-uniformity of the de-

vices's geometric structures.

- Two LPCVD oxide deposition steps result in a discontinuity of the dielectric insulator, creating gaps and holes in the oxide, resulting in lower quality gate oxide.
- The apex of the tip is below the gate for a distance of approximately  $0.23\mu\text{m}$ . This lowering makes it easier for the electrons to be attracted to the gate electrode, resulting in larger gate leakage current.
- The prolonged hydrofluoric acid solution oxide etching step (about 30 minutes) to expose the emitter tip in the final stage of the fabrication process may to some extent have damaged the surface of the emitter tip, creating small protrusions at the surface, also resulting in non-uniformity of the emission currents.

### 4.2.3 Summary

In summary, we successfully fabricated high aspect ratio field emitter arrays. The experimental I-V data agree well with the Fowler-Nordheim theory. The fabrication process has been demonstrated, but it still needs to be optimized in order to improve its properties, like turn-on voltage, current density and current uniformity.

## 4.3 Discussion of field emitter array breakdown mechanism

The usual thinking about the device breakdown mechanism is the avalanche process of the dielectric material  $\text{SiO}_2$ . When the field across the dielectric oxide reaches the threshold field, impact ionization process occurs inside the dielectric, causing an explosive increase of current through the dielectric, thus breaking down the dielectric

[156]. That was the mechanism we thought of when we were testing the  $1\mu m$  aperture ordinary (not high aspect ratio) field emitter array. If oxide breakdown is the main mechanism of the device breakdown, the breakdown voltage should be proportional to the thickness of the  $SiO_2$ . The device breakdown voltage of the regular  $1\mu m$  aperture ordinary field emitter array with an oxide thickness of about  $700nm$  could be as high as  $150V$ . Then for our high aspect ratio emitter array with oxide thickness of more than  $2000nm$ , the breakdown voltage should be around  $400V$ . However from the characterization of the high aspect ratio emitter array in the previous sections, we observed that the device breakdown voltages are mostly around  $150V$  with some devices surviving up to  $200V$ . This observation made us reconsider what the main mechanism of the breakdown of the field emitter arrays is.

In order to measure the breakdown voltage of the  $SiO_2$  alone without the involvement of the field emitter array, we fabricated a wafer that has no field emitter array on it, but only with the sandwich structure of polycrystalline silicon/silicon dioxide/silicon substrate. The conditions of fabricating this wafer are identical to those under which the real device wafers were fabricated in order to ensure that we are testing the oxide that has the same quality. The thickness of the  $SiO_2$  dielectric layer is about  $540nm$ . Figure 4-23(a) shows the top view of a picture of this structure taken from the video camera as shown in figure 3-16. It is observed that there are no devices on this wafer. The probe is touching the polycrystalline electrode, just as it did before to the wafer with the devices on it. A voltage  $V$  is applied to the polycrystalline silicon layer. Figure 4-23 (a) shows the picture at  $V = 100volts$ . There is no observable difference between the probed pad and other unprobed pads. Figure 4-23 (b) shows the picture at  $V = 260volts$ . Some gray-scale changes were observed along the edges of the pad, but the oxide has not broken down yet. Figure 4-23 (c) shows the picture at  $V = 350volts$ . The oxide broke down and left a portion of the pad visibly burned. Before the breakdown occurred, flashing light was observed from the points of breakdown. Figure 4-23(d) shows the picture of another pad with a different shape at breakdown voltage of  $V = 370volts$ . Again a burnt out portion of pad after break-

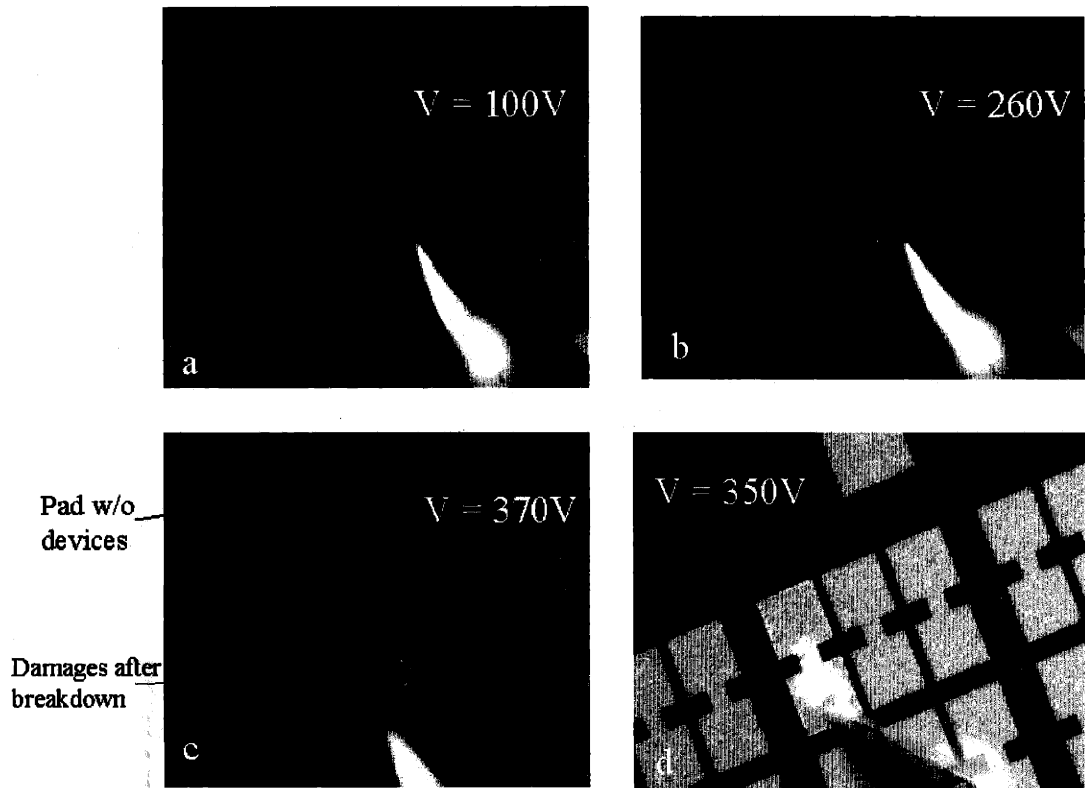


Figure 4-23: Oxide breakdown voltage measurement on test pads without field emitter arrays. Through the probe, we apply a voltage  $V$  to the polycrystalline silicon layer (a)  $V = 100\text{volts}$ . (b)  $V = 260\text{volts}$ . (c)  $V = 350\text{volts}$ . (d) shows another pad with dumbbell shape having a breakdown voltage of  $V = 370\text{volts}$ .

down is observed. Figure 4-24 shows the similar process of the breakdown for a square testing pad. After the square pad broke down at a voltage of  $V = 376\text{volts}$  it also left portions of the pad visibly burned. This burned portion is quite characteristic of the oxide avalanche breakdown.

Table C.1 [117] listed some of the important physical properties of  $\text{SiO}_2$ . The avalanche breakdown field of  $\text{SiO}_2$  is  $6 \times 10^6\text{V/cm}$ . So theoretically, for an oxide layer of thickness  $540\text{nm}$ , the breakdown voltage is

$$V_{\text{breakdown}} = 6 \times 10^6\text{V/cm} \times 540 \times 10^{-7}\text{cm} = 324\text{V} \quad (4.2)$$



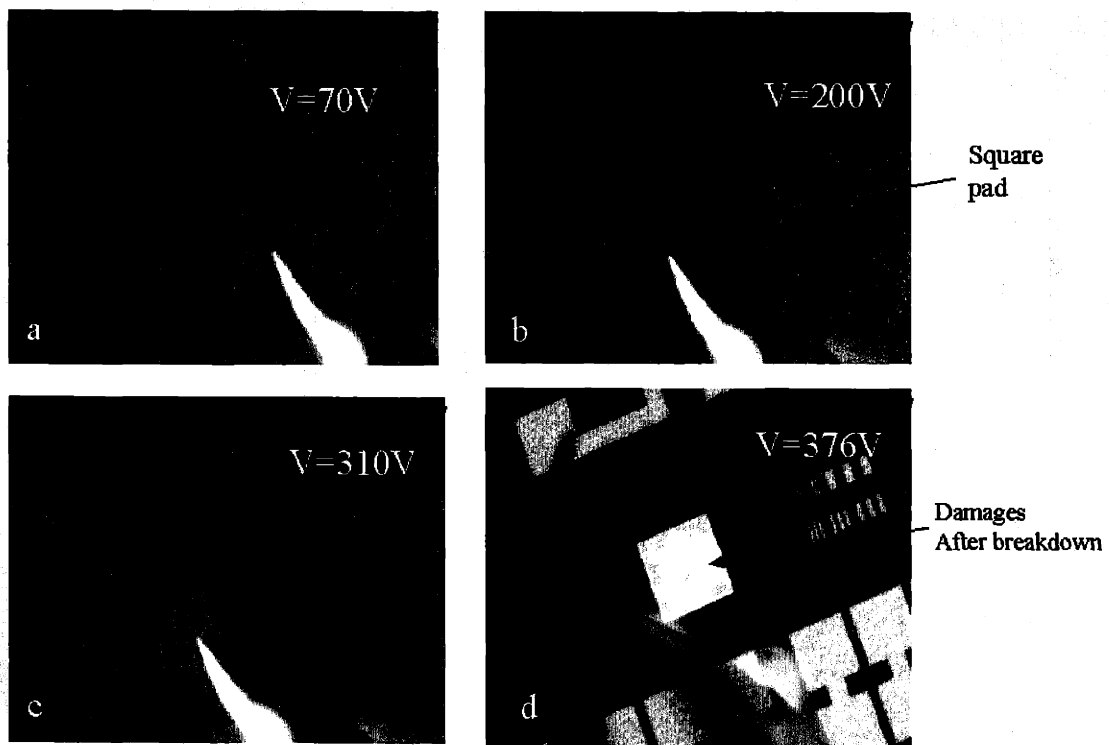


Figure 4-24: Oxide breakdown process of a square pad. After the square pad broke down at a voltage of  $V = 376\text{volts}$ , it also left a portion of the pad visibly burned. This burned portion is quite characteristic of an oxide avalanche breakdown.

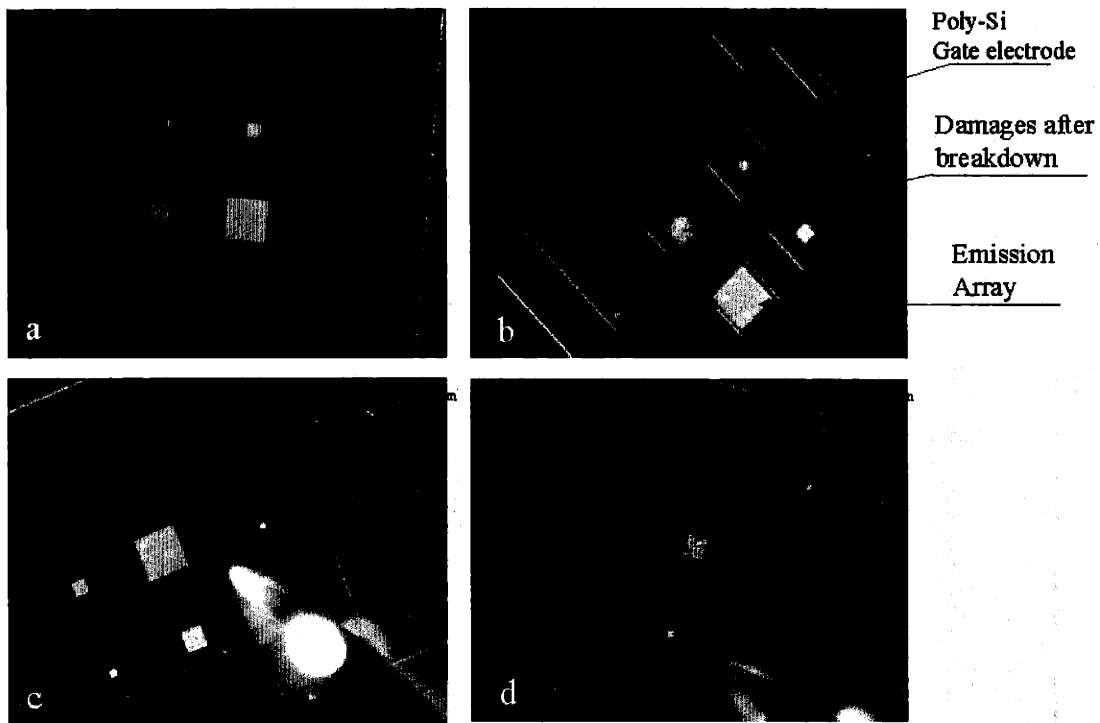


Figure 4-25: Breakdown images of real device wafers. (a) top view of a camera picture of a wafer surface with devices. This is before the testing of the device. Surfaces are “clean”. (b) after the breakdown of the devices. Significant damage is observed at the field emitter array area. (c) and (d) two other examples after device breakdown.

This value is in agreement with what we observed from our experiments. Furthermore, it also showed that there is no quality problem with our oxide. Busta et.al. also observed that bare silicon, tipless devices with  $0.85\mu m$   $SiO_2$  broke down around 500 – 600V which is the intrinsic breakdown voltage [86]. So, theoretically, for oxide layers of thickness of  $700nm$  and  $2000nm$ , the breakdown voltages should be around 420V and 1200V, respectively. However, it was not the case for our ordinary field emitter array and our high aspect ratio array, which have breakdown voltage typically less than 200V.

Figure 4-25 (a) shows the top view of a camera picture of a wafer surface with devices on it. This is before the testing of the device. The picture shows that the surface of the pad as well as the device area are “clean” and have no observable damage. Figure 4-25 (b) is a picture after the breakdown of the devices. It can be seen that

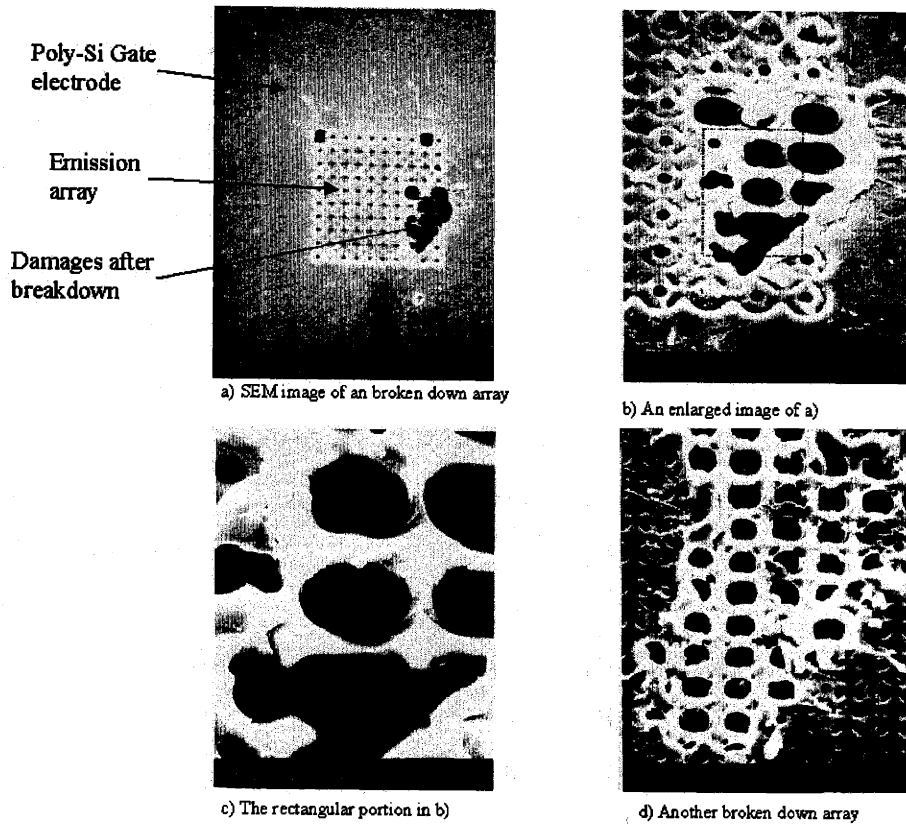


Figure 4-26: Images of breakdown damage in the emitter array area. (a) top view of a  $10 \times 10$  array. (b) An enlarged image of the melted polycrystalline gate. (c) An enlarged image of the damaged “holes” in the rectangular area in (b). (d) Damage images from a  $30 \times 30$  emitter array.

there is no burnt-out portion along the gate electrode as it is typically seen in the case of an oxide avalanche breakdown. However, it is observed that significant damage occurs in the field emitter array area. Figure 4-25 (c) and (d) are two other examples of device breakdown. They all exhibited the same observation as figure 4-25(b): with no burnt-out portion along the gate electrode, but with significant damage in the field emitter array area. Figure 4-26 shows the SEM images of the damaged array area. It is clear from the figure that the gate polycrystalline silicon was severely damaged and possibly melted. The images indicated that the breakdown of the device resulted from a rather “explosive” process in the array area. This is the evidence that there is something happening in the emitter array area that leads to breakdown, not the avalanche breakdown of the dielectric material  $SiO_2$ .

McGruer et al. fabricated silicon field emitter arrays with a gate aperture of  $2.3\mu\text{m}$ , a silicon tip height of  $1.3\mu\text{m}$ , and a  $\text{SiO}_2$  dielectric of thickness of  $1\mu\text{m}$ . The gate material of their device is aluminum, instead of doped polycrystalline silicon, as in our devices. The “theoretical” breakdown voltage for  $1\mu\text{m}$  thick  $\text{SiO}_2$  is above  $600\text{V}$ . However, most of their field emitter arrays experienced breakdown at gate voltages ranging from  $75\text{V}$  to  $200\text{V}$  [115], very similar to the breakdown voltage range in our devices. The images of the damage after our device breakdown are consistent with their images of the damage [114, 115]. Spindt et al. also reported similar surface damage in molybdenum field emitter arrays [18]. Shaw and Gray proposed that arc damage is a primary failure and degradation mechanism in field emitter arrays [114]. Jim Browning et al. also proposed that the breakdown is due to the arcing between the gate and the emitter [116]. Although there is not a consensus about the theory on how the arcing is initiated, it is generally believed that the arcing is due to the ionization of the neutral gas molecules, either desorbed from the surface or from evaporated tip materials [114, 116]. The desorption of gas molecules absorbed on the surface might be due to the heating produced by large emission currents going through the emitter tips.

Based on our observation and the comparison with the literature, we agree with the literature that the arcing between the emitter and the gate might contribute to the breakdown of our devices. The same mechanism also applies to the breakdown of the regular field emission arrays described in chapter 3. Certainly, the problem of device breakdown in the field emitter array case is very complicated due to the device’s non-planar structure.

The breakdown problem is a crucial limiting factor to the device’s properties such as performance, reliability, and lifetime. Further study of the device breakdown mechanism in field emitter arrays is needed to address the above concerns.

# Chapter 5

## Current saturation and valence band electron field emission

### 5.1 Literature background

In the two previous chapters the fabrication and characterization of silicon field emitter arrays were reported. In the two chapters it was observed that the Fowler-Nordheim plot leveled off at high applied gate voltages, indicating current saturation in these cases.

Most of the n-type semiconductor field emitters reported in the literature have current ( $I$ ) - voltage ( $V_g$ ) characteristics that obey the Fowler-Nordheim equation, showing a linear fit on the  $\ln(I/V_g^2)$  vs.  $1/V_g$  plot [20, 66, 122]. However the current-voltage characteristics of p-type silicon field emitter arrays were observed to obey Fowler Nordheim theory only at low gate voltages, showing a non-linear fit on the  $\ln(I/V_g^2)$  vs.  $1/V_g$  plot [124, 125, 126, 127, 128, 130].

It is believed that the emission from silicon is predominantly due to electron tunneling from the conduction band. Generally the conduction band electrons are treated as a

Fermi sea with the surface barrier height approximately equal to the electron affinity of silicon. In p-type silicon, the electron concentration in the conduction band is very low. So Fowler-Nordheim theory only holds at low applied voltages. At high voltage, the emission current is limited by the electron supply and hence the observed current saturation. At even higher gate voltages, the current increases rapidly with voltage [123, 125, 126].

Previous authors attributed the phenomenon to electron generation through impact ionization or other means. We argue that this phenomenon is probably due to electron emission from the valence band. For n-type silicon, the theories did not exclude the existence of a saturation region. Baskin, Lvov, and Fursey actually predicted that such saturation will occur at sufficiently high fields [123]. Gray, Campisi, and Greene found indications of current saturation in n-type silicon field emitter arrays [129]. These theories also predicted that electron emission from the valence band is possible and the current obeys Fowler-Nordheim theory by replacing the electron affinity  $\chi$  by  $\chi + E_g$ , where  $E_g$  is the energy gap of silicon [46, 62]. Borzyak, Yatsenko, and Miroshnichenko suggested the valence band as possible electron source in high-resistance silicon but argued that the electron emission comes from a two-stage process: electrons go from the valence band or impurity centers to the conduction band, and then to the vacuum [128]. In this model, all electron emission to vacuum comes from the conduction band.

There has been direct evidence of field emission from the valence band from other semiconductor materials like diamond and diamond-like-carbon (DLC). Diamond and diamond-like-carbon have negative electron affinities [132]. So, under normal conditions, there are no electrons in the conduction bands of these materials. Bandis and Pate at Washington State University conducted simultaneous field emission and photoemission measurement from diamond and measured the energy distribution of emitted electrons [133]. Figure 5-1 shows the experimental setup of their measurements.

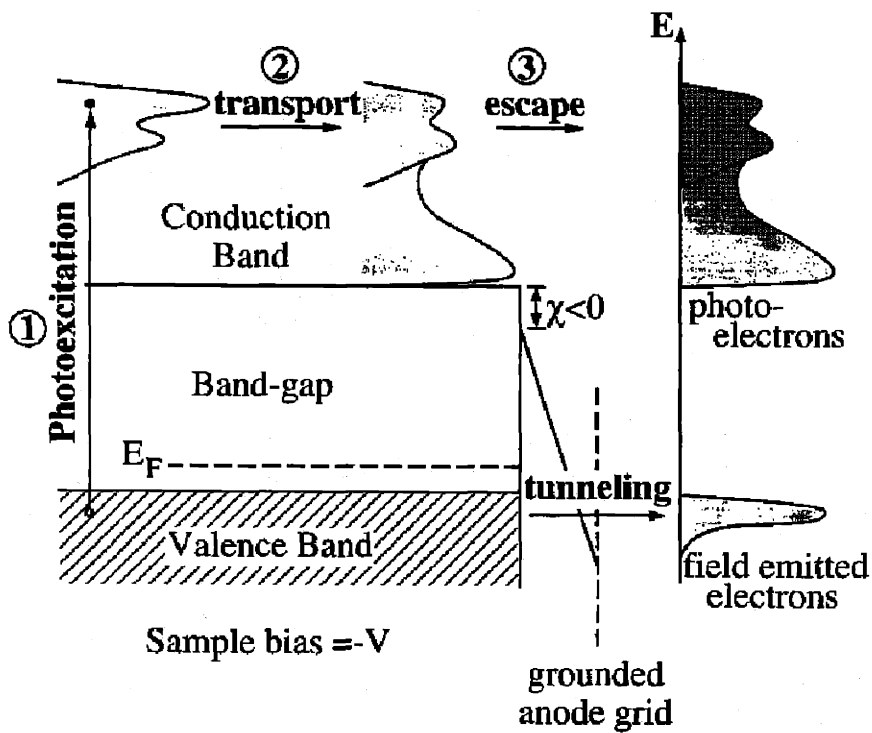


Figure 5-1: Energy diagram of the experiment performed by Pate et al. [133]. Under conditions of illumination with UV radiation and sufficiently high electric field at the surface, both field emission and photoemission occurs. Please note that the electron affinity of diamond  $\chi$  is negative.

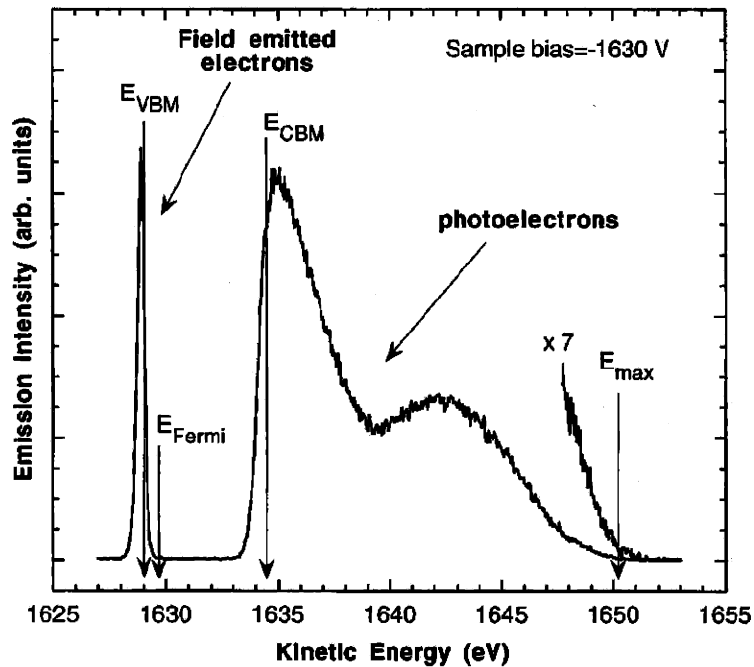


Figure 5-2: An electron energy distribution measurement from reference [133]. The sample is biased at  $-1630\text{V}$  and the surface is illuminated with  $2.12\text{eV}$  radiation. It is obvious that the field emission energy distribution peaks at the valence band maximum.

Figure 5-2 shows the energy distribution measurement of the emitter electrons in their experiments. There were two peaks in this energy distribution measurement: one at the valence band maximum and the other at the conduction band minimum. If the UV radiation was turned off while the sample was still biased, the peak at the conduction band minimum disappeared while the peak at the valence band maximum remain unaltered. This observation confirmed that the field emission electrons came from the valence band of diamond. Furthermore, it confirmed that the UV radiation excited the electrons from the valence band to the conduction band and that the electrons escaped from the conduction band to vacuum.

Gröning et al. [134] performed energy distribution measurements for the field emission and photoemission of diamond-like-carbon. Figure 5-3 shows the results of their measurements. This figure is very similar to figure 5-2. They concluded that the field



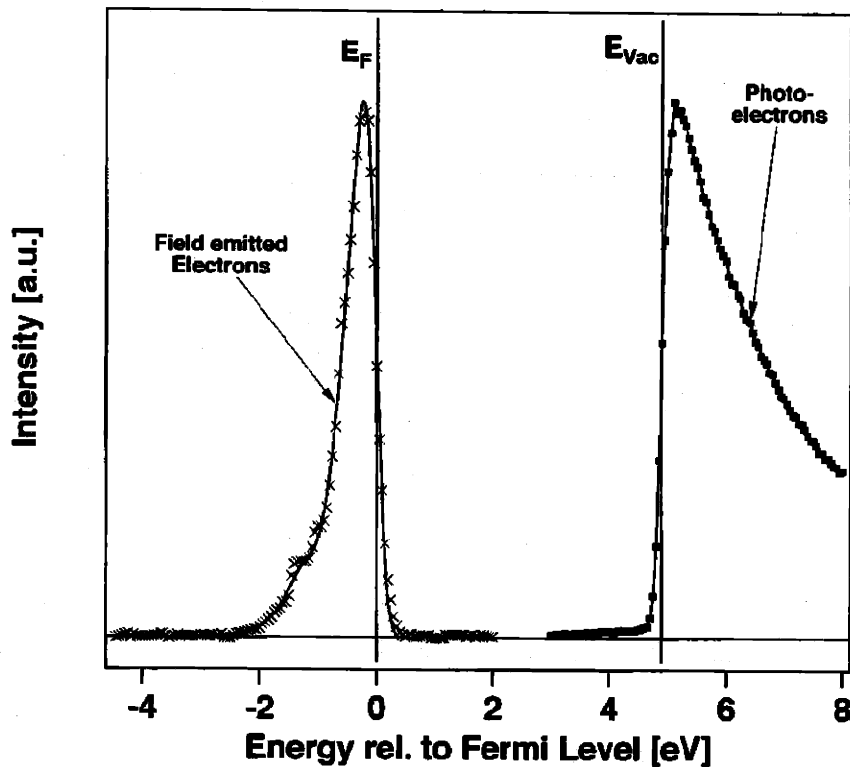


Figure 5-3: Field emission spectra (crosses) and UPS (ultraviolet photoelectron spectroscopy) photoemission spectra (dots) of the diamond-like carbon. This figure is quoted from reference [134].

emission came from the valence band of the semiconducting diamond-like-carbon with the Fermi level position at the top of the valence band.

Electron tunneling from the valence band of silicon is not an unfamiliar phenomenon in Metal-Oxide-Semiconductor field-effect-transistor (MOSFET) research. As the MOSFET technology approaches ever smaller dimensions, the gate oxide has become so thin that electrons can tunnel through it. Figure 5-4 is quoted from reference [136]. It shows an energy diagram of a MOS structure. Eitan and Kolodny [135] observed a hole current in the *p*-collector-substrate terminal of a 7.8nm oxide *n*+sourced MOS capacitor under positive gate bias and attributed it to valence band electron tunneling from the *p* type substrate. Klaus Schuegraf and Chenming Hu [136] reported that tunneling by valence band electrons contributed to the MOSFET

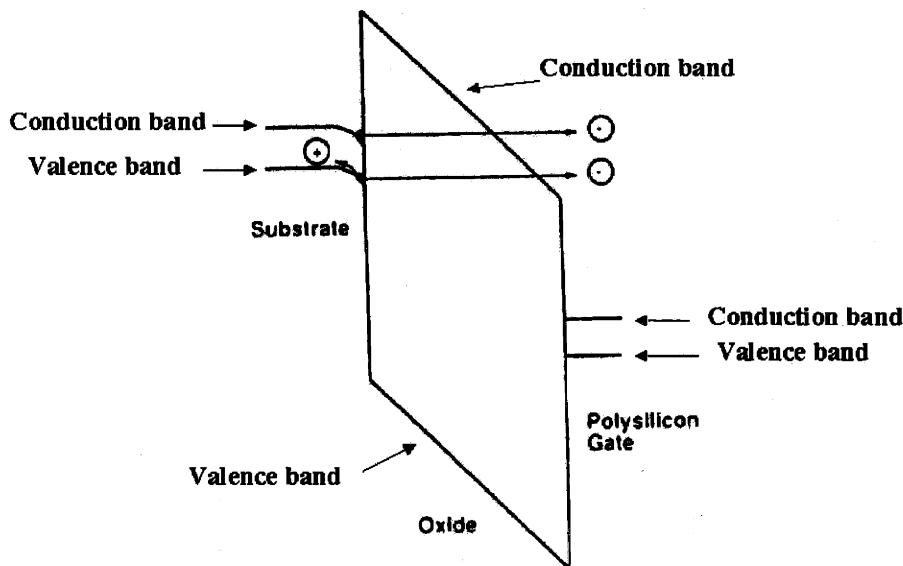


Figure 5-4: An energy diagram of a MOS capacitor. This diagram is quoted from reference [136].

substrate current devices with gate oxide thinner than  $45\text{\AA}$ . Junji Ikeda, Atsushi Yamada, Kazuya Okamoto, Yoshiaki Abe, Kaoru Tahara, Hidenori Mimura, and Kuniyoshi Yokoo reported evidence of tunneling emission from the valence band in a metal-oxide-semiconductor (MOS) cathode, using both  $n$  and  $p^+$  silicon wafers [137]. Similar reports can also be seen in references [138, 139, 140].

The discussions above all suggested that direct electron emission from the valence band to vacuum could occur in silicon field emitters.

In this chapter, the observation of the current saturation and electron field emission from the valence band of silicon field emission arrays, will be described. The detailed description of the device fabrication process and the characterization setup could be found in chapter 3, chapter 4, and reference [131]. An important requirement for achieving valence band electron emission is the fabrication of very small radius tips capable of producing high electric fields on the emitter surface. This requirement was achieved by the oxidation sharpening process described in the previous two chapters.

## 5.2 Device characterization

We first characterized the n-type silicon field emitter arrays with a low dopant concentration of  $10^{16} \text{cm}^{-3}$ . The wafer is the same as we presented in section 3.1. Figure 3-12 shows the cross section of the final devices. The SEM picture shows that the radius of curvature of the emitter tip is about  $9.2 \text{nm}$ , as shown in figure 3-7. The setup of the vacuum probe station and the electrical characterization setup were described in detail in section 3.2.1.

### 5.2.1 Observation of current saturation

In figure 3-19, the Fowler-Nordheim characteristics showed current saturation in a  $60 \times 60$  n-type silicon field emitter array at high gate voltage. The saturation current is approximately  $1 \times 10^{-7}$  A/tip. Figure 5-5 shows a clear demonstration of current saturation in two of the  $10 \times 10$  field emitter arrays.

### 5.2.2 Simple model for current saturation

We propose that the observed current saturation is due to the electron velocity saturation in the silicon conduction band. The silicon substrate has a relatively low dopant concentration of  $10^{16} \text{cm}^{-3}$  compared to an electron concentration of about  $10^{22} \text{cm}^{-3}$  in a metal. Figure 5-6 shows a schematic of a model we propose to account for the current saturation data.

The current through the neck of a tip is given by

$$I = \alpha' q n v_s \quad (5.1)$$

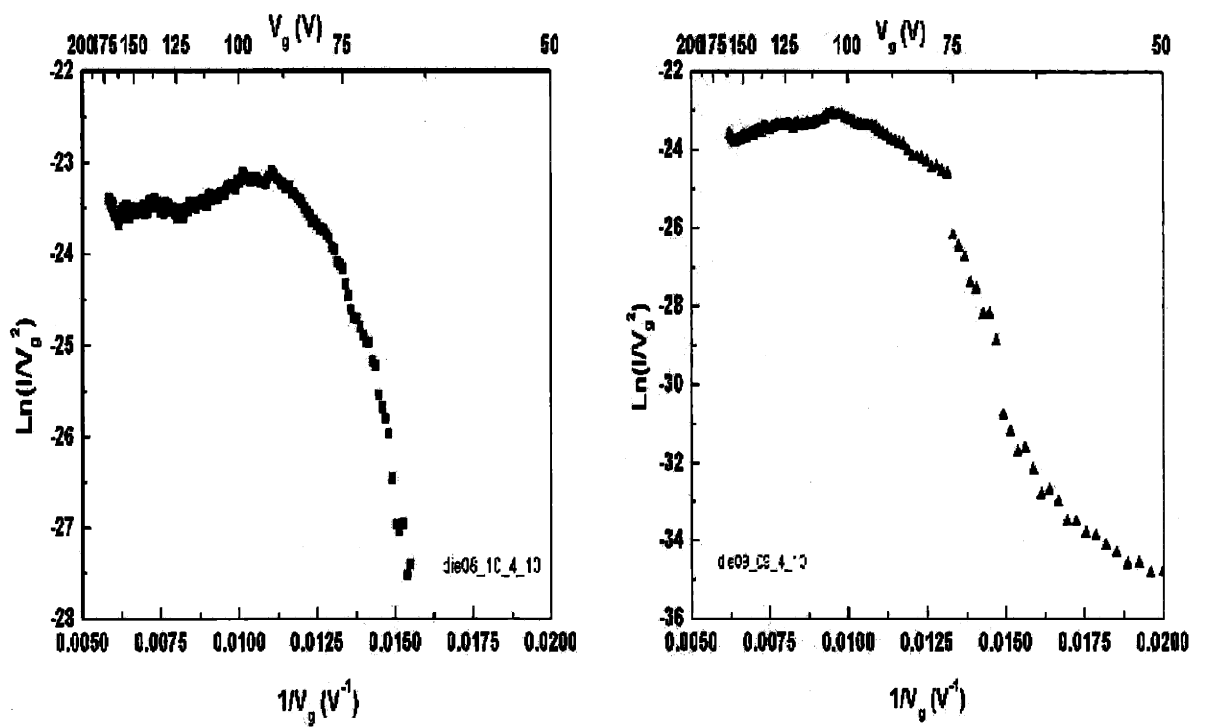
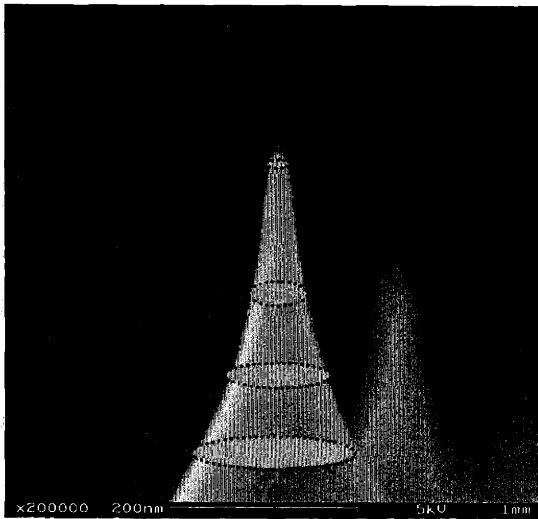


Figure 5-5: Fowler-Nordheim plots of the current voltage characteristics showing current saturation in two  $10 \times 10$  field emitter arrays.



$$\alpha' \sim \pi r_{\text{tip}}^2$$

$$I_{\text{sat}} = \alpha' q n v_{\text{sat}}$$

$$v_{\text{sat}} = 1 \times 10^7 \text{ cm} \cdot \text{s}^{-1}$$

$$n = 10^{16} \text{ cm}^{-3}$$

$$r_{\text{tip}} = 9.2 \text{ nm}$$

$$I_{\text{sat,th}} \sim 4.26 \times 10^{-8} \text{ A}$$

$$I_{\text{sat,ex}} \sim 1 \times 10^{-7} \text{ A}$$

Figure 5-6: A schematic of a current saturation model. The saturation is due to (a) the finite electron density and (b) the finite electron saturation velocity in silicon. The model limits the electron supply to the emitter surface, thus limiting the current, and leading to current saturation. The theoretical saturation current agrees with the experimental value well.

where  $\alpha'$  is the approximate cross-sectional area of the tip neck,  $v_s$  is the electron velocity,  $q$  is the electron charge and  $n$  is the electron concentration. To first order, this cross-sectional area is given by

$$\alpha' = \pi \cdot r^2 \quad (5.2)$$

where  $r$  is the radius of curvature of the tip.  $v_s$  is upper bounded by the electron saturation velocity in silicon:

$$v_{\text{sat}} = 1 \times 10^7 \text{ cm} \cdot \text{s}^{-1} \quad (5.3)$$

Using these parameters the saturation emission current per tip is estimated to be  $4.26 \times 10^{-8}$  A/tip. This value is consistent with the observed value of about  $1 \times 10^{-7}$  A/tip.

### **Possible application of current saturation**

The observed current saturation could be an advantage in display applications because a series feedback resistor would not be needed [143, 144]. Typically in a field emission display, an emitter array is connected to either an integrated resistor or a field effect transistor. The function of these auxiliary components is to stabilize the current even in the presence of non-uniform tip radius distributions. The inherent current saturation properties of a lightly doped semiconductor emitter will make this requirement obsolete. This could potentially simplify the fabrication process significantly, reduce the amount of needed integrated electrical components, and lower the cost.

### **5.2.3 Observation of valence band electron emission**

At even higher gate voltages, the Fowler-Nordheim plots in figure 5-5 show signs of another current increase. This suggests that the Fowler-Nordheim characteristics should be examined at even higher gate voltages.

Figure 5-7 is the Fowler-Nordheim plot of the average emitter current per tip from a  $10 \times 10$  array. The device was characterized at higher gate voltages than those in figure 5-5. Three regions of operation could be observed in figure 5-7

1. a sloped region at low voltage which obeys the Fowler-Nordheim equation,
2. a relatively flat segment at intermediate voltages and
3. a sloped region at high voltages which also obeys the Fowler-Nordheim equation.

The two "transition" voltages between the three regions are approximately  $V_1 = 90V$  and  $V_2 = 130V$ . Using the Fowler-Nordheim equation, the field factor  $\beta$  could be extracted at the lower gate voltages from the current-voltage characteristics, shown

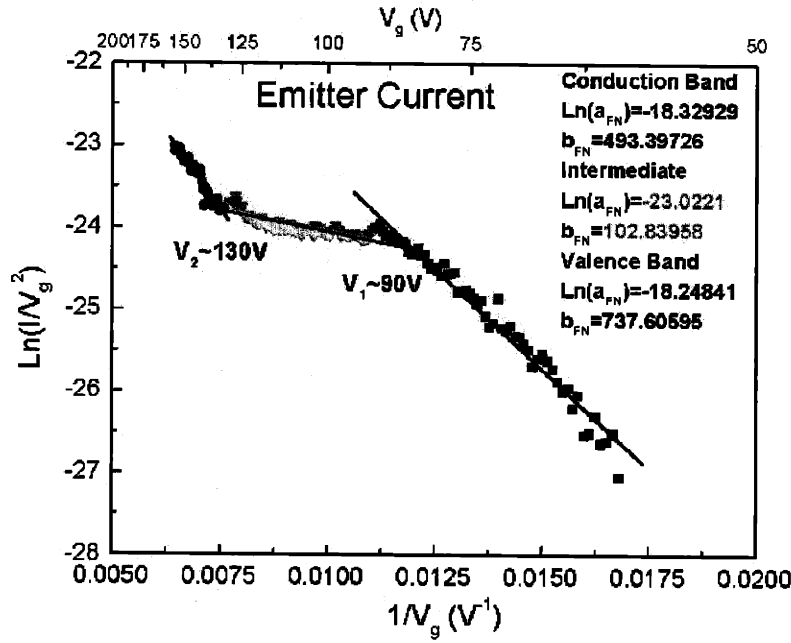


Figure 5-7: Demonstration of conduction band field emission, current saturation and valence band field emission in a  $10 \times 10$  array.

in figure 5-7. From figure 5-7, the field factor  $\beta$  was calculated to be  $1.07 \times 10^6 \text{ cm}^{-1}$ . At a gate voltage  $150\text{V}$  this gives a surface field of  $1.61 \times 10^8 \text{ V cm}^{-1}$  ( $1.61\text{V}/\text{\AA}$ ).

Using the “ball-in-sphere” model discussed in section 2.8.1 ( $\beta = \frac{1}{r}$ ), a tip radius is calculated to be about  $9.3\text{nm}$ . Using the numerical simulation method described in section 3.3.1 ( $\beta = \frac{22.73 \times 10^5}{r^{0.69266}} \text{ V/cm}$  as shown in equation 3.4), a tip radius is calculated to be  $2.97\text{nm}$ .

It is worth noting that the data presented here was obtained at tip electrostatic fields of  $6-16.5 \times 10^7 \text{ V/cm}$ . These fields are beyond what is necessary to overcome the internal barrier produced by surface states as suggested by Stratton [61]. As it is already shown in section 3.2.2 that for a typical surface state density of  $\sigma = 1.2 \times 10^{13} / \text{cm}^2$  [61, 130], only a small external electric field of  $F = \frac{\sigma}{\epsilon_0} = \frac{1.2 \times 10^{13} \times 1.6 \times 10^{-19} \text{ C/cm}^2}{8.85 \times 10^{-14} \text{ F/cm}} = 2.17 \times 10^7 \text{ V/cm}$  is needed to overcome the surface states.

## 5.2.4 Two band field emission model

We present a two-band field emission model as a possible explanation for the experimental data in figure 5-7. It is schematically depicted in Figure 5-8.

At low gate voltages most of tunneling electrons come from the conduction band. At this stage, the electron supply is sufficient and the device is in a quasi-static state. A quasi-static state is a state in which equilibrium can still be assumed. The current-voltage characteristic is controlled by electron transmission through the barrier and it follows the Fowler-Nordheim formula. As the gate voltage increases, the emission current increases too because the electron transmission increases. The electron supply is eventually limited by the flux of electrons to the surface, as described in equation 5.1, to be  $I_{sat} = \alpha' q n v_{sat}$ . At this stage the device is in steady state (which means the state does not change with time) but not a quasi-static state. Similar argument has been presented before by Gray et al. [129]. At even higher gate voltages electrons are emitted from the valence band into vacuum. The current-voltage characteristic in this region also obeys the Fowler-Nordheim formula but with a higher effective electron affinity  $\chi_{eff} = \chi + E_g$ . Since the electron concentration in the valence band is very high (it is a nearly full band), the predicted saturation current for valence band emission, if it occurs, is  $I \approx 1A - 10A/\text{tip}$ .

A simple test of the physical picture just proposed is provided by calculating the ratio of the slopes of Fowler-Nordheim plots in the valence band emission and conduction band emission regions. The experimentally observed value is

$$\frac{b_{FN,vb}}{b_{FN,cb}} \approx 1.50. \quad (5.4)$$

This value is in close agreement with the theoretically predicted value of



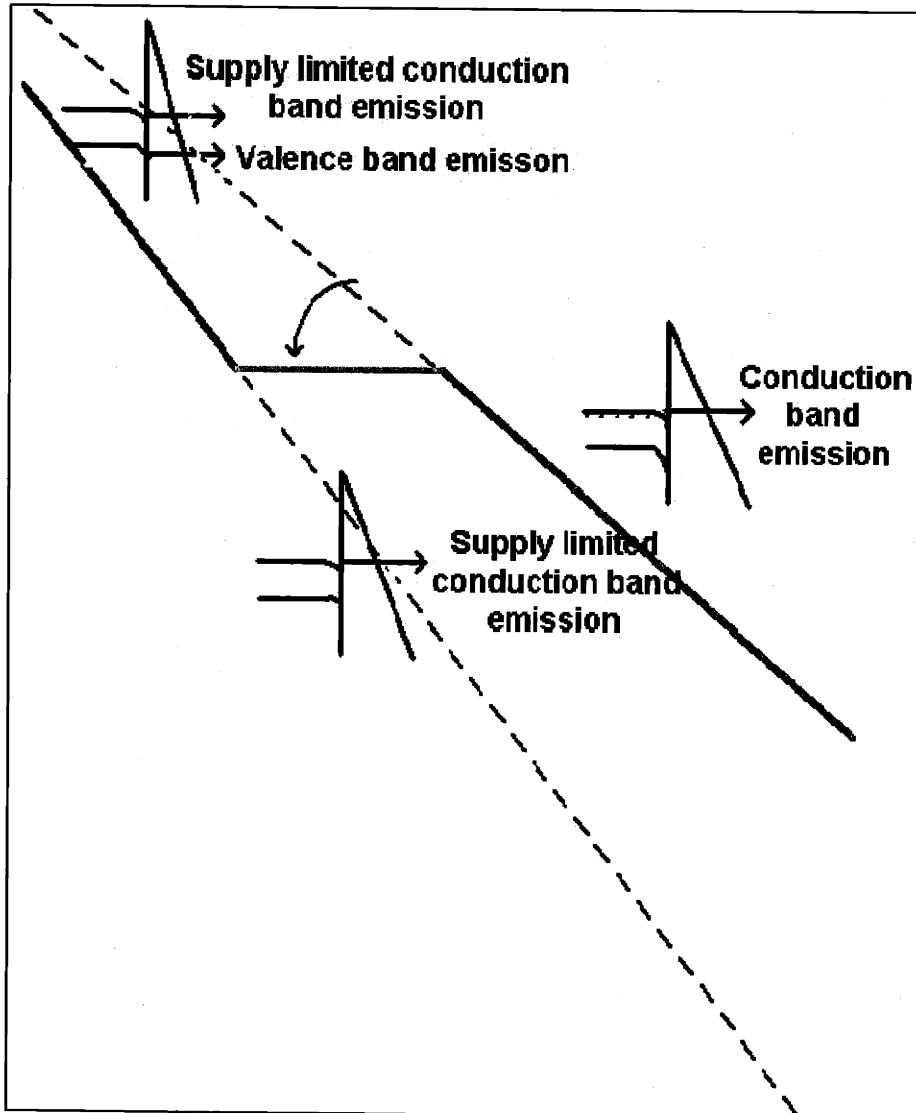


Figure 5-8: Two band field emission model. At low voltages most tunneling electrons come from the conduction band. The current-voltage characteristic is in the electron transmission controlled region. At intermediate voltages, the device is in an electron supply controlled region, and the current is limited by  $I_{sat} = \alpha/qnv_{sat}$ . At even higher gate voltages, electrons are emitted from the valence band into the vacuum.

$$\left(\frac{\chi + E_g}{\chi}\right)^{3/2} \approx 1.45 \quad (5.5)$$

where  $\chi = 4.05eV$  and  $E_g = 1.12eV$  for silicon.

Another simple test is the ratio of the value of the two transition voltages shown experimentally in figure 5-7. The first transition voltage  $V_1$  is the boundary between conduction-band-dominated emission and velocity saturation while the second transition voltage  $V_2$  is the boundary between velocity saturation and valence-band-dominated emission. A further analysis of the FN plot shown in Figure 5-7 reveals that two values of  $\ln(I/V_g^2)$  are approximately equal at  $V_1$  and  $V_2$ . It can thus be deduced that

$$\frac{-b_{FN,cb}}{V_1} \approx \frac{-b_{FN,vb}}{V_2} \quad (5.6)$$

and hence

$$\frac{(\chi)^{3/2}}{V_1} \approx \frac{(\chi + E_g)^{3/2}}{V_2} \quad (5.7)$$

The experimentally observed value of

$$\frac{V_2}{V_1} \approx 1.44 \quad (5.8)$$

is very close to the theoretically predicted value of

$$\left(\frac{\chi + E_g}{\chi}\right)^{3/2} \approx 1.45 \quad (5.9)$$

The above approximation only works if

$$\ln(a_{FN,cb}) \approx \ln(a_{FN,vb}). \quad (5.10)$$

From equation 2.42 and equation 2.53, it is observed that  $a_{FN} \sim \frac{\alpha m^*}{\varphi} e^{\frac{B(1.44 \times 10^{-7})}{\varphi^{\frac{1}{2}}}}$  where  $\alpha$  is the effective emission area which could be assumed to be the same for the conduction and valence band emission for the same device,  $m^*$  is the effective mass for electrons and holes, respectively, and  $\varphi$  is the barrier height, which is  $\chi$  and  $\chi + E_g$  for conduction and valence bands, respectively. It is observed that there are weak dependences of  $a_{FN}$  on  $m^*$  and on  $\chi$  or  $\chi + E_g$ . Taking  $m_e^* = 0.28m_0$ ,  $m_h^* = 0.41m_0$ ,  $\chi = 4.05eV$ , and  $\chi + E_g = 5.17eV$  (appendix B) into consideration, it is found that theoretically  $\frac{a_{FN,cb}}{a_{FN,vb}} \approx 1.53$ . This leads to a theoretical value of  $\ln(a_{FN,cb}) - \ln(a_{FN,vb}) \approx 0.43$ , which means the two values are very close. This closeness is demonstrated experimentally in figure 5-7. The slight difference in the value will not change the value of equation 5.8.

Recall equation 2.61, which calculated the decrease in barrier height due to field penetration,  $\Delta\varphi = \nu F^{\frac{4}{5}}$ , where  $\nu = 4.5 \times 10^{-7} \epsilon^{-\frac{2}{5}}$  and  $\epsilon = 11.9$  is the dielectric constant of silicon. Assume that this equation is still valid at high electric field. For the device in figure 5-7, the decrease in barrier height for the conduction band is of the order of  $0.4eV$  at  $V_g = 90V$  and  $0.58eV$  at  $V_g = 130V$ . However, at these voltages, the emission has entered the conduction band current saturation region or valence band emission region, and consequently it does not need to be considered.

As mentioned in the beginning of this chapter, some authors argued that the second rise of current beyond the saturation region in the Fowler-Nordheim plot might be caused by the impact ionization process in the semiconductor, due to strong field penetration of the external electric field [123, 127]. Other authors [128] proposed models that describe the process as a two-stage process: electrons go from the valence band or impurity centers to the conduction band and then to the vacuum [128]. We

disagree with these descriptions based on the following observation. For the above two models, the emitted electrons actually all come from the conduction band. The effect of these two processes is to increase the carrier (electron) concentration in the conduction band. However, in these situations the barrier height of these electrons remains to be approximately the electron affinity of silicon. So the slope of the Fowler-Nordheim plot should remain the same. In our experiments, we saw the slope change to the value that corresponds to the barrier height of electrons at the valence band. We do not rule out the possibility of impact ionization, but we argue that impact ionization can not quantitatively explain the experimental results. We propose that an energy distribution measurement performed on a silicon emitter, similar to the one described in figure 5-1, figure 5-2 and reference [133], would give a direct verdict on this discussion. This experiment will be carried out in the future.

#### **An analog to a water tank nozzle model**

In order to better understand the valence band emission, in the following text we provide a nozzle model as an analog to the two-band field emission model we presented above.

We model the whole process of field emission as a water(electron) tank with a nozzle as depicted in figure 5-9. The external electric field controls the faucet of the water nozzle. There are two sources of electron supply to the tank: the conduction band electrons and valence band electrons. In the "cut-off" region, the electric field is not strong enough so that the faucet is closed, and the electrons can not come out of the tank.

Figure 5-10 shows the conduction band emission transmission controlled region. The electric field is strong enough so that the faucet is opened and the electron from conduction band can "pour" out of the tank. At this stage the current density is controlled by how big the opening of the nozzle is, i.e., how strong the electric field

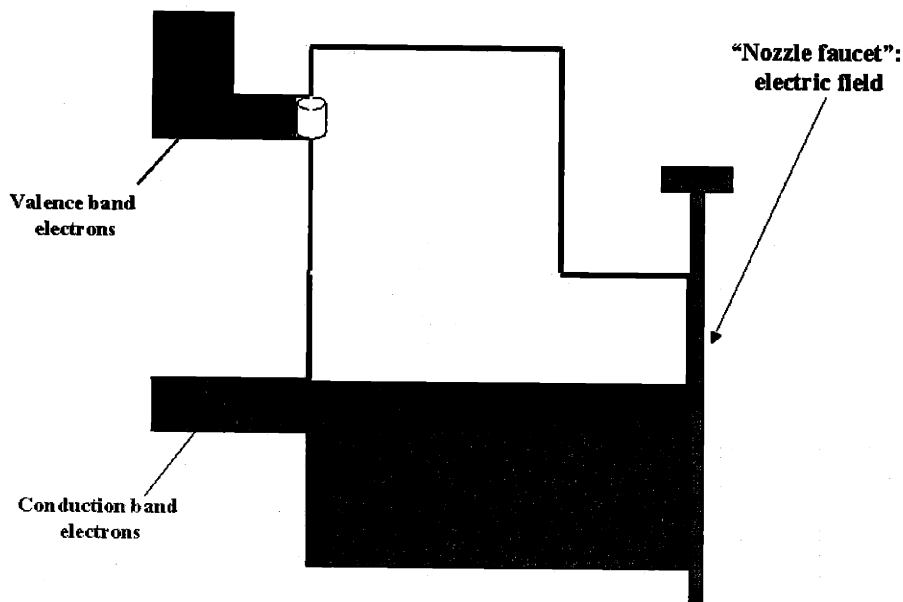


Figure 5-9: Water (electron) tank with a nozzle and a faucet model. The external electric field controls the faucet of the nozzle. This figure shows the “cut-off” region, where the electric field is weak and the faucet is closed, resulting in no emission current.

is. This is a steady state as well as a quasi-static state. The current is governed by the Fowler-Nordheim formula.

Figure 5-11 show the case of the current saturation of the conduction band electron field emission. The faucet has been opened enough (the external electric field is high enough) and the opening of the nozzle is so big that the increasing opening of the nozzle does not actually increase the emission current density. In this case the current is solely determined by the electron supply to the surface of the emitter tip. This is the current saturation of the conduction band field emission. It is a steady state, but not a quasi-static state.

Figure 5-12 shows the case that both conduction band and valence band electrons are available for the emission currents. As the external electric field gets larger and larger, the electron in the reservoir of the valence band become available, thus it fills the tank. At this case the opening of the nozzle is again not big enough. The field emission process goes back to the transmission controlled stage for the valence band electrons

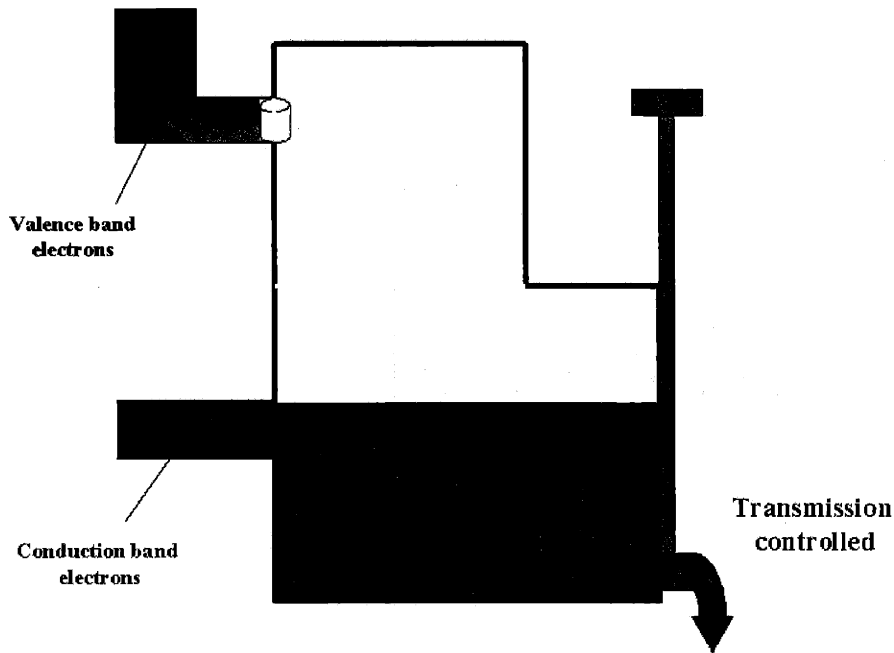


Figure 5-10: Transmission controlled conduction band field emission region. The current density is controlled by how big the opening of the nozzle is, i.e., how strong the electric field is.

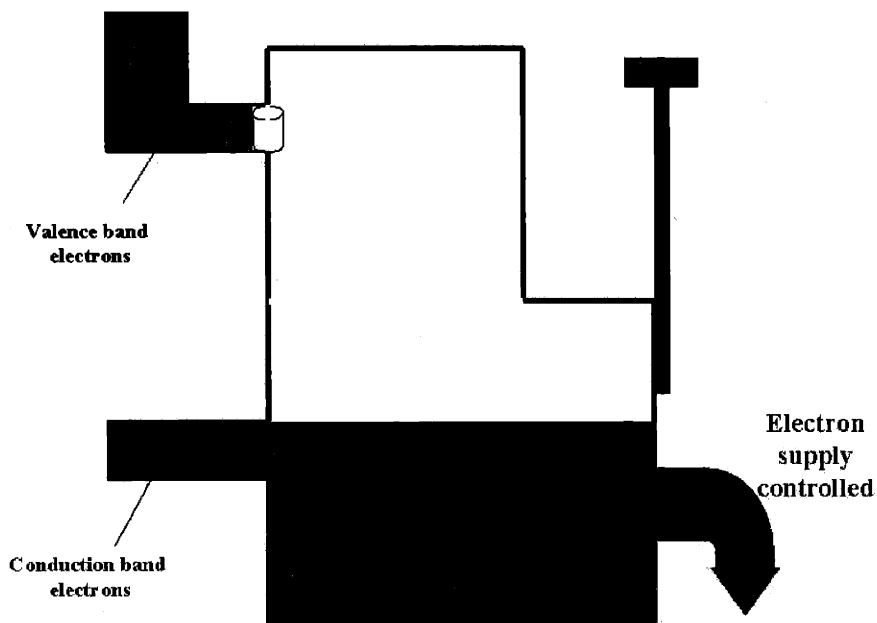


Figure 5-11: Current saturation of the conduction band electron field emission. The current is solely determined by the electron supply to the surface of the emitter tip. It is a steady state, but not a quasi-static state.

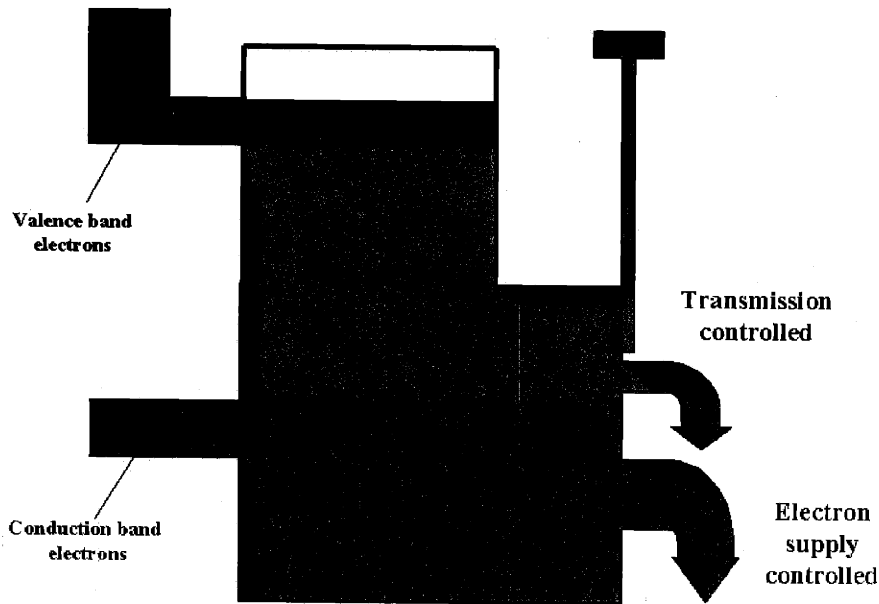


Figure 5-12: Electron field emission from both the conduction band and the valence band electrons. At high electric field, the electrons in the reservoir of the valence band became available, thus it fills the tank. The field emission process goes back to the transmission controlled stage for the valence band electrons (with conduction band emission current still in saturation).

(with the conduction band emission current still in saturation). Then once again, the opening of the nozzle is determining how much current we can get, giving rise to the second region that obeys the Fowler-Nordheim formula. Please note that it is the high electric field that makes the electron emission from the valence band become appreciable. The transition between figure 5-11 and figure 5-12 is actually gradual. However, because of the exponential nature of the Fowler-Nordheim equation, it is safe to say, at least as symbolically shown in figure 5-12, that at one point, the reservoir of electron in the valence band suddenly became available.

### 5.2.5 Valence band emission from silicon substrates with dopant concentrations

In order to solidify our observation of valence band electron field emission, we fabricated several regular field emitter arrays with different substrate dopant concentrations. Among them there are three n-type emitter arrays and one p-type emitter arrays. In all of these four types of devices, valence band electron field emission was observed.

Figure 5-13 shows the two-band field emission from an n-type  $30 \times 30$  field emitter arrays with a dopant concentration of about  $3.5 \times 10^{18} \text{cm}^{-3}$ . The device turned on at about  $18V$ . The current saturated at approximately  $5 \times 10^{-10} A$  per tip, which was much lower than expected.

Figure 5-14 shows the two-band field emission from an n-type  $30 \times 30$  field emitter array with a dopant concentration of about  $6 \times 10^{15} \text{cm}^{-3}$ . The device turned on at about  $42V$ . The current saturated at approximately  $1 \times 10^{-9} A$  per tip.

Figure 5-15 shows the two-band field emission from an n-type  $60 \times 60$  field emitter array with dopant concentration of about  $2 \times 10^{14} \text{cm}^{-3}$ . The device turned on at about  $33V$ . The current saturated at approximately  $5 \times 10^{-10} A$  per tip.

Figure 5-16 shows the two-band field emission from a p-type  $20 \times 20$  field emitter array with dopant concentration of about  $1 \times 10^{15} \text{cm}^{-3}$ . The device turned on at about  $30V$ . For this particular device the current saturation was not as pronounced as in figure 5-14 and in figure 5-15. The current saturation occurred approximately between  $1 \times 10^{-9} A$  and  $1 \times 10^{-8} A$  per tip.

Table 5.1 summarizes some of the major experimental results and calculated results of the four types of wafers described above.

From the table above we can see that the ratio of the two slopes in the Fowler-



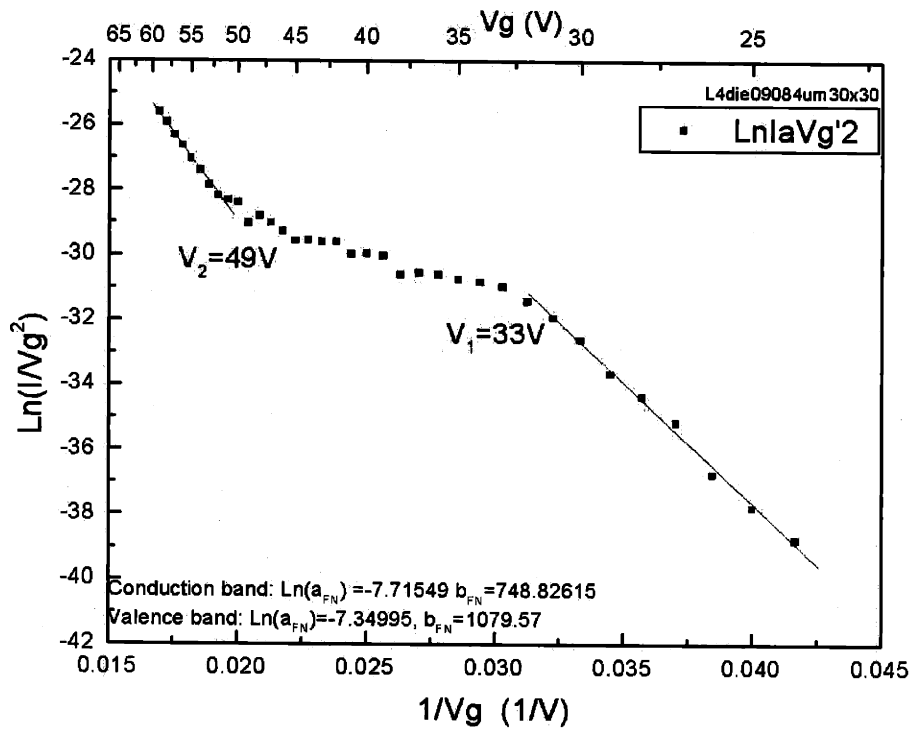


Figure 5-13: Two-band field emission from an n-type  $30 \times 30$  field emitter array with dopant concentration of about  $3.5 \times 10^{18} \text{cm}^{-3}$ . The ratio of the two slopes is about 1.44, and the ratio of the two corner voltages is about 1.48. The current saturated at about  $5 \times 10^{-10} \text{A}$  per tip.

Table 5.1: Summary of major experimental and calculated results from various substrate dopant concentration

Device Name	type	Dopant Concentration	Turn-on Voltage	$\beta \text{ (cm}^{-1}\text{)}$	$\frac{b_{FN,vb}}{b_{FN,cb}}$	$V_2/V_1$
L4die09084um30x30	n	$3.5 \times 10^{18} \text{cm}^{-3}$	18V	$7.10 \times 10^5$	1.44	1.48
L12die11074um30x30	n	$6 \times 10^{15} \text{cm}^{-3}$	42V	$4.46 \times 10^5$	1.487	1.59
L22die09074um60x60	n	$2 \times 10^{14} \text{cm}^{-3}$	33V	$4.91 \times 10^5$	1.50	1.52
R3die10074um20x20	p	$1 \times 10^{15} \text{cm}^{-3}$	30V	$7.84 \times 10^5$	1.389	1.44

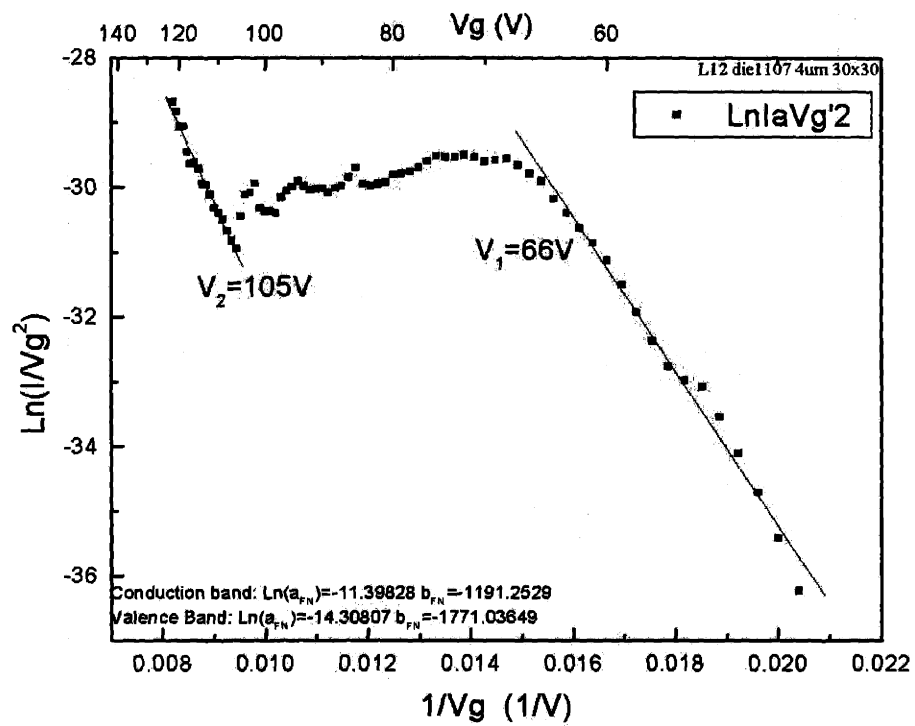


Figure 5-14: Two-band field emission from an n-type  $30 \times 30$  field emitter array with dopant concentration of about  $6 \times 10^{15} \text{ cm}^{-3}$ . The ratio of the two slopes is about 1.487, and the ratio of the two corner voltages is about 1.59. The current saturated at approximately  $1 \times 10^{-9} \text{ A}$  per tip.

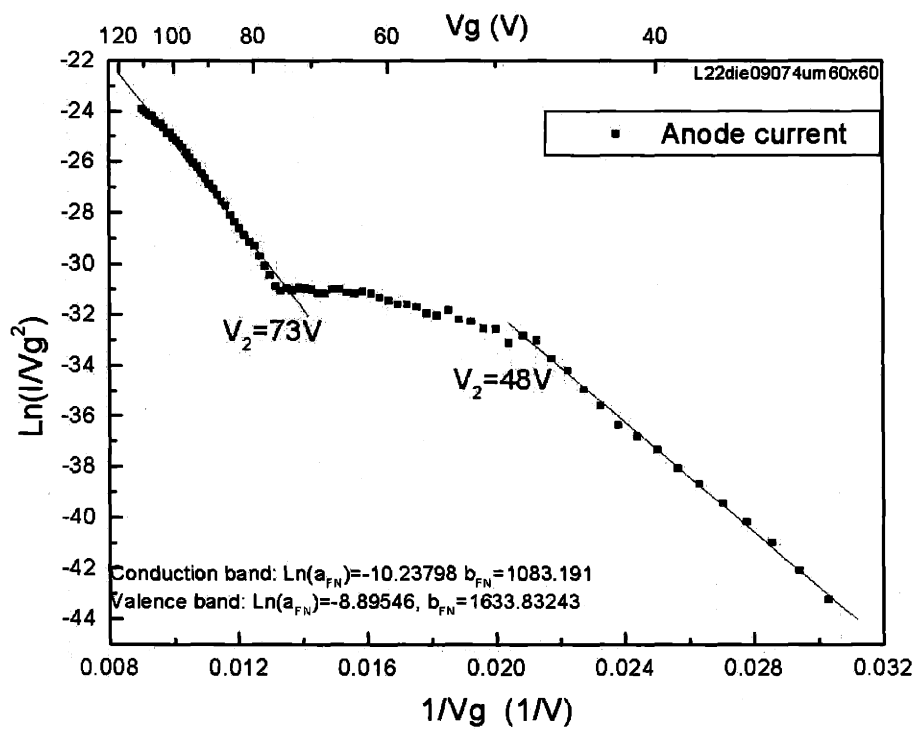


Figure 5-15: Two-band field emission from an n-type  $60 \times 60$  field emitter array with dopant concentration of about  $2 \times 10^{14} \text{ cm}^{-3}$ . The ratio of the two slopes is about 1.50, and the ratio of the two corner voltages is about 1.52. The current saturated at approximately  $5 \times 10^{-10} \text{ A}$  per tip.

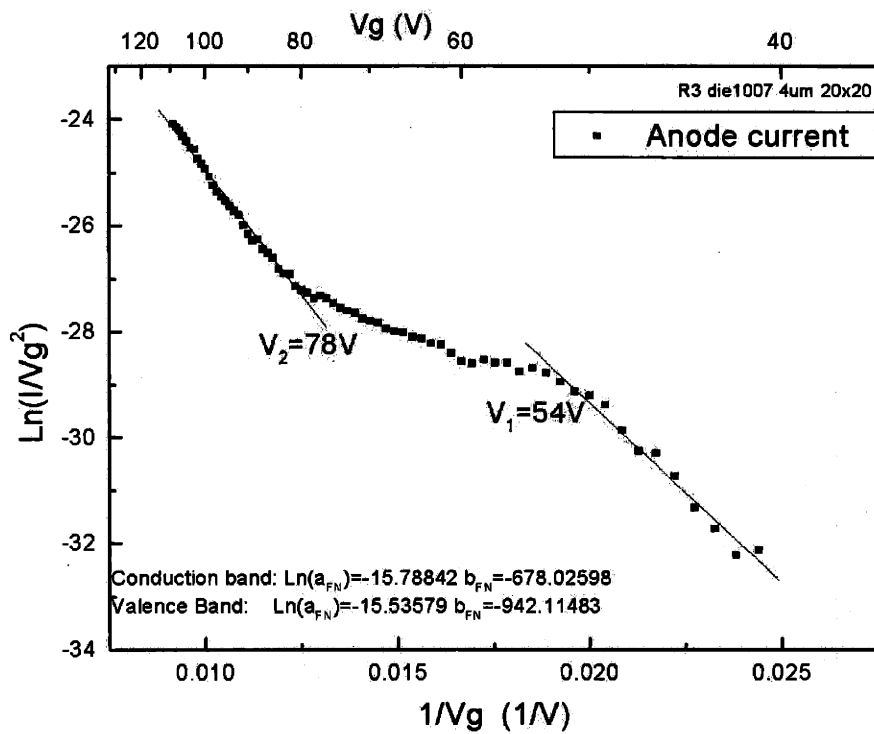


Figure 5-16: Two-band field emission from a p-type  $20 \times 20$  field emitter with dopant concentration of about  $1 \times 10^{15} \text{ cm}^{-3}$ . The ratio of the two slopes is about 1.389, and the ratio of the two corner voltages is about 1.44. The current saturated at approximately between  $1 \times 10^{-9} \text{ A}$  and  $1 \times 10^{-8} \text{ A}$  per tip.

Table 5.2: Summary of extracted parameters of devices with various substrate dopant concentrations

Device Name	type	Dopant Concentration	$r_{2D}$	$r$ from "ball in sphere"	$I_{sat,th}$
L4die09084um30×30	n	$3.5 \times 10^{18} cm^{-3}$	5.77nm	14.1nm	$5.85 \times 10^{-6}$ A
L12die11074um30×30	n	$6 \times 10^{15} cm^{-3}$	11.3nm	22.4nm	$3.85 \times 10^{-8}$ A
L22die09074um60×60	n	$2 \times 10^{14} cm^{-3}$	9.84nm	20.4nm	$9.73 \times 10^{-10}$ A
R3die10074um20×20	p	$1 \times 10^{15} cm^{-3}$	5.0nm	12.8nm	$1.25 \times 10^{-9}$ A

Nordheim plot in these four devices, the most compelling evidence indicating that the data are showing electron field emission from both conduction band and valence band, are all near the vicinity of the theoretical value of  $(\frac{\chi+E_g}{\chi})^{3/2} = 1.45$ . These results confirmed and reassured our belief in the two-band field emission model presented above.

From the experimentally observed field factor  $\beta$ , the tip radius of these four particular emitter arrays can be extracted using either "ball in sphere" model or the 2-D numerical simulation method described in section 3.3.1. Using the extracted tip radius value from the 2-D numerical simulation method, the substrate dopant concentration, and equation 5.1 in our simple current saturation model, the theoretical values of saturation currents for the three n-type devices are calculated. These results are summarized in table 5.2. It is worth noting how the name of the device is constructed. Take *L4die09084um30×30* as an example: *L4* is the wafer name, *die0908* is the name of the die on the wafer according to its  $x$  and  $y$  coordinates; here the die has an  $x$  coordinate of 09 and a  $y$  coordinate of 08. *4um30×30* means the array is a  $30 \times 30$  array with a  $4\mu m$  pitch (the distance between neighboring emitters).

It is observed that for high dopant concentration, especially for the wafer with  $3.5 \times 10^{18} cm^{-3}$  dopant concentration, the theoretically calculated saturation currents deviates from the experimentally observed value. It indicated that at high dopant concentration our simple current saturation model presented in section 5.2.2 broke

Table 5.3: Summary of major experimental and calculated results from high aspect ratio field emission array.

$\beta$ ( $cm^{-1}$ )	$r_{2D}$	$r$ from "ball in sphere"	$\frac{b_{FN,vb}}{b_{FN,cb}}$	$V_2/V_1$	$I_{sat,th}$
$8.49 \times 10^5$	$1.561nm$	$11.77nm$	1.493	1.62	$1.22 \times 10^{-9}$ A

down. The mechanism of current saturation in high dopant concentration n-type field emitters is not well understood at this time.

### 5.2.6 Valence band emission from high aspect ratio field emitter arrays

We were also able to observe valence band emission from the high aspect ratio field emitter arrays. As noted in the previous chapter, the characterization of high aspect ratio devices has been relatively more difficult than the characterization of the regular devices, due to the non-optimized fabrication process. But with careful testing and data analysis valence band emission could still be observed.

Figure 5-17 is an example of this observation. The device is a  $30 \times 30$  n-type device with substrate dopant concentration of about  $1 \times 10^{16} cm^{-3}$ . The device turned on at  $30V$ . The ratio of the two Fowler-Nordheim slopes shown in the figure is  $\frac{935.74}{626.35} = 1.493$  and the ratio of the two corner (transition) voltages is  $\frac{65V}{40V} = 1.62$ . These two values are in agreement with the theoretically predicted value of 1.45 as shown in equation 5.9. The saturation current is around  $1 \times 10^{-10} A$  per tip.

Table 5.3 summarizes the major experimental and calculated results of this device, where the  $r_{2D}$  is obtained by applying equation 4.1.

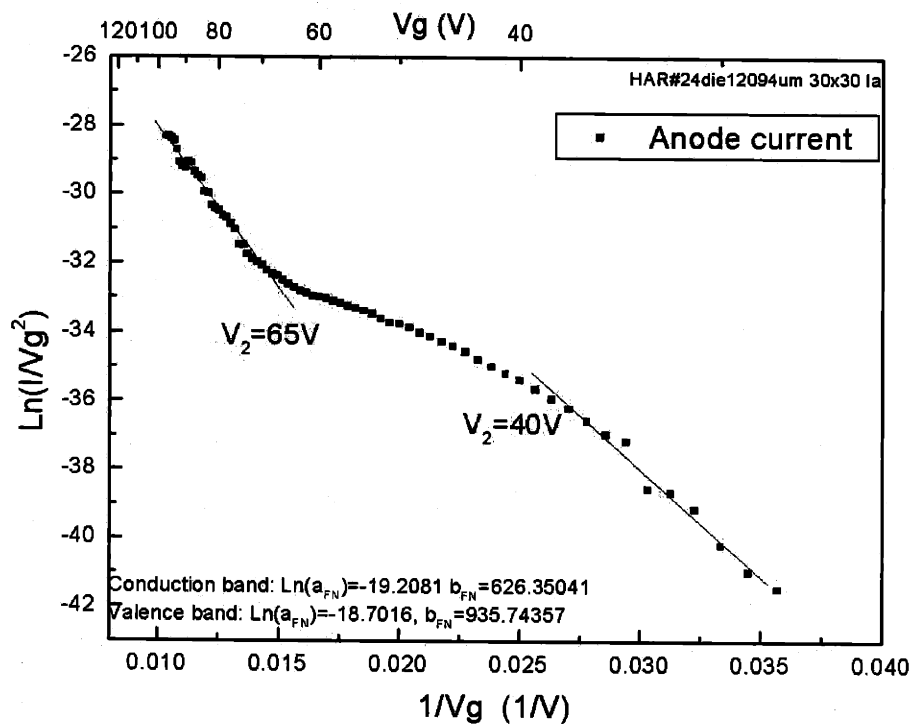


Figure 5-17: An example of the observation of field emission from the valence band in a  $30 \times 30$  high aspect ratio silicon field emitter array. The ratio of the two slopes is about 1.493, and the ratio of the two corner voltages is about 1.62. The current saturated at approximately  $1 \times 10^{-10}$  A per tip.

## 5.3 Summary

Nonlinear behavior of the Fowler-Nordheim plots of silicon field emitter arrays is reported. Three distinct regions of emission currents are observed. At low voltage most tunneling electrons come from the conduction band. At this stage the electron supply is sufficient and the device is in a quasi-static state. The current-voltage characteristic is in the electron transmission controlled region and obeys the Fowler-Nordheim formula. As the gate voltage increases, the emission current increases too because the electron transmission increases. At this stage, the emission is in a quasi-static state. At the intermediate voltage region current saturation is observed. We presented a simple supply channel model to account for the current saturation. The saturation is caused by the finite electron drift velocity in silicon: the saturation velocity, the finite carrier concentration, and the small dimension of the emitter tip radius:  $I_{sat} = \alpha' q n v_{sat}$ . At this stage, the emission is in a steady state, but not a quasi-static state. This very simplified model showed a limitation on applications, especially when the substrate dopant concentration was very high.

At higher gate voltages, a subsequent increase of current results in a second linear fit region on the Fowler-Nordheim plot. Valence band electron field emission together with conduction band electron emission are believed to represent this second linear fit. The two-band field emission is analogous to a tank-with-a-nozzle model. We fabricated silicon field emitter arrays of n-type and p-type and with different substrate dopant concentrations. All devices demonstrated valence band field emission. The slopes of the ratios of the two linear fit regions in the Fowler-Nordheim plots of all these devices agree with theoretical predicted value  $(\frac{\chi + E_g}{\chi})^{3/2} \approx 1.45$ , confirming the applicability of the two-band field emission model.



## Chapter 6

# Scanning Maxwell Stress Microscope

The property of field emission is mostly determined by two physical quantities: the surface barrier height (surface potential) and the barrier width. The surface barrier width at a certain external electric field is determined by the geometric shape of the field emitters, i.e. the topography of the emitter tip. It would be advantageous to be able to image the surface potential and the topography of the sample simultaneously. The construction of the Scanning Maxwell Stress Microscope (SMM) was initially motivated by this goal. This chapter will discuss the principles of operation of the SMM as well as the setup of SMM based on a commercially available Atomic Force Microscope (AFM). Results from imaging different materials using SMM will be presented and discussed.

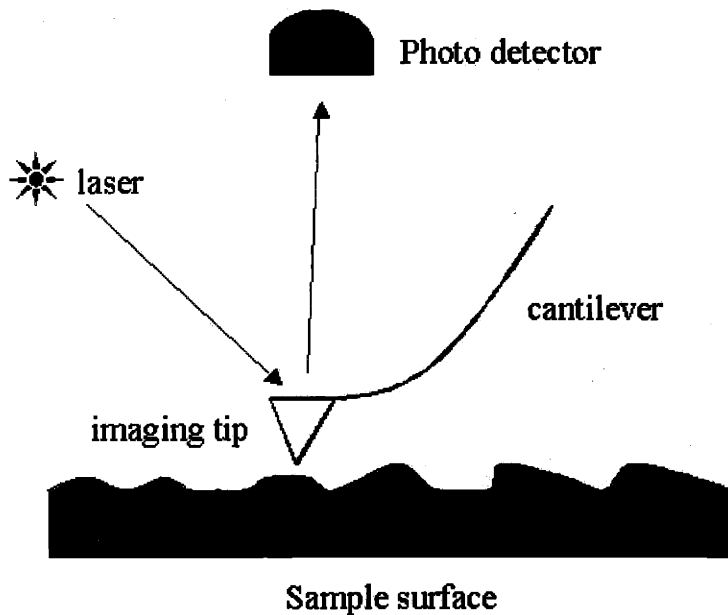


Figure 6-1: Schematic of an atomic force microscope. The cantilever and the imaging tip are the imaging components. The force between the tip and the sample surface deflects the cantilever and the change is detected by the deflection of the laser beam aimed upon the cantilever. The deflection of the laser beam is detected by the photo detector and the signal is transformed to information about the topography of the sample surface.

## 6.1 Principles of Scanning Maxwell Stress Microscope

The Scanning Maxwell Stress Microscope (SMM) is a variation of the scanning probe microscope (SPM), which is capable of imaging the surface potential and topography simultaneously. Typical SPM tools include the Scanning Tunneling Microscope (STM) and the Atomic Force Microscope (AFM) [146]. The Scanning Maxwell Stress Microscope is based on the Atomic Force Microscope. Figure 6-1 is a schematic of the AFM system.

The critical component of an AFM system is a cantilever with an imaging tip at one end of it. AFM has two basic operating modes: contact and non-contact. In the contact mode, the tip is touching the surface of the sample, and the force between

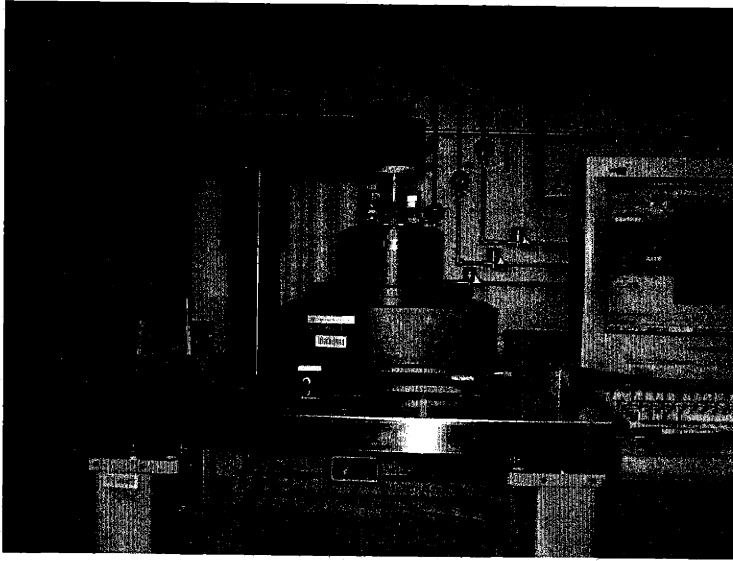


Figure 6-2: The AFM/STM system used in our lab. The whole microscope sits on a heavy air table. The computer on the right is connected to the output of the photo detector. Proprietary software is used to do data acquisition and image processing.

the tip and the sample is a mechanical force. In the non-contact mode, the cantilever oscillates near its resonance frequency, but the tip does not touch the sample surface, and the force between the tip and the sample is a van der Waals force and/or a magnetic force. In both modes, the force between the tip and the sample surface deflects the cantilever, and the change is detected by the deflection of the laser beam incident upon the cantilever. The deflection of the laser beam is detected by the photo detector and the signal is transformed into information about the topography of the sample surface. Due to the relatively large size of the tip ( $\sim 10 - 100nm$ ), the contact mode can not achieve atomic resolution. The non-contact mode is the typical way of achieving atomic resolution in atomic force microscopes.

Figure 6-2 is a digital picture of the AFM/STM system in our lab.

The Scanning Maxwell Stress Microscope is based on the non-contact mode of the AFM operation. In order for the SMM to work, the imaging tip and sample surface have to be electrically conductive. To operate the SMM, an alternating voltage  $V_{ac}(t)$  with frequency  $\omega_0$ , as well as a DC voltage  $V_{dc}$ , are applied to the imaging tip.

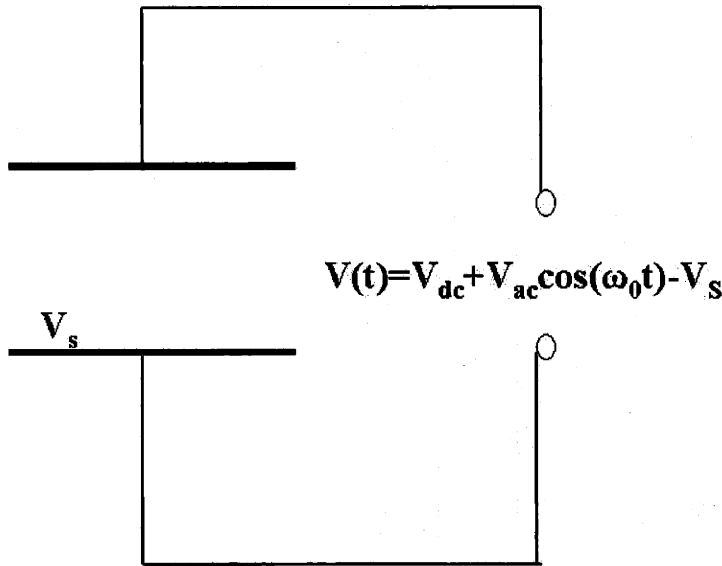


Figure 6-3: Parallel plate capacitor modeling of the tip-sample. The voltage difference between the two parallel plates is  $V(t) = V_{dc} + V_{ac} \cos(\omega_0 t) - V_s$ . The induced force between the tip and the sample surface has three components:  $F_{dc}$ ,  $F_{\omega_0}$ , and  $F_{2\omega_0}$ . The second harmonic component  $F_{2\omega_0}$  give us the topographic profile of the sample surface. The first harmonic component  $F_{\omega_0}$  maps the potential profile of the the sample surface.

The resultant forced oscillation of the tip is detected in the same manner as in the atomic force microscope (figure 6-1). The forced oscillation involves not only the fundamental but also the higher harmonics of the applied voltages, each carrying specific information about the electrical and topographical properties of the sample.

The electromagnetic force on the tip surface could be calculated in general ([63]) by equation:

$$F_\alpha = \oint_S \sum_\beta T_{\alpha\beta} n_\beta da \quad (6.1)$$

where  $\alpha = x, y, z$  represents the three coordinate directions,  $S$  represents the surface of the tip,  $\vec{n}$  is the outward normal unit vector to the tip surface  $S$ ,  $da$  is the differential area on the surface, and the *Maxwell stress tensor*  $T_{\alpha\beta}$  is defined as:

$$T_{\alpha\beta} = \frac{1}{\epsilon_0} [E_\alpha E_\beta + B_\alpha B_\beta - \frac{1}{2} (\vec{E} \cdot \vec{E} + \vec{B} \cdot \vec{B}) \delta_{\alpha\beta}] \quad (6.2)$$

where  $\vec{E}$  and  $\vec{B}$  are the electric and magnetic field respectively.  $\delta_{\alpha\beta} = 1$  when  $\alpha = \beta$ , and 0 otherwise.

The name Scanning Maxwell Stress Microscope follows the name of the Maxwell stress tensor.

In the absence of a magnetic field ( $\vec{B} = 0$ ) and in the case of a conductive surface, the above formula can be greatly simplified, owing to the absence of transverse field components on a conductive surface. In terms of the surface charge density  $\sigma_{t,r_s}$  at a point  $r_s$  on the tip at time  $t$ , we can write the force ([147]) as

$$F_z = \oint_S \frac{1}{2\epsilon_0} \sigma_{t,r_s}^2 dS_z. \quad (6.3)$$

The subscript  $z$  means that only the force in the  $z$  direction (the tip is either pulled down or pulled up) is considered.

For simplicity of the derivation, we model the tip-sample as a parallel plate capacitor. Figure 6-3 shows the schematic of the parallel capacitor. Assume that the sample surface has surface potential  $V_s$ . The applied voltage is  $V_{dc} + V_{ac} \cos(\omega_0 t)$ , so that the voltage difference between the the two parallel plates is

$$V(t) = V_{dc} + V_{ac} \cos(\omega_0 t) - V_s \quad (6.4)$$

Assuming  $C$  is the capacitance per unit area of the parallel capacitor, the surface charge density  $\sigma(t)$  induced at the surfaces of the two plates is

$$\sigma(t) = CV(t) = C(V_{dc} + V_{ac} \cos(\omega_0 t) - V_s). \quad (6.5)$$

The force between the two parallel plates  $F(t)$  is determined by

$$F(t) = E(t) \cdot \sigma(t) \quad (6.6)$$

where  $E(t)$  is the electrostatic field between the two plates. In a parallel plate geometry  $E(t) \approx \sigma(t)$  [63], giving rise to

$$\begin{aligned} F(t) &\approx \sigma(t)^2 \\ &= (C(V_{dc} + V_{ac} \cos(\omega_0 t) - V_s))^2 \\ &= C^2((V_{dc} - V_s)^2 + 2(V_{dc} - V_s)V_{ac} \cos(\omega_0 t) + V_{ac}^2 \cos^2(\omega_0 t)) \\ &= C^2(V_{dc} - V_s)^2 + 2C^2(V_{dc} - V_s)V_{ac} \cos(\omega_0 t) + C^2 V_{ac}^2 \left(\frac{1 + \cos(2\omega_0 t)}{2}\right) \\ &= C^2((V_{dc} - V_s)^2 + \frac{1}{2}V_{ac}^2) + 2C^2(V_{dc} - V_s)V_{ac} \cos(\omega_0 t) + \frac{1}{2}C^2 V_{ac}^2 \cos(2\omega_0 t) \\ &= F_{dc} + F_{\omega_0} + F_{2\omega_0} \end{aligned} \quad (6.7)$$

where

$$F_{dc} = C^2((V_{dc} - V_s)^2 + \frac{1}{2}V_{ac}^2) \quad (6.8)$$

$$F_{\omega_0} = 2C^2(V_{dc} - V_s)V_{ac} \cos(\omega_0 t) \quad (6.9)$$

$$F_{2\omega_0} = \frac{1}{2}C^2 V_{ac}^2 \cos(2\omega_0 t) \quad (6.10)$$

and  $\cos^2(\alpha) = \frac{1+\cos(\alpha)}{2}$ .

As we can see in equation 6.7, the induced force has three components: one DC component, one fundamental harmonic component  $F_{\omega_0}$  and one second harmonic component  $F_{2\omega_0}$ . The second harmonic component  $F_{2\omega_0}$  is dependent only on the capacitance  $C$  and  $V_{ac}$  which is a constant. The capacitance profile between the tip and sample surface is equivalent to the topography profile of the sample surface. The first harmonic component  $F_{\omega_0}$  is proportional to  $V_{dc} - V_s$ . During scanning,  $V_{dc}$  remains constant, so  $F_{\omega_0}$  maps the potential profile of the sample surface.

By using two lock-in amplifiers, we can accurately extract the first harmonic  $F_{\omega_0}$  and the second harmonic  $F_{2\omega_0}$  simultaneously, thus obtaining the surface potential and the topography information of the sample surface at the same time.

For more detailed derivation and discussion of the working principles of Scanning Maxwell Stress Microscopy please refer to [147, 148, 149, 150, 151, 152, 153].

## 6.2 Setup of the Scanning Maxwell Stress Microscope

We constructed the Scanning Maxwell Stress Microscope using a commercially available AFM system [154]. Figure 6-4 is the schematic of the microscope setup. The Lock-in amplifier [155] could also serve as a function generator. In fact, the alternating voltage  $V_{ac}$  we used is generated by Lock-in amplifier I. In the experiments, the two lock-in amplifiers are phase-locked together to ensure that they have the same phases. The signal access module is basically a signal pass-through box with a lot of test pins in it. When properly configured, the test pins serve as the output points of specific signals. In our experiments the output signal is the force between the tip and the sample surface. The signal access module only provides a signal access

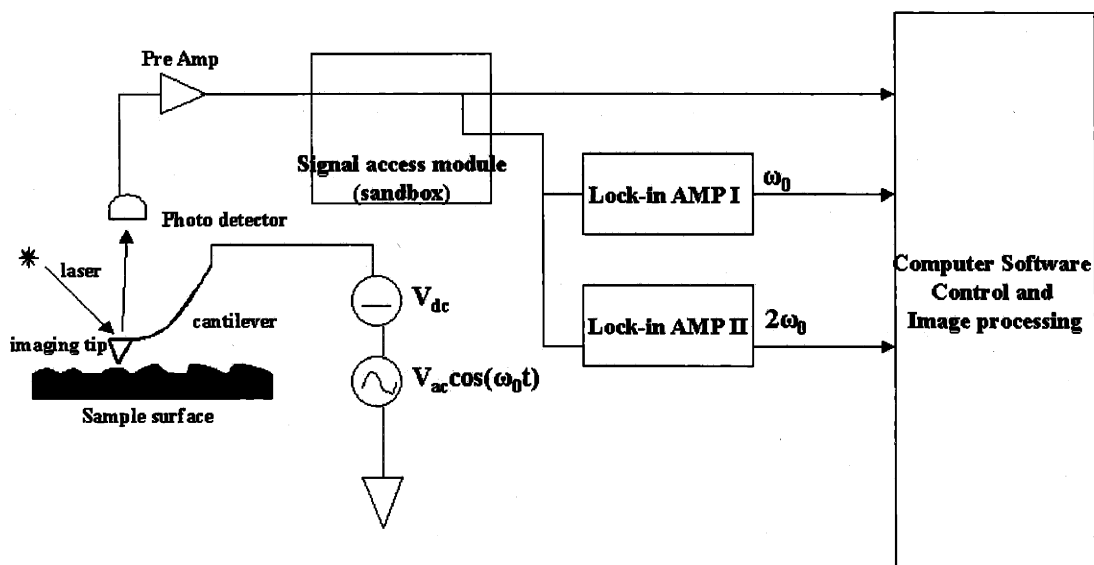


Figure 6-4: Schematic of the microscope setup. The alternating voltage  $V_{ac}$  is generated by Lock-in AMP I. Lock-in AMP I and Lock-in AMP II are phase-locked together to ensure that they have the same phase. The signal access module only provides a signal access point. Either we extract signal from it or not, the module will pass the signal directly to the controlling computer. In this sense, the setup of the SMM will not influence the normal operation of any AFM imaging.

point. Whether the signal is extracted from it or not, it will pass the signal directly to the controlling computer. In this sense, the setup of the SMM will not influence the normal operation of any AFM imaging.

### 6.3 Testing of the Scanning Maxwell Stress Microscope

Figure 6-5 shows the schematic of an integrated resistor. Figure 6-6 shows the Scanning Maxwell images of this integrated silicon resistor in a silicon substrate. The SMM operates at  $\omega_0 = 17kHz$ ,  $V_{dc} = 0$ , and  $V_{ac} = 1.0V$ .

Figure 6-6 (a) is the topography image taken from a normal AFM instrument in the non-contact scanning mode. Figure 6-6 (b) shows the first harmonic component



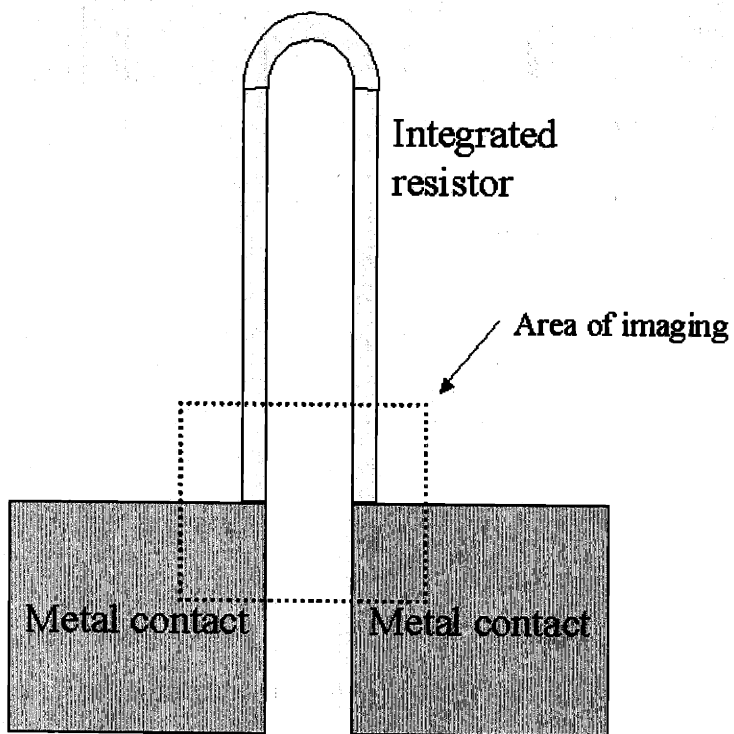
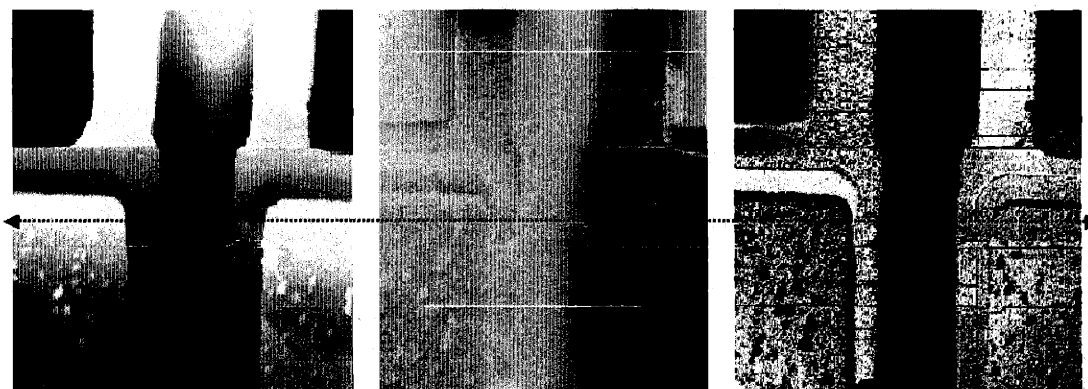


Figure 6-5: An inverse "U" shape integrated resistor on a silicon substrate. A voltage bias is applied through the two metal contact pads. The dashed line square indicates the imaging area.

## Integrated Resistor



a) AFM non-contact topography      b) First harmonic component of SMM      c) Second harmonic component of SMM

Figure 6-6: (a) Normal AFM non-contact mode topography image; (b) First harmonic component  $F_{\omega_0}$  of the cantilever deflection signal. ; (c) Second harmonic component  $F_{2\omega_0}$  of the cantilever deflection signal.

$F_{\omega_0}$  of the cantilever deflection signal. The two metal contacts are biased at  $0V$  and  $5V$ , respectively. We can see clearly the potential difference between the two metal contacts and the potential gradient along the left leg of the silicon resistor. Figure 6-6 (c) shows the second harmonic component  $F_{2\omega_0}$  of the cantilever deflection signal. It looks exactly like (even shows more details of the sample surface than) the topography images of the normal AFM topography scanning mode (figure 6-6 (a)). These three images are taken simultaneously and can be displayed on the same computer screen at the same time. Figure 6-7 shows the profile images of the cross-section, as illustrated by the dashed line in figure 6-6.

The surface potential result shown in figure 6-7 (b) can be used as a potential scale for subsequent SMM imaging measurements. In this case, the actually potential difference is known to be  $5V$  and the measured potential difference shown in figure 6-6 (b) is about  $105mV$ . So this gives a multiple factor of  $m = \frac{5}{0.105} = 47.62$  for future potential profile measurements. We will make use of this multiple factor in the next section.

## Integrated Resistor

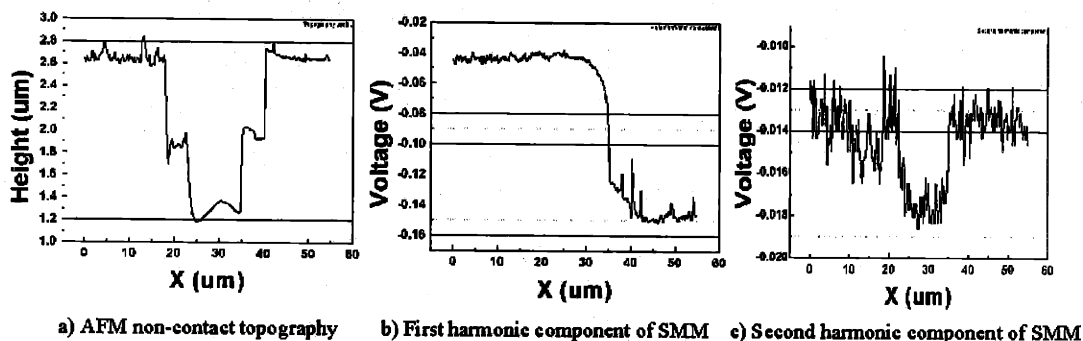


Figure 6-7: Cross-section profile of figure 6-6.

## 6.4 Imaging sample surfaces of different materials

### 6.4.1 Imaging aluminum, platinum, and gold pads on a silicon substrate

Aluminum and platinum thin film stripes of thickness of about  $3000\text{\AA}$  are formed on the surface of an n-type silicon substrate by e-beam deposition and photolithography. Gold thin film stripes of thickness of about  $1000\text{\AA}$  are formed on the surface of an n-type and a p-type silicon substrate by the same method. In order to avoid peeling of the platinum and gold thin film, very thin layers ( $50\text{\AA}$ ) of titanium and chromium were deposited first on the substrates, respectively, to increase the adhesion of the platinum and gold thin film to the silicon substrates.

Figure 6-8 shows a photo of these stripes under the AFM cantilever while figure 6-9 is an AFM non-contact image of the thin film stripes. A cross-section profile of this structure can be seen in figure 6-11 (a).

Figure 6-10 shows the SMM images of the aluminum stripes: (a) is the AFM non-contact mode topography image, (b) is the  $1\omega_0$  component from lock-in amplifier I, and (c) is the  $2\omega_0$  component from lock-in amplifier II. The SMM images were taken

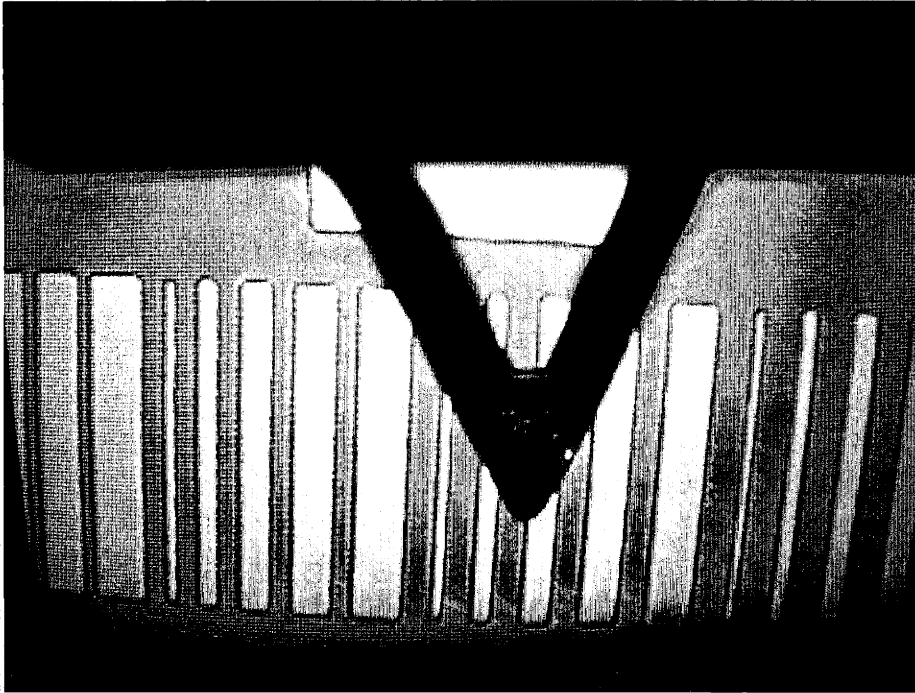


Figure 6-8: Photo of the thin film stripes under the AFM cantilever. The photo is taken from the TV screen. The light spot on the back of the cantilever is where the laser is incident.

at  $\omega_0 = 17kHz$ ,  $V_{dc} = 0$ , and  $V_{ac} = 2.0V$ . Figure 6-11 shows the profile images of the cross-section, as illustrated by the dashed line in figure 6-10. We argue that the relatively large noise in the  $1\omega_0$  and  $2\omega_0$  component imaging is caused by the closeness of the work functions of *Al* and n-type *Si*, making the two surfaces electrically difficult to distinguish from each other.

Figure 6-12 shows the SMM images of the platinum/titanium stripes with the same electrical parameters. Figure 6-13 shows the profile images of the cross-section, as illustrated by the dashed line in figure 6-12.

Figure 6-14 shows the SMM images of the gold/chromium stripes on a n-type silicon substrate with the same electrical parameters. Figure 6-15 shows the profile images of the cross-section, as illustrated by the dashed line in figure 6-14.

Figure 6-16 shows the SMM images of the gold/chromium stripes on a p-type silicon

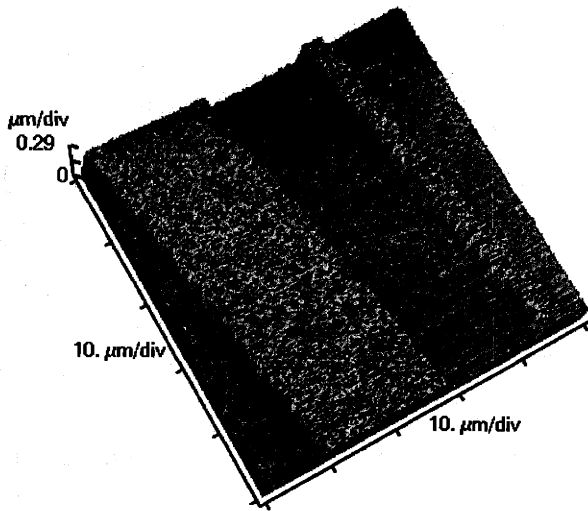


Figure 6-9: AFM non-contact image of thin film stripes. The elevated portion is the deposited *Al*, *Pt*, or *Au* stripe. In between the elevated portions is the silicon substrate.

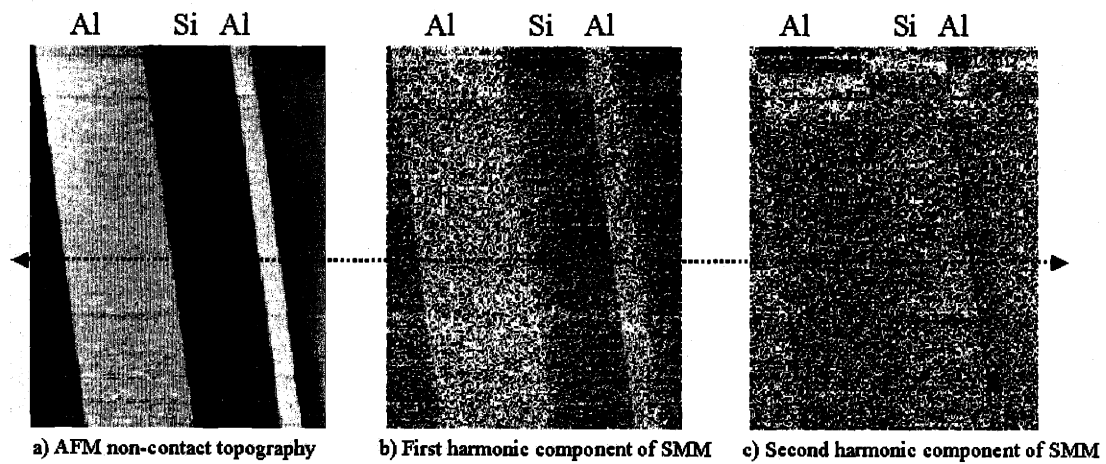


Figure 6-10: SMM images of the aluminum stripes in figure 6-9. (a) AFM non-contact mode topography image, (b)  $1\omega_0$  component from lock-in amplifier I, and (c)  $2\omega_0$  component from lock-in amplifier II.  $\omega_0 = 17kHz$ ,  $V_{dc} = 0$ , and  $V_{ac} = 2.0V$ .

### Al/Si Pad structure

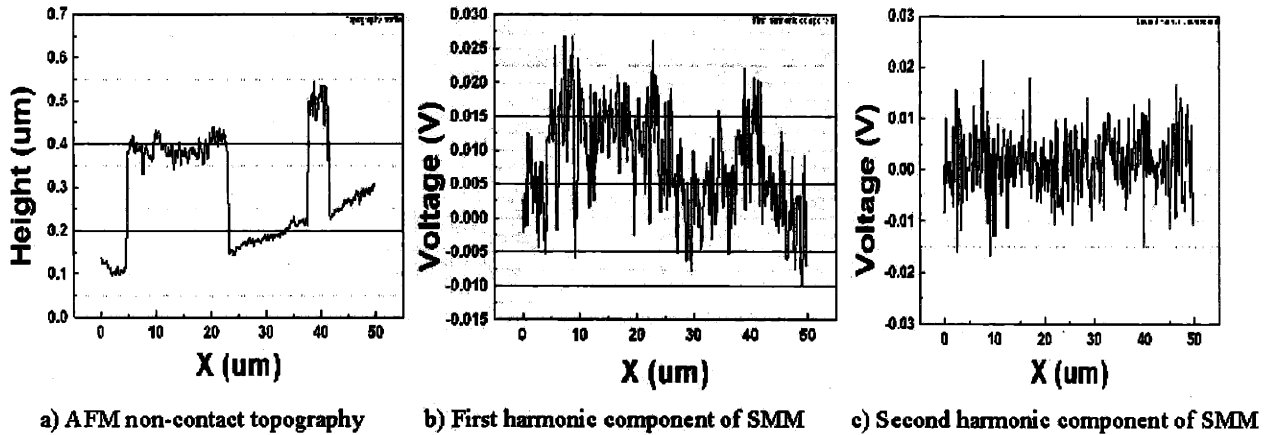


Figure 6-11: Cross-section profiles of figure 6-10. The relatively large noise in the  $1\omega_0$  and  $2\omega_0$  component imaging is caused by the closeness of the work functions of Al and n-type Si.

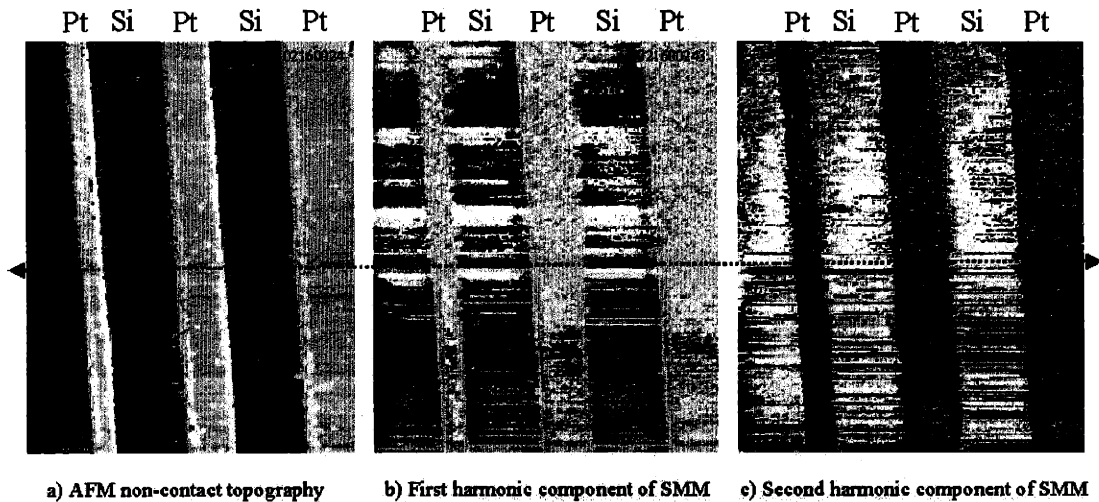


Figure 6-12: SMM images of the platinum/titanium stripes. (a) AFM non-contact mode topography image, (b)  $1\omega_0$  component from lock-in amplifier I, and (c)  $2\omega_0$  component from lock-in amplifier II.  $\omega_0 = 17kHz$ ,  $V_{dc} = 0$ , and  $V_{ac} = 2.0V$ .

### Pt/Si Pad Structure

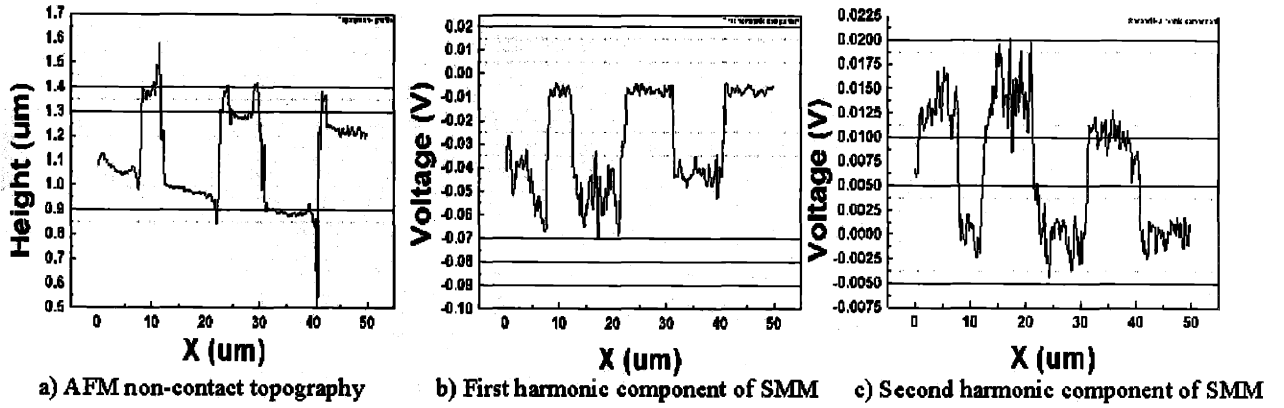


Figure 6-13: Cross-section profiles of figure 6-12.

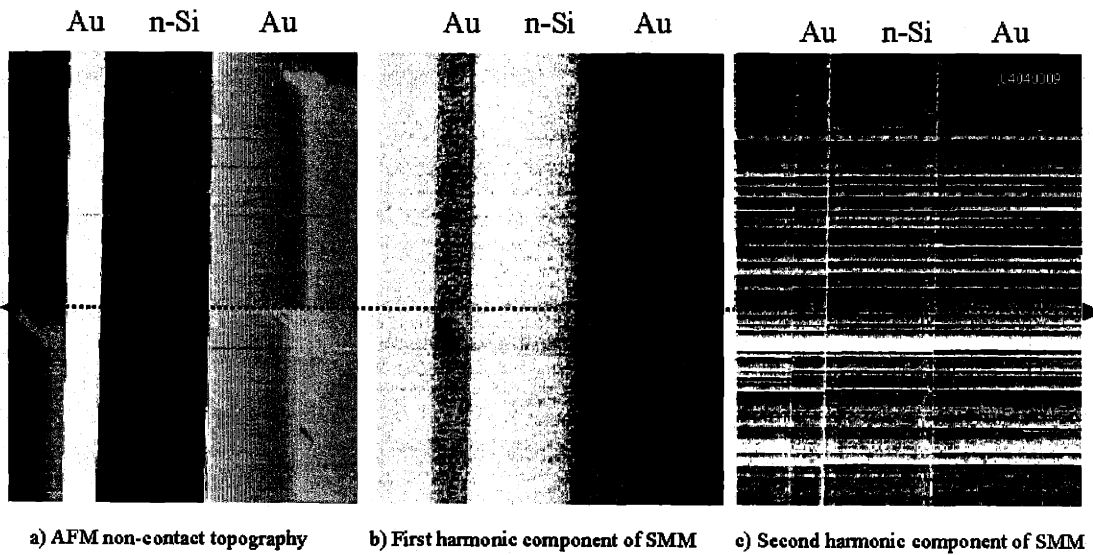


Figure 6-14: SMM images of the gold/chromium stripes on an n-type silicon substrate. (a) AFM non-contact mode topography image, (b)  $1\omega_0$  component from lock-in amplifier I, and (c)  $2\omega_0$  component from lock-in amplifier II.  $\omega_0 = 17kHz$ ,  $V_{dc} = 0$ , and  $V_{ac} = 2.0V$ .

## Au/n-Si Pad Structure

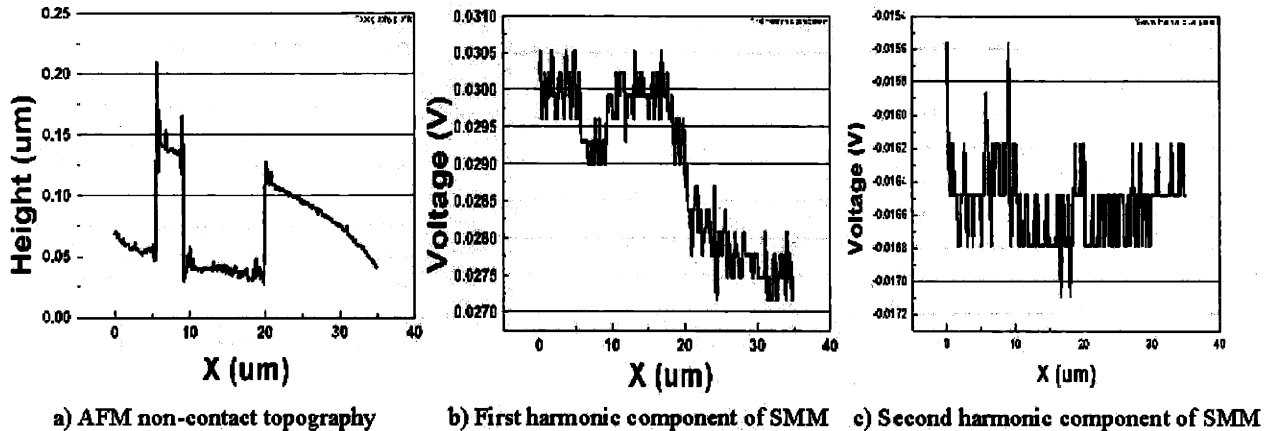


Figure 6-15: Cross-section profiles of figure 6-14.

substrate with the same electrical parameters. Figure 6-17 shows the profile images of the cross-section, as illustrated by the dashed line in figure 6-16.

From figures 6-10, figure 6-12, and figure 6-14 it is observed that the first harmonic signal ( $1\omega_0$ ) component could clearly distinguish between the metals (aluminum, platinum, or gold) and the n-type silicon substrate. This is because the two different materials have different surface potentials. However, in figure 6-16 it is observed that the first harmonic component can not very well distinguish the surface potential difference between the the gold and the p-type silicon substrate. The second harmonic signal ( $2\omega_0$ ) component reproduced the topography images with accuracy and had almost the same, if not better, transverse resolution. However, it is also observed that the second harmonic component has low resolution in the  $z$  direction.

From figure 6-11 (b), a nominal surface potential difference between the n-type silicon substrate and the aluminum pad can be estimated to be about  $12.5mV$ . With this value times the multiple factor discussed above, (since the data is taken at  $V_{ac} = 2.00V$  for the case of Al, the multiple factor needs to be reduced by half in this case) a real surface potential difference of  $0.298V$  is obtained.



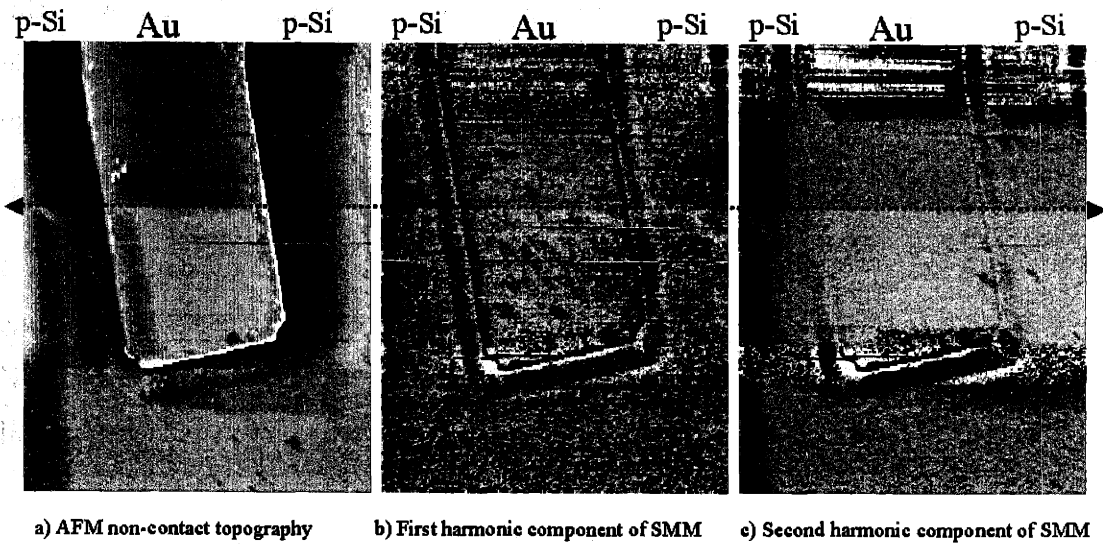


Figure 6-16: SMM images of the gold/chromium stripes on a p-type silicon substrate. (a) AFM non-contact mode topography image, (b)  $1\omega_0$  component from lock-in amplifier I, and (c)  $2\omega_0$  component from lock-in amplifier II.  $\omega_0 = 17\text{kHz}$ ,  $V_{dc} = 0$ , and  $V_{ac} = 2.0\text{V}$ .

### Au/p-Si Pad Structure

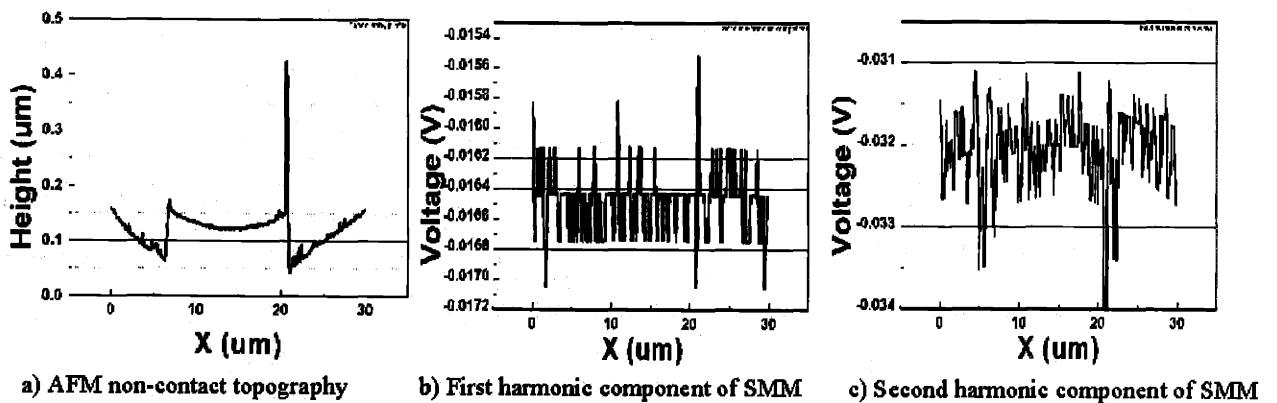


Figure 6-17: Cross-section profiles of figure 6-16.

From figure 6-13 (b), a nominal surface potential difference between the n-type silicon substrate and the platinum pad can be estimated to be about  $41.25mV$ . With this value times the multiple factor discussed above, (since the data is taken at  $V_{ac} = 2.00V$  for the case of Al, the multiple factor needs to be reduced by half in this case) a real surface potential difference of  $0.982V$  is obtained.

From figure 6-15 (b), a nominal surface potential difference between the n-type silicon substrate and the gold pad can be estimated to be about  $2.5mV$ . With this value times the multiple factor discussed above, (since the data is taken at  $V_{ac} = 2.00V$  for the case of Al, the multiple factor needs to be reduced by half in this case) a real surface potential difference of  $0.060V$  is obtained.

From figure 6-17 (b), the nominal surface potential difference between the p-type silicon substrate and the gold pad is indistinguishable and can be estimated to be about  $0mV$ . This also translates to a real surface potential difference of  $0V$ . That means the gold pad and the p-type silicon has almost the same workfunction.

The n-type silicon substrate has a dopant concentration of about  $1 \times 10^{16}cm^{-3}$ . This gives a potential difference of  $0.206eV$  between the electron affinity and the Fermi Level, which leads to the work function of the substrate being  $4.05eV + 0.206eV = 4.256eV$  [156]. The p-type silicon substrate has a dopant concentration of about  $5 \times 10^{19}cm^{-3}$ . This translates to a Fermi level  $0.036eV$  lower than the top of the valence band of the p-type silicon substrate, which leads to a work function of the p-type silicon of  $4.05eV + 1.124eV + 0.036eV = 5.21eV$  [156]. We assumed that these numbers are the correct work functions of the n-type and p-type silicon substrates. Based on the above SMM measurements, the work function of aluminum was calculated to be about  $4.55eV$ , and the work function of platinum was calculated to be about  $5.24eV$ . The work function of gold is calculated to be about  $4.32eV$  and  $5.21eV$ , based on the measurement on the n-type and p-type substrates, respectively. These values are consistent with the literature values of the work functions for aluminum ( $4.28eV$ ), platinum ( $5.65eV$ ), and gold ( $5.1eV$ ) [157]. The errors are 6.3% and -7.3%

Table 6.1: Summary of experimental results of metal pads on silicon substrates.

element name	work function measured	literature work function	discrepancy	percentage discrepancy
n-Si	4.256eV (assumed)			
p-Si	5.21eV (assumed)			
Al	4.55eV	4.28eV	0.27eV	6.3%
Pt	5.24eV	5.65eV	-0.41eV	-7.3%
Au(n-Si)	4.32eV	5.1eV	-0.78eV	-15.3%
Au(p-Si)	5.21eV	5.1eV	0.11eV	2.1%

for aluminum and platinum respectively. The error is about  $-15.3\%$  for gold on the n-type silicon substrate and is about  $2.1\%$  for gold on the p-type silicon substrate. The literature work functions of platinum or gold could also be taken as the reference point for the measurements. If we assume the work function of platinum to be  $5.65\text{eV}$ , the work function of n-type silicon can be calculated to be  $4.666\text{eV}$ . The selection of reference points would not change the characteristics of the measurements. Since all the samples are prepared based on silicon substrates we would stick to the selection of the silicon work function as the reference point. Table 6.1 summarizes the results from the pad measurements.

The error in the work function extracted from the gold on n-type silicon substrate sample is much larger ( $-15.3\%$ ) than that extracted from the p-type silicon substrate sample. One possible explanation for this difference is presented as follow. For lightly doped n-type silicon substrate, the existence of surface states could result in an additional internal barrier for the conduction band electrons [38, 39]. The conduction band near the surface will be bent while the Fermi Level remains constant across the solid. This could result in a larger difference between the Fermi Level and the bottom of the conduction band near the surface than that in the bulk of the silicon substrate. In turn, this will lead to a larger work function for n-type silicon substrate. We argue that this might be a possible explanation for the observation that there is only a small difference in work functions between the n-type silicon and the gold.

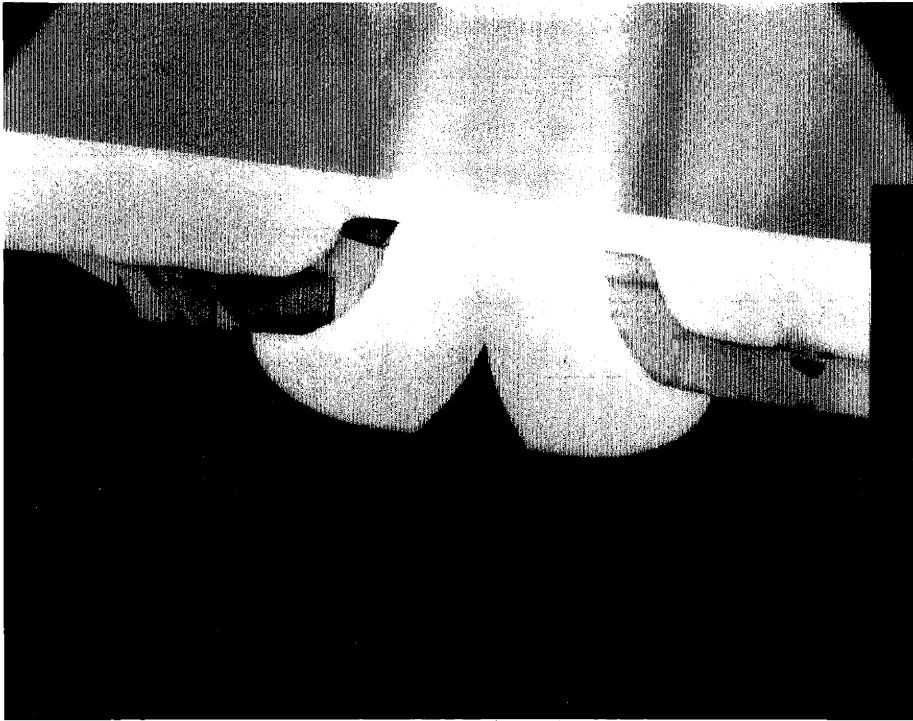


Figure 6-18: TEM cross section of a single gated emitter.

#### 6.4.2 Imaging a silicon field emitter with polycrystalline silicon gate

A silicon field emitter array with a polycrystalline silicon gate was also imaged using the Scanning Maxwell Stress Microscope. Figure 6-18 is a TEM cross section of a single such gated emitter and figure 6-19 is the non-contact AFM image of the array surface. A cross-section profile of this structure can be seen in figure 6-21 (a).

Figure 6-20 shows SMM images of the surface of a field emitter array with a polycrystalline silicon gate. (a) is the AFM non-contact mode topography image, (b) is the  $1\omega_0$  component, and (c) is the  $2\omega_0$  component. The SMM operates at  $\omega_0 = 17kHz$ ,  $V_{dc} = 0$ , and  $V_{ac} = 1.0V$ . The scanning rate is 1 line per second. Figure 6-21 shows the profile images of the cross-section, as illustrated by the dashed line in figure 6-20.

In figure 6-20 it is observed that the  $1\omega_0$  component (figure 6-20 (b)) diagram does

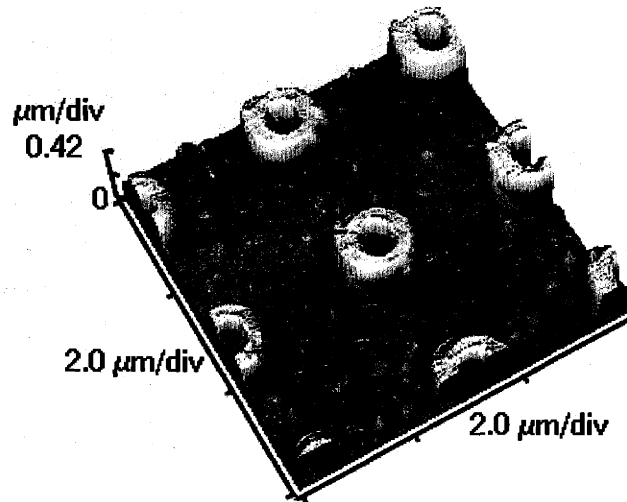


Figure 6-19: The non-contact mode AFM image of a field emitter array surface.

### Field Emitter Array with Polycrystalline Silicon Gate I

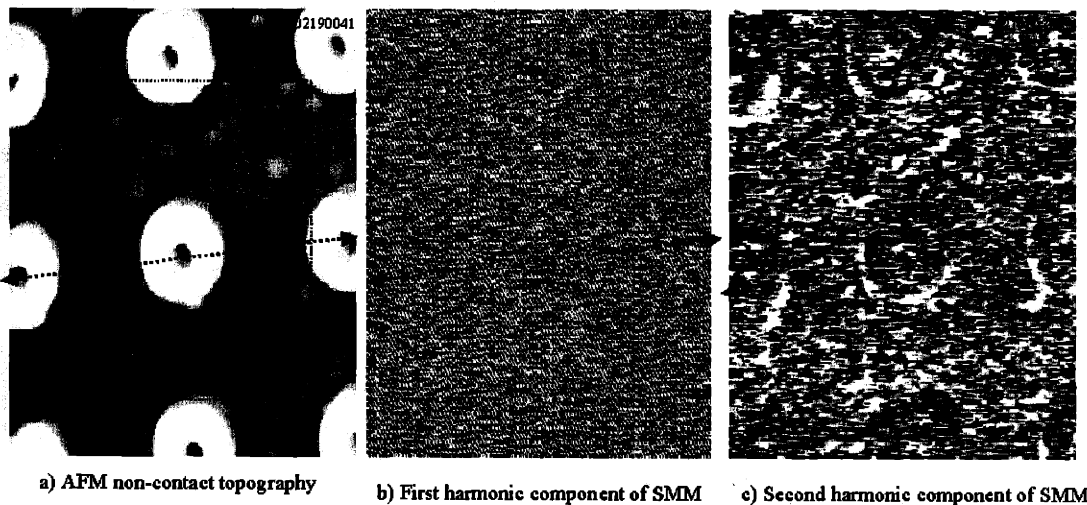


Figure 6-20: SMM images of the surface of a field emitter array with a polycrystalline silicon gate. (a) is the AFM non-contact mode topography image, (b) is the  $1\omega_0$  component from lock-in amplifier I, and (c) is the  $2\omega_0$  component from lock-in amplifier II. The SMM operates at  $\omega_0 = 17\text{kHz}$ ,  $V_{dc} = 0$ , and  $V_{ac} = 1.0\text{V}$ . The scanning rate is 1 line per second.

## Field Emitter Array with Polycrystalline Silicon Gate I

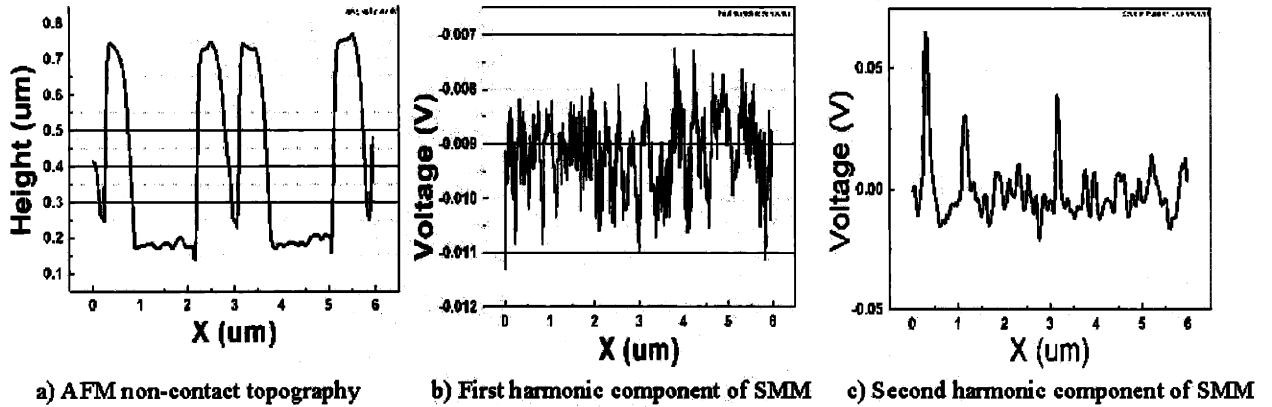


Figure 6-21: Cross-section profiles of figure 6-20.

not show any features on the sample surface. This is understandable because both the tip and gate have silicon surfaces and all the locations on the surface have almost the same surface potential. The  $2\omega_0$  component (figure 6-20 (c)) diagram has a topography that is similar to what is shown in figure 6-22 (a).

Figure 6-22 shows the SMM images of a selected portion of the same wafer surface as that in figure 6-20 (the dash-line rectangle in figure 6-20 is the selected region). The image is obtained at a much slower scanning rate of 0.1 line per second. The  $1\omega_0$  component showed some indication of the edges of the gate, but overall the diagram could not show features on the surface. What is quite striking is that the  $2\omega_0$  component actually revealed more details of the surface topography than the AFM non-contact mode image did as in figure 6-22. This result is consistent with the previous observation in figure 6-6 (c) of section 6.2 which revealed more details on the metal contact pad of the silicon integrated resistor. Figure 6-23 shows the profile images of the cross-section as illustrated by the dashed line in figure 6-22.

## Field Emitter Array with Polycrystalline Silicon Gate II

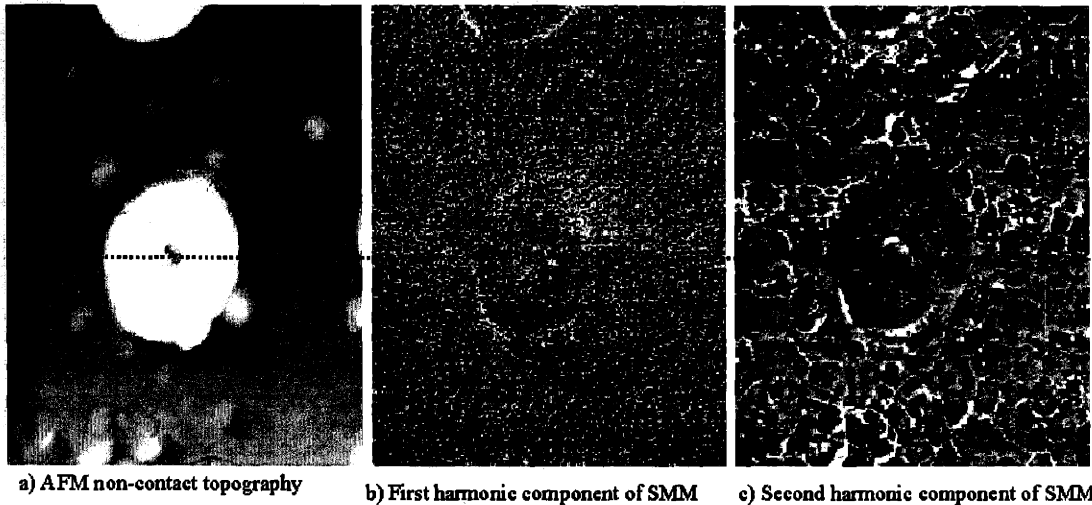


Figure 6-22: SMM images of the selected portion in figure 6-22 (a). a) AFM non-contact mode topography image, (b) the  $1\omega_0$  component, and (c) the  $2\omega_0$  component. The SMM operates at  $\omega_0 = 17kHz$ ,  $V_{dc} = 0$ , and  $V_{ac} = 1.0V$ . The scanning rate is 0.1 line per second.

## Field Emitter Array with Polycrystalline Silicon Gate II

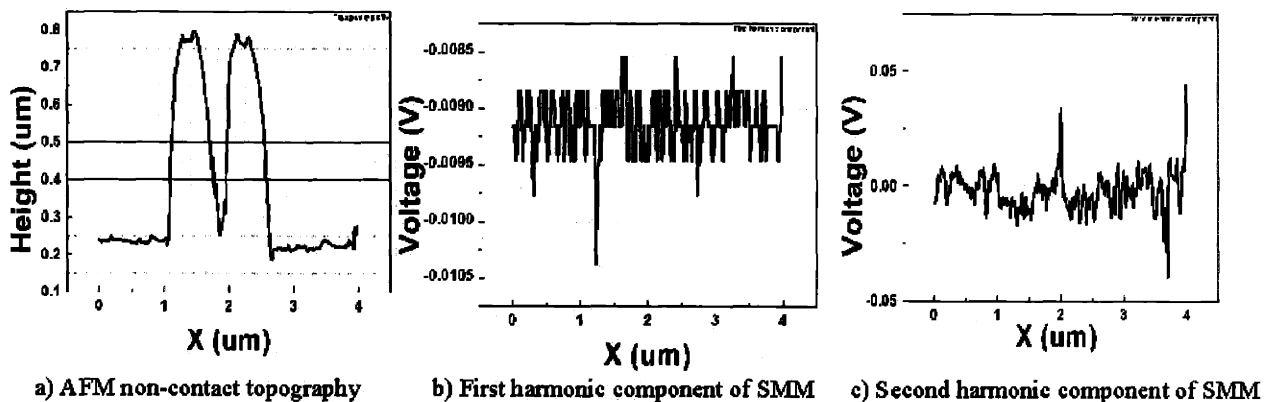


Figure 6-23: Cross-section profiles of figure 6-22.

## 6.5 Summary

A Scanning Maxwell Stress Microscope was successfully set up based on a commercially available Atomic Force Microscope. The microscope was successfully tested. Images taken on stripes of different metals (aluminum and platinum) and on field emitter array with a polycrystalline silicon gate showed that the first harmonic component of the SMM signal can clearly distinguish different materials on the sample surface, while the second harmonic component reproduces the topography of the surface accurately. It is also observed that the second harmonic component of the SMM signal has equal, if not better, transverse resolution compared with the AFM non-contact images. However, its vertical resolution in the  $z$  direction is not as good as that of the AFM non-contact mode. The measured work functions of aluminum and platinum determined from the first harmonic component of the SMM signal are consistent with the literature values of work functions. This set of Scanning Maxwell Stress Microscope was designed for ambient (air) operation. Efforts are underway to develop a Scanning Maxwell Stress Microscope for an ultra high vacuum.



# Chapter 7

## Thesis summary and recommendations for future works

### 7.1 Summary

Silicon emitter arrays attracted much attention in recent years because of their potential applications in many areas. This thesis work focuses on the experimental study of field emission from silicon, in terms of understanding the physics and advancing the technology.

We reported successful fabrication of  $\sim 1\mu m$  gate-aperture silicon field emitter arrays with a turn-on voltage as low as 14 V. The low turn-on voltage can ultimately allow integrating field emitter arrays with CMOS technology which will serve as electrical driver circuitry for various applications. The gate leakage current is observed to be less than 0.01% of the total emission current. Devices show excellent emission uniformity for different sized arrays. Transmission electron microscopy (TEM) pictures show that a tip radius as small as  $1 - 2nm$ , comparable to diameters of carbon nanotubes, could be obtained. It was achieved by isotropic etching of silicon and careful low

temperature oxidation sharpening of the emitter tips. Field emitters with a tip radius of about 10 nm could be routinely obtained. Optimization of the oxidation sharpening process should further reduce the tip radius and the operating voltage.

We also demonstrated the successful fabrication of the high aspect ratio silicon tip field emitter arrays. Silicon emitters as high as 5 – 6  $\mu\text{m}$  were fabricated in our facilities. High aspect ratio tips are not only useful in field emission applications, they could also be explored as imaging tips for an atomic force microscope, a writing head of atomic resolution information storage etc. Furthermore, we have also successfully fabricated and tested fully gated high aspect ratio field emitter arrays. The experimental current-voltage data agree well with the Fowler-Nordheim theory. The fabrication process is qualified.

We demonstrated electron field emission from both the conduction band and the valence band of n-type silicon simultaneously. We presented a two-band field emission model to explain the experimental data. Theoretical predictions for valence band emission were made in the past; however there was no conclusive data presented until now. We also reported the observation of previously theoretically predicted current saturation in n-type silicon field emitter arrays. A simple model is presented to account for the results. Current saturation is advantageous from a technological point of view in that a series current-limiting resistor would not be needed for stabilizing the field emission current.

Finally a Maxwell Stress Microscope, which is capable of imaging sample topography and surface potential simultaneously is set up for the purpose of further study of the properties of the surfaces of the silicon field emitters.

## 7.2 Recommendations for future work

The field emission process is a "violent" physical process. Because typically there are various adsorbants on the surface of solids, it is difficult to control the experiments and it is also difficult to obtain clean data. In order to verify other more subtle and delicate physical implications described by theory, we need to develop experimental and testing techniques that are able to control the emission process. Proposed measures include feeding hydrogen into the testing chamber to passivate the surface and get rid of native oxide on silicon surface.

The two most important steps in the fabrication process are the oxidation sharpening and the chemical mechanical polishing steps. The first one determines the sharpness of the emitter tip, thus to a large extent determining the performance of the emitter by influencing the turn-on voltage, current density, etc. The second one opens up the gate aperture and defines the opening of the aperture. In the process of fabricating our devices, it is observed that for both of these two steps, uniformity across the wafer is quite difficult to achieve. This might be due to the limited capability of the processing tools we have in our facility. However, fine tuning and careful control of the machine sometimes yield better results than on other occasions. In the future a careful and systematic study of the oxidation process and the chemical mechanical polishing process is necessary to guarantee the fabrication of high performance silicon field emitters.

The performance of the gated high aspect ratio emitters is less satisfactory than that of the regular field emitter arrays. This is partly due to the much more complicated fabrication process. Several process steps still need to be optimized in order to improve properties like turn-on voltage, current density and current uniformity.

The device breakdown is one of the major enemies of field emission devices and its potential for widespread application. Formerly the mechanism was believed to be the breakdown of the dielectric oxide. But our analysis indicates that the situation

is much more complicated in field emission devices than that in conventional CMOS devices. Further study of the breakdown mechanism is vital in developing useful field emission technologies.

Field emission is a surface physics phenomenon. With the Maxwell Stress Microscope set up, a tool is available for deeper study of the surface of the field emitters. Furthermore, a set up of a Maxwell Stress Microscope operational in high vacuum will be highly beneficial for this purpose.

### **7.3 Final words**

To look at it the simplest way, a field emitter is nothing but a microscopic cold electron source. It is exactly its “microscopic” and “cold” nature that make it a promising structure for many applications. The combination of the mature semiconductor processing technology and the great properties of silicon have brought silicon to the forefront of field emission applications. To understand the physics of electron field emission from silicon and to push technologies of making field emitter arrays present both opportunities and challenges. I hope this thesis work in some way contributed to this adventure.

# Appendix A

## Table of fundamental physical constants

Table A.1: Table of fundamental physical constants [118]

Physical constants	Symbol	Value	
		SI units	“microelectronic” units
Boltzman constant	$k$	$1.38 \times 10^{-23} J/K$	$8.62 \times 10^{-5} eV/K$
Electron charge	$q$	$1.60 \times 10^{-19} C$	$1.60 \times 10^{-19} C = 1e$
Electron rest mass	$m_0$	$9.11 \times 10^{-31} kg$	$5.69 \times 10^{-16} eV \cdot s^2/cm^2$
Planck constant	$h$	$6.63 \times 10^{-34} J \cdot s$	$4.14 \times 10^{-15} eV \cdot s$
Speed of light in vacuum	$c$	$3.00 \times 10^8 m/s$	$3.00 \times 10^{10} cm/s$
Permittivity of vacuum	$\epsilon_0$	$8.85 \times 10^{-12} F/m$	$8.85 \times 10^{-14} F/cm$

## Appendix B

### Table of important material parameters of Si and GaAs at 300K

The following table is quoted from reference [156]. The data of *GaAs* is for reference.

Table B.1: Table of Si and GaAs

Physical parameter	Symbol	Si value	GaAs value	units
lattice constant	$a$	0.543	0.565	$nm$
interatomic distance		0.235	0.245	$nm$
atomic density	$N_a$	$5.0 \times 10^{22}$	$4.4 \times 10^{22}$	$cm^{-3}$
density	$d$	2.33	5.32	$g \cdot cm^{-3}$
linear thermal expansion coefficient	$\alpha$	$2.59 \times 10^{-6}$	$5.73 \times 10^{-6}$	$K^{-1}$
dielectric constant	$\epsilon$	11.9	12.9	
electron affinity	$\chi$	4.04		$eV$
bandgap energy	$E_g$	1.124	1.422	$eV$
DOS electron effective mass	$m_{de}^*$	$1.09m_0$	$0.066m_0$	$eV \cdot s^2/cm^2$
DOS hole effective mass	$m_{dh}^*$	$1.15m_0$	$0.52m_0$	$eV \cdot s^2/cm^2$
effective density of the conduction band	$N_c$	$2.86 \times 10^{19}$	$4.21 \times 10^{17}$	$cm^{-3}$
effective density of the valence band	$N_v$	$3.10 \times 10^{19}$	$9.51 \times 10^{18}$	$cm^{-3}$
intrinsic carrier concentration	$n_i$	$1.07 \times 10^{10}$	$2.25 \times 10^6$	$cm^{-3}$
optical phonon energy	$E_{opt}$	0.063	0.035	$eV$
conductivity electron effective mass	$m_{ce}^*$	$0.28m_0$	$0.070m_0$	$eV \cdot s^2/cm^2$
conductivity hole effective mass	$m_{ch}^*$	$0.41m_0$	$0.44m_0$	$eV \cdot s^2/cm^2$
phonon-limited electron mobility	$\mu_e$	1430	8000	$cm^2/V \cdot s$
phonon-limited hole mobility	$\mu_h$	480	320	$cm^2/V \cdot s$
electron saturated drift velocity	$v_{esat}$			$cm/s$
hole saturated drift velocity	$v_{hsat}$			$cm/s$
optical G/R rate coefficient	$r_{rad}$	$2.0 \times 10^{-15}$	$7.2 \times 10^{-10}$	$cm^3/s$
electron-electron Auger coefficient	$r_{eeh}$	$1.8 \times 10^{-31}$	$1.8 \times 10^{-31}$	$cm^6/s$
hole-hole Auger coefficient	$r_{ehh}$	$9.5 \times 10^{-32}$	$4.0 \times 10^{-30}$	$cm^6/s$
impact ionization threshold energy	$E_{ii}$	1.12	1.72	$eV$

## Appendix C

### Table of important physical parameters of $SiO_2$



Table C.1: Silicon dioxide  $SiO_2$  properties

Physical parameter	value	units
Crystal structure	amorphous	for most VLSI applications
Atomic Weight	60.08	
Thermal Conductivity	0.014	$W/cm \cdot K$
Thermal diffusivity	0.006	$cm^2/s$
Relative Dielectric Constant	3.9	
Index of Refraction	1.46	
Dielectric Constant	$3.45 \times 10^{-11}$	$F/m$
Breakdown field	$6 \times 10^8$	$V/m$
Atomic Density	$2.27 \times 10^{22}$	$molecules/cm^3$
Density (dry oxide)	2.27	$g/cm^3$
Energy Gap	$\sim 9$	$eV$
Specific Heat	1.0	$J/g \cdot K$
Melting point	$\sim 1700$	deg
Coefficient of Thermal Expansion	$5 \times 10^{-7}$	$K^{-1}$ (lowest known material)
Electron affinity	1.0	$eV$

# Appendix D

## Fowler-Nordheim tunneling theory

### D.1 The supply function $N(W)$

The supply function  $N(W)$  is found from the equilibrium distribution formula for the electrons

$$dn = \frac{2v dp_x dp_y dp_z}{h^3 e^{\frac{\epsilon - \zeta}{kT} + 1}} \quad (\text{D.1})$$

where  $dn$  represents the number of electrons with  $x$ ,  $y$ , and  $z$  momentum components within intervals  $(p_x, p_x + dp_x)$ ,  $(p_y, p_y + dp_y)$ , and  $(p_z, p_z + dp_z)$ , respectively.  $v$  is the volume of the metal and  $h$  is Planck's constant.

The number of electrons per second per unit area moving in the  $x$ -direction and with  $x$ -momentum within  $dp_x$  is found by multiplying the number per unit volume with momenta within  $dp_x$  by the  $x$ -velocity and integrating over all  $p_y$  and  $p_z$ . The result is

$$\int_{p_y=-\infty}^{\infty} \int_{p_z=-\infty}^{\infty} \frac{p_x}{m} \frac{2}{h^3} \frac{dp_x dp_y dp_z}{e^{\frac{\varepsilon-\zeta}{kT}+1}} \quad (\text{D.2})$$

where  $\frac{p_x}{m}$  represents the  $x$  velocity of the electron. According to equation 2.22,  $p_x dp_x$  is equivalent to  $mdW$ . If this replacement is made, the quantity becomes the flux of electrons with  $x$ -energy within  $dW$  incident on the surface or, by definition,  $N(W)dW$ :

$$N(W)dW = \frac{2}{h^3} dW \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} \frac{dp_y dp_z}{e^{\frac{W-\zeta}{kT} + \frac{p_y^2 + p_z^2}{2mkT} + 1}} \quad (\text{D.3})$$

where equation 2.22 has been used to write  $\varepsilon$  in terms of  $W$  in the denominator. The double integral can be easily evaluated if polar coordinates are introduced

$$p_y = \rho \cos \theta \quad (\text{D.4})$$

$$p_z = \rho \sin \theta \quad (\text{D.5})$$

for then it is found that

$$\left. \begin{aligned} N(W) &= \frac{2}{h^3} \int_{\rho=0}^{\infty} \int_{\theta=0}^{2\pi} \frac{\rho d\rho d\theta}{e^{\frac{W-\zeta}{kT} + \frac{\rho^2}{2mkT} + 1}} \\ &= -\frac{4\pi mkT}{h^3} \ln\left(e^{\frac{W-\zeta}{kT}} + e^{-\frac{\rho^2}{2mkT}}\right) \Big|_{\rho=0}^{\rho=\infty} \\ &= -\frac{4\pi mkT}{h^3} (\ln(e^{\frac{W-\zeta}{kT}}) - \ln(e^{\frac{W-\zeta}{kT}} + 1)) \\ &= \frac{4\pi mkT}{h^3} \ln(1 + e^{-\frac{W-\zeta}{kT}}) \end{aligned} \right\} \quad (\text{D.6})$$

## D.2 The Transmission Coefficient $D(W)$

The transmission coefficient  $D(W)$  is to be found from a quantum mechanical discussion of the electrons incident on the barrier. Corresponding to the energy-momentum

connection of equation 2.22, the time-independent Schrödinger equation for the motion of one of the electrons in the  $x$  direction is

$$\frac{d^2u}{dx^2} + \frac{2m}{\hbar^2}(W - V(x))u = 0 \quad (\text{D.7})$$

where  $u(x)$  is the wave function and  $\hbar$  is  $\frac{h}{2\pi}$ . It would be awkward to carry through an exact solution of this equation, but the properties of the solutions can be studied easily in a WKB approximation [55, 56, 57]. In this approximation, the transmission coefficient is

$$D(W) = e^{-\int_{x_1}^{x_2} \sqrt{\frac{8m}{\hbar^2}(V(x)-W)} dx} \quad (\text{D.8})$$

where  $x_1$  and  $x_2$  are the zeros of the radicand, chosen so that  $x_1 < x_2$ . This formula is valid only when  $W$  is appreciably less than  $V_{max}$ ; this is the range required for field emission. Substituting for  $V(x)$  from equation 2.18 and evaluating the roots, one finds that

$$-\ln(D) = \int_{x_1}^{x_2} \sqrt{\frac{8m}{\hbar^2}(-eFx + |W| - \frac{e^2}{4x})} dx \quad (\text{D.9})$$

where

$$x_1 = \frac{|W|}{2eF} \left(1 - \sqrt{1 - \frac{e^3F}{W^2}}\right) \quad (\text{D.10})$$

$$x_2 = \frac{|W|}{2eF} \left(1 + \sqrt{1 - \frac{e^3F}{W^2}}\right) \quad (\text{D.11})$$

( $W$  is always negative). This integral was calculated by Nordheim [39]; his result

was improved by Burgess, Kroemer, and Houston [50]. The expression for the roots suggests introducing the parameter

$$y = \frac{\sqrt{e^3 F}}{|W|} \quad (\text{D.12})$$

and a new integration variable

$$\xi = \frac{2eF}{|W|} x \quad (\text{D.13})$$

so that

$$-\ln(D) = \frac{\sqrt{m|W|^3}}{\hbar e F} \int_{1-\sqrt{1-y^2}}^{1+\sqrt{1-y^2}} \sqrt{-\xi^2 + 2\xi - y^2} \frac{d\xi}{\sqrt{\xi}}. \quad (\text{D.14})$$

The substitution  $\eta = \sqrt{\xi}$  brings this to a standard form for an elliptic integral:

$$-\ln(D) = \frac{2\sqrt{m|W|^3}}{\hbar e F} \int_b^a \sqrt{(a^2 - \eta^2)(\eta^2 - b^2)} d\eta \quad (\text{D.15})$$

where

$$b = \sqrt{1 - \sqrt{1 - y^2}} \quad (\text{D.16})$$

$$a = \sqrt{1 + \sqrt{1 - y^2}}. \quad (\text{D.17})$$

An application of Byrd and Friedman's tables [51] yields

$$-\ln(D) = \frac{4\sqrt{m|W|^3}a}{3\hbar eF} \left[ \frac{(a^2 + b^2)}{2} E(k) - b^2 K(k) \right] \quad (\text{D.18})$$

where

$$k^2 = \frac{a^2 - b^2}{a^2} \quad (\text{D.19})$$

and  $K$  and  $E$  are the complete elliptic integrals of the first and second kinds:

$$K(k) = \int_0^{\pi/2} \frac{d\varphi}{\sqrt{1 - k^2 \sin^2 \varphi}} \quad (\text{D.20})$$

$$E(k) = \int_0^{\pi/2} \sqrt{1 - k^2 \sin^2 \varphi} d\varphi. \quad (\text{D.21})$$

Rewriting these equations in terms of the parameter  $y$ , one obtains finally for the transmission coefficient

$$D(W) = e^{-\frac{4\sqrt{2m|W|^3}}{3\hbar eF} v(y)} \quad (\text{D.22})$$

where

$$v(y) = 2^{-\frac{1}{2}} \sqrt{1 + \sqrt{1 - y^2}} E(k) - (1 - \sqrt{1 - y^2}) K(k) \quad (\text{D.23})$$

$$k^2 = \frac{2\sqrt{1 - y^2}}{1 + \sqrt{1 - y^2}} \quad (\text{D.24})$$

$$y = \frac{\sqrt{e^3 F}}{|W|} \quad (\text{D.25})$$

The function  $v(y)$  has been evaluated from representative values of  $y$  by Burgess, Kroemer, and Houston [50] as shown in Table D.1.

### **D.3 Some numerical values related to the Fowler-Nordheim formula**

Some numerical values of various functions related to the Fowler-Nordheim formula are given below in table D.1 and D.2.

Table D.1: Values of the functions  $v(y)$  and  $t(y)$  defined by equation 2.31, equation D.24, and equation 2.36

$y$	$v(y)$	$t(y)$
0	1.0000	1.0000
0.05	0.9948	1.0011
0.1	0.9817	1.0036
0.15	0.9622	1.0070
0.2	0.9370	1.0111
0.25	0.9068	1.0157
0.3	0.8718	1.0207
0.35	0.8323	1.0262
0.4	0.7888	1.0319
0.45	0.7413	1.0378
0.5	0.6900	1.0439
0.55	0.6351	1.0502
0.6	0.5768	1.0565
0.65	0.5152	1.0631
0.7	0.4504	1.0697
0.75	0.3825	1.0765
0.8	0.3117	1.0832
0.85	0.2379	1.0900
0.9	0.1613	1.0969
0.95	0.0820	1.1037
1	0	1.1107

Table D.2: Common logarithm of the current density  $j$  in  $amp/cm^2$  for various values of the work function  $\varphi$  in e-volts and the electric field  $F$  in volts/cm according to equation 2.44

$\varphi = 2.0$		$\varphi = 4.5$		$\varphi = 6.3$	
$F$	$\lg(j)$	$F$	$\lg(j)$	$F$	$\lg(j)$
$1.0 \times 10^7$	2.98	$2.0 \times 10^7$	-3.33	$2.0 \times 10^7$	-12.9
1.2	4.45	3.0	1.57	4.0	-0.88
1.4	5.49	4.0	4.06	6.0	3.25
1.6	6.27	5.0	5.59	8.0	5.34
1.8	6.89	6.0	6.62	10.0	6.66
2.0	7.40	7.0	7.36	12.0	7.52
2.2	7.82	8.0	7.94	14.0	8.16
2.4	8.16	9.0	8.39	16.0	8.65
2.6	8.45	10.0	8.76	18.0	9.04
		12.0	9.32	20.0	9.36



# Appendix E

## The surface electron accumulation layer

Let us assume that  $V(x)$  represents the bottom of the conduction band energy along the  $x$  direction. In figure 2-13 we take  $V_0 = V(0)$ .

If the Fermi statistics are valid, that is, when  $\mu - V(x)$  is positive, the chemical potential is given by, assuming a local free electron gas model, [46, 47]

$$\mu = cn^{\frac{2}{3}} + V \quad (\text{E.1})$$

where

$$c = \frac{\hbar^2}{8m} (3/\pi)^{\frac{2}{3}}. \quad (\text{E.2})$$

This treatment could be found in Kittel's book *Introduction to Solid State Physics* [47]. So the concentration of electrons is given by

$$n = (\mu - V)^{\frac{3}{2}} c^{-\frac{3}{2}}. \quad (\text{E.3})$$

Since the electrical potential is  $-V/e$ , the Poisson equation becomes

$$-\frac{d^2V}{dx^2} = \frac{4\pi ne^2}{\epsilon} \quad (\text{E.4})$$

which can be written as

$$\frac{d^2U}{dx^2} = \frac{4\pi e^2 U^{\frac{3}{2}}}{\epsilon c^{\frac{3}{2}}} = aU^{\frac{3}{2}} \quad (\text{E.5})$$

where

$$U = \mu - V \quad (\text{E.6})$$

and

$$a = \frac{4\pi e^2}{\epsilon c^{\frac{3}{2}}}. \quad (\text{E.7})$$

Introduction of the new variable  $p = dV/dx$  transforms the equation to

$$p \frac{dp}{dU} = aU^{\frac{3}{2}} \quad (\text{E.8})$$

which has the solution

$$p^2 = \frac{4}{5}aU^{\frac{5}{2}} + b \quad (\text{E.9})$$

where  $b$  is a constant. If the Fermi level lies close to the bottom of the undeformed conduction band, the field  $p/e$  will be small at the point where  $U = 0$ , so that  $b \cong 0$ . At the surface,

$$p_0 = \frac{eF}{\epsilon} \quad (\text{E.10})$$

so that

$$\frac{F^2 e^2}{\epsilon^2} = \frac{4}{5}aU_0^{\frac{5}{2}} \quad (\text{E.11})$$

or

$$U_0 = \mu - V_0 = \nu F^{\frac{4}{5}} \quad (\text{E.12})$$

where

$$\nu = 4.5 \times 10^{-7} \epsilon^{-\frac{2}{5}} \quad (\text{E.13})$$

for  $F$  in  $V/cm$  and the energies are in  $eV$ . So the quantity  $\nu F^{\frac{4}{5}}$  needs to be subtracted from  $\chi$  to get the new barrier height in using the Fowler-Nordheim equation.

# Appendix F

## Other field emitter structures

### F.1 The ridge type emitter and thin film emitter

In addition to the cone emitter, there are a few other types of emitter structures. Figure F-1 and figure F-2 are, respectively, the schematics of a ridge emitter and a thin-film edge emitter.

The thin-film edge emitter is a lateral device fabricated by surface micro-machining techniques. With a deflection electrode, the emitted electron beam can be deflected into the vertical direction. This device has proved to be a good candidate for a back-lighting lamp for Liquid Crystal Displays (LCDs) [10, 92].

### F.2 Field emitter with focusing electrode

In the cone shape emitter, the emitted electron beam diverges from the cone axis as the electrons move towards the anode because of their off-axis velocity on leaving the gate region. In this case, an additional electrode, the focusing electrode, can be

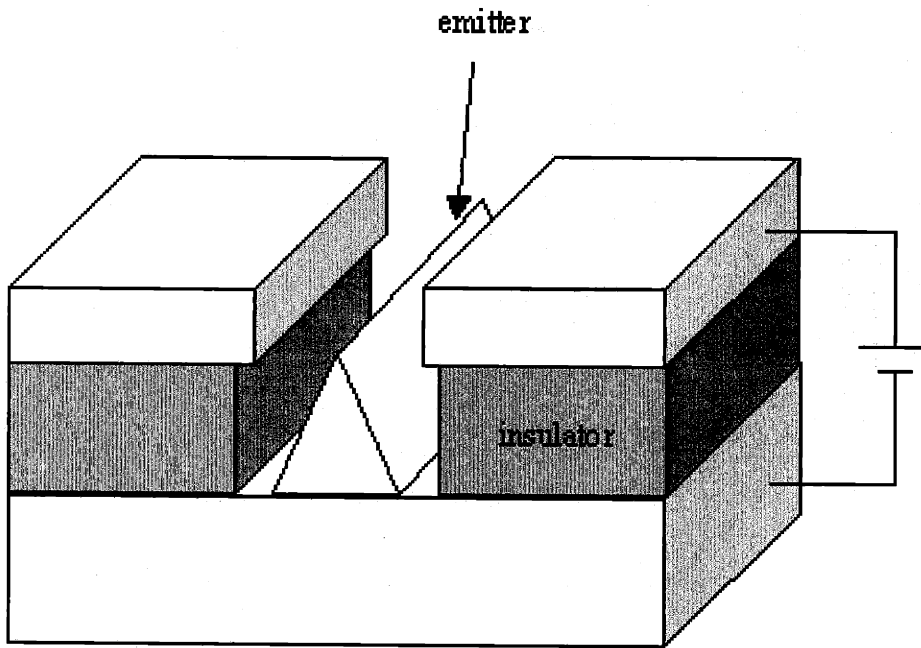


Figure F-1: Schematic of a ridge emitter.

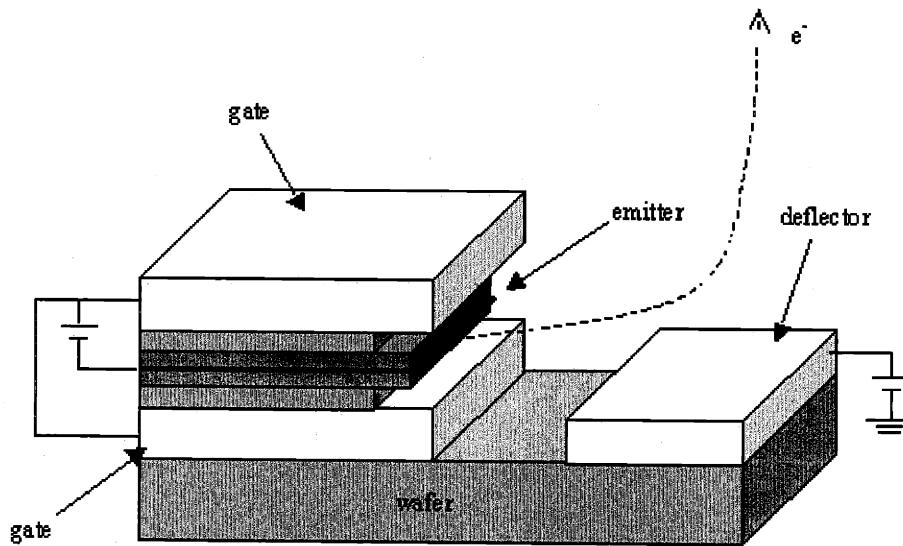


Figure F-2: Schematic of a thin-film emitter.

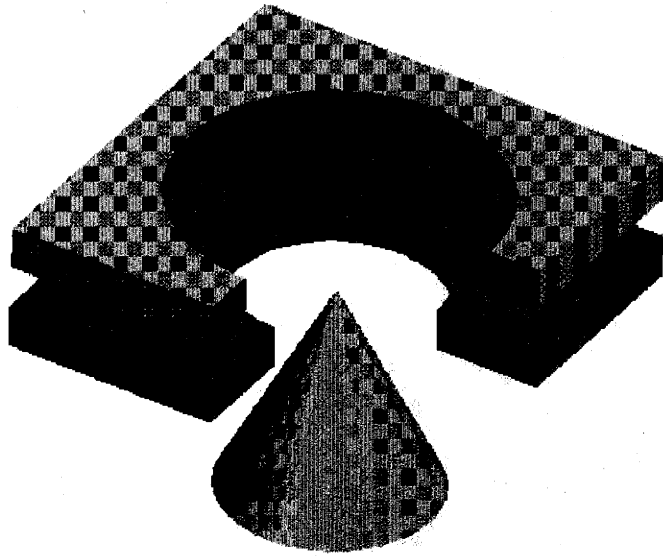


Figure F-3: Schematic of an emitter with an extracting gate electrode as well as a focusing electrode.

used between the gate and the anode. The focusing electrode, which is biased at a lower voltage than the gate, repels electrons towards the cone axis, thus making them converge [91, 93, 94]. Figure F-3 shows a schematic of an emitter with an extracting gate electrode as well as a focusing electrode.

### F.3 Field enhancement of ridge type emitter

A good model for the geometrical effects on field enhancement of the ridge type field emitter, shown in figure F-1, is the coaxial cylinder model, shown in figure F-4.

The interior cylinder is analogous to the cone ridge and the outer cylinder is analogous to the gate structure. The coaxial cylinder model can be solved analytically in cylindrical coordinates [64]. The solution gives the field at the surface of the cone ridge to be

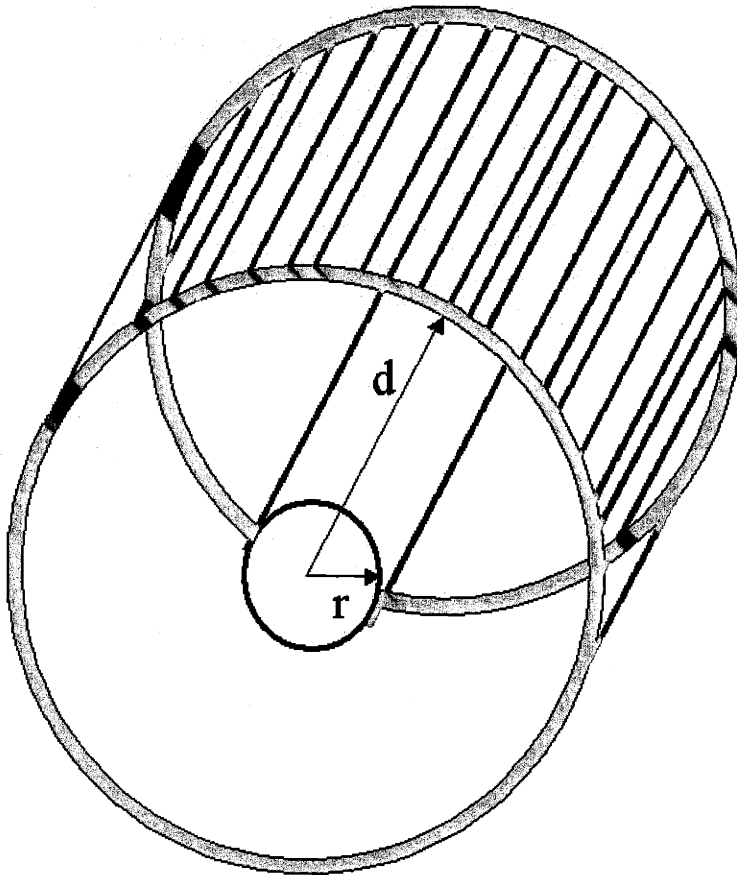


Figure F-4: "Coaxial cylinder" model. A solution to Laplace's equation in cylindrical coordinates gives the electric field at the ball's surface to be  $F = -\beta V_g = -V_g \frac{1}{r \ln(\frac{r+d}{r})}$ , where  $\beta = |F/V_g| = \frac{1}{r \ln(\frac{r+d}{r})}$  is the field factor.

$$\begin{aligned}
 F &= -V_g \frac{1}{r \ln(\frac{r+d}{r})} \\
 &= -\beta V_g
 \end{aligned}
 \tag{F.1}$$

with

$$\beta = \frac{1}{r \ln(\frac{r+d}{r})}.
 \tag{F.2}$$

The field factor associated with the "coaxial cylinder" model is less than the field factor associated with the "ball in a sphere" model. This is the reason that ridge like

structures are less useful for low voltage field emission display applications.



## Appendix G

# Liquid Crystal Display and Plasma Display

There are several other dominant display technologies available currently. [1, 4, 5, 6, 7, 8]. They include: liquid crystal displays, plasma displays, electro-luminescent displays, vacuum fluorescent displays etc. A detailed comparison of all the major currently available display technologies is presented in reference [9, 92]. We will talk about two of them: liquid crystal and plasma displays briefly.

### G.1 Liquid crystal displays

The Liquid crystal display (LCD) is the most dominant flat-panel display technology as of today. It represent over 90% of the overall flat-panel display market worldwide.

Liquid crystal display technology use addressable “light valves” to modulate the color/gray-scale of an image. The light valves consist of layers of a rear polarizer, an ITO pixel electrode, a polarizable liquid-crystal material, filters, color filters, and a front polarizer. The layer of the “light valve” is on top of a back-light/diffuser, as

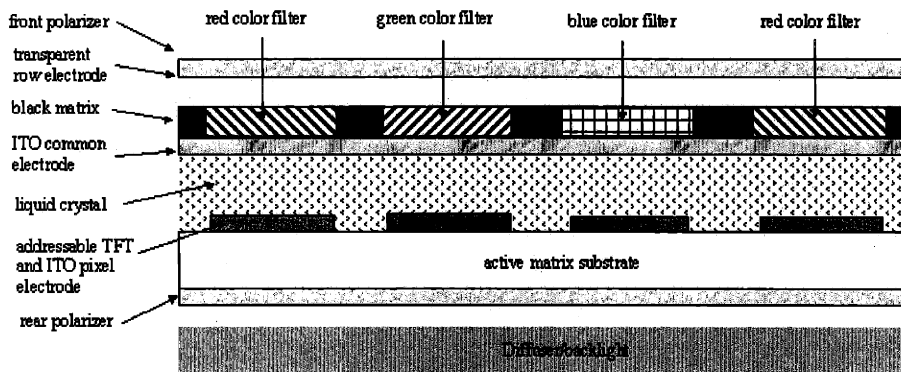


Figure G-1: Schematic of an active matrix liquid crystal display (AMLCD).

shown in figure G-1. An electric field across the liquid-crystal material can rotate the orientation of the molecules in the liquid crystal. The intensity of the light allowed through the liquid crystal is based on the rotational angle of the liquid crystal. The absence or presence of the field at any particular point of the liquid crystal layer determines whether and how much light passes through the "light valve" at that point. In a typical back-lighted LCD, only about 5 % of the original light intensity actually reaches the screen. Active-matrix liquid-crystal displays (AMLCD) improve the performance (dynamic range and non-linear response) by using a transistor on each pixel, see Figure G-1.

LCD technology still has many disadvantages:

- The requirement of a uniform and controlled light source (back-light)
- The low transmission of the "light valve" results in inefficiency in power consumption in portable systems.
- Slow refresh rate due to slow response of the liquid crystal
- Sensitivity to temperature and pressure

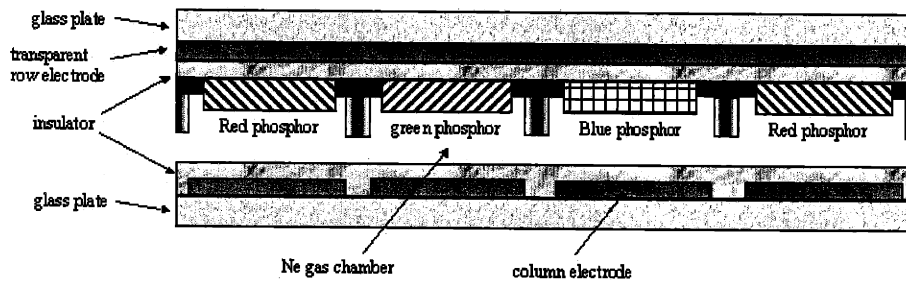


Figure G-2: Schematic of a plasma display.

## G.2 Plasma Display

A plasma display panel is a two-dimensional array of tiny neon lamps. Light is generated when a gas is rendered electrically conducting. A plasma display consists of two glass substrates separated by a dielectric spacer to form a chamber. A noble gas, such as  $Ne$ , is sealed inside the chamber. Transparent conductors patterned on the two glass substrates are orthogonal to each other and face the gas chamber and form a row and column addressing matrix. Phosphor dots are also coated on one of the glass substrates between conductor lines. When a high voltage is applied between the row and column electrodes, a plasma is produced at the intersection of the two electrodes, generating ultra-violet emission. Light is emitted from the phosphor that is excited by the ultra-violet radiation generated by the plasma. Figure G-2 is a schematic of a plasma display.

The disadvantage of a plasma display is that a sufficient volume of gas must be present to create a satisfactory intensity of light. This places a limitation on the resolution and portability. Typically a plasma display is only used as a large area display commercially.

# **Appendix H**

## **Microsystems Technology**

### **Laboratories's fabrication facilities**

Table H.1: Microsystems Technology Laboratories's fabrication facilities

Facility Name	Abbreviation	Description
Integrated Circuits Laboratory	ICL	Class 10 clean room for standard CMOS processing
Technology Research Laboratory	TRL	Class 100 clean room for processing silicon, III-V semiconductors, Au-contaminated substrates.
Nanostructures Laboratory	NSL	Class 10 clean room (inner) and Class 10,000 clean room (outer) for nano-size processing and metrology
Research Group Laboratory		Research group laboratory for device characterization

# Appendix I

## Process flow of the fabrication of the ordinary silicon field emitter arrays

Table I.1: Process flow of the fabrication of the ordinary silicon field emitter arrays

Step	Lab	Process Description & Parameter	Notes
1	ICL	Wafer Clean(pre-metal) $1H_2O_2: 3H_2SO_4$ (10min), 50:1HF(15 sec)	
2	ICL	$SiO_2$ growth (tubeB1 or tubeB2) Recipe 122: $1000^\circ C$ , 34 min, Steam	Thermal oxide growth, Target thickness=250nm
2-a	ICL	Measurement of $SiO_2$ thickness (UV1250)	
3	ICL	HMDS vapor deposition(HMDS) $125^\circ C$ , 25 min	HMDS is a vapor bake oven
4	ICL	PR coating and Pre-bake(coater) PR: KTI positive PR 820 35 cs. 8,500 rpm, thickness=920nm	

Table I.1: (continued)

Step	Lab	Process Description & Parameter	Notes
		Pre-bake: 115°C, 60 sec	
5	ICL	Exposure(stepper2)	Mask1 for $SiO_2$ dot formation
6	ICL	Post exposure bake(developer): 115°C, 60 sec Develop(developer): OCG 934 1:1 positive PR developer Post Bake(developer): 130°C, 60 sec	
6-a	ICL	Photo Resist dot diameter measurement(sem)	
7	ICL	$SiO_2$ etching(AME5000) Recipe: Isabela LTO Gas: $CF_4$ & $CHF_3$ , 12mTorr, 250 Watt	$SiO_2$ dot formation Anisotropic etching
7-a	ICL	Oxide thickness measurement(UV1280)	Confirm the endpoint of oxide etching
8	ICL	PR strip(asher) Recipe: STD, 1min	
9	ICL	Si etching(etcher1) Gas: $SF_6$ 95sccm /He 120 sccm 300mTorr, 100Watts, Gap spacing 1.5cm Reactor temperature: 13°C	Si formation isotropic etching
10	ICL	Oxide cape strip(oxide) Wet oxide etching in BOE station Recipe: 7:1BOE, 2-3 min,	etch rate: about 1000Å/min for thermal oxide and 2-3 times more for deposited oxide
11	ICL	Wafer cleaning(pre-metal) $1H_2O_2:3H_2SO_4$ (10min), 50:1HF(15sec)	Si tip sharpening
12	ICL	Oxidation Sharpening(tubeB1 or tubeB2)	

Table I.1: (continued)

Step	Lab	Process Description & Parameter	Notes
		Recipe 160 950°C, 15 hr, 100% dry O <sub>2</sub>	
13	ICL	Sharpened oxide layer strip(oxide) Wet oxide etching in BOE station Recipe: 7:1BOE, 1 min,	typically one should do say 3-4 minutes.
13-a	ICL	Inspection(microscope or sem)	
14	ICL	Wafer cleaning(pre-metal) 1H <sub>2</sub> O <sub>2</sub> :3H <sub>2</sub> SO <sub>4</sub> (10min) 50:1 HF(15sec)	
15	ICL	SiO <sub>2</sub> LPCVD growth(tubeA7) Recipe 462, 400°C, SiH <sub>4</sub> (50sccm)/O <sub>2</sub> (150sccm) 350mTorr,	Targeted thickness: 700nm Deposition rate: 103Å/min (02/07/99) 65Å/min (11/09/99) Gate insulator layer formation
15-a	ICL	SiO <sub>2</sub> thickness measuring (ellipsometer & nanospec)	
15-b	ICL	Inspection under (microscope)	
16	ICL	Wafer cleaning(pre-metal) 1H <sub>2</sub> O <sub>2</sub> :3H <sub>2</sub> SO <sub>4</sub> (10 min) 50:1HF(15 sec)	For LTO densification
17	ICL	LTO densification(tubeB4) Recipe: 183 1000°C, N <sub>2</sub> , (20-30 min)	
18	ICL	HMDS vapor deposition 150°C, (25 min)	
19	ICL	PR coating(coater) PR: KTI positive PR 820 35 cs. 5,500rpm, thickness=1,150nm	
20	ICL	Standard post-bake(developer)	



Table I.1: (continued)

Step	Lab	Process Description & Parameter	Notes
		Recipe 82: 130°C, (60 sec)	
21	ICL	Backside oxide strip(oxide) BOE 7:1	
22	ICL	PR strip(asher)	
23	ICL	Wafer cleaning(pre-metal) 1H <sub>2</sub> O <sub>2</sub> :3H <sub>2</sub> SO <sub>4</sub> (10 min) 50:1 HF(15 sec)	Prepare for poly-Si deposition
24	ICL	LPCVD poly-Si deposition(tubeA6)	Targeted thickness: 300nm
		Recipe: 461 625°C, SiH <sub>4</sub> (150sccm), 250mTorr	Deposition. rate: 73-74Å/min (02/12/99) 62Å/min (11/09/99) 58Å/min (03/02/00) Gate conductor layer formation
24-a	ICL	Poly-Si thickness measuring(UV1280)	
24-b	ICL	Inspection(microscope or sem)	
25	ICL	Phosphorus doping(tubeA4) Recipe: 310 POCl <sub>3</sub> , 925°C, (1hr 39 min)	Gate conductor layer doping
26	ICL	Doped oxide strip(oxide) BOE: 7:1	Strip the Phosphorus doped oxide
26-a	ICL	Poly-Si thickness measurement(UV1280)	
26-b	ICL	4-pt probe resistivity measurement of P doped poly-Si(prometrix)	
27	ICL	Chemical mechanical polishing(cmp)  Table: 25 rpm Quill: 15 rpm	Doped poly-Si and gate insulator etching, Opening the gate aperture

Table I.1: (continued)

Step	Lab	Process Description & Parameter	Notes
		Down: 2.5 psi Back 1.0 psi Slurry 150 ml/min.	
27-a	ICL	Inspection(microscope or sem)	
28	ICL	Wafer cleaning(pre-metal) $1H_2O_2 : 3H_2SO_4$ (10 min)	
29	ICL	HMDS vapor deposition $125^\circ C$ , (25 min)	
30	ICL	PR coating(coater) KTI positive PR 820 35 cs. 5,500rpm, Thickness=1,150nm Pre-bake: $115^\circ C$ , (60 sec)	
31	ICL	Exposure(Stepper 2)	Mask2 (gate conductor patterning) Aligned to Mask1
32	ICL	Develop(developer) OCG 934 1:1 positive PR developer Post-bake: $130^\circ C$ (60 sec)	
32-a	ICL	Inspection under (microscope or sem)	
33	ICL	Doped Poly-Si etching(etcher-1) Gate conductor patterning Reaction gas: $CCl_4/SF_6$ Recipe 10	
34	ICL	PR strip(asher)	
35	ICL	$SiO_2$ etching(oxide) BOE 7:1, (5 min)	

Table I.1: (continued)

Step	Lab	Process Description & Parameter	Notes
35-a	NSL	Observation of final structure(SEM)	

## Appendix J

# Process flow of the fabrication of the high aspect ratio silicon field emitter arrays

Table J.1: Process flow of the fabrication of the high aspect ratio silicon field emitter arrays

Step	Lab	Process Description & Parameter	Notes
1	ICL	RCA cleaning (rca)	
2	ICL	$SiO_2$ growth (tubeB1 or tubeB2) Recipe 122: 1000°C, 34 min, Steam	Thermal oxide growth. Target thickness: 250nm
2-a	ICL	Measurement of $SiO_2$ thickness (UV1250)	
3	ICL	HMDS vapor deposition (HMDS) 125°C, 25 min	HMDS is a vapor bake oven
4	ICL	PR coating and Pre-bake (coater) PR: KTI positive PR 820 35 cs. 8,500 rpm, thickness=920nm	

Table J.1: (continued)

Step	Lab	Process Description & Parameter	Notes
		Pre-bake: 115°C, 60 sec	
5	ICL	Exposure (stepper2)	Mask1 for $SiO_2$ dot formation
6	ICL	Post exposure bake (developer): 115°C, 60 sec Develop (developer): OCG 934 1:1 positive PR developer Post Bake (developer): 130°C, 60 sec	
6-a	ICL	Photo Resist dot diameter measurement(sem)	
7	ICL	$SiO_2$ etching (AME5000) Recipe: Isabela LTO Gas: $CF_4$ & $CHF_3$ , 12mTorr, 250Watt	Anisotropic etching $SiO_2$ dot formation
7-a	ICL	Oxide thickness measurement (UV1250)	Confirm endpoint of oxide etching
8	ICL	PR strip (asher), Recipe: STD, 1 min	
9	ICL	Si etching (etcher1) Gas: $SF_6$ 95sccm/He 120sccm 300mTorr, 100Watts, Gap spacing 1.5cm Reactor temperature: 13°C	Isotropic etching, Si tip formation. $SiO_2$ neck size should be about 110-120nm to ensure optimal following of the oxidation sharpening process
10	TRL	Si deep trench etching (sts or AME5000) Recipe: MIT59	Emitter pillar formation

Table J.1: (continued)

Step	Lab	Process Description & Parameter	Notes
10-a	ICL,NSL	SEM observation of the structure	
11	ICL	Oxide cap strip (oxide) Wet oxide etching in BOE station Recipe: 7:1BOE, 2-3 min	Etch rate: 1000Å/min for thermal oxide and 2-3 times higher for deposited oxide
12	ICL	Wafer cleaning (pre-metal) 1H <sub>2</sub> O <sub>2</sub> : 3H <sub>2</sub> SO <sub>4</sub> (10min), 50:1HF(15sec)	
13	ICL	RCA cleaning	
14	ICL	Oxidation Sharpening (tubeB1 or tubeB2)	Sharpen the emitter tip
		Recipe160:950°C,15hr,100% dry O <sub>2</sub>	
15	ICL	Sharpened oxide layer strip (oxide) Recipe: 7:1BOE, 1 min	Typically 3-4 minutes.
15-a	ICL	Inspection (microscope or sem)	
16	ICL	Wafer cleaning (pre-metal) 1H <sub>2</sub> O <sub>2</sub> : 3H <sub>2</sub> SO <sub>4</sub> (10min) 50:1HF(15sec)	16, 17 not necessary if step 18 done within same day of step 15
17	ICL	RCA cleaning (rca)	
18	ICL	SiO <sub>2</sub> PECVD (concept1) Recipe: dingm	Try to deposit as thick as covering all up to the tip
18-a	ICL	SiO <sub>2</sub> thickness measuring (UV1250)	
19	ICL	LTO densification (tubeB5) Recipe190: 1000°C, N <sub>2</sub> , 1 hour	
19-a	ICL	SiO <sub>2</sub> thickness measurement (UV1250)	
19-b	ICL	Inspection (sem)	
20	ICL	Chemical Mechanical Polishing of SiO <sub>2</sub> layer (CMP) Recipe:	Remove the LPCVD SiO <sub>2</sub> bump

Table J.1: (continued)

Step	Lab	Process Description & Parameter	Notes
		Table: 25 rpm Quill: 15 rpm Down: 2.5 psi Back 1.0 psi Slurry 150 ml/min.	
21	ICL	Post CMP cleaning	
22	ICL	Wafer cleaning (pre-metal) First in Blue boat, then in Green boat, Then HF dip. $1H_2O_2: 3H_2SO_4(10min) 50:1HF(15sec)$	
23	ICL	Etching down $SiO_2$ (oxide)	Be sure to use precise time etches to reveal just the conical tip (600-700nm).
23-a	ICL	$SiO_2$ thickness measurement (UV1250)	
23-b	ICL	Inspection (SEM)	
24	ICL	Wafer cleaning (pre-metal) $1H_2O_2: 3H_2SO_4(10min) 50:1HF(15sec)$	Step 24, 25 not necessary if step 26 is done within same day of step 23
25	ICL	RCA cleaning (rca)	
26	ICL	$SiO_2$ LPCVD (tubeA3)	Targeted thickness: 700nm
		Recipe462: $400^\circ C, SiH_4$ (50sccm)/ $O_2$ (150sccm), 350mTorr,	Dep. rate: $103\text{\AA}/\text{min}$ (02/07/99) (tubeA4)
26-a	ICL	$SiO_2$ thickness measuring (UV1250)	
27	ICL	Wafer cleaning (pre-metal) $1H_2O_2: 3H_2SO_4(10\text{ min}) 50:1HF(15\text{ sec})$	Step 27, 28 not necessary if step 29 same day as step

Table J.1: (continued)

Step	Lab	Process Description & Parameter	Notes
			26
28	ICL	RCA cleaning (rca)	
29	ICL	LTO densification (tubeB5) Recipe183: 1000°C, N <sub>2</sub> , (20-30 min)	
30	ICL	HMDS vapor deposition 150C, 25 min	
31	ICL	PR coating (coater) PR: KTI positive PR 820 35 cs. 5,500rpm, thickness=1,150nm	
32	ICL	Standard post-bake (developer) Recipe82: 130°C, 60 sec	
33	ICL	Backside oxide strip (oxide) BOE 7:1	
34	ICL	PR strip (asher)	
35	ICL	Wafer cleaning (pre-metal) 1H <sub>2</sub> O <sub>2</sub> : 3H <sub>2</sub> SO <sub>4</sub> (10 min) 50:1 HF (15 sec)	For poly-Si deposition
36	TRL	RCA cleaning (rca)	
37	TRL	LPCVD poly-Si deposition (lpcvd) Recipe461: 625°C, SiH <sub>4</sub> (150sccm), 250mTorr,	Targeted thickness: 300nm.
38	ICL	Poly-Si thickness measuring (UV1250)	
39	Outside	Ion-implantation of phosphorus	Gate conductor layer doping
40	ICL	Wafer cleaning (pre-metal) First blue boat, then green boat, finally HF dip, 1H <sub>2</sub> O <sub>2</sub> : 3H <sub>2</sub> SO <sub>4</sub> (10 min) 50:1HF(15 sec)	



Table J.1: (continued)

Step	Lab	Process Description & Parameter	Notes
41	ICL	RCA cleaning	
42	ICL	Implantation annealing (tubeA4)	
42-a	ICL	Poly-Si thickness measurement (UV1280)	
42-b	ICL	4-pt probe resistivity measurement Of Phosphorus doped poly-Si (prometrix)	Performed on control wafer
43	ICL	Chemical mechanical polishing (CMP) Recipe: (CMP) Recipe: Table: 25 rpm Quill: 15 rpm Down: 2.5 psi Back 1.0 psi Slurry 150 ml/min.	Doped poly-Si and gate Insulator etching Opening gate aperture
44	ICL	Post CMP cleaning	
45	ICL	Wafer cleaning (pre-metal) First blue boat, then green boat, then HF dip. $1H_2O_2$ : $3H_2SO_4$ (10min), 50:1HF(15sec)	
45-a	ICL	Inspection (microscope or sem)	
46	ICL	HMDS vapor deposition $125^\circ C$ , (25 min)	
47	ICL	PR coating (coater) KTI positive PR 820 35 cs. 5,500rpm, Thickness=1,150nm	

Table J.1: (continued)

Step	Lab	Process Description & Parameter	Notes
		Pre-bake: 115°C, 60 sec	
48	ICL	Exposure (stepper-2)	Note: Mask 2 (gate conductor patterning) Aligned to Mask 1
49	ICL	Develop (developer) OCG 934 1:1 positive PR developer Post-bake: 130°C, 60 sec	
49-a	ICL	Inspection (microscope or sem)	Gate conductor patterning
50	ICL	Doped Poly-Si etching (etcher-1 or AME5000) Recipe10 Reaction gas: $CCl_4/SF_6$	
51	ICL	PR strip (asher)	
52	ICL	$SiO_2$ etching (oxide) BOE 7:1, 10 min	Etch to reveal the whole tip
53	ICL	Diesaw to small pieces (diesaw)	
54	NSL	Observation of final structure	

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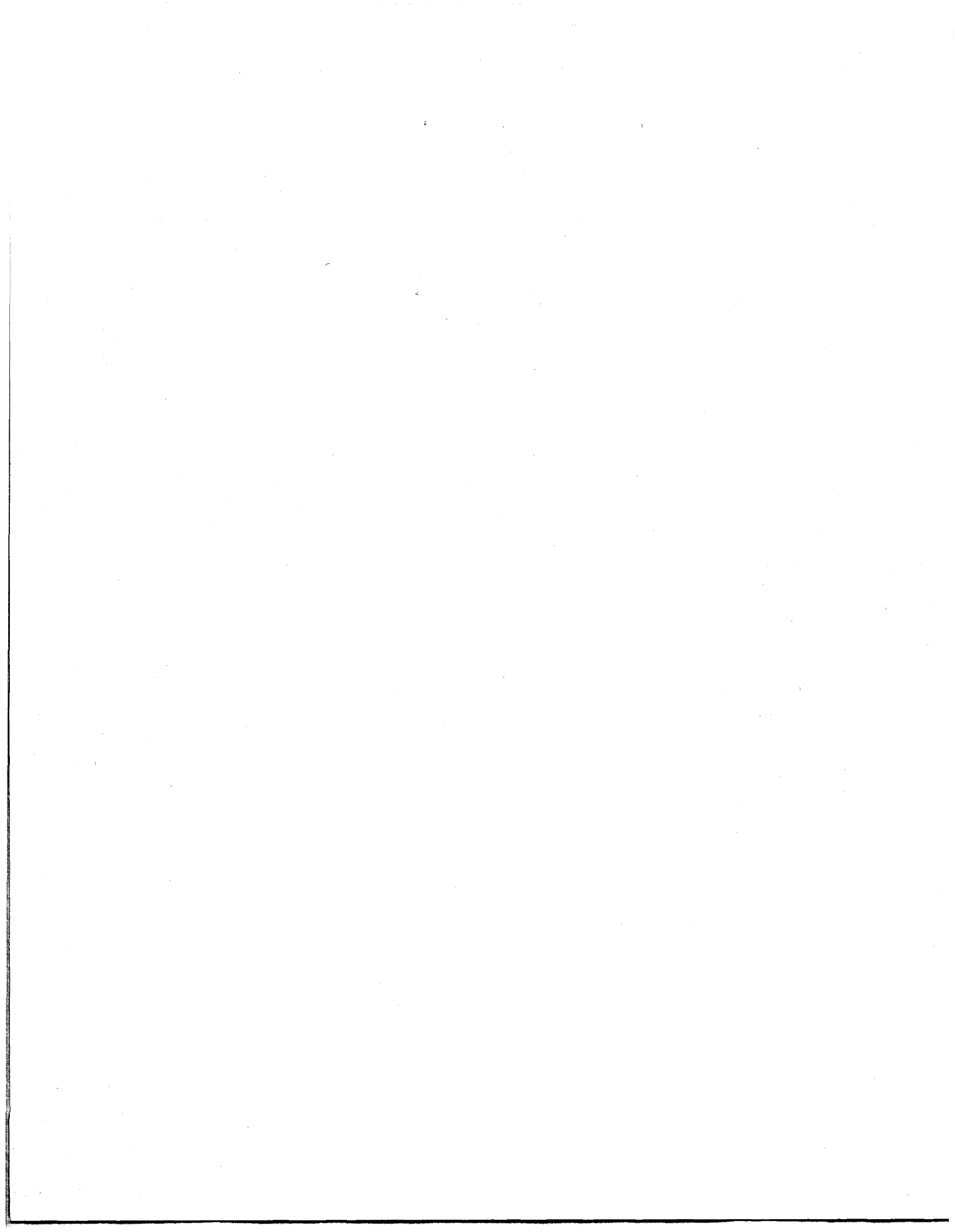
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