

Optoelectronic Integration Using Aligned Metal-to-Semiconductor Bonding

by

Wojciech Piotr Giziewicz

Submitted to the Department of Electrical Engineering and Computer
Science

in partial fulfillment of the requirements for the degree of

Bachelor of Science in Electrical Engineering
and Master of Engineering in Electrical Engineering

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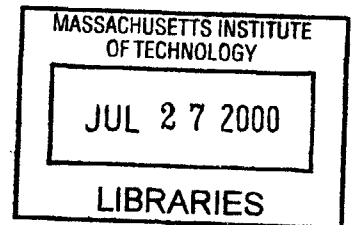
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Abstract

Methods of bonding optoelectronic devices to substrates containing VLSI circuitry were investigated. A procedure whereby an intermediary metal film is responsible for the mechanical bonding and ohmic contact formation between the two pieces was developed after three different metallization schemes were tested. Bonding was performed at or below 365°C, low enough to prevent damage to the VLSI electronics. Bonded devices were separated from their growth substrate by removal of an epitaxially growth sacrificial layer.

The procedure was successful on GaAs substrates, and there is every indication that it will be equally successful on chips from the OPTOCHIP project. The technique also has the potential to be used in bonding III-V devices to silicon substrates and electronics.

Thesis Supervisor: Clifton G. Fonstad, Jr.
Title: Professor of Electrical Engineering

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Dr. Gale Petrich and Kurt Broderick maintained the processing lab where photolithography and some wet etching were done and they deserve to be mentioned for their hard (and very effective) work.

Of course all work and no play leads to receding hair lines, and I would like to thank all of my friends and especially Nicole for distracting me often enough to keep me content with my life.

Contents

1	Introduction	9
1.1	Motivation for Optoelectronic Integration	9
1.2	Thesis Outline	11
2	Wafer Bonding Techniques	12
2.1	Thin Film Epitaxial Lift-off	12
2.1.1	Epitaxial Lift-off (ELO) Process	12
2.1.2	Merits of Thin Film ELO	14
2.2	Wafer Fusion	15
2.3	Palladium Bonding	17
2.4	Ternary Phases of the Pd-GaAs System	19
2.4.1	Low Temperature and Short Time Behaviour	19
2.4.2	High Temperature and Long Time behaviour	21
2.4.3	Quaternary System - The addition of Sn	21
3	Experimental Procedures	23
3.1	Apparatus and Methods	23
3.1.1	Wet Etching	23
3.1.2	Metal Deposition	24
3.1.3	Bonding Medium	25
3.1.4	Graphite Strip Annealer	27
3.2	Experiments	27
3.2.1	Palladium Deposition and Contact Processing	27

3.2.2 Bonding Procedures	28
4 Results and Discussion	34
4.1 Palladium Contact Resistance	34
4.2 Palladium Bonding	35
4.3 Pd-Sn-Pd Bonding	38
4.4 Alternate Pd-Sn-Pd Bonding Method	44
5 Conclusions and Future Work	48
5.1 Project Achievements	48
5.2 Bonding III-V Devices to Silicon VLSI	49

List of Figures

2-1	Schematic Representation of the Epitaxial Lift-Off Process	13
2-2	Schematic Representation of Wafer Fusion Process	17
2-3	Schematic representation of fabricated diodes bonded to GaAs wafers [15]	18
2-4	Images of the Pd-GaAs interface as deposited, and after 10 minute anneals at 220°C and 275°C respectively, from [12]	20
3-1	Calibration of deposited film thickness to crystal monitor reading. The slope is approximately 280 Å/kHz	26
3-2	Schematic of argon bubbling apparatus to treat reduce the amount of dissolved oxygen in the bonding medium	27
3-3	Schematic of the graphite strip annealer	28
3-4	Three techniques attempted for applying pressure to the samples dur- ing bonding	29
3-5	Schematic of Final Bonding Procedure	32
4-1	ESEM photo of a metallized sample that underwent compression be- tween two glass slides held together with clips.	36
4-2	ESEM photo of a long pillar that had bonded to the Pd-covered sub- strate. The two bonding samples were broken apart during handling, resulting in damage to the pillar and demonstrating the strength of the bond.	37
4-3	ESEM photo of the interface between the pillar and Pd-covered GaAs sample. An alloyed interfacial layer is clearly visible.	38

4-4	ESEM photo of an array of contact areas where bonding had occurred.	41
4-5	ESEM photo of the interface between deposited metal and bonding site. Metal is to the left of the interface, the polycrystalline alloyed region is to the right.	42
4-6	ESEM photo of an array of bonded pillars.	43
4-7	ESEM photo of part one bonded pillar. The alloyed bonding layer is clearly discernible	44
4-8	ESEM photo of one bonded pillar. The top surface appears damaged or imprinted.	45
4-9	ESEM photo of an array of contact areas.	46
4-10	ESEM photo of the corner of one contact area, showing what is believed to be palladium bonded to the host substrate.	47
4-11	ESEM photo of the side of one contact area, showing what is believed to be palladium bonded to the host substrate. Additionally, a difference in focus between the left and right sides of the bonded material is apparent, indicating different heights.	47

List of Tables

4.1	Summary of Contact Resistance Measurement	34
4.2	Summary of Pd-Sn-Pd Bonding Experiments. Epi1 and Epi2 refer to the two materials grown by MBE as described in Section 3.2.2	40

Chapter 1

Introduction

1.1 Motivation for Optoelectronic Integration

The goal of this project is to develop a technique for relatively low temperature bonding of semiconductors for the fabrication of monolithically integrated optoelectronic integrated circuits (OEICs). This technology has broad-ranging applications in a wide variety of fields such as communication systems, computing, and biomedical imaging.

Technologies for integrating optoelectronic devices and electronic circuitry can be classified as either hybrid or monolithic. Hybrid integration is available commercially, and involves combining optoelectronic devices and integrated circuits in common packaging, such as a multi-chip module. The device density of the resulting OEIC is however very low and many of the advantages of using optics are lost. Monolithic integration, where electronic and optoelectronic components are integrated on the same substrate, should be superior in terms of speed, power consumption, device density, system reliability, and manufacturing complexity. A major barrier for monolithic integration is that the material that is most widely used for microelectronic fabrication experience is silicon, while III-V materials are most suitable for optoelectronic devices. Epitaxial growth of such materials on silicon is complicated by the fact that there is a 4% lattice constant mismatch between the materials, and the thermal expansion coefficients of the materials differ by 50% or more.

These problems combined with increasing ability for large scale electronic integration on III-V substrates led to the OPTOCHIP [1, 2] project, an effort in integrate optoelectronic devices on GaAs electronics. The electronics portion of the chip was completely fabricated at an industrial foundry using a standard process flow, and regions of the chip were set aside for the growth of optoelectronic devices. Wells were etched in the aforementioned regions and LEDs were grown in the wells by molecular beam epitaxy. However, the device growth had to take place at a relatively low temperature so as not to exceed the temperature limitations of the integrated electronics. In other words, growth had to be done at a temperature low enough such that metal contacts and interconnects on the chip and the profiles of implanted dopants were not significantly affected [3]. This condition poses serious limitations on the growth of certain devices, most importantly vertical cavity surface emitting lasers (VCSELs), which require a higher temperature and growth quality than LEDs. Wafer bonding appears to be a more flexible method of integration, as devices can be grown in bulk on a separate substrate (which is optimised for MBE growth, unlike substrates used for integrated circuits) and then processed into pillars that fit in the wells previously mentioned.

A further important advantage of wafer bonding is the confinement and reduction of defects. In attempts to grow LEDs in the OPTOCHIP growth wells, many problems were encountered with contamination or very fine roughness of the growth substrate. These features prevent clean, high quality growths, resulting in the need for painstaking cleaning procedures for the growth windows. Additionally, growth of a material with a different interatomic spacing than the substrate creates stress at the growth interface. If the layer being grown becomes too thick, the stress can result in defects that propagate straight through the layer, ruining the growth. Wafer bonding alleviates these problems, because though defects may still be present when two materials are bonded together, they occur near or at the interface without penetrating deep into bonded structures [5].

Though various forms of wafer bonding have been explored, integration on the scale of the OPTOCHIP presents new requirements that have not previously been

the focus of research attention. The device and electronics substrates must be aligned prior to bonding. Also, a very large number of devices (or more generally pillars) that are not necessarily uniformly distributed must be bonded at once over a large area.

1.2 Thesis Outline

Many wafer bonding methods have been investigated. A number of these methods are described in Chapter 2, evaluating their strengths and weaknesses. The Pd-GaAs ternary system is also comprehensively described, illustrating the positive characteristics that make Pd an interesting choice as an intermediate layer in wafer bonding.

The experimental procedures used during the bonding experiments are summarized in Chapter 3. The results of the bonding experiments including images of bonded pillars are given in Chapter 4. Finally the conclusions suggested by the experiments are detailed in Chapter 5, along with processes and suggestions for further research.

Chapter 2

Wafer Bonding Techniques

2.1 Thin Film Epitaxial Lift-off

This technique utilizes single crystal epilayers which are grown lattice-matched to a sacrificial growth layer which was in turn grown lattice matched to the growth substrate. The sacrificial layer is selectively etched removing the epitaxial layer from the substrate. Alternatively the sacrificial layer may be used as an etch stop in a process to completely etch the away the growth substrate. Using the proper techniques, these layers may be handled and processed before bonding onto arbitrary host substrates. A substantial advantage of this method is that the bond is maintained by van der Waals forces, such that the host substrate need not be lattice matched. In fact it need not even be crystalline, as integration of GaAs and InP materials has been demonstrated with host substrates such as silicon, lithium niobate, glass, and polymers [17]. The only requirement on the host substrate is smoothness.

2.1.1 Epitaxial Lift-off (ELO) Process

The ELO process is illustrated in Figure 2-1 [17]. If it is assumed that a GaAs material system is being described in this case, then a sacrificial etch layer of $\text{Al}_x\text{Ga}_{1-x}\text{As}$ ($x > 0.6$) must be grown between the growth substrate and the epilayer to be bonded.

The first step is to apply an Apiezon W (black wax) layer to the epitaxial sample.

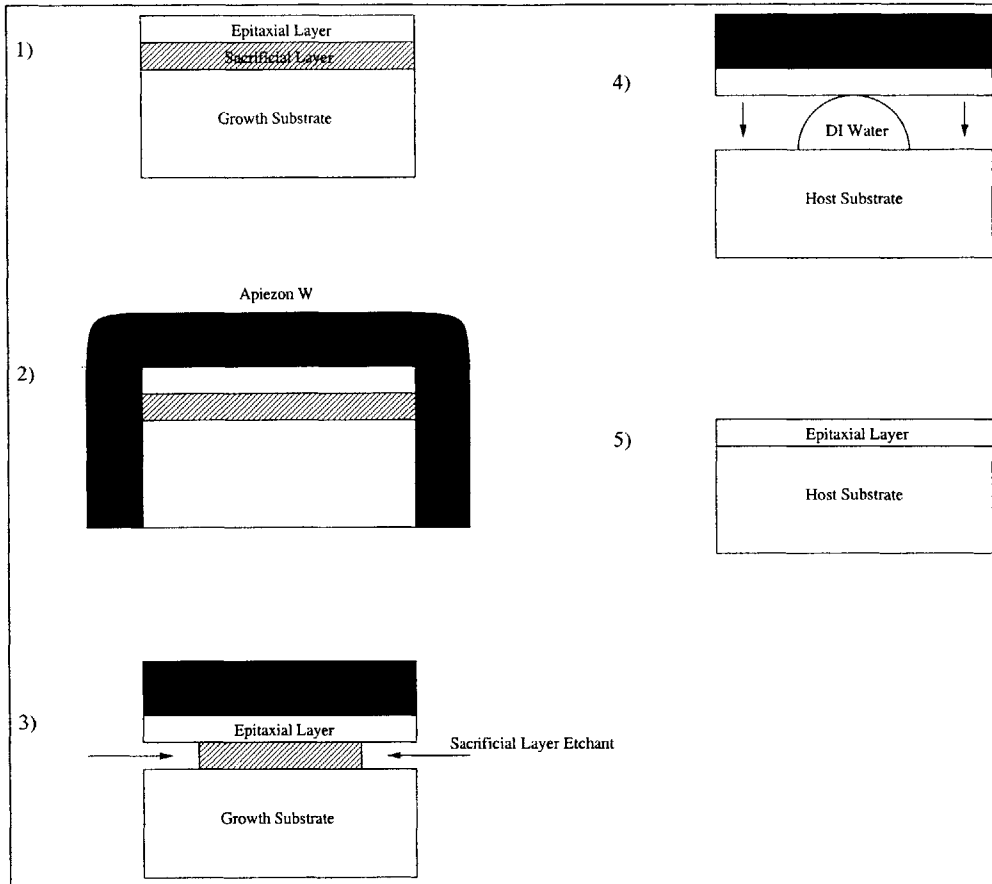


Figure 2-1: Schematic Representation of the Epitaxial Lift-Off Process

There are a number of ways to do this. One process consists of dissolving Apiezon W in trichloroethane and spraying several coats of this solution onto the sample to reach a thickness of ca. $100\ \mu\text{m}$. The sample is then air-cured and baked. Another technique involves placing a pellet of wax on top of the sample and heating the sample to 125°C . The Apiezon W melts and spreads across the sample, at which point the sample may be cured in an oven or a Teflon press may be applied. The important consideration is that the wax layer should be relatively flat, as it is a handling layer and bonding pressure will be applied (ideally uniformly) through it. After the application process is complete, the edges of the sample must be exposed either by cleaning with trichloroethane, cleaving of the sample, or mechanical grinding of the edges. Once the edges (and hence the sacrificial layer) have been exposed, the epitaxial layer is

ready to be separated from the growth substrate.

For a GaAs-based sample an HF etch is used, with etch rate varying with HF concentration and temperature. The sacrificial layer is selectively etched laterally, with the Apiezon W placing the epitaxial layer under tension, thereby curling it slightly away from the growth substrate. This helps to expose the sacrificial layer to the etchant and allows the reaction products to leave the etch interface.

After the epitaxial thin film has been separated from the growth substrate it is bonded to a host substrate. Water helps significantly in the bonding process. A drop of deionized water is placed between the thin film and host. Once the film has been appropriately positioned above the host, contact with the water will result in wetting of the thin film surface which pulls it towards the host substrate. Once in place, the water can be forced out from between the samples through the application of pressure to the thin film through the Apiezon W. The samples are then left to dry under pressure for several hours for the remaining water to diffuse out and for an interface layer between the samples to form. Once bonded the Apiezon W is removed using trichloroethane.

2.1.2 Merits of Thin Film ELO

While bonding of this sort does pass the qualitative scotch tape test [14], it relies on relatively weak van der Waals forces and the formation of an interface layer hypothesized to be surface oxides. Impurities in the bonding atmosphere or water produce bumps in the thin film which mature into blisters and eventually flaking under thermal cycling, which signals of potential difficulties in using an imperfectly bonding film in further standard processing steps such as metallization and annealing [17].

Another serious drawback is the necessity to bond to a very flat surface, making this technique impractical for integration with electronics. Additionally, more complicated processing steps are required for structures based on GaAs with high Al content as they are vulnerable to the HF separation etch. One solution is to mesa-etch the outer edges of the epitaxial sample down to the AlAs layer such that the outer edge

of the vulnerable structure is covered by Apiezon W. Similar measures are required in the InP materials system. In this case AlAs is not a good sacrificial layer as it is not lattice matched with an InP growth system. Therefore a mesa etch as described is performed, followed by the complete etching of the growth substrate down to an etch stop layer between the growth substrate and the epitaxial layer of interest.

In addition to these concerns, a further serious drawback as first reported by Yablonoitch was the inability to create an electrical contact between the thin film and the host substrate. Solutions such as wafer fusion and palladium bonding [14] attempt to address this problem.

2.2 Wafer Fusion

Wafer fusion, a technique developed over a decade ago by Liao [6], produces the highest quality semiconductor-semiconductor bond of all of the direct-bonding technologies currently being developed. Two samples are placed in contact and pressure and heat are applied to produce a strong covalent bond at the interface.

The primary mechanism in wafer fusion is mass transport [10]. As the surfaces are heated they decompose, with the Group V elements forming a gas which is prevented from escaping since it is trapped between the samples. The Group III atoms are mobile and diffuse along the two surfaces at the interface to fill in any gaps. When the materials are cooled, the Group V elements reform the original compounds with the Group III elements on either side of the bond, and also form an alloy of the elements at the interface, resulting in covalent bonding which preserves the electrical and optical properties of the original materials. Though the bond itself is of very high quality, the entire procedure is at first glance not perfectly adapted for use in integration of devices with already processed electronics. The high temperatures required for the procedure can promote dopant diffusion and degradation of ohmic contacts and layers of metallization. Additionally, the process is not effective with all material combinations. Finally, since the semiconductors may not be lattice matched, the interface between them will contain defects, harming electrical performance. The

only consolation on the final point is that the defects are confined to the interface and do not propagate into the surrounding material [5].

Integration by wafer fusion with the OPTOCHIP was attempted by Donald Crankshaw [10]. His procedure, as illustrated in Figure 2-2, was similar in principal to ELO. Epitaxial samples with sacrificial layers were grown by MBE. The samples were patterned to form device pillars and placed against the host substrate. These two samples were pressed together and heated, and once removed from the furnace bonding was observed if the conditions were acceptable. The growth substrate was then etched away as in the ELO procedure. Crankshaw found that the most successful bonding conditions (in terms of mechanical and electrical quality of the contact) were at temperatures incompatible with preservation of the quality of the electronics on the OPTOCHIP target. Additionally, the bonding pressure was not easy to control, and he found that some samples exhibited concavity of the target surface after bonding. Though the effect of this deformation on electrical and mechanical properties appeared small, it was difficult to quantify.

Aside from the aforementioned problems of temperature and mechanical deformation, the fusion process presents some processing challenges. For high quality bonding to take place, the two surfaces that are brought into contact must be clean and smooth. The first concern is native or deposited oxide that must be completely removed. The choice of etchants is important, as Crankshaw found that buffered oxide etch (7:1 $\text{NH}_4\text{F}:\text{HF}$) left a residue when etching SiO_2 that had been deposited to protect host substrates from damage. After etching the samples must either be immediately bonded or placed in an oxygen-deprived medium to prevent or significantly slow native oxide growth. Crankshaw used methanol (as opposed to water), but it is possible that this adversely affected his results as methanol, like water, contains dissolved oxygen that reacts with the semiconductor surface. A better procedure for preventing native oxide growth during sample storage and bonding is presented in Section 3.1.3. A final consideration in this procedure is the necessity to have very good crystallographic alignment between the host and devices to be bonded, something that is difficult to achieve due to jitters and bumps that inevitably occur during

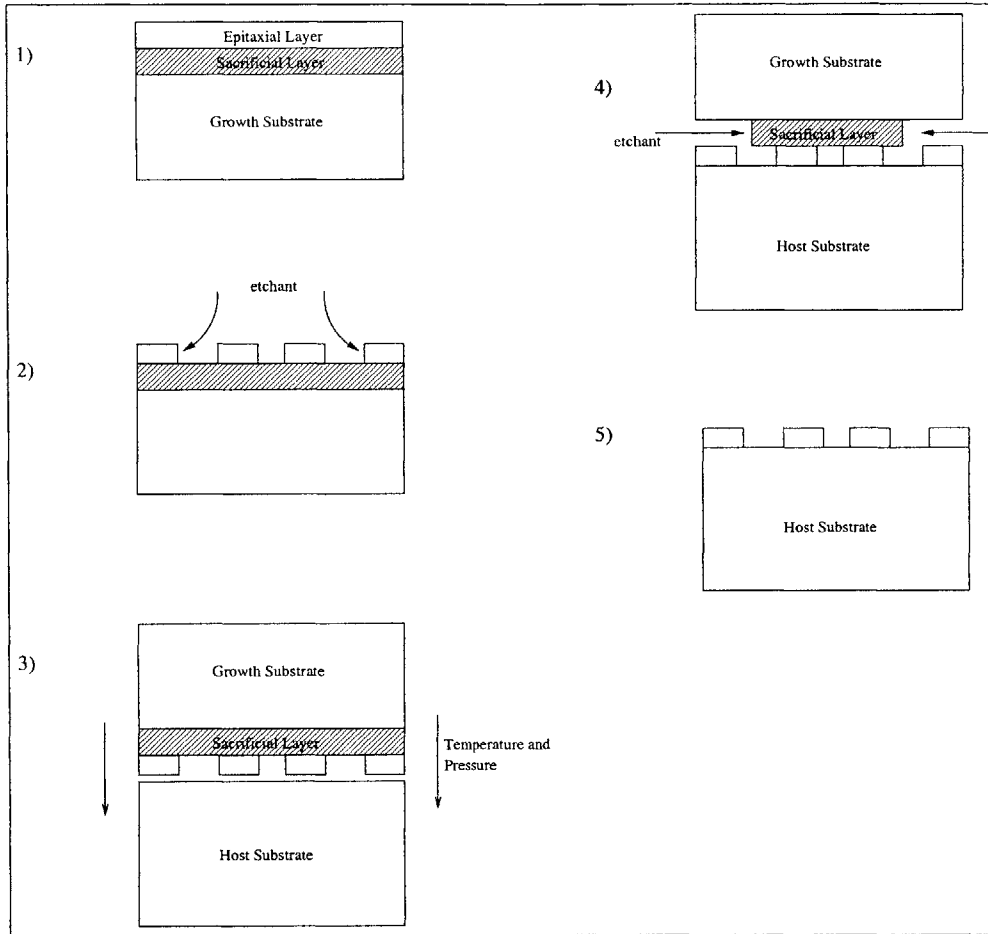


Figure 2-2: Schematic Representation of Wafer Fusion Process

sample movement, handling, drying, etc. by hand.

2.3 Palladium Bonding

As previously stated (2.1.2), a significant problem with the ELO method is that a contact between the host substrate and bonded structure cannot be made at the bonding site. Using palladium as an intermediary between the host and epitaxial layer provides a solution to this problem. Yablonovitch, Sands, et al. [14] first demonstrated palladium bonding of GaAs to various substrates, including silicon wafers, using a method nearly identical to ELO. A thin epitaxial GaAs film supported by wax was placed in contact (in DI water) with a substrate covered with a film of Pd.

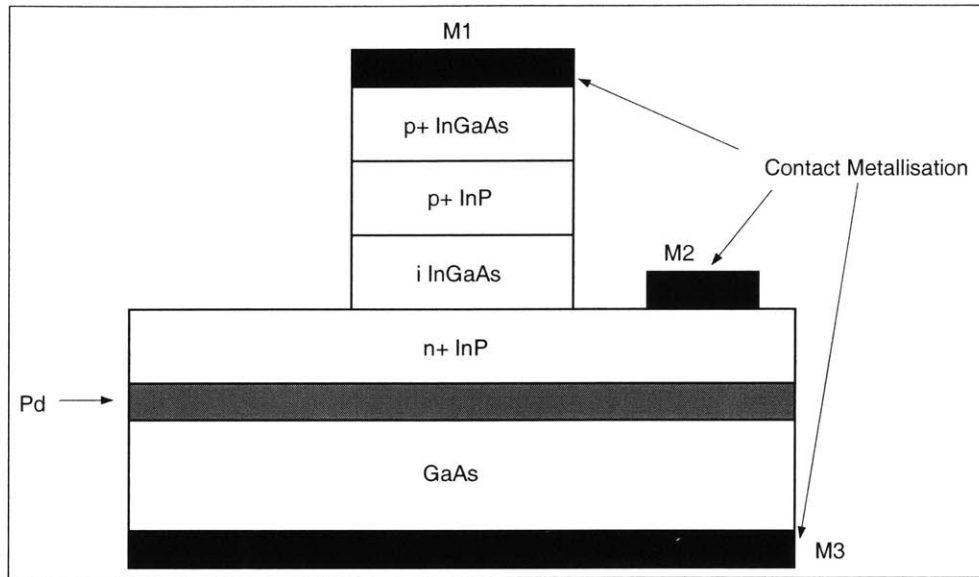


Figure 2-3: Schematic representation of fabricated diodes bonded to GaAs wafers [15]

Pressure was applied and the structure was dried overnight, resulting in a bonding of the film to the substrate. After annealing at 200°C, it was found that native oxide had been displaced into Kirkendall voids in the Pd layer, as it is the Pd that is the dominant moving species in the reaction. Performing this experiment with both n+ and p+ GaAs, they found that a bond occurs with a resultant contact resistance of not more than the order of $10^{-4} \Omega \text{ cm}^2$.

Tan, et al., presented Pd bonding of GaAs and InP [15], materials with significantly different lattice constants, finding that a Pd layer is sufficiently malleable to accommodate the stress resulting from the lattice and thermal expansion coefficient mismatches. As seen in Figure 2-3, a PIN diode structure was fabricated and bonded to a GaAs substrate. Bonding was at a higher temperature and for a longer time (350°C for 90 minutes) than in [14], but still low compared to wafer fusion methods. The Pd bond withstood the processing steps necessary to deposit, pattern, and anneal the contact metallization.

Electrical testing showed that an ohmic contact was formed at the Pd interface. Diode characteristics between the M1 and M2 contacts were virtually the same as between the M1 and M3 contacts. Additionally, they observed that while the reflec-

tivity of deposited Pd light in the IR range is approximately 90%, the reflectivity of on InP film bonded onto GaAs is approximately 35%, indicating consumption of the Pd in the bonding process.

2.4 Ternary Phases of the Pd-GaAs System

The two definitive studies of the Pd-GaAs material system were conducted by Sands et al. [12] and Lin et al. [13] over a decade ago. The first study concentrated on thin Pd films and the initial stages of phase formation (10 minute annealing cycles), while the second looked at both bulk and thin film conditions, though the bulk study is not interesting in a wafer bonding application as diffusion was carried out at temperatures above 500 °C. The results of the thin film experiments of the two studies were not entirely identical. A probable explanation is that the phase transformations are heavily dependent on the amount of Pd in the system. Sands used 50nm while Lin used 50 and 160 nm films. The exact nature of the ternary alloy is less important for the purposes of bonding than the initial stages of the reaction.

2.4.1 Low Temperature and Short Time Behaviour

Sands deposited palladium onto GaAs surfaces by electron beam evaporation to a thickness of 50 nm in a vacuum of approximately 10^{-6} Torr. Annealing was performed in flowing forming gas (95% Ar, 5% H₂) and lasted 10 minutes at the given temperatures. Several interesting reactions were observed in relatively low temperature anneals. They can be seen in the images of Figure 2-4, which are reproduced from the article by Sands *et al.* [12]

1. **As Deposited:** The Pd-GaAs reaction begins during deposition. The native GaAs oxide remains intact, but the reacted layer is between the substrate and the oxide layer, showing that Pd is by far the dominant moving species in the initial reaction. The reacted layer is called Phase I by Sands and has concentrations of gallium and arsenic atoms approximately 30% lower than the

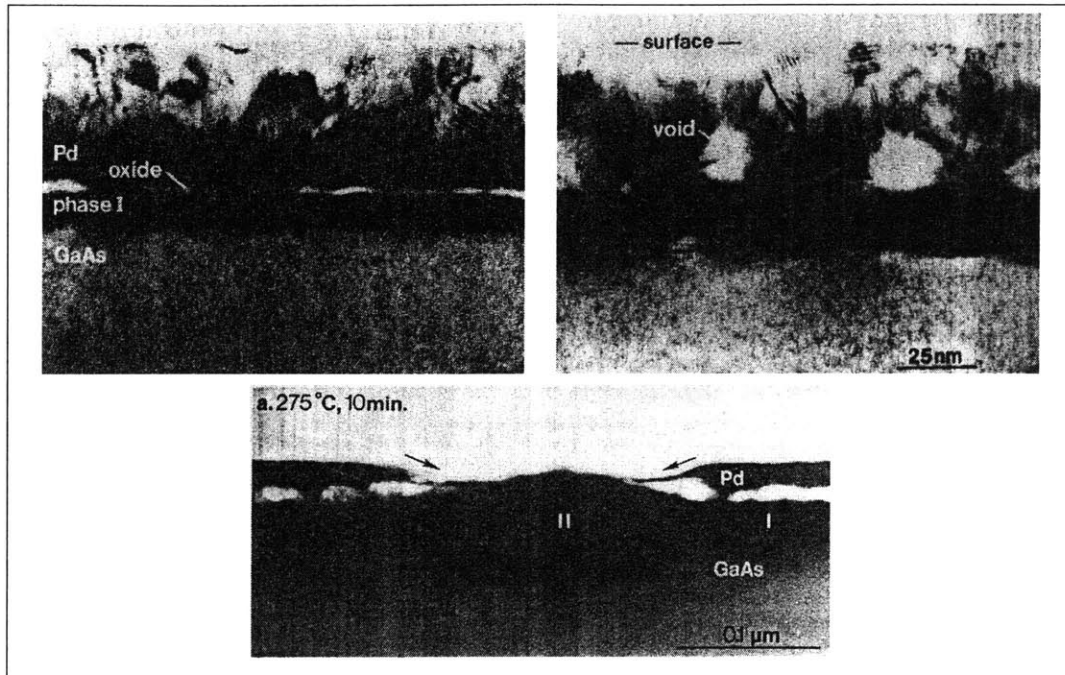


Figure 2-4: Images of the Pd-GaAs interface as deposited, and after 10 minute anneals at 220°C and 275°C respectively, from [12]

concentration of gallium and arsenic in GaAs. The grains of this phase are about 6 nm thick.

2. **220°C:** The Phase I layer thickens to approximately 10 nm and the native oxide is dispersed. Also, Kirkendall voids (about 15 nm in diameter) form at the Pd-Phase I interface, further confirming that palladium is the dominant moving species.
3. **275°C:** The reacted layer(s) after this processing are laterally non-uniform. The majority of the film consists of phase I with a surface layer of unreacted palladium. In highly localised areas however the palladium film is completely consumed. In these areas there is deep penetration of the reacted layer in the form of a new phase called Phase II by Sands. This phase is richer in palladium than Phase I. As the reaction proceeds the growth of Phase I is limited by the diffusion of palladium through the reacted layer, particularly as Phase I is relatively monocrystalline. The deep penetrations of Phase II

probably correspond to cracks, pores, or large grain boundaries in the Phase I layer that act as fast diffusion paths. The formation of Phase II in these areas is accompanied by significant lateral surface diffusion of palladium.

Lin *et al.* [13] also discuss the effect of oxygen on the material system. They conclude that the phases are in equilibrium with Ga_2O_3 , which is not an effective diffusion barrier for palladium. There is also apparently no noticeable solubility of oxygen in any of the phases observed in the system, suggesting that GaAs does not require stringent oxide cleaning procedures before metallizing with palladium.

2.4.2 High Temperature and Long Time behaviour

At high annealing temperatures only trace amounts of palladium remain and the two phases previously mentioned themselves undergo transformations. Lin *et al.* [13] suggest that the suitable phase for metallization of GaAs is the PdGa (ϵ) phase because of its chemical compatibility with GaAs and potential for longer term stability in the diffusion path. Both studies found that this phase forms at higher temperatures (approximately 400°C) or very long annealing times. Its growth is generally accelerated at temperatures where arsenic is leaving the system. This phase would therefore appear to be achievable within the temperature/time range to which processed chips may be subjected before a degradation of their electrical properties occurs. [2]

2.4.3 Quaternary System - The addition of Sn

Islam *et al.* [16] studied the formation of Pd/Sn contacts to n-GaAs. This metal system provides relatively low contact resistance while being more robust than conventional Au-Ge metallization in terms of spiking and behaviour in higher temperature processing steps. Pd/Ge contacts can be used but their thermal stability above 400°C requires further study. Although little work has been carried out on the Pd/Sn system, the authors believe that it could withstand the elevated temperatures associated with modern device processing.

The contact system consisted of 300 Å of Pd and 1500 or 900 Å of Sn evaporated and patterned onto n-GaAs samples. Contact resistivities varied depending on metal thickness and annealing processes, but were all on the order of 10^{-5} . In Pd/Ge metallization, Ge dopes n-GaAs and consequently a low resistance contact is obtained. The mechanism in Pd/Sn contact formation is similar with Sn taking the place of Ge. This suggests that a bonding scheme utilizing Sn could provide superior contact resistance to other metal bonding methods, but more importantly that there is relatively little interdiffusion of palladium and tin. The significance of this is that if palladium on both sides of the bonding interface were separated by tin, the Pd-GaAs alloys on either side of the interface could form without disturbing each other.

Chapter 3

Experimental Procedures

In consideration of the properties on the various bonding techniques presented in Chapter 2, a method incorporating the general technique of Crankshaw's wafer fusion and an intermediate metal layer was chosen, though the composition of the metal layer was unclear at the outset. This section outlines the general experimental and processing methods that were used, as well as specific procedures for a variety of bonding strategies.

3.1 Apparatus and Methods

3.1.1 Wet Etching

All of the etching done in the course of experimentation was wet. In the future, dry etching would be a preferable solution since it provides straighter feature definition, arguably more precise control, and better selectivity in general than wet etching.

To etch GaAs a solution of 5:1:1 DI H₂O:85% H₃PO₄:30% H₂O₂ was used, giving a fast etch rate of approximately 1.5 $\mu\text{m}/\text{min}$. This etch is not very selective between GaAs and AlAs such that samples with a thin AlAs sacrificial layer (as described in 2.1.1) were often etched through and beyond that layer. More dilute solutions of these compounds such as 50:3:1 apparently [18] give good selectivity (on the order of 10), but such a dilution not only gives a very slow etch (10:1:1 has a rate of

approximately $0.3 \mu\text{m}/\text{min}$), but the etch is most likely still not selective enough for these purposes. The sacrificial layer bonding samples would typically be between one and a few thousand angstroms thick, which is much thinner than the epitaxial layer of interest such that stopping on that layer would require very exact calibration and timing. Mixtures of the form $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2$ (PA etch) reportedly give excellent selectivity [18, 11]. This chemistry was attempted, but it was found that at high concentrations the etch is extremely fast. More trials would have been required to find a usable dilution. While more experimentation is necessary for this application, it appears that using an etch stop layer is only practical if the substrate has already been significantly thinned or if a dry etch is used. Other material systems however exhibit better selectivity in their wet etch chemistries than GaAs-AlAs.

A 25% HF solution was used for selectively etching AlAs over GaAs. The solution was heated slightly to about 60°C to slightly increase the etch rate. Yablonovitch had reported rates of $0.3 \mu\text{m}/\text{min}$ for 10% solution at 0°C with etch rates increasing with concentration and temperature. It was found in the course of processing that very high concentrations (50%) did not appear to increase the etch rate significantly compared to the 25% solution.

3.1.2 Metal Deposition

All deposition of metal was done by thermal evaporation. All metals came in pellet form with the exception of palladium which came in wire form. Initially it was evaporated using a coil, but it was quickly found that wrapping the material into a small ball and using a tungsten boat as with all other materials provided equally good deposition and better economy.

Deposition was preceded by a full solvent clean, except where lift-off was being performed. In that case the clean was done prior to photolithography. The solvent clean consisted of spraying the samples with (in order) 1,1,1-trichloroethylene, acetone, methanol, and isopropanol followed by blow-drying with nitrogen. Samples that were to be patterned with a shadow mask were attached to a glass slide with Crystal Bond (TM) transparent wax at this point to simplify the matter of aligning

and attaching the mask. The samples were then etched to remove native oxide in 7:1 $\text{NH}_4\text{F}:\text{HF}$ buffered oxide etch (BOE) for 10-15 seconds and rinsed in DI water. This process was repeated until water beaded on the surface of the sample indicating that the hydrophilic oxide layer had been removed. Ammonium hydroxide was also used to remove native oxide. It was effective but was slower than the BOE method and appeared to provide no additional benefit. As already mentioned 2.4.1, the surfaces to be bonded are not required to be perfectly free of native oxide when palladium is used.

The sample was then immediately mounted in the evaporator (with shadow mask if appropriate) and the system was pumped down to a base pressure of under 1.5×10^{-6} Torr, and generally under 7×10^{-7} Torr. The evaporator accommodates up to four boats at once, so in cases where multiple layers of material were to be evaporated this was done without breaking vacuum. The deposited layer thickness was measured with a crystal monitor during evaporation.

A rudimentary 3 point calibration, the data for which is plotted in Figure 3-1, was performed relating the crystal monitor readings to film thickness as measured with a Dektak profilometer (a shadow mask was used to pattern the palladium film). The results are approximate as the shadow mask does not give as even edges or surfaces as can be achieved with photolithography. Additionally there appeared to be some nonuniformity in the film heights across the sample. The source-to-monitor and source-to-sample distances were both approximately 30 cm.

3.1.3 Bonding Medium

Yablonovitch found that DI water is a clean [14] environment for bonding. Though the bonding surface need not be perfectly clean of oxide for bonding to occur the presence of a large amount of oxide will certainly not help in the bonding process. Oxygen may be found dissolved in untreated DI water, therefore a technique was borrowed from the field of electrochemistry that is used to displace dissolved oxygen when performing a polarographic analysis [19]. In that process an electrode is placed in an electrolyte and an increasing AC potential is applied. Different materials will

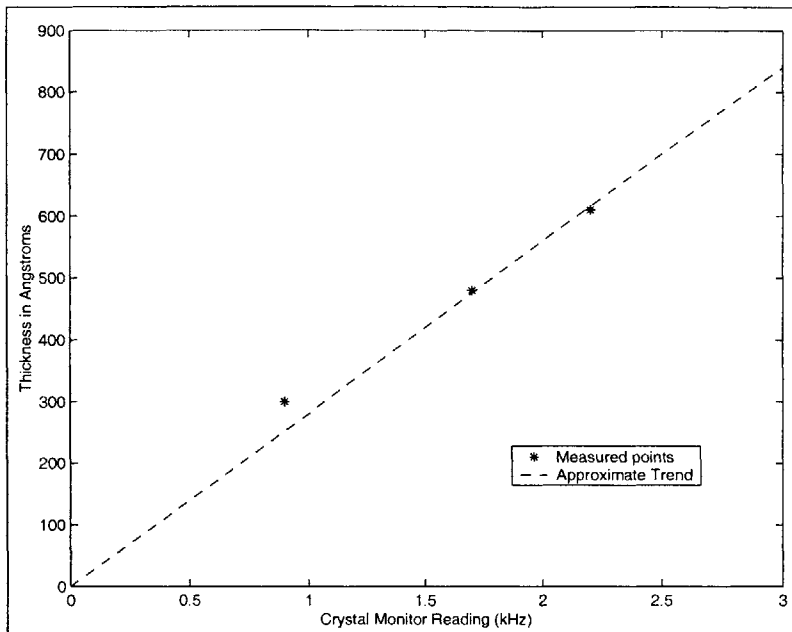


Figure 3-1: Calibration of deposited film thickness to crystal monitor reading. The slope is approximately 280 \AA/kHz

undergo reduction at different potentials, and the potential at which they are reduced is distinguished by a jump in current through the system. Oxygen both undergoes reduction at a low potential and is present in very high concentrations (several orders of magnitude in some cases) relative to the substances of interest. Therefore unless it is removed from the electrolyte, the signal to noise ratio of the analysis is too low to extract meaningful data. The same technique could be used with any solvent, and may have been helpful in Crankshaw's wafer fusion work (2.2).

A schematic of the apparatus is shown in Figure 3-2. Argon gas is bubbled into the liquid through a glass pipette. The bubbling is at first vigorous for approximately 15 minutes before the liquid is required for use, and is then reduced to a slow but steady flow for as long as the liquid is being used. The argon dissolves in the water and displaces much of the oxygen. Additionally, since argon is denser than air, a stagnant layer of gas forms above the liquid. Sample storage and manipulation can take place in this medium leading to cleaner bonds and surfaces without adding any additional complications to the processing steps.

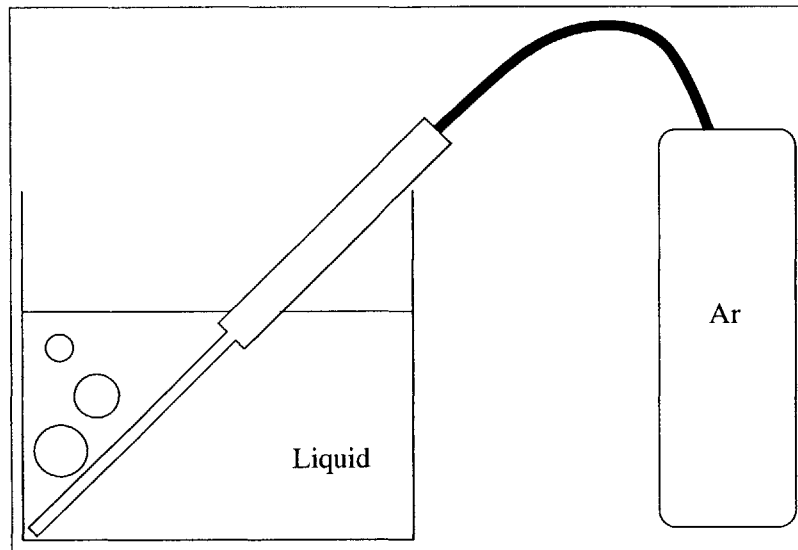


Figure 3-2: Schematic of argon bubbling apparatus to treat reduce the amount of dissolved oxygen in the bonding medium

3.1.4 Graphite Strip Annealer

Instead of a furnace it was decided to attempt to do the bonding experiments on a simple graphite strip heater. A schematic of the apparatus is shown in Figure 3-3. Before annealing or bonding the samples are placed in the chamber and a slow flow of forming gas is turned on for approximately 15 minutes to flush oxygen from the chamber. The temperature program is set in the controller, and the actual temperature follows the setpoints well with the exception of cooling cycles. The only cooling of the system is by radiation, so that when the temperature goes below approximately 100°C, the cooling rate can no longer keep up with the controller program. This is not a significant problem however, since all interesting activity happens above 200°C.

3.2 Experiments

3.2.1 Palladium Deposition and Contact Processing

The first experiments were performed to confirm ohmic contact formation with Pd, as well as to gather a qualitative sense for the relationship between annealing cycles,

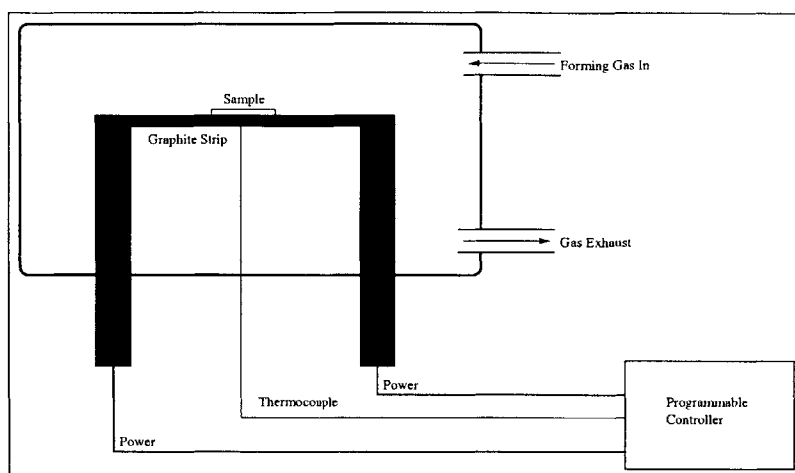


Figure 3-3: Schematic of the graphite strip annealer

metal thickness, and contact resistance. Deposition was done onto p-GaAs through a shadow mask using the procedure described in Section 3.1.2. The shadow mask used was a thin metal plate with circular holes approximately 0.5 mm in diameter, spaced in a 2 mm grid. Three different thicknesses were deposited and measured with a profilometer. The samples were subjected to different annealing cycles, following which their electrical performance was measured by looking at the I-V characteristics between two adjacent dots. The results are presented in Section 4.1.

3.2.2 Bonding Procedures

From the outset it was clear that the issue in designing a proper bonding procedure was to design a uniform method of pressing the samples together. Bonding using palladium had already been demonstrated and found to function properly [14, 15], the real difficulty of the project lay in creating a process that could compensate for non-uniformities over a relatively large area.

Palladium Film

The first four bonding attempts were made between two flat p-GaAs substrates. Palladium was deposited onto one substrate to a thickness of approximately 650

Å. The second sample underwent the same pre-metallization cleaning procedure to remove contaminants and native oxide. At this stage, the argon-bubbled bonding medium was not used.

The goal was to find a reliable method of providing pressure to the bonding interface. The three methods attempted are shown in Figure 3-4. It was decided not to use the method employed by Crankshaw as it provided much more pressure than was required, did not provide precise control over the applied pressure, and required the use of a furnace [10]. Bonding using a graphite heating strip was considered important for its simplicity, as a procedure that worked with such simple a apparatus could only be improved by using a more carefully designed system.

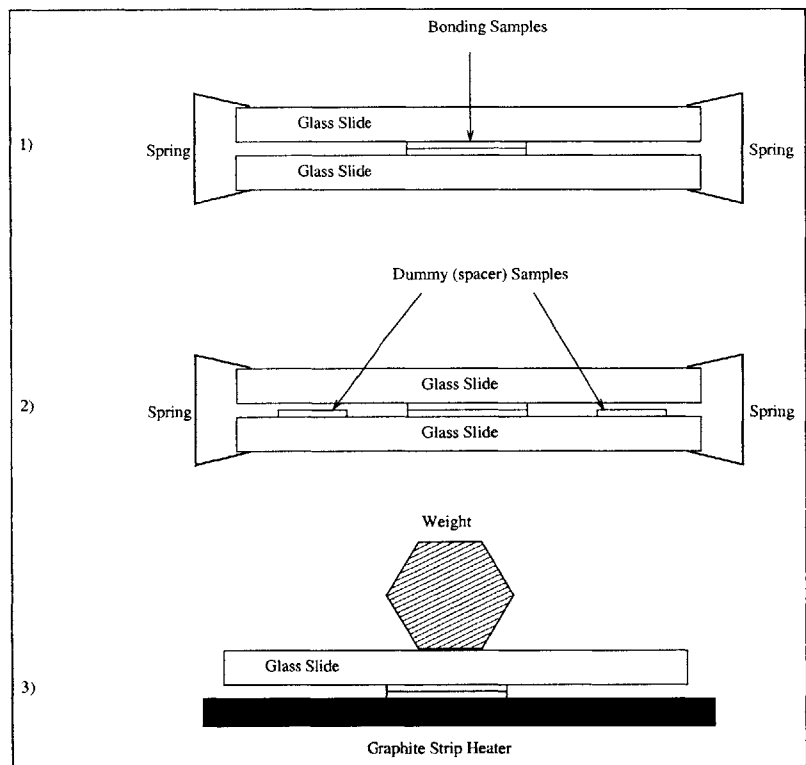


Figure 3-4: Three techniques attempted for applying pressure to the samples during bonding

Initial attempts involved using two glass slides clipped together at the ends to provide pressure. This was refined by placing dummy pieces at the ends to reduce the amount of pressure applied and the bowing of the glass slides. In both cases,

the assembly was placed in the annealer and heated at 360°C for 70 minutes with a 1 minute excursion to 415°C. Both methods were not satisfactory, as the glass slides showed considerable bowing due to the pressure of the clips. The methods also provided far more force than was required. There was no successful bonding, and profilometry of the substrates covered with palladium after the annealing showed a wide extent non-uniformity of the film surface (higher in the middle than the sides) that was not present before annealing. It is not clear whether that was caused by mechanical deformation of the GaAs or surface diffusion of palladium; in any case these methods were abandoned.

The subsequent method was simpler but proved to be more robust. Samples were prepared as described above, aligned face-to-face, and placed on the graphite heating strip. A glass slide was placed over the samples, and a force was applied by placing a large brass nut on the slide. Annealing took place in the same conditions as described above. The final trial involved bonding a patterned p-GaAs wafer. The unmetallized sample was etched as described in 3.1.1 to create 4 μm tall pillars (using the OPTOCHIP well clean mask). Slightly more Pd was deposited in this trial (approximately 750 Å). The patterned sample was placed into contact with the metallized sample in the same way as were the two unpatterned substrates, and pressure was applied by a 50 g brass nut through a glass slide (providing approximately 2 atm of pressure). The annealing cycle was once again unchanged.

Development of the Pd-Sn-Pd Technique

The melting point of tin is 232°C, much lower than that of palladium or GaAs, and also much lower than the temperatures at which the previously described annealing and bonding processes were run. The problem of bonding a large array of pillars to a stiff substrate is different from bonding a small piece or a large but thin piece (as Yablonovitch did [14]). In these cases non-uniformities are not important because they are either not seen (small piece) or can be easily absorbed (thin, flexible piece). The use of tin should allow for absorption of non-uniformities, since it is in liquid form during the annealing process, which should lead to smoothing under the pressure of

applied pillars. The initial trial of this method gave encouraging signs. A thin layer of tin followed by approximately 900 Å of palladium were deposited onto a substrate previously coated with approximately 750 Å of palladium. After annealing with a p-GaAs substrate with 4 μm pillars, successful bonding did not occur but observation under the microscope showed that many pillars had come into contact with the metal and metal had been transferred to the pillars. However, the original sample onto which the tin and palladium were deposited had been sitting for some time in an open atmosphere and its palladium surface was thought to have oxidized or otherwise become dirty during that time leading to poor adhesion of the tin.

The sight of metal transferred to the pillars validated the idea that tin could act as a compliant layer to compensate for mechanical non-uniformities in the bonding surfaces. Many trials were performed using Pd-Sn-Pd layers deposited onto GaAs substrates. The thickness of tin layer deposition was not calibrated in the evaporator as it does not seem to be of great importance. Generally one pellet of tin was used, and evaporation was done to reach 2.0-2.5 kHz on the crystal monitor. An EDX analysis performed on an annealed GaAs-Pd-Sn-Pd surface showed the ratio of palladium to tin to be about 3:1. This is however not a measure of the material on the surface since the electron beam has a penetration depth that takes it through all of the metal layers. Much experimentation would need to be done to ascertain an optimal tin layer thickness. This optimum would not only be dependent on how much cushioning is needed for good bonding, but also the thermal and long-term stabilities of different thicknesses. In this case it was decided to use a relatively small amount as compared to the amount of palladium used in order to minimize problems of tin diffusion through the palladium layers and oxidation of the diffused tin prior to bonding.

Over several trials the procedure was enhanced in many respects. The schematic of the final version is shown in Figure 3-5. Samples with epitaxial material came in two varieties: in both cases there was a 5 μm layer of p-GaAs that would be bonded, but the first sample had 2000 Å of AlAs separating the growth substrate from the p-GaAs layer while the second sample had only 1000 Å. The glass slide from Figure 3-4 was replaced with first two and later three glass slide covers because it appeared

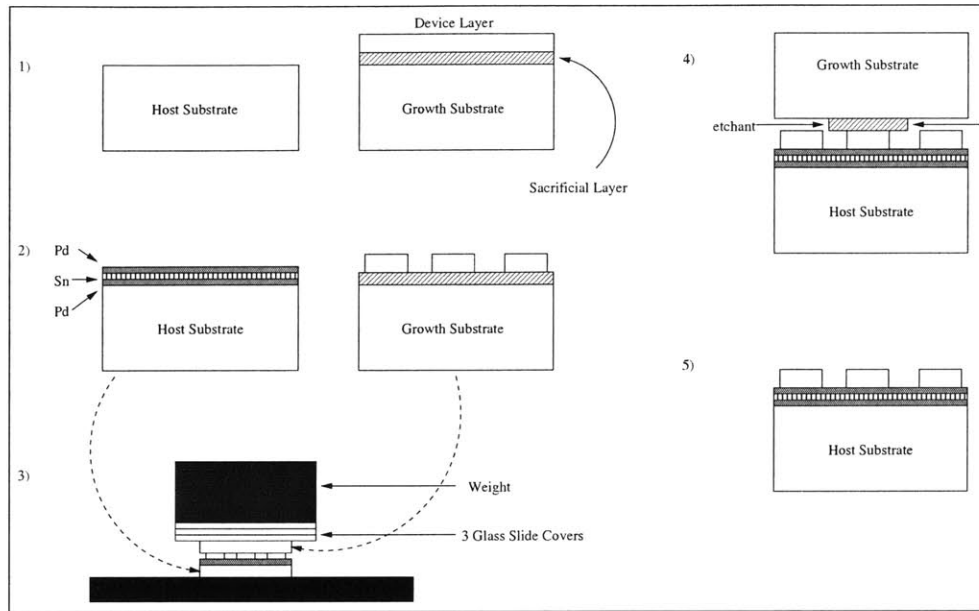


Figure 3-5: Schematic of Final Bonding Procedure

that the slide too easily tilted in a given direction providing non-uniform pressure. Additionally, the brass nut was replaced with a 27 g Swagelock (TM) nut that was chosen for its size (when placed on the slide covers it caused only very slight bowing) as well as for its shape. It had a large surface area that allowed somewhat faster radiative cooling than other aluminum and graphite pieces that were available for use. Finally, the alignment and initial contact of the pieces to be bonded was done in the low-oxygen bonding medium discussed in Section 3.1.3. After being removed they were held together by tweezers and carefully blow-dried with nitrogen to remove as much liquid as possible, and then immediately transferred to the annealer where a forming gas atmosphere was established.

Alternate Pd-Sn-Pd Method

It was thought that the cushioning performance of the tin layer might be improved if it were not trapped between palladium layers. The procedure was conceived as follows. The host substrate is covered with a palladium layer and then a tin layer, and then placed in the low oxygen bonding medium to prevent oxidation of the tin.

Palladium is patterned with the pillar etching mask by lift-off on the device sample. The patterned palladium is used as a mask to etch the pillars. The host substrate and Pd-covered pillars are then bonded as in Figure 3-5. In this way pillars to be bonded make contact with an open face of molten tin, which may help in the cushioning process.

Though palladium alloys with GaAs during deposition (refer to Section 2.4, this thin layer is not sufficiently strong to allow for a successful wet etch. Palladium is a very soft metal and is thus somewhat difficult to work with in lift-off applications. Comparing lift-off of gold and palladium, the latter breaks apart and folds onto itself within 1 minute of being placed in acetone, whereas gold requires mechanical intervention or an ultrasound bath to break apart and away from the underlying photoresist. Likewise, undercutting of the deposited palladium during a wet etch causes the metal to curl up and detach from the host surface. To counteract this problem, the samples were annealed after lift-off to make a more robust mask. Some results of these trials may be found in Section 4.4.

Chapter 4

Results and Discussion

4.1 Palladium Contact Resistance

As described in Section 3.2.1, three different film thickness were deposited through a shadow mask to achieve a qualitative understanding of the conditions needed for good contact resistance. The data is summarized in Table 4.1. The measured quantity was not in fact contact resistance, but the resistance between two adjacent dots of metal. This demonstrates whether the contacts are ohmic and gives a general sense of the relationship between contact resistance and processing conditions.

Sample	Pd Thickness (Å)	Annealing Cycle	Resistance
2	300	350°C, 30 min	Ohmic but unstable Resistance not measured
3A	480	350°C, 30 min	17-21 Ω
3B	480	415°C, 1 min 360°C, 60 min	14.5 Ω
4	600	360°C, 10 min 415°C, 1 min 360°C, 60 min	10 Ω

Table 4.1: Summary of Contact Resistance Measurement

Sample 2 showed instability while the measurements were being taken with the resistance first falling and then rising very quickly. Examination of the sample after

the probes were removed showed black residue indicating that the contacts had been destroyed during measurement (voltage input range approximately 0-1.5 V). Sample 3A showed much better stability and linearity, even in the operating regions where Sample 2 was destroyed. In Samples 3B and 4, 1 minute excursions to 415°C during annealing were used to promote the growth of the ϵ phase that Lin *et al.* [13] recommended as the best phase for contact metallization. In the case of Sample 3B, the resistance was more likely improved by the longer annealing time since the excursion was right at the beginning of the anneal, such that it most likely did not achieve its desired effect as the ϵ phase only appears after initial transformations to palladium-rich phases. The resistance was however improved over that of Sample 3A, and it was able to reach over 2.5 V with good stability before it was destroyed. Finally Sample 4 was held for 10 minutes at the base annealing temperature before its high temperature excursion. It showed the best resistance, stability, and longevity of all of the samples.

These tests did not provide controlled data on the best procedure for contact fabrication. However, they did indicate a low bound on the amount of metal required for a successful contact and that, at least to an undetermined point, applying more metal gives better results. They also suggest that though the initial phase reaction may be rapid (2.4), a longer cycle is beneficial for the equilibration of all of the phases in the contact region. More experimentation is required to confirm whether processing at over 400°C is the key element to better performance.

4.2 Palladium Bonding

Section 3.2.2 described the procedures used in bonding using a single palladium film as an intermediate layer. Two samples were used to test the effectiveness of providing pressure through two slides, and this procedure was quickly discontinued. An interesting artifact of this procedure was observed many weeks after the annealing took place. The surface of the metallized samples became very matte and later developed substantial cracking. An environmental scanning electron microscope (ESEM)

picture of the damage can be seen in Figure 4-1. This effect did not appear on samples where the metal had been deposited through the shadow mask, nor did it occur with any of the later samples, suggesting that it was caused by the stress of the bonding procedure.

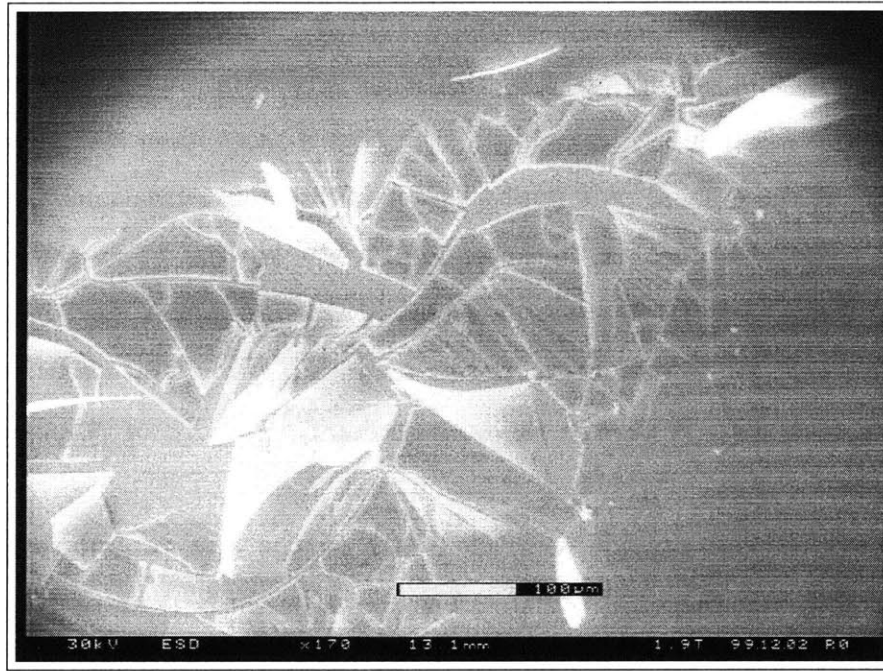


Figure 4-1: ESEM photo of a metallized sample that underwent compression between two glass slides held together with clips.

Two further sets of samples were processed with the third method shown in Figure 3-4. The first was a pair of GaAs substrates, one of which was covered with approximately 650 Å of palladium. While there was no mechanically observed bonding, the metal surface appeared discoloured or dirty in localized areas. Corresponding mirror-image discolourations were apparent on the other sample, indicating that some sort of contact and reaction had occurred, but that it was not uniform or strong enough to hold the samples together.

The final pair of samples processed with the aforementioned method was a GaAs substrate covered with 750 Å of palladium and a GaAs substrate out of which 4 μm pillars had been etched. In the annealing process, the pillar sample was placed

on the graphite strip followed by the metallized sample and the remainder of the assembly. After annealing, the samples appeared to hold together, but some handling and tapping quickly broke them apart. Examination under the microscope revealed that bonding had occurred at one corner of the sample involving just a few pillars.

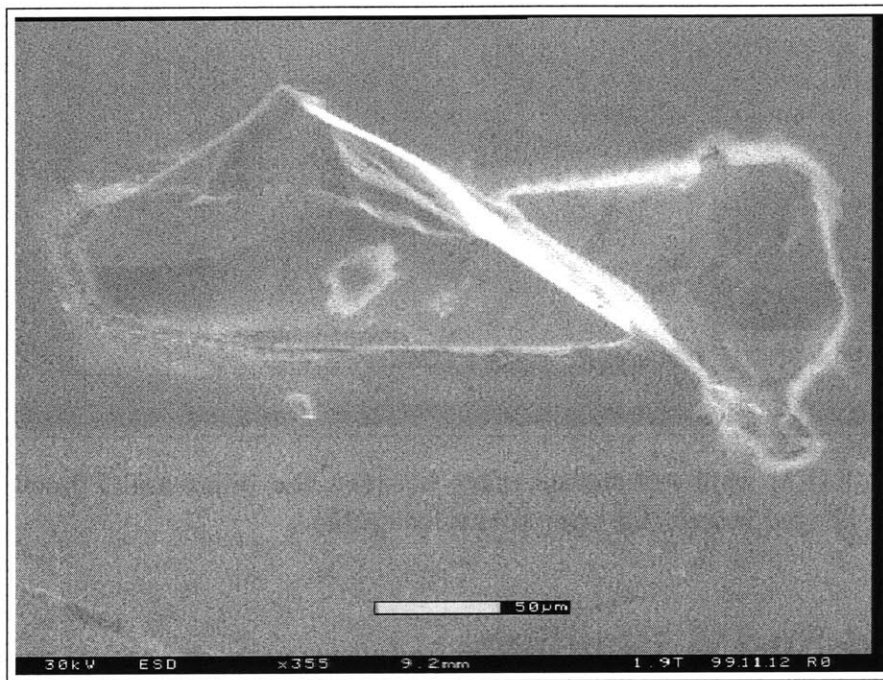


Figure 4-2: ESEM photo of a long pillar that had bonded to the Pd-covered substrate. The two bonding samples were broken apart during handling, resulting in damage to the pillar and demonstrating the strength of the bond.

Figure 4-2 is a photo of the remains of a bonded pillar at the corner of the sample where bonding occurred. The bond was apparently strong enough that it was able to withstand some of the handling shock that cracked the semiconductor. Figure 4-3 shows an enlarged view of the interface between the metal and the two semiconductors. The bottom layer is palladium on top of GaAs. An interfacial alloyed layer is clearly visible, as is a rectangular outline on the metal surface where some contact and perhaps bonding also occurred.

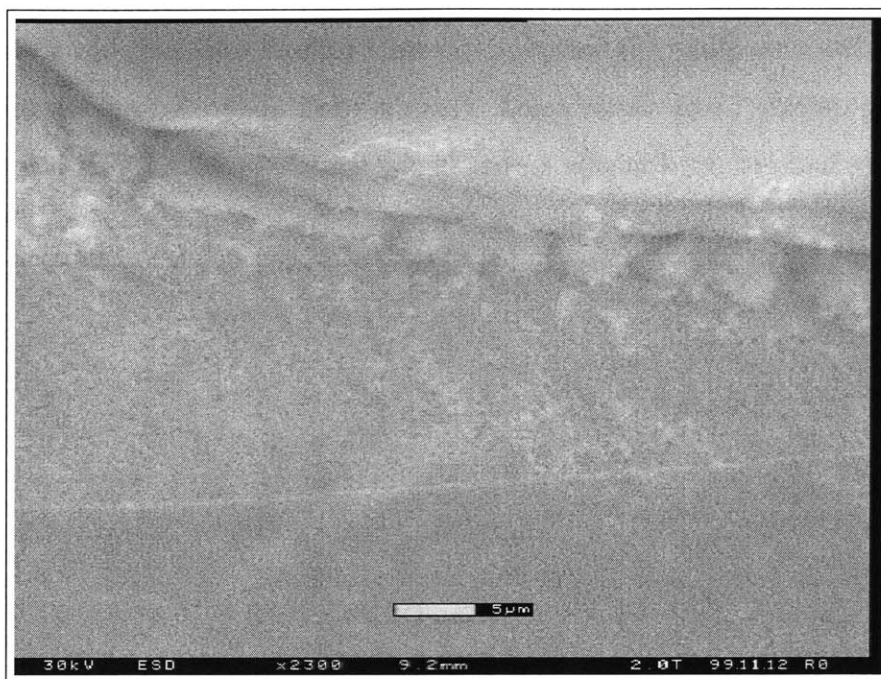


Figure 4-3: ESEM photo of the interface between the pillar and Pd-covered GaAs sample. An alloyed interfacial layer is clearly visible.

4.3 Pd-Sn-Pd Bonding

Many trials were performed with the three layer procedure described in Section 3.2.2 leading to gradual refinements in the process. The more important (or “milestone”) samples are summarized in Table 4.2. The table includes the following information: annealing temperature program, annealing configuration (number of slide covers supporting applied weight, order of samples in the stack), material used for the pillars (GaAs substrate, or the first or second epitaxial materials as described in 3.2.2), and comments as to the quality of the bond. Other samples were bonded as part of the experiment, but ones that repeated previous procedures or that failed for reasons unrelated to the bonding technique (ie. processing errors) are not mentioned. In all of the cases, the films deposited were approximately 1200 Å Pd - 2 kHz Sn - 1200 Å Pd. As previously stated the Sn deposition was not calibrated. Additionally, there is uncertainty in the thickness of the first palladium layer due to a mechanical problem with the evaporator that was used. A mirror used to monitor the evapora-

tion partly obscures the line of sight between the crystal monitor and the evaporation boat (but not between the boat and the sample). However, this is not a very significant detail as the bonding (and all fractures) that took place were all with the outer palladium layer. The thickness of the lower layer would be relevant for further study to optimize contact resistance of the entire structure.

Samples 10 and 12 were both bonded successfully but were not very robust mechanically. In both cases after they were snapped apart, observation revealed that metal transfer onto the pillars was non-uniform. In the case of sample 10, one side had made better contact than the other. Sample 12 showed all of the edges having very good contact and bonding while the centre of the sample had spotty performance at best. These results are partly a function of the glass slides used on which the compressive weight was placed. In the first case a large slide was used, which could easily shift a fraction of a degree in one direction if it was placed off-centre. In the second case two thin slide covers were used that showed some bowing at the edges where they made contact with the weight. For further samples a smaller nut was used such that it would not hang over the edges of the sample providing for better slide flatness. Sample 19 also added a third slide cover for additional stiffness.

Sample	Pillar Material	Annealing Cycle	Stack Configuration	Comments
10	GaAs	365°, 80 min	Glass slide Bottom sample: pillars	First successful attempt Bonded, failed "scotch tape" test
12	Epi1	365°, 80 min	2 Glass slide covers Bottom sample: pillars	Bonded, broke during handling Good metal coverage on side pillars Spotty coverage in centre
13	Epi1	365°, 80 min	2 Glass slide covers Bottom sample: pillars	Bonded well Sample ruined in PA etch Visible alloying
18	Epi1	365°, 70 min	2 Glass slide covers Bottom sample: metal	Bonded well Detached growth substrate
19	Epi2	365°, 60 min	3 Glass slide covers Bottom sample: metal	Bonded well Detached growth substrate Detached pillars have defects

Table 4.2: Summary of Pd-Sn-Pd Bonding Experiments. Epi1 and Epi2 refer to the two materials grown by MBE as described in Section 3.2.2

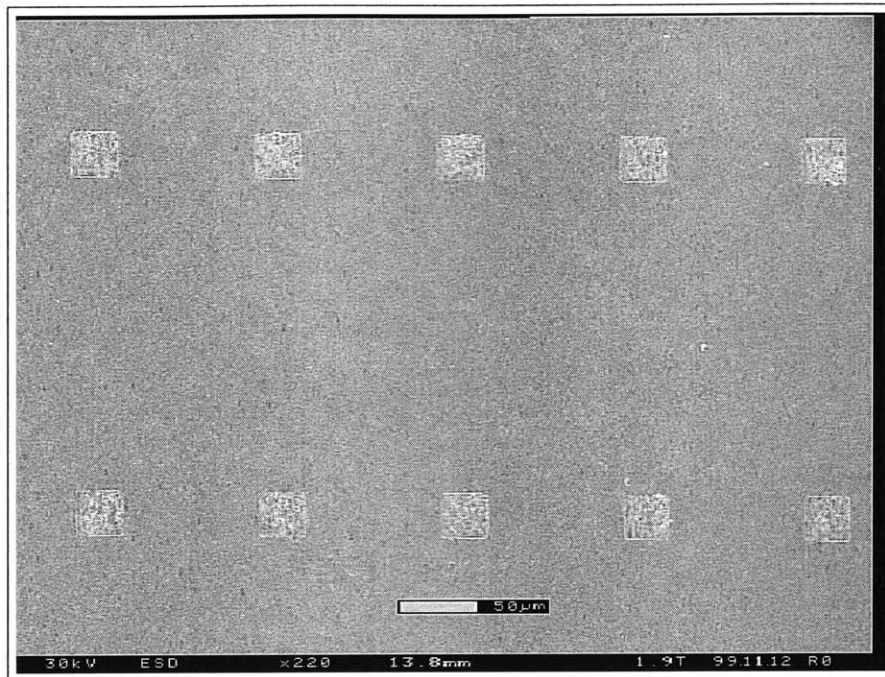


Figure 4-4: ESEM photo of an array of contact areas where bonding had occurred.

Sample 13 was the first bonded sample with epitaxial layers that was mechanically stable enough to attempt separation. Sample 12 had broken during handling related to separation. A PA etch was attempted for the separation (refer to Section 3.1.1), but as there was little experience with this etch it was not sufficiently diluted. This resulted in most of the sample being etched away, including the bonded pillars. However, this was not a terrible occurrence as it allowed for the photographing of the alloyed bonding regions. It also allowed easy visual confirmation that had the sample been separated, the bonding yield would have been very high. Figure 4-4 shows an array of contacts where pillars had successfully been bonded. Figure 4-5 is a closer view at one of the alloyed regions bordering on the unbonded metal. The difference in structure is obvious, and the straight line of the interface indicates good contact at the bonding interface.

Samples 18 and 19 were inspired by the experiments described in Section 4.4. Up to this point, the pillar piece was placed on the graphite strip and the metallized piece on top of the pillars. There was concern that the process was partly being driven

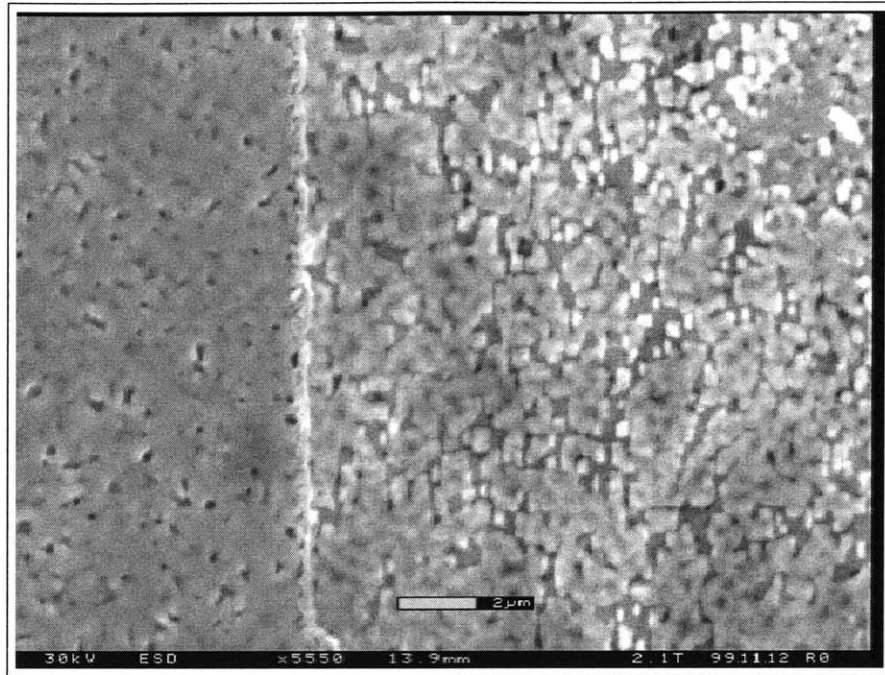


Figure 4-5: ESEM photo of the interface between deposited metal and bonding site. Metal is to the left of the interface, the polycrystalline alloyed region is to the right.

by heat conduction, whereby the pillars with good contact to the metal layer would locally heat the metal very quickly. Surface diffusion of palladium to active bonding sites could deprive some pillars of the palladium they require for contact formation. By placing the metallized piece on the graphite heater, there is an assurance that the whole metal surface at the interface is maintained at the appropriate temperature, which should provide a more uniform bonding surface. Both samples were successfully bonded in this way with very good yield. Although it was not carefully quantified, it appeared from casual observation to be above 70% on Sample 18 and over 90% on Sample 19. A further factor is that Sample 18 was damaged during photolithography, such that some of its pillars could not have been expected to bond even in perfect conditions.

Figures 4-6 and 4-7 are ESEM photos of bonded pillars from Sample 18, showing a number of them bonded (and properly aligned with respect to one another), as well as a single pillars where the alloyed interface is visible. An interesting feature of the

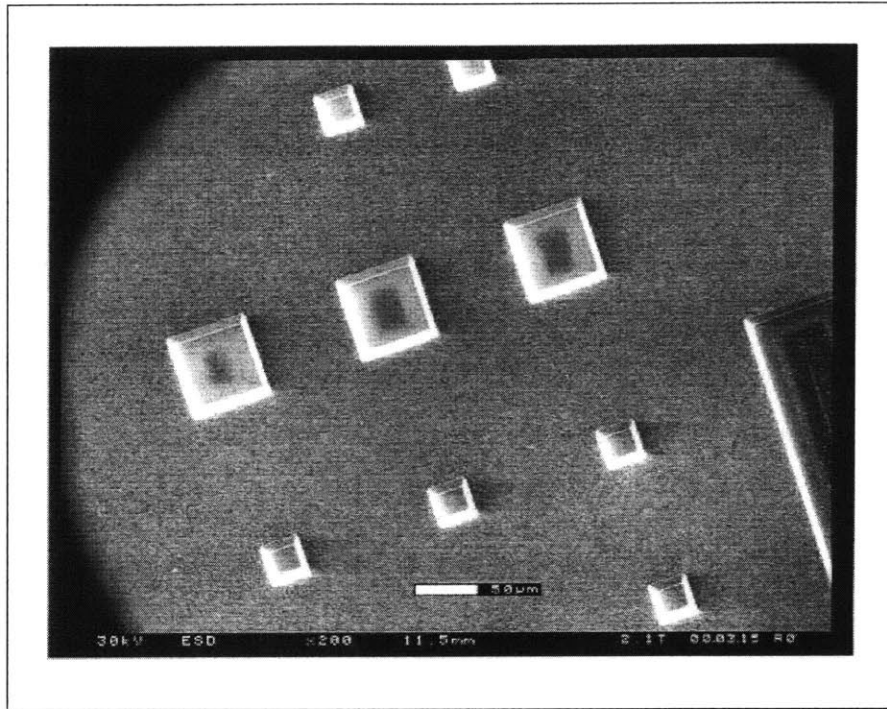


Figure 4-6: ESEM photo of an array of bonded pillars.

pillars is the texture of the top surfaces. Offset a few microns from the outer pillar edge, there is a pattern that appears to be another layer of material. Originally it was thought to be remnants of the AlAs sacrificial layer that had not been completely etched, but an HF dip did not eliminate the feature. EDX analysis confirmed that there was no detectable quantity of aluminum present and that Ga and As were present in an approximately 1:1 ratio, with slight more Ga than As which is consistent with all the processing that took place. It is therefore assumed that the material is simply GaAs, and that the several micron offset from the pillar edges is due to slow wet etching along some crystallographic face during the pillar patterning process.

Figure 4-8 shows a bonded pillar from Sample 19. The sample was tapped several times during the sacrificial layer etch before it detached from the growth substrate. Examination under the microscope found that the pillar tops of that sample all had the same defect pattern (with differing sizes) as seen in the Figures, all oriented in the same direction, meaning that the defects were most likely caused during the dismantling process.

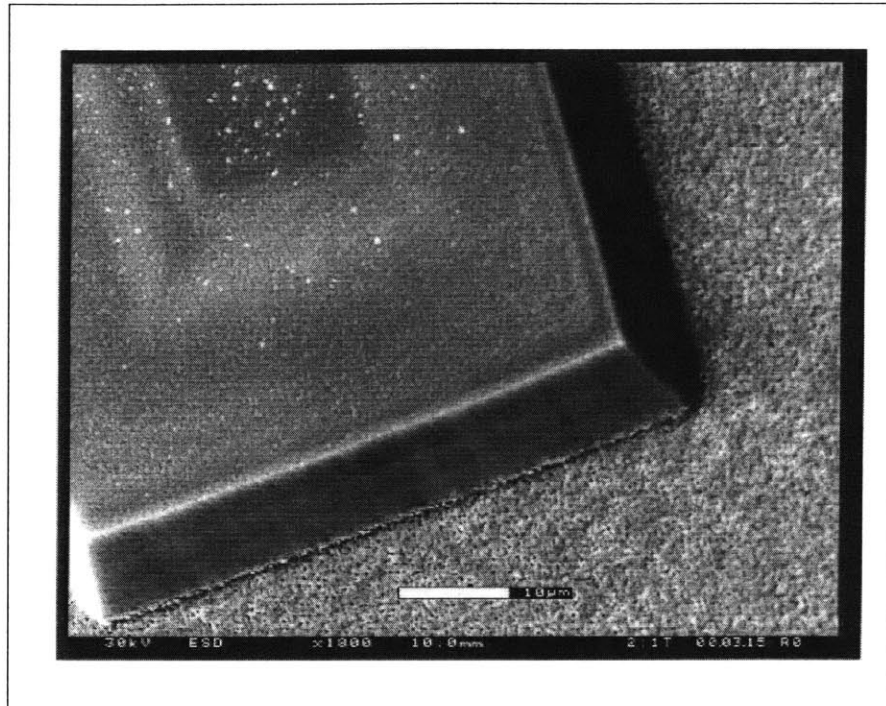


Figure 4-7: ESEM photo of part one bonded pillar. The alloyed bonding layer is clearly discernible

An attempt was made to pattern contacts on top of the pillars of Sample 19 to get a sense of the contact resistance of the bond. This was not successful due to the lack of appropriate mask, but the sample was subjected to all photolithographic processes (30 min dehydration bake, photoresist application, 30 min prebake, exposure, developing, O₂ ashing), metal deposition to form the ohmic contact, lift-off of the contact metallization, and finally rapid thermal annealing of the contact metallization. No pillars were lost during this processing, testifying to the strength and robustness of the bonding.

4.4 Alternate Pd-Sn-Pd Bonding Method

As described in Section 3.2.2, the as-deposited Pd-GaAs reaction creates too weak a layer for the palladium to act as an etch mask. Therefore two attempts were made to anneal the deposited palladium (approximately 120 nm) before etching, and then

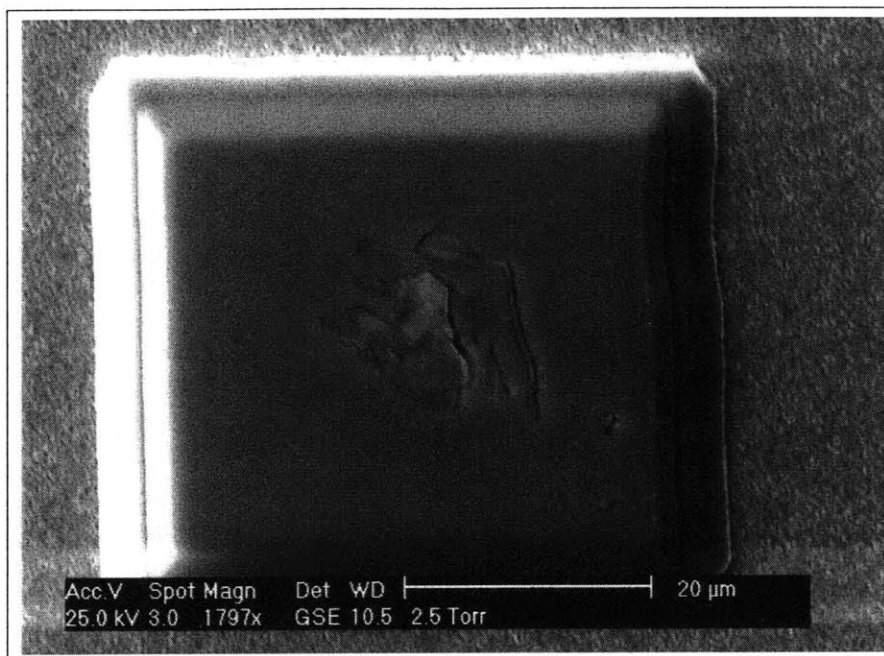


Figure 4-8: ESEM photo of one bonded pillar. The top surface appears damaged or imprinted.

bond the resulting pillars to a host substrate covered by films of palladium and tin (120 nm and 2 kHz respectively). The first attempt (Sample 16) was unsuccessful. A 350°C, 30 min anneal was used, and microscope observation showed a structure where it appeared that all of the palladium had reacted with the GaAs pillar. This was then bonded to the Pd-Sn substrate by a familiar method, but the bond was completely unsuccessful. The areas where the pillars had made contact with the host substrate were clearly visible (discoloured) but not a single pillar was bonded, though contact was made with approximately all of the pillars. This shows that the palladium, once alloyed with the GaAs does not undergo a phase reaction with tin which is consistent with the Pd/Sn contact metallization scheme described in Section 2.4.3.

For the next test (Sample 17), identical deposition conditions were used, but the initial anneal was done at only 275°C for 10 minutes. Observation of the pillar after annealing showed that the surface of the deposited layer was still metallic. The samples were then bonded, and when removed from the annealer, the samples showed some adhesion but quickly broke apart. Once again all the pillars had left impressions

in the Pd-Sn metallization. The difference in this sample (and the reason for the short adhesion) can be seen in Figures 4-9, 4-10, and 4-11.

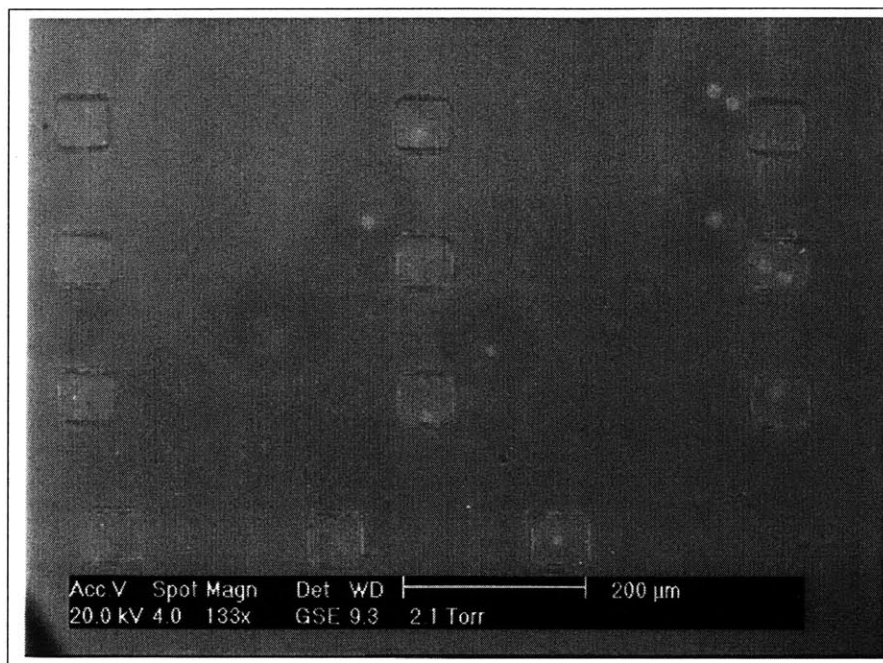


Figure 4-9: ESEM photo of an array of contact areas.

At the outline of where each pillar contacted the host substrate, some material has been bonded to the host substrate. The explanation for this occurrence is as follows. During the initial anneal, some alloying occurred at the Pd-GaAs interface. The wet etch performed some undercutting of the Pd-alloy layer. When the sample was bonded, the remaining palladium preferentially alloyed with the GaAs pillar (ie. the existing phase grew and/or changed to a different phase) rather than with the tin metal. However, the undercut palladium cannot as easily join the alloy since the GaAs that was underneath it was etched away, so it preferentially forms an alloy with the tin (which is liquid at the bonding conditions). The figures also show that one side of the “bonded material” interface is more in focus than the other, meaning that some compression occurred during the bonding process as the pillars pushed against the molten tin.

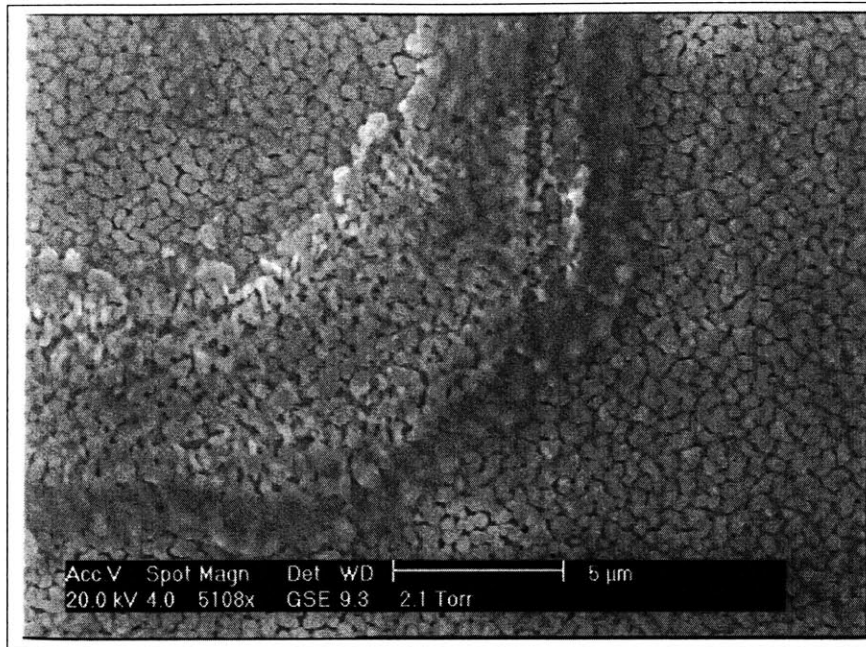


Figure 4-10: ESEM photo of the corner of one contact area, showing what is believed to be palladium bonded to the host substrate.

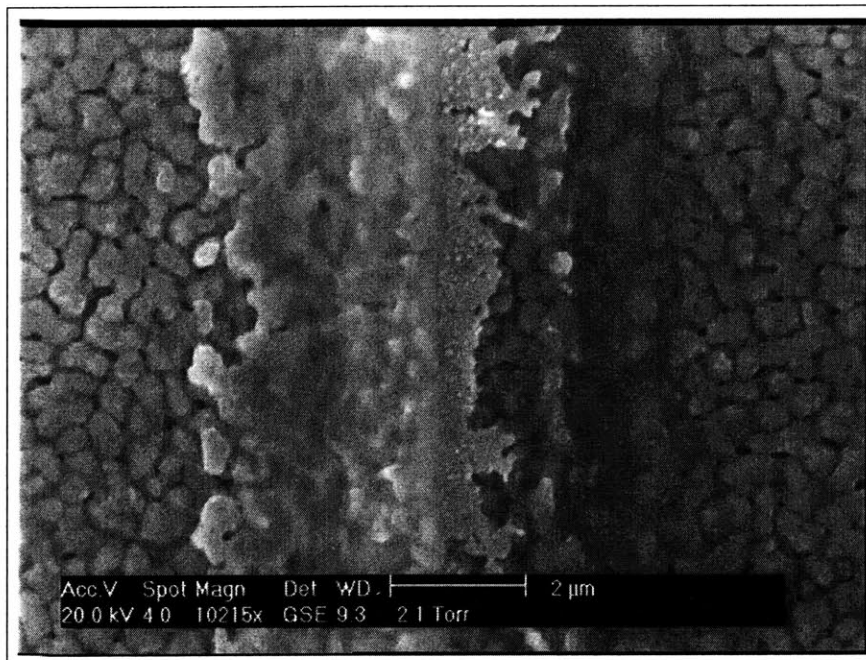


Figure 4-11: ESEM photo of the side of one contact area, showing what is believed to be palladium bonded to the host substrate. Additionally, a difference in focus between the left and right sides of the bonded material is apparent, indicating different heights.

Chapter 5

Conclusions and Future Work

5.1 Project Achievements

Bonding of arrays of a large number of patterned pillars was achieved. The pillar material was grown separately from the host substrate in conditions that would not have been compatible with growth on already fabricated electronics. Bonding of patterned growth material took place in relatively low temperature with low applied pressure (approximately 1 atmosphere), and the bonded material was separated cleanly from the growth substrate. Some intuition into the conditions required for good contact formation was acquired.

The most significant challenge in the course of the experiments was in the end not the materials system itself, which was found to be relatively flexible, but the relatively mundane problem of applying uniform pressure and heat to the samples. Some of the processing struggles may be solved by using more advanced equipment such as the kind expressly designed for wafer bonding. However, the simple equipment forced the creation of a process that was more resilient, such that it is quite sure to work in better equipment.

Though the contact resistance was never measured, the physical bonding itself is an indication that the contact is ohmic. More work is required to find an optimum set of film thicknesses to minimize contact resistance while preserving or enhancing mechanical properties. It is safe to say that an upper bound for the contact resistance

would be half of the resistances found in Section 4.1 (since the measurements went through two contacts), but the presence of tin should help to further decrease this resistance (as discussed in Section 2.4.3), at least in the n-GaAs case. Performance with p-GaAs contacts using tin in the bonding layer still needs to be quantified.

No attempts were made to bond devices to OPTOCHIP substrates because of time and equipment limitations. However, this procedure should be nearly identical to the bonding work that was successfully done. The first step is the cleaning of the dielectric growth windows on the chip, which is fully described by both Ahadian [2] and Crankshaw [10]. The photoresist used for this step need not be removed after this step. The usual Pd-Sn-Pd metallization is then applied and patterned by lift-off (using the photoresist from the well cleaning process). The situation at that point is that the bonding metallization is present at the bottom of the device wells. The patterned devices may then be aligned using an IR aligner (unreacted palladium has a very high reflectivity [15]), placed into contact, and bonded using a familiar process. Substrate removal could be performed by etching away the entire growth substrate. Alternately photoresist could be flowed between the chip and growth substrate to protect the chip's dielectric material and the two could be separated by an HF etch as was performed in this study.

5.2 Bonding III-V Devices to Silicon VLSI

An alternate technique to bonding devices directly to the VLSI substrate, as was done in this study, is to bond them to metal contact pads on the chip. This technique has been attempted in a number of studies [11, 20]. These methods however invariably carry a high overhead in terms the variety of metal layers required for adhesion, good electrical contact, and diffusion barriers.

There have been studies in the past regarding the suitability of palladium silicide contacts for VLSI applications [21]. The use of this system was ultimately not as easy or cost-effective as the aluminum metallization scheme currently in use, but it provides an avenue for a new bonding procedure. As with GaAs, palladium form

a Pd-rich alloy with silicon at relatively low temperatures (270°C). The problem of spiking does not appear to affect this system as it is once again palladium that is the dominant moving species.

These interesting qualities suggest that a very similar system to the one used in this study could be used for bonding devices onto silicon. Problems that would require investigation include how devices grown on a III-V substrate would be aligned with a silicon substrate during bonding since the substrates would behave differently upon heating. Another issue is how well the difference in thermal expansion coefficients would be absorbed by the metallization. This problem is certainly not as serious, as Tan [15] successfully bonded two different III-V compounds using just a palladium intermediary layer and did not report thermal stress problems.

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