Large-Signal Modeling of Bulk and SOI RF Power LDMOS FETs

By Tassanee Payakapan

Submitted to the Department of Electrical Engineering and Computer Science in Partial Fulfillment of the Requirements for the Degrees of Bachelor of Science in Electrical Engineering and Master of Engineering in Electrical Engineering at the Massachusetts Institute of Technology

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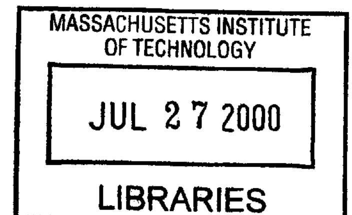

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Abstract

Radio frequency (RF) power devices are critical components of the transmitter of a wireless system, such as a cell phone. There is a need for a model to accurately predict power performance of these RF power devices for circuit and device design purposes. The Root Model, a look-up table description of current and charge of a device, is pursued here because it can be extracted automatically, which saves time and money. While the Root Model, has served as a useful model for bulk power metal-oxide-semiconductor field effect transistors (MOSFET), it has not been tested for silicon-on-insulator (SOI) power MOSFETs. The objective of this thesis is to determine whether the Root Model is useful for modeling these devices. We have used both bulk and SOI laterally diffused metal oxide semiconductor (LDMOS) devices fabricated at MIT. Device DC current and S-parameter measurements at 1.9 GHz are utilized to extract the Root Model. This model is then imported into a harmonic balance simulator to obtain the RF power figures of merit, such as output power, gain, power added efficiency (PAE), bias current, and IM3. These parameters have been separately measured in a load-pull setup at 1.9 GHz. The simulation results indicate a relatively good fit with RF power load-pull measurements for output power and gain. Simulations for PAE follows the general shape of the load-pull measurements, but the peak PAE of the simulations are consistently lower than the measurements. Bias current simulations also show some mismatch with measurements. These mismatches appear to arise from lack of measurement data during Root Model extraction at high gate voltages. IM3 simulations do not match the load-pull measurements very well, and more research is needed to determine if the Root Model can be used to predict IM3.

Thesis Supervisor: Jesús A. del Alamo
Title: Professor of Electrical Engineering

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It is my pleasure to record here two other contributors. The first is Chuck Webster from IBM in Burlington, VT who let us measure the devices on his load-pull measurement system. This research could not have been completed without his gracious cooperation. The second is Hewlett-Packard Company, now Agilent Technologies, for donating both IC-CAP and Libra software that was used to extract and simulate the Root Model.

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Chapter 1

INTRODUCTION

1.1 SOI LDMOS Devices and Modeling

Currently there is a great deal of research interest in integrated circuits (IC) technologies that will enable single-chip radio frequency (RF) wireless systems in the future. By integrating the entire system onto a single chip, there will be a decrease in die count, increase in performance, simpler packaging, better reliability, and, thus, presumably lower cost. While there are many advantages to a system on a chip (SOC) design, there are disadvantages as well. The initial research and development costs to design a single-chip RF wireless system can be large. In addition, with SOC, the time to improve a design for the next generation of products is much longer, since the entire chip has to be redesigned instead of a few components being modified. For practical purposes, the single-chip solution needs to be capable of handling RF, baseband, analog, and digital functions. At present, a few platforms are viable for single-chip wireless systems, including bulk silicon (Si) complementary metal oxide semiconductor (CMOS), Si or silicon-germanium (SiGe) BiCMOS, and silicon-on-insulator (SOI), as discussed below.

Although Si CMOS, with its process technology studied and tested extensively over the years, is a possible choice for SOC design, Si has low carrier mobility, which limits the speed of Si devices and makes Si problematic for RF and microwave applications. Another drawback to selecting CMOS for RF wireless SOC design is its limited power capability because CMOS devices are designed to operate at low voltages. Some work has been done to develop dedicated RF CMOS technologies by using different gate materials, such as nitrous oxide (N_2O) to reduce 1/f noise[1] and aluminum (Al) shorted metal-silicide/Si to improve f_T (unity gain cutoff frequency) and reduce on-state resistance[2]. In addition, there are problems with isolation and integration of passive components in bulk Si technology.

Alternatively, Si or SiGe BiCMOS can serve as a platform for SOC wireless systems. BiCMOS, which integrates bipolar and CMOS devices, allows for analog and RF circuits to be designed using bipolar technology. However, there are concerns with Si and SiGe bipolar transistors for RF power devices in terms of output power levels and linearity. Additionally, BiCMOS is very expensive, due to its complex process with many masks. Using SiGe instead of Si can improve the performance of the device, since SiGe heterojunction bipolar transistors (HBTs) are bandgap-engineered devices that allow for the Ge doping and profile to be adjusted to achieve better performance[3].

Among the platforms considered for SOC design, SOI is a technology that deposits a layer of oxide underneath the active region of the device and uses CMOS technology. There are several benefits to using SOI for a single-chip wireless system. SOI devices have a smaller junction capacitance than bulk devices[4], which gives SOI an advantage in low voltage and low power operation. This is especially useful for wireless communications applications. The lower output capacitance is also important since a power amplifier circuit usually has a matching network between the output transistor and the load to maximize output power and efficiency. A smaller output capacitance requires a smaller matching inductance and thereby, permits less power loss in the matching network built around the power amplifier. In addition, SOI has full dielectric isolation and cannot latchup. Because of this, SOI can have a high resistance substrate, which will reduce crosstalk up to 10 GHz[5]. Improved crosstalk is key to a system on a chip design with RF and analog circuits integrated with high speed digital circuits on the same substrate. In addition, with more flexibility in substrate resistivity, it should be possible to design high quality passive components on SOI. Therefore, SOI holds great potential in integrating a wide range of functions, RF, baseband, analog, and digital, onto a single chip.

Using SOI, it is possible to integrate a high-performance laterally diffused metal oxide semiconductor field effect transistor (LDMOS FET) for the RF power amplifier function, one of the crucial components of a wireless system. LDMOS devices have already been

established as the preferred Si RF power amplifier device because of its outstanding linearity, power level, and efficiency at lower operating voltages[6].

As part of Jim Fiorenza's Ph.D. thesis at MIT, LDMOS devices have been evaluated to determine if SOI substrate can improve their performance for future single-chip RF wireless systems. Figure 1-1 shows a cross-section of a SOI LDMOS device that is modeled in this research. In following the SOC design methodology, a design constraint is imposed to make the SOI technology compatible with CMOS. As a result, standard full-dose separation by implantation of oxygen (SIMOX) is used as the substrate. The specifications for these devices are tailored to future wireless systems: 1 W output power, 3.6 V supply voltage, 1.9 GHz operation frequency, and high power efficiency. These are classical LDMOS devices with a graded channel to enhance RF performance, prevent punchthrough, allow for control of threshold voltage, and increase device transconductance (g_m). The lightly doped drain region decreases the electric field at the drain side of the device and optimizes the on-state drain to source resistance R_{ds}(on), on- and off-state breakdown, and drain to gate capacitance (C_{dg})[7]. These devices also have a body contact to better control the substrate, thus, preventing the 'kink' effect and premature breakdown that are common in SOI MOSFETs. The SOI LDMOS devices are fabricated with a polysilicon gate, which have higher resistance than a metal gate. Since devices with wide gate widths exhibit poor gain, they are not modeled in this research.

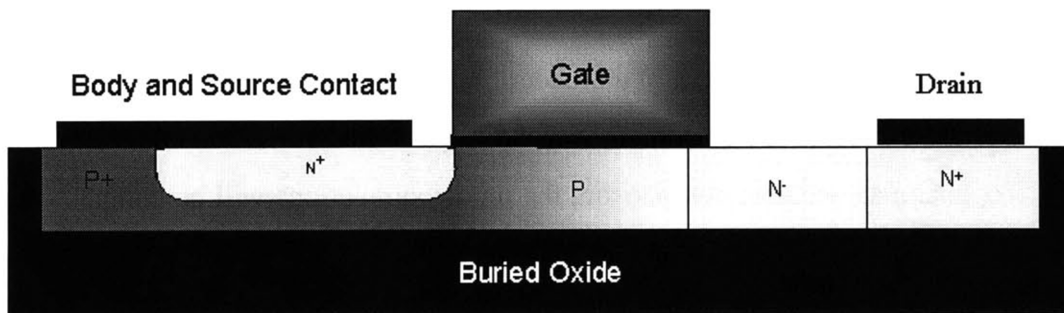

Figure 1-1: Cross-section of SOI LDMOS FETs.

1.2 Motivation

A model to accurately simulate power performance is needed to evaluate the merits of a device for portable communications products for which output power specifications are the main figures of merit. As an integral component of circuit design, device modeling allows a circuit designer to predict the behavior of circuits in meeting the performance specifications necessary for a particular application. A useful device model must be scalable, so that circuit designers are able to use devices with different widths depending on its function. Furthermore, a model can provide additional understanding of device behavior, which contributes to the development of the next generation of devices.

One such model for RF power devices is the Root Model, which is an automatically extracted and accurate model for three-terminal devices. The Root Model uses current and S-parameter measurements from a device to compute a lookup table description of the current and charge of the device. Thus, the advantages of the Root Model include its ease of generation, accuracy for device non-linearities, and generality to a variety of device processes and technologies. Since the Root Model allows for automatic model extraction, time and monetary savings in obtaining a model can be significant. The disadvantages, however, are that it can only be used for two- or three-terminal devices and that it may not be as accurate when applied to small-signals.

The Root Model has been shown to perform well for bulk devices[8], but has not been tested for SOI devices. Therefore, the primary objective of this thesis is to determine the validity of the Root Model as part of a broader framework in which device models for RF power amplifier devices are generated using bulk and SOI LDMOS devices fabricated at MIT. To ensure an accurate comparison, the model simulations will be compared to RF power measurements obtained from a load-pull system. The choice of this test is strongly supported by the following statement:

> "The most stringent test that can be applied to a simulator is to simulate a load-pull test, and results from such comparisons (reluctantly and rarely performed, it seems, requiring substantial cooperation between antagonistic parties) are at best only fair."[9]

Previous research results on modeling LDMOS devices indicate that a look-up table model, using a different type of spline interpolation than the Root Model approach, is useful[10]. In addition, a harmonic-balance simulator has been developed for power LDMOS devices, with biasing circuit and matching network, which solves semiconductor partial differential equations[11]. The devices modeled had a p+ sinker connecting the source and substrate and a metal field plate to reduce the electric fields at the edge of the gate to improve breakdown and reduce C_{dg}.

1.3 Outline

This thesis is organized into six chapters. Chapter 2 starts by describing the bulk and SOI LDMOS devices as well as the Root Model. It continues with the measurement setup and describes how the DC current and S-parameter measurements are taken using IC-CAP. Sample measurement results are shown in addition to a discussion of how the Root Model is extracted from the measurements.

Chapter 3 describes the simulation environment in Libra, a harmonic balance simulator, used to test the Root Model. This is followed by a description of the test benches set up for the large-signal RF power figures of merit. The definitions for all of the figures of merit are also given, together with sample simulation results.

In Chapter 4, the load-pull measurements, completed at IBM in Burlington, VT, are discussed. The measurements taken with the load-pull system correspond to the simulations run in Libra. Sample measurement results are also provided as part of Chapter 4.

Chapter 5 contains the results and key findings of this research. The comparative analysis between the Libra simulations and load-pull measurements is presented for both bulk and SOI devices. The chapter also includes a discussion about the possible reasons why certain figures of merit are not modeled well.

This thesis concludes with a summary of the results and suggestions for future research in Chapter 6.

Chapter 2

ROOT MODEL GENERATION

2.1 Overview

This chapter begins with background information on LDMOS device technology, followed by a detailed description of the Root Model, including its extraction process. The chapter discusses the measurement setup and how each measurement is taken to obtain the Root Model. For easy reference, sample measurement results are shown throughout this chapter. Since the Root Model is used to model both bulk and SOI LDMOS devices, the applicability of the Root Model for these devices will later be determined through simulations using Libra, as described in Chapter 3.

2.2 Device Technology

The devices used in this research have been fabricated by Jim Fiorenza at MIT. These devices are bulk and SOI LDMOS devices, shown in Figure 1-1, that have been optimized for high frequency and high power applications.

Three different types of devices are modeled in this research. Table 2-1 lists the device figures of merit for a device with a gate length of 0.7 μm and a gate width of 400 μm (10x40 μm). f_{MAX} is less than f_T because the gate resistance of these devices is high since they have a polysilicon gate. Table 2-2 lists the device location on the wafer as well as the biasing point for each device. The wafers are labeled 055, RB7, and RB3. The first two follow the same processing steps on two different types of wafers, bulk silicon (055) and SOI (RB7). To achieve adequate results, a minimum of two devices from each wafer is tested in this research. The third type of device (RB3) is fabricated using the same process on SOI, except that the drive time for the body implant is halved. This improves the characteristics of the device by increasing the transconductance (g_m). Three devices from this wafer are tested in this study. All of the devices modeled, except for the device

modeled in Section 5.3.3 and 5.4, have a gate length of 0.7 μm, a gate width of 800 μm, consisting of 20 fingers with a width of 40 μm.

WAFER	f_T (GHz)	f_{MAX} (Hz)	BV_{OFF} (V)	BV_{ON} (V)	V_T (V)
055	10.7	8.0	17	15	1.5
RB7	12.5	8.5	22	9	1.5
RB3	11.8	5.9	20	9	0.75

Table 2-1: Device characteristics.

WAFER	ROW	COLUMN	V_D (V)	V_G (V)
055	4	3	3.6	2.651
055	4	4	3.6	2.800
RB7	7	8	3.6	2.621
RB7	8	7	3.6	2.640
RB3	7	8	3.6	2.000
RB3	7	7	3.6	1.580
RB3	6	8	3.6	1.600

Table 2-2: Device location on wafer and bias point.

2.3 Root Model Description

The Root Model, developed by David Root at Hewlett-Packard Company[12], is used to model devices based on current and S-parameter measurements[13,14]. It is a large-signal FET model useful for modeling three-terminal devices, where substrate effects are not part of the model. A diagram of the three-terminal device as modeled in the Root Model is shown in Figure 2-1.

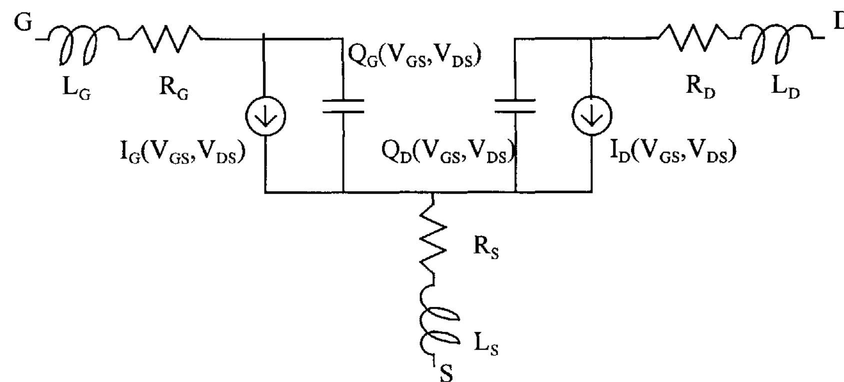

Figure 2-1: Root Model representation of a three-terminal device.

Basically, the Root Model is a look-up table, sketched in Table 2-3, of current, I_D and I_G, and voltage controlled charge sources (VCQS)[15], Q_G and Q_D, as a function of both the gate to source voltage (V_{GS}) and the drain to source voltage (V_{DS}). A VCQS is a reactive analog of a voltage controlled current source commonly used in circuit models. A transcapacitance, obtained by linearizing a VCQS, is a reactive analog of the transconductance.

V_{DS}	V_{GS}	I_D	I_G	Q_D	Q_G	I_D^{high}
$V_{DS}(1)$	$V_{GS}(1)$	$I_D(1)$	$I_G(1)$	$Q_D(1)$	$Q_G(1)$	$I_D^{high}(1)$
$V_{DS}(2)$	$V_{GS}(2)$	$I_D(2)$	$I_G(2)$	$Q_D(2)$	$Q_G(2)$	$I_D^{high}(2)$
...	...	...	...	...	...	...

Table 2-3: Sample Root Model table.

IC-CAP, a software package from Hewlett-Packard[16], is set up to extract the Root Model using I-V data and S-parameters at different bias points. Since the device is a MOSFET, the gate current, I_G, is zero[17], because there is no current through the gate oxide. The drain current, $I_D(t)$, is calculated by[18]:

$$I_D(t) = h_2^{(0)} I_D^{low} + \frac{d}{dt} Q_D + (1 - h_2^{(0)}) I_D^{high} \qquad \textit{Equation 2-1}$$

$h_i^{(n)}$ is a dynamical operator, with τ as the relaxation time to model the thermal and trap time constants, which acts on the nonlinear bias-dependent constitutive relations and can be written:

$$h_1^{(0)} = 1 \qquad \textit{Equation 2-2}$$

$$h_1^{(1)} = h_2^{(1)} = \frac{d}{dt} \qquad \textit{Equation 2-3}$$

$$h_2^{(0)} = \left(1 + \tau \frac{d}{dt}\right)^{-1} \qquad \textit{Equation 2-4}$$

$$h_2^{(2)} = \left(1 + \tau \frac{d}{dt}\right)^{-1} \tau \frac{d}{dt} = 1 - h_2^{(0)}$$ *Equation 2-5*

While I_D^{low} values, which contribute to $I_D(t)$ at frequencies below $1/\tau$, are obtained directly from the DC current data, I_D^{high} values, which contribute to $I_D(t)$ at frequencies above $1/\tau$, is represented by:

$$I_D^{high} = \int_{V_{GS0}}^{V_{GS}} \frac{\partial}{\partial V_{GS}} \mathrm{Re}[Y_{21}](V_{GS}', V_{DS}, \omega) dV_{GS}' + \int_{V_{DS0}}^{V_{DS}} \frac{\partial}{\partial V_{DS}} \mathrm{Re}[Y_{22}](V_{GS}, V_{DS}', \omega) dV_{DS}'$$

Equation 2-6

The charge values are computed from the measured S-parameters as described step-by-step below. The first step involves the procedure to calculate total gate charge, Q_G[19]. After the S-parameters are transformed into Y-parameters[20], the imaginary part of Y_{11} ($\mathrm{Im}[Y_{11}]$) is integrated over the gate voltage, V_{GS}, to obtain Q_G, as represented by:

$$\frac{\partial}{\partial V_{GS}} Q_G(V_{GS}, V_{DS})\Big|_{V_{GS}, V_{DS}} = \frac{\mathrm{Im}[Y_{11}](V_{GS}, V_{DS}, \omega)}{\omega}$$ *Equation 2-7*

Then the change in Q_G with respect to drain voltage, V_{DS}, is calculated from $\mathrm{Im}[Y_{12}]$ as shown by:

$$\frac{\partial}{\partial V_{DS}} Q_G(V_{GS}, V_{DS})\Big|_{V_{GS}, V_{DS}} = \frac{\mathrm{Im}[Y_{12}](V_{GS}, V_{DS}, \omega)}{\omega}$$ *Equation 2-8*

The total gate charge, Q_G, is obtained by integrating the two previously mentioned equations with respect to V_{GS} and V_{DS}, respectively, and can be written:

$$Q_G(V_{GS},V_{DS}) = \int_{V_{GS0}}^{V_{GS}} \frac{\partial}{\partial V_{GS}} Q_G\Big|_{V_{DS},V_{GS}'} dV_{GS}' + \int_{V_{DS0}}^{V_{DS}} \frac{\partial}{\partial V_{DS}} Q_G\Big|_{V_{GS},V_{DS}'} dV_{DS}' \quad \textit{Equation 2-9}$$

The starting point of integration can affect the actual path in voltage space used to define the integral[21]. The Root Model assumes that the charge and current vector fields are conservative[22]. If this requirement is not fulfilled, then the charge or current accumulates with every loop transversal, which may lead to the simulation crashing.

Similarly to Q_G, the total drain charge, Q_D, is calculated below:

$$\frac{\partial}{\partial V_{GS}} Q_D(V_{GS},V_{DS})\Big|_{V_{GS},V_{DS}} = \frac{\mathrm{Im}[Y_{21}](V_{GS},V_{DS},\omega)}{\omega} \quad \textit{Equation 2-10}$$

$$\frac{\partial}{\partial V_{DS}} Q_D(V_{GS},V_{DS})\Big|_{V_{GS},V_{DS}} = \frac{\mathrm{Im}[Y_{22}](V_{GS},V_{DS},\omega)}{\omega} \quad \textit{Equation 2-11}$$

$$Q_D(V_{GS},V_{DS}) = \int_{V_{GS0}}^{V_{GS}} \frac{\partial}{\partial V_{GS}} Q_D\Big|_{V_{DS},V_{GS}'} dV_{GS}' + \int_{V_{DS0}}^{V_{DS}} \frac{\partial}{\partial V_{DS}} Q_D\Big|_{V_{GS},V_{DS}'} dV_{DS}' \quad \textit{Equation 2-12}$$

The Root Model also incorporates values for the parasitic inductances and resistances. De-embedding the effects of parasitic elements makes the resulting intrinsic capacitances and conductances much less frequency dependent. Thus, the Root Model can be extracted at a single frequency, while still simulating accurately over a large frequency range. While the user inputs inductor values, the intrinsic parasitic resistance values are measured using a cold FET measurement[23,24]. With the device unbiased (setting both the gate and drain biases to zero), as displayed in Figure 2-2, the S-parameters across the frequency range are measured. Under these conditions, the device is turned off with the

transconductance and drain conductance being negligible. Specifically, the device consists of only parasitic capacitances and resistances. Accordingly, IC-CAP calculates the parasitic resistances of the device, after transforming S-parameters into Z-parameters[25], as shown below:

$$\mathrm{Re}[Z_{11}] = R_G + R_S \qquad \textit{Equation 2-13}$$

$$\mathrm{Re}[Z_{12}] = \mathrm{Re}[Z_{21}] = R_S \qquad \textit{Equation 2-14}$$

$$\mathrm{Re}[Z_{22}] = R_D + R_S \qquad \textit{Equation 2-15}$$

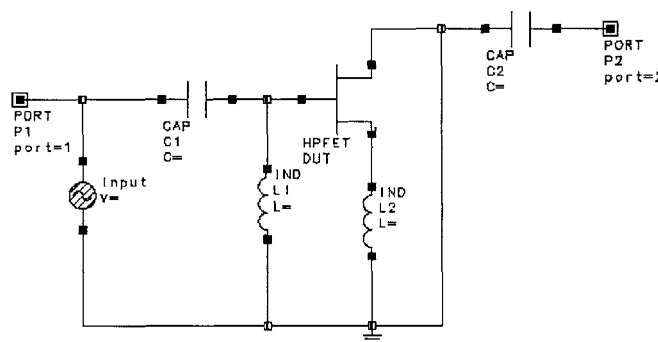

Figure 2-2: Setup for parasitics extraction of the device.

The resulting parasitic resistances, R_G, R_D, and R_S, are then used in the R matrix along with average DC current, $\tilde{I}_G^{DC}$ and $\tilde{I}_D^{DC}$, to compute the intrinsic voltages of the device, V_{GS} and V_{DS}, as shown below:

$$\begin{bmatrix} V_{GS} \\ V_{DS} \end{bmatrix} = \begin{bmatrix} V_{GS}^{ext} \\ V_{DS}^{ext} \end{bmatrix} - [R] \times \begin{bmatrix} \tilde{I}_G^{DC}(V_{GS}^{ext}, V_{DS}^{ext}) \\ \tilde{I}_D^{DC}(V_{GS}^{ext}, V_{DS}^{ext}) \end{bmatrix} \qquad \textit{Equation 2-16}$$

2.4 Measurement Setup

An automated system, as shown in Figure 2-3, is initially set up to extract current and S-parameter measurements from bulk and SOI LDMOS devices to generate the Root Model

for each device. The device is probed on a Cascade Microtech Summit 9600 Thermal Probe Station using GGB microwave probes with 100 μm pitch. IC-CAP, running on a Sun Ultra 5 workstation, is connected to the HP 8753 network analyzer and the HP 4155 Semiconductor Parametric Analyzer (used to bias the device). The HP Root MOSFET Model Generator Program (HP Root MOS) of IC-CAP is then used to control the instruments to take measurements of the device to generate the Root Model.

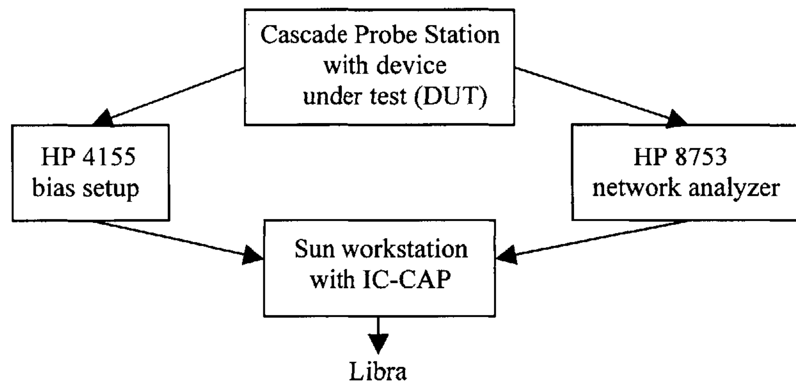

Figure 2-3: Experimental setup.

This automatic system functions as the data acquisition system and calculates the safe operating conditions of the device based on device current and power compliances provided[26]. The system takes data adaptively at multiple bias points, taking more densely spaced points in the nonlinear regions and fewer points in the linear regions. The model is then generated mathematically and stored as a table of current and charge components at each bias point. The generated file can be read by Libra and simulated to compare with actual load-pull measurements to verify the accuracy of the model.

2.5 Model Extraction

When the measurement setup is connected, IC-CAP is used to verify the device, extract the parasitics, acquire the data, and generate the Root Model.

2.5.1 Initializing Device Parameters, Calibrating the HP 8753, and Measuring the Port Series Resistance

To start using the HP Root MOS, certain parameters must be initialized. The program requires information about the device, such as number of gate fingers and gate width. This is also where values for extrinsic parasitic capacitances and inductances can be entered into the model. For this research, all extrinsic parasitic capacitances and inductances are set to zero to match the load-pull measurement setup, since the measurements taken at IBM include what is measured from probe tip to probe tip, including the pads of the device. The frequency at which the model is generated is also set at this point. For this research the frequency is set at 1.9 GHz, which is the frequency at which many cellular phones operate.

The HP 8753 must be calibrated in order to get good S-parameter measurements to obtain a valid model. The HP Root MOS measurement procedure requires two different calibrations: a broadband calibration and a continuous wave (CW) calibration. The broadband calibration is used for S-parameter pre-verification of the device and for parasitics measurements. The CW calibration is used for data acquisition of the S-parameters at the different bias points. One of the frequencies used in the broadband calibration must be the CW frequency. The HP 8753 is calibrated from 200 MHz to 6 GHz for the broadband calibration and at 1.9 GHz for the CW calibration.

The port series resistance can be measured by placing the probes on the short circuit standard of a calibration substrate. A sweep of current is done on both probes and the voltage is measured in order to compute the port series resistance, using Ohm's law (V = IR).

2.5.2 Pre-Verification of the Device

At this point, the device is installed and pre-verified. Initially, the DC characteristics of the device are obtained. This is done by sweeping the drain voltage and stepping the gate voltage and measuring the drain and gate currents to get the I-V curve for the device.

Figure 2-4 presents the device bias configuration for this measurement. Figure 2-5 exhibits a sample I-V curve for a SOI (RB7) device. By considering the DC characteristics of the device and the device limits, the measurement range for the main data acquisition can be determined. Also, this is a simple way of verifying that the device works as expected.

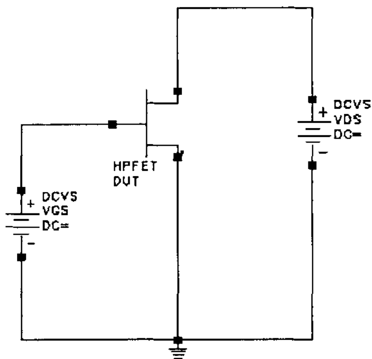

Figure 2-4: Setup for DC pre-verification of the device.

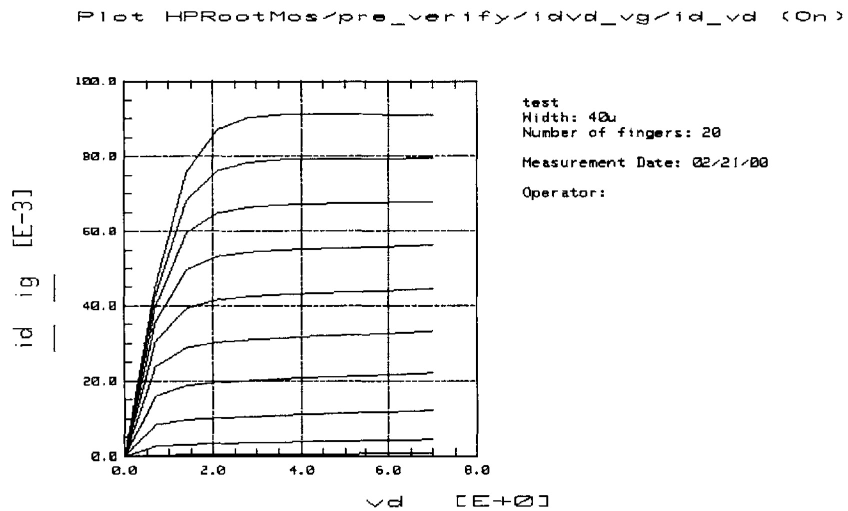

Figure 2-5: Sample drain current (A) and drain to source voltage (V) characteristics with V_{GS} stepped from 0 to 3.75V in 0.25V steps.

The S-parameters of the device are also pre-verified. Using a broadband sweep of frequencies with a sweep of drain bias and a step of gate bias, the S-parameters of the device are measured. The device bias configuration for this measurement is shown in Figure 2-6. The capacitor C1 and inductor L1 compose the bias T at the gate of the device, while C2 and L2 form the bias T at the drain of the device. A bias T is used to isolate the DC signal from the RF signal. At low frequencies, the inductor and capacitor behave like a short and an open circuit, respectively, so the device sees a DC source. At high frequencies, the inductor behaves like an open circuit, while the capacitor acts like a short circuit to only pass the RF signal. This measurement is useful in determining device behavior at high frequencies. Figures 2-7 and 2-8 show the measured S-parameters for the sample device.

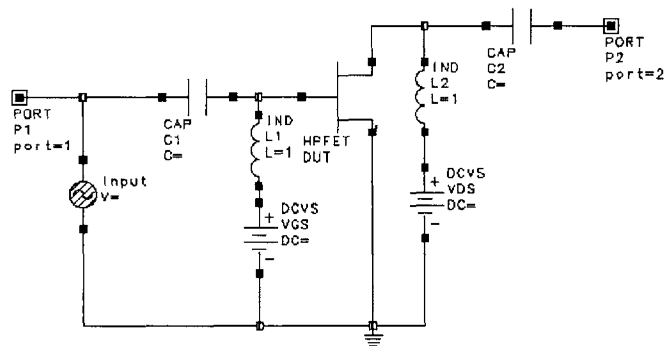

Figure 2-6: Setup for S-parameter pre-verification of the device.

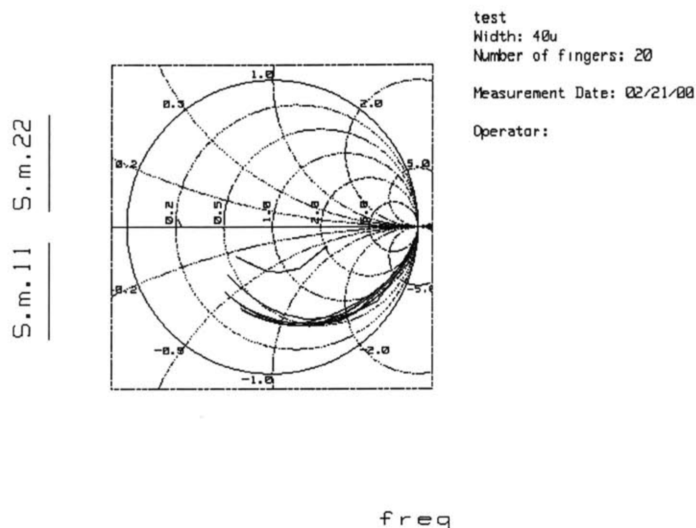

Figure 2-7: Sample S_{11} and S_{22} data at different V_{GS} and V_{DS} values.

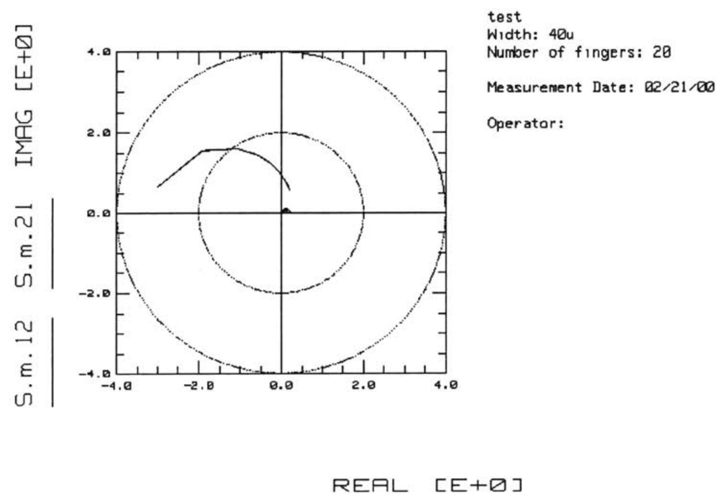

Figure 2-8: Sample S_{12} and S_{21} data at different V_{GS} and V_{DS} values.

2.5.3 Measuring Extracting Parasitics

The parasitic resistances are measured using a cold FET measurement, as described in Section 2.3. Figure 2-9 shows a graph of resistance vs. frequency for a sample device.

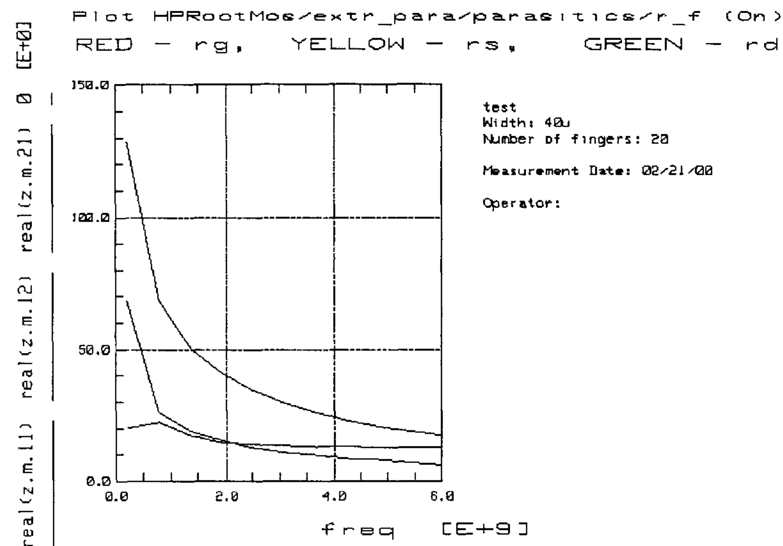

Figure 2-9: Sample resistance (Ω) vs. frequency (Hz) data.

2.5.4 Main Data Acquisition and Root Model Generation

For the main data acquisition, S-parameter measurements are taken at the CW frequency over a range of drain and gate bias voltages. The biases are adaptively set with a more dense spacing in the nonlinear regions of the device and a less dense spacing in the linear regions. Figure 2-10 shows the IV curve of a typical LDMOS device and its measurement points with the gate voltage stepped by 0.4 V increments from 0 to 3.6 V. Figures 2-11 to 2-14 show the admittance data of the sample device that are transformed from the S-parameters taken during the measurement.

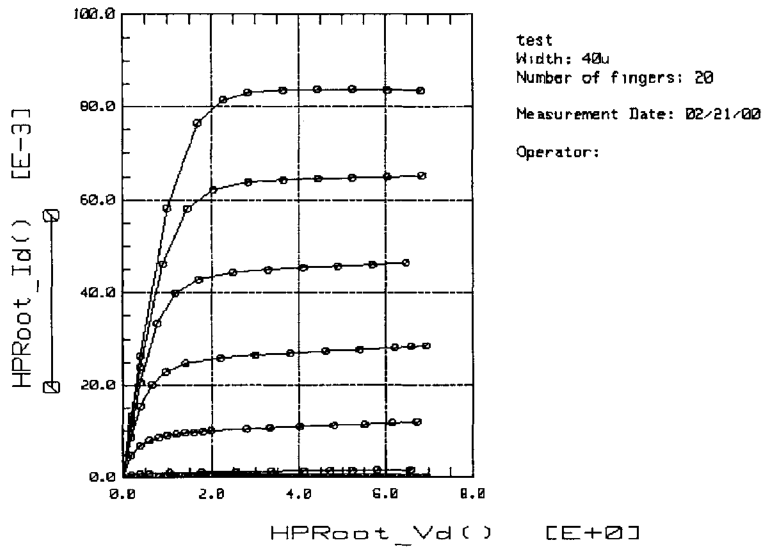

Figure 2-10: Drain current (A) vs. drain to source voltage (V) curve including data points with V_{GS} stepped from 0 to 3.6 V in 0.4 V steps.

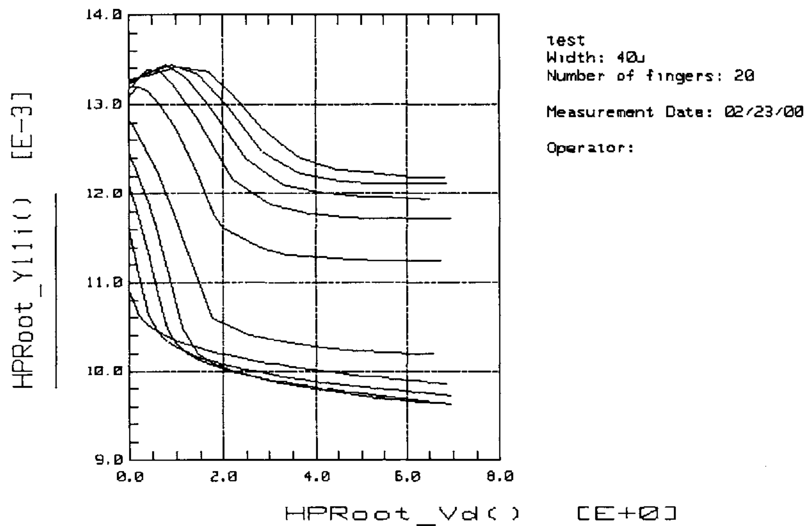

Figure 2-11: Sample $Im[Y_{11}]$ (S) vs. drain to source voltage (V) data with V_{GS} stepped from 0 to 3.6 V in 0.4 V steps.

Plot HPRootMos/main/create_mdl/Y12i (On)

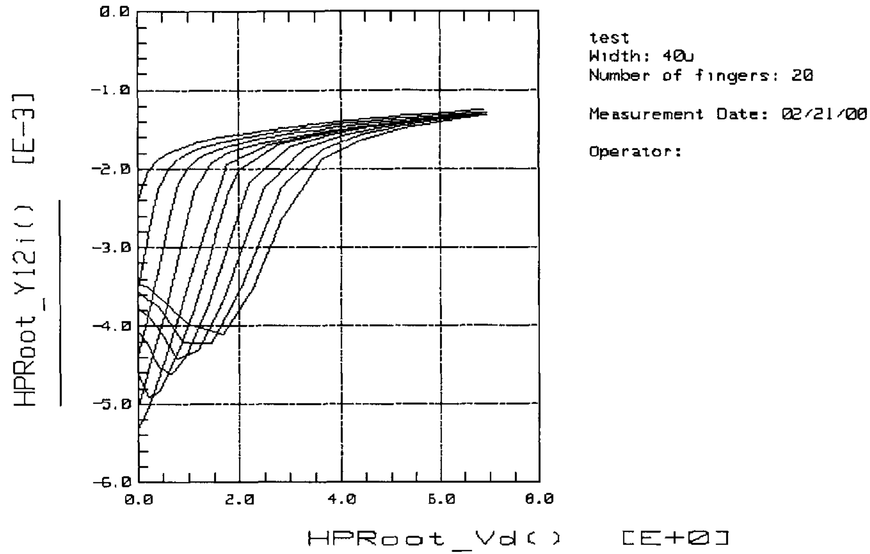

Figure 2-12: Sample Im[Y_{12}] (S) vs. drain to source voltage (V) data with V_{GS} stepped from 0 to 3.6 V in 0.4 V steps.

Plot HPRootMos/main/create_mdl/Y21r (On)

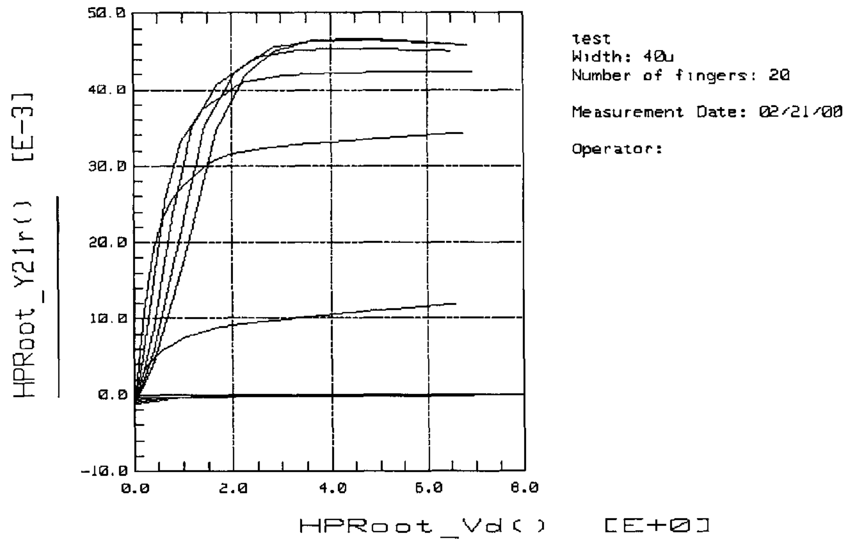

Figure 2-13: Sample Re[Y_{21}] (S) vs. drain to source voltage (V) data with V_{GS} stepped from 0 to 3.6 V in 0.4 V steps.

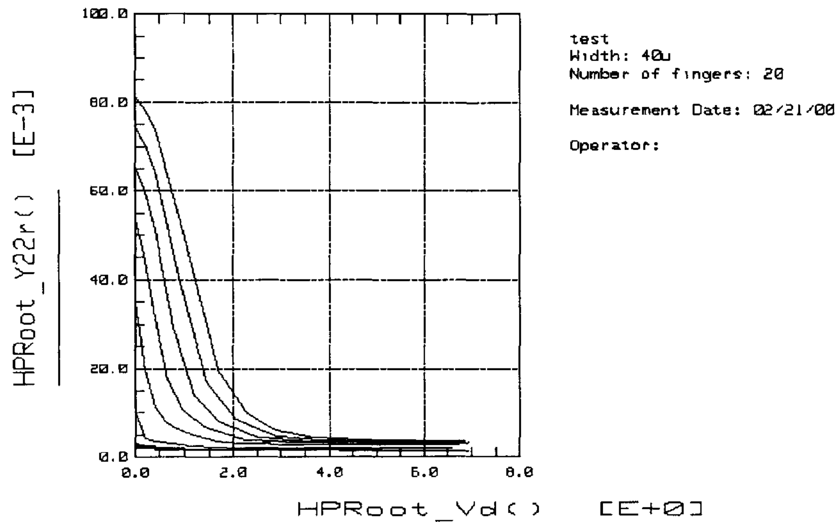

Figure 2-14: Sample Re[Y_{22}] (S) vs. drain to source voltage (V) data with V_{GS} stepped from 0 to 3.6 V in 0.4 V steps.

When the data acquisition is complete, the intrinsic parasitic resistances are updated using the measured data. At this point, the value for τ is inputted by the user. For this research, τ is 10^{-17} s, which means that I_D^{high} does not factor into the value for $I_D(t)$. After various starting points of integration are explored, the resulting model simulations are not identical but the difference is deemed negligible. Consequently, the operating point of the device, shown in Table 2-2, is used as the starting point for contour integration. Using this starting point for contour integration, the Root Model is finally generated. Figures 2-15 and 2-16 indicate the distribution of the charge current under the gate and drain, respectively. The resulting model file, shown in Appendix A, can be incorporated into Libra to simulate the model.

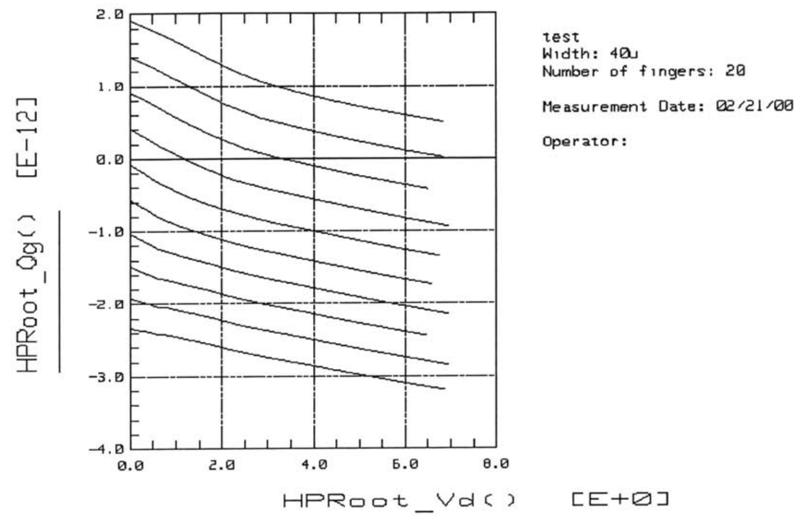

Figure 2-15: Sample Q_G (C) vs. drain to source voltage (V) data with V_{GS} stepped from 0 to 3.6 V in 0.4 V steps.

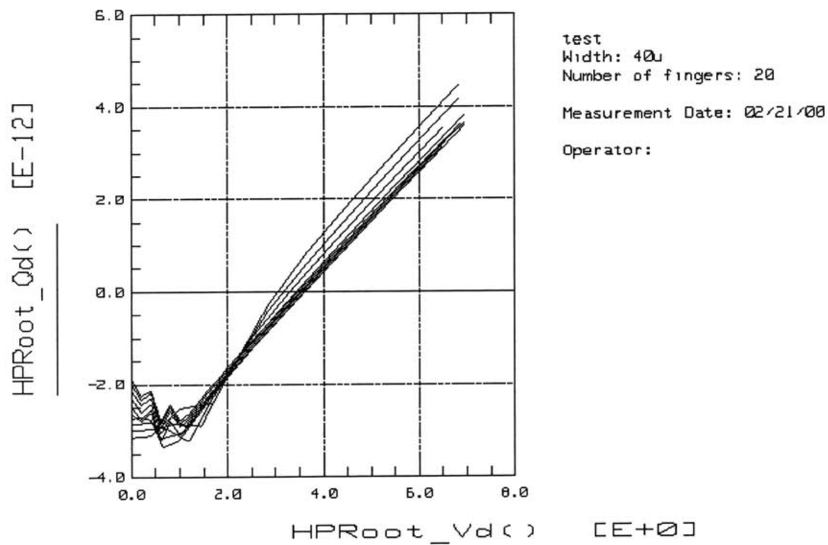

Figure 2-16: Sample Q_D (C) vs. drain to source voltage (V) data with V_{GS} stepped from 0 to 3.6 V in 0.4 V steps.

2.6 Summary

This chapter describes the Root Model extraction process, including the DC current and S-parameter measurements taken and the calculations performed to compute the lookup table. Once the Root Model is extracted for all the devices in this research, harmonic balance simulations using Libra can be performed to predict the RF power figures of merit, as described in the following chapter.

Chapter 3

MODEL SIMULATION

3.1 Overview

As a follow-up to Chapter 2, which describes how the measurements are taken to obtain the Root Model using IC-CAP, this chapter discusses how a harmonic balance simulator works and how the Root Model is incorporated into the Libra simulation environment. This chapter also describes the simulation test benches created to match the measurements taken with a load-pull system.

3.2 Harmonic Balance Analysis

As shown in Figure 3-1, harmonic balance analysis[27] is an iterative process that assumes that given a periodic input signal, there exists a steady-state solution that can be approximated using a finite Fourier series. For most high frequency analog design, a harmonic balance simulator is faster and more accurate than time-domain simulators, such as SPICE. The simulation frequency, number of harmonics, and sample points are inputs to the harmonic balance simulator. The number of harmonics is the number of harmonics that the simulator keeps track of during analysis. A DC analysis is done to determine all the node voltages of the complete circuit. This is the starting point of the harmonic balance simulation. The current flowing into linear elements are calculated using frequency-domain linear analysis. After the inverse Fourier transform is applied to the voltage at the input of the nonlinear elements to obtain the values in the time domain, the current flowing into nonlinear elements are calculated in the time-domain and then transformed, using the Fourier transform, into the frequency-domain. At this point, the currents from the linear and nonlinear elements are compared using an error function.

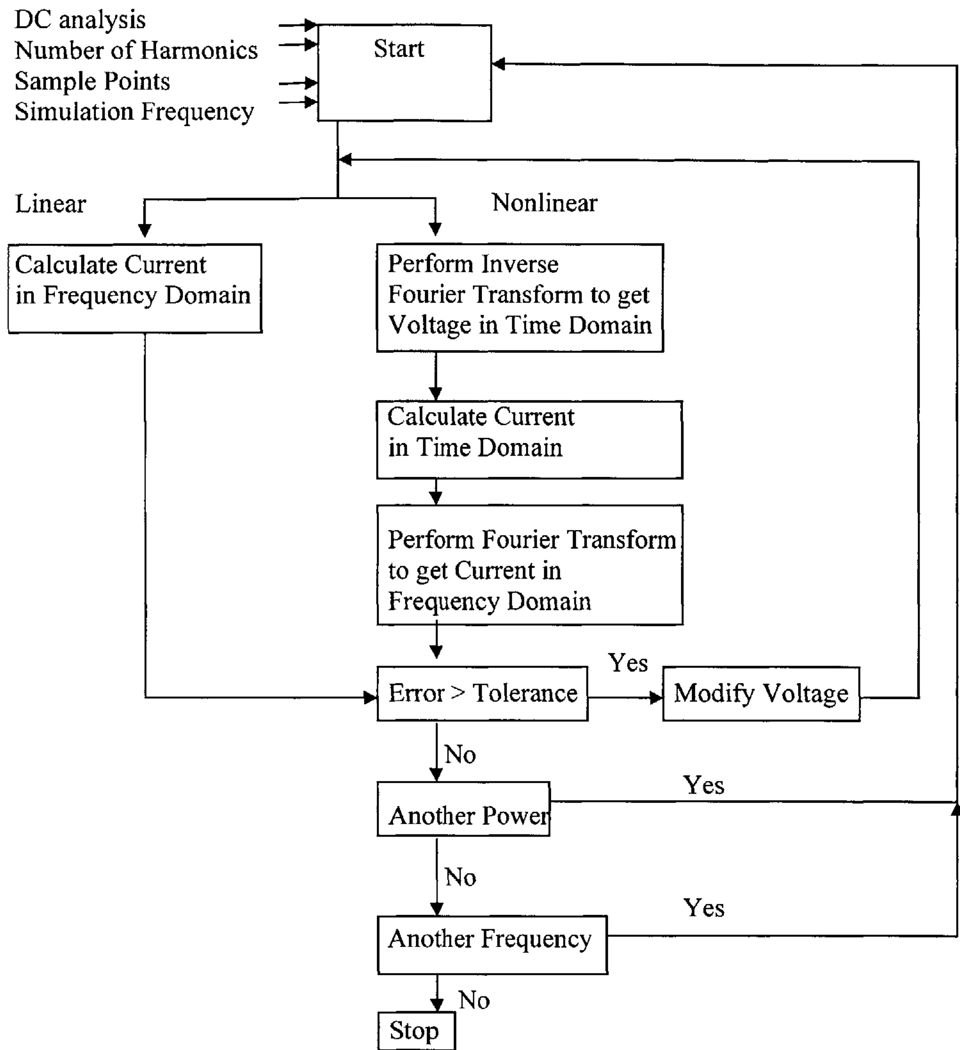

Figure 3-1: Harmonic balance analysis flow diagram[28].

According to Kirchoff's Current Law (KCL), the sum of the current flowing into or out of a node must be zero. This criterion is applied to the error function to exit the loop. If the error function (the amount by which KCL is violated) is greater than a given value, then the voltage amplitude and phase are adjusted and the process repeated. If the analysis converges, then the resulting voltage amplitude and phase approximate the steady-state solution. The entire process is repeated for different levels of power and frequency.

3.3 Simulation Environment

To accurately compare the simulations to the measured results, the simulation environment created in Libra is matched as closely as possible to the measurement setup used at IBM for the load-pull system, as described in Chapter 4. Figure 3-2 shows the simulation environment as it is set up in Libra, while Figure 3-3 shows how the device is biased in the simulation environment. The AC power source connects to the input tuner through a 50 Ω cable. The input and output tuners are then connected to the device through a 50 Ω impedance.

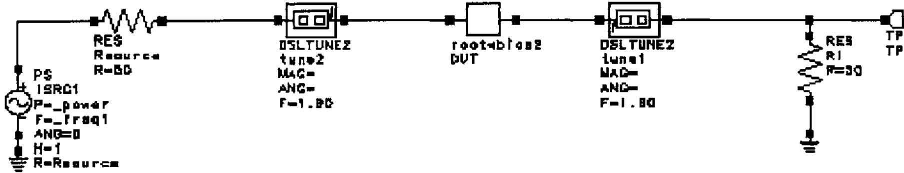

Figure 3-2: Simulation setup in Libra.

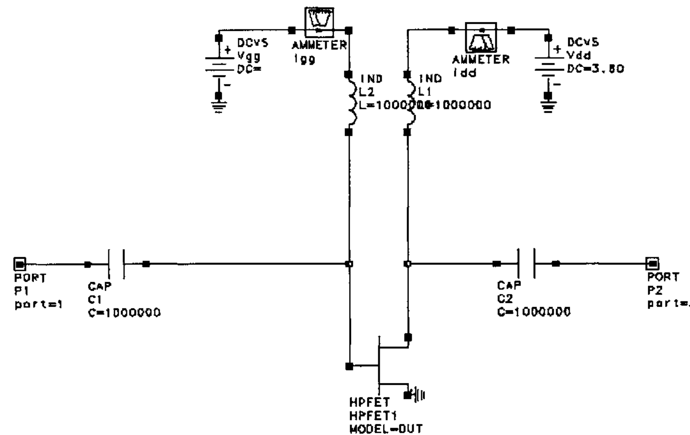

Figure 3-3: Biasing network for device.
(Shown as rootbias2 DUT in Figure 3-2)

For the simulations, the power source is swept over the same range as in the load-pull measurements for each device. The tuners are both manually tuned to the same conjugate impedance match at the fundamental frequency, as in the measurements taken using the load-pull system. The real part of the output tuner impedance is set to match the real part of the output impedance of the transistor to achieve maximum power gain. The imaginary part of the output tuner impedance is set at the conjugate match of the transistor output impedance to cancel the effect of the imaginary part of the impedance at the fundamental frequency. The drain and gate bias voltages are also manually set for each device to match the measurements taken at IBM, as shown in Table 2-2. Table 3-1 lists the measured devices and matching impedances, all referred to 50 Ω at 0 magnitude and 0 degrees. All the measurements are taken at 1.9 GHz.

WAFER	ROW	COL	INPUT TUNER MAGNITUDE	INPUT TUNER ANGLE	OUTPUT TUNER MAGNITUDE	OUTPUT TUNER ANGLE
055	4	3	0.68	81.6	0.57	56.3
055	4	4	0.68	81.6	0.57	56.3
RB7	7	8	0.68	72.6	0.58	42.6
RB7	8	7	0.68	72.6	0.58	42.6
RB3	7	8	0.67	77.2	0.56	44.0
RB3	7	7	0.74	72.1	0.67	39.6
RB3	6	8	0.74	72.1	0.64	41.5

Table 3-1: Device input and output tuner impedance match.

3.4 Large-Signal Test Benches

The test benches in Libra are used to obtain the RF power figures of merit to compare with the measurements taken with the load-pull system at IBM. This comparison is made to determine the accuracy and usefulness of the Root Model for both the bulk and SOI LDMOS devices.

3.4.1 Output Power

Output power is an important parameter in designing power amplifier devices. It is necessary to know how much power a device is capable of delivering to the load. Output power is calculated at the fundamental frequency (1.9 GHz), using:

$$P_{OUT}(f) = \mathrm{Re}[V_{OUT}(f) \times I^*_{OUT}(f)] \qquad \textit{Equation 3-1}$$

$V_{OUT}(f)$ is the rms output voltage and $I^*_{OUT}(f)$ is the complex conjugate of the rms output current. Sample output power simulations are plotted in an output power vs. input power graph shown in Figure 3-4. Output power is linear, with a slope greater than one because of power gain, until device nonlinearities start to dominate, as discussed in Section 3.4.3 on gain compression.

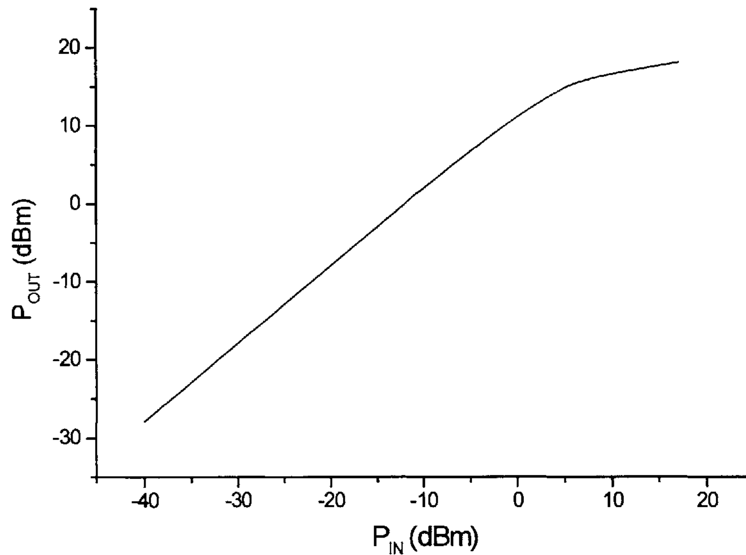

Figure 3-4: Sample output power simulation results for SOI (RB7) device with $L_G = 0.7$ μm and $W_G = 800$ μm (20x40 μm) at $V_{DS} = 3.6$ V and $V_{GS} = 2.64$ V and frequency = 1.9 GHz.

3.4.2 Power Added Efficiency (PAE)

Power added efficiency (PAE) is an important figure of merit to determine how much power is lost in the device and in the matching tuners. PAE is calculated as:

$$PAE = \frac{(P_{OUT} - P_{AV})}{P_{DC}} \qquad \textit{Equation 3-2}$$

Output power is determined as in Section 3.4.1. Available power is the maximum power that can be extracted from the power source. Available power is used instead of delivered power, which is the power coming into the device after passing through the input tuner, in order to match the definition of PAE used in the measurements taken at IBM. Using available power instead of delivered power means that PAE accounts for the power lost in the input tuner. DC power is the power that flows from the DC voltage supply, such as a battery. Consequently, PAE is a measure of the efficiency of the device in terms of how much net power it can deliver to the load for the amount of DC power it consumes. Furthermore, PAE is an important figure of merit because it directly impacts the battery lifetime in portable wireless applications.

A sample PAE vs. input power graph is plotted, as shown in Figure 3-5, in order to understand how efficiency evolves with increasing input power. The graph shows that PAE increases as input power increases, since DC power stays constant and the devices exhibit power gain. PAE decreases as device nonlinearities start to dominate, leading to gain compression and shifting bias current, as discussed in Sections 3.4.3 and 3.4.5, respectively.

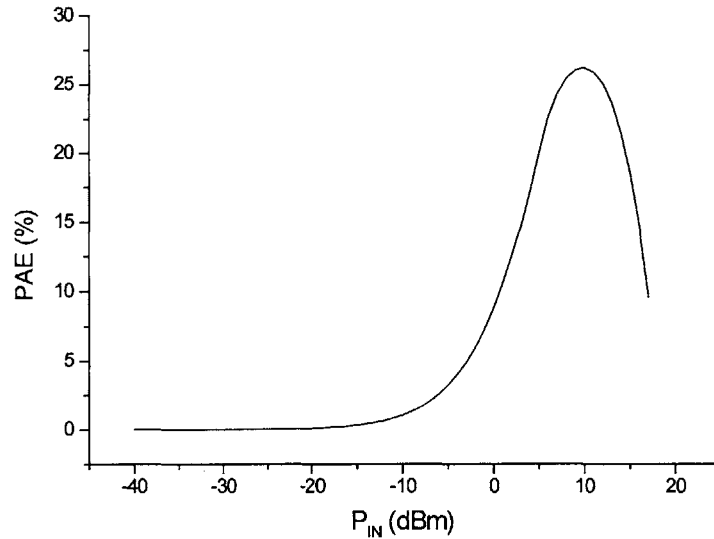

Figure 3-5: Sample PAE simulation results for SOI (RB7) device with L_G = 0.7 μm and W_G = 800 μm (20x40 μm) at V_{DS} = 3.6 V and V_{GS} = 2.64 V and frequency = 1.9 GHz.

3.4.3 Power Gain

Power gain is also a critical figure of merit, since these devices are developed for use in power amplifier designs. Power gain is defined as:

$$Gain = \frac{P_{OUT}}{P_{AV}} \qquad \textit{Equation 3-3}$$

This is the available power gain, since it is calculated as output power divided by available power. As seen in Figure 3-6, gain is constant up to a certain input power, where gain compression occurs. Gain compression results from the influence of device nonlinearity and clipping[29]. For high input power levels, gain rolls off and approaches zero, as output power stays constant for increasing input power. One important measure of gain compression is the 1-dB compression point of gain, defined as the input power level that causes the small-signal gain to drop by 1 dB. The 1-dB compression point is a general reference for specifying the power capability of a power amplifier and is the practical limit for a "linear" amplifier[30].

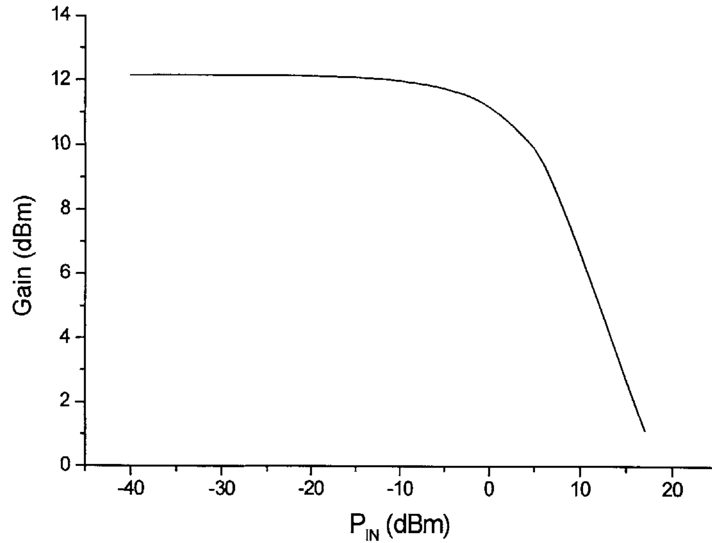

Figure 3-6: Sample power gain simulation results for SOI (RB7) device with L_G = 0.7 μm and W_G = 800 μm (20x40 μm) at V_{DS} = 3.6 V and V_{GS} = 2.64 V and frequency = 1.9 GHz.

3.4.4 IM3 Test Bench

When two signals, ω_1 and ω_2, are applied to a nonlinear system, such as a MOSFET, the output exhibits some components that are the intermodulation (multiplication) products of the input frequencies[31]. One important intermodulation measurement is IM3, the third-order intermodulation product. If ω_1 and ω_2 are close, then the components at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ appear near ω_1 and ω_2. This can corrupt the desired component and degrade performance. In addition, IM3 measurements are related to adjacent channel power (ACPr) in digital communications systems. In wireless communications, it is necessary to minimize the amount of power that is transmitted on adjacent channels, since those channels are being used to transmit other signals.

In the simulation environment set up to match the load-pull measurements, IM3 is measured using two power sources, with frequencies at 1 MHz above and below the fundamental. One power source is driven at 1.899 GHz (ω_1) and the other power source is driven at 1.901 GHz (ω_2). Thus, $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ appear at 1.897 GHz and 1.903

GHz, respectively, which is within the transmitted band near the fundamental frequency at 1.9 GHz. IM3 is defined as:

$$IM3 = \frac{(P_{OUT}^{2\omega_1-\omega_2} + P_{OUT}^{2\omega_2-\omega_1})/2}{P_{OUT}^{fundamental}} \qquad \textit{Equation 3-4}$$

Output power at the fundamental (1.9 GHz) is measured as in Section 3.4.1. A sample simulated IM3 vs. input power graph is shown in Figure 3-7. The slope of this curve is approximately 2, when it should be 3 because it is the third order intermodulation product. More discussion of IM3 simulations is presented in Section 5.4.

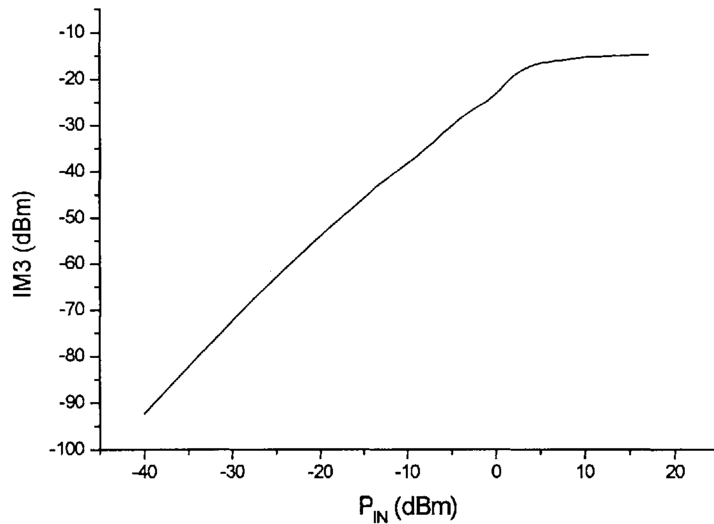

Figure 3-7: Sample IM3 simulation results for SOI (RB7) device with L_G = 0.7 μm and W_G = 800 μm (20x40 μm) at V_{DS} = 3.6 V and V_{GS} = 2.64 V and frequency = 1.9 GHz.

3.4.5 Bias Current

The bias current of a power amplifier device changes as the amplifier goes into compression, defined earlier as the point when output power starts to saturate. How well the bias current simulation matches the measurements indicates how accurate the Root Model is in modeling the device in gain compression. However, it is usually difficult to model gain compression at a detailed level. A sample bias current vs. input power graph

is shown in Figure 3-8. The bias current is the average current along the load-lines, as shown in Figure 3-9. Thus, if the device clips low, the bias current rises, because the average current increases. Conversely, if the device clips high, the bias current decreases.

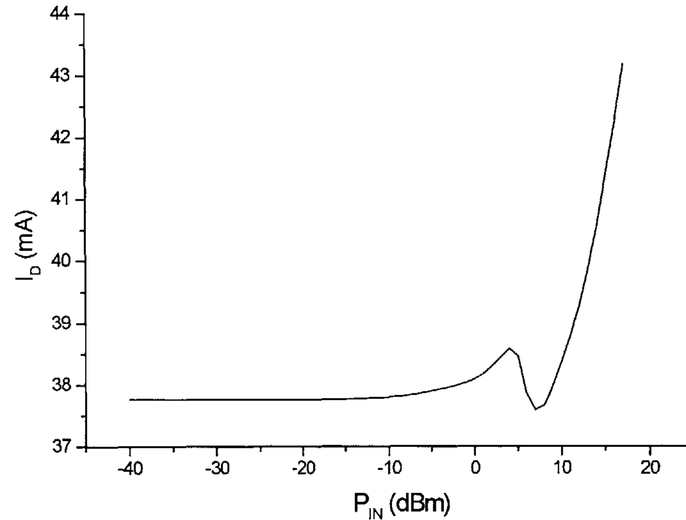

Figure 3-8: Sample bias current simulation results for SOI (RB7) device with L_G = 0.7 μm and W_G = 800 μm (20x40 μm) at V_{DS} = 3.6 V and V_{GS} = 2.64 V and frequency = 1.9 GHz.

3.4.6 Load-Lines

Load-lines are simulated to determine the time-dependent device behavior during RF drive. Load-lines illustrate curves in the I_D-V_{DS} plane for constant input power around a bias point. Load-lines show whether the device clips low or high first. The load-line simulations can aid in determining the exact location within the model where inaccuracies occur. For example, by examining the load lines in Figure 3-9, it becomes evident that there is inadequate data taken during model extraction at high gate biases in the linear region.

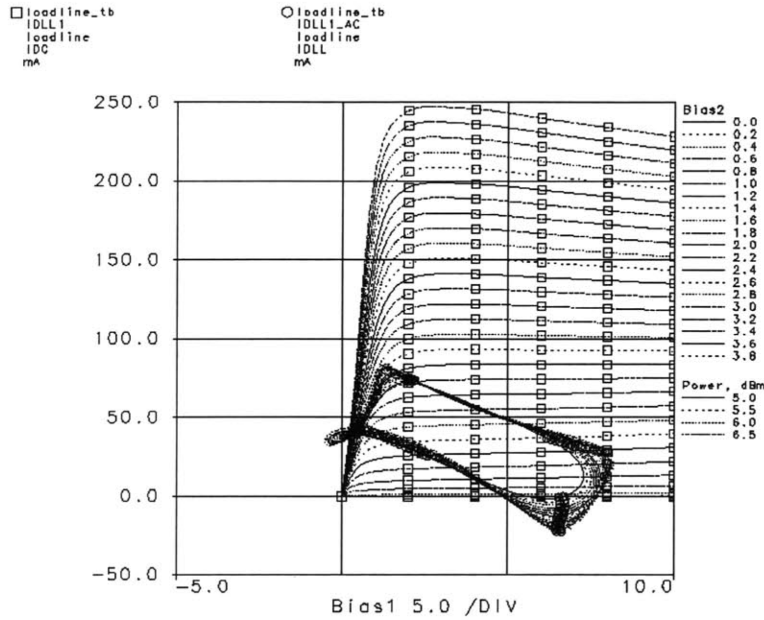

Figure 3-9: Sample load-line simulation results for SOI (RB7) device with L_G = 0.7 μm and W_G = 800 μm (20x40 μm) at frequency = 1.9 GHz.

3.5 Summary

This chapter discusses how a harmonic balance simulator works. The simulation environment in Libra and the different test benches run are also described. All of the simulation results discussed will be compared to the load-pull measurements taken at IBM that are described in the next chapter.

Chapter 4

LOAD-PULL MEASUREMENTS

4.1 Overview

To determine the accuracy of the Root Model, a load-pull system is used to obtain RF power measurements for both the bulk and SOI LDMOS devices. The data obtained from the load-pull system is compared to the simulation results of Chapter 3 to determine accuracy of the Root Model for both bulk and SOI LDMOS devices.

4.2 Measurement Setup

A load-pull system is a large-signal device characterization system used to measure power devices. The system combines solid-state tunable electronic load technology with a network analyzer. A load-pull system is capable of measuring S-parameters, DC characteristics, power parameters, efficiency, and intermodulation measurements.

Figure 4-1 illustrates the test equipment that composes a load-pull system[32]. The device (shown at DUT—device under test in Figure 4-1) is probed on a wafer probe station. These measurements are taken on wafer, so there are no package parasitics involved to better reflect the device characteristics. On the downside, the final product needs to be packaged, so package parasitics must be taken into account at some point. The network analyzer, at the center of the load-pull system, provides the power source at a selected frequency. The network analyzer also measures the S-parameters and output power of the device at a single frequency. For two-tone measurements, such as intermodulation, a second power source must be used. Signal conditioning modules (shown as SCM in Figure 4-1) are used to control the signal level and harmonics before the input signal is delivered to the device. The SCM ensures that there is one clean spike at the desired frequency. The spectrum analyzer is used to measure power over a wide range of frequencies. A DC supply is utilized to bias the device. The load-pull system is

controlled by a PC workstation, connected to the load-pull mainframe (LP mainframe in Figure 4-1) and the instruments via GPIB interfaces and cables.

The load-pull setup consists of a variable, precisely calibrated tuner[33] (shown as ELM—Electronic Load Module in Figure 4-1), between the transistor and the load, which operates as a matching network to present various impedances to the transistor according to a control input. The output tuner is adjusted to the conjugate match of the device at the fundamental frequency to increase the power gain of the device[34]. An input tuner, located between the signal generator and the transistor, ensures that the device sees a conjugate match. The tuners used in the system are solid-state tuners consisting of many diodes along a transmission line. The impedance of the tuner can, therefore, be adjusted by turning on the diodes (thereby reducing the resistance) or reverse biasing the diode (changing the capacitance). By using solid-state rather than mechanical tuners, the system benefits from the repeatability of the tuner impedance and the time savings of the tuning process. The disadvantages include greater tuner losses and a more limited frequency range.

Calibration of the load-pull system must be completed before measurements can be taken. Two-port calibrations are done at the input and output of the device and a one-port calibration is done after the output tuner, at the load. During the calibration, a table is computed to determine how much available power there is for each setting of the power source.

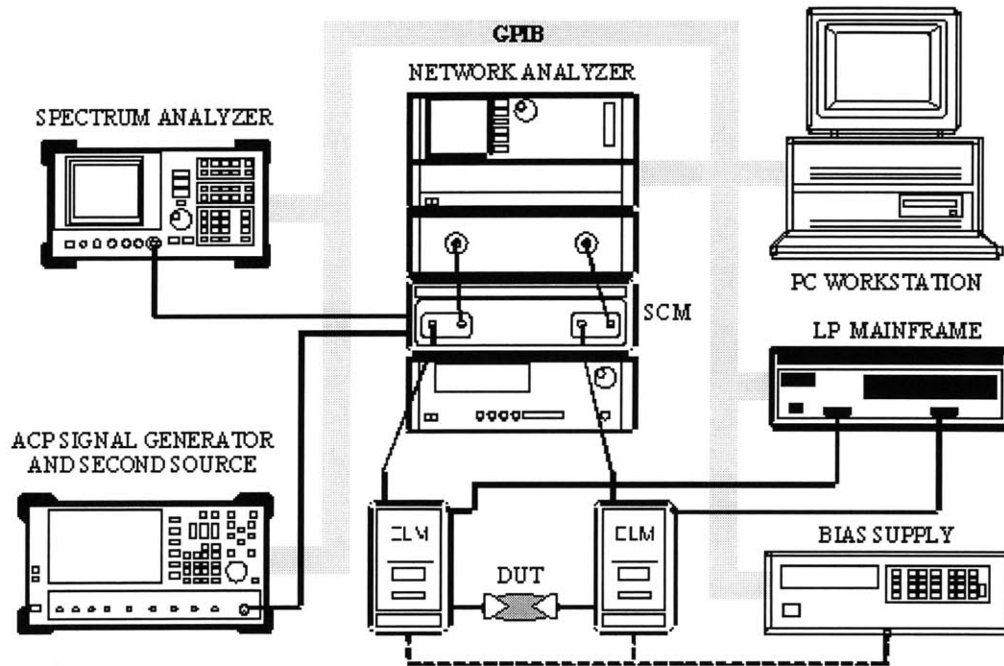

Figure 4-1: Load-pull measurement setup[35].

4.3 Measurements

Using the load-pull system, a number of power figures of merit are measured. These measurements correspond to the simulation test benches that are set up in order to determine the accuracy of the Root Model for bulk and SOI LDMOS devices.

During a sweep of input power, RF power figures of merit, such as output power, drain current, and gate current, are measured. The same definitions are used in the load-pull measurements as in the Libra simulation environment to accurately compare the results. Equations 3-2, 3-3, and 3-4 show how PAE, power gain, and IM3, respectively, are calculated. Sample load-pull measurements are shown in Figures 4-2 through 4-4 for output power, power gain, PAE, drain current, and IM3 for a SOI (RB7) device with a gate length of 0.7 μm and gate width of 800 μm (20 fingers each with a width of 40 μm).

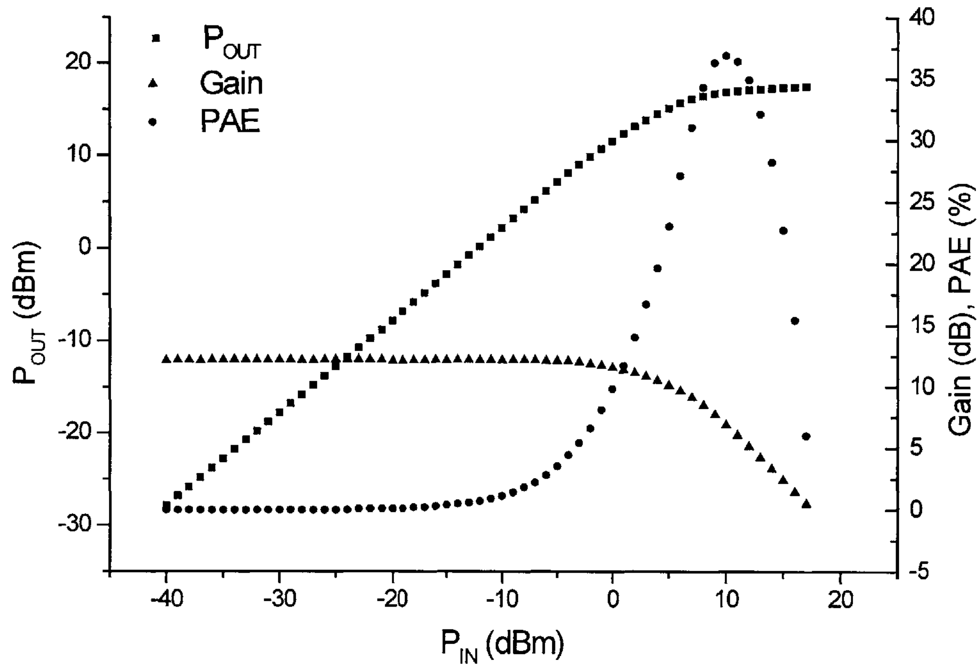

Figure 4-2: Sample output power, gain, and PAE measurements for SOI (RB7) device with L_G = 0.7 μm and W_G = 800 μm (20x40 μm) at V_{DS} = 3.6 V and V_{GS} = 2.64 V and frequency = 1.9 GHz.

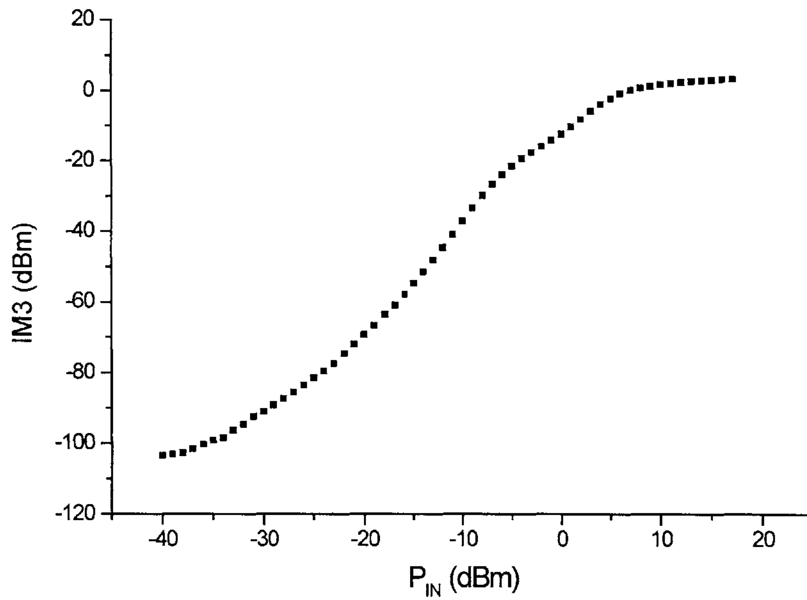

Figure 4-3: Sample IM3 measurements for SOI (RB7) device with L_G = 0.7 μm and W_G = 800 μm (20x40 μm) at V_{DS} = 3.6 V and V_{GS} = 2.64 V and frequency = 1.9 GHz.

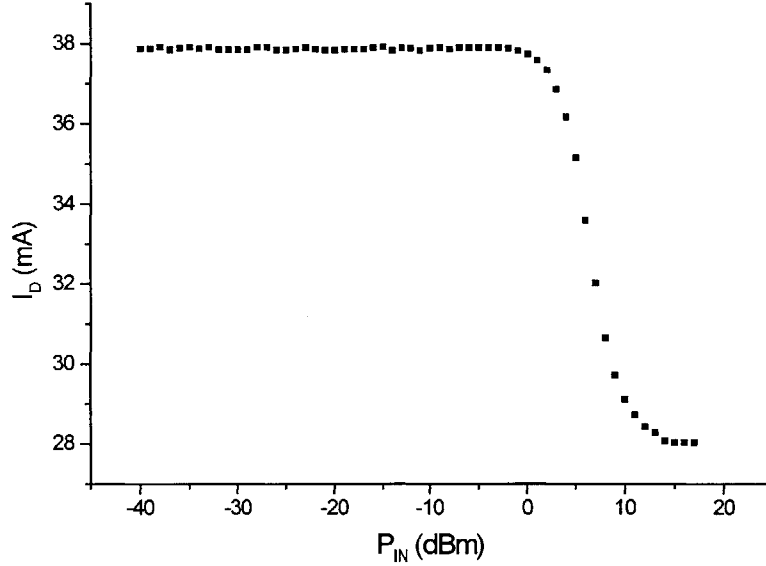

Figure 4-4: Sample bias current measurements for SOI (RB7) device with L_G = 0.7 μm and W_G = 800 μm (20x40 μm) at V_{DS} = 3.6 V and V_{GS} = 2.64 V and frequency = 1.9 GHz.

4.4 Summary

This chapter discusses the load-pull measurement system, including all of the measurement instrumentation used. Sample measurements are shown for the RF power figures of merit. Using the load-pull measurements included in this chapter along with the simulation results from Chapter 3, the accuracy of the Root Model for bulk and SOI LDMOS devices can be determined, as discussed in the following chapter.

Chapter 5

KEY FINDINGS AND RESULTS

5.1 Overview

In the previous chapters, the load-pull measurements and model simulations are described. With this information, the comparisons can be made to determine the accuracy of the Root Model. This chapter will present the comparative analysis and discuss the possible reasons for the observed mismatches.

5.2 Representative Results

The first pass of results of load-pull measurements and model simulations indicates that the Root Model is reasonably accurate in predicting several RF power figures of merit, such as output power and power gain. However, there are discrepancies in simulation results for peak PAE and bias current. Also, simulations for IM3 do not match the measurements. This chapter includes results, taken at 1.9 GHz, for a representative device from each wafer. Several sets of Root Model extractions have been performed, but the difference in simulation results is negligible, as shown in Appendix B. Appendix C shows the results from other devices studied.

5.2.1 SOI (RB7) Devices

The SOI (RB7) devices studied in this section have a gate length of 0.7 μm and a gate width of 800 μm (20x40 μm). These devices are located at row 8 and column 7 on the wafer with the upper left die labeled row 1, column 1.

5.2.1.a Output Power

Output power simulations track the load-pull measurements almost exactly, as shown in Figure 5-1.

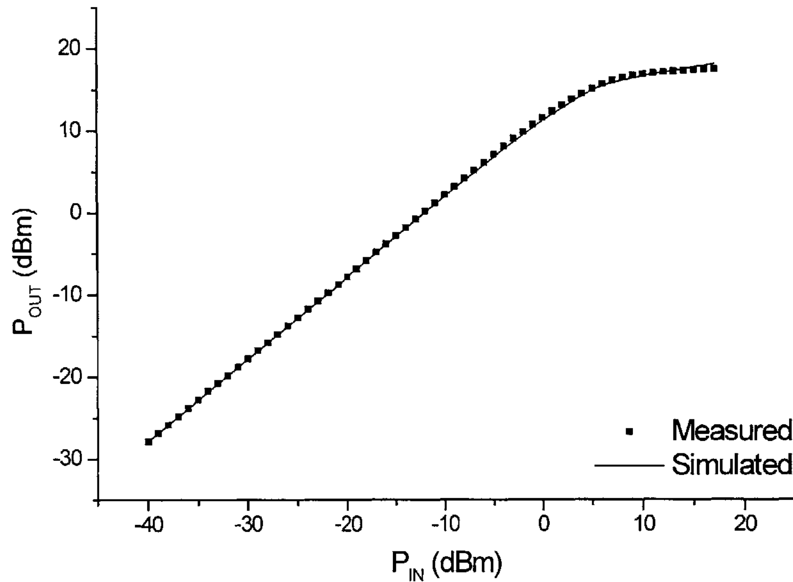

Figure 5-1: Output power simulations and measurements for SOI (RB7) device with $L_G = 0.7$ μm and $W_G = 800$ μm (20x40 μm) at $V_{DS} = 3.6$ V, $V_{GS} = 2.64$ V and frequency = 1.9 GHz.

5.2.1.b Power Added Efficiency (PAE)

Although, the shape of the curve for PAE simulations matches measurements, the values for peak PAE are consistently lower in the simulations, as seen in Figure 5-2. Also, the discrepancy in peak PAE can be as much as 10 percentage points (or 25% error).

One possible reason why PAE simulations show a lower peak efficiency than measurements is that the bias current I_D, as described in Section 5.2.1.e, in the simulations, for input power greater than 0 dBm, is higher than the measured I_D for the same input power. Thus, the efficiency extracted from the simulation is lower than the measured one since the DC power consumed by the device is higher with greater bias current.

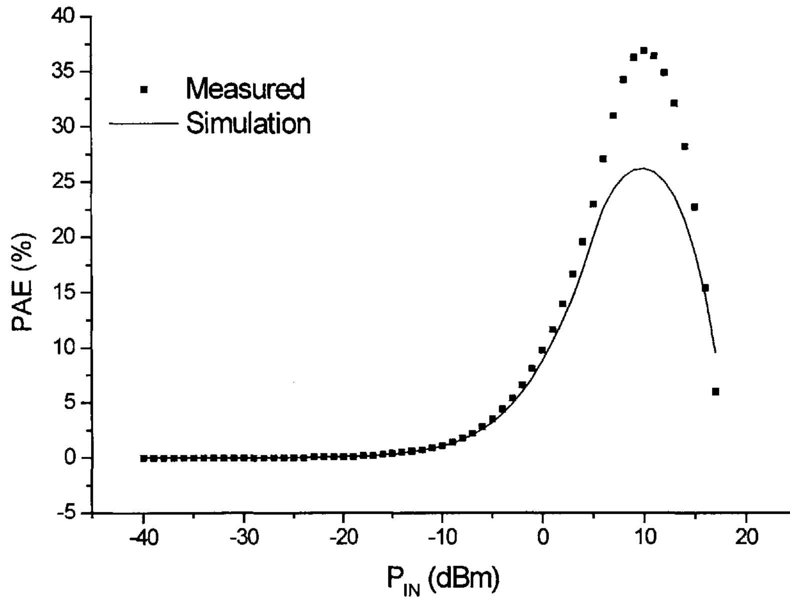

Figure 5-2: PAE simulations and measurements for SOI (RB7) device with $L_G = 0.7$ µm and $W_G = 800$ µm (20x40 µm) at $V_{DS} = 3.6$ V, $V_{GS} = 2.64$ V and frequency = 1.9 GHz.

5.2.1.c Power Gain

Since output power simulations track measurements, power gain simulations are also generally very close to measurements, within 1 dB. Gain simulations are typically higher than load-pull measurement results, but simulations can also match measurements very well, as shown in Figure 5-3.

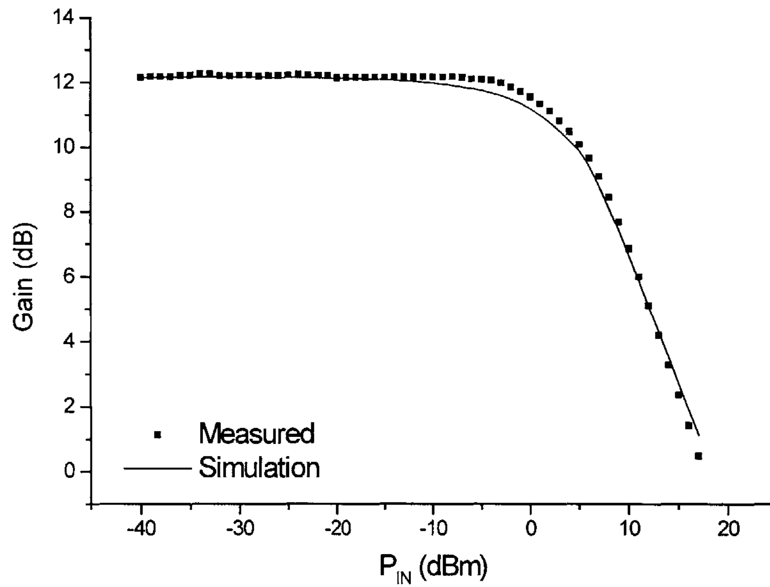

Figure 5-3: Power gain simulations and measurements for SOI (RB7) device at with L_G = 0.7 μm and W_G = 800 μm (20x40 μm) V_{DS} = 3.6 V, V_{GS} = 2.64 V and frequency = 1.9 GHz.

5.2.1.d IM3

In general, IM3 simulations do not match measurements, as seen in Figure 5-4. Section 5.4 discusses this discrepancy further.

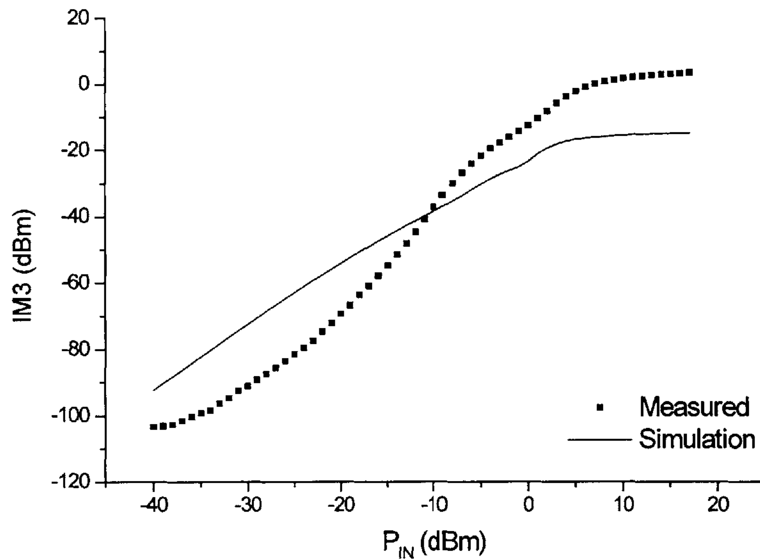

Figure 5-4: IM3 simulations and measurements for SOI (RB7) device with L_G = 0.7 μm and W_G = 800 μm (20x40 μm) at V_{DS} = 3.6 V, V_{GS} = 2.64 V and frequency = 1.9 GHz.

5.2.1.e Bias Current

Simulations for bias current match well with load-pull measurements until gain compression occurs, around 0 dBm for input power. In the particular case shown in Figure 5-5, the simulations predict that the bias current should rise, while the measurements show that the bias current decreases and then remains constant. An analysis of the load-lines of the simulations, as shown in Figure 3-9, indicates that the constant power lines extend well beyond where the measurements for Root Model extraction are made. Since the instruments used to measure the DC current and S-parameters for Root Model extraction are limited to 100 mA of current, measurements are only taken for gate voltages that result in drain saturation currents below 100 mA. This means that the linear regions for higher gate voltages are not measured. The model cannot predict the device behavior well in this region, since there is no available data. Since current clipping determines how the bias current changes, the model simulations can better match measurements when the current clips low, leading to increasing bias current. On the contrary, if the current clips high, leading to a decrease in bias current, the model simulations are not accurate because there are not enough DC current and S-

parameter measurements taken during model extraction for the linear region at high gate voltages. That is the case of the results shown in Figure 5-5.

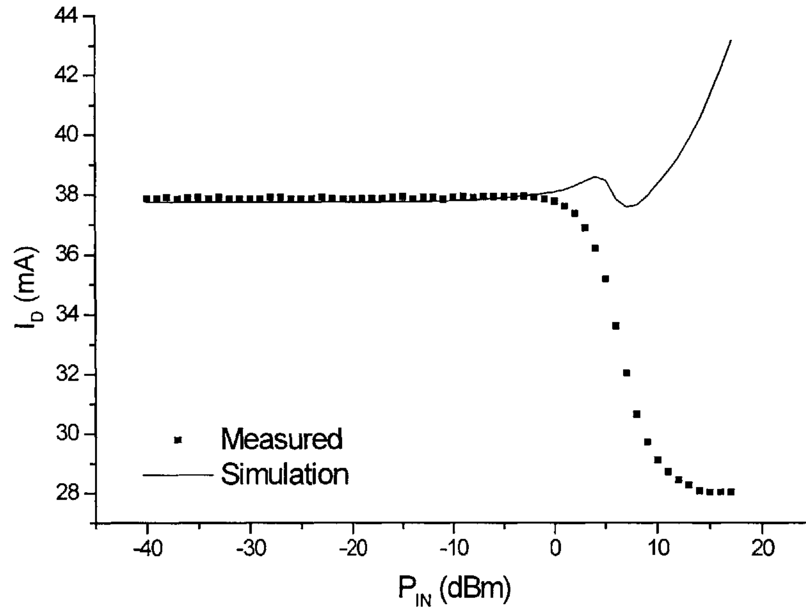

Figure 5-5: Bias current simulations and measurements for SOI (RB7) device with $L_G = 0.7$ μm and $W_G = 800$ μm (20x40 μm) at $V_{DS} = 3.6$ V, $V_{GS} = 2.64$ V and frequency = 1.9 GHz.

5.2.2 Bulk (055) Devices

Figures 5-6 to 5-8 show the simulation results and measurements comparison for the RF power figures of merit for a bulk (055) device at row 4, column 4. The results for bulk devices are similar to those for SOI devices, indicating that the Root Model works equally well for both types of devices. In general, the mismatch for peak PAE (16% error) is less in bulk devices than in SOI (RB7) devices (25%).

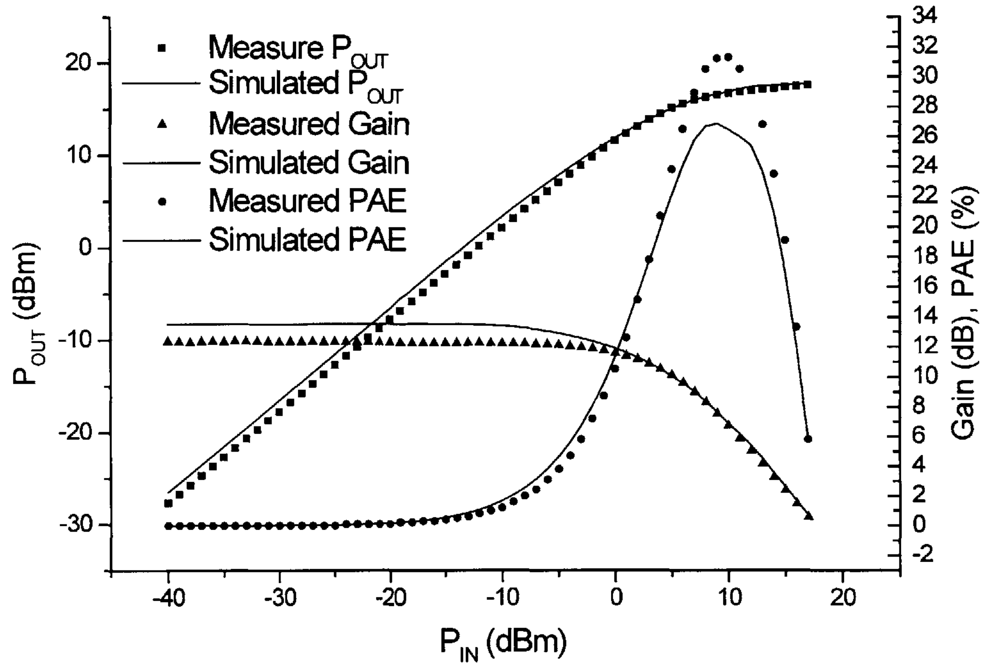

Figure 5-6: Output power, gain, and PAE simulations and measurements for bulk (055) device with L_G = 0.7 μm and W_G = 800 μm (20x40 μm) at V_{DS} = 3.6 V, V_{GS} = 2.8 V and frequency = 1.9 GHz.

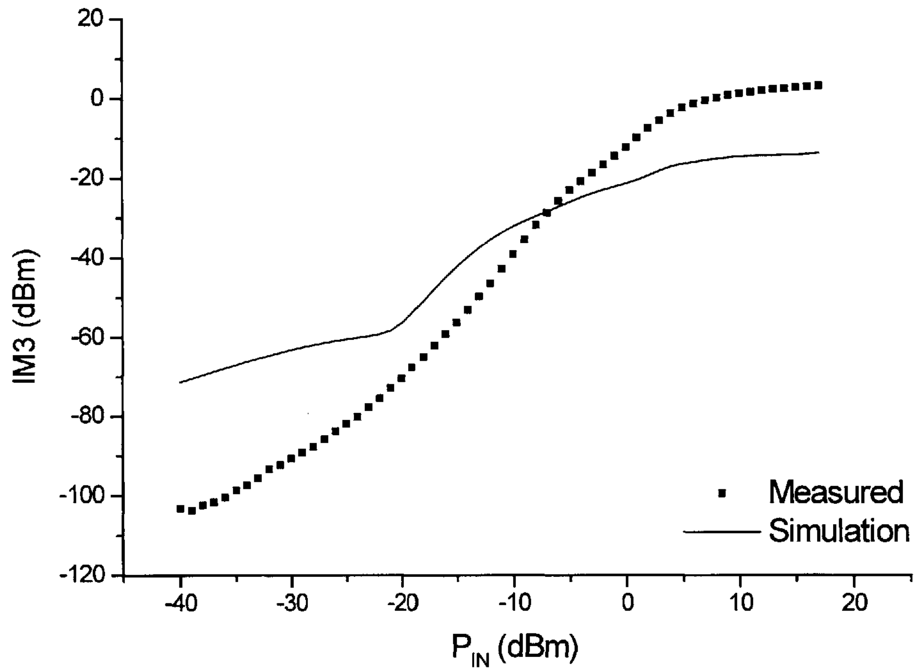

Figure 5-7: IM3 simulations and measurements for bulk (055) device with L_G = 0.7 μm and W_G = 800 μm (20x40 μm) at V_{DS} = 3.6 V, V_{GS} = 2.8 V and frequency = 1.9 GHz.

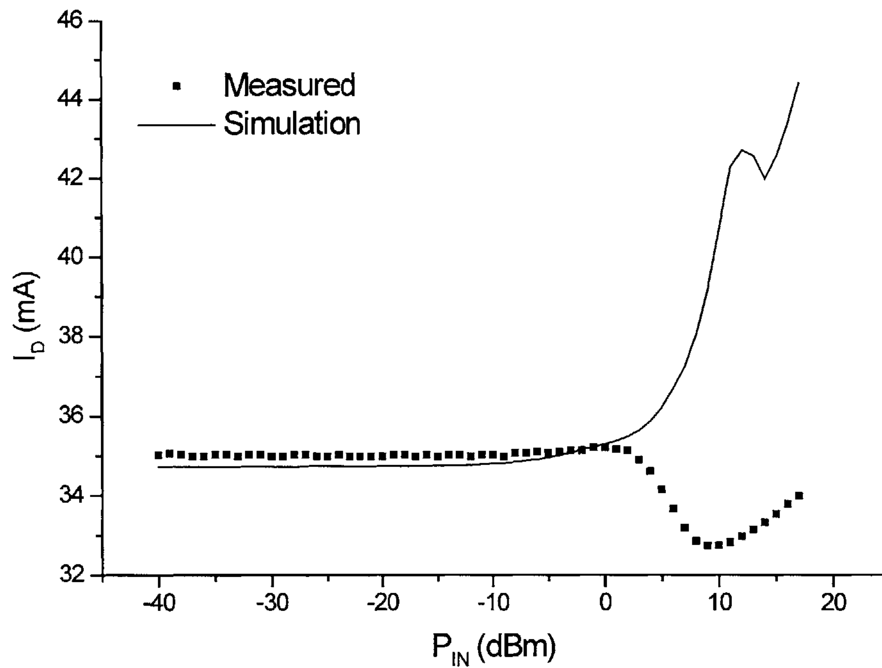

Figure 5-8: Bias current simulations and measurements for bulk (055) device with L_G = 0.7 μm and W_G = 800 μm (20x40 μm) at V_{DS} = 3.6 V, V_{GS} = 2.8 V and frequency = 1.9 GHz.

5.3 Discussion of Trends

5.3.1 Difference between SOI and Bulk

In general, the comparison between simulation results and measurements are similar for bulk and SOI LDMOS devices. One observed trend is that PAE simulations, in particular peak PAE, for bulk devices match measurements better than SOI devices. This may be caused by self-heating effects[36], since SOI devices exhibit more self-heating than bulk devices. In the load-pull measurements, the temperature of the device is related to the mean power dissipation as it swings along the load line. In the simulations, the temperature of the device is related to the instantaneous voltage and current of the device as it moves along the load-line. Thus, for small input power levels, the instantaneous temperature does not vary much from the DC bias point, so temperature effects are minimal. On the contrary, for high input power levels, the instantaneous voltage and current in the simulations move further away from the bias point, leading to temperature

variation between the simulations and measurements. Since there are more self-heating effects in SOI than in bulk, peak PAE for bulk devices matches better than SOI devices.

5.3.2 Impact of bias

When comparisons are made using a RB3, row 7, column 8 device, as shown in Figures 5-9 to 5-11, the match for PAE shows significant improvement, within 6 percentage points (or 18.3% error). The difference in these simulations is that the device is biased at a lower current. Lack of DC current and S-parameter measurements for high gate voltages during model extraction may not be as crucial if the device is biased at a lower current, since the device is more likely to clip low than high.

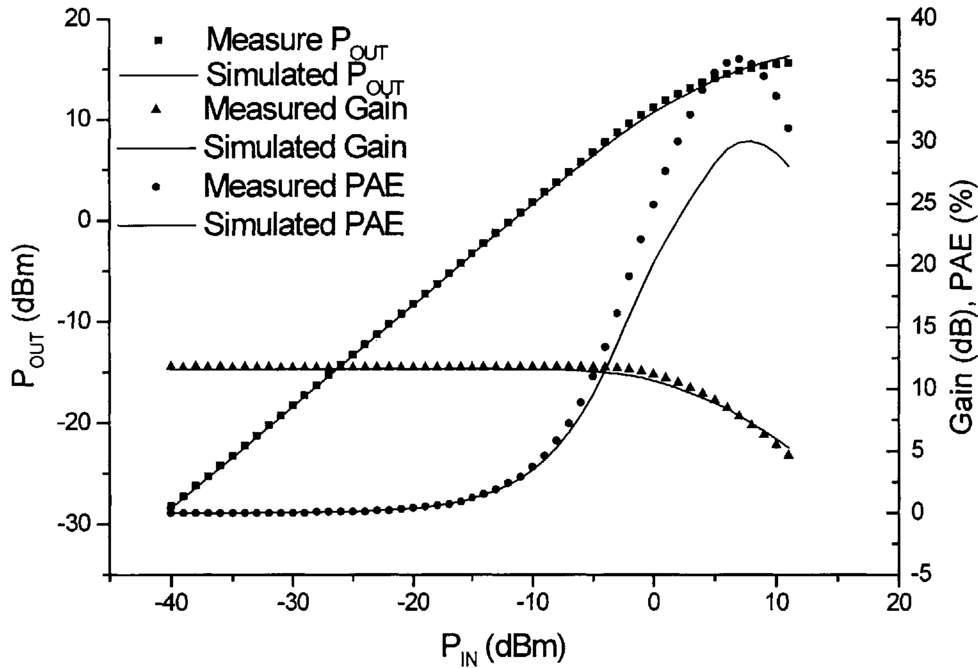

Figure 5-9: Output power, gain, and PAE simulations and measurements for SOI (RB3) device with $L_G = 0.7$ µm and $W_G = 800$ µm (20x40 µm) at $V_{DS} = 3.6$ V, $V_{GS} = 1.6$ V and frequency = 1.9 GHz.

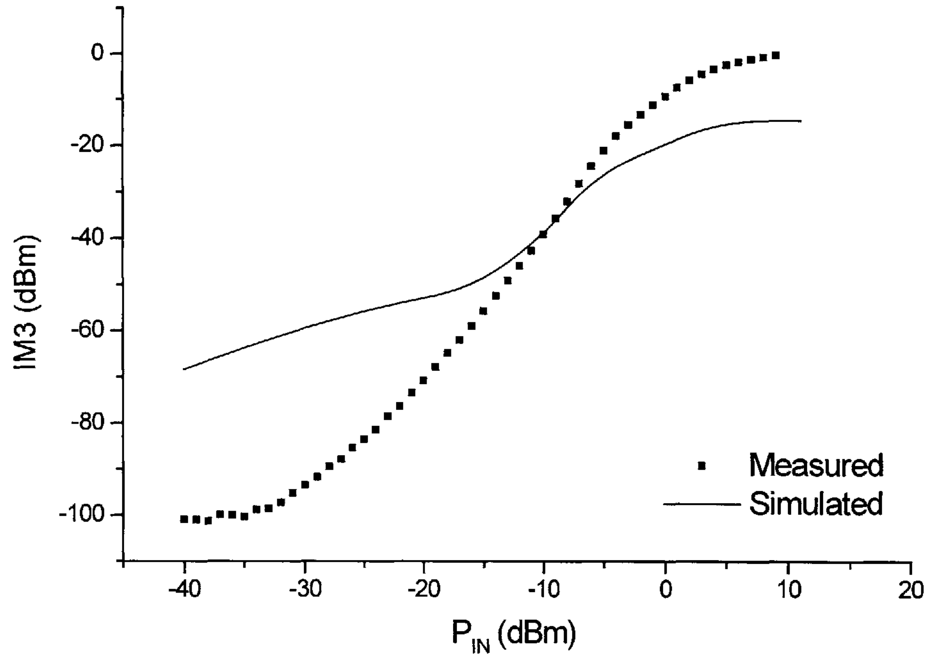

Figure 5-10: IM3 simulations and measurements for SOI (RB3) device
with L_G = 0.7 μm and W_G = 800 μm (20x40 μm) at V_{DS} = 3.6 V, V_{GS} = 1.6 V and frequency = 1.9 GHz.

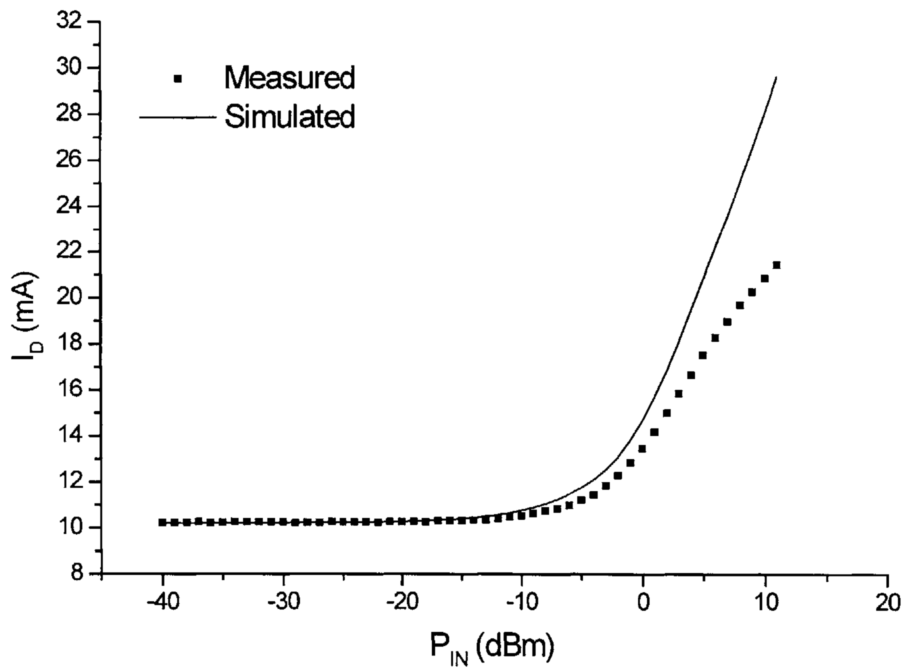

Figure 5-11: Bias current simulations and measurements for SOI (RB3) device
with L_G = 0.7 μm and W_G = 800 μm (20x40 μm) at V_{DS} = 3.6 V, V_{GS} = 1.6 V and frequency = 1.9 GHz.

To explore the impact of the bias point on the agreement of model simulations and measurements, simulations at varying biases are done for one device on bulk (055) and SOI (RB3) that have been previously measured using the load-pull system for a range of biases. Table 5-1 lists the devices, biases, and matching impedances, with 50 Ω as the reference point at 0 magnitude and 0 degrees.

WAFER	ROW	COL	VD	VG	INPUT TUNER MAG	INPUT TUNER ANGLE	OUTPUT TUNER MAG	OUTPUT TUNER ANG
bulk								
055	4	4	3.6	1.850	0.68	81.6	0.79	50.9
055	4	4	3.6	2.201	0.77	89.2	0.78	64.4
055	4	4	3.6	2.651	0.68	81.6	0.59	53.8
055	4	4	3.6	2.800	0.68	81.6	0.57	56.3
SOI								
RB3	7	8	3.6	1.200	0.75	61.2	0.75	31.1
RB3	7	8	3.6	2.000	0.67	77.2	0.56	44.0

Table 5-1: Device input and output tuner impedance match for varying biases.

Since the model simulations match measurements well for output power and gain, only the comparisons for PAE, IM3, and bias current for a range of biases are shown in Figures 5-12 to 5-14 for the bulk (055) device. Similarly, Figures 5-15 to 5-17 show the same comparison for the SOI (RB3) device. Looking at these results, it can be seen that the simulations more closely match the measurements at lower biases, especially for bulk devices. When the devices are biased at a low current, the current will clip low before clipping high. Since there are DC current and S-parameter measurements taken for high V_{DS}, low clipping is better modeled than high clipping where high V_{GS} measurements cannot be taken. As a result, bias current and PAE are better modeled at low V_{GS}.

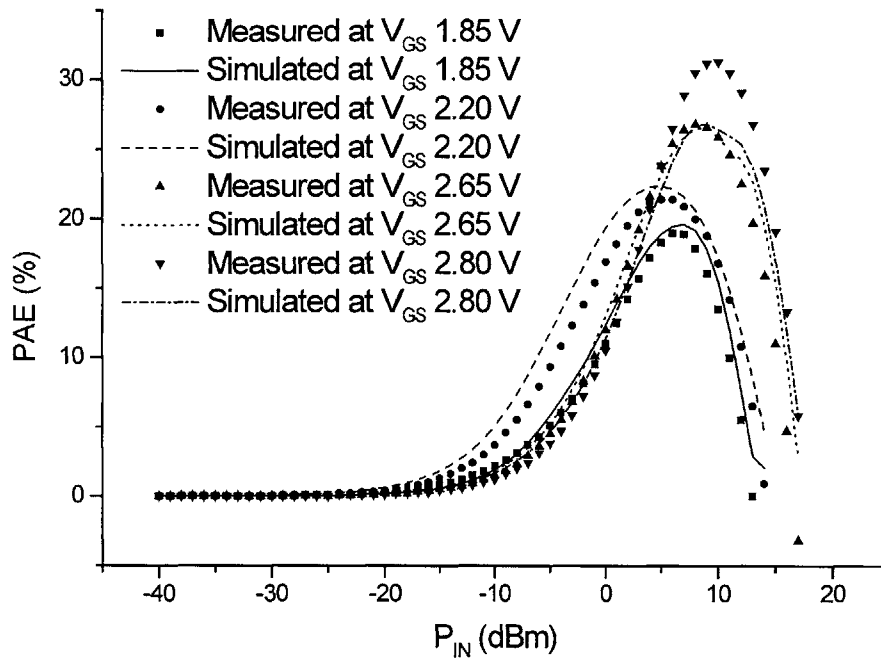

Figure 5-12: PAE simulations and measurements for bulk (055) device with $L_G = 0.7$ μm and $W_G = 800$ μm (20x40 μm) at $V_{DS} = 3.6$ V and varying V_{GS} and frequency = 1.9 GHz.

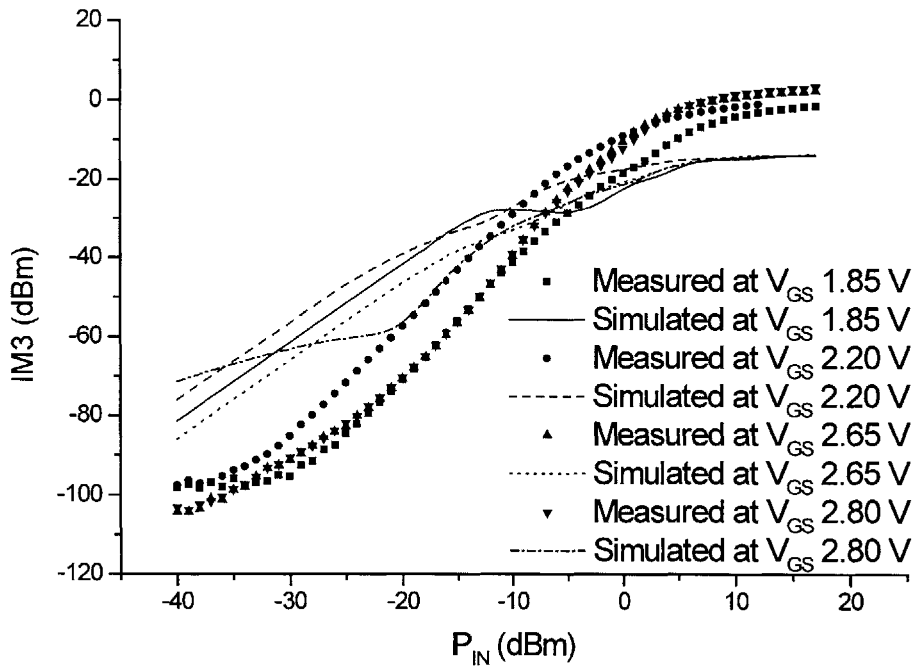

Figure 5-13: IM3 simulations and measurements for bulk (055) device with $L_G = 0.7$ μm and $W_G = 800$ μm (20x40 μm) at $V_{DS} = 3.6$ V and varying V_{GS} and frequency = 1.9 GHz.

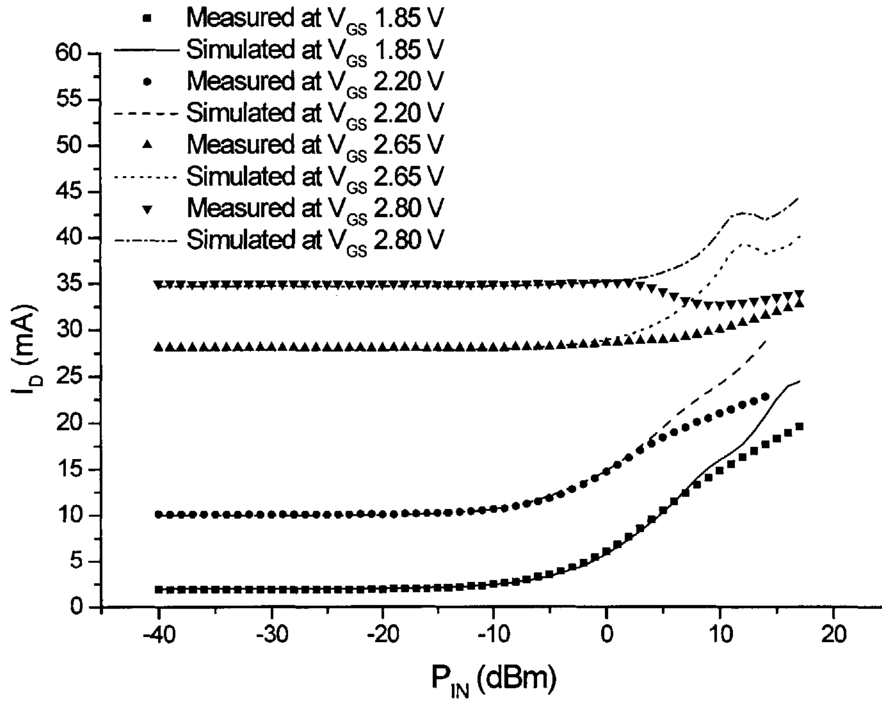

Figure 5-14: Bias current simulations and measurements for bulk (055) device with $L_G = 0.7$ µm and $W_G = 800$ µm (20x40 µm) at $V_{DS} = 3.6$ V and varying V_{GS} and frequency = 1.9 GHz.

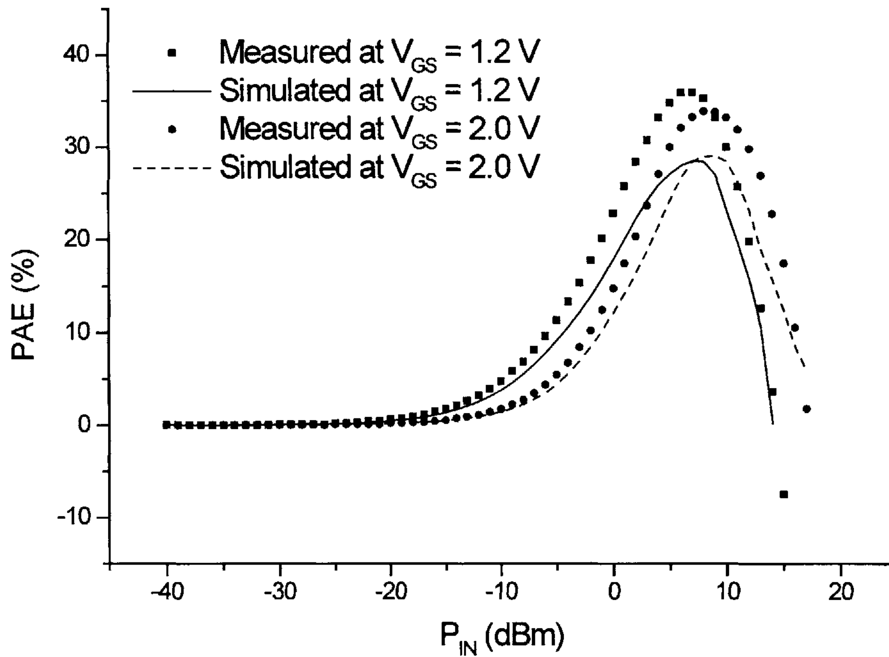

Figure 5-15: PAE simulations and measurements for SOI (RB3) device with $L_G = 0.7$ µm and $W_G = 800$ µm (20x40 µm) at $V_{DS} = 3.6$ V and varying V_{GS} and frequency = 1.9 GHz.

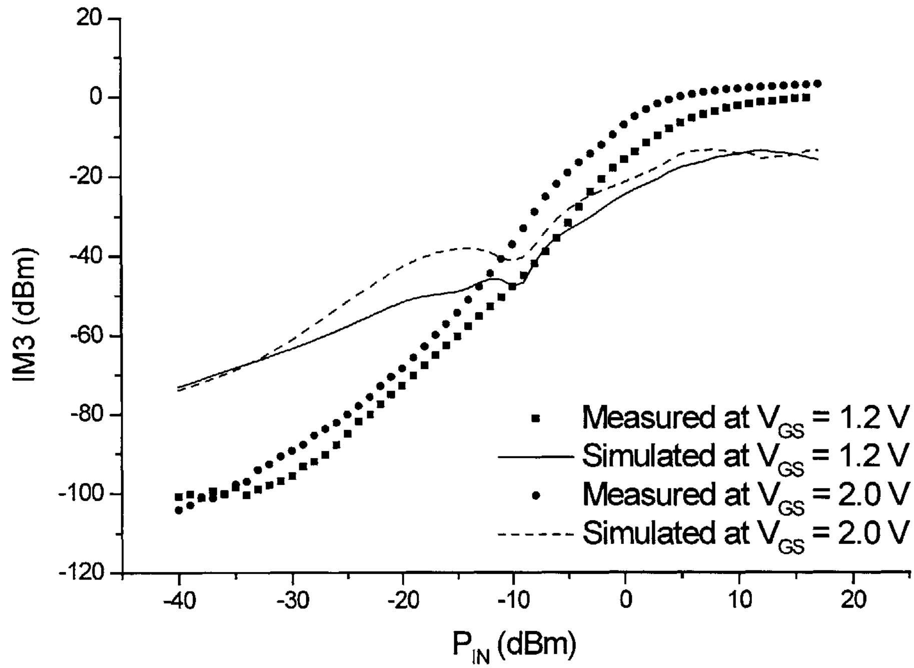

Figure 5-16: IM3 simulations and measurements for SOI (RB3) device
with L_G = 0.7 μm and W_G = 800 μm (20x40 μm) at V_{DS} = 3.6 V and varying V_{GS} and frequency = 1.9 GHz.

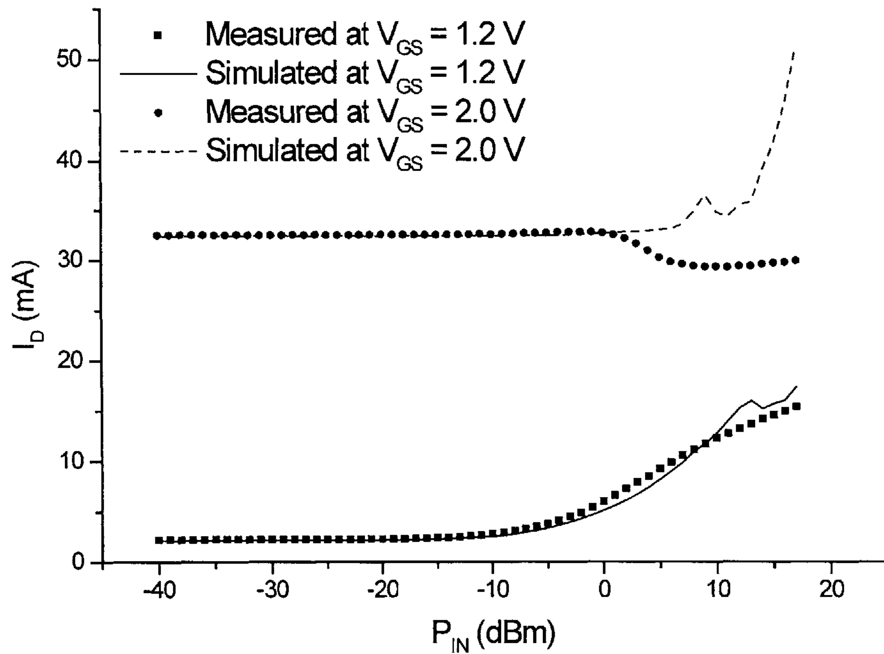

Figure 5-17: Bias current simulations and measurements for SOI (RB3) device
with L_G = 0.7 μm and W_G = 800 μm (20x40 μm) at V_{DS} = 3.6 V and varying V_{GS} at frequency = 1.9 GHz.

5.3.3 Smaller Gate Width Device

Since it seems that the lack of DC current and S-parameter measurements in the linear region contributes to Root Model inaccuracies, a device with a smaller gate width (200 μm, 10 fingers each with a width of 20 μm) at row 4, column 3 has been measured. Being a smaller device, DC current and S-parameter measurements can be taken at a higher V_{GS} without exceeding the 100 mA current compliance.

The model simulations for PAE, IM3, and bias current match the load-pull measurements better for this smaller gate width device as compared to a larger gate width device (800 μm, 20 fingers with 40 μm finger width), as shown in Figures 5-18 to 5-20. For the first time with high current bias, peak PAE in the simulation is higher than measurements. This indicates that having more DC current and S-parameter measurements available for Root Model extraction can improve the accuracy of the model.

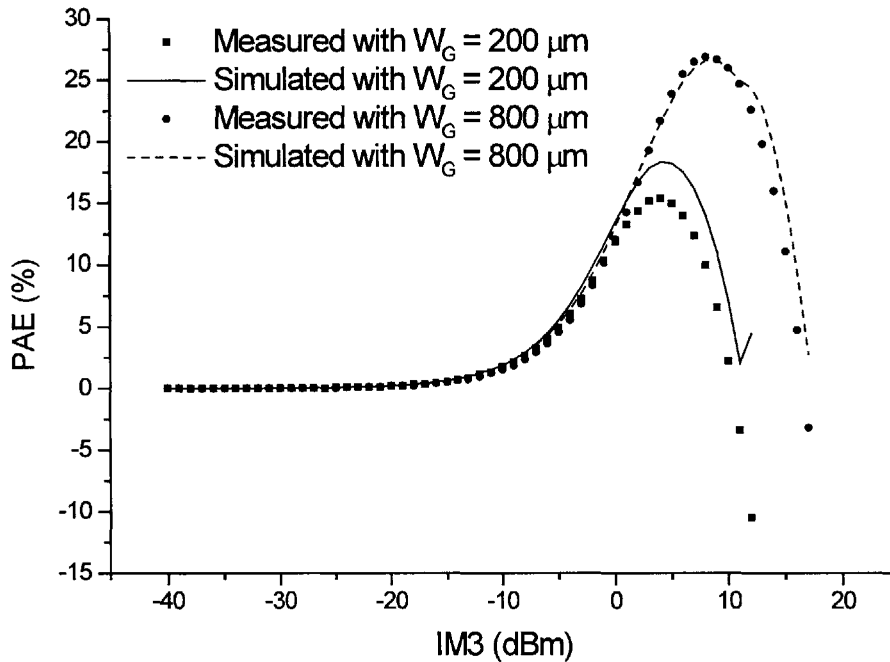

Figure 5-18: PAE simulations and measurements for bulk (055) device at V_{DS} = 3.6 V, V_{GS} = 2.65 V and frequency = 1.9 GHz with L_G = 0.7 μm and different device widths.

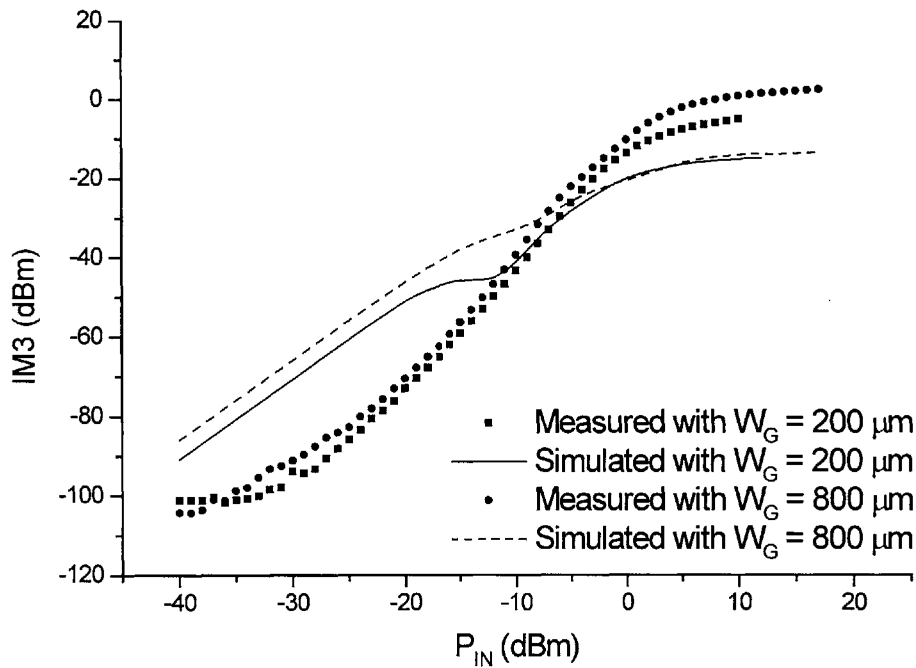

Figure 5-19: IM3 simulations and measurements for bulk (055) device
at V_{DS} = 3.6 V, V_{GS} = 2.65 V and frequency = 1.9 GHz with L_G = 0.7 µm and different device widths.

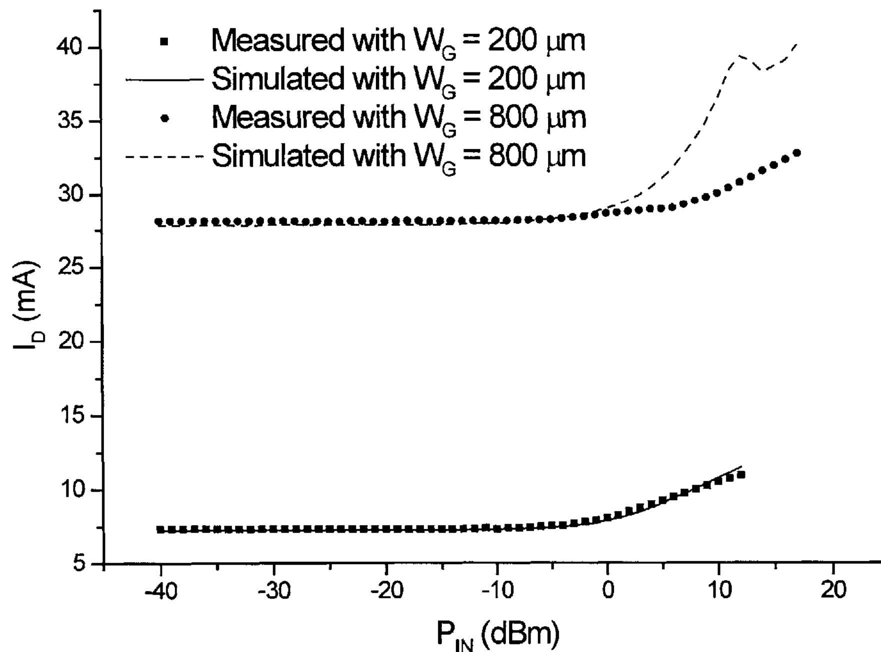

Figure 5-20: Bias current simulations and measurements for bulk (055) device
at V_{DS} = 3.6 V, V_{GS} = 2.65 V and frequency = 1.9 GHz with L_G = 0.7 µm and different device widths.

5.4 Closer Look at IM3 Simulations

For all of the simulations done for the range of biases and even for a smaller width device, the simulation results for IM3 do not match the load-pull measurements.

The mismatch at low input power may arise from lack of data measurements near the bias point. Thus, the simulator results for IM3 are based more on the spline interpolation of the model than on data for low input power. In an attempt to test this theory, more DC current and S-parameter measurements, at two different granularities, are taken just around the bias point for the smaller width device at row 4, column 3. These simulation results compared to load-pull measurements are shown in Figure 5-21. The simulation results for high input power do not match simulations, since such a small range of DC current and S-parameter measurements have been taken. The results for IM3 do not show a clear improvement from the earlier model extraction. In fact, the results for IM3 with more concentrated DC current and S-parameters taken for the Root Model extraction are even worse than the original simulations with the wide range of biases. Thus, further research is needed to determine why the Root Model cannot predict IM3 well for low input power.

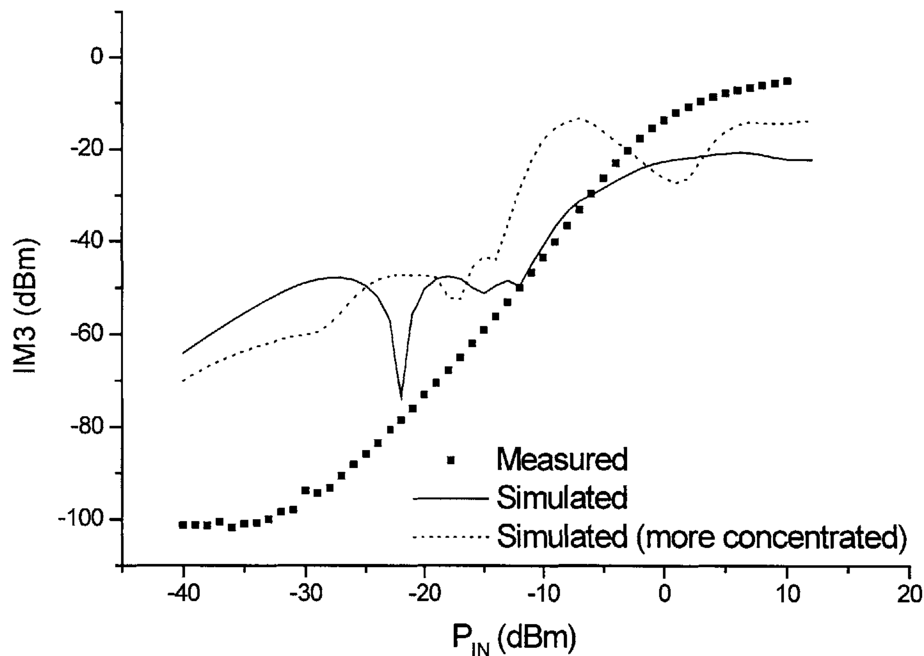

Figure 5-21: IM3 simulations extracted near the bias point for bulk (055) device with L_G = 0.7 μm and W_G = 200 μm (10x20 μm) at V_{DS} = 3.6 V, V_{GS} = 2.65 V and frequency = 1.9 GHz.

For high input power, it is possible that the mismatch arises from harmonic mismatch. In load-pull measurements, the tuner impedances for the second and third harmonics were set, but not recorded. Thus, the simulation setup does not match the measurement setup for the harmonics, which could lead to mismatch in the IM3 measurements for high input power.

To test this theory, the simulations have been repeated with a different tuner model. In the previous results, the tuners used in the simulations are based upon a physical design of a stub tuner modeled as a transmission line. Thus, there are impedances all throughout the frequency range as determined by the transmission line model for the tuners. For these new simulations, different tuners are used that are ideal and non-physical, presenting impedances at only the specified frequencies. These tuners are set to have the same tuner impedances at the fundamental frequency. Then simulations have been performed setting the tuner impedances at the second and third harmonics both to open (magnitude of 1 and angle of 0 degrees) and short (magnitude of 1 and angle of 180

degrees). Based on the IM3 simulations and measurements comparison in Figure 5-22, the tuner impedances for the second and third harmonics do not noticeably affect the simulations for the RF power figures of merit. The output voltage at the fundamental as well as second and third harmonics have also been simulated. The change in the output voltage is negligible when the tuner impedances for the second and third harmonics are varied from both being open to both being shorted.

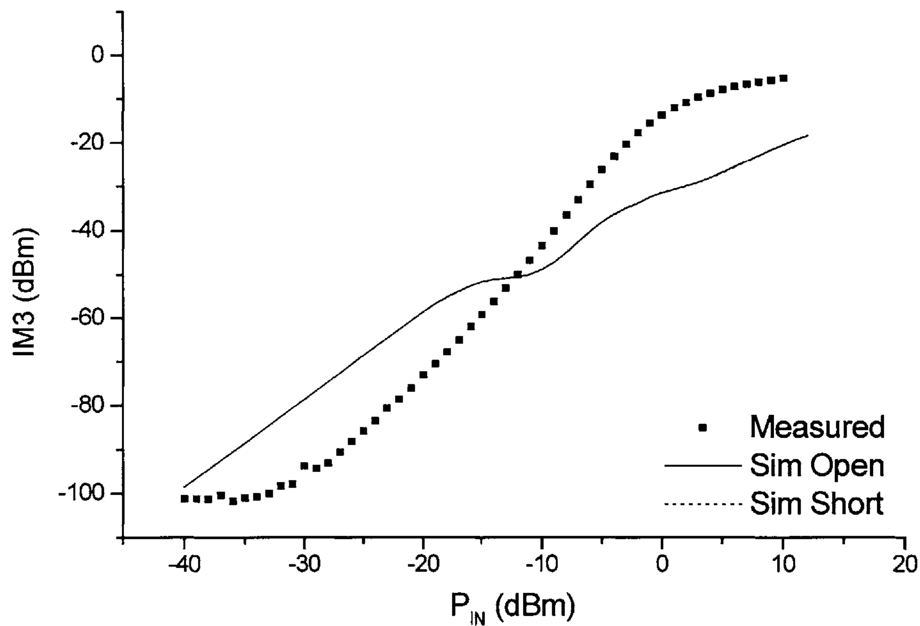

Figure 5-22: IM3 simulations with tuner harmonic impedances as opens and shorts for bulk (055) device with L_G = 0.7 μm and W_G = 200 μm (10x20 μm) at V_{DS} = 3.6 V, V_{GS} = 2.65 V and frequency = 1.9 GHz.

Thus, there needs to be more investigation to determine why the Root Model cannot be used to predict IM3. While analyzing the IM3 comparison, it is observed that the crossing point between model simulations and measurements is somewhere between -10 dBm and -5 dBm of input power. This is close to the amount of input power, measured to be –7.1 dBm using a HP 5347A power meter and a 50 Ω termination, delivered from the network analyzer port during Root Model extraction. Thus, the Root Model extraction process can be repeated at varying input power levels to determine if the IM3 crossing for simulation results and measurements changes. If that is the case, then it

shows that the Root Model is only accurate in predicting IM3 for similar input power as used in the extraction process.

5.5 Summary

When a series of measurements and simulations are analyzed, it is concluded that the Root Model is accurate for large-signal modeling of output power, power gain, efficiency, and drain current. There still needs to be more work done to determine if the Root Model can be used for non-linearity simulations. Drawn from the research results, it is expected that the model will be greatly improved if a wider range of DC current and S-parameter measurements are taken for Root Model extraction. To get a good model, a lot of data in the regions of operation is required.

Chapter 6

CONCLUSIONS AND FUTURE RESEARCH

6.1 Conclusions

In this work, bulk and SOI LDMOS devices have been measured for RF power figures of merit using a load-pull measurement system at IBM in Burlington, VT. The same devices have been used to extract a Root Model, from DC current and S-parameter measurements, using IC-CAP. The Root Model has been incorporated into Libra, a harmonic balance simulator, in a setup that matches the load-pull measurement system. Then the simulation results using the Root Model have been compared to the load-pull measurements for the RF power figures of merit, such as output power, power gain, PAE, IM3, and bias current.

Results from this research have led to a conclusion that the Root Model is reasonably accurate in large-signal modeling of both bulk and SOI LDMOS devices. For example, the simulation results for output power and gain are both accurate to within 1-2 dB. Simulations for PAE also match the shape of the measurement curve and are within an average of 15% percent of the peak PAE measurements. Bias current simulations match measurements well for low biases, but there are mismatches for high biases. Such discrepancies in modeling are likely to be attributed to the lack of DC current and S-parameter measurements in the linear region for high gate voltages during Root Model extraction. This limitation is due to the current compliance of the measurement instruments used in this research. To address this limitation, a smaller gate width device has been measured over a wider range of gate voltages. This device has been simulated and the results show a better match to the measurements, with the simulations for peak PAE actually higher than the measurements. The bias current simulations also more closely match for this smaller width device.

IM3 simulations do not match load-pull measurements very well. Attempts have been made to determine the reason for this, but these results have been inconclusive. It is likely that the mismatch in IM3 at low input power results from DC current and S-parameter data being too coarse around the bias point. More measurements have been taken, but the results do not conclusively indicate that a finer granularity of DC current and S-parameter measurements near the bias point will improve IM3 simulations for low input power. The discrepancy in IM3 simulations compared to load-pull measurements for high input power do not arise from harmonic mismatch. Since the tuner impedances for the second and third harmonics have not been recorded during the load-pull measurements, the simulation environment cannot be set up to match the measurement setup. This may have caused the mismatch in IM3 for high input power, when device non-linearities are significant. Additional simulations have been done using non-physical tuners to set the tuner impedances at the second and third harmonics to the two extremes, both being open or shorted. Comparative results of these simulations suggest that the tuner impedances at the second and third harmonics do not significantly affect the RF power figures of merit, including IM3.

Consequently, the Root Model has been shown to work for bulk and SOI LDMOS devices, although the results for the bulk devices seem to be better than results for the SOI devices, perhaps due to self-heating effects.

6.2 Suggestions for Future Research

Based on the research results, the Root Model will be more accurate if a wider range of DC current and S-parameter data can be measured for larger gate voltages. This research is limited by the measurement instruments, which are unable to handle currents larger than 100 mA. If a high power unit for the HP 4155 is obtained, DC current can be measured up to 1 A. This allows for a wider range of DC current and S-parameter measurements in extracting the Root Model. Given more data points, a more accurate model can be generated. Alternatively, using a HP 8510 network analyzer instead of the HP 8753 can probably lead to improvements in model extraction. HP 8510 is a newer

system—faster and more accurate. This may fix the timing issues that are occurring with the HP 8753 and the Sun workstation. As a result, the measurement process used to extract the Root Model may run for a longer period of time—to obtain more points to get a better model. Also, if a more stable system is set up, the averaging factor used in the network analyzer could be increased to obtain more accurate S-parameters measurements, which can also improve the model.

More research is still needed to determine why the Root Model is unable to accurately predict IM3. Although attempts have been made to try to resolve this issue, no concrete results have been determined to date. One concern is that the input power level during Root Model extraction was not very small. The Root Model simulations are only accurate for input power levels greater than that used during S-parameter extraction. Repeating the DC current and S-parameters measurements for Root Model extraction at a lower input power may help improve the accuracy of the simulations.

Another area for future research is to use a device simulator, such as MEDICI, to generate the DC current and S-parameter data to extract the Root Model, using IC-CAP. The simulations can be done in Libra to determine the RF power figures of merit before the device is even fabricated. Then the RF power figures of merit of a conceptual device can be obtained completely in the simulation environment, before the devices are fabricated. If this system is shown to be accurate in predicting RF power figures of merit, a powerful new tool in device design will be available. The device designer would be able to optimize the device at the design level for the RF power figures of merit without having to process many generations of devices. This will directly lead to large savings of time and money in developing RF power devices.

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[17] The gate current, I_G, is measured by IC-CAP to be in the μA range. This is believed to be leakage current in the bias-T's of the network analyzer.

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[19] Assuming that Q_G can be written in the form of $e^{i\omega t}$, Y_{11} is derived from the following relation:

$$Y_{11} = \frac{\partial I_G}{\partial V_G} = \frac{\partial\left(\frac{\partial Q_G}{\partial t}\right)}{\partial V_G} = \frac{\partial Q_G}{\partial V_G} i\omega$$

[20] The following formulas are used to convert from S-parameters to Y-parameters:

$$Y_{11} = \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$$

$$Y_{12} = \frac{-2S_{12}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$$

$$Y_{21} = \frac{-2S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$$

$$Y_{22} = \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$$

[21] D.E. Root, "Measurement-Based Active Device Modeling for Circuit Simulation," *European Microwave Conference*, 1993.

[22] For a conservative field assumption, these equations must be true:

$$\frac{\partial \operatorname{Im}[Y_{11}](V_{GS},V_{DS})/\omega}{\partial V_{DS}} - \frac{\partial \operatorname{Im}[Y_{12}](V_{GS},V_{DS})/\omega}{\partial V_{GS}} = 0$$
$$\frac{\partial \operatorname{Im}[Y_{21}](V_{GS},V_{DS})/\omega}{\partial V_{DS}} - \frac{\partial \operatorname{Im}[Y_{22}](V_{GS},V_{DS})/\omega}{\partial V_{GS}} = 0$$
$$\frac{\partial \operatorname{Re}[Y_{21}](V_{GS},V_{DS})/\omega}{\partial V_{DS}} - \frac{\partial \operatorname{Re}[Y_{22}](V_{GS},V_{DS})/\omega}{\partial V_{GS}} = 0$$

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[25] The following formulas are used to convert from S-parameters to Z-parameters:

$$Z_{11} = \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$$
$$Z_{12} = \frac{2S_{12}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$$
$$Z_{21} = \frac{2S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$$
$$Z_{22} = \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$$

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Appendix A: Sample Portion of Root Model File

```
File Format: MDS
Title: test
Date: Thu Mar  9 11:46:35 2000

Plotname: SP s-parameter[1].para[1]
Flags: real
No. sweep variables: 1
Sweep Variables:
No. Variables: 14
No. Points:    1
Variables:  0     swp    element plot=0 grid=1
        1     rs     element plot=0 grid=1
        2     rg     element plot=0 grid=1
        3     rd     element plot=0 grid=1
        4     ls     element plot=0 grid=1
        5     lg     element plot=0 grid=1
        6     ld     element plot=0 grid=1
        7     r1s    element plot=0 grid=1
        8     r2s    element plot=0 grid=1
        9     nfg    element plot=0 grid=1
        10    width  element plot=0 grid=1
        11    tau    element plot=0 grid=1
        12    taug   element plot=0 grid=1
        13    omega0 element plot=0 grid=1
Values:
0  0.0   11.51 13.71 30.84 1e-15 1e-15 1e-15 2.557 3.009 20 4e-05 1e-17 0 1.19381e+10
#

File Format: MDS
Title: test
Date: Thu Mar  9 11:46:35 2000

Plotname: SP s-parameter[1].cr[1]
Flags: real
No. sweep variables: 1
Sweep Variables:     vgs 0
No. Variables: 7
No. Points:    35
Variables:  0  vds  voltage plot=0 grid=1
    1  vgs  voltage plot=0 grid=1
    2  id   element plot=0 grid=1
    3  ig   element plot=0 grid=1
    4  qd   element plot=0 grid=1
    5  qg   element plot=0 grid=1
    6  idh  element plot=0 grid=1
Values:
0  0   0  -4.599e-08  -6.3781e-09  -1.89603e-12  -2.33491e-12  -0.0262795
1  0.2  0  2.34896e-07  1.6096e-07  -2.2543e-12  -2.36084e-12  -0.0284087
2  0.4  0  5.79056e-07  9.199e-08  -2.12854e-12  -2.38126e-12  -0.0287068
3  0.6  0  7.7494e-07  2.08409e-08  -2.80964e-12  -2.41841e-12  -0.0287742
4  0.8  0  9.19205e-07  2.6377e-09  -2.43802e-12  -2.42615e-12  -0.0329167
```

5 1 0 8.8792e-07 9.495e-08 -2.79151e-12 -2.453e-12 -0.0364388
6 1.2 0 1.13781e-06 8.51102e-08 -2.6324e-12 -2.48273e-12 -0.0384906
7 1.4 0 1.3724e-06 1.094e-08 -2.37568e-12 -2.50622e-12 -0.0432414
8 1.6 0 1.60699e-06 -1.25333e-07 -2.1097e-12 -2.53388e-12 -0.0455872
9 1.8 0 1.81143e-06 3.26775e-08 -1.89387e-12 -2.56193e-12 -0.0463882
10 2 0 2.00966e-06 -6.838e-08 -1.63334e-12 -2.59796e-12 -0.0469758
11 2.2 0 2.13926e-06 -1.9355e-09 -1.40789e-12 -2.63142e-12 -0.0475246
12 2.4 0 2.33725e-06 8.6958e-09 -1.17213e-12 -2.66248e-12 -0.0477649
13 2.6 0 2.60648e-06 2.15888e-08 -9.59111e-13 -2.68953e-12 -0.0478635
14 2.862 0 2.86168e-06 8.311e-08 -6.7152e-13 -2.72331e-12 -0.0478744
15 3.062 0 3.05269e-06 1.648e-08 -4.51932e-13 -2.74772e-12 -0.0478531
16 3.262 0 3.24471e-06 -6.324e-08 -2.30441e-13 -2.77191e-12 -0.0478024
17 3.462 0 3.55935e-06 -9.2694e-08 -9.38977e-15 -2.79513e-12 -0.0477273
18 3.662 0 3.61867e-06 -1.18851e-08 2.09873e-13 -2.81872e-12 -0.047649
19 3.862 0 2.1822e-06 5.48582e-08 4.26998e-13 -2.84176e-12 -0.0475797
20 4.062 0 3.93968e-06 -8.515e-08 6.43833e-13 -2.86448e-12 -0.0475196
21 4.262 0 4.20702e-06 -4.158e-08 8.60328e-13 -2.8936e-12 -0.0474555
22 4.462 0 4.53473e-06 7.71753e-08 1.07548e-12 -2.91766e-12 -0.0473818
23 4.662 0 4.61705e-06 3.137e-08 1.28966e-12 -2.94066e-12 -0.0472955
24 4.862 0 4.63968e-06 -1.875e-09 1.50506e-12 -2.96358e-12 -0.0471695
25 5.079 0 5.08678e-06 1.50401e-07 1.73987e-12 -2.99187e-12 -0.0470242
26 5.279 0 5.27445e-06 1.4943e-08 1.95517e-12 -3.01399e-12 -0.0468869
27 5.479 0 5.48989e-06 -6.122e-08 2.1691e-12 -3.03634e-12 -0.0467653
28 5.679 0 5.68771e-06 -7.21219e-08 2.37949e-12 -3.05895e-12 -0.0466675
29 5.879 0 5.87128e-06 1.6054e-07 2.58817e-12 -3.08463e-12 -0.0465777
30 6.079 0 6.05067e-06 6.16361e-08 2.79678e-12 -3.10682e-12 -0.0464782
31 6.279 0 6.3255e-06 -6.39e-08 3.00608e-12 -3.12901e-12 -0.0463876
32 6.479 0 6.53631e-06 -8.4849e-09 3.21713e-12 -3.15002e-12 -0.0462854
33 6.679 0 6.70589e-06 7.39973e-08 3.4275e-12 -3.17097e-12 -0.0461849
34 6.879 0 6.93266e-06 7.92e-10 3.63596e-12 -3.1924e-12 -0.0461174
#

Plotname: SP s-parameter[1].cr[5]
Flags: real
No. sweep variables: 1
Sweep Variables: vgs 1.6
No. Variables: 7
No. Points: 13
Variables: 0 vds voltage plot=0 grid=1
1 vgs voltage plot=0 grid=1
2 id element plot=0 grid=1
3 ig element plot=0 grid=1
4 qd element plot=0 grid=1
5 qg element plot=0 grid=1
6 idh element plot=0 grid=1
Values:
0 0 1.6 -4.30957e-05 1.11665e-06 -2.49814e-12 -5.63905e-13 -0.0252137
1 0.2 1.6 0.000554197 1.53938e-06 -2.75616e-12 -6.43562e-13 -0.0266061
2 0.4 1.6 0.000724954 1.51502e-06 -2.55588e-12 -7.1632e-13 -0.0267877
3 0.6 1.6 0.000838325 1.53475e-06 -3.17469e-12 -7.99282e-13 -0.0268206
4 1.044 1.6 0.000996119 1.57699e-06 -3.03644e-12 -9.1909e-13 -0.0350885
5 1.765 1.6 0.00111842 1.53399e-06 -2.13899e-12 -1.06876e-12 -0.0442726
6 2.565 1.6 0.00121449 1.12783e-06 -1.17432e-12 -1.21692e-12 -0.0457612
7 3.365 1.6 0.00130346 1.12508e-06 -2.78221e-13 -1.32783e-12 -0.045558

8 4.128 1.6 0.00138618 1.5391e-06 5.64335e-13 -1.43101e-12 -0.0451894
9 4.723 1.6 0.00144659 1.07626e-06 1.21187e-12 -1.50746e-12 -0.044869
10 5.23 1.6 0.00149895 1.11092e-06 1.7645e-12 -1.57258e-12 -0.0444737
11 5.799 1.6 0.0015575 1.12668e-06 2.37233e-12 -1.6438e-12 -0.0440884
12 6.599 1.6 0.00164371 1.42202e-06 3.21869e-12 -1.73581e-12 -0.0435834
#

Plotname: SP s-parameter[1].cr[9]
Flags: real
No. sweep variables: 1
Sweep Variables: vgs 3.2
No. Variables: 7
No. Points: 12
Variables: 0 vds voltage plot=0 grid=1
1 vgs voltage plot=0 grid=1
2 id element plot=0 grid=1
3 ig element plot=0 grid=1
4 qd element plot=0 grid=1
5 qg element plot=0 grid=1
6 idh element plot=0 grid=1
Values:
0 0 3.2 -2.09664e-05 3.07055e-06 -3.01111e-12 1.40723e-12 -0.0248651
1 0.2 3.2 0.0123752 3.03249e-06 -2.98566e-12 1.35203e-12 -0.0121615
2 0.4 3.2 0.0239567 3.0641e-06 -2.96824e-12 1.29474e-12 -0.000382159
3 0.8878 3.2 0.046213 3.1042e-06 -2.85369e-12 1.13149e-12 0.0229866
4 1.443 3.2 0.0580961 3.20519e-06 -2.9024e-12 9.46461e-13 0.0239898
5 2.05 3.2 0.0622236 3.19249e-06 -1.71508e-12 7.54197e-13 0.0203401
6 2.85 3.2 0.0638082 3.12276e-06 -4.12629e-13 5.5973e-13 0.0202426
7 3.65 3.2 0.0643331 3.11925e-06 6.06143e-13 4.2524e-13 0.0206305
8 4.45 3.2 0.0646317 3.12015e-06 1.53833e-12 3.07372e-13 0.0212167
9 5.25 3.2 0.0647776 3.29228e-06 2.44184e-12 2.00533e-13 0.0219258
10 6.05 3.2 0.0649174 3.09365e-06 3.32248e-12 1.03754e-13 0.0227146
11 6.85 3.2 0.0651902 3.19349e-06 4.17989e-12 1.37804e-14 0.0235036
#

Appendix B: Variation between Different Model Runs

For each device, the DC current and S-parameters have been taken several times to determine the repeatability of the measurements and subsequent model generation. Although there are small discrepancies between runs, the difference was deemed negligible, as seen in Figures B-1 to B-5.

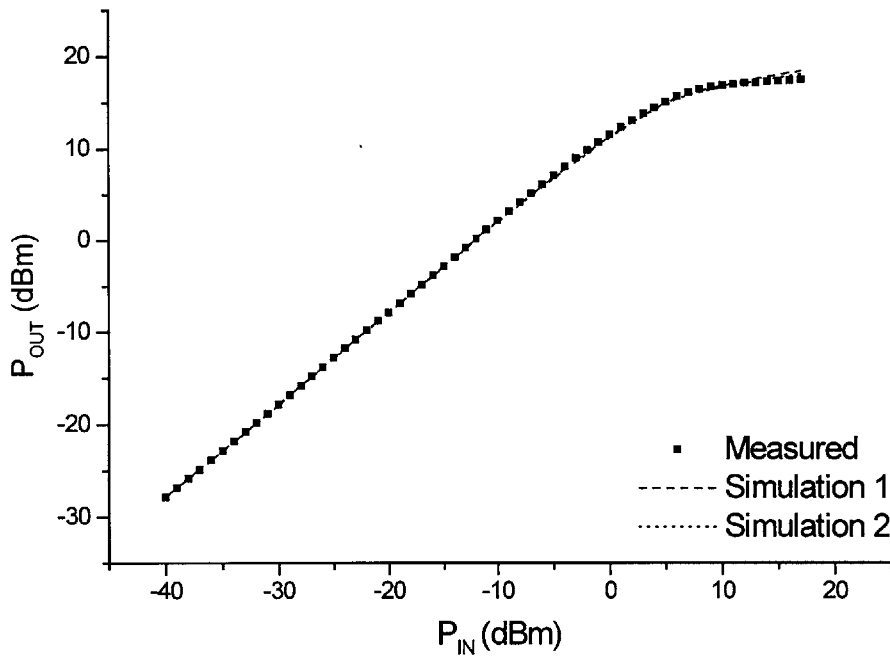

Figure B-1: Output power simulations and measurements for SOI (RB7) device with $L_G = 0.7$ μm and $W_G = 800$ μm (20x40 μm) at $V_{DS} = 3.6$ V, $V_{GS} = 2.64$ V and frequency = 1.9 GHz for different runs.

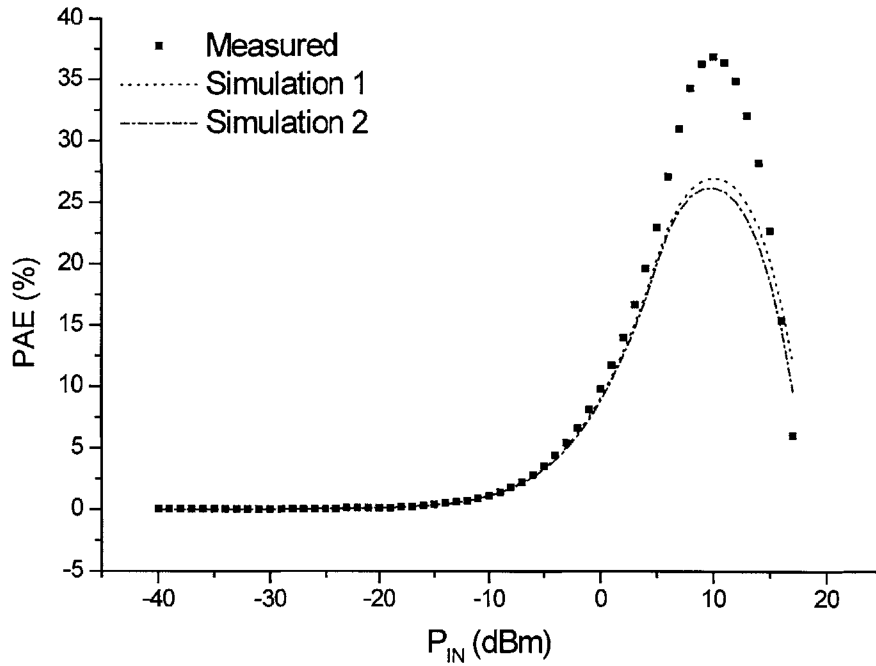

Figure B-2: PAE simulations and measurements for SOI (RB7) device with $L_G = 0.7$ μm and $W_G = 800$ μm (20x40 μm) at $V_{DS} = 3.6$ V, $V_{GS} = 2.64$ V and frequency = 1.9 GHz for different runs.

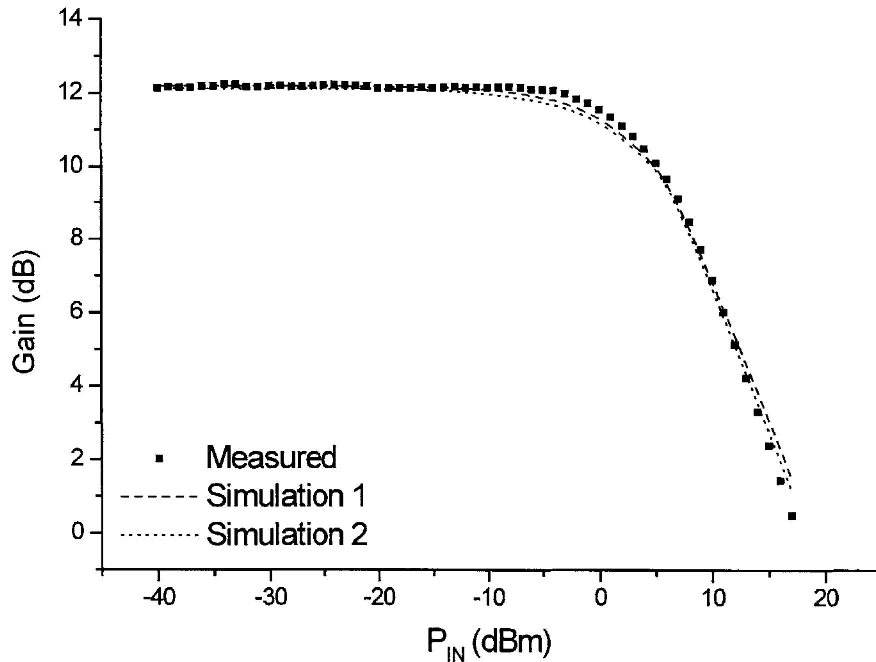

Figure B-3: Power gain simulations and measurements for SOI (RB7) device with $L_G = 0.7$ μm and $W_G = 800$ μm (20x40 μm) at $V_{DS} = 3.6$ V, $V_{GS} = 2.64$ V and frequency = 1.9 GHz for different runs.

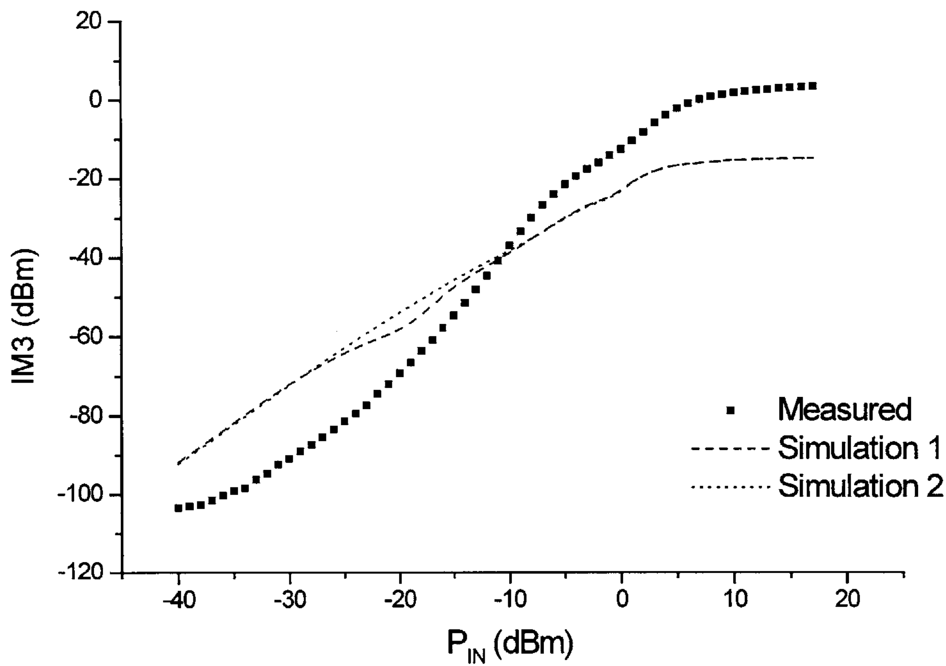

Figure B-4: IM3 simulations and measurements for SOI (RB7) device with $L_G = 0.7$ µm and $W_G = 800$ µm (20x40 µm) at $V_{DS} = 3.6$ V, $V_{GS} = 2.64$ V and frequency = 1.9 GHz for different runs.

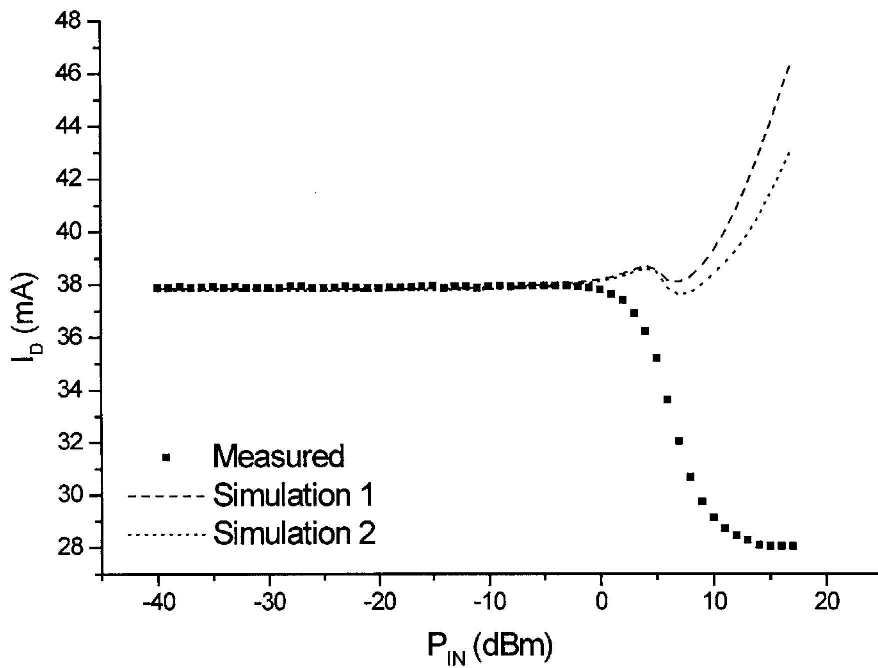

Figure B-5: Bias current simulations and measurements for SOI (RB7) device with $L_G = 0.7$ µm and $W_G = 800$ µm (20x40 µm) at $V_{DS} = 3.6$ V, $V_{GS} = 2.64$ V and frequency = 1.9 GHz for different runs.

Appendix C: More Results from Simulations and Measurements Comparison

Additional comparisons for bulk (055) and SOI (RB7 and RB3) devices are shown in Figures C-1 to C-12. These results show the same trends as discussed in Chapter 5, with simulations for bulk better than SOI devices and mismatches for IM3 simulations.

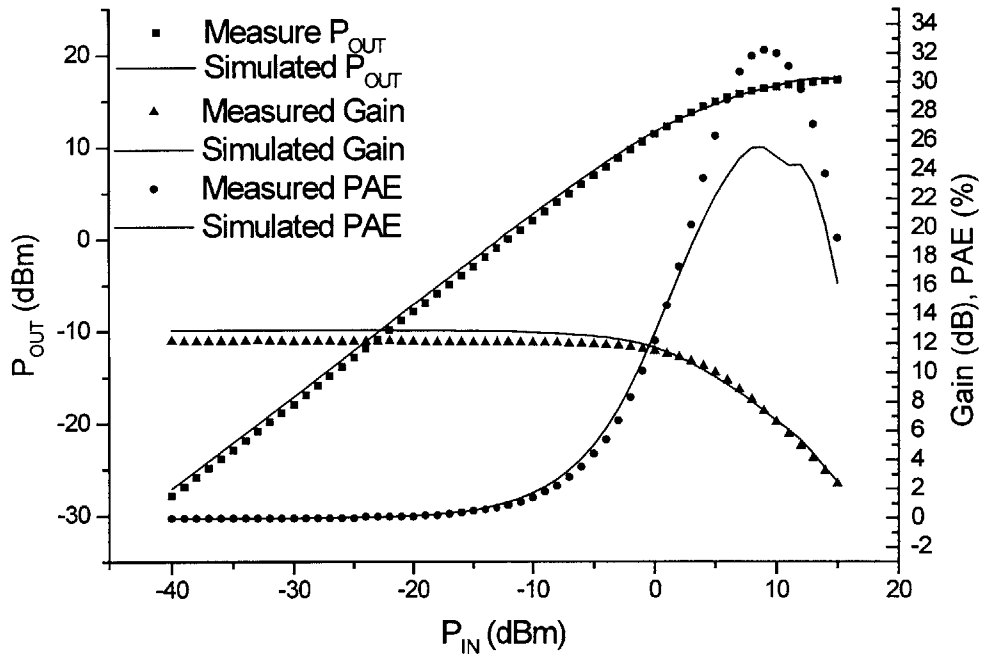

Figure C-1: Output power, gain, and PAE simulations and measurements for bulk (055) device with $L_G = 0.7$ µm and $W_G = 800$ µm (20x40 µm) at $V_{DS} = 3.6$ V, $V_{GS} = 2.651$ V and frequency = 1.9 GHz.

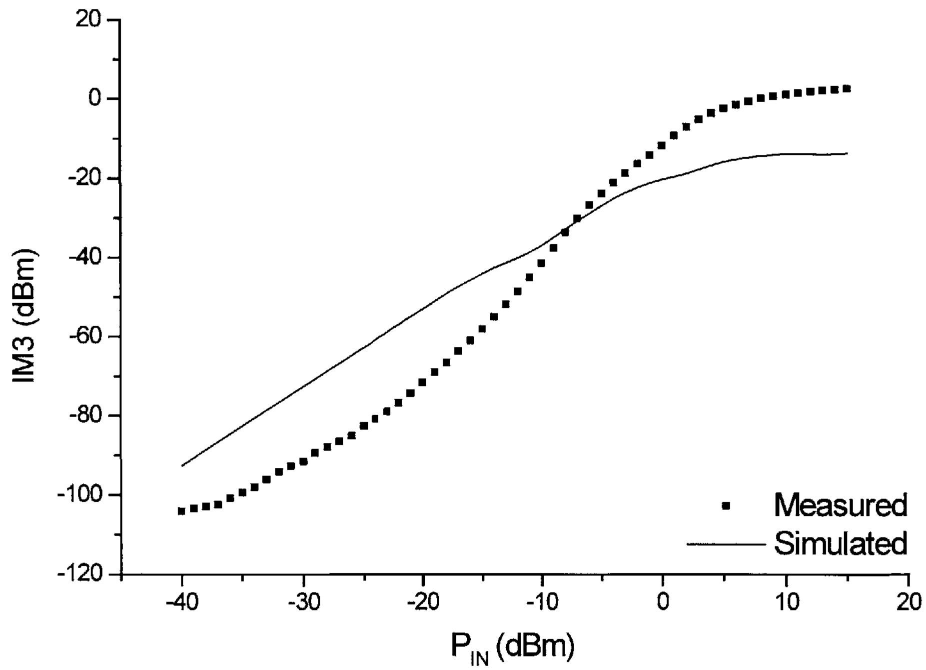

Figure C-2: IM3 simulations and measurements for bulk (055) device
with L_G = 0.7 μm and W_G = 800 μm (20x40 μm) at V_{DS} = 3.6 V, V_{GS} = 2.651 V and frequency = 1.9 GHz.

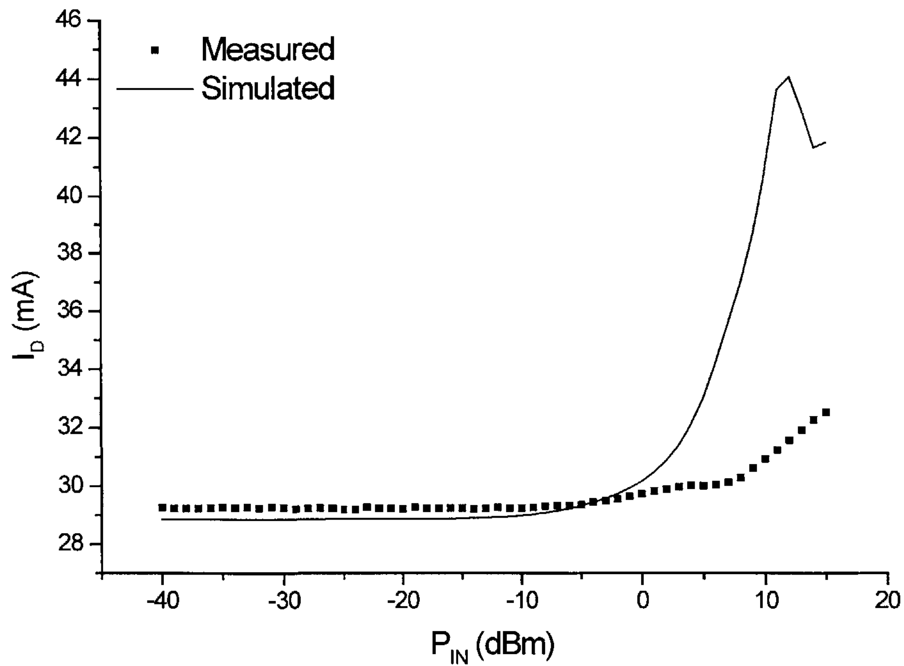

Figure C-3: Bias current simulations and measurements for bulk (055) device
with L_G = 0.7 μm and W_G = 800 μm (20x40 μm) at V_{DS} = 3.6 V, V_{GS} = 2.651 V and frequency = 1.9 GHz.

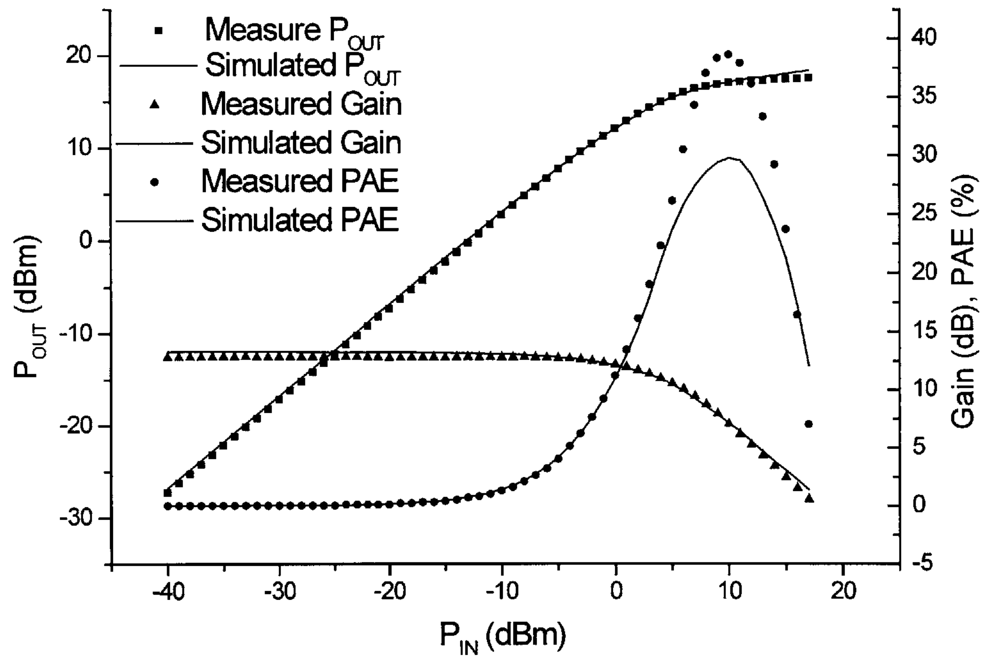

Figure C-4: Output power, gain, and PAE simulations and measurements for SOI (RB7) device with L_G = 0.7 μm and W_G = 800 μm (20x40 μm) at V_{DS} = 3.6 V, V_{GS} = 2.621 V and frequency = 1.9 GHz.

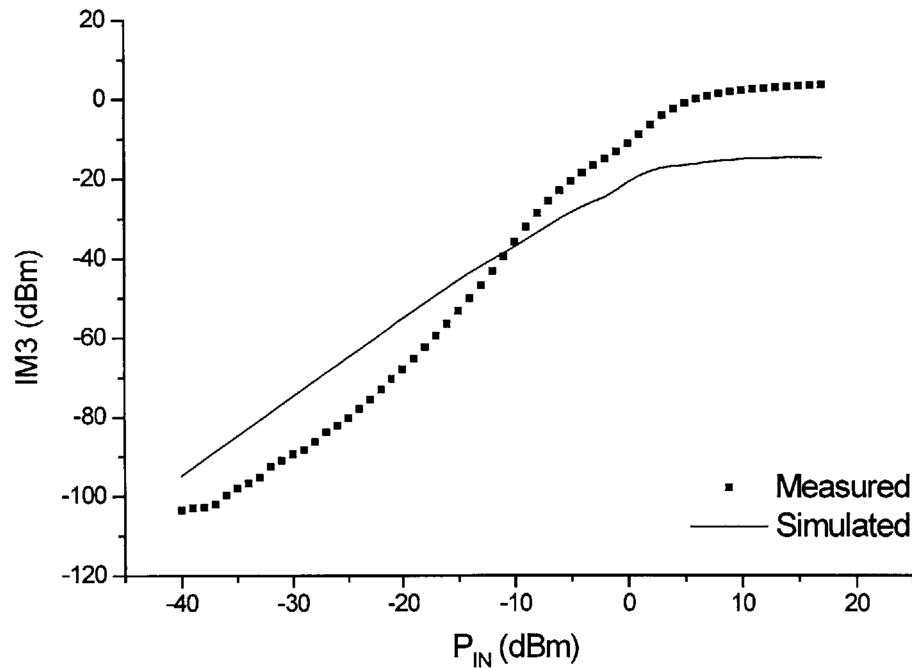

Figure C-5: IM3 simulations and measurements for SOI (RB7) device with L_G = 0.7 μm and W_G = 800 μm (20x40 μm) at V_{DS} = 3.6 V, V_{GS} = 2.621 V and frequency = 1.9 GHz.

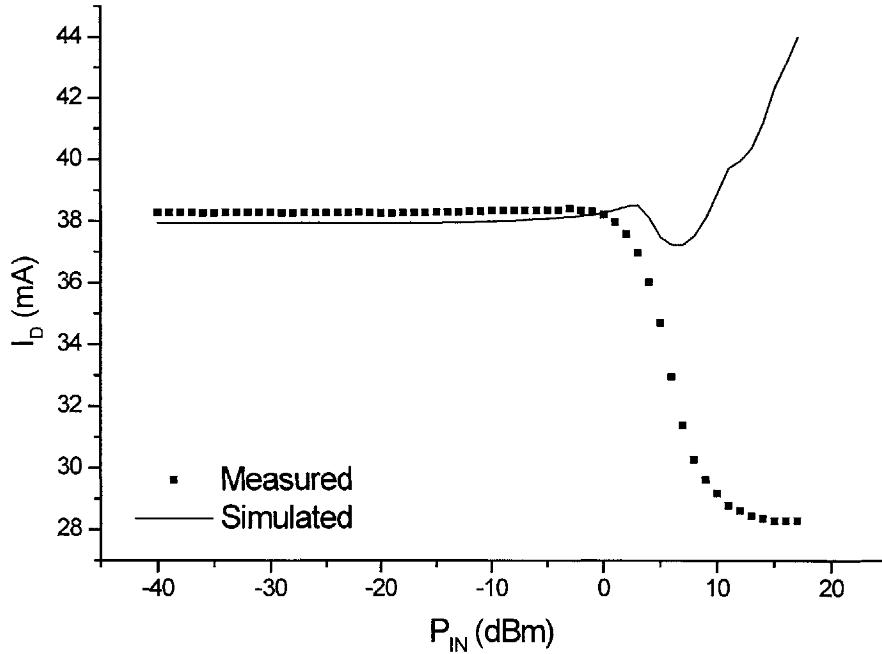

Figure C-6: Bias Current simulations and measurements for SOI (RB7) device with L_G = 0.7 μm and W_G = 800 μm (20x40 μm) at V_{DS} = 3.6 V, V_{GS} = 2.621 V and frequency = 1.9 GHz.

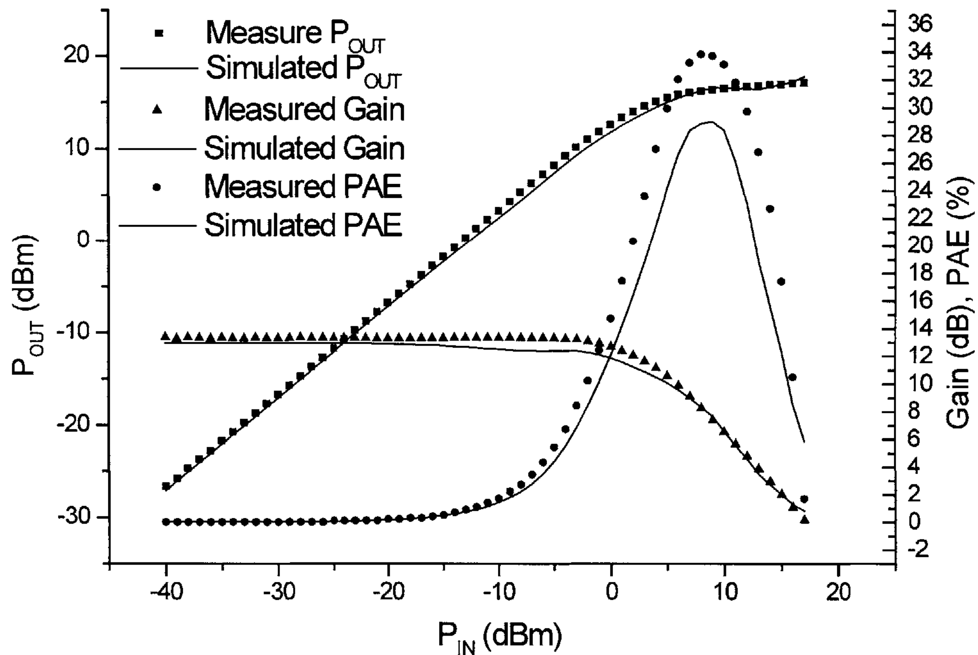

Figure C-7: Output power, gain, and PAE simulations and measurements for SOI (RB3) device with L_G = 0.7 μm and W_G = 800 μm (20x40 μm) at V_{DS} = 3.6 V, V_{GS} = 2.000 V and frequency = 1.9 GHz.

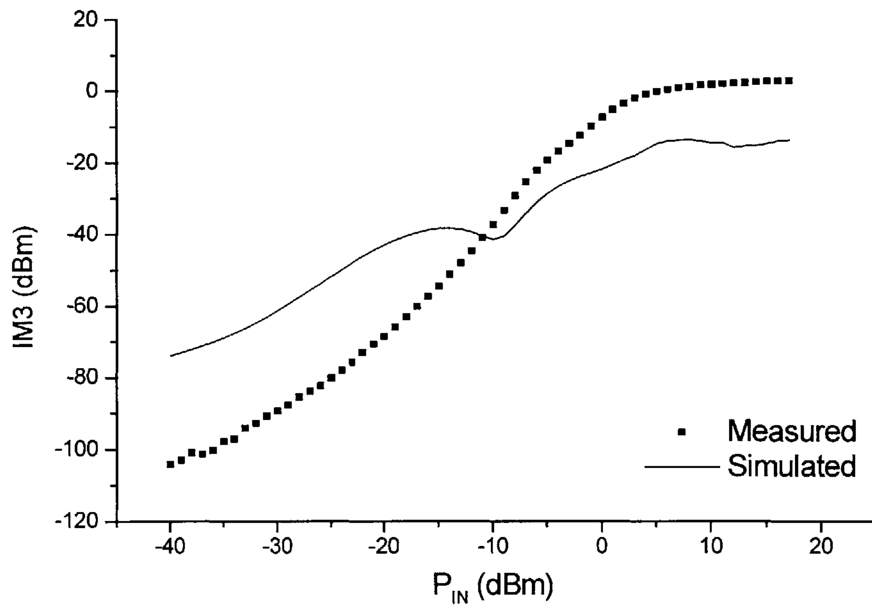

Figure C-8: IM3 simulations and measurements for SOI (RB3) device
with $L_G = 0.7$ μm and $W_G = 800$ μm (20x40 μm) at $V_{DS} = 3.6$ V, $V_{GS} = 2.000$ V and frequency = 1.9 GHz.

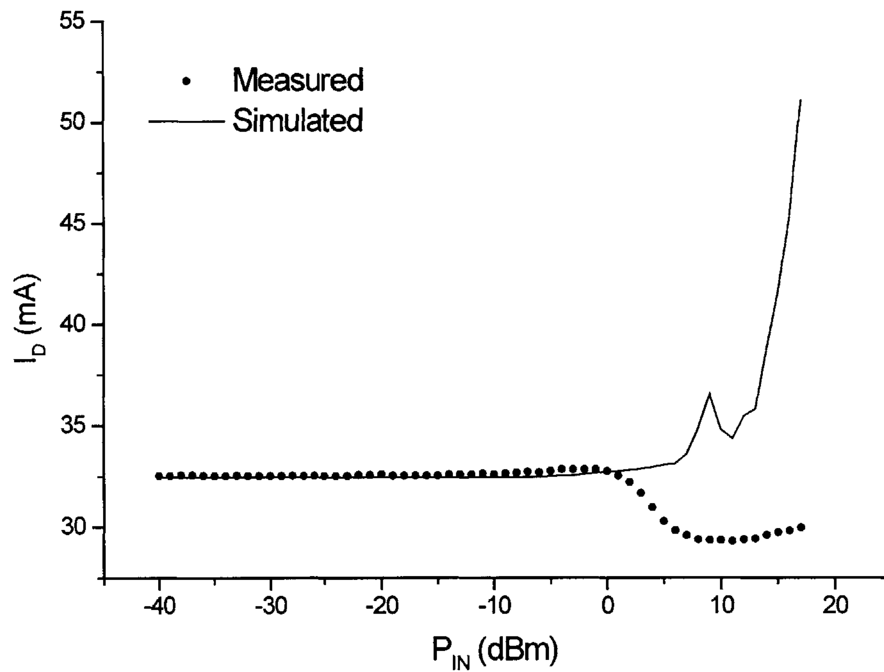

Figure C-9: Bias current simulations and measurements for SOI (RB3) device
with $L_G = 0.7$ μm and $W_G = 800$ μm (20x40 μm) at $V_{DS} = 3.6$ V, $V_{GS} = 2.000$ V and frequency = 1.9 GHz.

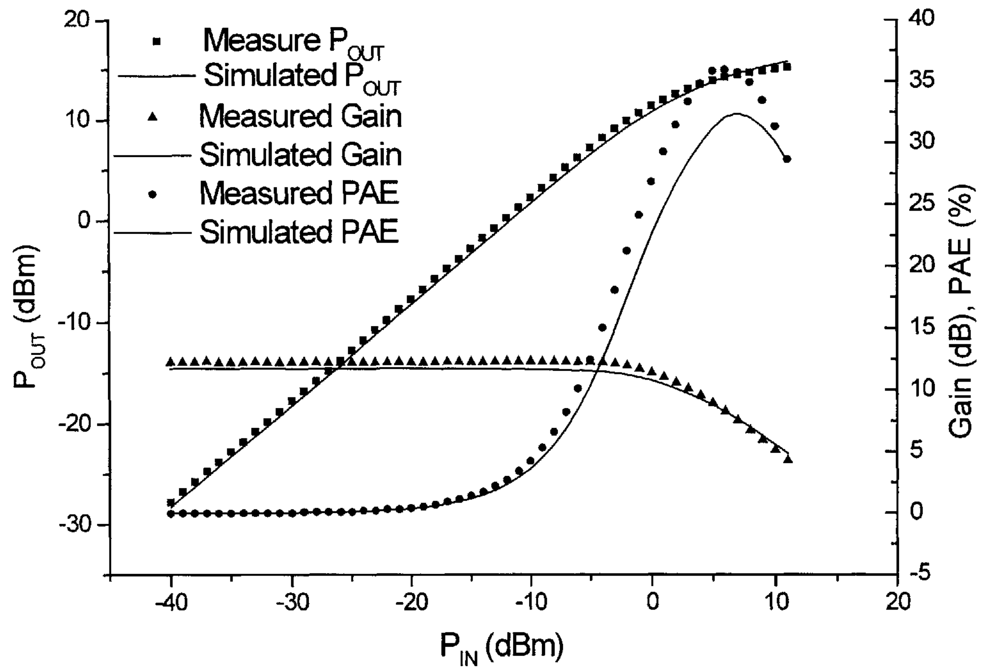

Figure C-10: Output power, gain, and PAE simulations and measurements for SOI (RB3) device with $L_G = 0.7$ μm and $W_G = 800$ μm (20x40 μm) at $V_{DS} = 3.6$ V, $V_{GS} = 1.58$ V and frequency = 1.9 GHz.

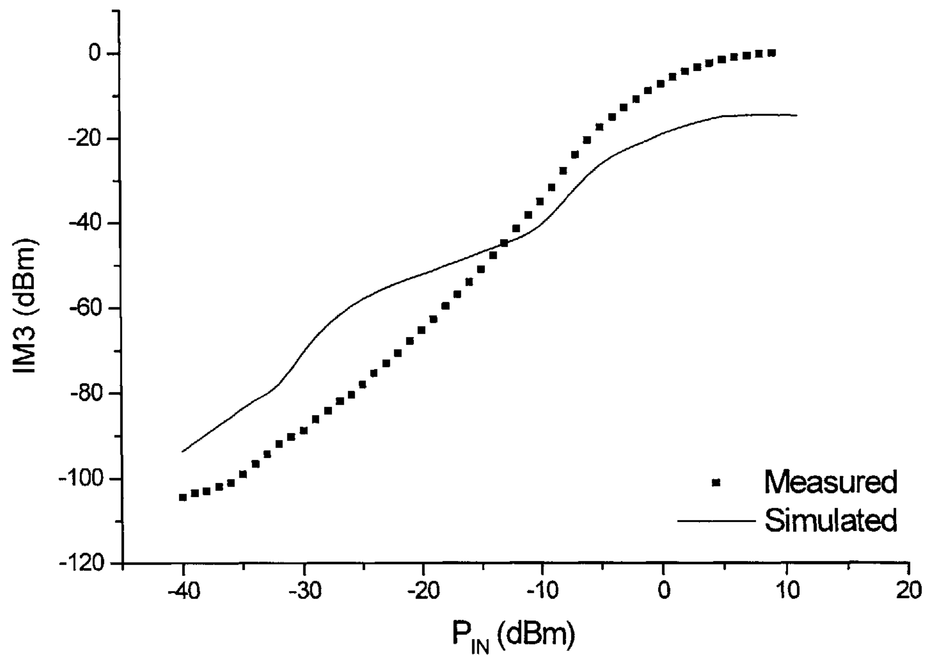

Figure C-11: IM3 simulations and measurements for SOI (RB3) device with $L_G = 0.7$ μm and $W_G = 800$ μm (20x40 μm) at $V_{DS} = 3.6$ V, $V_{GS} = 1.58$ V and frequency = 1.9 GHz.

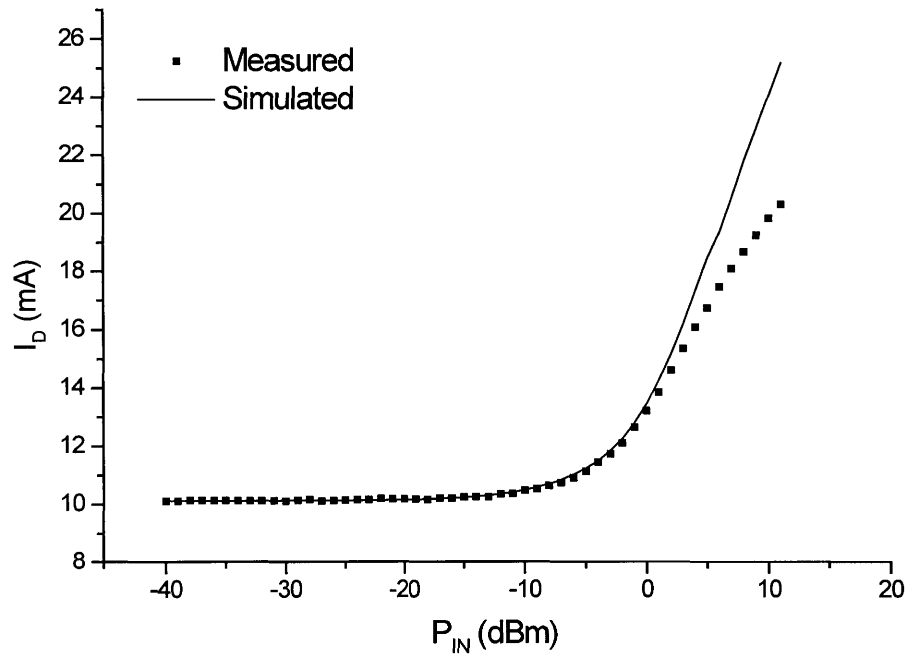

Figure C-12: Bias current simulations and measurements for SOI (RB3) device with $L_G = 0.7$ μm and $W_G = 800$ μm (20x40 μm) at $V_{DS} = 3.6$ V, $V_{GS} = 1.58$ V and frequency = 1.9 GHz.