Making Handheld Devices Smaller: A Boost Converter that Uses Minimum Board Space

by

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Submitted to the Department of Electrical Engineering and Computer Science

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Abstract

A method to decrease the board space of a boosting switching regulator is to increase the switching frequency. Specifications for a monolithic switching regulator operating at a nominal 10MHz switching frequency are described. The application circuit demonstrates efficiencies approaching 75%, operates with up to 200mA of switch current, and switches with current slew rates of 150mA per nanosecond. The high frequency of operation leads to some interesting test and measurement problems. In particular, measurement of the rise and fall times of the switch current requires custom board construction. Further increases in the switching speed lead to diminishing returns in board space.

Thesis Supervisor: Charles Sodini

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1 Introduction

1.1 Handheld Devices

In the late 1950's an obscure Japanese company, Tokyo Tsushin Kogyo KK, revolutionized the electronics industry with a groundbreaking product offering: the transistorized radio.[1] The radios were an immediate success, and the newly renamed Sony Corporation[2] became an international leader in electronics. The company founders had the vision to tap into the undiscovered market for handheld devices [1]. Businesses worldwide mobilized to satiate the consumer hunger for portable electronics. Today there is a wide array of handheld products available, such as Discmans, MP3 players, cellular phones, personal organizers, and palmtop computers. Several companies serving the handheld market command capitalizations well above the fifty billion-dollar mark[3], indicating that the handheld market is one of the most lucrative markets in business today.

1.2 New Arrivals

Amazing new handheld devices will arrive in the near future. There has been some hoopla in the news about electronic books, especially after Steven King's recent release of the e-book *Riding the Bullet*. A substantial amount of effort has gone into producing electronic paper and ink at Xerox PARC and several research universities. Products using electronic ink technology should be available to consumers before the end of the decade [2]. One step beyond

[1] Texas Instruments released the first transistorized radio, which was also an immediate success. However, Texas Instruments only produced the radio as a marketing scheme for its transistors, and did not continue production after their first run of radios quickly sold out in the stores.
[2] The founders of the minute Tokyo Tsushin Kogyo KK, decided to change the name to something that would be more attractive to the American consumer.

handheld computing will be wearable computing. There will be those who are so enthralled with connectivity that they would wear their computer wherever they go [3]. The current trend to make handheld devices smaller, cheaper, and more powerful should continue well into the future.

1.3 About this Thesis

One of the most interesting stories in the handheld market has been the evolution of the mobile phone. Mobile phones have been around for years, yet they have only recently become ubiquitous. Up until the late nineties, mobile phones were rarely found outside of executives' luxury sedans. Today, one out of every three people in America has a cell phone [4]. There are many reasons why they only recently became popular. The mobile phones of the eighties were pricey and service was even pricier. Unfortunately, you would get a lot of phone for your money. The phones were so big that they could barely fit in a briefcase. Now that mobile phones can fit in a pocket, people actually want to buy them.

Manufacturers of handheld devices will do whatever it takes to make their products smaller, because they know a smaller product will be more attractive to customers. To do this, they need to minimize the space consumed by the electronics. The power supply, in particular, can occupy a small but significant amount of the board area. The power supply is necessary because the batteries in a handheld device are rarely at the appropriate voltage for the microprocessor and other logic circuitry. For example, new batteries in the back of a Palm Pilot supply 3V. As the batteries drain, their voltage also drops, and can fall all the way to 0V if they are fully discharged. Most of the logic in the Palm Pilot needs 3.3V to work, however, so the battery voltage needs a boost. Manufacturers of handheld devices want the smallest possible

[3] Sony has a market capitalization of 66 billion dollars and Nokia has a market capitalization of 212 billion dollars. To put this in perspective, Cisco, the corporation with the largest market capitalization, is valued at 301 billion dollars. All this information is from the end of the trading day on January 4th, 2001

boosting circuit for their product. Therefore, one of the most important goals for designers of boosting circuits is to make their circuit as small as possible.

This thesis involves the design, construction, and testing of an integrated circuit boost converter that occupies the smallest possible circuit board area. The printed circuit board area is dominated not by the integrated circuit itself, but by the external circuitry. The integrated circuit is only one of several components needed to boost the output voltage. There are also input and output capacitors, an inductor, and a diode. In particular, the inductor and the capacitors occupy the most significant amount of board space. The sizes of the inductor and the capacitors have an inverse relation to the switching frequency of the boost converter. Increasing the switching frequency of the regulator will therefore decrease the size of the total boost converter. The goal was to build a commercially viable converter with the highest possible switching frequency. This Masters thesis documents what was learned in the process of pushing today's switching power supply technology to its limits.

1.4 A Brief History of DC/DC conversion

There was a time when putting a radio into an automobile posed a significant technical challenge. Radios needed high voltage to operate, and the only voltage available in a car was the 6V battery. Galvin Manufacturing Corporation figured out that if they converted the 6V DC from the battery to the greater than 90V DC needed to electrify a vacuum tube, they could build a high quality and low cost audio amplifier and radio receiver. In order to get the 90V DC from 6V, they built the world's first commercial DC/DC switching converter, a synchronous vibrator power supply.

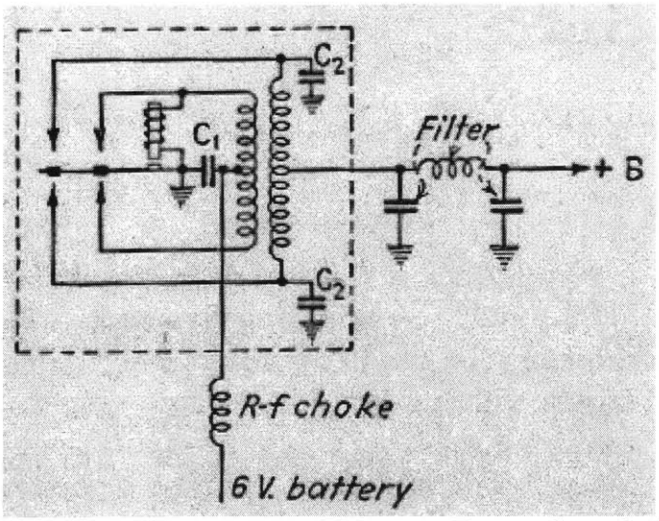

Figure 1-1: Synchronous Vibrator Power Supply [5]

To capture the idea of putting a radio in a motor car, the company gave the car radio product line the name Motorola. The car radio was so popular that the Galvin brothers soon changed their company name.

This great idea was only the beginning. Motorola's converter was noisy, bulky, inefficient, and prone to mechanical failure. The next big drive for improvements in power conversion came during the space race. Power supplies needed to be quiet, small, efficient, and extremely reliable, the exact opposite of their state at the time. Both industry and academics were supported through financial grants from the defense department to build the DC/DC converters needed to beat the USSR into space and to the moon. Further improvements came through continued support of the defense department, especially at the California Institute of Technology, where the modern control theory for switching regulators was developed [6]. Most the improvements since then have been driven by consumer-based demand for cheaper and smaller products.

2 Context

2.1 Scope

There are a few topics in DC/DC conversion where the author has the advantage of not only personal experience, but also expansive support from the staff of Linear Technology Corporation. These topics are investigated with the most amount of rigor.

Three areas in this thesis project are described in detail: the design of the switch, the performance of the application circuit, and measurement techniques. Although several months were spent designing the switching regulator, only a few facets of the design posed significant technical challenges. Monolithic[4] switching controllers have existed since the 1980's and it is doubtful that the design would garner academic interest [7].

The author does believe a 200mA switch that can operate at 10MHz with minimal power dissipation is a technically interesting creation. The design process is documented, focusing on the optimization of the switch. This process includes the choice of semiconductor technology and design driver circuitry.

The true test of the switch comes in the application circuit, when input to output efficiency is measured. The quality of the switch determines a majority of the efficiency loss in a power converter. The particularly important specifications will be the rise and fall times of the current in the switch, the on resistance of the switch, and the maximum output current of the switch.

Methods to perform measurements at high frequencies are dispersed in current literature. Any measurement techniques that were both nontrivial and important to characterizing the operation of the switching controller are carefully detailed. Some of the measurements pushed

[4] Monolithic – A monolithic switching converter includes the switching controller and the switch all in one chip.

available instruments to the specified limits of reliable operation. The action of taking some of the necessary measurements also altered the performance of the circuit.[5] These shifts in performance are accounted for and analyzed.

Other subjects investigated may be of interest to the reader. In particular, some performance of the integrated controller suffered because of the high switching frequency. In addition, in the course of modeling the switch and external components, insights were gained as to what the maximum possible switching frequency for a commercial boost controller might be. The author predicts a maximum frequency with some reservations. Those who have predicted limits to human capability have been predictably wrong.[6]

2.2 Approach

There are many different ways to approach the design of an analog circuit. A researcher can program a circuit with analog hardware description language, design a circuit with computer tools such as SPICE[7], hand design the circuit on paper, or breadboard a circuit on the bench. Each method has advantages and drawbacks in different applications. Analog hardware description language can be useful to those unfamiliar with analog design, but only if they need to meet low performance specifications. Computer tools such as SPICE are invaluable for the design of integrated circuits [8]. Designs based on SPICE simulations, however, should meet with practical experience as much as possible. Circuits that operate perfectly in SPICE simulations can fail miserably in the lab. For example, when the first design of the circuit was finished, and the simulated performance was acceptable, several staff members of the Linear

[5] Heisenberg's Uncertainty Principle has a parallel in analog electronics. All analog measurements, by nature, will alter the performance of the circuit being measured.
[6] "I confess that in 1901, I said to my brother Orville that man would not fly for fifty years... Ever since, I have distrusted myself and avoided all predictions." Wilbur Wright, 1908
[7] Simulation Program with Integrated Circuit Emphasis

Technology Corporation examined the circuit. They discovered design flaws that would cause the circuit to have miserable performance, and realized that the SPICE simulations were overly optimistic.

The best way to measure the performance of discreet based designs is through bench verification. SPICE simulations will sometimes lie[8]; the bench will generally tell the truth. There are caveats to this statement, however, in the cases of high frequency or high accuracy measurement techniques. In these cases, SPICE simulations will often lie[9], and without proper care, the bench will lie[10]. A project that necessitates high accuracy or high frequency measurement techniques should be approached with respect.

Hand calculating the performance of the circuit is also an invaluable exercise. Hand calculations will give the circuit designer a better understanding of his circuit, and therefore greatly aid him in both in troubleshooting and in improving performance. Every useful tool available was used in this design, including hand calculations, SPICE simulations, and thorough testing on the bench.

The best way to ensure this thesis would have timely relevance to the industrial community was to design the integrated circuit as if it would sell competitively in the open market. The power management integrated circuit market was 2.2 billion dollars in 1998, and continues to grow at a rapid pace [9]. Boost controllers comprise a significant portion of this

[8] The term 'lying' in reference to design may be unfamiliar to the casual reader. A manufactured circuit may have electrical characteristics that differ from those indicated in SPICE simulations. When a SPICE simulation indicates electrical characteristics significantly different from the electrical characteristics of the manufactured silicon, this is considered 'lying'.

[9] SPICE only gives results as accurate as the models it is given. If SPICE is given models that accurately predict the electrical characteristics of the transistors, and parasitics due to traces and packaging are taken into account, simulated performance should match well with measured performance.

[10] Poor measurement techniques can also indicate electrical characteristics that deviate from the true electrical characteristics of the circuit under test.

market. Improving the performance of boost controllers allows companies to maintain or increase their market share of this segment, and should be a profitable venture.

2.3 Prior Work

It is easy for an engineer to be caught up in a novel design and forget about the outside world. In the outside world there may be other researchers doing similar or more impressive work. It is important for an engineer to be keenly aware of the latest developments in his area of research; else, he may suffer from irrelevance.

Most of the research in the academic world has focused on high power designs using MOS switches. The designs have focused mainly on overcoming the limitations of the MOS switches, which have significant amounts of both gate and output capacitance. Driving the circuits adds a significant loss term. Experimental versions of power converters have reported switching frequencies of up to 14MHz [10].

Nearly all of the experimental designs of switching converters either required expensive components or processing techniques, or were application specific, and were far from being useful in a commercial situation. In order to achieve high frequencies, the researchers designed in flaws that made their designs commercially impractical. Commercial products available today gave a better guide for the design.

The biggest push for high frequency conversion today appears to be in the market for step down DC/DC conversion. Several companies have developed step down switching controllers with very fast frequencies. Their choice of switching frequencies elucidates the problems with switching at even higher frequencies. Efficiency decreases significantly with the increase in

speed of the switcher, and at some point the efficiency becomes so poor the switcher is unusable. Currently available step down converters switch at frequencies of up to 2 MHz.[11]

There are other methods to boost voltages than using switching regulators. A popular alternative is to use a switched capacitor charge pump. Switched capacitor charge pumps provide an attractive solution because they avoid the use of inductors, and occupy a small amount of board space. Charge pump circuits also provide a simple solution to disconnect the input from the output. Unfortunately, they draw current from the input in impulses, which adds a significant noise to the input supply. The output of a switched capacitor charge pump is also noisy compared to a switching regulator, unless the output is pre-regulated with a linear regulator. Switched capacitor charge pumps with linear regulated outputs do provide low noise outputs, but are inefficient. In general, switching regulators can provide more current, in a smaller amount of space, and with lower noise, than switched capacitor charge pumps.

Increasing the switching frequency is not the only way to decrease the total board space used in a boost converter. Improved packaging techniques such as 'flip chip' result in smaller solutions. Other external components such as the feedback resistor or the Schottky diode can be integrated into the chip. This unfortunately results in less flexibility for the applications engineer. If the feedback resistors are integrated, one chip would only be able to do one output voltage. The Schottky diode can be integrated as a switch, but only in a complementary process. A circuit that used all of these ideas could be made very small, but would be application specific.

[11] As demonstrated by the SEMTECH SC1144EVB.

2.4 System and Specifications

The integrated circuit is mounted in a five-pin SOT package. The typical application is boost conversion.

Typical Application

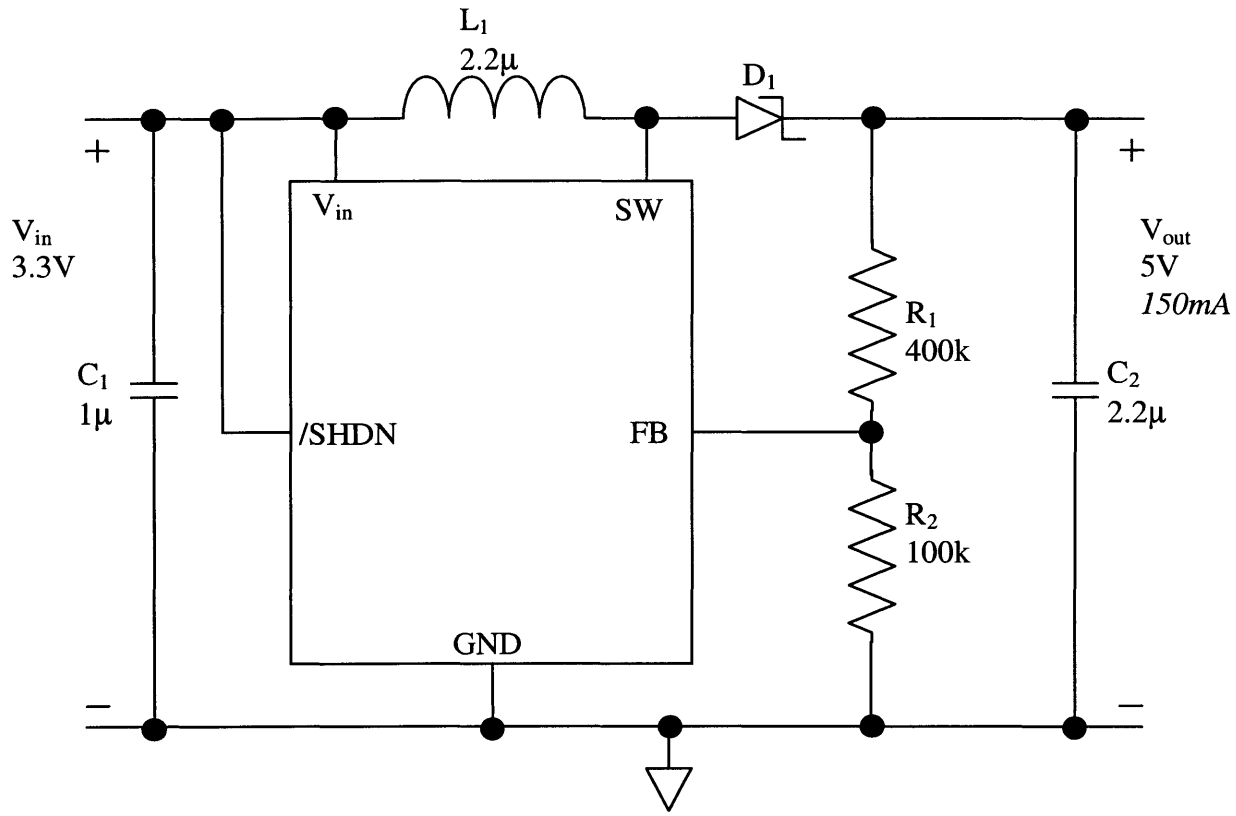

Figure 2-1: Typical Application of the Monolithic Boost Converter

The pin out in the typical application circuit corresponds to the numbered pins in Fig. 2-2. A boost converter works by switching inductor current between the output and ground. Inductor current, which corresponds to the input current, is only delivered to the output a fraction of each switching cycle. The fraction of the period the switch is on is called the duty ratio, and is often referred to simply as the letter D. The fraction of the switching cycle when inductor current is delivered to the output is therefore 1-D.

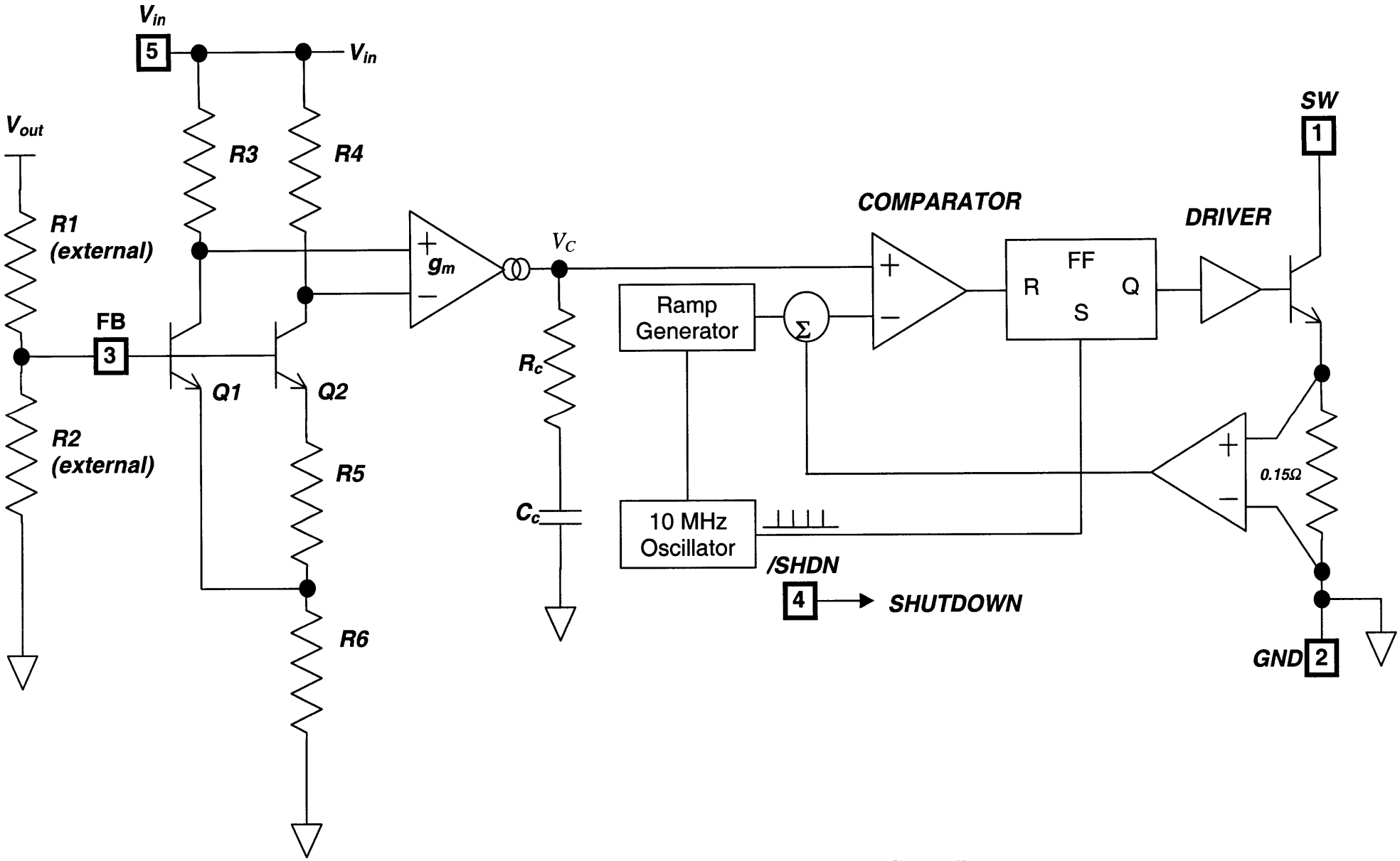

Figure 2-2: Block Diagram of the Monolithic Boost Controller

Since energy is conserved, the output voltage must be correspondingly greater than the input voltage:

$$V_{OUT} = \frac{V_{IN}}{1-D}$$

The architecture and the circuit design were based on the LT1613. By careful observation of the typical application circuit and block diagram, one can identify the control loop and understand the operation of the circuit. Resistors R1 and R2 are selected so that $V_{out} = 1.25V(1 + R_1/R_2)$. When V_{out} falls, the voltage at the FB pin will decrease. This increases the current out of the error amplifier, which increases V_C, the threshold of the comparator. Each cycle, the switch turns on and drops a positive voltage across the inductor. The current ramps upwards and is sensed by the 0.15 Ohm resistor. The sense voltage is amplified and compared to V_C. When it rises to a higher potential than V_C, the flip-flop resets and the switch turns off. The output current will therefore increase with increasing voltages at V_C. Increased current leads to increased output voltage and closes the negative feedback loop.

If the load is decreased, the switch will turn on for a shorter period each cycle. At even lighter loads, the converter will skip cycles to maintain output regulation.

Although design changes were required to increase the LT1613's switching frequency from 1.4 MHz to 10 MHz, the architecture remains the same. Some of the LT1613's impressive specifications were relaxed in order to speed up the design process, since a limited time was available. In particular, the circuit operates only to 2.4V, but the LT1613 operates down to 1.1V. Designing circuits that work at low-level voltages is both challenging and time consuming.

ELECTRICAL CHARACTERISTICS **The • denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A =25°C. V_{IN} =3.3V, V_{SHDN} =3.3V, unless otherwise noted.**

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage				**2.0**	**2.4**	**V**
Quiescent Current	**V_{SHDN} = 1.5V, Not Switching** V_{SHDN} = 0V			**4.7**	**6.1** 50	**mA** µA
Reference Voltage	**Measured at FB pin**	 •	 1.21	**1.24**	 1.27	**V** V
FB Pin Bias Current	**V_{FB} = 1.26V**	•		**150**		**nA**
Switching Frequency		•	**7**	10	13	MHz
Maximum Switch Duty Cycle		 •	**90** 76	92		%
Switch Current Limit		•	**220**	**350**		**A**
Switch V_{CESAT}	**I_{SW} = 150mA**			**200**	**240**	**mV**
Switch Leakage Current	**Switch Off, V_{SW} = 5V**	•		**0.01**	**5**	**µA**
SHDN Pin Current	**V_{SHDN} = 1.5V**			**65**	**100**	**µA**
Shutdown Threshold (SHDN pin)					**0.3**	**V**
Startup Threshold (SHDN pin)			**0.9**			**V**

Table 2-1: Electrical Characteristics of the Monolithic Boost Controller

These specifications were derived from testing the manufactured integrated circuit. The ranges of operation were chosen to allow for a high yield under a large production run, and were determined using known process variations. A manufactured circuit should only deviate from the specified electrical characteristics if process parameters are out of bounds, and this would be caught immediately by automatic test equipment.

2.4.1 Brokaw Cell

The circuit diagram of a Brokaw cell is shown in Figure 2-2, and is formed by Q1, Q2, R3, R4, R5, and R6 [11]. Transistor Q2 is scaled so it has a larger emitter area than Q1. When the feedback loop is closed around the total circuit, the collector currents are forced to be equal. This sets up a PTAT[12] voltage at the emitter of Q1. The voltage at the FB pin will be a sum of a V_{be}, which is CTAT[13], and a PTAT voltage. With appropriate scaling between R5 and R6, the voltage at the FB pin will be nearly independent of temperature.

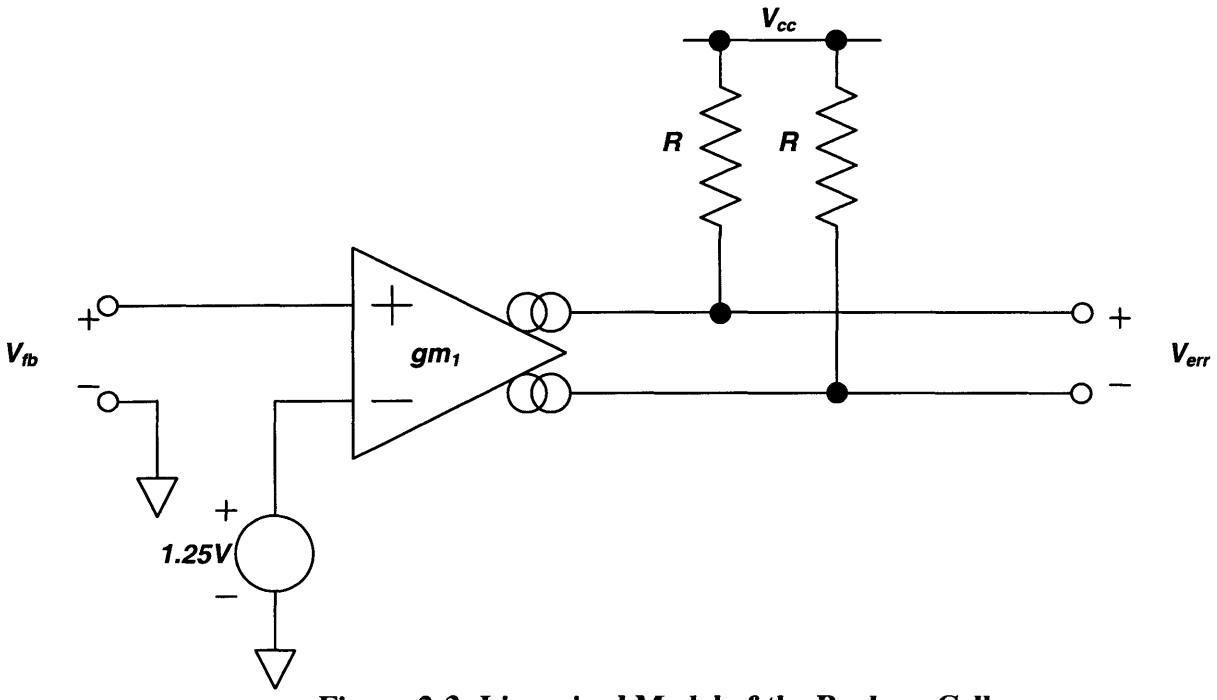

Figure 2-3: Linearized Model of the Brokaw Cell

A linearization of the Brokaw cell is shown in Figure 2-3. The Brokaw cell generates a differential output voltage that is proportional to the difference between the voltage at the FB pin and 1.25V. The input of the Brokaw cell is a high impedance, and the differential output is a

[12] Proportional To Absolute Temperature
[13] Conversely proportional To Absolute Temperature

lower impedance of 4.4k. The gain of this circuit is well below unity and has a marginal contribution to limiting the bandwidth of the feedback loop.

2.4.2 Error Amplifier and Compensation

The error amplifier generates an output current that is proportional to the difference in the voltages at its input. Both the input and the output are high impedances.

Error Amplifier

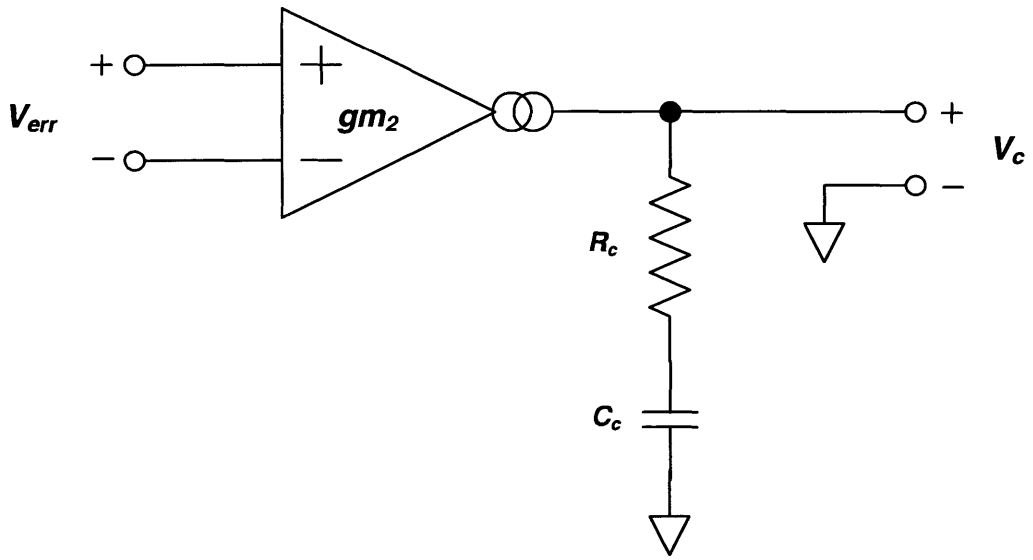

Figure 2-4: Linearized Model of the Error Amplifier

The compensation network provides both a pole and a zero. The pole is at a relatively low frequency, and the zero is at a higher frequency. The pole and zero are placed in locations to optimize transient response with a ceramic output capacitor. These components help determine the loop dynamics of the circuit. The transfer function of the circuit is calculated as follows:

$$\left|\frac{V_c}{V_{err}}\right| = gm_2 r_o \left\| \left(R_c + \frac{1}{sC_c} \right) = \frac{gm_2 r_o (sC_c R_c + 1)}{sC_c (r_o + R_c) + 1} \right.$$

The formulas are more manageable with a few simplifications. The first is to express the pole time constant in terms of the zero time constant by a factor of α. Lag type compensation is desired, so alpha must be greater than one. The lag compensation increases the open loop gain, but does contribute negative phase. This is acceptable because there is only ninety degrees of additional phase in the loop from the output capacitor, as long as the loop gain falls below unity well below the switching frequency of the converter [12].

$$T_p = \alpha T_z$$

$$H(s) = \frac{(T_z s + 1)}{(\alpha T_z s + 1)}$$

The phase of the transfer function over frequency is easily deduced from the transfer function:

$$\angle H(\varpi) = \tan^{-1}(T_z \varpi) - \tan^{-1}(\alpha T_z \varpi)$$

The frequency where the maximum phase dip due to the lag compensation is calculated by finding the zero crossings of the derivative:

$$\frac{d\angle H(\varpi)}{d\varpi} = \frac{T_z}{(T_z \varpi)^2 + 1} - \frac{\alpha T_z}{(\alpha T_z \varpi)^2 + 1} = 0$$

$$T_z^3 \varpi^2 (\alpha^2 - \alpha) - T_z(\alpha - 1) = 0$$

$$\varpi^2 = \frac{T_z(\alpha - 1)}{\alpha T_z^3 (\alpha - 1)}$$

$$\varpi = \frac{1}{T_z \sqrt{\alpha}}$$

The maximum phase dip therefore happens when the frequency is equal to the geometric mean of the two time constants:

$$\angle H\left(\varpi = \frac{1}{T_z \sqrt{\alpha}}\right) = \tan^{-1}\left(\sqrt{\alpha}\right) - \tan^{-1}\left(1/\sqrt{\alpha}\right)$$

For acceptable transient performance of the circuit, a maximum of 135 degrees of phase at crossover is allowed. The output capacitor contributes 90 degrees of phase. This allows for another 45 degrees of phase contribution from the compensation network. An α of six will lead to approximately 45 degrees of phase. An appropriate ratio between r_o and R_c can be determined:

$$T_z = R_c C_c$$

$$\alpha T_z = C_c (R_o + R_c)$$

$$R_c \approx \frac{1}{5} r_o$$

2.4.3 Ramp Generator

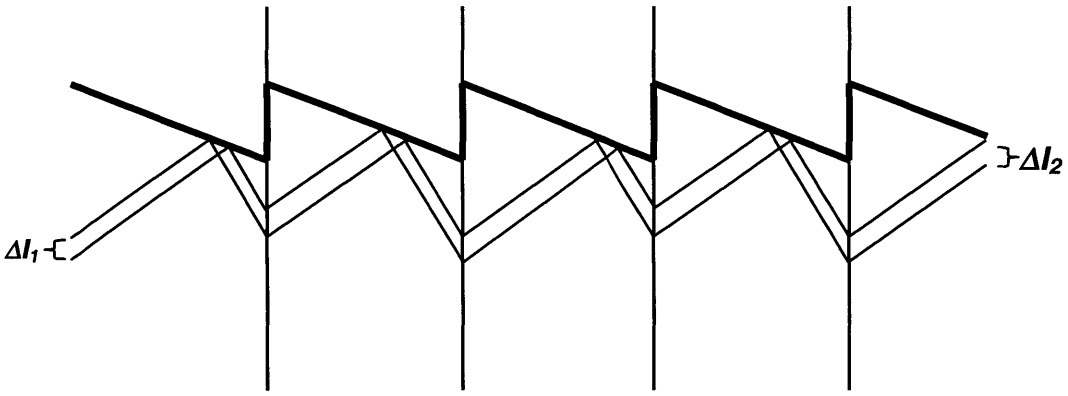

Figure 2-5: Perturbation with Slope Compensation

The ramp generator adds slope compensation to the current ramp created from the current sense amplifier. With slope compensation, a perturbation in the inductor current, such as ΔI_1, remains small or disappears after several cycles. There is enough slope compensation to prevent subharmonic oscillations under all normal operating conditions.

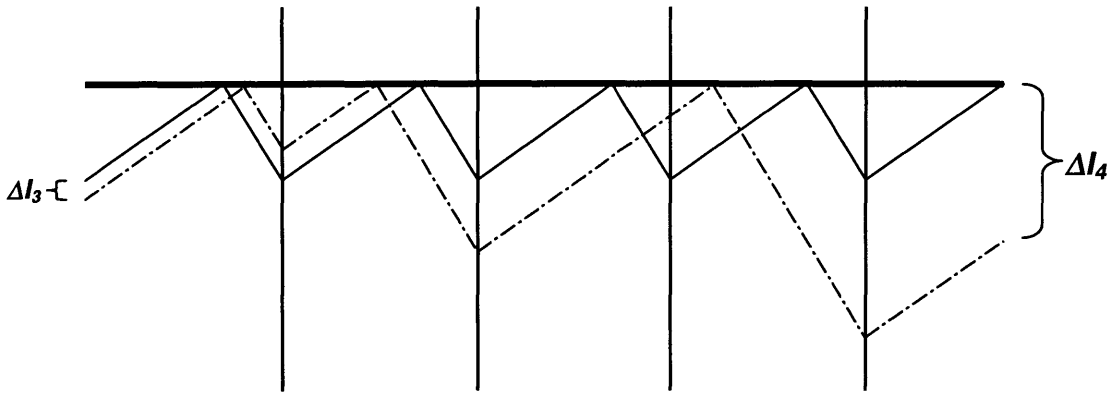

Figure 2-6: Perturbation without Slope Compensation

Without slope compensation, a small perturbation in the inductor current, such as ΔI_3, becomes increasingly larger, and the system is unstable for duty cycles greater than 0.5.

2.4.4 Oscillator

The oscillator is designed to operate at a nominal frequency of 10 MHz. The oscillator frequency will drift with supply and temperature variations. The oscillator should remain within plus or minus ten percent of nominal, under all operating conditions. One of the major advantages of fixed frequency control method is the predictable output frequency. If the switching frequency varies too much, the product will be unattractive to customers, because it can make the design of the application circuit difficult or impossible.

2.4.5 SR Flip Flop

Input			Output	
Present State	S	R	Q	Next State
DON'T CARE	↑	DON'T CARE	0	0
DON'T CARE	1	DON'T CARE	0	0
DON'T CARE	↓	0	1	1
DON'T CARE	↓	1	0	0
1	0	0	1	1
1	0	↑	0	0
0	0	DON'T CARE	0	0

Table 2-2: SR Flip-Flop Truth Table

2.4.6 Driver

The base drive requires more current than the digital logic can provide. The driver provides buffering between the output of the SR flip-flop and the switch. The driver is essentially a current booster, with anti-saturation circuitry for the switch.

2.4.7 Switch

The switch is a large NPN bipolar transistor. The layout is optimized for minimal input and output capacitance and even current distribution. The switch and the rest of the circuit are designed on a two-micron complimentary bipolar process, which has forward transit frequency of up to 6 GHz. Using a high frequency bipolar process leads to a minimal output capacitance on the switch, so the switch can operate at a very high frequency with low loss. A sense resistor is closely coupled with the switch.

2.4.8 Current Sense Amplifier

The current sense amplifier produces a voltage that is proportional to the difference in voltage across the two terminals of the sense resistor. This is called Kelvin sensing, and is the

most accurate way to measure voltage across a resistor. It is important to Kelvin sense the current sense resistor in a switching regulator, else significant errors can be introduced into the control loop.

2.4.9 Shutdown

If the shutdown pin is high, the part will operate in a normal fashion. If the shutdown pin is pulled low, the part will go into a minimum current mode, and the total current to the part will drop below 50uA. This functionality enables the user to conserve battery power when output voltage regulation is not needed.

SHDN	Mode
$V_{/SHDN} < 0.3V$	Shutdown
$V_{/SHDN} > 1.0V$	Normal Operation

Table 2-3: Shutdown Truth Table

2.4.10 Current Limit

Any time the current in the switch exceeds a certain level, the switch will turn off. This will happen on a cycle-by-cycle basis. The current limit will trip at no less than 200mA. This is included to protect the integrated circuit from damage during overload. Unfortunately, a boost converter is inherently vulnerable to short circuits since there is only a diode from the output to the input. During a short circuit, the diode, and possibly the input supply will suffer damage, but the integrated circuit should survive.

3 Design and Simulation

It is usually possible to take an existing schematic, make a few changes, and produce a better circuit. A circuit designer can do this without a good understanding of the circuitry

involved. Many excellent circuits designers hack[14] their circuits, getting superb results without ever getting out a calculator. A novice circuit designer would be better off cracking the books and developing a deep understanding of the circuits he is working on, and leave the hacking to the experts.

One of the best ways to understand analog circuits is to develop a linearized model of the circuit. The linearized model gives the designer a powerful tool to analyze the system. The designer can quickly iterate his design to provide the best performance possible. Researchers at the California Institute of Technology developed the first accurate linearized model of a buck, boost, and buck-boost converters [13]. Researchers at Unitrode developed a linearized model of the buck converter that is a more manageable than 'Cuk and Middlebrook's derivation [14]. The author derived a model for the boost converter in a similar fashion from the circuits described in Figure 2-1 and Figure 2-2. With this model in hand, intelligent design decisions for the loop and slope compensation were possible.

The derivation the linear model for a current mode boost converter starts with looking at the state space averaged equations for the inductor current and the output voltage:

$$\dot{I}_L = \frac{V_{in}}{L} D - \frac{V_{out} - V_{in}}{L}(1-D)$$

$$\dot{V}_{out} = \frac{I_L}{C}(1-D) - \frac{V_{out}}{CR}$$

An incremental change in the variables affects the change in inductor current:

$$\dot{\Delta} I_L = \frac{\Delta V_{in} D + \Delta D V_{in}}{L} - \left[\frac{\Delta V_{out} - \Delta V_{in}}{L}(1-D) + \frac{V_{in} - V_{out}}{L} \Delta D \right]$$

$$\Delta \dot{V}_{out} = (1-D)\frac{\Delta I_L}{C} - \frac{\Delta V_{out}}{CR} - \Delta D \frac{I_L}{C}$$

The expression for the inductor current can be simplified:

$$\dot{\Delta} I_L = [\Delta V_{in} - \Delta V_{out}(1-D) + \Delta D V_{out}]/L$$

[14] hack: designing circuits on gut instinct rather than hard and fast calculations

The control voltage for the current limit is related to the average current by the slope compensation, the sense resistor, the duty cycle, the period, the input voltage, the output voltage, and the inductor size:

$$I_L R_s = V_e - mDT - \frac{D^2 V_{in} T R_s}{2L} - \frac{(1-D)^2 (V_{out} - V_{in}) T R_s}{2L}$$

R_S = resistance of the sense resistor (Ohms)
V_e = output voltage of the error amplifier (Volts)
V_{in} = input voltage to the boost converter (Volts)
V_{out} = output voltage of the boost converter (Volts)
m = slope of the slope compensation ramp (Volts/second)
D = duty cycle of the converter (unitless)
L = inductance of the switching inductor (Henrys)
T = period of switcher (seconds)

The incremental change in inductor current with a change in the other variables is as follows:

$$\Delta I_L = \frac{\Delta V_e}{R_s} - \Delta D T \left(\frac{m}{R_s} + \frac{V_{in} D}{L} - \frac{(V_{out} - V_{in})(1-D)}{2L} \right) - \frac{T}{2L} \left[\Delta V_{in} D^2 + (\Delta V_{out} - \Delta V_{in})(1-D)^2 \right]$$

The duty cycle changes with control voltage, inductor current, and input and output voltages:

$$\Delta D = \left[\frac{\Delta V_e}{R_s} \underbrace{- \frac{T}{2L} \left[\Delta V_{in} D^2 + (\Delta V_{out} - \Delta V_{in})(1-D)^2 \right]}_{negligible} - \Delta I_L \right] \Big/ \underbrace{\left[\frac{Tm}{R_s} \right]}_{k}$$

Simplifying further:

$$\Delta \dot{I}_L = \frac{1}{L} \left[\Delta V_{in} - \Delta V_{out} (1-D) + \frac{V_{out}}{k} \left(\frac{\Delta V_e}{R_s} - \Delta I_L \right) \right]$$

$$\Delta \dot{I}_L = \frac{\Delta V_{in}}{L} - \Delta V_{out} (1-D) + \frac{\Delta V_e V_{out}}{L k R_s} - \frac{\Delta I_L V_{out}}{Lk}$$

$$\Delta \dot{V}_{out} = (1-D) \frac{\Delta I_L}{C} - \frac{\Delta V_{out}}{CR} - \frac{I_L}{Ck} \left(\frac{\Delta V_e}{R_s} - \Delta I_L \right)$$

It is possible to draw a linearized circuit model based on these equations:

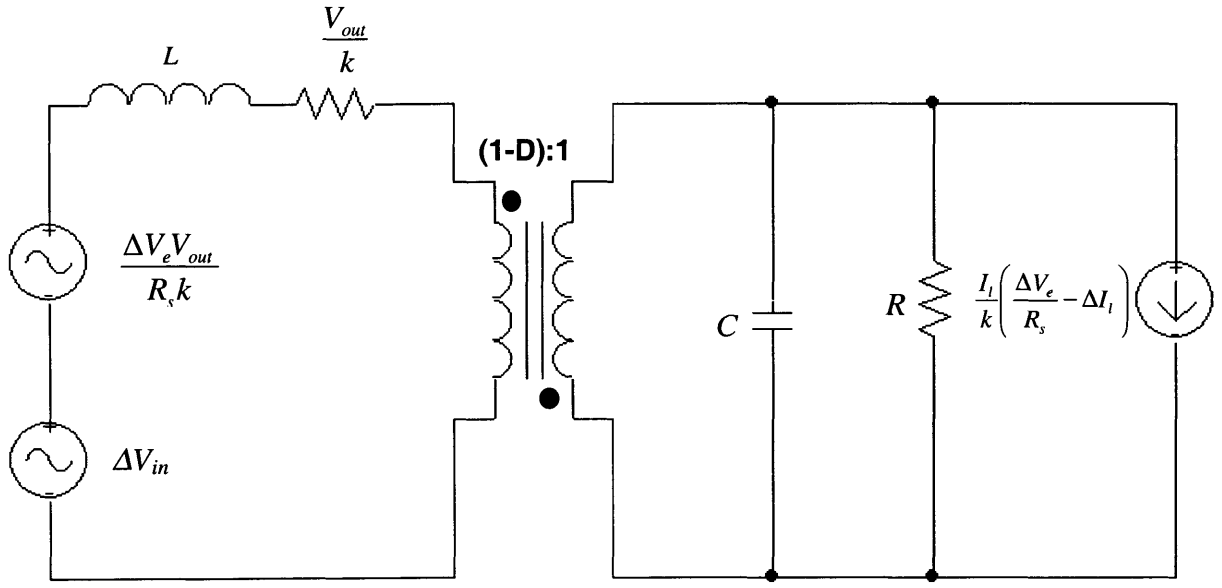

Figure 3-1: Linearized Model of Current Mode Boost Converter

The magnitude of k will largely determine the dynamics of the system. A smaller k will increase the magnitude of the damping resistance seen by the inductor and make the system look more like current source. If the inductor acts like a current source, the system will have first order dynamics.

If k is large, the system looks similar to that of a linearized circuit under duty cycle control. This makes intuitive sense, because the slope compensation is overwhelming the current sense ramp, and the circuit is operating like a voltage mode controller. The system will have a lightly damped pole pair due to the inductor and capacitor, which complicates the controller design.

Contrary to popular belief, a current mode boost controller with constant slope compensation is sensitive to changes in the input supply. It is easy to calculate the appropriate cycle-by-cycle waveform to give the boost converter ideal feed-forward characteristics.

$$I_L R_s = V_e - f(D) - \frac{(1-D)(V_{out} - V_{in})R_s}{2L}$$

The inductor current should only be dependent on the output voltage and the error voltage:

$$f(D) = \frac{(1-D)DV_{out}R_s}{2L}$$

But this curve looks like:

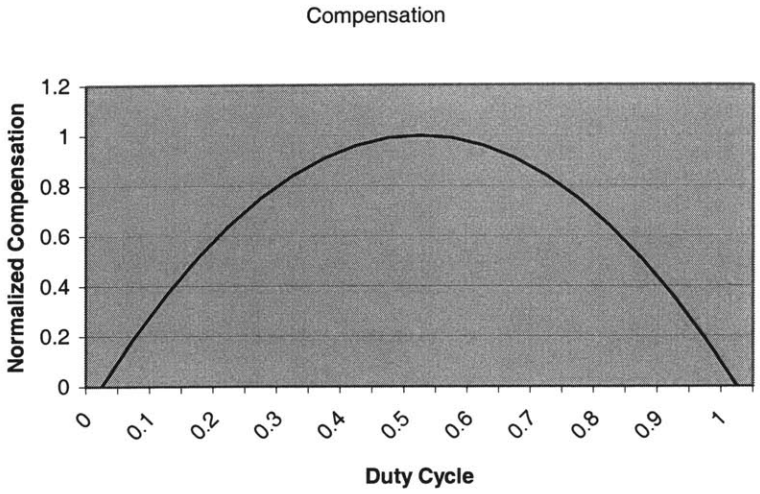

Figure 3-2: Theoretical Slope Compensation Curve

The loop will be unstable at duty cycles greater than 0.5. The inductor current will never be able to turn off at duty cycles greater than 0.5, and the system will not have the desired ideal feed-forward characteristics. Therefore, it is preferable to use simple slope compensation.

After hand analysis of the circuit was completed, the different blocks were simulated individually in SPICE and were checked over temperature and supply. Full chip simulations were not performed until all of the blocks were operating correctly, since full chip simulations take a much longer time to execute than simulations of the individual blocks. Load transients with a linearized model of the circuit were simulated before full chip simulations of load transients, which can take the better part of a day.

4 The Switch and Driver Circuitry

The most important part of the switching regulator is the switch. The switch and switch driver circuitry were carefully modeled and designed. This attention to detail allows informed tradeoffs in its design, and permits accurate optimization of efficiency and duty cycle specifications. A solid understanding of the switch and its driver circuit is fundamental to optimizing the design.

4.1 Transistor Modeling

To get the most mileage both out of hand designs and SPICE simulations, one needs to start with accurate models. The author was lucky in this instance, since most of the work was already done. Several engineers of the Linear Technology Corporation devoted months to developing models of their transistors so simulations accurately matched the measured performance of the transistors in the process. This thesis would not have been possible without their labor.

4.2 Design Choices

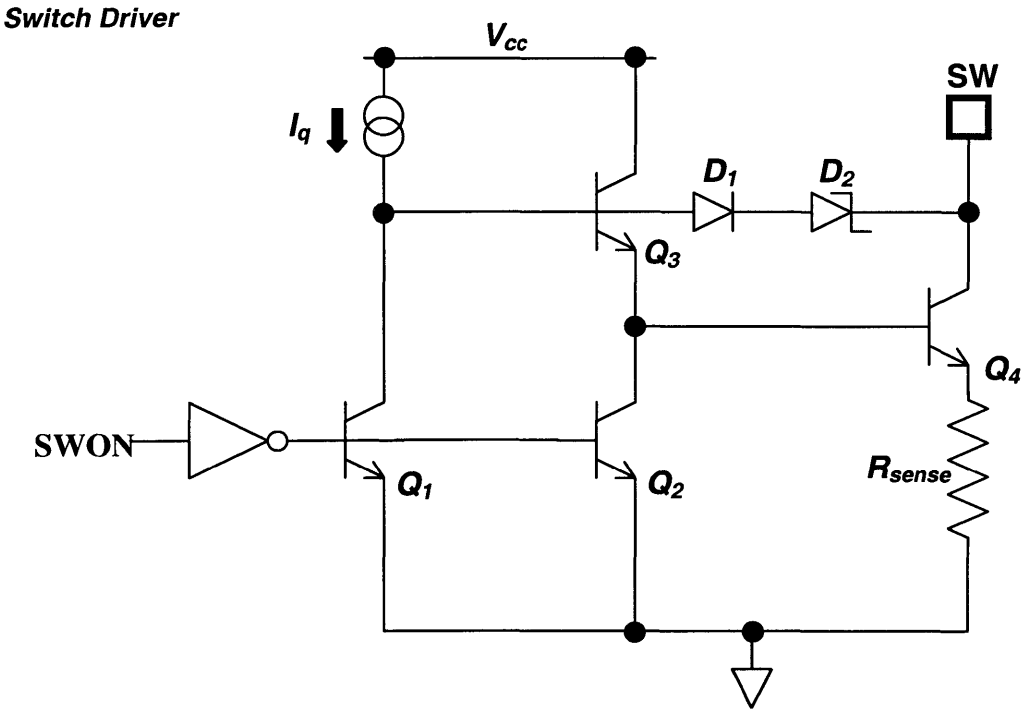

Figure 4-1: Simplified Circuit Diagram of the Switch Driver

The operation of the circuit is relatively simple. Q_4 is a large area transistor and operates as the switch. When SWON goes high, Q_3 turns on, and drives current into the base of the switch and it rapidly increases in current. Once the switch current is greater than the inductor current, the voltage on the switch decreases until the switch is saturated. The clamp diodes, D_1 and D_2, are then forward biased and steal base current from Q_3, and reduces base current in the switch until the switch comes out of saturation. When SWON goes low, Q_2 turns on and pulls charge out of the base of the switch. The switch turns off and the inductor then charges up the switch node until it is a diode drop above the output.

The topology of the switch driver circuit is decades old [15]. It is simply a Darlington configuration transistor with an active base pull-down. The drawback to the Darlington configuration is that it needs a significant supply voltage in order to run. To operate in the

forward active region, a switch in a Darlington configuration requires at least 2.1V of supply at – 55 degrees Celsius. If a switch needs to work with a lower supply voltage, it must be designed in a different configuration. Several important choices can be made in regards to the switch design. The first choice is the size of the switch. The optimal switch size will depend primarily on the output voltage and switch current of the target application. The second choice will be deciding the quiescent beta current, which will depend primarily on the maximum switch current. The third choice will be setting the saturation voltage of the switch. Some other considerations will be important in optimizing efficiency, such as the layout of the transistor, and size of the sense resistor.

4.2.1Switch Size

The size of the switch is the most important design choice in the switching regulator. A large switch will have lousy efficiency at high output voltages, but can supply more current and has better efficiency at lower output voltages. The size of the switch determines several important specifications: maximum switch current, on resistance, and output capacitance. Increasing the maximum switch current is important because it will increase the usability of the part. The switch can be used in any applications that require less than the maximum switch current, but not in applications that require more. Therefore, a bigger switch is usually better.

A larger switch will also have a lower on resistance. Lowering the on resistance generally improves the efficiency of the converter. This is not always the case, however, since at high output voltages, the dominant source of loss will be the output capacitance of the switch, and a larger switch has a larger output capacitance. A simple hand calculation gives a basic idea of what the optimal switch size for an application is.

Bipolar transistor output capacitance [16]:

$$C_{cs} = \frac{k}{\sqrt{1 + v_{cs}/\phi_{bs}}}$$

k = zero bias capacitance per unit area (Farads per meter squared)
C_{cs} = collector to substrate capacitance of the transistor per unit area (Farads per meter squared)
v_{cs} = collector to substrate voltage of a transistor (Volts)
ϕ_{bs} = built-in voltage of the collector substrate junction (Volts)

The collector resistance of a bipolar transistor is dependent on doping levels and layout. Modern bipolar transistor design usually includes a highly doped buried layer that greatly reduces the collector resistance. These doping levels are fixed by the process, so the designer can only choose the transistor size to set the output resistance. Collector and emitter resistance is directly proportional to transistor area.

Approximate power dissipation specifications for a bipolar transistor:

$$P_{diss} = A(fC_{cs}V_{out}^{\ 2}) + \frac{1}{A}(r_c + r_e) I_{sw}^{\ 2} D + V_{ce} I_{sw} D + V_{in} I_b D$$

I_{sw} = average current in the switch (Amps)
V_{out} = the output voltage of the switcher (Volts)
V_{in}= the supply voltage of the switcher (Volts)
I_b= the base current of the switch (Amps)
D = duty cycle of the switcher (unitless)
R_c = the collector resistance of a unit switching transistor (Ohms per meter squared)
R_e = the emitter resistance of a unit switching transistor (Ohms per meter squared)
V_{ce} = the voltage from the active collector to the active emitter (Volts)
A = the 'area' or number of unit transistors in the switch (meters squared)
f = the switching frequency of the converter (Hertz)

Change in power dissipation dependent on a change in area:

$$\frac{dP_{diss}}{dA} = fC_{cs}V_{out}^{\ 2} - \frac{1}{A^2} r_c I_{sw}^{\ 2} D$$

Local maximum and minimum of this equation will be where

$$\frac{dP_{diss}}{dA} = 0$$

The positive root of this equation will be the area that gives the minimum power dissipation:

$$A^2 = \frac{r_c I_{sw}{}^2 D}{f C_{cs} V_{out}{}^2}$$

$$A = \frac{I_{sw}}{V_{out}} \sqrt{\frac{(r_c + r_e)D}{f C_{cs}}}$$

Therefore, applications that require larger output voltages and less current will be more efficient with a smaller switch, whereas applications that require larger switch currents but smaller output voltages will be more efficient with a larger switch.

4.2.2 Quiescent Current

Deciding the quiescent current for the Darlington is more complicated than would appear at first glance. The quiescent current determines the maximum current the switch can sink. The relationship between the quiescent current and the maximum switch current is proportional to the square of the forward current gain of the transistors. This means the choice for quiescent current is highly dependent on beta[15]. Beta, however, is highly dependent on process and temperature. There needs to be enough quiescent current to drive the switch even when the beta is low. The decision for the minimum operating temperature of the part will largely decide the maximum quiescent current specification.

As a case example, one can examine the performance of a discreet Darlington circuit. At room temperature and fixed collector current, the beta of the popular 2n2222 transistor varies from 100 to 300 from lot to lot. Two 2n2222 transistors operating in a Darlington connection will therefore have a current gain of as low as ten thousand or as high as ninety thousand, nearly an order of magnitude of difference. Over the military temperature range, beta can vary by over a

[15] The DC forward current gain of the transistor will be referred to as beta or β for the remainder of this paper.

factor of four. This will result in over a 16:1 variation of current gain in a Darlington from 150 degrees Celsius to –55 degrees Celsius. With the worst case skew in process, the current gain of two Darlington connected transistors at high temperatures could be as much as 144 times as much as two Darlington connected transistors at low temperatures.

There are two options for designing the quiescent current source. It can be designed to be a constant current source, using a current so the switch will still work at the maximum switch current, minimum operating temperature, and worst-case beta due to process variation. The other option is to design a current source that tracks with temperature to only provide as much current as the Darlington needs. The current source can operate at much lower currents at room temperature than a static current source.

The maximum quiescent current drawn by the part is dependent on what the designer chooses as his minimum operating temperature. There are three basic temperature ranges: commercial, industrial, and military. The three temperature ranges vary from manufacturer to manufacturer, but the standard temperature ranges for the three are as follows:

Application Market	Temperature Range (in degrees Celsius)
Commercial	0 to 70
Industrial	-40 to 85
Military	-55 to 150

Table 4-1: Temperature Ranges for Various Application Markets

For example, by looking for a maximum switch current of 500mA, one can determine what the maximum quiescent current for the switch will be for each of the temperature ranges.

β (at room temperature) = 60
x = 2 (x is the exponent of the temperature coefficient of beta)
T_{nom} = 300 Kelvins (the temperature where the nominal beta was measured)
I_{swmax} = 500mA (the maximum operating current of the switch)

$$\beta = \beta_{nom}\left(\frac{T}{T_{nom}}\right)^{x}$$

$$I_{sw\max} = I_q \beta_{nom}{}^2\left(\frac{T}{T_{nom}}\right)^{2x}$$

$$I_q = \frac{I_{sw\max}}{\beta_{nom}{}^2 (T/T_{nom})^{2x}}$$

Maximum commercial quiescent Darlington current:

$$I_q = \frac{500mA}{60^2 (273/300)^4} = 202uA$$

Maximum industrial quiescent Darlington current:

$$I_q = \frac{500mA}{60^2 (233/300)^4} = 382uA$$

Maximum military quiescent Darlington current:

$$I_q = \frac{500mA}{60^2 (218/300)^4} = 500uA$$

The example shows that the maximum quiescent current is largely dependent on the designer's choice of the minimum operating temperature.

4.2.3 Forcing Beta Circuit

The design of the switch includes anti-saturation circuitry that limits the base current in the switch. The operating point of the circuitry can be chosen in order to optimize the performance and the efficiency of the switch. Richard Baker first addressed the performance problems associated with saturating bipolar transistors in a paper about digital logic [17]. He discovered that he could speed up the operation of bipolar transistor logic by keeping the transistors out of saturation. The physics behind saturation are now well understood.

When a bipolar transistor is saturated, the base-collector diode is forward biased. The forward biasing of this transistor stores charge in the PN junction. That charge must be removed before the transistor can be turned off. Saturated bipolar transistors require approximately three times longer to turn off than a bipolar transistor held outside of saturation. The transistors must stay well out of saturation in order to maximize the switching speed of the bipolar transistors.

The switch anti-saturation circuitry also decreases power dissipation of the integrated circuit. The anti-saturation circuitry limits the base current, so that at lower current levels the base current drive is only as much as necessary.[16] Otherwise, the base current drive would be the same at all output current levels. The operating point of the switch can be chosen in order to optimize efficiency.

The Ebers-Moll model of the transistor gives an idea of the relation between the saturation voltage and the effective beta:

$$I_c = I_s\left(e^{V_{be}/V_{th}} - 1\right) - \frac{I_s}{\alpha_r}\left(e^{V_{bc}/V_{th}} - 1\right)$$

Ebers-Moll Model of the Transistor when V_{be} & $V_{bc} > V_{th}$:

$$I_c = I_s e^{V_{be}/V_{th}} - \frac{I_s}{\alpha_r} e^{V_{bc}/V_{th}}$$

Simplification to find V_{ce} in terms of I_b and I_c:

$$I_c = I_s e^{V_{be}/V_{th}}\left(1 - \frac{1}{\alpha_r(\beta I_b - I_c)}\right)$$

but $I_s\exp(V_{be}/V_{th}) = \beta I_b$ so:

$$\frac{1}{\alpha_r e^{V_{ce}/V_{th}}} = 1 - \frac{I_c}{\beta I_b}$$

$$\frac{\beta I_b}{\alpha_r(\beta I_b - I_c)} = e^{V_{ce}/V_{th}}$$

[16] This is sometimes referred to as a forced beta circuit, because the transistor is forced to operate at a fixed current gain.

$$V_{ce} = V_{th} \ln\left(\frac{\beta I_b}{\alpha_r(\beta I_b - I_c)}\right)$$

It will be analytically easier to take the derivative in terms of I_b, and therefore easier to optimize I_b. Because of the earlier assumption that V_{be} & $V_{bc} > V_{th}$, this new equation is only valid if $\beta I_b < I_c$.

In order to minimize power dissipation by changing I_b, the previously calculated power dissipation equation is needed:

$$P_{diss} = A(fC_{cs}V_{out}^2) + \frac{1}{A}(r_c + r_e) I_{sw}^2 D + V_{ce} I_{sw} D + V_{in} I_b D$$

$$\frac{dP_{diss}}{dI_b} = DI_{sw}V_{th}\left[\frac{\alpha_r(\beta I_b - I_{sw})}{\beta I_b}\right]\left[\frac{\alpha_r(\beta I_b - I_{sw})\beta - \beta^2\alpha_r I_b}{(\alpha_r \beta I_b - \alpha_r I_{sw})^2}\right] + DV_{in} = 0$$

$$\beta(\beta I_b - I_{sw}) - \beta^2 I_b = -\frac{V_{in}}{I_{sw}V_{th}}[\beta I_b(\beta I_b - I_{sw})] = 0$$

$$I_b\left(\beta^2 - \beta^2 - \frac{V_{in}}{I_{sw}V_{th}}\beta I_{sw}\right) + I_b^2 \frac{V_{in}}{I_{sw}V_{th}}\beta^2 - I_{sw}\beta = 0$$

$$I_b^2 - \frac{I_{sw}}{\beta} I_b - \frac{V_{th} I_{sw}^2}{V_{in}\beta} = 0$$

The positive root gives the minimum power dissipation:

$$I_b = \frac{I_{sw}}{2\beta} + \sqrt{\frac{I_{sw}^2}{4\beta^2} + \frac{V_{th} I_{sw}^2}{V_{in}\beta}}$$

The equation indicates that he optimal I_b is approximately I_{sw}/β unless $V_{in}/V_{th} < 4\beta$. This makes intuitive sense. The only time efficiency increases by letting the switch saturate further is if the input voltage is small, because the P=IV loss will be less significant.

4.2.4 Dynamic Dissipation

Power is also dissipated in the switch during transitions. Analytically determining dynamic dissipation is tedious because it is dependent on higher order effects. Simplifying the calculations as much as possible makes the problem tractable, but still moderately accurate.

The dynamic dissipation of the switch at the full current load is a good test case. The inductor acts like a current source, whereas the switch makes transitions from full current to no

current. The voltage on the switch will make the transition from the output voltage to the switch saturation voltage when the switch current is more than the inductor current. This implies that when the switch is turning on, the voltage on the switch will remain the same until the switch current has risen almost to its maximum. When the switch turns off, however, the voltage on the switch is increasing as the current is decreasing. More power is dissipated in the switch during the transition when the switch is turning on. The dominant factor in determining the dynamic dissipation is the dissipation while the switch is turning on.

V_{out} = output voltage (Volts)
I_{smax} = maximum switch current (Amps)
f = switching frequency (Hertz)
$\frac{dI_{sw}}{dt}$ = rate of change of the switch during turn on (Amps per second)
P_{dyn} = power dissipated current turn on of the switch (Watts)

$$P_{dyn} = \frac{V_{out}}{2}\left(\frac{dI_{sw}}{dt}\right)^{-1}(I_{s\max})^2 f$$

The power dissipated while the voltage on the switch node is rising or falling is almost entirely captured by the amount of capacitance on the switch node. The capacitance on the switch node is dominated by the capacitance on the Schottky diode. Different Schottky diodes can have different capacitances, so the choice of Schottky diodes can be an important factor in efficiency. Using a larger Schottky diode than is necessary can cost several percentage points in efficiency. The easiest, and probably the best way to optimize efficiency is to swap in several manufacturers Schottky diodes on the bench, and to see which diode gives the best performance. It is also possible to estimate the dynamic losses due to the Schottky diode capacitance by examining the manufacturer's specifications.

4.2.5 Modeling of External Components

The previous discussion indicates the switch and the diode have less than ideal performance. The inductor and the capacitors also deviate from their expected performance. The inductor has a significant amount of resistance, which can be modeled as a series resistor. This resistance will lower the overall efficiency of the converter. The capacitance term in the inductor is usually small enough that it can be ignored. The output capacitor is ceramic, and has a nearly negligible amount of resistance and inductance. The series inductance in the capacitor is unfortunately still large enough to affect the performance of the circuit. The slew rates of the current through the capacitor are enough to excite the series inductance to a measurable voltage.

L_{Cesl} = equivalent series inductance of the output capacitor (Henrys)
$\frac{dI_{sw}}{dt}$ = rate of change of current during switch transitions (Amps per second)
V_{ptp} = peak to peak voltage of the output noise (Volts)

$$V_{ptp} = 2L_{Cesl}\frac{dI_{sw}}{dt}$$

For example, an equivalent series inductance of 1nH and a switch current slew rate of 150mA/ns will lead to 350mV of peak to peak output noise.

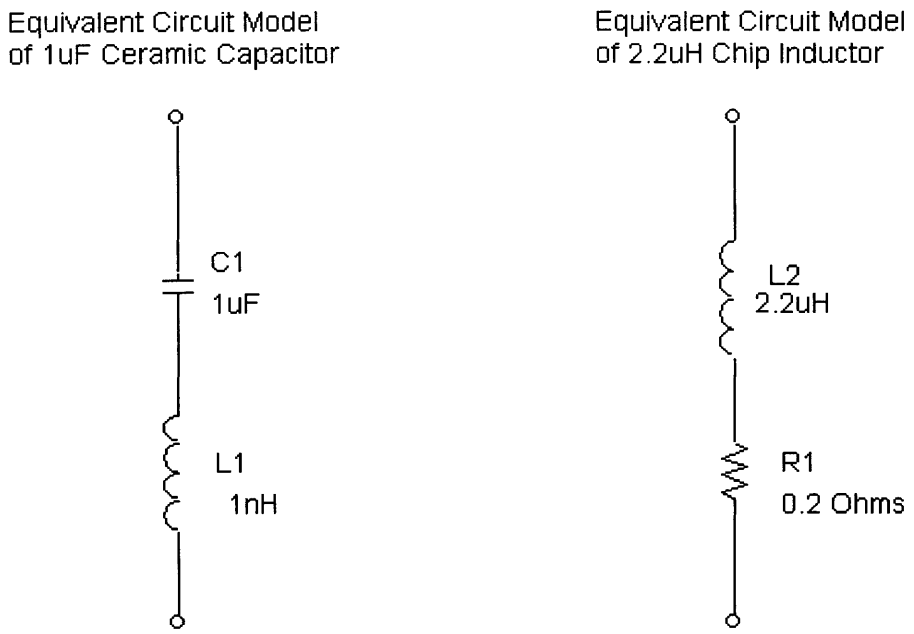

Figure 4-2: Equivalent Circuit Models of Energy Storage Elements

5 Testing

Careful testing of the integrated circuit on the bench serves several purposes. The designer can gain a better familiarity with the operation of the circuit in a shorter time than with SPICE because many things are easier to test.[17] The manufactured circuit may deviate in performance from simulations, and those performance deviations provide a great opportunity to learn more about the integrated circuit. A careful evaluation on the bench helps avoid customer complaints and field failures.

[17] A load step simulation in SPICE can take up to a day to simulate on a 700 MHz Pentium III, whereas a load step test on the bench can be set up and recorded within a couple minutes.

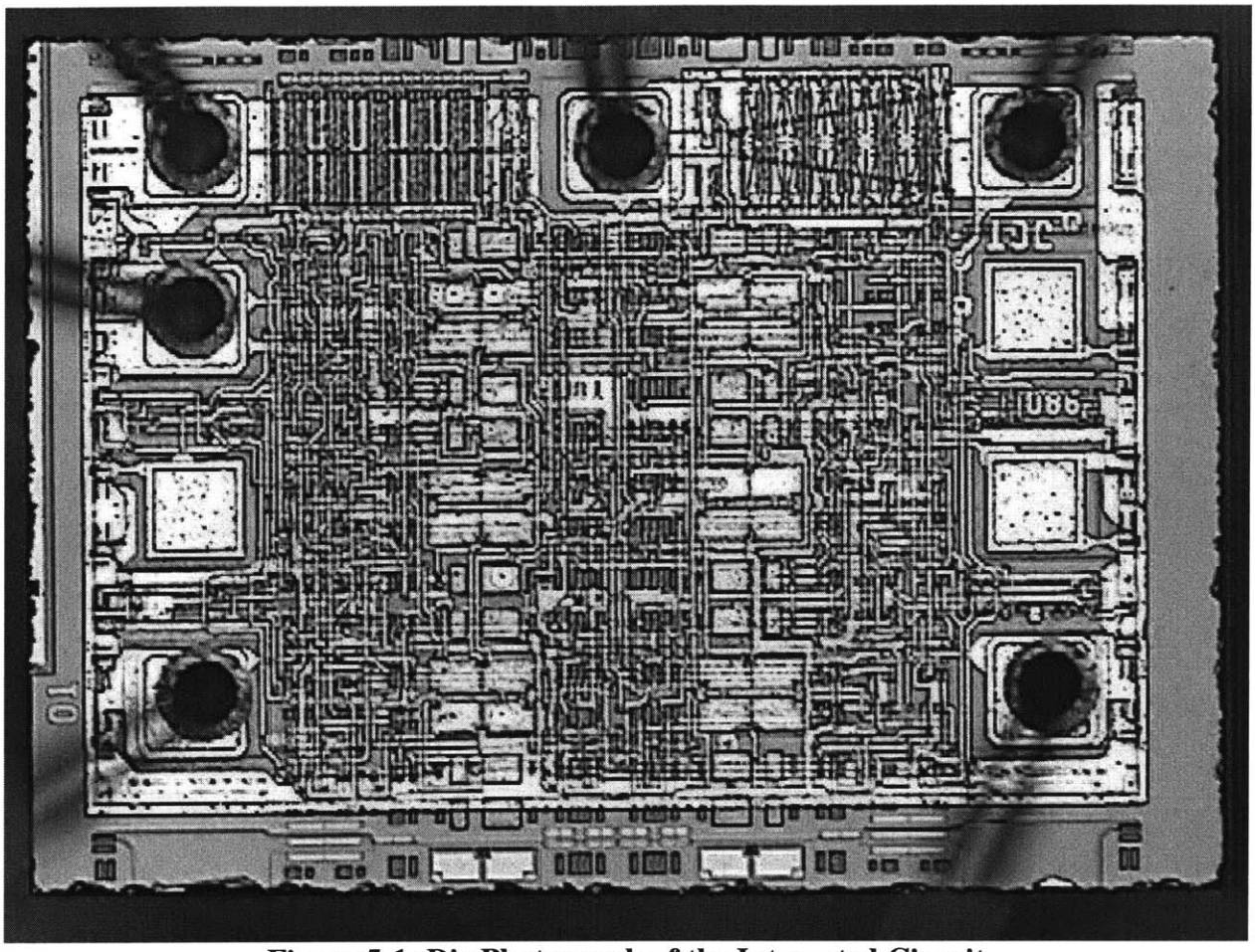

Figure 5-1: Die Photograph of the Integrated Circuit

5.1 Measurement Techniques for High Frequency DC/DC converters

As the frequency of operation of DC/DC converters increases, so will the sophistication of the measurement techniques required to characterize them. Several measurements of the converter required care and consideration. They are documented here.

5.1.1 Switch Current

The slew rate of the switch current significantly affects the performance of the circuit. Many people neglect to investigate this on the bench because it is not a simple measurement to take. This is not an excuse, however, especially because the measurement is usually

straightforward. This project, however, required care in selecting instruments, and in board construction. The predicted current rise times were better than three nanoseconds. The author was only able to find one current probe that was capable of making such measurements. Using standard current probes would lead the engineer to think that his current rise times were far slower than they actually were. A simple calculation demonstrates the required probe bandwidth required to preserve the fidelity of a rise time measurement. Most 'scopes and probes are designed to have a Gaussian high frequency cutoff, but this can be approximated with a first order low pass filter.

$$H(s) = \frac{1}{\tau s + 1}$$

Using the Laplace transform, the step response in the time domain can be determined:

$$f(t) = u_{-1}(t)\left(1 - e^{-t/\tau}\right)$$

The 10% to 90% risetime of the filter can be determined using this equation.

$$f(t_{90\%}) = 0.9 = 1 - e^{-t_{90\%}/\tau}$$

$$t_{90\%} = \tau \ln 10$$

$$f(t_{10\%}) = 0.1 = 1 - e^{-t_{10\%}/\tau}$$

$$t_{10\%} = \tau \ln\left(\frac{10}{9}\right)$$

$$t_{10\%to90\%} = t_{90\%} - t_{10\%} = \tau \ln 9$$

The risetime is therefore inversely related to the bandwidth or f_{-3dB} of the current probe:

$$f_{3dB} = \frac{1}{2\pi\tau} = \frac{\ln 9}{2\pi t_{10\%to90\%}}$$

$$t_{10\%to90\%} = \frac{\ln 9}{2\pi f_{3dB}} \approx \frac{0.35}{f_{3dB}}$$

In order to preserve the fidelity of a signal with a 2ns risetime, a current probe with at least 175MHz of bandwidth is required. The standard bench AC current probe from Tektronix, the P6022, has a high frequency bandwidth of 120MHz. Using this current probe leads to erroneous results. The Tektronix CT-1 has a bandwidth of 1GHz, however, and does the trick.

Board construction is also critical for this measurement. The inductance must be minimized in the switch current loop, so a custom board was built out of copper clad for this circuit. The current probe (not pictured) is placed through a hole drilled out of the center of the board, minimizing the loop through which the switch current must travel. Even this small loop adds enough inductance to corrupt the switch current waveform. A piece of copper tape (not pictured) was carefully threaded through the hole in the current probe and soldered to two ends of the board to bridge the contacts.

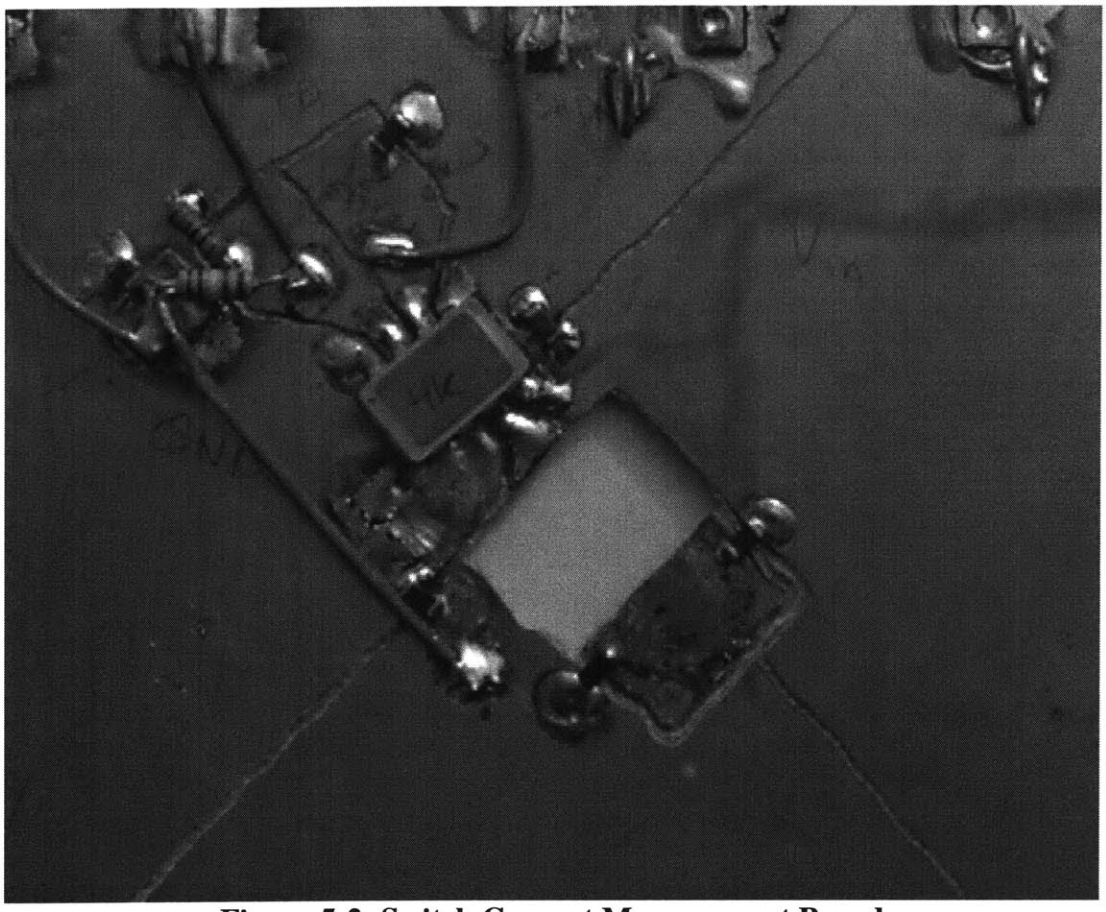

Figure 5-2: Switch Current Measurement Board

The rise and fall times should be faster than the 3ns that was measured, since the extra inductance added by the copper tape retarded the current slew rate. This measurement was taken when the part was forced into current limit. Switching regulators in equilibrium have a certain amount of phase jitter. The part is out of equilibrium when it is in current limit, and the phase jitter disappears. This gives a better look at the current edges and the rise and fall times.

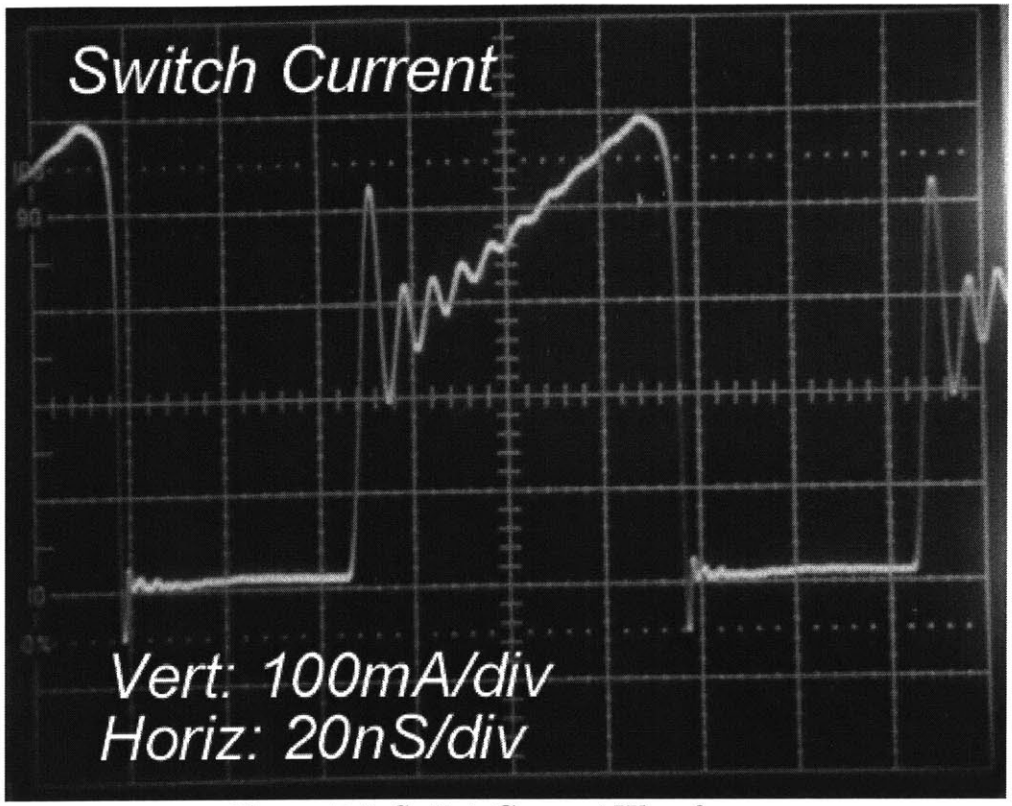

Figure 5-3: Switch Current Waveform

The switch current rings because of the added inductance from the current sensing loop. The switch current rise and fall times are fast enough that it is difficult to measure them merely by looking at the full cycle waveform. Zooming in on the rising and falling edge of the waveform shows better resolution.

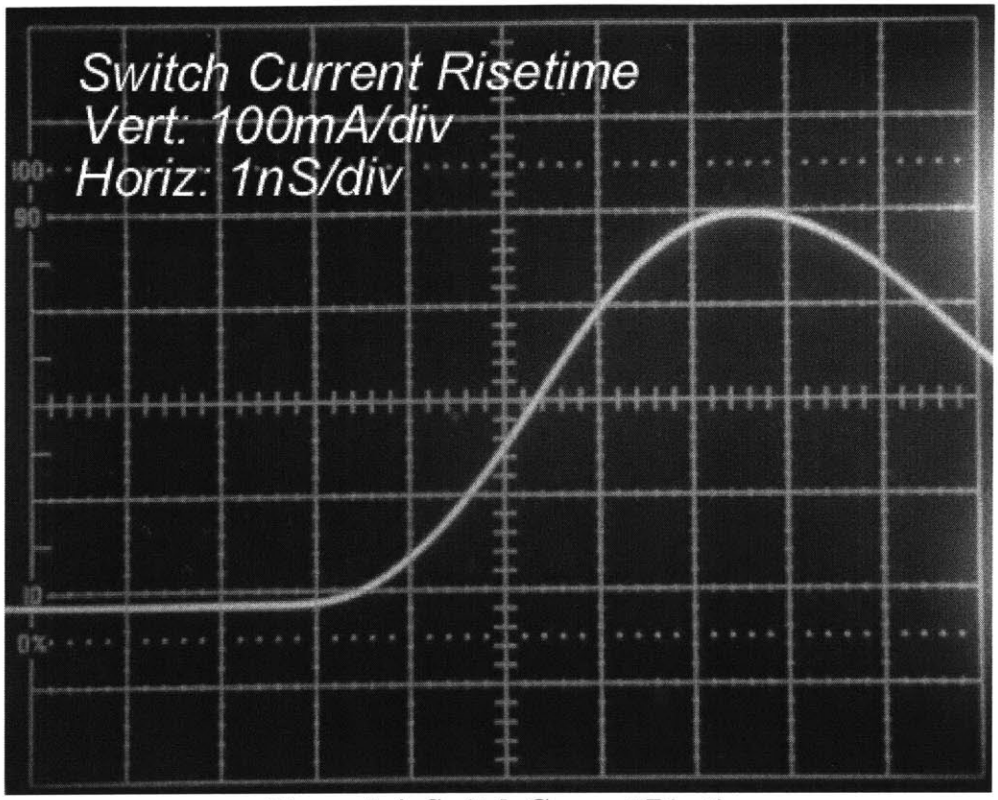

Figure 5-4: Switch Current Risetime

The switch current 10% to 90% risetime is better than 3ns, even with the added inductance from the current sensing loop.

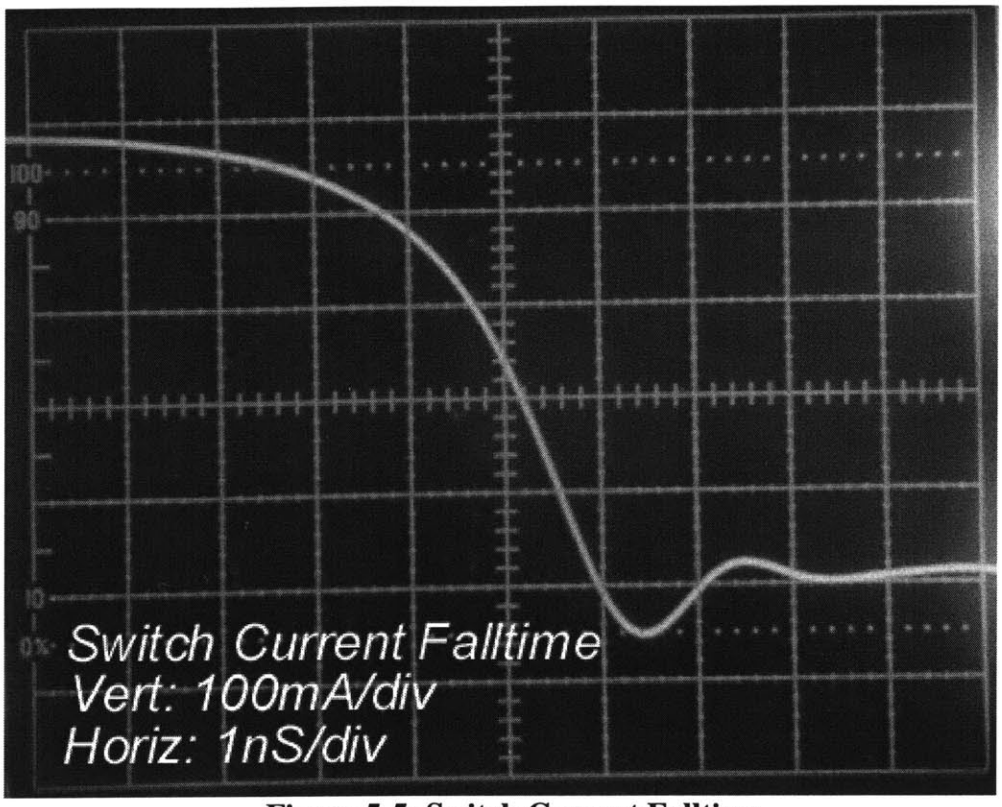

Figure 5-5: Switch Current Falltime

The switch current 90% to 10% falltime is also better than three nanoseconds. Knowing the rise and fall times of the switch current permits calculation of the dynamic dissipation.

5.1.2 Output Noise[18]

Getting an accurate look at the output noise of the converter takes a great deal of care. The high current and voltage slew rates of the converter generates radiated fields. These fields can corrupt test equipment without proper shielding. The signal also has very fast edges, so the measurement equipment must be able to detect very high frequency signals. The measuring device also must be properly terminated; otherwise, the signal will be corrupted due to transmission line effects.

[18] The author refers to unwanted output signals as noise. The classic meaning of noise implies a signal lacking coherence, and is due to the natural properties of resistors and PN junctions, for example.

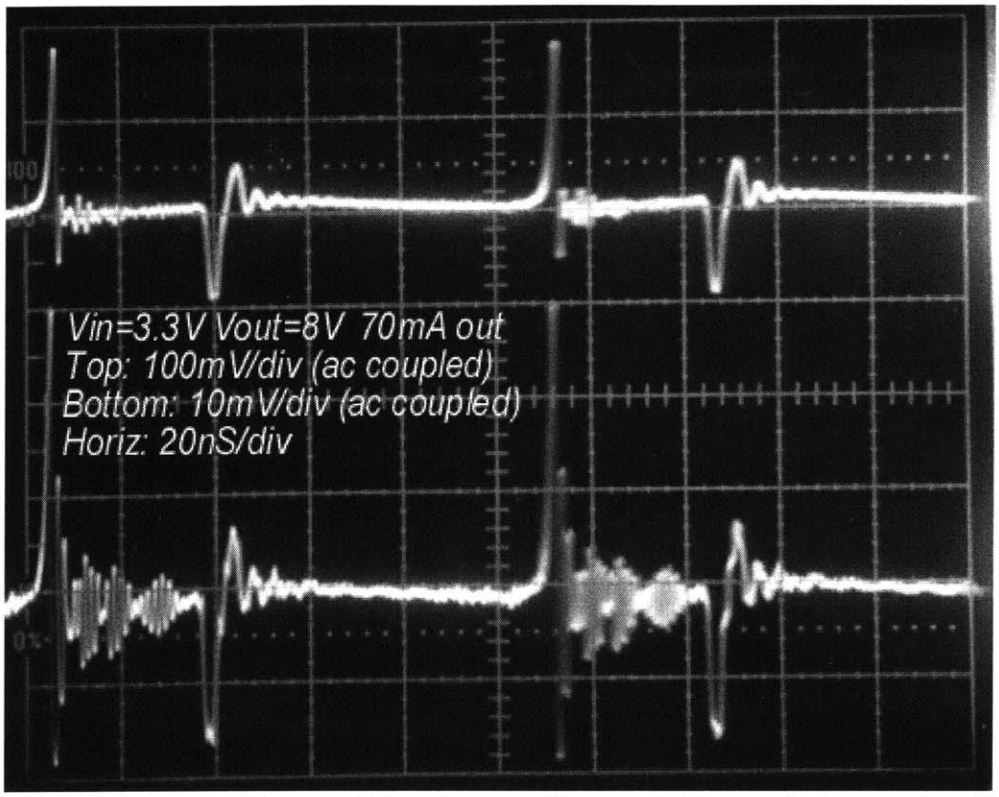

Figure 5-6: Top Trace – Output Noise, Bottom Trace – Filtered Output Noise. Note the change in scale. The scale for the top trace is 10x the scale of the bottom trace

The upper trace is a picture of the unfiltered output noise. The output noise is large, nearly 300mV peak to peak. This could prevent the converter from being usable in some applications. Slowing the current and voltage slew rates will decrease the output noise, but it will also decrease the efficiency because of the increased dynamic dissipation. There is an indirect relation between the efficiency of the converter and the output noise.

The output noise could also scare off potential customers, even though it should not be a problem in their application circuits. Since most of the output noise is due to high frequency content, it is an easy task to eliminate the noise. A small length of trace will have enough inductance that when connected to a capacitor it will form a second order filter. Since the boost converter is usually driving a microprocessor, there is often a second capacitor.[19] The lower

[19] Most microprocessor manufacturers specify a required number of capacitors that must be closely coupled to the power pins.

'scope trace in the above picture of output noise is filtered by a small amount of board trace, and is greatly reduced in magnitude. Therefore, this high level of output noise should not pose any problems to the microprocessor.

The possibility that output noise violates any FCC regulations, or if output noise would cause any problems with a microprocessor warrants further investigation.

5.2 Performance in the Application Circuits

5.2.1 Efficiency

After the circuit was manufactured, a board was built and the performance was evaluated. The results were pleasing, because they were extremely close to simulations. Unfortunately, what was expected was not so spectacular. In particular, due to time constraints it was not possible to make the switch as large as was needed. The on resistance of the switch was rather large, on the order of two ohms, and led to efficiency that was underwhelming.

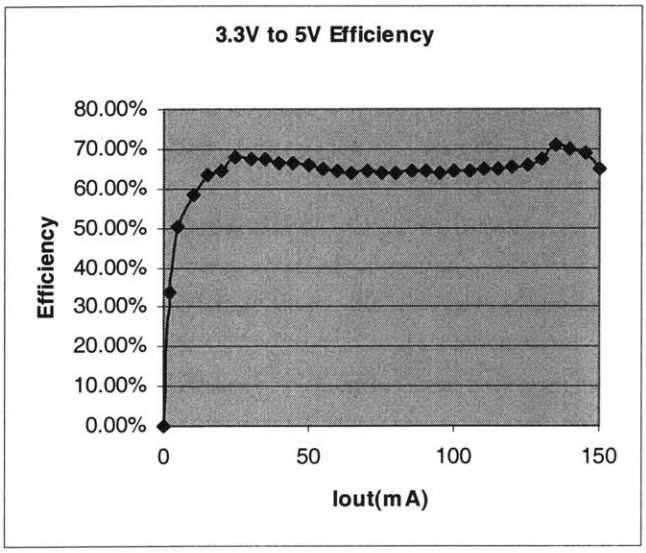

Figure 5-7: 3.3V to 5V Efficiency Curve

The efficiency is worse for lower output current because of the high quiescent current of the converter. For larger output currents, the losses are dominated by dissipation in the switch.

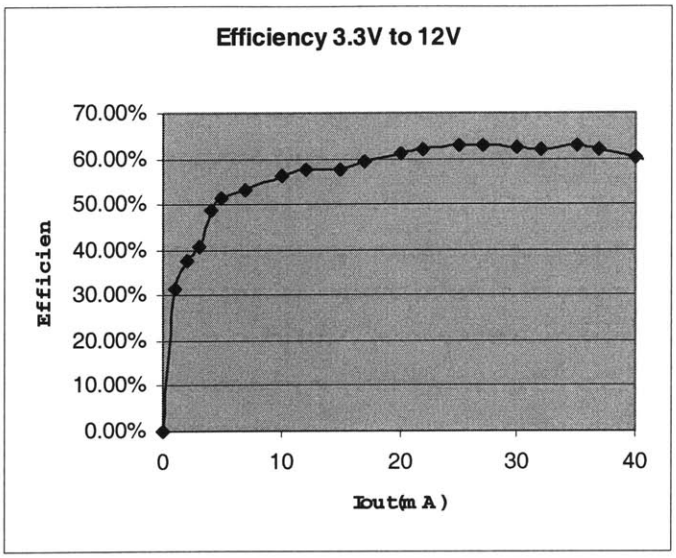

Figure 5-8: 3.3V to 12V Efficiency Curve

The efficiency is lower for the higher output voltage because the duty cycle of the converter is larger. Current is passing through the switch for a greater percentage of switching cycle, and more energy is lost in the on resistance of the switch. The converter delivers less output current because the switch current is proportionally higher for higher duty cycles. The converter is only rated for a certain amount of switch current. Once the switch current exceeds the current limit, the output falls out of regulation.

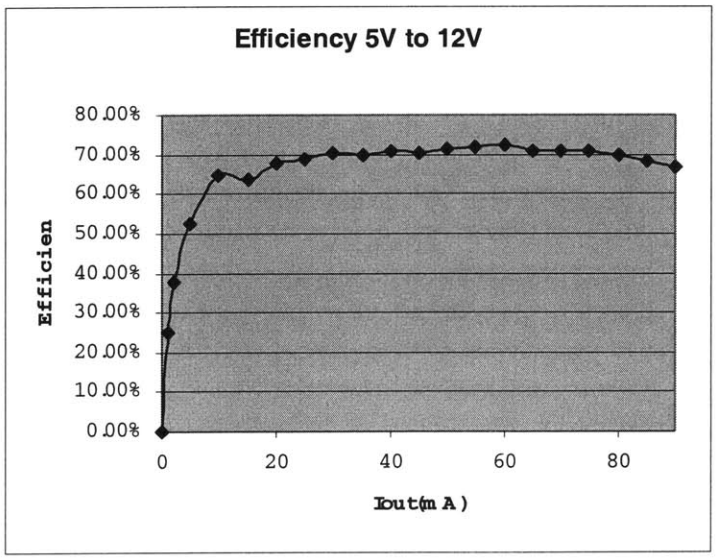

Figure 5-9: 5V to 12V Efficiency Curve

The efficiency and maximum output current is better for the 5V to 12V and 3.3V to 8V conversions because the converter is operating at a lower duty cycle.

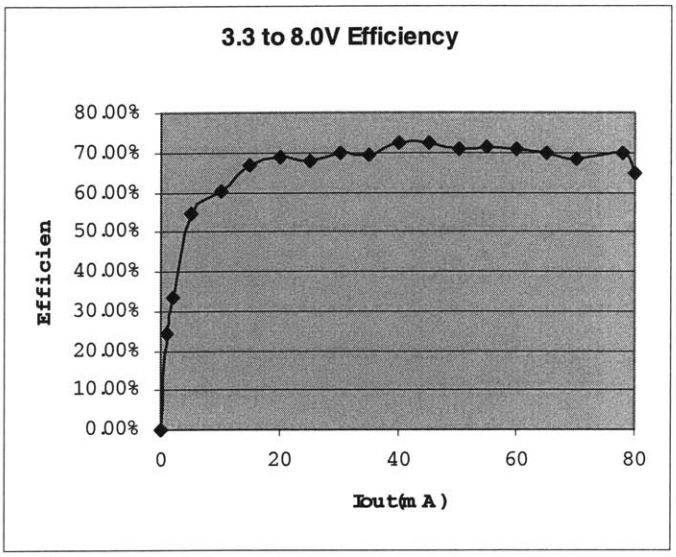

Figure 5-10: 3.3V to 8.0V Efficiency Curve

An another common application for a monolithic boost converter is the SEPIC configuration. This allows output voltages above and below the input voltage. A SEPIC converter also provides short circuit protection, since there is no direct connection from the input to the output.

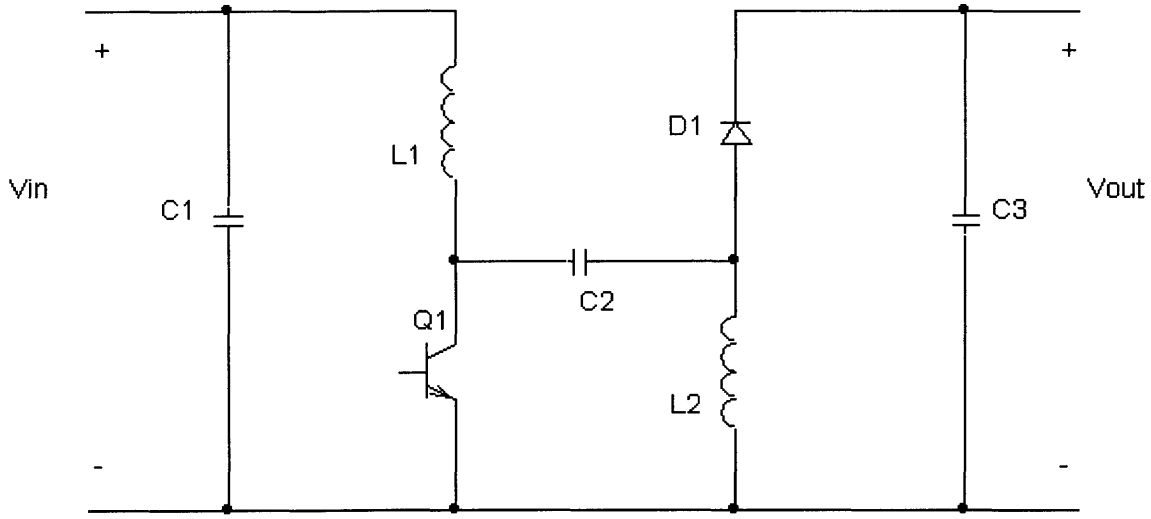

Figure 5-11: Circuit Diagram of a SEPIC Converter

A typical application for the SEPIC converter is for use with a lithium-ion battery. The rated voltage for a lithium-ion battery can vary from as low as 2.5V to as high as 4.2V. If the desired output voltage is 3.3V, then the converter must be able to step up or step down the output voltage. The SEPIC converter is one of the few converter types that can do this.

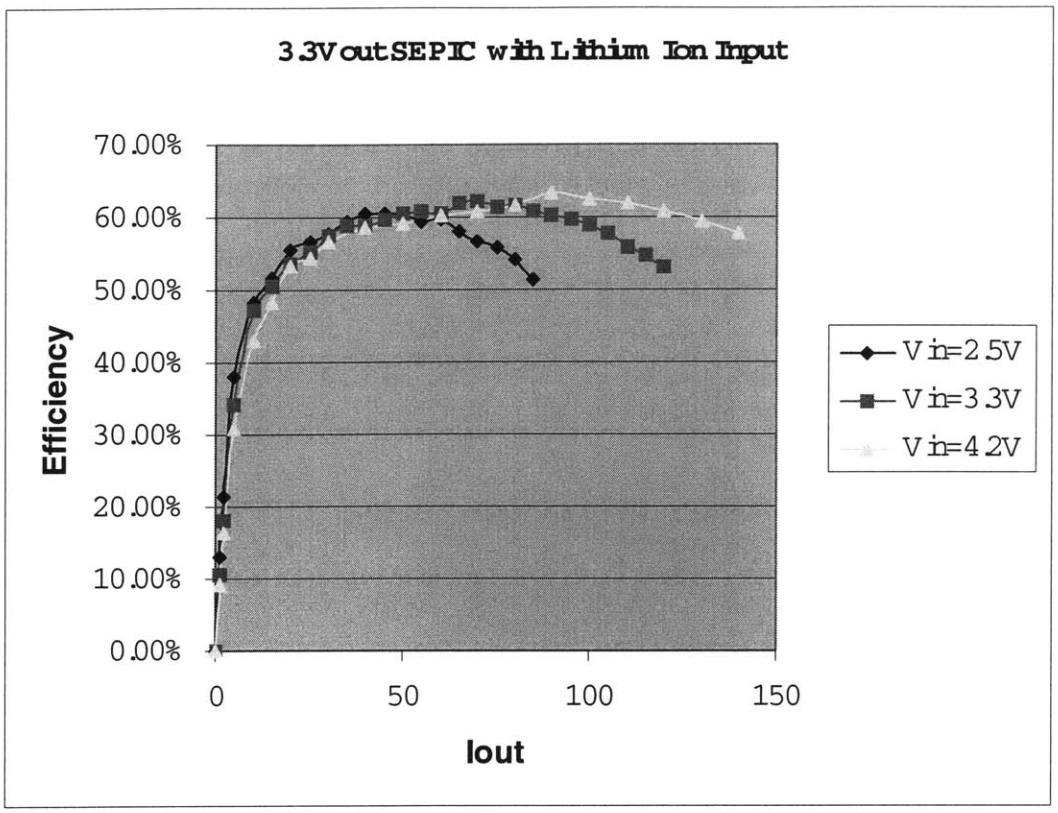

Figure 5-12: Efficiency Curves for 3.3V output SEPIC converter

Unfortunately, the efficiency for a SEPIC converter is significantly lower than for its direct converter counterparts, since there is more resistance in the current path, and more energy is being dissipated in the greater amount of parasitic capacitance.

5.2.2 Load Transient

A critical test for the circuit is a load step. The circuit must be able to regulate the output voltage during a load transient. Figure 5-13 shows the change in output voltage when the load steps from a small load to a maximum load. The circuit regulates the output voltage and recovers quickly.

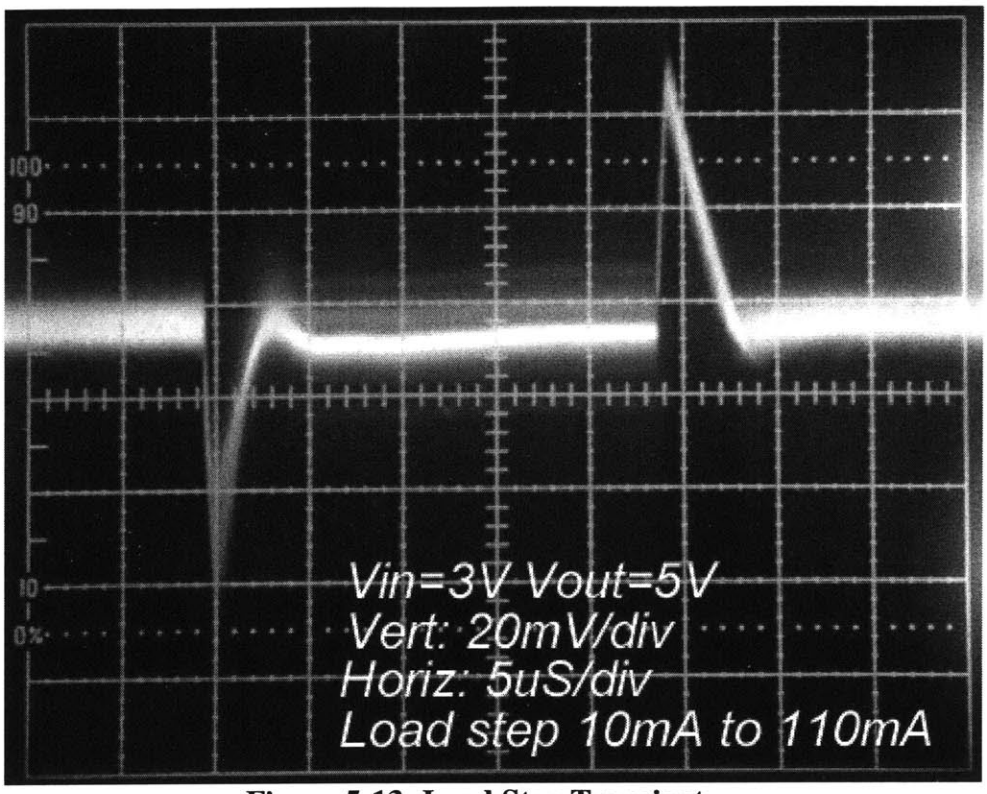

Figure 5-13: Load Step Transient

The step response illustrates the loop dynamics of the system. There is about a 20% overshoot. For a second order system a 20% overshot indicates fifty-five degrees of phase margin [14].

The change in the output voltage dependent on load is due to the change open loop gain of the circuit. The load resistance determines the open loop gain of the circuit, and a change in load resistance, such as a load step, will result in a small change in the output voltage. Since the open loop gain is large, the output voltage remains well within the specified bounds.

Testing the load transient provides ample opportunity to make a grievous testing error. The author initially tested the load transient on a circuit using a ceramic input capacitor. The resulting ringing on the input fed through to the output, and gives a waveform that appears as a poorly compensated loop. Replacing the ceramic input capacitor with tantalum capacitor increases the damping at the input. The load step transient then behaves as shown in Figure 5-13.

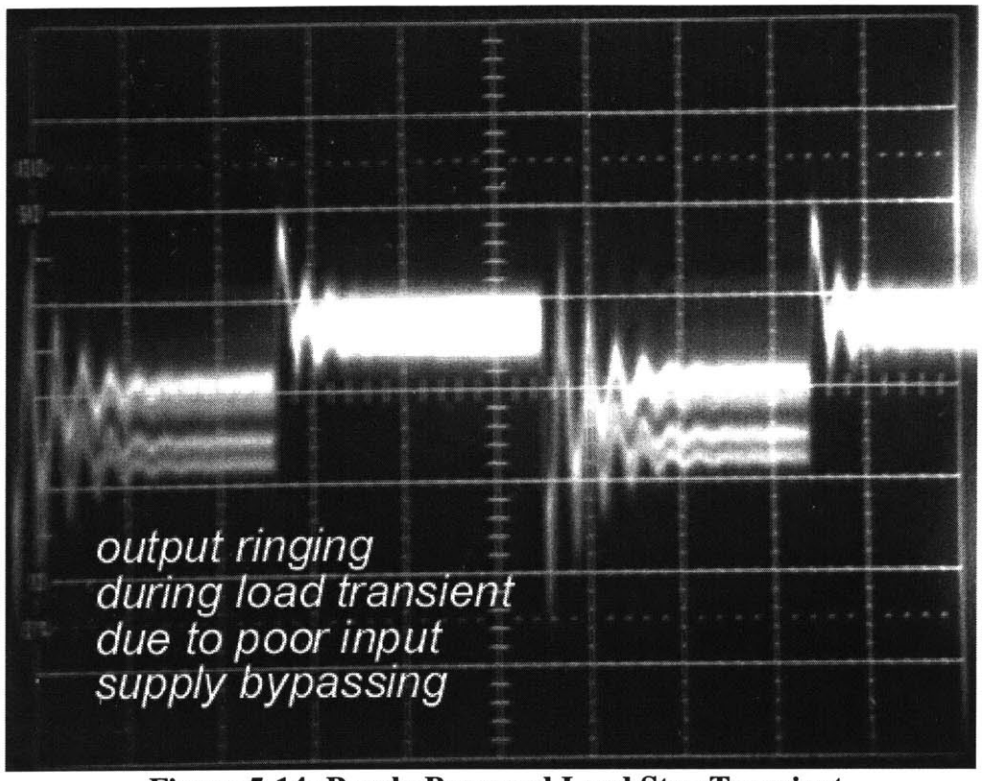

Figure 5-14: Poorly Bypassed Load Step Transient

5.3 Specifications

Most of the specifications were tested over the operating temperature ranges, and over the input voltage ranges. There were no surprises. The circuit performed similarly to SPICE simulations.

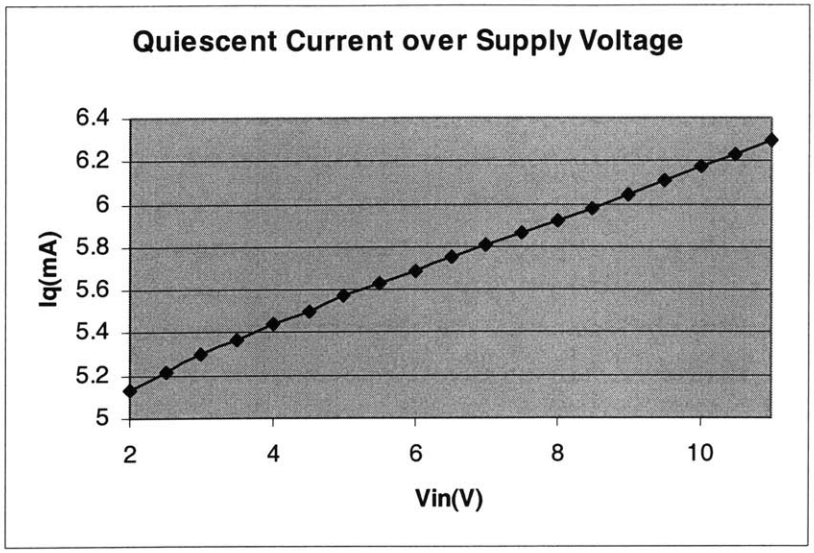

Figure 5-15: Quiescent Current over Supply Voltage

The quiescent current of the circuit increases with supply voltage. Although this is undesirable, not worrying about the supply dependence of the quiescent current allows simple circuit design.

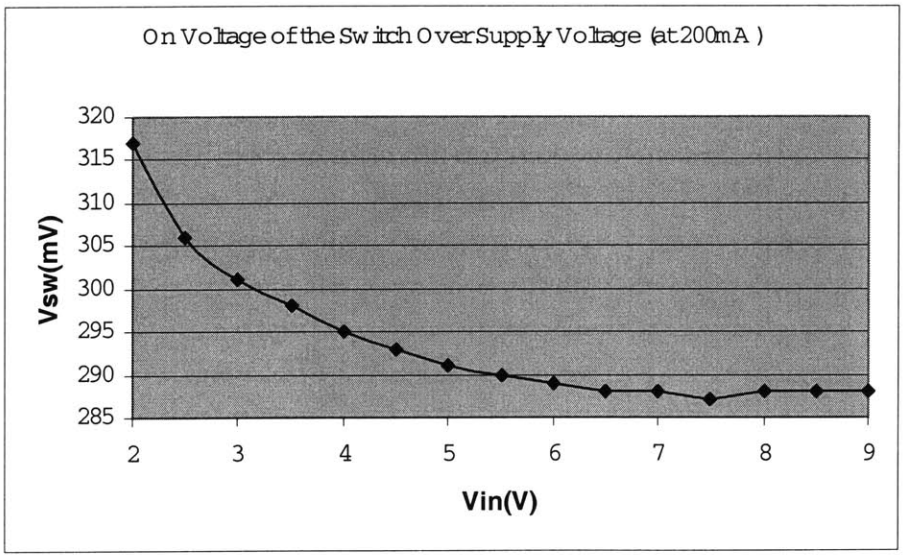

Figure 5-16: On Voltage of the Switch over Supply Voltage

The change of the on voltage of the switch over supply voltage is due to the design of the switch driver circuitry and improves the efficiency of the converter at higher input voltages.

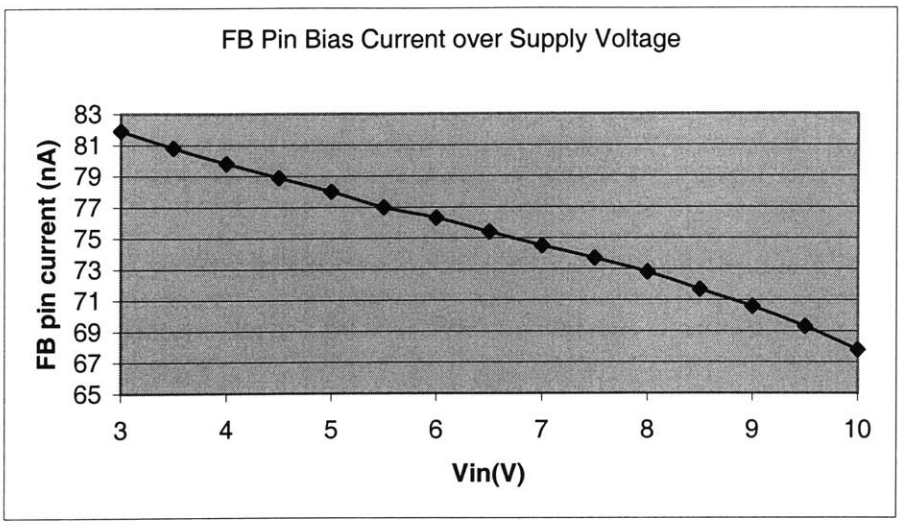

Figure 5-17: FB Pin Bias Current over Supply Voltage

The reason the FB pin bias current decreases with supply voltage is relatively complicated. It is due to supply dependence of several of the circuits in the feedback network. The change is quite small and should not affect the performance of the circuit in an application.

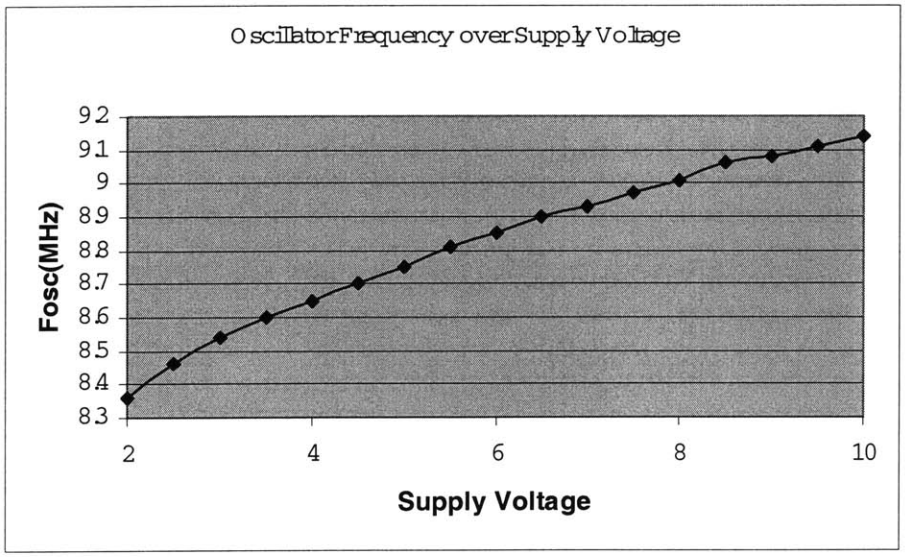

Figure 5-18: Oscillator Frequency over Supply Voltage

The bias current for the oscillator increases with voltage and increases the frequency of the oscillator. The change is relatively minor and should not affect the performance of the circuit in an application.

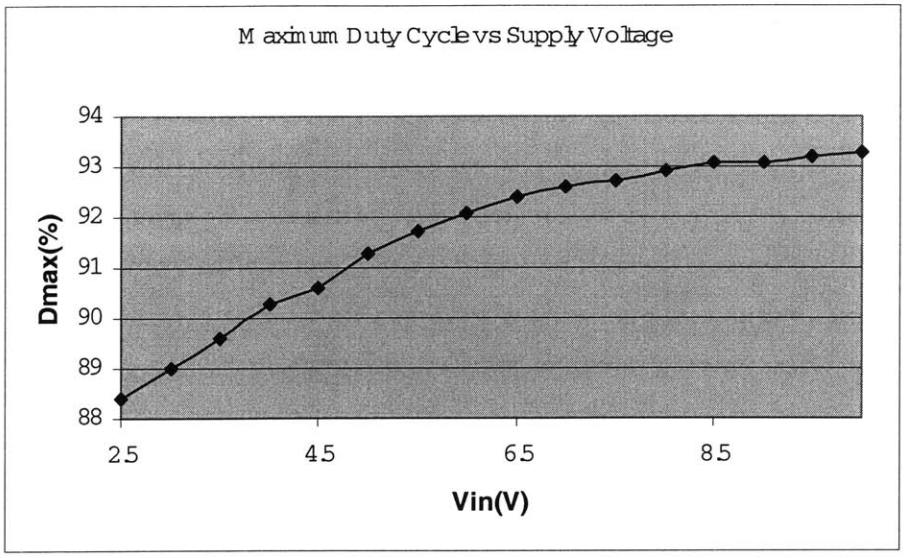

Figure 5-19: Maximum Duty Cycle over Supply Voltage

The greater quiescent current at higher voltages improves the speed of operation of the comparator and increases the maximum duty cycle. This is the exact opposite of what is desired, but ends up not mattering. The maximum voltage allowed on the switch is quite low, and the maximum duty cycle should not be a problem at any input voltage.

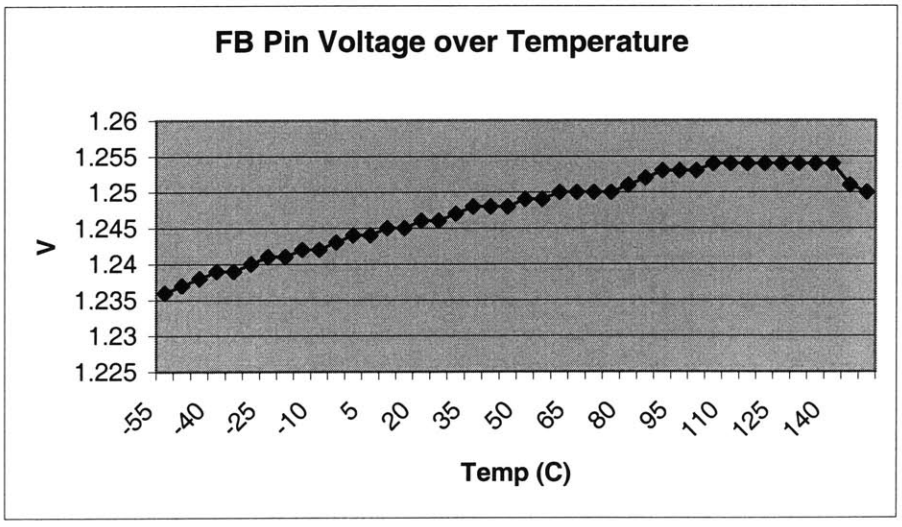

Figure 5-20: FB Pin Voltage over Temperature

The voltage at the FB pin remains relatively stable over temperature. The voltage could have a little more CTAT component to it. It remains within +/- 1% of nominal over the full temperature range.

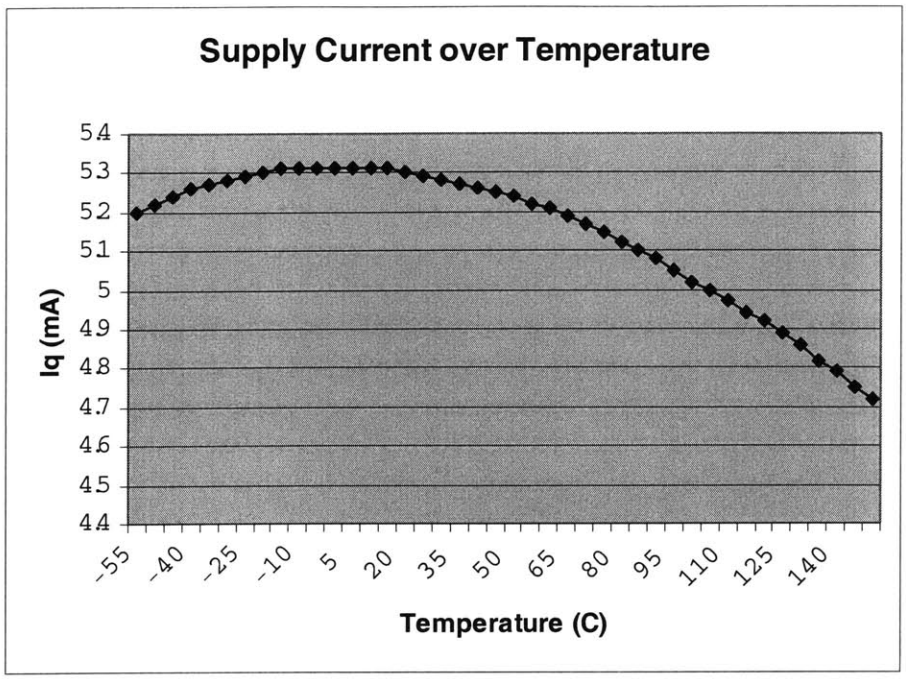

Figure 5-21: Supply Current over Temperature

The quiescent current decreases at higher temperatures due to design. Since the beta of the driver transistors increase with temperature, they require less quiescent current. The current falls off at lower temperatures due to higher order effects of the devices in the integrated circuit.

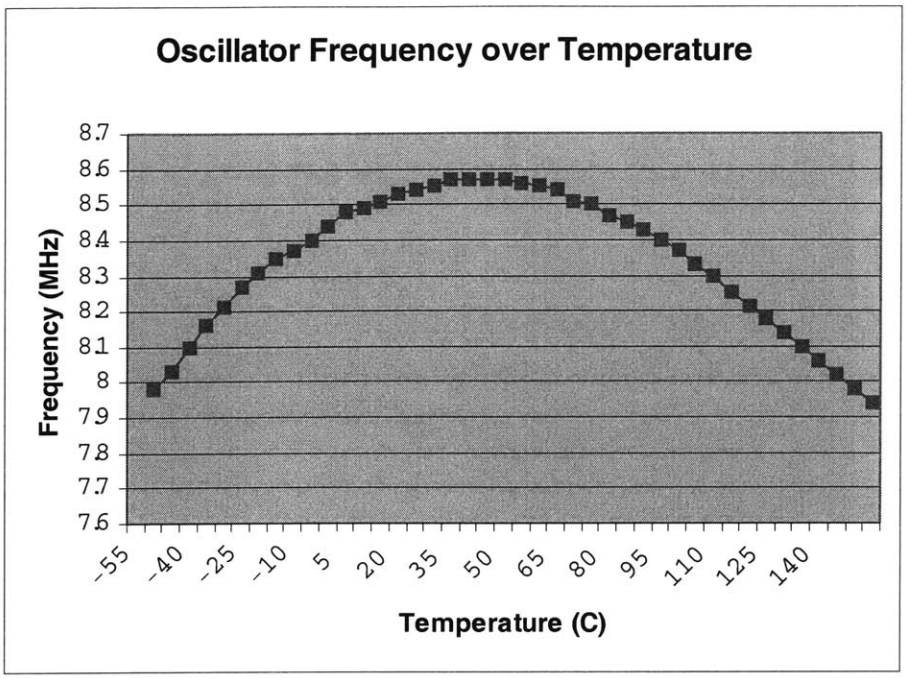

Figure 5-22: Oscillator Frequency over Temperature

The frequency of the oscillator remains relatively stable over temperature. The temperature stays within +/- 4% of the nominal frequency.

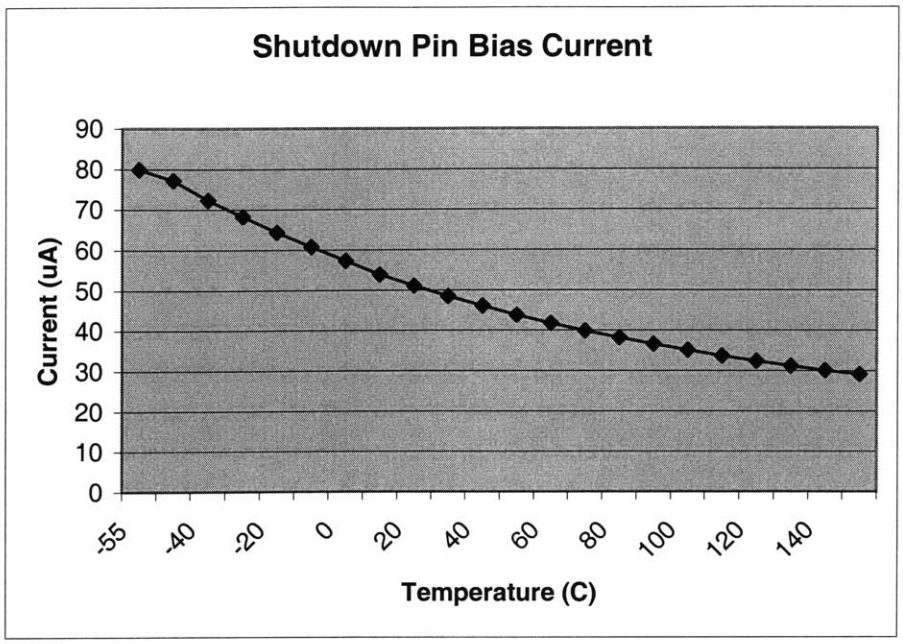

Figure 5-23: Shutdown Pin Bias Current over Temperature

The bias current for the shutdown pin decreases with temperature because the input impedance seen at that terminal is PTAT.

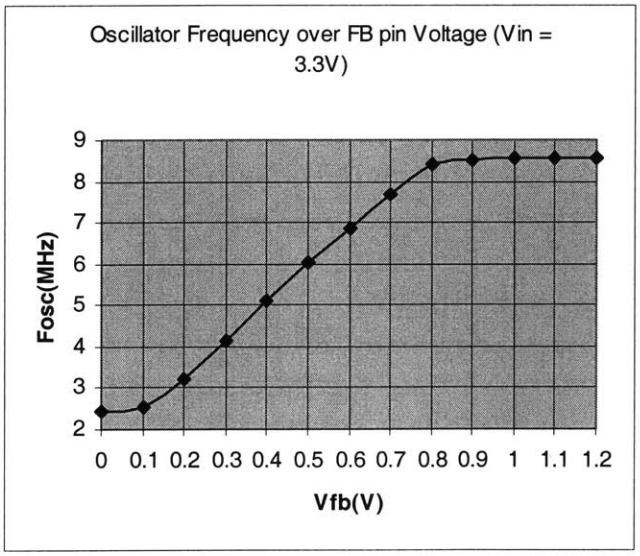

Figure 5-24: Oscillator Frequency over FB Pin Voltage

If the FB pin is at low voltage this indicates that the output is at a low voltage and the circuit is either starting up or it is in short circuit. In either case, the current in the inductor can be quite high. Decreasing the switching frequency decreases the power dissipation in the switch,

and protects the circuit from thermal breakdown. Once the output voltage comes up, the inductor current should be at a reasonable level, and the oscillator operates at its nominal frequency.

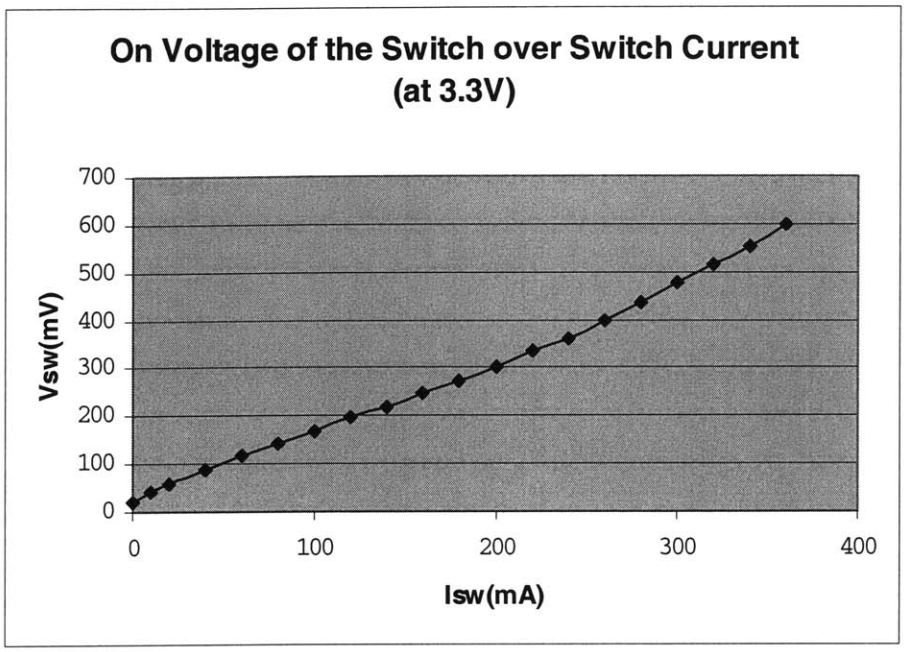

Figure 5-25: On Voltage of the Switch over Switch Current

The switch has a relatively constant on resistance. Therefore, the on voltage of the switch should increase with increasing current. The on resistance is high and dominates the efficiency loss of the part. A larger switch would have a lower on resistance, and would have been a better choice.

5.4 Speed Limits

There is a fundamental limit to the speed at which a boost converter can operate efficiently and with low noise. The current rise times must be very fast to maintain reasonable efficiency at high switching frequencies. Fast current rise times lead to large peak to peak output noise. Speeding up the rise times any further, which would be necessary for even higher switching frequencies, would lead to volts of noise on the output. Lowering the parasitic inductance of the output capacitor would also decrease the noise on the output. The parasitic

inductance of the output capacitor is proportional to its cross sectional area, however. Using a larger size capacitor would decrease the noise on the output, but is contrary to the original purpose of lowering the size and cost of the total circuit.

The controller circuitry will also reach a physical limitation at higher frequencies. Decreasing the feature width of a process improves the speed and the number of the transistors. It decreases, however, the breakdown voltage of the process. There is a fundamental limit to the speed of the process if the breakdown voltage must stay the same. Most microprocessors require low output voltages, so the process could stand to move to a lower feature width. With a one-micron complementary bipolar process, a designer could design a boost regulator with reasonable specifications that operates at more than 20 MHz. The benefit of such a fast switcher is not readily apparent. The total solution would be only slightly smaller, and the output noise would be higher. The efficiency would be worse.

6 Conclusion

This thesis has shown that it is possible to further reduce the amount of board space the power converter in a handheld device occupies by increasing the switching frequency. The reduction, however, is not dramatic. Some of the more difficult measurements and design choices that are involved with a high frequency switching regulator have been elucidated. It was also demonstrated that there are minimal benefits to increasing switching frequencies further. The controller circuitry could be designed to operate at higher frequencies with available processing technology. Reduction in the parasitic inductance due in the output capacitor is more difficult, because the inductance increases with decreasing cross sectional capacitor area.

These two relations are captured qualitatively in Figure 6-1. The required board area increases rapidly with decreasing frequency because the energy storage elements must be

significantly larger. Improving the processing technology allows the converter to operate at higher frequencies by both improving the efficiency, and increasing the maximum possible switching frequency. Processing technology improvements only decrease board area indirectly, by allowing for a higher switching frequency. At higher frequencies, the incremental decrease in board area diminishes, since the size of the energy storage components becomes comparable to the controller circuit, diode, and resistors. The output noise increases with increasing frequency because the current slew rates must increase in order to maintain reasonable efficiency. Decreasing the parasitic inductance of the capacitor reduces the output noise. Pushing the switching frequency past f_{crit} makes little sense, because the decrease in board area is minimal, whereas the increase in output noise is significant.

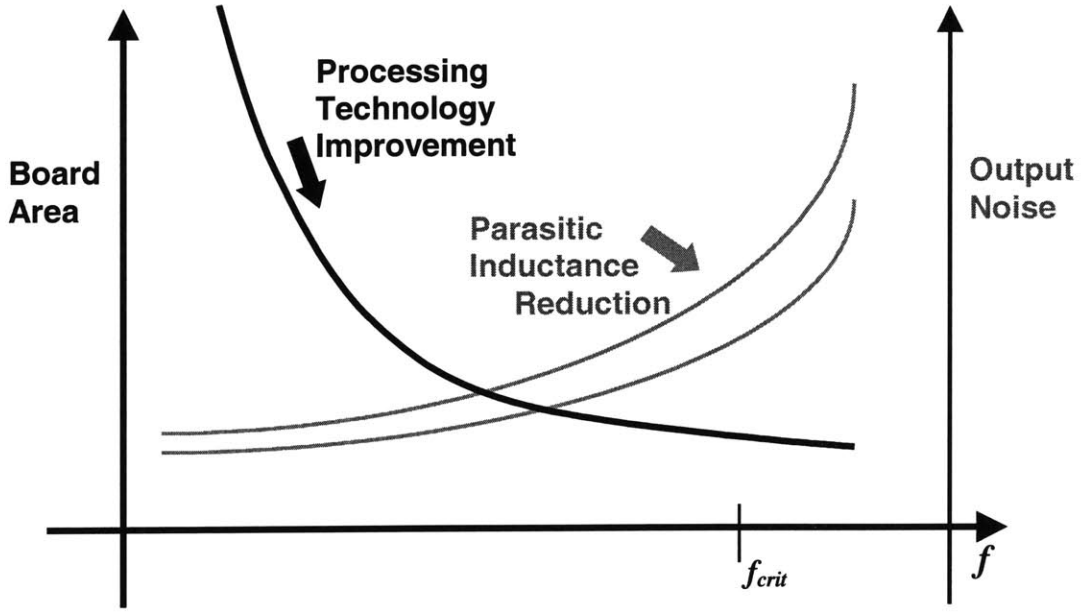

Figure 6-1: Qualitative Change in Board Area with Change in Switching Frequency. The black curve corresponds to board area. Gray curves correspond to output noise.

6.1 Contributions

A good deal amount of technical knowledge was gained as to what is required to significantly increase the speed of a switching regulator beyond the current generation of parts. Some definitive conclusions were made as to what the maximum speed a switching regulator should operate at. Measurement techniques, which would be useful for any engineers working with a high frequency switcher, were documented. The true goal will be achieved when the next generation of switchers that operate at higher frequencies are commercially available, and consumers can buy even smaller handheld devices at lower prices.

6.2 Future Work

The future work is clearly to build higher frequency switchers and is likely being pursued in several design centers. The highest performance monolithic switching regulator will operate at around 5 MHz. These circuits will combine reasonable efficiencies with lower total solution-size and cost. Everyone who purchases handheld devices utilizing these microchips will benefit since their devices will have more functionality at a lower cost.

There has been research in the realm of pushing the limits of switching speed in other topologies of switching regulators. There are fundamental problems with increasing the switching frequency further without increasing switching noise or increasing the board area. Capacitors inherently contain parasitic inductance. An incremental decrease in the parasitic inductance is possible, but a significant reduction is not. The researchers will likely run into the same noise problems.

6.3 Acknowledgements

Clearly, I was not able to design and manufacture an integrated circuit without significant help from the staff of Linear Technology Corporation. So many people provided valuable assistance that I fear if I list names, I will leave someone important out. It was great fun to design an integrated circuit and to see it manufactured and working in the lab. Thanks guys!

Many thanks to my advisors Charles Sodini and Duane Boning for being an unending source of good advice.

My friends and family have always been wonderfully helpful throughout my life. Special thanks to my parents for their unflinching encouragement, even in the face of adversity. Commendations to my roommate, John, who provided me transportation to and from Linear Tech, and heaps of entertainment. My friends Susie, Stacy, Katy, Danny, Brennan, Chrissie, Michelle, Alison, Anthony, Wesley, Dan, Paul, and Dave, who visited me in Mountain View while I was working on this project also deserve special thanks. Jason, I wish you were still here with us; I miss you buddy.

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Appendix A – Efficiency Data

The following is the data for the efficiency plots:

Efficiency Data
3.3V to 5.0V

Vin(V)	*Iin(mA)*	*Vout(V)*	*Iout(mA)*	*Efficiency*

3.3	6.2	5	0	0.00%
3.3	9	5	2	33.67%
3.3	15	5	5	50.51%
3.3	25.9	4.99	10	58.38%
3.3	35.8	4.99	15	63.36%
3.3	46.8	4.99	20	64.62%
3.3	55.5	4.99	25	68.11%
3.29	67.3	4.99	30	67.61%
3.29	79	4.99	35	67.20%
3.29	91.3	4.99	40	66.45%
3.29	102.6	4.99	45	66.52%
3.29	115	4.99	50	65.94%
3.29	129	4.99	55	64.67%
3.29	141	4.99	60	64.54%
3.28	154	4.98	65	64.08%
3.28	165	4.98	70	64.41%
3.28	178	4.98	75	63.97%
3.28	189	4.97	80	64.14%
3.28	200	4.97	85	64.40%
3.28	211	4.97	90	64.63%
3.28	225	4.96	95	63.85%
3.28	234	4.96	100	64.62%
3.28	246	4.96	105	64.54%
3.27	257	4.95	110	64.79%
3.27	268	4.95	115	64.96%
3.27	278	4.95	120	65.34%
3.27	286	4.95	125	66.16%
3.27	291	4.95	130	67.63%
3.27	290	4.98	135	70.90%
3.27	303	4.95	140	69.94%
3.27	320	4.97	145	68.87%
3.26	350	4.95	150	65.07%

Efficiency Data 3.3V to 12V

Vin(V)	*Iin(mA)*	*Vout(V)*	*Iout(mA)*	*Efficiency*
3.3	7	12	0	0.00%
3.3	11.5	12	1	31.62%
3.3	19.4	12	2	37.49%
3.3	26.9	12	3	40.55%
3.3	29.9	12	4	48.65%
3.3	35.4	12	5	51.36%
3.3	47.7	12	7	53.36%

3.3	64.5	12	10	56.38%
3.3	76	12	12	57.42%
3.29	94.8	12	15	57.71%
3.29	104.2	12	17	59.51%
3.29	119	12	20	61.30%
3.29	129	12	22	62.20%
3.29	145	12	25	62.89%
3.28	157	12	27	62.92%
3.28	176	12	30	62.36%
3.28	189	12	32	61.94%
3.28	204	12	35	62.77%
3.28	219	12	37	61.81%
3.28	243	12	40	60.22%
3.27	263	12	42	58.60%
3.27	286	11.94	45	
3.27	317	11.36	50	

Efficiency Data 5V to 12V

Vin(V)	*Iin(mA)*	*Vout(V)*	*Iout(mA)*	*Efficiency*
5	6.8	12.02	0	0.00%
5	9.7	12.02	1	24.78%
5	12.8	12.02	2	37.56%
5	22.8	12.02	5	52.72%
5	37	12.01	10	64.92%
5	56.5	12	15	63.72%
5	71	12	20	67.61%
4.99	87.3	12	25	68.87%
4.99	102.5	12	30	70.38%
4.99	121	12	35	69.56%
4.99	136	11.99	40	70.67%
4.99	154	11.99	45	70.21%
4.99	169	12	50	71.15%
4.98	185	12	55	71.64%
4.98	200	11.99	60	72.23%
4.98	220	11.98	65	71.08%
4.98	237	11.97	70	70.99%
4.98	255	11.97	75	70.69%
4.97	276	11.96	80	69.75%
4.97	299	11.95	85	68.35%
4.97	325	11.95	90	66.58%
4.97	300	10.14	95	

Efficiency Data 3.3V to

8.0V

Vin(V)	*Iin(mA)*	*Vout(V)*	*Iout(mA)*	*Efficiency*
3.3	6.4	8	0	0.00%
3.3	10	7.99	1	24.21%
3.3	14.4	7.99	2	33.63%
3.3	22.1	7.99	5	54.78%
3.3	40.2	7.98	10	60.15%
3.3	54.1	7.98	15	67.05%
3.29	70.3	7.98	20	69.01%
3.29	89.5	7.98	25	67.75%
3.29	104.3	7.98	30	69.77%
3.29	122.5	7.98	35	69.30%
3.29	134	7.98	40	72.40%
3.29	151	7.98	45	72.28%
3.28	171	7.97	50	71.05%
3.28	187	7.97	55	71.47%
3.28	205	7.97	60	71.12%
3.28	226	7.96	65	69.80%
3.27	249	7.96	70	68.43%
3.27	271	7.96	78	70.06%
3.27	300	7.95	80	64.83%
3.26	338	7.93	85	
3.26	351	7.66	90	

SEPIC Efficiency 3.3V to 3.3V

Vin(V)	*Iin(mA)*	*Vout(V)*	*Iout(mA)*	*Efficiency*
3.3	7.7	3.3	0	0.00%
3.3	9.4	3.3	1	10.64%
3.3	11	3.3	2	18.18%
3.3	14.6	3.3	5	34.25%
3.3	21.2	3.3	10	47.17%
3.3	29.6	3.29	15	50.52%
3.3	37.1	3.29	20	53.74%
3.3	45.2	3.29	25	55.14%
3.3	52	3.29	30	57.52%
3.29	59.4	3.29	35	58.92%
3.29	67.8	3.29	40	59.00%
3.29	75.3	3.29	45	59.76%
3.29	82.4	3.29	50	60.68%
3.29	90.6	3.29	55	60.71%
3.29	99	3.29	60	60.61%
3.29	104.7	3.29	65	62.08%
3.29	112.6	3.29	70	62.17%
3.29	122	3.29	75	61.48%

3.29	130	3.29	80	61.54%
3.28	140	3.29	85	60.90%
3.28	150	3.29	90	60.18%
3.28	159	3.28	95	59.75%
3.28	170	3.28	100	58.82%
3.28	181	3.27	105	57.83%
3.28	196	3.27	110	55.95%
3.28	210	3.27	115	54.59%
3.27	225	3.26	120	53.17%
3.27	231	3.1	125	
3.27	230	2.95	130	

SEPIC Efficiency 4.2V to 3.3V

Vin(V)	*Iin(mA)*	*Vout(V)*	*Iout(mA)*	*Efficiency*
4.2	7.5	3.3	0	0.00%
4.2	8.5	3.3	1	9.24%
4.2	9.6	3.3	2	16.37%
4.2	12.7	3.3	5	30.93%
4.2	18.3	3.3	10	42.94%
4.19	24.3	3.29	15	48.47%
4.19	29.5	3.29	20	53.23%
4.19	36.1	3.29	25	54.38%
4.19	41.5	3.29	30	56.76%
4.19	53.5	3.29	40	58.71%
4.19	66.4	3.29	50	59.13%
4.19	78.1	3.29	60	60.32%
4.19	90.5	3.29	70	60.73%
4.19	102	3.29	80	61.58%
4.18	112	3.29	90	63.25%
4.18	126	3.29	100	62.47%
4.18	140	3.29	110	61.84%
4.18	155	3.28	120	60.75%
4.18	172	3.28	130	59.31%
4.17	190	3.27	140	57.78%
4.17	196	2.86	150	

Sepic Efficiency 2.5V to 3.3V

Vin(V)	*Iin(V)*	*Vout(V)*	*Iout(mA)*	*Efficiency*
2.5	8.3	3.3	0	0.00%
2.5	10.2	3.3	1	12.94%
2.5	12.3	3.3	2	21.46%

2.5	17.4	3.3	5	37.93%
2.5	27.2	3.29	10	48.38%
2.5	38.1	3.28	15	51.65%
2.5	47.2	3.28	20	55.59%
2.5	58	3.28	25	56.55%
2.5	68	3.28	30	57.88%
2.5	77.6	3.29	35	59.36%
2.49	87.1	3.29	40	60.68%
2.49	98.2	3.29	45	60.55%
2.49	109.22	3.29	50	60.49%
2.49	122	3.29	55	59.57%
2.49	132.9	3.29	60	59.65%
2.49	147.8	3.28	65	57.93%
2.48	163.2	3.28	70	56.73%
2.48	178	3.28	75	55.73%
2.48	195	3.27	80	54.09%
2.48	218	3.26	85	51.25%
2.47	210	2.69	90	

Appendix B – Specifications Data

The following is the data for the specifications plots:

Quiescent Current over Supply Voltage

Vin	*Iq(mA)*
0.5	0
1	0.2
1.5	3.66
2	5.13
2.5	5.22
3	5.3
3.5	5.37
4	5.44
4.5	5.5
5	5.57
5.5	5.63
6	5.69
6.5	5.75
7	5.81
7.5	5.86
8	5.92
8.5	5.98
9	6.04

9.5	6.11
10	6.17
10.5	6.23
11	6.3

On Voltage of the Switch Over Supply Voltage (at 200mA)

Vin(V)	*Vsw(mV)*	*Rsw*
2	317	1.585
2.5	306	1.53
3	301	1.505
3.5	298	1.49
4	295	1.475
4.5	293	1.465
5	291	1.455
5.5	290	1.45
6	289	1.445
6.5	288	1.44
7	288	1.44
7.5	287	1.435
8	288	1.44
8.5	288	1.44
9	288	1.44

On Voltage of the Switch over Switch Current (at 3.3V)

Isw(mA)	*Vsw(mV)*	*Rsw(ohms)*
0	22	
10	40	4
20	59	2.95
40	89	2.225
60	117	1.95
80	144	1.8
100	169	1.69
120	195	1.625
140	220	1.571429
160	247	1.54375
180	274	1.522222
200	303	1.515
220	337	1.531818
240	360	1.5
260	398	1.530769
280	434	1.55
300	476	1.586667

320	515	1.609375
340	553	1.626471
360	598	1.661111

The DC current limit point is at 360mA

FB Pin Bias Current over Supply Voltage

Vin(V)	*FB pin current (nA)*
3	81.9
3.5	80.8
4	79.8
4.5	78.9
5	78
5.5	77
6	76.3
6.5	75.4
7	74.5
7.5	73.7
8	72.8
8.5	71.7
9	70.6
9.5	69.3
10	67.8

Oscillator Frequency over Supply Voltage

Vin(V)	*Fosc(MHz)*
2	8.36
2.5	8.46
3	8.54
3.5	8.6
4	8.65
4.5	8.7
5	8.75
5.5	8.81
6	8.85
6.5	8.9
7	8.93
7.5	8.97
8	9.01

8.5	9.06
9	9.08
9.5	9.11
10	9.14

Oscillator Frequency over FB pin Voltage (Vin = 3.3V)

Vfb(V)	*Fosc(MHz)*
0	2.46
0.1	2.54
0.2	3.2
0.3	4.16
0.4	5.1
0.5	6.02
0.6	6.88
0.7	7.7
0.8	8.4
0.9	8.53
1	8.55
1.1	8.56
1.2	8.57

Maximum Duty Cycle vs. Supply Voltage

Vin(V)	*Dmax(%)*
2.5	88.4
3	89
3.5	89.6
4	90.3
4.5	90.6
5	91.3
5.5	91.7
6	92.1
6.5	92.4
7	92.6
7.5	92.7
8	92.9
8.5	93.1
9	93.1
9.5	93.2
10	93.3

FB Voltage over temperature

°C	Volts
-55	1.236
-50	1.237
-45	1.238
-40	1.239
-35	1.239
-30	1.24
-25	1.241
-20	1.241
-15	1.242
-10	1.242
-5	1.243
0	1.244
5	1.244
10	1.245
15	1.245
20	1.246
25	1.246
30	1.247
35	1.248
40	1.248
45	1.248
50	1.249
55	1.249
60	1.25
65	1.25
70	1.25
75	1.25
80	1.251
85	1.252
90	1.253
95	1.253
100	1.253
105	1.254
110	1.254
115	1.254
120	1.254
125	1.254
130	1.254
135	1.254
140	1.254
145	1.251
150	1.25

Oscillator
Frequency over
Temperature

°C	f(MHz)
-55	7.98
-50	8.03
-45	8.1
-40	8.16
-35	8.21
-30	8.27
-25	8.31
-20	8.35
-15	8.37
-10	8.4
-5	8.44
0	8.48
5	8.49
10	8.51
15	8.53
20	8.54
25	8.55
30	8.57
35	8.57
40	8.57
45	8.57
50	8.56
55	8.55
60	8.54
65	8.51
70	8.5
75	8.47
80	8.45
85	8.43
90	8.4
95	8.37
100	8.33
105	8.3
110	8.25
115	8.21
120	8.18
125	8.14
130	8.1
135	8.06
140	8.02
145	7.98

150	7.94

Supply Current over Temperature

^oC	*mA*
-55	5.2
-50	5.22
-45	5.24
-40	5.26
-35	5.27
-30	5.28
-25	5.29
-20	5.3
-15	5.31
-10	5.31
-5	5.31
0	5.31
5	5.31
10	5.31
15	5.31
20	5.3
25	5.29
30	5.28
35	5.27
40	5.26
45	5.25
50	5.24
55	5.22
60	5.21
65	5.19
70	5.17
75	5.15
80	5.12
85	5.1
90	5.08
95	5.05
100	5.02
105	5
110	4.97
115	4.94
120	4.92
125	4.89
130	4.86
135	4.82

140	4.79
145	4.75
150	4.72

Shutdown Pin Bias Current over Temperature

°C	nA
-55	79.9
-50	77.2
-40	72.3
-30	68.3
-20	64.4
-10	60.8
0	57.3
10	53.9
20	51.1
30	48.5
40	46.1
50	43.8
60	41.8
70	39.9
80	38.2
90	36.6
100	35.1
110	33.7
120	32.4
130	31.2
140	30.1
150	29.1