RF Power CMOS

by

Jörg Scholvin

Submitted to the Department of Electrical Engineering and Computer Science

in Partial Fulfillment of the Requirements for the Degrees of

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ABSTRACT

In the mobile wireless industry, system size and cost are important factors for having a competitive product. Because of this, in the future system-on-chip (SOC) solutions are likely to emerge. For wireless communications products, this means that the power amplifier (PA) needs to be integrated with the rest of the analog and digital circuitry. This thesis has experimentally studied the suitability of a commercial 0.25 μm logic CMOS device technology for RF power applications. In particular, the suitability of the standard BSim3v3 device model for accurately capturing RF power behavior has been evaluated. Our study includes DC, small-signal RF, and large-signal RF characteristics. It was found that there are severe discrepancies between the BSim3v3 model and the measured results. A new model was constructed by adding a passive circuit topology that accounts for device parasitics not captured by the BSim3v3 model. The newly developed circuit model has been shown to accurately predict the device's RF power behavior. The physical origins of the new circuit elements and their dependencies on device layout have been identified.

Thesis Supervisor: Jesús A. del Alamo
Title: Professor of Electrical Engineering

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I would like to thank our sponsor Global Communication Devices (GCD), and Geoff Dawe for supporting this work and making it possible to have the devices fabricated at TSMC. I also want to thank Ethan Dawe at GCD for doing the device layouts.

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I want to thank Agilent Technologies for generously donating the software, ADS, without which this work would not have been possible.

Finally, I'd like to thank my parents for their support and initiative that led me to where I am now.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Motivation

The focus of this thesis is on the modeling and understanding of standard CMOS devices for RF power applications. In a wireless system, the power amplifier (PA) is a crucial component, and being able to implement it together with digital and RF analog circuitry would allow to have a system-on-chip (SOC) solution, which will result in improved cost efficiency, and overall smaller system size.

There has been some recent work on RF power amplifiers using logic CMOS technologies. Table 1.1 summarizes the performance of these amplifiers [1-3].

Technology	Frequency [GHz]	Supply Voltage	P_{out} [dBm]	Gain [dB]	PAE [%]	Reference
0.24 μm CMOS	2.4	2.5	18	11	24	[1]
0.35 μm CMOS	1.9	2.5	22	20	44	[2]
0.35 μm CMOS	2	2	30	20	48	[2]
0.35 μm CMOS	1.9	2	30	not reported	41	[1]
0.8 μm CMOS	1.9	3	20	13	16	[1]
0.8 μm CMOS	0.8	2.5	30	25	42	[3]
0.8 μm CMOS	1.9	3	24	17	32	[1]
Bipolar	2	3.3	27	35	35	[2]
GaAs	1.9	3.4	22.5	29	29	[2]
GaAs (PHEMT)	1.9	3.6	31	30	45	[2]

Table 1.1 PA performance figures for various CMOS technologies. The amplifiers are multistage, typically 2-stage, amplifiers. For comparison, three non-Silicon PA have been included. The figures are the ones reported in the papers, and do not mention the compression point at which the data was read off. Therefore direct comparison is difficult, yet the numbers give a sense of the orders of magnitude in PAs.

For evaluating device performance, we have to look at only the device itself. Table 1.2 lists the published performance figures for a commercial device [4].

Technology	Frequency [GHz]	P_{out} [dBm]	Gain [dB]	PAE [%]
0.24 μm CMOS	2.4	19	11.2	26

Table 1.2. Device performance at the 1dB compression point of the device reported in [4]

There are several interesting questions as one considers the suitability of logic CMOS for RF power applications:

- How far can logic CMOS technology go in delivering the RF power amplifier (PA) function?
- How does this picture change as CMOS continues to be scaled down?
- What can be done to logic CMOS device and process design to improve its RF PA capabilities? How can the device layout be optimized for the PA function?
- How well can device model developed for logic capture RF power behavior? How can we improve these models?

In this work, we will try to answer the questions in the last item, modeling of RF-CMOS devices. Improved and accurate models will help allow better designs of RF CMOS PAs.

1.2 Previous Modeling Work on RF-CMOS

RF-CMOS modeling is a relatively new field. The BSIM3v3 model has been shown to give good results for RF simulations when extended by a gate resistance [5] and a substrate network [4]. The need for these additions and an overview of some different

substrate network topologies has been described in [4], discussing their suitability to match the RF power measurements. However, neither of the two papers [4,5] discusses linearity for their modified BSim3v3 model. With the modulation schemes for digital wireless applications depending on a linear PA, the linearity figures of merit (IM_3 in this work) become increasingly important.

The small-signal RF accuracy of the BSim3v3 model and the addition of model elements to match S-parameter measurements has been more thoroughly studied, than the large-signal RF-CMOS models mentioned before [6,7]. From these publications, we can see that the gate resistance (being the most important element to add) occurs in all of the proposed models. However, there is a fairly large discrepancy on the other parameters, in particular the substrate network. Different models all claiming an accurate fit can be seen in [4-10].

1.3 Thesis Goals and Outline

The goal of this thesis is to show that an accurate RF device model can be built from the BSim3v3 model, and that it will be able to predict the results of DC, S-parameter and load-pull measurements. We will derive such a model by adding new circuit elements to the BSIM3v3 model, which itself will not be changed. Also, an explanation for the new model elements in terms of the layout of the device will be given.

Here is how this thesis is organized. Chapter two will first describe the devices, the measurements that have been carried out, and shows typical measurement data. The measurements consist of DC, S-parameter, and load-pull (P_{out}, Gain, I_d, PAE and IM_3) measurements. Chapter three will describe the simulation setups for the measurements of chapter two, and show typical simulation results obtained from TSMC's BSim3v3 device model. Having thus established the measurement and simulation setups, chapter four will compare the measurements with the BSim3v3 model. Finding that the model is not accurate enough, new elements will be added to create a device model that can accurately predict the S-parameter and load-pull measurements. The model is build step-by-step, with the goal to match the S-parameter measurements up to 20 GHz. The model element values are obtained without taking the load-pull data into account. At the end, a comparison of the new model with S-parameter and load-pull measurements is done to prove the model's accuracy in predicting the load-pull measurements. Having now an accurate model at hand, chapter five analyzes the new model elements and connects them with the device layout. This is done by looking into how the element values change as the device is scaled either in the unit finger width or in the number of fingers dimension. The work concludes with chapter six, presenting our conclusions and suggestions for future work.

Chapter 2

Measurement Setups

This chapter describes the devices and the measurement setup used in this thesis, and shows typical measurement results. The measurements performed are DC-characterizations, S-parameter measurements, and large signal measurements of P_{out}, Gain, I_d, PAE, and IM_3 as a function of P_{in}. We also show how the non-linearities of the device mathematically give rise to the intermodulation distortion (IM_3).

2.1 Device Design and Layout

The devices used in this thesis are fabricated in the digital 0.25 μm CMOS process of TSMC. Parameters available in the device design are the dimensions of the device (number of fingers, unit finger width), and the layout style of the device. This gives us three dimensions along which to explore device behavior. The layout style involves the routing of source, drain and gate interconnects and is important for the parasitics, but not the device behavior as such. Thus, we decided to reduce to two dimensions, namely the number of fingers and unit finger width. This space is explored in detail around a center design point. This allows a reasonable investigation of both dimensions, while keeping the number of test devices within reasonable bounds.

In the equations in this thesis, we will use the following symbols for the number of fingers, unit finger width and total width:

W_g = total gate width

w_g = unit finger width

n_f = number of fingers

where $W_g = n_f \times w_g$

Fig. 2.1-1 shows the design space of the devices used. The center device was chosen to be 16 fingers, 20 μm unit finger width (16x20 μm). From here, we can explore in three directions, holding one parameter constant at a time: the horizontal shows varying number of fingers, while the unit finger width stays fixed. In the vertical, the number of fingers stays constant, and the unit width changes. Furthermore, one can move along lines of constant total width trading off number of fingers and unit finger width. All variations of parameters occur in factors of two. The device layout for the 16x20 μm device is shown in Fig. 2.1-2. A schematic of the vertical cross-section showing the metal layers can be found in Fig. 2.1-3.

In addition to the devices, de-embedding structures are necessary to remove the impact of the pads and metal lines on RF measurements. These are identical to the device layouts, except that they have the device contacts removed so only the pad and interconnect parasitics are measured.

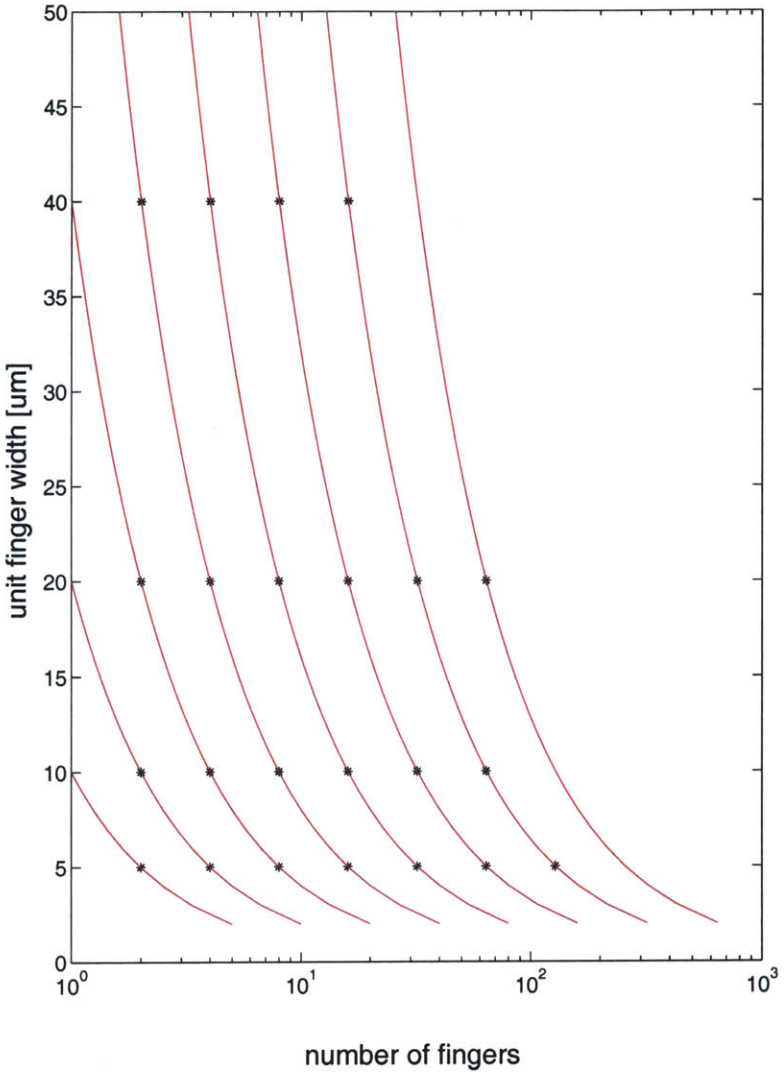

Fig. 2.1-1 Device design space. The lines connecting points indicate constant total widths of 10, 20, 40, 80, 160, 320, 640, and 1280 μm.

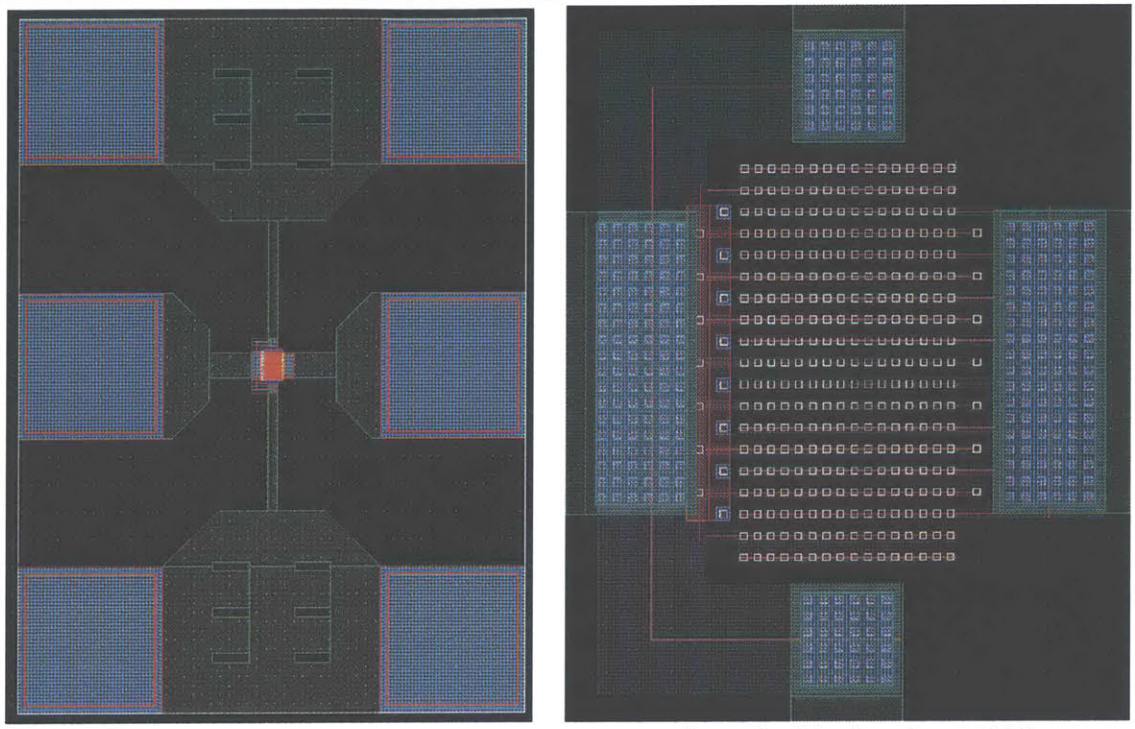

Fig. 2.1-2 Device layout for the 16x20 μm device. Left: pads (blue) and *metal4* lines (green) to the device. Right: Device itself, showing the *metal4* lines (green), *metal2* (red area), *metal1* (blue) and contact holes (white squares). The gates, which are not shown, run between the *metal1* fingers.

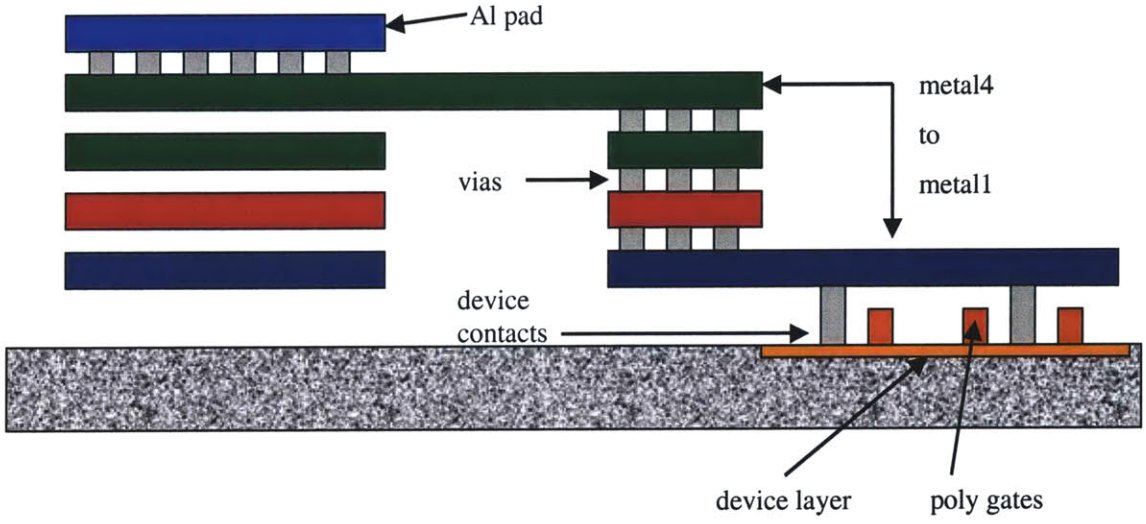

Fig. 2.1-3 Vertical cross-section of the device and metal layers, for the source or drain path. The gate would be routed on the metal2 level rather than the metal1, and then brought down to the poly silicon with vias.

2.2 DC Measurement Setup

The devices are characterized using a HP 4155 Semiconductor Parameter Analyzer, on a Cascade Wafer Probe Station. The measurements are performed on die. All measurements are performed around 23°C. The HP 4155 is connected to a HP 41501B High Current unit, to allow biasing currents up to 1 A. The setup is shown in Fig. 2.2-1. The line between the device and the measurement equipment contains a bias T, which separates the RF and DC components. The RF component is connected to a 10 dB attenuator, which is necessary to prevent the DC measurement from suffering from oscillations caused by RF noise.

A typical DC measurement result is shown in Figs. 2.2-2 to 2.2-6, including the output characteristics, output conductance (g_d), transfer characteristics, transconductance (g_m), and subthreshold characteristics for the 16x10 μm device. In the output characteristics, the drain-source voltage is swept for a set of given gate voltages (Fig. 2.2-2). Taking the derivative, we obtain the output conductance, g_d (Fig. 2.2-3). In the transfer characteristics we sweep the gate voltage, maintaining a constant drain-source voltage (Fig. 2.2-4). The derivative obtained here is the transconductance, g_m (Fig. 2.2-5). If we plot the transfer characteristics on a semi-log scale, we get the subthreshold characteristics, which allows looking closely at device behavior below the threshold (Fig. 2.2-6). Also, it allows for a good assessment of the drain induced barrier lowering (DIBL).

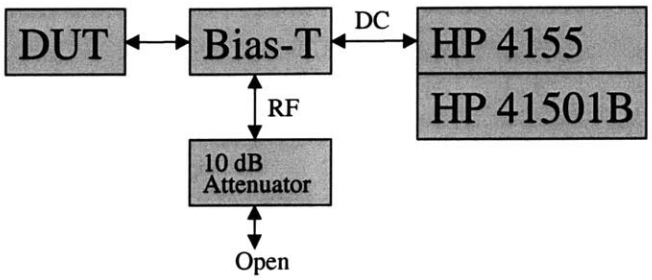

Fig. 2.2-1 DC Measurement Setup. The Bias-T has the purpose to avoid oscillations.

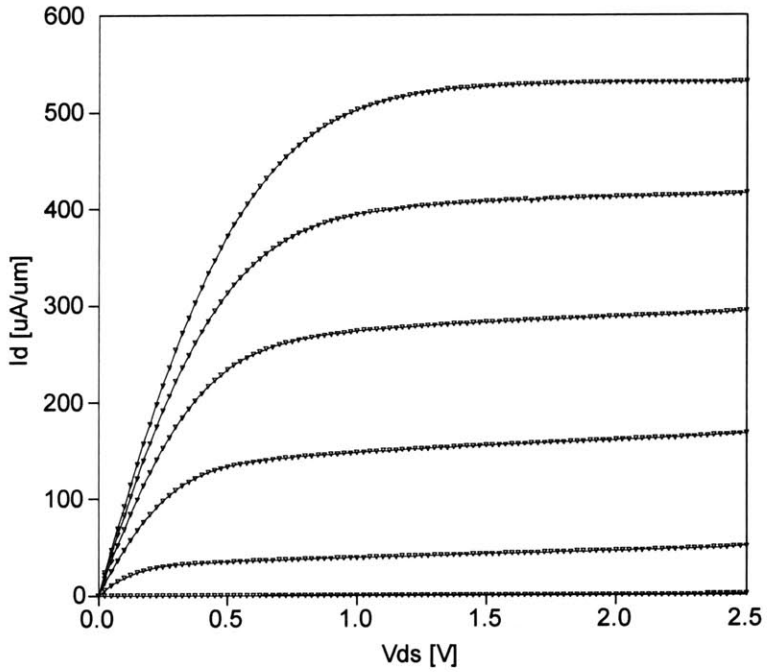

Fig. 2.2-2 Output Characteristics of the 16x10 μm device, with V_{gs} from 0 to 2.4 V in 0.2 V steps.

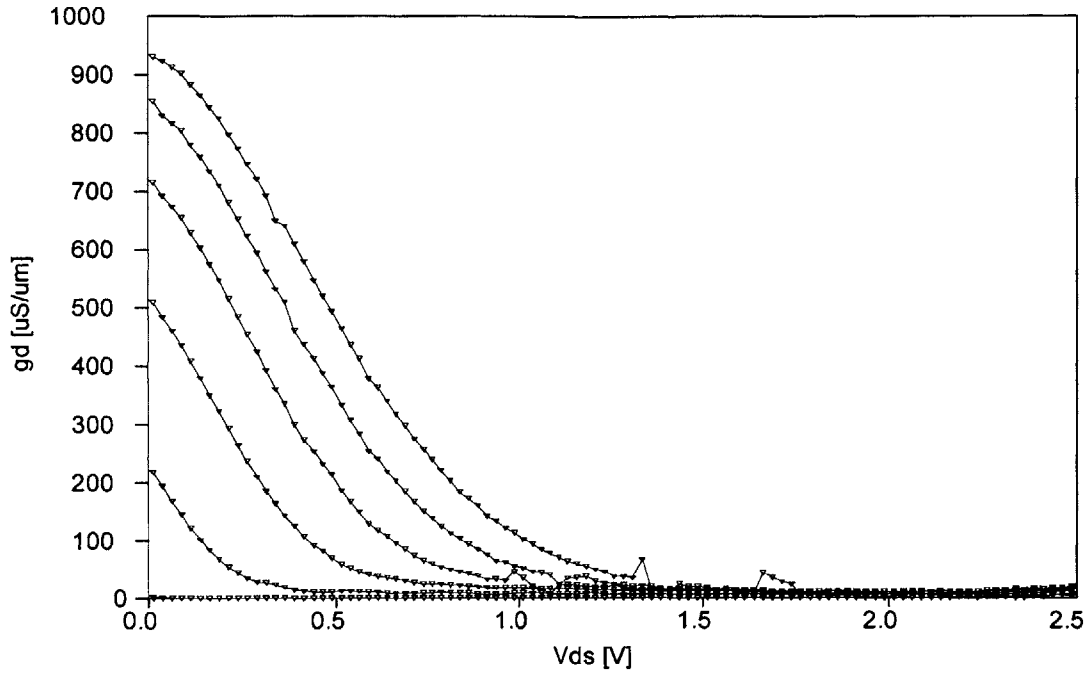

Fig. 2.2-3 Output Conductance for the 16x10 μm device, with V_{gs} from 0 to 2.4 V in 0.2 V steps.

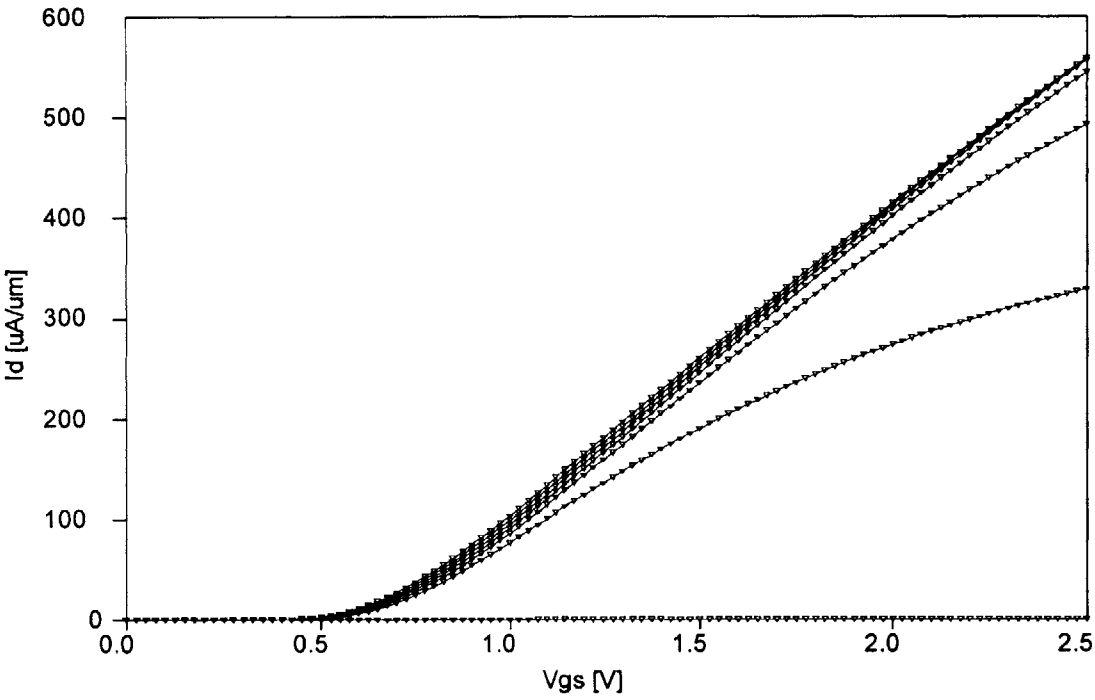

Fig. 2.2-4 Transfer Characteristics of the 16x10 μm device, with V_{ds} from 0 to 2.4 V in 0.2 V steps.

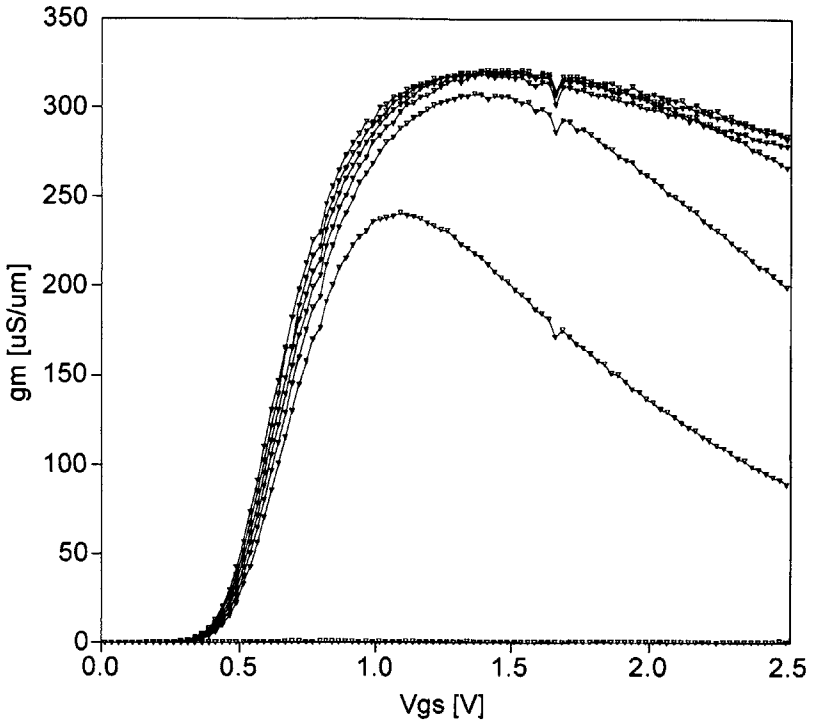

Fig. 2.2-5 Transfer Characteristics of the 16x10 μm device, with V_{ds} from 0 to 2.4 V in 0.2 V steps.

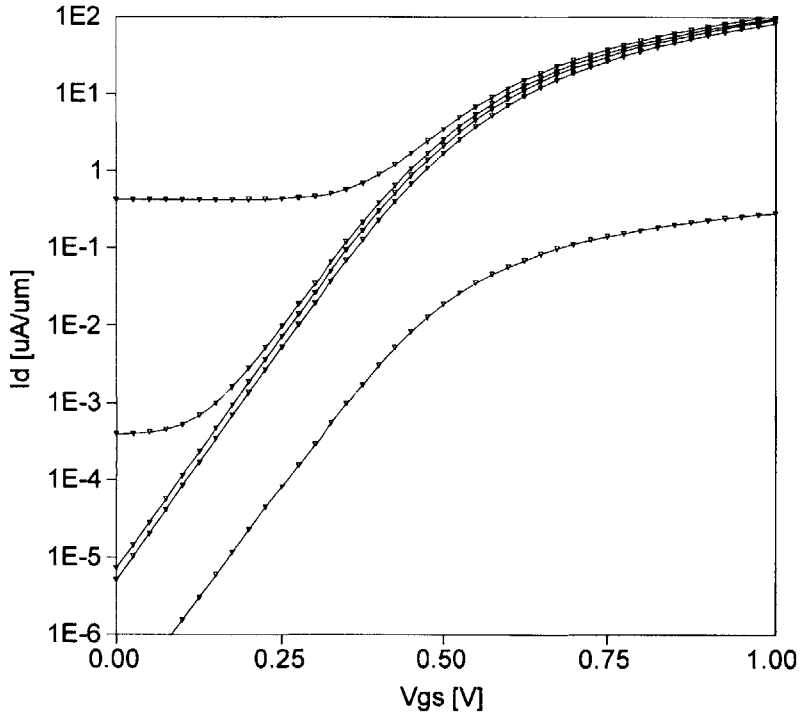

Fig. 2.2-6 Subthreshold Characteristics of the 16x10 μm device, with V_{ds} from 0 to 2.4 V in 0.2 V steps.

2.3 S-Parameter Setup

Fig. 2.3-1 shows the S-Parameter measurement setup. An Agilent 8510C network analyzer is used to perform the measurement, with the HP 4155/HP 41501B connected to it to supply the DC biasing through a bias-T inside the network analyzer. The network analyzer is capable of measuring up to frequencies of 50 GHz.

A typical S-parameter measurement from 500 MHz to 20 GHz is shown in Fig. 2.3-2, for the 16x20 μm device after de-embedding. The device is biased at V_{gs}=1.4 V, V_{ds}=2.0 V. De-embedding is important to remove the parasitic effects of the probe-pads from the measurement, which would otherwise mask the device behavior. Our de-embedding structures are identical to the devices, except that the contact layer to the device itself has been removed. Measurements of the device and the de-embedding structure are then taken. Assuming a primary parallel nature of the pad parasitics (capacitance dominates) the device can be de-embedded by subtracting the de-embedding structure's Y-parameters from the device Y-parameters [11]. The result is a S-parameter measurement of the device, without the impact of the pad-parasitics. The Y-parameters after de-embedding are shown in Fig. 2.3-3. Fig. 2.3-4 shows the short circuit current gain ($|h_{21}|$) and the unilateral gain (g_{tu}), both of which are important figures of merits for device and circuit designers. The de-embedding process will be described in more detail in section 2.5.

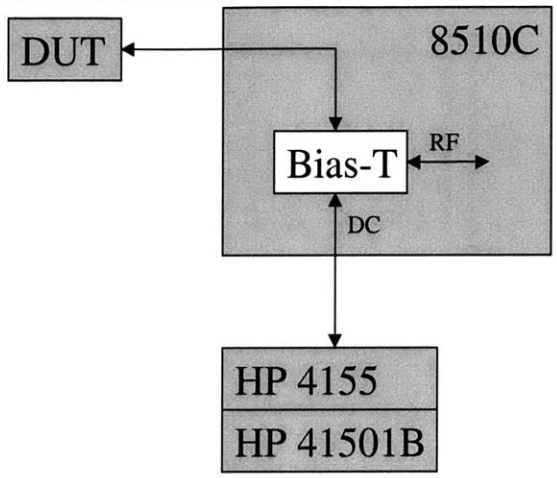

Fig. 2.3-1 S-Parameter Measurement Setup

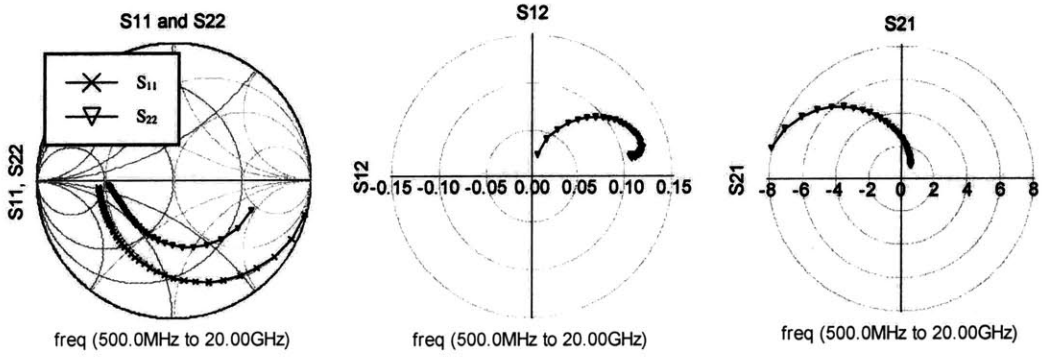

Fig. 2.3-2 Measured S-parameters for the de-embedded 16x20 μm device biased at V_{ds}=2V, V_{gs}=1.4V

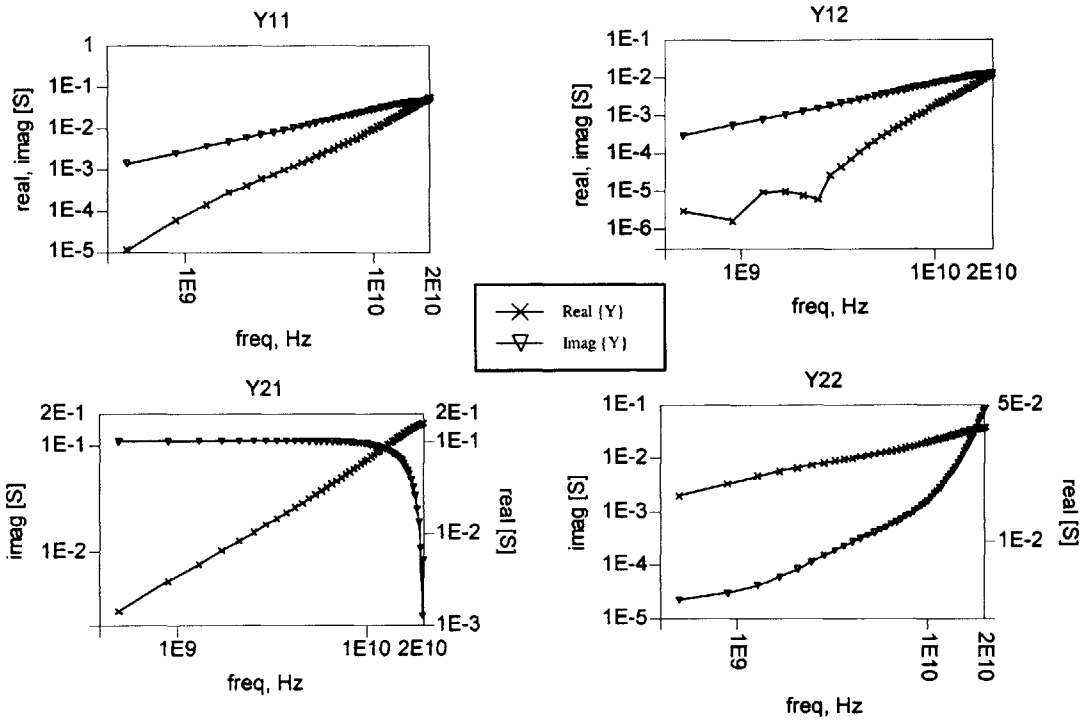

Fig. 2.3-3 Measured Y-parameters for the de-embedded 16x20 μm device biased at V_{ds}=2V, V_{gs}=1.4V

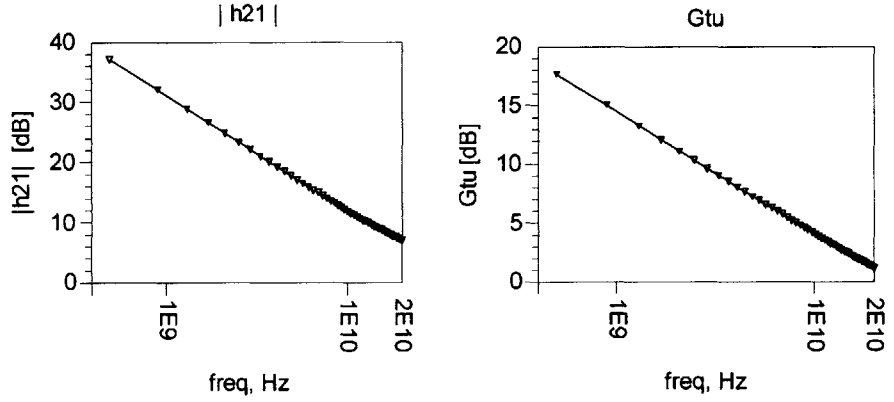

Fig. 2.3-4 Measured |h21| and G_{tu} for the de-embedded 16x20 μm device biased at V_{ds}=2V, V_{gs}=1.4V

2.4. Large Signal Characterization

Large signal characterization was performed on selected devices at 2.45 GHz. This included power-sweeps, IM3 measurements, and load-pull contour measurements. Measurements were done on a Load-Pull System at ATN Microwave Inc. The measurement allows determining the device behavior as a function of the input power, and source- and load-impedance.

In the power-sweep measurement, the available input power (which we will refer to simply as input power) is swept, while the source and load impedances are held constant. From this measurement the 1 dB compression point can be determined. A load-pull (or source-pull) measurement is then performed at the 1 dB compression point, varying the load (or source) impedance over a specified area of the Smith chart, while holding the input power constant. This helps to find a more optimal impedance. Generally, the power-sweep and load/source pull sequence is repeated until a stable optimum is reached. For modeling purposes, it is not necessary to run this cycle too many times. While it is important that the measurements are done in a region close to the optimum, finding the optimum itself is not essential. In our case, the sequence was a power sweep, followed by a load-pull at the 1 dB point, followed again by a power sweep at the load impedance that was giving the maximum output power. All power-sweep data used in this work is data from this stage. The optimized impedances are recorded and are later used in the simulations.

A typical result of a power sweep is shown in Fig. 2.4-1. For low power levels, the output power as a function of available input power has a slope of one,. As the input power increases the device eventually goes into compression and the slope flattens. The difference between input and output power is the gain, which starts to drop as the device goes into compression. The supply current equals to the DC current until the device enters compression. As the power is increased, the power added efficiency (PAE) goes up, because more power is delivered to the load for the same DC power dissipation. However, as the device enters compression, the efficiency will eventually decrease again, because the gain decreases due to compression. This cannot be seen in Fig. 2.4-4, because the device was not measured too far into compression.

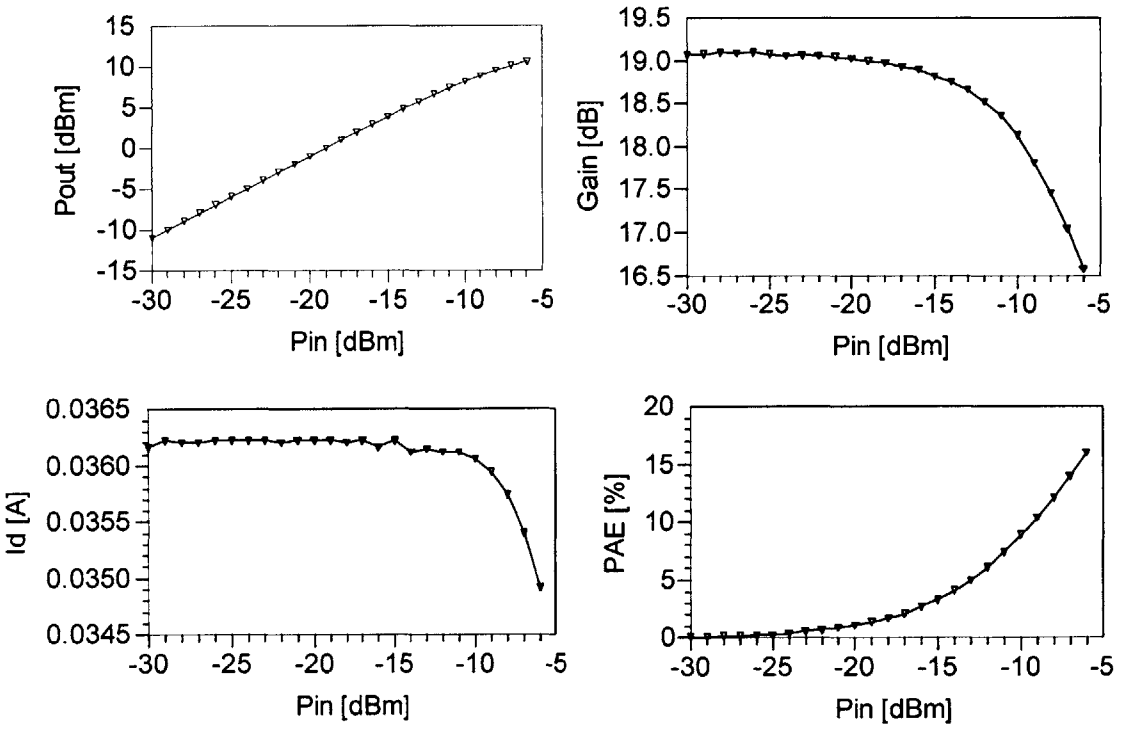

Fig. 2.4-1 Power-sweep measurements for the 08x20 μm device biased at V_{ds}=2 V, V_{gs}=1.4 V

2.4.1. Intermodulation Distortion (IM_3)

In digital wireless communication systems, linear modulation methods (QAM, PAM, PSK) require good linearity of the power amplifier. A typical measure for linearity is the intermodulation distortion, IM_3. The measurement principle and definition of IM_3 is explained in [12-14]. It evaluates the intermodulation distortion by introducing two closely spaced tones at the input.

Distortion arises from non-linearities in the amplifier. If we assume a memoryless time-variant system, the output *y(t)* to an input *x(t)* can be written as a Taylor expansion. Considering only the first three terms,

$$y(t) = \alpha_1 x(t) + \alpha_2 x(t)^2 + \alpha_3 x(t)^3 \qquad \text{[Eq 2.4.1-1]}$$

We let the input be a sum of two tones,

$$x(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t) \qquad \text{[Eq 2.4.1-2]}$$

where the two frequencies are

$$\omega_{1,2} = \omega_0 \pm \Delta\omega \qquad \text{[Eq 2.4.1-3]}$$

If we now insert the 2-tone input into equation [2.4-1], the higher order terms will result in products of cosines of both frequencies. Simplifying this into a sum of single cosines, we observe cross-terms:

$$y(t) = \left(\alpha_1 + \frac{9}{4}\alpha_3 A^2\right) A\cos(\omega_1 t) + \left(\alpha_1 + \frac{9}{4}\alpha_3 A^2\right) A\cos(\omega_2 t) + \frac{3}{4}\alpha_3 A^3 \cos((2\omega_1 - \omega_2)t) + \frac{3}{4}\alpha_3 A^3 \cos((2\omega_2 - \omega_1)t) \quad \text{[Eq 2.4-4]}$$

The later two terms are at frequencies

$$\omega = \omega_0 \pm 3\Delta\omega \quad \text{[Eq 2.4.1-5]}$$

Their amplitude depends on how linear the system is (i.e. α_3 small). The output spectrum is shown in Fig. 2.4-6. In the IM_3 measurement, the first and second terms of [2.4.1-4] are

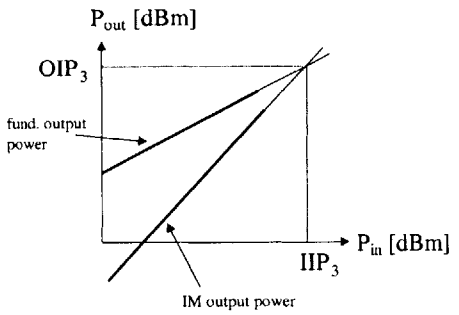

Fig. 2.4.1-1 Intermodulation and fundamental output power as a function of the input power

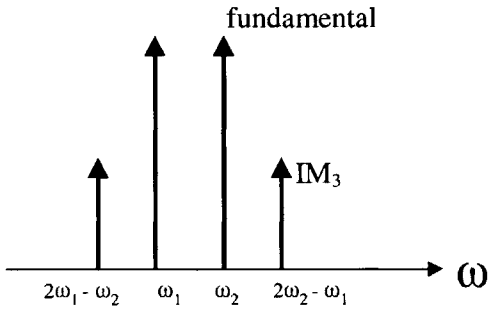

Fig. 2.4.1-2 Output frequency spectrum

the fundamental outputs, while the third and fourth terms are the third order intermodulation outputs. Obviously, the form of the system given in equation [2.4.1-1] does not have to be limited to the third power of x. If we were to include higher order terms (with coefficients getting smaller for higher orders), the coefficients in equation [2.4.1-4] will have additional terms. Also, there will be other frequencies at which interference occurs. However, those frequencies tend to be further away from the channel and at lower amplitudes. [13] lists a table of higher order terms and other intermodulation frequencies.

If we plot the power of the fundamental and intermodulation terms of equation [2.4.1-4], we see that the power of the interfering tones increases at a higher slope on a dBm/dBm plot. This is because of the cubic nature of the 3rd order term. If we extrapolate, the lines will intersect. This point is called the 3rd order intercept point. Extrapolation is required, because the device will go into compression before it reaches the intercept point. The x- and y- axis coordinates of the intercept point are referred to as the input- and output IP_3's, IIP_3 and OIP_3. Figure 2.4-5 illustrates this.

A potential source of confusion can be the input power. It is important to know whether P_{in} means available power, or power into the device, and whether it refers to the power of each individual tone, or the power of both tones. In this work, P_{in} for the IM_3 measurement refers to the overall available power of both tones combined. A similar ambiguity can arise when referring to P_{out}. In this work, P_{out} for the IM_3 measurement means the overall power out of both tones. A typical IM_3 measurement result is displayed in Fig. 2.4.1-3, showing IM_3 in a dBm as well as dBc plot.

Having the correct definition of IM_3 is important. The measurement can be taken in units of dBm and dBc. When in units of dBm, the measurement is the power of the third order IM tone (as in Fig. 2.4.1-1). Both the high and low IM tones are recorded, this work uses the average of both. We can use the average as long as the low and high IM_3 are close together in their values. When the high and low IM_3 diverge, the linearity is no longer accurately described by the IM3 measurement. In units of dBc, the measurement is

relative to the carrier power, which is equivalent to subtracting the fundamental output power [dBm] from the IM_3 output power [dBm].

It should be noted that for modern digital communication circuits, the adjacent channel power ratio (ACPR) is of great importance. It involves a more complex and time-consuming measurement. However, the ACPR can be related to the IM_3 data and reasonably well estimated from it [15].

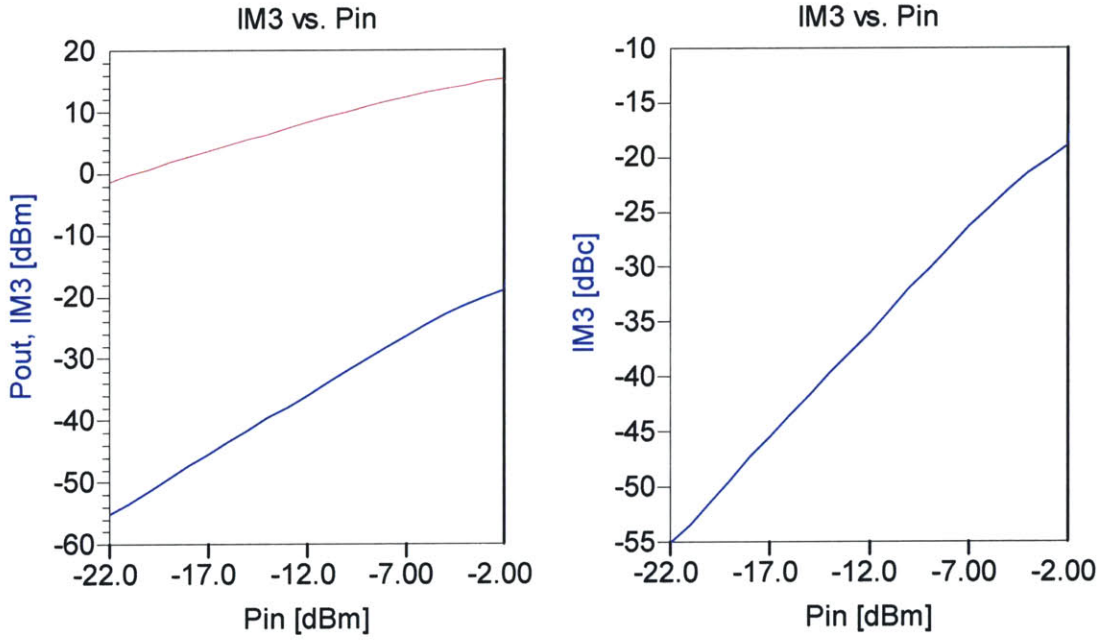

Fig. 2.4.1-3 IM_3 measurement versus total available power, for the 32x20 μm device biased at V_{ds}=2 V, V_{gs}=1.4 V. The left graph shows IM_3 (bottom) and the total output power (top), both in units of dBm, similar to the sketch of Fig. 2.4.1-1. The right graph shows IM_3 in units of dBc. One can see that the difference of IM_3 [dBm] and P_{out} [dBm] amounts to the IM_3 [dBc], with a slope of two.

2.5. De-Embedding

When doing RF measurements, the network analyzer calibration takes account of the wire and probe dissipation. Thus, the measurement plane is the tip of the microwave probes. Ideally, we would like to measure the device itself only, without any interconnects and pads. To achieve this, we could use a method similar to the network analyzer calibration, using open, short and through structures [16-20]. However, this would require not one but three de-embedding structures for each device. Given a fixed chip size, this would cut the number of devices we can explore in half.

A more primitive method is to assume that most of the parasitics will be in parallel with the device, as shown in Fig. 2.5-1. In this case, only one de-embedding structure is needed. It will be identical to the device, but with device contacts removed. To de-embed, we can see that the device and the parasitic network are in parallel. Thus, if we have a measurement of the parasitic network, we can obtain the intrinsic device data by subtracting the parasitic network measurement in Y parameter space from the 'device +

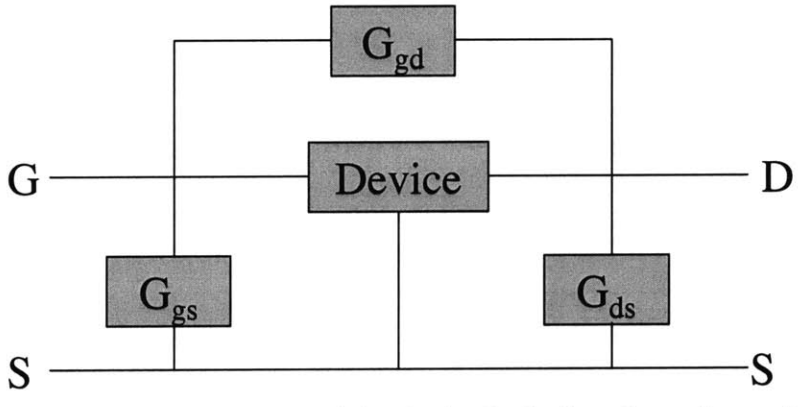

Fig. 2.5-1 Simple model of the device including the pad parasitics

parasitics' measurement.

Fig. 2.5-1 shows the Y-parameters before and after the de-embedding, along with the measured de-embedding structure. We can see that the measured pads are strongly influencing the measurement of Y_{11} and Y_{22}. This is because the source is overlapping with the drain and gate. The gate and drain are well separated, and thus do not have a lot of parasitic interaction. The effect of the de-embedding on Y_{21} is small, because the device's high gain results in the intrinsic Y_{21} being orders of magnitudes larger than the pad-parasitics. On the other hand, the intrinsic device has a very small Y_{12}, and the de-embedding has a small effect on the real part of Y_{12}, seen in Fig. 2.5-1.

2.6. Summary

This chapter has described the measurements performed on the CMOS devices. Characterization consisted of DC, S-parameter, and large signal measurements. For the S`-parameters, de-embedding is important to allow a look at the device behavior without having the pad parasitics interfering. In the large signal measurements, definitions of input and output power levels were made. This is important because one term can have several different interpretations.

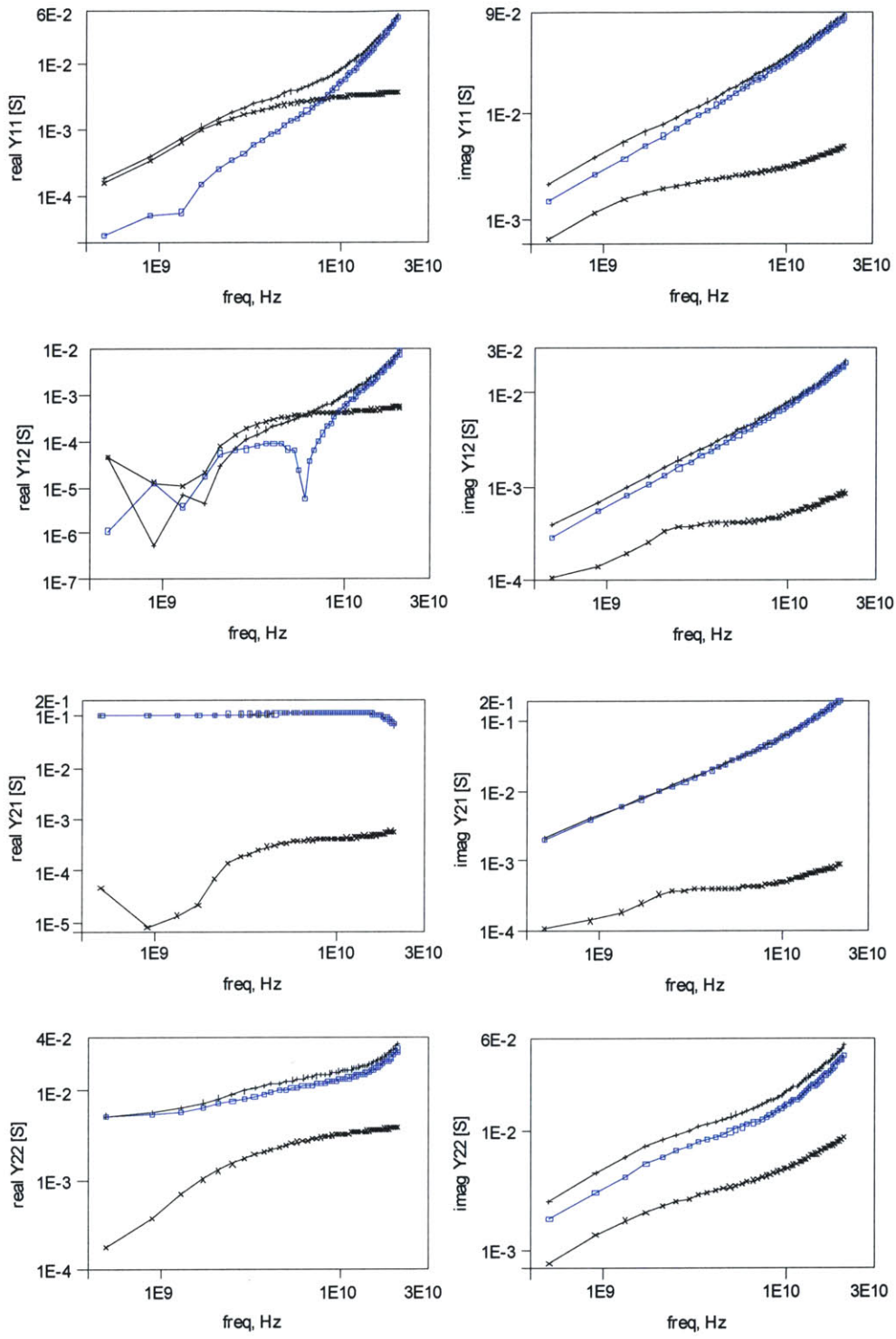

Fig. 2.5-2 Y-Parameter measurements, illustrating the impact of the de-embedding. Each graph shows the pad, the device + pad, and the de-embedded measurement (see legend below)

Chapter 3

Simulation Setups

The modeling that has been carried out in this thesis is based on the BSim3 model supplied by TSMC for their devices. This chapter describes the simulation setup, which is done in Agilent Advanced Design System, version 1.5 (ADS 1.5). The graphs are based on simulations with the TSMC BSim3 model only, and do not include any modifications to the model, which will be made in chapter 4. This chapter shows the simulation suites and the results, for DC, S- and Y-Parameter, IM_3 and power-sweep simulations. All simulations are performed using only the TSMC BSim3v3 device model, except for the IM_3 and power-sweep simulations, which included the measured pad data as well.

3.1. DC Verification

Before looking at the AC performance, it is important to model the DC characteristics. This assures that threshold voltage and other important DC parameters are accurate. A picture of the DC simulation setup and the simulation results are shown in Fig. 3.1-1. and 3.1-2-6 respectively. The simulation includes the probe resistance, which we measured to be on the order of 0.5 to 1.2 Ohm, depending on the quality of the contact.

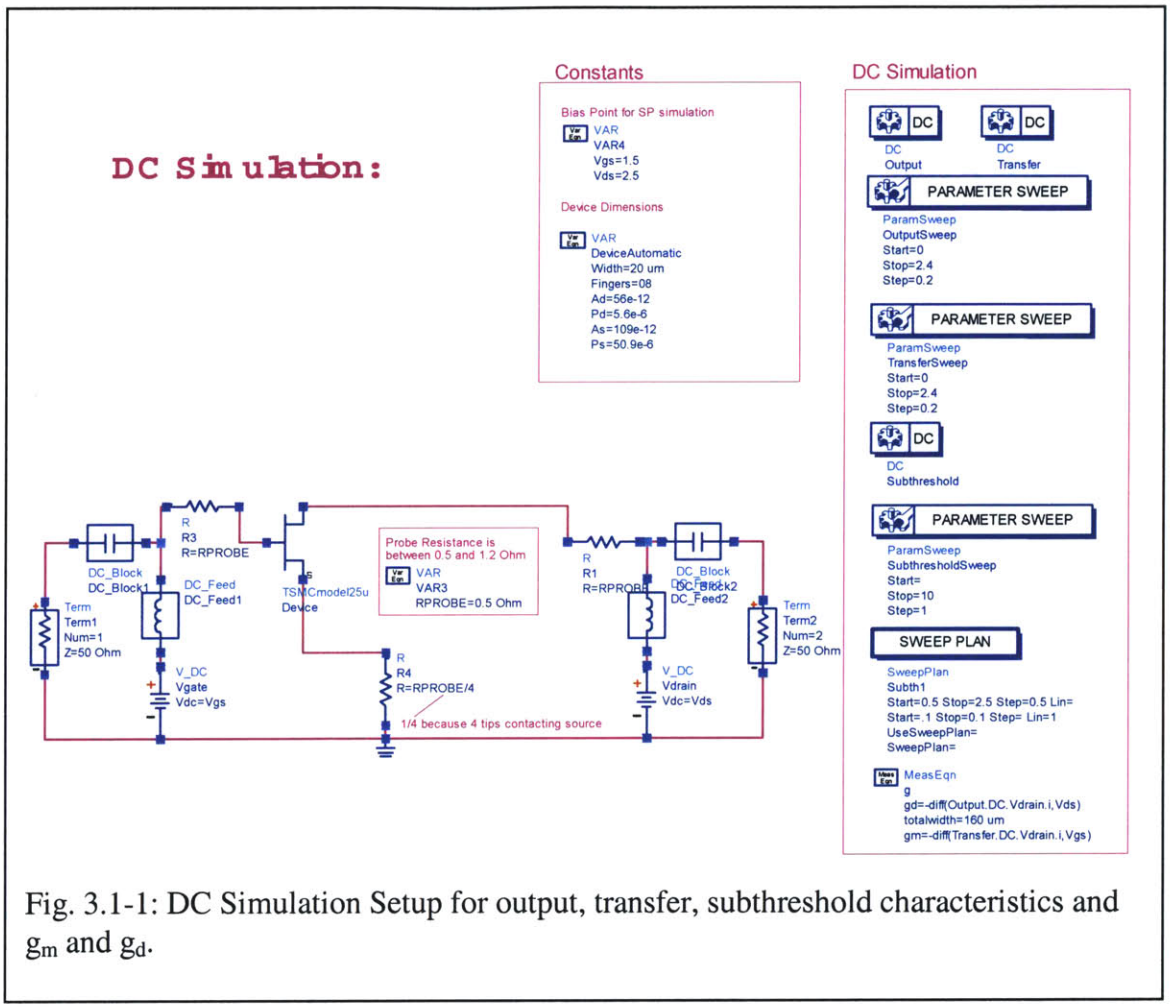

Fig. 3.1-1: DC Simulation Setup for output, transfer, subthreshold characteristics and g_m and g_d.

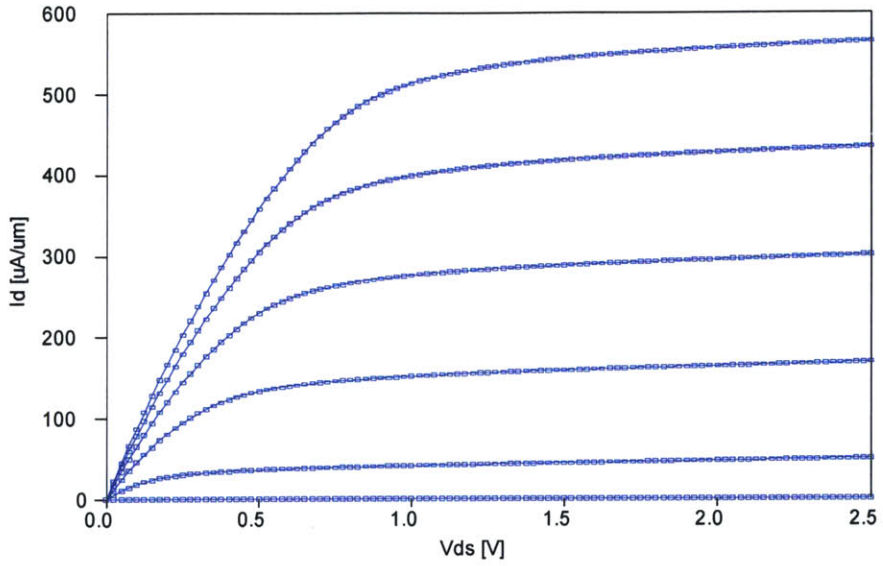

Fig. 3.1-2 Simulated output characteristics of the 08x20 μm device, with V_{gs} from 0 to 2.4 V in 0.2 V steps

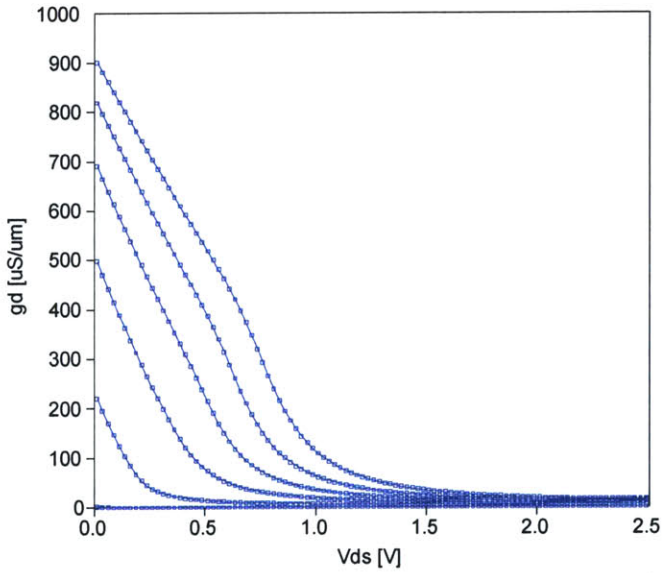

Fig. 3.1-3 Simulated output conductance of the 08x20 μm device, with V_{gs} from 0 to 2.4 V in 0.2 V steps.

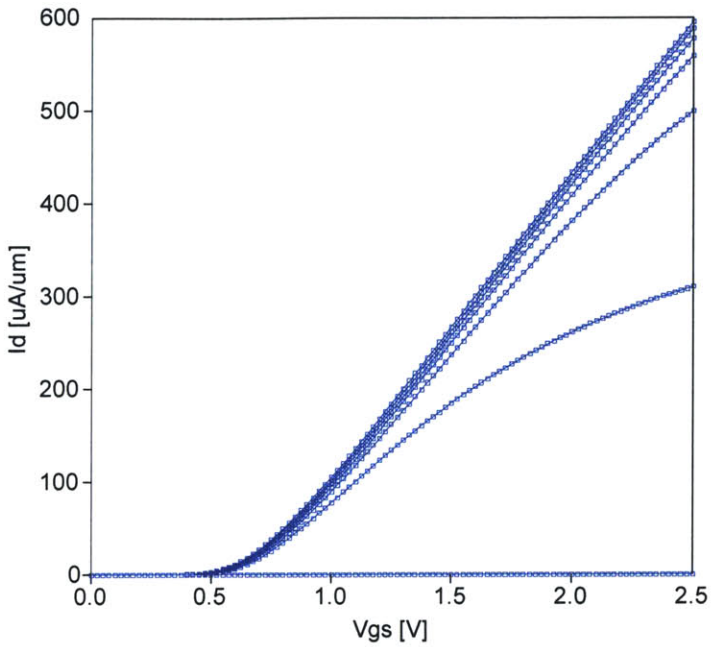

Fig. 3.1-4 Simulated transfer characteristics of the 08x20 μm device, with V_{ds} from 0 to 2.4 V in 0.2 V steps.

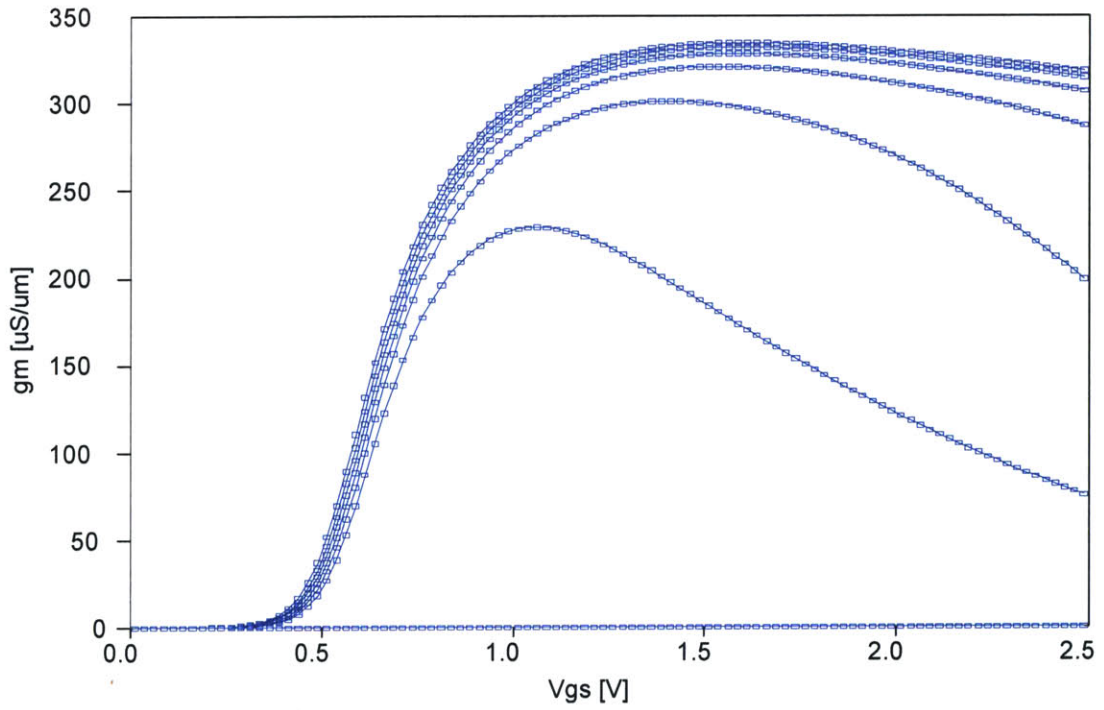

Fig. 3.1-5 Simulated transconductance of the 08x20 μm device, with V_{ds} from 0 to 2.4 V in 0.2 V steps.

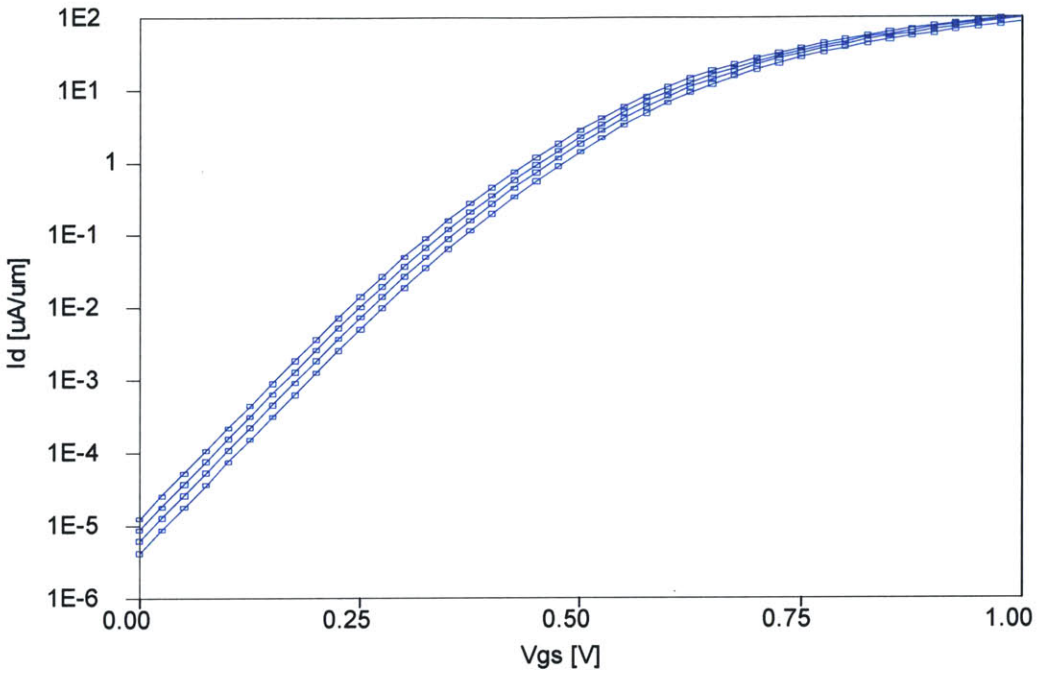

Fig. 3.1-6 Simulated Subthreshold characteristics of the 08x20 μm device, with V_{ds} from 0 to 2.4 V in 0.2 V steps

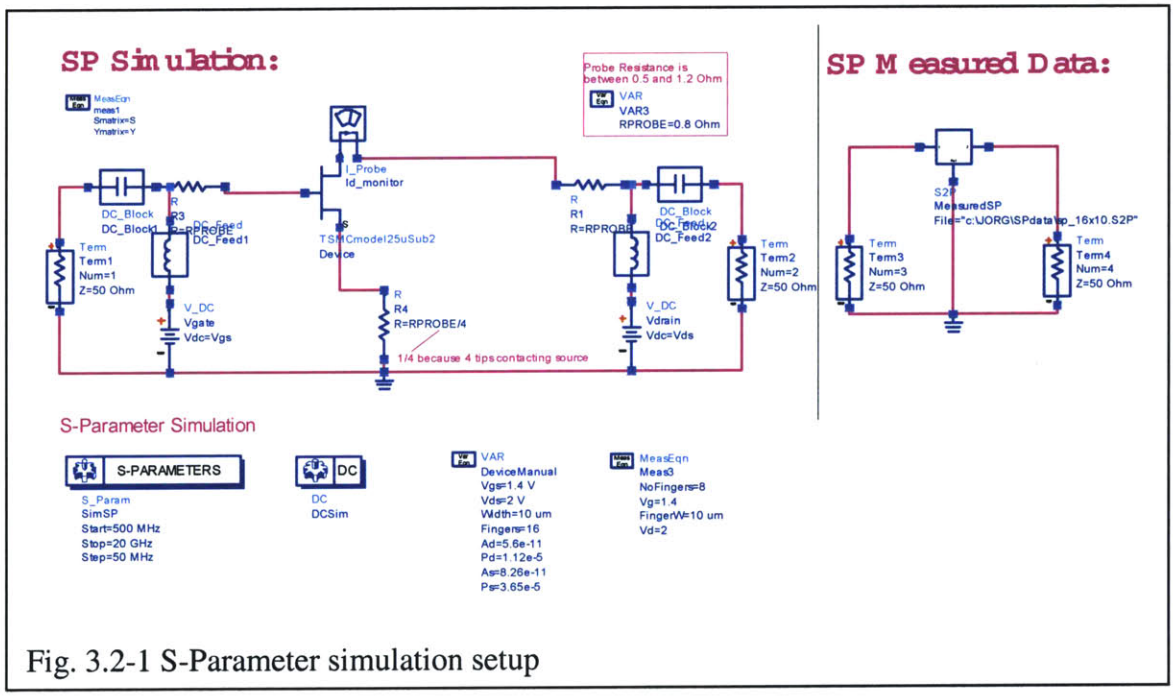

Fig. 3.2-1 S-Parameter simulation setup

3.2 S-Parameter Simulations

The S-Parameters simulation setup includes the same probe resistances, and ideal bias T's to mix the RF and DC signals. Both an S-Parameter as well as a DC simulation are done. The purpose of the DC simulation is to sweep the gate voltage V_{gs}, while monitoring the drain current. This allows adjusting the gate voltage in the S-Parameter simulation, such that the drain current coincides with the measured current level. This method compensates for very small inaccuracies in the model's threshold voltage. In Fig. 3.2-2-4, the simulation results for a 16x20 μm device are shown.

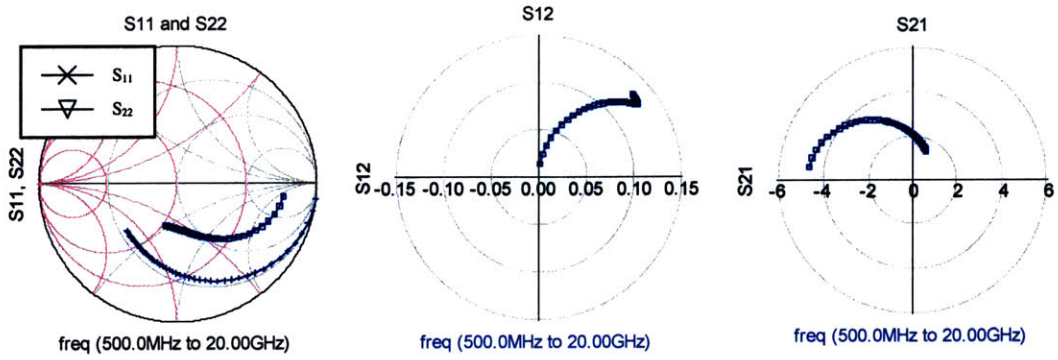

Fig. 3.2-2 Simulated S-parameters for the 16x20 μm device biased at V_{ds}=2 V, V_{gs}=1.4 V

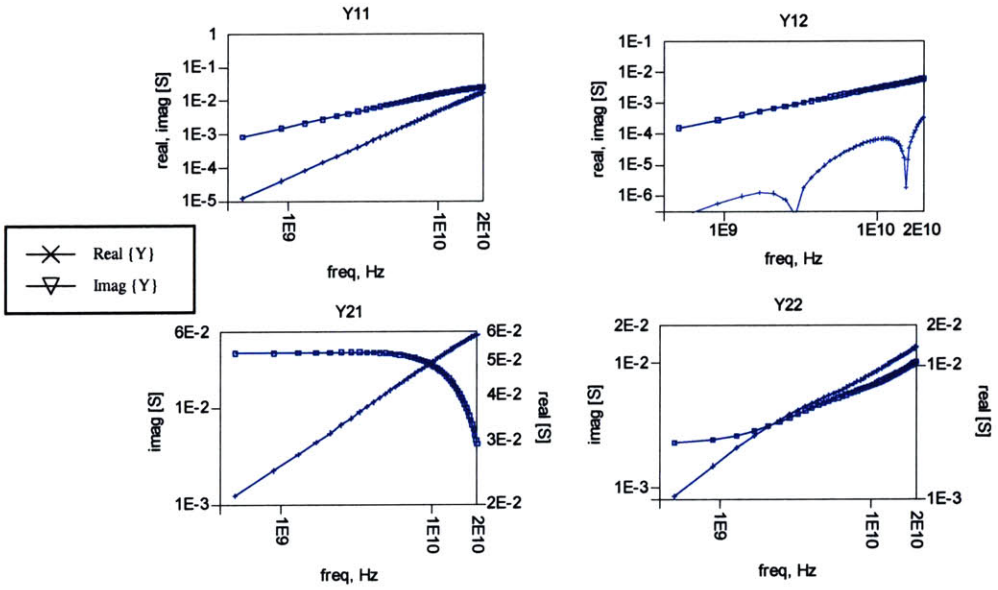

Fig. 3.2-3 Simulated Y-parameters for the 16x20 μm device biased at V_{ds}=2 V, V_{gs}=1.4 V

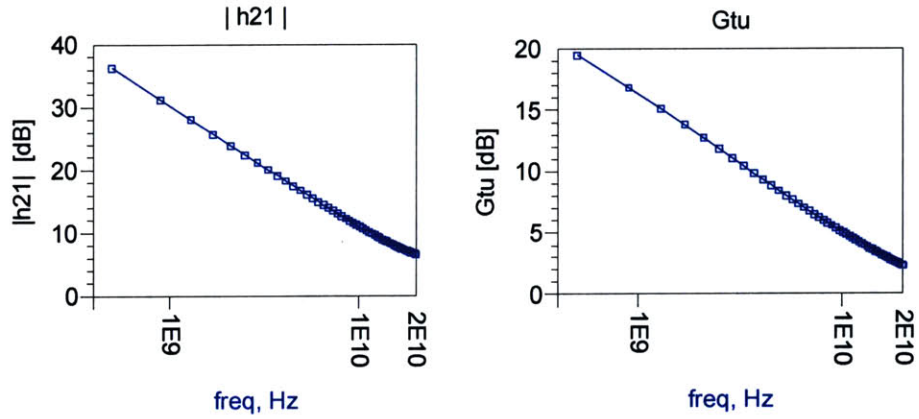

Fig. 3.2-4 Simulated |h21| and G_{tu} for the 16x20 μm device biased at V_{ds}=2 V, V_{gs}=1.4 V

3.3 Power-Sweep

The power sweep setup uses the harmonic-balance simulation component in ADS. The schematic in Fig. 3.3-1 shows the power source, biasing, device and the load impedance. Load and source impedances can be adjusted and are incorporated into the source and load elements. The main structure and equations are already supplied by ADS in the RF power-amplifier design guide, which is a library of simulation setups and result displays. The measured load and source tuner impedances are presented to the device.

An important part of the simulation setup is the de-embedding. While in the S-parameter case the measured data has been de-embedded before comparing it to the simulations, it is done inversely here. The measured large signal data is not de-embedded. To compare it with the device simulations, we have to add in parallel to the intrinsic device the measured Y-parameters of the pad and interconnect parasitics. This can be seen in the schematics in Figs. 3.3-1 and 3.4-1.

In the simulations and power-sweep graphs of Figs. 3.3-2 and 3.4-2, the input power P_{in} refers to the available input power from the source, as described in section 2.5.

In Fig. 3.3-3, the impact of the probe resistance on the P_{in} vs. P_{out} simulation is shown, by sweeping its value between 0.25 and 1.5 Ohm. This range of values was reported for the probe resistance, depending on the quality of contact [21]. We see that the uncertainty introduced by the probe resistance in the P_{out} level is roughly 0.5 dB.

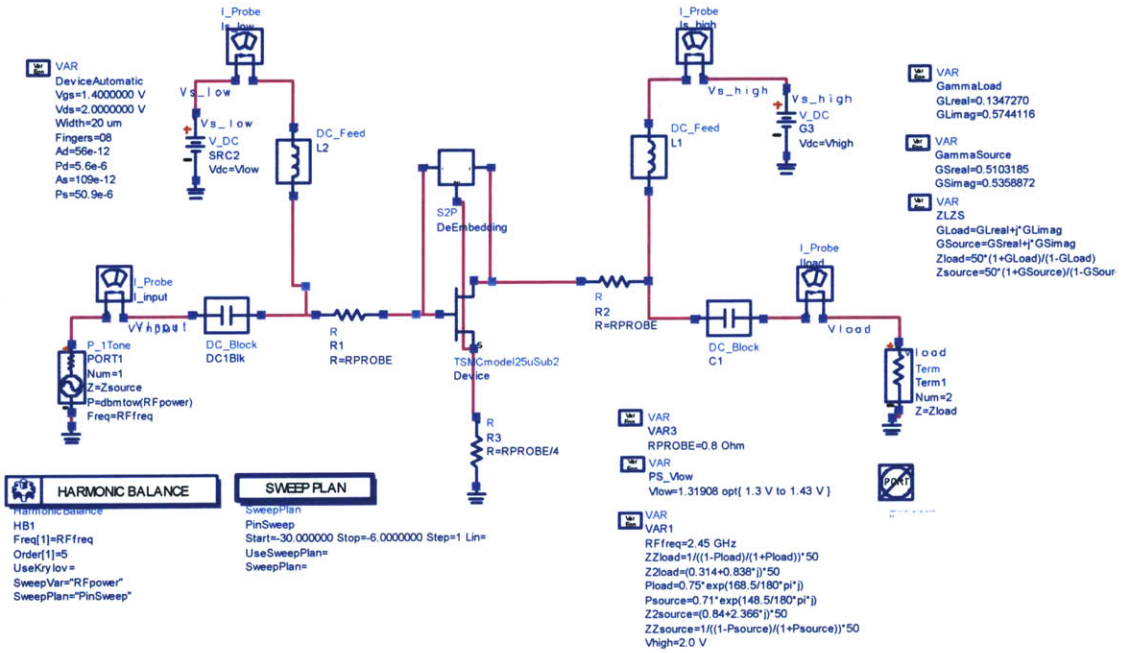

Fig. 3.3-1 Power-Sweep simulation setup

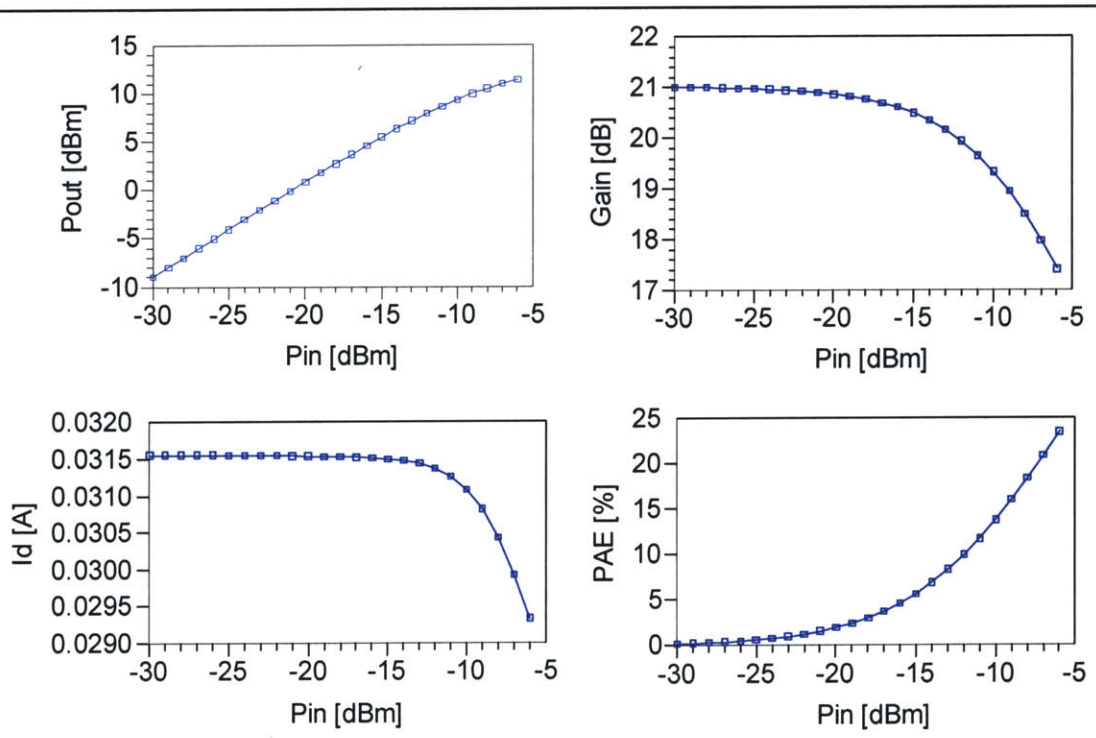

Fig. 3.3-2 Power-sweep simulations using the BSim3 model only, for the 08x20 μm device biased at V_{ds}=2 V, V_{gs}=1.4 V.

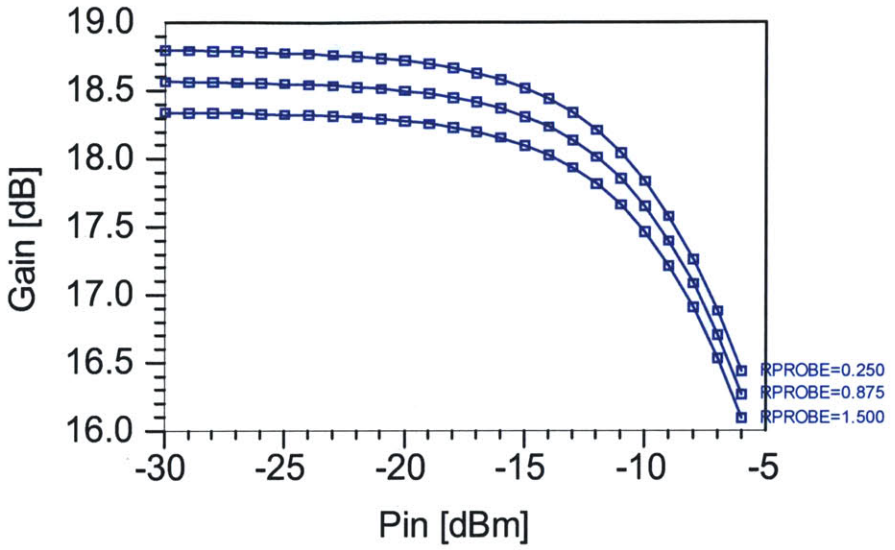

Fig. 3.3-3 Simulated Gain vs. P_{in} for the 08x20 μm device using the modified model, at V_{gs}=1.4 V, V_{ds}=2 V. Shown for three different values of probe resistance. The difference in gain between highest and lowest probe resistance is about 0.5 dB.

3.4 IM_3 Simulations

Fig. 3.4-1 shows the IM_3 simulation setup. It is very similar to the Power-Sweep setup, except that two signals are introduced at the input of the device. The equations for computing IM_3 are supplied in the ADS RF-PA design guide. As described in section 2.4, two different types of units are often used with IM_3, dBm and dBc. To convert the IM_3 [dBm] to IM_3 [dBc], the fundamental output power is subtracted from the output power of the IM_3 tone.

Again, the issue of input power definition is important. In this schematic, *RFpower* is the available input power of both tones combined, resulting in an individual tone available power of *RFpower-3dB*. In the results graphs, the total available input power P_{in} equals *RFpower*.

Although the measurements did not record the output power of the fundamental tones, we can compute them from the IM_3 [dBm] and IM_3 [dBc] data. We can extract the output power of each tone, by subtracting IM_3 [dBm] from IM_3 [dBc].

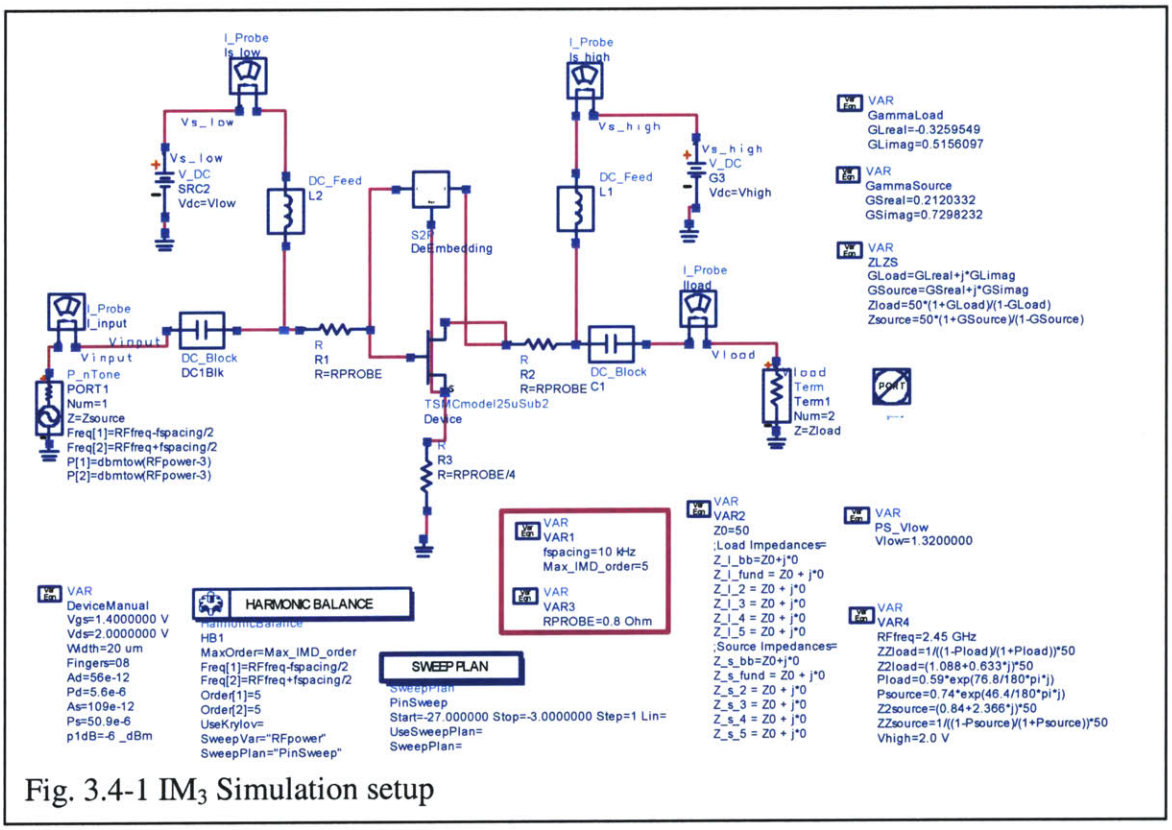

Fig. 3.4-1 IM_3 Simulation setup

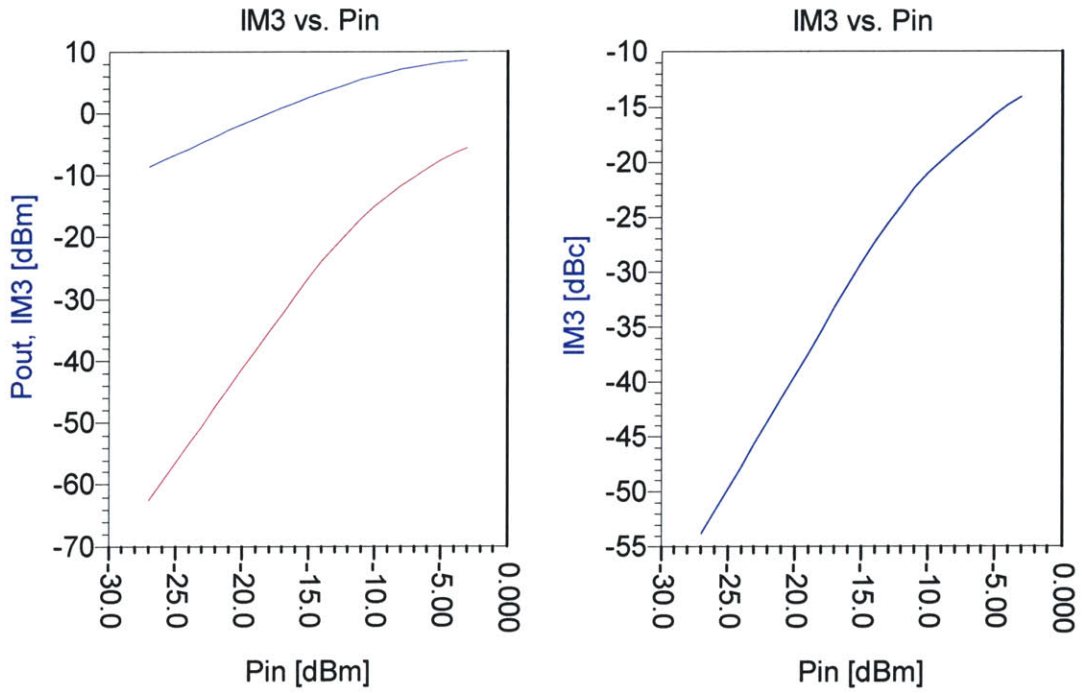

Fig. 3.4-2 IM_3 Simulation versus total available power, for the 08x20 μm device biased at V_{ds}=2 V, V_{gs}=1.4 V. The left graph shows IM_3 (bottom) and the output power (top) both in units of dBm. The right graph shows IM_3 in units of dBc.

3.5. Summary

The simulation setups have been described, showing both the simulation schematics in ADS as well as sample simulations obtained by using the BSim3v3 model. The simulations consisted of DC, S-parameter, and large signal simulations. The large signal simulations have to be broken up into 1-tone and 2-tone simulations. The latter is used to simulate the IM_3 behavior, while the 1-tone measurement gives P_{out}, Gain, I_d and PAE vs. P_{in}.

Chapter 4

Results: Comparison of Measurements and Simulations

This chapter compares the measurements with the simulations. First only the BSim3v3 model for the device is used. Then we build a new model that gives more accurate small and large signal simulations. A comparison of the final model with measured data concludes this chapter.

4.1 Intrinsic BSim Model

We will compare the DC, S-Parameter, and large signal simulations as predicted by the BSim3v3 model to the measurements. Figs. 4.1-1 to 4.1-5 show the DC characteristics of the 16x10 μm device.

We can see that the output characteristics in Fig. 4.1-1 are well matched for low V_{gs}, yet for higher V_{gs} the model does not predict the flattening of I_d that is probably due to self-heating. This can also be seen in the output conductance in Fig. 4.1-2. It would be nice to be able to take self-heating into account, however the transistor models in ADS do not support it currently.

Looking at the transfer characteristics in Fig. 4.1-3, we see that again for low V_{ds} the match is very good, while for higher V_{gs} the model overestimates the current slightly. The threshold voltage is modeled reasonably accurate. A clearer view is possible through the

transconductance plot in Fig. 4.1-4. Here, we can see that g_m is predicted correctly in shape, with a slight mismatch at high V_{ds}. Lastly, Fig. 4.1-5 shows the subthreshold characteristics. Overall, the match is good here, too, indicating that the short channel effects are modeled well.

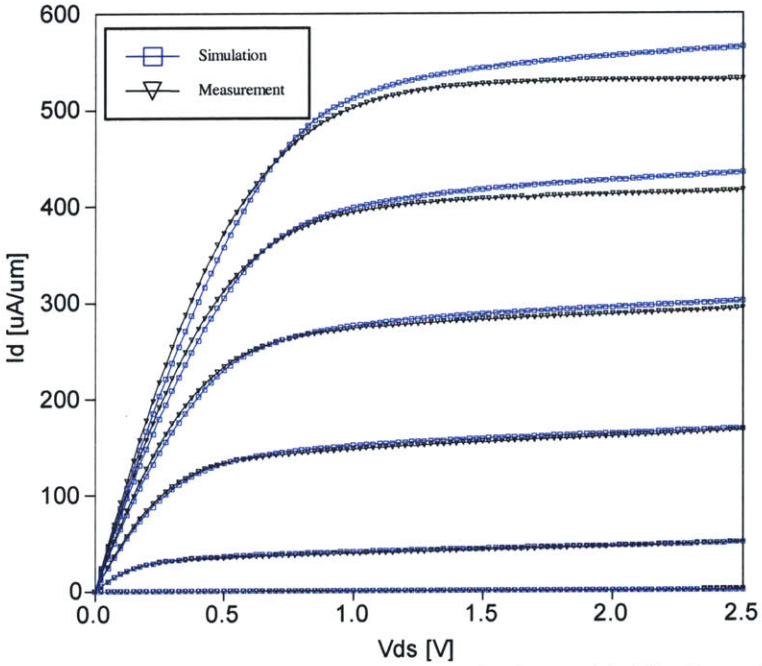

Fig. 4.1-1 Output Characteristics of the 16x10 μm device, with V_{gs} from 0 to 2.4 V in 0.4 V steps.

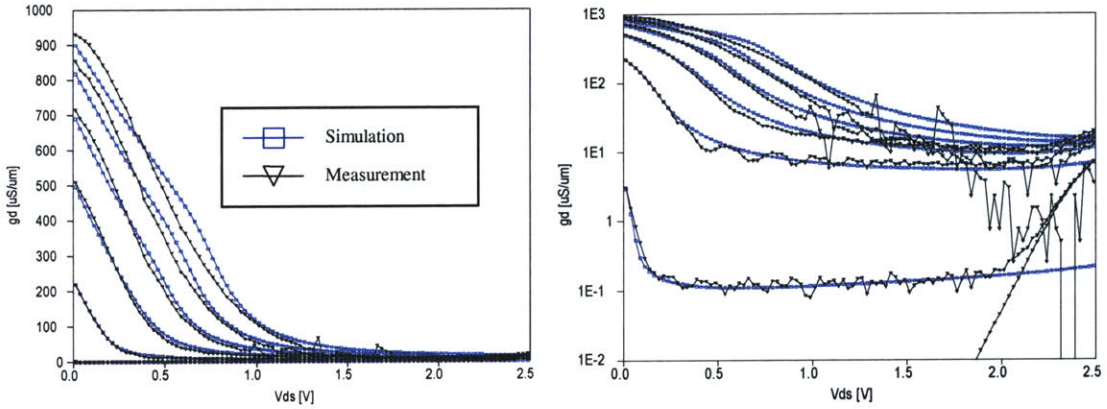

Fig. 4.1-2 Output Conductance for the 16x10 μm device, with V_{gs} from 0 to 2.4 V in 0.4 V steps. Left: linear scale, right: semi-log scale.

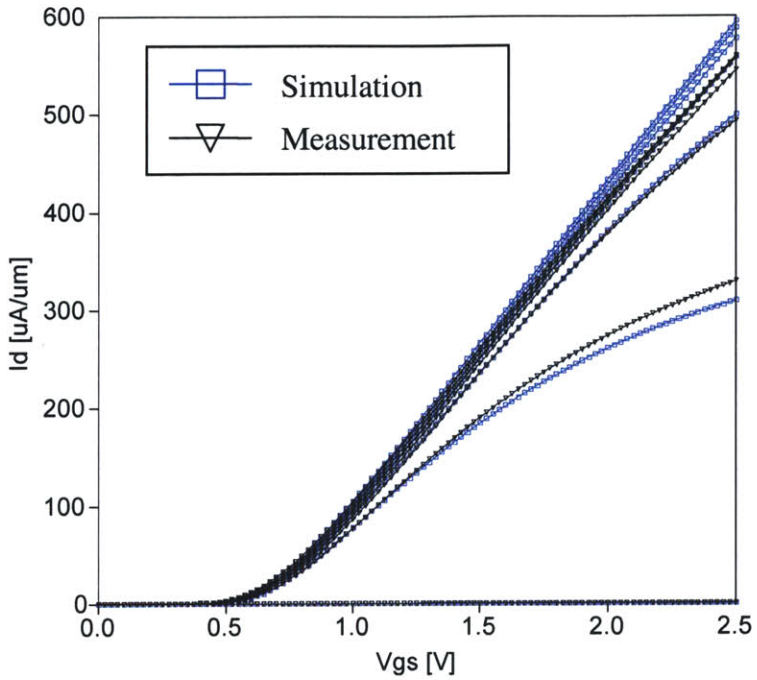

Fig. 4.1-3 Transfer Characteristics of the 16x10 μm device, with V_{ds} from 0 to 2.4 V in 0.4 V steps.

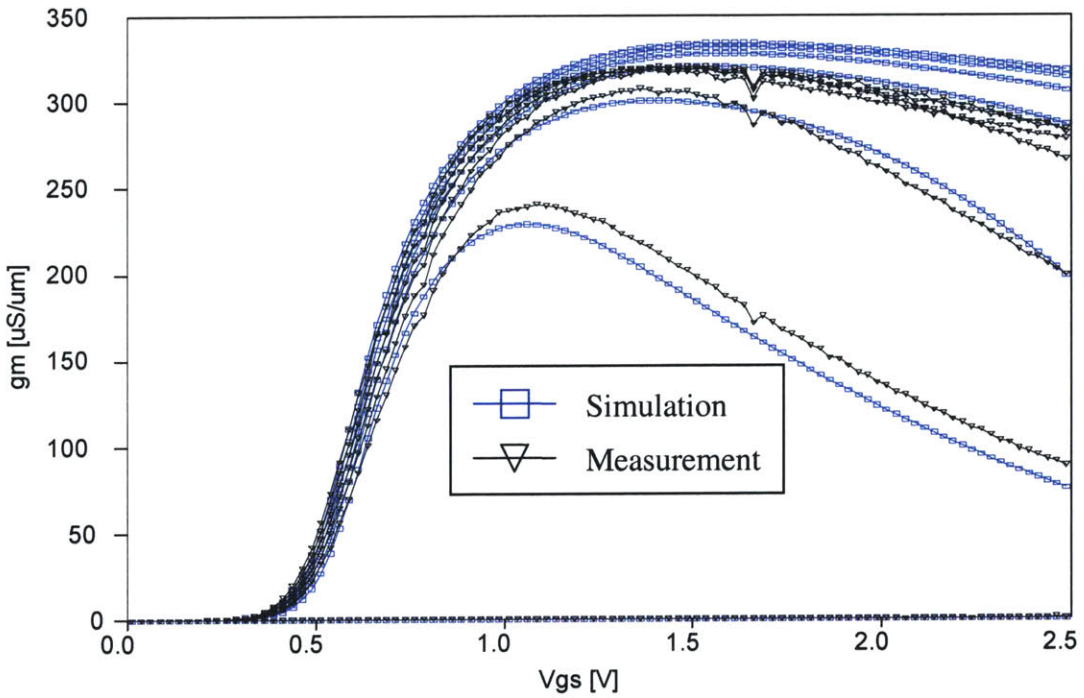

Fig. 4.1-4 Transconductance of the 16x10 μm device, with V_{ds} from 0 to 2.4 V in 0.4 V steps.

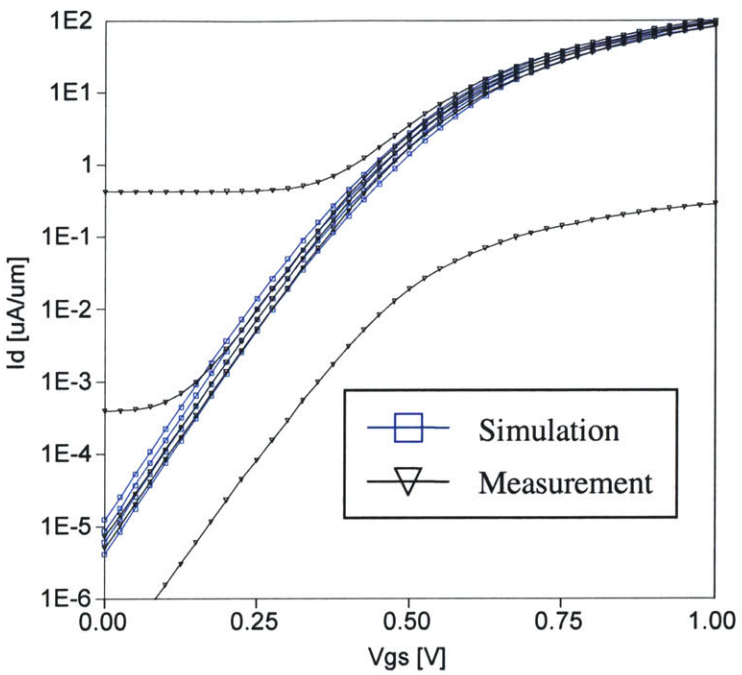

Fig. 4.1-5 Subthreshold characteristics of the 16x10 μm device, with V_{ds} from 0 to 2.4 V in 0.6 V steps. The lowest measurement line is for Vds=0 V, the simulations yield 0 A current here, so they are not shown.

Altogether, the DC characteristics are well captured by the intrinsic BSim3v3 model, so that there will be no need to append or modify the DC model.

Figures 4.1-6 to 4.1-8 show a comparison of AC simulations and measurements of the 16x20 μm device. Fig. 4.1-6 shows the S-parameter comparison. Both S_{11} and S_{22} are significantly off from the measurements. S_{12} and S_{21} are also not matching well with the measurements. Overall, the S-parameter simulations are not particularly accurate. Similarly, the Y-parameters in Fig. 4.1-7 also show significant discrepancies between the measured and BSim3v3 model. Finally, in Fig. 4.1-8, the model predicts $|h_{21}|$ well, although above 10 GHz the shapes diverge. G_{tu} is not well modeled, being several dB above the measurement.

The missing accuracy of the S-parameter simulations will directly translate into an impedance mismatch during the large signal measurements. This is because these simulations are done with identical load and source impedances as in the measurements, yet the reflection coefficients that the simulated device presents are different from those of the measured device. Thus the simulations will have an impedance mismatch. The results of the power sweep simulations compared to measurements are shown in Fig. 4.1-9. The simulations include the BSim3v3 model and, in parallel, the pad measurements as described in Chapter 3. Fig. 4.1-10 shows the IM_3 BSim3v3 simulation and measurement comparison. The BSim3v3 models IM_3 almost 30 dBc below the measurement value.

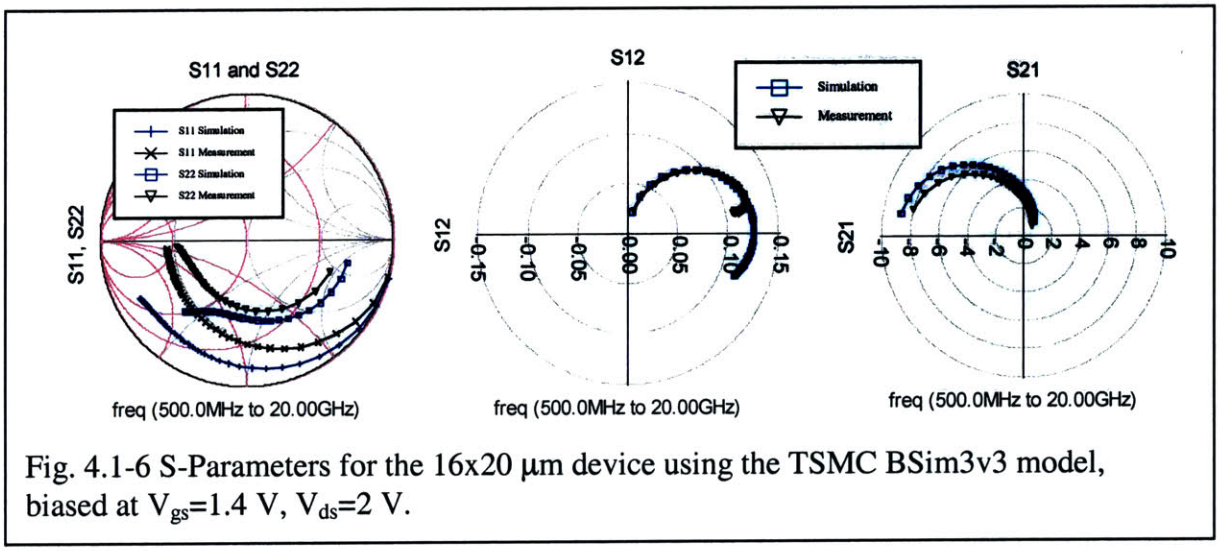

Fig. 4.1-6 S-Parameters for the 16x20 μm device using the TSMC BSim3v3 model, biased at V_{gs}=1.4 V, V_{ds}=2 V.

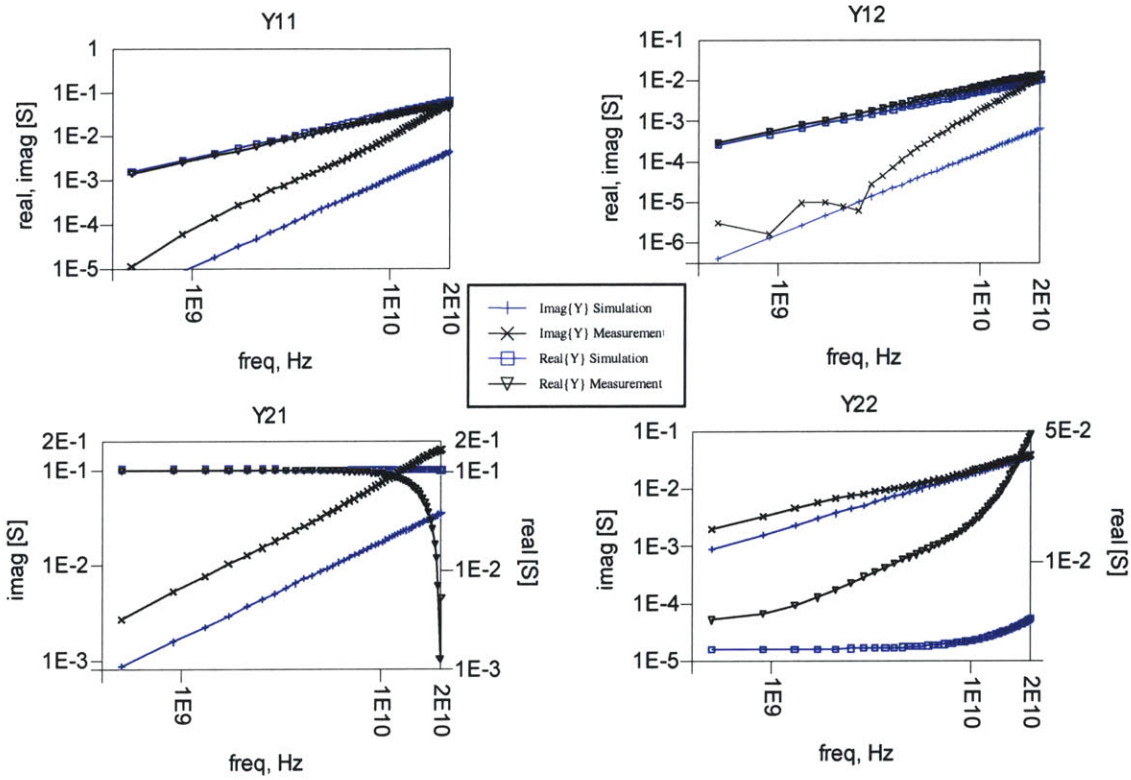

Fig. 4.1-7 Y-Parameters for the 16x20 μm device using the TSMC BSim3v3 model, biased at V_{gs}=1.4 V, V_{ds}=2 V.

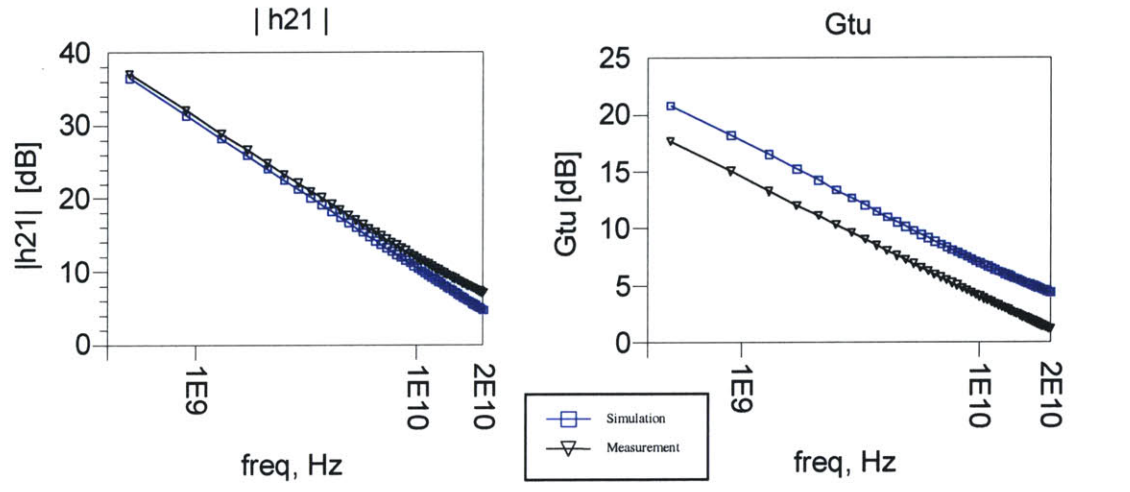

Fig. 4.1-8 Figures of merit $|h_{21}|$ and G_{tu} for the 16x20 μm device using the TSMC BSim3v3 model, biased at V_{gs}=1.4 V, V_{ds}=2 V.

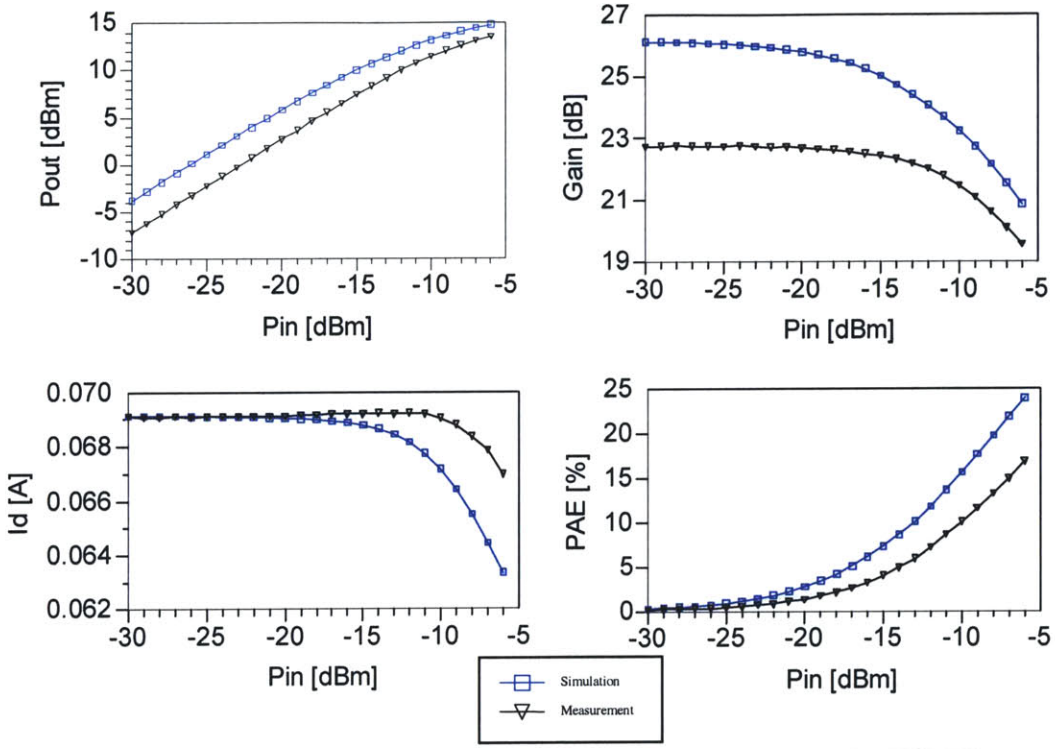

Fig. 4.1-9 Power sweep simulations for the 16x20 μm device using the TSMC BSim3v3 model, at V_{gs}=1.4 V, V_{ds}=2 V.

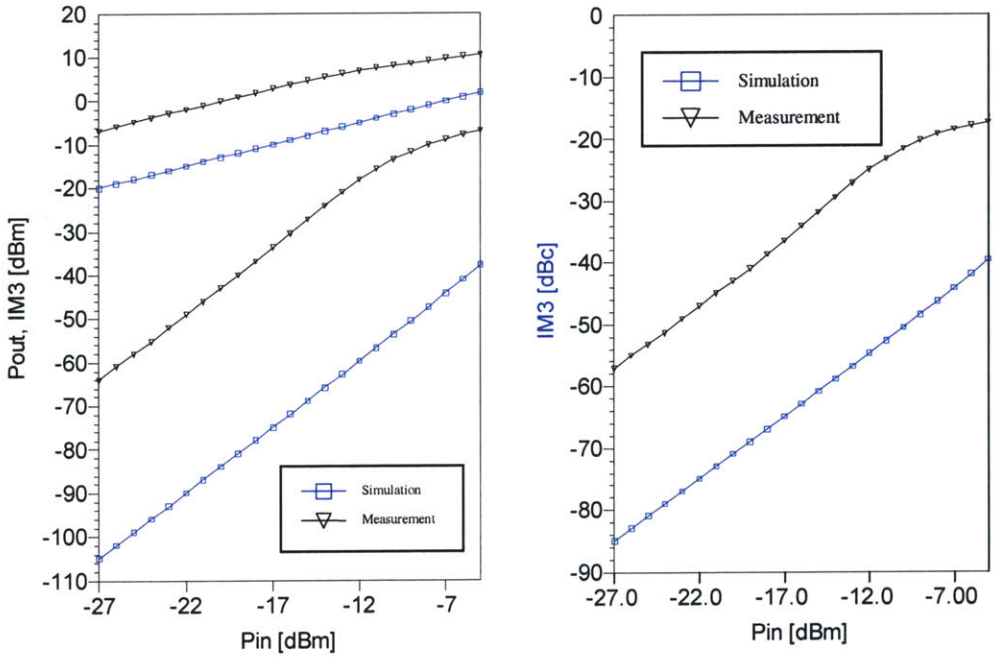

Fig. 4.1-10 IM_3 simulations for the 16x20 μm device using the TSMC BSim3v3 model, at V_{gs}=1.4 V, V_{ds}=2 V. Left: P_{out} (top) and IM_3 [dBm]. Right: IM_3 [dBc]

4.2. Modifying the BSim Model

In order to get a more accurate large signal fit, the first step is to match the small signal AC characteristics. The S-parameters were measured with an input power of about -30 dBm, which is equivalent to the lower input power of the power-sweeps (the load and source impedances are 50 Ohm in the S-parameter case). A good fit for the S-parameters should therefore lead to improved large signal simulations, for low input powers at least.

Appendix A shows the S- and Y-parameters of the simulations as each of the model parameters is swept up- and down from its optimal point in the final model. Following this helps to understand the impact of the model parameters on the device behavior.

Starting with the S- and Y-parameter plots from Figs. 4.1-6 and 4.1-7, we will add elements first that only influence one curve of the S- or Y-parameters.

4.2.1. Output Resistance

The real part of Y_{22} (from hereon denoted as Real[Y22]) at low frequency is the DC output resistance of the device. Fig. 4.2.1-1 shows Y_{22}, and we can see a mismatch of Real[Y22] at low frequency. The simulation shows too high an output resistance. To correct this, a resistor is added in-between the drain and source. The value of the resistor is determined such as to match only the very lowest frequency parts of Real[Y22]. This is because the shape at higher frequencies is influenced by other elements in the device.

Because the resistor is added in parallel between the drain and source, it will only influence Real[Y22]. A negligible change will occur in Y21, the other Y-parameters are not affected.

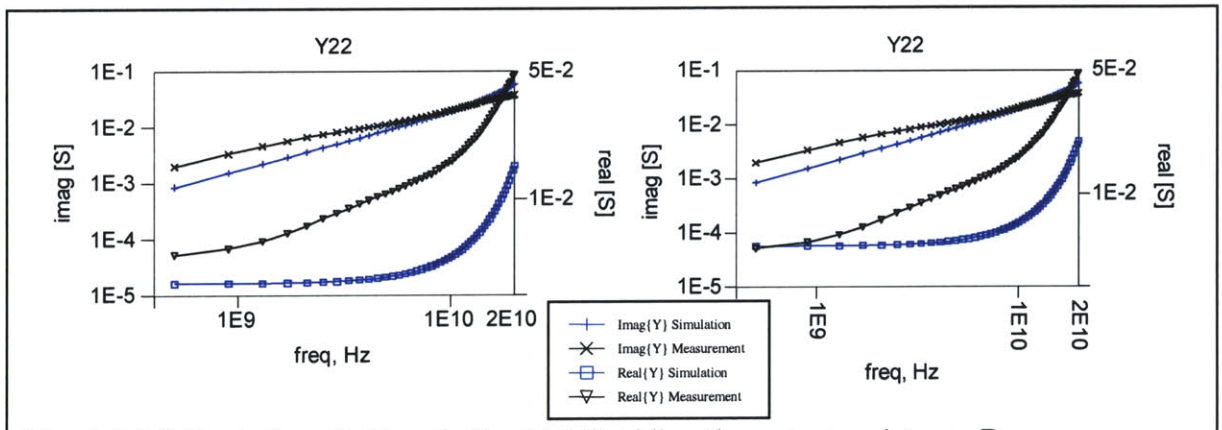

Fig. 4.2.1-1 Y_{22} before (left) and after (right) adding the output resistance R_{out}.

4.2.2. Gate Resistance

In the TSMC BSim3v3 model, the gate resistance model parameter is set to zero. While the gate resistance is negligible for very narrow devices, RF power devices have very wide fingers and thus the gate resistance will be an important parameter [4-7,9,10]. In the

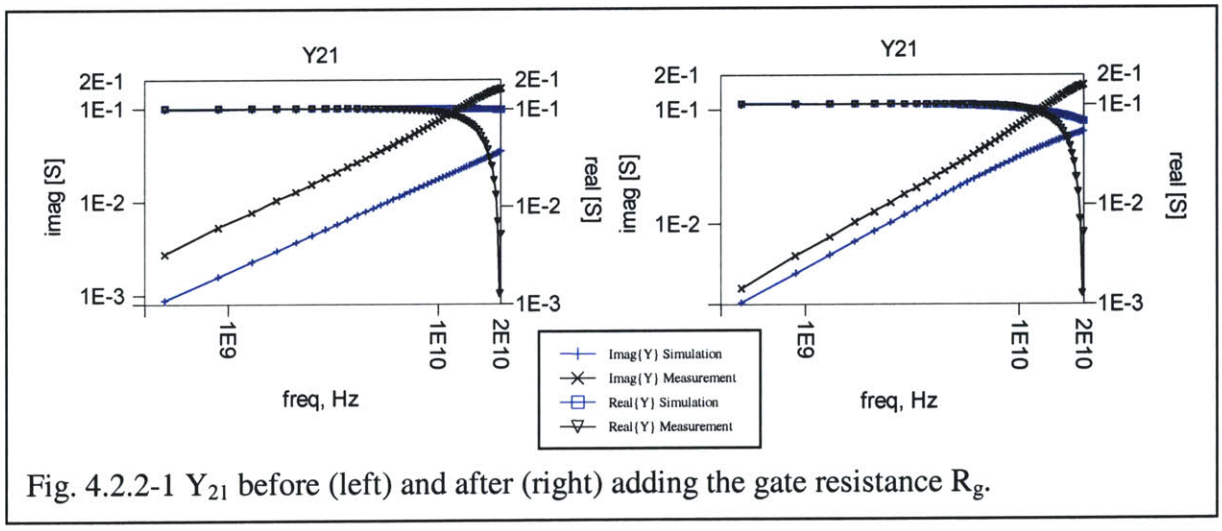

Fig. 4.2.2-1 Y_{21} before (left) and after (right) adding the gate resistance R_g.

S-parameters, the gate resistance primarily affects S_{11} by reducing the radius of the circle that S_{11} typically traces. Alternatively, its impact can be seen in Y_{21}, where the gate resistance causes Real[Y21] to bend. Fig. 4.2.2-1 illustrates this. Furthermore, while the gate resistance does not have an impact on $|h_{21}|$, it reduces G_{tu}. This eliminates some of the excess gain of the simulations.

4.2.3. Gate, Source, and Drain Inductances

While the simulations now give a reasonable fit at low frequencies, we can see several changes of sign in the measured Y-parameters, most prominently in Imag[Y21] as shown in Fig. 4.2.3-1. These do not occur in the simulations. They can be explained by the presence of parasitic inductances in the gate, source, and drain. When adding the inductances to the model, the sign changes are now modeled correctly. The reason that Real[Y21] is also matched, even though we do not see a sign change, is that there is a sign change in Real[Y21] which occurs at higher frequencies above the 20 GHz that the graph shows.

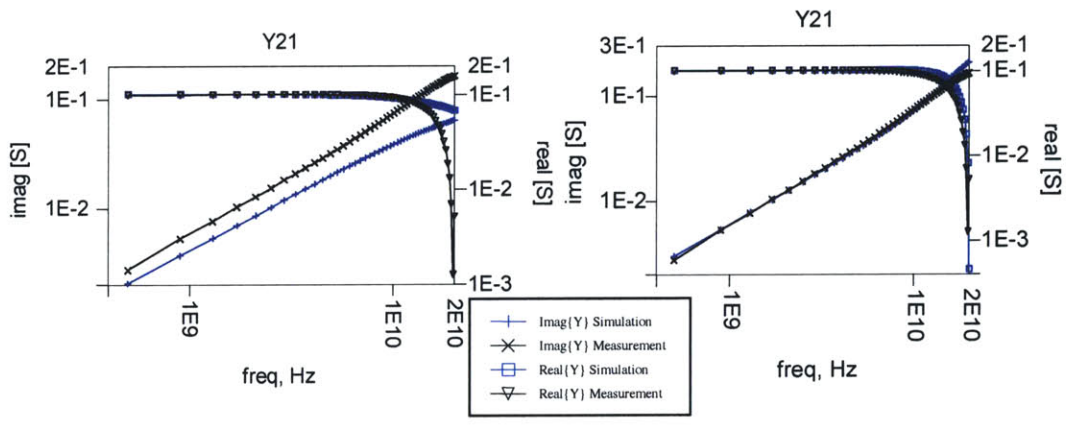

Fig. 4.2.3-1 Y_{21} before (left) and after (right) adding the inductances in the gate, source and drain.

4.2.4. Body Resistance

The importance of the substrate network has been discussed in various papers [8,9] as having an impact on the S-parameter and large signal characteristics. For our model, a simple resistance between the body and source appears sufficient to capture the substrate effects. This is equivalent to the model in [7,8] and the reduced version of the model proposed in [4]. The best way to observe the effect of the body resistance is by looking at Real[Y22] as shown in Fig. 4.2.4-1. Adding the resistance allows the curves to match. In the simplified small signal model, shown in Fig. 4.2.4-2, the body resistance results in an RC-network consisting of a parallel R_b-C_{sb} in series with C_{db}. This network is between the drain and source node, in parallel with the intrinsic device, which explains why its primary impact is on Y_{22}. However, through the backgate transconductance generator g_{mb}, R_b also affects Y_{21}.

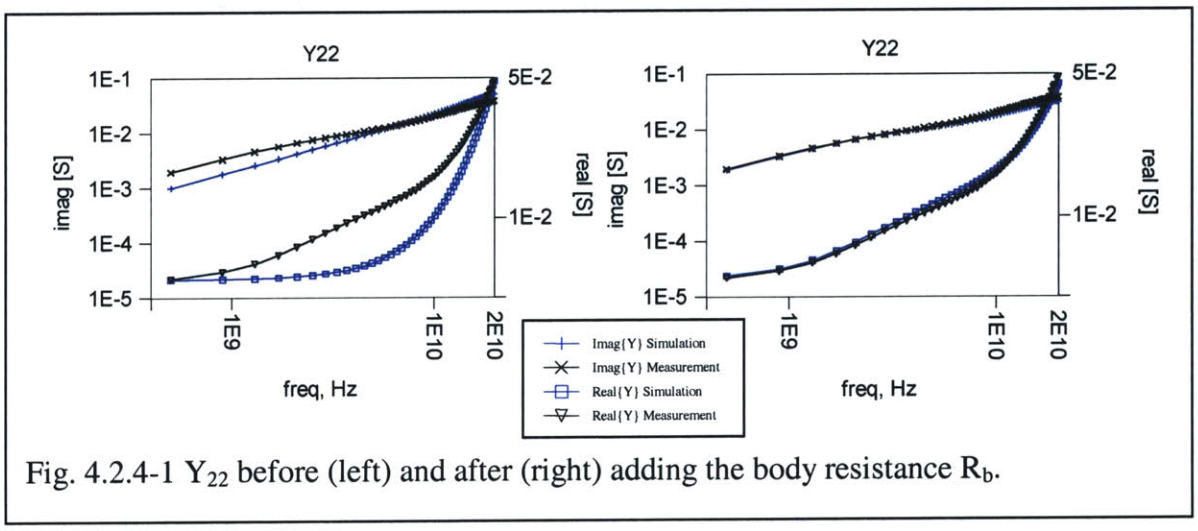

Fig. 4.2.4-1 Y_{22} before (left) and after (right) adding the body resistance R_b.

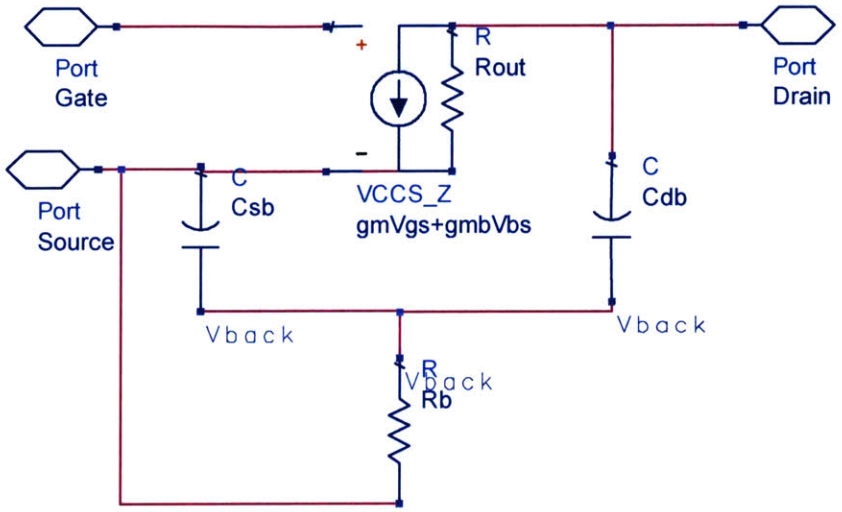

Fig. 4.2.4-2 Simplified small-signal model illustrating the effect of the body resistance, R_b. Without R_b, there is only a capacitor between the drain and source. With R_b in place, there now is an RC network between the two ports, giving rise to the observed changes in Y_{22}.

4.2.5. Gate-to-Drain Capacitance

Having now a very accurate model, we can as a final step add a small capacitor between the gate and drain. The effect can be best seen in S_{12}. The $C_{gd\text{-}ext}$ helps to move S_{12} out, matching it closer to the measured results, as seen in Fig. 4.2.5-1.

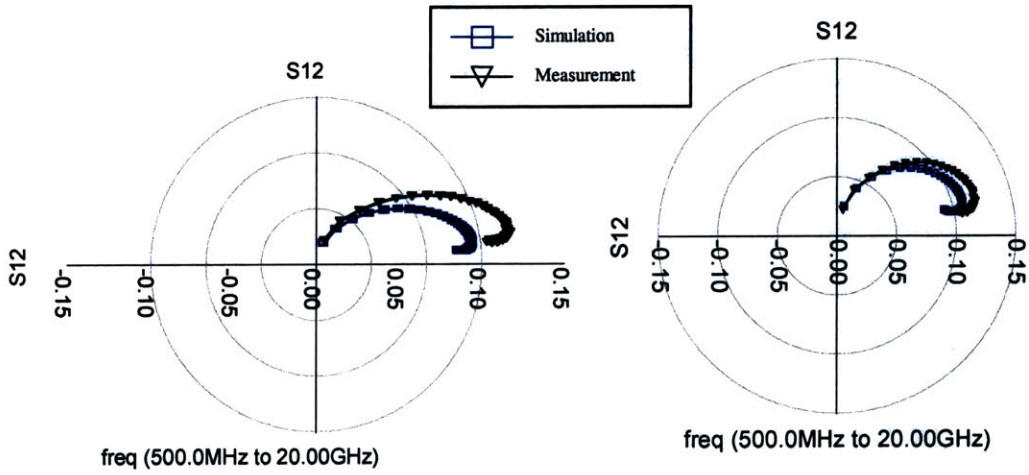

Fig. 4.2.5-1 S_{12} before (left) and after (right) adding the gate to drain capacitance $C_{gd\text{-}ext}$.

4.2.6. Small Signal Comparison of the Complete Model

The complete model is shown in Fig. 4.2.6-1. Comparisons of the measured and simulated S-parameters for the 16x20 μm device using the improved model are shown in Fig. 4.2.6-2. The fit is good, with a small discrepancy in S_{11} and S_{12} at frequencies approaching 20 GHz. The Y-parameters are compared in Fig. 4.2.6-3, and show very good agreement throughout the frequency range. The mismatch is below 10% for most of the Y-parameter curves. Lastly, Fig. 4.2.6-4 shows the figures of merit $|h_{21}|$ and G_{tu}, with very good agreement, although $|h_{21}|$ is a little bit too low in the simulations. This is due to a slight overestimation of Imag[Y11] of 20% in the model, as can be seen in Fig. 4.2.6-3. This 20% overestimation results in the simulated $|h_{21}|$ being lowered by 1.6 dB, which is

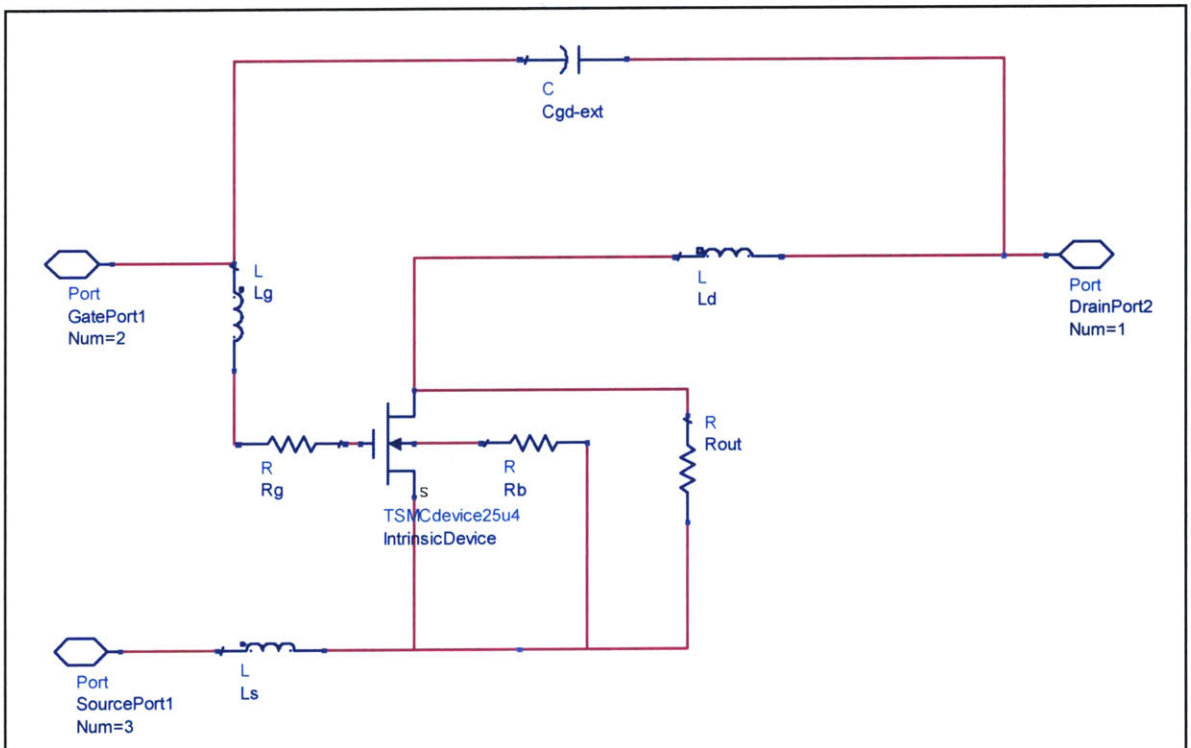

Fig. 4.2.6-1 Modified BSim3v3 model topology to take RF effects into account

the discrepancy of $|h_{21}|$ we observed in Fig. 4.2.6-4.

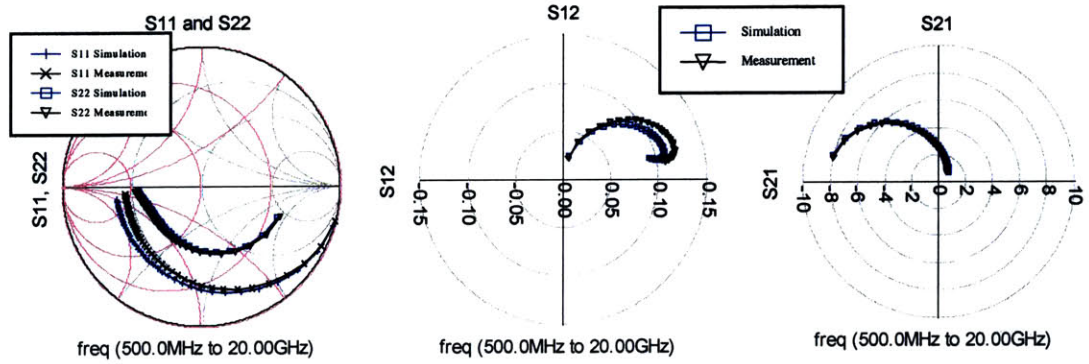

Fig. 4.2.6-2 S-Parameters for the 16x20 μm device using the modified model, biased at V_{gs}=1.4 V, V_{ds}=2 V.

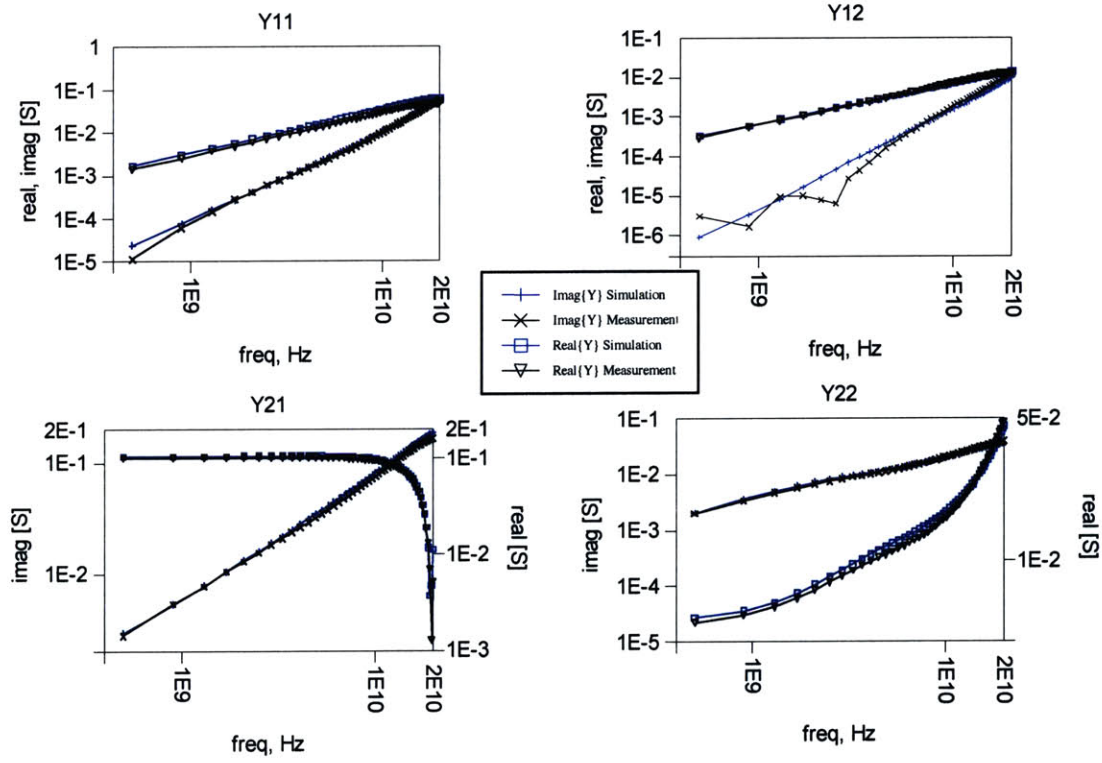

Fig. 4.2.6-3 Y-Parameters for the 16x20 μm device using the modified model, biased at V_{gs}=1.4 V, V_{ds}=2 V.

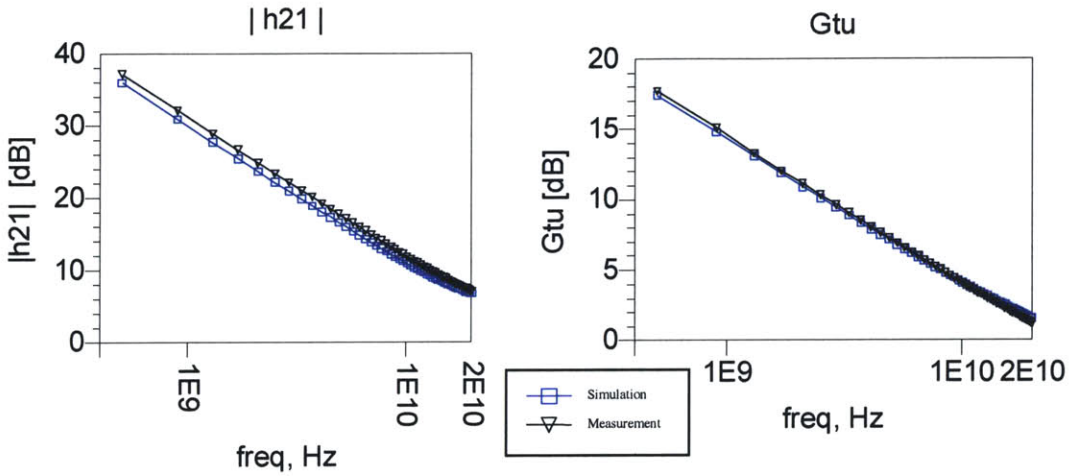

Fig. 4.2.6-4 Figures of merit $|h_{21}|$ and G_{tu} for the 16x20 μm device using the TSMC BSim3v3 model, biased at V_{gs}=1.4 V, V_{ds}=2 V.

4.3. Large Signal Comparison of Complete Model

Having built a model that accurately models the S-parameters, we will now test it against the large signal measurements. There are six devices, 08x20 μm, 16x05 μm, 16x20 μm, 16x40 μm, 32x10 μm and 64x05 μm, for which power sweeps were performed measuring P_{out}, gain, drain current, PAE, and IM_3 as a function of available power (P_{in}). After deriving the proposed model additions for each of these devices, S-parameter, and power sweep results were compared. All devices showed an equal accuracy in modeling the measurements, so we will only present the results of the 16x20 μm device here.

Figs. 4.3-2 shows the output power vs. input power for the measured device and the model. The model accurately predicts the magnitude and shape of the measurements. Looking at the Gain vs. P_{in} in Fig. 4.3-2 allows to see the model's accuracy more easily then in the P_{out} vs. P_{in} graph.

The low input power current should be identical for the measurements and simulations, as discussed in 3.2. This is achieved by changing the gate voltage to compensate for small threshold voltage mispredictions of the BSim3v3 model. The results of the drain current as a function of P_{in} are shown in the third graph of Fig. 4.3-2. The current, together with the P_{in}-P_{out} graph, will determine the power added efficiency, PAE. The results, the last graph of Fig. 4.3-2, show a very good agreement between measurements and simulation.

Fig. 4.3-3 shows IM_3 and P_{out} in dBm, and IM_3 in dBc as a function of input power. The 30 dBc discrepancy seen in section 4.1 has been eliminated, and the simulated IM_3 and P_{out} curves now track the measurements very closely. Important for the IM_3 match is to have an accurate match of P_{out}. Because IM_3[dBc] equals the difference of IM_3[dBm] and P_{out}, any mismatch in P_{out} is exactly transferred into the IM_3[dBc] curve.

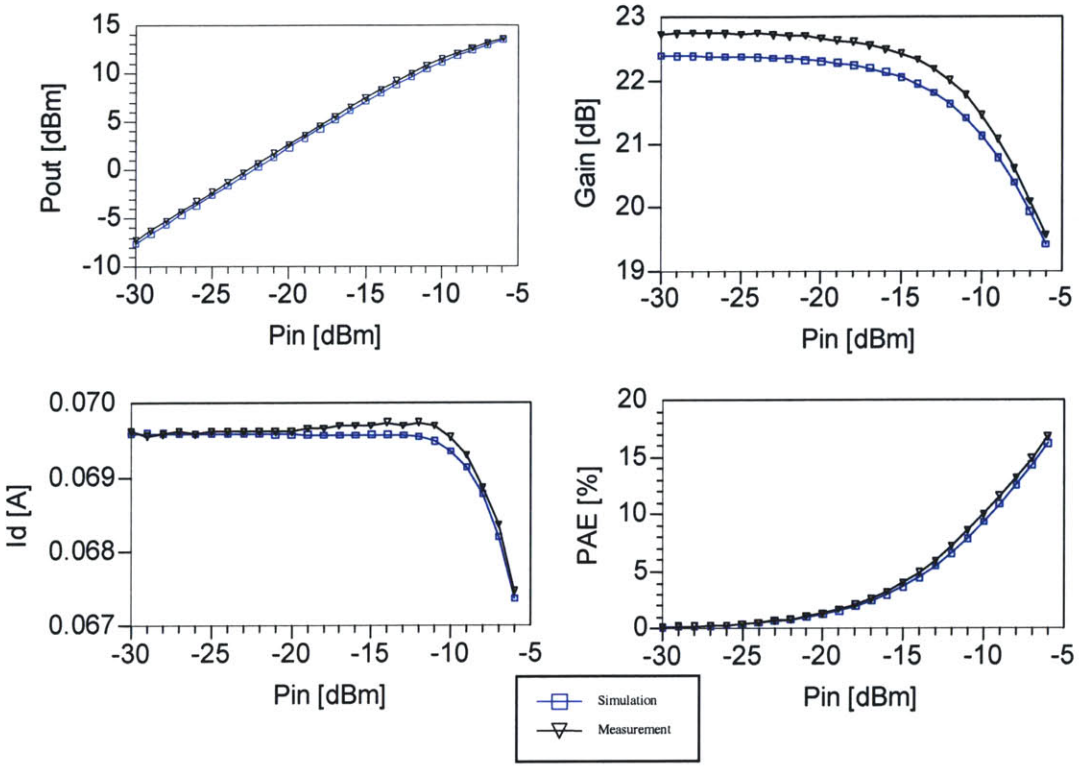

Fig. 4.3-2 Power sweep simulations and measurements for the 16x20 μm device using the modified model, at V_{gs}=1.4 V, V_{ds}=2 V.

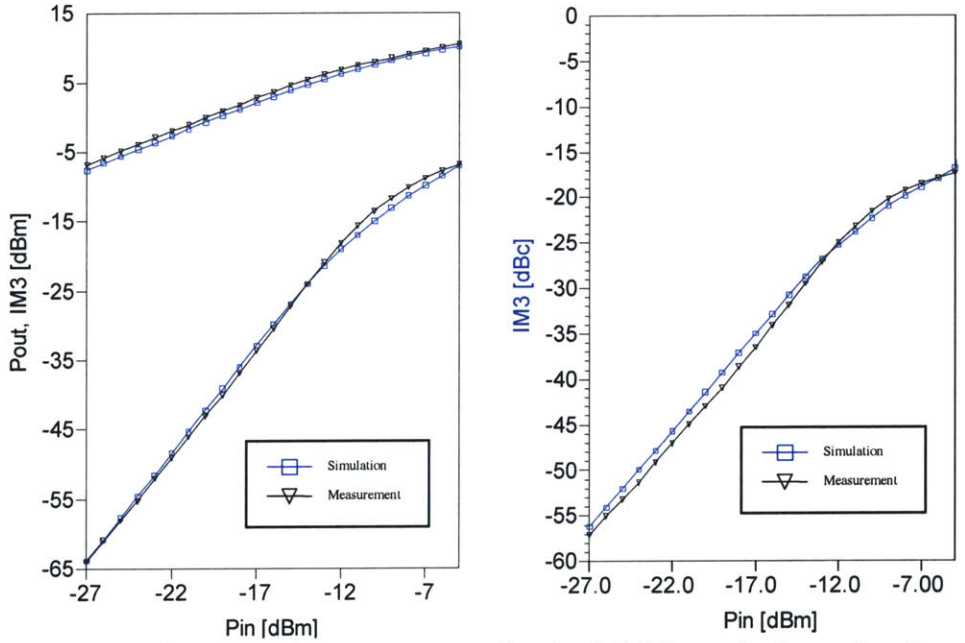

Fig. 4.3-3 IM_3 simulations and measurements for the 16x20 μm device using the modified model, at V_{gs}=1.4 V, V_{ds}=2 V. Left: P_{out} (top) and IM_3 [dBm]. Right: IM_3 [dBc]

4.4 Summary

We have compared the measurements with the BSim3v3 model and noted a significant discrepancy between the S-parameter and large signal simulations and measurements. A new model has been derived based on the BSim3v3 model that includes the six new elements, by only using S-parameter measurements. The new model was then compared against the S-parameter and large signal measurements. It showed a significant improvement, giving a good match to the S- and Y-parameters and all important power-sweep figures, including the linearity figure IM_3.

Chapter 5

Relation of New Model Parameters to Device Design

Having shown the capability of the model in Chapter 4, we will now take a closer look at the extracted model parameter values for the new elements that have been added to the device equivalent circuit model. We will examine these parameters in different devices. We will investigate in particular the impact of the number of gate fingers, the unit finger width and the total width of the device.

5.1 Output Resistance, R_{out}

The output resistance parameter is a fitting parameter that appears to simply compensate for the overestimation of R_{out} in the intrinsic BSim3v3 model. The dependence of Rout on unit finger width and number of fingers is shown in Fig. 5.1-1. It is inversely proportional to the total device width, as can be seen in Fig. 5.1-2.

At RF, the BSim3v3 model *overestimates* the output resistance (as seen in section 4.2.1 and Fig. 4.2.1-1.). Looking at the DC comparison in 4.1, Fig. 4.1-2 shows that R_{out} is lower for the BSim3v3 model, thus at DC, the model *underestimates* the output resistance. The model, which does not include self-heating effects, lies between the DC and the RF measured output resistance. The fact that the DC and RF measured output resistance is different is not a contradiction! Fig. 5.1-3 illustrates a zoom of the output characteristics around the DC bias point. If we were to increase V_{ds} by ΔV_{sweep}, in the DC

case, we would move along the solid curve. The increase in V_{ds} increases the power and thus temperature, which leads to more self-heating a smaller increase in current. If instead we now have an RF sweep, the additional current for the same ΔV_{sweep} is higher, because the temperature of the device does not increase during the short RF sweep. This is similar to a pulse measurement.

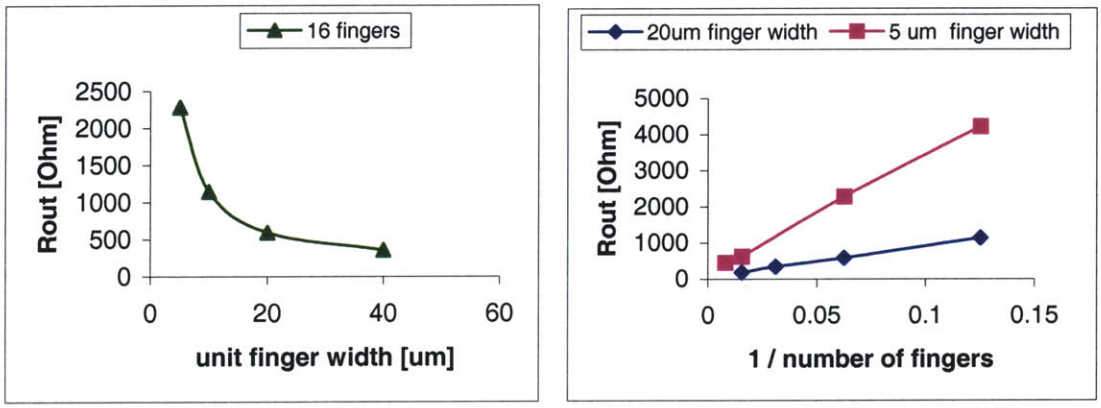

Fig. 5.1-1 R_{out} as a function of unit width (left) and number of fingers (right).

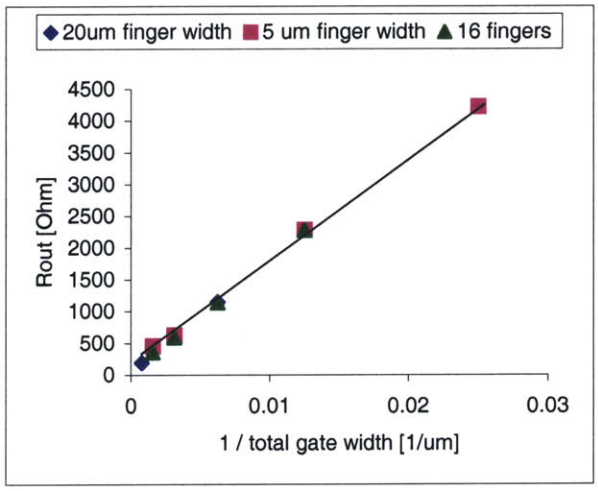

Fig. 5.1-2 R_{out} as a function of total device width.

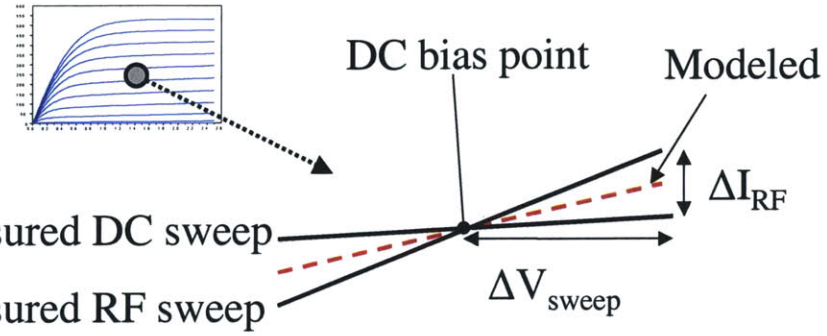

Fig. 5.1-3 Output characteristic around the DC bias point for the output resistance measurement under RF and DC conditions

5.2. Gate Resistance, R_g

We would expect the gate resistance to be proportional to the ratio of finger width and number of fingers. Shorter fingers result in a shorter gate and thus less resistance, which makes R_g proportional to the unit finger width. Fingers in parallel result in gate resistors in parallel, thus R_g is inversely proportional to the number of fingers.

In addition to this, we also expect a small constant resistance in series with the finger resistance. It consists of two parts: device layout independent via resistance that results from routing from *metal4* to *metal2*. The second part will be the resistance from the *metal2* layer to the gate finger. It includes the contact resistance between metal 2 and poly and the poly resistance up to the edge of the gate finger. This resistance ought to be inversely proportional to the number of fingers, since for every two gate fingers there is one contact, and more fingers means more resistors in parallel. Hence, we expect that:

$$R_g = R_{via} + R_{const}\frac{1}{n_f} + R_{g0}\frac{w_g}{n_f} \qquad \text{[Eq. 5.2-1]}$$

R_{via} and R_{const} are in units of Ohm. The resistance of the gate finger, R_{g0}, has units of Ohm/length. We expect $R_{g0}\frac{w_g}{n_f}$ to be the dominating term in Eq. 5.2-1, as long as the ratio of w_g and n_f does not become too small. In Fig. 5.2-2, the Rg is plotted against the w_g/n_f ratio. We can see a constant slope of one for the data, indicating that indeed the $R_{g0}\frac{w_g}{n_f}$ term is the dominating one in Eq 5.2-1.

Keeping in mind that the probe resistance can be as high as 1.2 Ohm, and that the simulations used a probe resistance of 0.8 Ohm, the value of R_g has an uncertainty due to the probe resistance of about 0.4 Ohm. In addition, for small values of R_g, the impact of R_g on the S- and Y-parameters is less significant, making it difficult to find the exact value by optimizing.

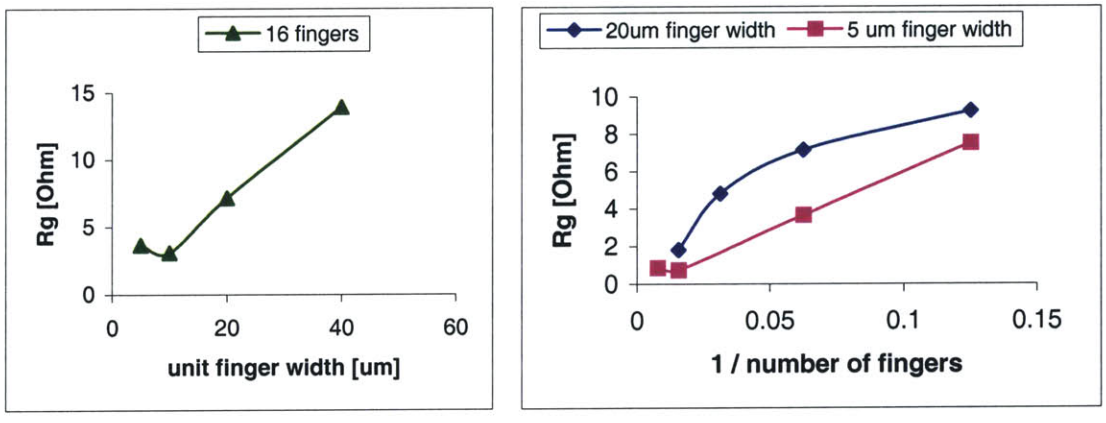

Fig.5.2-1 R_g as a function of unit width (left) and number of fingers (right)

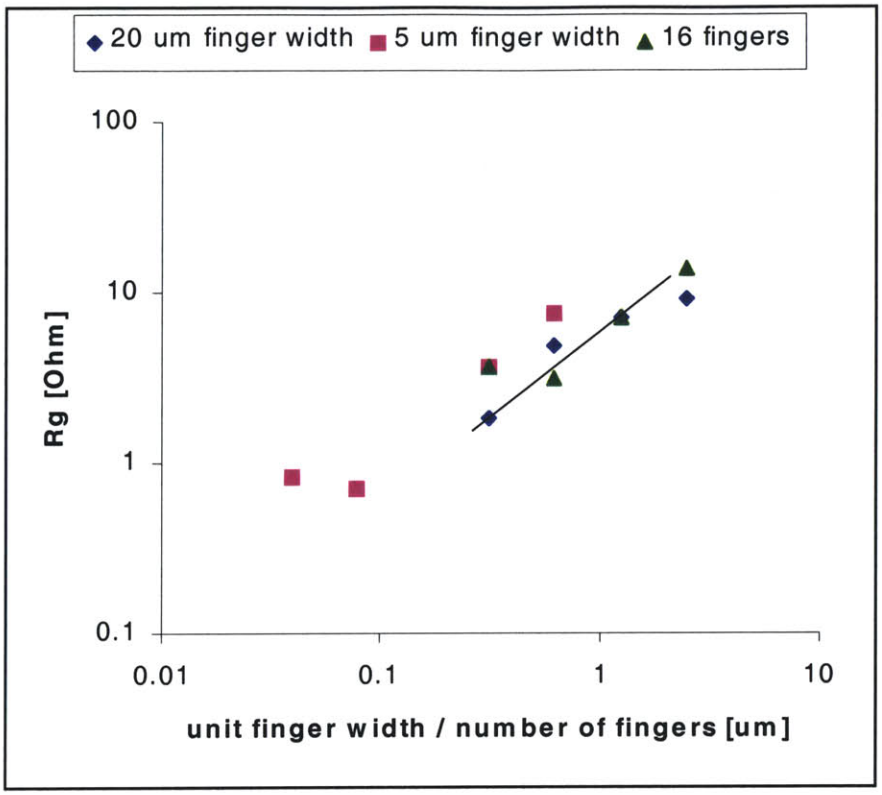

Fig. 5.2-2 R_g as a function of the ratio of unit finger width and number of fingers. The line is drawn at unity slope.

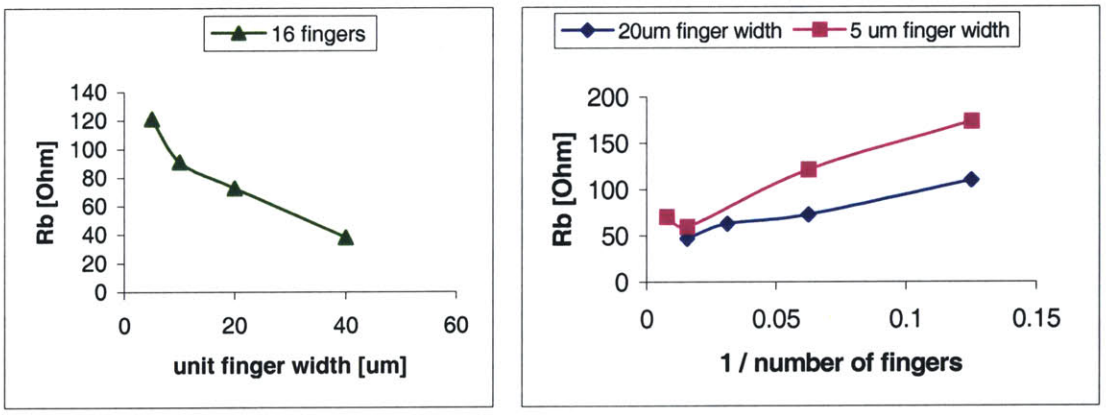

Fig. 5.3-1 R_b as a function of unit width (left) and number of fingers (right)

5.3 Body Resistance, R_b

The body resistance, shown in Fig. 5.3-1, has an interesting behavior, which we will understand by looking in more detail at the device layout. The resistance decreases both with unit finger width and number of fingers. The layout of the 16x10 μm device is shown in Fig. 5.3-2. There are body contacts surrounding the device. This leads to different path lengths to the nearest contact location, depending on where in the device area one starts. Furthermore, we can see that the contact density parallel to the gates is much higher, so that we would expect to have a better conducting (i.e. lower resistance) contact along these sides than along the sides perpendicular to the gates. In Fig. 5.3-3 we see the body resistance as a function of the inverse of the body perimeter. The body perimeter is the total length of the body contacting the active device area. The results show that the body resistance is proportional to the body perimeter, which is emphasized by plotting the product of R_b and the body perimeter. The product is nearly constant, indicating that indeed both parameters are inverse proportional to each other.

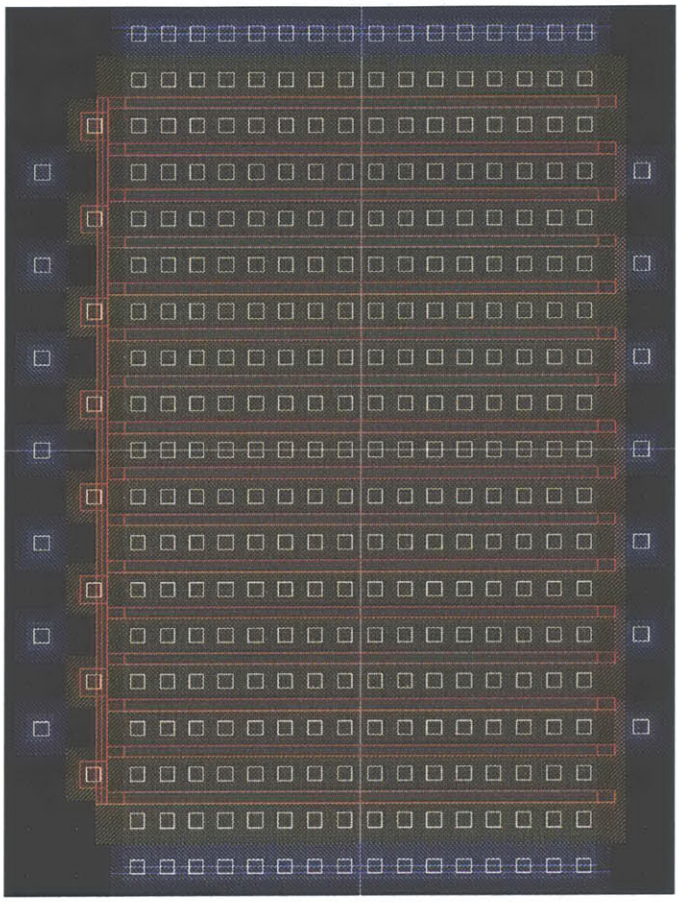

Fig. 5.3-2 Device layout for the 16x10 μm device. Shown are the p- and n-implants, the poly-silicon gate (red lines), and contact holes (white squares) from the *metal1* layer. The body contacts are shown in blue.

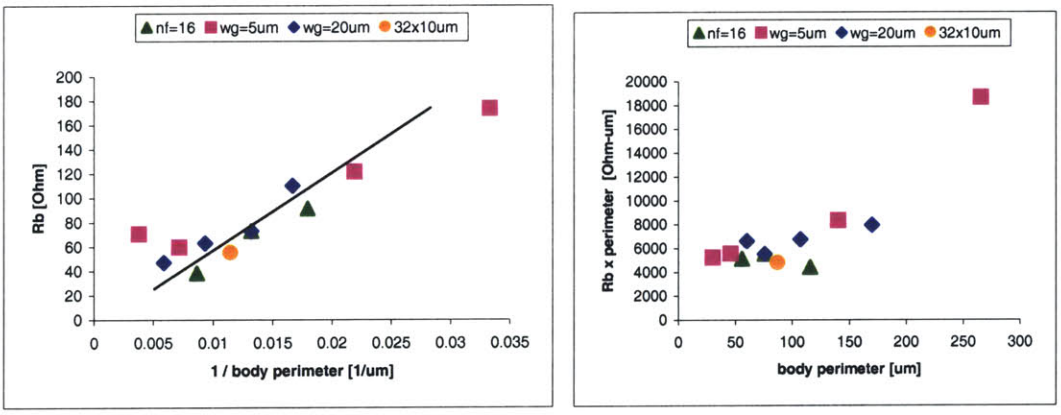

Fig. 5.3-3 (left) Body resistance as a function of the inverse body-contact perimeter, (right) Body resistance – perimeter product, illustrating the inverse proportionality of R_b and the body perimeter.

5.4. Inductances

The inductances take not only the line inductances of the intrinsic device portion into account, but also the metal line and via inductance from the pad to the device layer. This is because our de-embedding mainly removes parallel (i.e. capacitive) effects, but not serial elements such as inductors or resistors. Therefore, to understand the behavior of the inductance values, we will need to first know more about the dimensions of the metal interconnect lines. The signal is routed from the pads to the device on the *metal4* layer. We will now describe the geometry of these lines:

For clarity, the layout is reproduced in Fig. 5.4-1. There are two source lines of constant width of 5.1μm and a line of length of

$$l_{source} = 155\mu m - 0.98\mu m \cdot (n_f + 1) \qquad \text{[Eq. 5.4-1]}$$

The gate and drain lines are identical shapes between the pads and the device. The line length is given by

$$l_{gate,drain} = 33\mu m - \frac{1}{2} \cdot w_g \qquad \text{[Eq. 5.4-2]}$$

The width is roughly proportional to the number of fingers, with an upper limit of 40μm.

$$w_{gate,drain} = \min(1\mu m \cdot n_f, 40\mu m) \qquad \text{[Eq. 5.4-3]}$$

The *metal4* lines described by Eqs. 5.4-1 to 5.4-3 are only a part of the total inductance, which is also influenced by the vias, and the *metal1* and *metal2* lines that route the signals to the device contacts.

For the discussion of each inductance we will state how the inductances should behave with the layout. However, the data often deviates, showing different behavior than what we expected. One example are the drain and source inductance values. The drain and source layouts in the intrinsic device are identical, and the source has a much longer and thinner metal path to the pads than the drain. Yet, in the data, the drain inductance is often twice as much as the source inductance.

In Fig. 5.4-3, we trade off the drain and source inductance. As we can see, the relative error is very small, making it difficult for the optimizer to find exact values. In fact, looking at the sum of all three inductances, we can see in Fig. 5.4-2 that their sum stays roughly independent of the device layout. We believe that the optimizer was not capable of finding the exact inductance values. This is possible to see in the next three sections, when the behavior of the individual inductances is described.

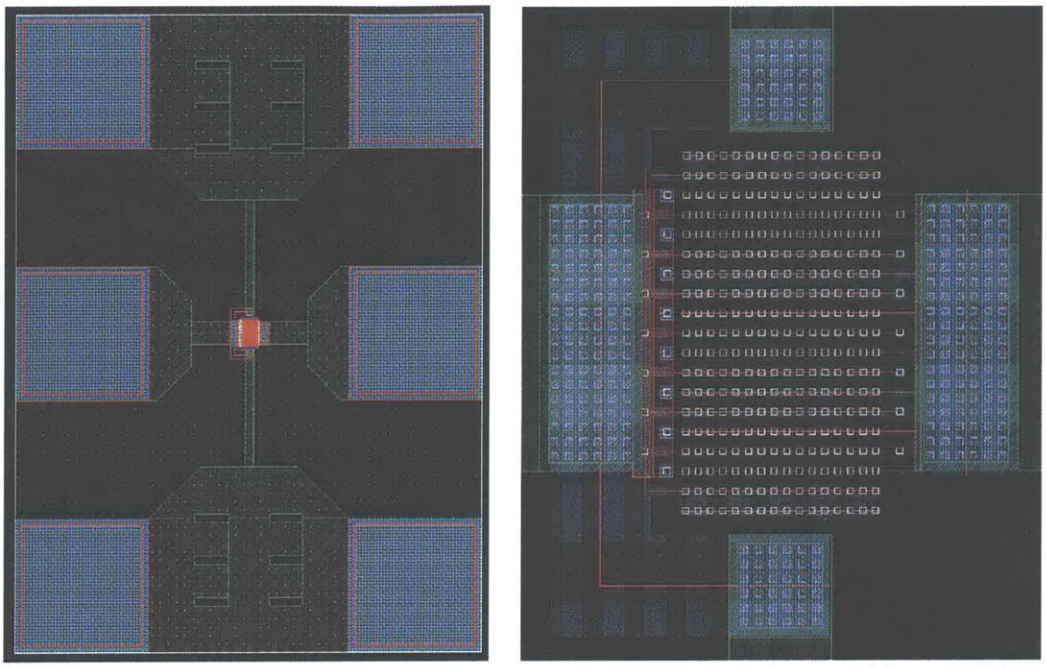

Fig. 5.4-1 Device layout for the 16x10 μm device. Shown are the metal layers (blue: *meatl1*, red: *metal2*, green: *metal4*) and the *metal1* to device contact holes. Left: Complete picture, including probe-pads, right: close-up on the device. The gate is coming in from the middle left pad, the drain from the middle right pad. The four top and bottom pads are the source, coming in to the device from the top and bottom.

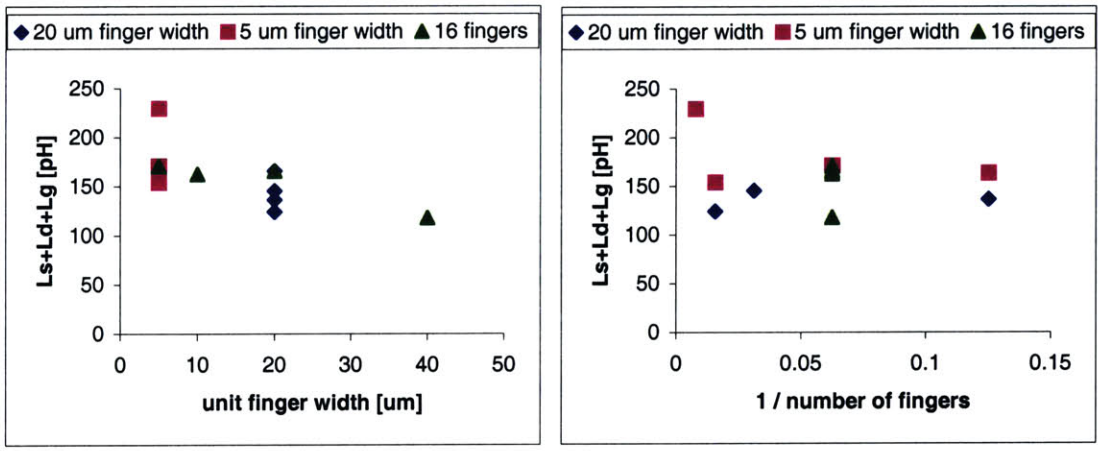

Fig. 5.4-2 The sum of the inductances as a function of unit finger with and the inverse of the number of fingers. The sum is roughly independent of the layout.

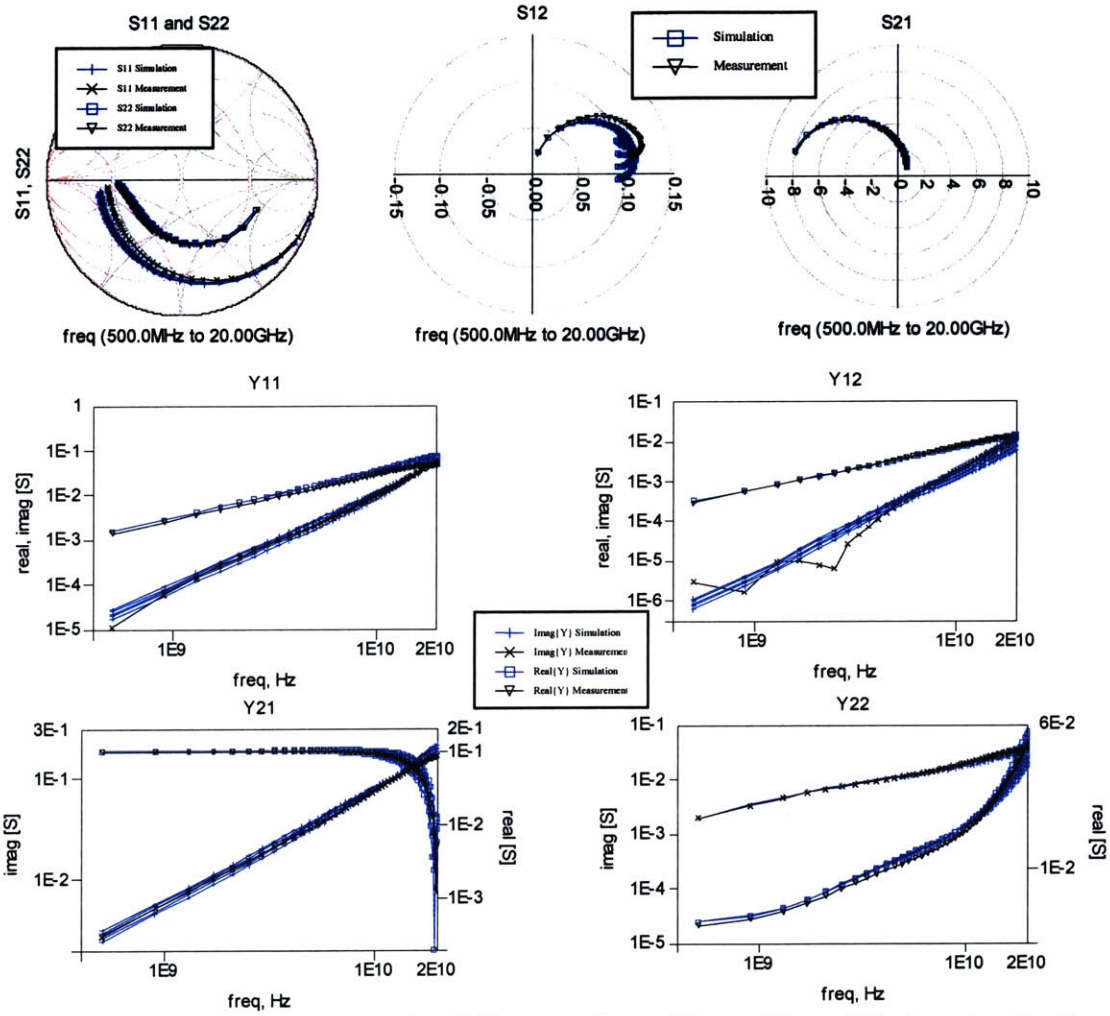

Fig. 5.4-3 S- and Y-parameters for different values of L_s and L_d, while keeping L_s+L_d constant. The device is the 16x20 μm biased at V_{gs}=1.4 V, V_{ds}=2.0 V. The values are L_s=22 pH + Δ_L, L_d=100pH - Δ_L with Δ_L of range ± 10 pH.

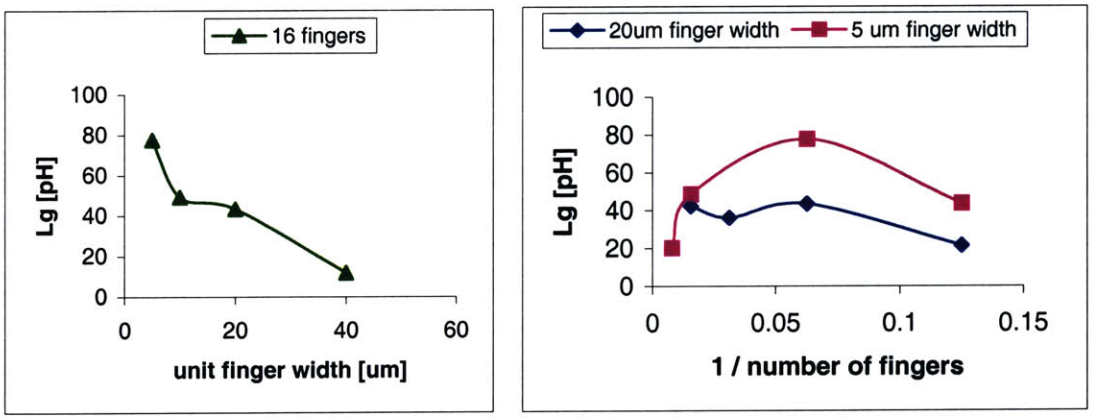

Fig. 5.4.1-1 L_g as a function of unit width (left) and number of fingers (right)

5.4.1. Gate Inductance, L_g

When we increase the unit finger width, while keeping the number of fingers constant, two parameters change that have an influence on the total gate inductance: the unit finger width, and the *metal4* line length. Increasing the unit finger width should decrease the inductance due to added parallel inductances in the gate fingers. At the same time, the *metal4* line is shortening, leading to a decrease of its inductance. In Fig. 5.4.1-1 we see that the gate inductance decreases with unit finger width.

Fig. 5.4.1-1 also shows the gate inductance as a function of the number of fingers. Scaling in this dimension, we would expect a decrease with the number of fingers. If we look at the layout, the metal4 line has approximately the same size as the device. This makes the layout is symmetric, and we can slice the layout into periodic sections of 2 fingers, as shown in Fig. 5.4.1-2. Thus, adding more fingers means to have a complete structure added in parallel, and thus the inductance should decrease. The discrepancy observed is due to the difficulty in optimizing the inductance values as mentioned in 5.4.

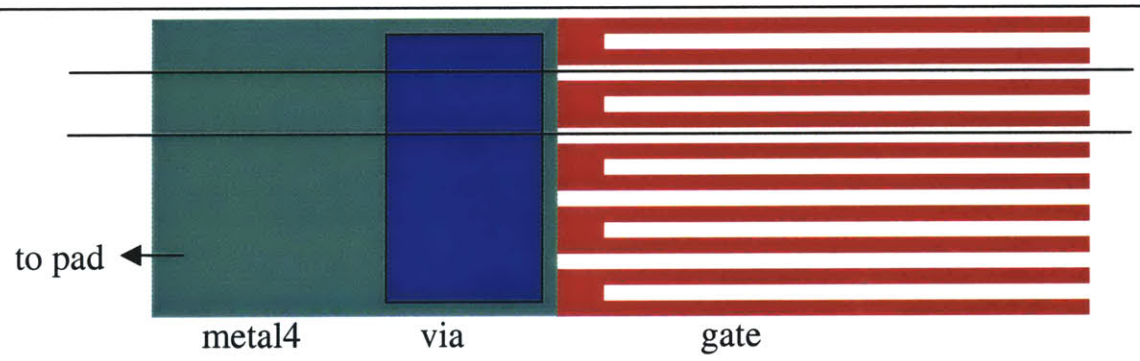

Fig. 5.4.1-2 Layout sketch of the gate structure. The periodic structure of 2 gate fingers is indicated by the lines

5.4.2 Drain Inductance, L_d

The drain inductance is shown as a function of number of fingers and unit finger width in Fig. 5.4.2-1. We would expect the same layout dependencies as the gate inductance previously. Increasing the gate width leads to a shorter metal4 line length, and to a lower finger inductance. Increasing the number of fingers should lead to the same parallel behavior as shown in Fig. 5.4.1-2. However, this behavior is not observed in Fig. 5.4.2-1. Again, we believe this is due to the difficulty in optimizing the inductance values as mentioned in 5.4.

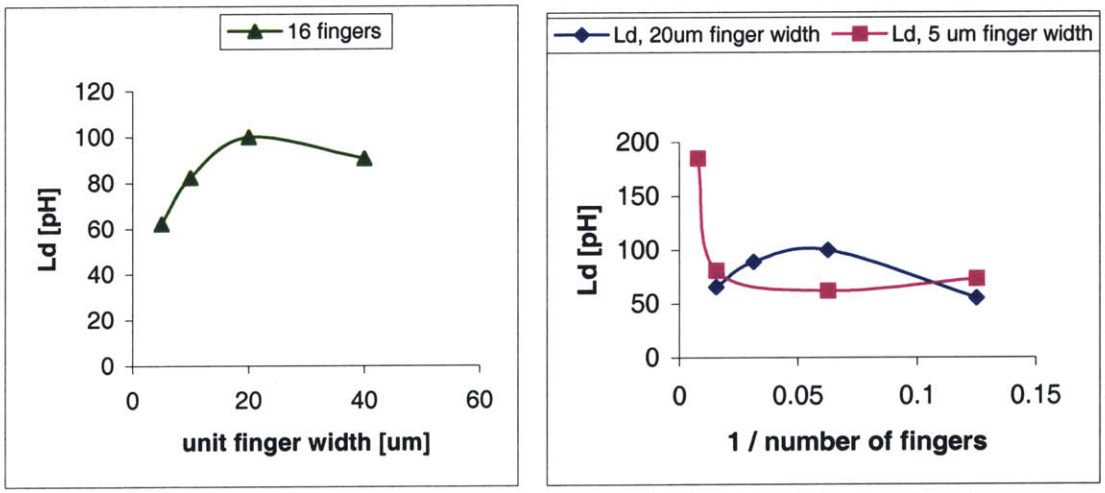

Fig. 5.4.2-1 L_d as a function of unit width (left) and number of fingers (right). Also shown is the difference between L_d and L_g

5.4.3. Source Inductance, L_s

The source inductance as a function of number of fingers and unit finger width is shown in Fig. 5.4.3-1. The sketch in Fig. 5.4.3-2 shows how we expect the dependencies on the layout to be. The overall metal line is constant. This means that the fingers have to be added from bottom to top in the schematic, keeping the source metal line constant. Thus, additional fingers will result in adding inductors in parallel and decreasing the source inductance. Similarly, a wider unit finger width leads to lower finger inductances, also decreasing the overall inductance. These dependencies are observed in Fig. 5.4.3-1.

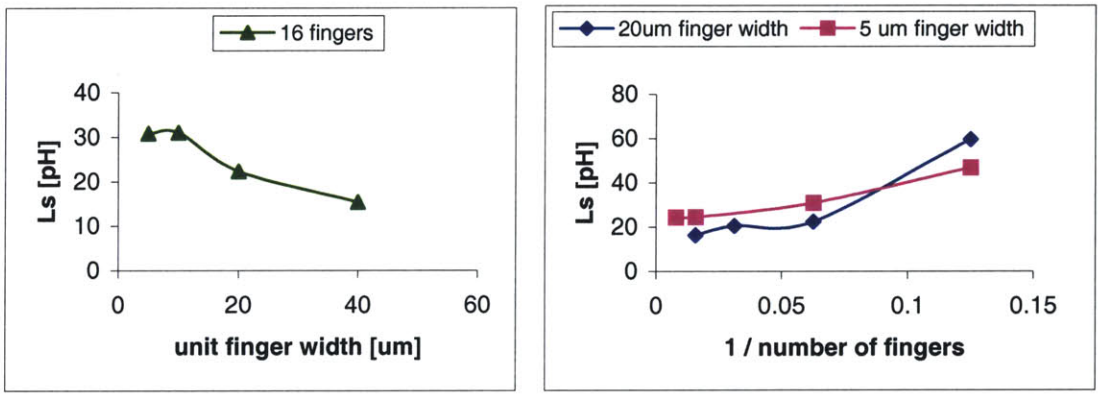

Fig. 5.4.3-1 L_s as a function of unit width (left) and number of fingers (right)

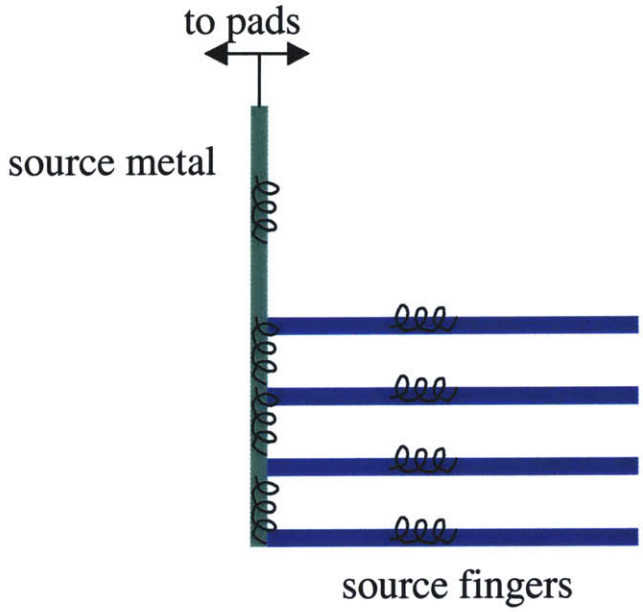

Fig. 5.4.3-2 Simplified sketch of the source inductances. As more fingers are added, the overall inductance decreases because inductors are added into the source metal line in parallel.

5.5. Gate-to-Drain Capacitance, C_{gd}

Fig. 5.5-1 shows the dependence of C_{gd} on unit finger width and number of fingers. It is difficult to make out a clear layout dependency from these graphs, because of the up and downward shaped curves. However, if we plot the data vs. the total device width, W_g, we can see that at least up to W_g = 320 μm, C_{gd} is proportional to the total device width. The reason why this is not seen also for the very wide devices at W_g=640μm and 1280μm is that the impact of C_{gd} on the Y-parameters is decreasing as the device gets wider. The primary impact of C_{gd} is on Y_{12}. Fig. 5.5-3 shows a comparison of Y_{12} for the 16x05 μm and the 128x05μm device, for various values of C_{gd}. We can see that the relative uncertainty is much larger for the 16x05μm device. In fact, for the 128x05 μm device, the

relative uncertainty is so small that for the optimizing algorithm, C_{gd} appears as a parameter with almost no influence. This will cause the parameter to drift somewhat randomly around its initial value during the optimization, which can be seen in the spread of C_{gd} as the device gets wider.

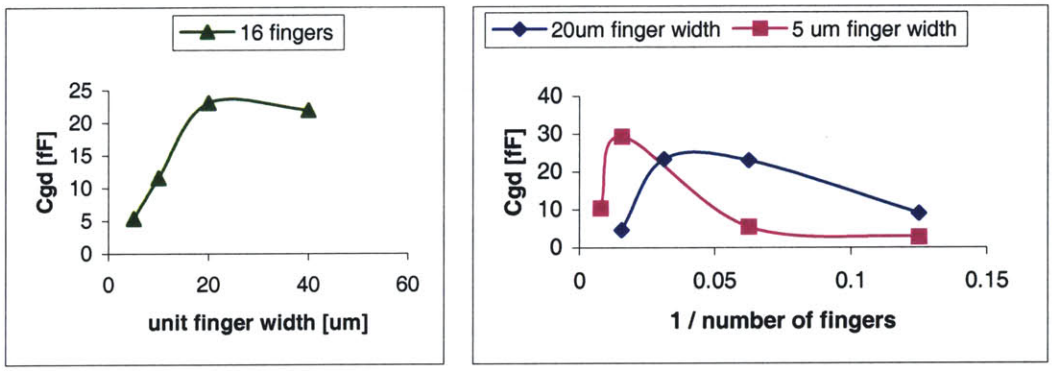

Fig. 5.5-1 C_{gd} as a function of unit width (left) and number of fingers (right)

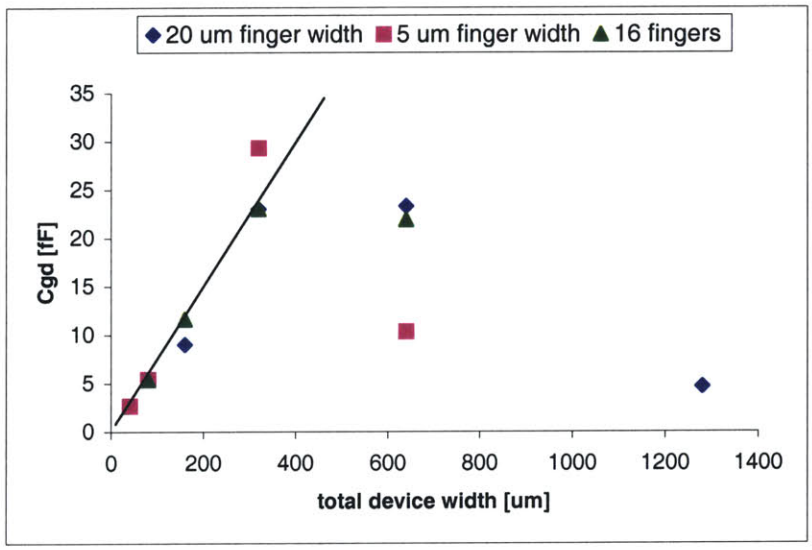

Fig. 5.5-2 C_{gd} as a function of total device width

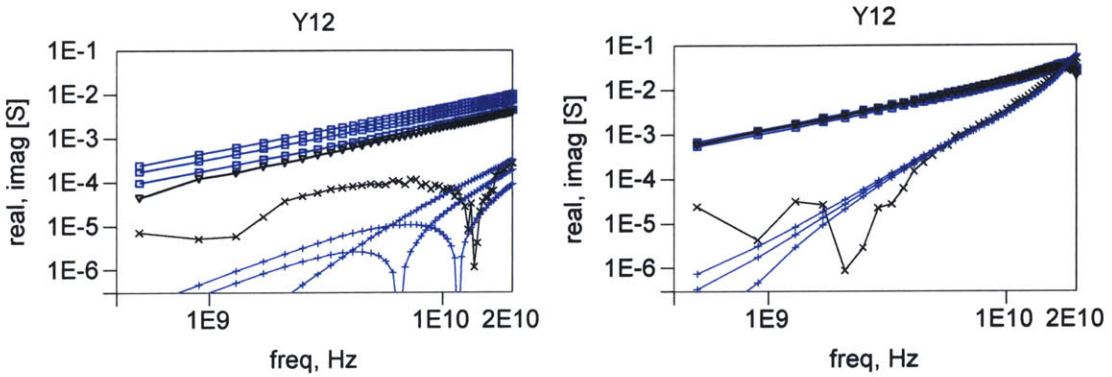

Fig. 5.5-3 Y_{12} for the 16x05 μm (left) and 128x05 μm (right) device, for different values of C_{gd} between 10 and 55 fF. The relative impact of Cgd on the 128x05 μm device is very small, explaining why for wide devices, Cgd does not follow the observed line in Fig. 5.5-2.

5.6. Summary

We have explained the physical origins of the new model parameters. The parameter values were linked to the unit finger width and number of fingers, to show their dependence on these two dimensions. The elements were found to be a function of different layout characteristics, such as total device width (R_{out}, C_{gd}), unit finger width (R_g), number of fingers (R_g), body perimeter (R_b). The sum of the inductances was found to be independent of the device layout.

Chapter 6

Conclusions

6.1. Conclusions

We have characterized the 0.25μm CMOS technology from TSMC for RF power applications. Based on the TSMC BSim3v3 device model for this technology, we successfully built a large signal model that enables us to accurately model the RF power performance of the devices. The BSim3v3 model without adding the new elements would yield poor RF power modeling results.

The values of the new model elements are found through matching the simulations with S-parameter measurements, without the need of an actual load-pull measurement. Having built the model on S-parameter small signal measurements, we showed that the model also gives excellent predictions of the load-pull characteristics at 2.45 GHz, including the figures P_{out}, Gain, I_d, PAE and IM3 as a function of P_{in}.

Explanations of the origin of the new model elements have been given, looking at how the parameter value changes, as the device is either scaled in number of fingers or unit finger width. Finally, a physical explanation for the observed changes was given, based on the device layouts.

6.2. Suggestions for Future Work

An ideal model should be valid for a broad range of biasing conditions, and the model parameters should be possible to be obtained from device dimensions and processing parameters. Currently, the model parameters are optimized to match the S-parameter measurements, at a single bias point that was also used for the power characterization. In order to achieve the goal of bias independence and analytical expressions for the model parameters, more work has to be done. This will involve a more extensive mapping of the parameters for different bias points, as well as trying to get rough analytical expressions for the new model parameters.

It would be interesting to study the impact of the device layout, and the body contact location in particular. This would involve developing a model that connects the RF power figures of merit with the device layout. Breakdown measurements for devices of various dimensions may give further insights, especially when studying the body contact locations.

The model described in this thesis matches the load-pull measurements very closely. In order to validate the model for power amplifier design, one could compare a load- or source impedance contour plot, to see how well the model performs in regions of greater impedance mismatch. If the performance is adequate, one can use the model to design a power amplifier to the specifications of various wireless applications. To find the biasing, power levels and impedances, either the traditional load-pull method can be used (using

load-, source-pulls and power-sweeps to approach the optimal point), or more preferably, one can use the ADS algorithms to find the best point by optimization.

The load-pull measurements in this thesis were done only at 2.45 GHz. The model accuracy is roughly constant over the measured range up to 20 GHz. It would therefore be worth measuring at other frequencies (around 900 MHz and 5 GHz) and to compare load-pull measurements at those frequencies with what the model would predict. Because the S-parameter model is uniformly accurate, we have all reason to believe that the load-pull accuracy at other frequencies would be similar to the one demonstrated in this work.

It would be interesting to use the model developed to design and build a power amplifier. This should also help demonstrate the accuracy of the model.

Another path to investigate would be the RF power performance of the devices for possible changes in processing parameters. This could be done through sweeping parameters of the BSim3v3 model that have a direct connection with the processing conditions, and registering their impact on the simulated device performance. The difficulty here is that it requires a very good knowledge of the process itself, which may be hard to obtain.

Testing the model against other generations (for example, the 0.18 μm technology) would help to verify that the model is universally applicable, and that it is not just tailored to the devices measured in this thesis.

Finally, we believe that with the model proposed in this thesis, it should be possible to design a power amplifier without the need of performing large-signal measurements. Only DC- and S-Parameter characterization will be necessary to determine the value of the model elements.

Appendix A

This appendix shows the S- and Y-parameters of the 16x20 μm device biased at V_{gs}=1.4 V, V_{ds}=2.0 V. The model used in the simulation has optimized parameter values. Each figure shows one of the new elements swept from 1/3 to 3 times its optimal value.

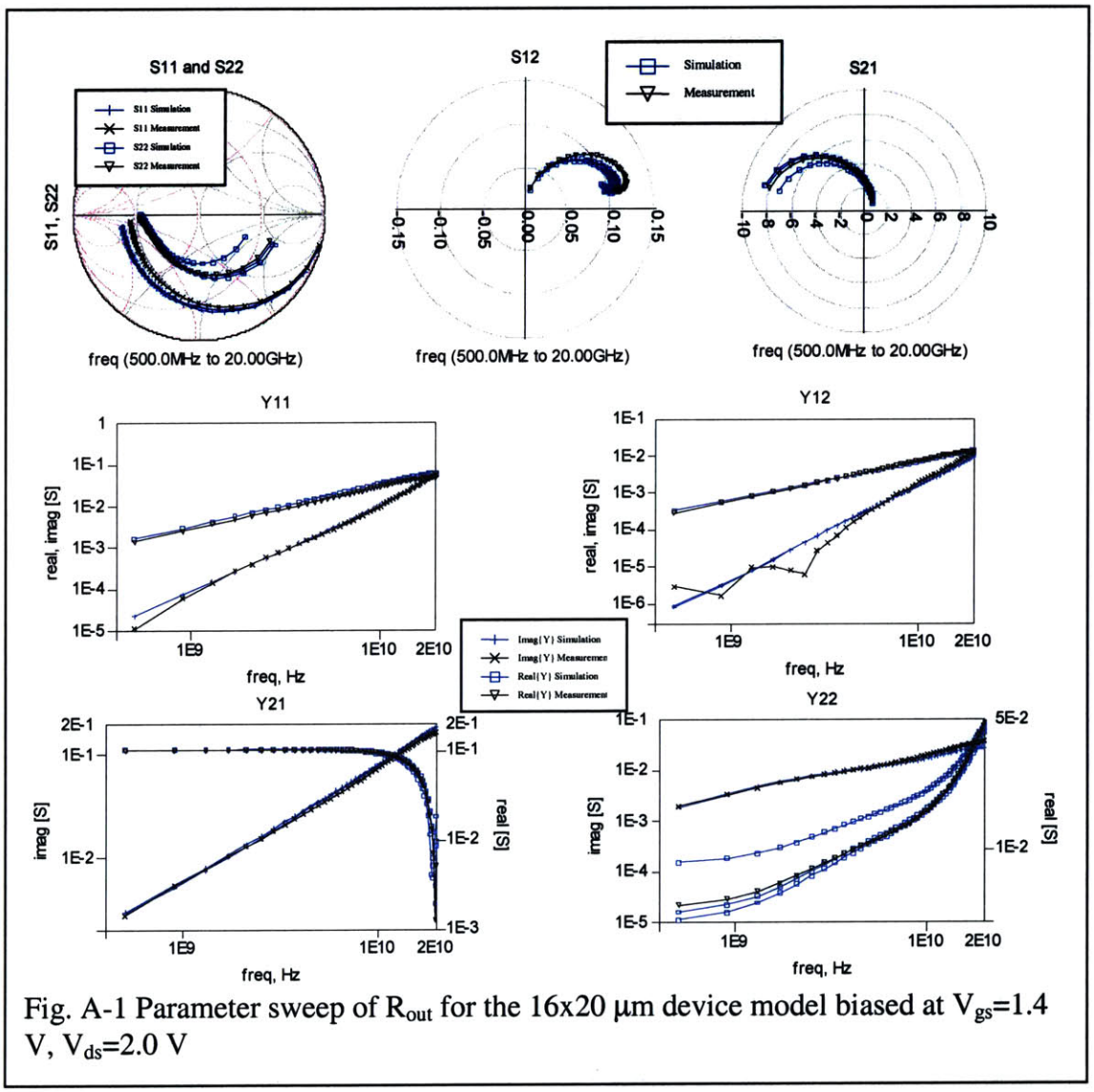

Fig. A-1 Parameter sweep of R_{out} for the 16x20 μm device model biased at V_{gs}=1.4 V, V_{ds}=2.0 V

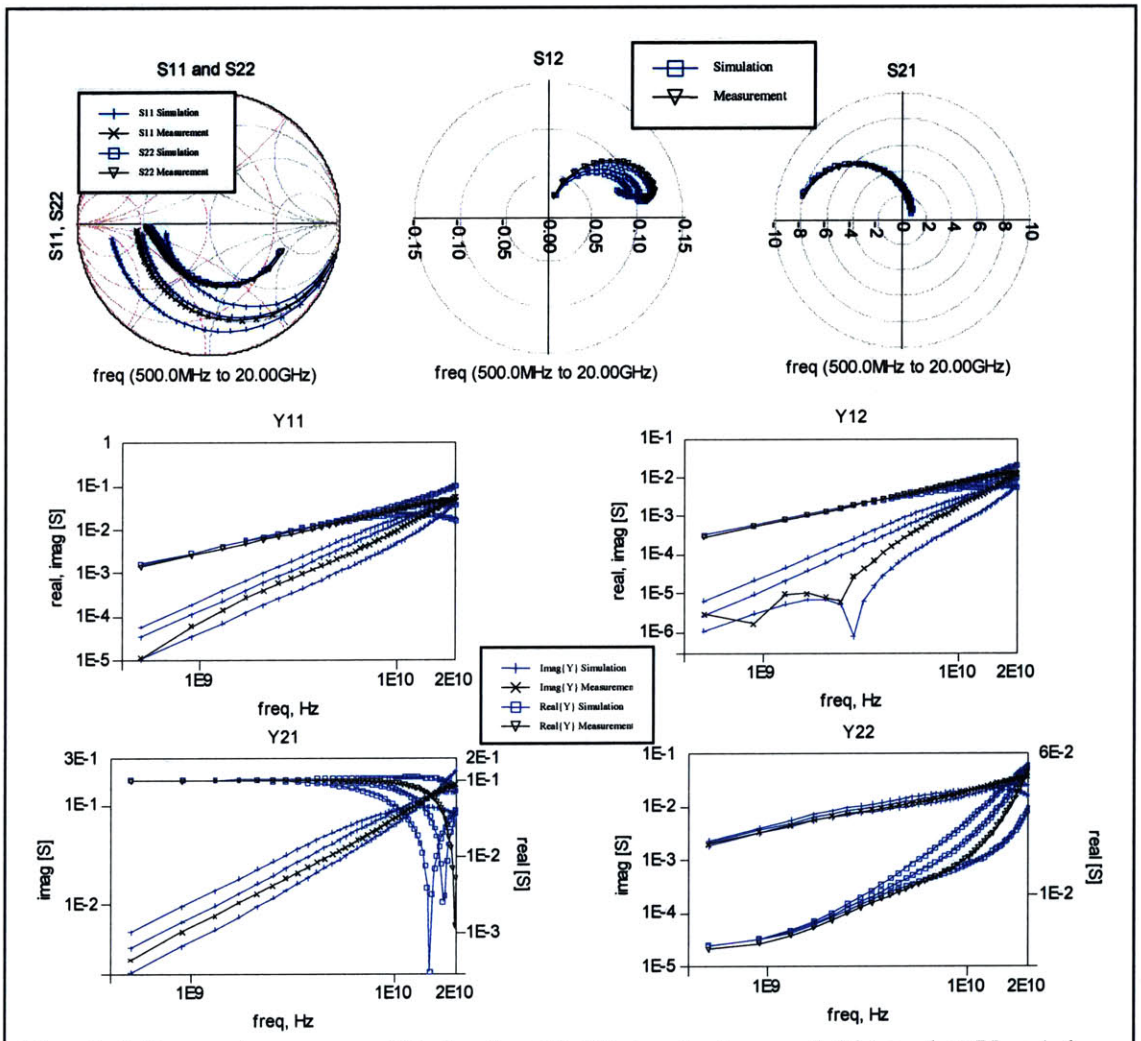

Fig. A-2 Parameter sweep of R_g for the 16x20 μm device model biased at V_{gs}=1.4 V, V_{ds}=2.0 V

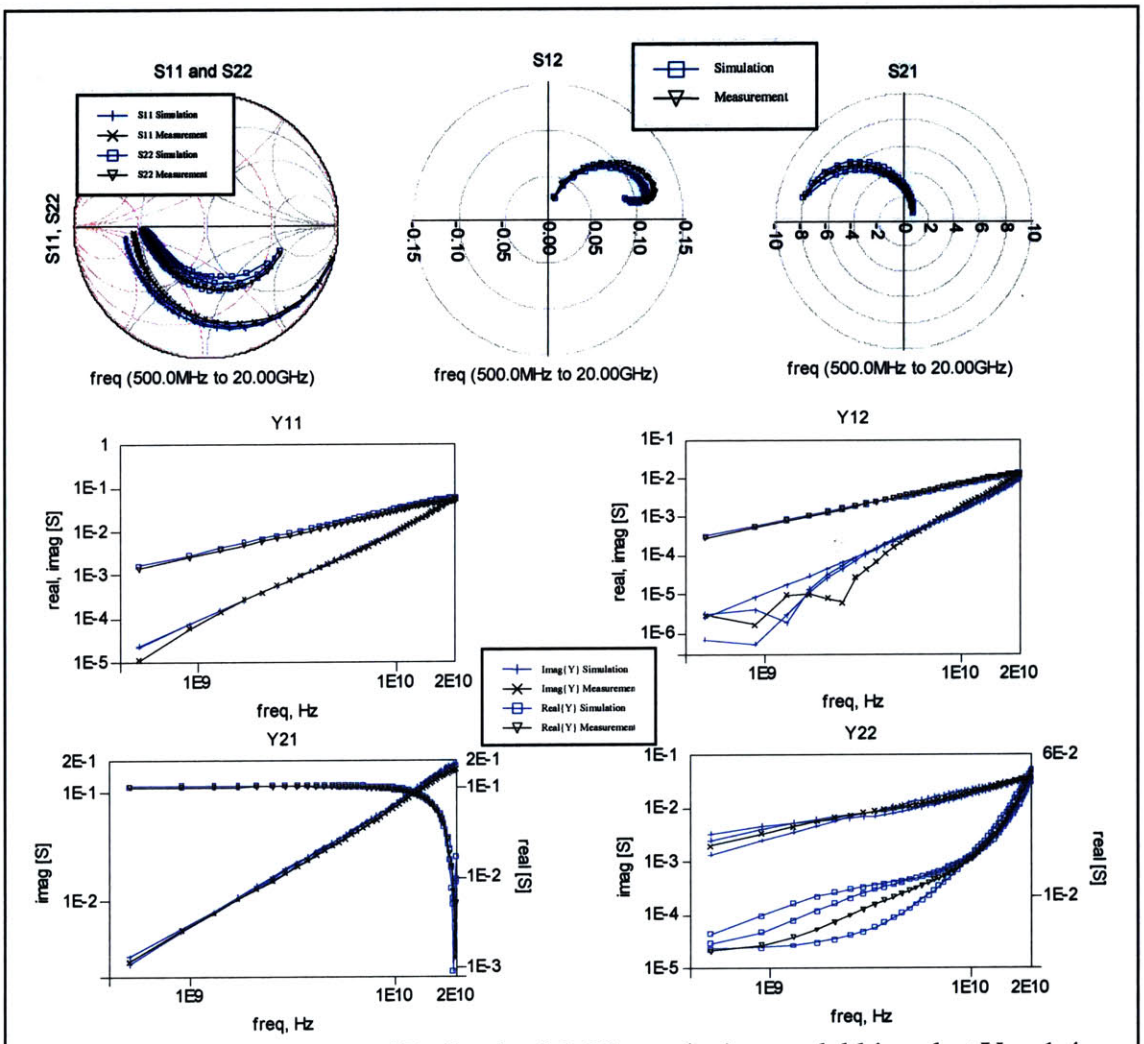

Fig. A-3 Parameter sweep of R_b for the 16x20 μm device model biased at V_{gs}=1.4 V, V_{ds}=2.0 V

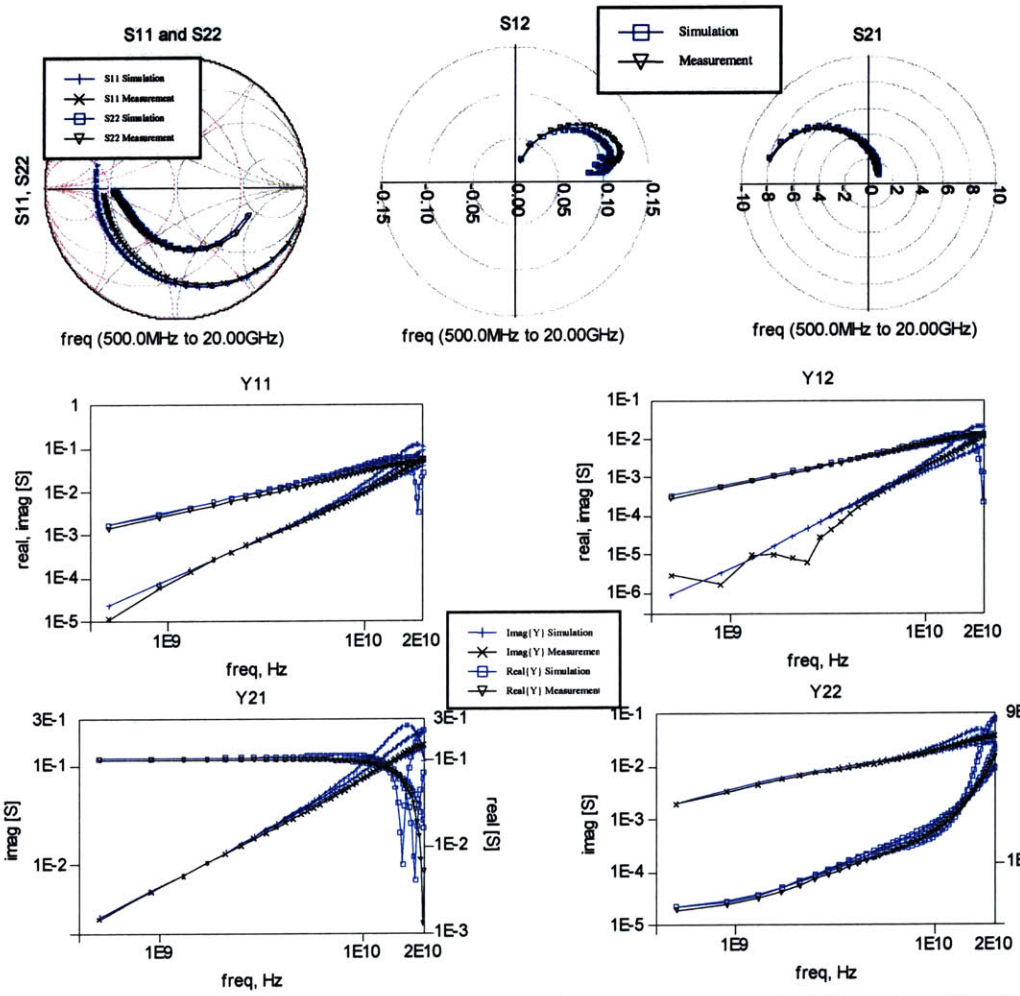

Fig. A-4 Parameter sweep of L_g for the 16x20 μm device model biased at V_{gs}=1.4 V, V_{ds}=2.0 V

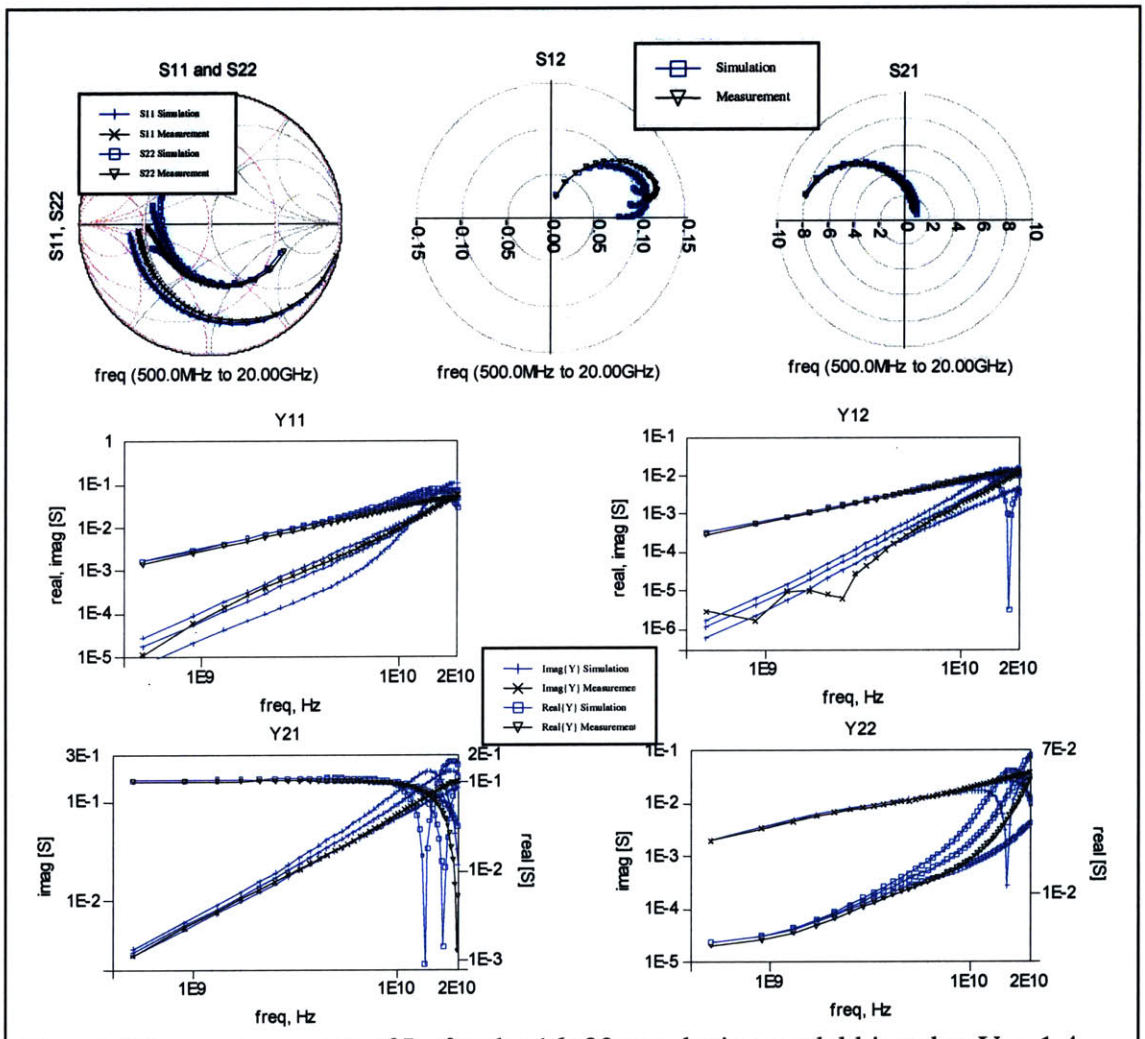

Fig. A-5 Parameter sweep of L_d for the 16x20 μm device model biased at V_{gs}=1.4 V, V_{ds}=2.0 V

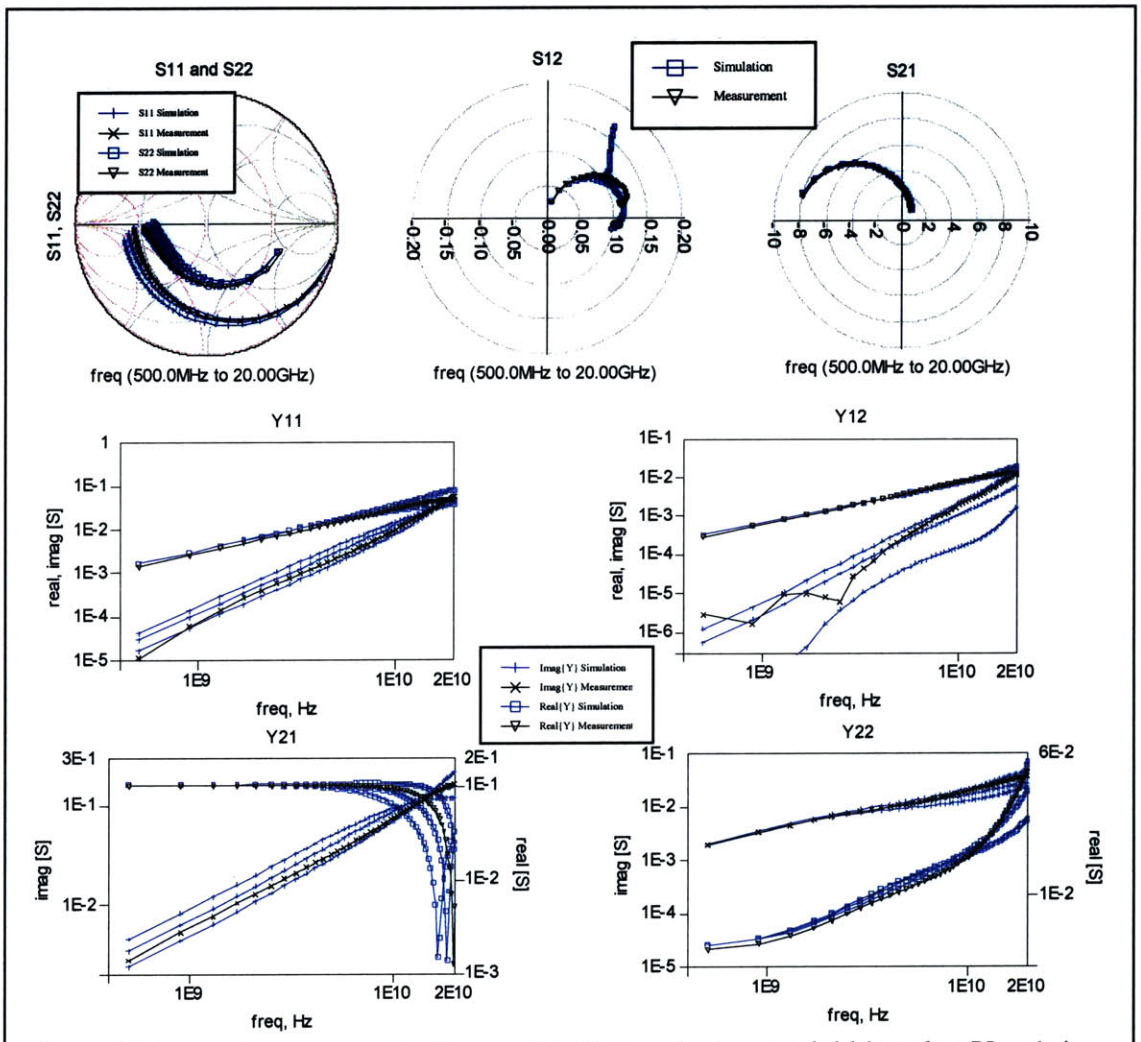

Fig. A-6 Parameter sweep of L_s for the 16x20 μm device model biased at V_{gs}=1.4 V, V_{ds}=2.0 V

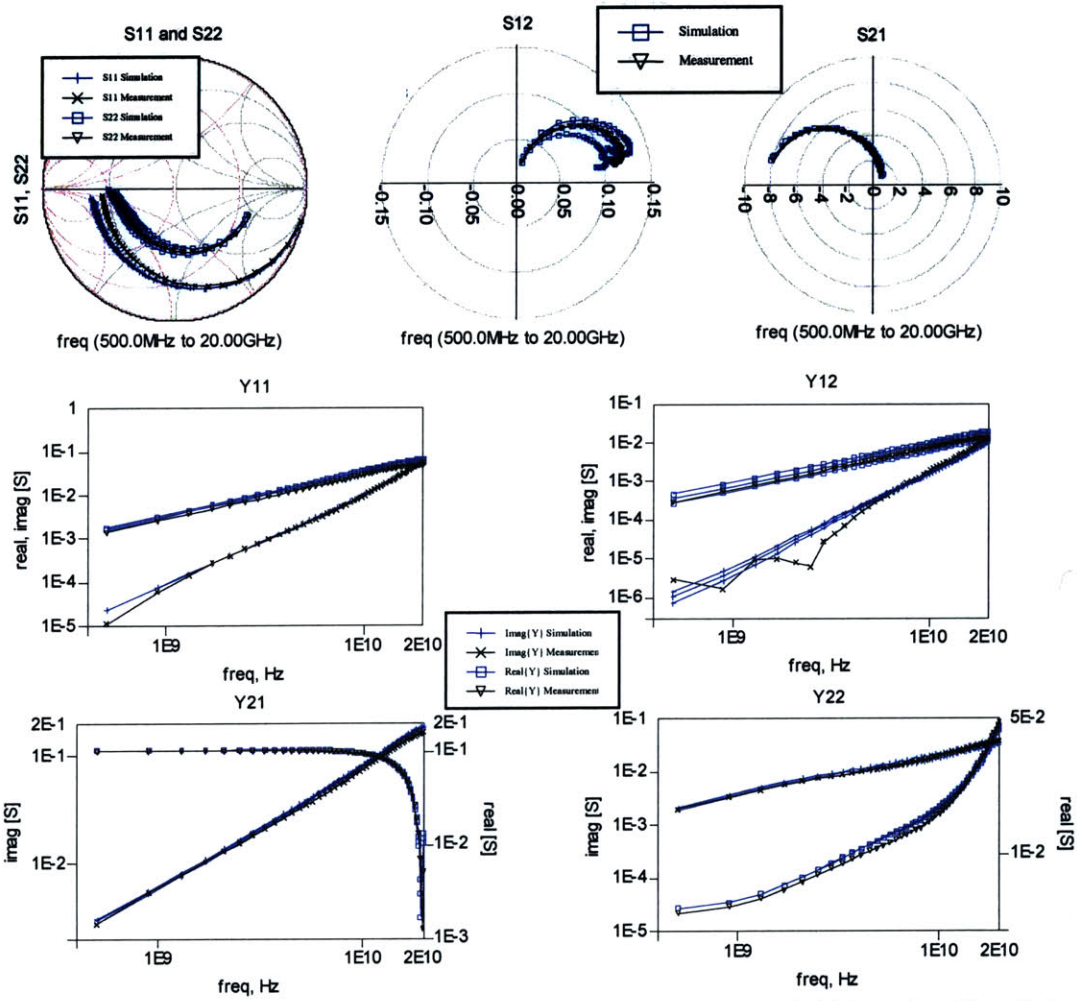

Fig. A-7 Parameter sweep of C_{gd} for the 16x20 μm device model biased at V_{gs}=1.4 V, V_{ds}=2.0 V

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