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Citation: Rivas, Juan M., Yehui Han, Olivia Leitermann, Anthony D. Sagneri, and David J. Perreault. "A High-Frequency Resonant Inverter Topology With Low-Voltage Stress." IEEE Trans. Power Electron. 23, no. 4 (n.d.): 1759–1771. © 2008 IEEE

As Published: http://dx.doi.org/10.1109/TPEL.2008.924616

Publisher: Institute of Electrical and Electronics Engineers (IEEE)

Persistent URL: http://hdl.handle.net/1721.1/86922

Version: Final published version: final published article, as it appeared in a journal, conference proceedings, or other formally published context

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A High-Frequency Resonant Inverter Topology With Low-Voltage Stress

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***Abstract*—This paper presents a new switched-mode resonant inverter, which we term the Φ_2 inverter, that is well suited to operation at very high frequencies and to rapid on/off control. Features of this inverter topology include low semiconductor voltage stress, small passive energy storage requirements, fast dynamic response, and good design flexibility. The structure and operation of the proposed topology are described, and a design procedure is introduced. Experimental results demonstrating the new topology are also presented. A prototype Φ_2 inverter is described that switches at 30 MHz and provides over 500 W of radio frequency power at a drain efficiency above 92%. It is expected that the Φ_2 inverter will find use as a building block in high-performance dc-dc converters among other applications.**

***Index Terms*—Class E inverter, class-F power amplifier, class Φ inverter, harmonic peaking, radio frequency inverter, very high frequency, VHF power converter.**

I. Introduction

RESONANT inverters suitable for high-frequency operation have numerous applications, including as radio-frequency power amplifiers [1]–[3], induction heating and plasma generation [4], [5], and in resonant dc-dc converters [6]–[9]. This paper introduces a new switched-mode inverter which utilizes a specially-tuned resonant network to achieve zero-voltage switching and low device voltage stress. The new design also realizes small passive components, fast dynamic response, and a high degree of design flexibility. These characteristics make the proposed topology advantageous in applications requiring very high frequency operation at fixed frequency and duty ratio.

Section II of the paper provides background on conventional tuned inverter configurations, and provides motivation for the present work. Section III introduces the structure and operation of the new topology. Section IV describes a detailed design procedure. Section V presents the design and experimental evaluation of a prototype converter operating at 30 MHz and providing over 500 W of output power at a drain efficiency of approximately 93%. Finally, Section VI concludes the paper.

II. Background and Motivation

This paper proposes a new switched-mode resonant inverter that overcomes some of the limitations of existing designs. We start by reviewing the characteristics and limitations of these existing designs.

Manuscript received April 6, 2007; revised December 29, 2007. Published July 7, 2008 (projected). This work was supported in part by General Electric Co. and by DARPA through the RIPE (Robust Integrated Power Electronics) program. Recommended for publication by Associate Editor Y.-F. Liu.

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Digital Object Identifier 10.1109/TPEL.2008.924616

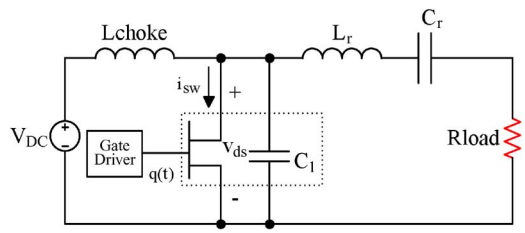

Fig. 1. Class E inverter. L_{choke} is a bulk inductor, while L_r is a resonant inductor.

Tuned switched mode inverters (e.g., classes E, E/F, Φ, and others) incorporate resonant networks in order to achieve efficient operation at very high frequencies and to meet other requirements. For example, the well-known class E inverter [10] uses resonant operation to provide zero-voltage switching and enable the use of (relatively) slow gating waveforms. Moreover, it requires only a single ground-referenced switch, and absorbs device parasitic capacitance as a natural part of its operation. As a result, the class E inverter topology has been widely used in a range of applications including radio-frequency dc-dc power converters [6]–[9], [11]–[13].

While the conventional class E inverter has many merits, it also has some important limitations. Among the undesirable characteristics of the class E inverter is the high voltage stress imposed on the switch. The peak switch voltage stress in an ideal class E circuit is about 3.6 times the input voltage [2], [10] (idealized operation using linear passive components, ideal switch, 50% duty cycle). In practical implementations, with operating frequencies reaching into the VHF range, the capacitance C_1 of the class E circuit of Fig. 1 is oftentimes solely provided by the semiconductor drain-to-source capacitance. The non-linear variation of the device capacitance with drain voltage can further increase the voltage stress across the semiconductor, reaching a value of almost 4.4 times the input voltage [14] for this circuit. Some radio-frequency power amplifiers, such as class F and variants, use resonant harmonic peaking of the input or output network [1], [15]–[21] to reduce the peak voltage on the switch. However, most practical rf amplifier designs of this type operate with significant overlap of device voltage and current (i.e. not fully in "switched mode"), thus providing unacceptably low efficiency for many power electronics applications.

A switched-mode variant of the class F inverter that can be made highly efficient is the so-called class Φ inverter [3], [22], [23]. This approach uses a transmission-line network or a high-

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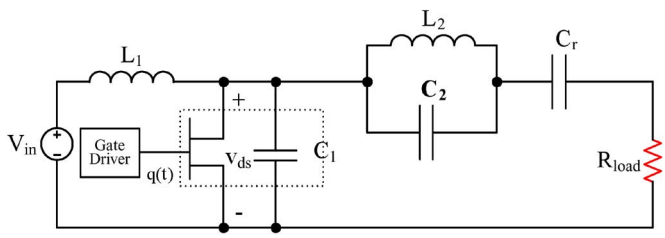


Fig. 2. Second harmonic class E inverter. Inductor L_1 in the this circuit is a resonant element; this reduces the energy storage requirements and provides a faster transient response than a conventional class E inverter.

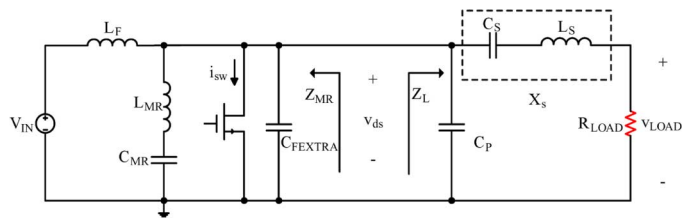


Fig. 3. Class Φ_2 inverter. The impedance Z_{MR} consists of the elements of a low order resonant network which has an impedance zero near the second harmonic of the switching frequency. The impedance Z_L determines the output power and also plays a role shaping the drain voltage.

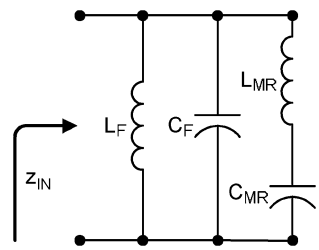


Fig. 4. Low-order lumped network at the input of the class Φ_2 inverter. The input impedance $Z_{\rm IN}$, when properly tuned, has relatively high impedance at the fundamental and the third harmonic and has low impedance at the second harmonic. This impedance characteristics of this network are similar to a shorted quarter wavelength transmission line.

order lumped simulating network at its input to provide waveform shaping. This reduces peak device stress and eliminates the need for a bulk rf choke. Unlike most practical class F designs, the Class Φ inverter operates entirely in switched mode (at duty ratios below 50%). This yields high efficiency and provides reduced device stress and improved energy storage requirements as compared to traditional inverters. However, these inverters utilize high-order resonant structures with many energy storage components and/or modes and relatively high complexity.

In systems requiring fast response to input voltage variations or where on/off control of the inverter regulates the output (e.g., [9], [24], [25]), it is desirable to achieve fast transient response. In this type of system, traditional class E converter circuits have the disadvantage of a large valued input inductor. This results in relatively large stored energy in the converter that increases the time for the converter to adjust its operating point (e.g., during startup or shutdown). Some less familiar inverter topologies, such as the "second harmonic Class E" [8], [26], [27] shown in Fig. 2, reduce the bulk energy storage requirement compared to the class E, but do not reduce the peak device voltage stress.

Both the class E and the second harmonic class E inverters also share the disadvantage of having a tight link between the output power and the drain-to-source capacitance of the switch. In the class E inverter, $P_{\rm OUT} = 2\pi^2 \cdot f_s \cdot V_{\rm IN}^2 \cdot C_1$, where $P_{\rm OUT}$ is the inverter output power, $V_{\rm IN}$ is the input voltage, f_s is the switching frequency, and C_1 is the net capacitance in parallel with the switch. Likewise, $P_{\rm OUT} = (1/2)\pi^2 \cdot f_s \cdot V_{\rm IN}^2 \cdot C_1$ for the second harmonic class E inverter. This implies that at high operating frequencies these topologies are bounded to a minimum output power (determined by the intrinsic switch capacitance) that may be higher than the desired output power. Even when acceptable, running at a design power greater than desired hurts efficiency, making this limitation a significant consideration. Of these two designs, the second harmonic class E has a higher allowable frequency limit for a given power throughput and device capacitance. However, both designs suffer from this tight tie between output power, capacitance, and efficiency.

In light of the above issues, there is need for improved topologies that enable VHF operation, provide low device stress and loss, and require a reduced number and size of energy storage components. This document introduces a new design that addresses these issues. This circuit topology is based on a simplified "Class-Φ" inverter which attenuates second harmonic voltage to provide waveform symmetry. Furthermore, the design of this topology permits absorbtion of device capacitance into the waveshaping network in a manner that breaks the tight link between the output power and device output capacitance. This provides the flexibility to realize designs over wider frequency and power ranges.

III. A New Class-Φ Based Inverter Topology

Here we introduce a new tuned inverter which overcomes many of the above-cited limitations of existing designs. The new inverter is suitable for very high-frequency operation, provides low device voltage stress, small passive component count and size, and fast transient response.

Fig. 3 shows the proposed switched-mode resonant inverter, which we term the Φ_2 inverter. It is closely related to the class Φ inverter of [3], [23], but has the high-order transmission-line network of the class Φ replaced by a low-order resonant network. In particular, the resonant network illustrated in Fig. 4 (or an equivalent network) forms a portion of the inverter network in Fig. 3, and provides impedance and waveforms shaping characteristics similar to those of a shorted quarter-wave transmission line. As in the case of the class Φ inverter [3], [23], [28], the resonant network acts to impose (approximate) half-wave voltage symmetry in the drain-source voltage waveform, yielding a quasi-trapezoidal drain-source voltage having a low peak value. More details about the relationship between impedance and waveform shaping may be found in [3] and [28].

The components of the inverter are tuned to obtain a voltage across the switch with low peak amplitude, and to allow switched-mode operation and low loss through near zero-voltage at turn on and turn off, and at a given frequency and duty ratio. In particular, one can achieve a quasi-trapezoidal voltage waveform across the switch. Moreover, with proper tuning one can obtain zero dv/dt across the switch at turn on, which is desirable for operating at frequencies in the VHF-UHF range. The zero-voltage switching and the zero

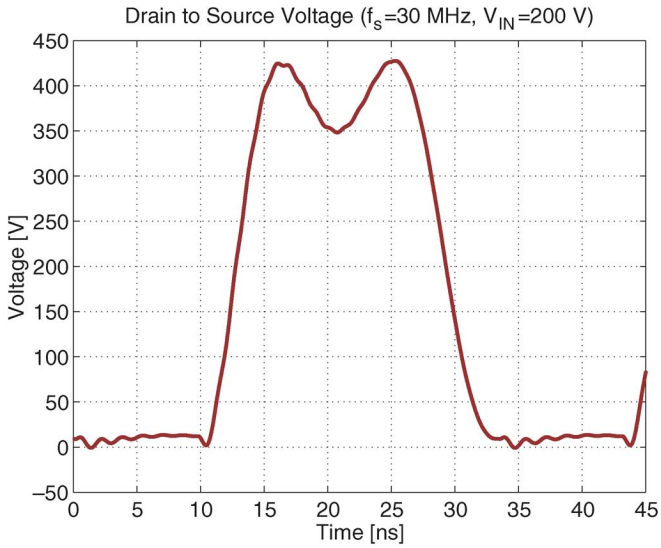


Fig. 5. Simulated drain to source voltage for a Φ_2 inverter. The simulated inverter delivers 380 W from a dc voltage of 200 V. The circuit parameters are: $\mathrm{L_F} = 270\ \mathrm{nH}$, $\mathrm{L_{MR}} = 375.3\ \mathrm{nH}$, $\mathrm{C_{MR}} = 18.8\ \mathrm{pF}$, $\mathrm{C_S} = 4\ \mathrm{nF}$, $\mathrm{L_S} = 198.8\ \mathrm{nH}$, $\mathrm{R_{LOAD}} = 33.3\ \Omega$. The total capacitance at the drain node is 88.2 pF. Of this total, 48.2 pF is the nonlinear $\mathrm{C_{OSS}}$ of the MOSFET when $\mathrm{V_{ds}} = 200\ \mathrm{V}$ and the remaining $40\ \mathrm{pF}(= \mathrm{C_{F,EXTRA}} + \mathrm{C_P})$ external capacitance. The switch is on for a duty ratio $\mathrm{D} = 0.3$ at a 30-MHz switching frequency.

dv/dt conditions are illustrated in Fig. 5: At switch turn on (at approximately 34 ns) it can be seen that the drain voltage is approximately zero, with nearly zero dv/dt. As will be shown, these features can be obtained by appropriately selecting the impedance seen at the drain-source port of the switch at the fundamental switching frequency and its first few harmonics.

To illustrate the working principles behind the operation of the Class Φ_2 inverter, the circuit in Fig. 3 has been divided in two parts: One part is formed by the switch and the low-order lumped network of Fig. 4 (connected appropriately to the dc input). $\mathrm{C_F}$ in Fig. 4 thus represents the output capacitance of the switch (C_{OSS}) plus an (optional) additional capacitance component $\mathrm{C_{F,EXTRA}}$. The passive portion of this part of the network provides an approximation to the impedance and waveform symmetrizing characteristics of a shorted quarter-wave transmission line [3], [22], [23], [28]. This portion of the network provides an output impedance Z_{MR} when the switch is off. The other part of the circuit is a load network comprising the resistance $\mathrm{R_{LOAD}}$, a reactive interconnect ($\mathrm{X_S}$ in the figure), and a shunt capacitance $\mathrm{C_P}$. This portion of the circuit presents an impedance Z_L, such that the total impedance seen looking into the drain-source port of the power MOSFET (or other switching device) is given by $Z_{ds} = Z_{MR} \| Z_L$ when the switch is off. Note that the separation of capacitances in Fig. 3 is purely for purposes of analysis and design. The only physical requirement is that the total capacitance selected for use at the drain-source node ($C_{OSS} + \mathrm{C_{F,EXTRA}} + \mathrm{C_p}$) be greater than or equal to the actual switch capacitance plus any unavoidable parasitic capacitance.

During inverter operation, and for the interval in which the switch is "on", energy flows from $\mathrm{V_{IN}}$ and is stored in the inductor $\mathrm{L_F}$. Also during this interval, energy is circulated (at two times the switching frequency) in the resonant leg formed by $\mathrm{L_{MR}} - \mathrm{C_{MR}}$. During the interval when the switch is "off" the drain to source voltage of the inverter rings with a characteristic determined by the impedance of the drain node.

A characteristic feature of the Φ_2 inverter is that components $\mathrm{L_{MR}}$ and $\mathrm{C_{MR}}$ are tuned to be series resonant near the second harmonic of the switching frequency. This condition imposes a low impedance across the switch at the second harmonic and prevents the drain voltage $v_{ds}(t)$ from having significant second harmonic content. The rest of the components (forming the reminder of Z_{ds}) are tuned to provide relatively high impedance at the fundamental and the third harmonic of the driving frequency.

These impedance characteristics are important in establishing approximate half-wave voltage symmetry at the drain node. In periodic steady state, the average drain voltage must equal the input voltage. Further, the switch periodically forces the drain node to zero volts for part of the cycle. Since the waveform has to maintain approximate half-wave symmetry, the drain voltage will rise during the remainder of the cycle approximating a trapezoid. The exact shape of the drain voltage is determined by the impedance Z_{ds} at the drain-source port, which is selected as part of the tuning process to secure the zero-voltage switching conditions that allow high-frequency switched-mode operation. Since the performance of the inverter relies on tuned components, the Φ_2 inverter operates most effectively at a fixed frequency and duty ratio.

IV. Design of the Φ_2 Inverter

Component selection in the inverter is based on achieving certain impedance characteristics as seen at the transistor output port when the transistor is off (Z_{ds}). While unusual, the authors have found this to be an effective and robust method for realizing the desired performance. The tuning methodology leads to component values yielding the following results.

- The impedance at the fundamental of the switching frequency is 30°–60° inductive.
- The impedance at the second harmonic is small due to the series resonance between $\mathrm{L_{MR}}$ and $\mathrm{C_{MR}}$.
- The impedance at the third harmonic is capacitive in phase and its magnitude is several decibels (between 4 and 8) below the impedance magnitude at the fundamental.
- The values of $\mathrm{X_S}$ and $\mathrm{R_{LOAD}}$ are selected to achieve the desired power transfer based on the voltage division from the trapezoidal operating waveforms of the inverter.

There are many ways to achieve this goal, but here we consider a single route.

1) Component Selection of the Reactive Interconnect X_S: Components $\mathrm{L_S}$ and $\mathrm{C_S}$ are part of the output tank that connects the drain to the load resistor $\mathrm{R_{LOAD}}$. This reactive interconnect (labelled $\mathrm{X_S}$ in Fig. 3) performs multiple functions: It provides dc blocking, and also forms an impedance divider that controls the ac power delivered to the resistive load. Moreover, the output tank forms part of the total impedance Z_{ds} and thus is also involved in the waveshaping of the switch voltage.

To determine the component values of the interconnect, we begin by assuming that the drain voltage $v_{ds}(t)$ is a trapezoid, which can be further approximated by a square wave to simplify the design. This square wave has 50% duty cycle, an average

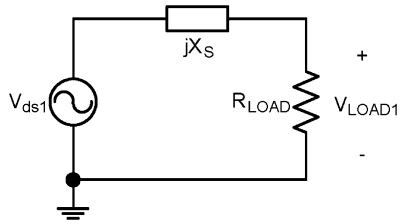


Fig. 6. Model at the fundamental frequency used to size the components of the reactive interconnect network.

voltage equal to V_{IN}, and swings between 0 and $2V_{IN}$. Further, we assume that the all the ac power is delivered to the load only at the fundamental of the switching frequency. Hence, we can represent the output tank of the Φ_2 inverter with the equivalent circuit shown in Fig. 6. Here, v_{ds1} represents the fundamental of $v_{ds}(t)$ which has an amplitude $V_{ds1} = (4/\pi) \cdot V_{IN}$. X_S can be implemented to either look capacitive or inductive at the fundamental: both possibilities are viable, but yield differences in the way harmonic components are handled.

Consider how the reactance X_S in Fig. 3 can be obtained. As mentioned above, X_S forms part of a reactive divider that sets the output power delivered to R_{LOAD}. By reference to Fig. 6, one can determine for a given output power, $v_{load1,RMS} = \sqrt{P_{OUT} \cdot R_{LOAD}}$. Knowing that the effective value of the fundamental component of $v_{ds}(t)$ (approximated by a square wave) is $v_{ds1,RMS} = (4/\pi\sqrt{2}) \cdot V_{IN}$ one can obtain the desired reactance X_S as

$$X_S = R_{LOAD} \cdot \sqrt{\left(\frac{v_{ds1,RMS}}{v_{load1,RMS}}\right)^2 - 1} \tag{1}$$

L_S and C_S are then selected to provide this desired reactive magnitude (with inductive or capacitive phase) and a desired frequency selectivity. Note that in some cases, a design with $L_S = 0$ is viable.

2) Initial Sizing of the Elements of Z_{MR}: The next step in the tuning procedure of the Φ_2 inverter is selecting the components that form the impedance Z_{MR} in Fig. 3. The elements forming Z_{MR} are part of the low-order network of Fig. 4, and play a major role in shaping of the voltage v_{ds} into a trapezoid.

One possible starting point is to tune the network represented by Fig. 4 such that the impedance maxima of Z_{IN} (or Z_{MR} in Fig. 3) are at the fundamental and the third harmonic of the switching frequency. Component values for tuning the poles of Fig. 4 at exactly the fundamental and third harmonic and placing the zero at the second harmonic can be determined starting from a selected value for C_F [29], [30]

$$L_F = \frac{1}{9\pi^2 f_S^2 C_F},\ L_{MR} = \frac{1}{15\pi^2 f_2^2 C_F},\ \text{and}\ C_{MR} = \frac{15}{16} C_F. \tag{2}$$

Notice that in the Φ_2 inverter of Fig. 3, the capacitance of the semiconductor switch and the capacitor C_{FEXTRA} in Z_{MR} form the capacitor C_F in the network of Fig. 4. The value of the capacitor C_F used to obtain the other components of Z_{MR} can be solely the semiconductor capacitance, a fraction of it, or a larger value. The specific value chosen can be used as a design handle that has a significant impact on the performance of the inverter.

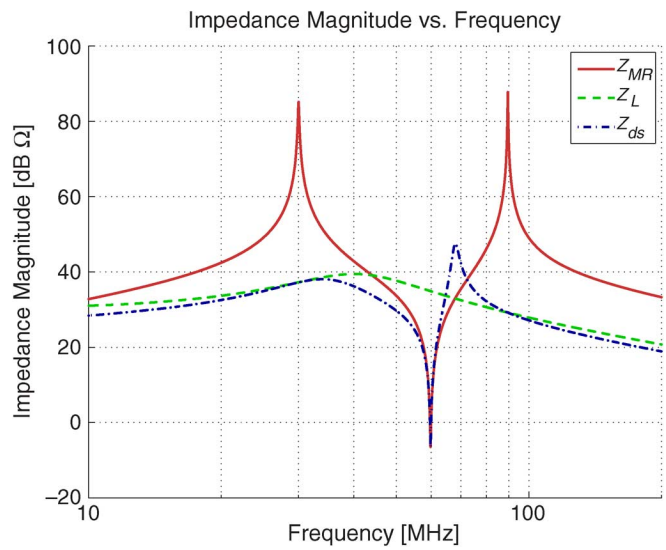


Fig. 7. Magnitude of the impedances Z_{MR}, Z_L and Z_{ds} in the Class Φ_2 inverter (at an intermediate point in the tuning process). Z_{ds} is equal to $Z_{MR}\|Z_L$. For this example $C_F = 20$ pF, $L_F = 625.4$ nH, $C_{MR} = 18.8$ pF, $L_{MR} = 375.3$ nH. $L_S = 198.8$ nH, $R_{LOAD} = 33.3\ \Omega$, $C_S = 4$ nF, $C_P = 75.4$ pF (35.4 pF remaining from the switch plus 40-pF external capacitance).

Using larger values of C_F in (2) will shift the impedance magnitude of the network in Fig. 4 down. Because the drain impedance $Z_{ds} = Z_{MR}\|Z_L$, reducing the magnitude of Z_{MR} may be a necessary step in applications in which the impedance Z_L heavily loads the drain impedance Z_{ds}. Smaller values of C_F increase the impedance of the rest of the components of Z_{MR}, and reduces the circulating currents throughout the network. On the other hand, using a very small or large value of C_F can result in unreasonable values for the rest of the components of the network. Then, the choice of the value of C_F is a trade-off between the allowable resonant losses (due to the Q of the components) and the output power delivered to Z_L.

Equation (2) gives a good starting point for the value of L_F, but extra tuning may be required. The detailed tuning of L_F is accomplished to obtain desirable waveform characteristics at the switch terminals. These characteristics may include zero-voltage switching (ZVS) of the semiconductor switch and zero dv/dt across the switch at switch turn on (it is recognized that highest efficiency operation may occur for other tuning objectives, however).

3) Achieving the Important Characteristics of Z_{ds}: The next step in the tuning process is selecting C_P, which includes any capacitance of the semiconductor not used as part of C_F in the previous tuning step. In a design in which the reactance X_S is positive (inductive tuning), the impedance of C_P dominates the high-frequency portion of the impedance Z_L in Fig. 3 (e.g., see Fig. 7). In this case, the impedance Z_L will look capacitive at low frequencies (for $0 \le \omega \le (1/\sqrt{L_S C_S})$), inductive near the fundamental of the switching frequency $((1/\sqrt{L_S C_S}) \le \omega \le (1/\sqrt{L_S C_P}))$, and capacitive again somewhere in between the fundamental and the third harmonic. Increasing C_P reduces the impedance Z_L (and Z_{ds}) at the third harmonic.

Looking into the drain node of the Φ_2 inverter, the relative magnitudes of the impedance Z_{ds} at the fundamental and the third harmonic of the switching frequency determine how large these components are going to be in the drain to source voltage $v_{ds}(t)$. Thus, the ratio of the impedance magnitudes of Z_{ds} at these frequencies has a direct impact on the maximum voltage across the semiconductor. Alternatively, the impedance ratio can be varied by making changes to the impedance at the fundamental driving frequency. For typical designs, the impedance at this frequency is determined by $j\omega L_F||(jX_S + R_{\mathrm{LOAD}})$.

The zero-voltage turn-on condition on the MOSFET occurs when the net impedance Z_{ds} is inductive at the fundamental (having somewhere between 30 and 60 degrees of phase). Because the proposed initial tuning of Z_{MR} achieved by (2) peaks at the fundamental (ideally, at $\omega = \omega_s$, $|Z_{MR}| \rightarrow \infty$), the impedance Z_L dominates Z_{ds} at this frequency. Although $\mathrm{X_S}$ is designed to look inductive at this frequency, the phase angle of $\mathrm{X_S}$ may be too small to achieve ZVS. The phase angle of Z_{ds} at the fundamental can be increased by reducing $\mathrm{L_F}$, an action that will also increase the frequency at which Z_{MR} peaks. Moreover, reducing the value of $\mathrm{L_F}$ will speed the transient response of the converter, but this consideration is secondary to the tuning process. Note that $\mathrm{C_P}$ and $\mathrm{L_F}$ may be adjusted iteratively to achieve the desired characteristics.

In the proposed Φ_2 inverter of Fig. 3, $\mathrm{L_F}$ acts as a resonant inductor. At driving frequencies in the VHF range, $\mathrm{L_F}$ has a very small numerical value and low energy storage as compared to the rf choke found in many inverters such as the traditional class E inverter [2], [10].

To summarize, the steps in the tuning process of a Φ_2 inverter are as follows.

1) Select the reactance $\mathrm{X_S}$ to deliver the desired output power. For the case in which $\mathrm{X_S}$ is inductive, $\mathrm{C_S}$ only provides dc blocking.
2) Starting with a suitable value for $\mathrm{C_F}$ use (2) to obtain values for $\mathrm{C_{MR}}$, $\mathrm{L_{MR}}$, and $\mathrm{L_F}$. With these values Z_{MR} will peak at the fundamental and third harmonic of the switching frequency and will have a null impedance at the second harmonic.
3) $\mathrm{C_P}$ is selected to attenuate the impedance Z_{ds} at the third harmonic, to achieve a ratio between the fundamental and the third harmonic of 4–8 dB. This ratio has a direct impact on the maximum drain to source voltage during operation of the inverter.
4) If necessary, $\mathrm{L_F}$ is reduced from its nominal value found using (2), to increase the phase angle of Z_{ds} at the fundamental. A phase angle between 30 and 60° results in ZVS. Reducing $\mathrm{L_F}$ increases circulating currents in the network and can have an adverse effect on the performance of the inverter.

These tuning goals can be met under a broad range of conditions and for a wide range of switch parasitic capacitance (which is absorbed as part of the resonant network). This provides a high degree of design flexibility that does not exist in the class E inverter. One consequence of this is that it is possible to realize Φ_2 inverter designs (for a specified power and switch capacitance) at much higher frequencies than can be achieved with a traditional class E inverter. Furthermore, because the individual inductive components (including $\mathrm{L_F}$) can be resonant elements having small energy storage, no bulk rf choke is required. Consequently, the Φ_2 inverter can provide rapid dynamic response (e.g., to variations in input voltage and to on/off control).

V. Φ_2 Experimental Demonstration

The Φ_2 resonant inverter introduced here provides low device stresses, eliminates the need for a bulk input inductor, and provides a greater degree of design flexibility than conventional designs such as the Class E resonant inverter. To show the trade offs involved in the design of the Φ_2 inverter, this section describes the step-by-step tuning process of a 30-MHz Φ_2 inverter designed to deliver up to 520 W to a 33.3 Ω resistive load and over an input voltage range between 160 V to 200 V.

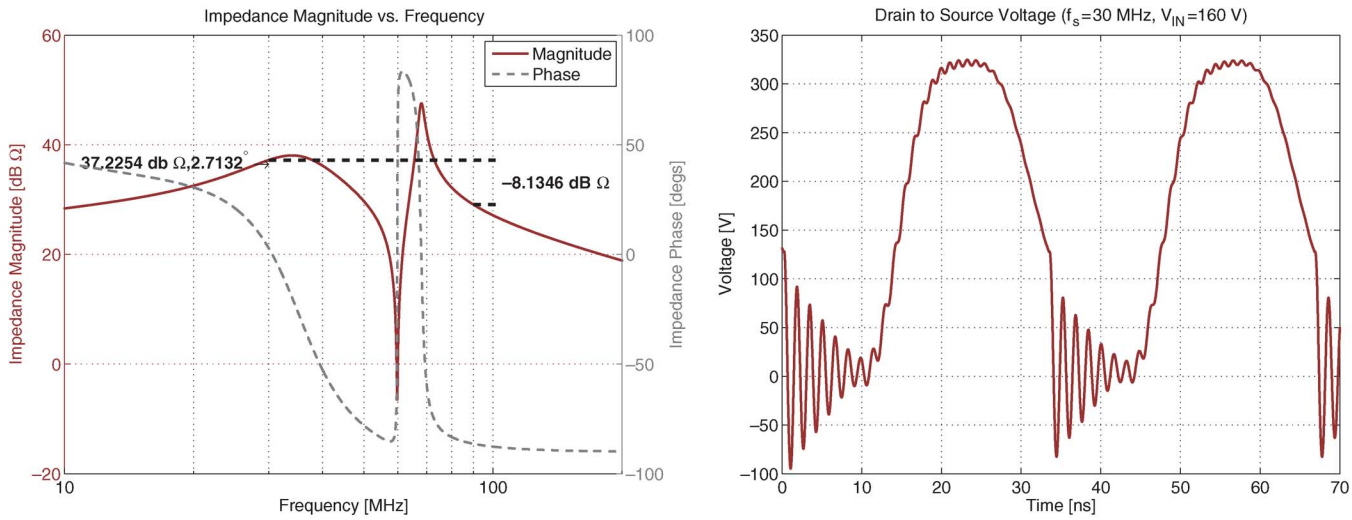
The semiconductor switch selected for this design is a 500 V vertical MOSFET (ARF521) which has an $\mathrm{R_{ds,ON}} = 1\ \Omega$ and an $\mathrm{C_{OSS}} = 55.42$ pF at $V_{ds} = 160$ V. Details on the modelling of the semiconductor in the simulation results presented here can be found in [30], [31]. For this design the MOSFET's duty cycle is selected to be 0.3.

We begin by calculating the value of the components forming $\mathrm{X_S}$. In this design, $\mathrm{X_S}$ will be designed to look inductive at the switching frequency. For an output power of 275 W when $\mathrm{V_{IN}} = 160$ V, with $\mathrm{R_{LOAD}} = 33.3\ \Omega$, we use (1) and set $X_S = 2\pi f_s \cdot L_S$. With this choice, and at a switching frequency of 30 MHz, $\mathrm{L_S} = 198.8$ nH. The value of $\mathrm{C_S}$ is selected to provide dc blocking and to have a low impedance when compared to the the series combination of $\mathrm{L_S}$ and $\mathrm{R_{LOAD}}$. This can be achieved with a capacitor $\mathrm{C_S} = 4$ nF. (Note that making the value of $\mathrm{C_S}$ excessively large can have a detrimental impact on the transient response of the inverter in certain applications.)

The elements comprising Z_{MR} are initially tuned according to (2) to peak at the fundamental and third harmonic and to have a zero in impedance at the second harmonic of the switching frequency. To minimize the circulating current throughout the resonant elements of the inverter, we calculate the value of the components of Z_{MR} assuming a value of $\mathrm{C_F} = 20$ pF, which for a switching frequency of 30 MHz results in $\mathrm{L_F} = 625.4$ nH, $\mathrm{L_{MR}} = 375.3$ nH and $\mathrm{C_{MR}} = 18.8$ pF. Here, the value of $\mathrm{C_F}$ (20 pF) was selected to be lower than the switch capacitance at the operating voltage ($\mathrm{C_{OSS}} = 55.4$ pF at $V_{DS} = 160$ V) to reduce the circulating currents throughout the Z_{MR} network. The remaining 35.4 pF of the switch capacitance forms part of $\mathrm{C_P}$ and contributes to the shape of the drain voltage waveform.

Fig. 7 shows the simulated magnitude of the impedances Z_L, Z_{MR} and the resultant drain impedance Z_{ds} as a function of frequency at this point in the tuning process. Here, $\mathrm{C_P}$ includes the remainder of the MOSFET capacitance and 40 pF of external capacitance needed to achieve the desired attenuation at the third harmonic of f_s.[1] Notice that while the magnitude of the impedance Z_{MR} peaks at 30 MHz and 90 MHz, it has a null at 60 MHz. Because $Z_{ds} = Z_{MR}||Z_L$, the maxima of the magnitude of Z_{ds} will not necessarily correspond to the maxima of

[1]Clearly, $\mathrm{C_P}$, $\mathrm{C_{FEXTRA}}$ and the switch capacitance are in parallel; however, we "assign" different portions of this to the sub-networks of the circuit for case of adjusting the design. The reader may choose to consider only the total capacitance and achieve the same result.



(a) Impedance plot (b) Time domain

Fig. 8. (a) Shows the magnitude and phase of Z_{ds} versus frequency. (b) Shows a transient simulation of v_{ds} of the Φ_2 inverter. Here, $\mathrm{V_{IN}} = 160\,\mathrm{V}$, $\mathrm{f_s} = 30\,\mathrm{MHz}$ and with a duty cycle of 0.3. Components values are: $\mathrm{L_F} = 625.4\,\mathrm{nH}$, $\mathrm{C_{MR}} = 18.8\,\mathrm{pF}$, $\mathrm{L_{MR}} = 375.3\,\mathrm{nH}$. $\mathrm{L_S} = 198.8\,\mathrm{nH}$, $\mathrm{R_{LOAD}} = 33.3\,\Omega$, $\mathrm{C_S} = 4\,\mathrm{nF}$, $\mathrm{C_P} = 75.4\,\mathrm{pF}$ (35.4 pF remaining from the switch plus 40-pF external capacitance). The MOSFET capacitance is modeled as $C_{oss} = C_0/(1 + (v_{ds}/\psi_0))^m$ with values that change dynamically as follows: $C_0 = 2478\,\mathrm{pF}$, $\psi_0 = 1.088\,\mathrm{V}$, $\mathrm{m} = 0.6946$ for $0 \le v_{ds}(t) < 14.5\,\mathrm{V}$ and $C_0 = 2478\,\mathrm{pF}$, $\psi_0 = 0.38\,\mathrm{V}$, $\mathrm{m} = 0.6285$ for $14.5 \le v_{ds}(t) \le 500\,\mathrm{V}$. Parasitic components for the time-domain simulation also include parasitic inductances in the MOSFET (1.5 nH at the drain, 1 nH at the source). (a) Impedance plot. (b) Time domain.

either Z_{MR} or Z_L, so the designer has to be aware of the impact that changes on each component can have in the overall impedance Z_{ds}.

To better appreciate the resulting impedance looking into the drain node of the inverter, Fig. 8(a) shows the magnitude and phase of the impedance Z_{ds} of this example at this stage of the tuning process. The figure shows that at the fundamental of the switching frequency, Z_{ds} has a magnitude of 37.2 $\mathrm{dB}\Omega$ and 2.7° of phase. Although the phase angle is positive, 2.7° of phase is not inductive enough to ensure ZVS for the selected duty ratio. This can clearly be seen in Fig. 8(b) which shows a transient simulation of a Φ_2 inverter with the values obtained so far. Notice that the drain voltage is near 125 V right before the MOSFET turns on.

Reducing the value of $\mathrm{L_F}$ from the value selected initially shifts the first peak of Z_{MR} to a higher frequency; this makes the net Z_{ds} look more inductive at the fundamental. Reducing $\mathrm{L_F}$ in this manner is a way to achieve the ZVS operation of the Φ_2 inverter. Fig. 9 shows the impedances Z_L, Z_{MR} and the drain impedance Z_{ds} of the inverter when the value of $\mathrm{L_F}$ is reduced from 625.24 to 270 nH. Notice that the impedance peaks of the magnitude of Z_{MR} are no longer at the fundamental and third harmonic of the switching frequency, but are significantly higher in frequency.

The effects of the reduction in the value of $\mathrm{L_F}$ can be better appreciated in Fig. 10(a), which shows that with a smaller value of $\mathrm{L_F}$, the phase angle of the impedance at the fundamental is now 40.6°, with a magnitude of 34.8 $\mathrm{dB}\Omega$. Under this conditions ZVS is achieved as can clearly be seen in the transient simulation of Fig. 10(b). The models in the simulation results include parasitic elements in most of the components, which are responsible for the high-frequency oscillations on $v_{ds}(t)$ when the MOSFET is on. Furthermore, the simulation accounts for the non-linear capacitance of the semiconductor device (ARF521 MOSFET) chosen for the design.

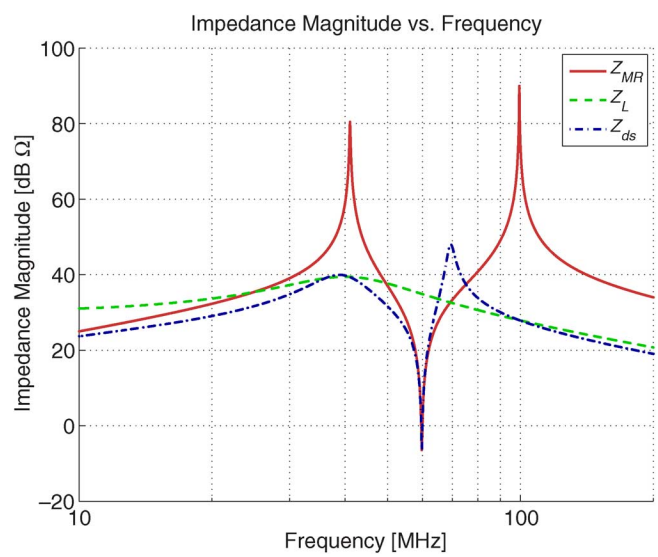
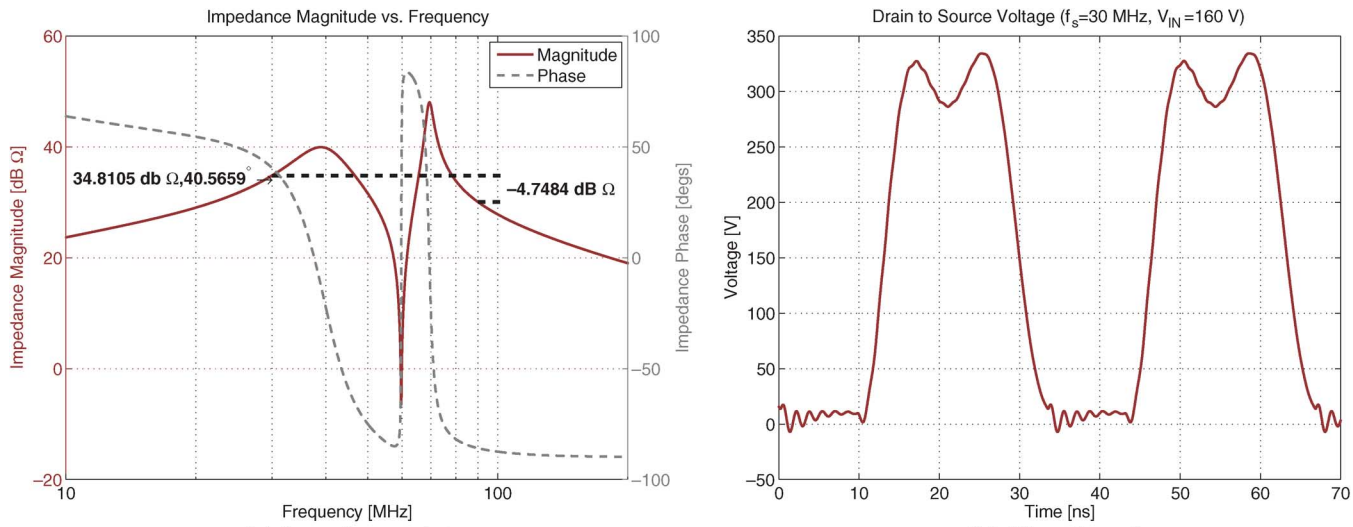


Fig. 9. Magnitude of the impedances Z_{MR}, Z_L and Z_{ds} the class Φ_2 inverter. For this example $\mathrm{C_F} = 20\,\mathrm{pF}$, $\mathrm{L_F} = 270\,\mathrm{nH}$, $\mathrm{C_{MR}} = 18.8\,\mathrm{pF}$, $\mathrm{L_{MR}} = 375.3\,\mathrm{nH}$. $\mathrm{L_S} = 198.8\,\mathrm{nH}$, $\mathrm{C_S} = 4\,\mathrm{nF}$, $\mathrm{R_{LOAD}} = 33.3\,\Omega$, $\mathrm{C_P} = 75.4\,\mathrm{pF}$ (35.4 pF remaining from the switch plus 40 pF external capacitance). Notice that the peaks in Z_{MR} are now at higher frequencies.

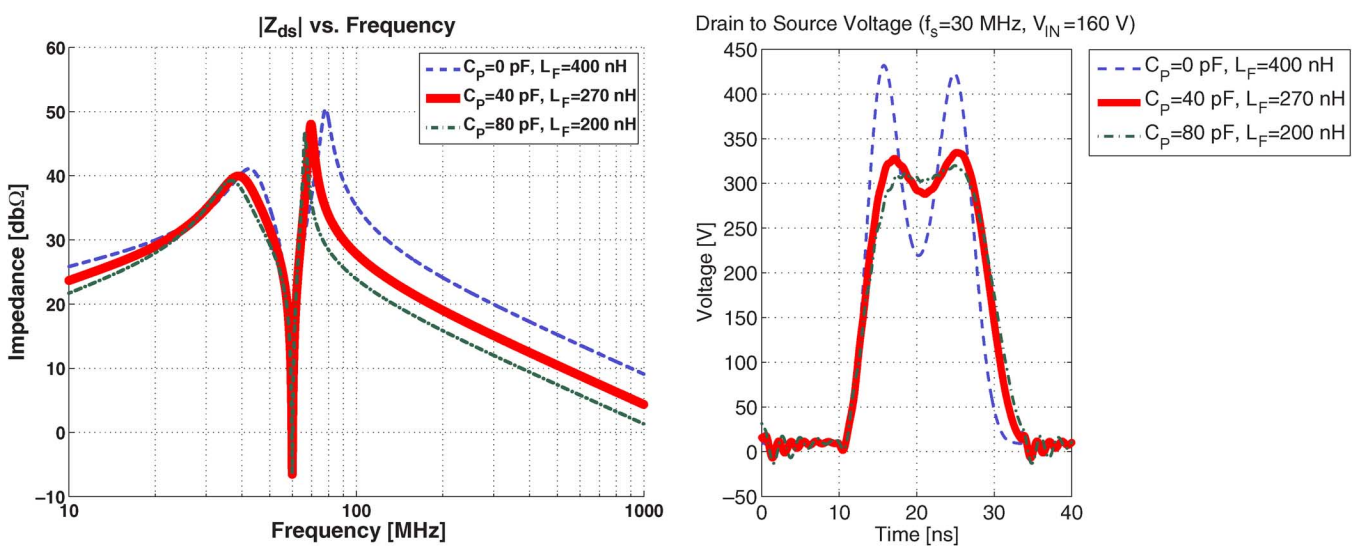
1) Importance of the Relative Impedance Ratio at the Fundamental and Third Harmonic: The ratio between the impedance magnitude at the fundamental and the third harmonic Z_{ds} has a direct impact on the shape of the drain voltage. In particular, this ratio determines the peak voltage across the MOSFET. For the simulation results shown in Fig. 10(a), this ratio is 4.75 dB.

To demonstrate the effects that the impedance ratio has on the performance of the Φ_2 inverter, we simulated the inverter



(a) Impedance plot (b) Time domain

Fig. 10. (a) Shows the magnitude and phase of Z_{ds} vs. frequency. (b) Shows a transient simulation of v_{ds} of the Φ_2 inverter. Here, $\mathrm{V_{IN}} = 160\,\mathrm{V}$, $\mathrm{f_s} = 30\,\mathrm{MHz}$ and with a duty cycle of 0.3. Components values are: $\mathrm{L_F} = 270\,\mathrm{nH}$, $\mathrm{C_{MR}} = 18.8\,\mathrm{pF}$, $\mathrm{L_{MR}} = 375.3\,\mathrm{nH}$. $\mathrm{L_S} = 198.8\,\mathrm{nH}$, $\mathrm{R_{LOAD}} = 33.3\,\Omega$, $\mathrm{C_S} = 4\,\mathrm{nF}$, $\mathrm{C_P} = 75.4\,\mathrm{pF}$ (35.4 pF remaining from the switch plus 40-pF external capacitance). The MOSFET capacitance is modelled as $C_{oss} = C_0/(1 + (v_{ds}/\psi_0))^m$ with values that change dynamically as follows: $C_0 = 2478\,\mathrm{pF}$, $\psi_0 = 1.088\,\mathrm{V}$, $\mathrm{m} = 0.6946$ for $0 \leq v_{ds}(t) < 14.5\,\mathrm{V}$ and $C_0 = 2478\,\mathrm{pF}$, $\psi_0 = 0.38\,\mathrm{V}$, $\mathrm{m} = 0.6285$ for $14.5 \leq v_{ds}(t) \leq 500\,\mathrm{V}$. Parasitic components for the time-domain simulation also include parasitic inductances in the MOSFET (1.5 nH at the drain, 1 nH at the source). (a) Impedance plot. (b) Time domain.



(a) Impedance magnitude (b) Time domain

Fig. 11. (a) Shows the magnitude of Z_{ds} vs. frequency for different tuning having the same impedance magnitude at the fundamental frequency, but different impedance magnitudes at the third harmonic. These characteristics were achieved by selecting different values for $\mathrm{C_P}$ and keeping the impedance magnitude at the fundamental constant by adjusting L_F. (b) Shows how $v_{ds}(t)$ changes as the impedance ratio between the magnitude at the fundamental and the third harmonic is varied. The thicker line highlights the actual design selected for the prototype system. (a) Impedance magnitude. (b) Time domain.

presented in the previous subsection with different values of capacitance $\mathrm{C_P}$ and inductance $\mathrm{L_F}$. By varying $\mathrm{C_P}$, we lower the impedance at the third harmonic, while keeping the impedance at the switching frequency constant by adjusting the value of $\mathrm{L_F}$. Fig. 11 summarizes the results of this process. Fig. 11(a) shows the magnitude of the drain impedance when the discrete component of capacitance $\mathrm{C_P}$ (in addition to the 35.4 pF contribution of the switch beyond the 20 pF considered as $\mathrm{C_F}$) is 0, 40, and 80 pF. $\mathrm{L_F}$ here is 400, 270, and 200 nH, respectively. Fig. 11(b) shows the resulting $v_{ds}(t)$. Notice how the relative impedance magnitudes relate to the peak voltage at the drain.

2) Summary of the Inverter Design: Table I shows the component values of the Φ_2 inverter presented here. The switching frequency is 30 MHz, with and input voltage going from 160 to 200 V.

A. Inverter Implementation

A prototype inverter based on the design presented above is described here. It was constructed on a printed circuit board (PCB) (2-layer, 1 oz. copper, FR4 material). Of particular importance during the fabrication of the prototype is the accurate determination of the drain impedance Z_{ds}. This measurement is

TABLE I
LIST OF COMPONENTS FOR THE 30 MHz, Φ_2 INVERTER. THE EXTERNAL 40 pF DRAIN TO SOURCE CAPACITANCE FORMS PART OF C_P. FOR THE DESIGN PRESENTED HERE $C_P = 75.4$ pF FROM WHICH 35.4 pF COME FROM THE SWITCH CAPACITANCE NOT FORMING PART OF $C_F = 20$ pF

Component	Value
L_F	270 nH
MOSFET	ARF521 C_{oss}=55.42 pF @ v_{ds}=160 V C_{oss}=48.23 pF @ v_{ds}=200 V
L_{MR}	375.3 nH
C_{MR}	18.8 pF
External drain-source capacitance	40 pF
C_S	4 nF
L_S	198.8 nH
R_{LOAD}	33.3 Ω

done using an impedance analyzer connected to the drain node (through an SMA connector) and in series with a DC blocking capacitor C_{BIAS} (such that the drain node can be biased to an appropriate voltage). The impedance analyzer is calibrated to compensate for the introduction of a 6 in., 50 Ω coaxial cable between the instrument head and the PCB under study. The calibration offers an accurate measure of the impedance up to a frequency of about 400 MHz.

The nonlinear dependance of the MOSFET's drain to source capacitance on voltage requires biasing the drain node to the nominal input voltage when measuring the impedance. The input voltage of the inverter $(160\ \mathrm{V} \leq V_{IN} \leq 200\ \mathrm{V})$ exceeds the biasing limits of the impedance analyzer available (Agilent 4395A, with ±40 V dc range.). Therefore, to allow for dc bias and protection of the analyzer, it is necessary to add a capacitor C_{BIAS} between the analyzer and the drain node. The role played by this capacitor is twofold: it prevents the dc voltage from reaching the measuring test point of the analyzer and holds the voltage across C_{BIAS} constant throughout the measurement. It is essential the impedance of C_{BIAS} be negligible when compared to the impedance of the drain node at a biased point. The length of the frequency sweep interval of the impedance analyzer is selected to be short enough so that no significant drop in bias voltage is observed.

The impedance Z_{ds} of the Φ_2 inverter design developed in this section, has the frequency dependance shown in Fig. 10(a). In the light of the above considerations, the impedance of C_{BIAS} is chosen to be ten times smaller than the Φ_2 design at 30 and 90 MHz. The impedance magnitude at these frequencies is 34.81 dBΩ and 30.06 dBΩ respectively. A 250 V, 1 μF ceramic capacitor (CKG57NX7R2E105M) meets these requirements.

The values of resonant inductors L_F, L_{MR}, and L_S (shown in Table I) are small and can each be implemented with a few turns of magnet wire. The air-core inductors built for this inverter have quality factors Q_L larger that those assumed in the design summarized in Table I. To ensure mechanical stability and repeatability, the inductors were wound on threaded Teflon cylinders.

TABLE II
LIST OF COMPONENTS FOR THE 30 MHz, 160 V TO 200 V Φ_2 PROTOTYPE INVERTER

Part	Measured Value	Q	Part number
L_F	306 nH	194	8 turns of AWG 16 wire on a 3/8 in. diam. Teflon rod with 14 turns/in. threads
C_F	Device capacitance		ARF521
L_{MR}	414 nH	280	9 turns AWG 16 wire on a 3/8 in. diam. Teflon rod with 14 turns/in. threads
C_{MR}	16.29 pF	10 K 10 K	2x56 pF ATC100B560JW 1x39 pF ATC100B390JW
C_P C_S	28.065 pF 2 nF	 3 K	Parasitic drain capacitance 2x1 nF MC22FD102J-F
L_S	193 nH	190	4 turns AWG 16 wire on a 5/8 in. diam. Teflon rod with 12 turns/in. threads
R_{LOAD}	≈ 33.3 Ω		3 parallel 100 Ω RA1000-150-4X
C_{bias}	1 μF		CKG57NX7R2E105M
C_{IN}	4 μF		4x CKG57NX7R2E105M

1) Placement of Resonant Elements: The first step in the construction of the prototype was the placement of the second harmonic resonator (formed by C_{MR} and L_{MR}). These components were tuned to resonate at the second harmonic of the switching frequency. Inductor L_{MR} was fabricated with 9 turns of AWG16 magnet wire on a 3/8 in. diameter Teflon rod with 14 turns/inch threads. Then, we added a $C_{MR} = 16.3$ pF capacitor in series with the inductor. The series network formed by L_{MR} and C_{MR} was found resonant at a frequency of 61.3 MHz. Hence, the effective value of L_{MR} is 414 nH. An important consideration in the layout of the PCB is the peak voltage across capacitor C_{MR}, which can reach 1.25 kV at $V_{IN} = 200$ V. Therefore, C_{MR} was implemented by connecting three 500-V porcelain capacitors in series. To avoid adding parasitic capacitance here, no ground plane was placed (on the other side of the board) below the midpoint connection of the $C_{MR} - L_{MR}$ tank.

Once the second harmonic leg was in place, the MOSFET and the rest of of the passive components were placed on the PCB. Throughout the placement of the resonant components of the inverter, the ARF521 gate and source were shorted using a low inductance connection. Hence, measurement of the drain-source impedance Z_{ds} included switch capacitance C_{oss}.

Table II shows the designed and measured values of all passive components of the inverter.

Fig. 12 shows a photograph of the prototype with all the inverter components in place. In order to keep the loop area of the input to a minimum, the inductor L_F was placed across the top of the ARF521.

The Φ_2 inverter delivers power to a resistor implemented by paralleling three 100 Ω RF power resistors, each rated to 150 W. Fig. 13 shows the PCB of the load network with the

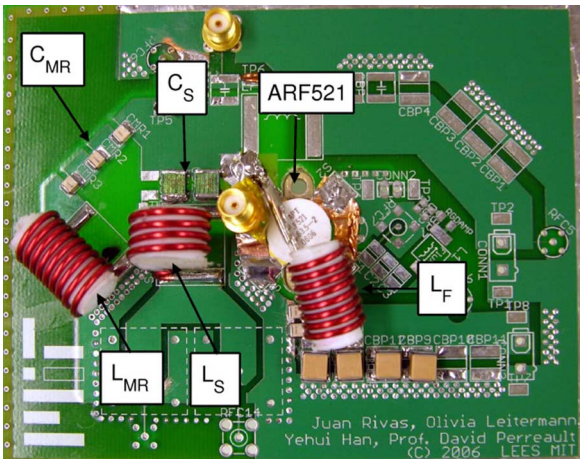


Fig. 12. Experimental class Φ_2 inverter.

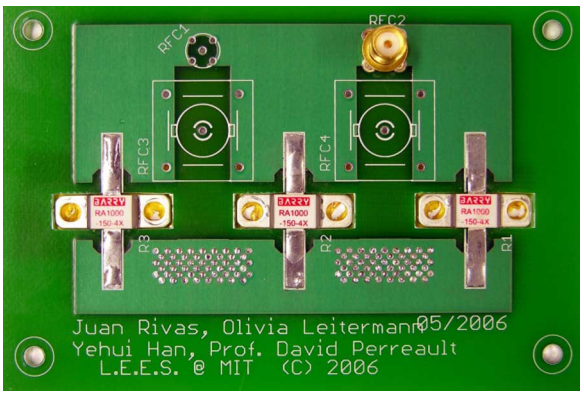


Fig. 13. RF load.

resistors placed symmetrically. The connection between the inverter stage and the RF Load was made using two 75 Ω coaxial cables in parallel. A subsequent section shows a detailed characterization of the load across frequency, and at the operating temperature.

2) Verification of the Impedance Z_{ds}: With the voltage of capacitor C_{BIAS} held to V_{IN}, we proceed to compare the measured impedance Z_{ds} to the one obtained by simulation using PSPICE with the values obtained in Table. II. Fig. 14 shows the magnitude of Z_{ds} when V_{IN} is 160 V. The difference between measurement and simulation in the frequency range between 70 and 80 MHz is due to the gate to drain capacitance C_{gd} and the gate-to-source inductance. C_{gd} is not included separately in the PSPICE model of the MOSFET but is rather treated as part of the device output capacitance C_{OSS}.

3) Implementation of the Gate Drive: The inverter operates with a constant duty cycle of approximately 0.3. The gate of the ARF521 MOSFET used here is driven sinusoidally by an RF power amplifier having 50 Ω output impedance (Amplifier Research 150A100B) with a dc offset on the gate voltage. Fig. 15 shows a schematic of the gate drive circuit where $V_{G,DC}$ is a dc voltage that controls the duty cycle. Capacitor $C_{G,RF} = 5$ nF presents a low impedance to the RF signal coming from the power amplifier. The inductor $L_{G,DC} = 568$ nH and $R_{G,DC} = 10$ kΩ prevent the RF signal from reaching the auxiliary supply $V_{G,DC}$.

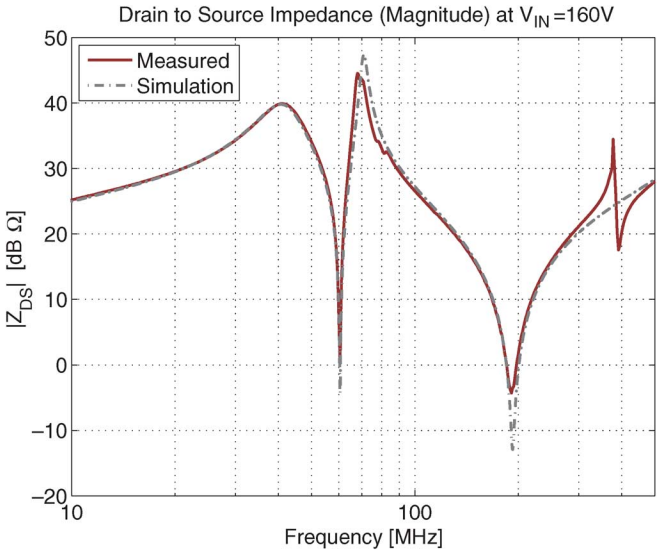


Fig. 14. Drain to source impedance versus frequency when $V_{IN} = 160$ V.

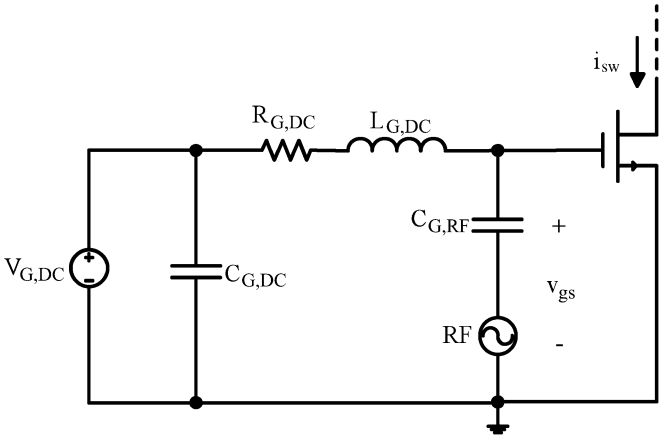


Fig. 15. Gate drive circuit schematic. In this prototype, $R_{G,DC} = 10$ kΩ $L_{G,DC} = 568$ nH and $C_{G,RF} = 5$ nF. The RF source is a 50 Ω-output power amplifier.

The impedance between gate and source of the ARF521 is modelled as a series resonant circuit, with $R_G = 0.116$ Ω, $C_{iss} = 920$ pF, and $L_G = 2.6$ nH. The measurement accounts for the gate and source lead inductances.

When a sine wave is used to drive the gate of the MOSFET, the power lost in the gate is (ideally) $P_{GATE} = 2\pi^2 f_s^2 V_{g,ac}^2 C_{iss}^2 R_G$. For $V_{g,ac} = 12$ V, the power lost at the gate is just $P_{GATE} = 251$ mW, which is negligible compared to the output power of the inverter.

B. Experimental Performance of the Inverter

The inverter and load were each mounted to appropriate heat sinks. In particular, the RF load was mounted on an aluminum heat-sink with two fan-cooled copper heat-sinks (type Zalman CNPS7700-Cu) also mounted to it to improve heat transfer. In thermal steady state, the net thermal impedance seen by the resistive load was found to be 0.2°C/W. The inverter MOSFET was mounted on a fan-cooled aluminum heat-sink with a thermal resistance of 0.5°C/W (Cooler-Master HAC-L82). This heat-sink was deliberately oversized to ensure acceptable

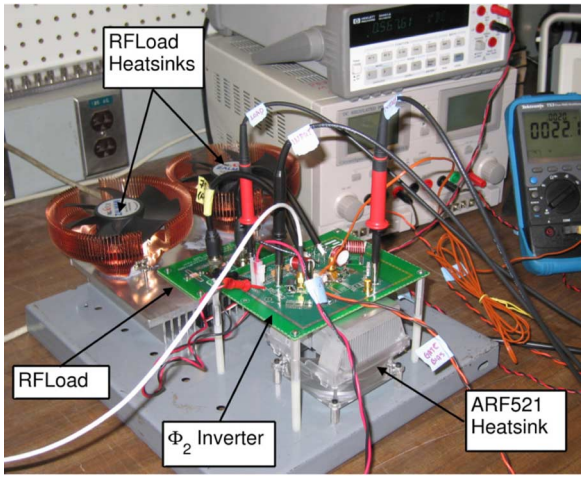


Fig. 16. Experimental class Φ_2 inverter connected to the RF load.

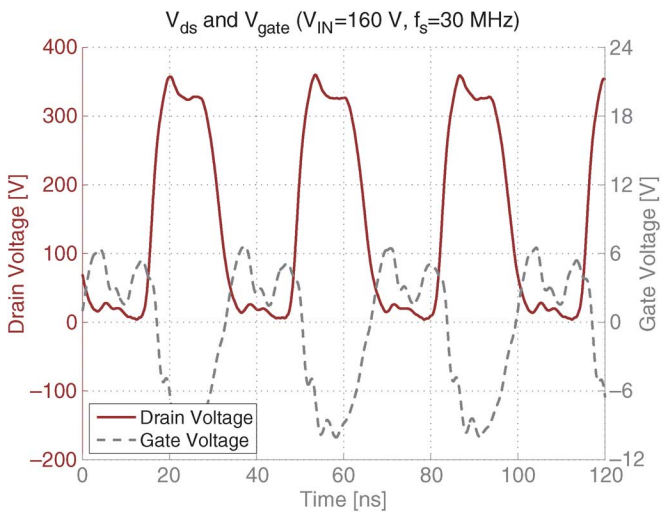


Fig. 17. Drain to source and gate voltage with $V_{IN} = 160$ V. Note that the (external) measured gate voltage does not precisely reflect the voltage at the gate due to parasitic inductance in the device leads.

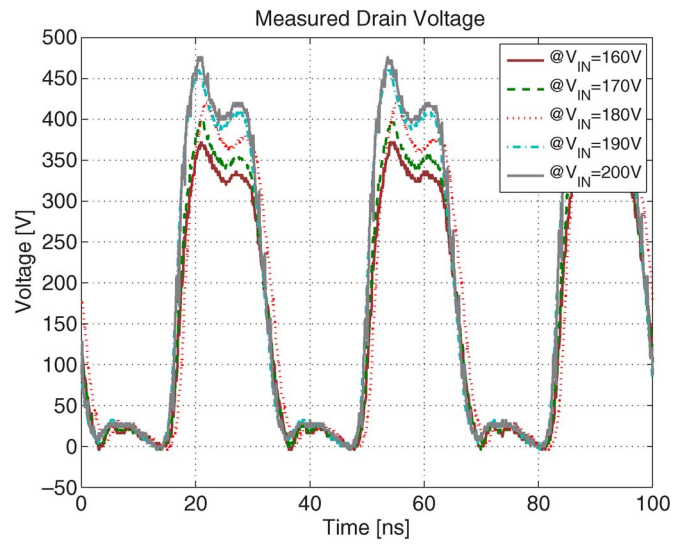


Fig. 18. Drain to source voltage for $160\ \mathrm{V} \leq V_{IN} \leq 200\ \mathrm{V}$. The peak drain voltage to input voltage ratio is $\simeq$2.4.

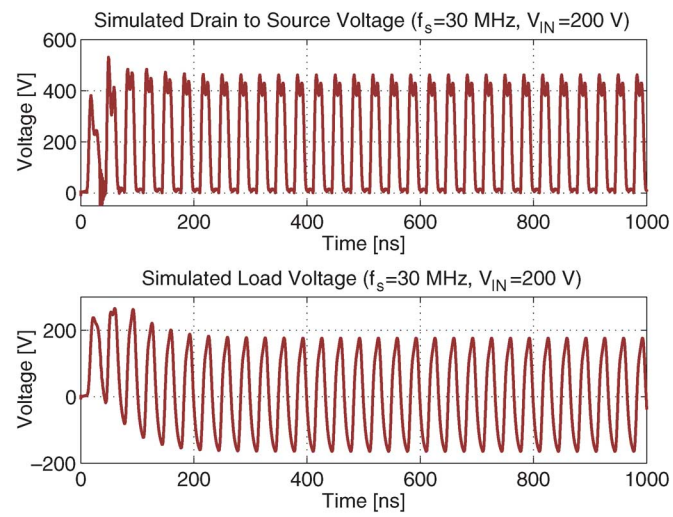


Fig. 19. Simulated transient response to initiation of gate drive signal. The top plot in the figure shows the drain to source voltage $v_{ds}(t)$ while the bottom plot the load voltage $v_{\mathrm{load}}(t)$. Steady state is achieved within ten switching cycles.

temperature rise on the inverter board even if the inverter did not operate as desired. The prototype inverter and load are shown in Fig. 16.

The measured drain to source voltage $v_{ds}(t)$ of the Φ_2 inverter is shown in Fig. 17 as well as the voltage at the MOSFET's gate (with $V_{IN} = 160$ V). The figure clearly shows ZVS condition and the expected waveshaping outlined in Section III. Fig. 18 shows experimental measurements of $v_{ds}(t)$ as the input voltage is varied over the $160\ \mathrm{V} \leq V_{IN} \leq 200\ \mathrm{V}$ range. The peak voltage across the switch is significantly smaller than the voltage obtained by conventional circuits (Class E, second harmonic Class E). The peak $v_{ds}(t)$ to V_{IN} ratio measured over the entire input range is approximately 2.4. Fig. 19 shows the simulated $v_{ds}(t)$ and $v_{\mathrm{load}}(t)$ response of the inverter to initiation of gate drive. It can be seen that steady-state performance is reached within ten switching cycles.

Fig. 20 illustrates the excellent agreement that exists between measurement and PSPICE simulation for the case when $V_{IN} = 160$ V. $v_{ds}(t)$ is shown on the left of the figure, while the load voltage $v_{\mathrm{load}}(t)$ is shown on the right.

C. Output Power Measurements and Performance

Measuring ac power at 30 MHz is difficult in RF systems, especially at impedance levels different from 50 Ω. To accurately measure the power delivered to the load, we obtained the frequency components of the voltage across the RF load and computed the power delivered at each harmonic frequency. To do this, we measured the impedance of the RF load across frequency and temperature. A plot of the load impedance in the frequency range between 1 and 400 MHz (at 25°C) is shown in Fig. 21. The measured value of the static thermal coefficient of the load was 4.23 $\mathrm{m}\Omega/^{\circ}\mathrm{C}$. We scaled the real part of the load impedance to account for the temperature increase of the load during operation of the inverter. We made the simplifying assumption that the effect of the thermal coefficient was constant with frequency.

Fig. 22 shows the voltage across the RF resistive load, and the magnitude and phase of the first 9 harmonic components. With

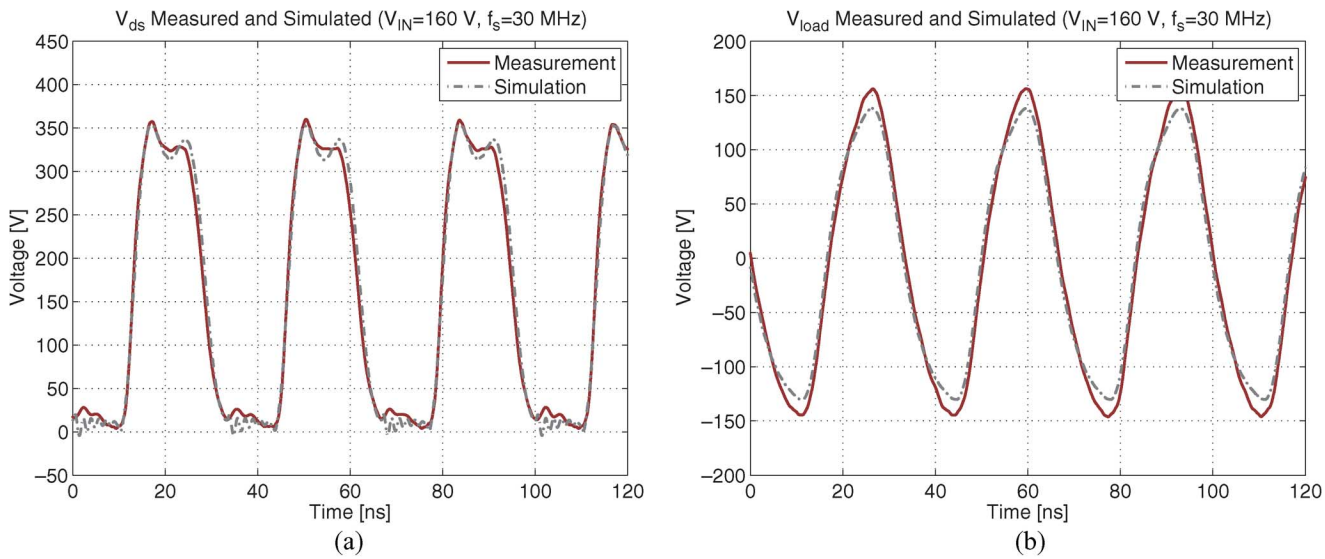


Fig. 20. Comparison between experimental measurements and simulation: (left) drain to source voltage, (right) load voltage. Both plots at $\mathrm{V_{IN}} = 160$ V. (a) $v_{ds}(t)$. ; (b) $v_{\mathrm{load}}(t)$.

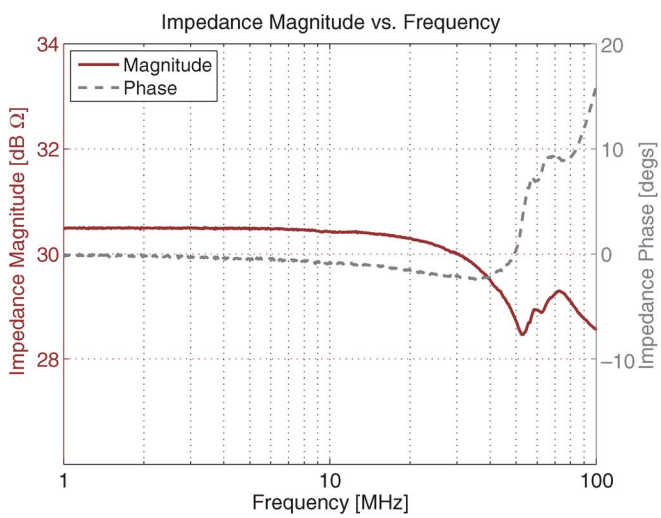


Fig. 21. Magnitude and phase versus frequency of the impedance of the RF load connected to two parallel 75 Ω coaxial cables of the same length.

the harmonic content, the impedance of the load, and the load temperature, the output power can be estimated with reasonable accuracy.

The output power and drain efficiency of the converter over the input voltage range are shown in Fig. 23. All the voltage measurements were made when the temperature of the load resistor reached 100°C. The drain efficiency[2] is over 92% over the operating range.[3] The performance of the prototype Φ_2 inverter demonstrates the high performance achievable with this approach.

[2]Drain efficiency [21] is defined as $P_{\mathrm{OUT}}/P_{DC,IN}$, and hence does not include gate drive loss. Total efficiency is defined as $P_{\mathrm{OUT}}/(P_{DC,IN}+P_{\mathrm{GATE}})$. As our gating loss (with resonant gating [9] is estimated to be much less than 5 W, the measured drain efficiency is quite close to total efficiency.

[3]Subsequent measurements on this converter made by colleagues at the University of Colorado at Boulder yielded efficiencies improvements of several percent with an improved gate drive.

D. Comparison to a Class E Inverter

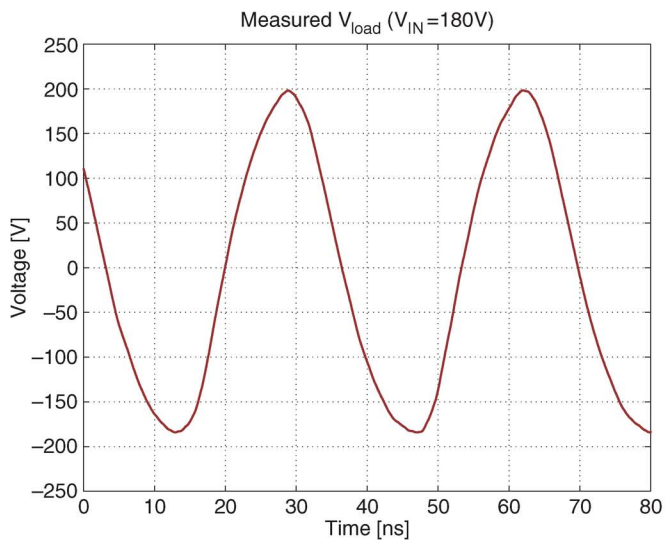
The Φ_2 inverter breaks the tight relation between frequency, output power and device capacitance characteristic of the class E topology, and allows operation at higher switching frequencies with lower voltage devices. This is demonstrated in the prototype design presented here in which utilizing the selected (ARF521 500-V breakdown) MOSFET rules out the use of a class E inverter topology to meet the required specifications:

- The peak voltage stress of a class E inverter $(> 3.6\mathrm{V_{IN}})$ exceeds the breakdown voltage rating of the MOSFET.
- The capacitance at the drain of the AF521 is ≈95 pF when $\mathrm{V_{IN}} = 160$ V and the device is mounted on a PCB board. Under these conditions, the maximum switching frequency for a conventional class E inverter designed to deliver 320 W at $\mathrm{V_{IN}} = 160$ V is ≈6.9 MHz, well below the switching frequency achievable by the Φ_2 example design presented here. The maximum switching frequency of a 2nd-harmonic class E inverter under the same conditions is ≈27.7 MHz.

The performance of the prototype Φ_2 inverter demonstrates experimentally many of the advantages that the topology has over conventional designs. In particular, it demonstrates low-voltage stress, small-valued passive components, and high design flexibility for high-frequency operation.

VI. Conclusion

There is an interest in power electronic systems that achieve a greater degree of miniaturization and better dynamic performance than present-day designs. These goals can be achieved through system designs that operate at greatly increased switching frequencies and take advantage of the resulting reductions in internal converter energy storage. This document presents a new switched-mode resonant inverter, which we term the Φ_2 inverter, that is well suited to operation at very high frequencies and to rapid on/off control. Features of this inverter topology include low semiconductor voltage stress, small



Harmonic	Amplitude [V]	Phase
1st	190.7836	0°
2nd	9.3254	216.1937°
3rd	9.6288	−76.4164°
4th	3.5710	113.8763°
5th	0.9197	205.3407°
6th	0.8111	−9.2473°
7th	0.4374	114.4041°
8th	0.0157	146.0846°
9th	0.2094	96.5012°

Fig. 22. Load voltage when $V_{IN} = 180$ V. The table shows the harmonic content of the waveform.

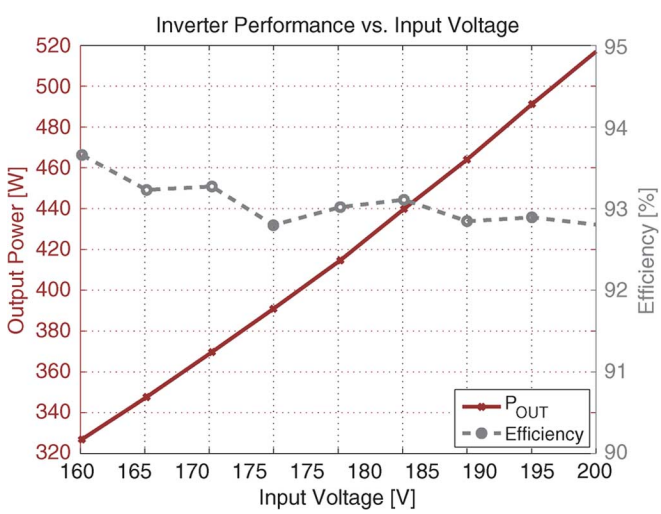


Fig. 23. Output power and drain efficiency versus input voltage for the prototype class Φ_2 inverter.

passive energy storage requirements, fast dynamic response, and high flexibility of design. The structure and operation of the proposed topology are described, and a design procedure is introduced. Experimental results demonstrating the new topology are also presented. It is expected that the Φ_2 inverter will find use as a building block in high-performance dc-dc converters among other applications.

ACKNOWLEDGMENT

The authors would like to thank Prof. C. R. Sullivan, Dr. J. Glaser, and Dr. L. Stevanović for their insights and suggestions during the development of the work described here.

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