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Radio-Frequency Inverters With Transmission-Line Input Networks

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Abstract—A soft-switching inverter topology (the Class Φ) is presented which draws dc source current through a transmission line or a lumped-network approximation of a distributed line. By aligning the inverter switching frequency just below the line's $\lambda/4$-wave resonance, the Class Φ topology enforces odd-and even-harmonic content in its drain voltage and input current, respectively. The symmetrizing action of the transmission-line dynamics results in natural square-wave operation of the switch, reducing the inverter stresses (relative to a Class E) for a given power throughput. The inverter waveforms and normalized power-output capability are analyzed in simple terms, and supported by measurements of an inverter built around a length of distributed line, and an inverter incorporating a lumped L–C ladder network. The latter implementation is constructed with air-core magnetics and inter-layer capacitances that are integrated into the thickness of a printed-circuit board. A comparison with a Class E inverter of similar size and ratings demonstrates the small passive-component values and manufacturing advantages afforded by the Class Φ topology.

Index Terms—Distributed system, inverter, lumped model, transmission line.

I. INTRODUCTION

DRIVEN by the availability of robust, low-loss radio frequency (RF) switches, power conversion at radio frequencies is a promising technique for reducing the volume of passive elements necessary to process power in dc–dc and dc–ac applications. The principal contribution of this paper is the detailed development of a soft-switching inverter (termed the Class Φ) adapted for high switching frequencies, passive miniaturization, and low device stress [1]. The name Class Φ was chosen because of it similarity to "Class F" while avoiding confusions with its variants (Class F inverse, Class EF, . . .). The Class F and Class Φ have fundamentally similar drain waveforms, but the Class Φ runs entirely in switched mode, whereas most practical Class F converters operate under bias, with significant voltage/current overlap that limits efficiency [2]–[10], [11, Ch. 7]. For practical converter designs, switched-mode operation requires that the switch be operated at a duty ratio of less than 50% (35%–40% duty ratios are typical).

The Class Φ topology is depicted in Fig. 1, and is distinguished by the transmission line (or approximating network)
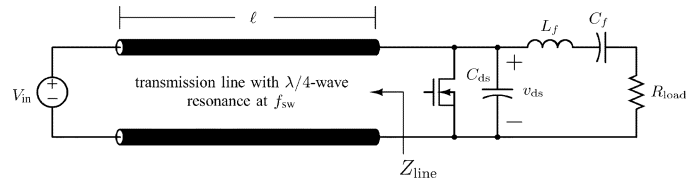

Fig. 1. Schematic of the Class Φ inverter, which draws dc input current through a $\lambda/4$-wave line at its input. A lumped approximating can be substituted for the distributed line.

at its input, through which the switch draws dc source current with switched-mode operation.[1] The harmonically related impedance extrema seen from the drain node through the transmission line (cf. Z_{line} in Fig. 1, see [12] and the Appendix) impose symmetries in the Class Φ waveforms that can be leveraged to reduce switch stresses and improve efficiency. Numerous ancillary issues not elaborated here—notably active adjustment of switching frequency and self-oscillating gate drives—are treated elsewhere [13]–[17].

After a brief discussion of voltage and current symmetries, Section II will present the waveforms of the Class Φ and compare its switch stresses to those of the Class E and Class F. Section III will show measured waveforms of a Class Φ inverter built around a length of distributed line, and Section IV will detail an implementation with a lumped line-simulating network integrated into the thickness of a PCB. The measured performance of the Class Φ inverter in Section IV will be compared to a Class E of similar ratings. This comparison highlights the reduction in passive-component volume achievable with the Class Φ topology which—significantly for miniaturization and control bandwidth—requires no bulky blocking elements. Section V will conclude with refinements to the basic Class Φ design.

II. ANALYSIS OF THE CLASS Φ INVERTER

Transmission lines and lumped resonators have long been incorporated into radio-frequency power amplifiers to improve efficiency and shape circuit waveforms (e.g., [18, Ch. 14] and [2]–[5], [19]), and are beginning to perform a similar roles in high-frequency switched-mode power electronics [14], [15], [20]–[22]. Key requirements for such filtering and shaping structures are reactive (ideally lossless) driving-point impedances with harmonically related maxima and minima. Such aligned peaks and nulls are treated at length in a complementary

[1]Class F power-amplifier variants utilizing a transmission-line analog as an input network have also been proposed [6], [7], [11]. These variants do not operate in a switched mode but in a biased mode, with voltage/current overlap that limits their efficiency compared to the Class Φ.
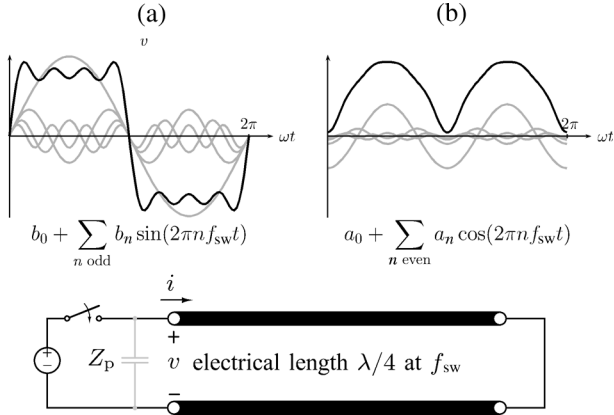
Fig. 2. When excited periodically at a frequency equal to the principle quarter-wave resonance, a transmission line enforces odd- and even-harmonic symmetries in voltage and current, respectively: (a) half-wave symmetric terminal voltage and (b) half-wave repeating terminal current i.

Fig. 3. Idealized waveforms of the Class Φ inverter built around a $\lambda/4$-wave transmission line.

paper see [12], and introduce useful symmetries in converter waveforms.

The symmetrizing function of a transmission line terminated in a short circuit is clarified in Fig. 2, which depicts a line of electrical length $\lambda/4$, where λ corresponds to a fixed switching frequency $f_{\rm sw}$. In the lossless case, the line transforms the short-circuit termination to its input terminals as an open → short → open → $\cdots$ for successive multiples of $f_{\rm sw}$ (at each of which the line is electrically one quarter-wavelength longer). Because the line's low input impedance will collapse applied voltages at even harmonics of $f_{\rm sw}$, an excitation periodic in $T = 1/f_{\rm sw}$ will contain only odd harmonics and be half-wave symmetric [cf. Fig. 2(a)]. At odd multiples of $f_{\rm sw}$, the line's high input impedance ensures that dc and even harmonics dominate the terminal-current waveform. The input current is therefore half-wave repeating [cf. Fig. (2b)] with a period $T/2$.

The V–I symmetry relations shown in Fig. 2 are valid even for a half-period of effort by the source. Referring to the schematic in Fig. 2, consider the case of a line excited by a switch which closes during the first half of the fundamental period T. When the switch imposes a voltage waveform during the first half of the cycle, the transmission line becomes energized so as to impose a half-wave symmetric voltage at the input terminal during the second half cycle. This property is analogous to the manner in which an inductor becomes energized such that it imposes zero average voltage across its terminals during periodic-steady-state operation. The line stores the voltage waveform in a travelling wave along its length, which returns delayed by one-half fundamental period and inverted, because of the power-reflection condition at the short-circuit termination. The applied current wave also returns, delayed $1/2f_{\rm sw}$ seconds but not inverted, so that the line attempts to do the same work on the input network that was done on the line in the first half of the cycle.[2]

[2] Note that the line's ability to enforce a terminal voltage depends on a linear weighting of its (characteristic) admittance to the terminal node, as compared to other branch admittances. Assuming that the switch has a low enough impedance to drive the input node when on, the line's ability to enforce voltage symmetries will depend on its ability to source current into whatever parasitic impedance Z_p is present in the switch-off state.
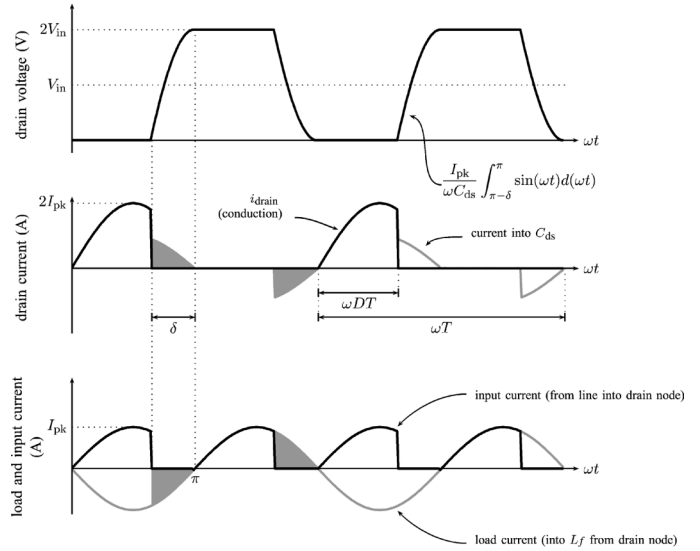
A. Class Φ Waveforms

With the aid of the voltage and current symmetries described in the previous section, the steady-state waveforms of the Class Φ in Fig. 1 can be readily derived (see Fig. 3). The switch imposes a constant voltage $(V_{\rm in})$ along the length of the line during the first portion of the switching cycle (when the switch is on). At turn-off, the differential current between the line and the load flows into $C_{\rm ds}$, as depicted by the shaded region over the interval δ in the bottom and middle plots of Fig. 3. The half-wave symmetries enforced by the line ensure that the drain voltage is symmetric about $V_{\rm in}$ (i.e., there is now a $-V_{\rm in}$ drop along its length). $v_{\rm ds}$ therefore assumes a value of $2V_{\rm in}$ for a time equal to the switch on time, until the line modes ring the drain back down to the switch-on voltage. At this point, the switch may be turned on with zero-voltage switching and zero drain current, and the cycle repeats.

If we assume a pulsed drain waveform like that shown in Fig. 3, details of the current waveform become clear upon consideration its half-wave repetition. In the switch-off state and with $v_{\rm ds}$ settled, the line current must equal the load current, and will repeat this sinusoidal behavior during the switch-on time. Because the differential current between load and line must drive half-wave symmetric edges in $v_{\rm ds}$, the drain displacement current must be half-wave symmetric (cf. the shaded areas of Fig. 3). The alternating sign in $i_{\rm d}$ can only come from $i_{\rm load}$, because $i_{\rm load}$ is half-wave symmetric; the line current, with its half-wave repeating content, must necessarily fall to zero during drain-voltage edges. This condition places a practical upper limit on the characteristic impedance of the line, which should be compliant enough to allow the switch to divert the entire load current quickly. To ensure turn-on with zero drain current, note that the load network should appear slightly inductive to the drain so that the load current lags the applied effort by δ radians, corresponding to the rise and fall times in $v_{\rm ds}$.

The output tank, comprising L_f, C_f, and the load resistance $R_{\rm load}$, is designed to extract the fundamental component of the
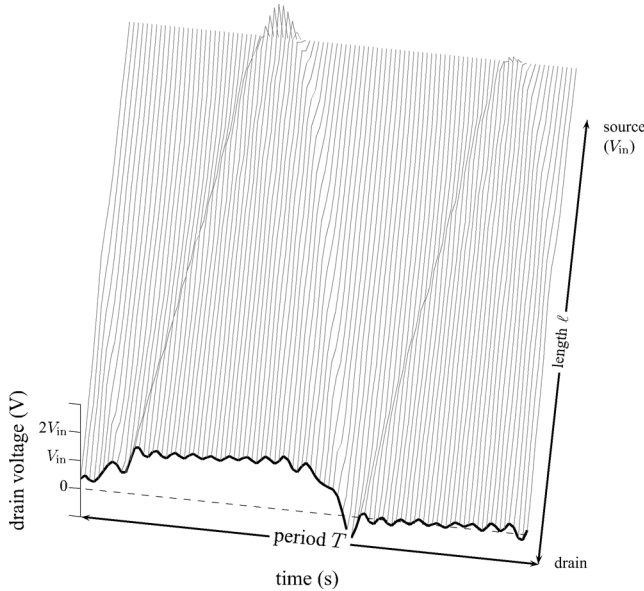
Fig. 4. Reflection diagram showing voltage waves along the $\lambda/4$-wave transmission line.

drain voltage waveform v_{ds}. The Q of the output tank is usually set by application constraints, and the tank inductor L_f typically contributes significantly to converter losses at higher Q values.

The reflection diagram of Fig. 4 clarifies drain-voltage symmetries by the travelling-wave properties of a transmission line. The time axis, showing the drain voltage during one switching period, is at the front of the figure. Voltages along the line—in this case across capacitors in a lumped model of the line—extend from the front of the plot back along the length axis, so that cross-sections parallel to the time axis show the time evolution of voltage at specific points along the line. The $2V_{\mathrm{in}}$ step in drain voltage launches a travelling wave down the line, which is reflected by the ac short at V_{in} and returns to the drain in time for a ZVS opportunity. The plot highlights the subsidiary waves which can propagate during the switch-on interval, and can reflect in time to complicate the v_{ds} rise at turn-off.

B. Normalized Power Output

The normalized power output capability P_N is a dimensionless figure of merit quantifying device stress, with lower values corresponding to poorer switch utilization [23]. P_N is defined in terms of output power P and peak switch stand-off and current

$$P_N \equiv \frac{P}{v_{ds,pk} \cdot i_{d,pk}}.$$

For heavy-load conditions, in which the drain-transition interval δ becomes smaller with respect to a switching period, v_{ds} is asymptotically square and the peak load current is

$$i_{\mathrm{load},pk} = \frac{4}{\pi} \cdot \frac{V_{\mathrm{in}}}{R_{\mathrm{load}}}$$

for large output-resonator Q. The output power is now readily calculated, as is the peak v_{ds} $(2V_{\mathrm{in}})$ under the square-wave

v_{ds} assumption. Since the input voltage source reflects current pulses such that a sinusoidal current from the line returns to the drain node in phase with the load current, the peak switch conduction current is twice the peak current in the load. We compute for the Class Φ, therefore, a normalized power-output capability of

$$P_N \equiv \frac{P}{v_{ds,pk} \cdot i_{d,pk}} = \frac{\left(\frac{4}{\pi}V_{\mathrm{in}}\right)^2 \cdot \frac{1}{2R_{\mathrm{load}}}}{2V_{\mathrm{in}} \cdot \left(\frac{8}{\pi} \cdot \frac{V_{\mathrm{in}}}{R_{\mathrm{load}}}\right)} = \frac{1}{2\pi} \approx 0.16$$

68% less demanding on the switch than the Class E ($P_N \approx 0.095$), exactly like the Class F. Note that the output power and peak values of v_{ds} and switch current in the Class Φ are individually equal to the Class F values.

III. DISTRIBUTED CLASS Φ IMPLEMENTATION

To demonstrate Class Φ operation with little design effort, a prototype converter was constructed incorporating a transmission line. The converter schematic and components are shown in Fig. 5. Details of the switch selection and choice of switching frequency (near the 13.56 MHz ISM band) will be deferred to Section IV-B. The input line is a 135.5-in section of RG-58/U, a quarter wavelength at 13.61 MHz. It is terminated at the dc source with three silver-mica snubber capacitors which are self-resonant near the switching fundamental and its fourth harmonic. Without this ac short, the line's boundary conditions are not enforced well enough to produce a square-wave voltage at the drain.

The output network is an L-match into a 50 Ω coaxial power resistor, designed to provide 20 Ω seen from the source. The series element of this L-match (a 47 nH inductor) is absorbed into the tank inductor, and the shunt element (a 286 pF capacitor) appears across the load. Both the match and tank capacitors are constructed from 62-mil copperclad FR4. These capacitors underlay the heat sink and gate drive, and support the tank inductor and output coaxial connector. The output inductor L_f is constructed from 5 1/2 air-core turns of unserved 175/40 litz in order to maximize Q at at the chosen switching frequency and limit the current density below 500 A/cm^2.

The gate capacitance (cf. Section IV-B) is resonated with a 27 nH inductor, which is itself in series with a 0.01 μF polypropylene blocking capacitor. This resonator has a peak impedance of 18 Ω and nearly resistive phase at 13.51 MHz, as seen from a 50 Ω ac drive through a second 0.01 μF blocking capacitor. The dc voltage at the gate can be set with this arrangement to vary the switch on-time, as required for Class Φ ZVS conditions. A duty cycle of about 0.38 was enforced with this technique using a gate bias of -4.4 V.

Measured drain- and load-voltage waveforms for the RG-58 converter are shown in Fig. 5 for $V_{\mathrm{in}} = 165$ V. The drain waveform shows the anticipated square-wave form, ringing up to around 320 V during the switch-off period. No power meter was available for this measurement, and the output power computed from the load-voltage measurement was 205.6 W. With the input source supplying 2.91 A at 165 V, the computed drain efficiency is 88%.
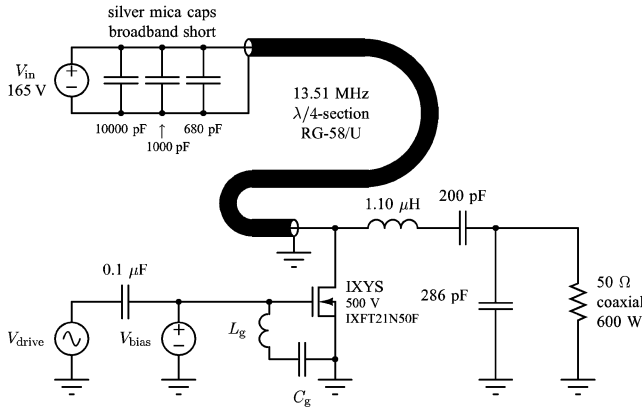
Fig. 5.   Class Φ resonant inverter constructed with a length of RG-58/U coaxial line.
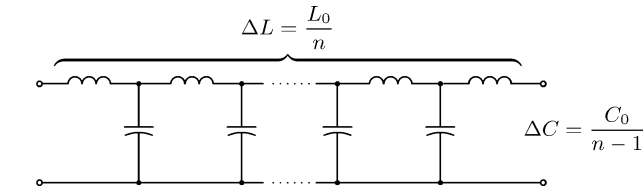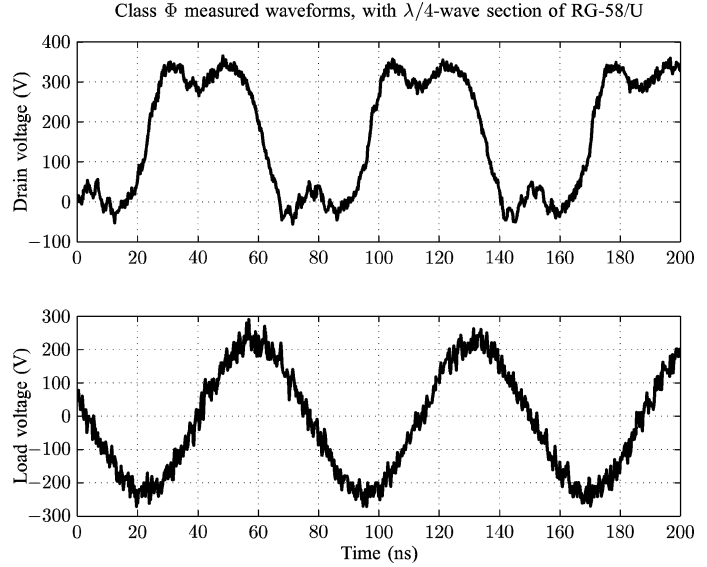

Fig. 6.   Iterated Cauer model for the transmission line.

IV. INTEGRATED CLASS Φ IMPLEMENTATION

Besides the lower switch stresses afforded by square-wave switch operation, transmission-line techniques can reduce the total amount of inductance or capacitance required to realize an energy-processing function. This reduction can have important manufacturing benefits, and will be elaborated on this section by a comparison of Class E and Class Φ inverters with similar power rating. In this comparison—to highlight the reduction of passive-component values achievable in a Class Φ design—the uniform-cross-section line of Section III will be replaced with a lumped line-simulating network constructed in the thickness of a PCB.

A. Lumped Line Analogs

A compact approximation of a transmission delay can be constructed by cascading LC-sections, as exemplified by the iterated network of Fig. 6. Here, the low-frequency inductance L_0 of an equivalent line is divided into n discrete section inductances ΔL. The low-frequency line capacitance is similarly divided into $n-1$ capacitances ΔC, so that an inductance ΔL appears in series with either port of the lumped network.[3] Though lumped line-simulating networks are often preferred to their distributed exemplars for reasons of design flexibility and manufacturability, the impedance peaks and nulls of such lumped

[3]In practice, n iterated T-sections can be concatenated, with L_0 divided into $2n$ equal ΔL (the left and right crossbars of each T-section). In this case, the terminal-mesh inductance (ΔL) is one-half the uniform section inductance from Fig. 6, an arrangement that has a higher cutoff frequency than n cascaded L-sections (see [12]).

networks must be aligned in a precise, harmonic manner to minimize loss and symmetrize converter waveforms. A complementary paper (see [12]) addresses this issue of harmonic frequency alignment, and details the construction of suitable line-approximating networks in printed-circuit form. For the Class E and Class Φ comparison at hand, the copper masks reproduced in Fig. 8 show a radial, laminar structure of the type considered in [12]. Dimensions and details for this structure can be found—along with a discussion of the surrounding Class Φ converter—in Section IV-D.

The total inductance L_0 and capacitance C_0 for the ladder network in Fig. 6 can be calculated from a specification of the characteristic impedance and quarter-wave resonant frequency of the transmission-line exemplar. From an exhaustive treatment in [24], the line modes can be expressed in terms of modal inductance and capacitance, parameterized by the critical-frequency number ν

$$L_\nu = \frac{L_0}{2} \quad C_\nu = \frac{8C_0}{\nu^2\pi^2}. \tag{1}$$

For a given C_0 and L_0, the first impedance maximum on a shorted line has an index $\nu = 1$, with $\nu = 0$ corresponding the dc zero. This first quarter-wave mode is located at the resonant frequency of C_1 and L_1

$$\frac{1}{2\pi\sqrt{L_1 C_1}} = \frac{1}{4\sqrt{L_0 C_0}} \text{ Hz.}$$

This distributed resonance is $\pi/2$ times higher than the lumped resonant frequency of L_0 and C_0. Specific guidance for the degree to which C_0 and L_0 should be divided (in the manner of Fig. 6) and the corresponding effect on impedance poles and zeros is provided in [12].

B. Frequency and Switch Selection

Metal-gate vertical MOSFET devices from IXYS and Advanced Power Technology were compared in simulations of the Class E and Class Φ to select a combination of device,

TABLE I
MEASURED AND NOMINAL PARAMETERS OF THE CANDIDATE MOSFETs
FOR THE INVERTERS IN SECTIONS III AND IV. V_{ds} AND I_d ARE NOMINAL
RATINGS. $r_{ds,on}$ HAS GREATER RELATIVE UNCERTAINTY THAN MANY OTHER
PARAMETERS, AND WAS INCREASED BY 1.8 TIMES FOR SIMULATIONS

Device	V_{dss}	I_d	C_g	R_g	C_{ds0}	ψ	n	$r_{ds,on}$
	V	A	pF	mΩ	pF	V		Ω
IXZ210N50L	500	10	857	1180	1970	0.184	0.421	1.00
DE150201N09A	200	15	1128	1064	2119	1.263	0.650	0.20
DE150102N02A	1000	2	673	1681	1314	1.775	0.756	3.20
IXFT21N50F	500	21	3190	56	4040	1.499	0.718	0.25
IXFT12N50F	500	12	2069	72	2335	1.075	0.635	0.40
ARF449A	450	9	1332	71	2381	0.129	0.514	0.80
ARF448B	450	15	2005	73	4683	0.151	0.542	0.40
ARF447	900	6	1975	80	4412	0.049	0.500	2.00

power level, and switching frequency for the proposed inverter comparison. Metal gate device were chosen because of their high-frequency gate pole $(R_g C_g)^{-1}$ and consequent low gating losses. Parameters of the candidate devices are summarized in Table I. The values of C_{ds0}, ψ, and n were obtained from drain-source impedance measurements with gate and source shorted, under three bias conditions. The parameters were fit by minimizing the deviation of the nonlinear capacitance expression

$$C_{ds} = \frac{C_{ds0}}{\left(1 + \frac{V_{ds}}{\psi}\right)^n} \qquad (2)$$

to the measured capacitances.

Anticipated power output and efficiency were calculated for the Class E inverter—at various switching frequencies and considering each device from Table I in turn—using reliable design guides in the literature [25], [26]. A Q of 10 was assumed in the output-tank inductor, and the peak drain voltage v_d was limited to 80% of the switch drain-source standoff (V_{dss}). The native C_{ds} of switches under consideration was not augmented in simulation, and was approximated by linearized switch C_{ds} (2) evaluated at $V_{ds} = V_{in}$. For some f_{sw} and fixed C_{ds}, then, the total tank resistance was set by a fit function reported in [26]

$$R = \frac{1}{34.2219 f_{sw} C_{ds}} \left(0.99866 + \frac{0.91424}{Q_L} - \frac{1.03175}{Q_L^2}\right).$$

The design equations presented by the same author were then applied in a straightforward manner

$$C_r = \frac{1}{2\pi f_{sw} R}\left(\frac{1}{Q_L - 0.104823}\right)\left(1.00121 + \frac{1.01468}{Q_L - 1.7879}\right)$$
$$L_r = \frac{Q_L R}{2\pi f_{sw}}.$$

The input choke inductance L_{choke} was conservatively selected 10 times larger than L_r, and reduced later based on simulation of acceptable waveform distortions.

From the design calculations and simulations, the IXFT21N50F (produced by IXYS) was chosen for the Class E and Class Φ comparison because it had the highest efficiency

at manageable power, and was the least expensive switch. A switching frequency in the ISM band at 13.56 MHz was selected because the manageable heat dissipation and passive ratings anticipated for designs at this frequency.

C. Class E Inverter

The schematic of a Class E inverter designed around the IXFT21N50F—including parasitics—is shown in Fig. 7. The output-inductor value is the combination of the Class E resonant inductance and the L-match inductance required to match a 13 Ω source impedance into the 50 Ω coaxial load. The 13 Ω source impedance is the tank load required for Class E operation, and was computed for the desired tank Q, C_{ds}, and switching frequency as outlined in [26]. Eight air-core turns (2.3 cm winding length) of unserved 175/40 litz were wound on a plastic former with a 26 mm diameter for the tank/match inductor. This geometry achieved a Q of 84 at 13.56 MHz. The input choke was also constructed as an air-core solenoid, 21 turns of 18 gauge wire on the same plastic former used in the output tank. The gate capacitance was resonated with a lead-trimmed 27 nH inductor, an air-core inductor of the Coilcraft Midi Spring family. This resonator had a peak impedance of 27 Ω at 13.56 MHz and nearly resistive phase as seen from the 50 Ω ac drive. Silver-mica chip capacitors were used in the output network, placed in series for higher standoff where necessary.

The 1 kW source (an HP 6015A dc power supply, 0–500 V/0–5 A) was set to 107 V and bypassed at the board with one 10000 pF and one 6800 pF silver-mica capacitor. The gate was driven by a 150 W Amplifier Research Class A power amplifier (Model 150A 100B, 10 kHz–100 MHz), with its gain set high enough that the switch transition could be controlled in the presence of drain-voltage feedback and harmonic distortion of the amplifier. High-voltage differential probes (two Tektronix P5205 100 MHz probes on a 500× attenuation setting) were used for both measurements. A Bird Series 5010 directional power sensor was placed between the load and converter, connected on either side with two-foot lengths of RG-58 cable. The sensor was equipped with a Bird DPM-500H forward power sensor (500 W full-scale from 2–30 MHz) and a DPM-50H reflected sensor (50 W full-scale from 2–30 MHz), with readout provided by a Bird Model 500-EX digital power meter. The Load was a 50 Ω Bird Model 8401 Termaline coaxial resistor, rated at 600 W and resistive from dc to 3 GHz (VSWR: dc to 1 GHz = 1.1).

Measured drain- and load-voltage waveforms for the Class E converter are shown in Fig. 7 for $V_{in} = 107$ V. Input current, as measured by the HP 6015A supply, was 1.88 A, close to the dc value of 1.93 A measured by a Tektronix A6303 current probe with AM503B amplifier. The Bird meter read 163 W forward power, close to the 162.2 W computed from the output-voltage measurement. The drain efficiency was around 81% (80.6% from voltage measurements, and 81% computed with the power meter). 85% efficiency was computed from a ideal-switching simulation of the schematic of Fig. 7, taking no account of finite switch times. The resonant inductor was lossy, and became hot enough during converter operation to soften its former.
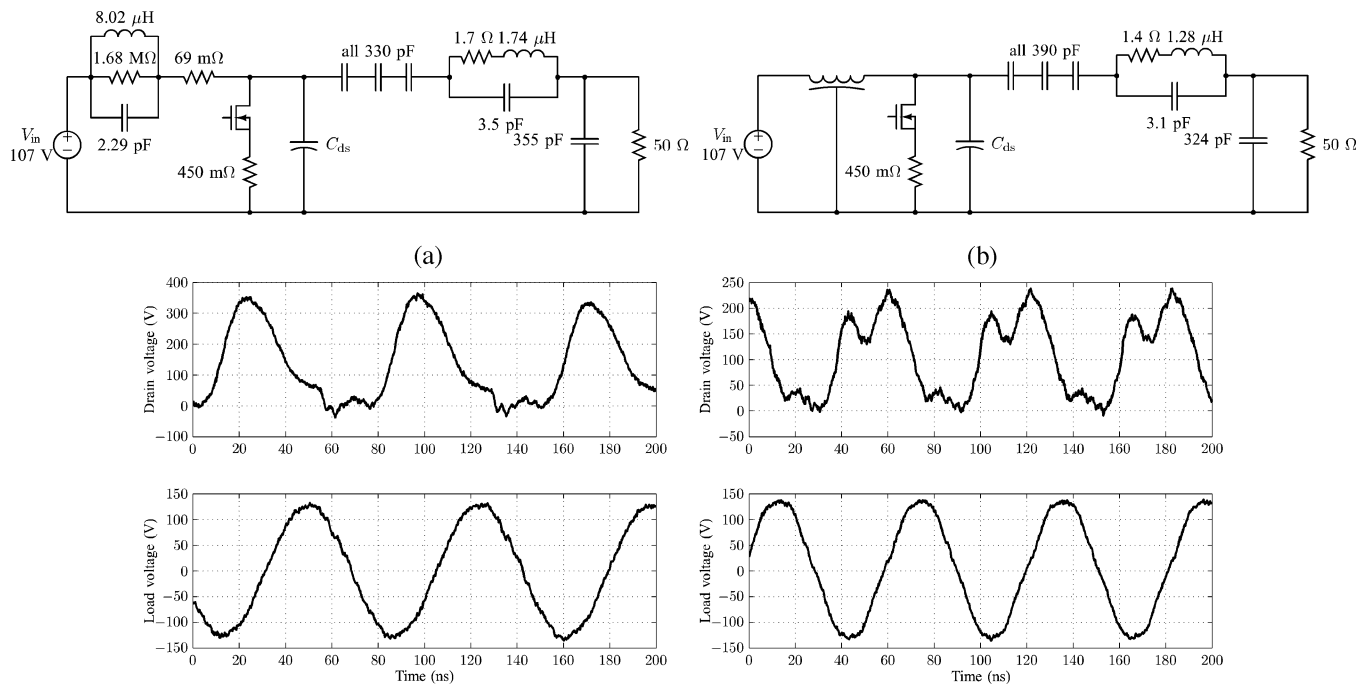
Fig. 7. Schematics and measured waveforms of the Class E and Class Φ inverters: (a) Class E measured waveforms and (b) Class Φ measured waveforms, with 20 Ω planar transmission-line analog.
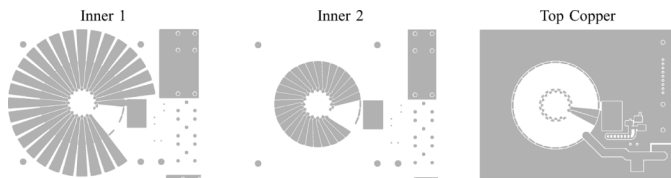

Fig. 8. Copper layers of the Class Φ converter constructed with a lumped 20 Ω transmission-line analog incorporated into the thickness of a PCB.
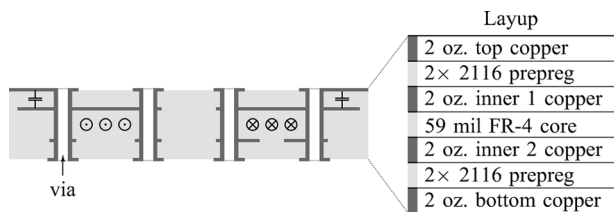

Fig. 9. Cross section of the toroidal structures from Fig. 8 in a multilayer board with exaggerated thicknesses. The toroidal flux path is indicated between pairs of vias on either side of central axis.

D. Integrated Class Φ Implementation

A Class Φ converter with integrated air-core magnetics was designed to match the performance of the Class E of Section IV-C with lower device stress. A 20 Ω line analog was constructed into the thickness of a four-layer PCB with 2 oz. copper on all layers (see Fig. 8). Fig. 9 depicts a PCB cross section through the central axis of the toroid. A 59 mil core was selected for the magnetic thickness dimension, with capacitors constructed across outer layers comprising two sheets of 2116 prepreg. The final laminate build was 83 mil, slightly more than anticipated because of an unexpectedly small prepreg compression. The inter-layer capacitances were smaller than

designed (500 pF, total), and the multiresonant structure had a principle peak at 15.7 MHz rather than 13.56 MHz.

As with the PCB structures considered in [12], the multiresonant toroid had an outer diameter of 2.5 in and an inner diameter of 0.75 in. The low-frequency inductance, measured at 100 kHz and far below the first $\lambda/4$-wave resonance, was 207 nH. The capacitors extended from each turn for a total diameter of 4.4 in. Two turns of the gapped, 28-turn toroid were brought to the outer copper layers after the drain connection and left free of soldermask. These bare turns are magnetically coupled to the input network, providing an adjustable connection point to implement the inductance-cancellation scheme of Fig. 10(a). The schematic of the complete converter with parastitcs is shown in Fig. 7, excluding details of the input bypassing (one each of four discrete silver mica values was used, 10000 pF, 6800 pF, 1000 pF, and 680 pF).

Measured drain- and load-voltage waveforms for the Class Φ converter with mult-resonant inductor are shown in Fig. 7 for $V_{\text{in}} =$102 V. The drain waveform has a roughly square-wave form, ringing up to around 200 V during the switch-off period. Input current, as measured by the HP 6015A supply, was 2.11 A for an input power of 215 W. 178 W load power was computed from the output-voltage measurement, and the Bird meter read 163 W forward power.[4] The drain efficiency was 82.7% from voltage measurements, and 75.2% computed with the power meter. The resonant inductor was constructed as in Section IV-C and was again very lossy, a likely target for efficiency improvement in subsequent designs. The multiresonant structure, likewise, became warm during operation (besides ohmic losses,

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[4]The unexpectedly large fourth harmonic at the drain could have contributed to harmonic current into the load sufficient to explain this discrepancy. This fourth-harmonic distortion is a symptom of poor zero coincidence, as compared with the ideal transmission line.
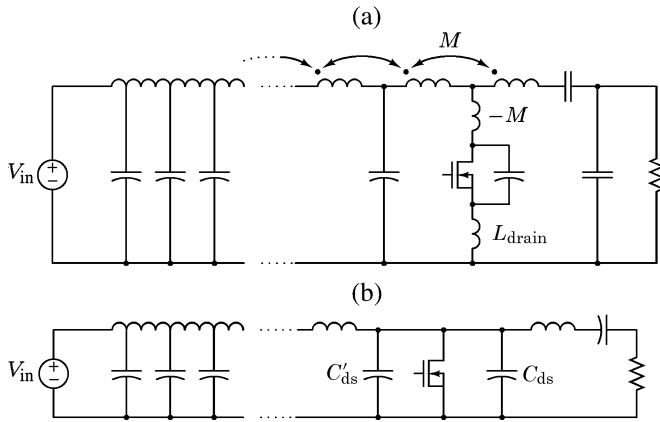
(a)

(b)

Fig. 10. Two methods of compensating for switch reactances in the Class Φ inverter: (a) cancellation of package inductance and (b) partial absorption of drain-source capacitance into line.

the Q of its capacitor taps was around 50). Overall efficiency could be improved by better pole/zero alignment in the transmission-line network, higher quality dielectrics, and thicker copper build.

E. Improvements to the Basic Class Φ Design

Two techniques for enhancing the basic Class Φ design by altering its effective switch reactance are shown in Fig. 10. Fig. 10(a) shows a means of compensating for the package inductance of the FET. As can be verified by a application of a transformer T-model, drain-path inductance can be developed by mutual induction between the branches communicating with the drain node (i.e., a magnetic coupling between L_r and the first section-inductance of the artificial line). Purposely added coupling (M) in the sense shown in Fig. 10(a) offsets this parasitic package inductance by $-M$, and is explained further in [12], [15]. Note that this technique is particular to the lumped transmission lines in Section IV, and cannot be implemented with a distributed line alone.

The second technique, shown in Fig. 10(b), is sometimes implemented with distributed lines in the Class F amplifiers which employ them [2]. Recall that for the Class E inverter, output power and switching frequency increase in unison, with no apparent means of reducing C_{ds} to decrease the charge delivered per cycle. Even if a switch is capable of operating at tens or hundreds of megahertz, a design may be limited by the power-handling ability of its switch and reactive elements. The achievable efficiency of a Class E converter ultimately declines with frequency for this reason. The Class Φ can offset this frequency/power scaling by absorbing part of the switch drain-source capacitance (C'_{ds}) into the line, either by shortening its electrical length for constant f_{sw}, or shifting to a lower f_{sw}. Further passive miniaturization and higher inductor Q can be expected by a move to faster switching.

V. CONCLUSION

A soft-switching inverter topology (the Class Φ) has been presented which draws dc source current through a transmission line or a lumped-network approximation of a distributed line. By aligning the inverter switching frequency just below

the line's $\lambda/4$-wave resonance, the Class Φ topology enforces odd- and even-harmonic content in its drain voltage and input current, respectively. The symmetrizing action of the transmission-line dynamics results in natural square-wave operation of the switch, reducing the inverter stresses (relative to a Class E) for a given power throughput. The inverter waveforms and normalized power-output capability have been analyzed in simple terms, and are supported by measurements of an inverter built around a length of distributed line, and an inverter incorporating a lumped L–C ladder network.

The Class Φ topology can reduce the total amount of inductance or capacitance required to realize an energy-processing function by exchanging large-valued blocking components for high-Q resonant elements. Resonant LC networks in the Class Φ are compatible with laminar construction methods, and are treated in detail in a complementary paper [12]. In a comparison between a Class Φ and Class E inverter presented here, the 8.02 μH input choke of the Class E was replacement by a planar structure comprising 207 nH of inductance and 500 pF of interlayer capacitance. Though the measured drain efficiencies of both converters were in the vicinity of 80%, the demonstrable impedance precision of the line-simulating networks (see [12]) promises to improve with iteration.

APPENDIX

An adjoint paper, "Synthesis of lumped transmission-line analogs" [12], addresses the harmonic-frequency alignment in LC ladder networks that approximate transmission lines. The paper presents new analytic expressions for the impedance-minimum and -maximum frequencies of LC networks in a Cauer (ladder) form with unmatched terminations. These expressions elaborate on the advice that the electrical length ℓ of concatenated LC networks be shorter than a some fraction of the smallest signal wavelength of interest (i.e., where "some fraction" is usually set somewhat arbitrarily as the upper bound $\ell < \lambda/10$).

Two means of correcting for the observed harmonic misalignment in practical ladder structures are presented, corroborated by measurements of toroidal structures built into the thickness of printed-circuit boards (see Fig. 8). These structures comprise inductances and capacitances whose dimensions are largely decoupled, such that the toroid's impedance can be accurately analyzed and designed on a lumped basis. In particular, the inductance matrix describing a base toroid can be approximated by inductance terms on the main diagonal and immediate off-diagonals. These mutual terms describe the magnetic coupling from turn to turn around the toroid, so that capacitor taps can be designed with an eye to preserving harmonic alignment of impedance extrema (i.e., impedance extrema of the complete ladder network, comprising the toroid and its capacitor taps). The inductance matrices in the adjoint paper are calculated using FastHenry, a freely available program which extracts inductances and resistances of 3-D conductor geometries on a quasi-static basis.

REFERENCES

[1] J. Phinney, D. Perreault, and J. Lang, "Multi-resonant microfabricated inductors and transformers," in *Proc. IEEE 35th Annu. Power Electron. Spec. Conf.*, Jun. 2004, pp. 4527–4536.

[2] V. Tyler, "A new high-efficiency high-power amplifier," *Marconi Rev.*, vol. 21, no. 130, pp. 96–109, Fall, 1958.

[3] F. Raab, "Class-F power amplifiers with maximally flat waveforms," *IEEE Trans. Microw. Theory Tech.*, vol. 45, no. 11, pp. 2007–2012, Nov. 1997.

[4] K. Honjo, "A simple circuit synthesis method for microwave Class-F ultra-high-efficiency amplifiers with reactance-compensation circuits," *Solid State Electron.*, vol. 44, pp. 1477–1482, 2000.

[5] F. Raab, "Maximum efficiency and output of Class-F power amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 6, pp. 1162–1166, Jun. 2001.

[6] A. Grebenikov, "Effective circuit design techniques to increase MOSFET power amplifier efficiency," *Microw. J.*, pp. 64–72, Jul. 2000.

[7] A. Grebenikov, "Circuit design techniques for high efficiency Class F amplifiers," in *Proc. IEEE Microw. Theory Tech. Symp.*, 2000, pp. 771–774.

[8] F. Raab, "Class-F power amplifiers with reduced conduction angles," *IEEE Trans. Broadcast.*, vol. 44, no. 4, pp. 455–459, Dec. 1998.

[9] D. Snider, "A theoretical analysis and experimental confirmation of the optimally loaded and overdriven RF power amplifier," *IEEE Trans. Electron Devices*, vol. ED-14, no. 12, pp. 851–857, Dec. 1967.

[10] S. Kee, I. Aoki, A. Hajimiri, and D. Rutledge, "The Class E/F family of ZVS switching amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 6, pp. 1677–1690, Jun. 2003.

[11] A. Grebenikov, *RF and Microwave Power Amplifier Design*. New York: McGraw-Hill, 2005.

[12] J. Phinney, D. Perreault, and J. Lang, "Synthesis of lumped transmission-line analogs," in *Proc. 37th Annu. Power Electron. Spec. Conf.*, Jun. 2006, pp. 2967–2978.

[13] J. Phinney, "Filters With Active Tuning for Power Applications," S.M. thesis, Dept. Elect. Eng. Comp. Sci., Lab. Electromagn. Electron. Syst., Mass. Instit. Technol., , Cambridge, 2001.

[14] J. Phinney and D. Perreault, "Filters with active tuning for power electronics," *IEEE Trans. Power Electron.*, vol. 18, no. 2, pp. 636–647, Mar. 2003.

[15] J. Phinney and D. Perreault, "Filters with active tuning for power electronics," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2001, pp. 363–370.

[16] J. Rivas, R. Wahby, J. Shafran, and D. Perreault, "New architectures for radio-frequency dc/dc power conversion," in *Proc. 35th Annu. Power Electron. Spec. Conf.* , Jun. 2004, pp. 4074–4084.

[17] Y. Han, O. Leitermann, D. Jackson, J. Rivas, and D. Perreault, "Resistance compression networks for resonant power conversion," in *Proc. 36th Annu. Power Electron. Spec. Conf.*, Jun. 2005, pp. 1282–1292.

[18] F. Raab, *Solid State Engineering*. Atlanta, GA: Noble, 2001.

[19] F. Lepine, A. Adahl, and H. Zirath, "L-band LDMOS power amplifiers based on an inverse Class-F architecture," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 6, pp. 2012–2207, Jun. 2005.

[20] R. Gutmann and J. Borrego, "Power combining in an array of microwave power rectifiers," *IEEE Trans. Microw. Theory Tech.*, vol. MIT-27, no. 12, pp. 958–967, Dec. 1979.

[21] Y. Han, O. Leitermann, D. A. Jackson, J. M. Rivas, and D. J. Perreault, "Resistance compression networks for resonant power conversion," in *Proc. IEEE 36th Annu. Power Electron. Spec. Conf.*, Jun. 2005, pp. 1282–1292.

[22] J. Phinney, "Multi-Resonant Passive Components for Power Conversion," Ph.D. dissertation, Dept. Elect. Eng. Comp. Sci., Lab. Electromagn. Electron. Syst., Mass. Instit. Technol., , Cambridge, 2005.

[23] T. Lee, *Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, U.K.: Cambridge Univ. Press, 1998.

[24] E. Guillemin, *Synthesis of Passive Networks: Theory of Methods Appropriate to the Realization and Approximation Problems*. New York: Wiley, 1957.

[25] N. Sokal and A. Sokal, "Class E—A new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE J. Sold-State Circuits*, vol. SC-10, no. 3, pp. 168–176, Jun. 1975.

[26] N. Sokal, "Class-E RF power amplifiers," *QEX Commun. Quart.*, pp. 9–20, Jan./Feb. 2001.

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