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Analysis and Design of High Efficiency Matching Networks

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Abstract—This letter presents analysis and design considerations for lumped (inductor and capacitor) matching networks operating at high efficiency (>95%). Formulas for calculating matching network efficiency are given, and it is shown that efficiency can be expressed as a function of inductor quality factor Q_L , capacitor quality factor Q_C , and transformation ratio. These formulas are used to evaluate the optimum number of L -section matching stages as a function of conversion ratio. Both simulation and experimental results are presented that validate the analytical formulation.

Index Terms—Impedance transformer, matching network, resonant converter.

I. BACKGROUND

A matching network is a passive two-port circuit designed to provide narrow-band impedance and voltage transformation between the two ports. While most widely associated with communications applications [1]–[3] matching networks also find useful application in resonant inverters, rectifiers, and dc-dc converters. Most analytical descriptions of matching networks are based on the assumption of no loss. Where efficiency is considered [4], it is typically treated as secondary to other performance goals, in accordance with the needs of communications applications. Moreover, literature focusing on the design of matching networks for very high efficiencies (e.g., >95%) appears to be lacking. This letter presents analysis and design considerations for high efficiency lumped-element matching networks.

In Section II, some possible topologies for matching networks are identified, and formulas to calculate their efficiency are developed. In Section III, the implications of the results of Section II are discussed, and the analytical results are compared to Pspice simulations. Strong agreement between analysis and simulation is demonstrated. Section IV presents experimental results validating the efficiency calculations of Section II. Finally, Section V concludes the letter.

II. MATCHING NETWORK DESIGN AND EFFICIENCY ANALYSIS

Two basic matching network topologies are shown in Fig. 1. Fig. 1(a) and (b) are low-pass and high-pass single-stage L -section matching networks. These networks can be used to step a load impedance up or down, depending upon which port is connected to the load and which is connected to the source [1]. They

can each be used to transform a load resistance of value R_s connected to the right-hand port to a resistance R_p seen from the left-hand port, or to transform a load resistance of value R_p connected at the left-hand port down to a resistance R_s seen from the right-hand port. T and Π matching networks could also be used as basic matching networks. However, they invariably have lower efficiency than an equivalent L -section network [2] and are thus not considered here. Inductor parasitic resistance R_L and capacitor parasitic resistance R_C are shown as explicit circuit elements in each network of Fig. 1. V_p and V_s are the peak voltages at the left-hand and right-hand ports. I_p and I_s are the peak currents in the shunt and series legs.

Design of the matching networks of Fig. 1 (neglecting R_L , R_C , and the loss associated with them) is well understood [1]–[3] and may be carried out as follows. Starting with a desired resistance transformation ratio

$$\frac{R_p}{R_s} = \frac{V_p^2}{V_s^2} \quad (1)$$

we can define an associated transformation quality factor

$$Q = \sqrt{\frac{R_p}{R_s} - 1} \quad (2)$$

a series-leg quality factor

$$Q_s = \frac{|X_s|}{R_s} \quad (3)$$

and a shunt-leg quality factor

$$Q_p = \frac{R_p}{|X_p|} \quad (4)$$

As shown in Fig. 1, Q_s is the quality factor of the series leg (where we include the external network resistances and neglect matching network loss) and Q_p is the quality factor of the shunt leg; R_p is the matched shunt resistance; X_p is the shunt reactance; R_s is the matched series resistance and X_s is the series reactance. To achieve the desired transformation neglecting loss, the matching network reactances are selected such that $Q_s = Q_p = Q$.

Losses in high-efficiency matching networks can be computed using the following approximation: the circuit is designed and the circuit currents are calculated on a no-loss basis; the inductor and capacitor losses and circuit efficiency are then calculated based on the losses induced by the calculated currents flowing through inductor resistance R_L and capacitor resistance

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R_C . This calculation thus assumes that the branch currents are not affected by the presence of small resistive components [2].

Shown in Fig. 1, P_s is the power entering the matching network from the right, P_p is the power entering the matching network from the left. We get

$$|P_s| = \frac{1}{2} I_s^2 R_s \quad (5)$$

$$|P_p| = \frac{V_p^2}{2R_p}. \quad (6)$$

$P_{\text{loss}C}$ is the loss power in the capacitor, $P_{\text{loss}L}$ is the loss power in the inductor, P_{loss} is the total loss power in the matching network and equal to $P_{\text{loss}C} + P_{\text{loss}L}$.

Consider, first, the low-pass matching network shown in Fig. 1(a). $Q_L = \omega L_s/R_L = |X_s|/R_L$ is the quality factor of the inductor, $Q_C = 1/\omega C_p R_C = |X_p|/R_C$ is the quality factor of the capacitor, and η represents the efficiency of the matching network. From Fig. 1(a) and above definitions, we have

$$P_{\text{loss}L} = \frac{1}{2} R_L I_s^2 = \frac{|X_s|}{2Q_L} I_s^2 = \frac{Q}{Q_L} |P_s| \quad (7)$$

$$\begin{aligned} P_{\text{loss}C} &= \frac{1}{2} R_C I_p^2 = \frac{|X_p|}{2Q_C} \left(\frac{V_p}{|X_p|} \right)^2 \\ &= \frac{V_p^2}{2Q_C |X_p|} = \frac{Q}{Q_C} |P_p|. \end{aligned} \quad (8)$$

If the left port is connected to the source and the right port is connected to the load, P_p is positive and P_s is negative

$$\begin{aligned} |P_p| &= |P_s| + P_{\text{loss}L} + P_{\text{loss}C} \\ &= |P_s| + \frac{Q}{Q_L} |P_s| + \frac{Q}{Q_C} |P_p| \end{aligned} \quad (9)$$

$$\eta = \frac{|P_s|}{|P_p|} = \frac{1 - \frac{Q}{Q_C}}{1 + \frac{Q}{Q_L}}. \quad (10)$$

If the left port is connected to the load and the right port is connected to the source, P_p is negative and P_s is positive

$$\begin{aligned} |P_s| &= |P_p| + P_{\text{loss}L} + P_{\text{loss}C} \\ &= |P_p| + \frac{Q}{Q_L} |P_s| + \frac{Q}{Q_C} |P_p| \end{aligned} \quad (11)$$

$$\eta = \frac{|P_p|}{|P_s|} = \frac{1 - \frac{Q}{Q_L}}{1 + \frac{Q}{Q_C}}. \quad (12)$$

Next consider the high-pass matching network shown in Fig. 1(b). The inductor quality factor $Q_L = \omega L_p/R_L =$

$|X_p|/R_L$ and the capacitor quality factor $Q_C = 1/\omega C_s R_C = |X_s|/R_C$. From Fig. 1(b) and above definitions, we have

$$P_{\text{loss}C} = \frac{1}{2} R_C I_s^2 = \frac{|X_s|}{2Q_C} I_s^2 = \frac{Q}{Q_C} |P_s| \quad (13)$$

$$\begin{aligned} P_{\text{loss}L} &= \frac{1}{2} R_L I_p^2 = \frac{|X_p|}{2Q_L} \left(\frac{V_p}{|X_p|} \right)^2 \\ &= \frac{V_p^2}{2Q_L |X_p|} = \frac{Q}{Q_L} |P_p|. \end{aligned} \quad (14)$$

If the left port is connected to the source and the right port is connected to the load, P_p is positive and P_s is negative

$$\begin{aligned} |P_p| &= |P_s| + P_{\text{loss}C} + P_{\text{loss}L} \\ &= |P_s| + \frac{Q}{Q_C} |P_s| + \frac{Q}{Q_L} |P_p| \end{aligned} \quad (15)$$

$$\eta = \frac{|P_s|}{|P_p|} = \frac{1 - \frac{Q}{Q_L}}{1 + \frac{Q}{Q_C}}. \quad (16)$$

If the left port is connected to the load and the right port is connected to the source, P_p is negative and P_s is positive

$$\begin{aligned} |P_s| &= |P_p| + P_{\text{loss}C} + P_{\text{loss}L} \\ &= |P_p| + \frac{Q}{Q_C} |P_s| + \frac{Q}{Q_L} |P_p| \end{aligned} \quad (17)$$

$$\eta = \frac{|P_p|}{|P_s|} = \frac{1 - \frac{Q}{Q_C}}{1 + \frac{Q}{Q_L}}. \quad (18)$$

When $Q/Q_L \ll 1$ and $Q/Q_C \ll 1$ (i.e., for the case of high efficiency), we can approximate (10), (12), (16), and (18) by neglecting products of these small quantities. In each case, this yields

$$\eta \approx 1 - \frac{Q}{Q_L} - \frac{Q}{Q_C}. \quad (19)$$

Notice we get the same efficiency for the low-pass and high-pass matching networks if $Q/Q_L \ll 1$ and $Q/Q_C \ll 1$ (i.e., for the case of high efficiency). Moreover, for most cases of practical interest, $Q_C \gg Q_L$, inductor loss far exceeds capacitor loss and is the only loss component that needs to be considered. In this case

$$\eta \approx 1 - \frac{Q}{Q_L} = 1 - \frac{\sqrt{\frac{R_p}{R_s}} - 1}{Q_L}. \quad (20)$$

It is important to observe that the matching network efficiency depends only on the inductor quality factor and the transformation ratio if $Q_C \gg Q_L$. For a given inductor quality factor, there is an upper bound on the efficiency of a single-stage matching network as expressed in (20).

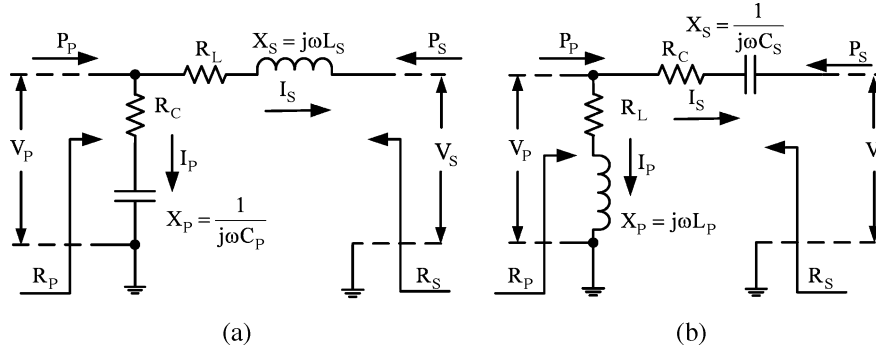


Fig. 1. L -section matching networks with inductor parasitic resistance shown explicitly: (a) Low-pass and (b) high-pass.

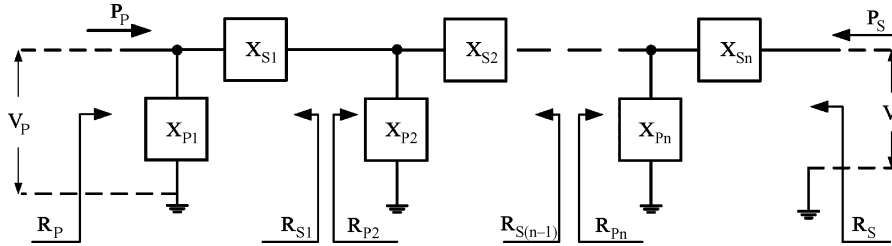


Fig. 2. Multistage matching network.

One route towards higher performance that is sometimes recommended is the use of a multistage matching network comprising a cascade of individual L -sections [2]. Consider the n -stage matching network illustrated in Fig. 2. Using (20) and assuming that all inductors' Q_L are identical, we get

$$\begin{aligned} \eta &= \left(1 - \frac{Q_1}{Q_L}\right) \left(1 - \frac{Q_2}{Q_L}\right) \dots \left(1 - \frac{Q_n}{Q_L}\right) \\ &= \prod_{i=1}^n \left(1 - \frac{Q_i}{Q_L}\right) \end{aligned} \quad (21)$$

where Q_i is the transformation quality factor of the n th stage [corresponding to the transformation ratio of one stage in (1) and (2)]. For high efficiency of each stage we require $Q_i/Q_L \ll 1$, and find:

$$\begin{aligned} \eta &\approx 1 - \frac{Q_1 + Q_2 + \dots + Q_n}{Q_L} \\ &= 1 - \frac{\sum_{i=1}^n Q_i}{Q_L} \\ &\leq 1 - \frac{n(\prod_{i=1}^n Q_i)^{\frac{1}{n}}}{Q_L} \end{aligned} \quad (22)$$

and from the formulas in [5], it can be shown that

$$\eta \approx 1 - \frac{n(\prod_{i=1}^n Q_i)^{\frac{1}{n}}}{Q_L} \quad \text{only when } Q_1 = Q_2 = \dots = Q_n. \quad (23)$$

Thus, for the optimal case of identical transformation ratios for each L -section stage, we select the transformation quality factors of all the stages as

$$Q_i = \sqrt{\left(\frac{R_p}{R_s}\right)^{\frac{1}{n}} - 1} = \sqrt{\left(\frac{V_p}{V_s}\right)^{\frac{2}{n}} - 1} \quad (24)$$

and achieve an overall efficiency of

$$\eta \approx 1 - \frac{n}{Q_L} \sqrt{\left(\frac{R_p}{R_s}\right)^{\frac{1}{n}} - 1}. \quad (25)$$

Considering (25), there is clearly an optimum number of stages n to maximize efficiency. This number is a function of the transformation ratio but not a function of inductor quality factor Q_L , assuming all inductors have an identical specified Q_L . Fig. 3 plots the optimum number of L -section stages n_{opt} as a function of the voltage transformation ratio V_p/V_s . As transformation quality factor Q increases, the optimum number of stages approaches

$$n_{opt} \rightarrow \lceil \ln Q \rceil \quad (26)$$

and the efficiency approaches

$$\eta_{max} = 1 - \frac{nQ^{\frac{1}{n}}}{Q_L} \quad (27)$$

where Q is as defined in (2). These results indicate that using multi-stage design may improve the efficiency, especially when the desired transformation ratio is very large. But the efficiency

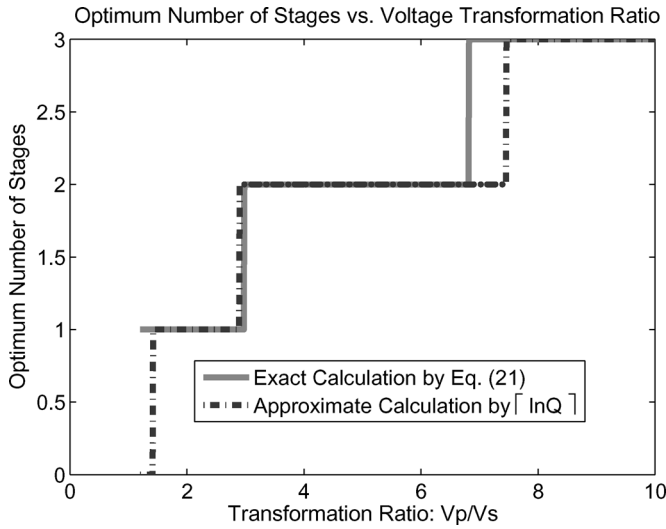


Fig. 3. Optimum number of stages versus transformation ratio.

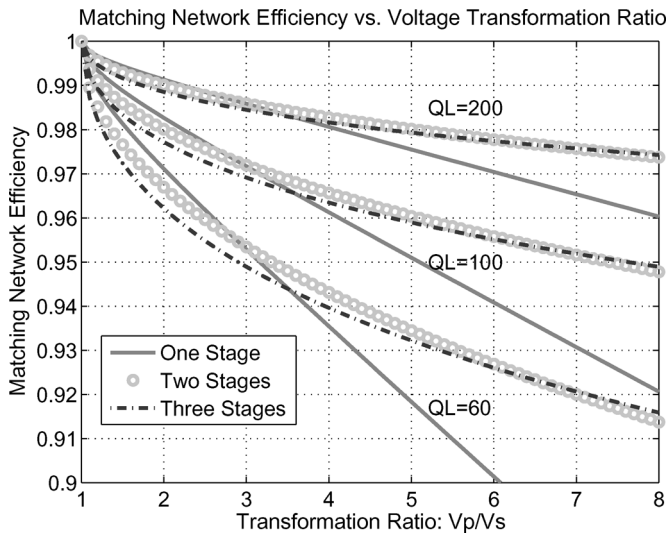


Fig. 4. Matching network efficiency versus transformation ratio V_p/V_s .

reaches its maximum at a certain number of stages and will decrease for more stages.

III. CALCULATION AND SIMULATION RESULTS

The previous section showed that matching network efficiency can be expressed as a function of inductor quality factor Q_L and transformation ratio. To illustrate the implication, Fig. 4 plots predicted matching network efficiency versus transformation ratio for three different inductor quality factors used in one-, two-, and three-stage designs. In all cases, matching network efficiency decreases with increasing transformation ratio, and decreases more rapidly with lower inductor quality factor. This is to be expected, given the forms of (20) and (25).

Fig. 4 also illustrates how the optimal number of matching network stages changes with transformation ratio for a specified inductor Q_L . Consider the one, two and three-stage design curves for $Q_L = 60$. For a voltage transformation ratio of 2, a

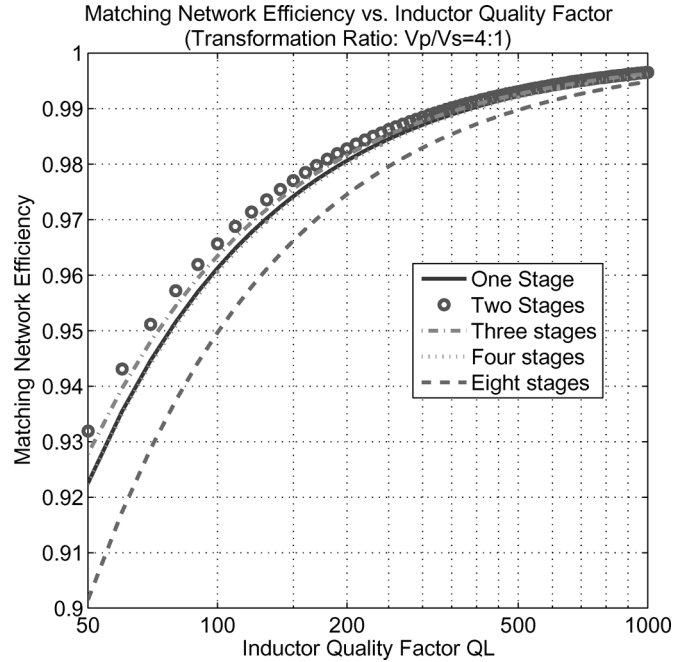


Fig. 5. Matching network efficiency versus inductor quality factor.

single-stage design has the highest efficiency. At a voltage transformation ratio of 5, a two-stage design has a significant advantage ($\sim 1.5\%$) in efficiency over a single-stage, and at a voltage transformation ratio of 8, the three-stage design is developing a marginal advantage over a two-stage design. Considering the tradeoffs at a voltage conversion ratio of 8, it can also be seen that if the space required to construct the three inductors for the three-stage $Q_L = 60$ design can be employed to build a higher Q inductor for a single-stage design (e.g., $Q_L = 100$), then a single-stage design may still be preferable. Thus, the optimal number of stages specified in Fig. 3 and (25) should only be considered an upper bound.

Fig. 5 illustrates the predicted efficiency of a matching network for a typical voltage transformation ratio of 4 as a function of inductor quality factor Q_L (parameterized by the number of stages). In each curve, percentage loss is inversely proportional to Q_L (20), (25) leading to the observed asymptotic behavior. Thus, for a single-stage design, doubling quality factor Q_L from 100 to 200 yields an efficiency improvement from (approximately) 96% to 98%, and doubling Q_L again to 400 changes efficiency from 98% to 99%. Still greater loss reductions require proportionally higher inductor quality factors, and under those conditions the capacitor quality factor starts to be a consideration (limiting efficiency) as indicated in (19). Nevertheless, it may be concluded that for a 4:1 voltage transformation ratio, it is possible to achieve high efficiency with inductors of reasonable quality factor. To further illustrate component sizing and efficiency, consider the design of matching networks having a voltage transformation ratio of $V_p : V_s = 4:1$. We assume $P_{in} = 25 \text{ W}$, $R_p = 50 \Omega$, and $R_s = R_p/16 = 3.125 \Omega$.

The component values for the matching networks of Fig. 1(a) and (b) are shown in Table I for frequencies of 25, 50, and 100 MHz. For the multistage network in Fig. 2, we assume that the shunt components are all inductors, the series

TABLE I
COMPONENT VALUES FOR THE MATCHING NETWORKS OF Fig. 1(a) AND (b) FOR $R_p = 50 \Omega$ AND $R_s = 3.125 \Omega$

Frequency	Matching network in Fig. 1(a)		Matching network in Fig. 1(b)	
	Ls	Cp	Lp	Cs
25 MHz	77.1 nH	493 pF	82.2 nH	526 pF
50 MHz	38.5 nH	247 pF	41.1 nH	263 pF
100 MHz	19.3 nH	123 pF	20.6 nH	132 pF

TABLE II
COMPONENT VALUES FOR THE MULTISTAGE MATCHING NETWORK IN FIG. 2 FOR $R_p = 50 \Omega$ AND $R_s = 3.125 \Omega$

Matching network in Fig. 2, n=2								
Frequency	Lp1	Cs1	Lp2	Cs2				
25 MHz	184 nH	294 pF	45.9 nH	1176 pF				
50 MHz	91.9 nH	147 pF	23.0 nH	588 pF				
100 MHz	45.9 nH	73.5 pF	11.5 nH	294 pF				
Matching network in Fig. 2, n=4								
Frequency	Lp1	Cs1	Lp2	Cs2	Lp3	Cs3	Lp4	Cs4
25 MHz	318 nH	255 pF	159 nH	509 pF	79.6 nH	1019 pF	39.8 nH	2037 pF
50 MHz	159 nH	127 pF	79.6 nH	255 pF	39.8 nH	509 pF	19.9 nH	1019 pF
100 MHz	79.6 nH	63.7 pF	39.8 nH	127 pF	19.9 nH	255 pF	9.95 nH	509 pF

TABLE III
CALCULATED AND SIMULATED RESULTS FOR THE MATCHING NETWORKS IN FIG. 1 AND FIG. 2

Frequency	Q_L	Fig. 1(a)		Fig. 1(b)		Fig. 2 n=2		Fig. 2 n=4	
		$\eta_{sim}(\%)$	$\eta_{cal}(\%)$	$\eta_{sim}(\%)$	$\eta_{cal}(\%)$	$\eta_{sim}(\%)$	$\eta_{cal}(\%)$	$\eta_{sim}(\%)$	$\eta_{cal}(\%)$
25 MHz	60	93.6	93.6	93.6	93.6	94.1	94.3	93.2	93.5
	100	95.9	96.1	95.9	96.1	96.3	96.6	95.7	96.1
	200	97.7	98.1	97.7	98.1	97.9	98.3	97.6	98.0
50 MHz	60	93.6	93.6	93.6	93.6	94.1	94.3	93.2	93.5
	100	95.9	96.1	95.9	96.1	96.3	96.6	95.7	96.1
	200	97.7	98.1	97.7	98.1	97.9	98.3	97.6	98.0
100 MHz	60	93.6	93.6	93.6	93.6	94.1	94.3	93.2	93.5
	100	95.9	96.1	96.0	96.1	96.3	96.6	95.7	96.1
	200	97.7	98.1	97.7	98.1	97.9	98.3	97.6	98.0

components are all capacitors, and the Q_i for each stage is the same. The component values for two- and four-stage designs are shown in Table II.

Efficiency results are listed in Table III for both calculated values using (20) and (21) and for simulations of the circuits in PSPICE. The simulation results show excellent agreement with the calculations. The maximum efficiency is about 98% when $Q_L = 200$ and approximately 93% when $Q_L = 60$. As expected, multistage matching networks don't provide a significant advantage (especially given the additional components required) because the required transformation ratio is not very large.

IV. EXPERIMENTAL RESULTS

In order to verify the theoretical calculations of (20) and (25), experiments were carried out using the experimental setup of Fig. 6 (equipment indicated in Table IV). The test

setup is designed to measure the performance of back-to-back connections of identical matching networks which transform impedance away from 50Ω and back to 50Ω . Cascading matching networks in this manner provides an increased loss which is easier to measure than that of a single network. Moreover, this method enables all power measurements to be made at 50Ω with a single power meter, thus providing for more accurate calculation of efficiency than could be obtained otherwise.

To find matching network efficiency, the forward and reflected powers are measured, with the same power meter, as at each of the two locations indicated in Fig. 6, and it is verified that the reflected power is low, indicating a good impedance match. (A $50\text{-}\Omega$ through-connector is utilized in whichever location the power meter is not used.) The efficiency of the matching network cascade is calculated as the ratio of the net power flow, forward minus reflected, measured at the load

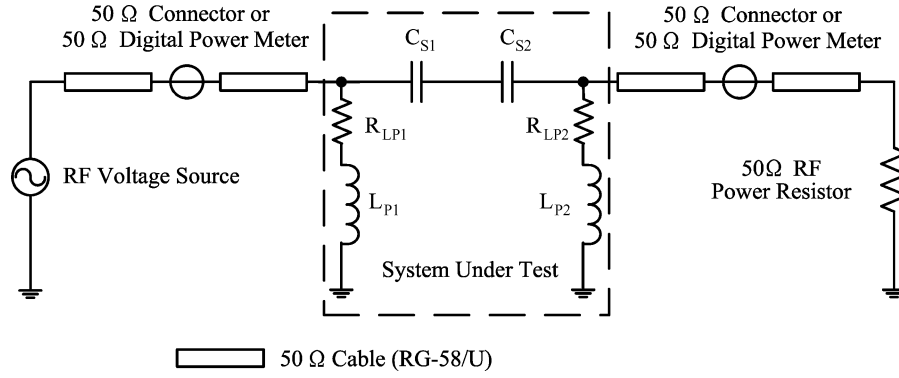


Fig. 6. Experimental setup for validating matching network efficiency calculations. Equipment and component values are detailed in Tables IV and V. The 50- Ω power meter can be placed in either location indicated, as described in the experimental methods.

TABLE IV
EQUIPMENT USED IN THE EXPERIMENTAL SETUP OF FIG. 6

Equipment	Model
RF Voltage Source	Agilent 33250A Waveform Generator plus AR 150A100B Power Amplifier
Digital Power Meter	BIRD Digital RF Power Meter Model 5000-EX with Series 5010 Thruline Directional Power Sensor and 25-60 MHz DPM sense elements.
50 Ω RF Power Resistor	BIRD Termline Coaxial Resistor 8401

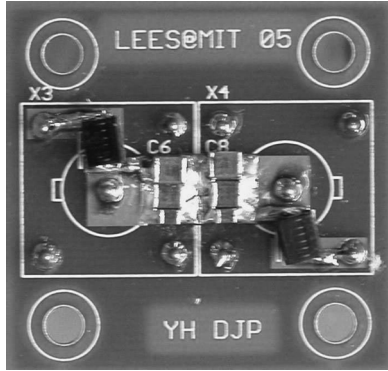


Fig. 7. Experimental back-to-back matching network cascade used in the setup of Fig. 6. The illustrated circuit has a voltage transformation ratio to the intermediate node of 4.27:1.

side to that measured at the source side. This measurement and calculation procedure eliminates scale factor errors in the power measurements, e.g., due to limits on absolute accuracy of the power meter.

Fig. 7 shows a back-to-back matching network cascade for the test setup of Fig. 6. The matching network cascade has the topology indicated in Fig. 6 and is implemented on a printed circuit board with 50- Ω BNC connectors mounted on the back side of the board. Two such matching network cascades were developed, each designed for a matched input and output resistance of 50 Ω at 50 MHz. The first was designed for a voltage transformation ratio (to the intermediate node) of $V_p/V_s = 3.0$, while the second was designed for a voltage transformation ratio of 4.27 (selected for the ready availability of inductor values). Nominal and measured inductor and capacitor values are indicated in Table V along with measured circuit board parasitics.

The expected efficiency of the matching network cascade can be calculated as in (21)

$$\eta = \left(1 - \frac{Q}{Q_{LP1}}\right) \left(1 - \frac{Q}{Q_{LP2}}\right). \quad (28)$$

For the matching network cascade with voltage transformation ratio to the intermediate node of $V_p/V_s = 3.0$, $Q = 2.83$ by (1) and (2). From Table V, $Q_{LP1} = \omega L_{P1}/R_{LP1} = 85.88$, and $Q_{LP2} = \omega L_{P2}/R_{LP2} = 83.98$. This results in a calculated efficiency $\eta_{cal} = 93.44\%$. Note that this corresponds to an expected efficiency of each 3:1 stage of approximately 96.66%. Likewise, for the design with $V_p/V_s = 4.27$, $Q = 4.15$ by (1) and (2). From Table V, $Q_{LP1} = \omega L_{P1}/R_{LP1} = 83.69$, and $Q_{LP2} = \omega L_{P2}/R_{LP2} = 81.93$, resulting in $\eta_{cal} = 90.21\%$.

The experimental results for the two designs are shown in Tables VI and VII. All data were measured with the rf digital power meter. P_{Fwd} is the input forward power to the matching network cascade. Due to the component tolerances and printed circuit board parasitics, there is a small amount of mismatch between the 50- Ω cable and the matching network input, resulting in a small reflected power measured by the power meter. The net input power is calculated as $P_{in} = P_{Fwd} - P_{Ref}$. Because the load is a tightly specified 50- Ω resistor and it matches well with the cable, there is no measured reflected power from the load resistor. Ten groups of data at different power levels were acquired for each design. The efficiencies are averaged to reduce the effects of sensor limitations. The average experimental efficiencies η_{exp} are very close to the theoretical results η_{cal} . η_{cal} is a little higher, at least in part, because the capacitor losses aren't considered in (28). From the capacitor data sheet, capacitor quality factor is roughly 1000, which accounts for 0.3% efficiency loss ($V_p/V_s = 3.00$) and 0.4% efficiency loss

TABLE V
COMPONENT TYPES AND VALUES FOR THE EXPERIMENTAL MATCHING NETWORK CASCADE USED IN THE TEST SETUP OF FIG. 6. MEASURED VALUES FOR CIRCUIT-BOARD PARASITICS ARE ALSO INDICATED. ALL MEASURED VALUES WERE OBTAINED AT A FREQUENCY OF 50 MHz USING AN AGILENT 4395A NETWORK/SPECTRUM/IMPEDANCE ANALYZER

Component Values for Transformation Ratio $V_p/V_s = 3.00$.					
Component Name	Nominal Value	Manufacturer and Part Style	Part Number	Measured Value	PC Board Parasitic Capacitance Value
L_{P1}	56 nH	Coilcraft	1812SMS-56N	55.59 nH	≈ 2.4 pF
R_{LP1}				0.197 Ω	
L_{P2}	56 nH	Coilcraft	1812SMS-56N	55.40 nH	≈ 2.4 pF
R_{LP2}				0.201 Ω	
C_{S1}	100 pF $\times 2$	CDE	MC12FA101J	99.91 pF + 100.18 pF	≈ 1.4 pF
C_{S2}	100 pF $\times 2$	CDE	MC12FA101J	101.82 pF + 100.42 pF	≈ 1.4 pF
Component Values for Transformation Ratio $V_p/V_s = 4.27$.					
Component Name	Nominal Value	Manufacturer and Part Style	Part Number	Measured Value	PC Board Parasitic Capacitance Value
L_{P1}	39 nH	Coilcraft	1812SMS-39N	37.86nH	≈ 2.4 pF
R_{LP1}				0.139 Ω	
L_{P2}	39 nH	Coilcraft	1812SMS-39N	38.03 nH	≈ 2.4 pF
R_{LP2}				0.143 Ω	
C_{S1}	100 pF $\times 2$ + 68 pF + 6 pF	CDE	MC12FA101J MC12FA680J MC08CA060D	99.86 pF + 102.02 pF + 69.64 pF + 5.99 pF	≈ 1.4 pF
C_{S2}	100 pF $\times 2$ + 68 pF + 6 pF	CDE	MC12FA101J MC12FA680J MC08CA070D	99.84 pF + 102.27 pF + 69.67 pF + 6.91 pF	≈ 1.4 pF

TABLE VI
EXPERIMENTAL RESULTS FOR THE MATCHING NETWORK CASCADE WITH AN INTERMEDIATE VOLTAGE TRANSFORMATION RATIO $V_p/V_s = 3.00$

$P_{Fwd}(W)$	$P_{Ref}(W)$	$P_{in}(W) = P_{Fwd} - P_{Ref}$	$P_{out}(W)$	$\eta_{exp}(\%) = P_{out}/P_{in}$	$\eta_{cal}(\%)$
5.15	0	5.15	4.85	94.18	93.44
10.60	0	10.60	9.80	92.45	
15.40	0	15.40	14.40	93.51	
20.20	0.04	20.16	18.60	92.26	
26.30	0.05	26.25	24.50	93.33	
30.20	0.07	30.13	28.00	92.93	
35.90	0.08	35.82	33.45	93.38	
42.30	0.10	42.20	39.30	93.13	
46.45	0.12	46.33	43.30	93.46	
50.00	0.13	49.87	46.50	93.24	
Average				$\eta_{exp}(\%)$	93.29

($V_p/V_s = 3.00$) in a single-stage matching network accounting for much of the small differences between calculated and experimental results. Still more accurate calculation results can be achieved by (16) and (18). Experimental measurements thus confirm the accuracy of the models for matching network efficiency introduced in Section II.

It is also useful to consider the difference between the experimental results with a 3:1 and a 4.27:1 (intermediate) voltage transformation ratio. The design for the 4.27:1 case resulted in a higher percentage of reflected power at the matching net-

work input, corresponding to a larger mismatch between the desired 50 Ω and the driving point impedance provided by the matching network cascade. This may be attributed both to the higher losses and the higher transformation quality factor Q in the 4.27:1 case. As Q increases, the design provides an increasingly narrow frequency band over which the desired impedance match is provided, and the impedance match becomes more sensitive to component tolerances. This suggests that the use of higher-order matching networks may be motivated by concerns other than efficiency if large transformation ratios are desired.

TABLE VII
EXPERIMENTAL RESULTS FOR THE MATCHING NETWORK CASCADE WITH AN INTERMEDIATE VOLTAGE TRANSFORMATION RATIO $V_p/V_s = 4.27$

$P_{Fwd}(W)$	$P_{Ref}(W)$	$P_{in}(W) = P_{Fwd} - P_{Ref}$	$P_{out}(W)$	$\eta_{exp}(\%) = P_{out}/P_{in}$	$\eta_{cal}(\%)$
5.40	0.24	5.16	4.60	89.15	90.21
10.60	0.49	10.11	9.15	90.50	
15.80	0.75	15.05	13.50	89.71	
20.48	0.98	19.50	17.30	88.72	
25.00	1.20	23.80	21.41	89.96	
30.35	1.47	28.88	26.03	90.13	
34.36	1.66	32.70	29.61	90.56	
40.66	1.98	38.68	34.68	89.67	
45.55	2.22	43.33	38.95	89.89	
50.65	2.48	48.17	43.34	89.97	
Average				$\eta_{exp}(\%)$	89.92

V. CONCLUSION

This letter presents analysis and design considerations for lumped (inductor and capacitor) matching networks operating at high efficiency (>95%). Formulas [see (19), (20), and (25)] for calculating matching network efficiency are given, and it is shown that efficiency can be expressed as a function of inductor quality factor Q_L , capacitor quality factor Q_C , and transformation ratio. These formulas are used to evaluate the optimum number of L -section matching stages as a function of conversion ratio. Both simulation and experimental results are presented that validate the analytical formulation. For a typical required voltage transformation ratio of 3–5 (e.g., for a resonant dc/dc power converter design), one can expect to achieve matching network efficiencies between 96% and 98.5%

for inductor quality factors of 100–200. Efficiency can be improved through higher quality factor magnetics, but efficiencies exceeding 99% are likely to be challenging to achieve with this approach.

REFERENCES

- [1] C. Bowick, *RF Circuit Design*. London, UK: Newnes, 1997, ch. 3, pp. 66–75.
- [2] W. L. Everitt and G. E. Anner, *Communication Engineering*, 3rd ed. New York: McGraw-Hill, 1956, ch. 11.
- [3] T. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed. Cambridge, UK: Cambridge Univ. Press, 2004, pp. 87–107.
- [4] E. Gilbert, "Impedance matching with lossy components," *IEEE Trans. Circuits Syst.*, vol. 22, no. 2, pp. 96–100, Feb. 1975.
- [5] L. Rade, *Mathematics Handbook for Science and Engineering*, 5th ed. New York: Springer, 2004, p. 49.