

# A Low-Power Reconfigurable Analog-to-Digital Converter

by

**Kush Gulati**

B.E., Electronics and Communication Engineering, Delhi Institute of Technology, New Delhi (1993)  
M.S., Electrical Engineering and Computer Science, Vanderbilt University, Nashville (1995)

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in partial fulfillment of the requirements for the degree of

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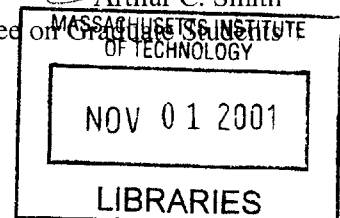
Certified by \_\_\_\_\_

Hae-Seung (Harry) Lee  
Professor of Electrical Engineering and Computer Science  
Thesis Supervisor

Accepted by \_\_\_\_\_

Arthur C. Smith  
Chair, Department Committee on Graduate Studies

BARKER





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## **ABSTRACT**

This thesis presents the concept, theory and design of a low power CMOS analog-to-digital converter that can digitize signals over a wide range of bandwidth and resolution with adaptive power consumption. The converter achieves the wide operating range by reconfiguring (1) its architecture between pipeline and delta-sigma modes (2) by varying its circuit parameters such as size of capacitors, length of pipeline, oversampling ratio, among others and (3) by varying the bias currents of the opamps in proportion with converter sampling frequency, accomplished through the use of a phase-locked loop. Target input signals for this ADC include high frequency and moderate resolution signals such as video and low I.F. in radio Receivers, low frequency and high resolution signals from seismic sensors and MEMs devices, and others that fall in between these extremes such as audio, voice and general purpose data-acquisition.

This converter also incorporates several power reducing features such as thermal noise limited design, global converter chopping in the pipeline mode, opamp scaling, opamp sharing between consecutive stages in the pipeline mode, an opamp chopping technique in the delta-sigma mode, and other design techniques. The opamp chopping technique achieves faster closed-loop settling time and lower thermal noise than conventional design.

At a converter power supply at 3.3V, the converter achieves a bandwidth range of 0–10MHz over a resolution range of 6 –16 bits, and parameter reconfiguration time of 12 clock cycles. Its PLL lock range is measured at 20KHz to 40MHz. In the delta-sigma mode, it achieves a maximum SNR of 94dB and second and third harmonic distortions of 102dB and 95dB, respectively at 10MHz clock frequency, 9.4KHz bandwidth, and 17.6mW power. In the pipeline mode, it achieves a maximum DNL and INL of +/-0.55LSBs and +/-0.82LSBs, respectively, at 11-bits of resolution, at a clock frequency of 2.6MHz and 1MHz tone with 24.6mW of power.

### **Thesis Supervisor:**

Hae-Seung (Harry) Lee

Professor of Electrical Engineering and Computer Science



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# Dedication

*To my family*



# Biography

Kush Gulati was born in Nagpur, India in 1971. He received the B.E. degree in Electronics and Communication Engineering from Delhi Institute of Technology (now known as the Netaji Subhas Institute of Technology), Delhi, India in 1993 and M.S. degree in Electrical and Computer Engineering in 1995 from Vanderbilt University, Nashville, TN.

Between 1993 and 1995, he worked on circuit techniques for minimizing susceptibility of DRAMs to alpha particles and cosmic ions.

Since September, 1995 he has been with the M.I.T. Microsystems Technology Laboratories, working towards his Ph.D. in the area of analog circuit design. His current research interests include low-power, high-performance analog integrated circuit design.



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# 1 Introduction

This thesis describes a low power analog-to-digital converter (ADC) that possesses the capability, in contrast to conventional converters, of digitizing a wide range of input bandwidth ranging from 1Hz to 20MHz, and of being able to produce resolution ranging from 6-bits to 16-bits while maintaining the minimum possible power consumption through this bandwidth/resolution space.

This vast operating space allows this converter to be employed for digitizing a variety of analog signals including low intermediate-frequency and baseband signals required in radio receivers, video data, voice, audio, seismic signals, and signals from micro-mechanical machined devices such as accelerometers and pressure transducers. Each of these signals demands different resolution and bandwidth of the converter. A possible subset of applications envisioned for the converter is depicted in Figure 1-1. The blocks within the figure show the converter operating range that would be required for these applications.

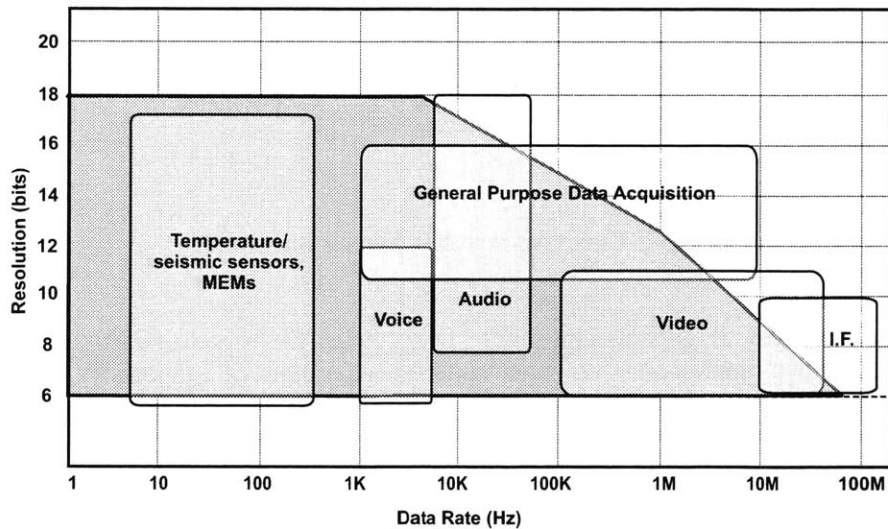


Figure 1-1: Application Space.

A converter with such a vast application space and optimized power consumption can be programmed either by the user or the manufacturer for targeting single fixed applications much like how field-programmable-gate-arrays are used. Employed in this manner, it could serve to dramatically reduce the time-to-market of products involving custom data converters.

Its real-time configuring capability, on the other hand, makes it possible to use such a converter in novel ways that would not be normally possible with custom-built solutions. It could be used to either handle, in real time, several different signals or instead to cater to changing specifications of the same application. A possible example of the former scenario is a universal wireless sensor as described below. Examples corresponding to the latter scenario include multi-standard systems, as well as variable quality of service systems as are commonly desired in present day communication systems. These scenarios are also described below.

Figure 1-2 shows a block diagram of a battery-operated wireless multi-sensor device [1] that includes a set of sensors, a converter, digital-signal-processing, a radio transceiver and a power system. Such a device could be used to sense, digitize, process, and transmit a variety of signals from its installed location to a remote base-station, with potential applications as a reconnaissance device and human-body sensing, among others. A reconfigurable converter with variable specifications and power would be the ideal candidate for a device of this nature not only because of its multi-signal conversion capability but also because of its ability to minimize power consumption and its small area.

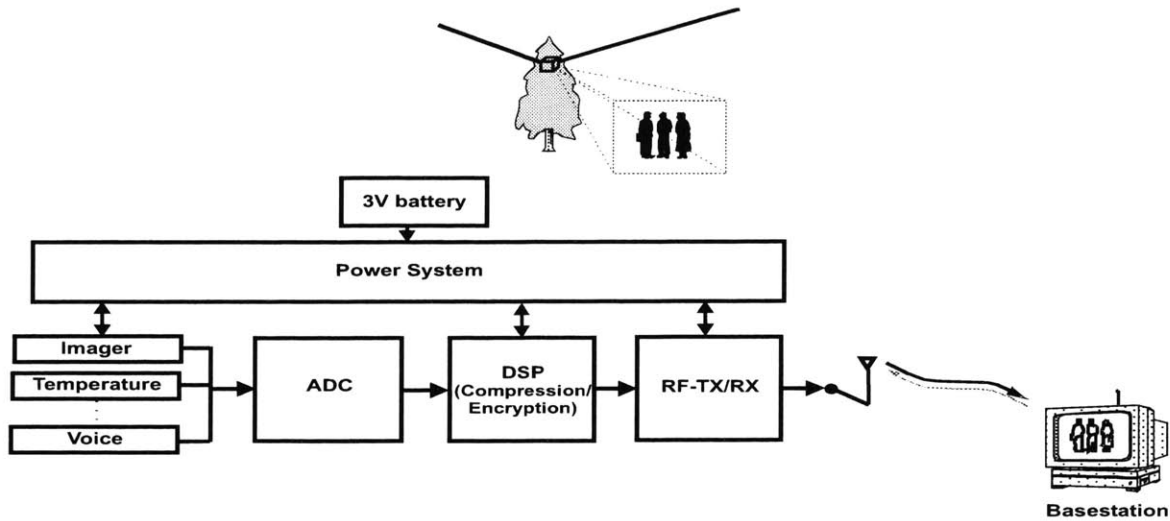


Figure 1-2: Universal Wireless Sensor Illustration.

The communications industry is experiencing explosive growth. The trend towards an ever increasing variety in communications applications as well as a proliferation of standards for each of these applications demands methods by which radio transceivers can be made to operate over a variety of specifications. Communications applications include cellular telephony, cordless telephony, satellite communications, pagers, wireless LANs [2][3][4][5][6][7][8]. Some of their corresponding standards are summarized in the following table along with bandwidth and dynamic range requirements for a converter used for implementing the standard. A single converter that can be reconfigured to adapt to these various standards towards the goal of creating a single universal transceiver is highly desirable.

Application	Standard	Bandwidth	SNDR
Cellular Telephony	AMPs	30KHz	-
	GSM	200KHz	84db
	WCDMA	5MHz	51dB
Cordless Telephony	DECT	700KHz	72dB
	CT2	10KHz	-
Paging Devices	FLEX (Motorola)	25KHz	-
Satellite Communications	GPS	2MHz	29.8dB
Wireless LAN	IEEE802.11B	22MHz	48dB



Another sought-after feature of a communication device is the possibility of adapting the performance of its electronics to the surrounding conditions. Sensitivity and selectivity [2] are two features of a communication device that can be tuned. If this communication device is in close proximity to its base-station, its sensitivity and hence the signal-to-noise ratio of the converter can be reduced leading to reduced power. If there are several other transmitting equipment in the neighborhood of this device, its selectivity and hence the dynamic range of the converter will need to be scaled up.

### **Construction of a wide operating range digitization system**

The first question to ask is why it is not possible for a conventional converter to digitize over a wide operating range. There are several basic converter architectures such as the pipeline, delta-sigma, cyclic, flash, successive approximation, and integrating converters. Each of these architectures possesses strengths and weaknesses that make them more amenable to working in certain ranges. They either will not work outside of these ranges or may consume prohibitively high power compared to other topologies. Even within these ranges, their performance level may be dictated by certain circuit parameters that generally are fixed for a given design. For example, converters typically consist of opamps that work at a certain speeds dictated by the bandwidth required of them. For making them work at different speeds, a method is needed to change their bandwidth in an efficient way. Likewise, resolution of certain type of converter is fixed by the thermal noise contribution of the components within it, thus the best resolution of the ADC is fixed for a given design.

There are two strategies for creating such a wide operating range digitization system: One option is to employ a single very high-performance ADC that can work at the highest common denominator of resolution and sampling rate. This would be either infeasible or extremely power inefficient.

The second strategy is to employ multiple A/D converter architectures each specified to cover a small sector in the entire two-dimensional resolution and sampling rate space. Such a converter implementation, however, would require a prohibitively large number of ADCs to achieve optimal power consumption with a reasonably fine granularity over input bandwidth and resolution. To illustrate this point consider, as an example, the fraction of the application space bounded by bandwidth and resolution ranging between 20Hz-20KHz and 6-16 bits, respectively; in order for the system to achieve a power consumption that in the worst case is as much as four times the optimal level, the system would need to include 50 different converters. This would be unacceptable for a portable system. In a discrete chip implementation, there would be a tremendous power overhead due to PCB wiring to connect these up, making such an implementation unattractive from the perspective of a portable system. Currently there is a push towards system-on-a-chip solutions; these systems can eliminate delays encountered due to PCB trace capacitance and hence lead to lower overall system power. A system with such a large number of ADCs precludes a system-on-a-chip solution.

A single ADC with reconfigurable parameters and reconfigurable topology would be able to achieve the above goal. Prior reconfigurable ADCs, however, achieve very limited reconfigurability.

For example, variable resolution in a delta-sigma converter has been proposed by changing OSR and bias currents of the converter over a predetermined set of values obtained from a look-up table [15]. This fixed arrangement offers relatively limited resolution reconfigurability, while its fixed delta-sigma architecture restricts its bandwidth to the low end. In addition, relying upon a predetermined bias current for each oversampling ratio works only if the relationship of speed of the operational amplifiers versus its bias current is fixed. However, this relationship does not hold over different fabrication processes. Even within the same process, it is not possible to know this relationship in advance of building the chip. This is especially true since bias current variation would place the input devices of the opamps into different

regimes. While it is possible to execute a calibration run for a given process and chip, calibration adds significant cost.

Another ADC with limited configurability, operates only at select values of 10bit / 3Msps, 8bit / 4Msps and 4bit / 8Msps [16]. Other examples of prior reconfigurable solutions include a flash ADC with two settings [17][18] and a cyclic ADC that can be configured for 8, 13, or 16 bits [19].

This work proposes the idea of a single converter [20][21] that can morph itself into different topologies to cover the desired continuum of resolution and bandwidth space with minimum power at each performance level. The proposed converter is designed to provide a significantly larger reconfigurability space.

### **Organization of this thesis**

A brief description of conventional architectures considered in this thesis is presented in Chapter 2 as a prelude to the description of the reconfigurable converter. The conceptual framework of the reconfigurable converter is discussed in Chapter 3, while the system level architecture of this converter is presented in chapter 4.

Selected circuits of major sub-blocks of the converter as well as testability considerations are described in Chapter 5. The converter employs a phase-locked loop for tuning the bandwidth of the opamps to the clock frequency of the converter. The concept for this technique as well as architectural and circuit details of the PLL are presented in Chapter 6.

The converter was successfully characterized over a bandwidth range of 0-10MHz and a resolution range of 6-bits to 16-bits with power consumption that is competitive with respect to state-of-art converters that were custom built for various performance points. Its phase-locked loop was shown to have a locking range of over three orders of magnitude from 20KHz to 40MHz. These and other test and measurement results are shown in Chapter 7.

Chapter 8 provides the concluding summary of this thesis and offers suggestions for the next generation reconfigurable converter.

Appendix A details the design, theory and implementation of a high-swing operational amplifier, Appendix B delves into a study of residue plots of a pipeline converter and a methodology to determine architectural errors based on histograms obtained from measurement. Appendix C and D detail lab troubleshooting tips. Finally, Appendix E derives the exact expression for opamp slewing time.

## 2 Conventional Converter Design

This chapter focuses on the concept, architecture and design of analog-to-digital converters that have been considered in the design of the reconfigurable converter. It is not the purpose of this chapter to provide detailed information about these architectures. Rather, it is the intention of this section to serve as a prelude to the architecture and design of the reconfigurable converter.

Section 2.1 and 2.2 describe the pipeline and cyclic converters, both of which are Nyquist-rate converters, while Section 2.3 presents an overview of the oversampling noise-shaped converter.

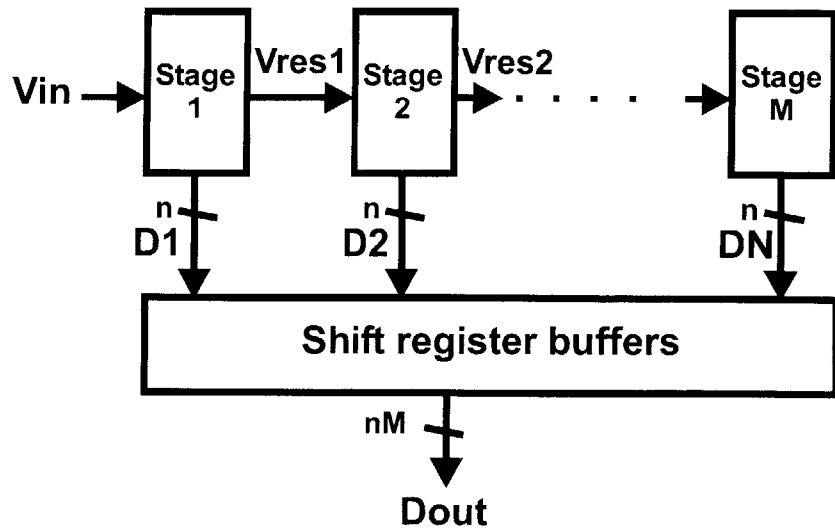
For more detailed information on the following architectures, the reader is encouraged to refer to the following excellent resources: [10][11][12][23][24][25][27][31][32][33][34][35].

### 2.1 Pipeline Converter

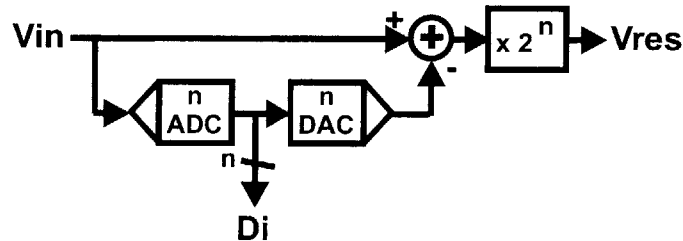
#### 2.1.1 Operation and Architecture

Figure 2-1a-b show a generalized basic architecture of a pipeline converter. Conceptually, this architecture is based on a binary search algorithm, in which the converter goes through a process of determining the location of the input signal in reference to a predetermined quantized voltage range.

The architecture consists of a cascade of stages as shown in the figure, each of which produces an  $n$ -bit digital code. The output of the converter is the concatenation of the digital codes from each of these stages. The structure of each stage is shown in Figure 2-1b. Each stage consists of an  $n$ -bit A/D converter that corresponds to the stage output  $D_i$ . This digital code is converted back to analog format using a D/A converter and then subtracted from the analog input. The difference is then amplified by a  $2^n$  multiplier to produce a voltage residue. This voltage residue is processed similarly by the next stage which then produces the next set of digital code and its own voltage residue. This process is continued through the  $M$  stages to produce  $M$  distinct  $n$ -bit words. A set of shift register buffers is required to time-align the words from these different stages since each stage produces code corresponding to the same analog input at different times. The output of the converter corresponds to a serial concatenation of all these digital codes to form an  $nM$ -bit digital output that corresponds to the analog input. While this architecture shows each stage producing the same number of bits, this is not necessary. A popular value for stage resolution is 1-bit, and this is the stage resolution employed in the pipeline mode of this converter.



(a)



(b)

Figure 2-1: Generalized pipeline architecture.

### 2.1.2 Circuit Implementation

A typical switched-capacitor half-circuit implementation of each stage of a 1-bit/stage pipeline converter is shown in Figure 2-2. The circuit employs two capacitors  $C1$  and  $C2$ , an opamp, a comparator and several switches.

The 2-phase clocking employed for this structure is shown below the figure. During phase  $ck1$ , the two capacitors are connected between the input  $V_{in}$  and the input common-mode level  $v_{icm}$ . Meanwhile the comparator compares the input to zero and generates a bit  $D_i$  corresponding to whether the input is above or below the threshold level. During the next phase  $ck2$ , capacitor  $C2$  is connected across the opamp, while the left plate of capacitor  $C1$  is connected to either a positive reference  $v_{refp}$  or a negative reference  $v_{refn}$  depending on the decision of the comparator in the previous phase. This arrangement implements a stage transfer function as follows:

$$V_o = \frac{C1 + C2}{C2} \cdot V_{in} + D_i \cdot \frac{C1}{C2} \cdot V_{ref} \quad (2.1)$$

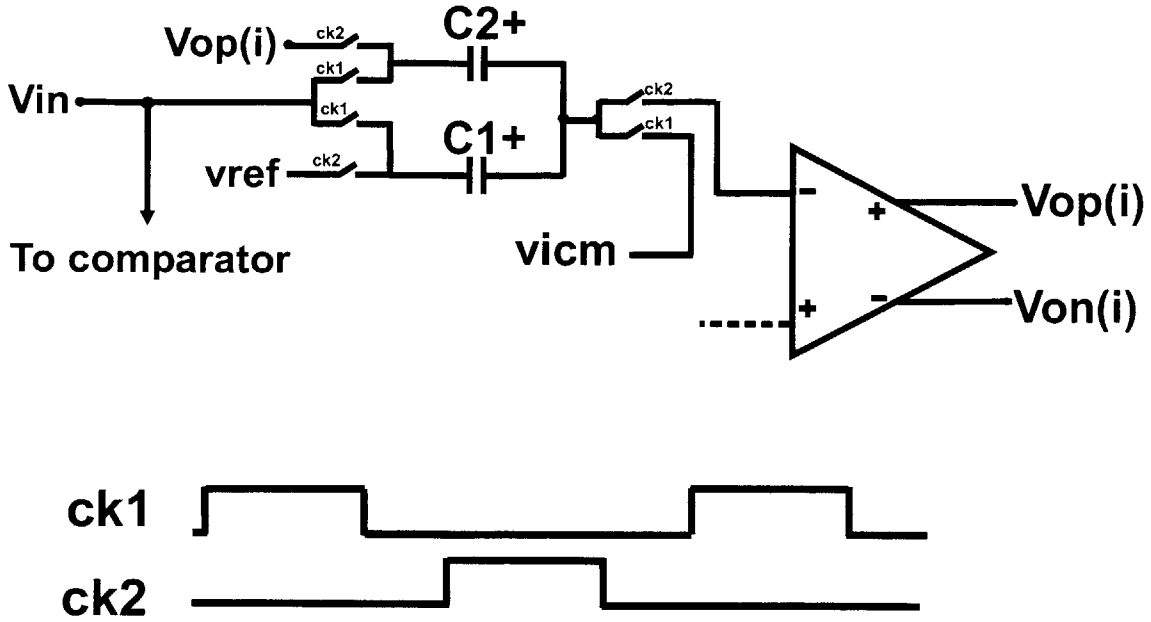


Figure 2-2: Switched-capacitor implementation of a single stage of the pipeline architecture.

Ideally  $C1=C2$ , therefore, the transfer function simplifies to:

$$V_o = 2 \cdot V_{in} + D_i \cdot V_{ref} \quad (2.2)$$

The value of  $D_i$  is determined as follows:

$$\begin{aligned} D_i &= -1 \quad \text{for } V_{in} < 0 \\ D_i &= 1 \quad \text{for } 0 < V_{in} \end{aligned} \quad (2.3)$$

The digital decision outputted by the stage is then 0 for the range  $V_{in} < 0$  and 1 for the range  $0 < V_{in}$ . The architecture described above is very susceptible to comparator offset. A popular method of minimizing this problem is a 1.5-bit/stage digital error correction [26] scheme. This scheme requires the use of two comparators to create two break points, instead of one, to generate three different decisions, summarized as follows:

$$\begin{aligned} D_i &= -1 \quad \text{for } V_{in} < -V_a \\ D_i &= 0 \quad \text{for } -V_a < V_{in} < +V_a \\ D_i &= 1 \quad \text{for } +V_a < V_{in} \end{aligned} \quad (2.4)$$

An optimal value for  $V_a$  is  $V_{ref}/4$ . The transfer characteristic of the stage is illustrated in the following residue plot. The use of the digital error correction scheme shifts the function in Zone B away from the  $+V_{ref}$  and  $-V_{ref}$  levels, as shown below. To elaborate,  $V_{ref}$  is subtracted from the transfer characteristic of a conventional converter in the region  $-V_a < V_{in} < 0$ , while  $V_{ref}$  is added to the transfer characteristic through the region  $0 < V_{in} < +V_a$ . The digital decisions outputted by the stage is then 00

for the range  $V_{in} < -V_a$ , 01 for the range  $-V_a < V_{in} < +V_a$  and 10 for the range  $+V_a < V_{in}$ . The second bit in the output is added to the MSB of digital word obtained from the rest of the converter stages. Essentially, by outputting a 01 decision for the zone in the middle, the analog manipulation of the transfer characteristic for the 1.5-bit/stage digital error correction scheme is compensated for in the digital domain.

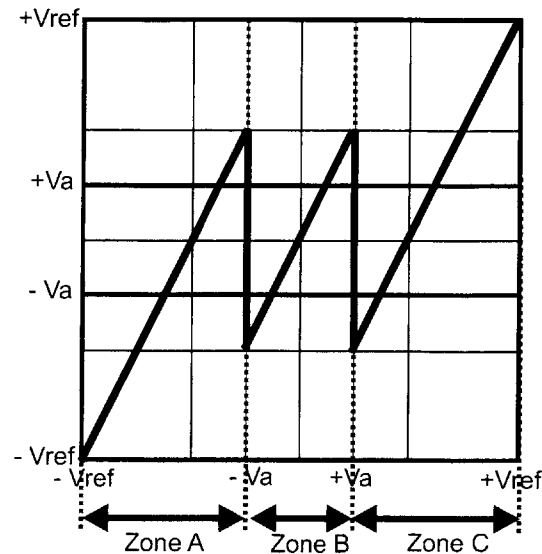


Figure 2-3: Residue plot of a single pipeline stage with digital error correction.

### 2.1.3 Non-idealities in Pipeline Converters

The pipeline converter as described above has several error sources causing one or more of the following manifestations in the residue plot.

1. Stage offset
2. Stage gain error
3. Stage transition point shift
4. Nonlinear variation of the transfer characteristic

Each of these stage manifestations stems from a circuit non-ideality such as opamp offset, charge injection, low opamp gain, mismatch between capacitors C1 and C2, among others. The reader is referred to [10][12][29] for a comprehensive review of these circuit non-idealities. More details on the impact of the above residue plot non-idealities on the overall performance of the converter is presented in the Appendix B.

## 2.2 Cyclic Converter

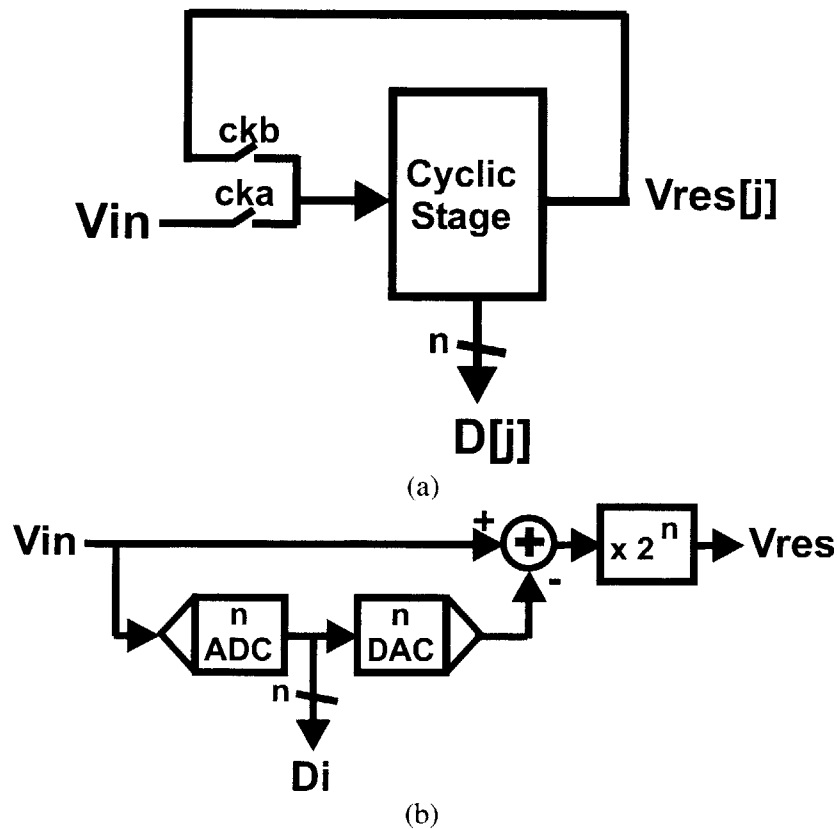
### 2.2.1 Operation and Architecture

The cyclic converter is based on the same concept as the pipeline converter. In fact, it behaves much like a pipeline converter. The overall architecture of a cyclic converter is shown in Figure 2-4a. Figure 2-4b shows a single stage that looks identical to a pipeline converter. The difference between this structure and

the pipeline, however, is that while a pipeline converter pumps the residue of a stage into another stage, the cyclic converter recycles the residue back to the input of the same stage. Hence while the pipeline converter has  $M$  stages working in parallel, the cyclic converter has only one stage that does the job of  $M$  stages in  $M$  sequential cycles. The clocking for this architecture is shown in Figure 2-4c. During the first cycle of the conversion period, the stage samples the converter input, when clock phase  $cka$  is high. During the next  $M-1$  cycles, the stage samples its own output during the time when clock phase  $ckb$  is high. Each time the stage produces an  $n$ -bit word. The overall digital output is constructed by concatenating the  $M$   $n$ -bit words.

Although only one stage has been shown for simplicity, the cyclic converter can employ a number of stages in cascade as long as it cycles back the residue. A popular stage resolution is 1-bit. In that case, the overall converter resolution is determined by the number of times the converter processes a signal corresponding to a single sample of the converter input.

An important point to note here is that in order to achieve the same input bandwidth as the pipeline converter, the cyclic converter needs to sample the input  $N$  times faster, where  $N$  is the resolution of the converter. However, it employs  $N$  times fewer stages. Hence the overall figure-of-merit of this converter is same as that of the pipeline converter with identical stages. This is not true if the pipeline converter stages are progressively scaled as will be also noted later.



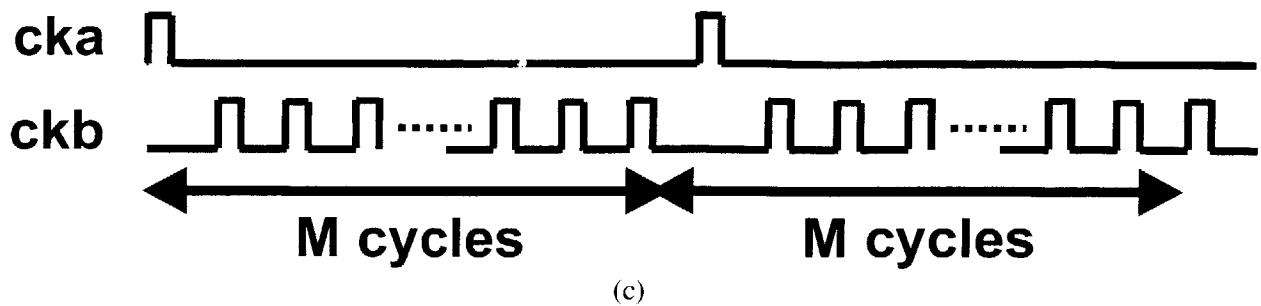


Figure 2-4: Architecture of n-bit/stage cyclic converter. (a) Top-level block diagram. (b) Stage block diagram. (c) Clock scheme.

## 2.2.2 Circuit Implementation and Non-idealities

Since the stage architecture is identical to the pipeline converter, the same circuit, as shown in Figure 2-2 is employed. Of course, an additional scheme that switches the stage input between the converter input and the residue at its output is necessary.

This structure is susceptible to many of the same non-idealities as the pipeline converter.

## 2.3 Delta-Sigma Converter

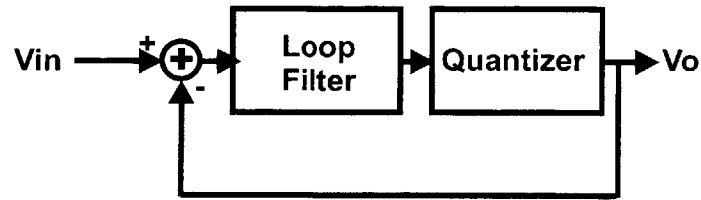
### 2.3.1 Operation and Architecture

The delta-sigma converter is not a Nyquist-rate converter. It works by oversampling its input by a certain oversampling ratio typically ranging from 8 to 1024. The basic architecture of this converter is shown in Figure 2-5a. It has a front-end summer that feeds the difference between the input and the output of a quantizer to a loop filter. The output of the loop filter is converted to an output digital stream by a quantizer.

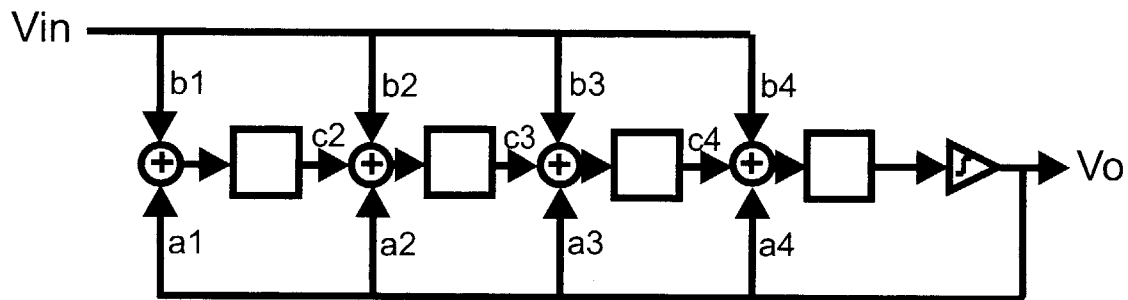
Given this construction, the error introduced by the quantizer is effectively high-pass filtered as seen at the output of the modulator. This process of noise shaping allows this converter to employ a very coarse quantizer, typically 1-bit, and yet have most of this noise occur at frequencies outside the signal bandwidth. Additionally the process of oversampling the input allows a reduction of the thermal noise introduced by the sampling front-end of the converter. Thus oversampling in conjunction with noise-shaping makes this converter an ideal candidate for low-speed and high signal-to-noise ratios.

The basic architecture shown in Figure 2-5a can be implemented in a variety of ways. The low-pass or the loop filter is generally implemented as a cascade of integrators. Applying the feedback from the quantizer in a distributed manner as shown in the bottom of the figure allows enhanced stability. On the other hand, applying the input in a distributed manner allows greater control of the signal transfer function, as shown in Figure 2-5b. It is also possible to apply local feedback across the integrators to obtain greater control over the noise transfer function.





(a)



(b)

Figure 2-5: Architecture of delta-sigma converter.

### 2.3.2 Circuit Implementation

Each stage of the delta-sigma converter, as shown by the Figure 2-5b, requires a 3-input summing integrator. Figure 2-6 shows a switched-capacitor implementation of each of these stages. It employs three capacitors in conjunction with an integrating capacitor. Capacitors  $C_a$ ,  $C_b$  and  $C_c$  implement  $a$ ,  $b$  and  $c$  coefficients as desired by the modulator. Signals  $v_{op}(i-1)$  and  $V_{in}$  refer to the output of the previous stage and the converter input, respectively. Signal  $v_{icm}$  refers to the opamp input common-mode voltage level, while  $v_{ref}$  is a voltage reference that could be either positive or negative depending on the decision from the comparator. In practice, the node marked  $gnd$  would be connected to the output common-mode level. During clock phase  $ck1$ , capacitors  $C_a$ ,  $C_b$  and  $C_c$  sample the common-mode level, the converter input and the previous stage output, respectively. In the next phase, left plate of  $C_a$  is connected to the quantizer output while the left plates of  $C_b$  and  $C_c$  are connected to the common-mode level, while the capacitor plates on the right are connected to the opamp input. This ensures that a charge corresponding to the relevant signals is transferred into the integrating capacitor  $C_f$ . The transfer characteristic of this stage can be written as:

$$Vo(i)[n] = Vo(i)[n-1] - Vq[n] \cdot \frac{Ca}{Cf} + Vin \left[ n - \frac{1}{2} \right] \cdot \frac{Cb}{Cf} + Vo(i-1) \left[ n - \frac{1}{2} \right] \cdot \frac{Cc}{Cf} \quad (2.5)$$

where,  $Vq$  is the quantizer output and  $[n]$  refers to the sample of the relevant signal at time  $n$ . This expression can be rewritten as:

$$Vo[n] = Vo[n-1] - Vq[n] \cdot a + Vin \left[ n - \frac{1}{2} \right] \cdot b + Vo(i-1) \left[ n - \frac{1}{2} \right] \cdot c \quad (2.6)$$

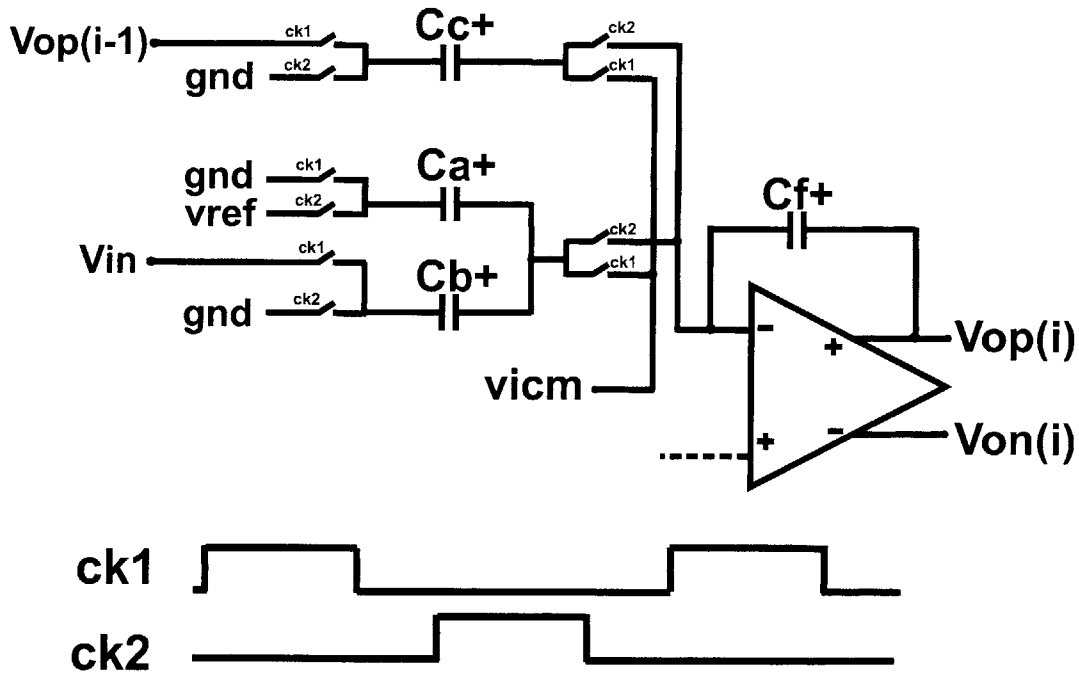


Figure 2-6: Switched-capacitor circuit schematic of one stage of the delta-sigma converter.

An enhancement over the above architecture [39] allows the designer to employ a single reference, while swapping between inverting-mode and non-inverting mode to effectively conform to the desired transfer function. This feature enhances the linearity of the converter.

### 2.3.3 Non-idealities in Delta-Sigma Converters

By virtue of its oversampling noise-shaping nature, this converter is far more robust to circuit non-idealities than its Nyquist-rate counterpart. Fundamentally, however, its signal-to-noise ratio is still limited by  $kT/C$  thermal noise from the sampling front-end. Its linearity and dynamic range is impacted by modulation of signals on the reference by the clock and charge-injection from switches, which is reduced, though not eliminated, by playing tricks with clock delays [13].

## 3 Concept of Proposed ADC

The concept of this ADC stems from the observation that ADC architectures such as the pipeline, cyclic and delta-sigma ADC topologies can cover a wide range of data-rate and resolution. While the pipeline is ideal for low to medium resolutions and medium to high speeds, the delta-sigma architecture can deliver very high resolutions at low to medium speeds. A combination of these architectures can cover a wide digitization space.

These ADC topologies, furthermore, are composed of the same basic components such as opamps, comparators, switches and capacitors. The difference between them, from a network perspective, is the interconnection between these devices. Thus, a converter composed of these basic building blocks in conjunction with a configurable switch matrix, can be made to construct these different topologies and work at different resolutions and bandwidths. At each point in the data-rate versus resolution space, the A/D converter adjusts its topology to minimize the power consumption. For example, if the data-rate requirement is low and the resolution requirement is high, the converter is modified to a delta-sigma architecture. On the other hand, a high data rate dictates the need for a pipeline structure.

Such a solution has one drawback: switch parasitics that lead to performance degradation. This problem has been addressed in the switch capacitor sample/amplify/integrator core by maximizing the re-use of switches between different modes, as will be discussed in detail in a later section.

### 3.1 Reconfiguration Methodology

Reconfiguration of this data converter occurs at three levels: (1) architecture reconfiguration – involving the choice of either the pipeline or the delta-sigma topologies. The converter is in delta-sigma mode for resolution greater than 12 bits; while for lower resolutions, it is in pipeline mode. (2) parameter reconfiguration – in the pipeline mode, the size of the capacitors and the length of the pipeline can be modified while the delta-sigma relies on variation of oversampling ratio (OSR) to change its resolution. Variation of the OSR at a fixed input bandwidth as well as the variation of the input bandwidth in either of the modes demands a method by which the power consumption of the converter can track the sampling rate. This leads us to the third reconfiguration method (3) Bandwidth reconfiguration – where a phase-locked loop (PLL) senses the clock frequency and varies the bias current of the opamps automatically to exactly the value that is necessary for the stage outputs to settle to the appropriate level at that clock frequency.

The reconfiguration methodology is described in greater detail in later sections.

### 3.2 Selection of Architectural Modes

Some of the popular analog-to-digital converter architectures are the flash, pipeline, cyclic, and over-sampling noise shaping (delta-sigma) converters. Each of these architectures is best suited to work over limited ranges of signal bandwidth and desired resolution.

In addition, these architectures each possess a plethora of parametric variational possibilities; examples of these variables include the number of comparators in a flash converter, the number of pipeline stages, the order of the delta-sigma converter, the size of capacitors employed, the coefficients of the delta-sigma, among others. It is this attribute of "parametric variability" of these various architectures that allow them to work and be power optimal over a range of resolution/bandwidth.

The idea behind the process of architecture selection is to select the minimum subset of architectures that bear topological similarity and whose combination of operating ranges covers the entire desired application space. Given this criterion, certain architectures such as the pipeline converter, cyclic converter and the delta-sigma converter lend themselves to the single reconfigurable ADC more so than others.

The pipeline converter is physically composed of cascaded switched-capacitor  $\times 2$  gain and adder stages and is composed of opamps, switched capacitors and comparators. Its conventional form is particularly suitable over a low-medium resolution/medium-high bandwidth. The cyclic converter is essentially very similar to the pipeline converter, but utilizes fewer stages and re-circulates the signal residues cyclically through these stages, thus in essence emulating a number of stages that is an integer multiple of the number of stages it actually possesses. Its simplest form consists of 1 stage. Hence to generate  $N$  bits of digital information, it re-circulates data residues through this stage  $N$  times. The cyclic converter can, therefore, work best at low-medium bandwidths and generates low-medium resolutions. The delta-sigma converter topologically consists of cascaded stages of multiple input switched capacitor integrators and one comparator. Conceptually it works by over-sampling the input and shaping the comparator quantization noise away from the input signal band. It is suitable for low-medium input bandwidths and medium-high resolution.

For the same clock frequency, the single stage cyclic works at  $1/N$ th the bandwidth of the pipeline converter, but also consumes  $1/N$ th the power of an un-scaled pipeline converter; where  $N$  is the desired resolution. However, a pipeline converter in conjunction with opamp scaling (a power saving technique frequently employed) has a higher performance metric than that of the cyclic.

Nonetheless, the cyclic still retains one advantage over the pipeline - being more power efficient than the pipeline converter at very low speeds. The minimum clock speed of any converter is limited by the leakage across the capacitors in its switch-capacitor network. In other words the clock speed of the converter cannot be too low lest the charge across the switched-capacitors (typically in the order of a few tens to hundreds of a femto-farad) leaks out to the extent that the converter fails to meet the desired resolution. Assuming, that both converters sample the input at the Nyquist rate, for the same bandwidth, the clock frequency of the cyclic converter is  $N$  times higher than the pipeline converter – thus the minimum attainable bandwidth of the cyclic converter is  $N$  times lower than that of the pipeline. To address this problem, pipeline converters can operate in a burst-mode or oversampling mode. Therefore, the cyclic was not selected among the architectures implemented in this converter.

Based on the above discussion, the delta-sigma and the pipeline architectures have been chosen for the primary modes of the reconfigurable converter. Since they share the same basic devices such as operational amplifiers, switched capacitors and comparators, a converter composed of basic building blocks each consisting of these common devices could be "configured" to any of these topologies.

# 4 System Level Architecture

## 4.1 System Level Description of Converter

The reconfigurable converter prototype shown in Figure 4-1 contains a main reconfiguring logic that utilizes a user defined “configuration-word” to generate internal control bits to determine the global structure of the converter, the state of each of the basic building blocks B1-B8 and the other peripheral blocks of the converter as shown in the figure. Each of the basic building blocks, described in more detail in the next section, contains a block reconfiguring logic and an analog core. The clock generator module uses the externally generated clock signal to create two non-overlapping phases and three delayed versions of each phase. It then provides these six clock signals along with their complements to the block configuring logic of the cascaded basic building blocks and the other peripherals. The phase-locked-loop utilizes the clock, and determines the appropriate bias current of the converter based on the clock frequency and the resolution desired of the converter. The output interface consists of several buffers for the task of temporal and spatial alignment of the output digital bits. This is explained in more detail in Section 5.6. The output interface then feeds the processed data to the output drivers that in turn send the information out of the chip. An off-chip decimator is employed for low-pass filtering and sample-rate reduction of the output stream while the converter is in the delta-sigma mode.

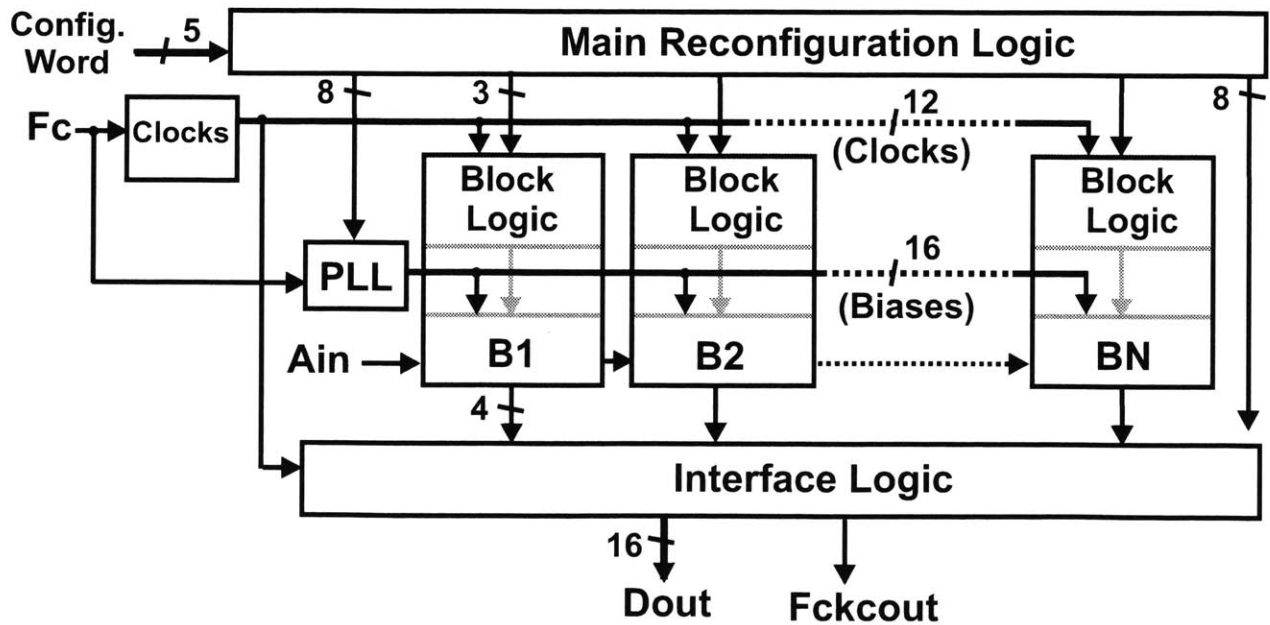


Figure 4-1: Converter Architecture.

## 4.2 Description of Data Converter Block

The basic building block of the converter possesses the capability of being able to work as sample-and-holds and gain stages for two consecutive stages of the pipeline architecture in the pipeline mode and as a multiple input integrating summer while in the delta-sigma mode.

The internal structure of each of the basic building blocks is shown in Figure 4-2. Each building block consists of a block reconfiguring logic, an opamp, several capacitors and switches, a programmable decision box, and an output conditioning logic. The block reconfiguring logic obtains the reconfiguring information from the main reconfiguring logic and creates several static reconfiguring signals for the various parts of the block. Based on the control information it receives from the main reconfiguring logic, it also conditions the clocks that the block receives from the main clock generator. Conditioning the clocks essentially implies controlling the status of the clocks (active or inactive), determining which phase and delayed version of the clock is fed to switches of the switch-capacitor network. It does this based on a variety of information such as the architecture mode, the location of the block within the sliding pipeline architecture, among others. The switched capacitor network and opamp itself are described in the circuit design section. The decision block consists of the several comparators. The state of these comparators, their thresholds, as well as their clocking is determined by the block reconfiguring logic based on information such as the mode of the converter, the location of this block in relation to the cascade of active blocks in the converter etc.

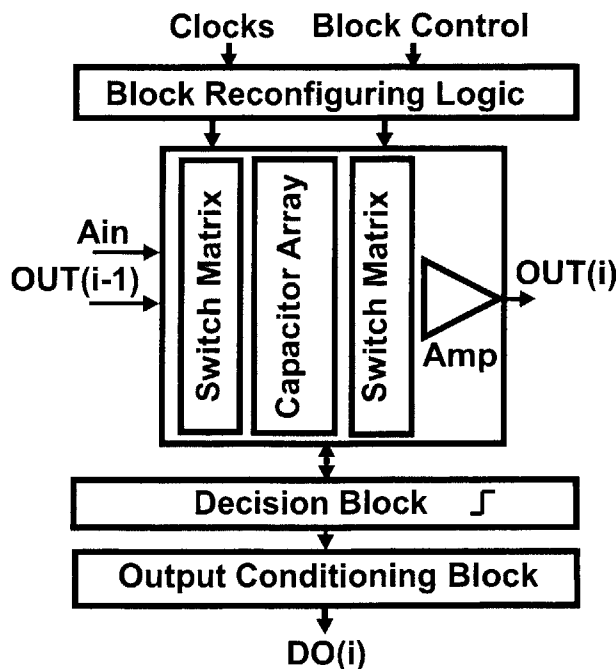


Figure 4-2: Structure of basic building block.

The output-conditioning block determines the flow of the data from each of the blocks to the output interface of the ADC and its neighboring blocks. In particular it determines which of the bits to allow outside of the block. It also contains cascaded buffered stages to drive its large interconnect capacitive loading. This is programmed by a variety of status bits.

## 4.3 Pipeline Mode Architecture

In the pipeline mode, the switched-capacitor portion of each block is transformed to a sample-and-hold and multiply-by-2 stage for two consecutive pipeline stages. The pipeline mode also incorporates a 1.5bit/stage digital error correction scheme [26] that digitally compensates for the offset of the comparator. This implementation of this technique requires two comparators with thresholds at  $\pm V_a$ , where  $0 < V_a < V_{ref}/2$ . Ideally  $V_a$  equals  $V_{ref}/4$ . This comparator pair is contained within the decision block shown in the illustration of the basic building block.

A bonus of using the digital error correction is that offset from the opamp itself no longer creates a differential non-linearity in the transfer characteristic of each stage of the pipeline ADC. An offshoot of this fact is that the offset of each opamp can be modeled as a shift in the residue plot of the pipeline stage corresponding to a simple offset. This implies that the opamp offset can then be conveniently referred to the input of the converter as a single global offset.

### 4.3.1 Offset Compensation in the Pipeline Mode

#### 4.3.1.1 Conventional Offset Compensation

Conventionally, an auto-zero scheme is employed to remove the offset of the opamp. The implementation of this scheme requires the opamp to be active in that pipeline stage during both phases. Here 'stage' refers to a single sample-and-hold and multiply-by-2 section. For constructing this auto-zero scheme, the opamp is placed in unity gain feedback to pre-sample the offset of the opamp in one of the phases and is placed in a multiply-by-2 configuration in the next. Another popular method for opamp offset correction in pipeline converters is through the use of an auxiliary amplifier that provides an offset nulling signal to the amplifier. Both the auto-zero mechanism and auxiliary amplifier method require additional power and complexity.

As mentioned earlier, the use of the 1.5bit/stage digital error correction allows the offsets of the amplifiers to be referred back to the primary input of the converter as a single global offset. To cancel this global converter offset, a global converter chopping mechanism is proposed.

#### 4.3.1.2 Proposed Global ADC Chopping

The proposed global converter-chopping scheme entails multiplying the input of the converter by a string of alternating 1s and -1s as shown in Figure 4-3. This process modulates the converter input to a higher frequency away from the DC offset and  $1/f$  noise of the converter. In specific, a string of alternating 1s and -1s will modulate a DC input to a frequency  $F_s/2$  or half the sampling frequency. The output, which consists of the signal at  $F_s/2$  and the  $1/f$  noise and offset at DC, is multiplied by an identical string to modulate the input signal back to the base-band. The offset and  $1/f$  noise are consequently displaced to  $F_s/2$  and subsequently removed by low-pass digital filtering.

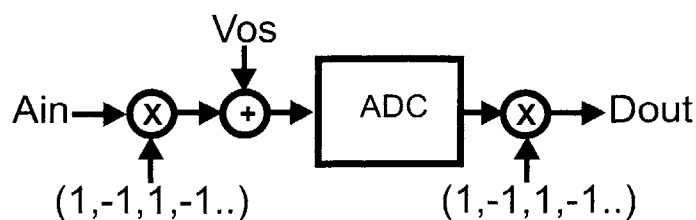


Figure 4-3: Illustration of Global Chopping of ADC

In terms of implementation, the input chopping is achieved simply by swapping the positive and negative inputs every clock cycle. The output chopping is achieved by inverting the sign of the digital output every other clock cycle. Global chopping of the analog-to-digital converter eliminates errors with even symmetry in the ADC transfer characteristic while leaving errors with odd symmetry undisturbed. More explanation can be found in [22] ADC chopping has been experimentally verified to eliminate the DC offset.

#### 4.3.1.3 Advantages of Global ADC Offset Cancellation

The global chopping scheme frees up the opamp during the sampling phase since we no longer do opamp-offset correction at a local level. The two operations that each pipeline stage now needs do are sample-and-hold without the need for an opamp and the multiply-by-2 operation (with an opamp) that it executes in the opposite phase. Since consecutive stages of the pipeline do not both simultaneously require the opamp, a single opamp is then time-shared between the two consecutive stages. This allows us to compress two stages of the pipeline architecture into one basic building block containing a single opamp and several capacitors. The process of opamp sharing [27][28] stems from the use of global offset chopping and leads to power and some area savings. Additionally, global offset compensation is far simpler to implement than doing opamp offset correction at a local opamp level.

Another significant advantage of global offset compensation is that this scheme can not only address offset due to the opamps but also other sources such as charge injection from switches in the switched capacitor circuit.

It may be argued that the process of chopping impacts the maximum bandwidth relative to the sampling frequency that can be handled by the converter. In other words the maximum bandwidth that can be digitized by the converter will be less than  $F_s/2$  by the knee of the  $1/f$  noise. The knee of the  $1/f$  noise is defined as the frequency at which the  $1/f$  noise equals the thermal noise floor. This will cause the converter to be no longer in a "Nyquist-rate" condition. However, in most cases the  $1/f$  noise knee, typically in the low kilohertz range, is relatively small compared to the sampling frequency.

#### 4.3.2 Opamp Scaling in the Pipeline Mode

Since successive stages of the pipeline architecture contribute less noise to the overall digital output signal, successive stages can employ capacitors that are scaled with respect to capacitors in the stages before it. For the same stage bandwidth across all the stages, this allows us to scale down the opamp size and power consumption of successive stages, leading to power savings. However, since the performance of the last few stages become dominated by the parasitic capacitance of interconnects, it is not beneficial to continue to scale the capacitors in these last few stages. Theoretical MATLAB analysis shows that the optimal inter-stage scale depends on various process related and design factors and is approximately in the range of 0.4 to 0.6. Most importantly, however, it is found that this optimal scale factor is quite broad. This is illustrated in Figure 4-4 that plots total power versus inter-stage scale factor. This plot has been



created with the assumption that the capacitors in all the stages in the pipeline have been scaled. The size of the transistors and the bias current through the opamps in the pipeline stages have been selected based on the capacitive loading of each of the opamps. Although the addition of parasitic capacitors alters the absolute minimum point on this curve, the minima still remains broad through roughly the same range of scale factor. The fact that the minima is broad allows us to choose a convenient factor of 0.5 as the inter-stage scale factor; since two pipeline stages are contained within one block of the reconfigurable ADC, the inter-block scaling factor is a quarter. The choice of 0.5, as we will see, paves the way for a novel parameter reconfiguration methodology when the converter is in the pipeline mode, as will be explained later.

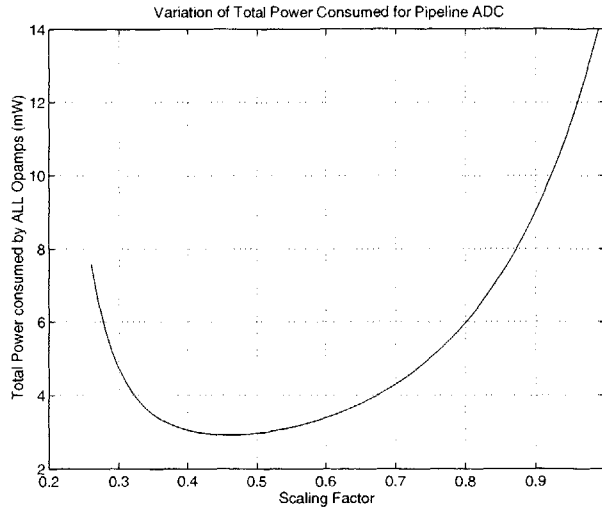


Figure 4-4: Total ADC Analog Power Consumption versus Inter-stage scale factor.

### 4.3.3 Opamp Sharing in the Pipeline Mode

As mentioned earlier, consecutive stages of the pipeline architecture share the same opamp. Since each basic building block shown in Figure 4-1 contains one opamp, each block encapsulates two stages of the pipeline architecture. While opamp sharing was not included in the creation of Figure 4-4, this feature does not alter the broad opamp scaling factor minima range of 0.4 to 0.6.

## 4.4 Delta-Sigma Mode Architecture

The delta-sigma mode of the reconfigurable ADC is based on a fourth order distributed feedback distributed feed-forward cascade-of-integrators type architecture [36] as shown in Figure 4-8. The chosen architecture does not employ resonator loops for reasons of simplicity and because, by way of design, the converter is in thermal noise limited regime for most oversampling ratios.

These four delta-sigma stages are embedded in the first four reconfigurable converter blocks. In other words each basic building block corresponds to a single delta-sigma stage.

Since increasing order of the delta-sigma converter merely implies adding more scaled operational amplifiers, it is power efficient to maximize the order of the modulator. However, high order modulators are also subject to increased instability. A 4th order modulator was selected to maximize power savings without running into stability issues.

#### 4.4.1 Offset Compensation in the Delta-Sigma Mode

The performance of the delta-sigma converter, as that of the pipeline converter is susceptible to  $1/f$  noise and offset from opamps in the converter especially the opamp in the first stage. Global ADC chopping cannot be employed with a low-pass delta-sigma converter to eliminate opamp offset and  $1/f$  noise. This is because the process of chopping the input modulates the input-band to  $F_S/2$ . Opamp offset in the delta-sigma mode is corrected by executing opamp chopping in the first block [37]. The conventional chopping circuit, however, degrades settling time as well as adds thermal noise to the modulator.

In this converter, opamp chopping is implemented in a way that does not degrade settling or add noise. The description of this technique is relegated to Section 5.5.3.2.

#### 4.4.2 Opamp Scaling in the Delta-Sigma Mode

The consecutive stages in this mode can also be scaled. Like in the pipeline converter, the noise from the successive stages of the delta-sigma modulator can be referred back to the input, however, here, the effective gain of each stage depends on the oversampling ratio. The effective stage gain increases as the oversampling ratio is increased. This implies that inter-stage scaling factor increases with the OSR.

For the analysis below, it is assumed that consecutive stages are scaled by the same factor. While, for large scale factors, this is not practical the results will not differ significantly. For determining the optimal scale factor, thermal noise contributions are considered at each stage of the 4<sup>th</sup> order modulator. As the scale factor is varied, the overall input referred noise level will change. To bring noise level back to its original position, all the noise sources are then scaled down uniformly. Thus for the analysis considered below, the SNR is kept fixed. Figure 4-5 shows the variation of total power consumption as the scale factor is varied for a specific case of OSR=256. In this case the absolute minimum point occurs at a scale factor of 141. At this scale factor the minimum power obtained is about a factor 3.5x times smaller than the modulator power for the case when the stages are not scaled. Notice, however, that the minima is very broad. It is clear from this graph that scaling close to the optimal scale factor can save significant power.

As mentioned earlier, the optimal scale factor will increase with oversampling ratio. The variation of optimal stage scaling factor with oversampling ratio is shown in Figure 4-6. It is found to increase almost linearly with OSR. To obtain an idea of how much power savings is obtained by scaling at the optimal scale factor for various OSRs, the upper curve in Figure 4-7 plots a ratio between the power when the stages are not scaled and the power when the stages are scaled at the optimal scale factor. For greater OSR, the optimal scale factor is lower and hence larger power savings is possible. Notice, however, that the power savings saturates very rapidly as OSR is increased. In this design, it is obviously not possible to vary the scale factor. In fact the scale factor was determined by the requirements from the pipeline converter and ease of reconfigurability. The inter-block scale factor, which is the same as inter-stage scale factor from the perspective of the delta-sigma mode (since each reconfigurable block corresponds to one delta-sigma stage), is fixed at 0.25. To get an idea of the power savings possible with a fixed scale factor of 0.25 and how it compares with the power savings possible when the stages are scaled at the optimal scale factor, the bottom curve in Figure 4-7 was obtained. This curve plots the power savings from a fixed scale factor of 0.25 for various OSRs. It is evident from the plot that while minimum power is achieved at the optimal scale factor, an inter-stage scale factor of 1/4 is sufficient to extract most of the power savings that occurs as a result of using scaled opamp blocks. In fact, a fixed scale factor of 0.25 saves almost 75%-85% of the power that can be saved in the best case. This observation further validates our initial decision of selecting an inter-block scale factor of 0.25.

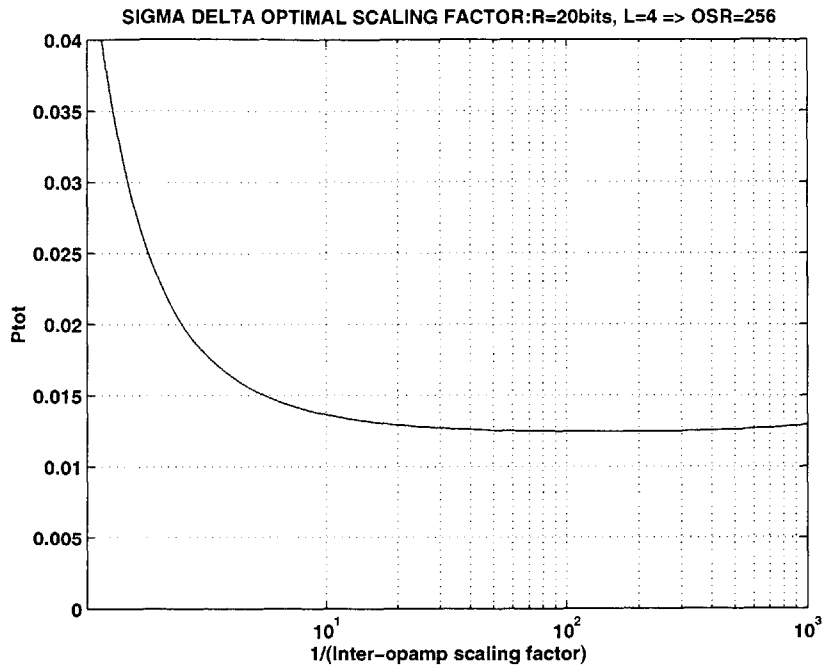


Figure 4-5: Variation of total modulator power consumption with scale factor for an oversampling ratio of 256.

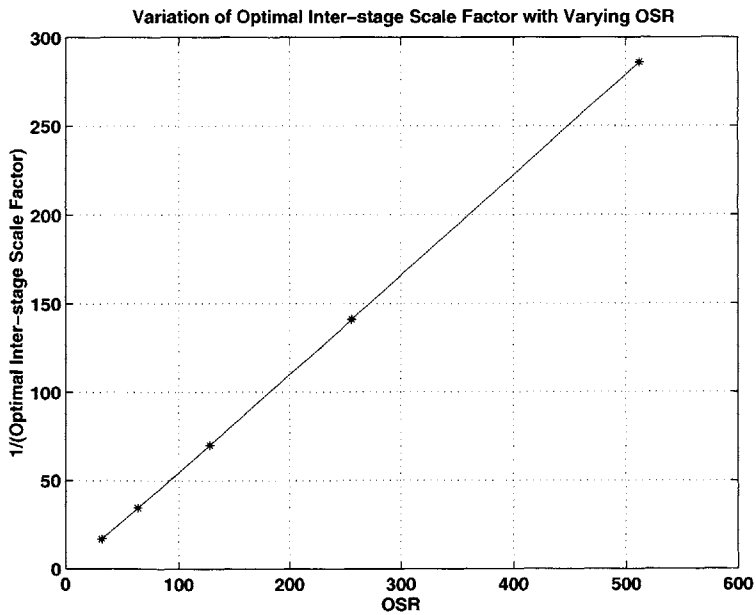


Figure 4-6: Variation of optimal stage scale factor with oversampling ratio.

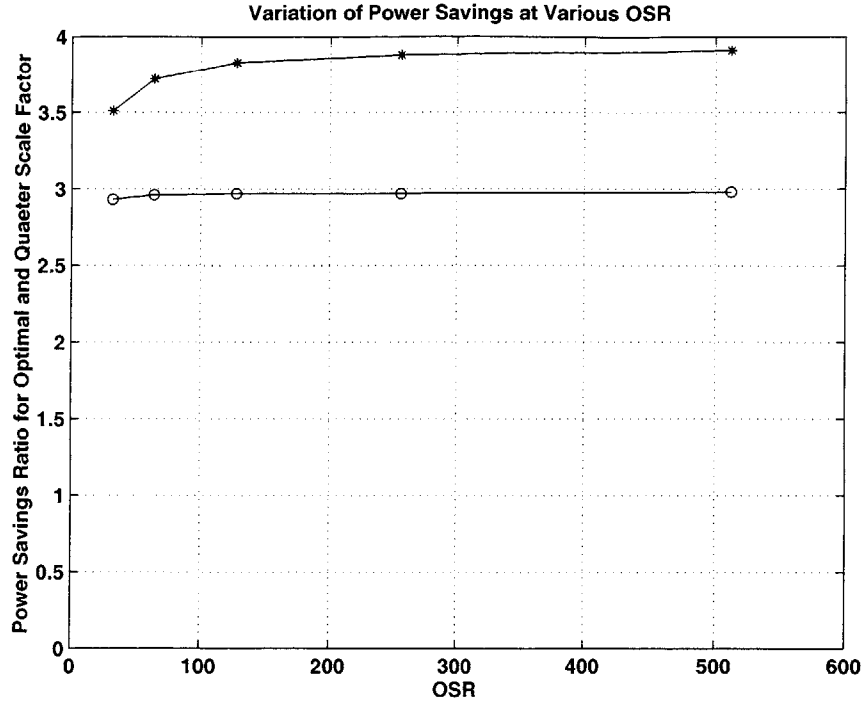


Figure 4-7: Variation of power savings due to scaling at various oversampling ratio. The curve marked by asterisk (\*) corresponds to the ratio of the modulator power without any scaling applied to the minimum power that can be obtained when the stages are scaled by the optimal scale factor (from Figure 4-6). The curve marked by circles (o) corresponds to the ratio of the modulator power without any scaling applied to the power obtained when the stages are scaled by a fixed scaling factor of 0.25, as in this design.

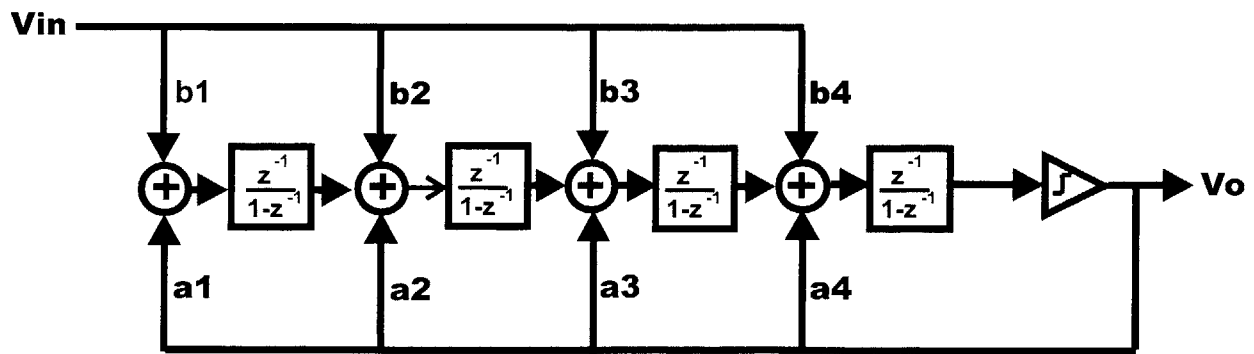


Figure 4-8: Architecture of converter in delta-sigma mode

Each block of the reconfigurable ADC corresponds to one stage of the modulator; the 4 blocks are fashioned out of the first 4 blocks of the reconfigurable ADC. In this mode, each basic building block is configured to a multiple input integrator.

## 4.5 Parameter Reconfiguration

In addition to architecture reconfiguration, various parameters of the converter in each of the modes can be modified for tuning the signal-to-noise ratio. In the pipeline converter mode, both the length of the pipeline as well as the thermal noise contributing capacitors can be modified. In the delta-sigma converter mode, the oversampling ratio can be modified to change the overall resolution of the converter.

### 4.5.1 Parameter Reconfiguration in the Pipeline Mode

With the inter-block scale factor of 1/4th employed in the reconfigurable converter, the RMS thermal noise voltage from the second block in the reconfigurable converter B2, as shown in Figure 4-1, is twice as high as that from the first block B1. This leads us to the resolution reconfiguring methodology in the pipeline ADC as illustrated in Figure 4-9. The top-most row in this figure shows the cascade of blocks, the size of each of these blocks is roughly representative of the power consumption in the block, although the figure is not to scale. A 12-bit mode pipeline employs blocks B1-B6. The last two blocks are deactivated. Any block that is not active does not consume any power. In the 11-bit mode, the first block B1 is switched off and the pipeline operation begins from the second block B2. Since Block B2 has capacitors that are 1/4th the size of the capacitors in block B1, the voltage noise level of the 11-bit configuration is twice that of the noise in the 12-bit configuration. This is commensurate with the 1 bit desired resolution reduction. Likewise, for the 10-bit mode, B2 is also switched off and B3 becomes the first active block. Simultaneously, because of the lesser number of digital bits that are required in this mode, the number of active blocks is also reduced. Thus a combination of shifting and truncating maintains kT/C limited operation and hence minimum power through varying resolution.

The configuration of the converter for the other resolutions is shown in Table 1. Figure 4-10 shows the designed power consumption variation as resolution is reduced. Clearly power consumption tracks resolution, as it should, however, while the ADC power consumption reduces exponentially at the beginning, and becomes linear with resolution very quickly. This occurs because the latter blocks of the converter, dominated by the parasitic capacitances due to interconnect loading, are not scaled as aggressively as the first few blocks. This is more so because of the fact that the capacitors in this converter were sized down to the fundamental thermal limit with the goal of minimizing the overall power consumption. This means that the stages reach the parasitic capacitance limitation sooner.

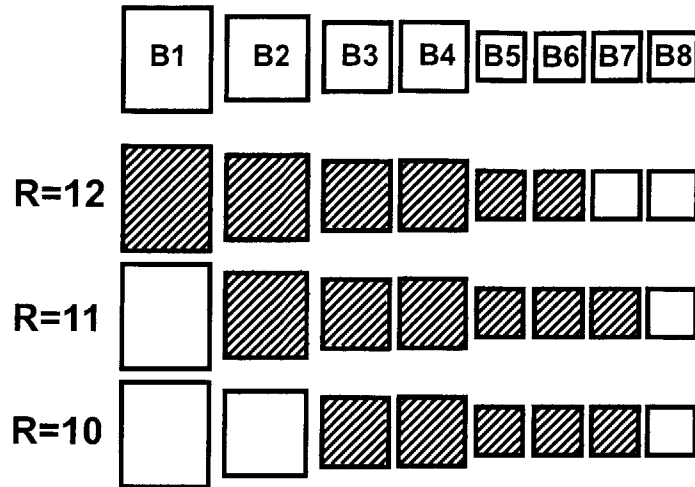


Figure 4-9: Resolution Variation in Pipeline Mode

Table 1: Reconfiguration Methodology of ADC in pipeline mode.

Resolution (bits)	Block enabled
12	B1-B6
11	B2-B7
10	B3-B7
9	B4-B8
8	B5-B8
7	B5-B8
6	B6-B8
5	B6-B8
4	B7-B8

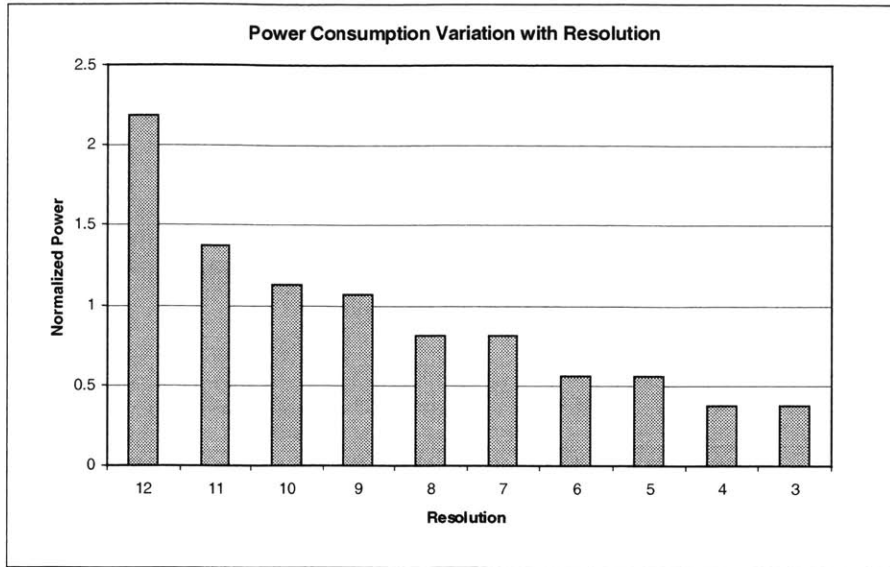


Figure 4-10: Power Consumption Variation with changing resolution in the Pipeline Mode

#### 4.5.2 Parameter Reconfiguration in the Delta-Sigma Mode

In the delta-sigma mode, resolution can be varied by variety of ways. Three possible methods for accomplishing this task are by varying the modulator order, by changing the coefficients of the modulator and by tuning the oversampling ratio (OSR). Since the modulator contains stages that are progressively scaled, adding order is cheap. Hence, as also explained earlier, the modulator with the highest stable order is most power efficient. An order of four was selected to maximize the figure-of-merit of the converter without making the modulator complex from a stability viewpoint. The thermal noise contributing capacitors in delta-sigma mode are reused from the pipeline mode. For this reason, the delta-sigma mode is in thermal noise dominated regime for most oversampling ratios. For this reason changing order to change the quantization noise will not impact signal-to-noise ratio significantly. This is another reason for keeping the modulator order fixed.

Changing coefficients (when resonator loops are employed) will allow us to move the noise shaping zeros away from DC and allow us to change the noise shaping transfer function. The benefit of this technique is very dependent on the oversampling ratio of the modulator. Again since the delta-sigma mode is in thermal noise dominated regime for most oversampling ratios, changing coefficients has little impact. Additionally, implementing variable coefficients is very complicated.

By far the simplest and most effective way of changing SNR is by varying the OSR. Varying the oversampling ratio of the ADC varies the resolution in the following manner when the modulator is quantization noise limited [31].

$$SNR \propto \frac{\sqrt{2L+1}}{\pi^L} \cdot OSR^{(L+0.5)} \quad (4.1)$$

where  $L$  is the order of the modulator,  $OSR$  is the oversampling ratio and  $SNR$  is the voltage-domain peak signal-to-noise ratio. This corresponds to a 27dB change in SNR as  $OSR$  is varied by a factor of 2.

On the other hand, when the converter is thermal noise limited, the voltage-domain SNR depends on OSR as follows:

$$SNR \propto \sqrt{OSR} \quad (4.2)$$

In this case, the SNR changes by 3dB for every factor of 2 change in OSR.

Based on the design of the converter, the oversampling ratios required at various resolutions, considering both thermal and quantization noise, are detailed in Table 2.

Table 2: Variation of Delta-sigma Mode Resolution with OSR.

Resolution (bits)	OSR	Expected Maximum Bandwidth (assuming $F_s=20\text{MHz}$ )
13	32	640KHz
14	64	160KHz
15	256	40KHz
16	1024	10KHz
17	4096	2.5KHz
18	16384	625Hz

For minimizing power consumption, variation of the sampling frequency either for the purposes of changing oversampling ratio at a fixed input bandwidth as well as for changing the overall system bandwidth in either of the modes demands a method by which the power consumption of the converter can track the sampling rate.

## 4.6 Summary

The top-level architectural and block level details have been presented. Architecture reconfiguration of this converter is accomplished by placing it in either the pipeline or the delta-sigma modes. The top-level issues related to both of these modes are described next. Some issues discussed are choice of architecture, offset compensation, opamp scaling, and opamp sharing. Finally, the methodology for parameter reconfiguration for tuning the converter signal-to-noise ratio in both of these modes is described.



# 5 ADC Circuit Implementation

## 5.1 Introduction

This chapter discusses the major circuit components employed in the converter pertinent to the architecture and parameter reconfiguration of the converter. The chapter begins with a high level description of the converter and interaction of the major circuit blocks of the converter. Following that, four major circuit blocks have been described: the main reconfiguration logic, the clock generator module, the converter core and the output interface circuit. Issues related to testing and substrate noise minimization have also been considered in this chapter.

## 5.2 Interaction of primary blocks

The overall block diagram shown in Figure 5-1 (reproduced here from chapter 4 for convenience) shows the major circuit and their relationship to each other. There are a total of 8 basic building blocks. The main reconfiguring logic accepts a 5-bit user defined configuration word and creates 3 control words each 8-bits of length determining which of the 8 blocks are active, and identifying the first and last active block. This information is also sent to the interface logic that needs this information to appropriately process the data from the blocks, and to the bias-current array included in the phase-locked loop module to activate and deactivate the currents flowing to the opamps in the various basic-building blocks. The clock generator module generates two primary non-overlapping clock-phases, and 2 delayed versions of each of these primary phases. The reason for synthesizing 3 versions for each of the 2 phases is to incorporate charge-injection reduction techniques in the switched-capacitor core in both the pipeline and delta-sigma modes. This will become clearer in the section describing the switched-capacitor core. These 6 clocks and their complements are then routed to the logic in each of the basic building blocks. It also routes 2 of these clock signals to the interface logic to synchronize it to the data output from the building blocks. The PLL uses the clock frequency to generate 16 bias currents, 2 for each opamp in the cascade of building blocks.

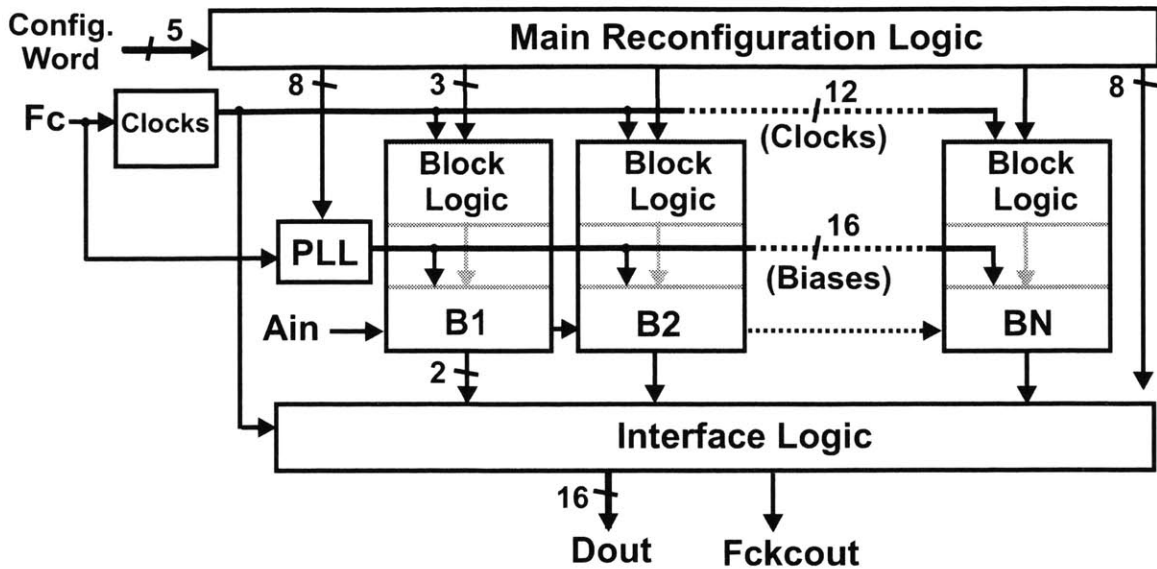


Figure 5-1: ADC architecture.

### 5.3 Main Reconfiguring Logic

A conceptual illustration of the main reconfiguration logic module is shown in Figure 5-2. A 5-bit configuration word is utilized for synthesizing a set of three 8-bit words, an enable word ENB1-ENB8 that defines all the active blocks, a first-block indicator that determines the first active block in the cascade of blocks, and a last-block indicator that determines the last active block in the cascade of blocks. A map showing all the active blocks for each resolution is shown in Table 3. M4-M0 represent the input configuration word, 'p' defines whether or not the converter is in the pipeline mode, and B1-B8 represents the various basic building blocks. A logical 1 corresponding to a block implies an active block, while a logical 0 represents a deactivated block.

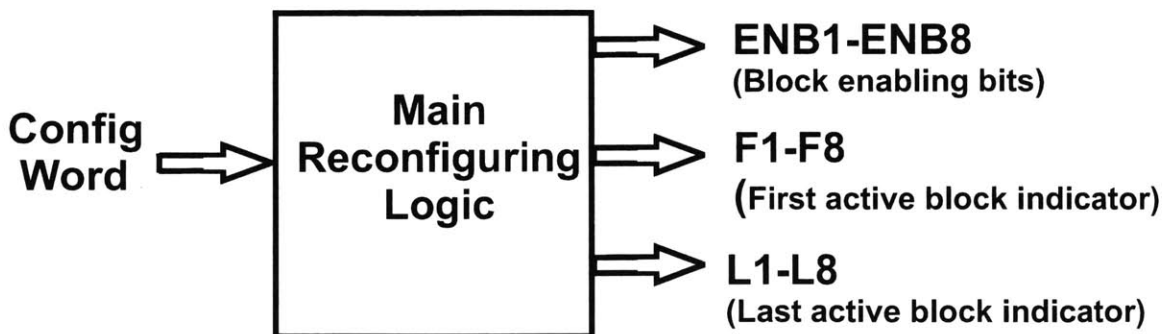


Figure 5-2: Conceptual diagram of the main reconfiguring logic.

Resolution	M4	M3	M2	M1	M0	p	B1	B2	B3	B4	B5	B6	B7	B8
5	0	0	1	0	0	1	0	0	0	0	0	1	1	1
6	0	0	1	0	1	1	0	0	0	0	0	1	1	1
7	0	0	1	1	0	1	0	0	0	0	1	1	1	1
8	0	0	1	1	1	1	0	0	0	0	1	1	1	1
9	0	1	0	0	0	1	0	0	0	1	1	1	1	1
10	0	1	0	0	1	1	0	0	1	1	1	1	1	0
11	0	1	0	1	0	1	0	1	1	1	1	1	1	0
12	0	1	0	1	1	1	1	1	1	1	1	1	0	0
13	0	1	1	0	0	0	1	1	1	1	0	0	0	0
14	0	1	1	0	1	0	1	1	1	1	0	0	0	0
15	0	1	1	1	0	0	1	1	1	1	0	0	0	0
16	0	1	1	1	1	0	1	1	1	1	0	0	0	0
17	1	0	0	0	0	0	1	1	1	1	0	0	0	0
18	1	0	0	0	1	0	1	1	1	1	0	0	0	0

Table 3: Reconfiguring map between resolution and architecture configuration.

## 5.4 Clock Generator

The clock generation module is run at a nominal voltage level of 4.6V in order to emulate clock boosting. This module is probably the single biggest noise producer on the chip. Hence extensive care was taken during layout. The clock generation takes place in 3 steps: generation of a pair of non-overlapping clocks, synthesis of a set of 3 delayed versions of the two phases, and driving these 6 clocks and their complements using clock buffering.

The clocks employed in the system, as well as the delays used are shown in Figure 5-3. ck1 and ck2 denote the primary clock phases, while derivatives of these primary phases are referred to as ck10, ck11, ck12, ck20, ck21 and ck22, as shown in the figure.

In order to enhance testability, and troubleshooting, some means of tuning the delays is required. Typically, analog methods are employed to achieve this task [29]. Typical analog methods, however, make it very difficult to know the actual internal delays corresponding to the tuning voltage. To be able to have greater control over the tuning process, digital tuning was employed.

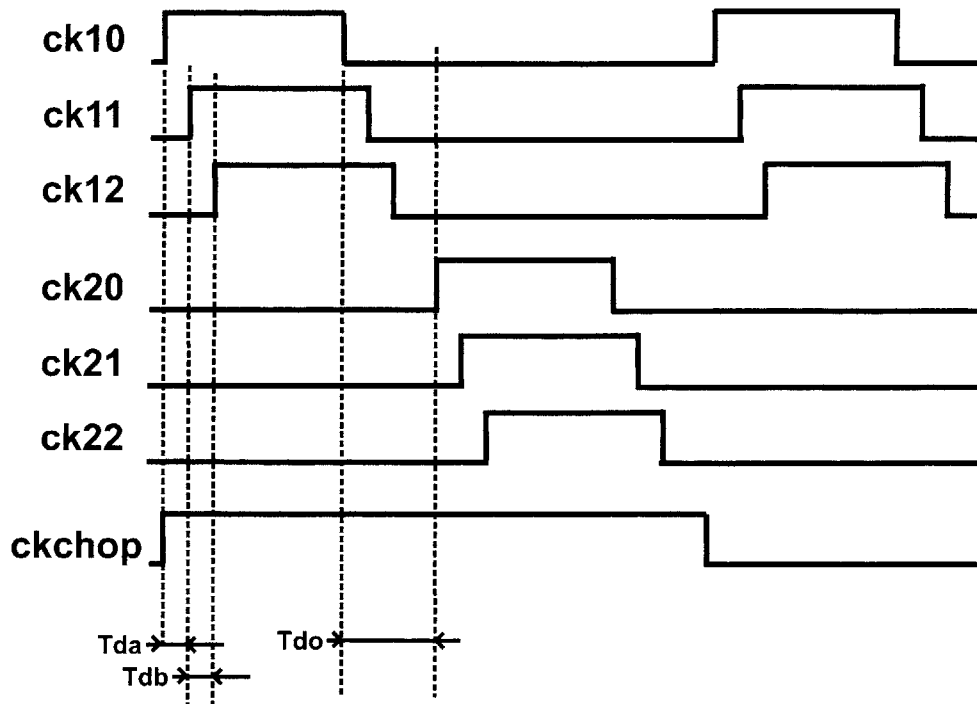


Figure 5-3: Clock timing employed for converter.

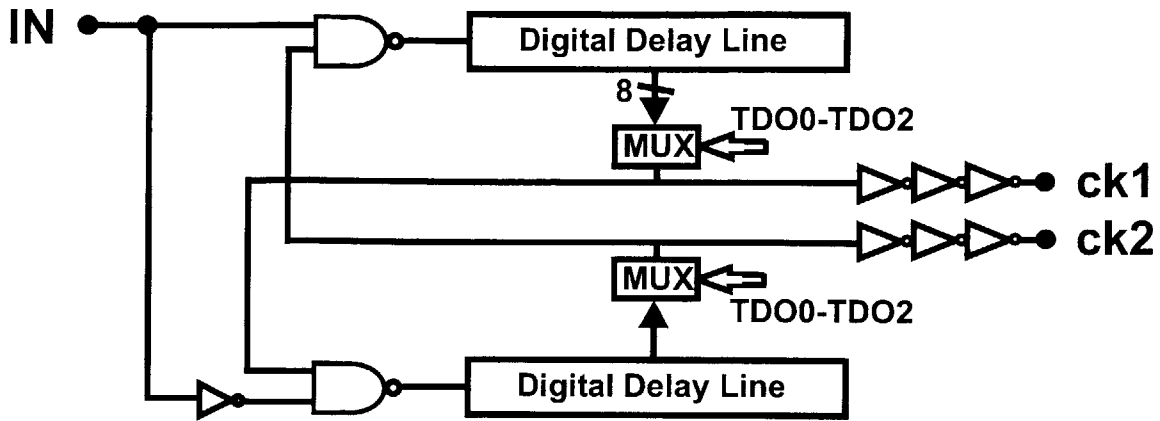


Figure 5-4: Non-overlapping two-phase clock generator.

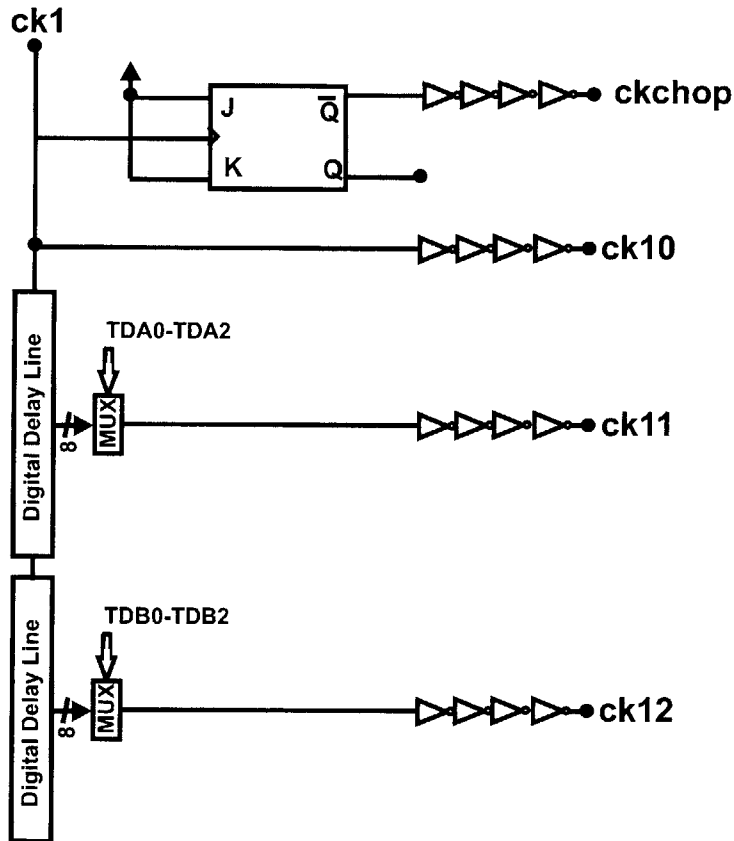


Figure 5-5: Simplified phase generator module.

### 5.4.1 Non-overlapping two phase Clock generator

A standard non-overlapping two-phase clock generator is employed as shown in Figure 5-4. The non-overlapping period  $T_{do}$  can be digitally tuned using a set of 3 bits TDO0, TDO1 and TDO2. The delay lines were constructed using inverting buffers. Eight different points were tapped from the delay line into

an analog multiplexer that selects from one of these points based on the 3 control bits. This signal is then fed back to one of the inputs of the NAND gates.

### 5.4.2 Digitally Tunable Multi-phase Clock generator

This circuit is responsible for creating the 3 delayed versions of each of the two phases, as well as the chopping clock as shown in Figure 5-5. All delays are digitally tunable with digital words shown in the figure. Each of the two delays  $T_{da}$  and  $T_{db}$  can be tuned with a set of 3 digital bits. The delays can be changed in steps of approximately 0.5ns.

### 5.4.3 Clock Buffers

The large size of the chip demands extensive buffering of the clocks before it can be driven to the various parts of the chip. As a rule of thumb, the inter-buffer ratio of a factor 4x is typically employed. This was the buffering ratio employed in most buffering operations on this chip. Several levels of buffering were needed to optimally drive the load capacitance. In order to sharpen the clock edges, it is usually a good idea to regenerate the clock signals close to the destination, in this case the basic-building blocks. The local block reconfiguring logic described earlier and used to condition the clocks in the block serves a dual purpose of serving as a local clock regenerator.

## 5.5 Converter Core

The converter core consists of 8 separate basic-building blocks, each consisting of block reconfiguring logic, an opamp, a switched matrix core, a decision block, and output-conditioning block. Each of these modules is described in this section

### 5.5.1 General Description of the Converter Core

Figure 5-6 illustrates the block level diagram of the converter core. It shows the relationship between the various core blocks as well as the signals going to and from these blocks.

The primary converter analog input is fed to a set of chopping switches in the global chopping module as shown in the figure. These switches are meant for global chopping of the converter in the pipeline mode. The output of the global chopping switch module is fed to the analog core of blocks B1-B8. At any given resolution configuration in the pipeline mode, the first active block uses the output from the global chopping module to serve as its input. All other active blocks derive their input from the residue from the previous block. In the delta-sigma mode, blocks B1-B4 simultaneously derive their input from the output of the global chopping module, while blocks B2-B4 also accept the output from the blocks prior to them. During this mode, however, the global chopping module is deactivated.

Each of the block logics accepts a set of clock phases from the clock generator module and generates, on the basis of control bits from the main reconfiguring logic, a set of conditional clocks for the switches in the switched-capacitor analog core as well as the decision block (not shown), and the output conditioning block (not shown).

The first block also contains logic for generating its internal chopping clocks for implementing opamp chopping in the first block used only during the delta-sigma mode.

Each block generates 2 bits of output in the pipeline mode that is sent to the output interface (not shown). Block B4 also generates a quantizer output in the delta-sigma mode that is sent to blocks B1-B3 as well as sent outside of the chip through the output interface.

In the delta-sigma mode, the feedback capacitors may need an occasional reset operation during ties when the modulator becomes unstable. This is achieved using a delta-sigma reset module that sends its reset signal to blocks B1-B4.

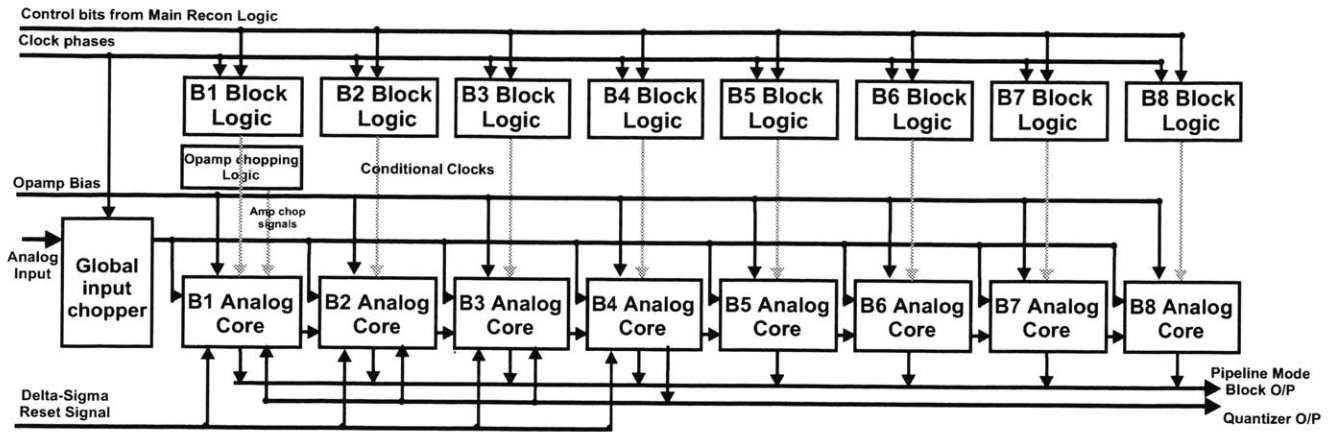


Figure 5-6: Block diagram of converter core.

## 5.5.2 Operational Amplifier Topology

Each of the first 5 converter blocks employs a conventional n-channel input device telescopic opamp with folded-cascode gain enhancement amplifiers, as shown in Figure 5-7. The last 3 blocks employ the same telescopic structure without the gain enhancement amplifiers.

### 5.5.2.1 Basic architecture

The telescopic architecture was used as the basic structure owing to the high figure-of-merit of this structure, i.e. the high speed and low power achievable from this topology as opposed to 2-stage or folded-cascode architectures. A standard switched-capacitor circuit is employed for the common-mode feedback with its feedback node at the gate of the p-load transistors. While all opamps use the same basic telescopic structure, different opamps have been scaled in order to save power.

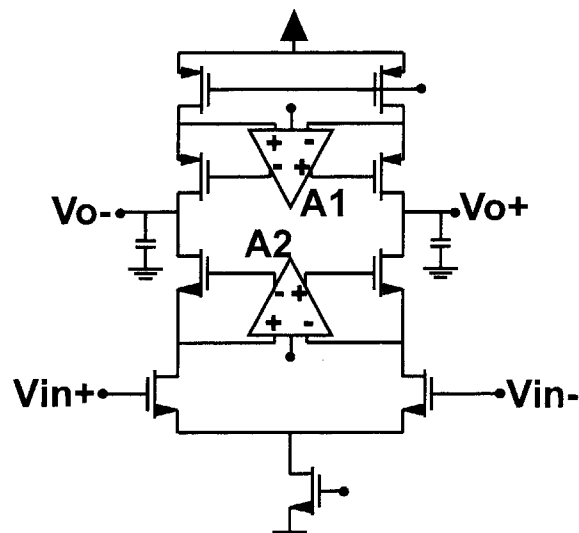
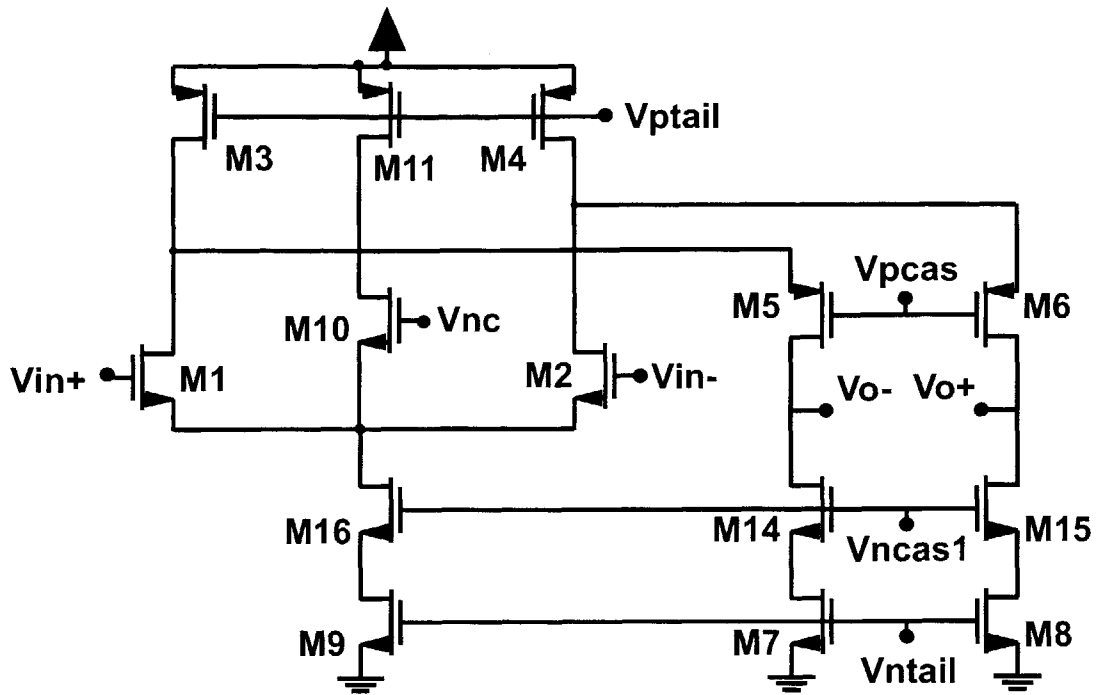


Figure 5-7: Opamp used in blocks B1-B5. The opamps in blocks B6-B8 are topologically identical without the gain enhancement amplifiers.

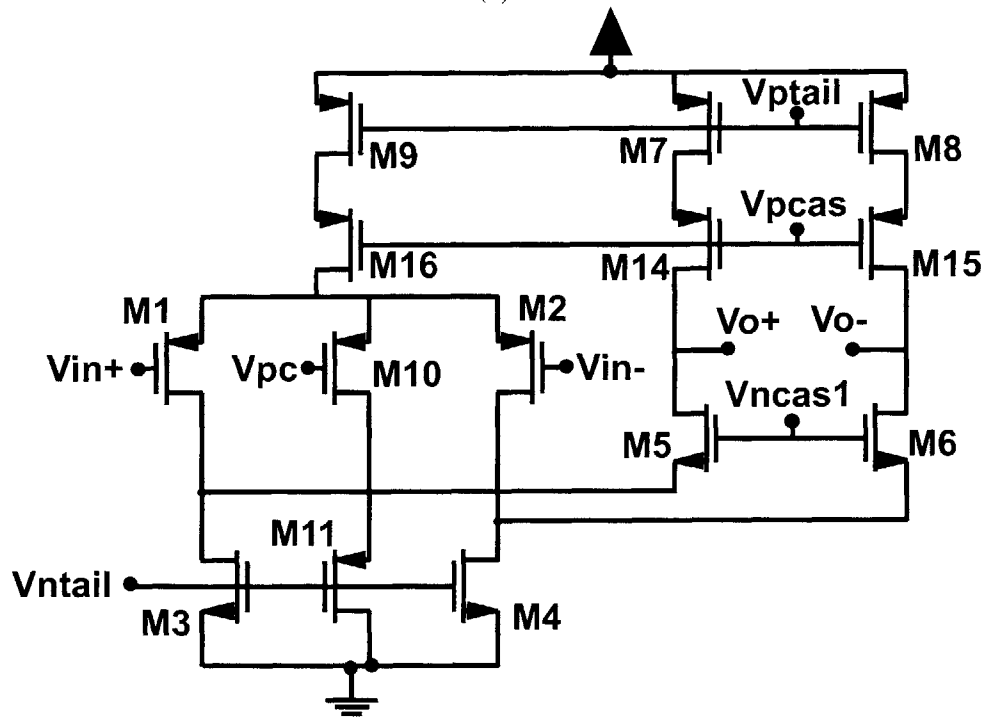
### 5.5.2.2 Gain enhancement amplifier architecture

The gain enhancement amplifiers [48] use a standard folded-cascode architecture; the choice of architecture was determined by requirements of speed and desired input/output voltage levels. These are shown in Figure 5-8a-b. Since the gain enhancement amplifiers drive much smaller capacitive loads than the main amplifier, it is possible to scale down these circuits with respect to the main amplifier. Here scaling entails reducing the device widths and current through the transistors. Such scaling will not change the voltage levels at various nodes in the circuit. This process allows us to minimize power consumption and area associated with the gain enhancement. After scaling, the power consumed by both gain-enhancement amplifiers combined is about a third of the total power consumption of the opamp. Again, the gain-enhancement amplifiers are identical along the various blocks except for the scaling.





(a)



(b)

Figure 5-8: (a) n-gain enhancement amplifier. (b) p-gain enhancement amplifier.

### 5.5.2.3 Bias Circuits

The bias circuit employs the well-known high swing current-mirror [11]. As much as possible, the bias circuits for the main topology and the gain-enhancement amplifiers are shared. Figure 5-9 shows the bias circuit for the opamp in the first block.

All the important details of the bias circuit are shown in the figure and are self-explanatory. To implement transistors N0 and N1 with an effectively smaller width, transistors were placed in series.

The bias circuit for blocks B1 and B2 were topologically identical while blocks B3-B5 have additional current legs to generate bias voltages for the gain enhancement amplifiers.

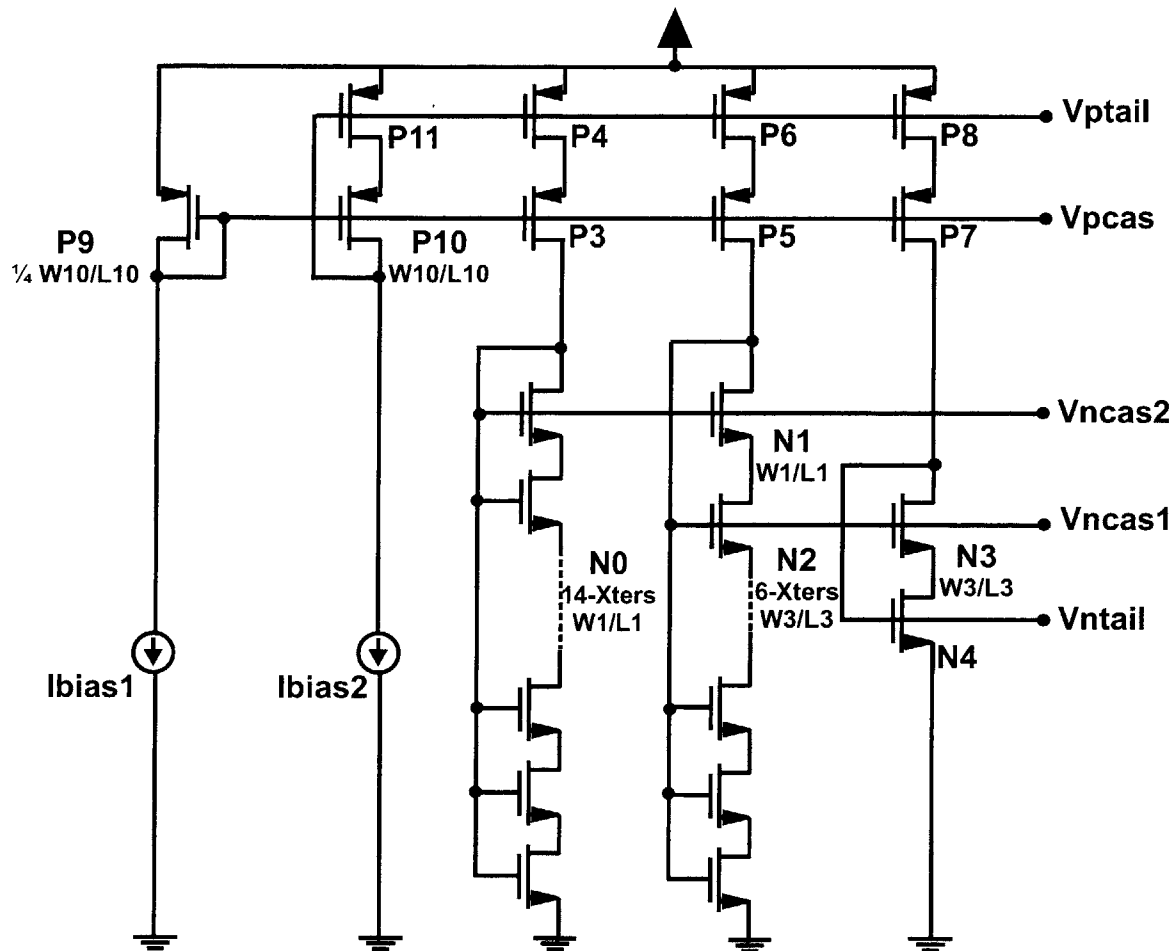


Figure 5-9: Typical bias circuit employed for the amplifiers.

### 5.5.2.4 Dynamic Biasing of the opamps

As mentioned before, the bandwidth reconfiguration of the opamps serves as one level of ADC reconfiguration. This section details the various effects of reducing current in the opamp.

At the highest current level the opamp is designed to handle, the input devices in the opamp as well as the transistors that correspond to them in the bias circuit are in the strong inversion regime. As the current is

reduced, since the gate size of these transistors is not varied, the transistors gradually go from the strong inversion regime into the sub-threshold regime. The bias circuit has been designed in order to keep the transistors in saturation in each of these regimes of operation. In order to illustrate how that is ensured, consider transistor N3 and N4 in Figure 5-9 and their counterparts in Figure 5-7 (the input and the tail transistors, respectively). In the strong inversion regime, transistor N2, that consists of a series section of 6 transistors, produces  $V_{NCAS} = V_{TN2} + 2\Delta V + V_{MAR}$ , where  $V_{TN2}$  is the threshold voltage of transistor N2,  $\Delta V$  corresponds to  $V_{GS} - V_T$  of a MOSFET, and  $V_{MAR}$  serves as a margin voltage that is created by making the effective size of N2 *less* than 1/4th the size of N4 (in this case by placing 6 transistors instead of 4 transistors in series). This ensures that the drain of the tail transistor in the telescope has a voltage equal to  $V_{NCAS} - V_{TIN} - \Delta V$ , where  $V_{TIN}$  is the threshold voltage of the input device in the telescope amplifier. This equals  $V_{TN2} - V_{TIN} - \Delta V + V_{MAR}$ . If  $V_{TN2} = V_{TIN}$ , then the voltage at the drain of the tail transistor has adequate voltage in addition to some engineering tolerance to keep it in saturation in the strong inversion regime. The reason for placing transistors in series to reduce its effective size as opposed to making a transistor with physically smaller width will become clear shortly.

When the current is reduced, because all transistors have the same current density, they will all move into weak inversion and sub-threshold regime at the same time. In the sub-threshold, a MOS transistor needs at least  $3kT/q$ , or about 75mV, across its drain-to-source terminals to maintain it in saturation [11]. However, both  $\Delta V$  and  $V_{MAR}$  (which is a function of  $\Delta V$ ) are voltage variables that scale down with reduced current. In fact, in weak inversion, both of these equal zero. Under these conditions, the voltage at the drain of the tail transistor in the telescope will go to zero. To prevent this from happening, the idea is to make  $V_{TN2} > V_{TIN}$ , in fact by the same amount that is required to keep the tail transistor in the telescope in saturation. This is achieved by constructing the transistor N2 as a series of transistors each equal in size to transistor N3, and by tying their body terminals to ground instead of tying them to their respective source terminals. This raises the effective threshold voltage of the overall transistor N2 relative to transistor N3, and provides for the needed difference between thresholds of transistors N2 and N3 (or the input device in the telescope). Since the threshold difference between the transistors also serves to provide voltage margin across the drain-to-source of the tail transistor when the transistors are in the strong inversion regime, the explicit  $V_{MAR}$  has been reduced correspondingly.

### 5.5.2.5 Effect of changing bias current on gain and opamp bandwidth

As the bias current through the converter opamps is varied over the desired bandwidth range of the reconfigurable converter, the characteristics of the transistors and consequently the opamps undergo several changes. It is important to ensure that the overall opamp specification continues to meet the desired performance level over the wide current range. Additionally, the action of the PLL relies on proper bandwidth matching of the VCO and the converter opamps. The current generated by the PLL needs to be at the level desired by the converter through this current range.

As mentioned earlier, as current is reduced from its maximum design value, the transistors of the opamps move from strong inversion into the sub-threshold regime. The total settling time based purely on the small-signal settling characteristics of the opamp is:

$$T_{SM} = M \cdot \tau$$

$$T_{SM} = \frac{M}{\beta} \cdot \frac{C_L}{gm} \quad (5.1)$$

where  $M$  is the number of time constants required for the opamp to settle to the desired accuracy,  $\beta$  is inverse of the noise gain (also known as the feedback factor) of the opamp in feedback,  $C_L$  is the load capacitance of the opamp and  $gm$  is the input transconductance of the amplifier.

When the input devices are in strong inversion,

$$T_{SM} = \frac{MC_L}{\beta\sqrt{2K_o}} \cdot \frac{1}{\sqrt{I}} \quad (5.2)$$

$$T_{SM} = \frac{MC_L}{\beta} \cdot \frac{1}{K_o(V_{GS} - V_T)} \quad (5.3)$$

where,  $I$  is the bias current flowing through the input device of the opamp, and  $K_o = \mu \cdot Cox \cdot \frac{W}{L}$ .

When the input devices are in sub-threshold,

$$T_{SM} = \frac{MC_L \cdot kT/q}{\beta} \cdot \frac{1}{I} \quad (5.4)$$

The slewing time in both regimes is:

$$T_{SL} = C_L \cdot V_{sw} \cdot \frac{1}{I} \quad (5.5)$$

where  $V_{sw}$  is the swing of the opamps in the converter. For any given condition, the output slews only for part of the overall settling waveform. Hence equation (5.5) is an approximation, however, for the purposes of this application, it is found that this is a fair approximation. The exact expression for  $T_{SL}$  is derived in Appendix E. The overall settling time of the opamp is the sum of  $T_{SL}$  and  $T_{SM}$  in the appropriate regimes.

Given these expressions, it is clear that the ratio of small-signal settling to the slewing time component continues to reduce as current is reduced while the input devices are in strong inversion. At the point where the transistor switches from strong inversion to sub-threshold, this ratio freezes and thereafter the small-signal settling is inversely proportional to the bias current just like the slewing time component. Henceforth, the clock frequency corresponding to the transition point will be referred to as the transition frequency.

At the transition point, that occurs approximately when  $V_{GS} - V_T = 2\frac{kT}{q}$  [10], the ratio, obtained by dividing (5.3) and (5.5) as shown below, is dependent only on the resolution of the converter, the noise-gain, and swing of the opamp.

$$\frac{T_{SM}}{T_{SL}} = \frac{M \cdot (V_{GS} - V_T)}{\beta \cdot V_{SW}} \quad (5.6)$$

For this design,  $T_{SM}/T_{SL} \cong 2.4$ . The swing of the opamps does increase as the bias current  $I$  is reduced, however, this is a second order effect and will be ignored here for simplicity.

### Matching the PLL current with the desired ADC current

This ratio needs to be considered while matching the current from the PLL and the desired converter bias point. By way of design the oscillation frequency of the VCO is dependent, for the most part, on the small-signal characteristics of the opamps. Hence the current delivered by the PLL is linearly related to the converter clock as long as the clock frequency is below the transition frequency, i.e. the clock frequency below which the input devices of the opamps move from strong inversion to sub-threshold operation. Thus if the current delivered by the PLL is matched to the desired bias current at the transition frequency, the PLL will generate the right current for all clock frequencies below the transition frequency. However as clock frequency is increased beyond the transition frequency, the PLL will gradually supply more than optimal current.

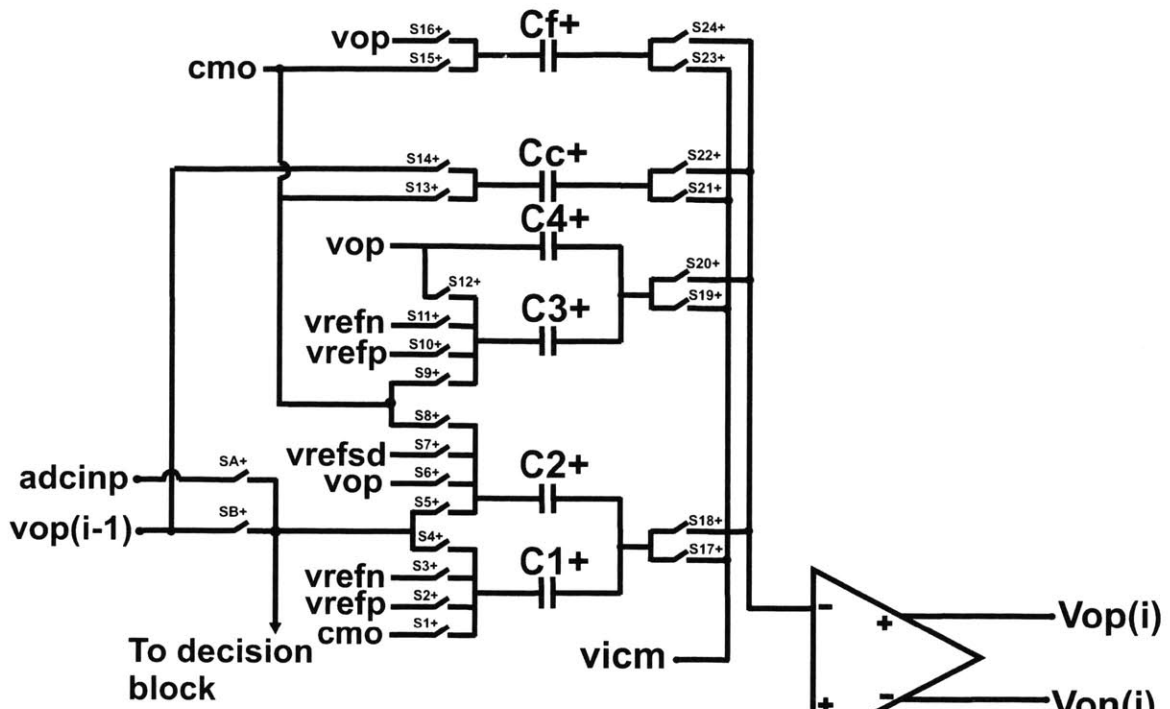
It can be shown that for clock frequencies much higher than the transition frequency, the VCO current supplies current that is double the optimal value. For practical values of clock frequency, the VCO current is close to optimal value for the most part.

## 5.5.3 Switched-Capacitor Network

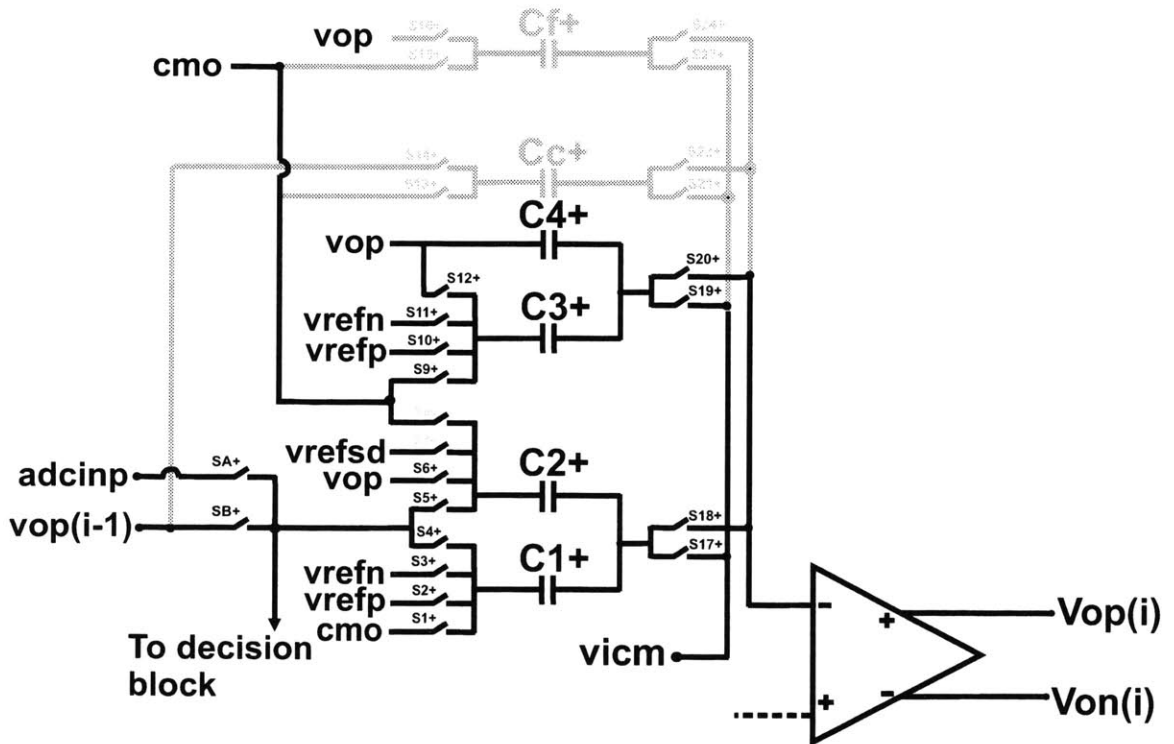
The design of the switched-capacitor circuit around the opamp is perhaps the most crucial component in determining the performance of the reconfigurable converter. This section describes the network and explains the rationale for the design. The first four blocks B1-B4 employ only NMOS switches while the last four blocks B5-B8 utilize full CMOS switches. NMOS switches yield higher performance compared to their PMOS counterparts because, for the same size, they have lower on-resistance owing to higher electron mobility. In order to maximize the signal range for the converter, the clock voltage is selected to be higher than the analog power supply voltage. This is normally achieved using standard clock boosting circuits such as that described in [30]. For simplicity, clock boosting circuitry was not included in this prototype. Higher clock voltage swing in this design was achieved by raising the power supply of the clock generator module. The nominal power supply of this converter is 3.3V, while the boosted clock is assumed to be at 4.6V. Since this circuit was implemented in a 5V process, the use of the raised clock voltage does not compromise the reliability of this chip.

### 5.5.3.1 Circuit Design of a typical Switched-capacitor half

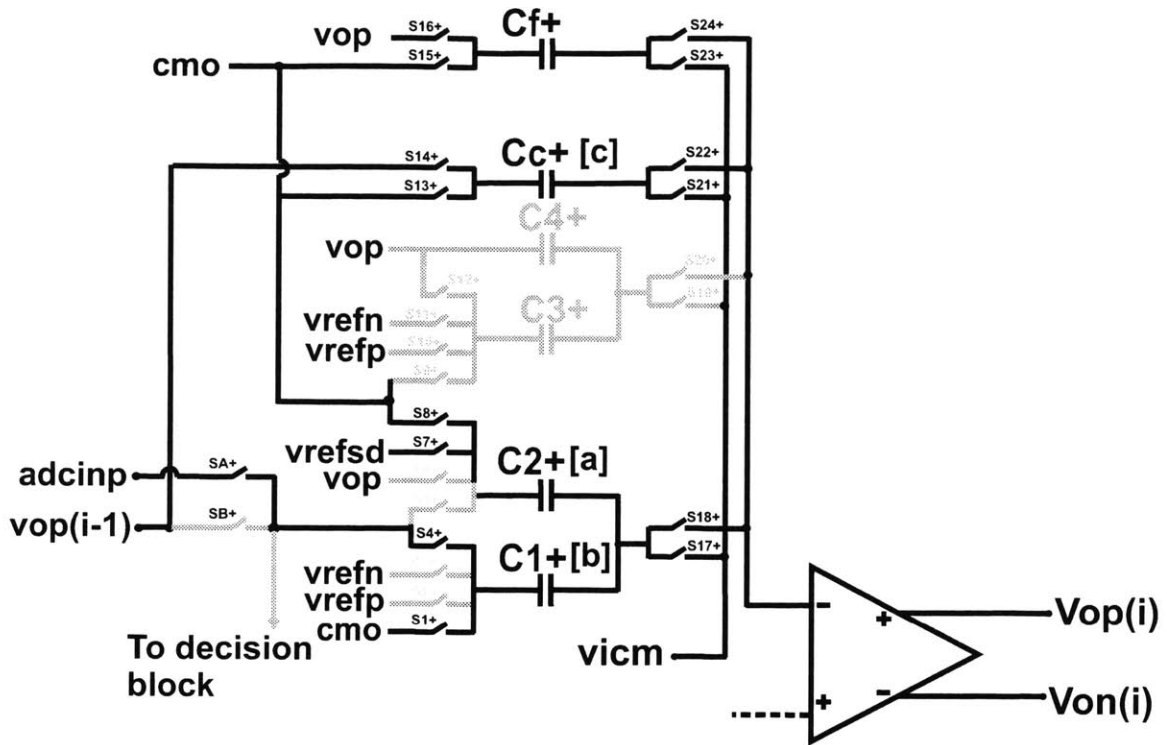
Figure 5-10a shows a typical switched-capacitor half network for a typical block in the converter. It employs 6 capacitors and several input and output switches. Figure 5-10b shows the signal paths that are active when the system is in the pipeline mode. In this mode, the capacitors  $C_f$  and  $C_c$  at the top of the figure along with their corresponding switches are deactivated. The capacitors  $C_1$  and  $C_2$  at the bottom are employed for implementing the first stage of the block in the pipeline mode, while capacitors  $C_3$  and  $C_4$  in the middle are employed in the second stage of the block in this mode. The value of  $C_1$  and  $C_2$  in the block B1 is 400fF, while capacitors  $C_3$  and  $C_4$  are sized down to 200fF in keeping with an inter-stage scale factor of 1/2. The values of all the capacitors as well as the delta-sigma coefficients in the converter are shown in Table 4.



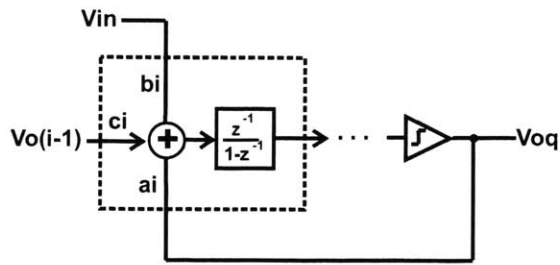
(a)



(b)



(c)



(d)

Figure 5-10: Switched-capacitor core in basic building block. (a) All switches shown. (b) switched-capacitor core in pipeline mode. (c) Switched-capacitor core in delta-sigma mode. (d) Simplified structure of block in delta-sigma mode.

	B1	B2	B3	B4	B5	B6	B7	B8
a	0.4568	0.4366	0.47	0.5588				
b	0.4568	0.4366	0.47	0.5588	1			
c		0.0781	0.1915	0.382				
C1	400	100	50	25	25	25	25	25
C2	400	100	50	25	25	25	25	25
C3	200	50	25	25	25	25	25	25
C4	200	50	25	25	25	25	25	25
Cf	875.6	229	106.38	44.7	-			
Cc	0	17.88	20.27	17.07				
Ccmfbx	100	25	12.5	12.5	12.5	12.5	12.5	12.5
Ccmfby	300	25	12.5	12.5	12.5	12.5	12.5	12.5

Table 4: Size of component values employed in the converter.

Figure 5-10c shows the switched-capacitor circuit when the converter is in delta-sigma mode. In this case, the capacitor pair in the middle comprising of C3 and C4 are switched off. Capacitors C1, C2 and Cc are used to implement the coefficients b, a and c, as shown in Figure 5-10d, respectively. Cf is wrapped around the opamp to serve as the feedback capacitor. Ccmfbx and Ccmfby, referred to in Table 4, are the common-mode feedback capacitors. While Ccmfbx is the capacitor that is explicitly placed across the opamp output and sense node, Ccmfby is the capacitor that is periodically connected in parallel to this capacitor to refresh it. The sizing of these capacitors has been done in order to equalize the load across the output of the opamps during the two phases.

Each of the switches in the network is controlled by a conditional clock phase synthesized in the block reconfigurable logic. The expression for the signals supplied to each of these is shown in Table 5, along with the definitions of some logical symbols used in the expression. As is seen in the table, these signals have several dependencies such as whether the system is pipeline or in the delta-sigma mode, whether its the first active block, the conditions of a stabilizing reset signal employed in the delta-sigma mode, as well as the conditions from the decision block. Each of the signals also depends on whether or not the block is in active state or not. This dependency has been omitted below for simplicity. An illustration of the various primary clock phases is shown in Figure 5-3.

Signal	Definition (1 when condition is true)
$p$	Pipeline mode indicator
$s$	Delta-sigma mode indicator
$f$	First active block indicator
$sreset$	Reset signal in delta-sigma mode
$q$	Quantizer output
A	$Residue(i-1) < -Vref/4$
B	$-Vref/4 < Residue(i-1) < +Vref/4$
C	$Residue(i-1) > +Vref/4$



Switch	Signal
SA	$p \cdot f + s$
SB	$p \cdot \bar{f}$
S1	$p \cdot B \cdot ck22 + s \cdot ck22$
S2	$p \cdot C \cdot ck22$
S3	$p \cdot A \cdot ck22$
S4	$ck11$
S5	$p \cdot ck11$
S6	$p \cdot ck22$
S7	$s \cdot q \cdot ck22 + s \cdot \bar{q} \cdot ck12$
S8	$s \cdot q \cdot ck12 + s \cdot \bar{q} \cdot ck22$
S9	$p \cdot B \cdot ck12$
S10	$p \cdot C \cdot ck12$
S11	$p \cdot A \cdot ck12$
S12	$p \cdot ck21$
S13	$p + ck21$
S14	$s \cdot ck11$
S15	$p + sreset$
S16	$\overline{s \cdot sreset}$
S17	$ck10$
S18	$p \cdot ck22 + s \cdot ck20$
S19	$s + ck20$
S20	$p \cdot ck12$
S21	$p + ck10$
S22	$s \cdot ck20$
S23	$p + sreset$
S24	$s$

Table 5: Signals controlling switches in the switched-capacitor network.

### 5.5.3.2 Opamp Chopping in the Delta-Sigma mode

To minimize the effect of offset and  $1/f$  noise on the performance of the converter in the delta-sigma mode, the first block opamp is chopped at half the sampling frequency. A conventional implementation of opamp chopping is depicted in Figure 5-11a. Switches are employed in series with the input and output of the opamp to chop the opamp at  $f_s/2$  frequency oblivious of the rest of the switched-capacitor circuit. These switches have a non-zero resistance and thus introduce higher order poles to the closed loop opamp system leading to greater ringing. This can slow down the overall speed of the converter. Alternatively, these switches could be sufficiently large so as to make the higher order poles not impact the order of the system. However, this, of course, would add additional parasitic capacitance thus reducing the unity-gain frequency of the system. To compensate, the opamps are made larger, at the cost of higher power consumption. Additionally these switches in series with the opamp input will contribute thermal noise

that will get boosted up by the noise gain of the closed loop system, just like thermal noise from the opamp, and thus reduce the overall signal-to-noise ratio of the converter.

In the proposed implementation [38], shown in Figure 5-11b, instead of chopping the opamp, the charge packet that is delivered to the opamp and its integrating capacitor is chopped between the positive and negative inputs of the opamp. In one clock period, the charge from  $V_{in+}$  is fed to the positive terminal of the opamp, while in the next the charge from  $V_{in+}$  is delivered to the negative terminal. In order to maintain the same transfer function, capacitor  $C_{f+}$  and  $C_{f-}$  also are interchanged every other clock period, while the next stage also samples the  $V_{o+}$  and  $V_{o-}$  alternatively every clock period. In other words the charge packets are chopped around the opamp. This operation leads to the same effect as conventional opamp chopping. From a network standpoint, this operation is tantamount to an implementation in which switches are used in parallel instead of in series. This mechanism eliminates the switches from inside the closed loop feedback around the opamp leading to faster settling time. Although these parallel switches still contribute some parasitic capacitance, an analysis shows that the total parasitic capacitance at the opamp inputs is also reduced to about 4/7ths of its original value. Note that the switches next to integrating capacitors  $C_{f+}$  and  $C_{f-}$  are needed in both cases for the purposes of resetting the system in case of modulator instability.

Removing the switch resistance in series with the opamp inputs and outputs leads to faster settling time and/or lower power compared to the conventional chopping mechanism. This scheme allows us to implement offset chopping in the delta-sigma mode without reducing the performance level of the converter in the pipeline mode. Additionally, the noise level of the proposed configuration is also lower compared to the conventional approach because there is no switch in series with the opamp input within the loop.

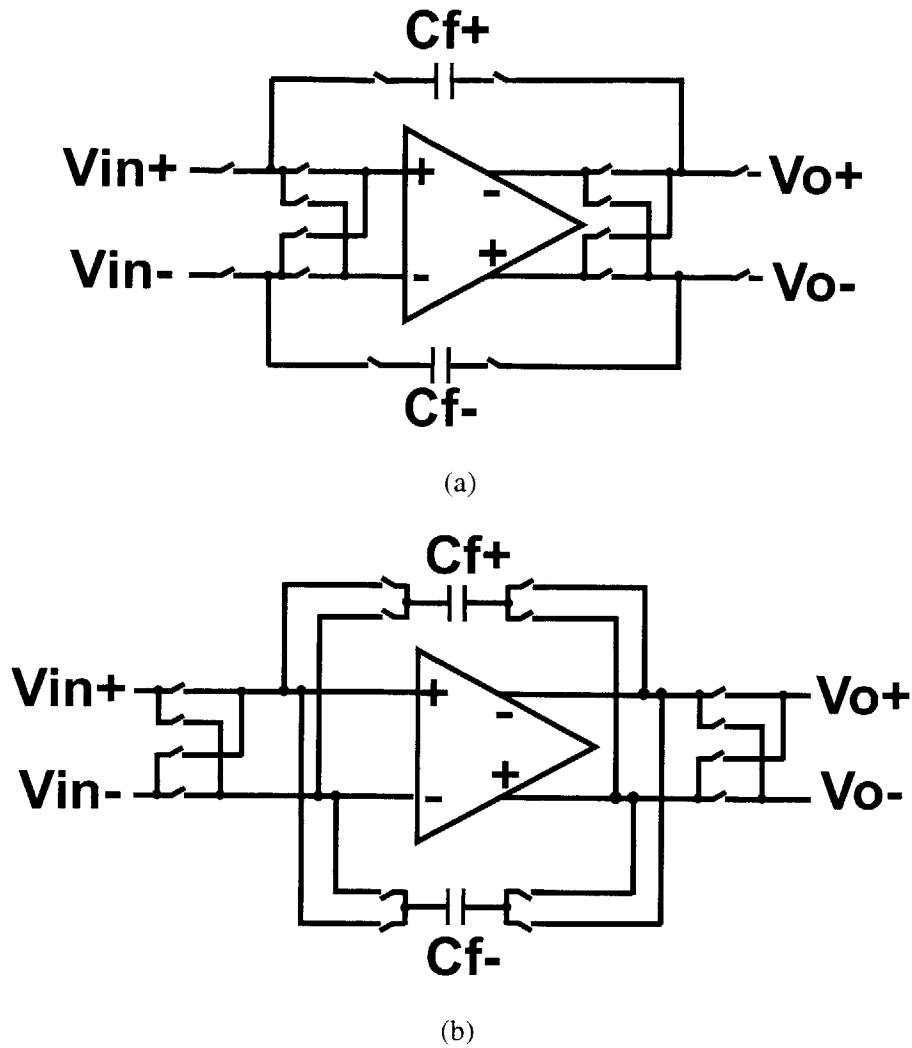


Figure 5-11: Illustration of opamp chopping to minimize opamp offset and  $1/f$  noise. (a) Conventional opamp chopping scheme. (b) Proposed opamp-chopping mechanism.

### 5.5.4 Block Reconfiguration Logic

The block reconfiguring logic is the control center of the basic-building block. It was perhaps the most complex part of the reconfigurable converter. It implements not only the signals that go to the analog switch core as shown in Table 5, but also conditional clocks and signals going to the decision block, the common-mode feedback logic and the output conditioning block.

Conceptually, a typical block reconfiguring logic is divided into 3 different sections, as shown in the figure. The static condition generation module synthesizes the static control bits that are used for either controlling the various sub-blocks inside the basic-building block or for the purpose of conditioning the clocks that are received by the basic-building block. These bits are static hence the logic gates for this module are of minimum size.

The clock conditioning logic receives the clocks from the clock-generator elsewhere in the converter and, based on control bits it gets from the static conditioning module, it parses or conditionalizes the clocks that are then sent forward to the switches and logic in the rest of the basic-building block. It is necessary to design this module very carefully since it determines the speed of transitions of the clocks or the slope of the edges of the clocks. In consideration of this observation, the load considerations for the logic need to be taken into account.

In many cases, the capacitive loading is dependent on the size of the switches in the basic building block, which in turn is dependent on which basic building block it is located in. As has been mentioned earlier, the opamps and capacitors are scaled as we go down the basic building blocks; consequently switches in series with some of the capacitors in the analog core are also scaled. Hence this part of the conditioning module is also scaled with the stages, and is referred to as the 'scaled clock conditioning module'. The other part, referred to as the 'unscaled clock conditioning module' remains unchanged through the various basic building blocks since its loading condition remains unchanged.

There are additional details in the construction of this logic that have been omitted for simplicity.

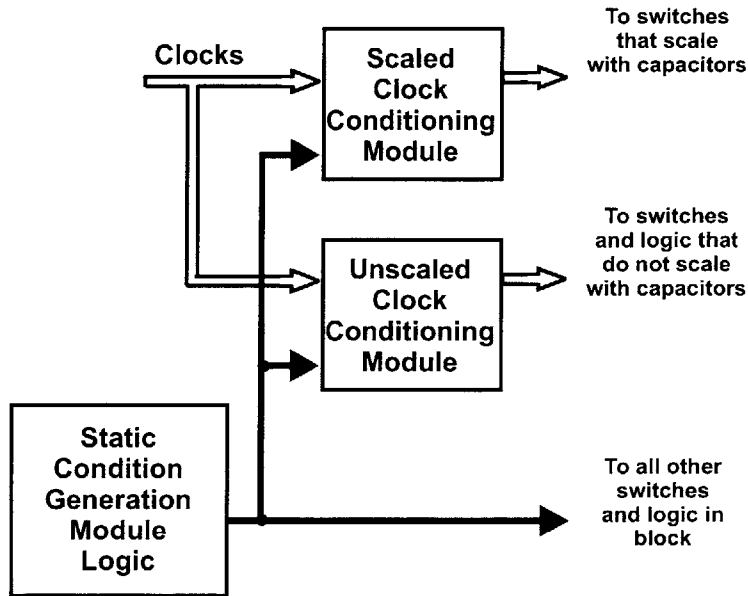


Figure 5-12: Conceptual block diagram of the block reconfiguring logic.

### 5.5.5 Decision Block

Different blocks in the reconfigurable converter require their comparators to have different thresholds at different times. For example, in the pipeline mode, all blocks except for the last require comparator thresholds of  $\pm V_{ref}/4$  in both its stages; on the other hand, the last block in the converter requires zero thresholds from its comparator in the second stage. In the delta-sigma mode, the last block requires zero threshold from its comparators, while the other comparators can be disabled.

Due to these variable requirements, a programmable comparator was created and shown in Figure 5-13. It consists of a switched-capacitor circuit followed by a latch. If the block containing the comparator is the last active block, the variable 'L', as shown in the figure, is high; consequently, the switched-capacitor circuit shifts the sampled voltage signal  $INA+$  (or  $INA-$ ) by  $V_{REFN}/4$  (or  $V_{REFP}/4$ ) before presenting

the signal to the latch. Simple analysis shows that this condition will implement a comparator threshold of  $V_{REF}/4$ . If the block is not the last active block, on the other hand, the sampled input INA+ (or INA-) is presented to the latch inputs without a shift effectively implementing a zero comparator threshold. Hence, based on whether the 'L' bit in the figure is 1 or 0, the comparator either implements zero-threshold or a  $\pm V_{REF}/4$  threshold. The circuit for the latch is shown in Figure 5-14. The latch outputs are first pre-charged to the positive supply and then released. After a small delay, capacitor plates are connected to the input devices.

In the pipeline mode, the decision box in all-but-the-last block is responsible for determining the level of the residue of the previous stage relative to threshold levels  $\pm V_{REF}/4$ , in accordance with the standard implementation of the 1.5-bit/stage digital error correction that was employed in this converter. In this scheme, the entire range from  $-V_{REF}$  to  $+V_{REF}$  is divided into 3 zones, as has been described in Section 2.1.2.

Each of the four square comparator modules, shown in Figure 5-15, compares its input with a single threshold. Hence a pair of comparators is required to determine which of the three zones the previous stage residue falls into. This is shown by the pair of square modules on the left. Following the 2 modules, the post comparator logic formats the data from the comparators into the right form in order to drive the switches in the analog-core as well as the output-conditioning-block that sends the data out of the basic-building-block into the output interface.

Since there are 2 stages in each block, there are two sets of the above comparator pair and post-comparator logic. The numbers 11, 20, 21 and 10 refer to the clock phases that are used to drive the comparator.

In the last stage of the pipeline mode as well as the delta-sigma mode, the comparators are programmed to serve as zero-threshold comparators, and therefore, both the comparators in the pair produce the same result. In this case, either one of the results can be selected.

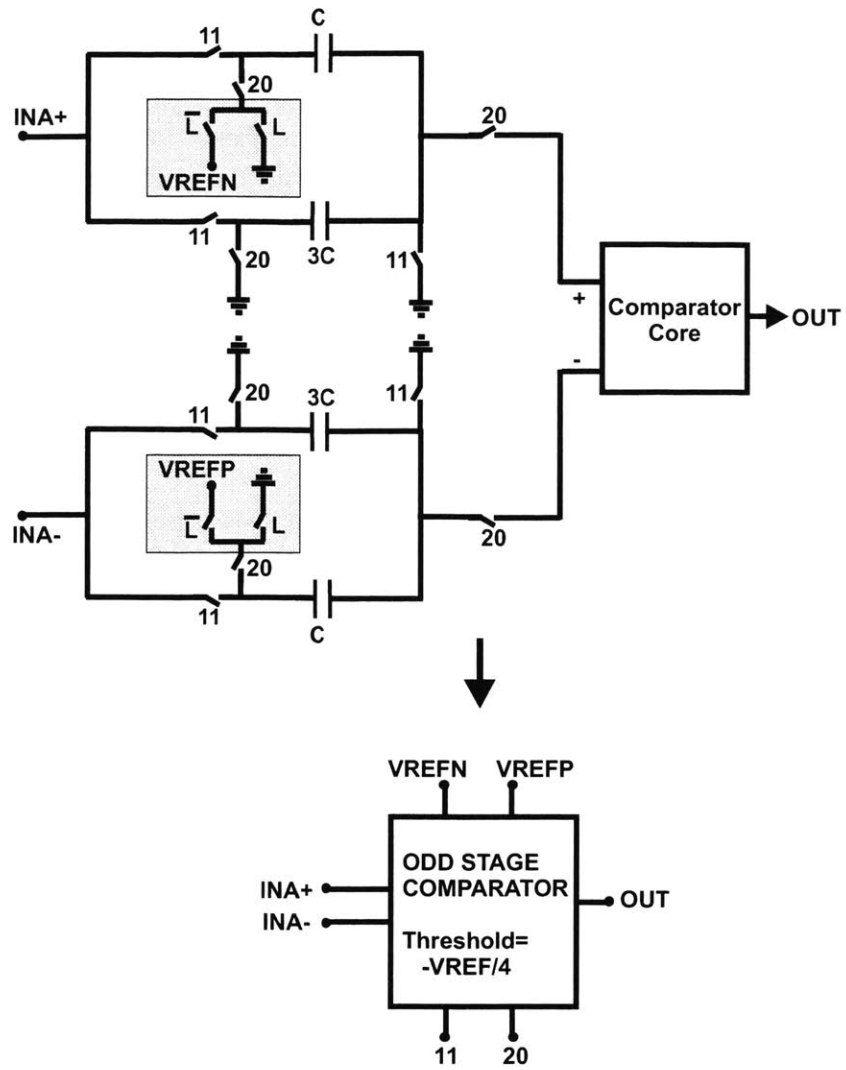


Figure 5-13: Switched-capacitor circuit details of each comparator.

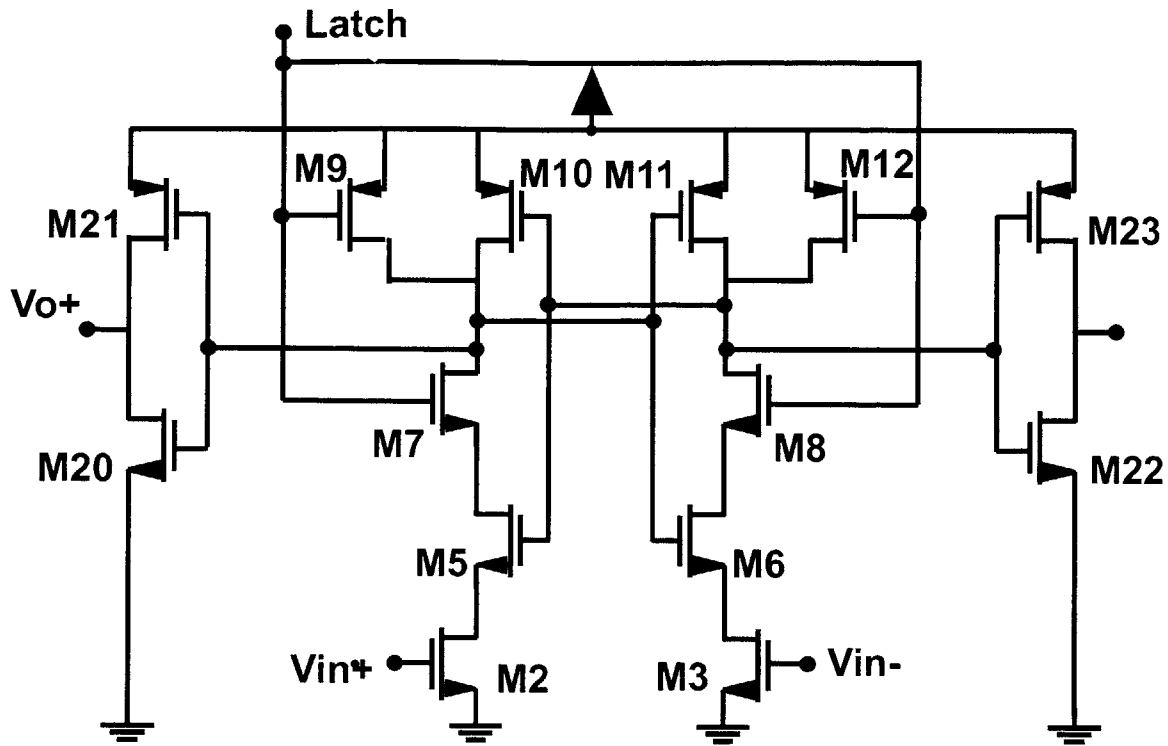


Figure 5-14: Transistor-level circuit details of the latch employed in the comparator.

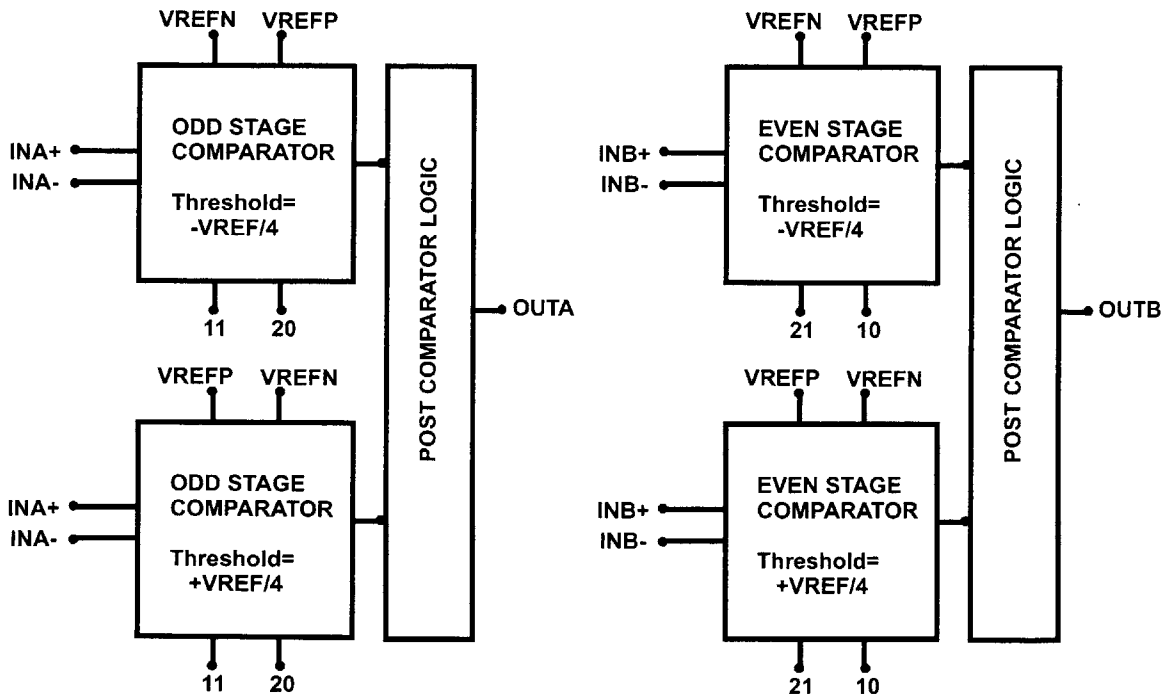


Figure 5-15: The block level diagram of the decision box in the basic building block.

### 5.5.6 Output Conditioning Block

The output conditioning block contains logic gates and serves two purposes: to process the data from the decision block and convert it to the format acceptable to subsequent blocks and to buffer the data in accordance with the added capacitive loading due to interconnect wiring.

## 5.6 Output Signal Processing and Interface

The output interface is responsible for four primary tasks: spatial alignment of bits from the basic building blocks, subsequent temporal alignment of these bits, signal processing for implementing the 1.5-bit/stage digital error correction, and lastly, driving the output data out of the chip.

### 5.6.1 Spatial Alignment of Digital Data

With each block containing 2 pipeline stages, there are a total of 16 pipeline stages in the converter. Each of these stages in the reconfigurable converter generates 2 raw bits (that corresponds to an effective number of 1.5-bits), denoted by  $a_i$  and  $b_i$ , where  $i$  corresponds to the  $i$ th stage. The idea behind spatially re-aligning bits is to make sure that the MSB always corresponds to output data bit D1, regardless of the architectural configuration of the converter.

Consider an example: When block B1 is the first active block, no re-alignment is required and all the bits are fed directly into the temporal alignment buffers, shown in Figure 5-16. On the other hand, if B2 is the first active block, all the output bits  $a_3, a_4, a_5...$  are shifted left so they appear in the nodes denoted as  $a_1', a_2', a_3'...$ , respectively. The same applies to all the  $b$  bits. To implement the shifting process, two 16-bit analog multiplexers are employed, one used for the  $a$  bits and the other for the  $b$  bits. The operation of this multiplexer is controlled by the main reconfiguring logic.

### 5.6.2 Temporal Alignment of Digital Data

The consecutive stages of the pipeline converter produce their bits corresponding to the same sample of input in consecutive clock phases. For example, the bits  $a_2$  and  $b_2$  are half clock delayed with respect to bits  $a_1$  and  $b_1$ . Hence it becomes necessary to re-align these bits. This is done using a triangular set of buffers constructed using D-flip-flops. The large number of flip-flops required makes it important to choose a flip-flop that has a very simple structure with few components. The schematic of the flip-flop employed here is shown in Figure 5-17.

### 5.6.3 Output Signal Processing and Output Buffering

The 16-bit adder shown in the figure implements the addition required to implement the 1.5-bit/stage digital error correction. Following the addition, a set of buffers drive the data to the low-swing output drivers that are ultimately responsible for transmitting the data out of the chip. The output of the quantizer in the delta-sigma mode is merged with the result right before the post addition buffering. The low-swing driver schematic is shown in Figure 5-18. The power supplies OUTHI and OUTLOW are selected in order to have the driver swing by about 0.4V-0.6V. The swings are reduced for two reasons: to reduce the noise injection into the substrate and to reduce the magnetic flux associated with the output bond-wires that, in some cases, can cause induced currents in the bond-wires associated with the converter input, and lead to data-dependent errors.



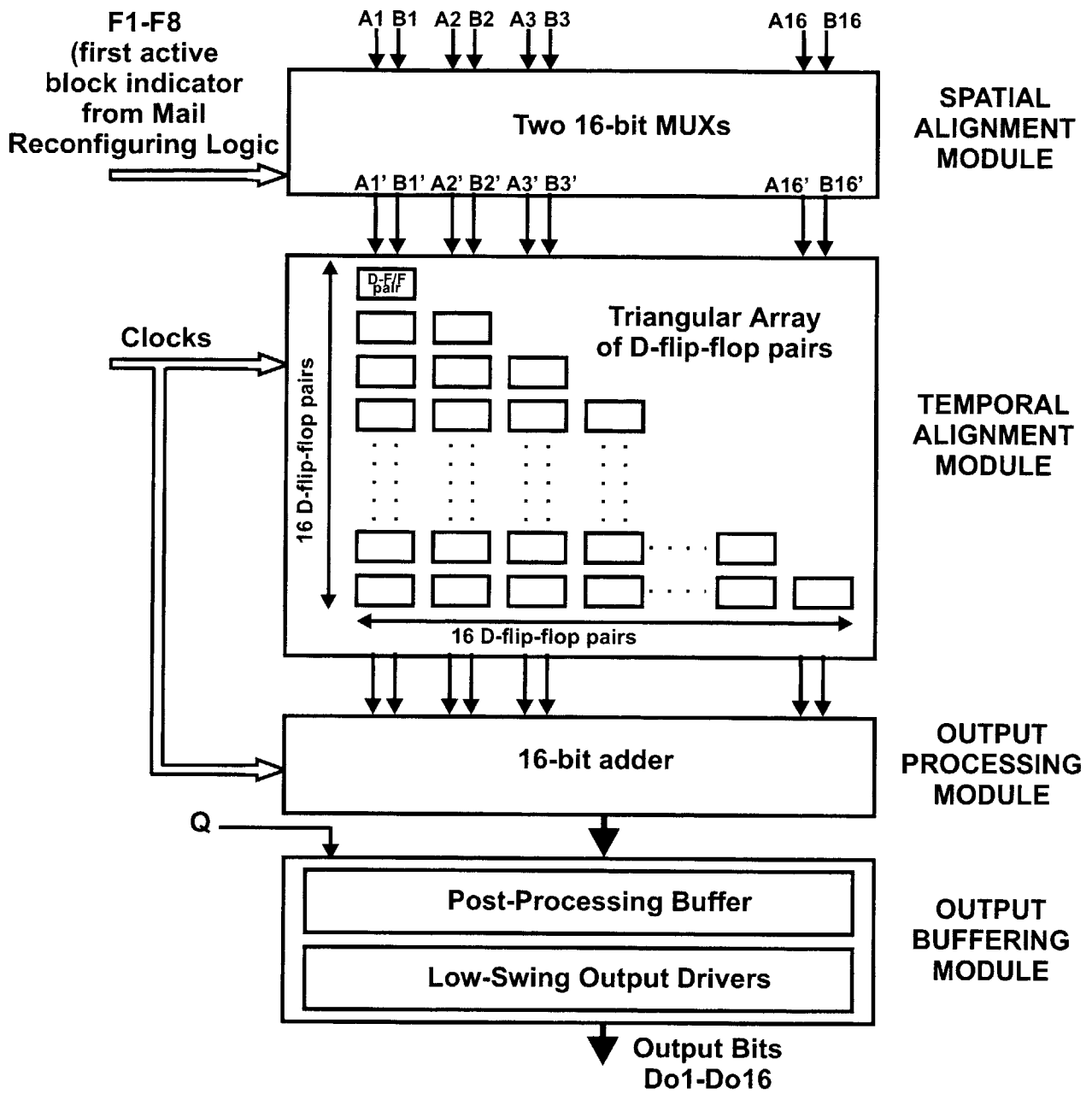


Figure 5-16: Block level diagram of the output interface.

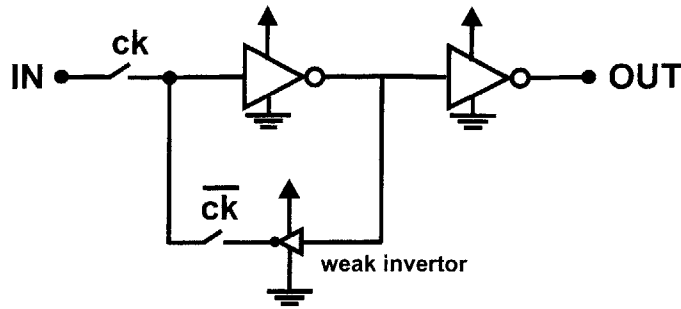


Figure 5-17: D-flip-flop employed for the spatial alignment buffers.

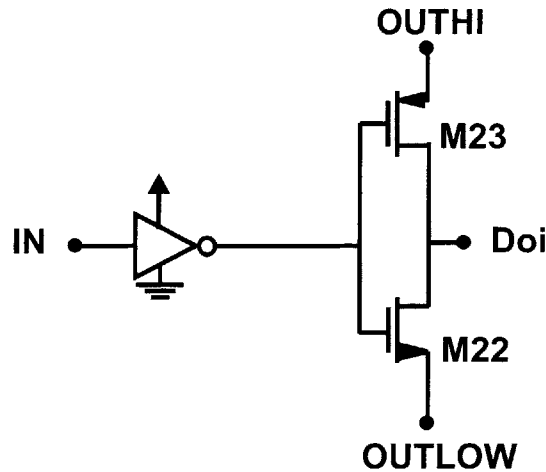


Figure 5-18: Schematic of low-swing output driver.

## 5.7 Testing Considerations

Several factors were considered to make the chip easier and more flexible to test and characterize. The following sub-sections list out the important features incorporated for this purpose.

**ESD Protection:** All pins except for the analog inputs and references are guarded with ESD protection circuits.

**Probing Pads:** Several probing pads were distributed over the chip in order to be able ascertain functionality of various sub-circuits for enhanced troubleshooting. Some of the nodes considered are: opamp voltage bias points, opamp common-mode feedback sensing point, global clock signals, some internal clock signals, selected output data from the basic-building blocks, outputs of VCO opamps, among others.

**Delta-sigma reset circuit:** In times of modulator instability, resetting the charge in the integrating capacitor across the opamps provides an effective method of inducing stability into the system. An on-chip circuit for sensing instability and then generating a reset signal has been provided. The circuit works by counting the consecutive 1s or 0s in the output. If a continuous string (of length 32) of either 1s or 0s is found, the modulator is considered instable. The circuit employs a binary counter for this job. Of course, it is possible to deactivate this circuit and instead apply a resetting signal from outside of the chip. This reset mechanism was not found to be necessary experimentally.

**Flexible reconfigurability:** For prototyping purposes, the entire main reconfigurable logic can be deactivated, and any combination of blocks in the converter can be activated.

**Fourth opamp in VCO:** To be able to test the hypothesis that the VCO oscillation frequency is indeed close to the unity-gain-frequency of the opamps, a fourth open-loop opamp has been placed with its inputs at the outputs of one of the three cascaded opamps in the VCO. At the oscillation frequency, the sinusoid at the output of the opamp should be observable.

**Output bias current from VCO opamps:** A bias current mirroring the bias currents in the VCO opamps are sent out of the chip to determine the functionality of the PLL.

**Method of deactivating major signals and blocks:** Several of the signals and circuits that have been referred to in this work can be simply switched off or bypassed. These include: global and opamp chopping signals, the delta-sigma reset circuitry and signal, PLL bias control, among others.

## 5.8 Mixed Signal Issues

Since the reconfigurable converter employs more digital circuits close to the sensitive opamp and switched-capacitor circuits, substrate noise coupling was a major concern. Certain steps were taken to alleviate the concerns caused by this malady. These are described below.

**Extensive On-chip bypass Capacitance:** Several sub-circuits in the converter employ bypass capacitors constructed using transistor gate capacitance. The total capacitance distributed over the chips is approximately on the order of 10nF.

**Extensive use of guard rings:** Guard rings consisting of both substrate contacts as well as n-well contacts have been employed to protect sensitive analog circuits such as opamps, comparators, switched-capacitor arrays among others.

**Spacing between Analog Circuit and block reconfiguring logic:** In order to reduce the noise injection from the block reconfigurable logic, significant empty space was kept between these modules. Taking the logic further away does increase the interconnect loading indirectly leading to larger logic, however, in a non-epi process, the noise injection drops exponentially. Since this circuit uses a non-epi process, it was considered a good trade-off to maintain some spacing between the circuits.

**Large number of ground and supply pins:** Approximately one-fourth of all pins in the chip are ground pins, while another fourth are supply pins. This is done to minimize the average bond-wire inductance of these signals.

**References from multiple pins:** The voltage references for the converter are supplied through physically separated pins in order, also to reduce bond-wire inductance.

**Sizing of clock generation circuit and other logic:** Wherever possible, logic has been constructed to make the signal edges as slow as tolerable by the circuit. For example, while several levels of buffering is employed in the clock drivers, the clock edge is kept deliberately slower than desired at the final destination. The block reconfiguring logic later sharpens the edges.

**Low swing output drivers:** As mentioned in an earlier section, a low-swing driver was employed for the dual reasons of reducing noise injection into the substrate as well as reduce magnetic flux associated with the bond-wires carrying the data.

## 5.9 Summary

This chapter presented the circuits details for several major circuit blocks of the reconfigurable converter. Some of the blocks considered are the main reconfiguring logic, the clock generator module consisting of the basic 2-phase generator, the multiple delayed phase generator, and clock drivers, the output interface circuits relevant to the spatial and temporal alignment, processing and driving of the output data, and the converter core. Within the converter core, interaction of the basic building blocks was described followed by a presentation of circuit details such as the opamp design, the decision block design and the block reconfiguring logic design. Issues related to making the chip easier to test and minimization of substrate noise coupling to sensitive analog circuits were also listed. The circuits related to the phase-locked-loop will be discussed in the next chapter.

## 6 Bandwidth Reconfiguration/PLL Design

### 6.1 Introduction

The goal of the reconfigurable converter is to digitize signals over a wide range of bandwidth and resolution. For varying resolution in the delta-sigma mode, the oversampling ratio is varied. Changing the sampling frequency either for the purpose of affecting resolution variation in the delta-sigma mode, or for changing the overall system bandwidth requires a method by which the bandwidth of the individual opamps are made to track the sampling frequency. This is accomplished by bandwidth reconfiguration as will be described in this chapter.

The simplest and most obvious approach to creating a bandwidth reconfiguration system is to divide the desired range of sampling frequency into a discrete number of bands, then employ a look-up table or some other mechanism to tune the opamp current based on the frequency band information. Perhaps a digital-to-analog converter could use the frequency band information to synthesize an appropriate bias current. As opamp bias current is decreased, the input devices of the opamp move from strong inversion through moderate and weak inversion regimes. In the strong inversion regime, the linear settling time of the opamp is inversely proportional to the square root of the current, while it is inversely proportional to current in the weak inversion region. This relationship is illustrated in Figure 6-1 that is a graphical depiction of the opamp speed versus bias current. Overall, this relationship is non-linear in nature. This non-linear characteristic imposes difficulty in the look-up table or digital-to-analog converter scheme. Even if this non-linearity can be incorporated into the tuning mechanism, the point where the transistors move from strong inversion to weak inversion is process dependent. Hence this scheme would require costly calibration to implement. Additionally, this tuning mechanism only affords bandwidth tuning over a finite set of discrete zones.

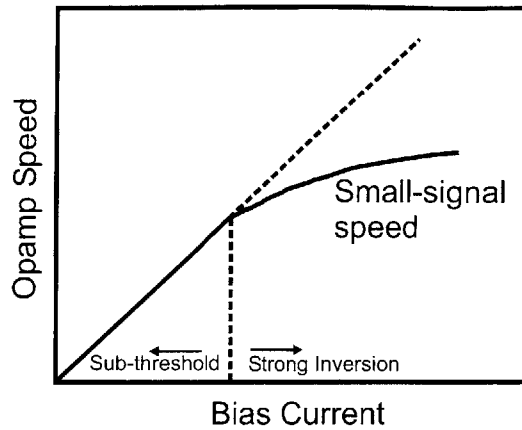


Figure 6-1: Variation of opamp linear settling speed versus bias current flowing through opamp inputs. The two regimes strong-inversion and sub-threshold refer to the regimes of the input devices of the opamp as bias current is varied.

The proposed solution employs a phase-locked-loop in order to sense the sampling clock frequency and generate an appropriate bias current that is exactly right regardless of the non-linear speed-current relationship. It also provides us with a continuous bandwidth reconfiguration methodology to cover the entire continuum of desired sampling frequency range.

## 6.2 Principle of operation of PLL

PLLs today are employed in a variety of applications such as clock synchronization, modulation and demodulation in communication systems, as well as frequency synthesizers. In this converter, a PLL is employed to generate optimized bias currents based on the clock frequency. PLLs have earlier been employed for tuning purposes in gm-C filters although their applications have mostly been restricted to fine tuning various filter parameters that depend on ratios of transconductance to capacitance within small ranges [10][40].

### 6.2.1 Bandwidth Reconfiguration

The front-end of the PLL employed in this converter consists of phase-frequency detector (PFD) that senses the difference in the converter clock frequency  $F_{\text{clock}}$  and the frequency of oscillation of an on-chip voltage-controlled-oscillator (VCO), as shown in Figure 6-2. This information is fed to the charge-pump (CP), which changes its output voltage corresponding to the change in the difference between the clock and VCO frequencies. A voltage-to-current converter (VIC) then converts the output voltage signal to a current, which is then fed to the converter and VCO as bias currents. The VCO itself is constructed using opamps that are replicas of the opamps in the converter, in such a way that the VCO frequency,  $F_{\text{vco}}$ , is proportional to the unity-gain-frequency of the opamps, which, of course, is in turn related to the bias current fed to the opamps. Since the VCO opamps are replicas of the opamps in the converter, the ratio of the speeds of the converter opamp and the VCO opamps remains fixed. The relationship between the unity-gain frequency and oscillation frequency is explored further in Section 6.3. If  $F_{\text{clock}} - F_{\text{vco}}$  is not zero, the action of the PFD, CP and VIC is to change the bias current of the VCO in such a direction that  $F_{\text{vco}}$  is made to ultimately (in steady state) track  $F_{\text{clock}}$ . The comparator shown in the figure serves to convert the sinusoidal VCO oscillations to a square wave.

If  $F_{\text{clock}}$  is increased, or in other words, the converter is clocked at a higher sampling frequency, the bias current fed to the opamps in the VCO and converter is increased in such a manner that the unity-gain-frequency of all the opamps tracks the clock frequency. Thus the settling time of the opamps in the converter is exactly proportional to the clock frequency regardless of the relationship between the transconductance of the opamps and the bias current.

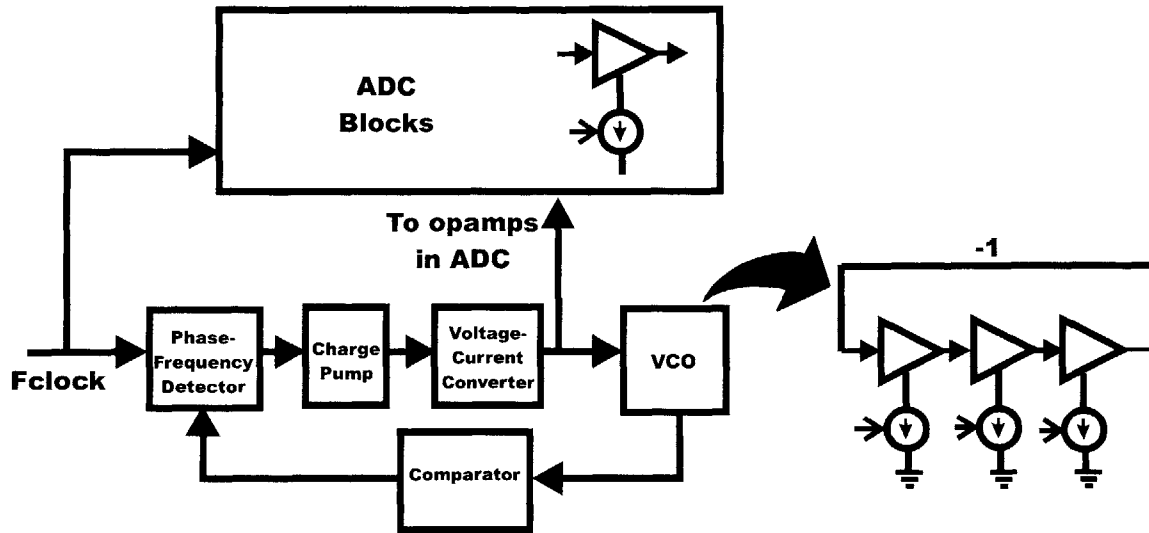


Figure 6-2: Bandwidth reconfiguration with a phase-locked-loop.

## 6.2.2 Effect of Changing Resolution on PLL operation

As converter resolution is increased, the stages in the converter need to settle to greater accuracy. The number of time constants to which the opamps must settle to is given by  $N \ln(2) \cdot \tau$ , where  $N$  is the desired resolution. In other words, the opamps must work faster and hence be supplied greater bias currents for the same clock frequency. As an example, at 16-bits of resolution, the desired bias current is as much as two and a half times the bias current when the converter operates in 6-bit mode. This elevated bias current at higher resolutions can be achieved by increasing the VCO capacitive load. Increased capacitive load will push the opamps in the VCO to work harder for the same speed. The capacitive calibration mechanism for this purpose is presented later.

## 6.3 Voltage Controlled Oscillator Theory and Design

As mentioned earlier, the VCO employed here consists of a cascade of three opamps placed in a loop. This section describes the theory behind the three-opamp VCO construction, including determination of the relationship between the oscillation frequency and the unity-gain frequency of the opamps, and design issues related to the VCO design.

### Basic Oscillator Theory

Figure 6-3 shows a simple feedback system with forward gain  $F(s)$  and feedback gain  $k$ . The loop transfer function  $L(s)$  is the product of the forward and feedback gains.

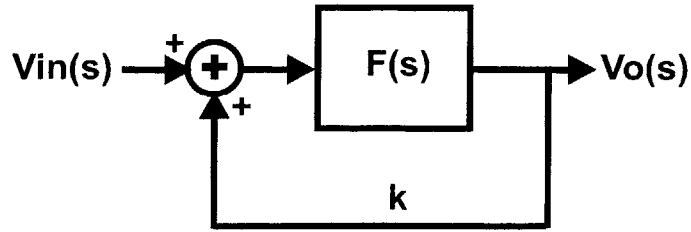


Figure 6-3: Basic feedback model with loop gain  $L(s)$ .

The overall transfer characteristic of this system can be written as:

$$T(s) = \frac{Vo(s)}{Vin(s)} = \frac{L(s)}{1 - L(s)} \quad (6.1)$$

where,  $s$  is the laplace operator. Considering the  $jw$  axis only, we have:

$$\frac{Vo(jw)}{Vin(jw)} = \frac{L(jw)}{1 - L(jw)} \quad (6.2)$$

For this system to behave as an oscillator,  $Vo(jw)$  should be finite even when no input is applied or  $Vin(jw)$  equals zero. For a finite  $L(jw)$ , this implies that:

$$1 - L(jw) = 0 \quad (6.3)$$

Equation (6.3) leads to the following criterion:

$$|L(jw)| = 1 \quad (6.4)$$

$$\angle L(jw) = n \cdot 360^\circ \quad (6.5)$$

where  $n$  is an integer. For sustained stable oscillations both of these conditions have to be simultaneously true.

Generally speaking, a system can either satisfy the above criterion for a given frequency, or have the two points where  $|L(jw)| = 1$  and  $\angle L(jw) = n \cdot 360^\circ$  not coincide. The latter case can be subdivided into two classes (a) systems where  $|L(jw)| < 1$  and  $\angle L(jw) = n \cdot 360^\circ$  and (b) systems where  $|L(jw)| > 1$  and  $\angle L(jw) = n \cdot 360^\circ$ .

In case (a), the poles of the system are on the left hand side of the laplace plane. Even if oscillations can be induced into the system through some form of energy injection, oscillations here are not self sustaining, and eventually will die out. In case (b), the poles are on the right hand side of the laplace plane and here, the oscillations will start on its own, and will continue to increase in amplitude.

There are a variety of ways of constructing oscillators. For an expansive review of these various oscillators, the reader is encouraged to refer to some excellent texts on this topic [41][42]. The following



will delve into some oscillator structures only for developing the oscillator that was designed for this application.

### A two-pole system as an oscillator

The simplest way of designing an oscillator is to employ a two pole system as the transfer function  $L(s)$ . An example of this approach is the quadrature oscillator shown below.

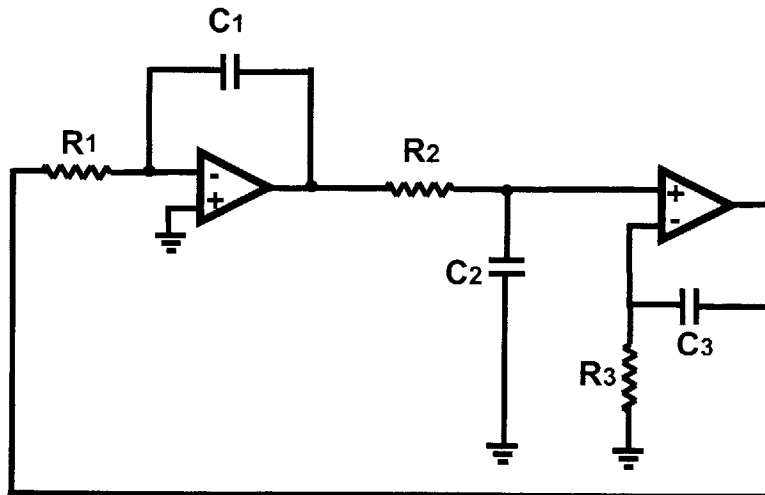


Figure 6-4: Quadrature oscillator circuit schematic.

With infinite opamp gain, the loop transfer function can be written as:

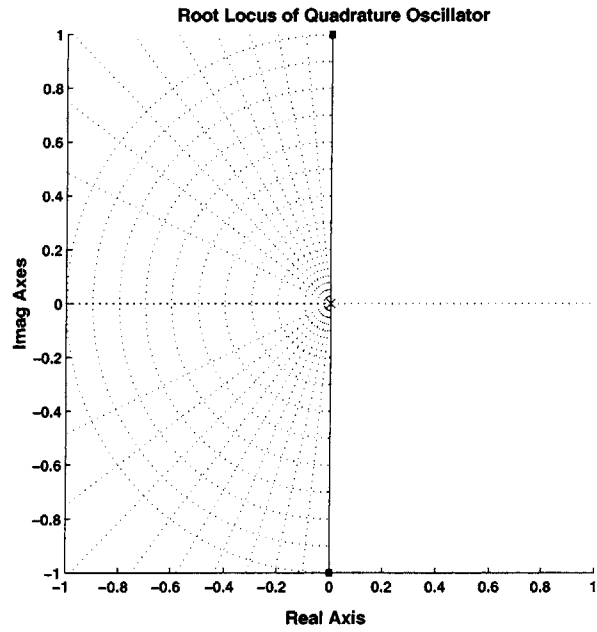
$$L(s) = \left( -\frac{1}{R_1 C_1 s} \right) \left( \frac{1}{R_2 C_2 s + 1} \right) \left( \frac{R_3 C_3 s + 1}{R_3 C_3 s} \right) \quad (6.6)$$

where, each of the parenthesis corresponds to one of the stages in the circuit. With  $R_1 C_1 = R_2 C_2 = R_3 C_3 = RC$ , the function can be simplified to:

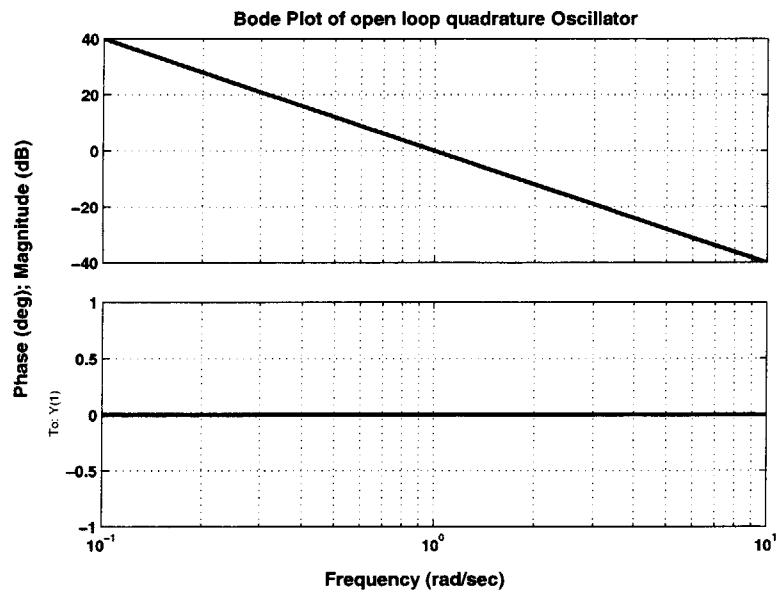
$$L(s) = -\left( \frac{1}{RCs} \right)^2 \quad (6.7)$$

Figure 6-5a shows the root locus of this structure. As  $k$  is increased from 0 to 1, the poles move along the  $j\omega$  axis. Various non-idealities such as finite opamp gain and component mismatch may cause the locus to fall to the left of the  $j\omega$  axis leading to unsustainable oscillations. One way to ensure sustainable oscillations is to force the poles to be slightly on the right-hand plane. A possible technique of accomplishing this is to make  $R_3 C_3$  slightly larger than  $R_2 C_2$  leading to a pole-zero doublet as shown in Figure 6-6. Thereafter, an automatic gain scheme can be employed to sense the amplitude variation and vary  $R_3$  to keep the oscillation amplitude constant.

Another approach of pushing the poles onto the right-hand plane is to place a zero at DC, as shown in Figure 6-7. This is tantamount to employing a band-pass function as the open-loop transfer characteristic. A popular implementation of this scheme is known as the Weinbridge oscillator [42]. In this specific oscillator a gain slightly greater than 3 places the poles just right of the  $j\omega$  axis.



(a)



(b)

Figure 6-5: Quadrature oscillator. (a) root-locus as feedback gain  $k$  is increased from zero to infinity. Location of poles when  $k$  is unity is represented by the squares. (b) Bode-plot.

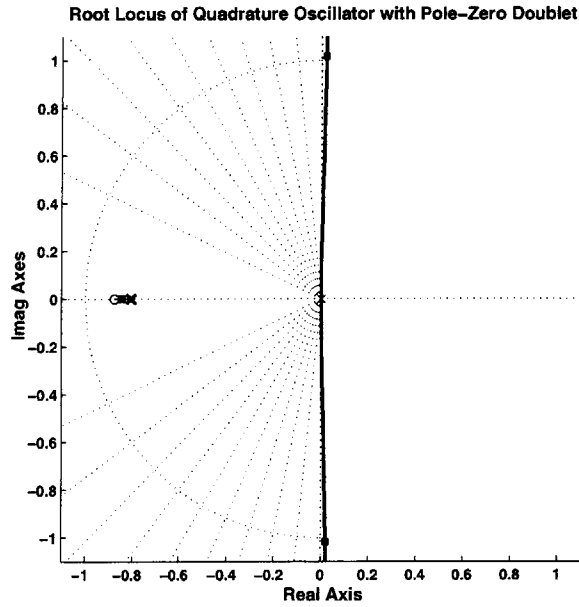


Figure 6-6: Root-locus of quadrature oscillator with pole-zero doublet as feedback gain  $k$  is increased from zero to infinity. The pole-zero doublet pushes the closed loop poles into the right-hand plane. The small dark squares represent the location of the poles when  $k$  is unity.



Figure 6-7: Root-locus of the two-pole system with zero at DC.

### A two-opamp cascade as an oscillator

In this application, the PLL needs to generate a bias current corresponding to the sampling clock frequency employed in the converter such that the settling time of the ADC opamps is optimal for the applied clock frequency. Ideally, therefore, an oscillator is required where the oscillation frequency corresponds to the unity-gain frequency by a constant factor. Figure 6-8a shows a conceptual diagram of a possible candidate for the oscillator. Here each of the gain blocks would be a replica of the telescopic opamp employed in the ADC. Each of these opamps can be modeled by network shown in Figure 6-8b.

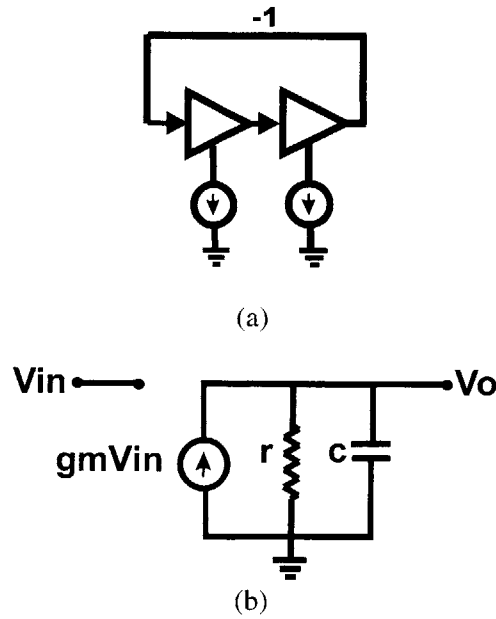


Figure 6-8: (a) Conceptual diagram of two-opamp oscillator. (b) Model of each opamp.

The transfer function of each of these amplifiers can be written as:

$$L_1(s) = \left( \frac{gm \cdot r}{1 + r \cdot Cs} \right) = \left( \frac{gm/C}{s + 1/(r \cdot C)} \right) \quad (6.8)$$

where  $gm$  is the transconductance of the amplifier and,  $r$  and  $c$  are the output resistive and capacitive elements, respectively. Rewriting, the overall loop function is:

$$L(s) = - \left( \frac{w_U}{s + w_p} \right)^2 \quad (6.9)$$

where,  $w_U = gm/C$  that is representative of the unity-gain frequency of the amplifier and  $w_p = 1/r \cdot C$  that represents the open-loop pole of the amplifier. Note that the exact location of the unity-gain

frequency is actually  $w_{TU} = \sqrt{w_U^2 - w_P^2}$ <sup>1</sup>. While  $w_U$  is conventionally referred to as the unity gain frequency of the amplifier, this is true only for  $w_U \gg w_P$ . This occurs for most high gain operational amplifiers. For the VCO, however, as we will see, the loop feedback shifts the open-loop pole  $w_P$  to a frequency close to  $w_U$ , so to be precise we will use the exact unity-gain frequency expression in this section.

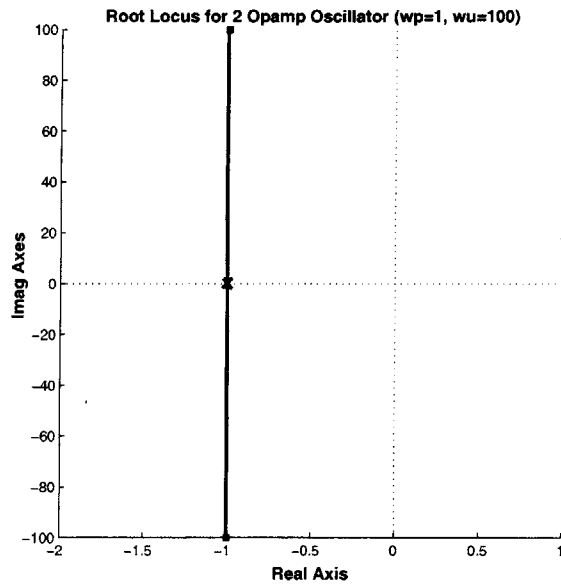
Figure 6-9a and Figure 6-9b show the root-locus and bode plot of such a system. For this oscillator the feedback gain  $k$  is fixed at unity. It is clear that such a system cannot oscillate sustainably because the poles remain on the left hand plane while the feedback gain is increased. Another way of arriving at the same conclusion is by observing that the 2-pole system does not provide sufficient phase-shift ( $180^\circ$ ) at the unity-gain frequency.

The opamps do have parasitic poles. However, as will be seen later, explicit capacitances have been employed at the outputs of each of these opamps to lower VCO oscillation frequency. This implies that these parasitic poles are at a much higher frequency compared to the unity-gain-frequency. Thus they do not contribute phase delay sufficient phase delay through the 2 opamps. Even if they do, it is not wise to rely on these poles since the location of these poles and hence excess phase due to these poles is not well controlled.

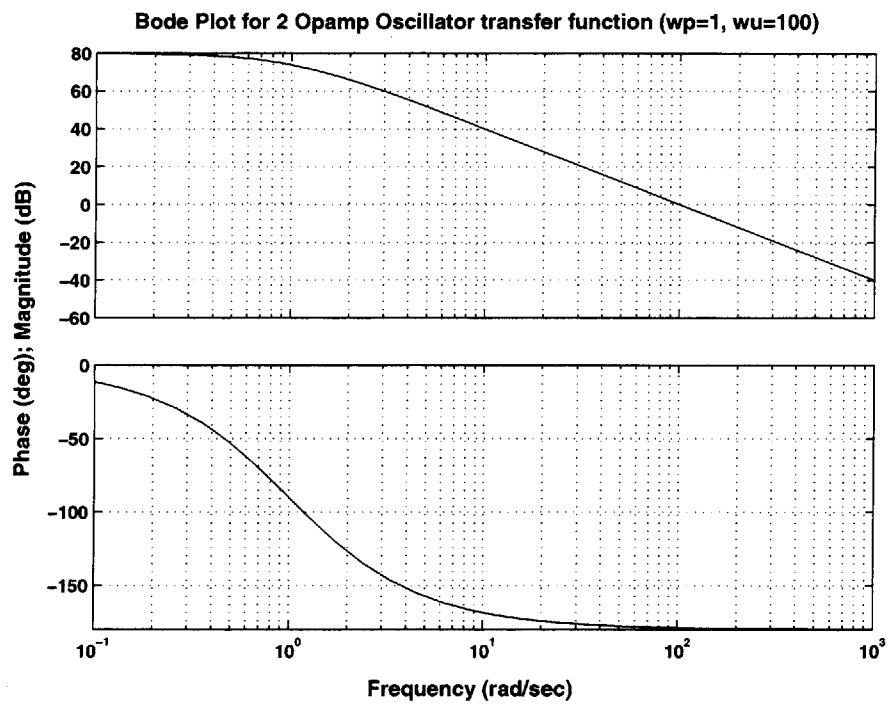
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<sup>1</sup> The true unity gain frequency point  $w_{TU}$  can be found by equating  $\left| \frac{w_U}{jw_{TU} + w_P} \right| = 1$ . This leads to

$$\frac{w_U}{\sqrt{w_{TU}^2 + w_P^2}} = 1 \text{ or } w_{TU} = \sqrt{w_U^2 - w_P^2}$$



(a)



(b)

Figure 6-9: Two-opamp oscillator. (a) root-locus as feedback gain  $k$  is increased from zero to infinity. Location of poles when  $k$  is unity is represented by the squares. (b) Bode-plot.

### A three-opamp cascade as an oscillator

To provide the excess phase required by the oscillator, an additional opamp is placed in the loop as shown in Figure 6-10. Figure 6-11a shows the root locus of the closed loop system as the feedback gain is increased. Here two of the poles are pushed into the right-hand plane as shown in the figure. The terminal points of the locus, marked by the black dots, represent a feedback gain of unity as is the case here. Clearly, the amplitude of the oscillations in this oscillator will exponentially increase with time unless it is limited by some means. The bode diagram of the open loop system is shown in Figure 6-11b.

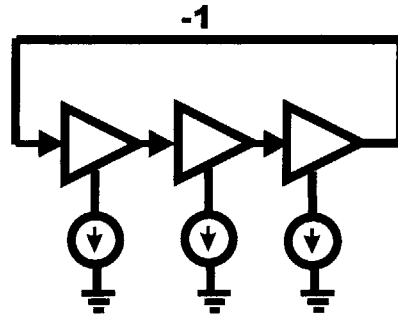
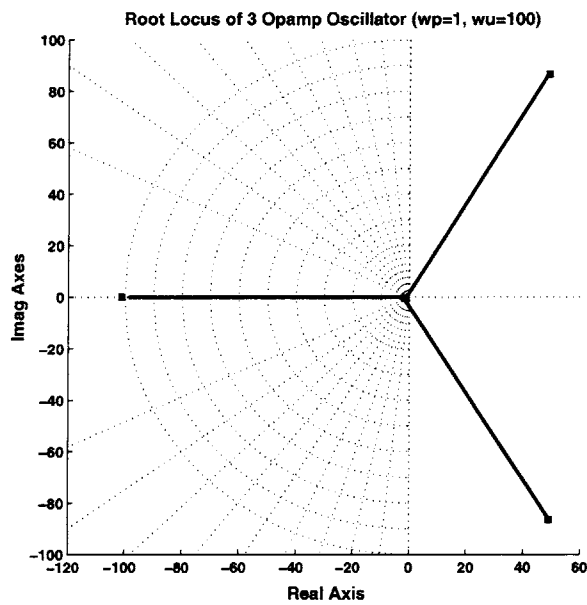


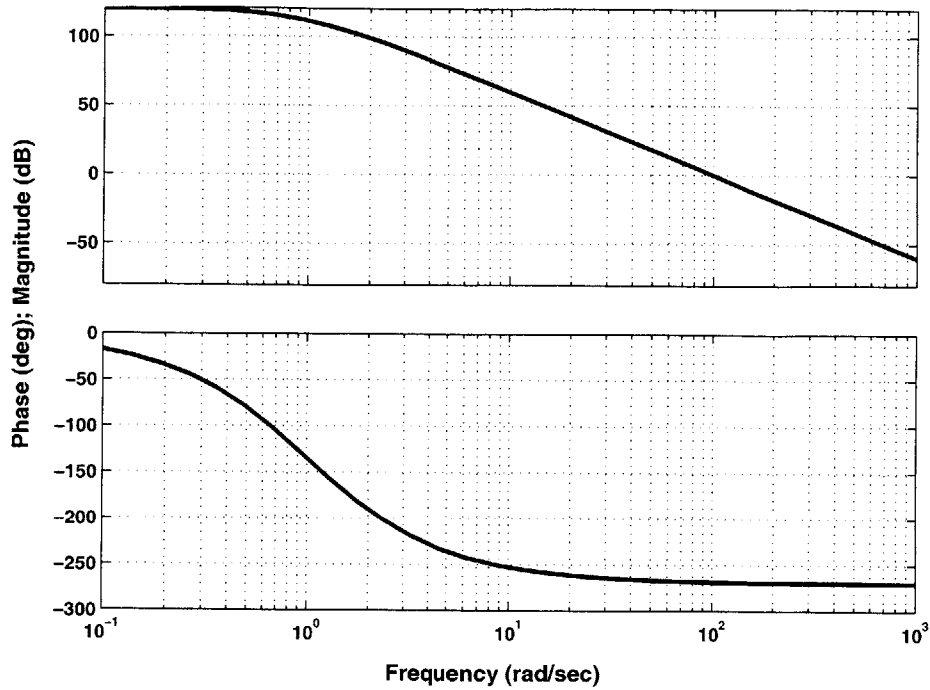
Figure 6-10: Conceptual diagram of three-opamp oscillator.



(a)



Bode Plot for Open-loop 3-opamp Oscillator transfer function ( $w_p=1, w_u=100$ )



(b)

Figure 6-11: Three-opamp oscillator. (a) root-locus as feedback gain  $k$  is increased from zero to infinity. Location of poles when  $k$  is unity is represented by the squares. (b) Bode-plot.

The precise position of the poles is estimated below. As described earlier, each of the opamps can be represented by a transfer function  $\left(\frac{w_u}{s + w_p}\right)$ , where,  $w_u = gm/C$  that is representative of the unity-gain frequency of the amplifier and  $w_p = 1/r \cdot C$  that represents the open-loop pole of the amplifier. The overall open-loop transfer function (including the sign inversion) through the 3 opamps can be written as:

$$L(s) = -\left(\frac{w_u}{s + w_p}\right)^3 \quad (6.10)$$

The closed loop pole locations can be determined by equating  $L(s) = 1$ , leading to:

$$s + w_u = (-1)^{1/3} w_u \quad (6.11)$$

Since the cubed-roots of  $-1$  are  $-1, \frac{1}{2} + j\frac{\sqrt{3}}{2}$  and  $\frac{1}{2} - j\frac{\sqrt{3}}{2}$ , the three closed loop poles are at:

$$w_{PC} = \begin{cases} -w_U - w_P \\ \left(\frac{1}{2}w_U - w_P\right) + j\frac{\sqrt{3}}{2}w_U \\ \left(\frac{1}{2}w_U - w_P\right) - j\frac{\sqrt{3}}{2}w_U \end{cases} \quad (6.12)$$

The 2 poles that lie on the right-hand plane have the same real part of  $\frac{1}{2}w_U - w_P$  and complementary imaginary parts of  $\frac{\sqrt{3}}{2}w_U$ .

To limit the amplitude of the oscillations in a controlled manner, diodes are placed across the outputs of each of the opamps. The effect of the diode is to reduce the “average” small-signal output resistance of each of the opamps. Output resistance variation can only shift the open-loop pole location  $w_p = 1/r \cdot C$  and will not impact  $w_U = gm/C$ . This implies that the diode limiting can only change the real part of the complex closed loop poles. Effectively, the closed loop poles will be shifted left, as shown by the dotted line in Figure 6-12, until the poles lie on the  $jw$  axis leading to sustained oscillations. For this to happen,  $\frac{1}{2}w_U - w_P$  must equal zero, or  $w_P = \frac{1}{2}w_U$ , or in other words the open-loop pole is pushed up to the point where it is half the value of  $w_U = gm/C$ . Under this condition, the oscillation frequency is equal to the imaginary part of the complex poles, or  $\frac{\sqrt{3}}{2}w_U$ .

To obtain more insight, let us consider the transfer function of each opamp under the condition that  $w_P = \frac{w_U}{2}$ . Under this condition, the transfer function of each opamp is  $\frac{w_U}{jw + \frac{w_P}{2}}$ . If we apply a pure

tone of frequency  $\frac{\sqrt{3}}{2}w_U$  the phase delay through the opamp is  $\tan^{-1}(\sqrt{3}) = 60^\circ$  and the gain through

the opamp is exactly  $\sqrt{\left(\frac{1}{2}\right)^2 - \left(\frac{\sqrt{3}}{2}\right)^2} = 1$ . Since there are 3 opamps, the phase delay is exactly what is

necessary to provide a sustained oscillation. From the bode plot in Figure 6-11(b), it is clear that the original open-loop opamp has much more than  $60^\circ$  phase shift at the unity-gain frequency point. The addition of the limiting action causes the open loop poles of the opamps to be shifted to such a point that the  $60^\circ$  phase delay point is shifted up to coincide with the *true* unity-gain point. Note that the true unity-gain frequency point is *not*  $w_U$  but  $\sqrt{w_U^2 - w_P^2}$  as was derived earlier.

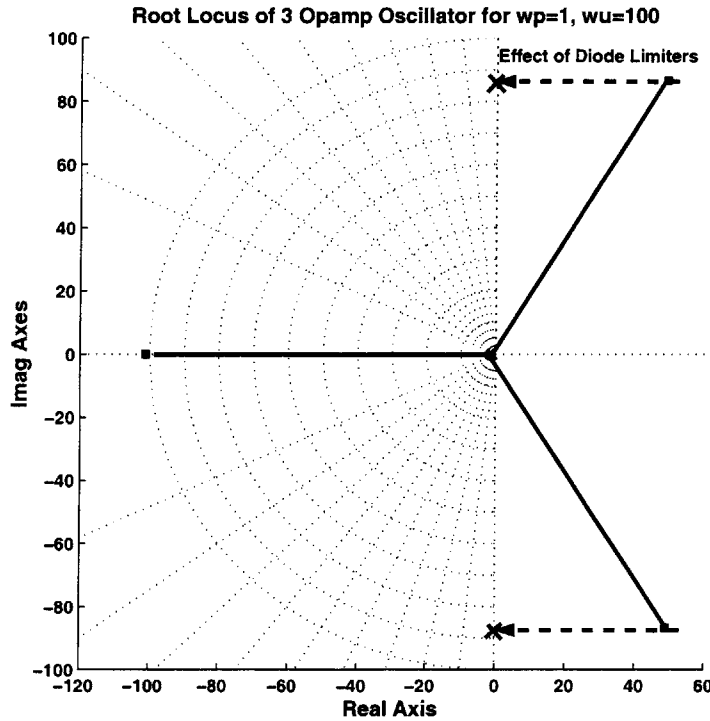


Figure 6-12: Root-locus of three-opamp oscillator with dashed line showing trajectory of poles due to diode limiting.

The oscillation frequency of  $\frac{\sqrt{3}}{2} \frac{gm}{C}$  has been obtained assuming a completely linear system (assuming that the small-signal output resistance is reduced uniformly over the entire voltage range). This is, of course, not completely true. However, the result obtained through the linear approximation, is very close to MATLAB and HSPICE simulations of both the transistor level model and the actual circuit. Figure 6-13 plots the ratio between the oscillation frequency and  $w_U = gm/C$  for a wide range of opamp bias current. The line in bold represents the  $\frac{\sqrt{3}}{2}$  ratio point as predicted through the linear systems model. It is clear that the simulated ratio remains below but close to this prediction over a wide operating range of the opamps.

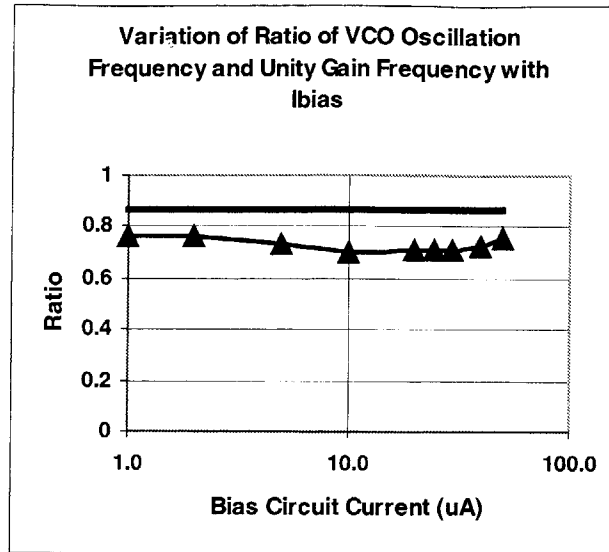


Figure 6-13: Variation of ratio of oscillation frequency and unity-gain frequency ( $gm/C$ ) as bias current through the opamps is varied. Results obtained from HSPICE simulations of actual VCO circuit employing junction diodes as the limiter.

As far as the limiters are concerned, the limiting action for the above plot was provided by junction diodes, whose implementation will be described in greater detail in a later section. When a MOS diode was employed as the limiter, it was found that this ratio tended to be slightly lower (around 0.65). For this reason as well as reducing the amplitude even further (for reasons described later), junction diodes were employed.

## 6.4 PLL Circuit implementation

### 6.4.1 Top Level Description

The primary circuit highlights of the PLL include the design of the charge-pump that includes a mechanism to reduce charge sharing between its internal nodes and the primary charge-pump output, the voltage-to-current converter that allows the PLL to track three orders of magnitude variation in clock frequency, the VCO design issues, and the comparator selection and design.

### 6.4.2 Voltage-controlled-Oscillator

#### 6.4.2.1 VCO Circuit

The opamp employed in the VCO has a plain telescopic architecture without the gain enhancement amplifiers and is an exact replica of the smallest telescopic structure used in the converter, in other words, the structure employed in Blocks B3-B8.

The bias circuit for this opamp only entails the circuits necessary for the telescopic structure as there are no gain-enhancement amplifiers; hence the bias circuits are topologically identical to the bias circuits in blocks B6-B8 that also do not incorporate the gain-enhancement amplifier.

These opamps employ the discrete-time switched-capacitor common-mode feedback (CMFB) as employed in the main converter. Although this does change the loading of the opamp from the high clock phase to the low clock phase, the influence of that on the overall VCO frequency is insignificant because of the relatively small size of the CMFB capacitors with respect to the overall opamp loading.

Since the outputs of the opamp are fed to the inputs of the next opamp successively through the VCO, the common-mode outputs of the opamps in the VCO are maintained, using the CMFB, at the level of the opamp input common-mode level, and *not* at a fixed voltage at the center of the power supplies as in the main converter. Hence with changing bias current through the opamp, this level also changes. Of course, it is ensured that all the transistors remain in the saturation mode through the entire working range of the opamps as the bias current is reduced (i.e. through strong and sub-threshold regimes). Fortunately this is not a very complex task as diode limiters only permit a small oscillation amplitude of  $\pm 300\text{mV}$  single-sided at the output of each opamp.

To construct the VCO three opamps are cascaded together, differentially, in a loop, as has been described earlier and shown in Figure 6-14. For simplicity every opamp has its own bias circuit. Each opamp is also equipped with its own diode limiter and capacitive load calibration circuit, as will be described later.

For the purposes of characterizing and validating the new design inherent in this VCO, a fourth opamp is employed whose inputs are fed by the outputs of one of the three opamps. The outputs of this fourth opamp are also tied to the diode limiters and capacitance calibration circuit. This opamp plays no role in the actual functioning of the converter. Test pads are provided in the layout to observe the input and output states of this opamp. Note that the load of the fourth opamp is insignificant compared to the explicit capacitance load applied to the VCO opamps.

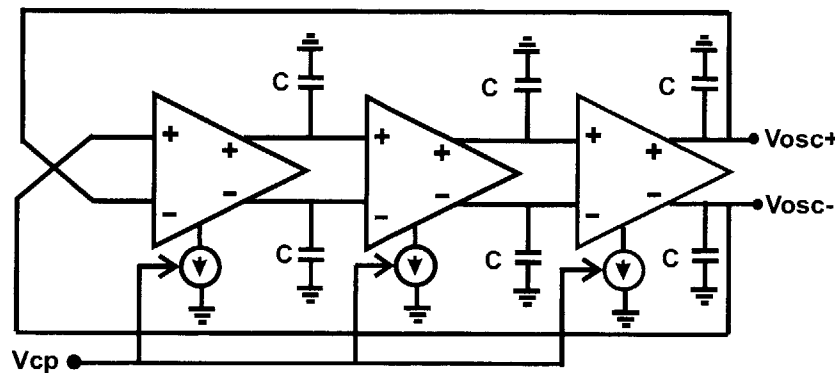


Figure 6-14: VCO construction.

As has been described earlier, diode limiters of the form shown in the Figure 6-15 are each placed across the differential outputs of the opamps in the VCO to limit the differential output level of the opamps to the forward bias voltage of the diodes at approximately  $600\text{mV}$ .

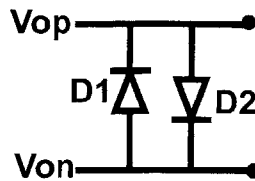


Figure 6-15: Circuit arrangement of diode limiters. Vop and Von refer to the positive and negative terminals of the opamps.

There are two main reasons for limiting the output level of the opamps:

If left unlimited, the amplitude of these opamps would increase unrestrained bounded only by the available swing of the amplifiers. At the upper and lower bounds of the voltage levels, the cascode transistors would be pushed deep into the linear range. This type of limitation provides *soft limiting* as opposed to the harder limiting provided by the diodes. As has been mentioned earlier, a hard limiter leads to purer sine functions in the oscillation, and thus makes the frequency of oscillation closer to the theoretical prediction of  $\sqrt{3}/2$  times the value of the unity-gain frequency.

The diode limiters restrict the swing of the oscillator opamps to about 600mv, which is about a fourth of the overall swing of the opamp. In the process they reduce the dependence of the oscillation frequency on slewing time. Hence the action of placing the diode limiters makes the VCO oscillate with frequency that is dominated by the small-signal characteristics of the VCO opamps.

### Implementation

Two-terminal diodes do not exist in a CMOS process. It is possible to employ a p+-diffusion in an n-well as shown in the top left of Figure 6-16. However, when the p+-diffusion and the n-well diode is forward biased, the reverse-biased junction of the n-well with the substrate can cause some charge flowing across the diode to be collected causing charge injection into the substrate. In fact this implementation can be modeled as the bipolar transistor shown in the bottom left corner in the figure. This injection can reduce the effectiveness of the 'diode'. More importantly, if these diodes are placed in physical proximity to other circuits, this injection can lead to latch-up. To minimize this the n-well contact should be placed as close to the p+-diffusion region as possible. Alternatively, another p+-diffusion connected to the same terminal as the well can be placed close to the p+-diffusion connected to Vop, the positive output terminal of the opamp, in order to attract more of the charge from Vop to Von, the negative opamp output terminal. This is depicted in the top right of the figure. Effectively, the addition of this p+-diffusion region connected to Von is tantamount to adding another collector in the original bipolar model to reduce the flow of charge into the substrate as shown on the bottom right. Essentially this is an effort to reduce the beta of the parasitic bipolar transistor shown in the bottom left corner.

Figure 6-17 shows the top view of the diode implementation. The p+ region in the center corresponds to node Vop shown in Figure 6-16. The p+ region connected to Von is created all around the p+ diffusion in the center in order to further reduce the charge injection into the substrate.

Additionally, in order to ensure that any charge injected into the substrate is removed from circulation, guard-rings consisting of alternate rings of p+-diffusion to ground and n-well connected to the positive supply are created.

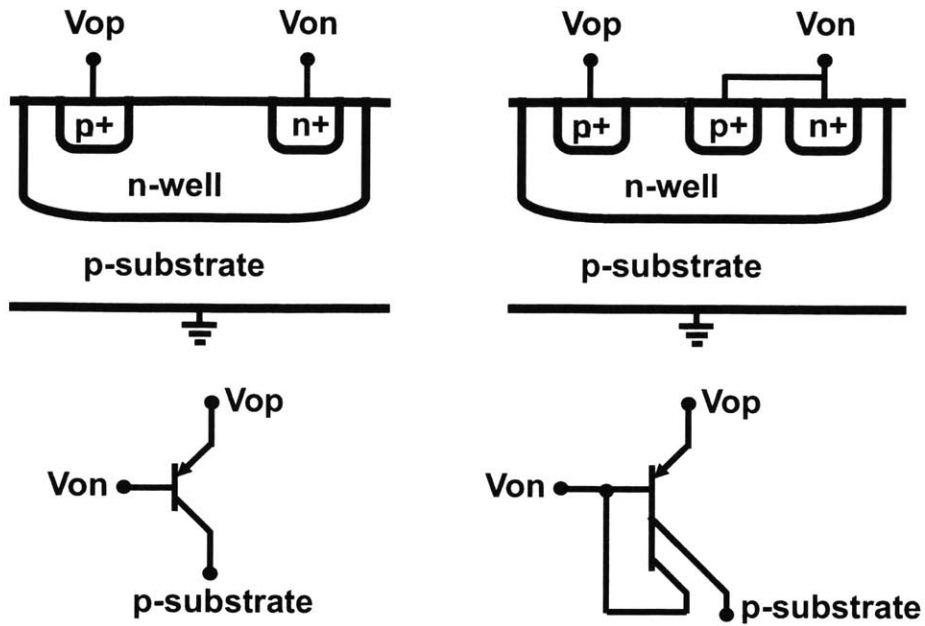


Figure 6-16: Implementation of diode limiters.

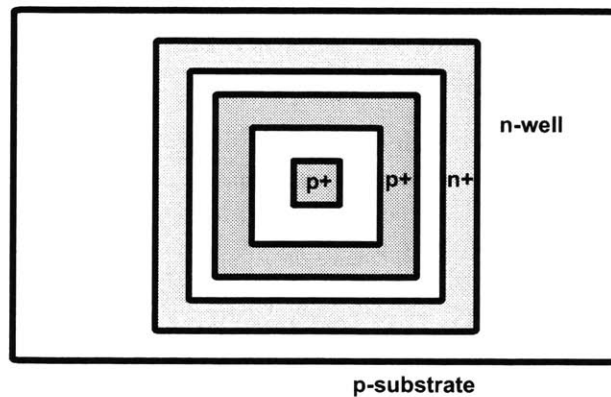


Figure 6-17: Top view of implementation of diode limiters.

#### 6.4.2.2 Capacitance Calibration Circuit

From a settling time perspective, the unity gain frequency of the opamp has to be several times larger than the clock frequency. As an example, assuming a feedback factor of  $\frac{1}{2}$ , the unity gain frequency has to be at least 34 times the clock frequency if the opamp has to settle to within a 12-bit LSB at the end of the clock period. Based on previous discussion it is known that the VCO oscillates at a frequency of  $\frac{\sqrt{3}}{2}$  times the unity gain frequency. In addition, as discussed earlier, this ratio depends on the resolution desired from the converter. In order to formalize the capacitive load relationship between the opamp in the VCO and the converter, we have:

$$V_o = V_f(1 - e^{-T/2\tau}) \quad (6.13)$$

where,  $T$  is the sampling period,  $\tau$  is the time constant of opamp settling,  $V_o$  is the output voltage and  $V_f$  is the expected final voltage. The worst case error  $\epsilon$  occurs when the final output voltage  $V_f$  equals  $V_{ref}$ . For half-LSB settling precision, the following expression holds:

$$\epsilon = V_{ref} \cdot e^{-T/\tau} \leq \frac{(2 \cdot V_{ref})}{2^{N+1}} \quad (6.14)$$

$$T \geq \tau \cdot 2N \ln(2) \quad (6.15)$$

$$F_{clock} \leq \frac{\beta}{2N \ln(2)} \cdot F_{ugf} \quad (6.16)$$

where  $N$  is the desired resolution,  $F_{clock}$  is the clock frequency and  $F_{ugf}$  is the unity-gain-frequency.

The minimum ratio between the unity-gain-frequency and clock frequency is:

$$\frac{F_{ugf}}{F_{clock}} = \frac{2N \ln(2)}{\beta} \quad (6.17)$$

There are several approaches to resolving the difference between the oscillation frequency and the absolute unity-gain-frequency desired from the converter opamps.

One approach is to divide down the oscillation frequency using a mechanism such as a counter before feeding it to the PFD. The divider ratio would be dependent on several factors such as the noise gain of the opamp in amplifying mode, settling precision required, among others. If this option were employed, the VCO would be oscillating at a frequency much higher than the clock frequency. This may generate some substrate noise that can possibly alias back into the signal band. Further, the sine wave from the VCO has to be converted into a square wave before feeding it into the PFD. This is achieved by a comparator. A slower oscillation frequency would significantly simplify the design of the comparator as will be described.

Another approach is to slow down the VCO oscillation by either increasing the capacitive load of the VCO or by reducing the transconductance of the VCO opamp relative to the opamp in the converter. The opamps used in the VCO are identical to the opamps in the latter blocks of the converter, in other words they are scaled-down versions of the largest opamp in the converter. At this size, it isn't possible to decrease the transistor size any further.

In this design, the second option is pursued; the VCO opamp unity gain frequency is reduced by adding an explicit fixed value of a poly-poly capacitor across the VCO opamp outputs. Additionally several capacitors with series switches are placed across the VCO that can be added or removed from the VCO opamps.

An additional benefit of providing a calibration circuit is to provide for contingency. The process of estimating the ratio between the clock frequency and unity-gain-frequency is not exact, as demonstrated in equation (6.17). Several assumptions with regards to expected noise gain, interconnect capacitance, among others, are made. As seen earlier, even the ratio between the unity-gain-frequency of the VCO opamps and the oscillation frequency can vary by small amounts. Capacitance calibration provides a



prudent method to combat these uncertainties. The calibration range has been designed in keeping with this observation.

### 6.4.3 Comparator

The diode-limited sinusoidal oscillations of the VCO need to be converted to a square waveform before it can be supplied to the phase-frequency detector. A continuous-time comparator is required for this purpose.

As the bandwidth of the reconfigurable converter is decreased, the bias current through the VCO reduces. The common-mode voltage level of the output of the VCO opamps is set to be equal to the desired input-common-mode level using a standard switched-capacitor CMFB circuit. When the input devices are in strong inversion, the desired common-mode voltage level is  $V_{TN} + 2\Delta V + V_{MAR}$ , where,  $V_{TN}$  is the threshold voltage of the input transistor shown in Figure 5-7,  $\Delta V$  corresponds to the  $V_{GS} - V_{TN}$  of the device, and  $V_{MAR}$  is the margin voltage across the drain-source terminals of the tail transistor in order to ensure that it remains in saturation. When the device is in sub-threshold, the appropriate input-common-mode voltage level is arranged to be  $V_{TN} + 3\frac{kT}{q}$ , where the factor  $3\frac{kT}{q}$  ensures that the tail transistor is in saturation [Refer Section 5.5.2.4 for more details]. With decreasing bias current, the factors  $\Delta V$  and  $V_{MAR}$  go from their maximum values to zero. This causes the common-mode level of the VCO oscillation to reduce when the input devices are in strong inversion. In fact, the common-mode voltage difference between the cases when the converter is running at maximum bandwidth and when it is running at its slowest can be as much as 1V.

The comparator needs to be designed with this in mind. The approach employed here is to employ a replica of the VCO opamp in open loop as the comparator. To account for the input-common-mode voltage variation, *the bias current through this comparator is also varied exactly in the same manner as the bias current through the VCO opamps*. Thus the appropriate input common-mode level of the comparator amplifier is exactly what is supplied by the VCO opamps.

There are two additional advantages of this choice. (1) The power of the comparator also scales with the rest of phase-locked-loop and converter. A fixed bias current comparator would have had to be designed for the maximum speed. At this power level, the comparator would easily have been one of the most power hungry components in the converter when it is working at low speeds (2) Since the current in the comparator is varied in lock-step, the ratio between the VCO oscillation frequency and the unity-gain-frequency of the comparator remains fixed. This means that the gain of the comparator amplifier remains fixed regardless of the oscillation frequency. This ensures that the voltage levels presented to the PFD are always at digital levels. In this case a gain of 10 was selected.

### 6.4.4 Phase-Frequency Detector

A standard phase-frequency detector described in [43] is selected for this design. The PFD that consists of two D-flip-flops and some logic places the following charge-pump in one of three states. If the clock frequency is greater than the oscillation frequency, then the charge-pump is commanded to pump more charge into the charge-pump output capacitor  $C_{cp}$ . The charge-pump is made to pump out charge from the output capacitor under the opposite condition. If the clock frequency is equal to the oscillation frequency, the PFD asks the charge-pump to do nothing. Please refer to [43] for more details on the three states.

## 6.4.5 Charge Pump

The charge-pump employed for the converter is shown in Figure 6-18. Transistors M1 and M2 serve as the current source that gets activated when the DOWN pulse is active, while transistors M3 and M4 serve to provide current into the charge-pump output when the UP pulse is active. The bias circuit supplies the voltages at the gates of these transistors.

The additional transistors M5-M8 as well as the logic gates are employed to activate or deactivate the current sources. Consider the lower current source. When Pd is low, M6 is on and M5 is off. M6 pulls the source of transistor M2 to a level near the positive power-supply minus the threshold of M6. Thus M2 is turned off, and the current flow is diverted to M6 instead. As soon as Pd goes to logic high, M6 is turned off; a narrow voltage spike is exerted on M5 to rapidly reduce the voltage on the source of M2. Then the current starts to flow through M2.

Another way of deactivating the current-sources is by disconnecting the gate of transistor M2 from the bias circuit and instead connecting it to ground. This approach, unfortunately, does not work due to the fact that because the current flowing through the bias transistors (as well as the current sources) is very low, the bias circuit requires some time to pull back the gate of M2 to its original level when the source is activated. The current level in the charge-pump is kept low in order to save power.

Charge sharing between internal current-source nodes and the charge-pump output is a pervasive problem in charge-pumps. Consider the state when the PLL is in locked condition. Voltage drift will cause the charge-pump output to change slightly. This will cause either of the current-sources to get activated. Each time this happens, the internal nodes of the current sources share charge with the Ccp causing an error voltage on Ccp. Thereafter, the action of the PLL serves to bring back the output to its original level. This phenomenon leads to high frequency noise on the output. Charge-sharing has been minimized in this implementation by appropriate sizing.

The passive components used in conjunction with the charge-pump are placed off-chip because of the size of these components.

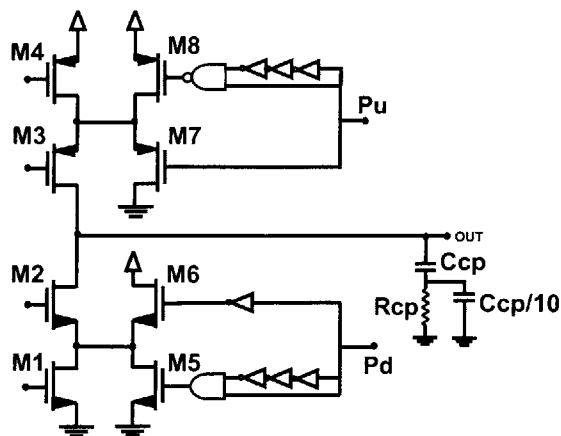


Figure 6-18: Charge-pump.

## 6.4.6 Voltage-Current Converter

Transistors M1 and M2 in Figure 6-19 shows the voltage-to-current converter. A single transistor M1 is employed to convert the voltage applied at its gate to a current. The cascode transistor is employed to maintain the voltage at the drain of transistor M1 nearly constant. In many PLL implementations, a linear voltage-to-current converter is employed for purposes of maintaining a constant forward loop gain in the PLL. However, due to the wide range of clock frequency over which the PLL is supposed to operate, such a linear converter would not work.

While transistors M1 and M2 provide current to the VCO opamps and PLL comparator, transistors M3 and M4 provide an identical current to a set of current mirrors that eventually scale and route the currents to the appropriate opamps in the converter. An external RC filter is employed to remove the high-frequency noise from the charge-pump output in order to prevent the bias currents of the converter opamps from being modulated by this noise. Special precaution was taken in order to minimize the noise coupling into the sensitive gate of transistor M3. For this reason, the routing involved for the off-chip RC filter is kept to a minimum.

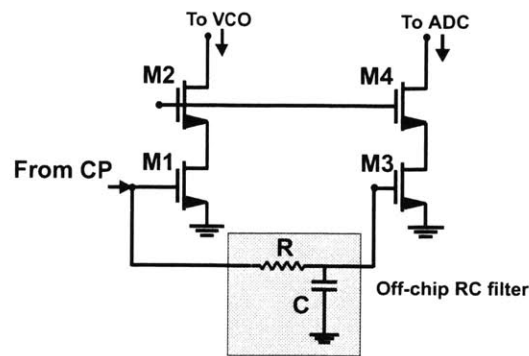


Figure 6-19: Voltage-to-current converter.

## 6.5 PLL Dynamics

This section describes the loop dynamics of the phase-locked loop employed here and determines the relationship between various loop parameters to the clock frequency supplied to the converter. Since the converter is meant to be operated over a wide operating range, care is necessary to ensure that the loop remains stable over this range.

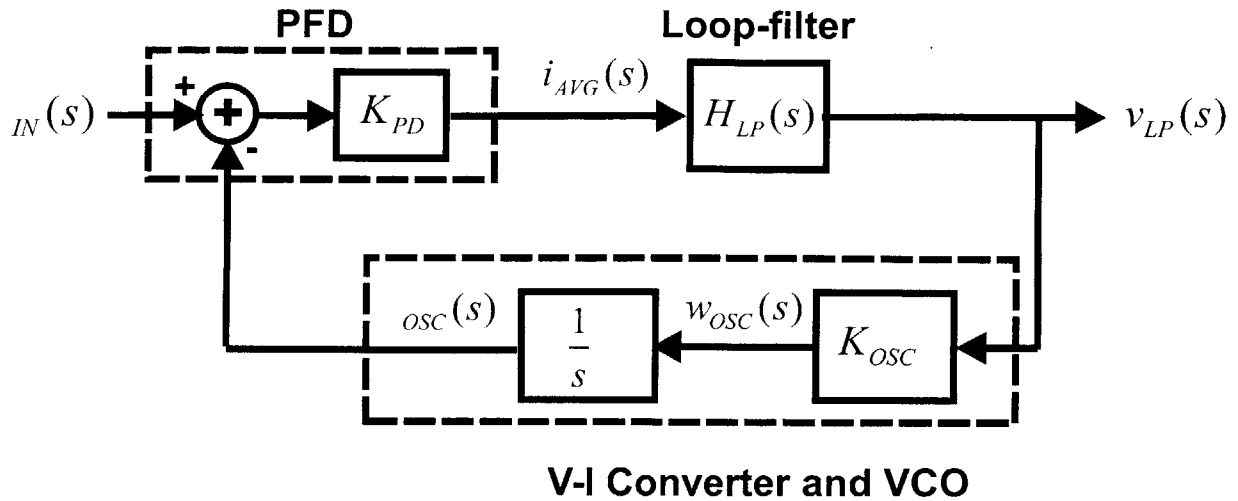


Figure 6-20: Model of the PLL for obtaining information about the loop dynamics.

Figure 6-20 shows the model of the phase-locked loop. To keep this model consistent with the circuit, the various blocks in this model are associated with the following dimensions. The phase-frequency-detector (PFD) has a phase input and current as its output and gain of  $K_{PD}$ . The low-pass filter has a gain of  $H_{LP}(s)$  with current input and voltage output.  $\frac{K_{OSC}}{s}$  is the transfer function through the voltage-to-current converter and the voltage-controlled oscillator with voltage input and phase output. After routine analysis, the overall PLL relationship is found to be:

$$\frac{V_{LP}(s)}{\phi_{IN}(s)} = \frac{sK_{PD}H_{LP}(s)}{s + K_{OSC}K_{PD}H_{LP}(s)} \quad (6.18)$$

$$\frac{V_{LP}(s)}{\omega_{IN}(s)} = \frac{K_{PD}H_{LP}(s)}{s + K_{OSC}K_{PD}H_{LP}(s)} \quad (6.19)$$

where, equation (6.18) shows the relationship assuming a phase input while equation (6.19) shows the overall transfer function with frequency input.

Each of the parameters  $K_{PD}$ ,  $H_{LP}(s)$  and  $K_{OSC}$  will now be determined and substituted back into the above relationships.

For a standard tri-state charge-pump phase-frequency detector,  $K_{PD}$  can be easily determined to be [10]:

$$K_{PD} = \frac{I_{CP}}{2\pi} \quad (6.20)$$

where,  $I_{CP}$  is the current flowing through the charge-pump.

For the low-pass filter employed (shown in Figure 6-18), the average input current to output voltage transfer function is:

$$H_{LP}(s) = \frac{v_{LP}(s)}{I_{AVG}(s)} = R_{CP} + \frac{1}{sC_{CP}} = \frac{1 + sR_{CP}C_{CP}}{sC_{CP}} \quad (6.21)$$

Here the second capacitor  $C_{CP}/10$  has been ignored for simplicity since its inclusion does not change the overall relationship much.

The estimation of  $K_{OSC}$  is more involved. It consists of two parts – the  $\frac{I_{BIAS}(s)}{v_{LP}(s)}$  due to the voltage-to-

current converter and  $\frac{w_{VCO}(s)}{I_{BIAS}(s)}$  due to the VCO. Here  $I_{BIAS}$  is the bias current that is generated by the V-I

converter and fed to the opamps in the VCO. Based on Figure 6-19, the transfer function of the V-I converter is simply the transconductance of the transistor that converts the voltage to current. For simplicity, we limit our analysis to the case when this transistor is in the sub-threshold regime. This is a fair assumption because we will find that stability of the PLL becomes an issue only at very low clock

frequencies where the transistor is in the sub-threshold regime. Thus  $\frac{I_{BIAS}(s)}{v_{LP}(s)} = \frac{I_{BIAS}}{kT/q}$ .

The  $\frac{w_{VCO}(s)}{I_{BIAS}(s)}$  transfer function in the VCO can be determined as follows. We know that the oscillation

frequency of the VCO,  $w_{OSC} = K_{RATIO} \frac{gm}{C_{VCO}} = K_{RATIO} \frac{qI_{BIAS}}{kT \cdot C_{VCO}}$ , where  $K_{RATIO}$  is the ratio between the

oscillation frequency and unity-gain frequency that was theoretically estimated to be  $\frac{\sqrt{3}}{2}$ . When  $I_{BIAS}$

varies by  $\Delta I_{BIAS}$ , the oscillation frequency varies by  $\Delta w_{OSC}$ , where:

$$w_{OSC} + \Delta w_{OSC} = K_{RATIO} \frac{q(I_{BIAS} + \Delta I_{BIAS})}{kT \cdot C_{VCO}} \quad (6.22)$$

$$\Delta w_{OSC} = K_{RATIO} \frac{q}{kT \cdot C_{VCO}} (\Delta I_{BIAS}) \quad (6.23)$$

Thus the small-signal transfer function  $\frac{w_{VCO}(s)}{I_{BIAS}(s)} = K_{RATIO} \frac{q}{kT \cdot C_{VCO}}$ .

Combining the transfer functions of the V-I converter and that of the VCO,

$$\frac{w_{VCO}(s)}{v_{LP}(s)} = \frac{I_{BIAS}(s)}{v_{LP}(s)} \times \frac{w_{VCO}(s)}{I_{BIAS}(s)} = \frac{qI_{BIAS}}{kT} \times K_{RATIO} \frac{q}{kT \cdot C_{VCO}} \quad (6.24)$$

After some rearrangement, we obtain a simple expression for  $K_{OSC}$ :

$$K_{OSC} = \frac{w_{VCO}(s)}{v_{LP}(s)} = \frac{q}{kT} \cdot w_{VCO} \quad (6.25)$$

Substituting equation (6.21) into equation (6.18), we obtain:

$$\frac{V_{LP}(s)}{\phi_{IN}(s)} = \frac{sK_{PD} \left( \frac{1+sR_{CP}C_{CP}}{sC_{CP}} \right)}{s + K_{OSC}K_{PD} \left( \frac{1+sR_{CP}C_{CP}}{sC_{CP}} \right)} \quad (6.26)$$

or,

$$\frac{V_{LP}(s)}{\phi_{IN}(s)} = \frac{1}{K_{OSC}} \frac{s(1+sR_{CP}C_{CP})}{1+sR_{CP}C_{CP} + s^2 \left( \frac{C_{CP}}{K_{OSC}K_{PD}} \right)} \quad (6.27)$$

Comparing this relationship to a general second order system with the denominator  $D(s) = 1 + \frac{s}{w_o Q} + \frac{s^2}{w_o^2}$ , where  $w_o$  is the natural frequency and  $Q$  is the quality factor of the system, we get:

$$w_o = \sqrt{\frac{K_{PD}K_{OSC}}{C_{CP}}} \quad (6.28)$$

$$Q = \frac{1}{R_{CP}C_{CP}w_o} = \frac{1}{R_{CP}\sqrt{C_{CP}K_{PD}K_{OSC}}}$$

Substituting equations (6.20), (6.25) into the above expressions:

$$w_o = \sqrt{\frac{I_{CP}}{2\pi} \frac{1}{C_{CP}} \frac{qw_{OSC}}{kT}} = \sqrt{\frac{I_{CP}}{C_{CP}} \frac{q}{kT} f_{CLK}} \quad (6.29)$$

$$Q = \frac{1}{R_{CP}C_{CP}w_o} = \frac{1}{R_{CP}} \sqrt{\frac{kT}{qC_{CP}I_{CP}f_{CLK}}}$$

From the above, it is observed that the quality factor of the system continues to increase as  $f_{CLK}$  is reduced. The lowest clock frequency that the PLL can work at is that frequency at which the system becomes unstable. As a reference point, at  $Q = 1/2$ , the system is critically damped.  $I_{CP}$  is chosen in order to ensure that the power consumption of the overall converter is never dominated by the charge-pump through the entire clock frequency range.  $C_{CP}$  is then chosen to fix the lower frequency bound. At higher clock frequencies, the PLL automatically remains stable, albeit, becomes possibly over-damped. In this design the quality factor is set to be  $1/4$  for  $f_{CLK} = 100\text{KHz}$ . With  $I_{CP} = 10\mu\text{A}$  and the above low-

frequency bound condition,  $C_{CP} = 470nF$  and  $R_{CP} = 851\Omega$ . Another way of looking at stability variation over varying clock frequency is determining the number of clock cycles corresponding to one time constant of the phase-locked loop. The time constant of the PLL is:

$$\tau = \frac{1}{\omega_o} \quad (6.30)$$

With the above component selection, the number of clock cycles corresponding to one time constant of the PLL is 10 at  $f_{CLK} = 100KHz$ . Below this clock frequency, this number continues to drop. Since  $C_{CP}$ ,  $R_{CP}$  and  $I_{CP}$  are determined off-chip, it is always possible to modify them in order to change the lower clock frequency bound for the PLL. While  $I_{CP}$  remains fixed in this design, it is possible to tune this as well to extend the locking range even further.

The total capture time of the PLL is dominated by the slewing at the output of the charge-pump. The slew rate is  $I_{CP}/C_{CP}$ . For the entire desired locking range (20KHz to 40MHz), it is found that the voltage at the output is required to slew from a minimum of 0.4V to 1.2V. For the above numbers, the worst case slewing time is 38ms. It is possible to reduce the locking range and speed up the PLL. To ensure start-up, the charge-pump output is initialized to 0.4V. This ensures that at least some current flows through the VCO opamps at start-up.

## 6.6 Summary

This chapter begins with the role of the PLL in the reconfigurable converter, as well as the concept behind bandwidth reconfiguration using a PLL. The theory behind the 3-opamp cascaded VCO is discussed next. Other oscillators are also described to provide a comparison between the proposed oscillator and existing solutions. The circuits of the various components of the PLL such as the VCO, comparator, the phase-frequency-detector, charge-pump and voltage-to-current converter are presented next. Finally, the dynamics of the PLL is discussed with a focus on how the loop dynamics change with varying clock frequency.





# 7 Test System and Experimental Characterization

## 7.1 Introduction

This chapter describes the conceptual and physical layout of the prototyping circuits placed on the test board, general information on the various tests employed for testing this converter, the experimental results of the converter in the pipeline and delta-sigma modes as well as the phase-locked-loop, comparison of the converter performance with custom-built converters and finally, envisioned future improvements for the test system.

## 7.2 Test and Characterization System

A printed circuit board in conjunction with a Pentium III PC, National Instruments Data Communication boards and software (Labview) was employed to test the prototype of the reconfigurable converter. A conceptual diagram of the test system used to test the chip is shown in Figure 7-1. The figure shows the various parts of the system along with specific details on these parts.

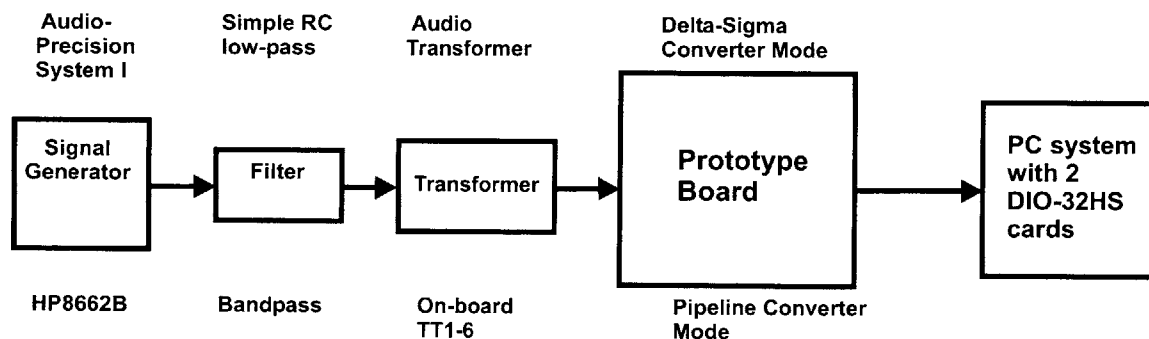


Figure 7-1: Test setup. The component description above the blocks correspond to the delta-sigma mode, while those below the blocks correspond to the pipeline mode.

### 7.2.1 Printed Circuit Layout

The printed circuit board has been fabricated as a 6-layer system. The detailed description of the physical planes can be found on the silkscreen of these planes from [14]. While the 1<sup>st</sup> (top) and 6<sup>th</sup> (bottom) layers are employed to route the various nets connecting the components on the board, the inner layers are used to route the power supplies. The 2<sup>nd</sup> layer consists of the ground signal; this layer, however, is split into several sections for the purpose of isolating noisy parts from the quiet parts.

The 3<sup>rd</sup> layer primarily consists of the signal OUTHI that serves as the positive power supply (nominally 0.3V above the common-mode level) for the on-chip output drivers. In addition, it also contains certain routing signals that could not go on the 1<sup>st</sup> and 6<sup>th</sup> layers.

The 4<sup>th</sup> layer contains 3 power supply signals:

OUTLOW: the lower power supply for the on-chip output drivers (nominally 0.3V below the common-mode level).

BVDD: the positive power supply for the on-chip clock generator module. Nominally, this is at a boosted level of 4.6V in order to hard-drive the switches in the switch-capacitor circuitry.

AVEE: The negative power supply for the on-board opamps used to generate the reference, bias voltages and bias currents. This is nominally equal to  $-1V$  in order to maximize the swing of these amplifiers.

The 5<sup>th</sup> layer contains the following positive power supplies:

- DVDD: positive supply for all the non-clocking on-chip digital circuit
- AVDD: positive supply for all the analog parts of the chip
- AVDD2: positive supply for the PLL within the chip
- AVDD3: positive supply for analog parts of the board
- BRDVDD: positive supply for line-receivers and FIFO
- NBRDVDD: positive supply for the bus-transceivers.

## 7.2.2 Prototyping Circuits and Considerations

The circuits for the prototyping board can be classified in the various following categories. More information on converter prototyping circuits can also be obtained for a wide selection of data-sheets and application notes on commercial converters. These have been listed in the Bibliography.

### Converter Input Interface

The input circuit (shown in Figure 7-2) has been constructed to maximize the flexibility for testing the 2 modes of the converter. The PCB has 2 input paths, one via an on-board transformer (for high frequency testing in the pipeline mode) and another that bypasses the transformer for low frequency testing primarily for the delta-sigma mode. Common to both paths is the option of adding a cascade of either RC type low-pass filters or RC high-pass filters, primarily for the purpose of anti-aliasing. These components can be either soldered in or not soldered at all. The flexibility of this path essentially stems from the addition of small “solder-jumpers”, jumpers that can be soldered in to make connection and de-soldered to break connection. These solder jumpers have been used extensively in other places as well to make a flexible prototyping network.

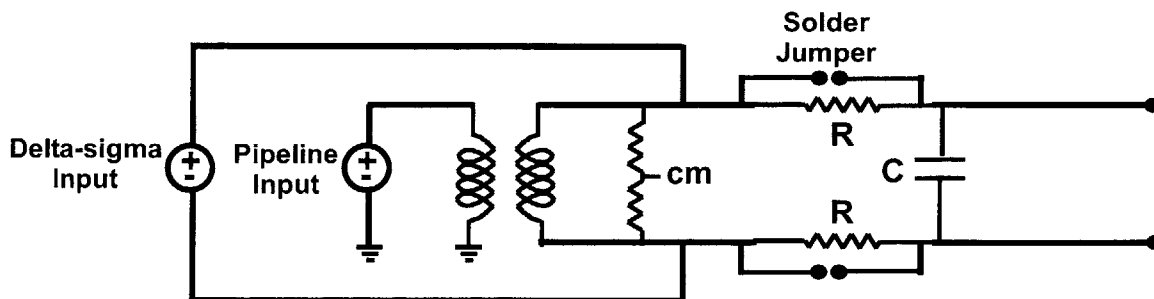


Figure 7-2: Input structure on the prototype board.

### Signal Source

The input of this test is typically provided by the sine wave generator converter (the audio precision system I for audio range signals and an RF generator (HP8656 and HP8662) for higher frequencies) to a

differential format using a transformer. The transformers employed were: an on-board Mini-circuits TT1-6 for frequencies higher than 200KHz and Jensen line transformer JT-11SSP-6M for a frequency range of 20Hz-20KHz. The Jensen transformer is rated for <100dB distortion through this frequency range and was thus employed for delta-sigma-mode in conjunction with the audio precision System I as the signal source.

While the primary purpose of the transformer is to create a differential signal, an additional advantage is that it eliminates or minimizes the ground interaction between the signal generator and the test board. This transformer eliminates the ground loop involving the input and helps improve the signal-to-noise ratio of the obtained signal. The common-mode level of the differential signal from the transformer can be set by setting the DC level of the center tap of the secondary coil of this transformer; however, it is far better to employ two resistors in series across the secondary coil, and apply the common-mode voltage at the center of the two resistors. This is because the center tap of the transformer is invariably not precisely located leading to an unbalanced signal [59]. The resistors in the preferred solution should, of course, be handpicked for good matching. An unbalanced signal, if added, can cause even order distortion in the signal.

### **Front End Filtering Considerations**

To improve input distortion, the input is also typically filtered using a band-pass filter (manufactured by TTE and Allen Avionics). Since these filters normally work on single-ended signals, this device is placed just before the transformer. Filters at various center frequencies were employed to obtain the signal for the pipeline mode operation. For the delta-sigma mode, on the other hand a simple RC anti-alias filter was employed to remove high frequency spurs due to external interference. It is important to remove these spurs because they can alias back to the signal-band and reduce the SNR.

The performance of the converter especially in the delta-sigma mode was severely impacted due to external interference. A more detailed observation of the effect of this interference as well as solutions to minimize its effect are described in Appendix D.

### **Reference and Bias Voltage Circuits:**

Three reference voltages are provided to the converter: VREFP and VREFN used in the pipeline mode and VREFSD used in the delta-sigma mode. In addition, bias voltages are required to create QCMO (the common-mode voltage level of the input), CMO (the common-mode voltage level of the opamp outputs) and CCMI (the Comparator Common-mode Inputs used to provide the common mode level to the latches in the converter. All of these have been constructed using opamps (SSM2135), passive components and a zener voltage source (AD1580). A single Bias voltage Generation circuit is shown in Figure 7-3.

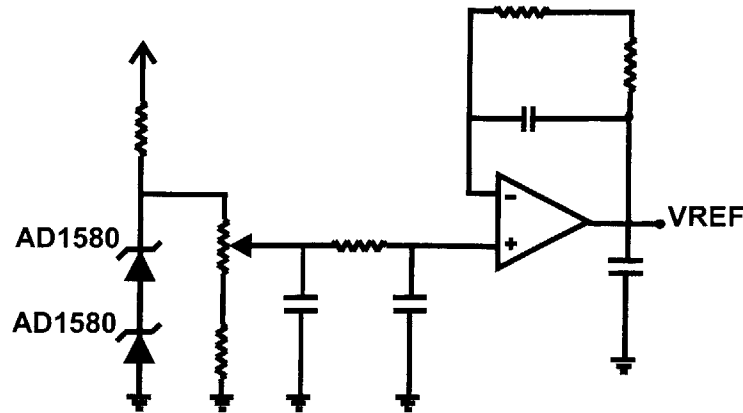


Figure 7-3: Voltage bias circuit.

The bias currents for the converter opamps (when the PLL is deactivated) as well as the currents fed to the charge-pump are supplied from the board. These are created using opamps (OP493), passive components and bipolar transistors (MMBT2484LT1). One such bias current generator is shown in Figure 7-4.

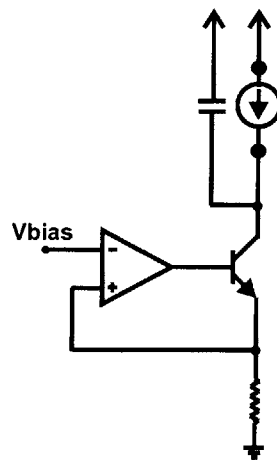


Figure 7-4: Current bias circuit.

#### PLL Control Circuit:

As mentioned earlier in this work, the output of the on-chip charge pump is not connected directly to the Voltage-to-Current Converter going to the converter. The output of the charge pump is RC filtered before it is connected to the converter V-I generator to remove the high-frequency ripples that is commonly found at the charge-pump output. This RC filtering is done off-chip on the prototyping board.

Additionally the charge-pump output needs to be initialized at start-up. This is done using an on-board analog switch (CD4066BC) that connects this node to an analog voltage (typically 0.2-0.4V)

#### Clock Generator Module:

The clock for the converter is obtained from a sine-wave generator (any low-jitter RF synthesizer). This sine wave is fed through a transformer for noise reduction purposes. The transformer output is fed to a differential line receiver (DS90LV048A) that converts the sine wave into a clock waveform. In the actual circuit, three line-receivers (within the same package) are employed in parallel to create 3 different clock waveforms, one for the converter, one for the PLL and the other is fed, optionally, to the FIFO that stores

the data from the converter. The outputs of the line receiver are appropriately terminated to preserve the integrity of the clock edges.

#### **On-board Digital Acquisition:**

The 16 outputs of the converter are fed along with a clock signal (generated on-chip in order to synchronize the clocking of the digital chips following the converter to the digital data) to line receivers (DS90LV048A) that essentially convert the small-swing signal (nominally  $-0.3\text{V}$  to  $0.3\text{V}$  about a reference level) at the output of the converter into large-signal digital waveforms. The reference signal is created using a resistor divider from the OUTHI and OUTLOW signals that serve as the power supplies of the on-chip digital drivers.

The output of these line receivers is sent to a 262Kx18 FIFO (IDT72V2105) that stores all the outputs in parallel registers for sequences as long as 262K.

#### **PCB-PC Interface:**

The On-board interface to the PC is achieved by employing bus-transceivers (MC74LCX245) that have the capacity to drive large capacitive loads of a long bus. Each path through these chips can be configured as either receivers or transmitters, and hence can be used for either retrieving data from the FIFO into the PC or for controlling the board from the PC, respectively.

Two 68pin SCSI ports are used to serve as the mechanical/electrical interface to the PC.

On the PC itself, 2 National Instruments DIO-32HS cards are inserted into the expansion slots to serve for the data acquisition and control of the board. Labview, a National-Instrument Software, in turn controls these boards.

### **7.2.3 Prototyping Software**

Labview, a software package from National Instruments was employed for acquiring and managing all the data obtained from the test board. This software interfaces with the 2 National Instruments boards (6533 DIO-32HS) and can be easily programmed using graphical means. A full description of this software can be found in the Labview User Manual.

Labview was employed for acquiring data and storing into appropriately formatted text files. MATLAB was then employed to process the data and obtain the time-domain, frequency-domain FFT and the INL/DNL plots. It was also used to determine the SNR, SNDR, THD, and the various harmonic distortions.

## 7.3 Test and Characterization Experiments

Testing and characterization of the various converter specifications as well as debugging of converter performance typically involves acquiring converter data in many different ways. The following are methods that have been employed to test the reconfigurable converter. A brief description of the process and the limitations of the method is also included. Most of these have traditionally been employed to obtain the linearity and noise measures of the converter.

### 7.3.1 Histogram Code Density Test

The primary purpose of this test [57] is to provide a measurement of the linearity of the converter. The sine wave code density histogram method is very popular owing to its speed, ease and availability of low-distortion single tone generators. In this test, the output codes of the converter in response to a pure sine wave at the input are collected and plotted as a histogram. The histogram bins correspond to the various output codes. The measured histogram is then compared to the probability distribution function of an ideal sine wave to generate the differential and integral non-linearity of the converter. Further details of this method can be obtained from [57].

For a valid non-linearity measurement, it is important to ensure that an integer number of sine wave periods are included in the data under consideration. In addition, in order to ensure a high degree of confidence in the measurement, a large number of samples need to be obtained [57]. If the local on-board memory is not sufficiently large to provide the desired data length, it is also possible to obtain several shorter data lengths, create the histogram for each data set separately and then combine them to synthesize a histogram for an effectively much larger set of data.

**Limitations of the sine wave histogram code density test:** Noise in the converter can lead to random shifts in the converter decision levels and blur sharp INL changes in the code density across the histogram bins. This, in turn, leads to a DNL measurement that is better than the actual DNL of the converter. Hence more stress is normally paid on the INL measurement. However, the INL measurement is valid only for converters with monotonic transfer characteristics. This converter employs a 1.5bit/stage digital error correction and can, under certain conditions, be non-monotonic.

### 7.3.2 Zero-input Test

This test provides us with a measurement of the static offset and static noise level of the converter. For this test, the inputs of the converter are shorted and a histogram test is done. The output codes typically span 2-4 code levels with a normal distribution because of the thermal noise associated with the converter. The distance between the mean of this distribution and the mid-code is of course the offset, while the standard deviation of codes is representative of the converter noise.

### 7.3.3 FFT Test

The primary purpose of this test is to obtain the SNR, SNDR and SFDR of the converter. While the INL and DNL tests described earlier offers an insight into the linearity of the converter, it does not provide a measure of the signal-to-noise ratio of the system. In fact a large amount of noise in the converter can result in better-than-actual differential non-linearity. On the other hand, distortion in the converter can cause several higher order harmonics that can alias back and spread over a large number of bins and can lead to a misleadingly low SNR. In this case, care is necessary to ensure that these higher order harmonics are not considered during SNR computation. Appendix C discusses the location of these higher order harmonics in detail.

This test essentially entails running an N point FFT on the sequence of the analog equivalent of the digital output. Some primary issues related to this test include the types of window employed, the relationship between the clock frequency and input frequency, the number of sine wave periods contained in the data record used for the FFT, synchronization of the input and clock among others. All of these issues dramatically affect the overall integrity of the test. The Hanning window provided by MATLAB V5 works reasonably well for the converter FFT test. A detailed analysis of these various issues are described in the Appendix C.

### **7.3.4 Envelope Test**

Given the limitations of the sine wave code density test, it may be useful, under certain conditions, to obtain a time-domain perspective of the converter output [12]. Any non-linearity masked by the noise or non-monotonicity of the converter will become evident with the time domain. However, unless the input is at a frequency much lower than the clock frequency, the output does not bear any resemblance to a sine function. Providing such a low frequency input may require changes in signal generator, input filter as well as the input transformer. Additionally operating the converter at low input frequencies may in itself mask converter non-linearity.

In the envelope test [12], the input frequency is set to be very slightly lower than the clock frequency. The resulting output wave shape will then be at a frequency equal to the difference between the two frequencies. This difference can be made arbitrarily small.

### **7.3.5 Signature Analysis**

Various non-linearity errors in a pipeline type architecture result in certain signature patterns in the output code histogram. The idea here is to compare the measured histogram with previously catalogued error patterns. The input for this analysis can be a pure sine wave. In order to make the error patterns more visible and hence make the task of comparing histograms easier, the measured histogram can be normalized to a uniform distribution across all the bins, in other words to a histogram that would be obtained had we applied a ramp waveform at the converter input.

This technique is applicable to non-monotonic converters, and hence can be effectively employed for debugging purposes. More details on this debugging method can be found in Appendix B.

## **7.4 Experimental Results**

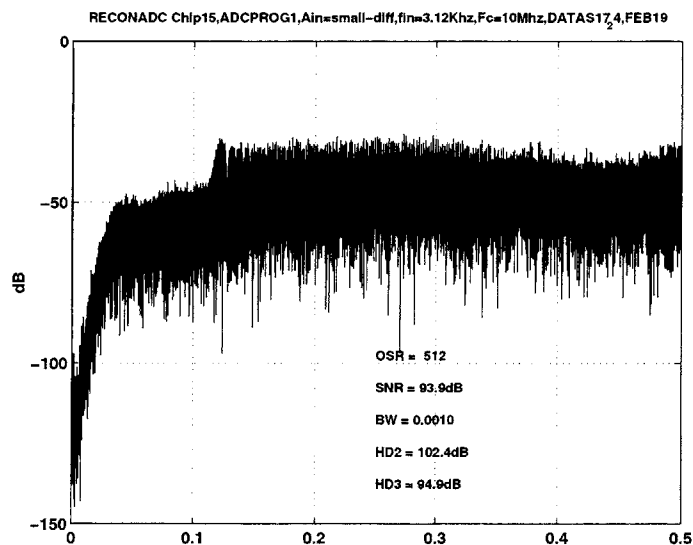
The following section presents the measured results of the converter. Since the converter works at a variety of frequencies and resolutions several different front-end peripheral devices such as transformers, signal generators and filters are employed. These have been detailed wherever relevant. Sections 7.4.1 and 7.4.2 describe the results from the converter core while Section 7.4.3 describes measurements from the PLL.

### **7.4.1 Delta-Sigma Mode**

The delta-sigma mode in the reconfigurable converter is designed to cover a bandwidth from 0-1MHz and deliver resolutions ranging from 12 bits to 16 bits. As mentioned earlier, the SNR variation in this mode is achieved by varying the oversampling ratio of the converter. The opamp speed is adjusted to varying clock speed using the PLL method described earlier.

#### **Delta-Sigma Mode FFT Test**

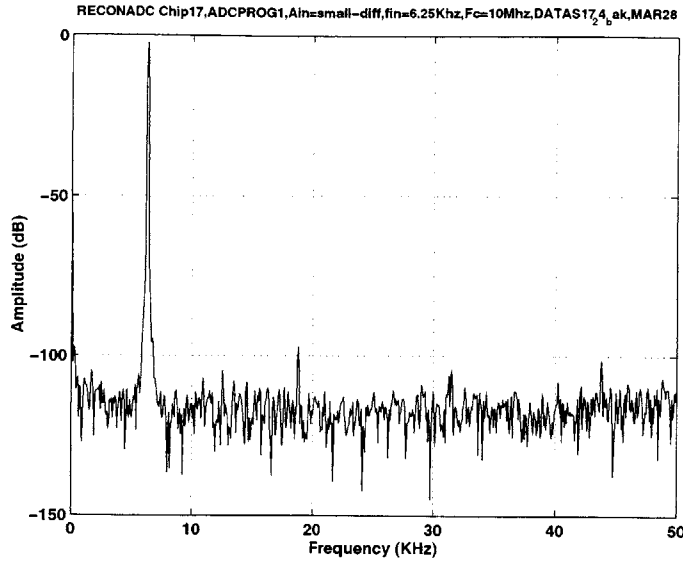
Figure 7-5 shows the measured FFT of the converter output for a sample performance point of the reconfigurable converter. The x-axis in Figure 7-5a ranges from 0 to 0.5fs. In this case, at a clock frequency of 10MHz and an oversampling ratio of 512 (input at 6.25KHz which is 2/3rds of the total band), the converter possesses a SNR of 93.9dB. The second harmonic and third harmonics are 102.4dB and 95dB below the signal. The spikes seen outside the baseband in Figure 7-5a at around 0.12fs are related to the signal strength relative to the reference range and hence corresponds to 'converter tones'. Interestingly, the location of this spike is highly correlated to the signal strength.<sup>2</sup> Nevertheless, any noise outside of the baseband does not affect the performance of the converter. Figure 7-5c shows a clearer picture of the quantization noise shape.



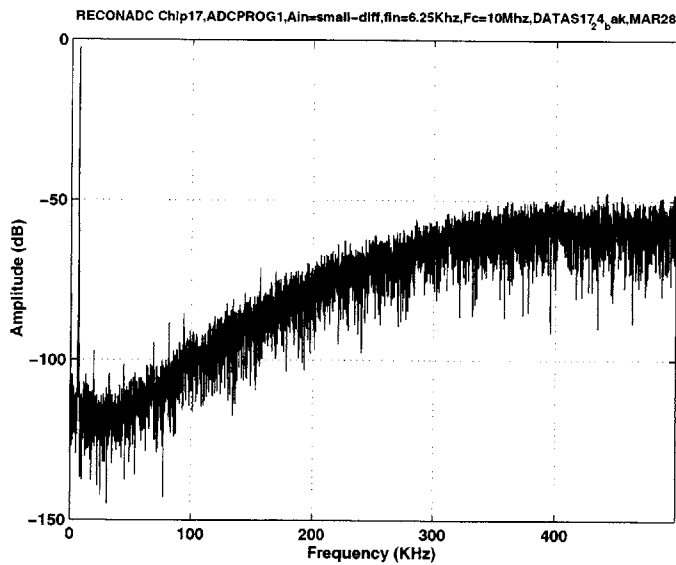
(a)

<sup>2</sup> The location of these spikes were found to be dependent on the signal amplitude referenced to the reference applied to the converter. Interestingly, the left most edge of the onset of these tones can be modeled by the following expression:  $\frac{(V_{ref} - V_{amp})}{V_{ref}} \cdot \frac{f_s}{2}$ , where  $V_{ref}$  is the half of the full-scale of the converter input,  $V_{amp}$  is the amplitude of the input tone and  $f_s$  is the sampling frequency. This expression holds true for most signal amplitudes.





(b)



(c)

Figure 7-5: Converter performance in delta-sigma mode with a clock frequency of 10MHz and oversampling ratio of 512.

### Delta-Sigma Mode Performance at Varying Resolution

Figure 7-6 shows the relationship between the analog power consumption and the SNR of the converter at varying oversampling ratio. Here the input tone is held constant at 6.25KHz and the clock frequency is varied. It is evident from this plot that there is a trade-off between power and SNR. It is this trade-off that the reconfigurable converter exploits.

As the oversampling ratio of the converter is varied, different noise sources dominate the performance obtained from the delta-sigma mode converter. The delta-sigma mode reuses the capacitors from the pipeline mode that is designed for a maximum of 12-bits of SNR. However, for stability reasons, the input of the converter in the delta-sigma mode can be at a maximum of one-half the reference range. This implies that for at an OSR of 32, the converter would possess 13.5-bits of SNR considering only thermal noise. At this oversampling ratio, the modulator would have in-band quantization noise that is roughly equal to the thermal noise. Thus, when the oversampling ratio is below 32, the converter is strongly quantization noise limited. In this regime, the SNR of the converter would change by 27dB for every factor of 2x change in OSR. For oversampling ratios in the range of 32 and about 256, the converter is influenced by both quantization noise as well as thermal noise. In this case, the SNR improves by a value between 3dB and 27dB per octave change in OSR. Oversampling ratios greater than 256 cause the delta-sigma to be strongly thermal noise limited. In this case, the SNR improves only by 3dB with doubling of the OSR. As the OSR is increased beyond 1024 (not shown here), the converter becomes 1/f noise limited. In this case, the SNR improves by less than 3dB as the OSR is doubled. In this regime, activating the opamp chopping circuit would make significant difference. In all three regimes, the converter performance as measured in the lab is constrained by interference noise from external sources.

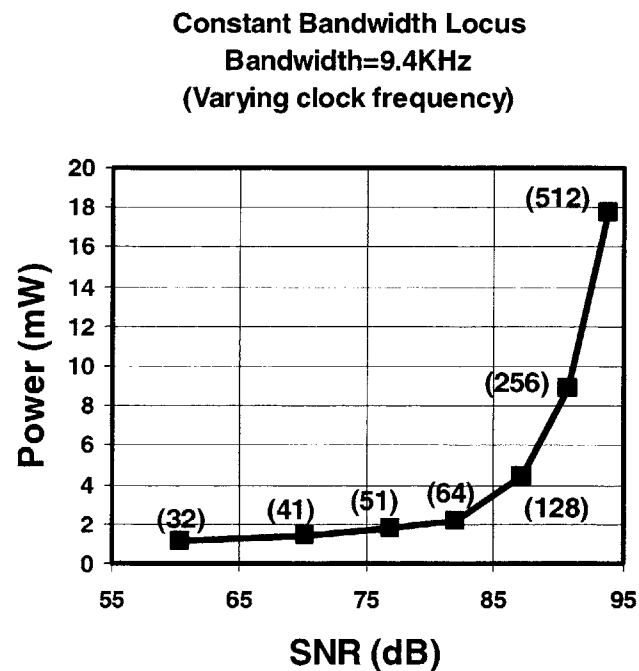


Figure 7-6: Measured variation of analog power with varying signal-to-noise ratio for changing oversampling ratio (shown in parenthesis).

### Delta-Sigma Mode Performance at Varying Bandwidth with Constant Clock Frequency

Figure 7-7 shows the relationship between the SNR as the input bandwidth is increased at a fixed clock frequency. Since the clock frequency is fixed, the power consumption is also fixed. Hence the curve shown is a constant power locus.

As has been derived earlier, if the converter is thermal noise limited, the SNR should vary as the negative of the logarithm of the input bandwidth or the data rate. In fact the change in SNR for every doubling of

oversampling ratio is expected to be 3dB. Between the oversampling ratios of 512 and 64, the measured curve shown below does approximate a linear segment, although the drop in SNR as a result of reduced OSR is progressively greater than can be explained just from consideration of thermal noise. Additionally for OSR variation from 64 to 32, the SNR drops nearly 18dB. The progressively larger-than-3dB drop in SNR for every doubling of OSR is completely understandable when the quantization noise of the converter is also considered. As OSR is reduced, the contribution of quantization noise to the overall noise of the converter becomes significant. When the converter is completely quantization noise limited, the expected drop in SNR for a fourth order modulator, as is the case here, is approximately 27dB. This is what is expected for even lower OSR. This point, however, could not be measured the signal generator employed (Audio Precision System I) could not produce the appropriate amplitude at the desired input frequency.

Please note that the input tone is applied at a factor 2/3rd of the edge of the band of interest in all measurements in the delta-sigma mode.

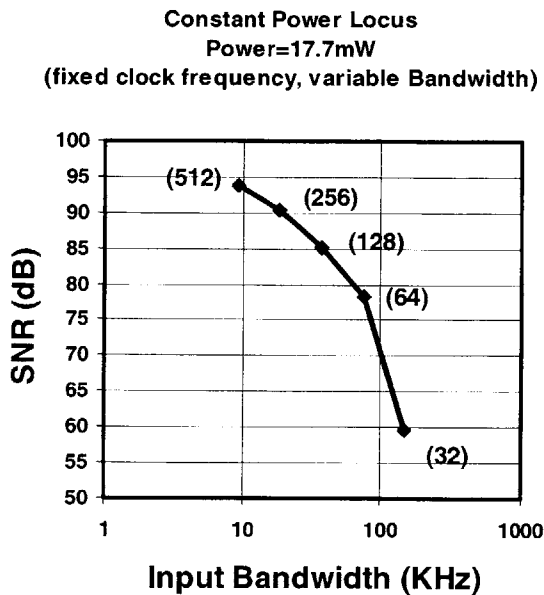


Figure 7-7: Variation of SNR with input bandwidth at fixed clock frequency. The oversampling ratio at each point is shown in parenthesis.

### Offset Correction in Delta-Sigma Mode – First Stage Opamp Chopping

As mentioned earlier, the performance of the converter is susceptible to opamp 1/f noise and offset. This is especially true for the opamp in the first block. To minimize the effect of this non-ideality, the first block opamp is chopped at  $f_s/2$  frequency in order to modulate the 1/f noise to  $f_s/2$ . Table 6 shows the effect of the opamp chopping on the converter performance. Activation of the first block opamp chopping reduces the signal strength in the first and second bins by about 16db and 18dB, respectively. For the OSR considered here (512), the overall SNR improves by 1dB, although larger improvements are possible with lower OSR.

Opamp Chopping State	1 <sup>st</sup> bin (0-76Hz)	2 <sup>nd</sup> bin (76 –152Hz)
----------------------	------------------------------	---------------------------------

<b>Disabled</b>	-49.8dB	-55.8dB
<b>Enabled</b>	-66dB	-72.5dB

Table 6: Comparison of converter performance and bin strengths with and without opamp chopping.

Figure 7-8a-b show the frequency band of interest with and without chopping.

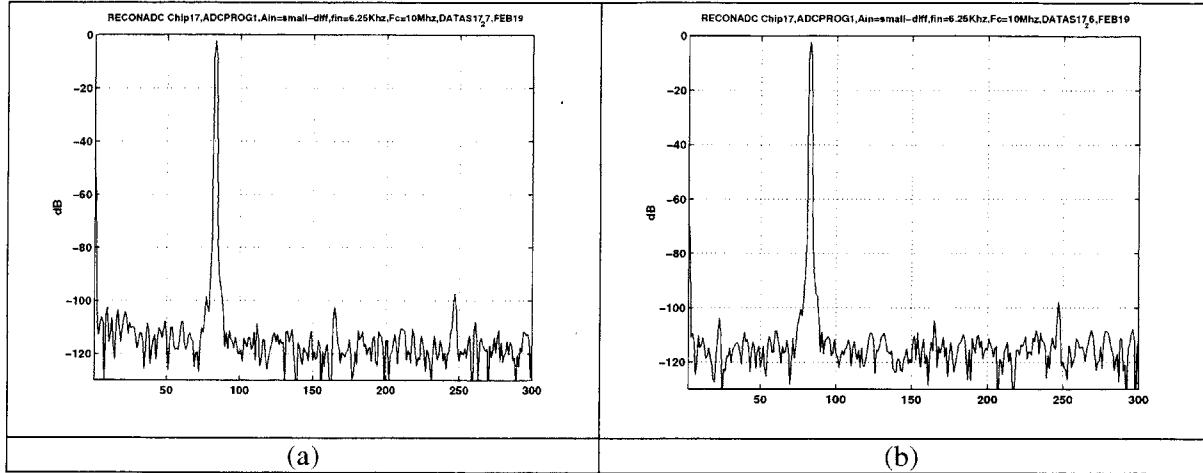


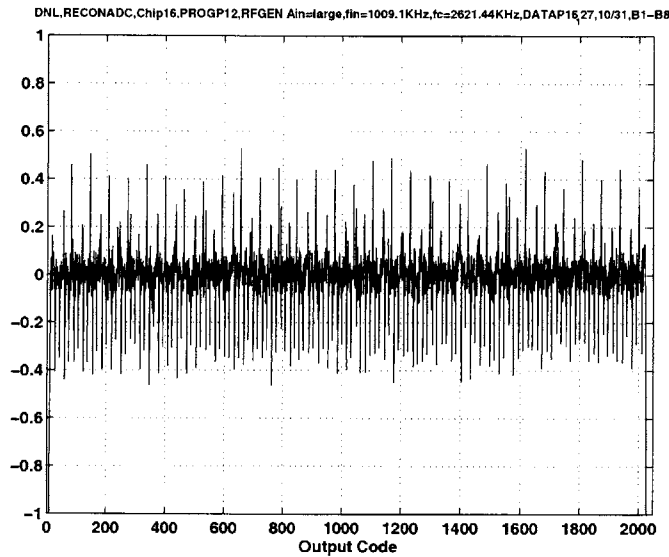
Figure 7-8: Effect of opamp chopping. (a) Opamp chopping disabled. (b) Opamp chopping enabled.

## 7.4.2 Pipeline Mode

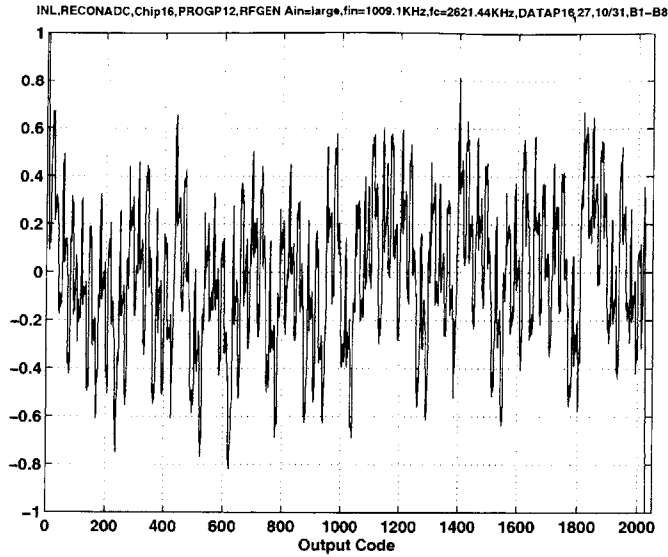
The pipeline mode is designed to work through 6-12 bits of resolution, and a clock speed of 20KHz to 20MHz. To obtain different resolutions, the architecture is placed in different configurations, as was described earlier. This section provides the measurement results of the converter at different resolution configurations as well as the performance of the global chopping concept described earlier.

### Pipeline mode Linearity Measurements

Figure 7-9a and Figure 7-9b show the DNL and INL, respectively, of converter in the 11-bit pipeline mode. At 12-bits, the measured INL and DNL exceeded  $\pm 1$  LSB due to mismatch among the small capacitors that we used. The non-linearity visible in Figure 7-9a has been determined, based on the signature analysis presented in Appendix B, to stem from stage gain-error in the 6<sup>th</sup> stage (2<sup>nd</sup> stage of the 3<sup>rd</sup> block) of the pipeline configuration. Standard digital calibration [58], which was not implemented on this chip for simplicity, would correct this problem. This would also allow us to operate the chip at higher clock and input frequencies than has been done here. Under these circumstances, the resolution of the converter degraded as clock frequency was increased. An input of 10MHz and a sampling rate of just under 10Ms/s, 8-bits of resolution was obtained.



(a)



(b)

Figure 7-9: Linearity of the converter in pipeline mode at a sample performance point. (a) Differential non-linearity. (b) Integral non-linearity.

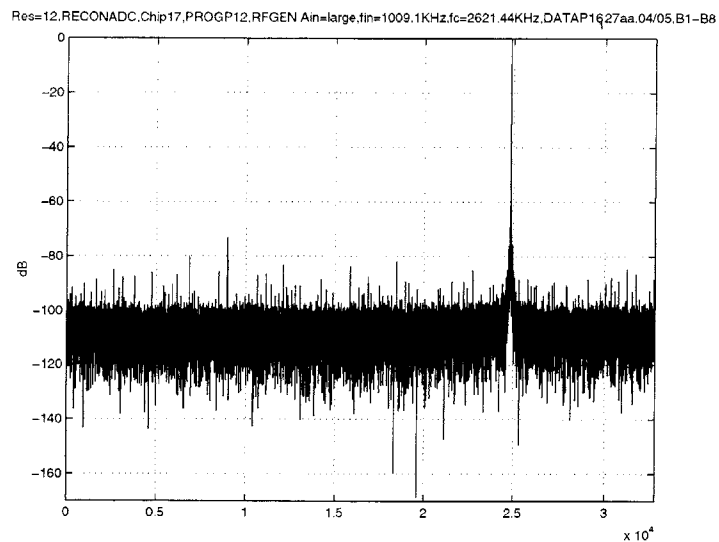


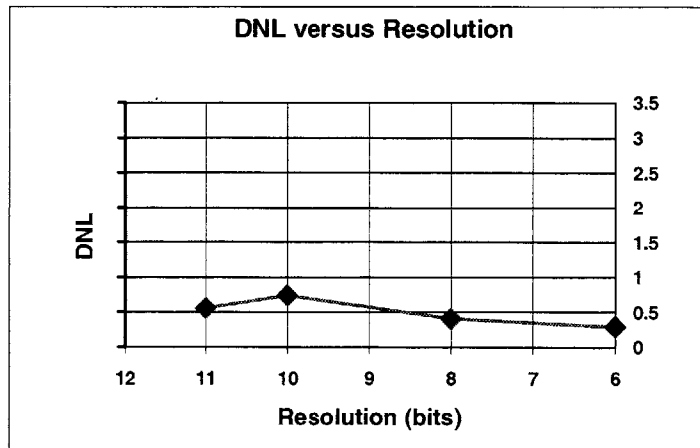
Figure 7-10: FFT of converter output data in the pipeline mode for a clock frequency of 2.62MHz and input frequency of 1MHz. The x-axis represents the bins of the FFT.

Figure 7-10 shows the FFT of the output data of the converter when it is placed in the pipeline mode. The SNR obtained is 62.5dB while the SFDR and THD are 72dB and 71dB, respectively.

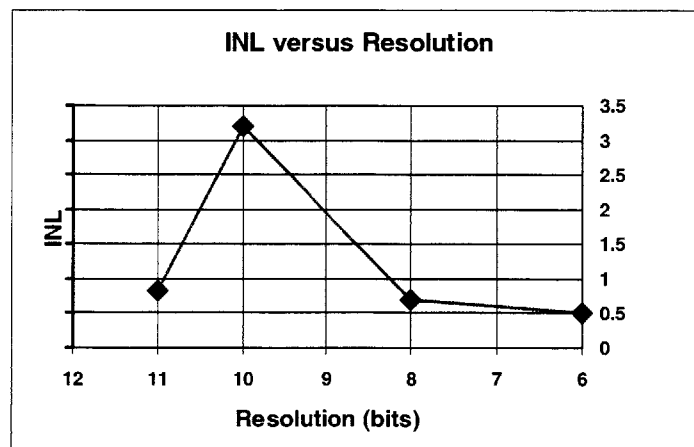
### Pipeline mode performance at varying resolution

Figure 7-11a and Figure 7-11b show the variation of the differential and integral non-linearity through the various configurations of the converter. The requisite DNL and INL specs are obtained at all resolutions except for the 10-bit mode in which the maximum INL is almost 3.2LSBs. The 11-bit resolution data in

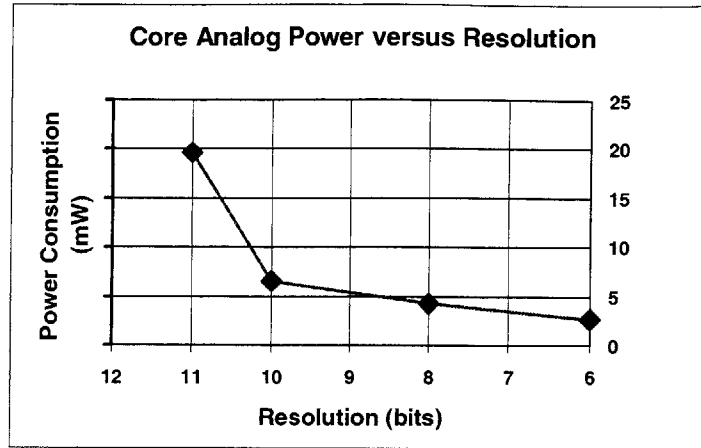
these graphs were obtained from the 12-bit mode of the reconfigurable converter since the 12-bit resolution mode did not yield 12-bit data. On the basis of the ADC results, these graphs would have 12-bit data if standard digital calibration has been employed. This was not employed for simplicity. The location, size, and type of errors obtained here again points to gain error from the 2<sup>nd</sup> stage of the 3<sup>rd</sup> reconfigurable block. For the 10-bit mode, this stage forms the 2<sup>nd</sup> stage of the pipeline. The power of the converter tracks the resolution variation. This is illustrated in Figure 7-11c. While the power of the converter drops rapidly at the high end of the resolution scale, it does not drop as quickly for the lower end of the resolution scale. This is indicative of the fact that the latter stages of the converter are parasitic capacitance dominated, and that the latter stages are not scaled as aggressively. The onset of the parasitic capacitance domination occurs especially early for this converter because of the small sized capacitors employed in its implementation.



(a)



(b)



(c)

Figure 7-11: Variation of (a) Differential and (b) Integral non-linearity, and (c) Power consumption of converter at various resolution configurations.

### Offset Correction in Pipeline Mode – Global ADC Chopping

As with the delta-sigma mode, the performance of the pipeline mode is susceptible to opamp offsets and  $1/f$  noise. As described earlier, this non-ideality can be corrected for by chopping the entire converter as a single block. The results of this scheme are encapsulated in the follow

Opamp Chopping State	1 <sup>st</sup> bin (0-80Hz)	2 <sup>nd</sup> bin (80 –160Hz)
Disabled	-41dB	-47.2dB
Enabled	-73.5dB	-79.4dB

Table 7: Effect of global ADC chopping. (a) Global chopping disabled. (b) Global chopping enabled.

### 7.4.3 PLL Measurements

The bandwidth of the operational amplifiers employed for the converter is tuned by varying the bias current flowing through the transistors in the amplifier. This is achieved using a phase-locked-loop through the method that was described earlier. This section details the various specifications commonly used to describe PLL performance.

#### PLL Tracking Range

In order to make the reconfigurable converter operate at a wide range of clock frequencies, the phase-locked loop implemented in this chip was designed to possess a wide locking range. Figure 7-12 illustrates the tracking range of the PLL. The VCO opamp bias currents track the clock frequency over 3 orders of magnitude while it is varied between: 20KHz and 40MHz.



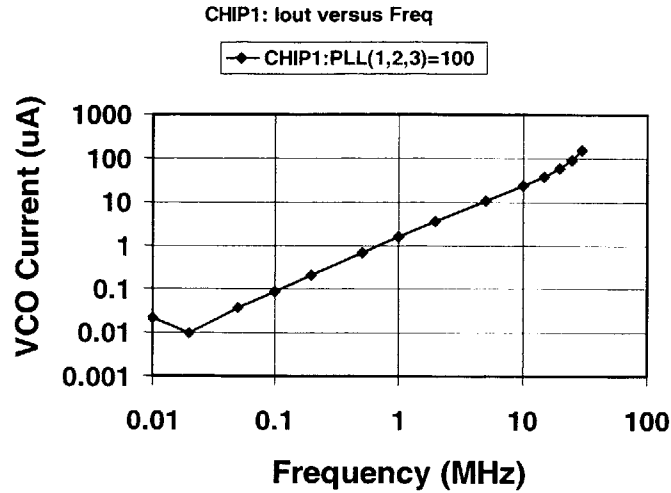


Figure 7-12: Variation of opamp bias current with varying clock frequency.

### PLL Calibration Circuit

The load of the PLL can be varied through 8 levels using a set of 3 PLL calibration bits. Figure 7-13 illustrates the operation of the PLL calibration circuit. Specifically, the upper curve in the figure plots clock period versus the bit states as they are varied from 000 to 111 while bias current flowing through the VCO is kept constant. For this measurement, the bit states were varied one at a time to increase the VCO capacitive load. This causes the bias current to increase. Thereafter, the clock frequency is reduced to bring back the bias current to its original value. This methodology gives us a measure of the change in VCO oscillation period as the capacitance is varied.

The lower curve corresponds to data obtained from HSPICE simulations of the extracted layout. Note that there is a constant gap between the two curves while the slope is identical. This points to a discrepancy in modeling the fixed capacitance across the VCO (the part of the capacitive load that remains across the VCO regardless of the calibration circuit).

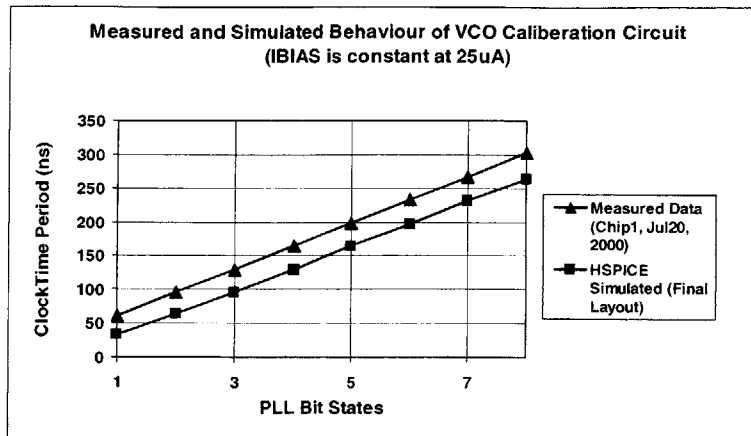


Figure 7-13: Operation of the PLL calibration circuit. This plot shows the clock frequency required to keep the bias current through the VCO constant at 25uA.

### PLL Dynamic Behavior

Figure 7-14a and Figure 7-14b shows the settling behavior of the PLL while the clock is varied from 100KHz to 10MHz. The settling time is 14ms for an off-chip charge pump capacitive load and current of 470nF and 10uA, respectively. The slewing time expected for the PLL based on design values and the voltage shift in the measurement is 14ms. This agrees very well with obtained measurements. Some noise is visible on the measured waveform that is partially due to measurement noise and partially due to high frequency voltage noise due to the charge pump and the phase-frequency-detector.

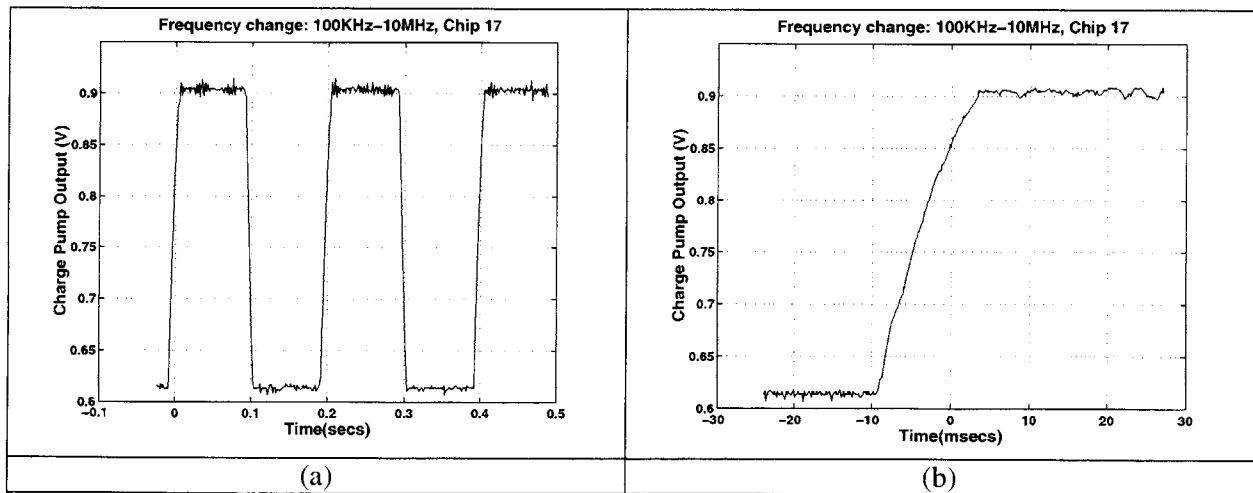


Figure 7-14: PLL dynamics for  $C_{cp}=470nF$  and  $I_{cp}=10uA$ .

### VCO Oscillation Frequency versus VCO Opamp Unity Gain Frequency

The operation of the PLL is based on the premise that the VCO oscillation frequency is a constant factor times the unity gain frequency of the opamps used in the VCO. The following figure is included from HSPICE simulations to demonstrate that this is indeed true for a wide range of bias current variation.

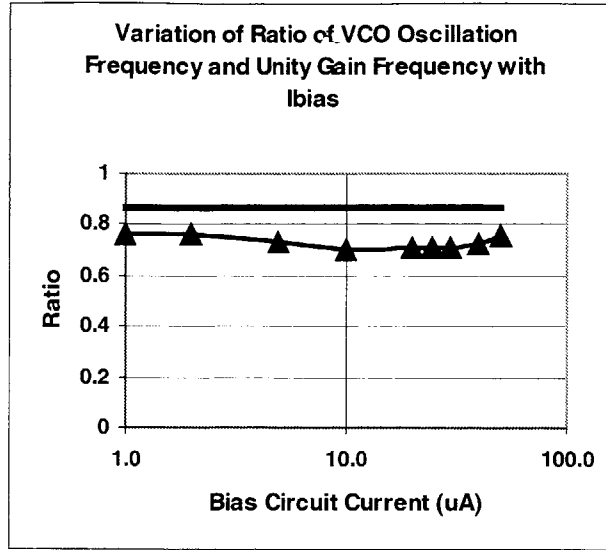


Figure 7-15: Simulated relationship between the VCO oscillation frequency and unity-gain-frequency. The horizontal line shows the theoretical prediction of the ratio between the VCO oscillation frequency and the unity gain frequency.

#### 7.4.4 Comparison of the proposed converter to existing custom solutions

The reconfigurable converter was built in a 0.6μm CMOS process. Its operation has been validated over a bandwidth of 1Hz to 10MHz and resolution ranging from 6 to 16 bits. If this reconfigurable converter is to serve as an attractive solution in the applications considered earlier, the converter needs to possess performance that is competitive with existing custom-built converter solutions. Here a custom-built converter refers to any design that is built for a specific resolution and speed. Additionally the area overhead for constructing a reconfigurable solution needs to be small.

The performance of the reconfigurable converter is compared to measured performance of several custom converters published in the ISSCC and the JSSC over the past three years in Figure 7-16. For completeness, converters fabricated with a variety of feature lengths and power supplies have been considered. The smallest feature length considered is 0.18μm while the highest supply voltage considered is 5V. The definition of the figure-of-merit (FOM) considered for this comparison is encapsulated in the following expression:

$$\text{FOM} = \frac{2^{2N} \times (\text{Data Rate})}{\text{Power}} \quad (7.1)$$

where, N, Power and Data Rate refer to the resolution, power consumption and output data rate of the converter. Notice that the average figure-of-merit for all of the converters represented in the figure drop with reducing resolution. This follows directly from the above expression. In this comparison care has been taken to ensure that the results from the delta-sigma mode have been compared to custom delta-sigma solutions, while the results from the pipeline mode have been compared to custom pipeline converters. For this comparison, resolutions from 12-16 bits have been obtained from the delta-sigma mode with an input bandwidth of 9.4KHz and clock frequencies of 0.625KHz (12-bit), 1.25MHz (13-bit), 2.5MHz (14-bit), 5MHz (15-bit) and 10MHz (16-bit). For resolutions below 12-bits the converter was placed in the pipeline mode. For all the data corresponding to this mode, the clock frequency was 2.6MHz

at an input frequency of 1MHz. For all the data from 12-16 bits, resolution was extracted from SNDR for both the reconfigurable converter and custom solutions. For all the data below 12-bits linearity was used for all the data points. Care was taken to ensure that the comparison was made using only the analog power for all data points on this graph.

It is instructive to consider certain features of the figure that reveal dominant bottlenecks in the converter performance. For most resolutions, the reconfigurable solution is comparable to the best custom solution available. For low resolutions, the figure-of-merit of the reconfigurable converter reduces faster than that suggested by (7.1) as resolution is dropped. This occurs because as resolution is reduced in the pipeline mode, the converter becomes progressively parasitic capacitance dominated and does not remain thermal noise limited. Likewise, at the high end of resolution especially for resolutions of 16-bits and higher, the converter becomes 1/f noise limited and moves out of thermal limited performance. This causes its figure-of-merit to increase at a rate less than a factor of 4 per bit.

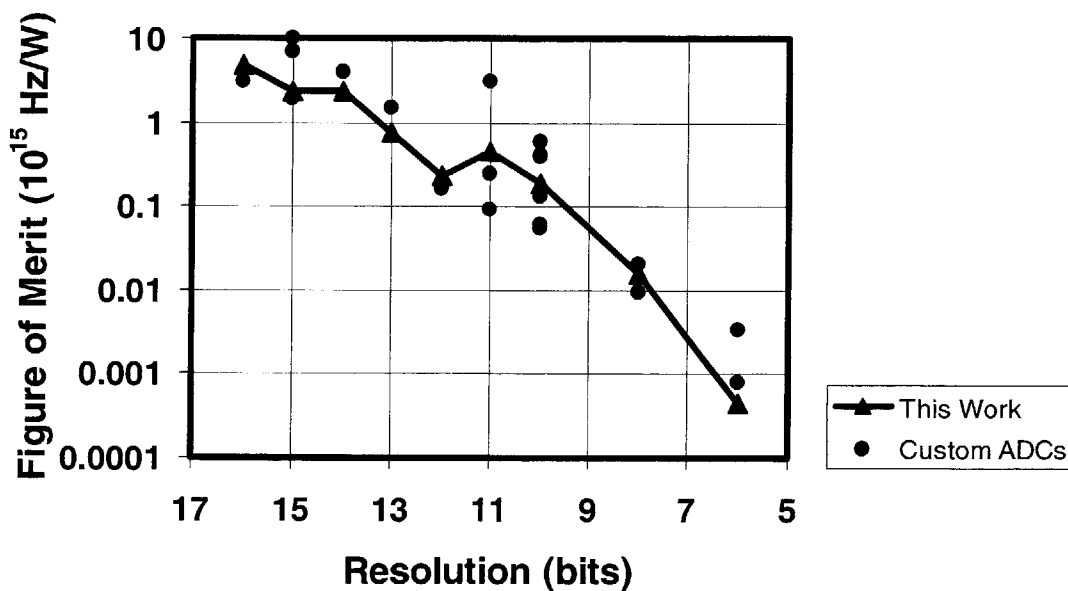


Figure 7-16: Comparison of figure of merit of reconfigurable converter to custom-built converters published in the ISSCC and JSSC from 1997-2000.

Next we discuss the area overhead of the reconfigurable solution. A detailed analysis of the layout and circuit suggests that the reconfigurable converter would occupy approximately 20%-30% over and above a single pipeline converter designed to generate 12-bits of resolution and operate at the highest frequency that can be expected from this design. Area penalty for a reconfigurable solution comes from three sources. These include the two additional basic building blocks required of the reconfigurable converter compared to a dedicated 12-bit solution, the additional logic required to condition the clocks before they are fed to the switches in each block, as well as the phase-locked-loop that is unique in the reconfigurable solution.

Figure 7-17 illustrates a prototype used as a proof-of-concept vehicle for the reconfigurable converter. While the overall area is considerably large, it arises from non-optimal layout, as well as large chunks of the chip devoted for maximizing flexible testing of the converter. The active area for the chip is 5.5mm<sup>2</sup>, however, since it is difficult to count only the transistor area for estimating active regions; this area is also expected to shrink in an optimally designed reconfigurable layout.

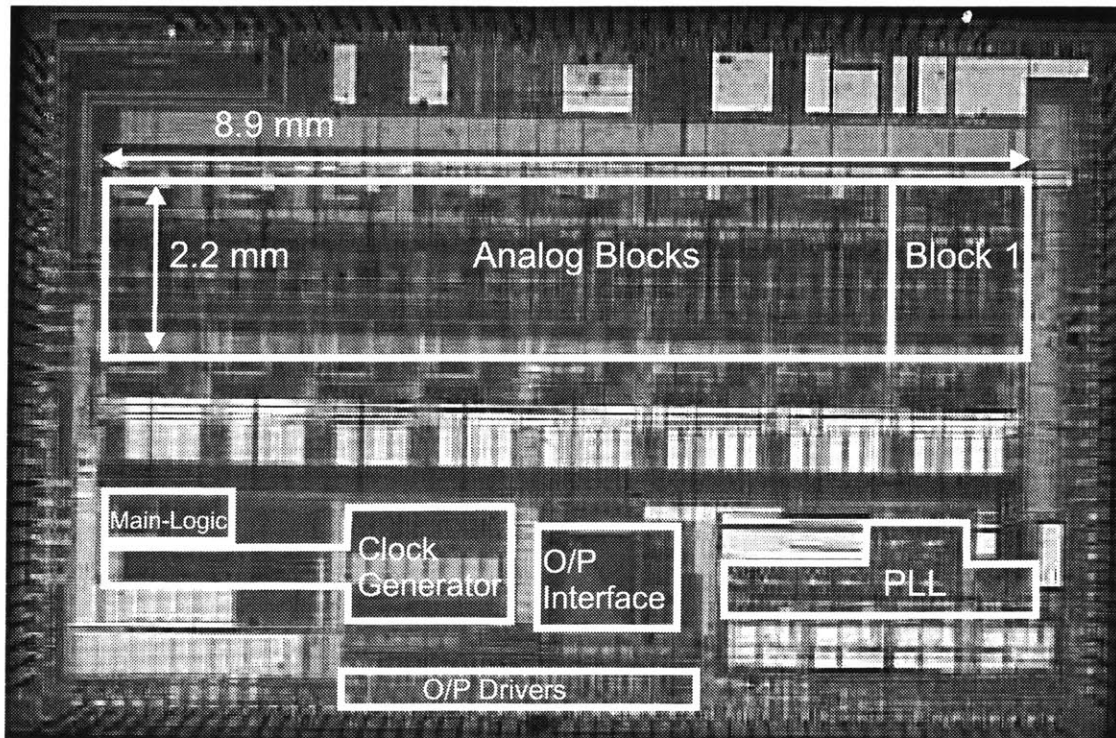


Figure 7-17: Proof-of-concept prototype of reconfigurable converter. The layout is optimized for maximum testability of chip.

### 7.4.5 Summary of Experimental Results

The following table summarizes the primary chip statistics and two specific performance points of the converter.

The architecture, parameter and bandwidth reconfiguration times are relevant to systems where the converter is required to swap between different applications in real-time.

The bandwidth reconfiguration time is dependent on the total capacitive load across the charge-pump. Reducing this capacitive load at the cost of reduced PLL lock range can lower the bandwidth reconfiguration time. This capacitance can be selected based on the application space desired of the converter. For a general-purpose application, opamp bandwidth would also need to be varied; in that cas, bandwidth reconfiguration time needs to be considered.

When the current can be kept constant the converter reconfiguration time is 12 clock cycles regardless of the clock frequency. This is the time it takes for the common-mode feedback across the amplifiers to converge. This measurement has been taken with the view that it may enable applications in the future that include real-time swapping of different signal formats. Notice that that the reference used for the delta-sigma and the pipeline mode for these performance measures are different. The reference for the delta-sigma mode was enhanced to maximize the SNDR for the converter.

Also note that the ADC in pipeline mode was operated at a clock frequency lower than it was designed for. This is because higher clock frequency would exacerbate the gain error from the 2<sup>nd</sup> stage of the 3<sup>rd</sup> reconfigurable block. Standard digital calibration [58] would have corrected this error and allowed us to operate the chip at higher clock frequencies.

<b>Process</b>	<b>0.6<math>\mu</math>m CMOS, DPTM</b>		
<b>Total Die Area (including pads)</b>	<b>10.5mm x 7.6mm</b>		
<b>Total Active Area</b>	<b>5.5mm<sup>2</sup></b>		
<b>Power Supply</b>	<b>2.7V-4.6V (analog), 4.6V (clocks)</b>		
<b>Architecture and Parameter Reconfiguring Time</b>	<b>12 clock cycles</b>		
<b>Bandwidth Reconfiguration Time</b>	<b>14ms (with Ccp=470nF)</b>		
<b>PLL Lock Range</b>	<b>20KHz-40MHz (with Ccp=470nF)</b>		
<b>Delta-Sigma 16 bit Mode (3.3V)</b>	<b>Pipeline 12 bit Mode (3.3V)</b>		
<b>Resolution</b>	<b>16 bits</b>	<b>Resolution</b>	<b>11 bits</b>
<b>Fclock</b>	<b>10MHz</b>	<b>Fclock</b>	<b>2.62MHz</b>
<b>Fin</b>	<b>6.25KHz (1.5V p-p diff.)</b>	<b>Fin</b>	<b>1MHz (1V p-p diff.)</b>
<b>OSR</b>	<b>512</b>	<b>Power</b>	<b>24.6mW</b>
<b>Power</b>	<b>17.7mW</b>	<b>DNL</b>	<b>&lt; +/- 0.55LSB</b>
<b>SNR</b>	<b>94.4dB</b>	<b>INL</b>	<b>&lt; +/- 0.82LSB</b>
<b>HD2</b>	<b>102dB</b>	<b>SNR</b>	<b>62.5dB</b>
<b>HD3</b>	<b>95dB</b>	<b>SFDR</b>	<b>72dB</b>
		<b>THD</b>	<b>71dB</b>
		<b>(HD2=82dB, HD3=72dB)</b>	

Table 8: Performance summary of reconfigurable converter.

## 7.5 Future Improvements of Test System

The test system could be improved in several ways as listed below:

a) Larger Local Memory

The on-board memory size limits the size of the oversampling ratio of the converter in the delta-sigma-mode. The FIFO employed has a depth of 262K points. Given that some of the initial points in the FIFO need to be discarded, the largest data sequence that is a power of 2 that can be extracted from the memory is 128K. This limits the maximum OSR of 1024. A larger memory would allow greater OSR multiples.

b) Option to route Delta-Sigma Output to Fast Logic Analyzer

Another way of obtaining a large memory set is to collect the output data in a fast logic analyzer. A mechanism for routing the output of the converter into this logic analyzer would allow this possibility.

c) Bypassing of Line receiver reference node

The reference node that is supplied to the line receivers at the output of the converter has large parasitic coupling with the digital out from the converter. When several digital outputs change simultaneously the reference node can be yanked away from its nominal value leading to errors. In fact this phenomenon can lead to data dependent errors. To prevent this, this node needs to be extensively bypassed. The initial prototyping board did not have sufficient bypassing. Additional capacitors were later added using makeshift copper strips.



# 8 Conclusions and Future Work

## 8.1 Summary

This thesis presents the concept and design of a low-power reconfigurable converter. This converter can digitize a wide variety of signals over a bandwidth range of 1Hz to 10MHz and a resolution range from 6-bits to 16-bits. A converter of this nature can be programmed by the user for targeting fixed applications or can be employed in scenarios where real-time programmability is desired such as in multi-sensor systems, multi-standard systems, and systems in which variable quality of service is desired.

The concept of this converter stems from the observation that certain converter architectures such as the pipeline and delta-sigma converter topologies are composed of the same basic components such as opamps, comparators, switches and capacitors. The difference between them, from a network perspective, is the interconnection between these devices. Thus, a converter composed of these basic building blocks in conjunction with a configurable switch matrix, can adapt to these different topologies and work at different resolutions and bandwidths. Any performance degradation due to switch parasitics is minimized by maximizing the re-use of switches between different modes. The converter has three levels of reconfiguration – architecture, parameter and bandwidth.

This converter also serves as a vehicle to demonstrate circuit techniques for reducing overall power consumption of general pipeline or delta-sigma converters. The use of capacitors that are sized to the fundamental  $kT/C$  noise limit minimizes the overall power of the converter. Global converter chopping that eliminates the need for opamp offset correction at the local opamp level also reduces overall converter power while dramatically simplifying the process of offset correction. The opamp chopping technique in the delta-sigma mode serves to reduce the effect of the offset and  $1/f$  noise without the need for switches in series with the operational amplifier leading to enhanced settling speed and reduced thermal noise. Both of these positive attributes can then be traded off for lower power.

In order to have the bias current of the opamps in the converter track the clock frequency, a phase-locked-loop is employed. The PLL utilizes a cascade of opamps in feedback as the VCO. Theoretical analysis, HSPICE simulations as well as measurements have been used to validate the concept and design of this VCO. In order to maximize the sampling frequency range over which the converter can operate, the PLL incorporates features to enhance its tracking range. These include the design of the charge-pump low-pass filter, the voltage-to-current converter that can work over almost four orders of magnitude variation in current and the post-VCO comparator methodology. Theoretical analysis was done in order to ensure proper loop stability over the entire range of PLL operation.

As the clock frequency is varied over 3 orders of magnitude, the input devices of the opamps in both the VCO as well as the converter move from strong inversion to sub-threshold regimes. The bias circuit of the opamps incorporates a technique to keep these input devices in saturation over both these regimes.

The converter was successfully characterized over an input bandwidth range of 0-10MHz and a resolution range of 6-bits to 16-bits with power consumption that is competitive with respect to state-of-art converters custom built for various performance points. Its phase-locked loop was shown to have a locking range of over three orders of magnitude from 20KHz to 40MHz. The architecture and parameters

of the converter can be varied within 12 clock cycles, while the bias current can be modified within 14ms. The bias current switching time can be reduced using adaptive charge-pump current and by reducing the PLL locking range.

In order to debug the converter in the pipeline mode a signature analysis (Appendix B) methodology that is also applicable to other pipeline converters is proposed. This technique allows determination of pipeline errors by looking for certain tell-tale error signatures in the output code histogram of the converter.

Information on a high-swing replica-tail amplifier that was conceived, designed and tested as a separate chip is presented in Appendix A.

## **8.2 Future Work for the Next Generation Reconfigurable Converter**

The overall resolution and bandwidth range of the reconfigurable converter can be extended by adding new architectural modes to the system and/or by making architectural modifications to the existing modes. The following are suggestions that would be useful for constructing the next generation reconfigurable converter.

### **8.2.1 Enhancements in the Delta-Sigma Mode**

Within the delta-sigma mode, all the noise-shaping zeros of the converter lie at DC. This implies that at low oversampling ratios such as 16 or 32, the converter becomes quantization noise dominated and its resolution drops very fast with any further reduction in oversampling ratio. A system with zeros that are spread away from DC will extend the lower limit of OSR over which the converter will be thermal noise limited. This will allow the converter be useful even at low OSR thus be capable of moderate resolution at higher input bandwidth.

The noise shaping zeros can be spread away from DC using simple resonator loops and can be implemented with two additional capacitors and a few extra switches for the first four blocks of the reconfigurable converter.

An additional feature would be variable delta-sigma order. This can be implemented by simply switching off the first and possibly second modulator stages to obtain lower order and hence lower power at lower resolutions.

### **8.2.2 Enhancements in the Pipeline Mode**

The upper bandwidth within the pipeline mode was limited by the linearity of the converter related to the size of capacitors. The next generation reconfigurable converter should probably employ larger sized capacitors to extend the pipeline converter bandwidth limitation. Additionally, techniques to reduce effect of capacitor mismatch such as digital calibration [58] or Commutative feedback switching scheme (CFCS) [29] should be incorporated in the next generation of the reconfigurable converter.

### **8.2.3 Additional Architectures**

To target very high speeds at low to moderate resolutions a flash type architecture is needed. This can perhaps be incorporated after the last pipeline stage to serve the dual purposes of providing the reconfigurable converter with a flash mode as well as providing the pipeline converter mode with additional lower significant bits.

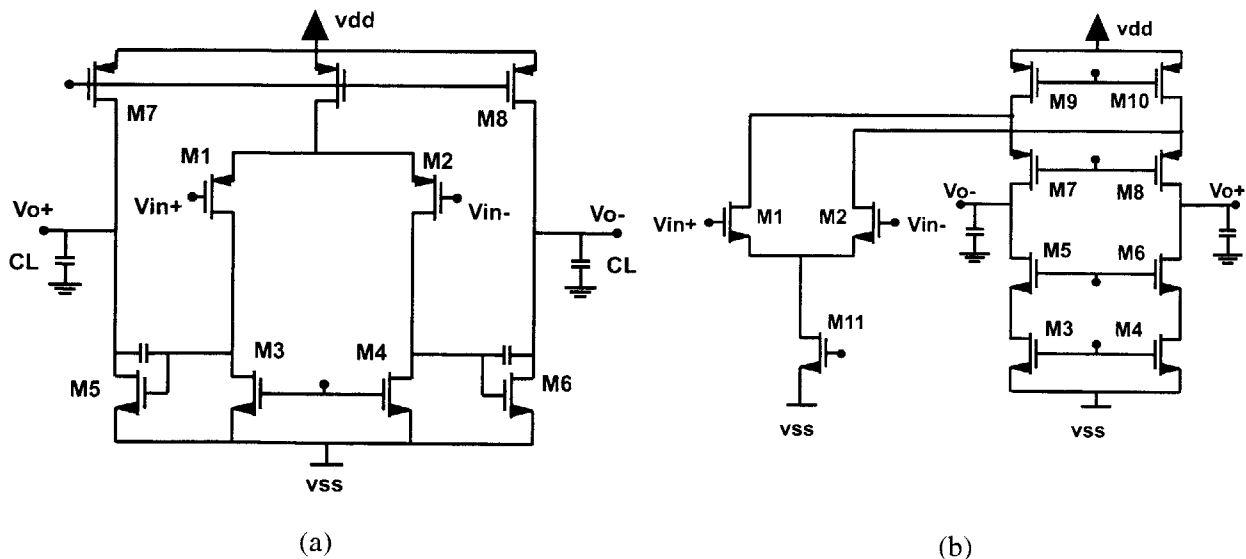
The lower bandwidth end is dictated by the lower end of the PLL locking range as well as the leakage of the capacitors through junction leakage and, in future deep-submicron processes, leakage through transistor gates. A cyclic converter would serve as a viable solution to achieve this purpose. A cyclic converter could be constructed out of single pipeline stages, and it could change the pipeline stage it employs in order to affect thermal noise variation.



# Appendix A: A High-Swing CMOS Telescopic Operational Amplifier

## A.1 Introduction

Designing high performance analog circuits is becoming increasingly challenging with the persistent trend towards reduced supply voltages. The main bottleneck in an analog circuit is the operational amplifier. At large supply voltages, there is a trade-off between speed, power and gain amongst other performance parameters. Often these parameters present contradictory choices for the opamp architecture. At reduced supply voltages, output swing becomes yet another performance metric to be considered when designing the opamp. Of the several architecture alternatives, Figure A-1 shows some of the most popular topologies. Figure A-1a shows the design of a simple 2-stage amplifier. With all the transistors in the output stage of this amplifier placed in the saturation regime, it has a differential output swing of  $2V_{\text{sup}} - 4V_{\text{ds,sat}}$ , where  $V_{\text{sup}}$  is the supply voltage and  $V_{\text{ds,sat}}$  is the minimum  $V_{\text{ds}}$  required to saturate a transistor. For a typical  $V_{\text{ds,sat}}$  of 200mV, the differential swing is about  $2V_{\text{sup}} - 0.8\text{V}$ , which is superior to that of most other topologies. Its non-dominant pole, arising from its output node, is located at  $gm_6/C_L$ , where  $gm_6$  is the transconductance of transistor M5 or M6 and  $C_L$  is the load capacitance. Since this pole is determined by an explicit load capacitance, it typically occurs at a relatively low frequency. As a result, this amplifier has a compromised frequency response. Other drawbacks of this architecture include high power consumption because of 2 stages in its design and poor negative power supply rejection (from  $V_{\text{SS}}$ , in the figure) at high frequencies.



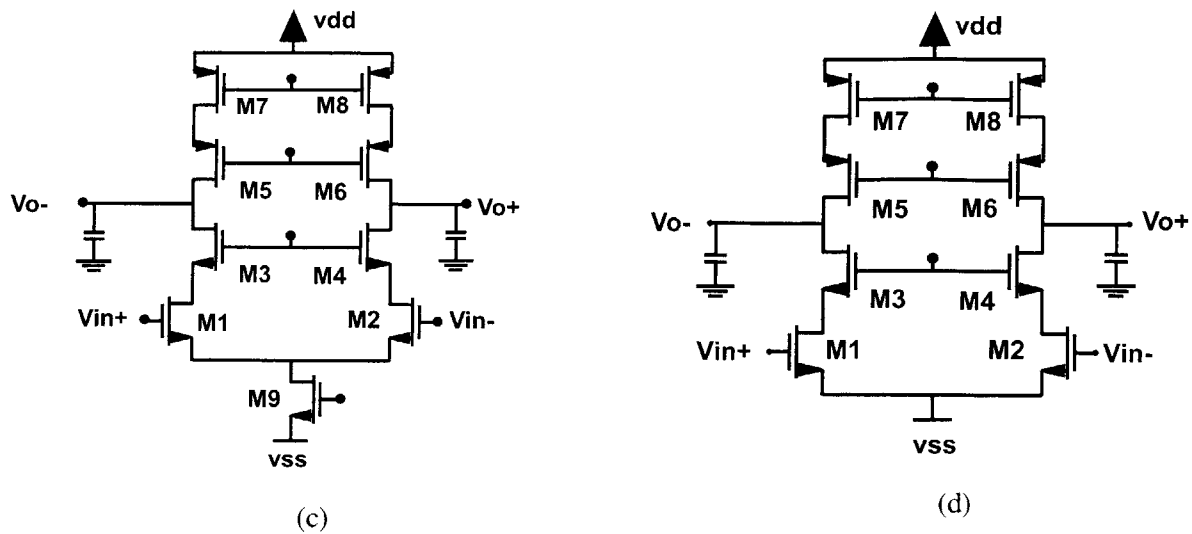


Figure A-1: Conventional opamp topologies. (a) 2-stage amplifier. (b) Folded-cascode amplifier. (c) Telescopic amplifier. (d) No-tail telescopic amplifier.

The folded cascode topology is shown in Figure A-1b. The swing of this design is constrained by its cascoded output stage. Although only  $V_{ds,sat}$  is needed to saturate the bottom-most load transistors and the top-most current source transistors, in order to allow for process variations, a small safety margin  $V_{margin}$  is often added to their  $V_{ds}$  to ensure saturation. Accounting for these, and the  $V_{ds,sat}$  required across the cascode devices, the differential output swing is  $2V_{sup} - 8V_{ds,sat} - 4V_{margin}$ . With a voltage margin of 100mV, this is estimated to be  $2V_{sup} - 2V$ . The second pole of this opamp is located at  $gm_g/\Sigma C_p$ , where  $gm_g$  is the transconductance of transistor M7 or M8 and  $\Sigma C_p$  is the sum of the parasitic capacitance contributed from transistors M2, M8 and M10 at the source of transistor M8. Since its second pole frequency is higher than the non-dominant pole of a typical 2-stage topology, this design has correspondingly superior frequency response. Also, because the compensation for this amplifier terminates to ground in contrast to the 2-stage compensation style, it has better high frequency PSRR. The power consumption of this design is approximately the same as that of the 2-stage design. Although the current in the output stage can be much smaller than that flowing through the input devices, in practice, the output stage current is picked to be the same or almost the same as the current in the input stage. If the current in the output stage is smaller, a slow common-mode feedback circuit leads to non-symmetrical output slewing, and the output current becomes the bottleneck for the differential slew rate of the opamp. On the other hand, if the common-mode feedback is as fast as the differential path of the opamp, the differential slew rate is independent of the quiescent current in the output in which case the output current can be reduced without affecting the slew rate. A fast CMFB, however, compromises the differential frequency response. Typically, the differential frequency response is optimized at the cost of slower common-mode feedback. Therefore, it becomes necessary to have the output stage current equal to that of the input stage.

A telescopic cascode opamp, as shown in Figure A-1c typically has higher frequency capability and consumes less power than other topologies. Its high frequency response stems from the fact that its second pole corresponding to the source nodes of the n-channel cascode devices, is determined by the transconductance of n-channel devices as opposed to p-channel devices as in the case of a folded-cascode. Also, the parasitic capacitance at this node arises from only 2 transistors instead of 3 as in the latter. The

single stage architecture naturally suggests low power consumption. The disadvantage of a telescopic opamp is severely limited output swing. It is smaller than that of the folded-cascode because the tail transistor directly cuts into the output swing from both sides of the output. In the telescopic opamp shown in Figure A-1c, all transistors are biased in the saturation region. Transistors M1-M2, M7-M8 and the tail current source M9 must have at least  $V_{ds,sat}$  to offer good common-mode rejection, frequency response and gain. The maximum differential output swing of a telescopic opamp is shown to be  $2V_{sup} - 10V_{ds,sat} - 6V_{margin}$ . Under identical conditions as before, the output swing of this design can be shown to be limited to  $2V_{sup} - 2.6V$ . In a 3V supply system, this represents a 45% reduction of the available output swing.

At large supply voltages, the telescopic architecture becomes the natural choice for systems requiring moderate gain from the opamp. Reducing supply voltages, on the other hand, forces reconsideration in favor of the folded-cascode, or in the extreme case, the 2-stage design. Although a telescopic opamp without the tail current source [49] (Figure A-1d) improves the differential swing by  $2V_{ds,sat} + 2V_{margin}$  (600mV), the common-mode rejection and power supply rejection of such a circuit is greatly compromised. Moreover, the performance parameters (such as unity-gain frequency and settling time) of an opamp with no tail or with a tail transistor in the linear region is sensitive to input common-mode and supply voltage variation which is undesirable in most analog systems.

Other opamps that have traditionally been employed in high performance applications include the Class AB opamp [50]. This amplifier, however, requires a minimum supply voltage of  $2V_t + 4V_{ds,sat} + 2V_{margin}$ , where  $V_t$  is the threshold. For  $V_t$  of 0.8V,  $V_{sup}$  must be greater than 2.6V. This requirement renders this architecture unsuitable in future low-voltage applications. Other drawbacks include degraded frequency response because of the presence of current-mirrors (which lead to pole-zero doublets in the differential path) and large opamp noise. Other rail-to-rail amplifiers with class AB type output stage [51] deliver very high swing. These too, however, typically require current-mirrors in the differential path with a high minimum supply voltage requirement.

This paper presents a design that combines the low-power, high-speed advantage of the telescopic architecture with the high-swing capability of the folded-cascode and the 2-stage design. It achieves its high performance while maintaining high common-mode and supply rejection, and ensuring constant performance parameters. The techniques described are general and can potentially be applied to improve the performance of some other topologies as well.

## A.2 High swing operational amplifier

### A.2.1 Importance of High Swing in Operational Amplifiers

In analog circuits where  $kT/C$  noise is the dominant noise, the relationship between opamp performance metrics such as speed, signal-to-noise ratio (SNR) and power consumption can be shown to be

$$\frac{\text{SNR} \cdot \text{Speed}}{\text{Power}} = \frac{(\text{Swing})^2}{\gamma(kT/C)} \cdot \frac{\beta(gm/C)}{V_{sup} \cdot (\lambda I)} \quad (\text{A.1})$$

where the constants  $\beta$ ,  $\gamma$ , and  $\lambda$  are the feedback factor of the closed loop opamp, the number of  $kT/C$  noise contributions of the switches and the opamp at the output of the amplifier, and the ratio of the total

current consumption of the opamp to the current  $I$  flowing through one of the input devices, respectively. Here, speed corresponds to the dominant pole location of the opamp. The above expression simplifies to

$$\frac{\text{SNR} \cdot \text{Speed}}{\text{Power}} \propto \frac{(\text{Swing})^2}{V_{\text{sup}}} \quad (\text{A.2})$$

when  $g_m \propto I$  as in the case when the input devices are in weak inversion or in the saturation region of strong inversion. The proportionality constant in the last term is a function of the architecture of the opamp and the switched-capacitor circuitry around the opamp. It is clear from this expression that increase in the swing of the opamp leads to overall performance improvement that can be exploited to achieve lower power or higher SNR or speed.

## A.2.2 Methodology for Improved Swing

In the topology shown in Figure A-2, transistors M7-M8, and M9 are deliberately driven deep into the linear region. Since these transistors normally operate in the linear region,  $V_{\text{margin}}$  is not needed across these devices. Under these conditions, the output swing is shown to be  $2V_{\text{sup}} - 6V_{\text{ds,sat}} - 2V_{\text{margin}} - 2V_{\text{ds,lin-tail}} - 2V_{\text{ds,lin-load}}$ , where  $V_{\text{ds,lin-tail}}$  and  $V_{\text{ds,lin-load}}$  are the drain-to-source voltages for the tail and load transistors, respectively. With  $V_{\text{ds,sat}}$  of 200mV,  $V_{\text{margin}}$  of 100mV,  $V_{\text{ds,lin-tail}}$  of 80mV and  $V_{\text{ds,lin-load}}$  of 160mV, the differential output swing is  $2V_{\text{sup}} - 1.88\text{V}$ , which is superior not only to a telescopic amplifier by about 0.7V, but also to a regular folded-cascode amplifier by roughly 100mV. The swing enhancement stems not only from the difference between  $V_{\text{ds,sat}}$  and the voltage across the devices in the linear region but also because of the fact that we no longer need  $V_{\text{margin}}$  across devices placed in the linear region. It is important to note that any reduction in voltage across the tail transistor improves differential swing two-folds as the tail transistor cuts into the output swing from both sides of the amplifier. Also, the elimination of  $V_{\text{margin}}$  across the tail and the load devices itself contributes to a swing enhancement of  $4V_{\text{margin}}$ . This benefit of increased swing by pushing the load and tail transistors in the linear region, however, is accompanied by degraded CMRR, PSRR, and differential gain of the amplifier. Additionally, as in the case of the no-tail telescopic amplifier, performance parameters of the amplifier are sensitive to the input common-mode voltage level. The reduction in dc gain has been compensated by a regulated cascode gain enhancement scheme and a replica-tail feedback technique is used to recover the CMRR and PSRR, and to ensure constant performance parameters for the opamp.



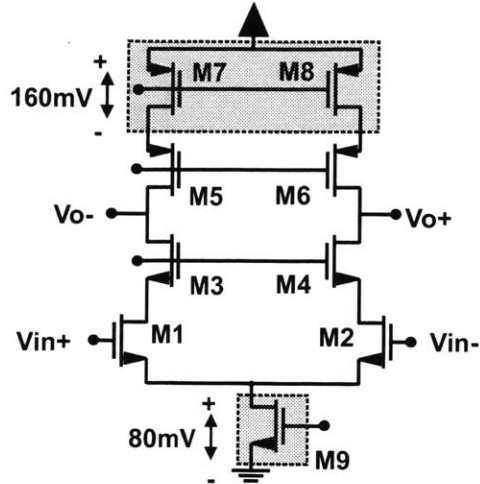
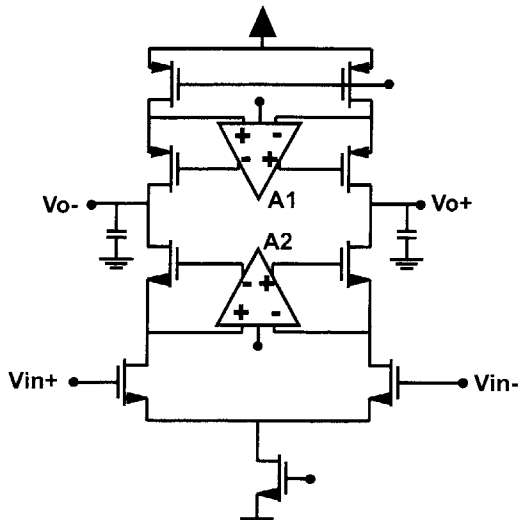


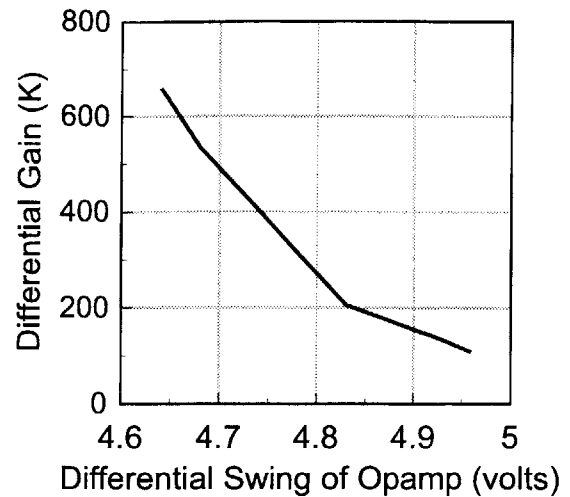
Figure A-2: Methodology for enhancing swing.

### A.2.3 Regulated Cascode for Recovering Gain

The gain enhancement used in the amplifier employs the well-known differential regulated cascode structure [52] as shown in Figure A-3a, with the difference being the presence of a third input in the gain-enhancement amplifiers [48] to bias the load transistors and the input devices in the linear and saturation region, respectively. In addition, the bottom gain-enhancement amplifier incorporates part of the replica-tail feedback scheme, as will be described in section 9.3.1. Figure A-3b illustrates the trade-off between differential gain and swing of the opamp. Pushing the load devices deeper into the linear region increases swing at the cost of reduced gain. This trade-off can be invoked as long as the gain of the opamp is greater than the application requirements. The dot on the curve represents the operating point for the opamp presented in this paper, as will be described.

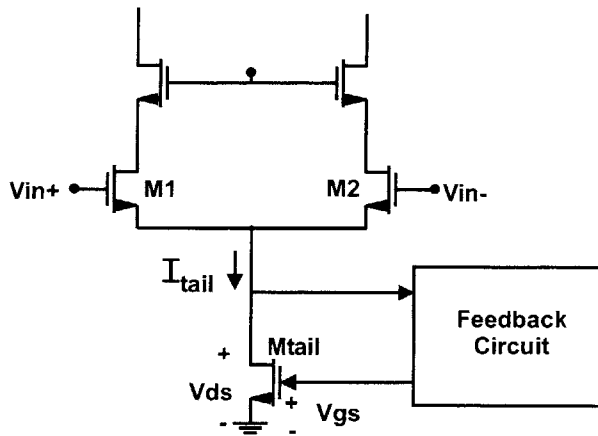


(a)

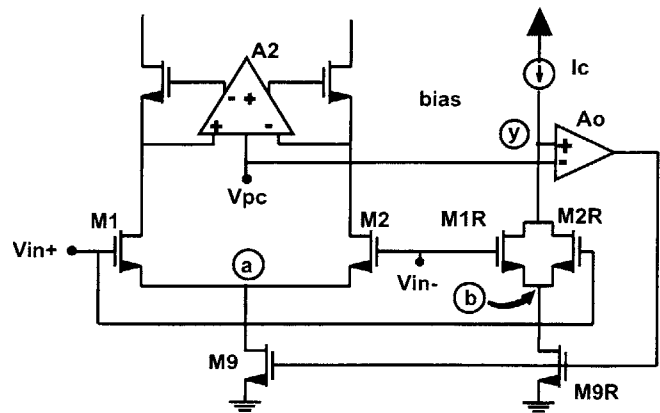


(b)

Figure A-3: (a) Regulated cascode scheme to recover differential gain. (b) Variation of differential gain with differential swing of opamp.



(a)



(b)

Figure A-4: (a) Basic concept of replica-tail feedback. (b) Circuit realization of replica-tail feedback.

## A.2.4 Concept of Replica-Tail Feedback Technique

The concept of the replica tail feedback is illustrated in Figure A-4a. The basic goal of the replica tail feedback is to keep the tail current constant despite variations in the input common-mode voltage level. It accomplishes this by sensing the drain-to-source voltage across the transistor and modulating its gate voltage. The circuit realization of the 'feedback circuit' is shown in Figure A-4b. Transistors M1, M2 and M9 represent the input devices and tail current source of a differential amplifier, while M1R, M2R and M9R form their corresponding replicas. A constant current  $I_c$  is forced through the replica transistors. Amplifier  $A_o$  is placed in negative feedback across the replica circuitry which forces the voltage at node y

to be equal to the voltage  $V_{pc}$  at the third input of the gain-amp. Also, the common-mode gain of the gain enhancement amplifier A2 forces the common-mode component of the drain voltages of M1 and M2 to be equal to the voltage  $V_{pc}$ . Under these conditions, it can be shown that the voltage at the drain of the tail transistor (node a) always equals the voltage at the drain of the replica tail transistor (node b). Since current through M9R is fixed by  $I_c$ , current through M9 must also remain fixed, thus suggesting a larger “effective” resistance looking into the tail transistor. This “excess tail resistance” can be traded off for output swing by pushing M9 into the deep linear region, while retaining the CMRR and PSRR of the conventional telescopic amplifier. A similar technique was proposed for the tail current of a 2-stage amplifier, but without silicon results [54]. It can be shown that our method, however, provides superior CMRR and PSRR by ensuring better replica-main circuit match by making use of a gain-enhancement amplifier.

Under the conditions that the main and replica circuits are perfectly matched, small-signal analysis shows that the effective resistance looking into the tail-current transistor can be approximated as:

$$R_{tail} = r_{o9} \left( 1 + A_o \cdot \left( g_{m_{9R}} \cdot r_{o_{9R}} \right) \cdot \left( g_{m_{1R}} \cdot r_{o_{1R}} \right) \right) \quad (A.3)$$

Since M9R is in the linear region, its  $g_m \cdot r_o$  product is less than unity. Thus, the enhancement is mainly provided by the product of  $A_o$  and  $g_{m_{1R}} \cdot r_{o_{1R}}$ . It is intuitively consistent to note that the enhancement in the effective resistance equals the loop gain of the replica loop.

## A.3 Implementation of opamp

### A.3.1 Circuit Description

The internal structure of the gain enhancement amplifier A1, as shown in Figure A-3a, is depicted in Figure A-5a. This amplifier uses a standard folded-cascode architecture; the choice of architecture was determined by requirements of speed and desired input/output voltage levels. The third input (applied at the gate of transistor M5E) sets the drain voltages of M7 and M8 in the main amplifier. The left side of Figure A-5b shows a complementary version of the amplifier A1. Normally, an amplifier of this type would serve as the lower gain enhancement amplifier A2. We have modified this architecture, (shown on the right side of the figure), to incorporate the amplifier  $A_o$  used in the negative feedback loop across the replica circuit. The basic idea is to split the 3rd input transistor M3W, in the circuit on the left, to create a new differential pair consisting of transistors M3X and M4X, and transistors M7X and M8X acting as an active load, as shown in the shaded region on the right. The differential amplifier, thus realized, serves as the replica amplifier  $A_o$  with output  $V_t$ . Viewed in the common-mode sense, this differential pair still acts like the third input that enables us to set the dc level of the common-mode voltage at the drains of the input devices of the main amplifier as before. This implementation has several advantages. First, the current through the single 3rd input transistor is being reused in the new differential pair. Hence no additional power consumption is required to construct amplifier  $A_o$ . Second, since the differential gain enhancement amplifier (with input transistors M1X and M2X) is in common-mode unity gain feedback across the cascode devices in the telescopic amplifier, the common-mode voltage at the inputs of this enhancement amplifier equals the common-mode voltage of the inputs of amplifier  $A_o$ . Also, since amplifier  $A_o$  is in negative feedback, its inputs are virtually shorted. Hence, the voltage at the drain of transistors M1R and M2R (node y), as seen in Figure A-4b, tracks the common-mode voltage at the drains of transistors M1 and M2, thus ensuring good replica-main matching, which improves the performance of the replica-tail feedback technique. Additionally, this implementation allows simultaneous setting of the dc levels of the common-mode voltage at the drains of the input devices and the replica input devices and ensuring their equality.

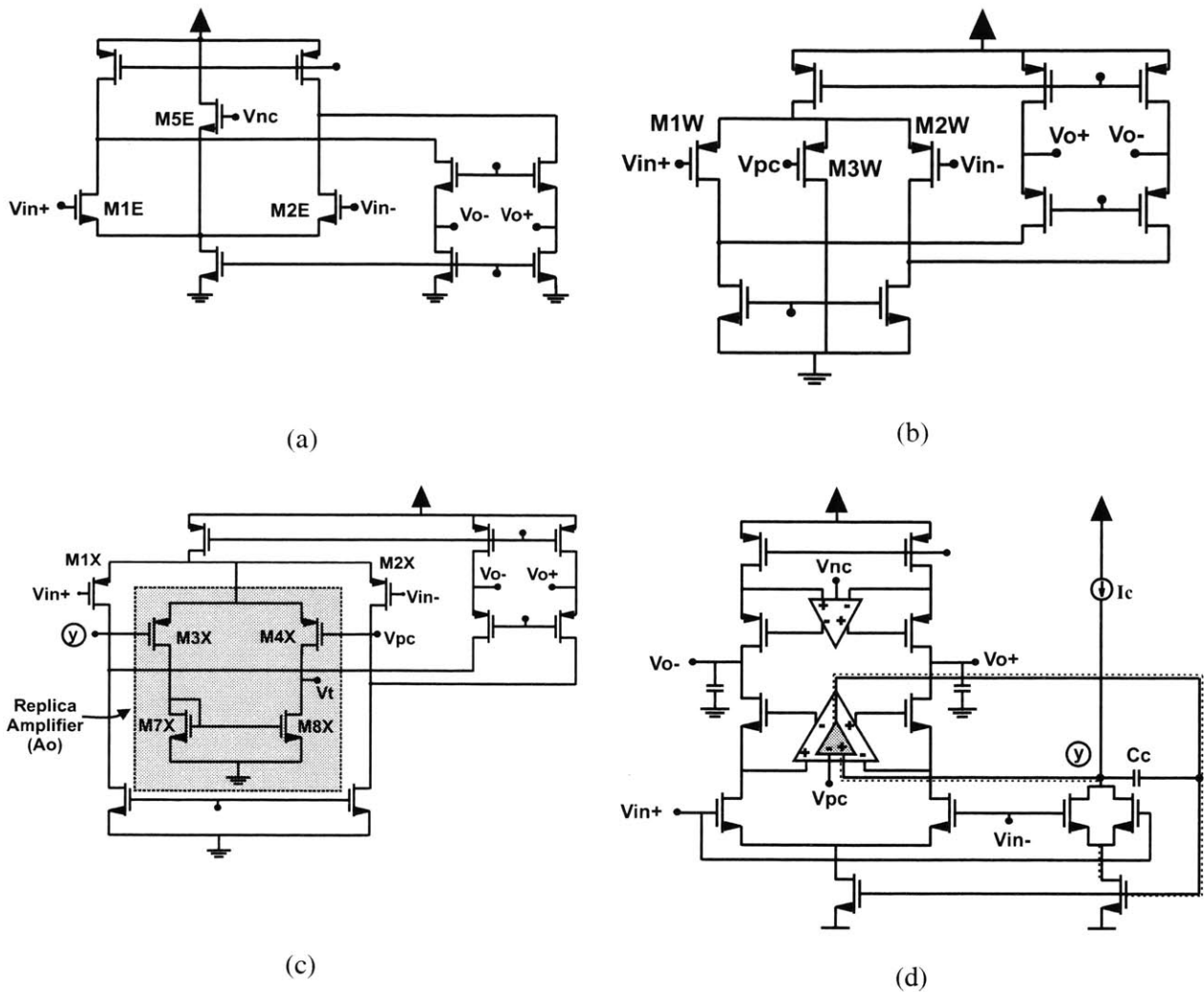


Figure A-5: (a) Gainamp across p-channel cascodes. (b) Gainamp across n-channel cascodes. (c) Overall implementation.

The overall implementation of the operational amplifier is shown in Figure A-5c. The common-mode loop as highlighted by the dashed path can be regarded as a 2-stage amplifier with the replica amplifier  $A_o$  as the first stage and the replica circuit as the second stage. Capacitance  $C_c$  is used to push the pole corresponding to node  $y$  (or the second stage pole) to a higher frequency. Note that the unity gain frequency of the replica-loop is determined by the ratio of the transconductance of the replica amplifier to the capacitance  $C_c$ . The gainamps, on the other hand, are stabilized by the combination of an explicit capacitance and parasitic capacitance placed at the gates of the cascode devices. A cascode current-mirror is used to supply the current to the replica circuit. For the common-mode feedback, the standard switched-capacitor circuit is employed.

### A.3.2 Optimization of Power Consumption and Area

Since the replica-circuit and the gain enhancement amplifiers drive much smaller capacitive loads than the main amplifier, it is possible to scale down these circuits with respect to the main amplifier. Here scaling entails reducing the device widths and current through the transistors. Such scaling will not

change the voltage levels at various nodes in the circuit. This process allows us to minimize power consumption and area associated with the gain enhancement and replica tail feedback. The process of scaling reduces the non-dominant pole location of the 2-stage amplifier in the replica-loop and would ultimately force the reduction of the unity-gain frequency (given the need for adequate phase margin) of the loop, which in turn would degrade the high frequency PSRR and CMRR of the overall amplifier. Thus the limit to such scaling is determined by the requirements of high frequency CMRR and PSRR on the amplifier. In this implementation, the transistor widths and current in the replica circuitry were scaled by a factor of 4, while 2.6 is the scaling factor employed for the gain enhancement amplifiers. These circuits can be scaled further; such aggressive scaling, however, was not executed here because the main idea in this paper was to forward the concept. After scaling, the power consumed by both gain-enhancement amplifiers combined is about a third of the total power consumption of the opamp.

### A.3.3 Effect of Mismatch

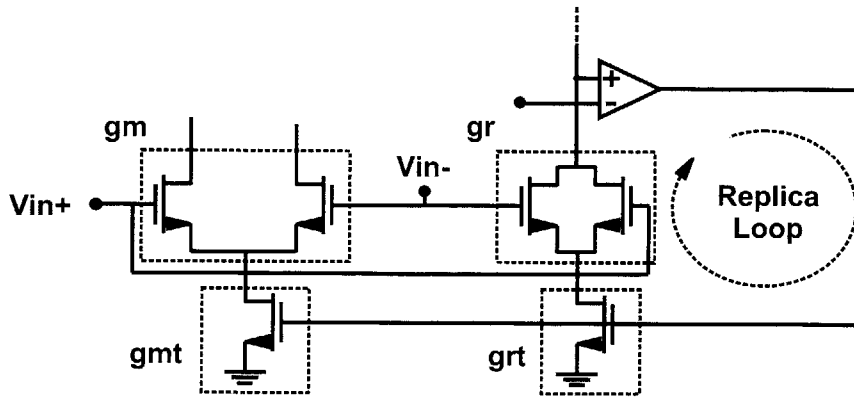


Figure A-6: Effect of mismatch.

Previous analysis in this paper assume that the main and replica circuits are perfectly matched. In practice, mismatch limits the effectiveness of the replica-tail feedback, thereby limiting the enhancement of common-mode rejection that arises from the use of this scheme. It can be shown that the effective output resistance and CMRR enhancement due to the replica circuit can be described by:

Condition	Enhancement
$\Delta_{rep} \ll \frac{1}{A_{loop}}$	$1 + A_{loop}$
$\Delta_{rep} \gg \frac{1}{A_{loop}}$	$\frac{1}{\Delta_{rep}}$

where,  $\Delta_{rep}$  is a factor that encapsulates the mismatch between the main and the replica circuits and can be expressed as  $\Delta_{rep} = 1 - \frac{g_r / g_{rt}}{g_m / g_{mt}}$  when the tail transistors are in the deep linear region. Here,  $g_r$ ,  $g_{rt}$ ,

$g_{m_r}$  and  $g_{m_t}$  are the transconductances of the replica and the main transistors as shown in Figure A-6. Please refer to Section A.6 for details.

If the main-replica mismatch as embodied by the mismatch factor is very small, the enhancement factor equals the loop gain of the replica circuit. Mismatch, on the other hand, leads to reduced enhancement.

### A.3.4 High Frequency Behavior of CMRR

The first pole for the common-mode rejection of the amplifier can be shown to be located at  $\omega_{p_{rep}} + \Delta_{rep} \cdot (\omega_{p_{rep}} \cdot A_{loop})$ , where  $\Delta_{rep}$  is the mismatch factor as defined above,  $\omega_{p_{rep}}$  is the pole location for the open-loop replica circuit, and  $A_{loop}$  is the replica circuit loop gain (see A.6). For the

second condition as defined in the previous sub-section, i.e. for  $\Delta_{rep} \gg \frac{1}{A_{loop}}$ , the first pole location

of the CMRR is equal to  $\Delta_{rep} \cdot (\omega_{p_{rep}} \cdot A_{loop})$ , where  $\omega_{p_{rep}} \cdot A_{loop}$  is essentially the unity gain frequency of the replica circuit over its loop. Mismatch between the main and replica circuits, as mentioned in the previous section, reduces the CMRR enhancement achievable by replica-tail feedback scheme. However, increasing mismatch leads to increased CMRR bandwidth (as represented by its first pole location). In fact, it can be shown that the product of the CMRR at dc and the bandwidth of the CMRR is independent of the main-replica mismatch.

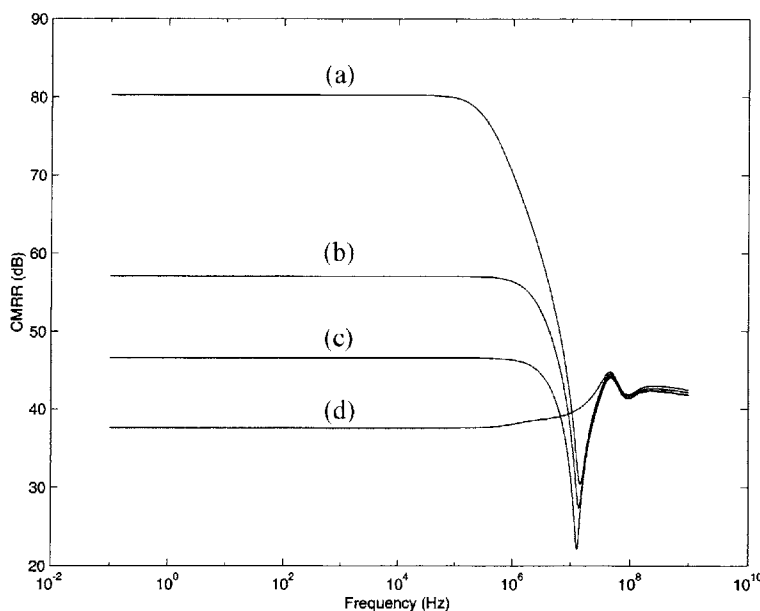


Figure A-7: Behavior of CMRR with frequency.

Figure A-7 depicts the simulated high-frequency behavior of the common-mode rejection of the replica-tail feedback telescopic operational amplifier, with and without mismatch between the main and replica circuitry, and compares them to a telescopic topology without the replica feedback. Curve (a) in the figure illustrates the CMRR-frequency dependency for the opamp using the replica feedback scheme with no main-replica mismatch. The CMRR for the amplifier employing replica-tail feedback with certain mismatch applied between the replica circuit (transistors M1R, M2R and M9R) and the main circuit (transistors M1, M2 and M9) is shown by (b). The mismatch applied between the main and the replica

transistors that are supposed to match is  $\Delta V_t=1\text{mV}$  for the  $V_t$  mismatch and  $\Delta L=0.02\mu\text{m}$  for the length mismatch. Curve (c) is the case when the  $V_t$  mismatch between the main and the replica transistors is increased to  $10\text{mV}$  with the same length mismatch as in (b). The increase in CMRR bandwidth with an increase in mismatch is clearly evident from these curves. Curve (d) shows the behavior of the common-mode rejection for the amplifier that does not use the replica tail scheme while still employing the tail transistor in the linear region.

## A.4 Experimental results

The opamp shown in Figure A-5c has been implemented in a standard  $0.8\mu\text{m}$  n-well, single-poly, double-metal CMOS process. The micro-photograph of the chip is shown in Figure A-8. It occupies a die area of  $600\mu\text{m} \times 630\mu\text{m}$  and consumes a total power of  $4.8\text{mW}$  at a  $3.3\text{V}$  supply. As indicated earlier both the area and power consumption can be further minimized by additional scaling of the replica and the gain enhancement amplifiers. To minimize the mismatch between the main and the replica circuits, a cross-quad layout was employed for the critical transistors.

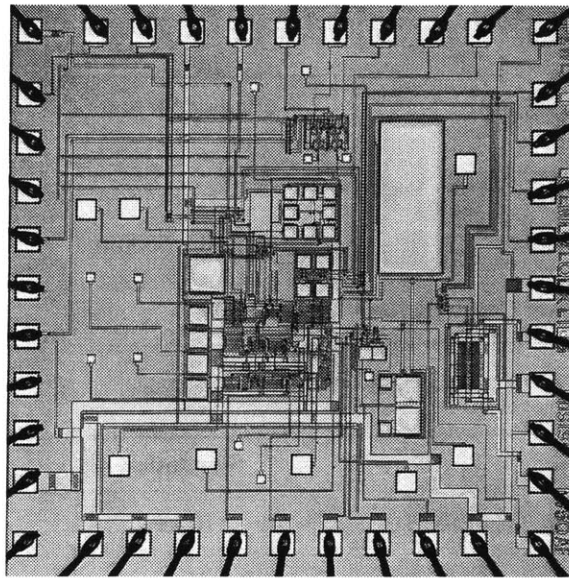


Figure A-8: Opamp micro-photograph.

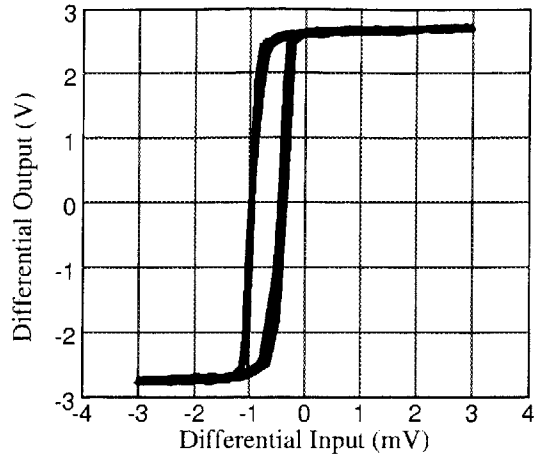


Figure A-9: Transfer characteristic of opamp.

Technology	0.8 $\mu$ m CMOS
Power Supply	3.3 V
Die Size	600 $\mu$ m x 630 $\mu$ m
Power Consumption	4.8mW

Table 9: Chip specifications.

Opamp Specification	Simulation	Measurement
Differential Open Loop Gain (500Hz)	105db	90dB
Differential Output Swing	$\pm$ 2.4V	$\pm$ 2.45V
Unity Gain Frequency (Output Load=3.52pf)	93MHz	90MHz
Phase Margin	78 $^{\circ}$	—
Settling Time (1%; noise gain > 2, Output Load ~ 3.65pF)	17.3ns	26ns
Slew Rate	133mV/ns	125mV/ns
Offset (typical)	9.5mv	1-2mv
CMRR (500Hz)	57dB	>50dB

Table 10: Opamp measured and simulated performance.

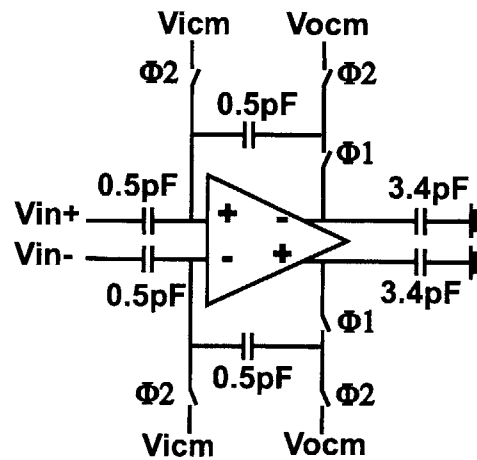
Figure A-9 shows the transfer characteristic of the amplifier. The “hysteresis-type” behavior observed in the curves occurs due to the phase difference between the input and the output of the amplifier at the



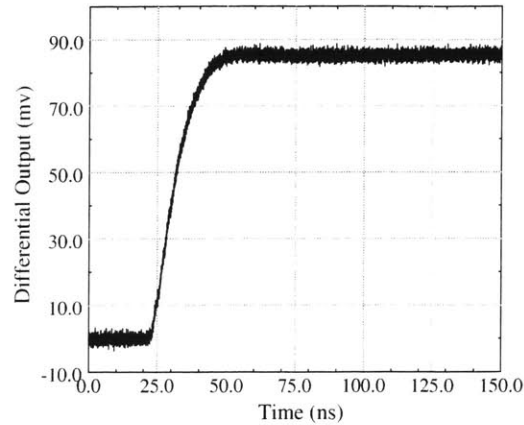
500Hz frequency at which this measurement was taken. The maximum output range and the slope of this characteristic near its mid-point were used to estimate the swing and the differential gain of the amplifier, respectively.

Figure A-10a shows the test circuit employed for measuring the settling time of the amplifier. For this measurement, the opamp was placed in negative feedback using periodically refreshed capacitors in the feedback path. Figure A-10b and Figure A-10c show the measured small signal and large signal step response, respectively, of the amplifier. With a 3.65pF capacitive load and a noise gain of greater than 2, the 1% settling time of the amplifier is measured to be 26ns. The slew rate of the amplifier, as estimated from the large signal step response, is 125mV/ns.

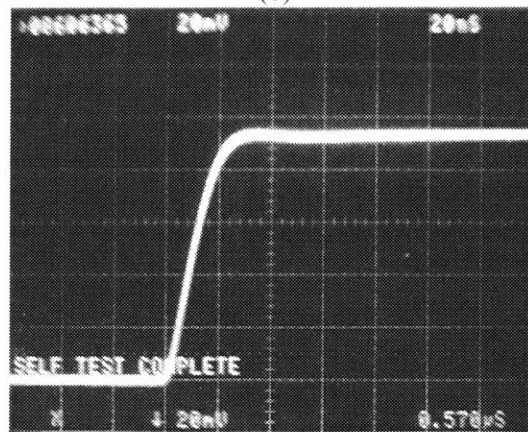
The chip specifications and performance summary are given in Table 9 and Table 10, respectively. The discrepancy between the measured and simulated settling time is attributed to the finite settling time of approximately 10ns (at a 1% precision) of the input waveform itself. The amplifier has a measured differential output swing of  $\pm 2.45\text{V}$  at a voltage supply of 3.3V. The swing of the amplifier has been estimated from the maximum output range at which the amplifier maintains a differential small-signal gain of at least 66dB. At a capacitive loading of 3.52pF, its measured unity gain frequency is 90MHz. The CMRR of the opamp is greater than 50dB and its differential gain is 90dB, both measured at a frequency of 500Hz. Telescopic style opamps typically have a limited input common-mode voltage range. This opamp has a simulated input common-mode voltage range of 220mV about the nominal input common-mode voltage measured at the points where the small-signal differential gain drops to 90% of its nominal value; note, however, that the application of this opamp is in a switched-capacitor environment where the common-mode voltage remains fairly fixed.



(a)



(b)



(c)

Figure A-10: Step response of opamp: (a) Test setup. (b) Small-signal step response. (c) large-signal step response (horz: 20ns/div, vert: 200mV/div considering picoprobe attenuation).

## A.5 Conclusions

With supply voltages becoming more limited, opamp output swing becomes an extremely critical parameter. While the telescopic architecture achieves a superior speed and power consumption, it has a very limited output swing. The proposed design combines the high speed, low-power advantage of the telescopic architecture with the high-swing capability of the folded-cascode and the 2-stage design while maintaining high common-mode and supply rejection, and ensuring constant performance parameters. The techniques we describe are general and can potentially be applied to improve the performance of some other topologies as well. We have experimentally demonstrated an amplifier with an output swing of  $\pm 2.45\text{V}$  at a supply of  $3.3\text{V}$ , a unity-gain frequency of  $90\text{MHz}$  and power consumption of  $4.8\text{mW}$  at a capacitive load of  $3.6\text{pF}$ , and  $>50\text{ dB}$  of CMRR. We have shown, qualitatively and through simulations, that the amplifier maintains its high CMRR even at high frequencies. In the light of ever-decreasing supply voltages, this opamp serves as an attractive alternative to conventional topologies.

## A.6 Appendix

In order to understand the interaction of the replica circuitry with the main amplifier, it is useful to look at the entire transistor level circuitry in the common-mode sense assuming that the input to the amplifier is a pure common-mode signal. Figure A-11 shows the transformation of the full-circuit to its common-mode counterpart. A simplified model for the common-mode circuit is shown in Figure A-12a. The top half shows the model for the main circuit, while the bottom part represents the replica circuitry. For simplicity, the common-mode feedback is not shown here and a first-order model is assumed for the replica circuit. The analysis will first be carried out at dc; the results will then be generalized for all frequencies. The transconductance of the tail and the replica-tail transistors is  $g_t$  and  $g_{rt}$ , respectively, as shown in Figure A-11.  $R_{om}$  is the total common-mode small-signal resistance at the output of the main amplifier, while  $R_{or}$  is the corresponding small-signal resistance at the output of the replica amplifier. The transconductances  $G_m$  and  $G_r$  are the source-degenerated transconductance of the main and replica input devices. The degeneration of the transconductance stems from the non-zero intrinsic small-signal resistance of the main and replica tail transistors. Although, degeneration of the input devices is nominal when the tails are in the deep linear region, this effect has been taken into account for generality. The degenerated transconductances can be approximately expressed as:

$$G_m = \frac{g_m}{1 + g_m \cdot r_t} \quad (\text{A.4})$$

and

$$G_r = \frac{g_r}{1 + g_r \cdot r_{rt}} \quad (\text{A.5})$$

$f_r$  is the feedback factor in the replica-loop that, in this case, represents the gain of the replica amplifier. From this model, the open-loop transfer function of the replica-loop can be written as

$$\frac{v_{or}}{v_{inc}} = \frac{G_r \cdot R_{or}}{1 + f_r \cdot g_{rt} \cdot R_{or}} \quad (\text{A.6})$$

which can simply be obtained using Black's formula. Representing  $v_t$  in terms of  $v_{inc}$  the model in Figure A-12a can be simplified as shown in Figure A-12b. The effective transconductance  $G_e$  of the overall model is

$$G_e = G_m \cdot \left( \frac{1 + A_{loop} \cdot \Delta_{rep}}{1 + A_{loop}} \right) \quad (\text{A.7})$$

where,

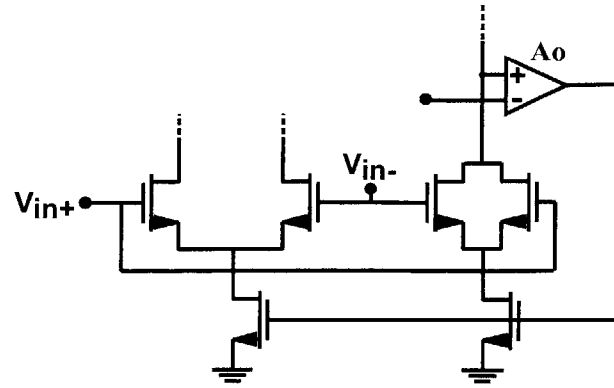
$$A_{loop} = f_r \cdot g_{rt} \cdot R_{or} \quad (\text{A.8})$$

which represents the gain through the replica loop.

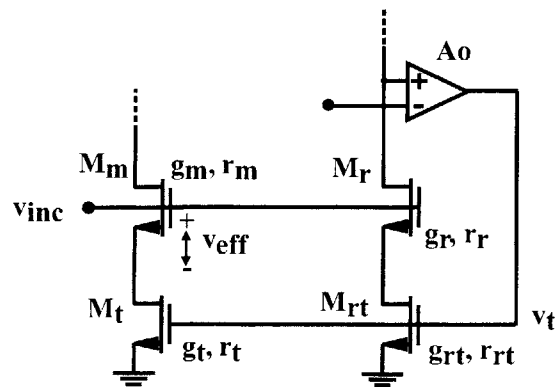
and

$$\Delta_{rep} = 1 - \frac{g_t}{g_{rt}} \cdot \frac{G_r}{G_m} \quad (\text{A.9})$$

Here,  $\Delta_{rep}$  encapsulates the mismatch between the main and the replica circuits.



(a)



(b)

Figure A-11: Differential to common-mode transformation for replica-tail feedback circuit.

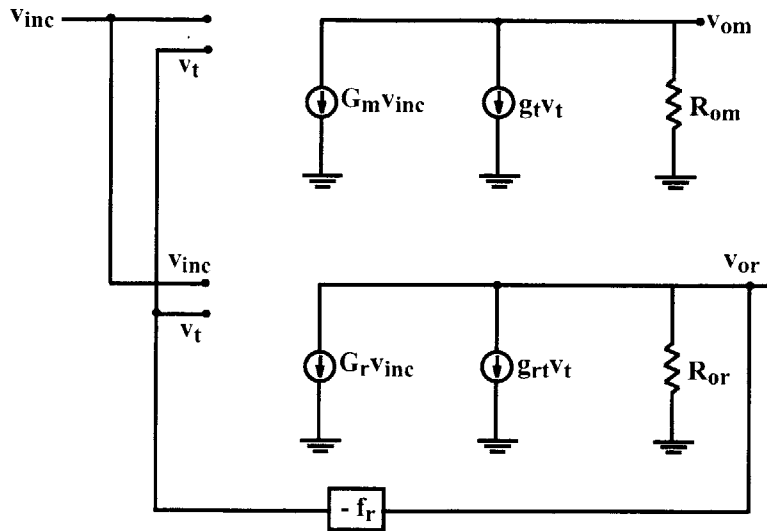
Until now we have shown a model for the common-mode path of the amplifier. To extract the CMRR of the amplifier, note that the common-mode small-signal voltage that eventually appears across the gate-to-source nodes of the main input devices, shown as  $v_{\text{eff}}$  in Figure A-11, for a certain common-mode input voltage  $v_{\text{inc}}$ , can be obtained by referring the common-mode current  $i$  to the voltage across the gate-to-source nodes of the input transistors. Mathematically, this can be expressed as  $v_{\text{eff}} = i / g_m$ , where  $g_m$  is the intrinsic transconductance of the input devices. The transfer function from the input to  $v_{\text{eff}}$  can be written as

$$T = \frac{v_{\text{eff}}}{v_{\text{inc}}} = \left( \frac{1}{1 + g_m \cdot r_t} \right) \cdot \left( \frac{1 + A_{\text{loop}} \cdot \Delta_{\text{rep}}}{1 + A_{\text{loop}}} \right) \quad (\text{A.10})$$

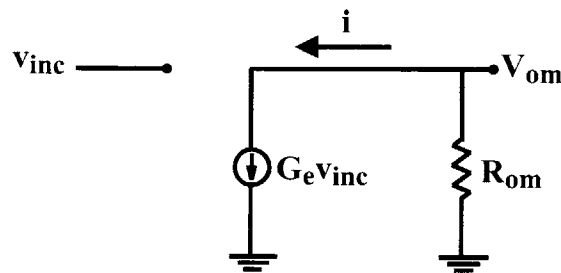
Noting that  $v_{\text{eff}}$  is amplified by the asymmetry in the main input devices to eventually create a differential signal at the output of the opamp, the CMRR of the amplifier is inversely proportional to  $T$ . Rewriting,

$$\text{CMRR} \propto \left(1 + g_m \cdot r_t\right) \cdot \left(\frac{1 + A_{\text{loop}}}{1 + A_{\text{loop}} \cdot \Delta_{\text{rep}}}\right) \quad (\text{A.11})$$

which takes into account both the source degeneration due to the intrinsic resistance of the tail transistor (shown by the 1st term) as well as the CMRR enhancement due to the replica-tail feedback (shown by the 2nd term). The enhancement in CMRR due to the replica circuit can be emulated in an amplifier merely by employing a tail transistor with a larger small-signal resistance  $R_{\text{efftail}}$ . The value of  $R_{\text{efftail}}$  gives us an idea of the effectiveness of the replica-tail circuitry. Using the above expression, the effective tail resistance can be found to be  $R_{\text{efftail}} = R_{\text{tail}} \cdot (1 + A_{\text{loop}})$  for small main-replica mismatch. Thus, the resistance of the tail is enhanced by the loop gain of the replica-loop.



(a)



(b)

Figure A-12: Small-signal model for the common-mode opamp circuit. (b) Simplified common-mode opamp model.

The frequency behavior of the CMRR can be obtained by employing the following transformations

$$A_{\text{loop}} \rightarrow A_{\text{loop}}(s) = \frac{A_{\text{loop}}}{1 + \left( \frac{s}{\omega_{\text{pr}}} \right)}, \quad r_t \rightarrow \frac{r_t}{1 + s \cdot (r_t \cdot C_t)} \quad \text{and} \quad r_{\text{tr}} \rightarrow \frac{r_{\text{tr}}}{1 + s \cdot (r_{\text{tr}} \cdot C_{\text{tr}})} \quad (\text{A.12})$$

where,  $\omega_{\text{pr}}$  is the open loop dominant pole location of the replica circuit, and  $C_t$  and  $C_{\text{tr}}$  are the capacitances across the main and replica tail transistors.

Rewriting,

$$\text{CMRR}(s) \propto \left( 1 + \frac{g_m \cdot r_t}{1 + s \cdot (r_t \cdot C_t)} \right) \cdot \left( \frac{1 + A_{\text{loop}}(s)}{1 + A_{\text{loop}}(s) \cdot \Delta_{\text{rep}}(s)} \right) \quad (\text{A.13})$$

### A.6.1 Case A: Mismatch factor $\Delta = 0$

In this case, the replica-tail feedback enhances the CMRR(s) by  $1 + A_{\text{loop}}(s)$ . In other words, the CMRR of the amplifier is enhanced by the loop gain of the replica circuitry. The overall frequency dependent part of the CMRR can be represented as

$$\text{CMRR}(s) \propto \left( \frac{s + \omega_{\text{zt}}}{s + \omega_{\text{pt}}} \right) \cdot \left( \frac{s + \omega_{\text{zr}}}{s + \omega_{\text{pr}}} \right) \quad (\text{A.14})$$

where,  $\omega_{\text{zt}} = \left( \frac{1 + g_m \cdot r_t}{r_t \cdot c_t} \right)$  and  $\omega_{\text{pt}} = \frac{1}{r_t \cdot c_t}$  are the zero and pole associated with the source degeneration, and  $\omega_{\text{pr}} = \frac{1}{R_{\text{Or}} \cdot C_{\text{Or}}}$  and  $\omega_{\text{zr}} = \omega_{\text{pr}} + \omega_{\text{pr}} \cdot A_{\text{loop}}$  are the pole and zero associated with the replica circuitry. Since, the tail transistors are in the linear region,  $g_m \cdot r_t$  is comparable to unity; therefore,  $\omega_{\text{pt}}$  and  $\omega_{\text{zt}}$  are very closely spaced and hence represent a pole-zero doublet.

### A.6.2 Case B: Mismatch factor $\Delta \gg \frac{1}{A_{\text{loop}}}$

In this case, it is easy to show that the CMRR enhancement due to the replica circuitry is  $\frac{1}{\Delta_{\text{rep}}}$ . The frequency response will contain other poles and zeros as well due to the frequency dependent mismatch between the main and the replica circuitry.

## Appendix B: Signature Analysis – Identifying Pipeline Converter Errors from Measurement Histograms

The goal of this chapter is to provide a method to relate error sources in the pipeline converter to signature patterns in the histogram obtained from the converter using the histogram test as outlined in Chapter 7. As was mentioned earlier, differential non-linearity (DNL) measurements obtained using the histogram can be optimistic because of converter noise. Integral non-linearity (INL) measurements can reflect internal error more accurately. However, INL measurements can be misleading for converters that do not have a monotonic transfer characteristic as is the case for converters employing the popularly used 1.5-bit/stage digital error correction.

This chapter investigates the various high level errors possible in a pipeline converter and determines give-away signature patterns in the output histogram. Armed with a library of these signature patterns, it becomes possible to link observed non-idealities in the histogram to the possible cause of error. In many cases, different high-level errors lead to unique patterns. When they are not unique, this methodology may still be able to isolate potential error candidates. In the latter case, additional tests may be required to pinpoint the actual error.

Section B.1 provides an analysis of residue plots of a standard pipeline converter with the 1.5-bit/stage digital error correction scheme. This section focuses on issues that are important for the eventual determination of the histogram error pattern. Section B.2 details the important non-idealities in a 1.5-bit/stage and their corresponding error patterns.

This analysis is by no means exhaustive, but does provide certain preliminary information and methodology to build a larger library of these error patterns. It is also possible to implement an automated means of correlating observed error patterns with actual errors.

### B.1 Analysis of Pipeline Converter Residue plots

A thorough understanding of the residue plots helps offer insight into how various sources of error in the pipeline converter manifest themselves in the converter output.

Figure B-1 illustrates residue plots of an ideal errorless converter. Figure B-1a shows the residue transfer characteristic for the first stage. This residue plot is identical to the residue plot for any of the other stages. There are two transition points, one at  $+V_{ref}/4$  and the other at  $-V_{ref}/4$ , corresponding to the comparator thresholds. Both the x and y axes range from  $-V_{ref}$  to  $+V_{ref}$  (represented by -1 and +1 in all of the plots in this chapter). Figure B-1b shows the relationship of the residue of the second stage and the converter input. This plot is identical to the transfer characteristic across any two stages of the pipeline. Figure B-1c shows a similar relationship of the residue of the third stage and the converter input that, in turn, is identical to the transfer characteristic across any three stages in the pipeline.

The following are certain key observations from Figure B-1a-c.

### Number of transitions in a residue plot

The first stage has 2 transitions implying that there are 3 segments of the characteristic where  $V_{res1}$  sweeps through the values  $-V_{ref}/2$  to  $+V_{ref}/2$ . The two horizontal lines on the plot correspond to the transition points of the second residue,  $V_{res2}$ . Since three segments of  $V_{res1}$  cross these two horizontal lines, every time the converter input sweeps through from  $-V_{ref}$  to  $+V_{ref}$ , the residue of the second stage  $V_{res2}$  will undergo 6 transitions. This validated by Figure B-1b. The number of transition points of any residue  $V_{res}(j)$ , where  $j$  is the stage number can be determined in the following manner.

If  $T(j)$  is the number of the transition points in a transfer characteristic across  $j$  stages.

$$T(j+1) = 2 \cdot (T(j) + 1) \quad (B.1)$$

Given that  $T(1)$  equals 1, we obtain the following expressions:

$$T(2) = 2 \cdot T(1) + 2 = 2^1 + 2$$

$$T(3) = 2 \cdot T(2) + 2 = 2^3 + 2^2 + 2$$

$$T(4) = 2 \cdot T(3) + 2 = 2^4 + 2^3 + 2^2 + 2$$

or more generally, we can express  $T(j)$  as follows:

$$T(j) = 2^{(j+1)} - 2 \quad (B.2)$$

From this, we determine that  $T(3)=14$ , as is substantiated by Figure B-1c.

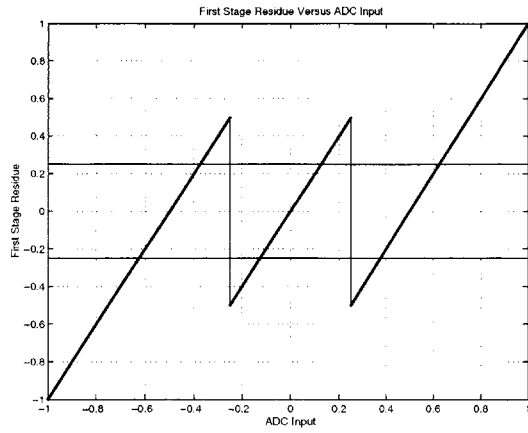
### Nature of transitions

Since each stage transition occurs when the input is at  $-V_{ref}/4$  and  $+V_{ref}/4$ , the stage output at the location of the transition will always involve an output change from  $+V_{ref}/2$  to  $-V_{ref}/2$ . Additionally, all segments in between any two transitions will be linear and contiguous.

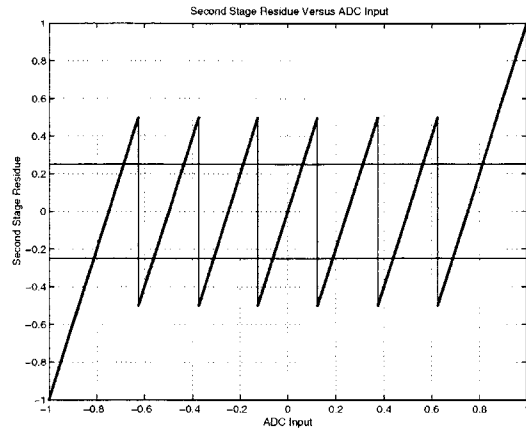
### Location of transitions

Based on the transfer characteristic, the transition of the residue of the second stage with respect to the converter input will be spaced  $\frac{1}{2} \left( \frac{V_{ref}}{4} + \frac{V_{ref}}{4} \right) = \frac{V_{ref}}{4}$  away from each other. More generally, the transitions will be spaced  $\frac{V_{ref}}{2^j}$  away from each other in the case of the transfer characteristic across  $j$  stages. For an  $N$ -bit converter, an input range from  $-V_{ref}$  to  $+V_{ref}$  corresponds to  $2^{(N)}$  output codes. In terms of the output codes, therefore, the spacing  $S$  of these transitions is  $S = \frac{2^{(R-1)}}{2^j} = 2^{(R-j-1)}$ . The closest transitions from the mid-point of the transfer characteristic are  $-S/2$  and  $+S/2$ . Because of symmetry, the  $T(j)$  transitions are distributed equally on either side of the zero crossing.

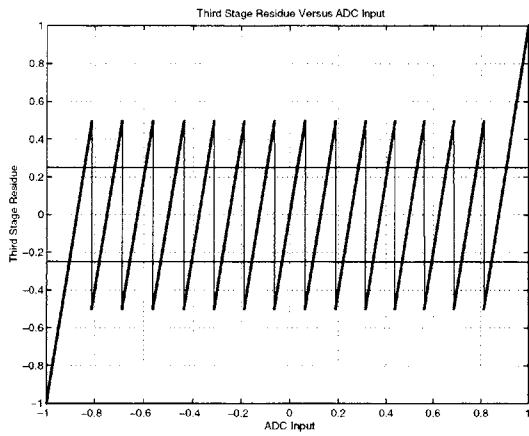




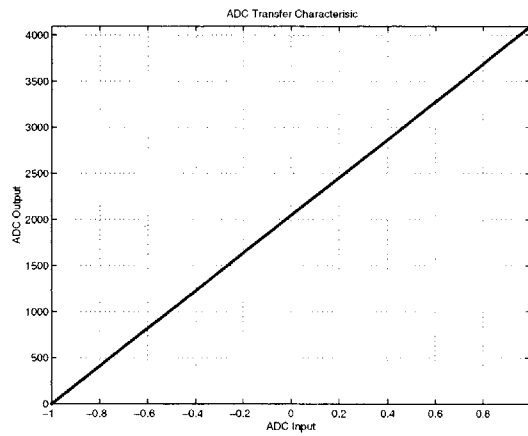
(a)



(b)



(c)



(d)

Figure B-1: (a) Residue plot for Stage 1. (b) Residue plot through Stage 1-2. (c) Residue plot through Stages 1-3. (d) ADC Transfer Characteristic.

**Summary of transition points in the transfer characteristic of the residue of the  $j$ th stage with respect to the converter input**

Number of transition points (T):	$2 \cdot (2^j - 1)$
Spacing (S):	$\frac{V_{\text{ref}}}{2^j}$ (in terms of Vref) or $\frac{2^{(N-1)}}{2^j}$ (in # of codes)
Location:	Symmetrically situated about code $2^{(R-1)}$ (the mid-point code, after offset adjustment) with T/2 on left hand side and T/2 on the right hand side of this code.

## **B.2 Effect of Important Non-idealities**

Non-idealities in the pipeline converter lead to various performance anomalies. One way to analyze these anomalies is by considering the histogram of the digital output. The performance errors of the pipeline converter can be classified into one of the following four fundamental types of errors.

1. Stage offset
2. Stage gain error
3. Stage transition point shift
4. Nonlinear variation of the transfer characteristic

Any practical converter will have a combination of all of the above manifestations, however, it is likely that one of these will be more dominant than others. Each of these above classifications corresponds to certain circuit non-idealities. Some common circuit non-idealities along with the error classification are summarized in the following table.

All of these four fundamental stage errors cause anomalies in the histogram of the output which can be traced back by considering the number, location and spacing of these anomalies and relating them to the number, location and spacing of comparator transition points.

Circuit non-ideality	Comments	Manifestation on residue plot	Diagnosis
Opamp offset		Stage offset	
Charge injection from sampling switch connected to top-plate of capacitor	This error is composed of 2 components.		
	(a) Fixed component	Stage offset	Reduced digital supply.
	(b) Input dependent component	Non-linear variation of the residue plot *	
Differential parasitic capacitance from amplifier inputs and some logic	Logic injects signal into overall transfer characteristic.	Stage offset with magnitude dependent on logic level	Raising logic power supply will change the ADC offset and increase contiguous set of missing codes.
Capacitor Mismatch		Stage gain error	
Overlap between opamp inputs and outputs	Leads to effective capacitor mismatch	Stage gain error	
Reduced opamp gain	Creates error in final opamp settling value	Stage gain error	Reduced bias current.
Common-mode parasitic capacitance from opamp inputs to digital signal	For certain topologies such as the telescopic architecture, can reduce opamp gain	Stage gain error	Changing digital power supply will change the size of the wide code caused by reduced opamp gain.
Excess common-mode charge injection	For certain topologies such as the telescopic architecture, can reduce opamp gain	Stage gain error	Adjust common-mode level.
Incomplete opamp settling	If the settling of the amplifier is of first order type, then incomplete settling essentially corresponds to effective gain reduction if the opamp outputs are pre-charged to a certain fixed value. However in the case when the opamp is shared between stages, that doesn't happen, and the result is more complicated	Stage gain error if settling is first-order and opamp outputs are pre-charged	Slow down ADC or increase bias currents
Comparator offset		Stage transition shift	
Reduced opamp swing	Will cause the residue plot to vary as the tanh of the opamp output (as the opamp gain changes with changing output voltage).	Non-linear variation of residue plot *	Reduction of reference voltage levels.
Not enough points in DNL or histogram analysis	Will cause randomly occurring missing codes that will be more frequent in the middle of the cusp (if we apply a sine wave for the histogram analysis). This effect causes an inverse cusp shape in the DNL i.e. large DNL in the middle and smaller towards the sides where there are more points.	-	Increase number of points

Table 11: Examples of circuit non-idealities and their effect on the stage residue plot.

## B.2.1 Stage offset

Stage offset can arise from a variety of sources as summarized in previous table. With a stage offset of  $V_{os}$  (as referred to the input of that stage), the transfer characteristic of that stage can be written as:

$$V_o = \frac{C_1 + C_2}{C_2} \cdot V_{in} + D_i \cdot \frac{C_1}{C_2} V_{ref} + \frac{C_1 + C_2}{C_2} \cdot V_{os} \quad (\text{B.3})$$

where the value of  $D_i$  is determined as follows:

$$\begin{aligned} D_i &= -1 & \text{for } -V_{ref} < V_{in} < -V_{ref}/4 \\ D_i &= 0 & \text{for } -V_{ref}/4 < V_{os} < V_{ref}/4 \\ D_i &= 1 & \text{for } +V_{ref}/4 < V_{in} < +V_{ref} \end{aligned} \quad (\text{B.4})$$

where the full-scale range is  $2V_{ref}$  and  $V_{os}$  is the input referred stage offset.

There are 2 cases when stage offset can lead to errors:

- Case 1A:  $V_{os} > V_{ref}/4$   
Case 1B:  $V_{os} < -V_{ref}/4$

While these errors are fairly large, these magnitudes are still possible. Graphically the residue plot simply shifts along the vertical axis as shown in

Figure B-2a-c for the first stage residue. As is clear from this plot and the transfer characteristic and output code density (for a ramp input), as long as the absolute value of the offset is lesser than  $V_{ref}/4$ , the stage transfer function remains contained within the maximum bounds and the all this results is in overall stage offset which can be referred back to the ADC input as overall ADC offset.

### Case 1A ( $V_{os} > V_{ref}/4$ )

If, however,  $V_{os}$  is greater than  $V_{ref}/4$  (Case1A), the upper tips of the transfer characteristic (shown in

Figure B-2e reaches the upper bound beyond which the next stage will continue to interpret that value to be  $+V_{ref}$ . In other words, this will lead to a *single wide code* at the digital code corresponding to the position when input to the succeeding stages is  $V_{ref}$ . *Immediately following the wide code are one or more missing codes* depending on how far above  $V_{ref}/4$  the offset is.

At first glance it would seem that the location of the wide/missing codes will occur at  $-V_{ref}/4$  and  $+V_{ref}/4$  in the ADC transfer characteristic; however, note that  $V_{os}$  also shifts the entire transfer characteristic. For a 12-bit converter, when  $V_{os}$  is slightly above  $V_{ref}/4$ , there will be a wide code at  $1535+512=2047$  and at  $2559+512=3071$ , respectively as shown in the

Figure B-2d and

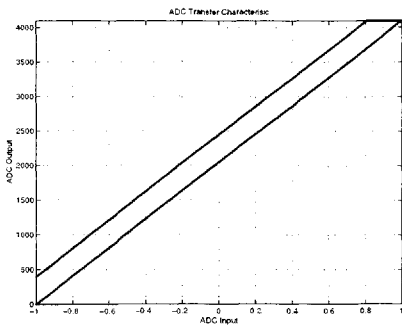
Figure B-2f. As  $V_{os}$  is increased beyond  $V_{ref}/4$ , the wide code appears earlier as seen from the perspective of the ADC input, but the offset is also greater. These two effects cancel out and it just so happens that the wide code always occurs at the same position, the center and the one to its right.

Likewise for offsets in other stages, the spacing between these wide codes is reduced by a certain exponent of 2 depending on the stage number; nevertheless, the input-referred  $V_{os}$  is also divided by the same exponent of 2.

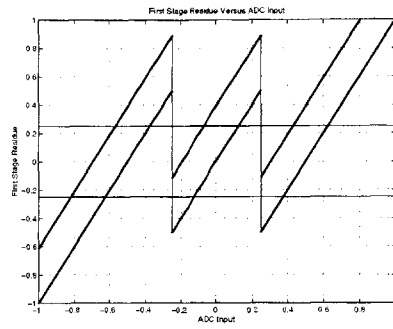
Figure B-2g-i, show the situation for offset in the second stage.

**Case 1B ( $V_{os} < -V_{ref}/4$ )**

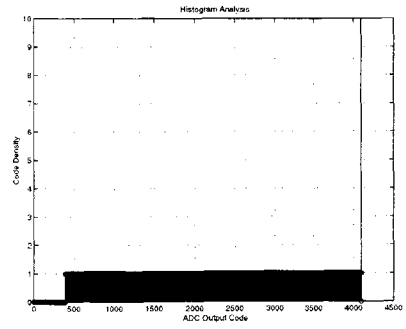
Figure B-3 refers to a similar set of plots except for the case when  $V_{os} < -V_{ref}/4$ . *Here the single wide code occurrences are preceded by a contiguous set of missing codes.*



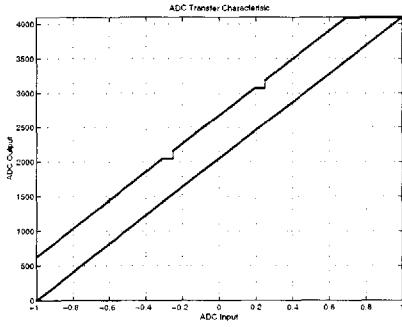
(a)



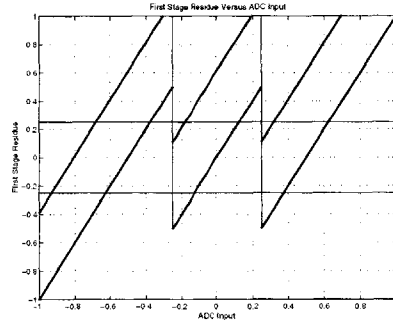
(b)



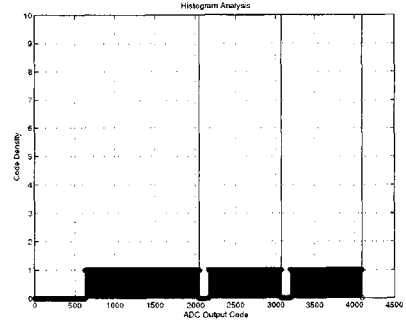
(c)



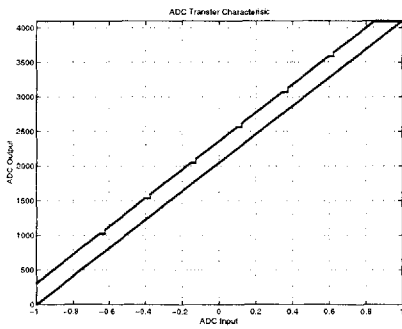
(d)



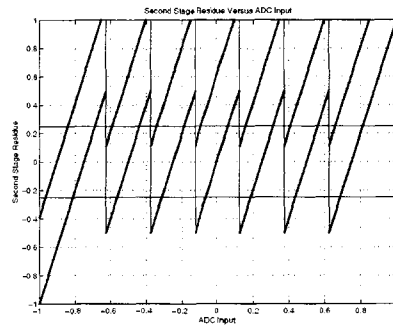
(e)



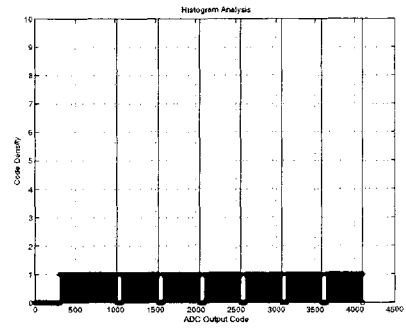
(f)



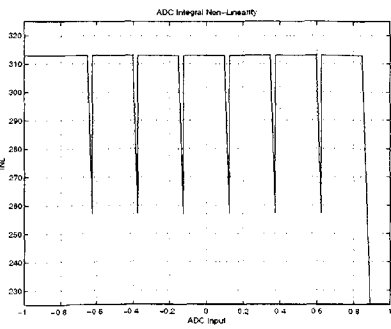
(g)



(h)

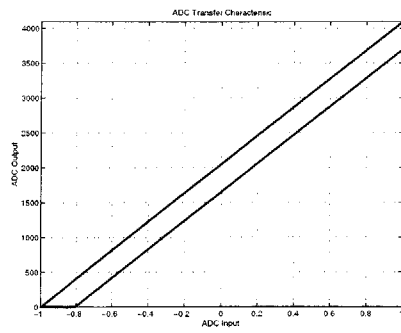


(i)

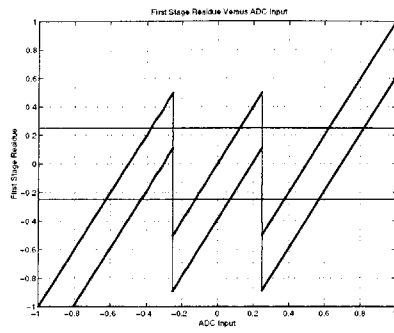


(j)

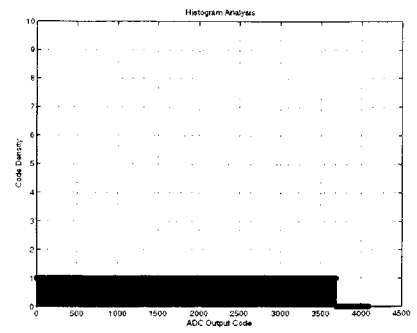
Figure B-2: Transfer Characteristic, residue plot and code density for a ramp input, respectively, for (a)-(c)  $0 < V_{os} < V_{ref}/4$  in the 1<sup>st</sup> stage. (d)-(f) Case 1A:  $V_{os} > V_{ref}/4$  in the 1<sup>st</sup> stage. (g)-(i) Case 1A:  $V_{os} > V_{ref}/4$  in the 2<sup>nd</sup> stage. (j) INL for previous case.



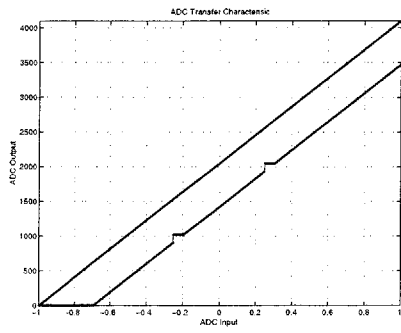
(a)



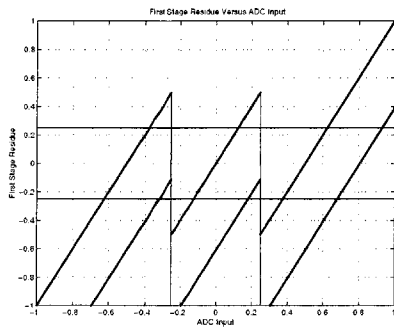
(b)



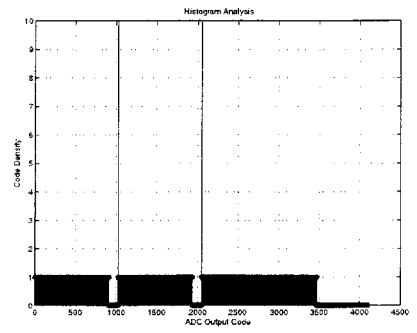
(c)



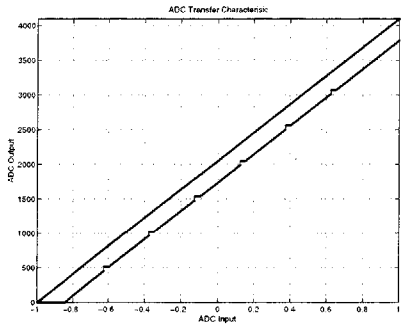
(d)



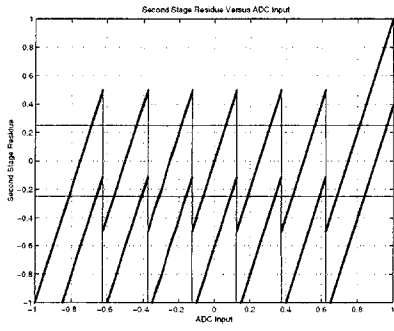
(e)



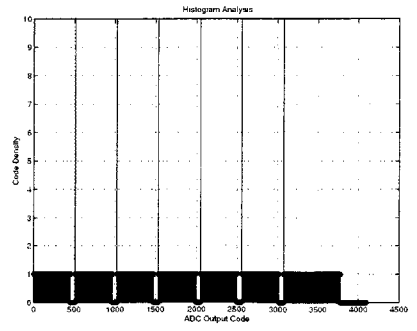
(f)



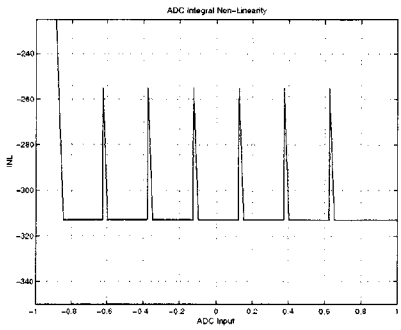
(g)



(h)



(i)



(j)

Figure B-3: Transfer Characteristic, residue plots and code density for a ramp input, respectively, for (a)-(c) –  $-V_{ref}/4 < V_{os} < 0$  in the 1<sup>st</sup> stage. (d)-(f) Case 1B:  $V_{os} < -V_{ref}/4$  in the 1<sup>st</sup> stage. (g)-(i) Case 1B:  $V_{os} < -V_{ref}/4$  in the 2<sup>nd</sup> stage. (j) INL for previous case.



## B.2.2 Stage Gain Error

There are three primary forms of stage gain error that originate from different circuit non-idealities. These can be mathematically described in the following manner:

$$\begin{aligned}
 \text{Class I: } & V_o = (2+\epsilon) \cdot V_{in} + (1+\epsilon) \cdot D_i \cdot V_{ref} \\
 \text{Class II: } & V_o = (2+2\epsilon) \cdot V_{in} + (1+\epsilon) \cdot D_i \cdot V_{ref} \\
 \text{Class III: } & V_o = (2+2\epsilon) \cdot V_{in} + D_i \cdot V_{ref}
 \end{aligned} \tag{B.5}$$

where  $D_i$  is +1,0 or -1 depending on location of  $V_{in}$  relative to certain thresholds. The above classes of errors lead to completely different error patterns in the output histogram.

### Class I type gain error

**Sources of class I type stage gain error:** This class of gain error can arise from at least two different types of circuit non-idealities:

#### (a) Capacitor Mismatch

A pipeline converter stage is governed by the following transfer function:

$$V_o = \frac{C_1 + C_2}{C_2} \cdot V_{in} + D_i \cdot \frac{C_1}{C_2} V_{ref} \tag{B.6}$$

For the case when  $C_1 = C(1+\epsilon)$  and  $C_2 = C$ , we obtain the transfer relationship as shown in Class I in Equation at the top of this section(A.1). Here the error  $\epsilon$  can be positive or negative.

#### (b) Incomplete opamp settling with opamp sharing

This applies to only the condition when the opamp is being shared between the previous stage (the (i-1)th stage) and this stage (the ith stage). When the opamp is shared, and its output is not reset between the two phases, the output of the opamp has to slew from its previous phase output to its new value. The error due to incomplete opamp settling therefore is dependent on the *difference* between the new and old output values. For the case when the opamp is being shared between the previous stage and this stage, the opamp output in the previous phase is  $V_{in}$ . Hence the net error due to incomplete opamp settling can be written as:

$$\begin{aligned}
 \epsilon' &= (V_o - V_{in}) \cdot \epsilon = \left( \frac{C_1 + C_2}{C_2} \cdot V_{in} + D_i \cdot \frac{C_1}{C_2} V_{ref} - V_{in} \right) \cdot \epsilon \\
 \text{or } \epsilon' &= \left( \frac{C_1}{C_2} \cdot V_{in} + D_i \cdot \frac{C_1}{C_2} V_{ref} \right) \cdot \epsilon
 \end{aligned} \tag{B.7}$$

Combining this with the previous equation, we obtain  $V_o = (2+\epsilon) \cdot V_{in} + (1+\epsilon) \cdot V_{ref}$ , which fits the Class I type gain error. Of course, for this circuit error  $\epsilon$  is negative.

**Classification of class I type stage gain error:** Class I gain error can be sub-divided into three cases based on the polarity and magnitude of the error. Each of these cases leads to a different result. These have been classified in terms of the transfer function gain  $g$ , where  $g = 2 + \epsilon$ .

**Case 2IA:**  $2 < g < 8/3$

**Case 2IB:**  $4/3 < g < 2$

**Case 2IC:**  $g > 8/3$

Figure B-4a-c shows case A in the first stage, while Figure B-4d-g shows the same type of mismatch in the second stage. Figure B-5a-c shows case B in the first stage, while Figure B-5d-g shows the same type of mismatch in the second stage. Likewise, Figure B-6a-c shows case C in the first stage, while Figure B-6d-g shows the same type of mismatch in the second stage. Note that the magnitude of errors considered in these figures is deliberately large in order to be able to illustrate the effect graphically.

### Case 2IA

Consider a key observation to aid in drawing the residue plots for this class of gain error. There are three values of the converter input that will always generate the same value at the output of all the stages, regardless of the magnitude of the error. These are  $-V_{ref}$ , 0 and  $+V_{ref}$ . In other words, these points in the input map to the same values in the stage outputs. As an example, if  $V_{dcin}=0$ ,  $V_{res}(i)=0$  for  $i=1:N$ , where  $N$  is the number of stages of the pipeline corresponding to the resolution of the converter. Another observation to note is that for an ideal stage the output of that stage changes abruptly from  $+V_{ref}/2$  to  $-V_{ref}/2$ .

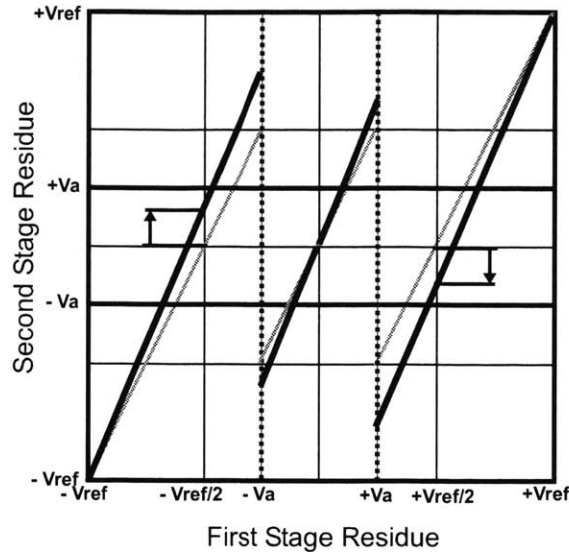
**Gain error in the first stage:** Consider the Figure B-4a-c for this type of gain error. The positive gain error will cause the stage transfer characteristic to have a slope greater than the ideal slope of 2. Combining this result with the observation above leads us to the residue plot shown in Figure B-4b. This corresponds to a non-monotonic converter transfer characteristic leading to wide codes.

These wide codes will have a density that is double that of the average code density, as shown in the histogram in Figure B-4c. In this case, the sets of wide codes will approximately occur at the transition points of this stage, or in other words, at codes corresponding to  $\pm V_{ref}/4$  from the mid-point.

A more detailed analysis shows, however, while the codes corresponding to the transition points lie within the contiguous set of wide codes, it does not actually coincide with the center of this set of wide codes. This observation can be gleaned directly from the residue plot in Figure B-4b. Considering the transition point that occurs at  $-V_{ref}/4$ , note that the discrepancy between the non-ideal and ideal characteristics will be three times larger on the immediate left of the transition as compared to the discrepancy on the right of the transition. Consider the implication of this fact on the set of wide codes that is located on the left of the mid point. If  $L$  is the width of one of the contiguous set of wide codes, the transition point is located exactly  $L/4$  codes right of the center of the set. For the set on the right of the mid-point, however, transition point is located exactly  $L/4$  codes left of the center of the set. This is graphically illustrated in Figure B-7a.

**Gain error in the second stage:** Consider the Figure B-4d-f for this type of gain error. This is slightly trickier to analyze. Consider Figure B-4e for this analysis. As in the previous case, there will clearly be wide codes at the six transition points in the transfer characteristic from the converter input to the second stage residue. The exact locations are visually shown in Figure B-7b. In addition to wide codes, however, there are also two contiguous sets of missing codes corresponding to the transition points of the *previous* stage. The reason for the presence of these missing codes becomes clear when we realize that precisely at the transition points of the previous stage (the first stage, in this case), the output of that stage changes

abruptly from  $+V_{ref}/2$  to  $-V_{ref}/2$ . For these values, this stage will output values that differ from the ideal outputs as shown in the figure below. This causes a finite discontinuity leading to missing codes.



### Case 2IB

For the case when the gain error is negative, all the results will be similar to the positive gain error case with the missing codes replaced by wide codes and vice versa. For gain error in the first stage, this is graphically depicted in Figure B-5a-c as well as Figure B-7d, while the corresponding figure for error in the second stage is shown in Figure B-5d-f and Figure B-7e.

### Case 3IC

The third case involves gain error that are very large ( $g > 8/3$ ). While this may not be commonly found in converters, they are, nevertheless, possible under catastrophic situations or through some mechanism that hasn't been considered in this chapter.

**Gain error in the first stage:** Consider the Figure B-6a-c for this type of gain error. As the input gain is increased, the contiguous set of wide codes continues to increase in width. Eventually at an input gain of  $8/3$ , the residue plot will saturate the next stage. At this point, the contiguous set of wide codes on either side of the mid-point will merge. If the input gain is increased beyond  $8/3$ , two codes about the mid-point will become extra wide, and continue to grow as the input gain increases. Hence we obtain the histogram of Figure B-6c.

**Gain error in the second stage:** Consider the Figure B-6d-f for this type of gain error. For the same type of error in the second stage, the 6 set of wide codes corresponding to the transitions of this stage will merge to form 3 sets of wide codes, with 2 extra wide codes corresponding to  $-V_{ref}/2$ , 0 and  $V_{ref}/2$ . A detailed graphical depiction of this case is shown in Figure B-7c

## Class II type gain error

**Sources of class II type stage gain error:** This class of gain error can arise from at least two different types of circuit non-idealities:

- (a) **Input dependent charge injection in the sample-and-hold of the next stage (the (i+1)st stage)**
- (b) **Incomplete opamp settling (no opamp sharing)**

In both these cases, the overall transfer characteristic will be governed by the following transfer function:

$$V_o = (2 \cdot V_{in} + D_i \cdot V_{ref}) \cdot (1 + \epsilon) \quad (\text{B.8})$$

where  $D_i$  is +1, 0 or -1 depending on location of  $V_{in}$  relative to certain thresholds. This conforms to the Class II type error. Both these circuit errors will yield a negative  $\epsilon$ .

**Classification of class II type stage gain error:** Class II gain error can be sub-divided into two cases based on the polarity of the error.

- Case 2IIA:**  $\epsilon < 0$
- Case 2IIB:**  $0 < \epsilon < 1$

Figure B-8a-c shows case A in the first stage, while Figure B-8d-f shows the same type of mismatch in the second stage. Figure B-9a-c shows case B in the first stage, while Figure B-9d-g shows the same type of mismatch in the second stage. Note that there can be a third subdivision where  $\epsilon > 1$ , however, since this is unlikely to happen, it hasn't been considered here.

### Case 2IIA

This will lead to contiguous sets of missing codes that are *centered* on the transition points of the stage in which the Class II type error is located. The width of each set, of course, depends on the magnitude of gain error.

### Case 2IIB

This will lead to contiguous sets of wide codes that are *centered* on the transition points of the stage in which the Class II type error is located. The code density of these wide codes is double the average code density. Again, the width of each set depends on the magnitude of gain error.

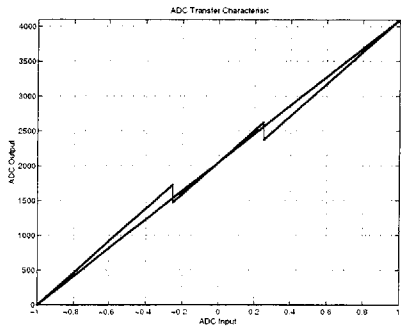
### **Class III type gain error**

**Sources of class III type stage gain error:** The linear component of input dependent charge injection in the sample-and-hold of the first stage can cause this class of gain error. The overall transfer characteristic in this error is governed by the following transfer function:

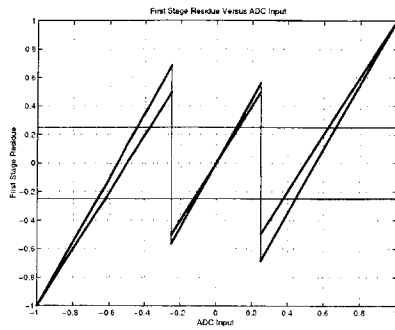
$$V_o = (2 + 2\epsilon) \cdot V_{in} + D_i \cdot V_{ref} \quad (\text{B.9})$$

where  $D_i$  is +1, 0 or -1 depending on location of  $V_{in}$  relative to certain thresholds.

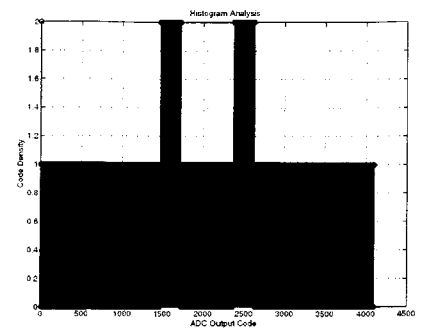
This type of error will only change the overall gain of the converter transfer function. It will not introduce any non-linearity in the transfer characteristic.



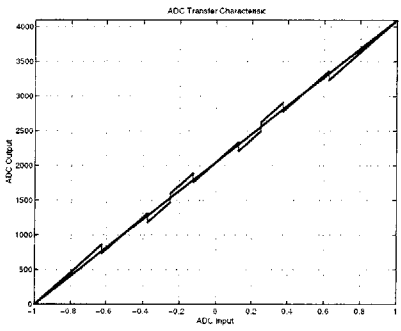
(a)



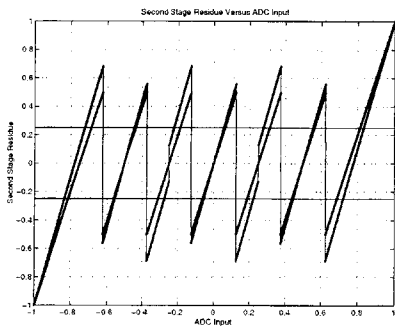
(b)



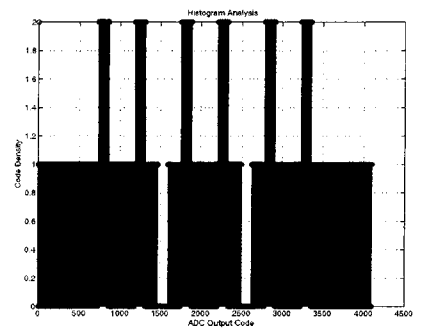
(c)



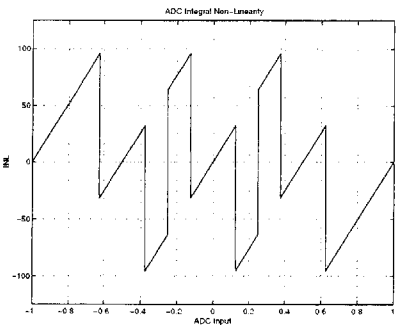
(d)



(e)

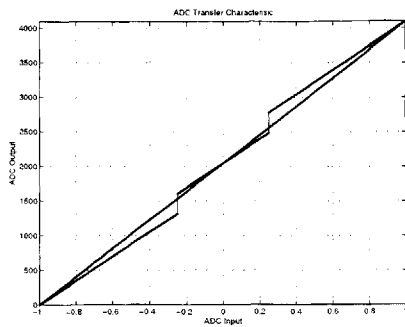


(f)

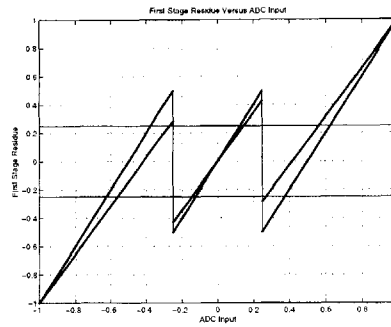


(g)

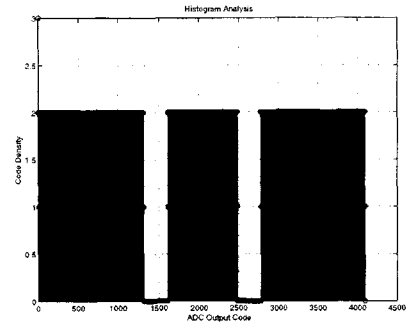
Figure B-4: Transfer Characteristic, residue plot and code density for a ramp input, respectively, for  $2 < g < 8/3$  (Case 2IA) (a)-(c) mismatch in 1<sup>st</sup> stage. (d)-(f) mismatch in 2<sup>nd</sup> stage. (g) INL for previous case. Here  $g=2.2$ .



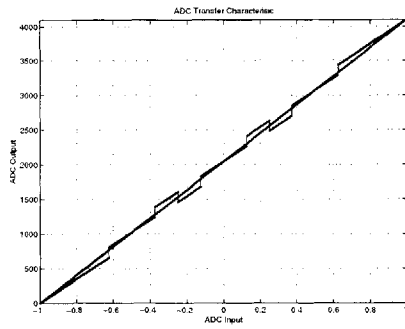
(a)



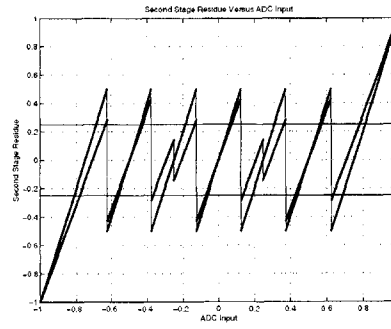
(b)



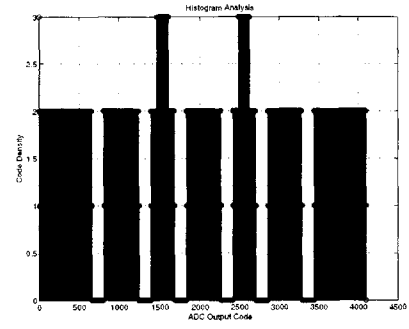
(c)



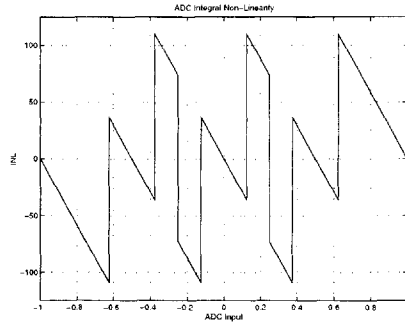
(d)



(e)



(f)



(g)

Figure B-5: Transfer Characteristic, residue plot and code density for a ramp input, respectively, for  $4/3 < g < 2$  (Case 2IB) (a)-(c) mismatch in 1<sup>st</sup> stage. (d)-(f) mismatch in 2<sup>nd</sup> stage. (g) INL for previous case. Here  $g=0.7143$ .

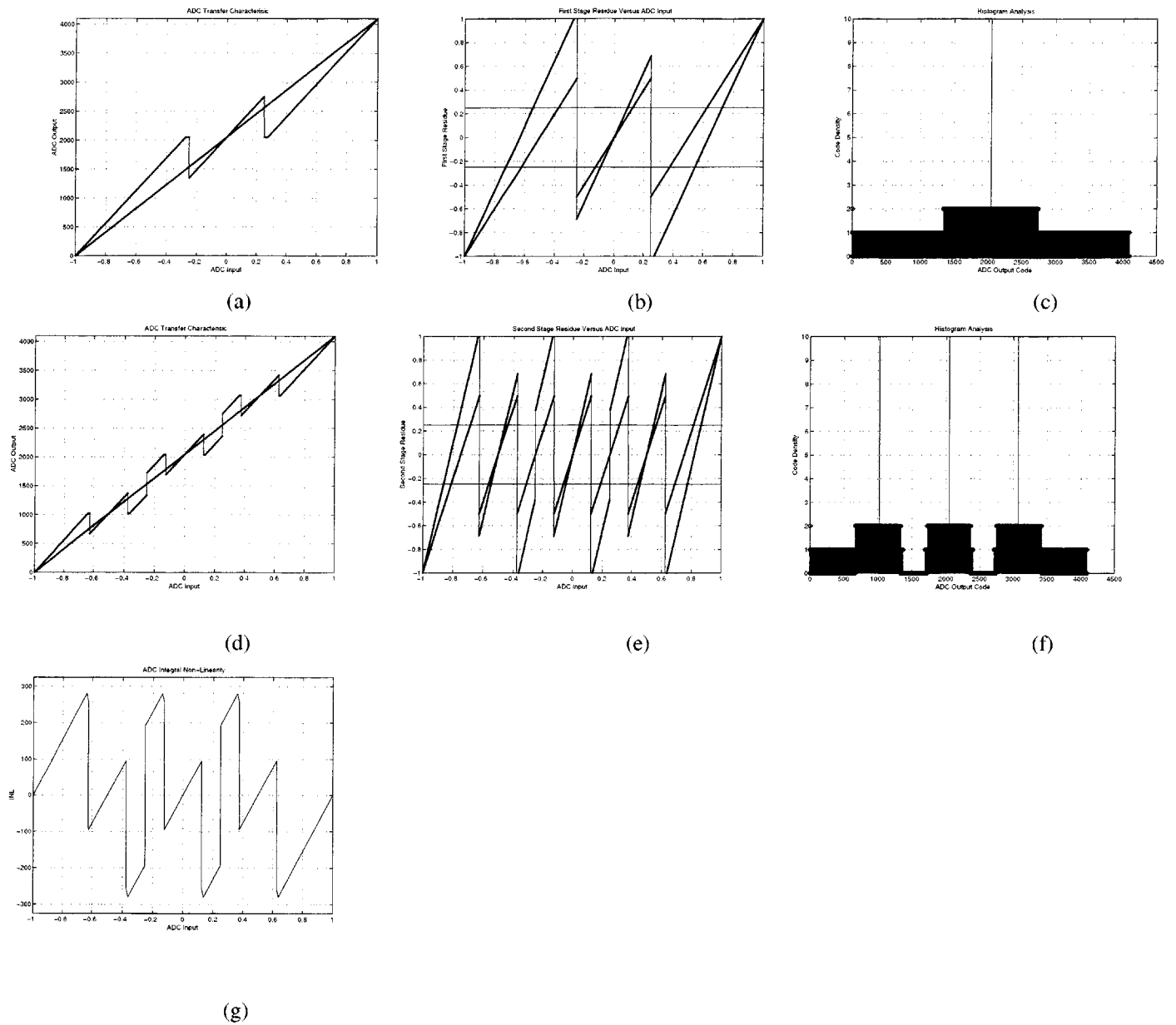


Figure B-6: Transfer Characteristic, residue plot and code density for a ramp input, respectively, for  $g > 8/3$  (Case 2IC) (a)-(c) mismatch in 1<sup>st</sup> stage. (d)-(f) mismatch in 2<sup>nd</sup> stage. (g) INL for previous case. Here  $g=2.7544$ .



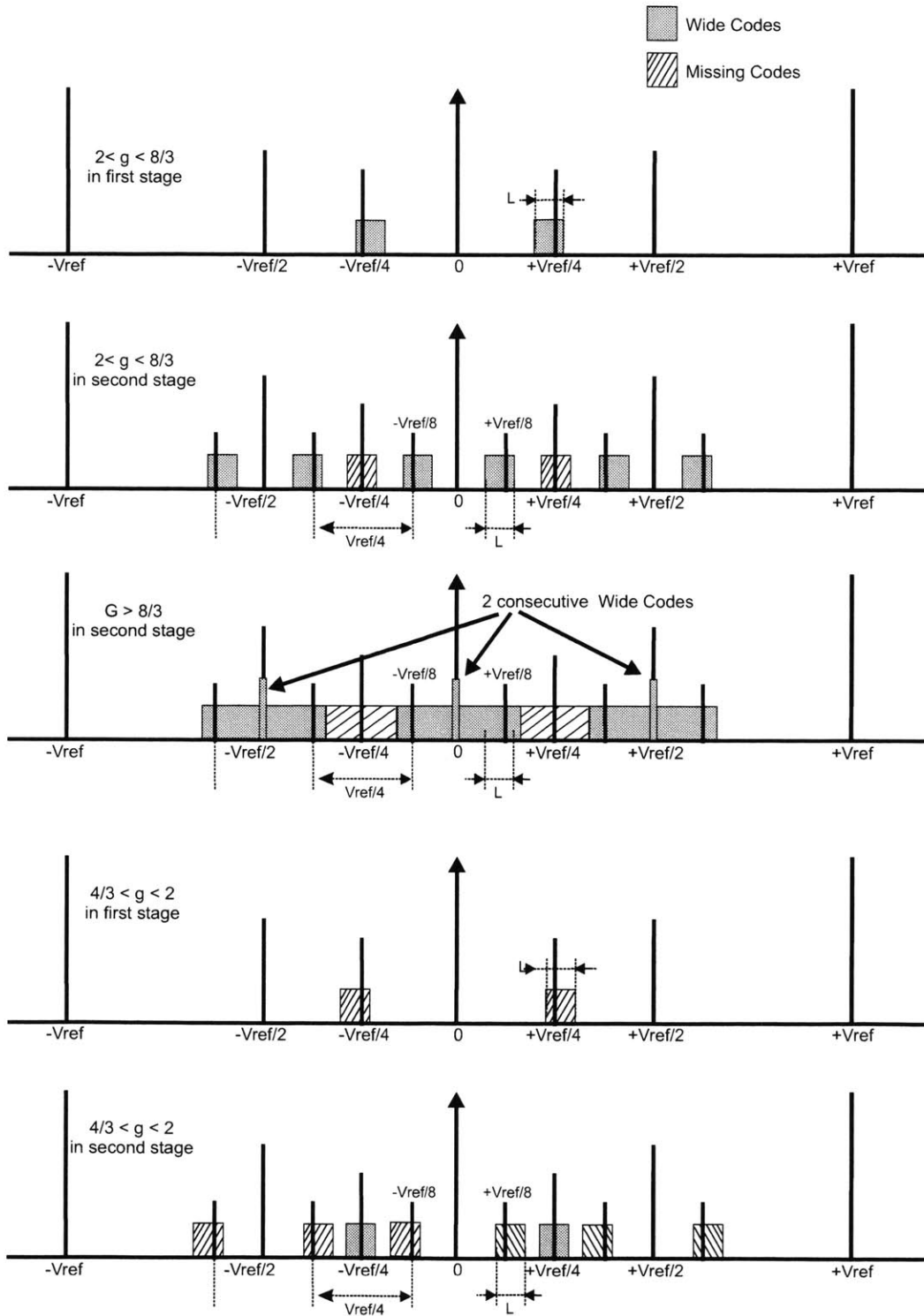
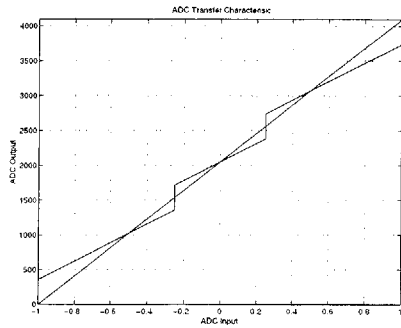
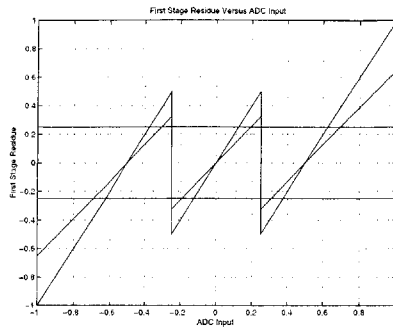


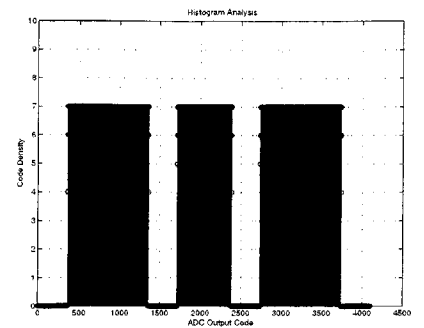
Figure B-7: Output Code Density in various cases. (a)  $2 < g < 8/3$  in 1<sup>st</sup> stage. (b)  $2 < g < 8/3$  in 2<sup>nd</sup> stage. (c)  $g > 8/3$  in 2<sup>nd</sup> stage. (d)  $4/3 < g < 2$  in 1<sup>st</sup> stage. (e)  $4/3 < g < 2$  in 2<sup>nd</sup> stage.



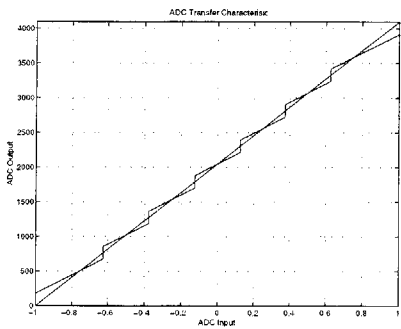
(a)



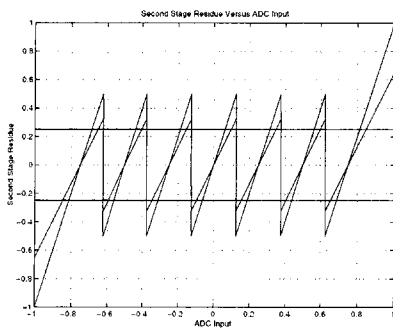
(b)



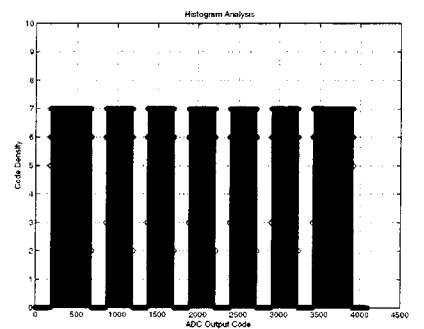
(c)



(d)

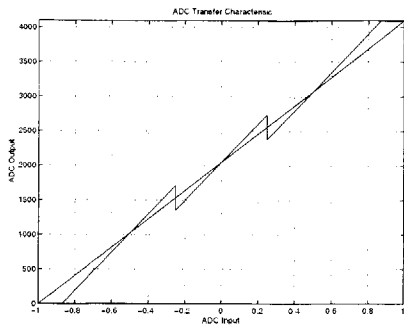


(e)

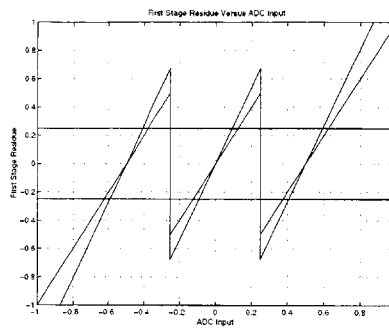


(f)

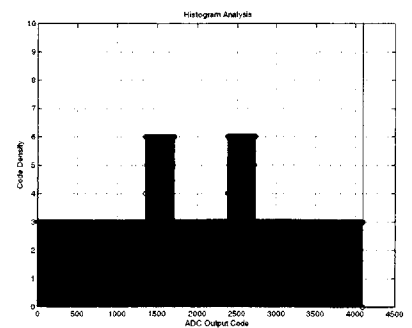
Figure B-8: Transfer Characteristic, residue plot and code density for a ramp input, respectively, for  $\epsilon < 0$  (Case 2IIA) (a)-(c) mismatch in 1<sup>st</sup> stage. (d)-(f) mismatch in 2<sup>nd</sup> stage. Here  $\epsilon = -0.35$ .



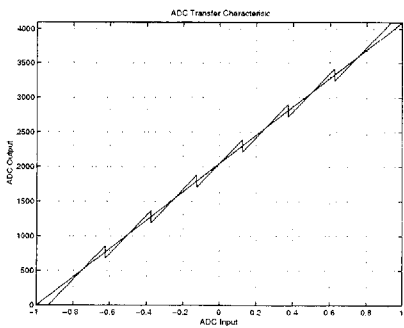
(a)



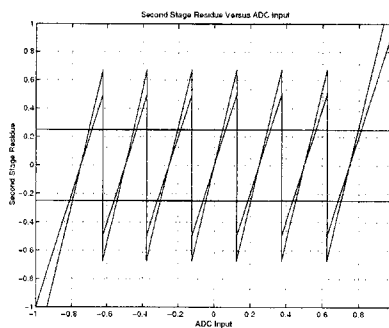
(b)



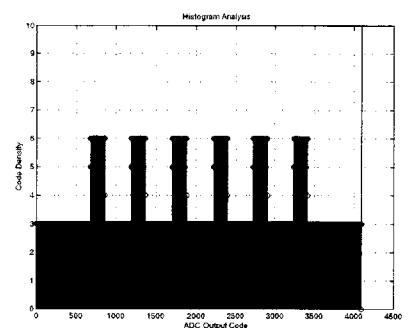
(c)



(d)



(e)



(f)

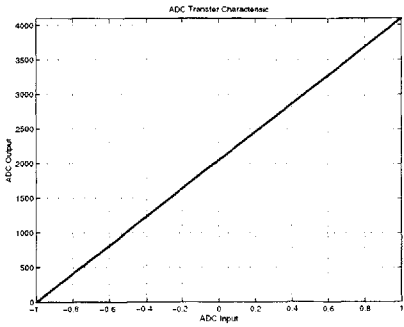
Figure B-9: Transfer Characteristic, residue plot and code density for a ramp input, respectively, for  $\epsilon > 0$  (Case 2IIB) (a)-(c) mismatch in 1<sup>st</sup> stage. (d)-(f) mismatch in 2<sup>nd</sup> stage. Here  $\epsilon = 0.35$ .

### B.2.3 Stage Transition Shift

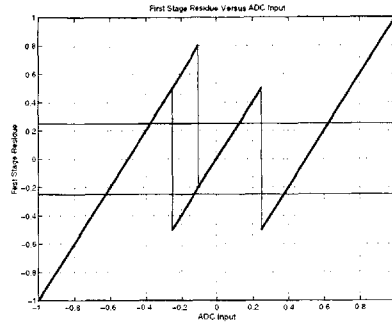
As the name implies, here the location of the stage transition shifts. This can happen through comparator offset. There are four sub-divisions for this type of error. Here  $V_{transhift1}$  and  $V_{transhift2}$  refer to the shift of first and second transition points, respectively.

- Case 3A:  $0 < V_{transhift1} < V_{ref}/4$
- Case 3B:  $V_{transhift1} > V_{ref}/4$
- Case 3C:  $-V_{ref}/4 < V_{transhift2} < 0$
- Case 3D:  $V_{transhift2} < -V_{ref}/4$

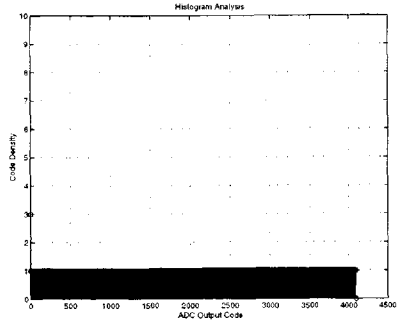
Figure B-10 and Figure B-11 illustrate the effect of transition point shifts on the output code density. Note that this shift will cause errors only for cases 3B and 3D. When a transition shift and any other error described earlier occur simultaneously, the location of the histogram error events will also shift correspondingly.



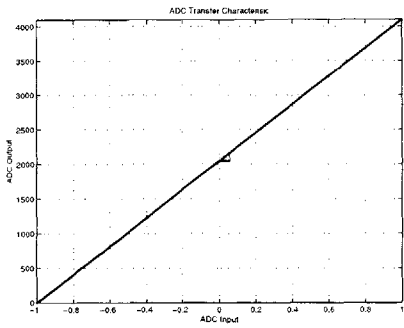
(a)



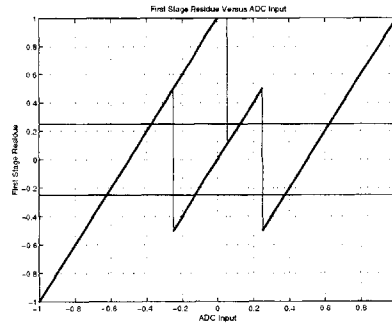
(b)



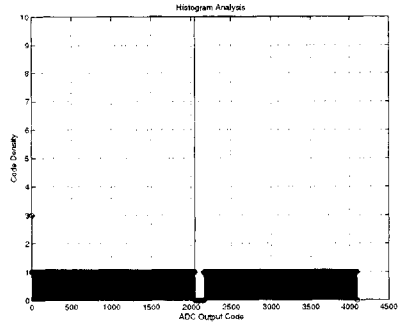
(c)



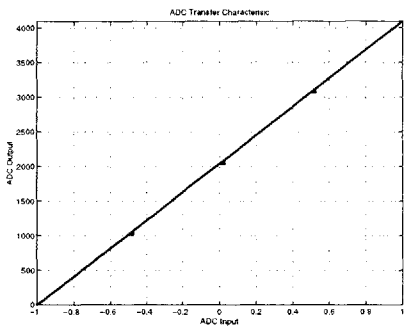
(d)



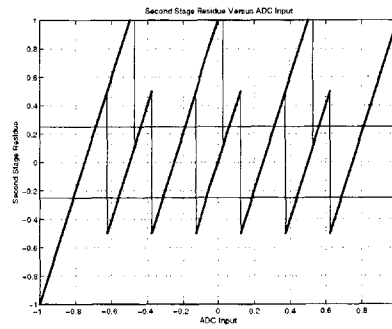
(e)



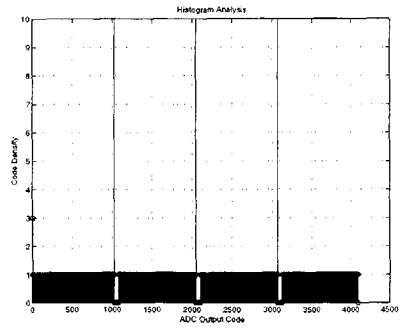
(f)



(g)

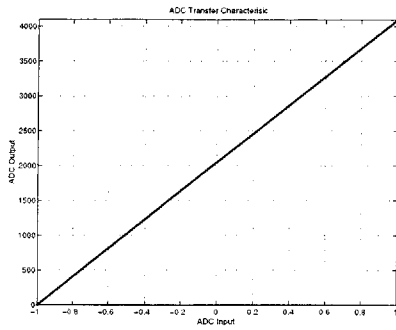


(h)

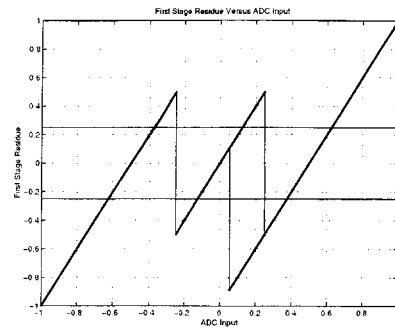


(i)

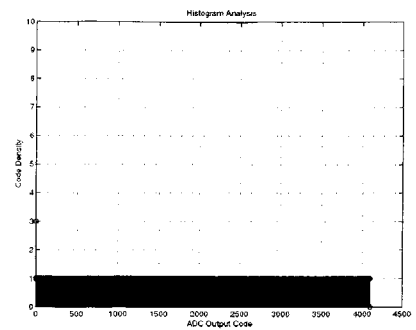
Figure B-10: Transfer Characteristic, residue plot and code density for a ramp input, respectively, for (a)-(c):  $0 < V_{\text{transhift1}} < V_{\text{ref}}/4$  (Case 3A). (d)-(f):  $V_{\text{transhift1}} > V_{\text{ref}}/4$  (Case3B) in 1<sup>st</sup> stage. (g)-(i):  $V_{\text{transhift1}} > V_{\text{ref}}/4$  (Case3B) in 2<sup>nd</sup> stage.



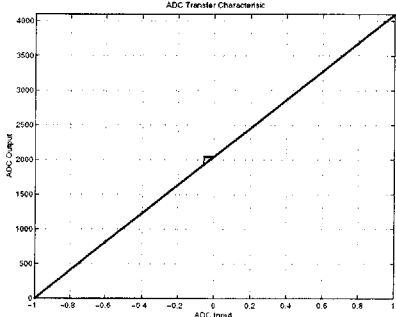
(a)



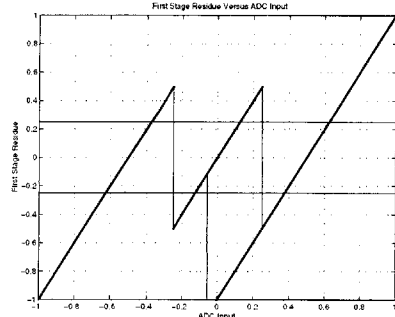
(b)



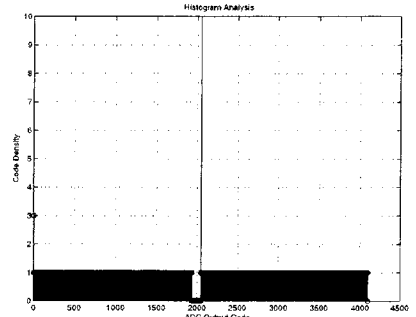
(c)



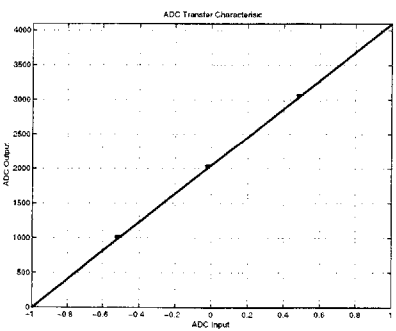
(d)



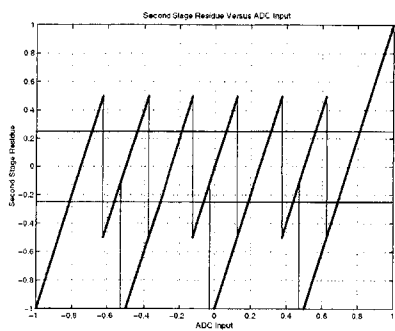
(e)



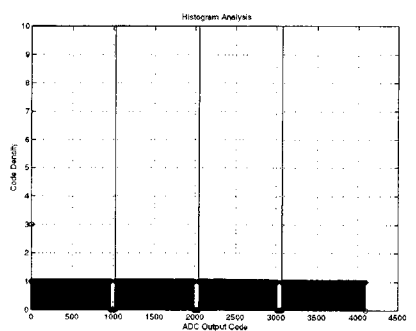
(f)



(g)



(h)



(i)

Figure B-11: Transfer Characteristic, residue plot and code density for a ramp input, respectively, for (a)-(c):  $-V_{ref}/4 < V_{transhift2} < 0$  (Case 3C). (d)-(f):  $V_{transhift2} < -V_{ref}/4$  (Case3D) in 1<sup>st</sup> stage. (g)-(i)  $V_{transhift2} < -V_{ref}/4$  (Case3D) in 2<sup>nd</sup> stage.

## **B.2.4 Non-linear variation of stage transfer characteristic**

This type of error will lead to histogram anomalies similar to those obtained for stage gain error. The difference is that the segments in-between the error events will be non-linear in nature.

### Characteristics of the Code Density Error for Basic Pipeline Anomalies

\*Approximate location because of the fact that the sets are not centered on the transition points. For exact location see Fig. 6.  $j$  refers to stage number. Missing or wide codes due to the following errors located at the edges of the voltage range are not considered for determining number of error events.

Case No.	Non-ideality on Residue Plot	Nature	Number of error events (M):	Spacing (in terms of) Signal range=2Vref.		Location
				Vref	Codes	
<b>1</b>	<b>Stage Offset (before ADC offset compensation), Vos is stage offset referred to input of that stage.</b>					
1A	$V_{os} > V_{ref}/4$	1 wide code <i>followed</i> by one or more missing codes.	$2 \cdot (2^j - 1)$	$\frac{V_{ref}}{2^j}$	$\frac{2^{(N-1)}}{2^j}$	One occurrence at $2^{(N-1)} - 1$ (one left of mid-point code) with M/2-1 on left hand side of this code and M/2 on the right hand side of this code.
1B	$V_{os} < -V_{ref}/4$	1 wide code <i>preceded</i> by one or more missing codes.	$2 \cdot (2^j - 1)$	$\frac{V_{ref}}{2^j}$	$\frac{2^{(N-1)}}{2^j}$	One occurrence at $2^{(N-1)}$ (mid-point code) with M/2 on left hand side of this code and M/2-1 on the right hand side of this code.
<b>2I</b>	<b>Stage Gain Error – Class I (locations estimated after ADC offset compensation)</b>					
2IA	$2 < g < 8/3$					
	Wide codes	One or more contiguous wide codes in each set.	$2 \cdot (2^j - 1)$	$\frac{V_{ref}}{2^j} *$	$\frac{2^{(N-1)}}{2^j} *$	The wide codes are symmetrically situated about code $2^{(N-1)}$ (the mid-point code, after offset adjustment) with M/2 on left hand side and M/2 on the right hand side of this code. The locations <i>correspond to but are not centered</i> on the transition points of this stage.
	Missing codes	One or more contiguous missing codes in each set. (Length of this set equal to length of wide code set)	$2 \cdot (2^{(j-1)} - 1)$	$\frac{V_{ref}}{2^{(j-1)}}$	$\frac{2^{(N-1)}}{2^{(j-1)}}$	The missing codes are symmetrically situated about code $2^{(N-1)}$ (the mid-point code, after offset adjustment) with M/2 on left hand side and M/2 on the right hand side of this code. The locations correspond to the transition points of the previous stage. The transition points are <i>located exactly in the center</i> of the missing code sets.
2IB	$4/3 < g < 2$					



	Missing codes	One or more contiguous missing codes in each set.	$2 \cdot (2^j - 1)$	$\frac{V_{\text{ref}}}{2^j} *$	$\frac{2^{(N-1)}}{2^j} *$	The missing codes are symmetrically situated about code $2^{(N-1)}$ (the mid-point code, after offset adjustment) with $M/2$ on left hand side and $M/2$ on the right hand side of this code. The locations <i>correspond to but are not centered on the transition points</i> of this stage.
	Wide codes	One or more contiguous wide codes in each set. (Length of this set equal to length of missing code set)	$2 \cdot (2^{(j-1)} - 1)$	$\frac{V_{\text{ref}}}{2^{(j-1)}}$	$\frac{2^{(N-1)}}{2^{(j-1)}}$	The wide codes are symmetrically situated about code $2^{(N-1)}$ (the mid-point code, after offset adjustment) with $M/2$ on left hand side and $M/2$ on the right hand side of this code. The locations correspond to the transition points of the previous stage. The transition points <i>are located exactly in the center</i> of the wide code sets.
2IC	$g > 8/3$					
	Super-wide codes	2 contiguous wide codes in each set.	$(2^j - 1)$	$\frac{V_{\text{ref}}}{2^{(j-1)}}$	$\frac{2^{(N-1)}}{2^{(j-1)}}$	The wide code sets are symmetrically situated about code $2^{(N-1)}$ (the mid-point code, after offset adjustment) with $M/2 - 1$ on left hand side and $M/2 - 1$ on the right hand side of this code and one in the center.
	Wide codes	One or more contiguous wide codes in each set.	$(2^j - 1)$	$\frac{V_{\text{ref}}}{2^{(j-1)}}$	$\frac{2^{(N-1)}}{2^{(j-1)}}$	The wide code sets are symmetrically situated about code $2^{(N-1)}$ (the mid-point code, after offset adjustment) with $M/2 - 1$ on left hand side and $M/2 - 1$ on the right hand side of this code and one in the center.
	Missing codes	One or more contiguous missing codes in each set. (Length of this set less than or equal to length of wide code set)	$2 \cdot (2^{(j-1)} - 1)$	$\frac{V_{\text{ref}}}{2^{(j-1)}}$	$\frac{2^{(N-1)}}{2^{(j-1)}}$	The missing code sets are symmetrically situated about code $2^{(N-1)}$ (the mid-point code, after offset adjustment) with $M/2$ on left hand side and $M/2$ on the right hand side of this code. The locations correspond to the transition points of the previous stage. The transition points <i>are located exactly in the center</i> of the missing code sets.
<b>2II</b>	<b>Stage Gain Error – Class II (locations estimated after ADC offset compensation)</b>					
2IIA	$\epsilon < 0$					
	Missing codes	One or more contiguous missing codes in each set.	$2 \cdot (2^j - 1)$	$\frac{V_{\text{ref}}}{2^j}$	$\frac{2^{(N-1)}}{2^j}$	The missing codes are symmetrically situated about code $2^{(N-1)}$ (the mid-point code, after offset adjustment) with $M/2$ on left hand side and $M/2$ on the right hand side of this code. The locations <i>are centered on the transition points</i> of this stage.
2IIB	$0 < \epsilon < 1$					

	Wide codes	One or more contiguous wide codes in each set.	$2 \cdot (2^j - 1)$	$\frac{V_{ref}}{2^j}$	$\frac{2^{(N-1)}}{2^j}$	The wide codes are symmetrically situated about code $2^{(N-1)}$ (the mid-point code, after offset adjustment) with $M/2$ on left hand side and $M/2$ on the right hand side of this code. The locations <i>are centered on the transition points</i> of this stage.
<b>2III</b>	<b>Stage Gain Error – Class III</b>					
	Any $\in$	No wide or missing codes	-	-	-	-
<b>3</b>	<b>Stage Transition Shift</b>					
3A	$0 < V_{transhift1} < V_{ref}/4$	No error				
3B	$V_{transhift1} > V_{ref}/4$	1 wide code <i>followed</i> by a contiguous set of missing codes	$(2^j - 1)$	$\frac{V_{ref}}{2^{(j-1)}}$	$\frac{2^{(N-1)}}{2^{(j-1)}}$	$2^{(N-1)} - 1$ and symmetrically located about this point
3C	$V_{ref}/4 < V_{transhift2} < 0$	No error				
3D	$V_{transhift2} < -V_{ref}/4$	1 wide code <i>preceded</i> by a contiguous set of missing codes	$(2^j - 1)$	$\frac{V_{ref}}{2^{(j-1)}}$	$\frac{2^{(N-1)}}{2^{(j-1)}}$	$2^{(N-1)}$ and symmetrically located about this point
<b>4</b>	<b>Non-linear Characteristic</b>					
	Similar to Type 2 error					

# Appendix C: Troubleshooting – Minimizing Testing Artifacts

This chapter focuses on artifacts that show up in converter measurement data that do not reflect on the actual performance of the converter. One such artifact is the presence of spurious spikes as found on the FFT measurement of the converter that simply arises due to certain repetitive patterns that may occur because the relationship between the sampling frequency and input frequency may satisfy certain conditions. The following discussion is intended to explain this phenomenon. The latter part of this chapter also includes a discussion on the location of higher order harmonics of the input signal and some of their properties.

## Types of sampling

On the basis of the relationship between the sampling frequency  $F_s$  and the input frequency  $F_{in}$ , we find two fundamental classes: coherent and incoherent sampling [60][61][62][63][64].

### (a) Coherent Sampling

Sampling is considered coherent if the ratio of  $F_{in}/F_s$  is rational *and* number of sine wave periods in the data record equals an integer multiple. In other words the following expression should be satisfied:

$$\frac{F_{in}}{F_s} = \frac{M}{N} \quad (C.1)$$

where,  $F_{in}$  is the input frequency,

$F_s$  is the sampling frequency

$N$  is an integer equal to the total number of samples in the data record

$M$  is an integer equal to the total number of sine wave cycles in the data record

Coherent sampling automatically implies that the data record has an integer number of sine wave cycles – which means that the end points of the data record are continuous from the perspective of sine wave periodicity. In the event that the data record end points are continuous, the sine wave component in the FFT of the data record will occupy only one bin. In such a case, multiplying the raw data with a window is not necessary. Although strictly speaking, taking a finite set of data points is tantamount to using a rectangular window with an apparently infinite set of data.

Nonetheless, it is important to note that for true coherent sampling to take place, the input signal and the clock signal must be locked to the same time base. One way to achieve this is to create these different signals off a master clock or signal. If the time bases of the two generators are not locked, even small frequency drifts will lead to discontinuous end points and hence non-coherent sampling [12].

### (b) Incoherent sampling

Sampling is considered non-coherent if the ratio  $F_{in}/F_s$  is not rational and hence cannot be expressed as a ratio of integers, or if the total number of sine wave periods in the data record does not equal an integer.

#### Origin and Location of Spurious Spikes

It is imperative that the samples in the data record be non-repetitive. Repetitive data can be injected into the data record because of the amplitude quantization of the converter for certain input /clock frequency relationships. Under these conditions, the quantization noise is no longer white but concentrated in digital frequency bins corresponding to the frequency of the patterns [61]. These will appear as spurious peaks leading to misleading spurious-free-dynamic-range (SFDR). These spurious tones can also lie on the harmonics of the input signal leading to reduced signal-to-distortion ratio (SDR).

To illustrate and quantify these patterns, consider the following example.

Let  $F_{in} = 200\text{kHz}$   
 $F_s = 2048\text{ kHz}$   
 $N$  (total number of samples in data record) =  $2^{17}$

Then using the previous equation ,  $M$  (the input frequency bin) = 12800.

First reduce the ratio  $\frac{M}{N}$  to the ratio of minimum integers (cancel out common factors to make this an irreducible ratio).

$$\frac{F_{in}}{F_s} = \frac{M}{N} \rightarrow \frac{m}{n} \quad (C.2)$$

where,  $m, n \in \text{int}$  with no common factors.

Here  $m$  sine wave periods would equal  $n$  sampling periods implying that there are quantization noise patterns every  $m$  sine wave periods. For the above example,

$$\frac{m}{n} = \frac{25}{256}$$

A closed form means of expressing this quantization noise periodicity,  $K$ , is:

$$K = \frac{\text{LCM}(M,N)}{N} \quad (C.3)$$

Here,  $K$  is the number of sine periods corresponding to one quantization noise period,  $\text{LCM}(M,N)^3$  is the least common multiple of  $M$  and  $N$ .  $\text{LCM}(M,N)$  is found to be  $2^{17} \times 5^2$ . Thus,

---

<sup>3</sup>  $\text{LCM}(M,N)$  can be found as follows:

$$M=12800=2^9 \times 5^2$$

$$N=2^{17} \times 5^0$$

Take each common factor to the maximum exponent and multiply them together.

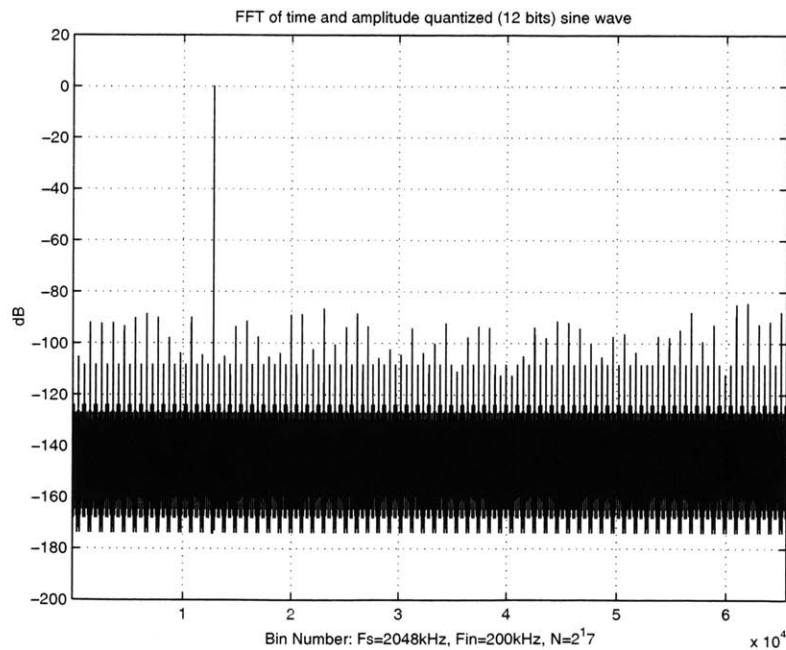
$$K = \frac{\text{LCM}(M, N)}{N} = \frac{2^{17} \times 5^2}{2^{17}} = 25$$

Since the input occupies bin number 12800, the quantization noise pattern corresponds to the  $12800/25=512^{\text{th}}$  bin. From above, the quantization noise will be concentrated at bins corresponding to multiples of 512 leading to spurious peaks at these digital frequencies. Varying the converter resolution will not change these spurious spike bin locations, but will cause different amounts of noise to be allocated to each of these bins.

### Reduction of Quantization Noise Correlation

If we restrict M to be odd or prime, since N is a power of 2 there will no common factors between M and N. In this case,  $\text{LCM}(M, N) = M \times N$ . Thus the smallest quantization noise period will correspond to  $\frac{\text{LCM}(M, N)}{N}$  sine wave periods or M sine wave periods. Since there are only M sine wave periods in the entire record, there no quantization noise patterns in the entire record! Figure C-1 illustrates the effect of proper selection of the input frequency.

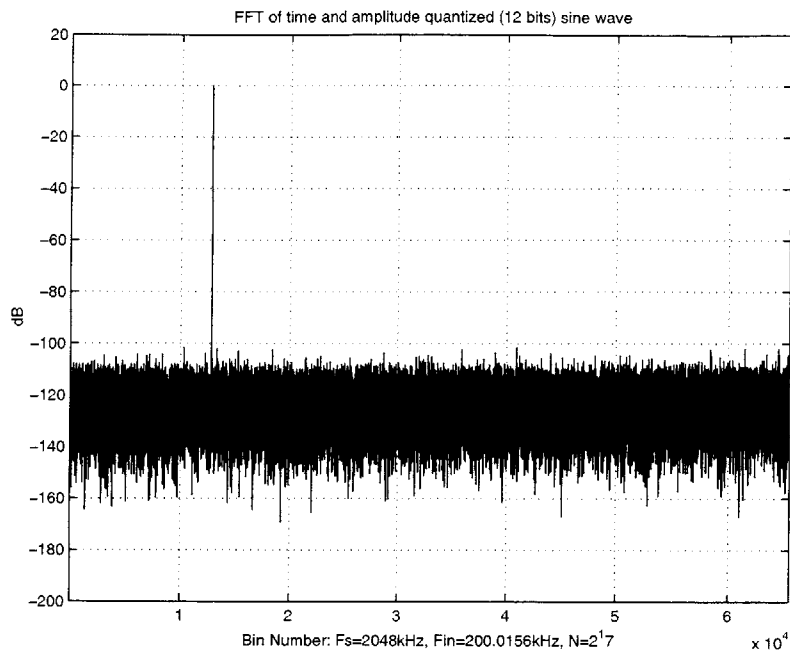
Note: N needs be a power of 2 only to be able to employ the FFT algorithm (for speed). Generally speaking, N does not have to be a power of 2. In this case, M needs to be prime in order to ensure that there are no common factors between M and N.



(a)

---

So  $\text{LCM}(M, N) = 2^{\max(9,17)} \times 5^{\max(2,0)} = 2^{17} \times 5^2$



(b)

Figure C-1: FFT of idealized amplitude quantized sampled sine waveform. (a) With  $M=12800$  and  $N=2^{17}$ . The quantization noise patterns are clearly visible at bin numbers 512 and its multiples. The SNDR obtained from above was 76.3dB. (b) With  $M=12801$  and  $N=2^{17}$ . ( $F_{in} = F_s/N * M = 12801 * 2048 / 2^{17} = 200.0156\text{kHz}$ ). Note that the spurious tones have vanished! Interestingly, the SNDR obtained in this case decreases to 75.7dB, although, the distortion has improved vastly.

MATLAB (VERSION 5.3.1.29215a, Sep 28, 1999, for PCs) CODE FOR IMPLEMENTING FFT TESTS WITH IDEALIZED SINE WAVES

```

%Testing the FFT
%* by doing an FFT of an idealized Sine wave and checking the noise floor
%* varying the resolution R of the quantized sine wave and seeing the noise floor until
%   it doesn't reduce anymore (i.e. limited by MATLAB noise.
%*   Observing effect of various values of Fin and Fs on the presence of spurious peaks
in the
%   FFT of the ideally time and amplitude quantized sine wave.

clear
cd d:\users\kush\labview\MAIN\THEORY
%enter all frequencies in Khz
fs=2048          %||| input
%fin=200.0156    %||| input
fin=200          %||| input

N=2^17; f=(fin/fs)*N;

%Creating Time quantized Sine wave (but continuous in amplitude)
n=1:1:N;
x=sin(2*pi*n/(N/f));          %time quantized signal only
fftx=fft(x.*hanning(N)/(N/4));

figure(1000), plot(linspace(1,N/2,N/2), 20*log10(abs(fftx(1:N/2))));
title('FFT of time quantized sine wave only');
grid
axis([1 N/2 -370 20]);
ylabel('dB')
xlabel('Bin Number: Fs=2048kHz, Fin=200kHz, N=2^17')

%-----
%Quantizing the amplitude of the time quantized signal
R=12;
q=2/2^R;
vq=floor(x/q);          %process of quantizing the signal!! The signal ranges from +2^(R-1) to -
2^(R-1)
vq=vq*q;                %Scaling back the quantized signal to fall within +1 and -1

fftvq=fft(vq.*hanning(N)/(N/4));

figure(1002), plot(linspace(1,N/2,N/2), 20*log10(abs(fftvq(1:N/2))));
title('FFT of time and amplitude quantized (12 bits) sine wave');
grid
axis([1 N/2 -200 20]);
ylabel('dB')
xlabel('Bin Number: Fs=2048kHz, Fin=200kHz, N=2^17')
expectednoiselevel=-(6.02*R+1.76+10*log10(N/2))
%-----
fB=N/2; f=(fin/fs)*N;
cd d:\users\kush\labview\MAIN\datamatlabpipe
s ndr=calculatesNDRnodc_pipe(fftvq(1:fB),f)

cd d:\users\kush\labview\MAIN\THEORY

figure(1000); print('-deps', '-tiff',
['D:\users\kush\labview\MAIN\THEORY\idealtimesampled.eps'])
figure(1001); print('-deps', '-tiff',
['D:\users\kush\labview\MAIN\THEORY\idealtimesampled.eps'])

```

### For guaranteed N bit signal-to-noise ratio, more than N converter bits are required

To obtain a noise floor corresponding to N bits, it is imperative to have greater than N bits generated from the converter. Consider a zero input test on a 12-bit converter. If the converter offset is such that the DC level is perched close to a converter decision level – in other words, close to the middle of an analog LSB, then even the smallest of thermal or other converter noise will cause the least-significant-bit (LSB) to flip randomly. For such condition, data with the LSB flipping randomly can correspond to a range of noise amplitudes ranging from near zero to as high as 2 analog LSBs (until the noise amplitude reaches the next decision level)! FFT of data (12 bits wide) with the LSB flipping randomly will yield, at best, a noise floor of about 67dB below the full-scale signal tone.

Of course, if the DC level is perched in between two decision levels, the signal-to-noise ratio will be higher, with its best value depending on the converter noise

This fact has been verified through MATLAB. Data with randomly flipping LSB was generated artificially using the 'rand' facility in MATLAB. This function creates uniformly distributed random numbers between 0 and 1.

Figure C-2 shows the FFT of the above data. The raw data is  $2^{17}$  points long and flips between the codes 2008 and 2009 (on a scale of 0 to 4096 codes corresponding to a 12-bit converter). The noise floor was found to be  $-67.5\text{dB}$  below the 0dB reference level (that corresponds to a full-scale input tone, if it were present).

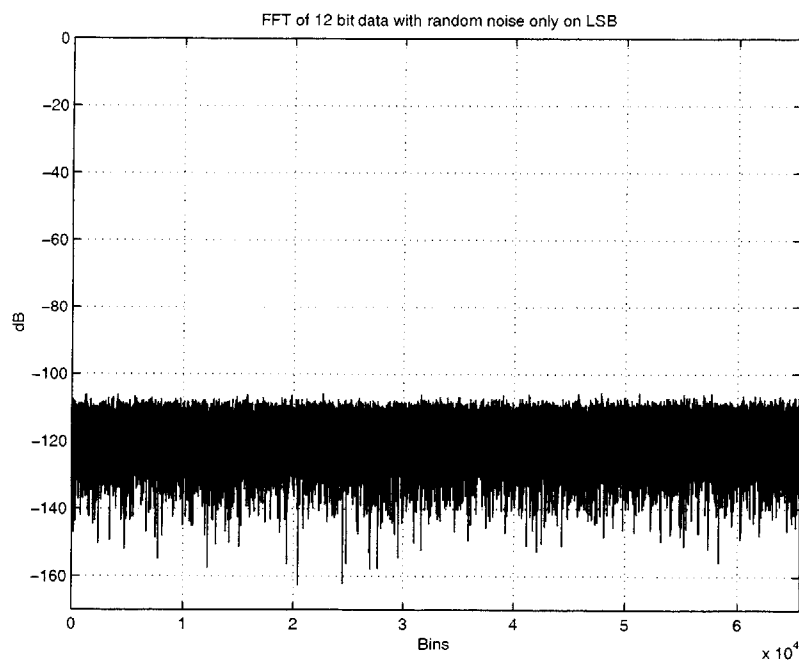


Figure C-2: FFT of data with noisy least-significant bit. The noise-floor is at  $-67.5\text{dB}$ .



## Synchronizing the input and the clock

For obtaining coherent sampling as described above, the input signal and the clock signals must be synchronized to the same time base. This can be achieved by feeding the time base output (10MHz) signal of the generator that provides the clock signal to the time base input of the generator that provides the converter tone. To be able to observe the clock and the input signal on the scope the scope was triggered off the *slower* signal.

## Closed form solution for determining location of all aliased and un-aliased harmonics of the signal fundamental.

This section presents a closed form methodology for determining the location and order of the higher order harmonics that lie within the frequency range from 0 to  $F_s/2$ .

Given any sine wave with frequency  $F$  sampled at  $F_s$ , where  $N$  is the length of the total record, the bin location of the input frequency can always be represented as follows:

$$\text{bin}(F) = j \cdot N \pm \text{bin}(\Delta) \quad (\text{C.4})$$

where,  $|\text{bin}(\Delta)| \leq \frac{N}{2}$  and represents the bin of the input harmonic that lies in the 0 to  $F_s/2$  range.

$\text{bin}(\ )$  refers to the bin corresponding to the argument. The bin location of all aliased frequency harmonics of the fundamental is represented by  $\text{bin}(\Delta)$  and can be written as:

$$N \cdot \left| \text{round}\left(\frac{\text{bin}(F)}{N}\right) - \frac{\text{bin}(F)}{N} \right| \quad (\text{C.5})$$

### Proof:

Replace  $\text{bin}(F)$  with  $j \cdot N \pm \text{bin}(\Delta)$

$$\begin{aligned} \text{Thus } & N \cdot \left| \text{round}\left(\frac{\text{bin}(F)}{N}\right) - \frac{\text{bin}(F)}{N} \right| \\ \rightarrow & N \cdot \left| \text{round}\left(\frac{j \cdot N \pm \text{bin}(\Delta)}{N}\right) - \frac{j \cdot N \pm \text{bin}(\Delta)}{N} \right| \\ \rightarrow & N \cdot \left| j - \left( j \pm \frac{\text{bin}(\Delta)}{N} \right) \right| \\ \rightarrow & N \cdot \left| \frac{\pm \text{bin}(\Delta)}{N} \right| \\ \rightarrow & \text{bin}(\Delta) \end{aligned}$$

### Corollary:

For any given input signal  $F$ , there is one and only one aliased version that falls within the range from 0 to  $F_s/2$ .

**Proof:**

The aliased versions of  $F$  can be represented as :

$$\pm k \cdot F_s \pm F, \text{ for } k \geq 1$$

Here,  $F > \frac{F_s}{2}$  for it was not, no aliasing would take place, and only the original signal would be present in the range from 0 to  $F_s/2$ . Among the four combinations possible, clearly  $+k \cdot F_s + F$  and  $-k \cdot F_s - F$  would not fall in the converter band of interest, i.e. in the range from 0 to  $F_s/2$ . The remaining possibilities are:  $+k \cdot F_s - F$  and  $-k \cdot F_s + F$ . You can always find a value of  $k$  that will place one of them within 0 to  $F_s/2$ . Since one of them is the negative of the other, if one falls in the desired range, the other will be the mirror image of the other across the zero point, and hence will not be in the 0 to  $F_s/2$  range.

**Algorithm for identifying all harmonics (both aliased and otherwise) of the input signal (MATLAB format)**

```

For i = 0 : 1 : D      % D = order of highest harmonic to consider

F(i) = i * Fin

f_aliased_harmonic(i) = N * |round( (bin(F(i))) / N) - bin(F(i)) / N|

end

```

As an example consider the following:

Let      $F_{in} = 200\text{KHz}$   
           $F_s = 2048\text{ kHz}$   
           $N$  (total number of samples in data record) =  $2^{17}$

Then the bin corresponding to the input,  $M = 12800$ .

For these set of values, the first 128 aliased harmonics are included in Table 12 below. These harmonics have an interesting property that is outlined below. The first 128 harmonics are distributed from bin locations 512 to 65536 in increments of 512. All bin locations of the first 128 harmonics are unique. Harmonics higher than the first 128 harmonics, however, fall into the same bin locations that the first 128 harmonics lie in. Interestingly, the basic periodicity found for the patterns in the quantization noise is also 512! For this specific case, the quantization noise happens to coincide with these 128 harmonics.

Order of Harmonic	Un-aliased Bin Location	Bin Location after Aliasing
1	12800	12800
2	25600	25600
3	38400	38400
4	51200	51200
5	64000	64000
6	76800	54272
7	89600	41472
8	102400	28672
9	115200	15872
10	128000	3072
11	140800	9728
12	153600	22528
13	166400	35328
14	179200	48128
15	192000	60928
16	204800	57344
17	217600	44544
18	230400	31744
19	243200	18944
20	256000	6144
21	268800	6656
22	281600	19456
23	294400	32256
24	307200	45056
25	320000	57856
26	332800	60416
27	345600	47616
28	358400	34816
29	371200	22016
30	384000	9216
31	396800	3584
32	409600	16384
33	422400	29184
34	435200	41984
35	448000	54784
36	460800	63488
37	473600	50688
38	486400	37888
39	499200	25088
40	512000	12288
41	524800	512
42	537600	13312
43	550400	26112
44	563200	38912
45	576000	51712
46	588800	64512
47	601600	53760
48	614400	40960
49	627200	28160
50	640000	15360
51	652800	2560
52	665600	10240
53	678400	23040
54	691200	35840
55	704000	48640
56	716800	61440
57	729600	56832
58	742400	44032
59	755200	31232
60	768000	18432

61	780800	5632
62	793600	7168
63	806400	19968
64	819200	32768
65	832000	45568
66	844800	58368
67	857600	59904
68	870400	47104
69	883200	34304
70	896000	21504
71	908800	8704
72	921600	4096
73	934400	16896
74	947200	29696
75	960000	42496
76	972800	55296
77	985600	62976
78	998400	50176
79	1011200	37376
80	1024000	24576
81	1036800	11776
82	1049600	1024
83	1062400	13824
84	1075200	26624
85	1088000	39424
86	1100800	52224
87	1113600	65024
88	1126400	53248
89	1139200	40448
90	1152000	27648
91	1164800	14848
92	1177600	2048
93	1190400	10752
94	1203200	23552
95	1216000	36352
96	1228800	49152
97	1241600	61952
98	1254400	56320
99	1267200	43520
100	1280000	30720
101	1292800	17920
102	1305600	5120
103	1318400	7680
104	1331200	20480
105	1344000	33280
106	1356800	46080
107	1369600	58880
108	1382400	59392
109	1395200	46592
110	1408000	33792
111	1420800	20992
112	1433600	8192
113	1446400	4608
114	1459200	17408
115	1472000	30208
116	1484800	43008
117	1497600	55808
118	1510400	62464
119	1523200	49664
120	1536000	36864
121	1548800	24064
122	1561600	11264
123	1574400	1536
124	1587200	14336
125	1600000	27136

126	1612800	39936
127	1625600	52736
128	1638400	65536

Table 12: Bin locations for the first 128 harmonics of the input signal. Here, input frequency  $F=200\text{KHz}$  (bin 12800), and sampling frequency  $F_s=2048\text{KHz}$  (bin  $2^{17}$ ).



# **Appendix D: Troubleshooting – Minimizing Test Setup Noise**

The following is a brief compilation of noise sources experienced during the test and characterization of the reconfigurable converter and possible solutions for eliminating them.

## **D.1 External Interference and its Minimization**

The performance of the converter both in the delta-sigma mode as well as in the pipeline mode was severely impacted due to external interference. This interference would manifest itself as large spurs at several frequencies in the several MHz range. These spurs would alias back to the signal band and lead to reduced signal-to-noise ratio.

This interference was especially large when the Audio Precision System-I was employed as the signal source. This noise was characterized with a spectrum analyzer and is reported below. Specific steps taken to reduce this external interference are also described below.

### **D.1.1 Noise coupling in Audio Precision System-I**

Analysis of the output from the Audio Precision System-I revealed spurious spikes at a variety of frequencies over a range of 1MHz to 20MHz. The following table lists all the observed spikes and the conditions under which they were experienced.

Source: Audio precision (System-I), balanced output, grounded common-mode level.		
Observation: Spectrum Analyzer (HP 8568B): Frequency Span: 200 kHz, ATTEN: 40dB, Ref: 24.6dBm		
Tone number	Frequency	Magnitude*
Signal	31.8133KHz	1V p-p (-20dB)
Noise tone 1	71KHz	-80dB
Noise tone 2	94KHz	-70dB
Noise tone 3	190KHz	-75dB
Noise tone 4	285KHz	-77dB
Noise tone 5	375KHz	-80dB
Noise tone 6	470KHz	-82dB
Noise tone 7	1.4308MHz	-85dB
Noise tone 8	1.5108MHz	-75dB
Noise tone 9	7.8MHz	-85dB (This spike had a time periodicity, throbbing up and down approximately every second!)

Table 13: External interference with the Audio Precision System-I signal generator.

\*Notice that the magnitudes shown are with respect to the upper reference of the spectrum seen on the analyzer. Since the signal itself was -20dB below, a spike magnitude of -80 dB is actually -60dB below the signal.

A series of steps were taken to change the observed noise. The following lists the steps taken towards this end. All of these spikes remained invariant to signal frequency and amplitude variation. Spikes 1-6 disappeared when the monitors of the PCs lying within a few feet of the system were switched off. Spikes 7-9 persisted even after every single device in the lab was switched off. In fact they persisted even when the audio precision and its controlling PC were switched off! Possibly these were caused by external magnetic field linked to the ground loop formed between the audio precision, spectrum analyzer, and the connection between the main grounds to which these two systems were connected. To lend credence to this theory were the following observations\*\*:

- Disconnection of the power supply of the System-I and its associated PC caused the spikes to vanish. (Possibly because this action broke the above loop).
- The power supply of the System-I and its associated PC were reconnected to the same power plane to which the spectrum analyzer was connected, and the spikes re-appeared at the same frequencies, but were diminished in magnitude. In this case, the 'ground loop' was probably shortened. Nevertheless, these spikes were still large.
- These spikes persisted even the spectrum analyzer was disconnected from the System-I and its signal connection was brought in contact with the chassis of the System-I.

**Conclusion:** The above spikes were eliminated and/or diminished by switching off all PC monitors close to the set-up and by connecting the audio precision to the same ground panel the spectrum analyzer is connected to. So, although some of these spikes could not be eliminated, minimizing the length of the ground loop did diminish the magnitude of these spikes.



**\*\* Corollary:** The converter setup (the power supplies), and the audio precision, and any other equipment such as a PC (that serves as the data acquisition system) *should be* connected to the same power plane to minimize the length of the ground loop that might collect externally interference.

### **D.1.2 Shielding**

The test setup was shielded in order to reduce possible interference. This was achieved by using commercial-grade aluminum foil with commercial-grade plastic wrap on both surfaces as insulation. Both the aluminum and plastic foils are commonly available in any department store. The aluminum foil is then connected to ground. This shield is wrapped around the cables carrying the input signal and the entire test board. Under certain conditions, shielding was found to improve SNR of the converter in delta-sigma mode by almost 3dB!

### **D.1.3 The use of input transformer**

As mentioned earlier in this thesis, an input transformer breaks the ground loop between the signal source and the test board. This helps reduce the interference in the system.

### **D.1.4 Position of Computer CPU**

Signal-to-noise ratio was also found to improve when the CPU of the computer (386) used to control the Audio Precision System-I was positioned further away from the test board. This computer was found to affect the performance of the converter much more than the Pentium III computer employed for data acquisition.

## **D.2 Printed circuit board noise and its minimization**

### **D.2.1 Noise on the input common-mode reference line of the line receivers**

As described earlier, the limited-swing outputs of the data converter drive line receivers, which in turn convert these small swings to large digital signals. The second input of all these line receivers is connected to the common-mode level that of the two limited-swing power supplies. It is generated from the power supplies that are fed to the output buffers of the converter using a simple two-resistor network.

The common-mode reference line should be bypassed to the same ground that is connected to the output buffers of the converter so that any noise on that ground that is coupled to the converter outputs is also coupled to the common-mode reference line leading to a certain canceling effect between the two inputs of the line receivers.

However, despite extensive bypassing, it was noticed that certain glitching noise (with amplitude as much as 500mV, sometimes) on the common-mode reference line persisted. This glitching noise was synchronized to the edges of the clock generated on-board!

**Solution:**

The edges of the clock generated on-board were very sharp- much sharper than needed. 220pF capacitors were used to slow down the edges significantly. This significantly reduced the noise on the critical node to about 10-20mV. It is possible that the clock signals were electro-magnetically coupling into a loop formed by the reference line!

**D.2.2 Glitching noise on the converter outputs**

This noise was similar to the above noise except it was synchronized to the edges of the clock that emanated from the converter as well as the other digital outputs from the data converter. Slowing down the data-output edges of the converter by adding capacitance from these nodes to ground, similarly, reduced this noise.

## Appendix E: Exact Slewing Time Expression in an Amplifier

The small-signal settling waveform is described by the following expression:  $V_O = V_{SW} \left(1 - e^{-t/\tau}\right)$ . The slope at any point of this waveform is given by:  $\frac{\partial V}{\partial t} = \frac{V_{SW}}{\tau} e^{-t/\tau} = \frac{V_{SW} - V_O}{\tau}$ . The slope due to the slewing process is  $\frac{I}{C}$ . The amplifier slews as long as the slew rate is smaller than the slope of the small-signal settling. In other words, the amplifier slews as long as  $\frac{V_{SW} - V_O}{\tau} \geq \frac{I}{C}$ . Replacing  $\tau$  by  $\frac{C}{\beta gm}$ , we get  $V_O \leq V_{SW} - \frac{I}{\beta gm}$ . Here  $\beta$  is the feedback factor of the opamp. Thus the amplifier slews for a voltage range of  $V_{SW} - \frac{I}{\beta gm}$ .

For the sub-threshold regime,  $gm = \frac{qI}{kT}$ . In this case, the amplifier slews for a voltage range of  $V_{SW} - \frac{kT}{q\beta}$ . For  $\beta = 0.25$ , this slewing range is  $V_{SW} - 0.1V$ . Thus for  $V_{SW} = 1V$ , the amplifier slews for 90% of the voltage range!

For strong inversion,  $gm = \frac{2I}{(V_{GS} - V_T)}$ . Under this condition, the amplifier slews through a voltage range of  $V_{SW} - \frac{(V_{GS} - V_T)}{2\beta}$ . For  $V_{GS} - V_T = 100mV$ , and  $\beta = 0.25$ , the slewing range is  $V_{SW} - 0.2V$ . As  $V_{GS} - V_T$  is increased, the slewing range gradually reduces.



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