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Large-scale 2D Electronics based on Single-layer MoS₂ Grown by Chemical Vapor Deposition

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Abstracts

2D nanoelectronics based on single-layer MoS₂ offers great advantages for both conventional and ubiquitous applications. This paper discusses the large-scale CVD growth of single-layer MoS₂ and fabrication of devices and circuits for the first time. Both digital and analog circuits are fabricated to demonstrate its capability for mixed-signal applications.

Introduction

A single-molecular layer of MoS₂ consists of a layer of Mo atoms sandwiched between two layers of S atoms (Fig. 1(a)). As a 2D material, it shares many properties of the well-known graphene such as excellent mechanical flexibility and high thermal stability up to 1090 °C. While with a direct bandgap of 1.8 eV [1], it also overcomes the key shortcomings of graphene for electronic applications - the lack of clear current saturation and pinch-off [2]. 2D electronics based on MoS₂ represents the ultimate limit of scaling in the vertical direction, which is necessary to keep pushing Moore's Law. Its relatively wide bandgap is also advantageous over silicon for suppressing the source-to-drain tunneling at the scaling limit of transistors [3]. Moreover, 2D nanoelectronics based on MoS₂ and other transition metal dichalcogenides (TMD) materials are attractive as high-mobility options in the emerging field of large-area low-cost electronics that is currently dominated by low-mobility amorphous silicon and organic semiconductors (<10 cm²/Vs) [2, 4, 5]. Single-layer MoS₂ can also complement graphene [6, 7, 8] to build flexible digital and mixed-signal circuits. This paper addresses several key challenges in the development of 2D nanoelectronics on MoS₂ and TMD materials in general. The main contributions are three-fold. First, large-area single-layer MoS₂ material is grown by chemical vapor deposition (CVD) that makes the wafer-scale fabrication of MoS₂ devices and circuits possible for the first time. Second, the top-gated transistors, fabricated for the first time on single-layer MoS₂ grown by CVD, show multiple state-of-the-art characteristics, such as record mobility for CVD MoS₂ (>40 cm²/V.s), ultra-high on/off current ratio (>10⁸), record current density (close to 20

μA/μm), current saturation and the first GHz RF performance. Finally, the first fully integrated digital and analog circuits based on MoS₂ are constructed to demonstrate its capability for both logic and mixed-signal applications.

CVD Growth and Device/Circuit Fabrication

Fig. 1(b) shows the experimental set-up for the CVD synthesis of single-layer MoS₂, using S and MoO₃ as the precursor, and perylene-3,4,9,10-tetracarboxylic acid tetrapotassium salt (PTAS) as the seed [9]. Optical micrograph and Raman spectroscopy confirm that single-layer MoS₂ with uniformity greater than 95% can be grown at centimeter-scale, which is only limited by the size of the reaction furnace. The high quality of the material is also evidenced by the outstanding photoluminescence peaks (Fig. 2) derived from its 1.8 eV direct bandgap and the highly ordered lattice structure that can be observed under high resolution TEM (Fig. 3). AFM data confirms the thickness of the material is about 6.9 Å, typical of single-layer MoS₂ (Fig. 4). The devices/circuits fabrication starts from the formation of ohmic contacts by depositing a 5nm Ti/ 50 nm Au metal stack using e-beam evaporation. Device isolation is achieved by O₂ plasma etching. The top gate dielectric consisting of 30 nm HfO₂ is then deposited by ALD at 170°C. To fabricate discrete transistors, the top gate is then formed by depositing 50 nm Pd. For the construction of integrated logic circuits, via holes are created on HfO₂ before the formation of the gate metal layer (M2, Fig. 5) using reactive ion etching (RIE) with BCl₃/Cl₂ gas chemistry to connect M2 to M1. Fig. 6(a) and shows the chip fabricated using single-layer MoS₂ grown on SiO₂. Fig. 6(b) shows a top view of the various integrated device and circuit arrays on the chip of Fig. 6(a).

FETs Based on CVD Grown Single-Layer MoS₂

Fig. 8(a) shows the output characteristics of the fabricated single-layer MoS₂ FET with L_G=L_{DS}=1 μm. The device shows clear current saturation, which is due to the pinch-off of the channel at the drain side of the gate at high V_{DS} since the saturation voltage V_{sat} closely matches the gate overdrive V_{GS}-V_t. This is the first demonstration of current saturation in top-

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gated MoS₂ FETs, a crucial device characteristic that has been missing in previous reports of MoS₂ FETs [10]. The maximum on-state current reaches 16 $\mu\text{A}/\mu\text{m}$ at $V_{\text{DS}}=5$ V and $V_{\text{TG}}=2$ V. The threshold voltage is at -2 V (Fig. 8(b)), indicating that the material is unintentionally doped n-type during the growth and fabrication process. The peak transconductance is around 3 $\mu\text{S}/\mu\text{m}$. The classical drift-diffusion model [11] accurately fits the device characteristics (Fig. 8(a,b)). Due to a larger bandgap than Si and excellent electrostatic control of 2D electronics, the device exhibits a remarkable on/off current ratio exceeding 10^8 , giving the material great potential for ultra-low power applications such as driving circuits for flat panel display, where most of the incumbent materials - organics and amorphous Si - have mobility below 1 $\text{cm}^2/\text{V}\cdot\text{s}$ due to their intrinsic disorder and tunneling-based transport mechanism. In contrast, carrier mobility in polycrystalline CVD single-layer MoS₂ is extracted to be above 40 $\text{cm}^2/\text{V}\cdot\text{s}$ at 300 K (Fig. 7) while single-crystalline exfoliated multi-layer MoS₂ shows mobility around 150 $\text{cm}^2/\text{V}\cdot\text{s}$ at 300 K. Such mobility allows MoS₂ FETs to operate even at GHz frequency. Fig. 8(c) shows the first RF performance characterization of MoS₂ FETs. This device with $L_{\text{G}}=300$ nm shows an f_{T} of 900 MHz and f_{max} of 1 GHz, giving MoS₂ the potential to enable high performance RF circuits on bendable substrates, such as flexible RFID tags.

Integrated Logic Circuits based on Single-Layer MoS₂

A key contribution of this paper is the demonstration of large-scale fabrication of integrated circuits based on CVD single-layer MoS₂. Fig. 9 and 10 show fully integrated inverters and NAND gates in depletion mode configuration. The inverters can operate under a wide range of V_{dd} from 0.5 V to 5V with peak voltage gain close to 20 at $V_{\text{dd}}=5$ V (Fig. 9(c)). Fig. 10(c) shows the NAND gate performing logic function on two input signals. This demonstration of an NAND gate, one of the two types of universal logic gates (the other being NOR), shows that it is possible to realize any Boolean functions on CVD MoS₂ thin film.

Integrated Mix-Signal Circuits based on Single-Layer MoS₂

Finally, to demonstrate the mixed-signal capability of MoS₂, a 1-bit analog-to-digital converter (ADC) is constructed (Fig. 11(a)) based on a matched long-tail pair differential amplifier (Fig. 11(b)). Using the differential gain of the long-tail pair, the ADC converts a 1 kHz sinusoidal signal to a square wave, which is essentially a digital output with two logic levels. Any part of the input signal above (or below) the reference voltage V_{ref} is represented by logic level 0 (or 1) in the output signal

V_1-V_2 (Figure 11(c)). The successful operation of the ADC also demonstrates the excellent matching between the characteristics of the various transistors used in the circuit, necessary for a successful differential amplifier.

Conclusion

Integrated devices and circuits based on large-scale single-layer MoS₂ grown by CVD are presented for the first time. The transistors fabricated on this material demonstrate excellent characteristics such as record mobility for CVD MoS₂, ultra-high on/off current ratio, record current density and GHz RF performance. The demonstration of both digital and analogue circuits shows the remarkable capability of this single-molecular-layer thick material for mixed-signal applications, offering scalable new materials that can combine silicon-like performance with the mechanical flexibility and integration versatility of organic semiconductors.

Acknowledgements

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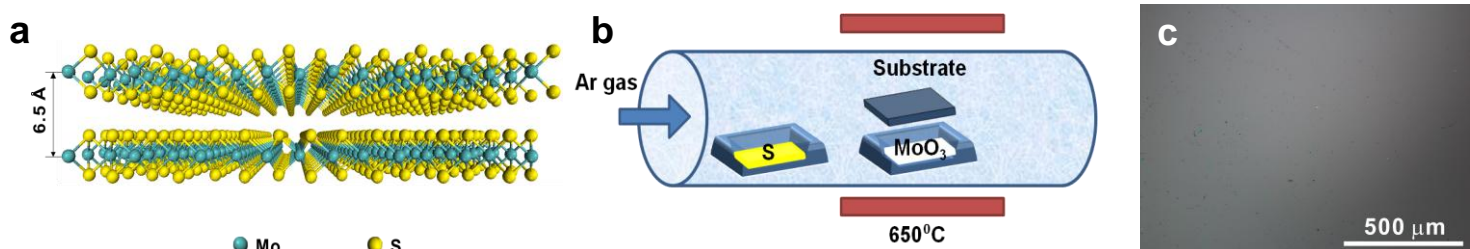


Fig. 1 (a) lattice structure of MoS₂. (b) Schematic of the CVD process for growing single-layer MoS₂. A ceramic boat containing MoO₃ powder (0.02 g) was placed in the center of the quartz tube and a second ceramic boat with sulfur powder (0.01g) was placed upstream. The substrate was pretreated with a droplet of aqueous PTAS solution and then mounted on top of the boat containing MoO₃ powder. During the growth, the furnace was heated to 650°C in Argon environment. The sulfur vapor was carried by the Argon gas and reduced the MoO₃ powder to form volatile suboxide MoO_{3-x}, which diffused to the substrate and was further reduced by sulfur vapor to form MoS₂ films. The same approach can also be used to grow other TMD semiconductors such as WS₂, MoSe₂ and WSe₂. (c) Optical micrographs of single-layer MoS₂ sheets grown by this method. MoS₂ obtained shows great uniformity with more than 95% of the area covered by single-layer MoS₂. This is the first time high quality single-layer MoS₂ can be grown at wafer scale. Since the material can be grown directly on any insulating substrates that are stable at the growth temperature such as SiO₂ and sapphire, no transfer step is required. The material is hence free of wrinkles, which are common sources of mobility degradation often associated with the transfer of CVD grown graphene.

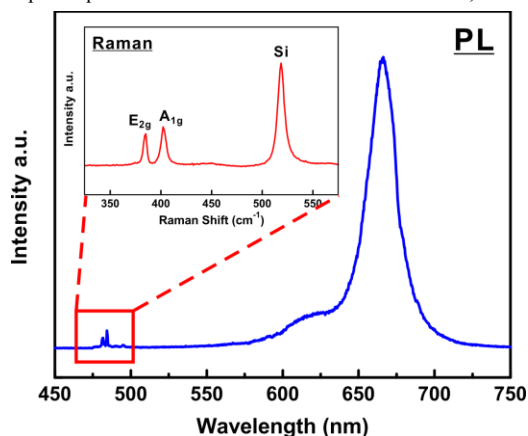


Fig. 2 Photoluminescence (PL) of the single-layer MoS₂ grown by CVD. Inset: the corresponding Raman spectra. Both Raman and PL experiments were performed in a confocal spectrometer using a 473 nm excitation laser.

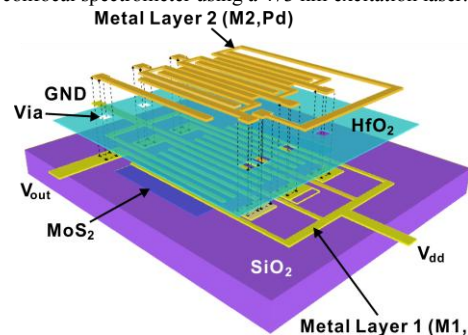


Fig. 5 Schematic illustration of the fabrication process for building transistors and integrated circuits on MoS₂.

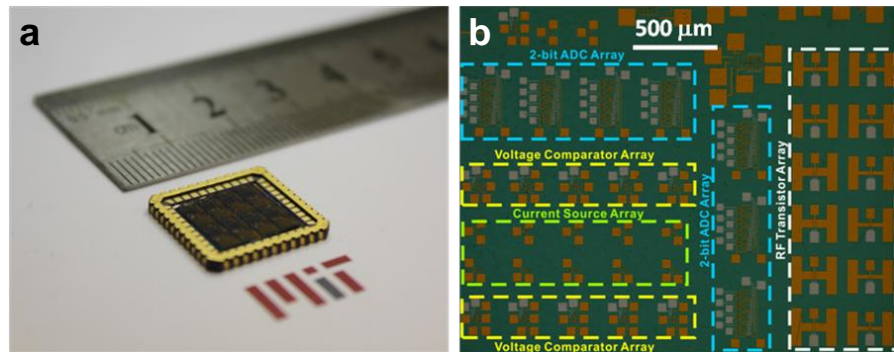


Fig. 6 (a) Transistors and integrated circuits fabricated at the wafer scale for the first time using single-layer MoS₂ grown directly on SiO₂/Si substrate by CVD methods. (b) Optical micrograph of the chip fabricated using CVD single-layer MoS₂ grown on SiO₂/Si substrate, showing arrays of RF transistors, current sources, 1-bit and 2-bit analog-to-digital converters (ADC).

Fig. 7 Hall mobility of exfoliated multi-layer MoS₂ and CVD single-layer MoS₂ and their temperature dependence. At high temperature, the mobility in both samples are limited by phonon scattering. At lower temperatures, the exfoliated multi-layer sample shows improved mobility due to reduced phonon scattering while the CVD single-layer sample shows reduced mobility below 200 K, which can be explained by the fact that in this polycrystalline CVD single-layer sample, the transport at low temperature is dominated by charge carrier hopping through localized states.

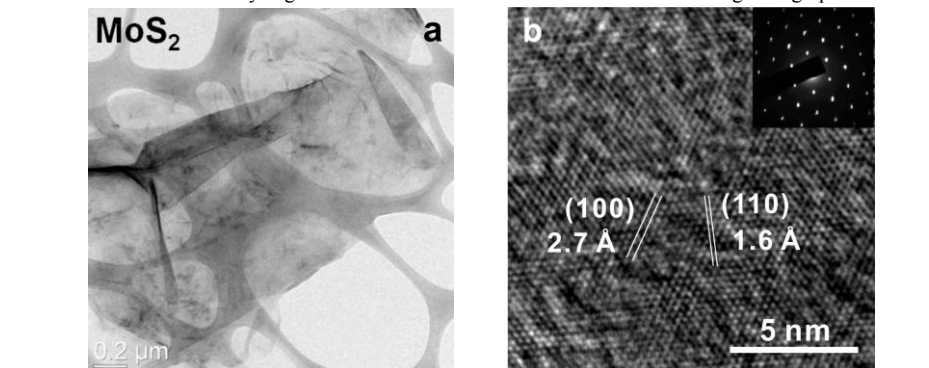


Fig. 3 (a) TEM image of single-layer MoS₂ monolayer grown by CVD. (b) HRTEM image and the corresponding selected area electron diffraction (SAED) pattern (Inset) show the hexagonal crystal nature and the lattice spacing of 0.27 and 0.16 nm assigned to the (100) and (110) planes of MoS₂.

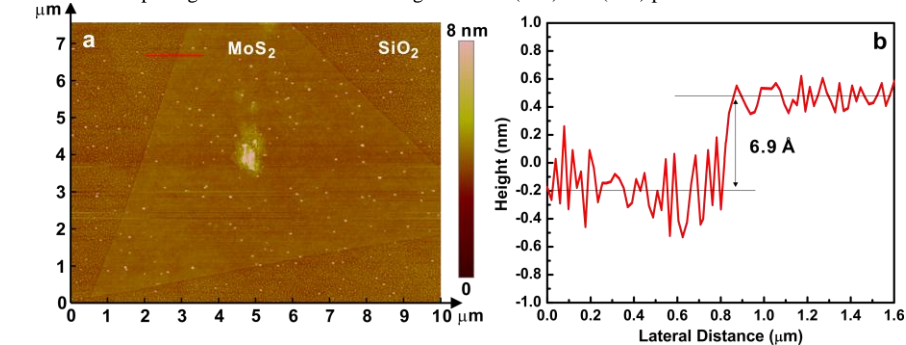


Fig. 4 (a) AFM images and (b) cross-sectional profiles of the single-layer MoS₂ thin film grown by CVD. The coated PTAS seeds act as a nucleation site to initiate the growth. In this sample, the CVD growth process is intentionally stopped before the growth initiated from neighboring seeds merges. The AFM image hence shows the single-layer MoS₂ grown in an equilateral-triangle pattern that is determined by its underlying lattice structure. The CVD single-layer MoS₂ has a thickness of 6.9 Å, typical for single-layer MoS₂ sheets.

