Extraction of Variation Sources Due to Layout Practices

By

Karen M. González-Valentín

Submitted to the Department of Electrical Engineering and Computer Science in partial fulfillment of the requirements for the degree of

Master of Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

May 24, 2002

Author _____

Electrical Engineering and Computer Science
May 24, 2002

Certified by _____

Duane S. Boning
Associate Professor
Electrical Engineering and Computer Science

Accepted by _____

Arthur C. Smith
Chairman, Department Committee on Graduate Studies
Electrical Engineering and Computer Science

Extraction of Variation Sources Due to Layout Practices

By

Karen M. González-Valentín

Submitted to the Department of Electrical Engineering and Computer Science on May 24, 2002 in Partial Fulfillment of the Requirements for the Degree of Master of Science in Electrical Engineering and Computer Science

Abstract

Modern circuit design needs efficient methods to characterize and model circuit variation in order to obtain high-yielding integrated circuits. Circuit and mask designers need accurate guidelines to prevent failures due to layout-induced variation. This thesis addresses this need by contributing a variation test chip and variation analysis methods. The test chip consists of carefully designed ring oscillator circuits which are made sensitive to some of the most common and critical layout-dependent variations; analysis of the ring oscillator output frequencies enables assessment of variation impact at both the device (FEOL) level and interconnect (BEOL) level. FEOL variations studied are density vs. isolation, polysilicon fingers proximity, global polysilicon density, orientation and others. BEOL variations studied include parasitic coupling, fringing and planar capacitance, among others.

The testing of the designed test chip has proven successful for both device and interconnect test structures. Different ring oscillator layout practices are seen to result in significant differences in mean and standard deviation of measured ring oscillator frequencies. Increases in variance of nominally identical structures due to layout practice are ascertained with 95% confidence level tests on variance ratios. ANOVA is performed to demonstrate that the means of different structures are different at a high (over 95%) confidence. The FEOL structure analysis shows strong dependencies between the layout practice and gate length variations: spacing between poly fingers can shift ring oscillator frequency by 4.4%, and polysilicon density can change frequency by 2.1%. BEOL structure analysis shows dependencies due to the metal geometry. Spatial analysis reveals both a large die-to-die (within-wafer) trend, and systematic within-die spatial patterns for particular test structures. Variation analyses such as these, made possible by the novel variation test chip, enable identification of likely variation sources, quantification of circuit impact and sensitivity, and specification of layout practices for variation minimization.

Thesis Supervisor: Duane S. Boning
Title: Associate Professor of Electrical Engineering and Computer Science

Acknowledgements

This thesis could have not been completed without the collaboration of several people, at both professional and personal levels.

First of all I want to thank God for giving me the opportunity, strength and enthusiasm to be here today. Thanks for letting me be surrounded by amazing people who have made my life so pleasant. Thank you very much for all your blessings, which are countless in my life.

I want to especially thank my beloved grandfather, Don Ernesto Valentín Sánchez (1909-2001), for all his love, care and encouragement through the 23 years I was able to spend with him. Abuelito, I am sure you're happy to see me graduating and I know you'll be watching the commencement from heaven like you did for so many years on earth. With all my heart I want to dedicate this milestone to you. Please watch me for the rest of my life and I'll meet you up there someday, sometime.

I want to deeply thank my family for all their help, love and support through all my life. Mami y papi, thank you so much for all the sacrifices you have done to let me be here today. Thank you for all your love. Thank you so much for taking so good care of me and for being such great role models. To my brother Tatito, thank you for all your love and inspiration. Thanks for encouraging me to be an electrical engineer, for all your support and for giving me the most beautiful niece and nephew. Thank you Marcos and Kristina for bringing such big joy to my life. Thank you Waleska for being such a good sister in law and for taking good care of my brother and your babies. To my sister and best friend Betsy, thank you for all your sweetness, your patience, your understanding and mainly for your love. I'm so lucky to have such a wonderful sister. Thanks to my

grandmother whose love and good advice have always protected me. Overall, thanks to all my family for all their love and support that has been so crucial through graduate school and all my life.

Very special thanks to Andy, the love of my life and my future husband. Not only would Boston or MIT have been impossible to survive without you, but you have made my life happier than I ever dreamed. It is wonderful to be your girlfriend, and it will be even better to spend the rest of my life with you. Thank you so much for making me feel my best and encouraging me to finish my work even when it seemed impossible. I love you very much and cannot thank God enough for letting you be in my life.

I also want to thank my officemates, who have made it so enjoyable to be part of this research group and the MIT experience. Thanks to Aaron, Allan, Dave, Han, Joe, Mike, Nigel and Vikas for all the fun times they've contributed at the 39-328 office, and for helping me settle here. I would also like to acknowledge Brian, Tae, Tamba and Xiaolin for their group support and friendship. Thanks to Debb for her friendship and her unconditional help with MTL's administration, including the endless supplies of the hot chocolate machine. Thanks to all the staff of MTL and EECS graduate department for all their help for the last two years.

Special thanks go to Sani Nassif and his research group in IBM for all their ideas and overall contributions to this project. Thank you so much for giving me the opportunity to work with your brilliant team and giving me countless ideas and suggestions regarding our project.

I want to thank International SEMATECH for funding this project and special thanks to Manuela Huber for all her effort and enthusiasm regarding our research. Thank you so

much for all your help in the organization and all the ideas regarding the analysis. I hope we keep in touch for many more years.

Special thanks to Joseph Panganiban, my partner in this project, and to Duane Boning, my research advisor. Joseph, thanks for all your help in everything related to this project and for your friendship. Special thanks for collaborating with the appendixes. To Duane, thank you so much for all your help with the variation analysis, and for guiding me through graduate school. Thanks for all your enthusiasm throughout the last two years.

I also want to thank the *Cooperative Research Fellowship Program* for funding my studies.

Table of Contents

ABSTRACT 3

ACKNOWLEDGEMENTS 5

CHAPTER 1 INTRODUCTION AND MOTIVATION FOR RESEARCH 15
1.1 Motivation and Overview 15
1.2 Previous Work 17
1.2.1 MOSIS 0.35 μm Run 18
1.3 Summary 19

CHAPTER 2 TEST STRUCTURES DESCRIPTION 20
2.1 FEOL Structures 20
2.1.1 Canonical FEOL RO 21
2.1.2 Orientation-Varied ROs 23
2.1.3 Poly Line-Spacing ROs 24
2.1.4 Poly-Density ROs 25
2.1.5 Single-Fingered RO 25
2.1.6 Dense vs. Isolated ROs 26
2.1.7 P-N Structures 27
2.2 BEOL Test Structures Description 28
2.2.1 Canonical BEOL RO 28
2.2.2 Fringing Capacitance Interconnect Structure 29
2.2.3 Coupling Capacitance Interconnect Structure 30
2.2.4 Plane Capacitance Interconnect Structure 30
2.2.5 Vertical vs. Horizontal Structures 31
2.2.6 ILD Structures 32
2.3 Summary 33

CHAPTER 3 CHIP ARCHITECTURE AND TESTING SETUP 34
3.1 Tile 34
3.2 Row 36
3.3 Chip 37
3.4 Testing Report 38
3.5 Summary 39

CHAPTER 4 FEOL TEST STRUCTURES TESTING AND ANALYSIS 41
4.1 Functionality 42
4.2 Statistical Analysis Methodology 43
4.2.1 Chip-to-chip and Within-chip Variance Components 44
4.2.2 Evaluation of Mean Differences and Variance Ratios 46

4.3 Structure Variation Components 46
4.3.1 Dense vs. Isolation and Single Finger Structures 48
4.3.2 Polysilicon Proximity Structures 52
4.3.3 Polysilicon Density Structures 54
4.3.4 Vertical vs. Horizontal Structures 56
4.3.5 P/N Structures 59
4.4 Summary 60

CHAPTER 5 BEOL TEST STRUCTURES TESTING AND ANALYSIS 61
5.1 Functionality 62
5.2 Statistical Analysis Methodology 62
5.3 Structure Variation Analyses 63
5.3.1 Coupling Capacitance Structures 63
5.3.2 Fringing Capacitance Structures 68
5.3.3 Plane Capacitance Structures 71
5.3.4 Vertical vs. Horizontal BEOL Structures 74
5.4 Future Work: Separation of Interconnect Capacitance Components 75
5.5 Summary 78

CHAPTER 6 SPATIAL ANALYSIS 80
6.1 Chip-to-chip Spatial Analysis 80
6.1.1 Chip Mean (All Structures) Spatial Trend 81
6.1.2 Chip Mean (Canonical BEOL Structure) Spatial Trend 83
6.1.3 Chip Mean (Canonical FEOL Structure) Spatial Trend 85
6.2 Within-chip Spatial Analysis 87
6.2.1 Spatial Analysis Procedure 87
6.2.2 Within-chip Trend - Canonical BEOL Structure 88
6.2.3 Within-chip Trend - Canonical FEOL Structure 89
6.2.4 Within-chip Trend - Single Finger FEOL Structure 91
6.2.5 Within-chip Trend - Large Plane M1 BEOL Structure 91
6.3 Summary 92

CHAPTER 7 CONCLUSION 93
7.1 Test Structures Analysis 93
7.1.1 FEOL Analysis 93
7.1.2 BEOL Analysis 94
7.1.3 Spatial Analysis 95
7.2 Future work 96
7.3 Summary of Contributions 96

BIBLIOGRAPHY 97

APPENDIX I THRESHOLD VOLTAGE ANALYSIS 99

APPENDIX II PARASITICS IMPACT IN FEOL ANALYSIS 102

List of Figures

Figure 1-1: Geometry of Wiring: Single Line to Ground Plane 18
Figure 2-1: Schematic Canonical RO 21
Figure 2-2: Equivalent Device RO Inverter 22
Figure 2-3: Inverter Layout 22
Figure 2-4: Layout Canonical RO 23
Figure 2-5: Horizontal and Vertical ROs 24
Figure 2-6: Line-Spacing Variation 24
Figure 2-7: Polysilicon Density 25
Figure 2-8: Equivalent Device Single Finger Inverter 26
Figure 2-9: Same gate length in different polysilicon fingers 26
Figure 2-10: P vs. N 1. Canonical, 2. N-ish, 3. P-ish, 4. J-ish, and 5. F-ish 27
Figure 2-11: Interconnect Capacitances – 1.Fringing, 2.Coupling, 3.Plane 28
Figure 2-12: Fringing Capacitance - Metal m snake with Metal m-1 ground plane underneath 29
Figure 2-13: Coupling Capacitance. Metal m snake and ground at minimum distance ... 30
Figure 2-14: Plane Capacitance. Metal m plane and m-1 ground plane underneath 31
Figure 2-15: Horizontal (left) and vertical (right) 31
Figure 2-16: Planar Capacitance dimensions 32
Figure 3-1: Tile Block Diagram 35
Figure 3-2: Double Tile Block Diagram 36
Figure 3-3: Row Block Diagram 36
Figure 3-4: Chip Block Diagram 37
Figure 3-5: Chip Layout 38
Figure 3-6: Bonding Diagram 38
Figure 3-7: Schematics of Circuitry Added to PC Card 39
Figure 4-1: Frequency Response for All Structures 43
Figure 4-2: Schematic representation of chip-to-chip versus within-chip variation. 44
Figure 4-3: Mean Differences for Dense vs. Isolated Structures 49
Figure 4-4: Total Standard Deviations for Dense vs. Isolated Structures 49
Figure 4-5: Local Polysilicon Proximity Effect 52
Figure 4-6: Global Polysilicon Density Effect 55
Figure 4-7: Vertical (Solid Line) vs. Horizontal (Dashed Line) Frequency Response 58
Figure 5-1: Coupling Capacitance Frequency Response 65
Figure 5-2: PDF Plot for Coupling Structures 67
Figure 5-3: PDF Plot for Coupling Structures at Mean = 0 67
Figure 5-4: Fringing Capacitance Frequency Response 69
Figure 5-5: PDF Plot for Fringing Structures 70
Figure 5-6: PDF Plot for Fringing Structures at Mean = 0 71
Figure 5-7: Plane Capacitance Frequency Response 72
Figure 5-8: PDF Plot for Plane Structures 73
Figure 5-9: PDF Plot for Plane Structures at Mean = 0 74
Figure 5-10: RC Equivalent of Inverter Chain 76
Figure 5-11: RO with Dummy Inverter 76

Figure 5-12: RC Equivalent of Inverter Chain with Dummy Inverter 76
Figure 6-1: Chip Mean Frequencies by Spatial Location 82
Figure 6-2: Spatial Location in Wafer 82
Figure 6-3: Chip Mean Frequencies by Chip Number 83
Figure 6-4: Mean Frequencies of Canonical BEOL by Spatial Location 84
Figure 6-5: Canonical BEOL - Mean Frequencies By Chip 84
Figure 6-6: Mean Frequencies of Canonical FEOL by Spatial Location 86
Figure 6-7: Canonical FEOL - Mean Frequencies Per Chip 86
Figure 6-8: Spatial Analysis for Canonical BEOL 89
Figure 6-9: Spatial Analysis for Canonical FEOL 90
Figure 6-10: Spatial Analysis for Single Finger FEOL 91
Figure 6-11: Spatial Analysis for Large Plane M1 BEOL 92

List of Tables

Table 1-1: Multiple Chip Measurements for 0.35 μm TSMC MOSIS Run 19
Table 4-1: FEOL Structures Frequency Response 47
Table 4-2: Density vs. Isolation Analysis 51
Table 4-3: Density Vs. Isolation Structures; Variation Decomposition 51
Table 4-4: ANOVA Table for Proximity Structures 53
Table 4-5: Polysilicon Proximity Effect Analysis 54
Table 4-6: Polysilicon Proximity Effect; Variation Decomposition 54
Table 4-7: ANOVA Table for Polysilicon Density Structures 55
Table 4-8: Polysilicon Density Effect Analysis 56
Table 4-9: Polysilicon Density Effect; Variation Decomposition 56
Table 4-10: Vertical vs. Horizontal Analysis 59
Table 4-11: Orientation Effect: Variation Decomposition 59
Table 5-1: BEOL Structures Frequency Response 63
Table 5-2: Coupling Structures; Percentages of the individual σ^2 values 65
Table 5-3: ANOVA Table for Coupling Structures 66
Table 5-4: Fringing Structures; Percentages of the individual σ^2 values 70
Table 5-5: ANOVA Table for Fringing Structures 70
Table 5-6: Plane Structures; Percentages of the individual σ^2 values 72
Table 5-7: ANOVA Table for Plane Structures 73
Table 5-8: Horizontal and Vertical Structures; Percentages of the individual σ^2 values .. 75

Chapter 1

Introduction and Motivation for Research

This chapter presents the motivation for studying variation sources due to layout practices and the need for efficient means to extract them in current technology. It discusses previous work in the field, including an overview of a previous test structure chip in an older technology. This thesis attempts to detect variations due to layout practices by analyzing a test circuit with greater numbers of test structures than the previous test circuit and a larger variety of types of variation.

1.1 Motivation and Overview

Process variations are becoming an important issue in today's design of integrated circuits. The aggressive technology scaling that this industry has been experiencing in the last few years make it a challenge to circuit/layout designers to produce high yielding integrated circuits. Some process variations, such as line-width changes of poly or interconnect, can significantly affect circuit performance. This requires the development of new techniques to measure and extract variation in a given process and link it to circuit performance.

The main objective of this thesis is to address this issue by developing such a technique for timing variation. This is to be achieved by designing test circuits that will present some of the most challenging and common sources of variation in a controlled way. This way, by adding variations on purpose and controlling their magnitude and

behavior, it will be possible to identify, model and suggest ways to prevent these variations from contributing to performance failure.

The test structures to be studied can be divided into two types: *Front End Of the Line* (FEOL) and *Back End Of the Line* (BEOL) structures. FEOL structures concentrate on the variations found in the devices that are part of a circuit. This part of the project mainly focuses on transistors, and how variations affect them. Variations such as sensitivity to poly width changes due to proximity effect, etch loading and orientation could affect the performance of transistors that will further carry these variations to the entire circuit where they are used. FEOL structures are tested by carefully laying out sets of ring oscillators (ROs) whose inverters have been carefully laid out to enhance a specific source of variation. Variations in the inverters may affect the overall output frequency of the ring oscillator (RO), and this will provide a sense of how the specific variation is affecting the circuit.

BEOL test structures are structures that simulate common scenarios of interconnections within a chip. These structures must simulate parasitic capacitances such as fringing, coupling and plane capacitance. To do so, ring oscillators are carefully laid out to enhance all these variations, but exclusively one at a time in order to detect how this specific variation is affecting the output frequency of the circuit.

Chapter 2 describes all test structures included in the test chip, for both BEOL and FEOL. After a brief description of the chip architecture based on the design by Panganiban [3] and the testing methodology on Chapter 3, Chapter 4 presents testing results and analysis for FEOL structures, and Chapter 5 the testing results and analysis

for BEOL structures. Chapter 6 presents spatial analyses at both die and die-to-die levels. Chapter 7 is an overall conclusion.

1.2 Previous Work

The topic of variations in circuits due to layout practices has been an increasingly popular one in the last few years. Nassif [1] discussed the modeling and analysis of manufacturing variations, noting that there are two different sources of variations in integrated circuits: environmental factors and physical factors. The environmental factors "include variations in power supply voltage and temperature" and they are "highly design dependent." The physical factors "include variations in the electrical and physical parameters characterizing the behavior of active and passive devices." These "exhibit long time constants" and can fall into two categories: "die-to-die physical variations" and "within die physical variations." This thesis studies both.

In Nassif's paper, the physical sources of variation are further divided between device variations (D) and wire variations (W). In this study, wire variations are expected to increase in importance dramatically through the years. Nassif concludes that interconnect variation impact will continue increasing in importance and that appropriate methods of modeling it must be developed to keep up with technology scaling.

There are several papers about modeling parasitic capacitances in wire interconnections. Chern, Huang, et al. [2] published an illustrative paper which explains how to calculate the parasitic capacitances on interconnect wires. These models are empirical, calculated with data based on SIERRA 3D device simulations. Although sufficiently accurate, these formulas are complicated and depend on a large number of parameters. The paper references Sakurai, et al. [7], whose empirical formulas are

simpler and dependent on fewer parameters. The basic "single line on ground plane" formula used in this thesis is presented as:

$$\frac{C_1}{E_{ox}} = 1.15\left(\frac{W}{H}\right) + 2.80\left(\frac{T}{H}\right)^{0.222}$$

E_{ox} represents the dielectric constant of the oxide and the parameters W, H and T are illustrated in Figure 1-1.

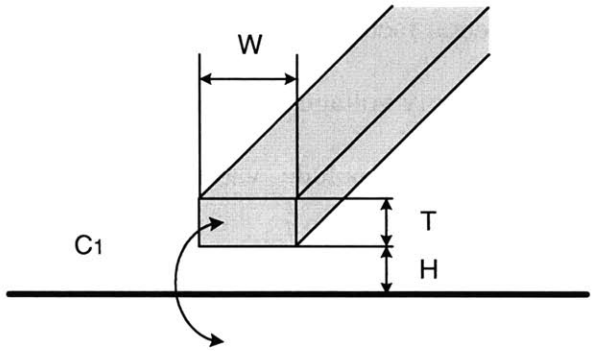

Figure 1-1: Geometry of Wiring: Single Line to Ground Plane

1.2.1 MOSIS 0.35 μm Run

As mentioned before, this thesis includes carefully laid out structures to extract and analyze variation parameters on ring oscillators. As proof of concept, our research group at MIT ran a 0.35 μm TSMC MOSIS run with device-focused and interconnect-focused structures. Device-variation (or FEOL) circuits include circuits sensitive to poly width changes due to proximity effect, etch loading and orientation. Interconnect-variation (or BEOL) circuits include circuits that accentuate fringing, coupling and plane capacitance. The proof of concept was successful, and the results showed that:

1. Different types of FEOL ring oscillators showed different output frequencies, proving that specific layout practices at the device level may produce a significant

variation in the performance of a circuit. As shown in the Table 1-1, the largest difference in frequencies observed is from the canonical to the vertical RO. This difference, due to orientation, is from 2.5 MHz to 2.39 MHz, or approximately of 8%.

2. BEOL structures did not work, apparently because of wiring issues.

Cell Name	Measured Data at 3.3V		Overall Standard Deviation Voltages from 1.3V to 3.3V	
	Frequency [MHz]	σ [MHz]	[KHz]	%
Canonical	2.5006	0.053	79.3	3.2
2x Spacing	2.3016	0.047	50.4	2.2
3x Spacing	2.2082	0.044	46.9	2.4
Full Poly	2.4874	0.051	54.7	2.2
Half Poly	2.4993	0.050	54.1	2.2
Single Finger	2.7507	0.033	34.7	1.3
Vertical	2.3932	0.055	41.8	1.7

Table 1-1: Multiple Chip Measurements for 0.35 μm TSMC MOSIS Run

The design and results for the MOSIS 0.35 μm run is documented in the Sematech Report of 2001 [4].

1.3 Summary

In modern integrated circuits it is becoming increasingly important to detect and model process variations due to layout practices. The goal of this thesis is to design test circuits that will isolate process variations in such a way that a specific variation can be extracted and modeled. The following chapters present the design and analysis of these structures.

Chapter 2

Test Structures Description

Carefully designed ring oscillators (ROs) are the fundamental test structures used to acquire measurements to link how the layout practice may affect the performance of a circuit. Each of these ring oscillators is intended to accentuate one source of variation, in order to relate frequency measurements to a particular geometric device or interconnect structure deviation. A description of how the test structures are laid out to achieve this is the focus of this chapter. In Section 2.1, we consider front-end-of-line or transistor oriented test structures. Back-end-of-line, or interconnect dominated test structures are then presented in Section 2.2. This chapter focuses on the principles behind each individual test structure or family of related test structures. Section 2.3 is an overall summary.

2.1 FEOL Structures

The first major category of ring oscillator structures developed in this project tests front-end-of-line (FEOL) variations. The FEOL ring oscillators consist of only inverters with no additional capacitive load (other than parasitics which are minimized) between inverter stages. Since these ROs consist of devices only, the oscillator frequency is mainly influenced by device parameters. The current drive strength of a transistor is dependent on the width to length ratio of the polysilicon gate. Since the gate length is generally smaller than the width, variations in gate length have a greater influence on the

current drive of the transistor. In the ring oscillator case, variations in gate length cause fluctuations in the current drive of the inverters, which result in differences in oscillator frequency. These ROs can extract across-chip line width variation (ACLV) of the polysilicon gate by comparing the frequencies of several of these oscillators laid out across the die. Also, by varying some of the dimensions of the ROs and how they are laid out, we can accentuate certain gate-length variations due to specific process sources.

Research on how the parasitics may affect this analysis is documented in Appendix II.

2.1.1 Canonical FEOL RO

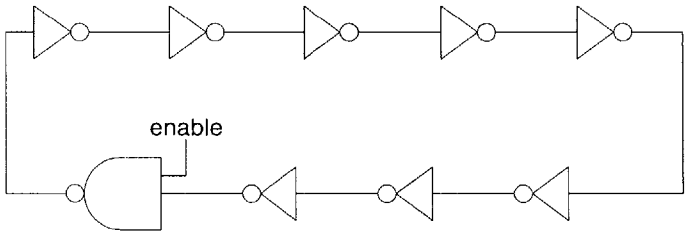

Figure 2-1: Schematic Canonical RO

The canonical FEOL ring oscillator consists of an odd number of inverters in a chain, in this case nine. These inverters consist of three minimum channel-length fingers of polysilicon. This three-fingered configuration is equivalent to an inverter that has three minimum-length PMOS and NMOS transistors in series, as illustrated in Figure 2-2. This increases the effective gate length of the inverter by a factor of three compared to the channel length of a single finger. One effect of this is to slow down the oscillator frequency while maintaining the same ratio between gate length and change in gate length (ΔL variation). A two input nand gate with one of the inputs connected to an enable signal is equivalent to an inverter in the chain. If the RO is enabled, the nand gate works just as any other inverter.

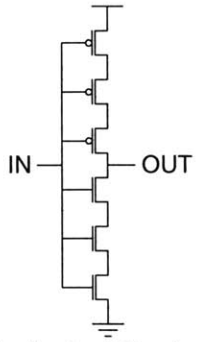

Figure 2-2: Equivalent Device RO Inverter

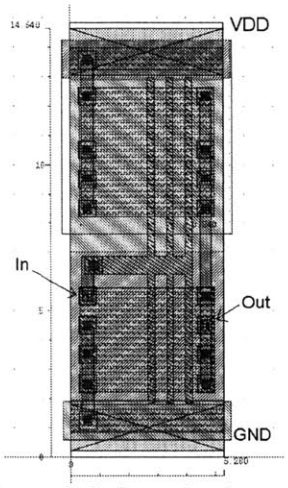

Figure 2-3: Inverter Layout

Figure 2-2 and Figure 2-3 illustrate the schematic and layout of the inverter used to build the canonical FEOL RO. The canonical FEOL cell was built in the 0.25 μm technology by arranging inverters whose transistors had a minimum nominal gate lengths, and widths of 4.42 μm for PMOS and 3.58 μm for NMOS. The spacing between the polysilicon fingers is the minimum for this technology (0.4 μm). All the local wiring is in the lowest metal layers, metal 1 and metal 2.

A snapshot of the layout of the canonical FEOL RO is shown in Figure 2-4. Seen in the figure is the presence of the three-fingered transistors, the way P and N types of transistors are arranged so there is only one power supply connection, and the nand gate at the end. At the end of this and all other FEOL structures there is a buffer inserted for

reliable measurements. This buffer adds a load to the ring oscillator that must be considered in modeling the RO frequency.

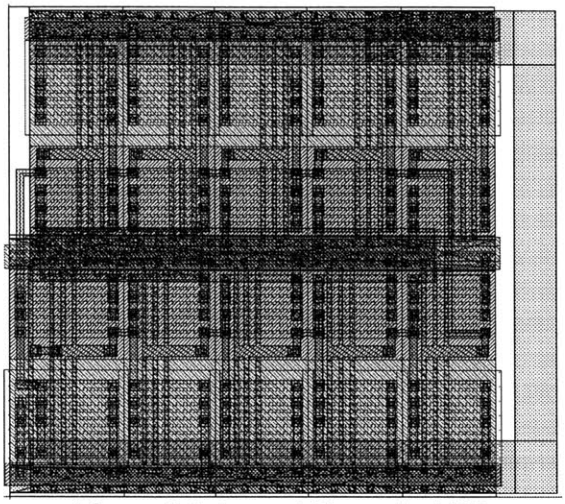

Figure 2-4: Layout Canonical RO

This ring oscillator is termed the "Canonical FEOL RO" because the other differently laid-out device ROs (or FEOL structures) are variants of the layout of this ring oscillator. These other ROs incorporate different layout practices at the device level, such as changes in orientation, poly-line spacing, poly fill, finger density and variants due to P-type vs. N-type of transistors.

2.1.2 Orientation-Varied ROs

By varying the orientation of how the ring oscillators are laid out, variation in the mask scan bias, ion implantation directionality, or other direction dependent fabrication processes can be captured. Oscillators are laid out both horizontally and vertically. The horizontal ring oscillator is the same as the canonical FEOL structure, and the vertical is the canonical FEOL RO rotated by 90 degrees. These two structures are placed right next to each other within the chip to detect variations depending on orientation and not other factors which might be affected by the spatial location.

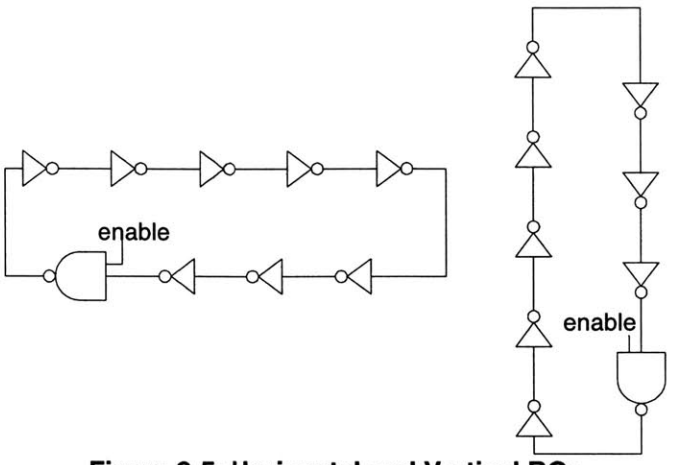

Figure 2-5: Horizontal and Vertical ROs

2.1.3 Poly Line-Spacing ROs

Variations due to lithography proximity can be extracted by varying the line spacing between polysilicon fingers. Figure 2-6 describes the idea of varying the line spacing of the transistors. The canonical FEOL RO structure has minimum spacing between the poly fingers of the transistors. Other ring oscillators are laid out identically to the canonical FEOL structure except with different spacing between the poly fingers.

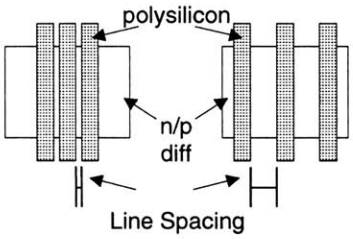

Figure 2-6: Line-Spacing Variation

There are five different types of ring oscillators based in this test structure laid out in the MOSIS 0.25 μm run. There is the canonical FEOL, with minimum spacing between the fingers (or 0.4 μm as described in the *Canonical FEOL RO* subsection), and structures with 1.2, 1.5, 2 and 3 times the minimum spacing (or 0.48 μm, 0.6 μm, 0.8 μm, and 1.2 μm spacing respectively).

2.1.4 Poly-Density ROs

By varying the global polysilicon density around the ring oscillators, we can extract variations due to the polysilicon etch loading effect. Figure 2-7 describes the basic concept of these RO structures. The canonical FEOL RO structure is laid out in an area free from any extraneous polysilicon density. Other canonical FEOL ROs are laid out surrounded with varied densities of polysilicon. By comparing the frequencies of these poly-density ROs, we can obtain information on the poly etch loading effect.

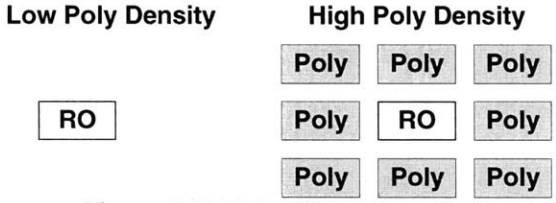

Figure 2-7: Polysilicon Density

There are five different types of ring oscillators based in this test structure laid out in the MOSIS 0.25 μm run. There are structures with 0%, 12%, 25%, and 50% pattern density of polysilicon surrounding the ring oscillator. An additional structure, a basic canonical FEOL cell, is placed at the beginning and end of the group of cells with different polysilicon density to avoid the density affecting other non-poly density structures. This structure is in a different category than the canonical FEOL, and is referred to as the *Canonical At End Of Density Structure*.

2.1.5 Single-Fingered RO

A single-fingered RO is laid out in the MOSIS 0.25 μm run to compare any differences in frequency with the three-fingered RO. This single-fingered RO has a gate length of three times the minimum width for polysilicon in this technology, or 0.75 μm. It is illustrated in Figure 2-8. The rest of the dimensions of the RO, such as gate width, are similar to the canonical FEOL structure. Nominally, the frequency of the single-fingered

RO should be close to the frequency of the canonical FEOL RO, since the effective gate length of the canonical FEOL structure is also three times the minimum length (because it is three-fingered). This structure should present a ΔL variation of approximately one third of the canonical FEOL because the variation may only occur in one finger, as opposed to three in the canonical FEOL. This may provide evidence of gate-length variation among the ring oscillator circuits.

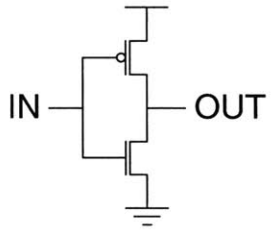

Figure 2-8: Equivalent Device Single Finger Inverter

2.1.6 Dense vs. Isolated ROs

The dense versus isolation (D/I) ring oscillators vary the local density and number of poly fingers. Different ring oscillators have transistors with the same effective gate length but distributed across a different number of polysilicon fingers. These oscillators should nominally oscillate at a similar frequency. The distribution of the gate length into different arrays of polysilicon fingers accentuates variation due to gate length variation, since ΔL may be x-times present in x-fingered transistors.

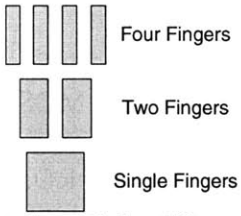

Figure 2-9: Same gate length in different polysilicon fingers

There are six structures in the MOSIS 0.25 μm test chip that may be used to study the D/I effect. These structures are divided into two groups. The first group is composed of

the single finger structure along with the canonical FEOL RO and a third structure that has the same effective total gate length (0.75 μm) but divided into two fingers of 1.5 times the minimum (or 2 x 1.5 x 0.25 μm or 0.75 μm total).

The second group is composed of three structures all with effective gate length of 1 μm. The structures are a single finger structure with 1 μm gate length, a two-finger structure whose fingers are twice the minimum (0.5 μm each) and a four-finger structure constructed of minimum size fingers (0.25 μm each).

2.1.7 P-N Structures

The P-N structures are ROs whose inverters show a variety of P/N ratios. These structures are intended to separate variations due to the P-type transistors and the N-type transistors. There are five variants of these structures, as shown in Figure 2-10. The "N-ish" is a structure where the N-type transistors are the ones doing most of the work in the inverter. In the "P-ish" the P-type transistors are the ones dominating the inverter, and the "F-ish" basically works like a two finger structure with R_{on} resistances to power and ground. Finally, the "J-ish" structure works like a one finger structure with R_{on} resistances to power and ground. All the structures are built with the basic three-finger transistors with minimum spacing between the fingers and minimum width in each finger.

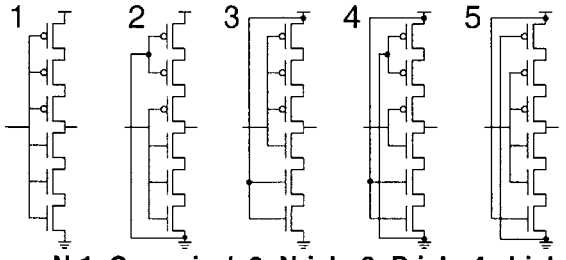

Figure 2-10: P vs. N 1. Canonical, 2. N-ish, 3. P-ish, 4. J-ish, and 5. F-ish

2.2 *BEOL Test Structures Description*

The "back end of the line" or BEOL structures used for variation measurements are ring oscillators which have a metal layer structure loading the output of one of the inverter stages in the chain. These metal structures are intended to be big enough to dominate the output frequency of the ring oscillators, but their shape and dimensions are chosen so that a specific variation is accentuated. The goal of these interconnect test structures is not only to detect variation in interconnect dimensions (such as ILD thickness, metal thickness, and metal width), but also to identify properties due to metal geometry variation. Interconnect capacitance is composed of three different capacitances: planar, fringing, and coupling capacitances, as illustrated in Figure 2-11.

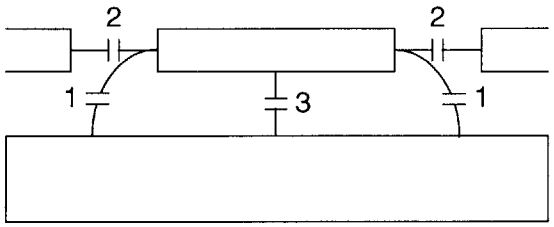

Figure 2-11: Interconnect Capacitances – 1.Fringing, 2.Coupling, 3.Plane

2.2.1 Canonical BEOL RO

The canonical BEOL RO structure is similar to the *Single Finger FEOL* structure. It is composed of single fingered transistors with three times minimum gate length transistors. The purpose of this choice is to add robustness and minimize sensitivity to ΔL variations; instead, the goal is to be primarily sensitive to interconnect load variation.

The canonical BEOL RO is built in the 0.25 μm technology by arranging inverters whose transistors have a 0.75 μm gate length and widths of 4.42 μm for PMOS and 3.58 μm for NMOS. Like the FEOL canonical structure, all the local wiring is in the

lowest metal layers, metal 1 and metal 2, and a two input nand gate with one of the inputs connected to an enable signal replaces one of the inverters in the chain.

2.2.2 Fringing Capacitance Interconnect Structure

Fringing capacitance is the capacitance between the sidewall surfaces of the metal structure and the top surface of the metal layer (or substrate) underneath. The structure consists of a snake-like structure of minimum width wires with a large separation between them, as shown in Figure 2-12. Minimum width wires are required to maintain the overlap or area capacitance that goes from the metal to the substrate or a lower metal layer (plane capacitance) as small as possible. A large separation between the wires is necessary to avoid metal to metal coupling capacitance. The ring oscillator is the *Canonical BEOL RO*.

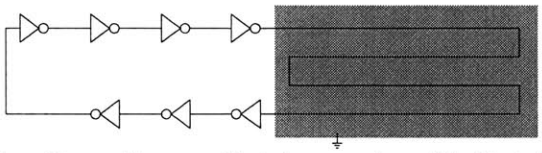

Figure 2-12: Fringing Capacitance - Metal *m* snake with Metal *m-1* ground plane underneath

This structure is laid out in the MOSIS 0.25 μm chip with loads (or "snakes") on metal 1, 2 and 3. The widths of the metals are the minimum allowed by this technology: 0.32 μm for metal 1 and 0.4 μm for metal 2 and metal 3. The spacing between the wires is about 4 μm (or ~10 times minimum distance) for all metal layers. Metal 2 and metal 3 snakes are placed on top of metal 1 and metal 2 ground planes respectively. These ground planes are 20 μm x 50 μm in size. There is one structure with a metal 1 snake with a similar polysilicon ground plane, and another metal 1 structure with nothing underneath.

2.2.3 Coupling Capacitance Interconnect Structure

Coupling capacitance is the capacitance associated between adjacent metal structures within the same metal layer. The structure consists of the same snake-like interconnect shape as the structures that measure fringing capacitance. However, these coupling capacitance structures also have the same metal layer surrounding the snake structure, as shown in Figure 2-13. This emphasizes the coupling capacitance associated between the sidewalls of the snake structure and metal structure surrounding it. The surrounding metal structure is connected to ground to further accentuate this capacitance.

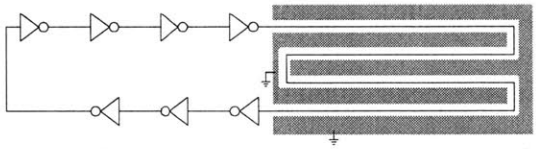

Figure 2-13: Coupling Capacitance. Metal *m* snake and ground at minimum distance

This structure is laid out in the MOSIS 0.25 μm with loads and ground planes on metal 1, 2 and 3. The snakes are the same as used in the fringing structure. The minimum spacing between wires depends of the type of wire used. The spacing used for the metal 1 structure is 0.32 μm, and for metal 2 and 3 it is 0.4 μm.

2.2.4 Plane Capacitance Interconnect Structure

Planar capacitance is the capacitance between the parallel surfaces of the metal layer and its top or bottom neighbor, whether it is another metal layer or the substrate. The structure consists of a large metal square structure, large enough to be the dominant load of the oscillator (minimizing the fringing capacitance contribution), as shown in Figure 2-14. The large metal plane is placed on top of another lower-metal plane that is grounded. No other wires are close to it, so the coupling effect should not be present.

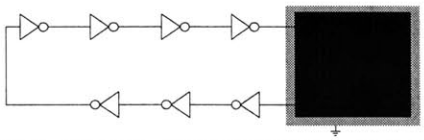

Figure 2-14: Plane Capacitance. Metal *m* plane and *m-1* ground plane underneath

This structure is also laid out in the MOSIS 0.25 μm test chip with loads and ground planes on metal 1, 2 and 3. The loads are metal in a square shape that measures 15 μm long per 15 μm wide, with a ground plane underneath of a lesser metal number. The ground planes are slightly larger (10 μm larger on each side) to avoid misalignments during lithography affecting the plane capacitance. There are two structures with a metal 1 load, one with a polysilicon ground plane underneath and another one with just the substrate.

2.2.5 Vertical vs. Horizontal Structures

The vertical and horizontal BEOL structures are designed to investigate if interconnect variations have a dependency in the orientation in which the wiring is done. Thin wires (0.32 μm wide) of metal-1 simulate interconnect lines prone to variations due to the Δ-width, while thick wires (2 μm wide) are robust to variation.

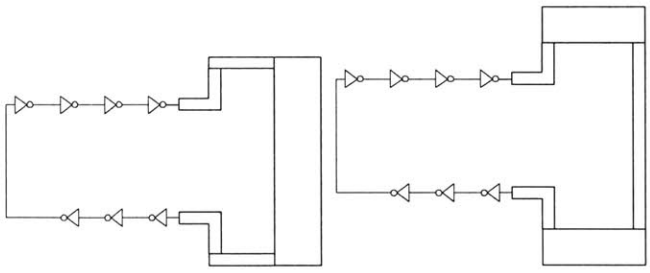

Figure 2-15: Horizontal (left) and vertical (right)

These structures are designed with almost equivalent loads to have almost equivalent output frequencies, as shown in Figure 2-15. The horizontal structure (top) has a total length of 20 μm of thin horizontal wire and 20 μm of thick vertical wire. The vertical

structure (bottom) has a total length of 20 μm of thin vertical wire and 20 μm of thick horizontal wire. The elbow used to reach the loads is also in thin metal-1 and measures 3.05 μm in the top and 5.05 μm in the bottom for the vertical structure and 3.89 μm in the top and 5 μm in the bottom for the horizontal structure. These measurements make the equivalent amount of interconnect load of almost identical equivalent dimensions.

2.2.6 ILD Structures

These test structures are designed to assess the vertical geometric variations in a given metal layer. Using the planar capacitance formula from Sakurai [7], the planar capacitance is a function of the thickness (*T*), width (*W*), length (*L*) and height (*H*), with dimensions as shown in Figure 2-16. Nassif [8] proposed the idea of extracting the capacitance ratio by building structures with different *W* to *L* ratios. If *L* is kept the same, then the capacitance of two structures with different widths would be:

$$\frac{C_1}{C_2} = \frac{f(W_1, H, T)}{f(W_2, H, T)}$$

This means that three structures with same *L* and different *W* provides an equation for *C1/C2* and another for *C1/C3*, which gives two equations in *T* and *H*. The ILD thickness may then be calculated by solving for the height *H*.

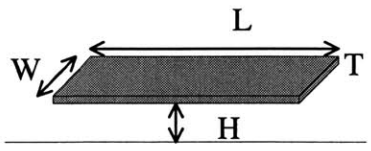

Figure 2-16: Planar Capacitance dimensions

Five structures are included in the MOSIS 0.25 μm test chip to investigate the feasibility of this approach. There are structures with dummy inverters, such as the canonical BEOL structure (the buffer at the output that works as a load), a structure

called ILD1, with a dummy inverter in addition to the buffer, and *ILD2*, with two dummy inverters. These structures are intended to support the extraction of the capacitance due to the inverters chain. The plane capacitance structures with different widths are the already mentioned plane capacitance interconnect structure, and another structure similar but with $W = 45$ μm. These structures have the loads necessary to calculate H.

2.3 Summary

This section has described the fundamental ring oscillator test structures for investigation of process induced variation. By making each structure, or each family of structures, primarily sensitive to a particular variation source, the pattern induced impact of these variations can be studied. Both front-end-of-line (FEOL) and back-end-of-line (BEOL) structures have been described. The assembly of these different types of RO structures into the full test chip will be described in Chapter 3.

Chapter 3

Chip Architecture and Testing Setup

The architecture for the 0.25 μm run chip, also known as the *variation-2* (V-2) chip, is designed for better data acquisition while improving the density and testability of the 0.35μm or *variation-1* (V-1) chip. This architecture, designed by J. Panganiban [3] with Nassif's [1], [8] research group collaboration, improves density by about 10 times, going from approximately 200 ring oscillators in V-1 to approximately 2000 in V-2.

Variation-2 emphasizes hierarchy, regularity, and repetition in a scan chain approach. This approach helps to transfer the test chip design to other technologies using automated tools. The chip is composed of macro-blocks and sub-blocks. This chapter focuses on the three major blocks of V-2: the tile, row, and chip blocks. It also describes the setup to automate measurements through LabVIEW.

3.1 Tile

The tile sub-block is the basic building block of the chip. Each one of the tiles contains a ring oscillator and control circuitry, as shown in Figure 3-1.

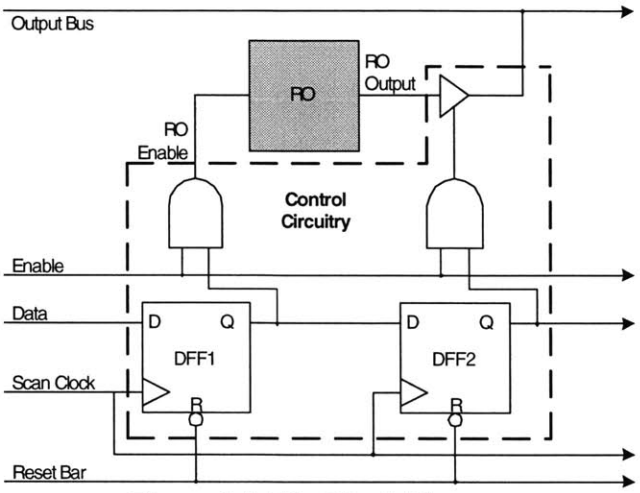

Figure 3-1: Tile Block Diagram

Two shift registers control the ring oscillators. The output of the left register enables the ring oscillator, while the output of the second register passes the RO signal onto the output bus. The output of the ring oscillator is connected to the input of a tri-state buffer, whose enable input is connected to the output of the second register, and the tri-state's output is wired to the output bus.

The ring oscillators of some interconnect structures are too large to fit in a single tile, and there is a special tile for these structures. These tiles are called *Double Tiles*, and are the size of two regular tiles. They contain two control circuits per tile, as shown in Figure 3-2. The second control circuit is not connected to any oscillator, and its output is 0 Hz. These outputs are used to verify the scan chain and make sure that the location we mean to measure is indeed the one being scanned.

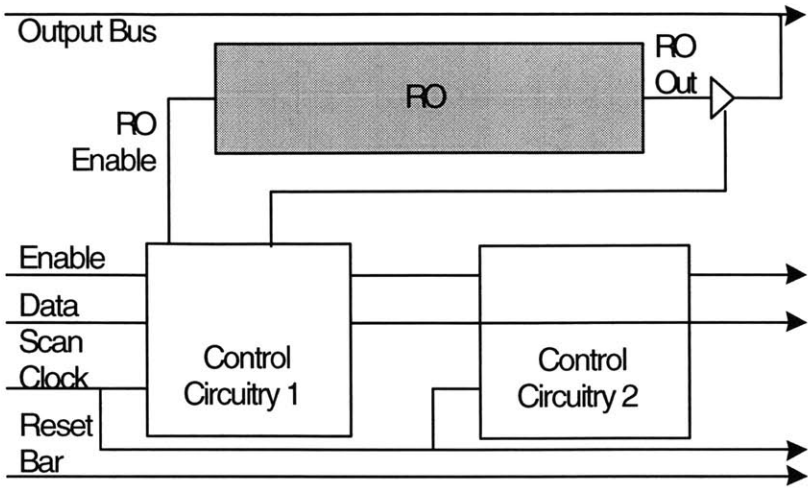

Figure 3-2: Double Tile Block Diagram

Each one of the tiles has four input signals: *scan-clock* (the clock for the shift registers), *data* signal (the control signal for the DFF), *enable* (used with the AND gates to enable the RO), and *reset* (resets the registers). They have one overall *output bus* signal.

3.2 Row

A horizontal chain of tiles comprises the row sub-block, which extends across the width of the chip. This array is shown in Figure 3-3.

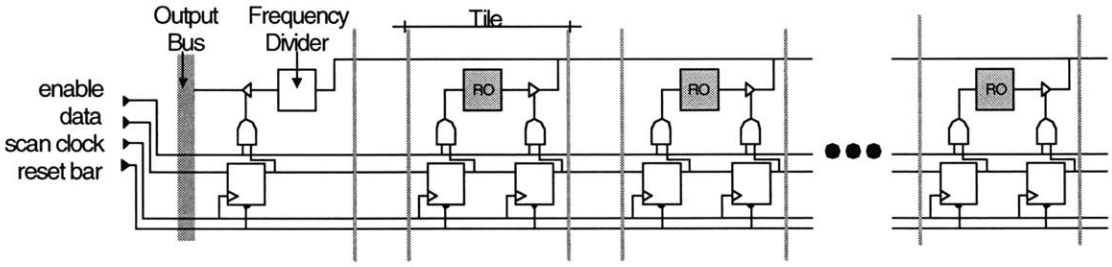

Figure 3-3: Row Block Diagram

Buffers are used at the beginning of each row to buffer the four input signals and drive them to every tile in the row. A divider tile divides the frequencies of the output bus down to a more measurable frequency for off-chip measurement. This divider tile

also has a control register for the tri-state used to drive the *row output bus*, which connects the divider outputs of each row.

Each row consists of 43 tiles, counting each double tile as two tiles.

3.3 Chip

A representation of the entire chip is shown in Figure 3-4. Each chip consists of 54 rows of ring oscillator and 6 rows of higher polysilicon density, for a total of 60 rows. The 54 rows of normal polysilicon density have 43 tiles each. There are 30 tiles among all 6 high polysilicon rows, for a total of 2,352 tiles per chip. We have 35 replicates of bounded chips, for a total of 82,320 tiles accessible by a ceramic package. There are five un-bonded chips, for a total of 11,760 tiles that are accessible by a probing station.

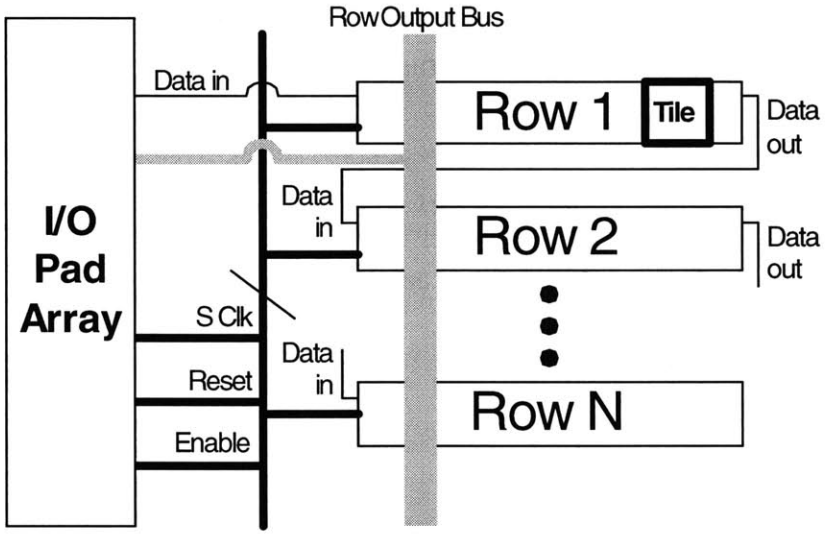

Figure 3-4: Chip Block Diagram

The fabricated chip for the MOSIS 0.25 µm looks as follows. Fabricated in TSMC technology, the measurements of the die are 4 mm by 2.5 mm, as shown in Figure 3-5.

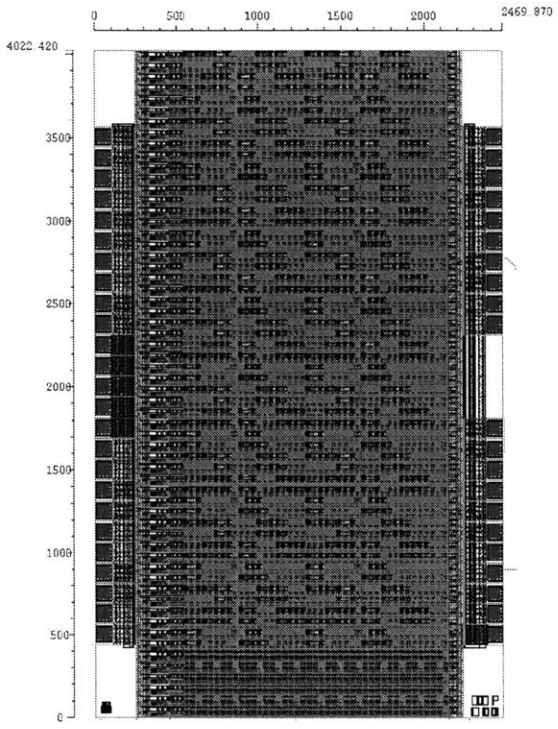

Figure 3-5: Chip Layout

3.4 Testing Report

Each chip contains 46 pads, and 22 of these are wire bonded to a standard 40 pin DIP package. The wire-bonded signals are the scan-clock, enable, data-in, nres, output, data-last (for debugging purposes), 5 oscillator power supplies, 3 logic power supplies, and 8 grounds. A diagram of the wire bonding is shown in Figure 3-6.

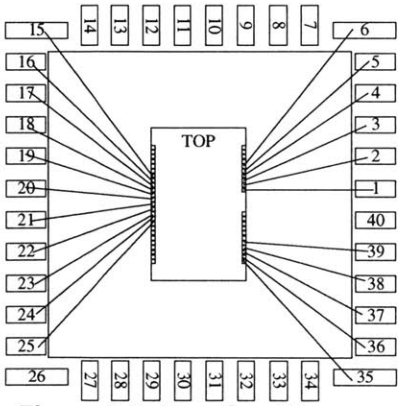

Figure 3-6: Bonding Diagram

The testing process is automated using a SCB-68 PC Card from National Instruments. This card is suitable because of its portability and flexibility, and it contains the features required to test the chip, such as DAC's and frequency counters. It can also be easily programmable through LabVIEW.

The scan chain architecture makes it easy to specify which oscillator to measure through LabVIEW. LabVIEW sends the stream of bits that turn on a specific oscillator. At most one ring oscillator is ever on.

Figure 3-7 shows the custom level-converter circuitry added to interface between the NI card and the test chip. Since the card can only deliver a 5 V nominal voltage, the level-converter circuitry delivers the lower voltages needed for test. Another level-converter is connected to the output pad of the chip. This is used to convert the 2.5 V oscillating output to a 5 V signal needed as input to the frequency counter of the NI card.

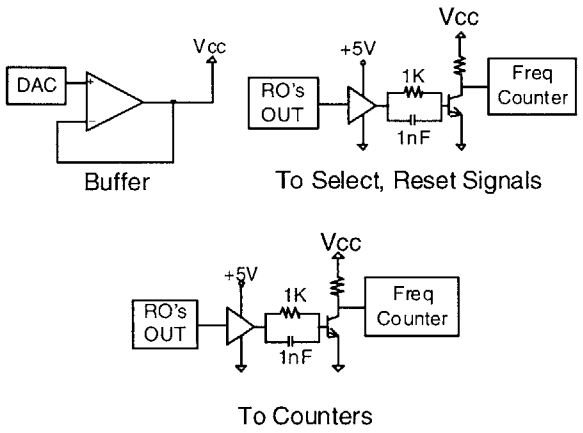

Figure 3-7: Schematics of Circuitry Added to PC Card

3.5 Summary

The variation-2 (V-2) chip is composed of three main building blocks: the tile, row, and chip blocks. The tile is the main building block, comprising the oscillator and control

circuitry. A row is a group of tiles, and the chip is the group of all rows. There are a total of 60 rows in a chip or 2,352 tiles.

The hierarchy of the chip makes it easy to read the output through LabVIEW. The chips are accessed through a SCB-68 PC Card from National Instruments, while LabVIEW sends the input signals and reads the output.

Chapter 4

FEOL Test Structures Testing and Analysis

This chapter analyzes the front end of line (FEOL) test structures based on electrical test data, focusing on structure functionality, frequency response, and variation due to layout practices. Section 4.1 first discusses the functionality of the structures to determine which work as expected when tested. The statistical methodology used to identify chip-to-chip, within-chip, and structure-to-structure frequency variation components is presented in Section 4.2. In Section 4.3 we then examine the resulting measurements for various sets or families of structures in order to understand how structures within that family differ due to designed layout practices. First, density vs. isolation structure analysis investigates how the channel length variation changes when different structures have the same total gate length but using a different number of fingers. The proximity and poly structure analysis focuses on the impact on channel length due to the global effect of polysilicon pattern density (polysilicon loading around a ring oscillator) and the local effect of polysilicon proximity (due to interaction between the different fingers of polysilicon in a device). The vertical structure analysis studies the effect of orientation in the behavior of devices. The P/N structures analysis investigates if variations are different in P-type or N-type devices. Finally, in Section 4.4 the chapter is summarized and suggestions for future analyses of the front end of line test structures are offered.

4.1 Functionality

The data shown in Figure 4-1 illustrates an example set of RO frequency measurements for a single chip, where the output (divided) RO frequency is measured and plotted for a sweep of power supply voltages from 1 V to 2.5 V for each structure on the chip (excluding the poly density structures). We see that nearly all structures behave as expected: RO frequencies on the order of a few MHz are observed, and the frequencies increase with larger power supply as expected. Nearly all structures operate across the full range from 1 V to 2.5 V power supply, with the notable exception of the "PN-J-ish" structures that oscillate too fast for the control circuitry at higher voltages. Because this structure cannot be analyzed at 2.5 V as all other structures can, we will omit this structure from our analyses in the rest of this chapter. For the remaining structures, we will primary focus on the observed RO frequency at the full power supply voltage of 2.5 V. Appendix I proposes a method of using these to identify threshold voltage variation information.

In addition to successful output of an RO frequency, a second functionality question is how repeatable these electrical measurements are. To examine this, all 2,352 structures within a particular chip are measured five times, and the standard deviation across these five measurements for each of the 2352 structures is calculated. An aggregate indicator of measurement variation is then formed by dividing the root-mean-square (RMS) value of all standard deviations by the mean of the frequency. The resulting electrical repeatability is about 0.1%. It should be noted that for shorter measurement times (i.e., for shorter lengths of time for acquisition), this repeatability can degrade due to too few RO periods being gathered. For long enough measurement periods as used here, the measurement

repeatability is excellent and the measurement variation is small enough that we will neglect this variation in the analyses to follow.

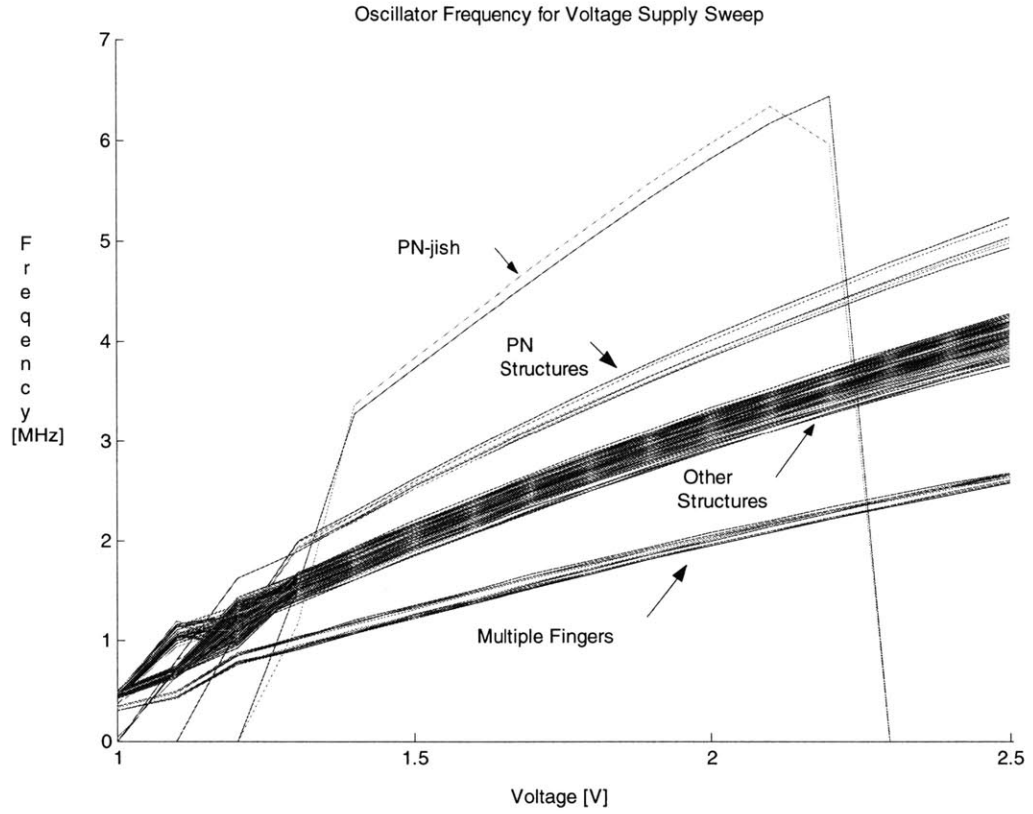

Figure 4-1: Frequency Response for All Structures

4.2 Statistical Analysis Methodology

In this chapter, we focus on two key questions related to the observed variation in RO frequency. The first goal is to consider the observed total variation in each type of test structure, and to decompose that variation into two components: "chip-to-chip" variation giving an indication of across wafer effects, and "within-chip" variation due to the effect of local or global layout environment on the test structure. We will see that some test structures are more prone to vary across the wafer than others. Similarly, we will also see that some test structures appear to be more sensitive to within-chip layout factors.

The second goal of the statistical analysis in this chapter is to consider particular layout practices in more detail and identify their likely impact on RO frequency. To accomplish this, sets of structures designed to investigate each layout effect are considered. In general, we will be interested in two characteristics of the resulting RO measurements: to what extent has the *mean* RO frequency been affected, and to what extent has the RO frequency *variance* (or standard deviation) been impacted.

4.2.1 Chip-to-chip and Within-chip Variance Components

As illustrated in Figure 4-2, there are two components of variation we would like to understand and separate based on measurements of frequency across multiple replicates and multiple chips of a particular ring oscillator structure type. First, there is some spread in RO frequency within each chip for that particular test structure type – the within-chip variance (across the replicates of that test structure within each chip, shown as a vertical set of points in the figure). Second, there may also be variation or differences between the mean frequencies (the line drawn within each chip group in the figures) from one chip to the next. We summarize these components of variation and their computation below.

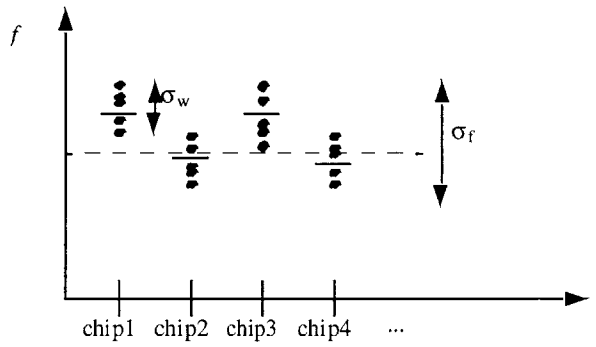

Figure 4-2: Schematic representation of chip-to-chip versus within-chip variation.

Total variation: Let r be the number of ring oscillator replicates within a given chip of some test structure type being considered, and c be the number of different chips being

considered. We assume that r is the same for all chips. Let $\bar{f}$ be the grand mean across the total number of ring oscillators cr of a given type being measured. Then the total sample variance s_f^2 in frequency including both chip-to-chip and within-chip variance components is:

$$s_f^2 = \text{var}(f) = \frac{1}{cr-1}\sum_{j=1}^{c}\sum_{i=1}^{r}(f_{ij} - \bar{f})^2$$

Chip-to-chip variation: The chip-to-chip variation is based on the differences observed between the means of frequency from one chip to the next. If $\bar{f}_j$ is the mean frequency for the j^{th} chip, then the component of variance that is due to chip-to-chip variation, s_c^2, is given by

$$s_c^2 = \frac{1}{c-1}\sum_{j=1}^{c}(\bar{f}_j - \bar{f})^2$$

Within-chip variation: The within-chip variation can now be "backed out" using the fact that the total variance is the sum of the chip-to-chip and within-chip sample variance s_w^2 (under the assumption that the "true" within-chip population variance σ_w^2 is approximately the same from one chip to the next) using $s_f^2 = s_c^2 + s_w^2$ or $s_w^2 = s_f^2 - s_c^2$.

To get a better qualitative feel for the observed variation numbers we will sometimes present a "percent variation" as a scaled ratio of the standard deviation to the mean. In particular, in the table below, these are normalized by the overall frequency mean for that test structure, e.g. $s_w^{\%} = \frac{s_w}{\bar{f}} \cdot 100$ gives the percent within-wafer standard deviation for some structure of interest. Finally, we note that the within-chip variation may be greater

than or less than the chip-to-chip variation – the sources of variation would physically be different and one or the other could well be larger.

4.2.2 Evaluation of Mean Differences and Variance Ratios

In many cases, we will be interested in determining how significant an observed mean difference is between two or more samples. For the example shown earlier in Figure 4-2, we might ask whether the mean difference is "real" – that is, how unlikely is it that we would observe the indicated mean difference given the spread within each set of measurements. We will use the analysis of variance, or ANOVA, formulation in the work below. In this case, the ratio of variance explained by group-to-group variation as a whole (e.g. s_c^2 in the example figure) is compared to the within group variation (e.g., s_w^2), and this ratio evaluated using an F test.

We will also be interested in understanding if the spread or variance observed in two populations are "the same" or significantly different. For example, we might want to understand if the variance in chip 1 is different than in chip 2, or if the observed ratio of variances is likely to occur simply by chance given the spread and number of measurements taken within each chip. Here again we will use an F test to make this evaluation.

4.3 Structure Variation Components

Thirty-five chips are measured, with all FEOL test structures (except the PN-J-ish ring oscillators) measured at 2.5 V power supply voltage, and the results shown in Table 4-1. The first column indicates the "description" or family to which that structure belongs, followed by the particular RO type. The mean $\bar{f}$ and standard deviation σ_f of the structure frequency averaged across all chips and all replicates for that particular

structure are then shown. The final two columns indicate the chip-to-chip variation σ_c and within-chip variation σ_w for that test structure type, computed as described earlier.

In examining this table, we note that the single finger and D/I structures appear to vary substantially less across the chip compared to the other structures. This also appears to be true for many, but not all, of the single finger and D/I structures when we consider the within-chip variation. These structures emphasize RO structures with channel lengths larger than the minimum feature size and so it is not surprising that they are less sensitive in general to process variation.

Description	FEOL RO Types	Mean Frequency [MHz]	Total Variation σ_t [KHz]	Chip-to-chip σ_c [KHz]	Within-chip σ_w [KHz]
P/N	PN Structure, Canonical	4.00	133	126	43.6
	PN Structure, 2P And 2N	5.29	164	154	55.6
	PN Structure, 1P And 1N	0.00	0	0	0.0
	PN Structure, N Strong	5.47	172	161	60.9
	PN Structure, P Strong	5.23	163	153	54.6
Single Finger	Single Finger	4.25	52	47	21.5
	Small Single Finger	4.23	51	48	17.7
Canonical	Canonical FEOL	4.42	130	122	45.2
D/I	2 Fingers, 1.5x Minimum Length	4.21	76	73	18.7
	4 Fingers, Minimum Length	2.76	77	71	28.2
	2 Fingers, 2x Minimum Length	2.64	39	36	14.8
	Single Finger, 4x Minimum Length	2.70	29	25	13.2
Proximity	1.5x Spacing Between Poly Lines	4.20	127	122	34.2
	2x Spacing Between Poly Lines	4.13	129	120	46.3
	3x Spacing Between Poly Lines	4.12	135	126	49.3
	1.2x Spacing Between Poly Lines	4.30	132	123	48.2
Vertical	Vertical Canonical FEOL	4.36	144	135	50.7
	Vertical, 3x Spacing Between Poly Lines	4.05	143	134	49.2
	Vertical Single Finger	4.22	59	51	30.5
Poly	0% Polysilicon Density	4.38	126	124	27.0
	12% Polysilicon Density	4.36	127	125	22.7
	25% Polysilicon Density	4.32	129	125	30.4
	50% Polysilicon Density	4.29	128	124	33.4
	Canonical At End Of Density Structures	4.38	126	120	40.0

Table 4-1: FEOL Structures Frequency Response

In the following subsections, we consider layout-induced differences in variation for each of the different families of test structures.

4.3.1 Dense vs. Isolation and Single Finger Structures

Several important variation effects can be seen by examination of the dense vs. isolated (D/I) RO structures. The key effect being probed with these structures, is to what degree does variation increase if ring oscillator devices have their channel length "split" across multiple fingers but with an equivalent (designed) total channel length. As a reminder, the minimum feature dimension in this design is 0.25 μm, so the single finger with 4x (4 times) minimum length structure has a total channel length of 1 μm, and the 3x minimum length single finger structure has a total channel length of 0.75 μm. If the RO variation is sensitive to the total channel area, then the single finger and split or multiple finger structures should all behave similarly. If the RO frequency is most sensitive to variations along an "edge" of a finger (e.g. line width variation due to lithography), then we would expect that the multiple finger devices will suffer more variation.

The results for the D/I test structures are summarized in Figure 4-3, Figure 4-4, Table 4-2, and Table 4-3. If we first consider Figure 4-2, we see that there is a clear mean difference in frequency observed for both the 3x and 4x minimum sized structures. Interestingly, the two-fingered variants appear to be slightly slower than the single finger version, and the three or four-fingered variants are appreciably faster than the fewer fingered variants. Our conjecture is that these mean frequencies depend on the interplay between channel length variation effects, as well as additional parasitic capacitances which are affected by the number of fingers in the structure. Future work should consider

the possibility of separating out the parasitics (e.g. overlay capacitance) from the channel length effects.

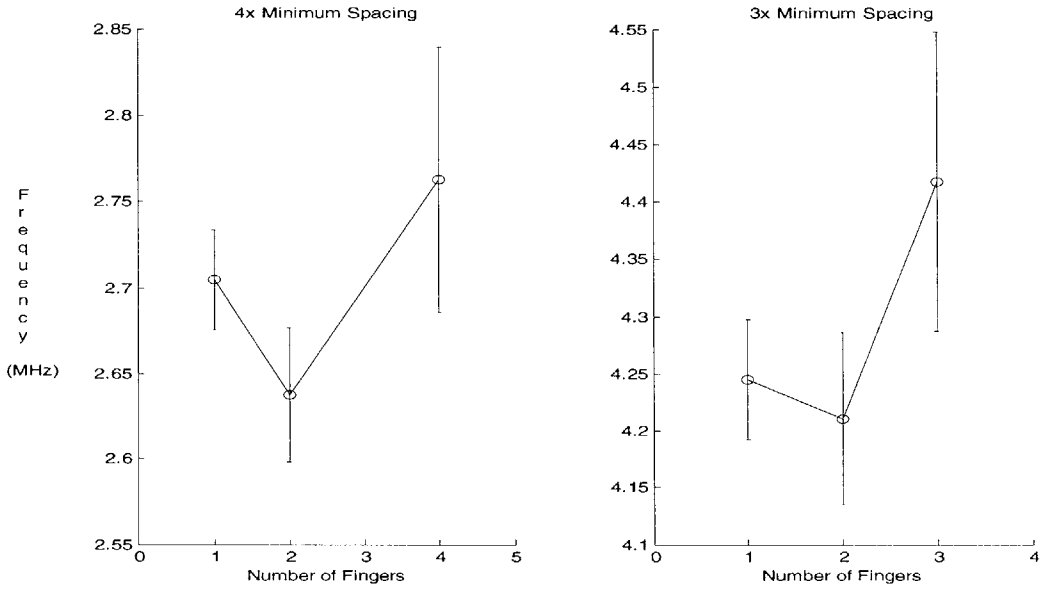

Figure 4-3: Mean Differences for Dense vs. Isolated Structures

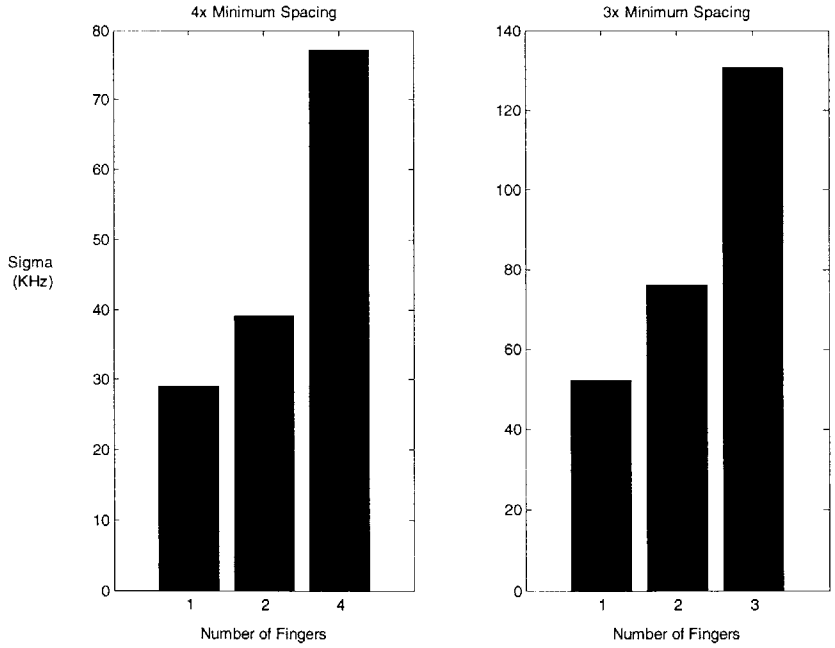

Figure 4-4: Total Standard Deviations for Dense vs. Isolated Structures

Looking at the one-sigma error bars shown in Figure 4-3, we can replot the standard deviations for these RO variants in Figure 4-4 to more clearly examine the effect of

number of fingers on the *variance* rather than the mean in the observed RO frequency. Here we see a clear increase in the overall standard deviation as we increase the number of fingers, in both the 3x and 4x minimum sized structures. Table 4-2 quantifies this effect, seen in both the chip-to-chip and within-chip percent standard deviations for these structures. This is consistent with our expectation that more "edges" or fingers gives more opportunity for line width variation to have an impact. As a crude estimate, if the ΔL variations from one finger to the next are independent (not a very good assumption), then we might expect the total variance for a four fingered structure to have four times the variance of a single fingered structure, or a factor of two in the standard deviation. This is consistent with the within-chip observation of 1.02% standard deviation in the four fingered structure compared to 0.49% standard deviation for the single finger structure (in the 4x minimum spacing set) seen in Table 4-2. Another area for future investigation is to determine to what extent "inner" versus "outer" edges of these fingered test structures might be sensitive to line width or other variation, particularly in the case when such ΔL variation is not independent and additive.

If we consider the ratio of the overall variance of the 4-fingered, minimum length structure to the variance of the single finger, 4x minimum length structure we get $r = (77/29)^2 = 7.05$. The inverse of the cumulative distribution function (cdf) for F gives a critical ratio corresponding to the largest ratio of variances one would expect to observe with a given probability, and for specific degrees of freedom in the numerator and denominator variances. In this case we choose a 95% probability, and the nominator and denominator degrees of freedom are the number of the specific type of ring oscillators (for all chips) minus one. If we compare the ratio 7.05 to $F_{0.95,\ 1889,\ 1889} = 1.08$ (in this

case, we have 54 of these structures in each chip, times 35 chips), we see that the observed expansion in variance is indeed significant at the 95% confidence level. The largest component of variation is due to chip-to-chip variation, as shown in Table 4-2 and Table 4-3.

Test Structure		Standard Deviation		
		Overall σ%	Chip-to-chip σ%	Within-chip σ%
Four Times Minimum Spacing	Single Finger, 4x Minimum Length	1.07%	0.96%	0.49%
	2 Fingers, 2x Minimum Length	1.48%	1.37%	0.56%
	4 Fingers, Minimum Length	2.79%	2.60%	1.02%
Three Times Minimum Spacing	Single Finger	1.23%	1.12%	0.51%
	2 Fingers, 1.5x Minimum Length	1.80%	1.75%	0.44%
	Canonical FEOL	2.95%	2.77%	1.02%

Table 4-2: Density vs. Isolation Analysis

Test Structure		% of Variance	
		Due to Chip-to-chip	Due to Within-chip
Four Times Minimum Spacing	Single Finger, 4x Minimum Length	79.36%	20.64%
	2 Fingers, 2x Minimum Length	85.54%	14.46%
	4 Fingers, Minimum Length	86.68%	13.32%
Three Times Minimum Spacing	Single Finger	83.19%	16.81%
	2 Fingers, 1.5x Minimum Length	93.95%	6.05%
	Canonical FEOL	87.99%	12.01%

Table 4-3: Density Vs. Isolation Structures; Variation Decomposition

Finally, we can also use the D/I structures to illustrate an additional point about the observed variation in nearly all of the test structures examined here. In Table 4-3, we show the percentage of the total variation (across all 35 chips for all replicates of each structure type) due to chip-to-chip (across wafer) variation, and due to within-chip (e.g. layout neighborhood induced) variation. The great majority, typically 80 to 94%, of the variation (variance) is dependent on the location of the chip within the wafer. This measures the degree to which the chip seems to move "as a whole" around some mean

value of RO frequency that depends on wafer location. The remaining 6 to 20% of the variance appears to be due to location within the chip. This variation may be a combination of spatial patterns imposed by the projection of gentle wafer trends onto the chip, as well as systematic layout environment effects. We return to the wafer level and die level spatial patterns in Chapter 6, the spatial analysis chapter.

4.3.2 Polysilicon Proximity Structures

The *Proximity Effect Structures* are the *1.5x Spacing Between Poly Lines*, *2x Spacing Between Poly Lines*, *3x Spacing Between Poly Lines*, and *1.2x Spacing Between Poly Lines* structures as tabulated in Table 4-1 and summarized in Figure 4-6. The key question being investigated here is the extent to which the spacing or proximity between individual lines or fingers in the RO inverter affects frequency shifts and variance ratios.

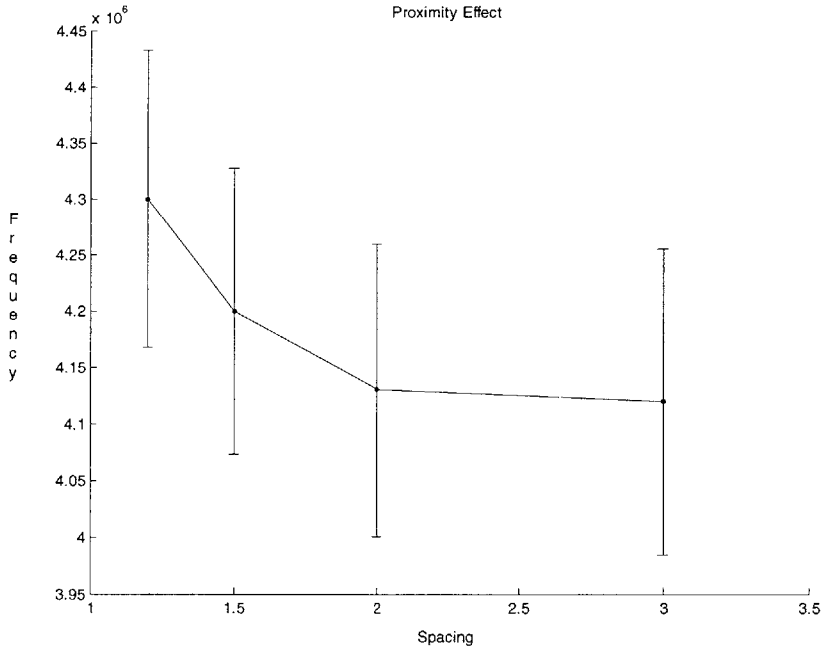

Figure 4-5: Local Polysilicon Proximity Effect

A strong trend is observed in this figure: larger spacing or separation between poly fingers leads to slower RO frequency. This suggests that the channel length is somewhat

reduced as we pack the transistor fingers more closely together, consistent with a lithographic or etch proximity effect that shortens or narrows these features as they approach each other. Alternatively, it is possible that the parasitic capacitances in these structures are affected as the finger spacing changes.

This spacing between neighboring polysilicon lines (the local proximity effect) results in an approximately 4.4% change in the resulting mean frequency, or an average of 4.3 MHz for the minimum spaced finger structures and an average of 4.12 MHz for the three times minimum-spaced-fingers structures. The results of a one-way ANOVA analysis for comparing the means of the spacing structures are shown in Table 4-4. In this table, the "columns" variability source refers to the four levels for the spacing parameter. The F ratio of 1236 confirms that the mean differences between the different spacing polysilicon structures are highly significant.

Source	SS	Df	MS	F	Prob>F
Columns	6.333e+13	3	2.111e+13	1236	0
Error	1.93611e+14	11336	1.70793e+10		
Total	2.56941e+14	11339			

Table 4-4: ANOVA Table for Proximity Structures

We can also examine the effect of the *Proximity Effect* structures on the variance: the overall standard deviation percentages are 3.07%, 3.02%, 3.11% and 3.28% for the 1.2x, 1.5x, 2x, and 3x line spacing structures. In this case, there is only a modest increase in the variation as we increase the line spacing; the spread in frequencies is almost the same independent of the line spacing between the structures. We can use an F test to determine if the observed variance ratios are significant, as discussed in Section 4.2.2 above. If we consider the ratio of the overall variance of the 3x line spacing structure to the variance of the 1.2x spacing structure, we get $r = (135/132)^2 = 1.046$. If we compare this to $F_{0.95, 2834, 2834} = 1.06$, we see that the observed expansion in variance is not significant at the 95%

confidence level. The largest component of variation is due to chip-to-chip variation, as shown in Table 4-8 and Table 4-9.

Test Structure		Standard Deviation		
		Overall σ %	Chip-Chip σ%	Within-chip σ%
Proximity	1.2x Spacing Between Poly Lines	3.07%	2.86%	1.12%
	1.5x Spacing Between Poly Lines	3.02%	2.91%	0.82%
	2x Spacing Between Poly Lines	3.11%	2.90%	1.12%
	3x Spacing Between Poly Lines	3.28%	3.05%	1.20%

Table 4-5: Polysilicon Proximity Effect Analysis

Test Structure		% of Variance	
		Due to Chip-to-chip	Due to Within-chip
Proximity	1.2x Spacing Between Poly Lines	86.70%	13.30%
	1.5x Spacing Between Poly Lines	92.71%	7.29%
	2x Spacing Between Poly Lines	87.01%	12.99%
	3x Spacing Between Poly Lines	86.68%	13.32%

Table 4-6: Polysilicon Proximity Effect; Variation Decomposition

4.3.3 Polysilicon Density Structures

The *Poly Density Structures* are the family of 0% to 50% polysilicon density structures, with mean and standard deviation information shown in Table 4-1 and summarized in Figure 4-6. By analyzing the frequency response of these structures we may explore the effect of a more global or regional polysilicon pattern density on RO variation. As a reminder, these structures are formed using a ring oscillator tile with the surrounding eight tiles filled with polysilicon patterns at the specified pattern density, thus forming a spatial region of approximately 114 μm by 200 μm of the designated pattern density around the tile of interest.

We observe in Figure 4-6 that the measured RO frequency decreases slightly as the polysilicon pattern density increases. This is an interesting trend, and may be related to polysilicon plasma etch loading effects. When the poly pattern density increases, the amount or area fraction of polysilicon that must be removed through etch decreases. If we take slower RO frequency as an indication of wider poly features, then the observed trend

would suggest that regions with less poly to be removed actually etch somewhat more slowly. This runs counter to conventional "etch loading" expectations, and is an interesting area for further investigation. To confirm the significance of the observed mean differences in frequency, a one-way ANOVA is shown in Table 4-4, where the "columns" variation source refers to the four levels of polysilicon pattern density considered. The F ratio of 21.79 indicates an extremely low probability that the means of the different polysilicon density structures are equal and thus poly density has a significant effect on RO frequency.

Source	SS	df	MS	F	Prob>F
Columns	1.05529e+12	3	3.51763e+11	21.79	1.36224e-13
Error	1.34972e+13	836	1.61449e+10		
Total	1.45525e+13	839			

Table 4-7: ANOVA Table for Polysilicon Density Structures

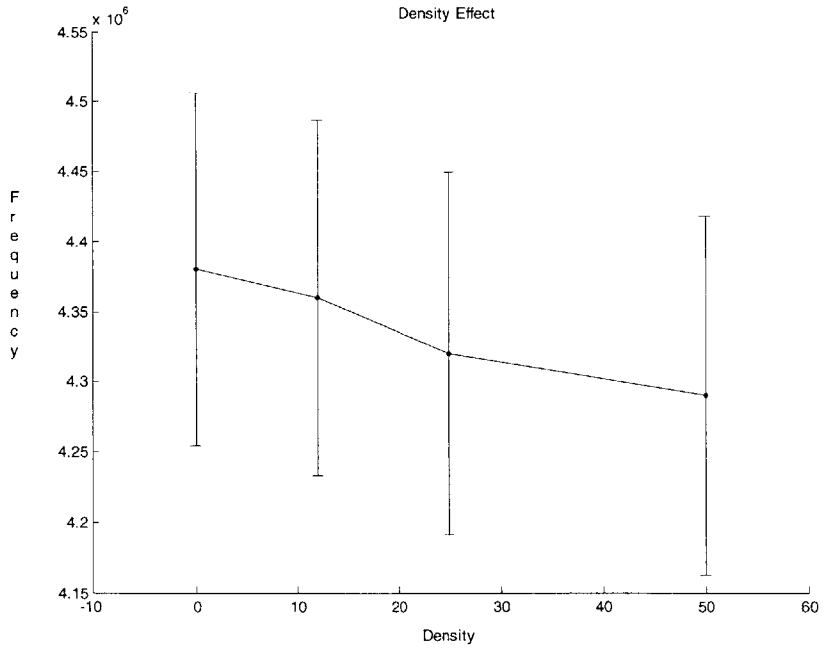

Figure 4-6: Global Polysilicon Density Effect

We can also ask how the poly-density structures impact the spread or variation in RO frequency. Here we see that the *Poly-Density* structures have overall standard deviation

percentages of 2.89%, 2.91%, 2.98% and 2.99% for the 0, 12, 25, and 50 percent polysilicon density structures as summarized in Table 4-8 and Table 4-9. Again, the standard deviation appears to be quite consistent across the different pattern density structures. While we do observe a shift in the mean RO frequency as a function of pattern density, the variance in RO frequency appears not to depend on pattern density.

If we consider the ratio of the overall variance of the 25% polysilicon density structure to the variance of the 0% polysilicon density we get $r = (129/126)^2 = 1.05$. If we compare this to $F_{0.95,\ 209,\ 209} = 1.26$, we see that the observed expansion in variance is not significant at the 95% confidence level. The largest component of variation is due to chip-to-chip variation, as shown in Table 4-8 and Table 4-9.

Test Structure		Standard Deviation		
		Overall σ %	Chip-Chip σ%	Within-chip σ%
Density	0% Polysilicon Density	2.89%	2.82%	0.62%
	12% Polysilicon Density	2.91%	2.86%	0.52%
	25% Polysilicon Density	2.98%	2.90%	0.70%
	50% Polysilicon Density	2.99%	2.88%	0.78%

Table 4-8: Polysilicon Density Effect Analysis

Test Structure		% of Variance	
		Due to Chip-to-chip	Due to Within-chip
Density	0% Polysilicon Density	95.45%	4.55%
	12% Polysilicon Density	96.78%	3.22%
	25% Polysilicon Density	94.44%	5.56%
	50% Polysilicon Density	93.22%	6.78%

Table 4-9: Polysilicon Density Effect; Variation Decomposition

4.3.4 Vertical vs. Horizontal Structures

The vertical versus horizontal RO structures are identical in all ways, except their orientation on the layout. If all of the fabrication processes were insensitive to wafer orientation, we would expect these structures to result in identical RO frequencies. The mean and standard deviations of the observed frequencies are presented in Table 4-1. Here we see that all of the vertical structures have a larger sigma and lower frequency

than their counterpart horizontal structure. In particular, the vertical canonical, 3x spacing and single finger structures have average frequencies of 4.36 MHz, 4.05 MHz, and 4.22 MHz respectively, while their horizontal twins have frequencies of 4.42 MHz, 4.12 MHz, and 4.25 MHz, or an offset in frequency of 1.36%, 1.7% and 0.7% respectively. Even though the changes are small, they are very consistent.

Figure 4-7 plots the average of the vertical and horizontal structures for each of the 35 chips fabricated. The large "jagged" curve indicates a substantial within wafer effect on the RO frequencies. The feature we wish to note, however, is that the vertical structure frequency is consistently lower than that of the corresponding horizontal structure, regardless of chip location within the wafer. This is a very interesting effect; we conjecture that there may be a mask-making scan bias, or an ion implantation effect at work, since both processes systems scan a beam in a preferred direction.

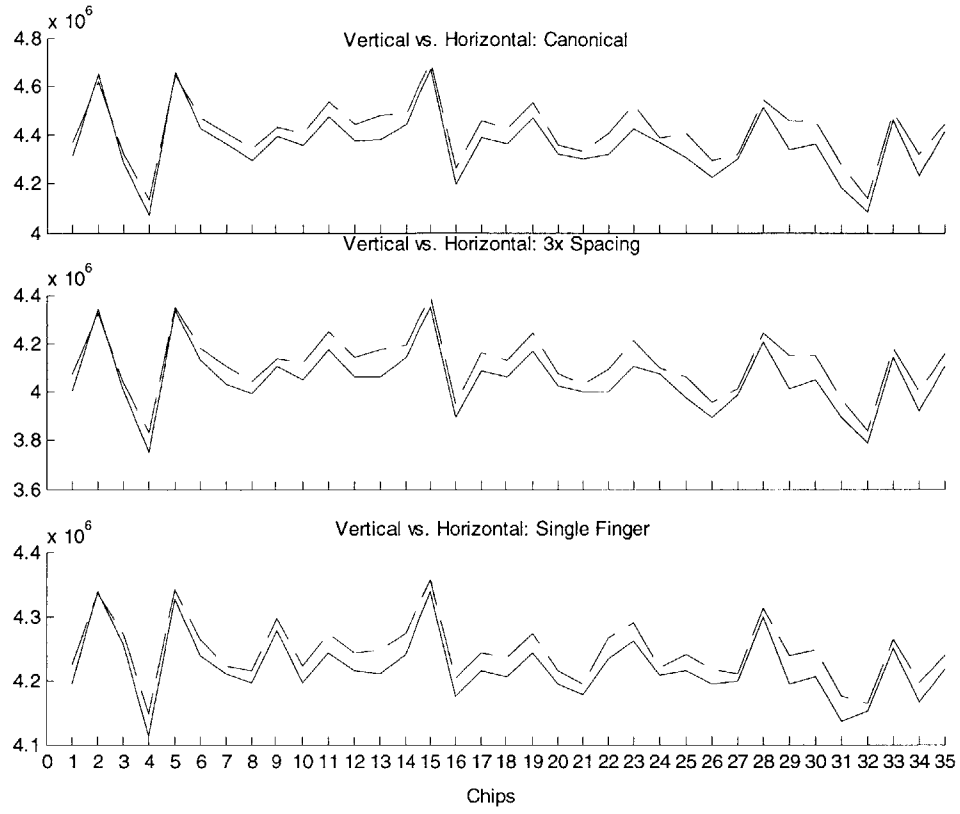

Figure 4-7: Vertical (Solid Line) vs. Horizontal (Dashed Line) Frequency Response

We have already noted that the vertical structures are slower for all chips and all types of structures. Next we consider the effect of orientation on the spread or variance in RO frequency. The overall standard deviation for each vertical structure is higher than their counterpart horizontal structures, as summarized in Table 4-10. The canonical horizontal has a standard deviation of 130 KHz while the vertical has a standard deviation of 144 KHz, or a 10.8% higher standard deviation than the canonical horizontal. The single finger horizontal has a standard deviation of 52.3 KHz while the vertical has a standard deviation of 59.8 KHz, or 14.4% higher than the single finger horizontal. The 3x-spacing horizontal has a standard deviation of 135 KHz while the vertical has a standard deviation of 143 KHz, or 5.9% higher than the canonical horizontal. Finally, we

note that the dominant component of variation is still the chip-to-chip variation, as shown in Table 4-11.

	Overall σ %		Chip-to-chip σ %		Within-chip σ %	
	Horizontal	Vertical	Horizontal	Vertical	Horizontal	Vertical
Canonical FEOL	2.95%	3.31%	2.77%	3.10%	1.02%	1.16%
Single Finger	1.23%	1.42%	1.12%	1.22%	0.51%	0.72%
3x Spacing Between Poly Lines	3.28%	3.52%	3.05%	3.31%	1.20%	1.21%

Table 4-10: Vertical vs. Horizontal Analysis

Test Structure		% of Variance	
		Due to Chip-to-chip	Due to Within-chip
Horizontal	Canonical FEOL	87.99%	12.01%
	Single Finger	83.19%	16.81%
	3x Spacing Between Poly Lines	86.68%	13.32%
Vertical	Canonical FEOL	87.66%	12.34%
	Single Finger	73.95%	26.05%
	3x Spacing Between Poly Lines	88.12%	11.88%

Table 4-11: Orientation Effect: Variation Decomposition

4.3.5 P/N Structures

The P/N structures are intended to explore the effect of variation on P-type versus N-type transistors. The mean and standard deviation values in Table 4-1 show that structures with stronger N-type architecture have a slightly larger standard deviation than do the P-type structures. In particular, we see that the P-Strong structures have an overall standard deviation of 163 KHz, while the N-Strong structures have a 172 KHz standard deviation, or 5.5% higher standard deviation than the P-type. This corresponds to a variance ratio of 1.113; compared to $F_{0.95, 629, 629} = 1.14$, this is not quite significant at the 95% confidence level. Both of these structures show higher variations than the canonical PN-structure (N and P sides equally strong): the canonical PN-structures have a standard deviation of 133 KHz, or 22.6% less than the N-type and 18.4% less than the P-type

Considering the ratio of the overall variance of the N-Strong structure to the variance of the canonical PN-structure we get $r = (172/133)^2 = 1.67$. If we compare this to $F_{0.95, 629, 629} = 1.14$, we see that the observed expansion in variance is significant at the 95% confidence level. It is also significant for the overall variance of the P-Strong structure to the variance of the canonical PN-structure, which is $r = (163/133)^2 = 1.5$. Therefore we can say that the variance ratios between the P-strong structure to the canonical PN and the N-strong structure to the canonical PN are significant.

4.4 Summary

All structures work for all voltages between 1 V and 2.5 V, except for the "PN-J-ish" structures which oscillate too fast for the control circuitry at higher voltages, and therefore are not analyzed at 2.5 V. Considering the RO frequencies at 2.5 V for all the remaining structures, we see several effects. First, for all structures the chip-to-chip variation is substantially larger than the within-chip variation. This is consistent with previously reported trends in process variation, where the chip-to-chip trend remains quite large. However, a pure chip-to-chip variation would imply that, within each chip, the matching between nominally identical structures could still be excellent (and thus potentially have little impact on timing). The within-chip analysis presented in this chapter, however, shows a number of clear dependencies on layout practices. Indeed, in many cases the offsets in mean frequency introduced by a particular layout choice are large compared to the within-chip or chip-to-chip variation.

Chapter 5

BEOL Test Structures Testing and Analysis

The goal in the testing and analysis of the interconnect or back end of line (BEOL) structures is to understand changes in frequency due to process induced variation in the interconnect structures used for the capacitive load. This analysis is important for modern circuit design, in which the interconnect variations are no longer negligible; although interconnect variations tend to have a smaller impact than the device variations on circuit performance, the relative impact of interconnect variation in future technologies is expected to increase.

This chapter studies the variation across different metal layers in the interconnect on resulting RO frequency. Three types of structures are considered, each of which is dominated by a different component of capacitance: coupling capacitance load, fringing capacitance load and plane capacitance load structures. Each of these loads is tested in metals 1, 2 and 3. This chapter also studies how the orientation of the wires affect the interconnect performance. In addition, we would ideally like to use the combination of the multiple interconnect test structures to decouple or separate out mean and variance information about different geometric elements of the interconnect structure. In Section 5.4 we discuss the difficulty encountered in doing this, and suggest possible future approaches. Finally, in Section 5.5 we summarize the BEOL analysis.

5.1 Functionality

As previously shown in Figure 4-1, all of the interconnect ring oscillator structures were found to successfully operate across the range of power supply voltages from 1.0 to 2.5 V. In the following analyses, we focus on the RO frequency data taken for all 35 chips and all replicates of each interconnect test structure within each chip, at the 2.5 V power supply level.

One important observation should be made about the shifts and variations observed in the interconnect structures, compared to the FEOL structures. In general, the presence of the interconnect load introduces perhaps a 10% shift compared to the unloaded "canonical" BEOL structure. Additional differences between different structures must then be observed within this already reduced 10% measurement range. For example, a 5% offset between one RO and another in terms of actual load capacitance will result in approximately a 0.1 x 0.05 or 0.5% difference in RO frequency. Thus our sensitivity in observing variation in the interconnect structures is about one tenth that of the FEOL structures, which are directly dependent on the device variations in the RO.

5.2 Statistical Analysis Methodology

The analysis of the BEOL structures that follows is similar to that described for the FEOL structures in Section 4.3. In the back end of line structures, however, we are particularly interested in comparisons between similar test structures at different metal layers. For example, we consider in the section below the differences between interconnect load observed in Metal 1 compared to Metal 2. Here again we will focus on mean differences and possible increases in the variance from one metal layer to the next, where we will use the F test to determine if observed increases are significant or not.

5.3 Structure Variation Analyses

The mean and variation for the frequency responses of the BEOL structures are summarized in Table 5-1. As mentioned in the previous section, we note first a relatively compressed dynamic range in the mean frequency observed, ranging from 4.30 MHz for the "unloaded" canonical BEOL RO to 3.92 MHz for the most heavily loaded RO with large plane capacitors. We also see a substantially compressed range in the total, chip-to-chip, and within-chip variations. Specific observations related to the different families of BEOL structures are made in the following subsections.

Description	BEOL RO Types	Mean Frequency [MHz]	Total Variation σ_f [KHz]	Chip-to-chip σ_c [KHz]	Within-chip σ_w [KHz]
Canonical	BEOL Canonical	4.30	58.3	49.3	31.2
Coupling	Coupling, M1	4.03	57.0	48.5	30.0
	Coupling, M2	4.03	51.6	46.8	21.8
	Coupling, M3	4.03	59.2	48.5	34.0
Fringing	Fringing, M1 Over Substrate	4.16	52.6	47.9	21.7
	Fringing, M1 Over Poly Ground	4.11	51.1	47.3	19.3
	Fringing, M2 Over M1 Ground	4.11	53.0	46.4	25.7
	Fringing, M3 Over M2 Ground	4.09	55.9	46.7	30.7
Plane	Plane Capacitance, M1 Over Substrate	4.22	51.7	48.9	17.0
	Plane Capacitance, M1 Over Poly Ground	4.16	62.8	48.7	39.8
	Plane Capacitance, M2 M1 Ground	4.18	72.5	46.5	55.5
	Plane Capacitance, M3 M2 Ground	4.15	50.3	46.8	18.3
Vertical vs. Horizontal	Vertical BEOL	4.26	53.3	48.5	22.1
	Horizontal, BEOL	4.26	50.9	48.4	15.6
ILD	Ild1	4.08	50.6	47.2	18.4
	Ild2	3.85	46.3	44.3	13.5
	Large M1 Plane Capacitance, Square	4.02	49.6	47.2	15.3
	Large M1 Plane Capacitance, Rectangular	4.02	50.8	45.8	22.2
	Large M2 Plane Capacitance, Square	3.92	47.7	45.6	14.0
	Large M2 Plane Capacitance, Rectangular	3.92	47.2	45.2	13.5

Table 5-1: BEOL Structures Frequency Response

5.3.1 Coupling Capacitance Structures

The coupling capacitance dominated RO structures have interconnect loads consisting of snake-comb lines, which maximize the within-layer coupling between a grounded set

of lines and the switching signal lines. The resulting average across all replicates and chips are summarized in Figure 5-1. Qualitatively, we see that all three coupling structures have a similar output frequency for the three metal layers; the significance of the small observed mean differences is examined in more detail below. We also observe, qualitatively, a small difference in the observed variance due to the metal layer used. Structures with loads of metal-2 show the lowest variation, or 51.6 KHz, while metal-1 structures have 57 KHz of variation, and metal 3 structures 59.2 KHz. There is a 14.2% increase in standard deviation (from the metal 3 structure to the metal 2 structure), as shown in Figure 5-1. We will quantify the significance of these observed variance ratios in more detail later in this subsection. We can also make a third observation regarding the coupling structures. As with the FEOL structures, we see that the largest component of the variation is due to the chip-to-chip variance, as summarized in Table 5-2. In this case, however, we see that the chip-to-chip variance is responsible for 82% to 67% of the variance, while the within-chip variance is responsible for 18% to 33%. Thus the within-chip variation appears to be a larger percentage of the total variation than in the FEOL structures.

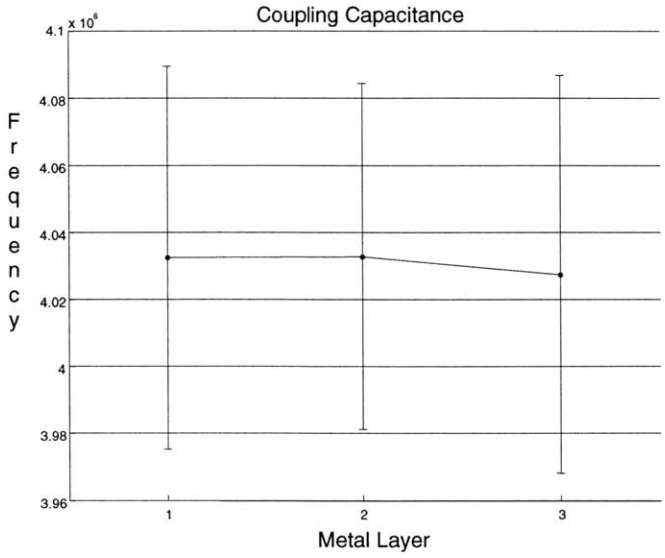

Figure 5-1: Coupling Capacitance Frequency Response

Test Structure	% of Variance	
	Due to Chip-to-chip	Due to Within-chip
Coupling, M1	72.29%	27.71%
Coupling, M2	82.14%	17.86%
Coupling, M3	67.07%	32.93%

Table 5-2: Coupling Structures; Percentages of the individual σ^2 values

We next examine in more quantitative terms the observed mean differences in frequency observed in Figure 5-1. The results of a one-way ANOVA analysis for comparing the means of the coupling structures are shown in Table 5-3. This table was generated by MATLAB and the description of each column follows:

Column 1: Source of the variability. Here "columns" refers to the three different metal structures

Column 2: Sum of Squares (SS) due to each source.

Column 3: Degrees of freedom (df) associated with each source.

Column 4: Mean Squares (MS) for each source, which is the ratio SS/df.

Column 5: F statistic, which is the ratio of the MS's.

Column 6: P-value, which is derived from the cdf of F. As F increases, the p-value decreases.

Source	SS	df	MS	F	Prob>F
Columns	2.14089e+10	2	1.07044e+10	3.41	0.0332
Error	1.18595e+13	3777	3.13993e+09		
Total	1.18809e+13	3779			

Table 5-3: ANOVA Table for Coupling Structures

Table 5-3 shows that even though the mean frequencies look very similar, there is only a 3.3% probability that the observed mean differences between the different structures would occur by chance. That is to say, the small mean differences are quite likely "real" differences detected by the measurement. Figure 5-2 and Figure 5-3 show the normal PDF plots for these structures, in which we can see that the mean and standard deviations (indicated by the 2 sigma lines at the edges of each distribution in the figures) vary due to the metal layer. We are able to detect such small mean differences fairly reliably, because we have a very large number of replicated structures across all chips and metal layers (3,780 total structures in this case). While this mean difference is "real" (that is, the metal 1, metal 2, and metal 3 structures do in fact differ), we can also say from an engineering point of view that these observed differences are quite small, and we find that the different metal layers behave quite similarly in terms of the resulting coupling capacitances.

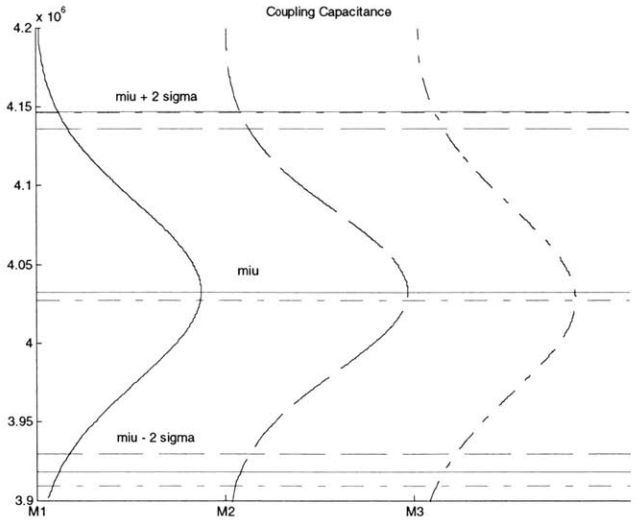

Figure 5-2: PDF Plot for Coupling Structures

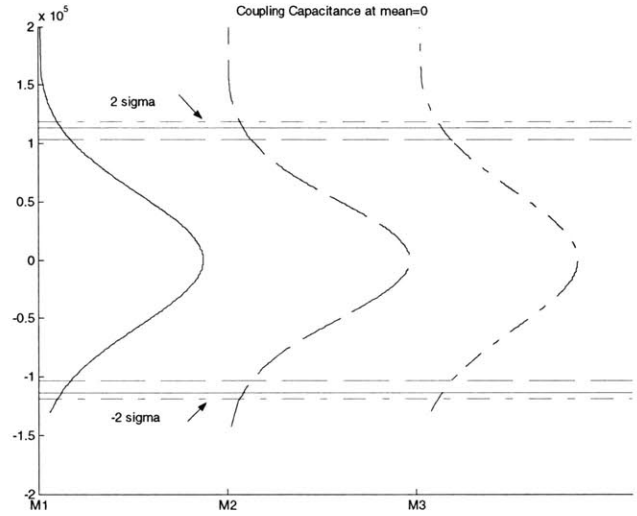

Figure 5-3: PDF Plot for Coupling Structures at Mean = 0

We can also quantify the degree of similarity in the observed variances for the three metal layer coupling capacitance structures. A test of the inverse of the cumulative distribution (cdf) gives a critical ratio for the variances. This is, if the ratio of the variances of the different metal types is larger than this critical ratio, then we have evidence to say that the variances of these structures are different. For the coupling structures, we use $F_{0.95,\ 1259,\ 1259} = 1.1$ to find the critical ratio of 1.1 for the coupling

structures at the 95% confidence level. The variance ratio of coupling structures is 1.32 (comparing the variance of metal 2 structures to metal 3 structures); therefore we can say, with 95% confidence, that the variances for these structures are different. The difference in the structures may be seen in Figure 5-3. Again, the analysis suggests that the metal layers are, in fact, slightly different in both mean and variances from one metal layer to the next.

A remaining question is how much geometric variation these mean shifts might imply, if we transform them back to the original interconnect loads. A sensitivity analysis based on simulation of the original designed test structure is useful here. The coupling structure (with 0.32 μm separation) is compared to another coupling structure whose separation between lines is 6.25% larger (0.34 μm separation). In simulation, the structure with the larger separation has a faster frequency by 2.27%: the 0.32 μm-separation structure has a simulated output frequency of 222.2 MHz, and the 0.34 μm separation structure has an output frequency of 227.7 MHz. Based on the simulated sensitivity, we might estimate that a 1.4% difference in frequency (e.g. the observed spread in frequency) corresponds to ~3.5% difference in geometric spacing between lines in the capacitance test structure.

5.3.2 Fringing Capacitance Structures

The fringing capacitance structures have been designed to maximize or enhance the metal to underlying metal fringing capacitance. This is achieved by using a snake interconnect structure, similar to that in the coupling capacitance case, but now without the nearby ground lines within the same layer. Instead, the underlying layer is grounded.

The fringing structures show a small difference in output frequency and in variation due to the metal layer used, as shown in Figure 5-4. The structure of M1 over substrate is faster than the M1 over poly, as expected because the plane capacitance in the latter is larger (because the separation between M1 and poly is smaller than between M1 and the substrate). Structures with loads on metal-2 show the lowest variation, and the ones with loads of metal-3 show the largest, as in the coupling capacitances structures. The structures with their load over the substrate have a larger variation than their twin structures over polysilicon, possibly because the variations related with the layer to layer capacitances (e.g. ILD thickness) affect them more. There is a total change in standard deviation of 9.4% between fringing structures. Most of the variation is due to the chip–to-chip variance. The chip-to-chip variance is responsible for 70% to 86% of the variance, while the within-chip variance is responsible for 14% to 30%, as shown in Table 5-4. The higher the variation in a structure, the bigger effect the within-chip variation has on it.

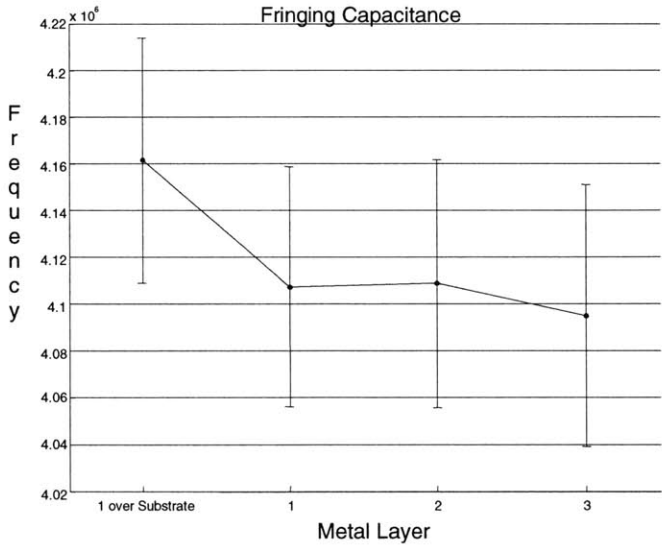

Figure 5-4: Fringing Capacitance Frequency Response

Test Structure	% of Variance	
	Due to Chip-to-chip	Due to Chip-to-chip
Fringing, M1 Over Substrate	82.95%	17.05%
Fringing, M1 Over Poly Ground	85.71%	14.29%
Fringing, M2 Over M1 Ground	76.49%	23.51%
Fringing, M3 Over M2 Ground	69.83%	30.17%

Table 5-4: Fringing Structures; Percentages of the individual σ^2 values

The results of the one-way ANOVA analysis for fringing structures, as explained in the *Coupling* section, are shown in Table 5-5.

Source	SS	df	MS	F	Prob>F
Columns	1.43403e+11	2	7.17016e+10	25.15	1.40915e-11
Error	1.07674e+13	3777	2.85079e+09		
Total	1.09108e+13	3779			

Table 5-5: ANOVA Table for Fringing Structures

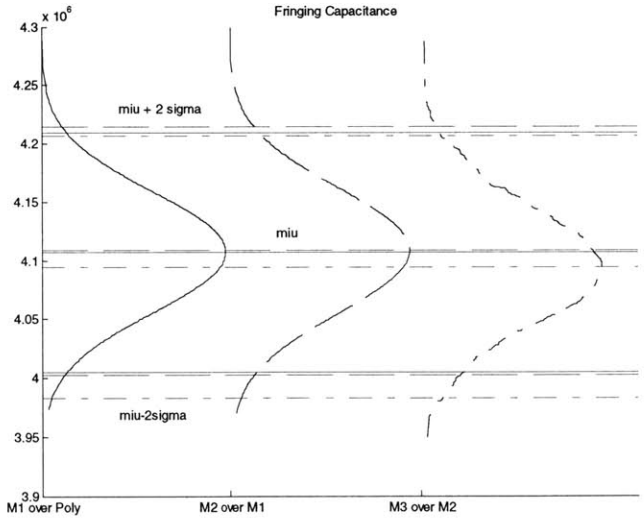

Figure 5-5: PDF Plot for Fringing Structures

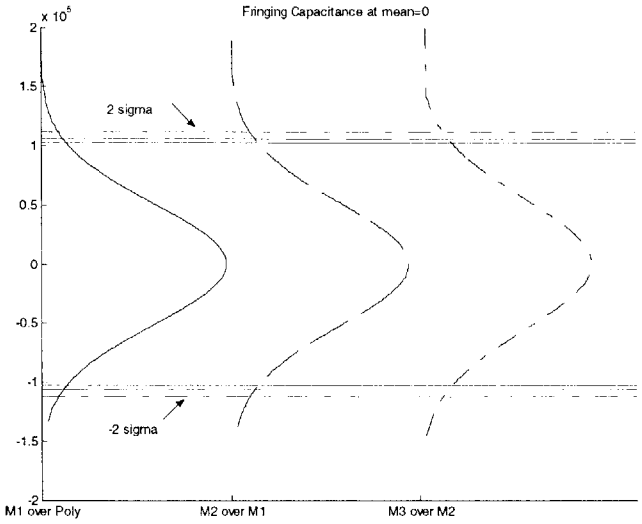

Figure 5-6: PDF Plot for Fringing Structures at Mean = 0

Applying the same test of the inverse of the cumulative distribution performed in the coupling structures, the critical ratio for these structures is 1.1 for 95% confidence that the variances are different. The variance ratio for the fringing structures is 1.19; therefore we can say, with 95% confidence, that the variances for these structures are different, as with the coupling structures. The difference in the standard deviation of structures may be seen in Figure 5-6. Again, this increase in variance is significant, although from an engineering point of view the increase is relatively small.

5.3.3 Plane Capacitance Structures

The plane capacitance test structures are designed to highlight the layer-to-layer capacitance impact on RO frequency. The plane structures also show a small difference in output frequency and in variation due to the metal layer used, as shown in Figure 5-7. The structure of M1 over substrate is faster than the M1 over poly, as expected because the plane capacitance in the latter is larger, as already mentioned. Now the structures with loads of metal-3 have the lowest variation and the ones with loads of metal-2 have the largest, opposing the pattern found in the snake-like structures. Here the difference in

variation is much larger, going from 50.3 KHz to 72.5 KHz, or about 44% difference in variation.

An important observation is that in this case, the variation is not mostly due to chip-to-chip variance, but rather has strong components from both chip-to-chip and within-chip variation. For the metal-2 structures (the ones with the highest overall variation), the within-chip variance is actually higher than the chip-to-chip. These results suggest a very strong effect from the layout environment within the chip on the layer-to-layer dielectric thickness. This effect is most likely due to ILD thickness variations arising from the CMP pattern density dependence. Pattern-dependent effect in CMP is thoroughly studied by Stine **Error! Reference source not found.**. Other relationships are shown in Table 5-6.

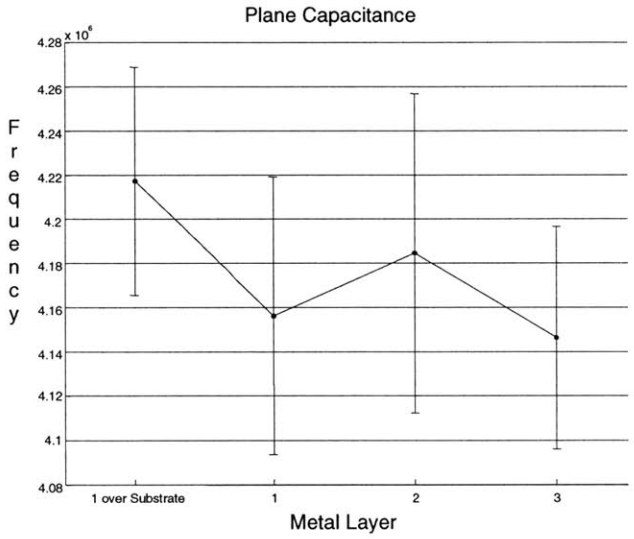

Figure 5-7: Plane Capacitance Frequency Response

Test Structure	% of Variance	
	Due to Chip-to-chip	Due to Chip-to-chip
Plane Capacitance, M1 Over Substrate	89.16%	10.84%
Plane Capacitance, M1 Over Poly Ground	59.95%	40.05%
Plane Capacitance, M2 M1 Ground	41.27%	58.73%
Plane Capacitance, M3 M2 Ground	86.78%	13.22%

Table 5-6: Plane Structures; Percentages of the individual σ^2 values

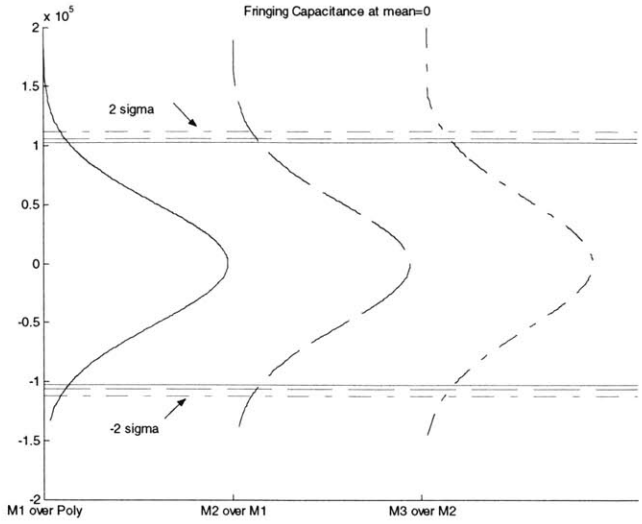

Figure 5-6: PDF Plot for Fringing Structures at Mean = 0

Applying the same test of the inverse of the cumulative distribution performed in the coupling structures, the critical ratio for these structures is 1.1 for 95% confidence that the variances are different. The variance ratio for the fringing structures is 1.19; therefore we can say, with 95% confidence, that the variances for these structures are different, as with the coupling structures. The difference in the standard deviation of structures may be seen in Figure 5-6. Again, this increase in variance is significant, although from an engineering point of view the increase is relatively small.

5.3.3 Plane Capacitance Structures

The plane capacitance test structures are designed to highlight the layer-to-layer capacitance impact on RO frequency. The plane structures also show a small difference in output frequency and in variation due to the metal layer used, as shown in Figure 5-7. The structure of M1 over substrate is faster than the M1 over poly, as expected because the plane capacitance in the latter is larger, as already mentioned. Now the structures with loads of metal-3 have the lowest variation and the ones with loads of metal-2 have the largest, opposing the pattern found in the snake-like structures. Here the difference in

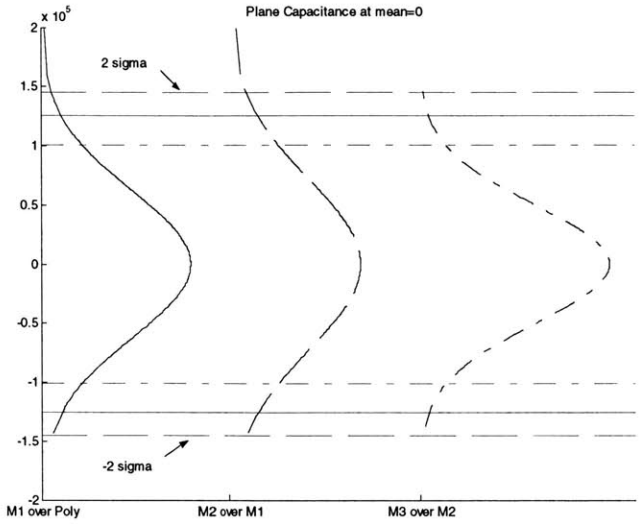

Figure 5-9: PDF Plot for Plane Structures at Mean = 0

Applying the same test of the inverse of the cumulative distribution performed in the coupling and fringing structures, the critical ratio for these structures is $F_{0.95,\ 630,\ 630} = 1.14$ for 95% confidence that the variances are different. The variances ratio for the plane structures is 2.08; therefore we can say, with 95% confidence, that the variances for these structures are different. The difference in the standard deviation of structures may be seen in Figure 5-9.

5.3.4 Vertical vs. Horizontal BEOL Structures

The Vertical and Horizontal BEOL structures have about the same output frequency as expected, since both structures were designed with loads of equivalent dimensions. Variations in these structures show how the routing compares horizontally and vertically. In contrast to the FEOL vertical and horizontal structures, the underlying RO structure has been intentionally designed to be insensitive to individual transistor variations (the goal is to identify interconnect load differences). Thus, we would expect the vertical and horizontal BEOL test structures to differ much less than did the FEOL vertical and horizontal structures. Furthermore, any differences detected imply different things about

the variation: they indicate a directionality dependence in the geometric formation of the interconnect layers rather than a device variation.

In examining the data, we see that the structures prone to vertical variations in width have a slightly larger variation than structures prone to horizontal variations in width. The variation of the vertical structure is 4.7% higher than the horizontal. Variation for both structures is mainly due to chip-to-chip variation, as shown in Table 5-8.

Test Structure	% of Variance	
	Due to Chip-to-chip	Due to Within-chip
Vertical BEOL	82.85%	17.15%
Horizontal, BEOL	90.55%	9.43%

Table 5-8: Horizontal and Vertical Structures; Percentages of the individual σ^2 values

The critical ratio for these structures for 95% confidence that the variances are different is $F_{0.95,\ 630,\ 630} = 1.14$. The variance ratio for the vertical vs. horizontal structures is 1.097; therefore we cannot say, with 95% confidence, that the variances for these structures are different. As expected, then, the BEOL structures do not appear to have a significant variance dependence on orientation.

5.4 Future Work: Separation of Interconnect Capacitance Components

A goal of the designed BEOL structures is to support the separation of the various components of the capacitance based on the set of RO frequencies for the multiple test structures, and so determine variation sources such as ILD thickness variation. In this section, we discuss a method for accomplishing this, proposed by Nassif [8]. We then note a limitation in the current set of test structures that prevent use of this approach, so that future work might extend the BEOL structures in order to better support capacitance extraction.

In a ring oscillator the delay of each inverter can be approximated with a delay *RC*. We would like to account for (and cancel) this RC stage delay in a capacitively loaded RO test structure, so that we can focus on the capacitance introduced just by the interconnect load introduced into the test structure. If we first consider an unloaded *N* stage ring oscillator, the frequency is $f \sim \frac{1}{NRC}$, as shown in Figure 5-10.

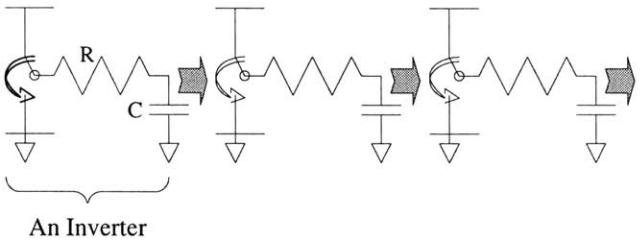

Figure 5-10: RC Equivalent of Inverter Chain

Ring oscillators loaded with an extra "dummy inverter" and its respective RC network are shown in Figure 5-11 and Figure 5-12.

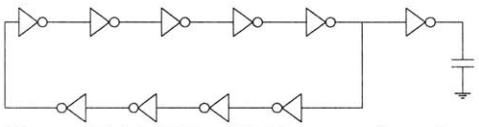

Figure 5-11: RO with Dummy Inverter

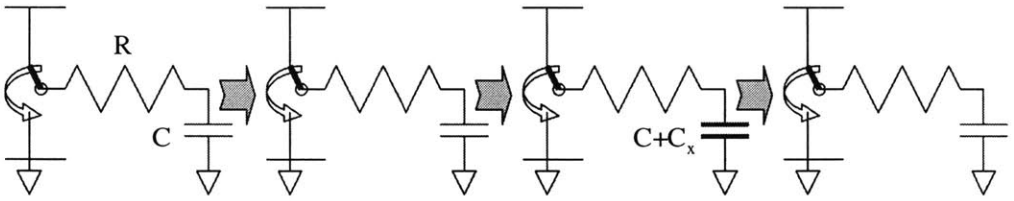

Figure 5-12: RC Equivalent of Inverter Chain with Dummy Inverter

Oscillators with extra dummy inverters along with oscillators with plane capacitance loads will produce enough equations to extract the *C* value out of the frequency.

– Oscillators with no dummy inverters (canonical): $f_{canonical-ILD}^{-1} = NRC = T_0$

– 1 dummy inverter on 1 node (ILD1): $f_{ILD}^{-1} = (N-1)RC + R*2C = (N+1)RC = T_1$

Ring oscillators with different loads provide sufficient information to extract the capacitance value out of the frequency. Plane capacitance structures can be modified to

have different capacitive loads by changing their *width x length* ratio. A structure loaded with a plane capacitance, produces

$$f^{-1} = (N-1)RC + R(C + Cx) = NRC + RCx.$$

where Cx is the capacitance value for a specific type of plane capacitance structure. Now we have the following structures:

- RO-La: Ring oscillator with nominal plane capacitance (area of load equals to $A1$).
- RO-Lb: Ring oscillator with plane capacitance of area $A2 = A1$ times X
- RO-Lc: Ring oscillator with plane capacitance of area $A3 = A1$ times Y, where X and Y are constants.

The inverse output frequency of RO-La, RO-Lb, RO-Lc are the following:

$$f_{RO\_La}^{-1} = (N-1)RC + R(C + C_a) = NRC + RC_a = T_a$$
$$f_{RO\_Lb}^{-1} = (N-1)RC + R(C + C_b) = NRC + RC_b = T_b$$
$$f_{RO\_Lc}^{-1} = (N-1)RC + R(C + C_c) = NRC + RC_c = T_c$$

We can then determine the delta ratios of the plane capacitance structures and the dummy inverter structure:

$$\Delta a = \frac{T_a - T_0}{T_1 - T_0} = \frac{RC_a}{RC} = \frac{C_a}{C}$$
$$\Delta b = \frac{T_b - T_0}{T_1 - T_0} = \frac{RC_b}{RC} = \frac{C_b}{C}$$
$$\Delta c = \frac{T_c - T_0}{T_1 - T_0} = \frac{RC_c}{RC} = \frac{C_c}{C}$$

The ratio of the deltas is easily expressed as *Ca/Cb, Cb/Cc,* etc. These ratios give the two equations we need for T and H from Sakurai [7]:

$$\frac{Ca}{Cb} = \frac{f(Wa,T,H)}{f(Wb,T,H)}$$

The *ILD* structures included in the MOSIS 0.25μm run were intended to do this, but there is a lack of a "canonical-ILD" cell, because all structures in the V-2 run have a buffer that works as a load to access the output line. There is no T_0 structure in the 0.25 μm run. This structure is necessary because it is not certain that the way we estimate frequency as a function of capacitance is correct. We are saying that $T = N\,RC$ and $f = 1/T$ but it is possible that $T = N(a*C + b)$, where a and b are constants. The additional a and b constants would need to be propagated throughout the rest of the equations and eventually found. This requires an extra couple of equations, and a lack of a canonical-ILD structure (with no buffer) is necessary. Future research should explore how to solve this problem.

5.5 Summary

All BEOL structures worked as expected. The metal-1 structures placed over substrate oscillate faster than those placed over a polysilicon ground. Coupling structures have a 14.2% change in standard deviation, the metal-2 loads being the one with the lowest variation and metal-3 loads the ones with the highest. ANOVA analysis gives a 96.7% probability that the means of the different structures are different, and there is 95% confidence the variances for these structures are different. Fringing structures have a 9.4% change in variation, the metal-2 loads being the one with the lowest variation and metal-3 loads the ones with the highest. ANOVA analysis gives an approximately 100% probability that the means of the different structures are different, and there is 95% confidence the variances for these structures are different. Plane structures have a 44% change in variation, the metal-3 loads being the one with the lowest variation and metal-2

loads the ones with the highest. ANOVA analysis gives an approximately 100% probability that the means of the different structures are different, and there is 95% confidence the variances for these structures are different. Vertical vs. horizontal interconnect analysis show that the variation of the vertical structure is 4.7% higher than the horizontal, but this ratio is too small for 95% confidence of having difference in the variation. Variation for all BEOL structures are mainly due to chip-to-chip variation, except for some plane capacitance structures which appear to be highly sensitive to within-chip pattern density. An idea for future studies of interconnect variation would be to include families of test structures with slight differences in layout practice for the same type of structure; this would allow additional exploration of pattern dependent impact on interconnect performance. The next chapter studies these chip to chip and within chip variations as a function of spatial location.

Chapter 6

Spatial Analysis

The chips from the 0.25 μm run are labeled with their spatial location within the whole wafer fabricated by MOSIS. This, along with the within-chip location from the layout, provides data to perform chip-to-chip and within-chip spatial analysis. This chapter focuses on analyzing the variations due to spatial location at the wafer and die level. First, the wafer level trends based on patterns in the chip-to-chip variation are examined in Section 6.1. Next, in Section 6.2 within-chip trends are considered for a number of different test structures. In all these sections, the particular approach used to perform the spatial analysis is also described. Finally, Section 6.3 summarizes the results of the spatial analyses conducted to date.

6.1 Chip-to-chip Spatial Analysis

The goal of the chip-to-chip spatial analysis is to explore whether or not there is a systematic wafer trend in the observed RO frequencies. We will use spatial plots of frequency in order to seek out such trends, in two different ways. First, we consider a plot of the total RO average for each chip, where each chip location on the spatial map is represented by the average of all 2,352 RO frequencies across all different test structures for that particular chip. Second, we also consider plots of frequency across the wafer for individual types of test structures. In this case, an average is still formed for each of the

chip locations plotted, but now this is only averaged across the multiple replicates (from 252 to 36 replicates, depending on the structure type) within that chip.

6.1.1 Chip Mean (All Structures) Spatial Trend

Figure 6-1 shows the overall mean frequencies (averaged across all test structures in each chip) for the 35 bonded chips fabricated by MOSIS. Figure 6-2 illustrates the location of these chips in the wafer in a simplified way, and also labels the chips by an arbitrary chip number. In reality, the designed test chips do not take all the indicated area represented in the maps (since they are fabricated as part of a "multiproject run" in which multiple subdie are combined into a single chip which is then stepped across the wafer), but they are located within that area. All 35 of the chips returned by MOSIS are located in the upper half of the wafer, so that we only gain a partial wafer level trend.

While the spatial distribution of the chips on the wafer is not sufficient to conclude how the wafer variation behaves across the entire wafer, we do observe a clear pattern in the areas covered by our 35 chips. The spatial pattern in Figure 6-1 shows the chip average frequency increasing diagonally from the top right corner to the bottom left corner.

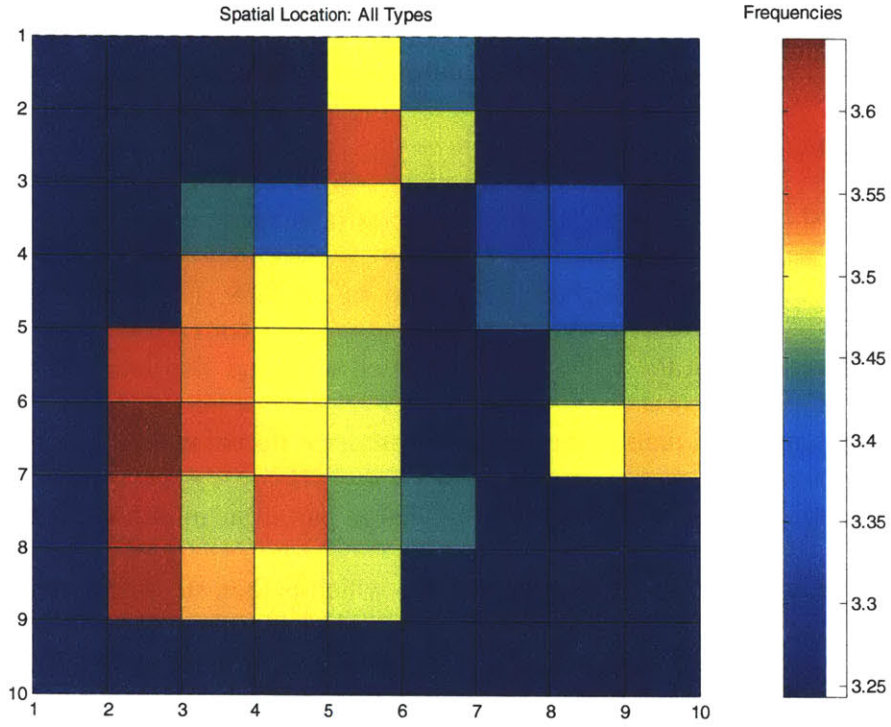

Figure 6-1: Chip Mean Frequencies by Spatial Location

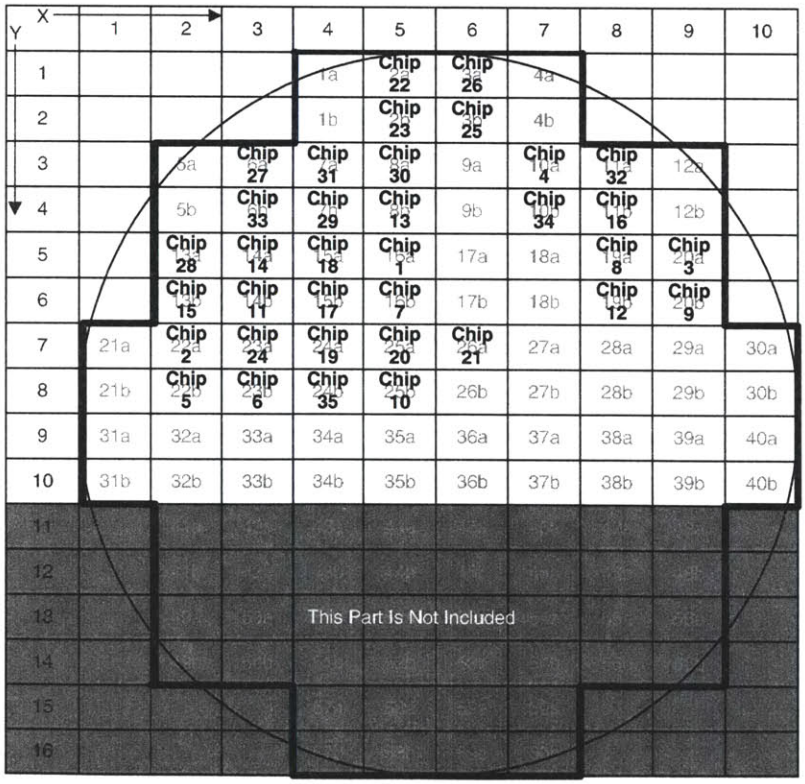

Figure 6-2: Spatial Location in Wafer

The observed differences in frequency span a 9% difference in the means, as shown in Figure 6-3 where the same data as in Figure 6-2 is plotted as a function of chip number rather than by spatial location. The slowest chip, chip 4, has an oscillator frequency of 3.34 MHz and is located in the top right side of the wafer. The fastest, chip 15, has an oscillator frequency of 3.64 MHz and is located in the bottom left corner of our sample.

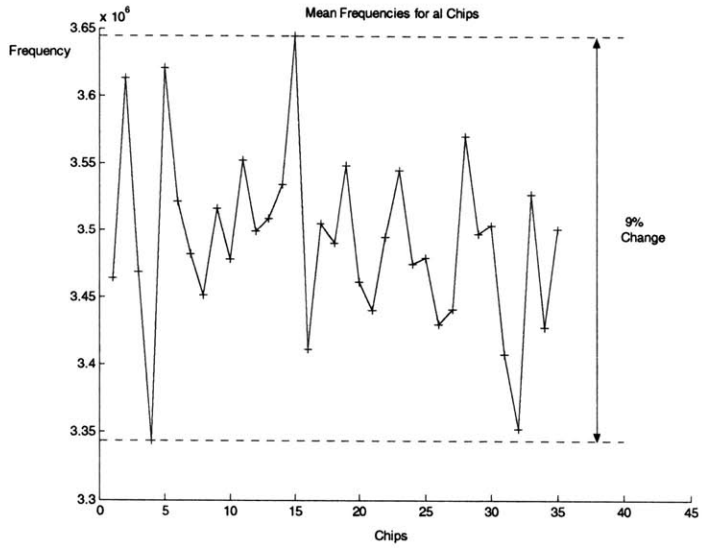

Figure 6-3: Chip Mean Frequencies by Chip Number

6.1.2 Chip Mean (Canonical BEOL Structure) Spatial Trend

While the previous subsection showed the spatial trend averaged across all structures for each chip, this subsection considers the spatial trend for an individual type of test structure. Figure 6-4 shows the mean frequencies of the canonical BEOL structures for all 35 bonded chips. In this case, there are 252 replicates of the canonical BEOL structure within each chip used to form each chip average. Figure 6-2 illustrates the location of these chips in the wafer. The pattern in Figure 6-4 again shows the frequency diagonally increasing from the top right corner to the bottom left corner, with a pattern that is very similar to that seen in Figure 6-1.

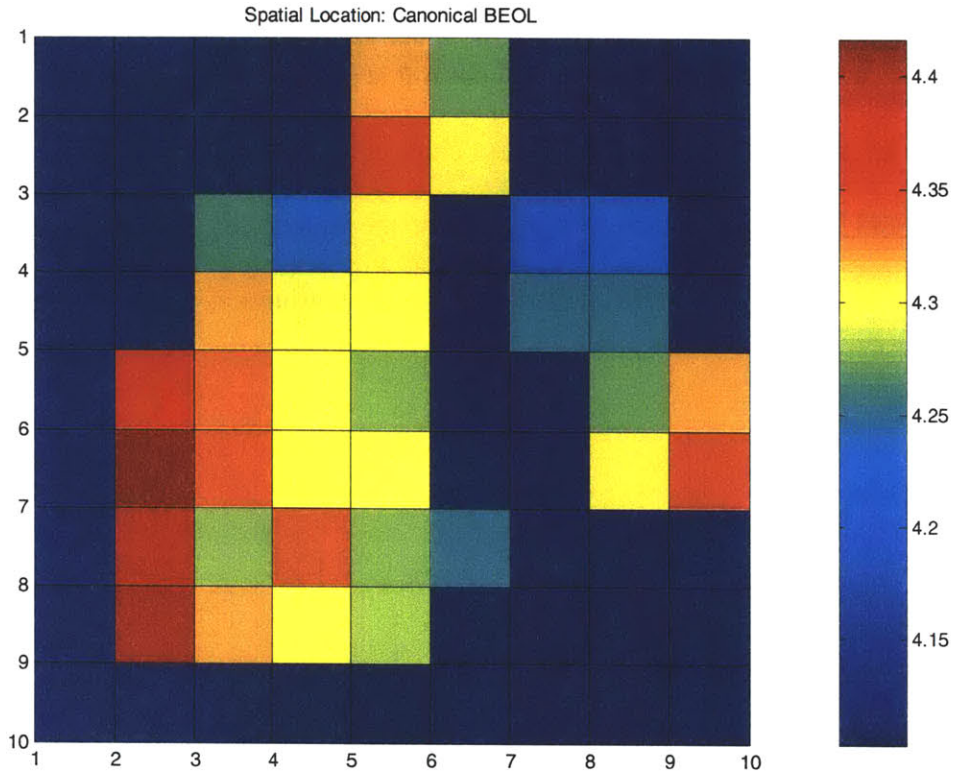

Figure 6-4: Mean Frequencies of Canonical BEOL by Spatial Location

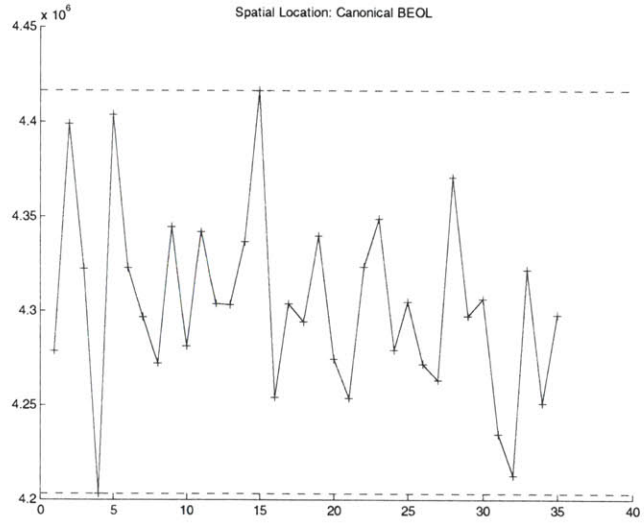

Figure 6-5: Canonical BEOL - Mean Frequencies By Chip

In this case, there is a 5% difference in the means, as shown in Figure 6-5. The slowest chip, chip 4, has an oscillator frequency of 4.20 MHz and is located in the top

right side of the wafer. The fastest, chip 15, has an oscillator frequency of 4.42 MHz and is located in the bottom left corner of our sample. These chips are also the slowest and fastest chips respectively of the all-types analysis shown in Section 6.1.1.

6.1.3 Chip Mean (Canonical FEOL Structure) Spatial Trend

Next we consider one additional test structure type, and again plot the spatial trend for the chip average computed just using the replicates of that particular test structure type. In this case, we examine the canonical FEOL structure. Recall that the BEOL structure was designed to be less sensitive to transistor variations and more sensitive to interconnect effects, while the FEOL canonical structure is expected to be more device variation sensitive. Figure 6-6 shows the mean frequencies of the canonical FEOL structures for all bonded chips. The pattern in Figure 6-6 again shows frequency diagonally increasing from the top right corner to the bottom left corner, with the same pattern of Figure 6-1. This possibly indicates that the same wafer scale variation effects are influencing both the BEOL and FEOL canonical structures, or that there is no "stronger" wafer level trend in the interconnect to overcome the underlying BEOL device variation.

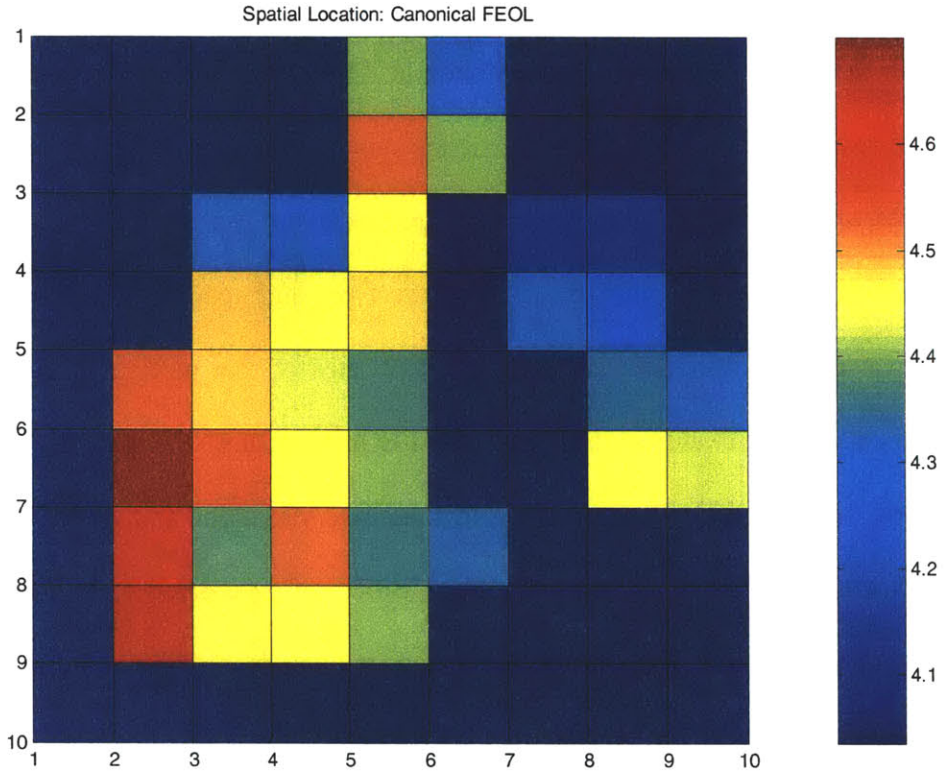

Figure 6-6: Mean Frequencies of Canonical FEOL by Spatial Location

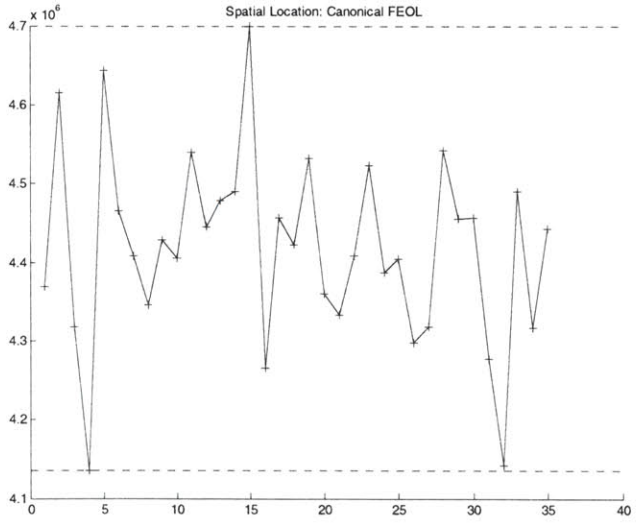

Figure 6-7: Canonical FEOL - Mean Frequencies Per Chip

We do, however, note that there is a 13.7% difference in the means in the FEOL canonical structures (as compared to the 5% range in frequencies for the BEOL

structure), as shown in Figure 6-7. The slowest chip, chip 4, has an oscillator frequency of 4.13 MHz and is located in the top right side of the wafer. The fastest, chip 15, has an oscillator frequency of 4.70 MHz and is located in the bottom left corner of our sample. These results indicate that the prevalent wafer level spatial trend appears to be device oriented. Similar trends are seen for the BEOL and FEOL canonical structures as for the total chip average frequencies, although the scaling of these variation trends differs depending on the sensitivity of the designed RO to variation. Further investigation of the wafer level trends for all the different types of RO chips might reveal that some particular structures have a different chip-to-chip spatial trend (e.g. the plane capacitance BEOL structures), which might provide information about wafer level variations other than channel length effects.

6.2 Within-chip Spatial Analysis

In this section, we focus our attention more narrowly on the analysis of systematic spatial dependencies or trends within the chip. First, we discuss the procedure used to identify "similar" chips for a given structure type, and the use of these chips to estimate the consistent or system spatial trend which acts as a "signature" spatial pattern for that test structure. This procedure is then applied to consider the within-chip trend for a selected subset of the FEOL and BEOL test structure types.

6.2.1 Spatial Analysis Procedure

The goal in the within-chip analysis is to produce a "map" of any systematic trends in the RO frequency values for a given test structure. An important concern in this analysis is the possibility that one or more "outlier" chips can substantially skew the analysis of what is common between the majority of the chips. We thus use a screening procedure to

identify and eliminate potential or likely "outlier" chips, when considering any given test structure type. This screening procedure examines the variances of a given test structure within different chips, to detect those chips with unusually large spreads in variance. Additional methods, including comparison of the (largely deterministic as opposed to random) distribution shapes can also be used.

In order to produce the within-chip spatial trend for a given structure type, the average RO frequency for a particular structure location within the chip is computed across all 35 chips (or fewer if some chips have been excluded as outliers for this structure type). The assumption is that any systematic spatial pattern will be reinforced through this spatial averaging, while random variations, or spatial dependencies that vary depending on the chip location within the wafer, will cancel or not be reinforced. We then produce a plot of the resulting average RO frequency, based on the position on the chip of the structure. In this case, the position is shown abstractly as the row and column position on the test chip. Note that the bottom of the chip contains the poly density structures, and they are not shown in these within-chip maps.

6.2.2 Within-chip Trend - Canonical BEOL Structure

The canonical BEOL structure is the structure replicated the most in a chip, and therefore is the most interesting one to study for patterns due to within-chip location. Figure 6-8 shows a map of these structures across the chip and their frequency response.

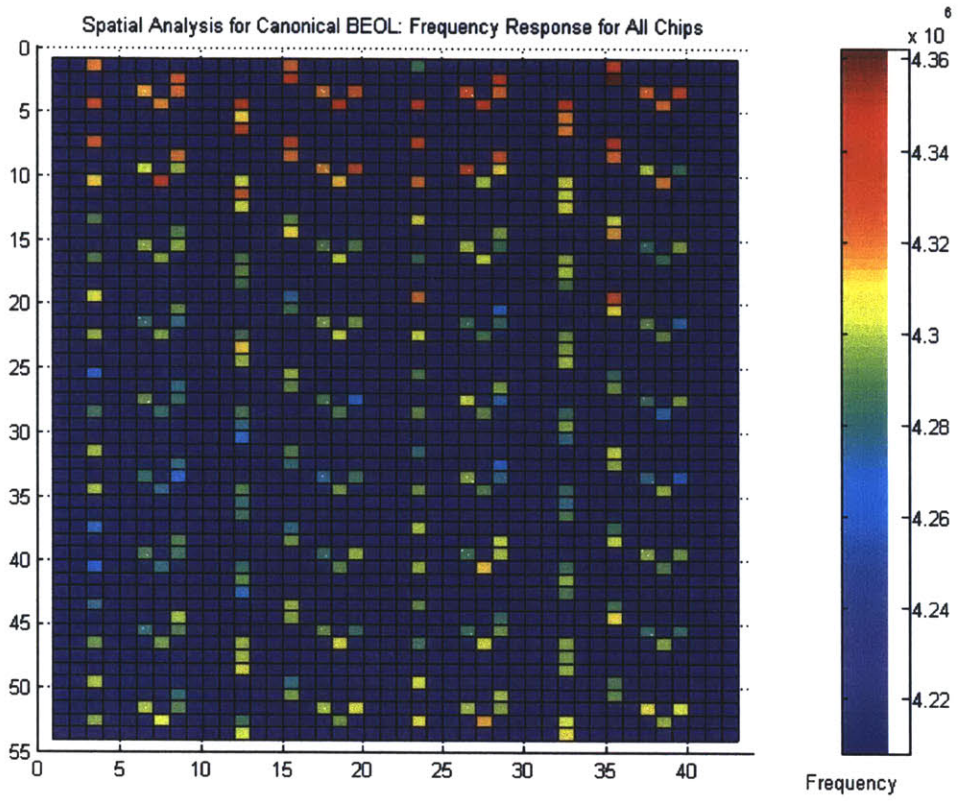

Figure 6-8: Spatial Analysis for Canonical BEOL

The range in frequencies for these structures is from 4.258 MHz to 4.362 MHz, or a 2.4% change. The frequency pattern shows the fastest structure to be at the top.

6.2.3 Within-chip Trend - Canonical FEOL Structure

The 3x spacing between poly lines FEOL structure behaves as shown in Figure 6-9, which shows a map of where the structures are located across the chip and their frequency response.

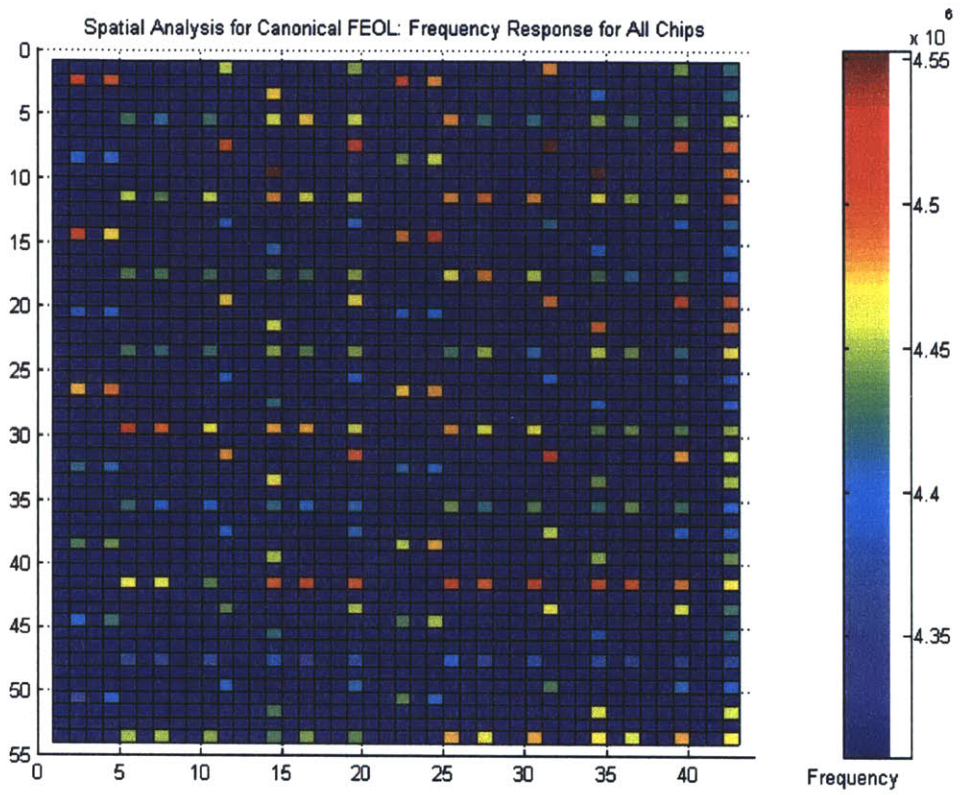

Figure 6-9: Spatial Analysis for Canonical FEOL

The range in frequencies for these structures is from 4.47 MHz to 4.55 MHz, or a 4.4% change. Comparison of this map to that for the canonical BEOL is interesting. While a gentle chip scale trend is seen the BEOL structures, in the case of the FEOL structures the variation appears to be somewhat more localized and does not show a consistent trend across the entire chip. For example, it appears that several structures across a given row behave somewhat similarly, but there are substantial differences in frequency from one row to the next. Further investigation of the different spatial patterns of variation in the BEOL and FEOL test structures might provide insight into particular sources of long-range chip-scale variation.

6.2.4 Within-chip Trend - Single Finger FEOL Structure

The single finger (3x minimum width) FEOL structure, behaves as shown in the within-chip frequency map in Figure 6-10. The range in frequencies for this structure is from 4.19 MHz to 4.30 MHz, or a 2.7% change. The frequency pattern shows the fastest structure to be at the top, similar to the canonical BEOL structures. In this case, the pattern is more systematic or shows a clearer chip-scale trend, compared to the FEOL canonical structures..

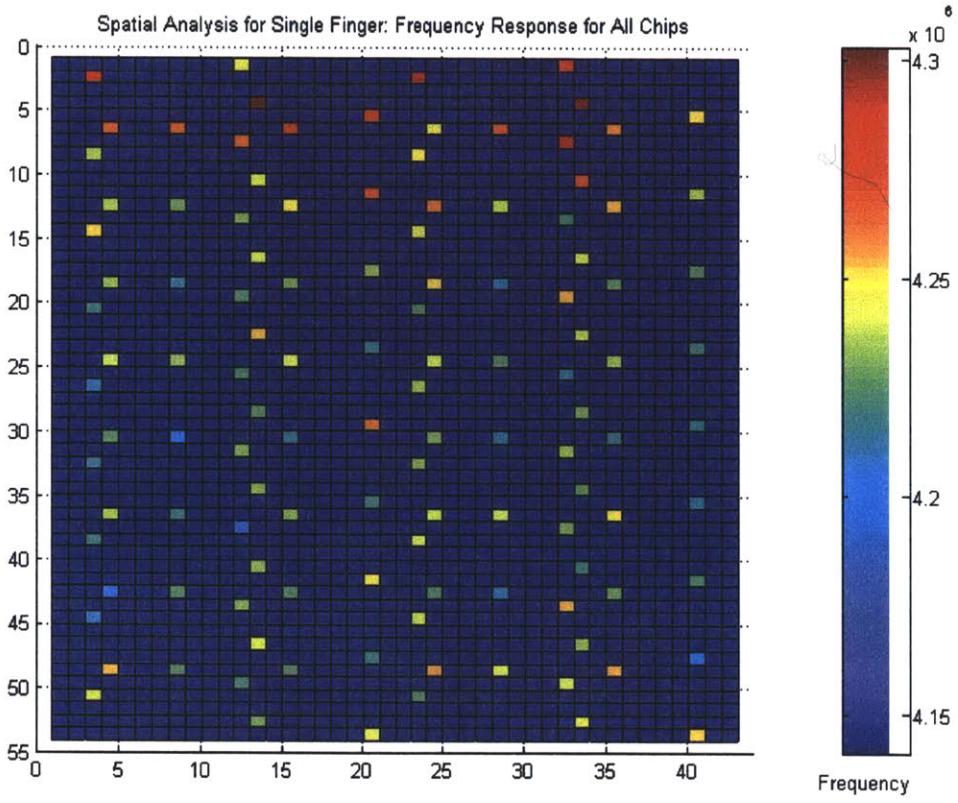

Figure 6-10: Spatial Analysis for Single Finger FEOL

6.2.5 Within-chip Trend - Large Plane M1 BEOL Structure

This chip-scale frequency map for the large, square plane on metal-1 BEOL structure is shown in Figure 6-11. The range in frequencies for these structures is from 3.99 MHz to 4.05 MHz, or a 1.58% change. The fastest structures appear to be near the top of the

chip, although the limited replication of these structures across the chips makes detection of any clear pattern somewhat difficult.

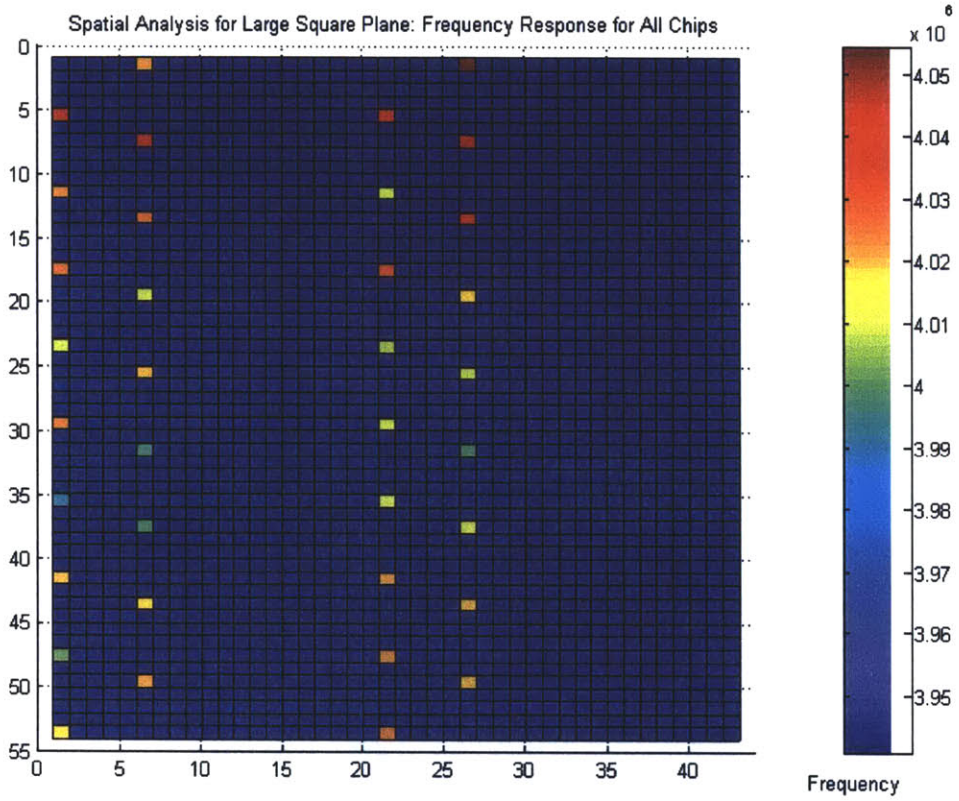

Figure 6-11: Spatial Analysis for Large Plane M1 BEOL

6.3 Summary

The chip-to-chip spatial variation shows a trend of increasing frequency diagonally from the top right corner of the chip to the bottom left of our sample. Within-chip analysis shows a recurring pattern of higher frequency structures in the top. The within-chip analysis pattern is more uniform in the back end of line structures than in the front end of line structures. There is not sufficient data to determine if the chip-to-chip pattern continues in the whole chip or to show how the bottom of the chip behaves for the within-chip analysis.

Chapter 7 Conclusion

This thesis has presented the design, successful fabrication, and analysis of test structures with variations due to layout practice. The analysis at 2.5 V of all structures shows particular trends for particular manufacturing practices.

7.1 Test Structures Analysis

The V-2 test chip fabrication run has proven successful. Different structures are seen to behave differently depending of the layout practice for both device level structures (FEOL) and interconnect level structures (BEOL).

7.1.1 FEOL Analysis

All FEOL structures work as expected except for the "PN-J-ish" structure; the equivalent channel length for this structure is small enough to make it oscillate too fast for the control circuitry at higher voltages.

The density vs. isolation analysis shows that as the number of fingers increases, the variation increases for all types of structures (3x minimum length structures, the 4x minimum length structures and the vertical). This is likely due to ΔL changes. As the number of fingers increases the variation is also seen to increase, as projected.

The polysilicon effect analysis shows that both local and global density of polysilicon affect circuits performance. They both follow a similar trend of decreasing frequency as the polysilicon proximity or density around the ring oscillators increases. The proximity, or local effect has a more drastic impact than the global or polysilicon density effect.

Both groups of structures have small variation, but the local effect structures variation is large enough to be considered real.

All vertical structures have a larger standard deviation and lower frequency than their corresponding horizontal structures. Conjectured physical reasons for this are (a) raster scan orientation effects during mask making, or (b) ion implantation scanning orientation dependence. This project shows that the difference in orientation produces a consistent offset behavior, and that the designer should take the orientation of the circuit seriously to achieve good matching.

Chip-to-chip variation has proven to be larger than the within-chip variation for almost every structure, in both the device and interconnect structures.

7.1.2 BEOL Analysis

All BEOL structures work as expected. The results show that for thin line interconnections, such as the snake, the metal layer used may produce different load, which may affect the circuit's performance. Coupling capacitances, such as the snake with a ground line nearby, have an even larger difference due to the metal layer used for the interconnection. These differences might be due to other reasons besides the metal geometry, such as ILD thickness variation, but it is most likely due to the combination of both.

Plane capacitance structures have a larger variation change. This may be partly because the resistance is decreased and the change is mainly due to the capacitance, which is less controlled than the resistance. The changes between these structures may reflect even more strongly the changes in ILD thickness across the chip. To quantify changes in ILD thickness has proven difficult and so is not included in this thesis; future

work is needed to help separate out the ILD thickness given the multiple interconnect structure frequency measurements.

Vertical vs. horizontal interconnect analysis shows that the variation of the vertical structure is slightly higher than the horizontal, but the difference is too small for drawing conclusions. An area for possible future work is to also characterize the variation dependence in new non-Manhattan wiring techniques having 45-degree routings.

Chip-to-chip variation has proven to be larger than the within-chip variation for almost every structure, in both the device and interconnect structures.

7.1.3 Spatial Analysis

Spatial analysis shows consistent patterns of variation. The chip-to-chip spatial variation shows a trend of increasing frequency diagonally from the top right corner of the chip to the bottom left of the sample across the wafer. Our chips only cover the upper half of the wafer, and it is not possible with these 35 chips to explore whether or not the patterns continue throughout the entire wafer.

Within-chip analysis also shows a consistent pattern of higher frequency structures in the top of the chip. Because the within-chip analysis pattern is more uniform in the back end of line structures than in the front end of line structures, it supports the design expectation that back end of line structures are less sensitive to frequency dependencies on the most local surrounding structures. The bottom of the chip has not been submitted to spatial analysis, because the structures in the bottom are not replicated throughout the rest of the chip.

7.2 Future work

There is a wide range of future research that this thesis may lead to. Additional variation analysis is needed to make specific connections between circuit timing variation and layout practice induced variation. The study of separating interconnect capacitance components as described in Section 5.4 seems necessary to describe how variations like ILD thickness, metal thickness, and others affect circuit performance. More work needs to be done on identifying if the P-type transistors or N-type transistors are more sensitive to variation. Also, future work should consider the possibility of separating out the parasitics (e.g. overlay capacitance) from the channel length effects in FEOL structures. Chip to chip spatial analysis shows interesting trends that should be studied with a larger sample of chips that covers the entire wafer. Within chip analysis may also be expanded by exploring the behavior at all edges of a die to find out if the pattern found in this thesis applies to them.

7.3 Summary of Contributions

This thesis has focused on the analysis of carefully designed test structures which isolate specific variations to study their impact thoroughly. The different test structures have proven to have significant differences and different methods of analysis have been used to investigate process induced variation and the significance of this variation. All results obtained from previous work in the V-1 run have been proven with a much larger set of data. Several methods have been shown to explore the implications of the ring oscillator frequency measurements as a function of layout and spatial parameters, and many possibilities for future research are available in the topic.

Bibliography

[1] S. Nassif, "Modeling and Analysis of Manufacturing Variations," *IEEE Conference on Custom Integrated Circuits*, pp. 223-228, 2001.

[2] J.-H. Chern, J. Huang, L. Arledge, P.-C. Li, and P. Yang, "Multilevel metal capacitance models for CAD design synthesis systems," *IEEE Electron Device Letters*, vol. 13, no. 1, pp. 32-34, Jan. 1992.

[3] J. Panganiban, "A Ring Oscillator Based Variation Test Chip," MEng. Thesis, MIT EECS, May 2002.

[4] V. Mehrotra, "Modeling the effects of Systematics Process Variation on Circuit Performance," PhD. Thesis, MIT EECS, May 2001.

[5] J. Panganiban, K. Gonzalez-Valentin, D. Boning, and M. Huber, "Documentation of the MOSIS 0.35μm TSMC Variation Test Structures Chip," International SEMATECH, October 2001.

[6] J. Panganiban, K. Gonzalez-Valentin, D. Boning, and M. Huber, "Documentation of the MOSIS 0.25μm TSMC Variation Test Structures Chip," International SEMATECH, May 2002.

[7] T. Sakurai and K. Tamani, "Simple Formulas for Two- and Three-Dimensional Capacitances," *IEEE Transactions on Electron Devices*, vol. ED-30, no. 2, pp. 183-185, February 1983.

[8] S. Nassif, "Capacitance Test Structures Principles," private communication, December 2001.

[9] B. Stine, D. Ouma, R. Divecha, D. Boning and J. Chung, "Rapid Characterization and Modeling of Pattern Dependent Variation in Chemical Mechanical Polishing," *IEEE Transactions Semiconductor Manufacturing*, vol. 11, no. 1, pp. 129-140, February 1998.

Appendix I

Threshold Voltage Analysis

This analysis is contributed by J. Panganiban, in an effort to understand the impact of threshold voltage variation in the test structures of the V-2 run.

Spatial Chip-to-Chip V_t Variation Results and Analysis

The frequencies of the matched single-fingered ROs at a supply voltage of 1.0 V are analyzed, and the results of all 35 tested chips are summarized in the table below. The low-Vdd frequencies within each chip are averaged, resulting in a chip average frequency. This frequency is termed the *chip_mean*. The *total_mean* corresponds to the low-Vdd frequencies of all the matched RO-SFs across all the chips. This *total_mean* is calculated to be approximately 455 KHz. The second column of the table below shows the percentage difference of the *chip_mean* away from the *total_mean* for each chip. These deviations away from the *total_mean* are evidence of threshold voltage variation.

The *nominal_V_t* is defined as the threshold voltage that would correspond to oscillations at the *chip_mean* frequency. The third column of the table below shows the change in chip threshold voltage (*chip_V_t*) away from the *nominal_V_t* that would result in the differences between the *chip_mean* frequency and the *total_mean* frequency. This column gives the actual extent of how much threshold voltage varies from chip-to-chip. The fourth column of the table shows the number of matched single-fingered ROs there are for each chip. Notice that seven out of the 35 chips contained no RO-SFs that match frequencies at the higher supply voltage of 2.5 V. Therefore, these seven chips cannot be used in the analysis, since gate-length variation cannot be completely eliminated for these chips (Recall there are a total of 126 RO-SFs in each chip).

Chip #	% Difference in Chip_Mean Frequency from Total_Mean @ Vdd = 1 V	% Difference in Chip_V_t from Nominal_V_t	Number of Matched RO-SFs
1	-1.72	1.94	10
2	-	-	0
3	3.54	-4.00	9
4	-	-	0
5	-	-	0
6	-0.095	0.107	19
7	-2.26	2.55	6
8	-1.24	1.40	9
9	4.20	-4.74	2
10	-2.04	2.30	9
11	-0.320	0.361	11
12	-0.627	0.707	23
13	-0.981	1.11	23
14	0.892	-1.01	7
15	-	-	0
16	2.78	-3.13	2
17	-0.778	0.877	16
18	-0.696	0.785	22
19	-0.470	0.530	11
20	-2.32	2.61	10
21	-4.69	5.29	2
22	3.13	-3.53	11
23	3.98	-4.48	2
24	-2.06	2.32	12
25	2.34	-2.64	22
26	3.31	-3.73	10
27	1.33	-1.50	5
28	-	-	0
29	-1.05	1.18	26
30	-1.28	1.44	20
31	-	-	0
32	-	-	0
33	1.35	-1.53	14
34	-1.28	1.44	2
35	-2.97	3.35	19

Table AI - 1: Threshold Voltage Analysis Data of Matched RO-SFs

Figure AI – 1 basically maps the third column of the table above spatially across the wafer. A clear trend in threshold voltage can be observed across the wafer. The upper-right corner is where the ROs oscillate the fastest, corresponding to lower V_t values. The V_t values increase as you more down and to the left from the upper-right corner. This analysis shows a definite spatial trend in threshold voltage.

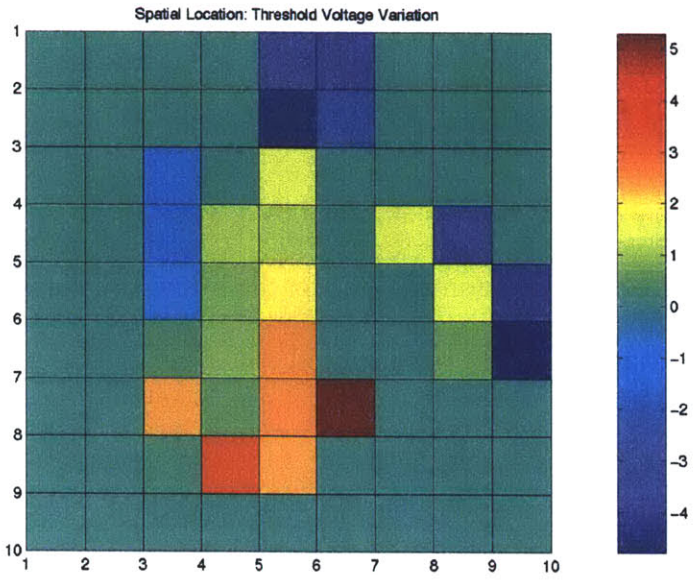

Figure AI - 1: Threshold Voltage Variation Across Wafer

Future V_t Work

This analysis shows how the V-2 test structures can be used to extract threshold voltage variation, which makes the FEOL test structures twice as powerful. However, there is still room for improvement in this analysis. For example, the previous section grouped the NMOS and PMOS threshold voltages together. In actuality, variations between the V_t values of the two transistor types are not necessarily correlated, but may be completely independent of each other. Separating out the PMOS and NMOS V_t variations remains a problem to be solved. Also, this analysis only shows the spatial trends at the wafer-level, since showing any trends within-chip is not feasible because of the limited matched ROs within each chip. Another testing methodology can be investigated to get around this limitation, so that within-chip V_t variation can be extracted.

Appendix II

Parasitics Impact in FEOL Analysis

The following analysis has been contributed by J. Panganiban, in order to study how the parasitics may affect the variation analysis for the FEOL structures. This analysis has also influenced the design of all FEOL structures.

FEOL RO Parasitics

Neglecting any process variation, the FEOL ROs with an effective gate length of three times the minimum length (whether it be single-fingered, double-fingered, or three-fingered) would ideally oscillate at the exact same frequency. Therefore, any slight differences in the observed RO frequencies can be attributed to gate-length variation. However, this assumes that the parasitic components of the ring oscillator are neglected. In reality, however, differently laid out ROs may have different valued parasitic components that may contribute to non-uniform RO frequencies. This section discusses the design methods used to minimize the differences of some of the RO parasitics such as source/drain resistance and output node capacitance. Also explained is the parasitic fringing capacitances of the poly gate fingers, which is the most dominant parasitic of the V-2 FEOL ROs with varied layouts.

Neutralization of Source/Drain Resistance

There will always be a certain degree of parasitics associated with each ring oscillator, and these parasitics do contribute to the oscillator frequency. However, for the RO frequencies to be reliable in detecting variation, the values of these parasitic components must be kept constant from RO to RO. If the parasitics are kept constant, then their contributions to the RO frequencies become identical, keeping the integrity of

the frequency measurements remain intact. This section explains how the values of two different parasitics associated with the RO transistors are held constant from RO to RO.

The source/drain parasitic resistance of a transistor is illustrated in Figure AII - 1. This figure is an example of the three-fingered PMOS transistor (which effectively is three smaller PMOS inverters in series) of the canonical FEOL RO. When the transistor is on, current flows from the drain node that is connected to Vdd of the left-most transistor to the output node through the source/drain diffusion areas of the three series PMOS transistors. The source/drain diffusion areas are not perfect conductors and have a degree of parasitic resistance associated with them. This resistance affects the amount of current that flows through the transistor, and thus has an impact on the RO frequency.

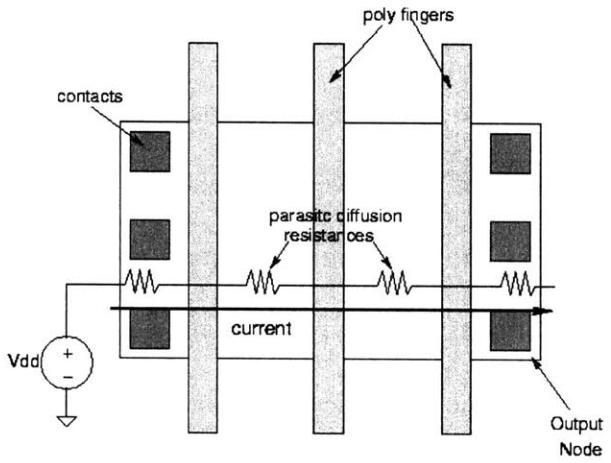

Figure AII - 1: Source/Drain Parasitic Resistances in PMOS

In order to neutralize the undesirable contributions of the parasitic source/drain resistances, the resistance values must be held identical across all FEOL ROs. Since the parasitic resistance is proportional to the combined area of the all the source/drain resistances, this combined area is kept constant for each ring oscillator. This is illustrated with the canonical inverter and the *3x line-spacing* inverter in Figure AII - 2. Although these two transistors have different finger topologies, the total area of the source/drain

diffusion areas is kept constant since the total transistor area dimensions are identical. This ensures identical source/drain parasitic resistances among the different FEOL ROs.

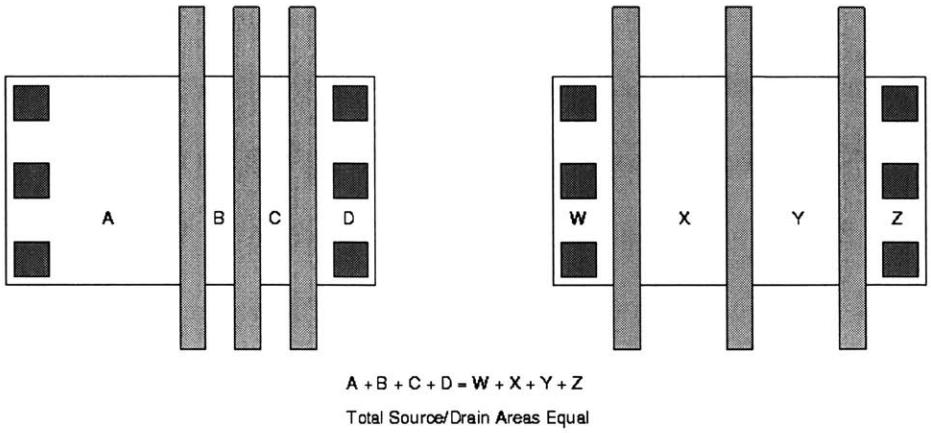

Figure AII - 2: Total Source/Drain Diffusion Areas Constant

Neutralization of Output Node Capacitance

The output node capacitance of each inverter is another critical RO parasitic that should be held constant between the differently laid out ROs. As previously illustrated in Figure AII – 1, the output node of each inverter is where the sources of both the PMOS and NMOS transistors meet. The parasitic capacitance associated with the combined source diffusion areas is critical, since it is the only node that fully charges and discharges in each inverter. If the parasitic capacitance value differs from RO to RO, unwanted fluctuations in RO frequency can result due to this parasitic.

To keep the output node capacitance constant, the source diffusion areas have to be identical. However, because the total source/drain areas are kept constant (as explained in the previous section), it does not guarantee the capacitance associated with the source diffusion area of the output node is constant. The output node capacitance is dependent on the placement of the poly fingers, as illustrated in Figure AII - 3. This figure shows two different placements of the poly fingers of the canonical inverter. The

case on the left has a higher output node diffusion area because the fingers are placed in the center, causing an increased source area and thus a higher output node capacitance. The transistor on the right has a smaller output node capacitance since the fingers are shifted all the way to the left. Therefore, to keep the parasitic capacitances constant, the poly fingers for all the FEOL inverters are shifted to the extreme right side of the diffusion area, similar to the second transistor of Figure AII - 3. This pins the area of the output node diffusion constant for every FEOL transistor.

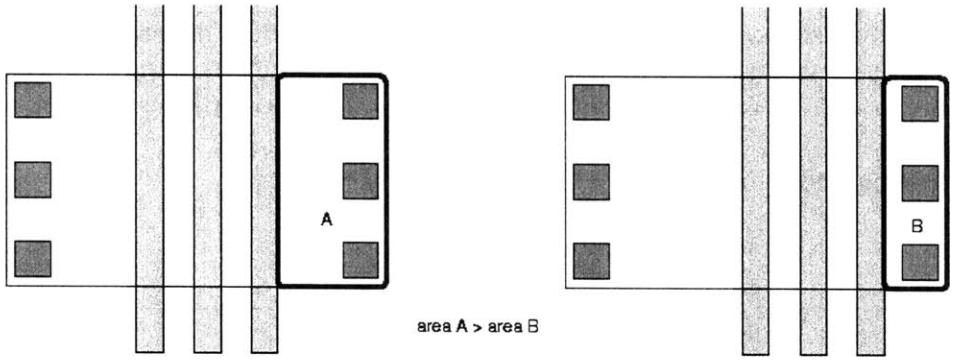

Figure AII - 3: Different Output Node Parasitic Capacitances

Note that the other source/drain diffusion areas other than the output node may vary from RO to RO, such as the drain area connecting to Vdd for a PMOS transistor. However, because this node is always shorted to Vdd (or shorted to Gnd for NMOS transistors), it is always pinned at the same potential, which makes this parasitic capacitance contribute nothing to the RO frequency. However, the intermediate nodes between fingers (for multi-fingered configurations) can also vary their diffusion areas as well, causing different-valued parasitic capacitances in these intermediate nodes. To first order, however, the voltages on these intermediate nodes stay charged at Vdd at all times. When the transistor is on, these nodes are shorted to Vdd (or shorted to Gnd for NMOS transistors). When the transistors turn off (assuming the all poly

fingers activate or deactivate at the same time), the intermediate nodes float, maintaining the previous voltage. Therefore, these nodes do not charge or discharge either, making the frequency contributions of these capacitances negligible.

Poly Gate Fringing Capacitance Effects

The poly gate fringing capacitance causes the greatest degree of mismatched frequencies among all RO parasitics. This parasitic capacitance is associated with the fringing capacitance component between the sidewalls of the poly fingers and the source/drain diffusions. This capacitance varies with the different poly finger configurations, and it is impossible to totally neutralize its effects without keeping constant the finger topologies.

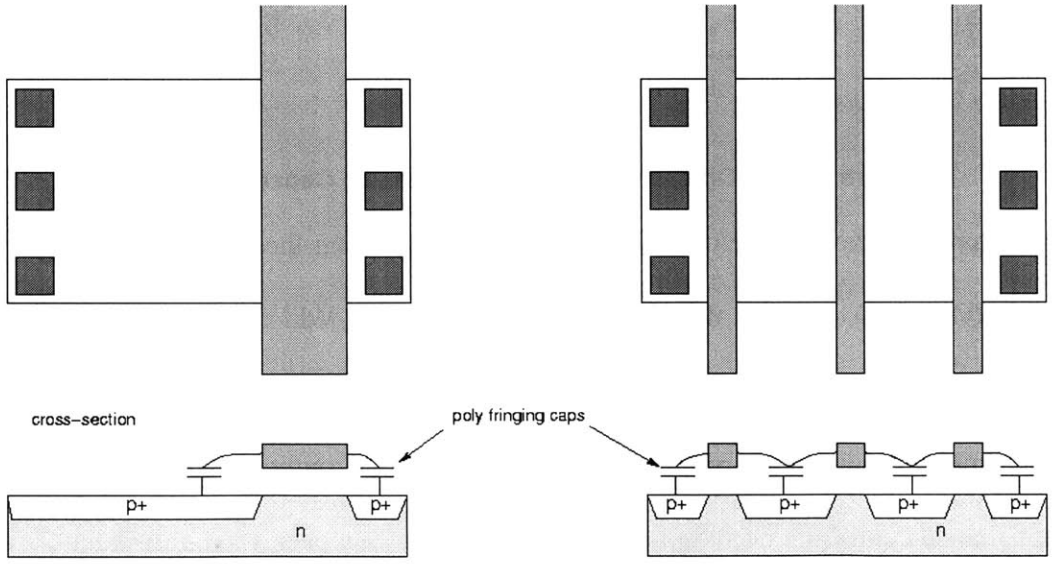

Figure AII-4: Different Poly Fringing Capacitances Due to Different Finger Configurations

Figure AII - 4 shows the different fringing components between the single-fingered RO and the three-fingered RO. Because the three-fingered RO has more fringing components, the total poly gate fringing capacitance is higher than the single-fingered. This can result in a slightly slower frequency than the single-fingered RO, since the three-fingered RO has to charge and discharge more capacitance. Also, a *3x line-spacing*

RO has more fringing capacitances than the *1x line-spacing* (canonical) because the poly fingers see more source/drain diffusion area in the internal nodes. This will also result in slight discrepancies in RO frequencies among the different proximity ROs.