A Low Noise, Low Power DC/DC Converter

for Cell Phone Power Applications

by

Sauparna Das

Submitted to the Department of Electrical Engineering and Computer Science

in Partial Fulfillment of the Requirements for the Degrees of

Bachelor of Science in Electrical Science and Engineering

and Master of Engineering in Electrical Engineering and Computer Science

at the Massachusetts Institute of Technology

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ABSTRACT

The goal is to design a low noise, low power DC/DC converter and controller IC to power an Analog Devices' digital signal processor that will run at 1.2 V from a 3.6 V battery and has a rated maximum current draw of 300mA. A switch-mode DC/DC converter is proposed as a possible way of efficiently stepping down the battery voltage to 1.2 V. The control chip is designed using Taiwan Semiconductor Manufacturing Corporation's 0.25 μm CMOS process. Component selection issues for the power stage and input and output filters are discussed. Dynamic modeling of the DC/DC converter and feedback control design are also presented. A 1.5 MHz, synchronously rectified, current-mode controlled step-down converter was designed and simulated using Analog Devices' spice simulator ADICE.

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1 Introduction

1.1 Power consumption in a cell phone

Modern day cell phones use a digital signal processor (DSP) to process voice and data signals. DSPs are being fabricated using smaller and smaller process geometries in order to increase their transistor density and processing power. The smaller transistors have a lower maximum voltage rating and thus the supply voltage for DSPs continue to decrease. A cell phone also contains a power amplifier to amplify signals for transmission from the cell phone to the base station. The power amplifier typically requires a supply voltage greater than 3 V. In order to save space and reduce weight, a cell phone is typically powered with one 3.6 V lithium ion (LiIon) battery cell or three 1.2 V nickel metal-hydride (NiMH) battery cells. A linear regulator steps the 3.6 V battery voltage down to a lower voltage for the DSP. The efficiency of a linear regulator is approximately equal to its output voltage divide by its input voltage. The current Analog Devices (ADI) DSP runs at a supply voltage of 1.8 volts and uses up to 100 mA of current. In this case the regulator is only 50% efficient. This was satisfactory because the DSP typically draws less than 30 mA and thus the power lost in the regulator (< 54 mW) was acceptable. In addition, linear regulators take up little space on a printed circuit board (PCB) and produce little noise so do not interfere with sensitive RF and mixed-signal circuitry in the cell phone.

As supply voltages continue to decrease the amount of power lost in the regulator becomes unacceptable. The next generation ADI DSP can run at 1.2 V from a 3.6 V battery and has a rated maximum current draw of 300mA. The DSP is designed for data intensive applications (e.g. wireless internet) and will consume large amounts of current for longer periods of time. GSM cell phones transmit and receive voice and data information in 577 μsec blocks of time called slots. 8 slots are put together to create a frame. Standard voice only phones use 3 out of the 8 slots in a frame for transmitting and receiving data. In the future more data intensive

schemes, such as GPRS or EDGE, can use up to 6 out of the 8 slots. The DSP in these cell phones can draw 300 mA of current during each of the 6 slots used and could draw close to 300 mA all the time. Thus the average current consumed during a frame can be more than 225 mA. If a linear regulator was used to power the DSP in this case, the efficiency would be only 33% and more than 560 mW would be lost in the regulator. This is not only a severe drain on the battery, but can also cause overheating of the cell phone.

1.2 Why use a DC/DC converter?

To step down the supply voltage for the DSP efficiently, a high frequency switch-mode DC/DC converter is proposed as a possible solution. The step-down converter, also known as a buck converter, uses a switch and a diode to produce a square wave voltage waveform across a filter network (Figure 1-1). The square wave can be thought of as having a DC component equal to the duty cycle, D, times the input voltage and a high frequency ripple component. The square wave is applied to a low pass LC filter which allows the DC component to pass, but attenuates the voltage ripple to an acceptable level (Figure 1-2). Ideally, the switches, inductor and capacitor do not dissipate any power and the converter is 100% efficient. However, real components dissipate power and thus the attainable efficiencies of DC/DC converters is less, typically around 70-90%.

While a DC/DC converter of this type is potentially very efficient, there are some important issues that must be resolved before it can be used on a cell phone. The primary concern is with noise generated from the switching power MOSFET. The sharp rise times of the square wave voltage pulses can lead to conducted and radiated electromagnetic interference (EMI). The noise from the converter can adversely effect the proper operation of the radio and other sensitive analog circuitry in the phone. This interference is not only at the switching frequency of the converter but also at harmonics that extend into the hundreds of MHz. The size of the converter is another important design constraint. Cell phones are small devices with very tightly packed

circuit boards where space is at a premium. DC/DC converters can require large, bulky input and output filters that take up valuable space. In order to reduce the size of the filter components, the converter needs to be switched at very high frequencies (> 1MHz). However care must be taken so that capacitive losses in the power transistor and core losses in the inductor, which increase with switching frequency, do not severely degrade converter efficiency.

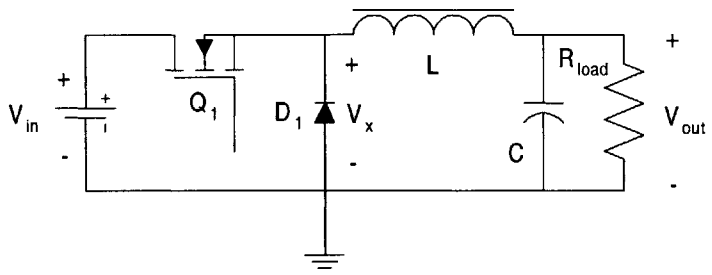

Figure 1-1: A buck converter employing a MOSFET switch and a free wheeling diode. The LC filter attenuates the AC component of the square wave voltage V_x to produce a DC voltage with a small ripple voltage.

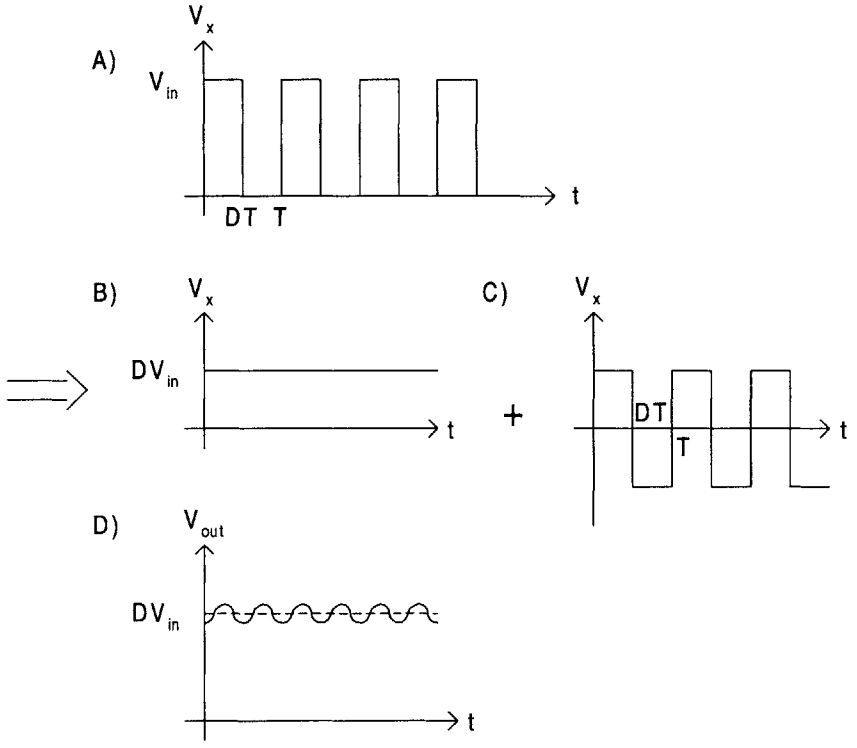

Figure 1-2: Buck converter waveforms. A) The square wave voltage V_x across the diode. B) DC component of the diode voltage. C) AC component of the diode voltage. D) The LC filter attenuates the AC component, leaving a DC voltage with a small ripple at the output.

1.3 Organization

This thesis covers the design of a high frequency buck converter and an integrated circuit controller for the converter. Chapter 2 discusses the issues involved in designing the power stage, input filter and output filter for the buck converter. The emphasis is on the losses in real devices and the effects their parasitic components have on the design of high frequency switch-mode power supplies. The design of the feedback control system using the state-space averaged model of the buck converter is presented in chapter 3. The design of the control chip is discussed in chapter 4. The integrated circuit is design using TSMC 0.25 μm CMOS process. The overall function of the control chip is describes as well as detailed explanations of the analog and digital sub-blocks. Chapters 5 present the converter to be simulated and the simulation results. The simulation is done on Analog Devices' spice simulator ADICE.

2 Buck Converter Design

2.1 Specifications for the buck converter

The DC/DC converter, including its control circuitry, must run off a 3.6 volt LiIon or NiMH battery. The input voltage can range from 2.9 volts when the battery is almost drained to 4.2 volts when the LiIon battery is charging or 5.1 volts when the NiMH battery is charging. At the highest power setting, the power amplifier draws 1 amp from the battery for 177 μsec when the phone is transmitting data. This may cause the input voltage to drop by as much as 600 mV with a rise/fall time of 3.7-15 μsec. The converter must be able to maintain output voltage regulation in the presence of these input voltage pulses. The converter must produce an output voltage of 1.2 volts with less than 1% steady state error and no more than 5 mV of peak-to-peak voltage ripple. The converter must be able to supply 30 mA - 300 mA of output current and have less than a 5% overshoot and a 20 μsec settling time to a current load step of 30 mA - 300 mA in 9 μsec. The target efficiency of the converter is 70% with a minimum allowable efficiency of 50%. Typical ambient operating temperature is 25 °C, but the converter has to be able to operate between –40 °C and 85 °C.

A mixed-signal IC provides the D/A and A/D conversion necessary for the DSP to communicate with the radio. The D/A converter in the mixed-signal IC operates at 6.5 MHz with a bandwidth of ±100 kHz but is sensitive to noise in frequency bands centered at integer multiples of 6.5 MHz. This is because the frequency content of the digital signal is repeated every 6.5 MHz in the analog domain. Interference in these bands can mix down to DC during a transmission burst and degrade the outgoing signal. Two other frequencies that are very sensitive to noise are 13 MHz and 26 MHz. 13 MHz is the frequency of the system clock, and 26 MHz is the operating frequency of the receiver A/D converter (using the rising and falling edge of the system clock). In order to reduce interference, it is required that there be no switching noise within 500 kHz of 6.5, 13 and 26 MHz. Thus there can be no switching harmonic falling in the following frequency

bands: 6-7 MHz, 12.5-13.5 MHz and 25.5-26.5 MHz. Switching frequencies that satisfy this requirement are 1.5, 2.5 or 3 MHz.

The PCB trace from the battery to the converter is usually the largest radiator of EMI, basically acting like an antenna. In order to reduce EMI, an input filter may be used to reduce the input current ripple to an acceptable level. Input filters that reduce the input current ripple to 1, 5 and 10 mA when the converter draws maximum load current will be designed and evaluated.

2.2 Power Stage

2.2.1 Pass transistor

The buck converter of Figure 1-1 shows a NMOS device as the pass transistor. The pass device can be either an NMOS or PMOS transistor. An NMOS transistor has lower input, output and miller capacitance than a PMOS with the same on-state resistance. This is important for good efficiency at high frequency and low output power, where capacitive losses dominate. The drawback for NMOS devices is that they require a charge pump to produce sufficient gate to source voltage to turn on. This requires two external components: a schottky diode and capacitor. Unfortunately, the maximum voltage the control IC can withstand is 5 V. The NMOS device would have to be charged to $2\times V_{bat}$ = 7.2 volts to properly turn on. The drive for PMOS transistors, on the other hand, can be ground referenced. Thus, a PMOS transistor will be used as the pass device.

2.2.2 Synchronous rectification

The loss due to diode forward voltage drop is too large for such a low voltage application. The power loss as a percentage of output power due to the forward voltage drop of the freewheeling diode is:

$$\frac{P_{diode}}{P_{out}} \approx \frac{(1-D)V_{diode}}{V_{out}} \tag{2-1}$$

For an output voltage of 1.2 V, duty cycle of 1/3 and a schottky diode with 0.4 V forward voltage drop, the diode power loss is 22% of output power. In order to achieve 70% efficiency,

$$\frac{P_{out}}{P_{out} + \sum \text{Losses}} \geq 0.7 \tag{2-2}$$

This means that total losses must be less than 43% of output power at a given output current. The freewheeling diode contributes half of the total losses allowed.

To remedy this, an NMOS power device is used in parallel with a schottky diode. The use of a MOSFET as a rectifying device in place of a freewheeling diode is known as synchronous rectification. The synchronous rectifier will be an NMOS transistor because it can be switched using a ground-referenced driver. However, using the MOSFET alone as a rectifier would also cause problems. If the NMOS rectifying device is turned on before the PMOS device is fully off, then power rail is shorted to ground (a shoot-through condition) creating a surge of current that can cause EMI and destroy the transistors. In order to prevent this the NMOS device is kept off while the PMOS device is turned off completely, letting the body diode of the NMOS device conduct and act like a freewheeling diode. Once the body diode is conducting full load current we can turn on the NMOS switch. We can then turn off the NMOS switch, let its body diode carry the output current and then turn on the PMOS switch. However, the reverse recovery loss in this body diode would be excessive and the reverse recovery time would be too long (30-50 ns) for such a fast switching converter. The body diode also has a high forward voltage, typically 0.8-1.2V. To prevent the body diode of the NMOS from conducting a schottky diode is added in parallel to act as a freewheeling diode between the turn on and turn off times of the power transistors. Low power schottky diodes typically have a forward voltage drop of 360 to 400 mV and a reverse recovery time of 10 ns.

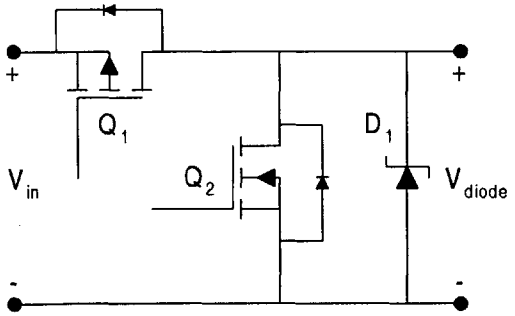

Figure 2-1: Power stage for the buck converter using a PMOS pass transistor, NMOS synchronous rectifier, and a schottky diode for free–wheeling conduction when both power MOSFETS are off.

2.2.3 Losses in the power stage

In order to properly select the transistors for the power stage, the losses in the power MOSFETs must be analyzed. There are three main loss mechanisms in power MOSFETs: capacitive loss, switching transition loss and conduction loss.

There are two types of capacitive loss, gate drive and capacitive turn-on loss. The gate drive loss is due charging and discharging the input capacitance of the power MOSFET. The total gate charge required to put a certain voltage across the gate and source is usually specified because the input capacitance is nonlinear [13]. Capacitive turn-on loss depends on the size of output capacitance. This capacitance is charged when the MOSFET turns off and is discharged when it is turned on (Figure 2-2). These losses are independent of the current through the MOSFET and depend only on switching frequency.

The switching transition losses are due to currents flowing through the MOSFET when their drain to source voltage rises and falls [9]. The smaller the input capacitance the less charge it takes to reach the turn-on gate voltage and the shorter the time in which there is current through the FET while a large voltage is across the drain and source (Figure 2-3). The power dissipated in the switching transition loss depends on frequency and current through the MOSFET. See Appendix A for a more detailed analysis of losses in MOSFETs.

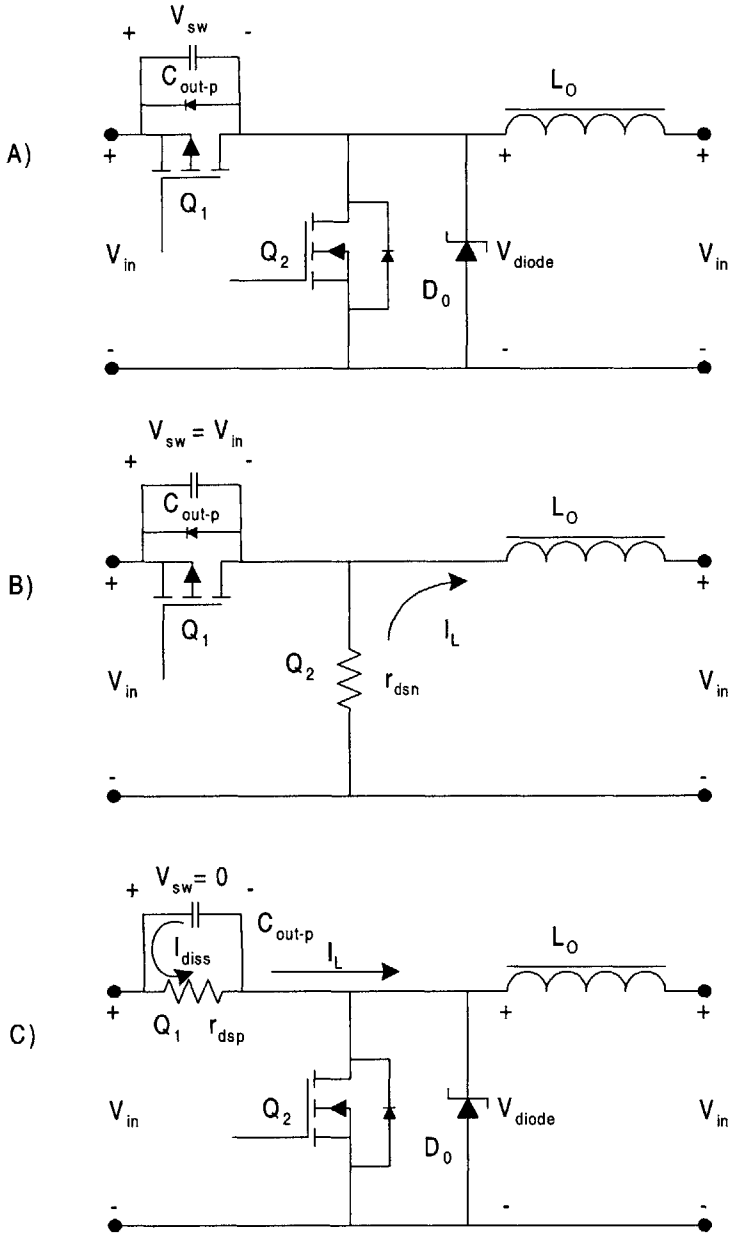

Figure 2-2: Capacitive turn-on loss in the PMOS pass device (Q_1). A) Power stage and inductor. The PMOS transistor is shown with its output capacitance across its drain and source. B) When the NMOS is conducting the PMOS device is off. The voltage across r_{dsn} is very small (~ 100 mV) and C_{out-p} charges up to V_{in}. C) When the PMOS device turns on C_{out-p} discharges through the on-state resistance r_{dsp} dissipating $\frac{1}{2}C_{out-p}V_{in}^2$ every cycle.

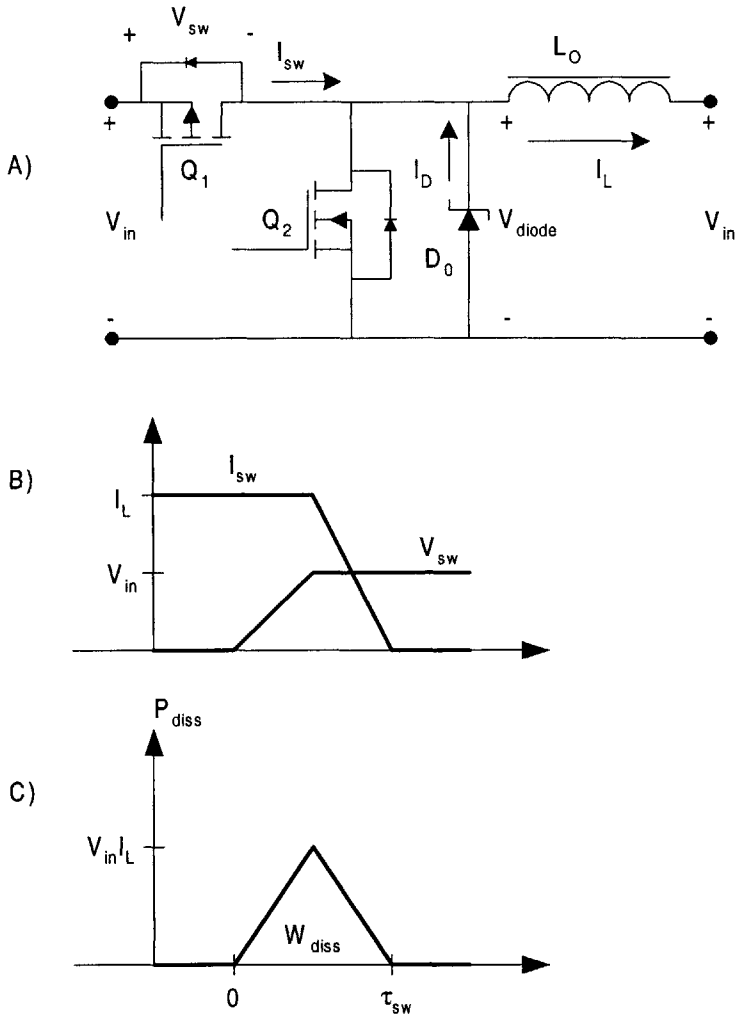

Figure 2-3: Switching transition loss when the PMOS device turns off. A) Power stage and inductor. B) In order for the current through the PMOS device to go to zero the schottky diode must turn on and start to carry the inductor current. In order for this to happen the voltage across the PMOS device, V_{sw} must rise to V_{in}. Since $V_{in} = V_{sw} + V_{diode}$, the schottky diode turns on and starts to conduct once V_{sw} equals V_{in} and the voltage across the diode is zero. C) The total energy dissipated while the PMOS device switches off is $W_{diss} = \frac{1}{2}V_{in}I_L\tau_{sw}$. The power dissipated in a cycle is the switching frequency, f, times W_{diss}. The lower the input capacitance the shorter τ_{sw} is. A similar power loss occurs when the PMOS device turns on.

Conduction loss is the third major loss mechanism in the converter. It is proportional to the on-state resistance of the power MOSFET. The input and output capacitances are proportional to the conduction area of the MOSFET while the on-state resistance is inversely proportional to the conduction area. Thus, there is always a trade off between the two loss mechanisms when

selecting MOSFETs. Since the converter's switching frequency is very high, the frequency dependent losses must be kept small. Thus, it is desirable to switch at the minimum allowed frequency of 1.5 MHz. Also, the converter is designed to carry low amounts of current (< 1A). Therefore, MOSFETS with small input capacitances (< 500 pF) and high on state resistances (> 0.2Ω) will be used.

Vishay Siliconix Si1555DL, Si1303/4DL and Si3585DV are suitable complementary power MOSFETs. The Si1555DL contains PMOS and NMOS transistors in a SOT-363 package while the Si3585DV transistor pair comes in a TSOP-6 package. The Si1303DL and Si1304DL each come in a SOT-323 package. The B0520WS from Diodes Inc. and the ZHCS400 from Zetex are small surface mount schottky diodes that come in a SOD-323 package and are suited for low power, high frequency applications. Their forward voltage drops are 360 and 400 mV at 300 mA, respectively. These diodes have small junction capacitances (< 100 pF at 3.6 V reverse voltage), very small leakage currents and reverse recovery times of 10 ns.

Table 2-1 compares the gate charge, input capacitance, output capacitance and on-state resistance of the three MOSFET pairs. The table shows the tradeoff between on-state resistance and input capacitance with the Si1555DL MOSFET pair having the smallest input capacitance and highest on-state resistance and the Si3585DV MOSFET pair having the largest input capacitance and lowest on-state resistance. Figures 2-4 and 2-5 show the various losses for the SI1555DL pair of transistors computed using the methods of Appendix A. Notice that the gate drive and capacitive turn on losses are independent of output current while both the switching transition and conduction losses increase with output current. Figure 2-6 compares the total losses in the power stage as a percentage of output power ($1.2V \times I_{out}$) over an output current range of 3 to 300 mA. All three MOSFET pairs have a loss of 10% of output power at then 150 mA of output current. Below 150 mA, the Si1555DL, with its small capacitance, has the least amount of power loss while above 150 mA, the Si3585DV MOSFET pair, with its small on-state resistance has the least amount of power loss. Thus, it is possible to optimize the converter for operation at

high or low currents depending on the time averaged profile of the DSP current draw. Figure 2-6 also shows the maximum amount of power loss that the converter can have in order to be 70% and 80% efficient. If the loss in the input and output filters and the control circuitry are kept low, then it is feasible to design a converter with over 80% efficiency.

Table 2-1: Gate charge, capacitances and resistances of different power MOSFETs

MOSFET	Gate Charge (nC) @ $V_{ds} = V_{gs} = 3.6V$	C_{in} (pF) @ $V_{ds} = 0$	C_{out} (pF) @ $V_{ds} = 0$	$R_{ds\text{-}on}$ (Ω) @ 25° C and $V_{gs} = 3.6$ V
Si1555DL PMOS	2.05	154	100	0.67
Si1303DL PMOS	2.7	230	150	0.45
Si3585DV PMOS	4	432	243	0.28
Si1555DL NMOS	1.33	84	64	0.47
Si1304DL NMOS	1.722	183	183	0.355
Si3585DV NMOS	2.9	250	175	0.16

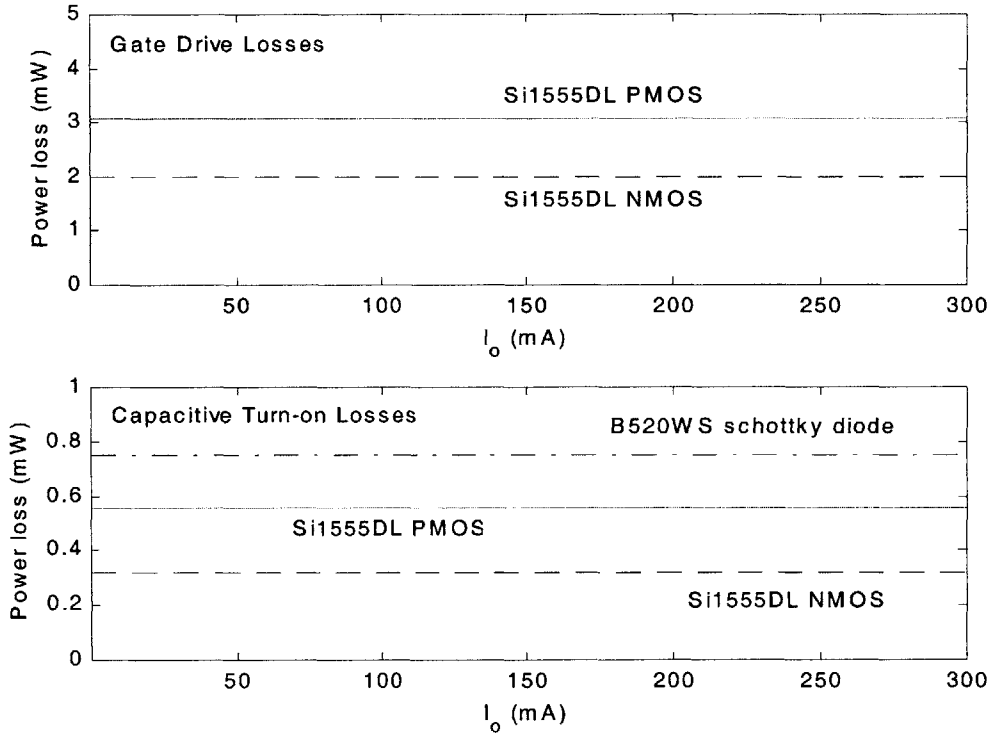

Figure 2-4: Top: Si1555DL PMOS and NMOS gate drive losses. Bottom: Capacitive turn-on losses in the Si1555DL PMOS and NMOS transistors and the B0520WS schottky diode.

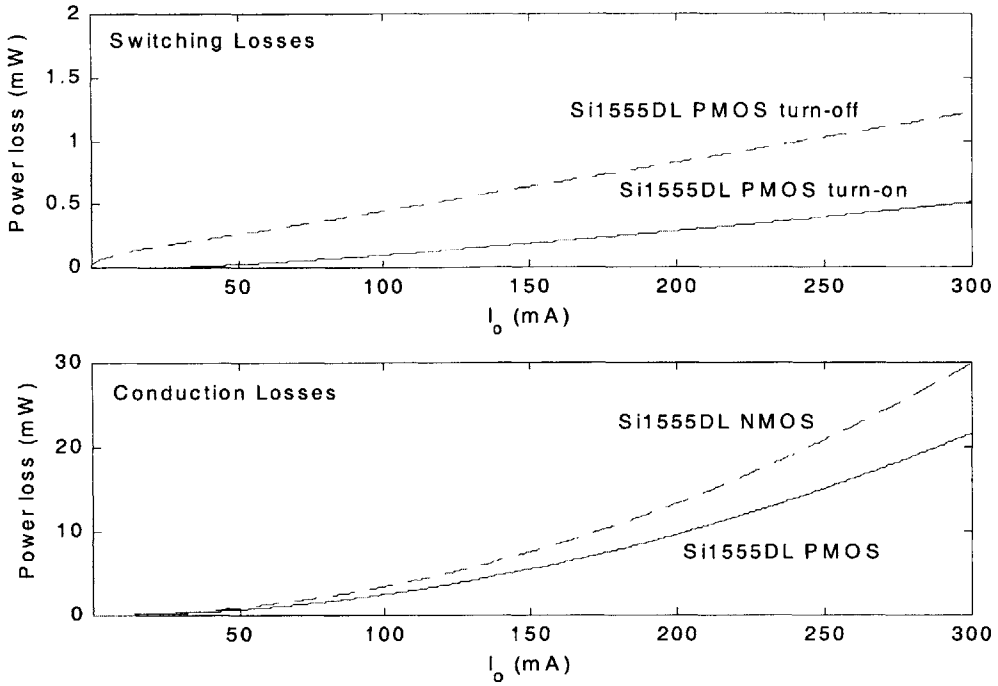

Figure 2-5: Top: Turn on and turn off switching losses for the Si1555DL PMOS pass transistor. Bottom: Conduction loss in the Si1555DL PMOS and NMOS transistors.

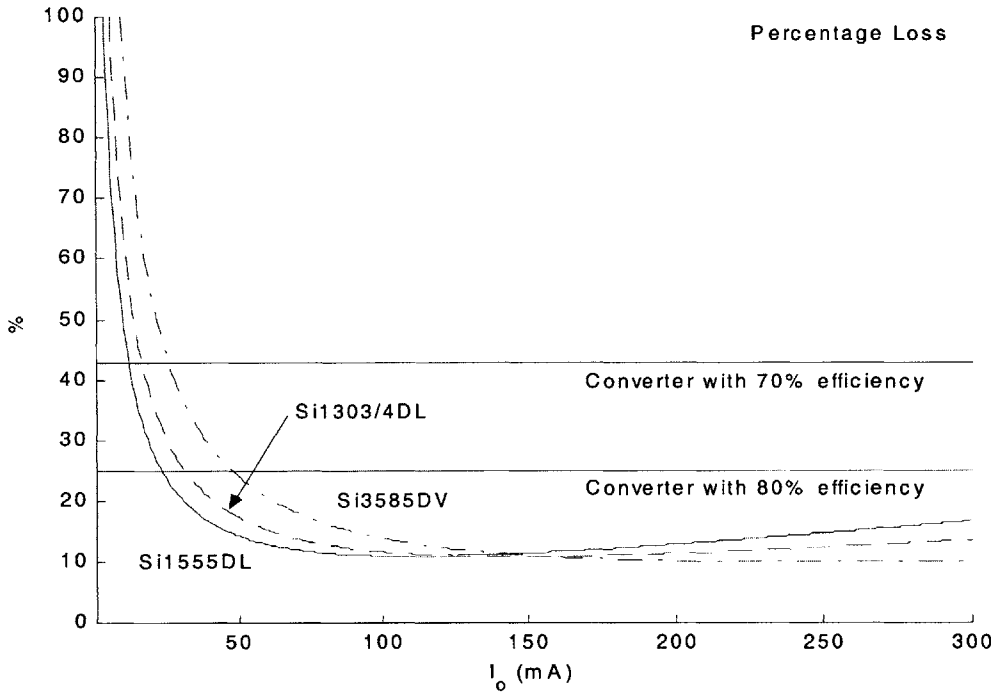

Figure 2-6: Power loss as a percentage of output power for Si1555DL, Si1303/4DL, and Si3585DV transistors as output current is varied. The solid line at 25% corresponds to an 80% efficient converter and the solid line at 43% corresponds to a 70% efficiency converter.

2.3 Output Filter Design

2.3.1 Filter size requirements

The output filter is a second order LC filter that is designed to attenuate the AC component of the square wave produced by the power stage while allowing the DC component pass through. The inductor integrates the square wave voltage into a triangular current waveform that has a DC current and a triangular current ripple. The magnitude of the current ripple is give by:

$$\Delta I_{p-p} = \frac{(1-D)TV_{out}}{L_O} \tag{2-3}$$

The DC current from the inductor flows directly into the load resistor to produce V_{out}. The ripple current will flow into the capacitor because at high frequency the capacitor has much lower impedance than the load resistor. The high frequency characteristics of the capacitor determine the peak-to-peak voltage ripple. The equivalent series resistance (ESR) and equivalent series inductance (ESL) of the capacitor dominate at high frequency. If the self-resonant frequency (SRF) of the capacitor is at least an order of magnitude above the switching frequency and the ESR is low, then the capacitor acts as a capacitive impedance and the ripple voltage produced by the ripple current though it is given by:

$$\Delta V_{p-p} = \frac{(1-D)T^2V_{out}}{8LC} \tag{2-4}$$

If the capacitor looks resistive at the switching frequency and above (i.e. ESR dominates) then the peak-to-peak ripple voltage is given by:

$$\Delta V_{p-p} = \Delta I_{p-p} \times ESR \tag{2-5}$$

However, above 1 MHz, most large capacitors (> 10 μF) are dominated by their ESL. In this case the ripple voltage can be approximated by:

$$\Delta V_{p-p} \approx \Delta I_{p-p} \times \omega_{switch} \times ESL \tag{2-6}$$

The energy storage requirement of the capacitor is also important for determining its size. The energy stored in the output filter capacitor should be greater than that of the inductor. Suppose the buck converter is supplying maximum output current to the DSP. If the DSP suddenly goes into sleep mode or is turned off the output current goes to zero. The current in the inductor will flow into the capacitor increasing the output voltage. If the inductor dumps all its energy into the capacitor the output voltage should not increase significantly. For a 5% change in output voltage:

$$0.5LI_{peak}^2 + 0.5CV_{out}^2 = 0.5C(V_{out} + \Delta V_{out})^2 \tag{2-7}$$

Simplifying and ignoring second order terms, the above equation reduces to:

$$LI_{peak}^2 + CV_{out}^2 \approx C(V_{out}^2 + 2V_{out}\Delta V_{out}) \tag{2-8}$$

Since ΔV_{out} = 5% of V_{out}, the requirement for the output filter capacitor becomes:

$$C \geq 10L\left(\frac{I_{peak}}{V_{Out}}\right)^2 \tag{2-9}$$

Since the switching frequency is 1.5 MHz or higher, small values of output filter capacitance and inductance can be used. The size of the inductor is determined by the amount of ripple current in the converter. Typically, the peak-to-peak ripple should be 20% to 40% of the peak output current or 60–120 mA for this design. For D = 1/3, T = 1/(1.5 MHz), this corresponds to inductor sizes of 8.8 μH for a current ripple of 60 mA and 4.3 μH for a 120 mA current ripple. Standard inductor values of 4.7, 6.8 and 10 μH are suitable. For an output ripple voltage of 5 mV and using a 10 μH inductor, the capacitor needs to be at least 0.89 μF using Equation 2-4. If the capacitor looks resistive at 1.5 MHz then its ESR must be less than 94 mΩ (Equation 2-5) and if it looks inductive then its ESL must be less than 10 nH (Equation 2-6). However, in order to have enough energy storage, the capacitance must be greater than 7.56 μF. Since the storage requirement for choosing the capacitor value is larger than the filter requirement any capacitor greater than 7.56 μF will satisfy the filter requirement.

2.3.2 Output filter inductor selection

There are three main issues in inductor selection. They are the self-resonance frequency, the current limit and the losses in the inductor. The first two parameters affect the physical size of the inductor while the third affects the efficiency of the buck converter.

The inductor should be chosen so that its self-resonance frequency (SRF) is at least an order of magnitude above the switching frequency. This is because the inductor integrates the square wave voltage produced by the power stage and a square wave can be reasonably approximated by its first ten harmonics. Beyond the SRF, the inductor's inter-winding capacitance dominates and acts as a short circuit at high frequency. This inter-winding capacitance is represented as a lumped capacitor across the terminals of the inductor (Figure 2-7). Typically, the larger the magnetic core of an inductor, the fewer number of windings it needs to achieve a given inductance. The fewer number of windings an inductor has, the smaller the overall inter-winding capacitance.

The current limit of an inductor specifies the current at which inductance drops by 20%. The inductance decreases because the inductor core is starting to saturate. It is critical that the sum of the ripple and DC output current not saturate the core. If the core saturates, the inductance will decrease dramatically and the ripple current will increase. This will lead to a higher output ripple voltage. Typically the inductor is chosen so that it can handle at least twice the output current without saturating the magnetic core. As in the case of the SRF, a larger magnetic core allows the inductor to store more flux without saturating and thus, handle more current.

Finally, the losses in the inductor must be analyzed. The resistance in the winding, represented as R_{DC} in Figure 2-7, should be kept small so that it does not contribute significant conduction loss. A good rule of thumb is that the power dissipated in R_{DC} should be less than 5% of output power at maximum output current. So at 300 mA, the output power is 360 mW. In order for conduction loss to be less than 5% of 360 mW, or 18 mW, R_{DC} should be less than 0.2 Ω.

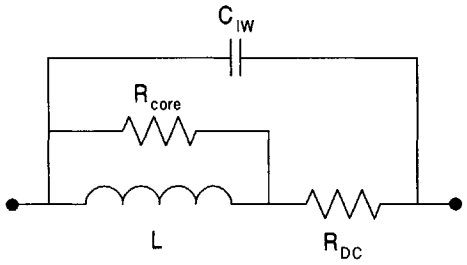

Figure 2-7: Lumped parameter circuit model of a real inductor. R_{DC} is the DC resistance in the windings. C_{IW} is the inter-winding capacitance and R_{core} is a nonlinear resistor that represents the energy lost aligning the magnetic domains in the inductor core.

The loss in the inductor's magnetic core can be a significant source of loss at switching frequencies greater than 1 MHz. This loss is due to the energy required to realign the magnetic domains in the core as the current through the inductor changes. This energy is dissipated as heat and is represented as a nonlinear resistor, R_{core}, in parallel with the inductor in Figure 2-7. The core loss is dependent on the frequency and magnitude of the ripple current through the inductor. For a given core size, the larger the inductance the lower the loss. It is best to experimentally verify that losses from the core are small.

Surface mount power inductors should be used due to their small size, high SRF and large current handling capabilities. Table 2-2 shows the characteristic of 3 suitable 10 μH surface mount inductors from Coilcraft, Wilco and Renco. The losses in these inductors were tested at 1.5, 2.5 and 3 MHz using the method described in Appendix B. The power loss as function of output current is shown in figures 2-8. Notice that the losses do not vary significantly with frequency. The core loss is proportional to frequency, so as the frequency goes up the core loss increases [12]. However, as the frequency increases the ripple current in the inductor decreases so that the overall loss slightly decreases. This will not be the case for all inductors so testing their losses is important.

Table 2-2: Surface mount power inductor characteristics

Inductor	Value (μH)	DCR (Ω)	SRF (MHz)	I_{sat} (A)	Tolerance	Size (mm) LxWxH
Coilcraft DS1608C	10	0.075	38	1	±20%	6.6x4.45x2.92
Wilco SMPI20	10	0.08	23.5	1.02	±10%	4.5x3.96x4.29
Renco RL-1608-S10	10	0.075	38	1	±20%	6.6x4.45x2.92

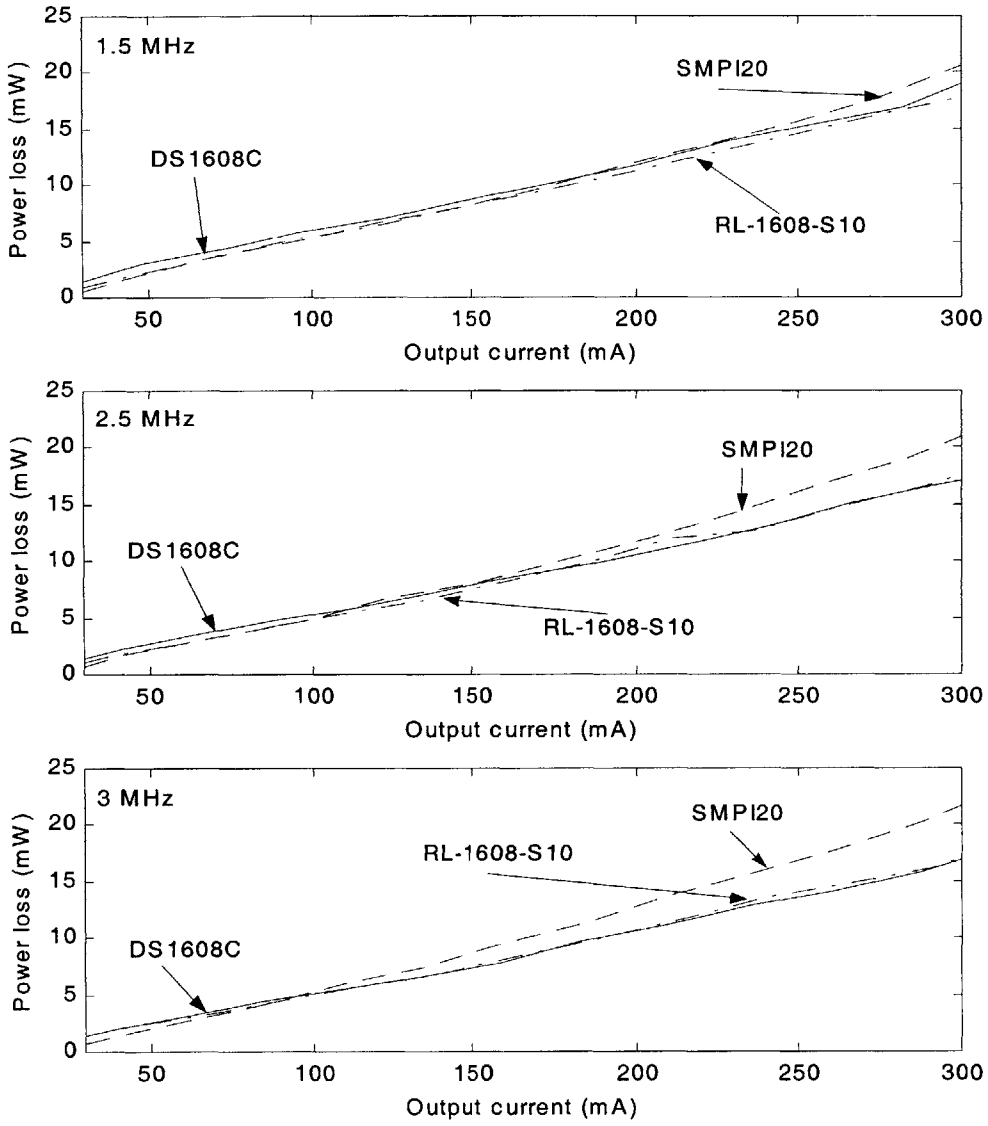

Figure 2-8: Power loss vs. output current in the DS1608C, SMPI20 and RL-1608-S10 inductors at 1.5 MHz (top), 2.5 MHz (middle) and 3 MHz (bottom).

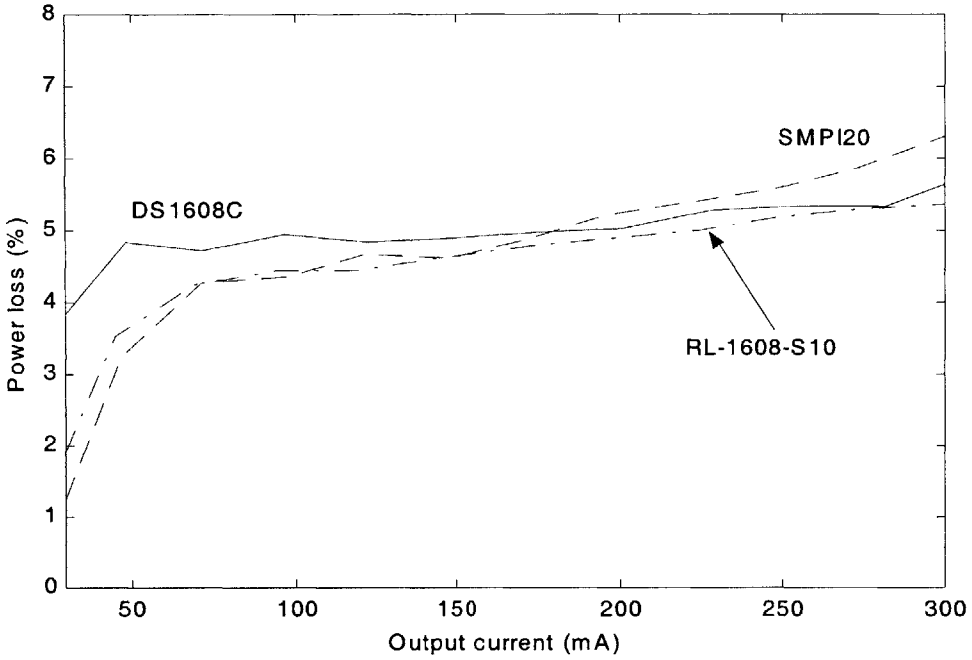

Figure 2-9: Power loss as a percentage of output power vs. output current in the DS1608C, SMPI20 and 1608-S inductors at 1.5 MHz.

Since the switching frequency of the converter is 1.5 MHz, Figure 2-9 shows the power loss as percentage of output power for the three 10 μH as the output current varies from 30 to 300 mA. The loss percentage is relatively steady at about 5% from 30 to 300 mA. This is because the ripple current through the inductor is independent of output current.

A sense resistor is often placed in series with the output filter inductor to sense the current through the inductor (Figure 2-10). Knowing the inductor current is important for over-current protection as well as enabling the use of current-mode control for regulating the buck converter's output voltage. Current-mode control will be discussed in Chapter 3. The sense resistor should be placed on the same side as the output filter capacitor. This is because the voltage across the diode is rapidly changing from 0 to V_{in}. Placing the sense resistor near the power stage would introduce noise in the current sense amplifier and prevent accurate sensing of the inductor current.

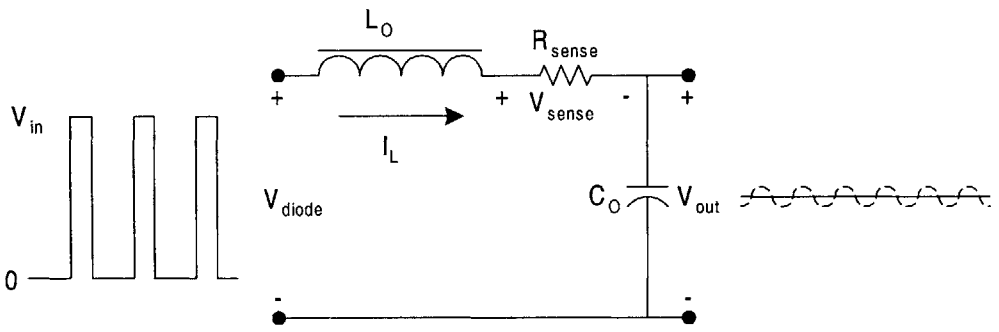

Figure 2-10: The sense resistor, R_{sense}, is placed in series with the output filter inductor, L_O. It is placed on the same side as the output filter capacitor, C_O, to minimize noise due to the diode voltage switching between 0 and V_{in} rapidly.

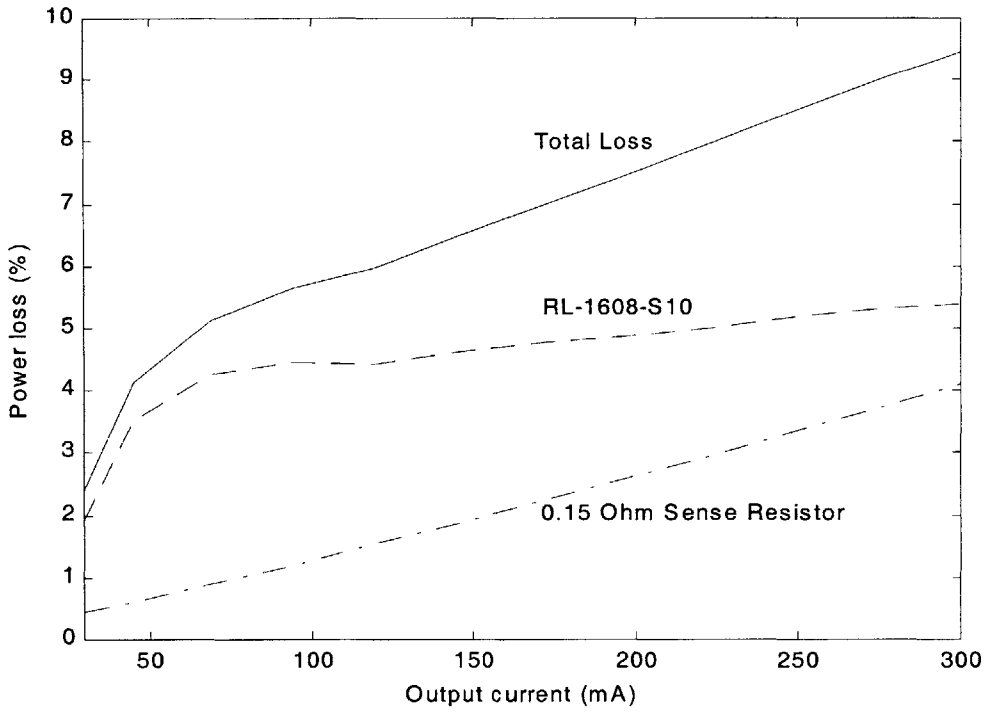

Figure 2-11: Power loss, as a percentage of output power, in the 0.15 Ω sense resistor, the RL-1608-S10 inductor and the total loss in the inductor-resistor pair.

The sense resistor should be small enough so that conduction losses due to it are small. Figure 2-11 shows the conduction loss as a percentage of output power for a 0.15 Ω sense resistor. It also shows the total loss percentage of the inductor-sense resistor combination for the RL-1608-S10 inductor. The sense resistor adds less than 1% of loss when output current is less than 100 mA and up to 4% at the maximum output current of 300 mA.

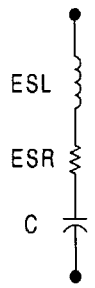

Figure 2-12: Lumped parameter circuit model of a real capacitor. ESL is the equivalent series inductance and ESR is the equivalent series resistance of the capacitor leads. These parasitic elements make the capacitor look inductive or resistive at high frequencies.

2.3.3 Output filter capacitor selection

For switching frequencies above 1 MHz, attention must be paid to ESR and ESL of filter capacitors. These parasitic elements limit the effectiveness of a capacitor at high frequencies and are shown in series with the capacitor in Figure 2-12. There are two possible choices of filter capacitors: tantalum electrolytic chip capacitors and multi-layer ceramic chip capacitors. Suppliers include Kemet, AVX and TDK and Taiyo Yuden.

Tantalum capacitors provide very large capacitances, typically 6.8 – 470 μF, in EIA 3216-7343 sized packages. An EIA 7343 corresponds to a package that is 7.3 mm long and 4.3 mm wide. These capacitors look resistive above 100kHz and inductive above 5-10 MHz. Since the first few harmonics of the switching frequency (1.5, 3, 4.5 and 6 MHz) usually fall within the resistive impedance range the output ripple voltage can be approximated to be equal to the capacitors ESR times the peak-to-peak inductor ripple current. As calculated previously, the ESR must be less than 94 mΩ in order for the ripple voltage to be less than 5 mV. Tantalum capacitors with ESRs less than 94 mΩ come in EIA 7343 size packages and have capacitance values of 100 to 470 μF.

Multi-layer ceramic caps are much smaller in size, coming in EIA 0603-1210 size packages. For ceramic capacitors, an EIA 1210 size package is 0.12 by .1 inches or 3.2 mm by 2.5 mm. Ceramic capacitors have capacitance values up to 47 μF for an EIA 1210 package. X7R

or X5R dielectric materials should be used due to their good temperature stability. The X5R and X7R dielectrics have a ±15% capacitance variation from –55 to +85 °C and –55 to +125 °C respectively. These capacitors have excellent high frequency characteristics and have very small parasitic resistances (< 10 mΩ for a 10 μF capacitor). The conduction loss for a capacitor with an ESR of 10 mΩ and 120 mA of ripple current is only 12 μW.

The ESL of ceramic capacitors dominates at high frequencies but is typically less then 1 nH. Table 2-3 shows the parasitic inductances due to different package sizes for TDK capacitors. For a given package size, the ESL varies with capacitor value. Notice that there is a difference between the ESL of an 0508 package and an 0805 package even though their volumes are the same. The ESL is proportional to the width of the package leads. An 0508 package has a width of 2 mm while a 0805 package has a width of 1.25 mm. This why the 0508 package has a much lower ESL. Thus is always preferable to use capacitor packages with wide leads to reduce ESL.

The main drawback of ceramic capacitors is that they do not have as high a capacitance as the tantalum capacitors. Fortunately, since we are switching at very high frequencies, large capacitance values are not needed. At least 7.56 μF is required for energy storage. EIA 0805 (2 mm × 1.25 mm) size packages can have capacitance values of 10 μF. Currently, EIA 0508 packages have at most 1 μF. Multi-layer ceramic capacitors are the best choice due to their small size and small ESR and ESL.

Table 2-3: Parasitic inductances due to package size of TDK ceramic capacitors

EIA Code	Package size, L× W× H (mm)	Parasitic Inductance (nH)
0306	0.81×1.6×0.9	0.3-0.35
0508	1.25×2×1.3	0.3
0603	1.6×0.81×0.9	0.6-0.8
0612	1.6×3.2×1.5	0.4
0805	2×1.25×1.3	0.6-0.9
1206	3.2×1.6×1.5	1.1-1.4
1210	3.2×2.5×1.7	1.1-1.2

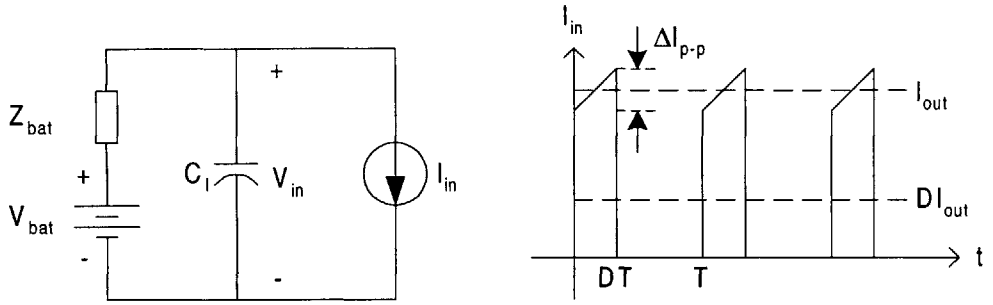

Figure 2-13: The power stage is modeled as a current source that equals the inductor current when the pass transistor is on and equals zero when the pass transistor is off. The inductor current rises from I_{out} - ½ΔI_{p-p} to I_{out} + ½ΔI_{p-p}. This current source sees the battery impedance in parallel with the input capacitor, C_I.

2.4 Input Filter Design

2.4.1 Overview

An input filter may be used to reduce the EMI generated from the power MOSFETS. The power stage of the buck converter can be modeled as a current source I_{in} that has a value of I_l when the pass transistor is on and 0 when the pass transistor is off (Figure 2-13). This square wave current has a DC value of DI_{out}. This current source sees the input filter capacitor and battery impedance in parallel. If the battery impedance is larger than the input capacitor impedance, then any ripple current through the battery can produce large voltage swings. These voltage swings will interfere with the supply rail of the cell phone. If the battery impedance is smaller than the input capacitor then most of the ripple current will flow through the PCB trace from the pass transistor to the battery. This trace will act as an antenna and radiate considerable amounts of EMI. This EMI will interfere with the radio and the D/A converter in the cell phone. As discussed is section 2.1, the D/A is sensitive to noise in frequency bands 200 kHz wide centered at multiples of 6.5 MHz. The EMI generated from the square wave current source, I_{in}, will have harmonics that fall into these bands. For instance, the 26^{th} harmonic of I_{in} can cause interference at 39 MHz, which is the fourth multiple of 6.5 MHz.

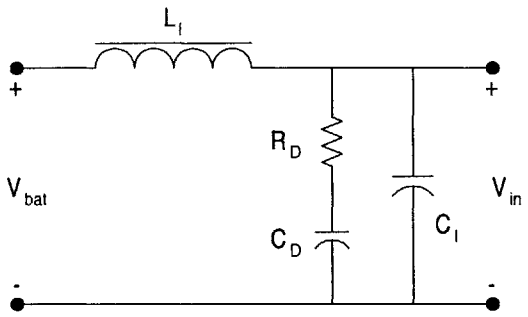

Figure 2-14: Second order input filter consisting of inductor L_I and capacitor C_I. R_D and C_D make up the damping leg that reduces the peaking at the resonance frequency of the LC filter.

To reduce the EMI generated by the PCB trace from the battery to the power stage the impedance of the source must be made larger than the impedance of the input filter capacitor at the ripple frequency. Placing an inductor between the battery and the input capacitor does the job. The LC filter attenuates the ripple current generated by the buck converter to a negligible level. The input capacitor will source most of the ripple current to the power stage while the battery supplies a DC current equal to DI_{out}. The DC current from the battery will flow to the output filter inductor when the pass transistor is on and will charge up the input filter capacitor when the pass transistor is off. The LC filter will need to be damped so that it will not ring at its resonance frequency. This is accomplished by placing a resistor and capacitor in parallel with the input filter capacitor [10]. This RC network is known as a damping leg. Figure 2-14 shows a complete second order LC input filter with a parallel RC damping leg.

2.4.2 Input filter size requirements

The actual interference in the radio and mixed-signal chips due EMI generated by the buck converter is highly dependent on the circuit layout within the cell phone. Since actual interference is unknown, input filters will be designed to reduce the ripple current through the input filter inductor, L_I, to be 50, 100 and 200 times smaller than the peak inductor current. The peak inductor current is $I_{out} + \frac{1}{2}\Delta I_{p\text{-}p}$ (Figure 2-13). The maximum output current is 300 mA.

From Section 2.3.1, the ripple current in the output filter inductor, L_O, is:

$$\Delta I_{p-p} = \frac{(1-D)TV_{out}}{L_O} \tag{2-10}$$

The maximum ripple current, $\Delta I_{p-p,max}$, is 166 mA and occurs when the output filter inductor is 3.76 μH and the duty cycle is 0.282 (V_{in} is 5.1 V). Therefore the peak inductor current is I_{out} + $\frac{1}{2}\Delta I_{p-p,max}$ = 376 mA.

The LC input filter must attenuate the pulsed current by a factor of 50, 100 and 200 at the switching frequency of 1.5 MHz. For a given output current the ripple current through the input filter inductor is given by:

$$I_{ripple} = \frac{Z_c \| Z_d}{Z_c \| Z_d + Z_l}\left(I_{out} + \frac{\Delta I_{p-p}}{2}\right) = \frac{Z_c \| Z_d}{Z_c \| Z_d + Z_l} I_{peak} \tag{2-11}$$

where Z_c, Z_d and Z_l are the real impedances of the capacitor, damping leg and inductor, respectively. The battery impedance is assumed to be 0, which is the worst-case scenario. If the filter capacitor and inductor behave like ideal components at 1.5 MHz then:

$$\frac{I_{ripple}}{I_{peak}} = \frac{Z_c \| Z_d}{Z_c \| Z_d + Z_l} \approx \frac{1}{L_I C_I s^2 + \frac{L_I}{R_D} s + 1} \approx \frac{1}{LC\omega_{sw}^2} < \frac{1}{\eta} \tag{2-12}$$

where η is either 50, 100 or 200. The product of L(μH)×C(μF) must be greater than 0.563, 1.125 and 2.25 for η of 50, 100 and 200, respectively . The input filter capacitor value is typically made much larger than the input filter inductance since a large capacitor is smaller in size and cheaper than a large inductance.

The components of the damping leg should be sized so that it looks resistive at the resonance frequency of the input filter. The damping resistor should be made equal to the characteristic impedance of the LC filter so that there is no overshoot at the resonance frequency:

$$R_D = \sqrt{\frac{L_I}{C_I}} \tag{2-13}$$

The damping capacitor must be made large so that its impedance is much less than the damping resistor at the resonance frequency of the LC filter. That allows the damping leg to provide parallel damping without any DC power dissipation. This requires that:

$$\frac{1}{C_D \omega_{res}} << \sqrt{\frac{L_I}{C_I}} \tag{2-14}$$

or

$$\frac{1}{C_D} << \sqrt{\frac{L_I}{C_I}} \sqrt{\frac{1}{L_I C_I}} = \frac{1}{C_I} \tag{2-15}$$

C_D is usually made to be 4 to 10 times larger than the C_I so that the damping leg's impedance is resistive at the resonance frequency of the input filter.

2.4.3 Component selection

The main issue when choosing the input filter inductor, L_I, is to make it large enough to handle the average current into the converter. Ideally the power into the converter equals the power delivered to load. The power into the converter is $V_{in}I_{in}$ and the power to the load is $V_{out}I_{out}$ or $DV_{in}I_{out}$. Equating input and output power, the average current into the converter is DI_{out}. This means that L_I must handle much less current than the output filter inductor. The maximum of DI_{out} is 150 mA when V_{in} in 2.9 V. The maximum current rating of the inductor should be at least two times the maximum input current.

Two small surface mount power inductors were found suitable for the input filter. They are the 1 μH NLFC201614 and the 1 μH NLFC 252018 from TDK. Table 2-4 compares their characteristics. These were the smallest power inductors found capable of handling at least 300 mA of current.

Table 2-4: Input Filter Inductors

Component	Inductance (μH)	Tolerance	SRF (MHz)	DCR (Ω)	I_{sat} (A)	Size (mm)
NLFC201614	1	±20%	100	0.16	0.3	2.1×1.6×1.4
NLFC252018	1	±20%	100	0.13	0.455	2.5×2.0×1.8

Since L_I is 1 μH, C_I must be 0.56 μF, 1.125 μF and 2.25 μF to attenuate the input current ripple by a factor of 50, 100 and 200 respectively. The closest standard capacitor values are 0.47 μF, 1 μF and 2.2 μF. The 0.47 μF and 1 μF multi-layer ceramic capacitors come in EIA 0603 size package (1.6 mm × 0.8 mm × 0.8 mm) and the 2.2 μF capacitor comes in an EIA 0805 size package (2.1 mm × 1.25 mm × 0.85 mm). The ESL for these capacitors is 600-700 pH, making SRF greater than 4 MHz. At 1.5 MHz, these capacitors are dominated by their capacitive impedance and not their parasitic elements.

The damping capacitor, C_D, will be a 10 μF coming in an EIA 0805 package. This makes the damping capacitor 4.5 times larger than the 2.2 μF input filter capacitor and 10 times larger than the 1 μF input filter cap. If a 0.47 μF input filter capacitor is used, C_D could be reduced to 4.7 μF. However, since the smallest package size for a 4.7 μF capacitor is EIA 0805, no reduction is size is gained so a 10 μF capacitor can be used for all three input filter capacitors. The SRF of the 10 μF capacitor is 2 MHz, so it still looks capacitive at the switching frequency.

A chip resistor should be used for the damping resistor. The characteristic impedances for the input filters with L_I equal to 1 μH and C_I equal to 0.47 μF, 1 μF and 2.2 μF are 1.46Ω, 1 Ω and 0.674 Ω, respectively. The closest standard values for these resistors are 1.5 Ω, 1Ω and 0.68 Ω. All three resistors come in an EIA 0402 size package (1 mm × 0.5 mm × 0.35 mm).

Table 2-5 summarizes the performance of the input filter for different values of input filter capacitor and damping resistor. The peak-to-peak ripple current through the input filter inductor is given by:

$$I_{ripple} = \frac{Z_c \parallel Z_d}{Z_c \parallel Z_d + Z_I} I_{peak} \tag{2-16}$$

The peak current is assumed to be 376 mA as calculated in Section 2.4.2. The performance of the input filter is as expected because the parasitic elements of the components used do not dominate.

Table 2-5: Input Filter performance for different component values

L_I (μH)	C_I (μF)	C_D (μF)	R_D (Ω)	I_{ripple} (mA) when I_{peak} = 376 mA
1	0.47	10	1.5	7.5
1	1 μF	10 μF	1	3.72
1	2.2 μF	10 μF	0.68	1.75

2.4.4 Input filter losses

The ripple current through the inductor calculated in Section 2.4.2 is much smaller than the pulsed current going into the power stage. For the purpose of the loss calculation, it is assumed that the entire ripple current from the power stage is sourced by C_I and the inductor only supplies the average current DI_{out}. DI_{out} flows through L_I and is sourced to the output filter inductor when the PMOS pass transistor is on (Figure 2-15). C_I provides the difference between I_L and DI_{out}. When the PMOS device turns off, the current through L_I flows into C_I and charges up the capacitor. The charge lost when the PMOS is turned on is $(1\text{-}D)I_{out} \times DT$. The charge gained by C_I when the PMOS device is off is $DI_{out} \times (1\text{-}D)T$. Thus the net change in V_{in} is zero.

In Figure 2-15, the resistance R_P is shown in series with C_I. R_P represents the sum of the ESR and PCB trace resistance. The multi-layer ceramic capacitors from Section 2.4.2 have only 2 to 3 mΩ of ESR, which dissipate negligible amounts of power. The resistance of the PCB trace from the PMOS pass transistor to C_I would be larger, around 10 to 50 mΩ. This relatively large trace resistance is possible because of the thin trace widths used on the compact printed circuit boards in cell phones. The current flowing through R_p is shown in Figure 2-15(D). The power lost in this trace resistance is:

$$P_{trace} = \left[D\left((1-D)^2 I_{out}^2 + \frac{\Delta I_{p-p}^2}{12} \right) + (1-D)(DI_{out})^2 \right] R_P \qquad (2\text{-}17)$$

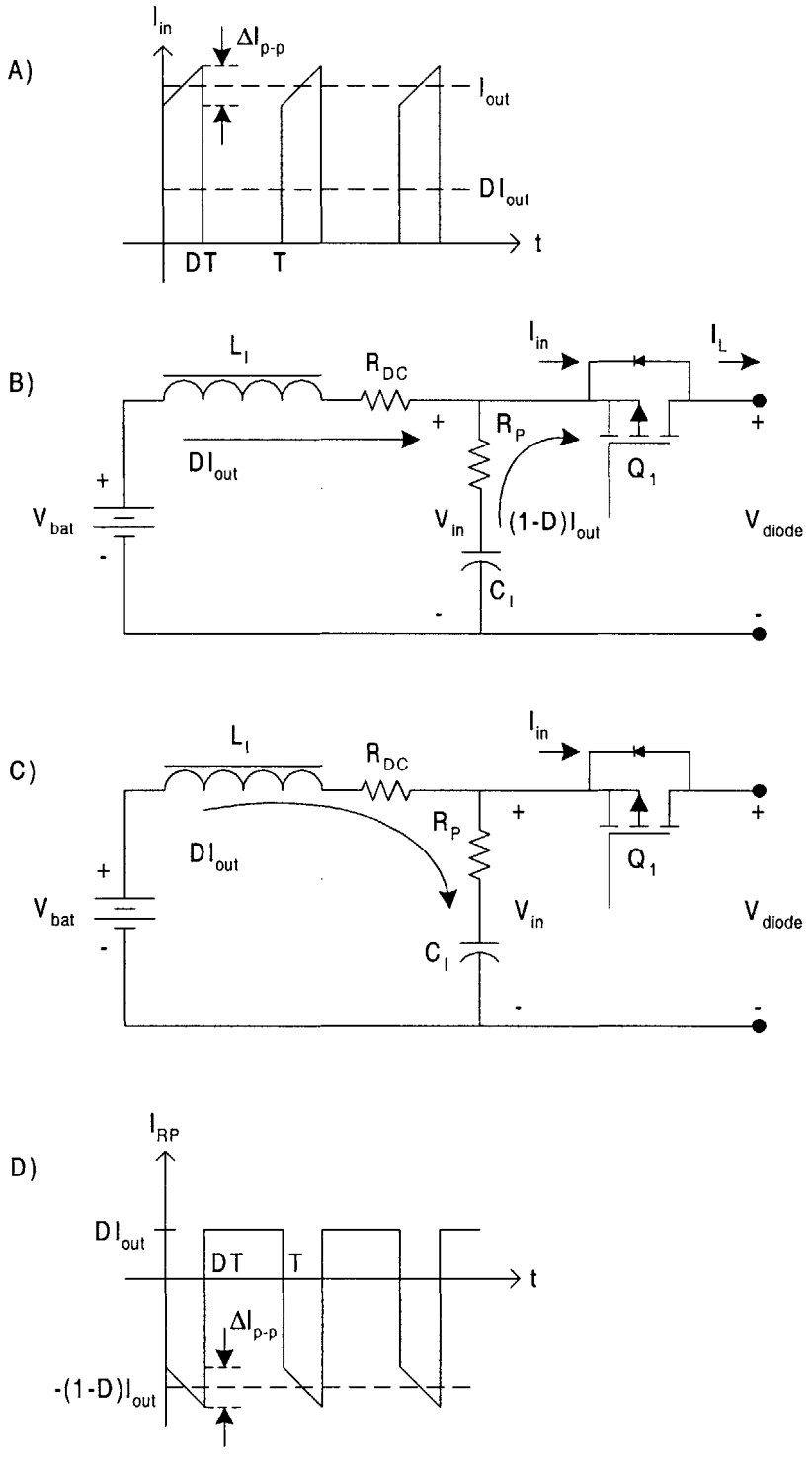

Figure 2-15: A) Current into the power stage of the buck converter. B) When Q_1 is on, the current through L_I, DI_{out}, flows to the output filter inductor while C_I sources an average current of $(1\text{-}D)I_{out}$. C) When Q_1 is off, the current through L_I flows into C_I, recharging the capacitor. D) Current through the resistor R_P. R_P is the resistance of the PCB trace from the Q_1 to C_I. The average current through C_I, which equals the average current flowing through R_P, is zero so that average value of V_{in} does not change.

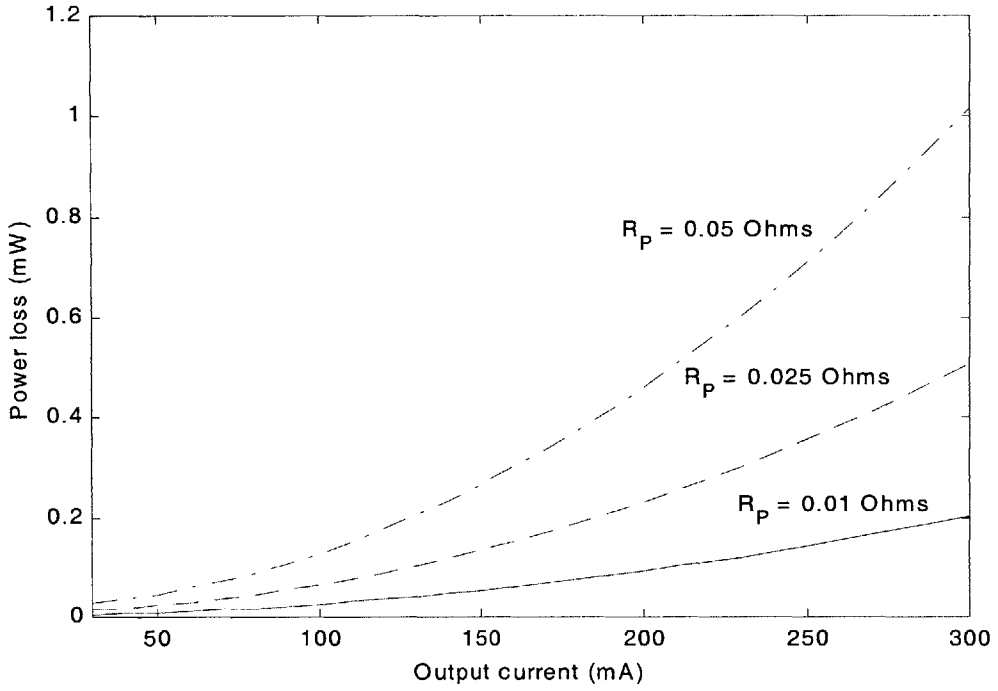

Figure 2-16: Power dissipated in the trace resistance, R_P, for R_P equal to 10, 25 and 50 mΩ. Duty ratio is 0.333 and L_O is 4.7 μH, making ΔI_{p-p} is 120 mA.

The loss as a function of output current is plotted in Figure 2-16. The loss was calculated assuming the duty ratio is 0.333 and L_O is a 4.7 μH inductor. The power dissipated in R_P is very small, only 1 mW when the trace resistance is 50 mΩ and the converter is sourcing 360 mW to the DSP.

The power lost in the inductors DC resistance is $P_{RDC} = (DI_{out})^2 R_{DC}$. This power loss is plotted versus output current in Figure 2-17 for NLFC201614 inductor. The DC resistance of this inductor is 0.16 Ω. The power lost increases as the input voltage decreases. When V_{in} is 2.9 volts, the duty ratio is 0.41 and the maximum power dissipated is less than 2.5 mW when output power is 360 mW.

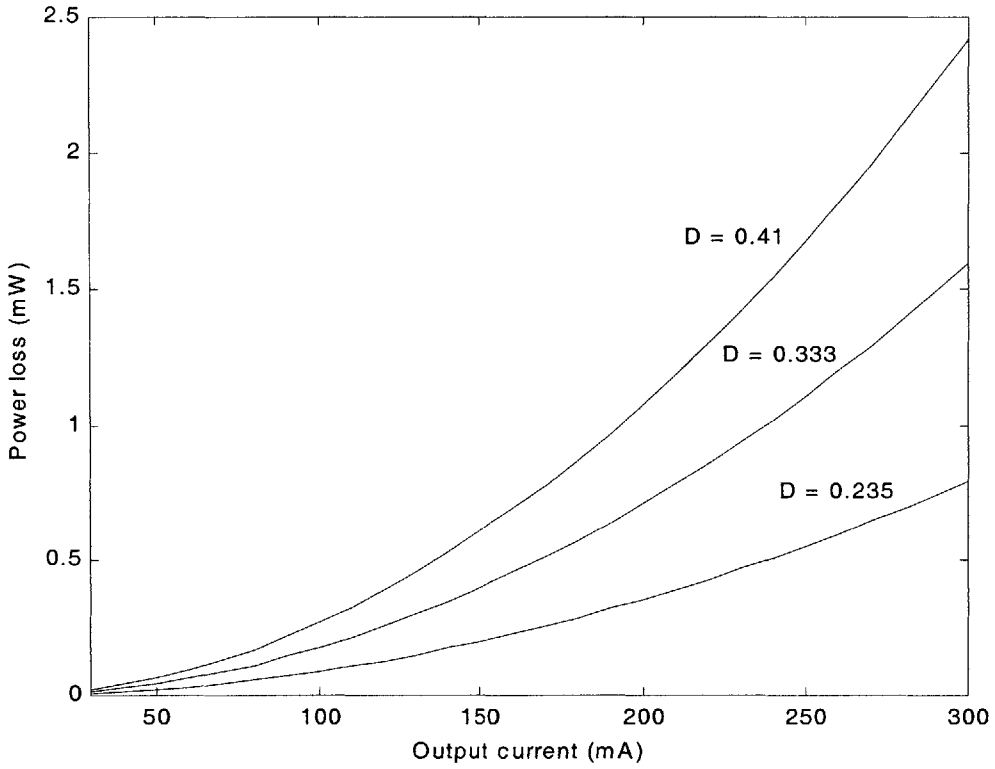

Figure 2-17: Power dissipated in the DC resistance of the NLFC201614 input filter inductor for different duty cycles. When battery is drained and the input voltage falls to 2.9 V, D will equal 0.41. When the battery is fully charged at 3.6 V D will equal 0.333 and if a NiMH battery is charging the input voltage rises to 5.1 volts so that D is reduced to 0.235.

The core loss in L_I is much smaller than the core loss in L_O. In Figure 2-9, the power lost in the 10 μH output filter inductors was 5% of output power. The ripple current through the inductors was 53.3 mA. The core loss in the inductor is proportional to $B_{ac}^{1.6-2}$, where B_{ac} is the AC magnetic flux through the inductor [9]. The AC magnetic flux is proportional to the ripple current through L_O, ΔI_{p-p}. Therefore, the core loss is proportional to $(\Delta I_{p-p})^{1.6-2}$. Since the ripple current through L_I is at most 7.66 mA, the core loss can be approximated to be more than 22 times smaller than the core loss in the output filter inductor if core loss is assumed to be proportional to $(\Delta I_{p-p})^{1.6}$. This translates to a loss of only 0.22% of output power, which can be ignored.

The amount of power dissipated in the damping leg is also negligible. The impedance of the damping leg is much larger than that of the input filter capacitor so little current flows into it. The total loss percentage in the input filter as a function of output current is shown in Figure 2-19 for different duty cycles. The input filter consists of the NLFC201614 inductor and an R_P of 50 mΩ. Even when the input voltage is 2.9 V (D = 0.41) and output current is 300 mA the input filter contributes less than 1% of output power to the losses in the converter.

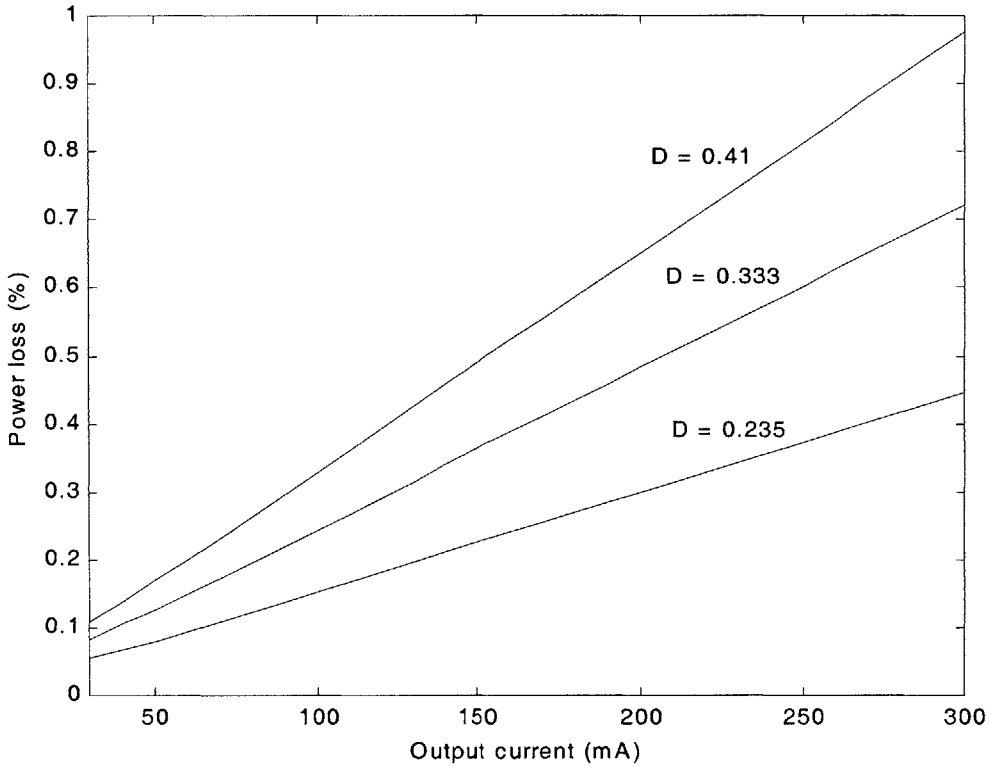

Figure 2-18: Power loss as a percentage of output power for the input filter using the NLFC201614 inductor and an R_P of 50 mΩ. The loss percentage is plotted at the nominal duty cycle (0.333) and at the min (0.235) and max (0.41) duty cycle.

2.5 *Summary of buck converter design*

The buck converter presented uses a PMOS device as a pass transistor and an NMOS device for synchronous rectification. The power MOSFETs used in the converter have low input capacitance and high on-state resistance. There is a schottky diode in parallel with the NMOS device to prevent the body diode of the NMOS from turning on. The output filter consists of a 10 μF capacitor and either a 4.7, 6.8 or 10 μH inductor. There is a second order LC input filter to reduce input current ripple. The filter has a damping leg in parallel with the input filter capacitor to prevent ringing at the filter's resonance frequency. All inductors are surface mount power inductors and all capacitors are multi-layer ceramics.

The converter switches at a constant frequency of 1.5 MHz, which is the lowest frequency whose harmonics do not fall in the 6-7 MHz, 12.5-13.5 MHz and 25.5-26.5 MHz frequency bands. The DSP that the converter supplies is modeled as a current source that sinks anywhere from 30 to 300 mA. There is a sense resistor in series with the output filter inductor and is used for current sensing. Current sensing is important for both over-current protection and feedback control. The converter designed in this chapter is shown in Figure 2-19.

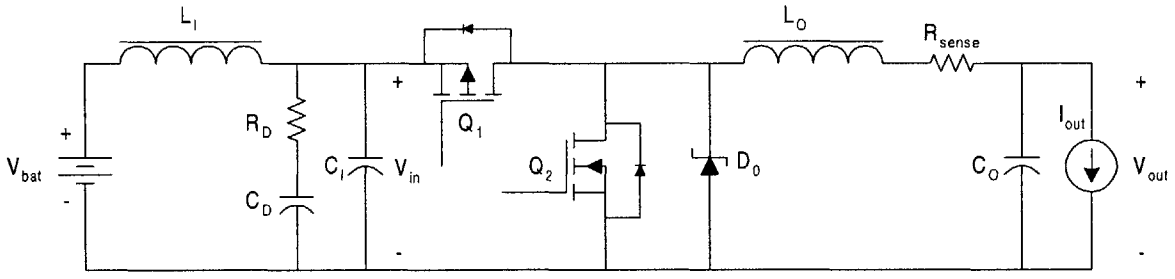

Figure 2-19: Synchronously rectified buck converter with second order input filter. The DSP is modeled as the current source load I_{out}. The sense resistor R_{sense} is used for current limiting and feedback control.

3 System Modeling and Controller Design

3.1 Dynamic model of Buck Converter

A dynamic model of the buck converter must be formulated in order to design a control system to meet the performance specifications. This is done by determining the state equations of the local average capacitor voltage, $\bar{v}_C$, and inductor current, $\bar{i}_L$, over one cycle and then linearizing the equations as described in [9]. The local average of a variable is defined as:

$$\bar{x}(t) \equiv \frac{1}{T}\int_{t-T}^{t} x(\tau)d\tau \tag{3-1}$$

Figure 13 shows the model for the synchronous buck converter used to determine its dynamics. Notice that regardless of which MOSFET is on, the state equation for the average voltage across the output capacitor is:

$$C_O \frac{d\bar{v}_C}{dt} = \bar{i}_L - \bar{i}_{OUT} \tag{3-2}$$

To determine the state equation for the current through the inductor, we define a switching function q(t), such that q(t) = 1 when the PMOS in on and NMOS is off and q(t) = 0 when the NMOS is on and PMOS is off. The average of q(t) is d, the duty ratio of the converter. Then the state equation for the average inductor current is:

$$L_O \frac{d\bar{i}_L}{dt} = \overline{qv}_{IN} - \bar{v}_C - (r_L + r_{sense})\bar{i}_L - \overline{qi_L} r_{DSP} + (\bar{i}_L - \overline{qi_L}) r_{DSN} \tag{3-3}$$

where r_L is the DC resistance of the inductor, r_{sense} is the sense resistor and r_{DSP} and r_{DSN} are the drain to source resistances of the PMOS and NMOS respectively.

The inductor equation is not a true state equation because the inductor current depends on the product of $\overline{q(t)v_{IN}(t)}$ and $\overline{q(t)i_L(t)}$. It is assumed that the variables $i_L(t)$ and q(t) have small ripple and that their average values do not vary rapidly (less than half the switching frequency).

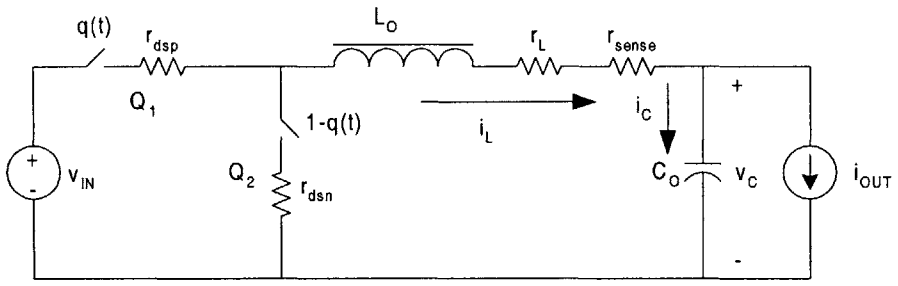

Figure 3-1: Equivalent circuit of synchronous buck converter for state space modeling. The power MOSFETS are replaced by their respective on-state resistances and switching functions.

Therefore, the average of the products $\overline{q(t)v_{IN}(t)}$ and $\overline{q(t)i_L(t)}$ can approximated to be the product of their averages,

$$\overline{q(t)v_{IN}(t)} \approx \bar{q}(t)\bar{v}_{IN}(t) = d(t)\bar{v}_{IN}(t) \tag{3-4}$$

and

$$\overline{q(t)i_L(t)} \approx \bar{q}(t)\bar{i}_{IN}(t) = d(t)\bar{i}_{IN}(t) \tag{3-5}$$

Now the inductor state equation becomes:

$$L_O \frac{d\bar{i}_L}{dt} = d\bar{v}_{IN} - \bar{v}_C - (r_L + r_{sense} + dr_{DSP} + (1-d)r_{DSN})\bar{i}_L \tag{3-6}$$

The last step is to linearize the two state equations. Each variable is written as a DC term plus a small variation, for example $\bar{v}_{IN} = V_{IN} + \tilde{v}_{in}$. Noting that $I_{OUT} = I_L$ and $DV_{IN} = V_C + r_x I_L$, where $r_x = r_{sense} + r_L + Dr_{DSP} + (1-D)r_{DSN}$, the linear small signal dynamics of the buck converter becomes:

$$\frac{d}{dt}\begin{bmatrix}\tilde{v}_c \\ \tilde{i}_l\end{bmatrix} = \begin{bmatrix}0 & 1/C_O \\ -1/L_O & -r_x/L_O\end{bmatrix}\begin{bmatrix}\tilde{v}_c \\ \tilde{i}_l\end{bmatrix} + \begin{bmatrix}0 & -1/C_O & 0 \\ D/L_O & 0 & V_{IN}/L_O\end{bmatrix}\begin{bmatrix}\tilde{v}_{in} \\ \tilde{i}_{out} \\ \tilde{d}\end{bmatrix} \tag{3-7}$$

3.2 Current-mode control

3.2.1 Current-mode operation

The current drawn by the DSP varies rapidly, on the order of microseconds. This poses the problem of designing a converter that has very accurate voltage regulation while being able to track a rapidly changing load current. A control system for the converter needs to have high bandwidth in order to respond and compensate for the rapid changes in load current. Current-mode control has the possibility of providing sufficient bandwidth.

Current-mode control is a two-loop control system [7,8]. The fast inner loop controls the inductor current while the slower outer loop regulates the output voltage (Figure 3-2). The reference current i_P is generated from the outer voltage loop. The reference voltage is compared to the output voltage and the difference is sent to a compensator $G_c(s)$. The output of the compensator is i_P. The inner loop pushes the inductor pole out to close to the switching frequency (1.5 MHz). Since the bandwidth of the controller needs to be around 100 kHz, the dynamics of the converter become first order with the capacitor pole dominating. This makes the overall system faster and easier to compensate.

Figure 3-3 shows the architecture for current-mode control. At the start of each cycle, the clock goes high, resetting the R-S latch. The output of the latch, Q, goes from 1 to 0. The shoot-through protection circuit forces the gate drive to the NMOS synchronous rectifier, N_{DR}, to go to 0. This turns the transistor off. Once the NMOS device is off, the shoot-through protection circuit forces the gate drive to the PMOS pass transistor, P_{DR}, to go to 0. This turns the PMOS device on. While the PMOS device is on, voltage across the inductor is V_{in}-V_{out}. The inductor current increases until the sensed current, $A_iR_{sense}i_L$, equals the reference current, i_P, at which point the current comparator trips and goes high. The comparator sets S high, which forces Q to 1. The shoot-through protection circuit first forces P_{DR} to equal V_{bat}, turning off the PMOS device. Once it is off, the shoot-through protection circuit then forces N_{DR} to equal V_{bat}, turning on the NMOS

device. While the synchronous rectifier is on, voltage across the inductor is now $-V_{out}$ and the inductor current falls for the rest of the cycle. The NMOS device will be on until the beginning of the next cycle, when the clock goes high again.

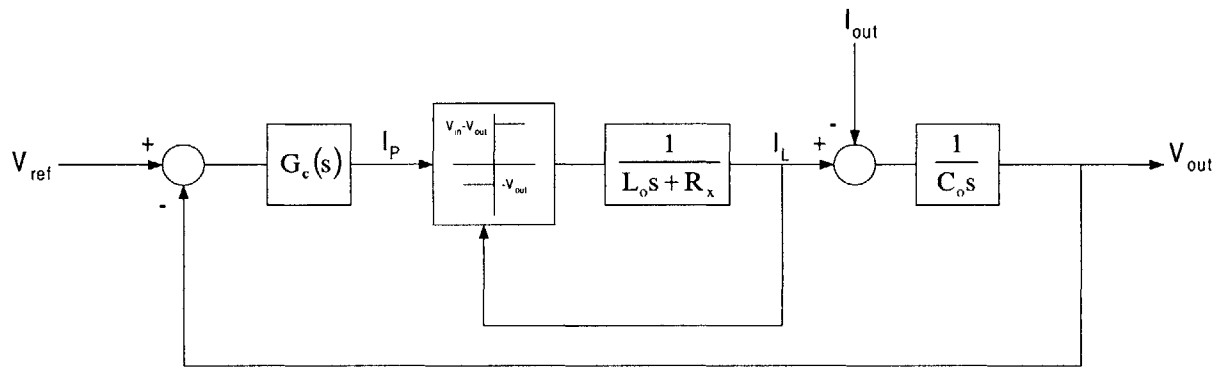

Figure 3-2: Block diagram of a current mode controlled buck converter. The nonlinear block in the minor loop represents the switching MOSFETS, schottky diode and switching logic circuitry. This block produces a voltage of $V_{in} - V_{out}$ across the inductor when the PMOS switch is on and a voltage of $-V_{out}$ when the NMOS is on.

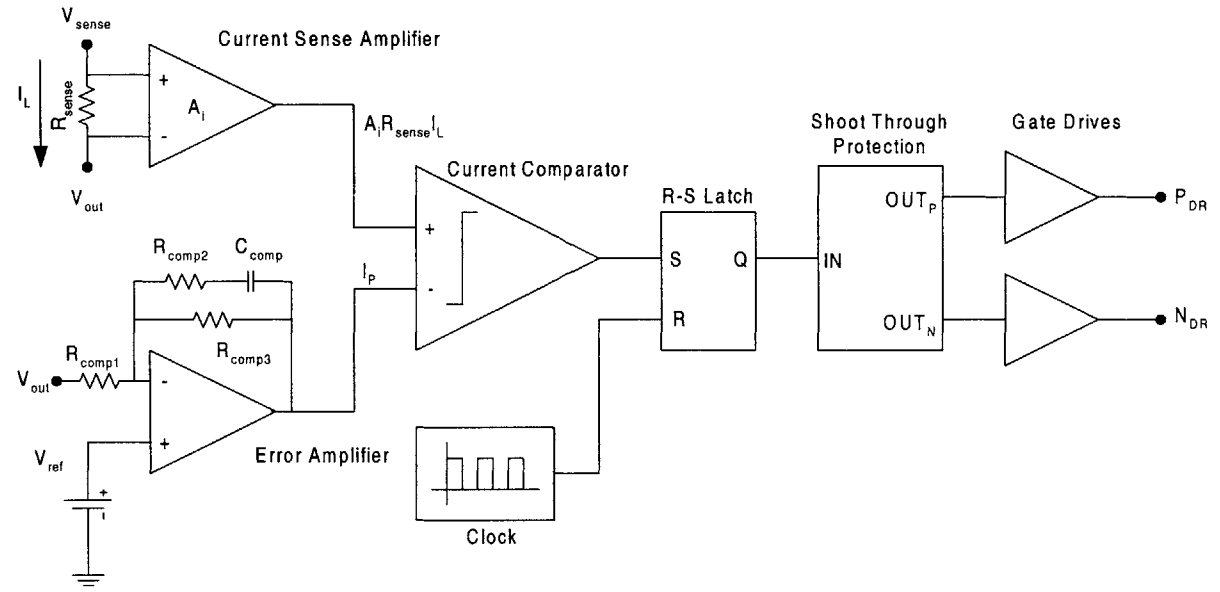

Figure 3-3: Current-mode control architecture. The resistor-capacitor network across the error amplifier implements $G_c(s)$. The shoot through protection circuit prevents both power MOSFETs from turning on.

3.2.2 Ripple instability and slope compensation

Instability in the inductor current, known as ripple instability, can occur in current mode controlled converters [11]. A perturbation in the inductor ripple current can cause limit cycling if the duty ratio is greater than 0.5. At the start of a cycle, the current through the inductor can be perturbed from its nominal value by ΔI_1. From Figure 3-4, this will lead to a perturbation of size ΔI_2 at the start of the next cycle. ΔI_2 is determined geometrically to be:

$$\left|\frac{\Delta I_2}{\Delta I_1}\right| = \left|\frac{m_f}{m_r}\right| = \left|\frac{V_{out}/L_O}{V_{in}/L_O - V_{out}/L_O}\right| = \left|\frac{V_{out}}{V_{in} - V_{out}}\right| \tag{3-8}$$

For stability, the ratio must be less than 1. This requires that $V_{out} < \frac{1}{2}V_{in}$. Nominally, this requirement is satisfied since V_{in} = 3.6V and V_{out} = 1.2V and no instability occurs. Even if the battery is close to being fully discharged and the voltage is 2.9V there is no instability. However, the ratio of ΔI_2 to ΔI_1 is only 0.7 making the perturbation poorly damped. Slope compensation can be used to make perturbations in the inductor current die off rapidly.

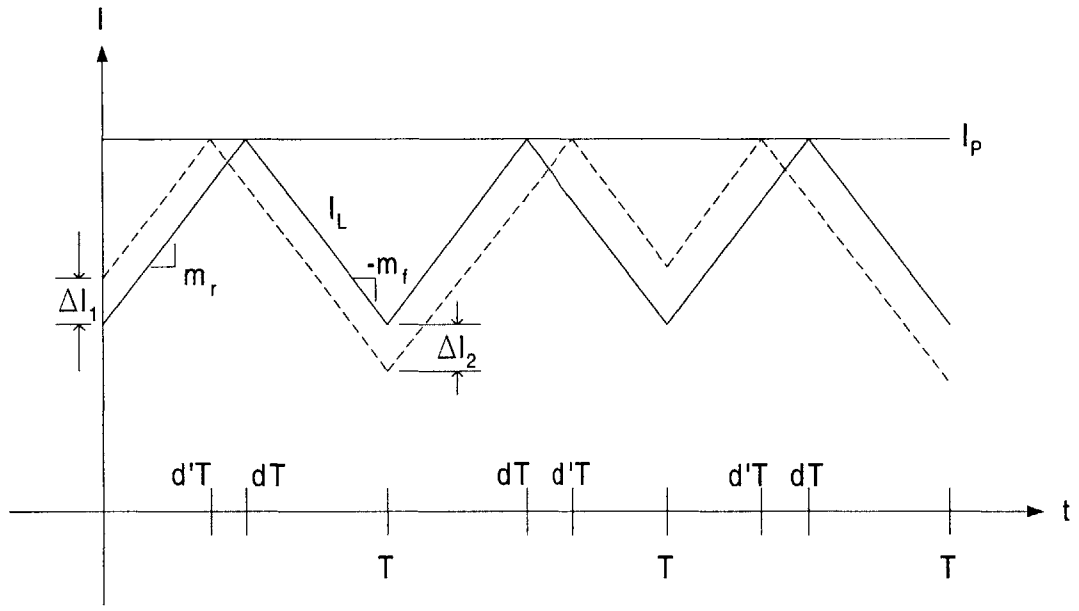

Figure 3-4: Ripple instability in the inductor current of a current-mode controlled converter. The duty cycle is 0.5 and therefore the perturbation, ΔI_1, in the inductor current is marginally stable.

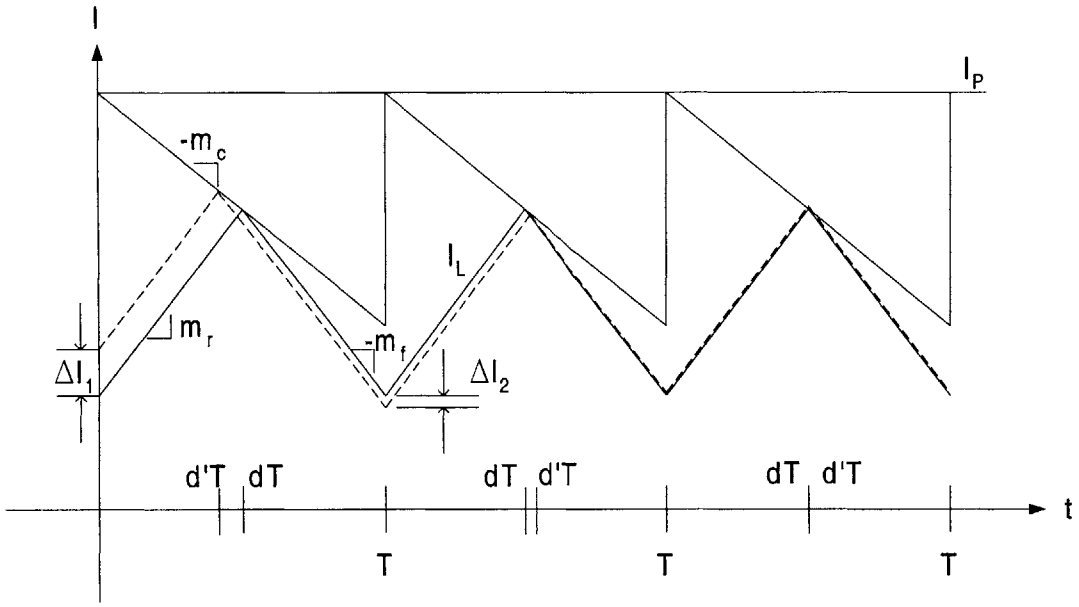

Figure 3-5: Current-mode control with slope compensation m_c. The perturbation ΔI_1 dies out in 3 periods due to the compensation.

In order to prevent instability a compensating ramp is added to the inductor current [11]. In Figure 3-5, the compensating ramp, with slope m_c, is shown subtracted from i_P. The new condition for ripple stability is:

$$\left|\frac{\Delta I_2}{\Delta I_1}\right| = \left|\frac{m_c - m_f}{m_c + m_r}\right| = \left|\frac{m_c - V_{out}/L_O}{m_c + (V_{in} - V_{out})/L_O}\right| \leq 1 \qquad (3\text{-}9)$$

The compensating ramp causes the perturbation in the inductor current, ΔI_1, to die out rapidly. If the ramp slope is made equal to the falling slope of the inductor current, then a perturbation in one cycle will not show up in the next. This is sometimes known as dead-beat compensation. L_O can vary from 3.76 μH to 12 μH due to tolerances. For 3.76 μH and 12 μH inductors, m_c needs to be between 3.2×10^5 A/s and 10^5 A/s, respectively, for approximately deadbeat compensation. The compensation slope, m_c, should be between these two values so that, regardless of the size of the inductor chosen, perturbations in the inductor current will die out

rapidly. m_c will be chosen to be 1.6×10^5 A/s so that perturbations decay as $(-0.26)^n$ if L_O is 3.76 μH and decay as $(0.2)^n$ if L_O is 12 μH.

3.3 Closed loop model

In order to design the voltage compensator $G_c(s)$, the transfer functions for the reference current, i_p, output current, i_{out}, and input voltage, v_{in}, to output voltage $v_{out} = v_c$ must be determined. The inductor current is converted to a voltage by sensing it through a 0.15 Ω sense resistor and then amplifying the voltage through a current sense amplifier with a gain $A_i = 3.75$. Since the control circuit operates on in terms of voltages, it is convenient to convert the inductor current and slope compensation waveforms into equivalent voltage waveforms.

To do this we define A_L as the gain from inductor current, i_L, to the sensed voltage v_L:

$$A_i r_{sense} i_L = (0.5625\,\Omega) i_L = A_L i_L = v_L \tag{3-10}$$

The rising and falling slopes of the inductor current m_r and m_f are also multiplied A_L to get the sensed inductor voltage rising and falling slopes n_r and n_f, respectively. Similarly, the reference current i_p will instead be a reference voltage v_p. The slope compensation ramp, $m_c = 1.6\times10^5$ A/s will also be multiplied by A_L and will be denoted as $n_c = 9\times10^4$ V/s.

Before deriving the transfer functions, it must be noted that there has to be an offset voltage, such that if the inductor current is zero, $v_P = v_{offset}$. This is due to fact that the control circuit must operate from the same 3.6V battery as the converter. The voltage swing of the error amplifier will typically be from $V_{ds,sat}$ to $V_{bat} - V_{ds,sat}$. Thus, v_{offset} should be larger than $V_{ds,sat}$ so that the error amplifier does not leave the active region. Figure 3-6 shows the relationship between all the waveforms in the inner control loop.

The average inductor current $\bar{v}_L$ is solved for geometrically [8]:

$$\bar{v}_L = \bar{v}_P - \bar{v}_{OFFSET} - n_C dT - 0.5\bar{n}_R d^2 T - 0.5\bar{n}_F (1-d^2) T \tag{3-11}$$

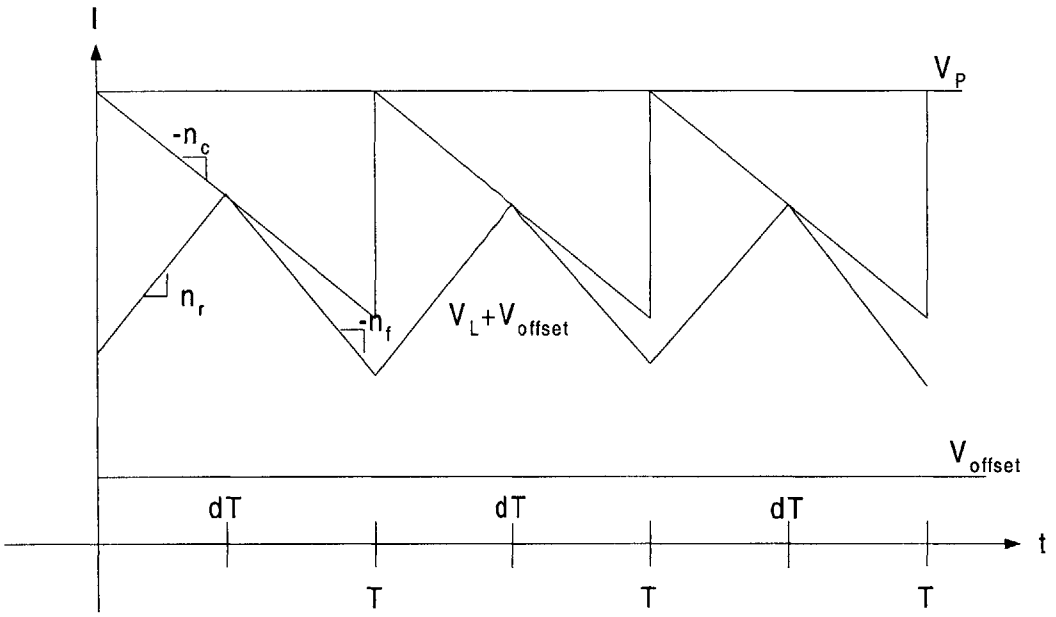

Figure 3-6: Inner control loop inductor current waveforms represented as voltages with the control IC.

Linearizing the above equation and noting that in steady state, $N_R D = N_F(1-D)$ and $V_L = V_P - V_{OFFSET} - (N_C - 0.5N_R)DT$, the small signal equation for the inductor current is:

$$\tilde{v}_l = \tilde{v}_p - \tilde{v}_{offset} - N_C T\tilde{d} - 0.5D^2 T\tilde{n}_r - 0.5(1-D)^2 T\tilde{n}_f \tag{3-12}$$

Substituting $\frac{A_L}{L_O}(\tilde{v}_{in} - \tilde{v}_c)$ for $\tilde{n}_r$ and $\frac{A_L}{L_O}\tilde{v}_c$ for $\tilde{n}_f$, the above equation reduces to:

$$\tilde{v}_l = \tilde{v}_p - \tilde{v}_{offset} - N_C T\tilde{d} - \frac{A_L D^2 T}{2L_O}\tilde{v}_{in} - \frac{A_L(1-2D)T}{2L_O}\tilde{v}_c \tag{3-13}$$

The final step is to eliminate the duty ratio. This is because the duty ratio is not a control variable, but is indirectly set by the inductor current rising and crossing the reference current threshold. The above equation is solved for the small signal duty ratio:

$$\tilde{d} = \frac{\tilde{v}_p - \tilde{v}_{offset} - \tilde{v}_l}{N_C T} - \frac{A_L D^2}{2N_C L_O}\tilde{v}_{in} - \frac{A_L(1-2D)}{2N_C L_O}\tilde{v}_c \tag{3-14}$$

The duty ratio equation is substituted into small signal state space equation for the inductor current and the resulting state space dynamics for the output voltage and inductor current are:

$$\begin{bmatrix} s\tilde{v}_c \\ s\tilde{i}_l \end{bmatrix} = \begin{bmatrix} 0 & 1/C_O \\ -\rho & -\beta \end{bmatrix} \begin{bmatrix} \tilde{v}_c \\ \tilde{i}_l \end{bmatrix} + \begin{bmatrix} 0 & -1/C_O & 0 \\ \gamma & 0 & \delta \end{bmatrix} \begin{bmatrix} \tilde{v}_{in} \\ \tilde{i}_{out} \\ \tilde{v}_p - \tilde{v}_{offset} \end{bmatrix} \tag{3-15}$$

where ρ, β, γ, and δ are defined as:

$$\rho = \frac{1}{L_O}\left(1 + \frac{(1-2D)A_L V_{IN}}{2N_C L_O}\right) \tag{3-16}$$

$$\beta = \frac{1}{L_O}\left(r_x + \frac{A_L V_{IN}}{N_C T}\right) \tag{3-17}$$

$$\gamma = \frac{D}{L_O}\left(1 - \frac{A_L D V_{IN}}{2N_C L_O}\right) \tag{3-18}$$

$$\delta = \frac{1}{L_O}\left(\frac{V_{IN}}{N_C T}\right) \tag{3-19}$$

In the transfer functions from v_p, i_{out}, and v_{in}, to v_c, β represents the amount of damping. The maximum value of the average series resistance, r_x, is 1 Ω. This occurs when the Si1555DL MOSFETs and an inductor with R_{DC} of 0.3 Ω are used and the duty ratio is at its highest at 0.5. With an N_C of 9×10^4 V/s and A_L of 0.5625 Ω, $\frac{A_L V_{IN}}{N_C T}$ is minimum at 27.2 when the battery voltage is 2.9 V. The term, $\frac{A_L V_{IN}}{N_C T}$, is much larger than r_x even in the worst-case condition. Going a step further, suppose the DSP chip could be modeled as a resistive load, R_{DSP}, equal to 1.2 V divided by I_{out}. This would lead to an additional damping term of $\frac{1}{C_O R_{DSP}}$, which reaches a maximum at 300 mA of output current. For a 10 μH inductor and a 10 μF capacitor, the magnitudes of the damping terms are:

$$\frac{1}{L_O}\left(r_x + \frac{A_L V_{IN}}{N_C T}\right) + \frac{1}{C_O R_{DSP}} = (1 + 27.2 + .25)\times 10^5 \tag{3-20}$$

The damping due to the average series resistance, r_x, and the output resistance, R_{DSP}, is negligible compared to the damping provided by the inner current loop term $\frac{A_L V_{IN}}{N_C T}$ even in the worst case condition. Nominally, the current loop term is much larger than r_x or R_{DSP} (usually by a factor of at least 30). Thus, it can be concluded that variations in the resistances of the MOSFETs, inductor and sense resistor, as well as the load resistance of the DSP do not significantly affect the input-output transfer functions of the converter. With that approximation, the transfer functions for the buck converter are:

$$\frac{\tilde{v}_c}{\tilde{v}_p}(s) = \frac{\tilde{v}_c}{-\tilde{v}_{offset}}(s) = \frac{\dfrac{2fL_O V_{IN}}{2N_C L_O + (1-2D)A_L V_{IN}}}{\dfrac{2N_C L_O (L_O C_O)}{2N_C L_O + (1-2D)A_L V_{IN}} s^2 + \dfrac{2fA_L V_{IN}(L_O C_O)}{2N_C L_O + (1-2D)A_L V_{IN}} s + 1} \tag{3-21}$$

$$\frac{\tilde{v}_c}{\tilde{v}_{in}}(s) = \frac{D\dfrac{2N_C L_O - A_L D V_{IN}}{2N_C L_O + (1-2D)A_L V_{IN}}}{\dfrac{2N_C L_O (L_O C_O)}{2N_C L_O + (1-2D)A_L V_{IN}} s^2 + \dfrac{2fA_L V_{IN}(L_O C_O)}{2N_C L_O + (1-2D)A_L V_{IN}} s + 1} \tag{3-22}$$

$$\frac{\tilde{v}_c}{\tilde{i}_{out}}(s) = \frac{-A_L \dfrac{2L_O f V_{IN}}{2N_C L_O + (1-2D)A_L V_{IN}}\left(\dfrac{N_C L_O}{A_L f V_{IN}} s + 1\right)}{\dfrac{2N_C L_O (L_O C_O)}{2N_C L_O + (1-2D)A_L V_{IN}} s^2 + \dfrac{2A_L f V_{IN}(L_O C_O)}{2N_C L_O + (1-2D)A_L V_{IN}} s + 1} \tag{3-23}$$

The poles of the transfer functions are at:

$$s = \frac{A_L f V_{IN}}{2N_C L_O}\left(-1 \pm \sqrt{1 - \frac{2N_C(2N_C L_O + (1-2D)A_L V_{IN})}{(A_L f V_{IN})^2 C_O}}\right) \tag{3-24}$$

The term under the radical is close to unity. For V_{IN} = 2.9 V, L_O = 10 µH and C_O = 10 µF:

$$\frac{2N_C(2N_C L_O + (1-2D)A_L V_{IN})}{(A_L f V_{IN})^2 C_O} = 0.00626 \tag{3-25}$$

Since the term subtracted from one under the radical is small, the following approximation can be made:

$$\sqrt{1-\frac{2N_C\left(2N_CL_O+(1-2D)A_LV_{IN}\right)}{\left(A_LfV_{IN}\right)^2C_O}}\approx 1-\frac{N_C\left(2N_CL_O+(1-2D)A_LV_{IN}\right)}{\left(A_LfV_{IN}\right)^2C_O} \tag{3-26}$$

The result is a dominant low frequency pole at:

$$s=\frac{1}{\tau_D}=-\frac{\left(2N_CL_O+(1-2D)A_LV_{IN}\right)}{2A_LfV_{IN}L_OC_O} \tag{3-27}$$

and a high frequency pole at:

$$s=\frac{1}{\tau_H}=-\frac{A_LfV_{IN}}{2N_CL_O}\left(2-\frac{N_C\left(2N_CL_O+(1-2D)A_LV_{IN}\right)}{\left(A_LfV_{IN}\right)^2C_O}\right)\approx-\frac{A_LfV_{IN}}{N_CL_O} \tag{3-28}$$

Note that in the transfer function from i_{out} to v_c there is a high frequency zero located at $s = -\frac{A_LfV_{IN}}{N_CL_O}$. This makes the dynamics from i_{out} to v_c first order.

An important result is obtained from these equations. The DC gain of the transfer function from v_p to v_c and A_Li_{out} to v_c is:

$$\frac{\tilde{v}_c}{\tilde{v}_p}(0)=\frac{\tilde{v}_c}{A_L\tilde{i}_{out}}(0)=\frac{2L_OfV_{IN}}{\left(2N_CL_O+(1-2D)A_LV_{IN}\right)} \tag{3-29}$$

To get the gain-bandwidth product (GBW), the DC gain is divided by τ_D:

$$GBW=\frac{2L_OfV_{IN}}{\left(2N_CL_O+(1-2D)A_LV_{IN}\right)}\times\frac{\left(2N_CL_O+(1-2D)A_LV_{IN}\right)}{2A_LfV_{IN}L_OC_O}=\frac{1}{A_LC_O} \tag{3-30}$$

The gain-bandwidth product only depends on the output filter capacitor and the total current gain. A_L has a tolerance of 1% while C_O can vary by ±20%. Figure 3-7 shows the variation in the transfer function from v_p to v_c due to the tolerance in C_O. The change in the unity gain crossover frequency is small and reduces the phase by one degree at crossover. Fortunately, GBW is independent of the input voltage, the size of the output filter inductor the slope of the compensation ramp. The input voltage varies from 2.9 to 5.1 V, while the inductor can vary from 4.7 μH to 10 μH with a ±20% tolerance. N_C could have been chosen to be anywhere from 5.6×10^4

V/s to 1.8×10^5 V/s. Figure 3-8 shows how the transfer function from v_p to v_c varies for different combinations of V_{IN}, L_O and N_C. The high frequency dynamics, as expected, are unaffected by the variation in the location of the dominant pole due to variations in V_{IN}, L_O and N_C.

The high frequency pole can vary by an order of magnitude. If V_{IN} = 2.9 V and L_O = 12 μH the high frequency pole is at its minimum value of 2.27×10^6 rad/sec. The maximum value of the high frequency pole is 1.27×10^7 rad/sec, which occurs when V_{IN} = 5.1 V and L_O = 3.76 μH. If 80 kHz of bandwidth is needed for the control system is needed then the unity gain crossover frequency will be 5×10^5 rad/sec. The high frequency pole can add up 12.42° of phase if it located at 2.27×10^6 rad/sec.

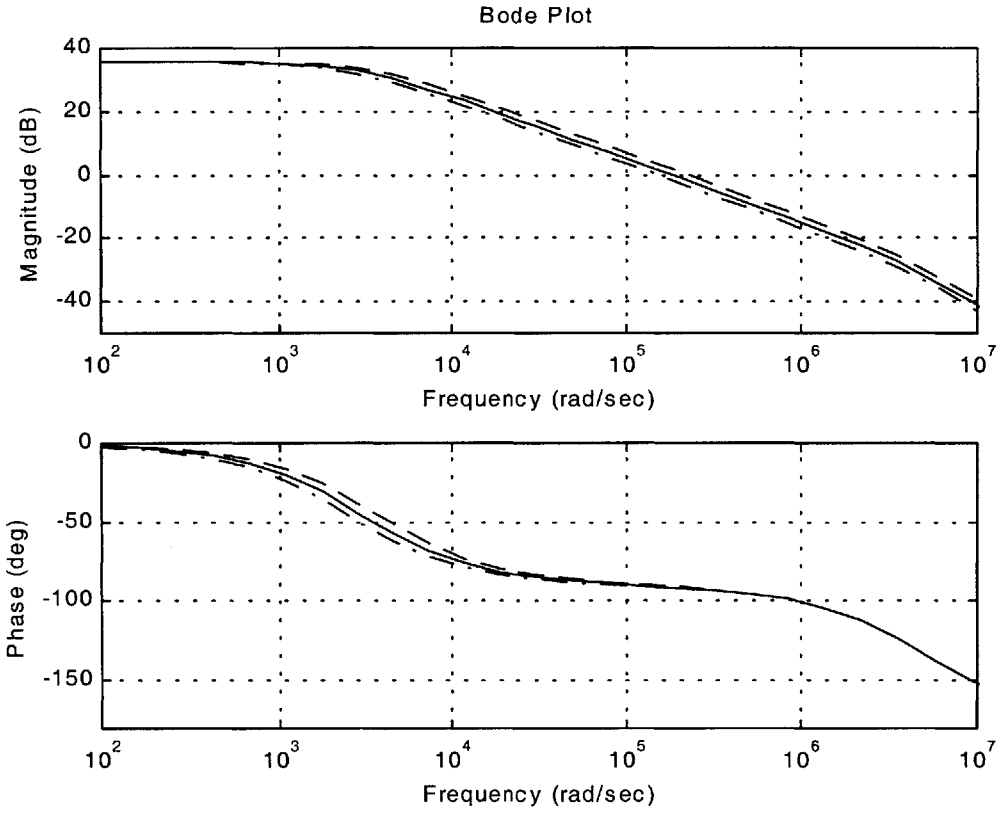

Figure 3-7: Bode plot of the transfer function from v_p to v_c for C_O equal to 10 μF (solid), 8 μF (dashed) and 12 μF (dashed-dot). The variation in C_O due to its tolerance changes the gain-bandwidth product of the transfer function.

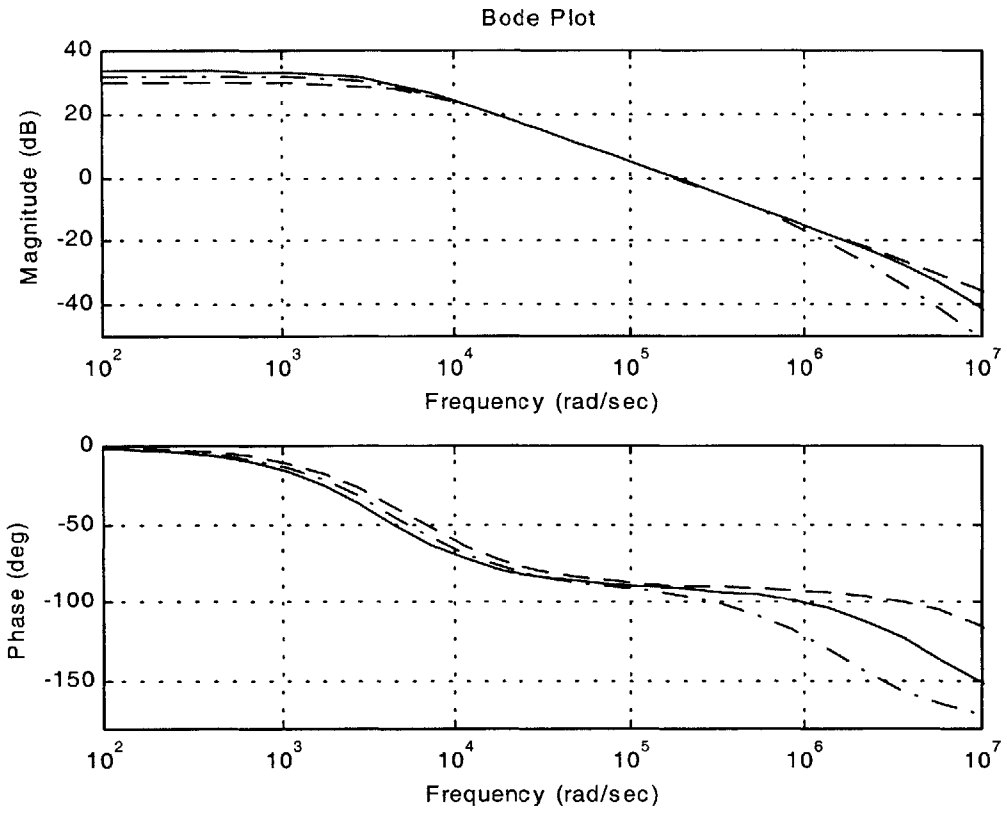

Figure 3-8: Bode plot of transfer function from v_p to v_c for different combinations of V_{IN}, N_C and L_O. Solid line is V_{IN} = 3.6 V, $N_C = 9\times10^4$ V/s and L_O = 6.8 μH. Dashed line is V_{IN} = 5.1 V, $N_C = 5.6\times10^4$ V/s and L_O = 3.76 μH. Dashed-dot line is V_{IN} = 2.9 V, $N_C = 10^5$ V/s and L_O = 12 μH.

3.4 Compensator Design

The block diagram for the closed loop converter is shown in Figure 3-9. The minor loop has been incorporated into the transfer functions leaving only the outer voltage control loop. Variations in the output current, input voltage and offset voltage can be thought of as disturbances acting on the closed loop buck converter. The job of the compensator $G_c(s)$ is to maintain the output voltage at 1.2 volts in the presence of rapid variations in output current and input voltage.

Figure 3-10 shows the compensation section of the current-mode architecture. The reference voltage, v_p, is:

$$v_P = v_{ref} + G_c(s)(v_{ref} - v_{out}) \tag{3-31}$$

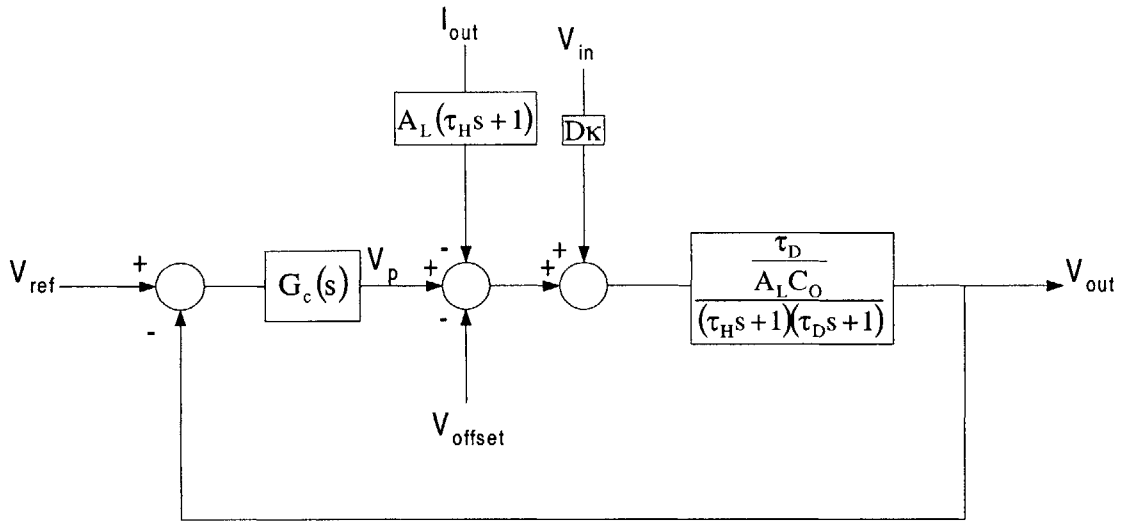

Figure 3-9: Closed loop block diagram of buck converter.

where $G_c(s)$ will be a lag compensator of the form:

$$G_c(s)=G_o\frac{(\tau_z s+1)}{(\tau_p s+1)}=\left(\frac{R_{comp3}}{R_{comp1}}\right)\frac{(R_{comp2}C_{comp})s+1}{(R_{comp3}+R_{comp2})C_{comp}s+1} \tag{3-32}$$

The sensed inductor current has a DC bias v_{bias}. The bias comes from a DC current source tied to the output resistor, R_2, of the current sense amplifier. The bias voltage is equal to 250 mV. The total offset voltage, v_{ref}-v_{bias}, is positive. In Figure 3-9, the offset voltage was assumed to be negative and there is a minus sign at the summing junction. However, since the offset voltage is positive, it will be added to v_p.

The steady-state error requirement is for the output voltage to be within 1% of the 1.2 V reference voltage. From Figure 3-9, the DC output voltage is:

$$v_{out}=\frac{G_o\frac{\tau_D}{A_L C_O}}{1+G_o\frac{\tau_D}{A_L C_O}}v_{ref}+\frac{DK\frac{\tau_D}{A_L C_O}}{1+G_o\frac{\tau_D}{A_L C_O}}v_{in}+\frac{\frac{\tau_D}{A_L C_O}}{1+G_o\frac{\tau_D}{A_L C_O}}(v_{offset}-A_L i_{out}) \tag{3-33}$$

where $K=\frac{2N_C L_O - A_L D V_{IN}}{2L_O f V_{IN}}$. The DC gain of the converter, $\frac{\tau_D}{A_L C_O}$, is greater than 20.

Consequently, $G_o \frac{\tau_D}{A_L C_O} >> 1$ and the above equation reduces to:

$$v_{out} = v_{ref} + \frac{1}{G_o}(v_{offset} + \kappa D v_{in} - A_L i_{out}) \tag{3-34}$$

The term $\kappa D v_{in}$ is much smaller than the other two terms and can be ignored. The maximum DC error occurs when the output current is 30 mA. The maximum error voltage is:

$$v_{error} = \frac{1}{G_o}(0.95 - 0.0169)V = \frac{1}{G_o}(0.933)V \tag{3-35}$$

G_o will be set to 100 so that the error voltage is at most 9.33 mV, which translates to a steady state error of 0.77 %. The steady state error improves as output current increases and reaching a minimum of 7.81 V or 0.65%.

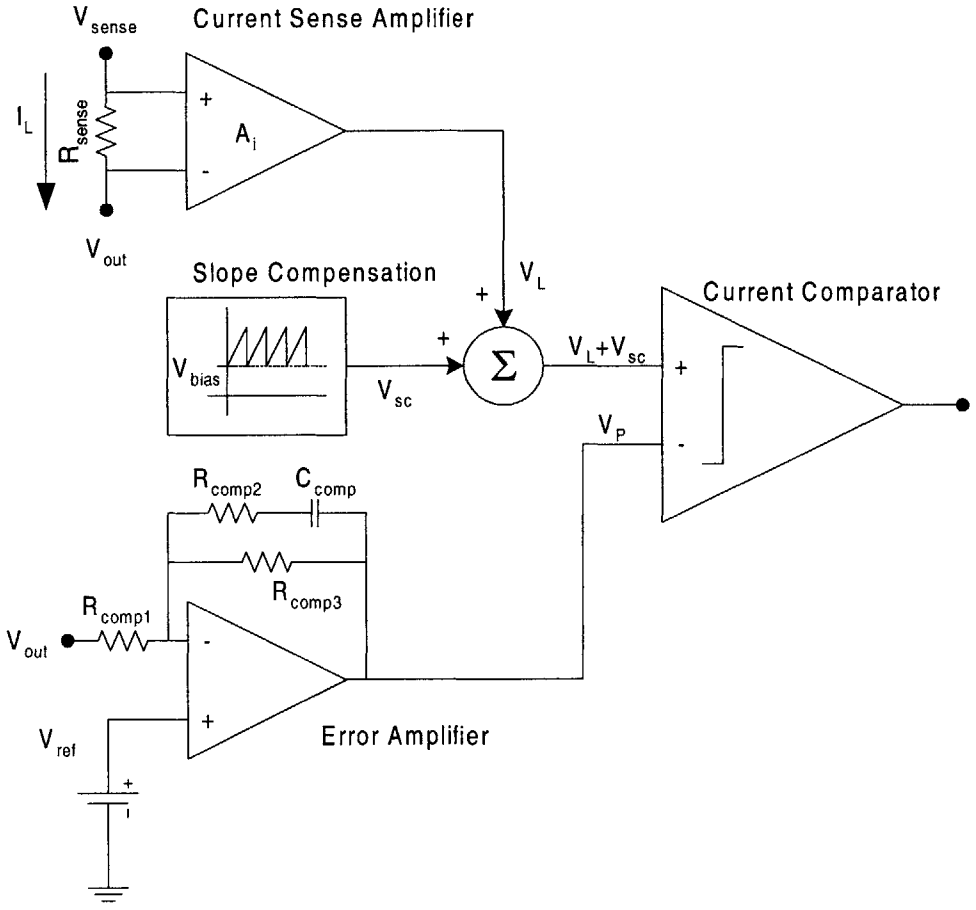

Figure 3-10: Compensation section of current-mode control architecture.

The next requirement to consider is the transient output voltage response to a step change in the input voltage. When the radio's power amplifier draws power to transmit data, the battery voltage may drop by 600 mV in 4 μsec. This voltage drop lasts for 177 μsec. The input filter that is used to attenuate the ripple current that the battery sees also attenuates the voltage pulse from the battery in the same way the output filter reduces the ripple voltage from the power stage. Therefore the change in V_{in} is very small. A variation in V_{in} causes little change in the output voltage. To see this, the closed loop transfer function from input voltage to output voltage is:

$$v_{out} = \frac{P(s)}{1 + G_c(s)P(s)}\left(\frac{2N_C L_O - A_L D V_{IN}}{2L_O f V_{IN}}\right) Dv_{in} \tag{3-36}$$

where

$$P(s) = \frac{\frac{\tau_D}{A_L C_O}}{(\tau_H s + 1)(\tau_D s + 1)} \tag{3-37}$$

The term $\frac{2N_C L_O - A_L D V_{IN}}{2L_O f V_{IN}}$ has order of magnitude of $\sim 10^{-3}$ or –60 dB. Even without the input filter, the 600 mV step changes would produce a very small change in output voltage.

The rapid changes in output current causes the largest errors in the output voltage. The compensator is required to allow no more than a 5% overshoot for a step in current from 50 μA to 300 mA in 10 μsec. The output voltage must settle back to within 1% of 1.2 V in less than 20 μsec from the beginning of the current step. With the outer voltage loop in Figure 3-9 open, the transfer function from i_{out} to v_{out} is:

$$v_{out} = \frac{\frac{\tau_D}{C_O}}{(\tau_D s + 1)} i_{out} \tag{3-38}$$

with the high frequency zero of the current gain canceling the high frequency pole of the converter. The high frequency zero comes from the limit on how fast the current can change due to the size of the inductor. The poles and zeros of this transfer function are shown in the s-plane in Figure 3-11, along with the location of the compensator pole and zero.

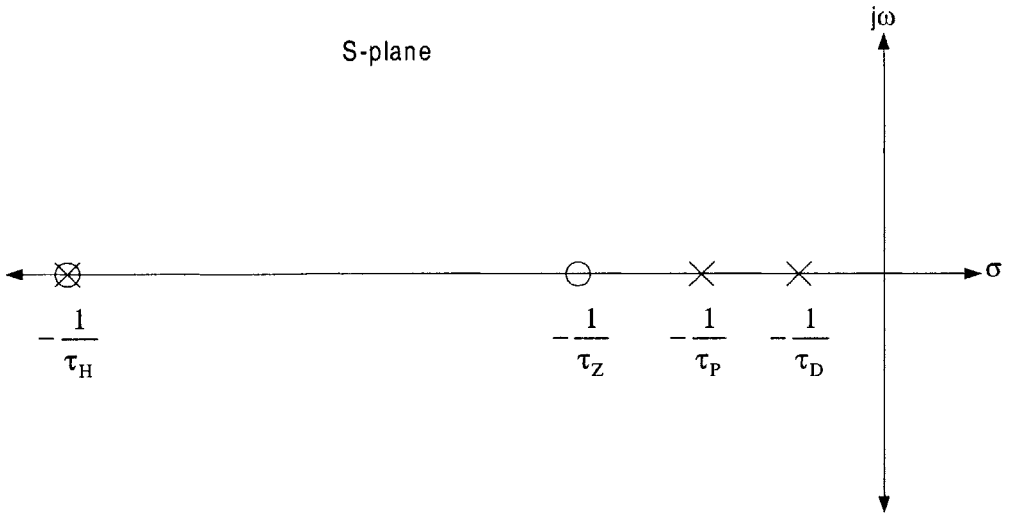

Figure 3-11: Pole and zero locations for $\frac{v_{out}}{i_{out}}(s)$ and $G_c(s)$ with the outer voltage loop open. $\frac{v_{out}}{i_{out}}(s)$ has a dominant pole at $s = -1/\tau_D$ and a pole-zero cancellation at $s = -1/\tau_H$. The pole and zero of $G_c(s)$ are at $s = -1/\tau_P$ and $s = -1/\tau_Z$, respectively.

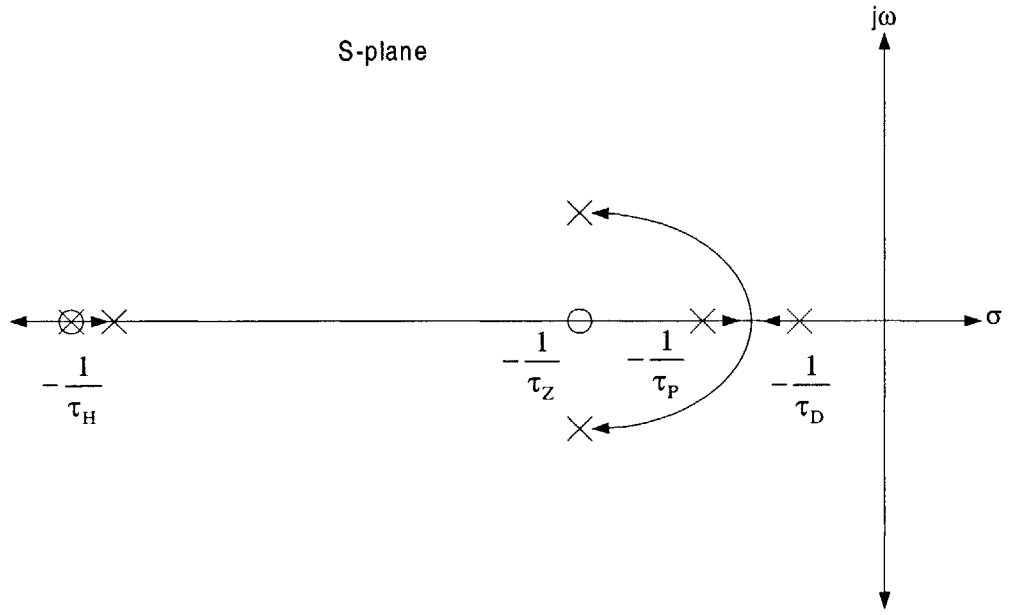

Figure 3-12: Root locus of $\frac{v_{out}}{i_{out}}(s)$ when the outer voltage loop is closed. The dominant pole of the converter and the compensator pole become complex poles and move toward the compensator zero. The high frequency pole moves inward so that there is no longer a pole-zero cancellation.

When the outer voltage loop is closed, the DC gain of the compensator pushes the converter's dominant pole and the compensator pole past the compensator's zero (Figure 3-12). Following the rules of root locus, the high frequency pole moves inwards to a lower frequency so that there is no longer a pole-zero cancellation. However, because the DC of the compensator is only 100, the pole moves only a few hundred kilo-rad/sec below the high frequency zero. The high frequency pole and zero add only a few degrees of phase if the unity-gain crossover frequency is 5×10^5 rad/sec. Since the high frequency pole at $s = -1/\tau_H$ does not affect have much affect on loop gain it will be ignored. The closed loop transfer function between i_{out} and v_{out} is now:

$$v_{out} = \frac{-\frac{\frac{\tau_D}{C_O}}{(\tau_D s+1)}}{1+G_o\frac{(\tau_z s+1)}{(\tau_p s+1)}\frac{\frac{\tau_D}{A_L C_O}}{(\tau_D s+1)}} i_{out} = \frac{-\frac{\tau_D}{C_O}(\tau_p s+1)}{\tau_p\tau_D s^2+\left(\tau_D+\tau_p+\frac{G_o\tau_D}{A_L C_O}\tau_z\right)s+1+\frac{G_o\tau_D}{A_L C_O}} i_{out} \quad (3\text{-}39)$$

Dividing through by $\frac{G_o\tau_D}{A_L C_O}$, the above equation becomes:

$$v_{out} = \frac{-(\tau_p s+1)}{\frac{A_L C_O}{G_o}\tau_p s^2+\tau_z s+1}\left(\frac{A_L}{G_o}\right) i_{out} \quad (3\text{-}40)$$

The approximation $\left(1+\frac{\tau_p}{\tau_D}\right)\frac{A_L C_O}{G_o}+\tau_z \approx \tau_z$ is used since $\frac{A_L C_O}{G_o}$ is 5.625×10^{-8} sec. and τ_z is $\sim10^{-6}$ sec.

Before choosing the location of the τ_z and τ_p it is important to consider tolerances in the compensator. The compensator is an op-amp with a resistor-capacitor network from the output back to the negative input of the op-amp. The compensator pole and zeros come from the inverse of the product of the resistors and capacitors used in the circuit. For the CMOS process used, the integrated resistors have a tolerance of ±20% while the capacitors have a tolerance of ±30%. This means that $1/\tau_p$ and $1/\tau_p$ can vary from 64% to 178% of their nominal value. However, the resistors can be matched to ±1% of each other so that if τ_z is 178% of its nominal value, so is τ_p.

The current load step consists of a 300 mA jump in 9 μsec. It can be thought of as a disturbance concentrated at a frequency of $\omega = (9\ \mu\text{sec})^{-1} = 1.1\times10^5$ rad/sec. The bandwidth of the closed loop converter should be roughly three times this frequency so that there is enough gain in the feedback loop to reduce the overshoot in output voltage. Since the natural frequency, ω_n, of the close loop system is closely related to its bandwidth,

$$\frac{1}{\omega_n^2} = \frac{A_L C_O}{G_o}\tau_p \approx \frac{1}{\left(3\times1.11\times10^5\right)^2} \tag{3-41}$$

This requires that τ_p be $\sim10^{-4}$ sec. To determine τ_z, the damping ratio, ζ, is set to 0.69. This corresponds to a 5% overshoot in the output voltage. $\tau_z = \frac{2\zeta}{\omega_n} = 4\times10^{-6}$ sec. These pole and zero locations are used as a starting point to design a compensator that satisfies the transient requirements even when the pole and zero can vary from 64% to 178% of their nominal value. A compensator that satisfies all the control requirements is:

$$G_c(s) = 100\frac{\left(3.6\times10^{-6}s+1\right)}{\left(1.6\times10^{-4}s+1\right)} \tag{3-42}$$

Figure 3-13 shows the output voltage response to the output current step using this compensator. Also shown is the variation in the voltage response as the compensator pole and zero move from 64% to 178% of their nominal value. Regardless of the exact location of the pole and zero, the peak overshoot is less than 5% and the settling time is with 20 μsec as desired. The bandwidth provided by $G_c(s)$ is 80 kHz.

Figure 3-14 shows the output voltage response to the step change in input voltage if no input filter is used. As previously stated, the rapid variations in the input voltage produce very small changes in the output voltage. The overshoot in the output voltage is only 600 μV above the steady state output voltage.

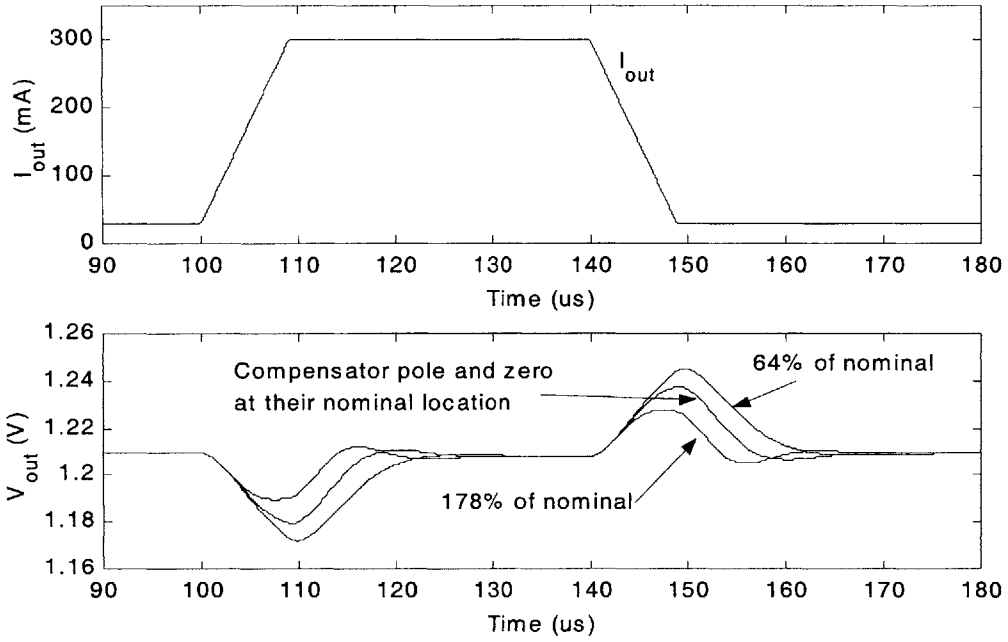

Figure 3-13: Output voltage response to a step change in current. (Top) Output current pulse. (Bottom) Output voltage response with the compensator pole and zero at their nominal value 64% of their nominal value and 178% of their nominal value.

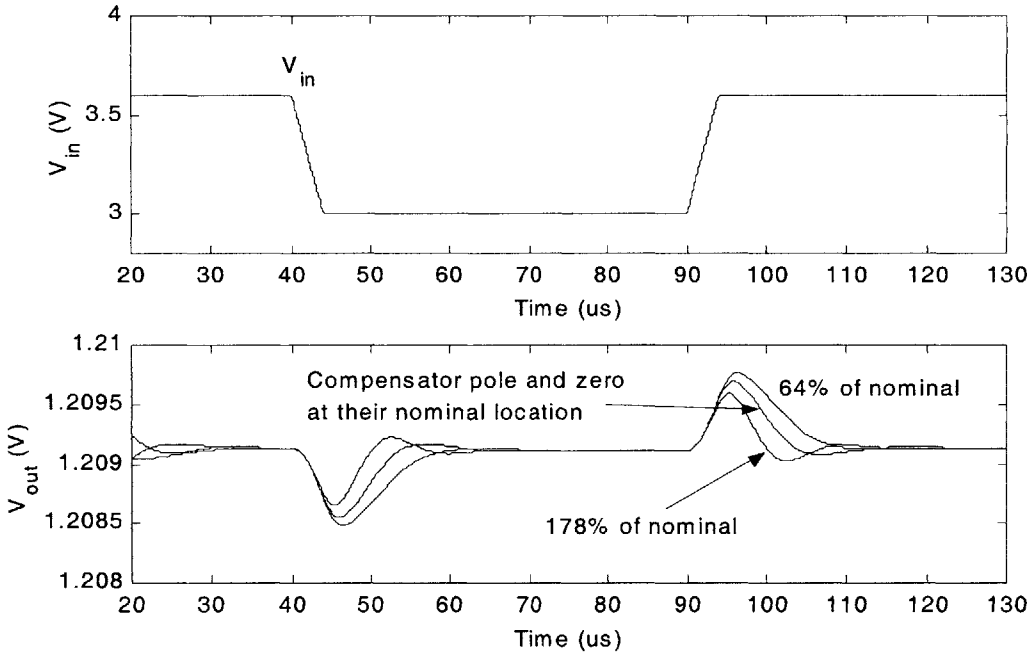

Figure 3-14: Output voltage response to a step change in input voltage. (Top) Input voltage pulse. (Bottom) Output voltage response with the compensator pole and zero at their nominal value, 64% of their nominal value and 178% of their nominal value.

3.5 *Input filter and closed loop stability*

3.5.1 Interaction between closed loop converter and input filter

The closed loop buck converter in Figure 3-15 can become unstable when an input filter is used. Under feedback control, the converter delivers constant power to the DSP. If the input voltage decreases, then the current into the converter must increase to maintain the power delivered to the DSP. Since a negative change in input voltage creates a positive change in input current, the input impedance of the closed loop converter is negative. In Figure 3-16 the thevenin equivalent circuit of the battery and input filter's output impedance, Z_s, drives the converter modeled as its input impedance, $-Z_{in}$. The input voltage to the converter is:

$$V_{in} = \frac{-Z_{in}}{-Z_{in}+Z_s} V_{bat} = \frac{1}{1-Z_s/Z_{in}} V_{bat} \tag{3-43}$$

The closed loop buck converter will become unstable when $\frac{Z_s}{Z_{in}} = 1$. Therefore, in order to maintain stability, the magnitude of the input filter's output impedance, $|Z_s|$, must be much smaller than the input impedance of the closed loop converter [11]. As a starting point $|Z_s|$ should always be made smaller than the magnitude of the low frequency small signal impedance:

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{V_{out}/D}{-DI_{out}} = -\frac{V_{out}}{D^2 I_{out}} \tag{3-44}$$

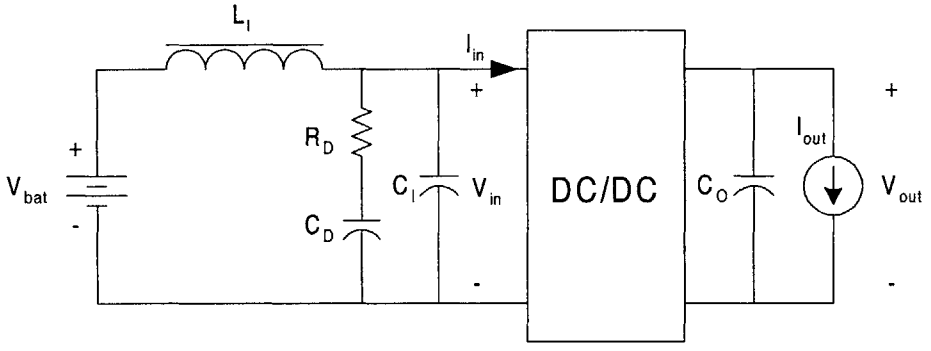

Figure 3-15: Battery and input filter driving a DC/DC converter. The block labeled DC/DC contains the power stage, power inductor and control circuitry.

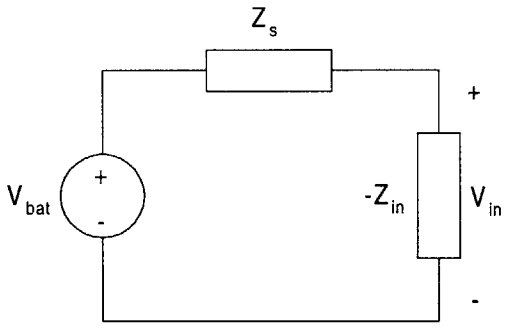

Figure 3-16: Thevenin equivalent of battery and input filter driving the closed loop buck converter modeled as a negative impedance.

3.5.2 Input impedance of a current-mode controlled buck converter

The input impedance of the closed loop converter is found in the same manner as the small signal dynamics in section 3.1. The current into the converter's power stage is equal to the inductor current when the PMOS pass transistor is on. This can be represented as the product of the inductor current i_L and switching function q(t):

$$i_{IN}(t) = q(t)i_L(t) \tag{3-45}$$

The average current over one switching cycle is:

$$\bar{i}_{IN}(t) = \overline{q(t)i_L(t)} \approx d(t)\bar{i}_L(t) \tag{3-46}$$

This equation is nonlinear since it is the product of two time varying functions. To arrive at the incremental input impedance, the average input current is linearized. Noting that $I_{IN} = DI_L$, the current into the converter is:

$$\tilde{i}_{in} = I_L\tilde{d} + D\tilde{i}_l \tag{3-47}$$

The small signal inductor current $\tilde{i}_l$ is equal to $\tilde{i}_{out} + C_O s\tilde{v}_c$. However, when determining the input impedance, all exogenous variables are set to zero. Therefore $\tilde{i}_l$ equals $C_O s\tilde{v}_c$ and the input current is now:

$$\tilde{i}_{in} = I_{OUT}\tilde{d} + (DC_O s)\tilde{v}_c \tag{3-48}$$

In section 3.3, the small signal duty ratio was found to be:

$$\tilde{d} = \frac{\tilde{v}_p - \tilde{v}_{offset} - \tilde{v}_l}{N_C T} - \frac{A_L D^2}{2N_C L_O}\tilde{v}_{in} - \frac{A_L(1-2D)}{2N_C L_O}\tilde{v}_c \tag{3-49}$$

Since all exogenous variables are set to zero, there is no small signal reference or offset voltage. The control variable, $\tilde{v}_p$, and capacitor voltage, $\tilde{v}_c$, equal $\tilde{v}_{out}$. Substituting for the small signal duty ratio, the following equation for the input current is arrived at:

$$\tilde{i}_{in} = -\left[\left(\frac{A_L I_{OUT}}{N_C T} - D\right)C_O s + \frac{(1-2D)A_L I_{OUT}}{2N_C L_O} + \frac{I_{OUT} G_c(s)}{N_C T}\right]\tilde{v}_{out} - \frac{A_L I_{OUT} D^2}{2N_C L_O}\tilde{v}_{in} \tag{3-50}$$

To eliminate the small signal output voltage, remember that when the outer voltage loop is closed

$$\frac{\tilde{v}_{out}}{\tilde{v}_{in}}(s) = \frac{D\left(\frac{2N_C L_O - A_L D V_{IN}}{2L_O f V_{IN}}\right)\frac{\tau_D}{A_L C_O}}{(\tau_H s + 1)(\tau_D s + 1) + \frac{\tau_D}{A_L C_O}G_c(s)} \tag{3-51}$$

By eliminating the small signal output voltage the inverse of the input impedance of the converter is obtained:

$$\frac{1}{Z_{in}} = \frac{\tilde{i}_{in}}{\tilde{v}_{in}} = -\frac{I_{OUT} D^2}{V_{OUT}}\left[\frac{\left[\left(A_L - \frac{D N_C T}{I_{OUT}}\right)C_O s + G_c(s)\right]\frac{\tau_D}{A_L C_O}}{(\tau_H s + 1)(\tau_D s + 1) + \frac{\tau_D}{A_L C_O}G_c(s)}\left(1 - \frac{A_L V_{OUT}}{2N_C L_O}\right) + \frac{A_L V_{OUT}}{2N_C L_O}\right] \tag{3-52}$$

At low frequencies, the compensator gain is large and the input impedance reduces to:

$$Z_{in}(0) \approx -\frac{V_{OUT}}{I_{OUT} D^2} \tag{3-53}$$

which is exactly what was obtained in the section 3.5.1. At high frequencies the $\tau_H \tau_D s^2$ term dominates making the first term in the bracket small and increasing the input impedance to:

$$Z_{in}(\infty) \approx -\frac{2N_C L_O}{A_L I_{OUT} D^2} \tag{3-54}$$

Note, however that the small signal impedance is valid only up to one-sixth of the switching frequency, or 250 kHz.

3.5.3 Closed loop stability with an input filter

Lowest value of the input impedance of the converter occurs when the input voltage is 2.9 V (D = 0.5), the inductance is 3.76 μH and the DSP is drawing 300 mA of current. The magnitude of the input impedance is 16 Ω at frequencies from 0 to 250 kHz. This is so because coincidentally,

$$\frac{2N_C L_O}{A_L} = \frac{2\left(9\times10^4\,V/s\right)\left(3.76\times10^{-6}\,H\right)}{0.5625\Omega} = 1.2V = V_{OUT} \tag{3-55}$$

The output impedance of the input filter, Z_s, must be less than 10.6 Ω from 0 to 250 kHz. The output impedance for the input filter in Figure 3-15 is:

$$Z_s = (r_{DC} + L_I s) \| \frac{(R_D C_D s + 1)}{C_D s} \| \frac{1}{C_I s} \tag{3-56}$$

The 0.16 Ω resistance of the 1 μH input filter inductor is the only parasitic element included in the impedance equation. The SRF of L_I is 100 MHz so the inter-winding capacitance has no effect on the impedance at frequencies of 250 kHz or less. The self-resonance frequencies of the 0.47 μF, 1 μF and 2.2 μF input filters capacitors and 10 μF damping capacitor are all greater than 2 MHz. Therefore, ESL of these capacitors produces a negligible effect on the impedance. Similarly, the ESR of the capacitors is ignored because they are much smaller than the impedance of the capacitors.

The magnitude of the output impedance of the input filter is shown for the three choices of input filter capacitor in Figure 3-17. Also shown is the minimum input impedance of the converter. Z_s is much smaller than Z_{in} by roughly an order of magnitude for all three input filter capacitors. The maximum of Z_s occurs at the input filter's resonance frequency and is equal to the damping resistor, R_D. The maximum value of R_D is 1.5 Ω when C_I equals 0.47 μF. Since the minimum of Z_{in} is 10.6 Ω the closed loop converter with the input filter from Chapter 2 is stable.

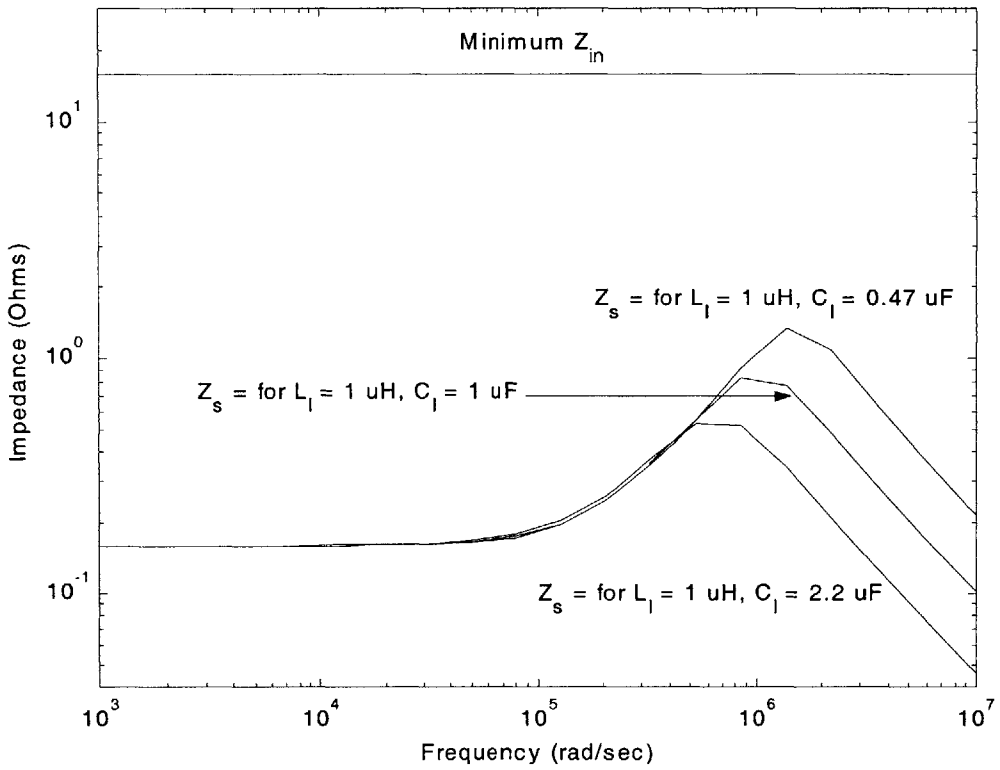

Figure 3-17: The magnitude of the output impedance of the input filter is plotted for different input filter capacitor values. Also shown is the magnitude of the input impedance of the current-mode controlled buck converter for V_{bat} = 2.9 V, L_O = 3.76 μH and I_{out} = 300 mA. The magnitude of Z_{in} is much larger than Z_s ensuring that the closed loop buck converter with the input filter is stable.

4 Control IC

4.1 Overview of the control IC

The control IC for the buck converter was designed using transistors from Taiwan Semiconductor Manufacturing Corporation's (TSMC) L46 0.25 μm CMOS process. The transistors used have a maximum drain to source voltage rating of 5 V. The minimum widths and lengths are 0.6 and 0.5 μm, respectively. Table 4.1 summarizes some of the properties of the CMOS transistors.

The control IC implements the current-mode control architecture presented in Chapter 3. The IC has three major sections: the compensation stage, the decision stage and the drive stage (Figure 4-1). The compensation stage is composed of the error amplifier, current sense amplifier and slope compensation circuit. These circuits implement the compensation for the voltage and current control loops, which regulate the output voltage of the buck converter. The decision to turn the power MOSFETs on or off is made in the decision stage, comprises of the current comparator, current limiter, clock and RS-latch. The drive stage takes the output of the decision stage and turns the power MOSFETS on and off and prevents both power MOSFETs from being on at the same time. It comprises of gate drives and a shoot-through protection circuit. The circuit for generating the bias currents for the IC is from Analog Devices and is considered proprietary material.

Table 4-1: Transistor properties for TSMC's L46 CMOS process

Property	NMOS transistor	PMOS transistor
$V_{threshold}$	0.9V @ $V_{bs} = 0$	1.2 V @ $V_{bs} = 0$
$\mu_i C_{ox}$	62 μA/V^2	30 μA/V^2
$V_{ds,max}$	5 V	5 V
W_{min}	0.6 μm	0.6 μm
L_{min}	0.5 μm	0.5 μm

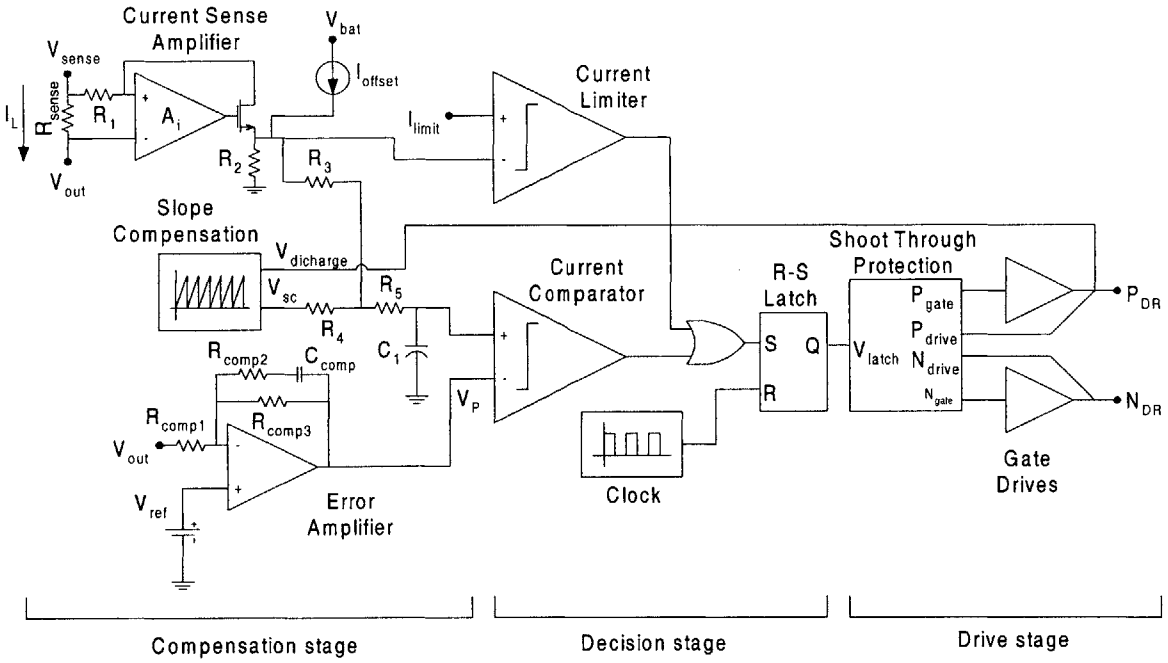

Figure 4-1: Control IC for the buck converter. The IC implements current-mode control and comprises of three stages: the compensation stage, the decision stage and the drive stage.

4.2 Compensation stage

4.2.1 Error amplifier

The error amplifier used in the control circuit is a folded cascode op-amp. The op-amp utilizes wide swing cascode current mirrors for maximum voltage swing [14]. There is only one gain stage in the op-amp, which makes it simple to compensate. The schematic of the error amplifier is shown in Figure 4-2.

PMOS devices are used for the input transistors Q_1 and Q_2 because the input voltages to the error amplifier not much higher than the threshold voltage of the NMOS transistors. The input voltages to error amplifier are V_{ref}, which is 1.2 V, and V_{out}, which can vary from 1.19 to 1.21 volts depending on the changes in the output current. The threshold voltage for the NMOS transistors is 0.9 V while the current source transistor for the input stage has a saturation voltage of about 0.2 V. The input transistors would barely turn on if they were NMOS transistors.

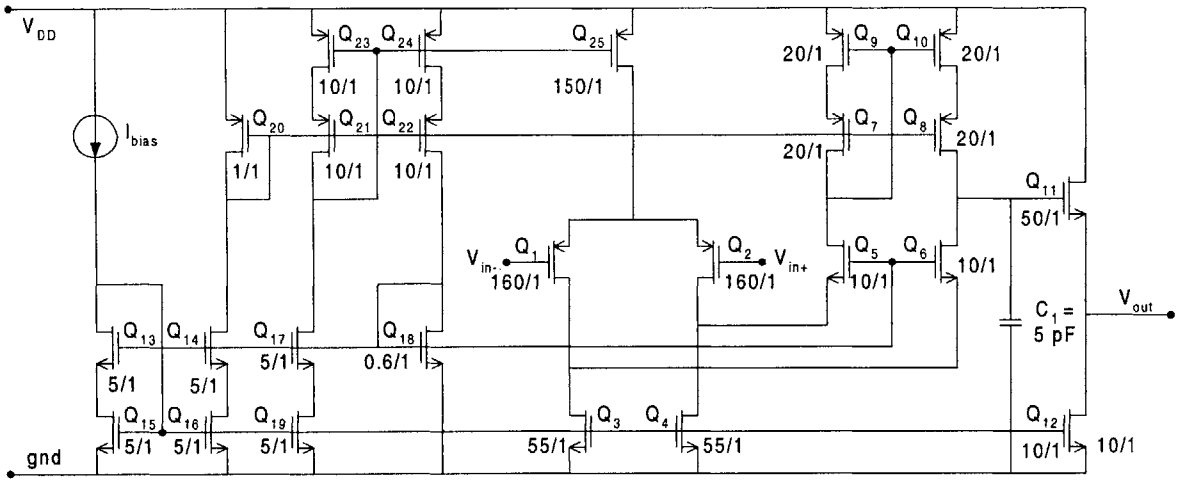

Figure 4-2: The error amplifier is a folded cascode op-amp utilizing a wide swing current mirror gain stage followed by a NMOS output buffer.

The transistors are sized according to the formula [14]:

$$\left(\frac{W}{L}\right)_i = \frac{2I_{Di}}{\mu_i C_{ox} V_{effi}^2} \tag{4-1}$$

W and L are the width and length of the transistor in μm, respectively. The minimum length of the transistors is chosen to be 1 μm to minimize short channel effects. I_{Di} is the drain current of the transistor. V_{effi} is the effective gate to source voltage and is defined as $V_{gs} - V_{ti}$, where V_{ti} is the threshold voltage of transistor Q_i. It is also the minimum drain to source voltage needed for the transistor to be in the saturation region of operation. To find the width of the transistors, V_{effi} is set to 0.15 V. The resulting width is then rounded to the nearest multiple of 5. With an I_{bias} of 5 μA, the widths of transistors Q_{13} and Q_{15} are 5 μm and have a V_{eff} of 0.18 V. Transistors Q_{14}, Q_{16}, Q_{17} and Q_{19} mirror the 5 μA bias current and are also set to 5 μm. The transistors Q_{21}-Q_{24} also have 5 μA of current through them. In order for V_{eff} of these transistors to be 0.18 volts, their widths are double to 10 μm because $\mu_i C_{ox}$ of PMOS transistors is half that of NMOS transistors (Table 4-1).

The transistor Q_{18} is sized so that the drain to source voltage of Q_{15} and Q_{16} is just above their saturation voltage, which is equal to $V_{gs15} - V_{tn}$ or V_{eff15}. The gate to source voltage of Q_{18} is:

$$V_{gs18} = V_{tn} + V_{eff18} > V_{tn} + V_{eff13} + V_{eff15} \quad (4\text{-}2)$$

The above equation simplifies to:

$$V_{eff18} > V_{eff13} + V_{eff15} = 2V_{eff15} \quad (4\text{-}3)$$

V_{eff18} should be at least twice as large as V_{eff15} so that Q_{15} never enters the linear region. Q18 is 0.6 μm wide so that V_{eff18} is 0.52 V and V_{ds15} is 0.26 V, well above the saturation voltage of 0.18 V. Q_{20} is similarly sized so that the drain to source voltages of Q_{23} and Q_{24} are above their saturation voltage of 0.18 V. Q_{20} is 1 μm wide so that the source to drain voltages of Q_{23} and Q_{24} are 0.2V.

The cascode amplifier is designed to consume 360 μW of power when $V_{DD} = V_{bat} = 3.6$ V. Therefore, transistors Q_3 and Q_4 have a drain current of 50 μA each. The sum of drain current through Q_1 and Q_6 flow into Q_3. The current through Q_1 is 40 μA and the current through Q_5 is 10 μA. Since the current through Q_7-Q_{10} is twice that of Q_{21}, their widths are increased to 20 μm each so that V_{eff} for the transistors is 0.18V. Similarly, the widths of Q_5 and Q_6 are also double that of Q_{13}. The current through Q_3 and Q_4 is mirrored from Q_{15}. Q_3 and Q_4 each have 50 μA so their widths should be ten times the width of Q_{15} or 50 μm. A 10:1 ratio in widths leads to matching errors so that in order for Q_3 and Q_4 to have 50 μA of drain current, their widths must be 55 μm. Q_{25} supplies a total of 80 μA to Q_1 and Q_2. The current through Q_{25} is mirrored from Q_{23}. This requires that Q_{25} be sixteen times wider than Q_{23}. The 16:1 width ratio also creates matching errors. A width 150 μm is need for Q_{25} to have a drain current of 80 μA.

The current through Q_1 is made four times larger than the current through Q_5. The gain of the folded cascode op-amp is on the order of $\frac{1}{2}g_{m1}r_{ds5}^2$. The transconductance of a MOSFET is proportional to the square root of the drain current through the transistor while the drain to source resistance is inversely proportional to the drain current. By making the current through Q_1 much larger than that of Q_6, the transconductance of Q_1 and the drain to source resistance of Q_6 are both increased. This makes the DC gain of the cascode amplifier 77.1 dB.

The output buffer has 10 μA of quiescent current through it. Since the bias current is mirrored from Q_{15}, the Q_{12} is made 10 μm wide. The width of the buffer transistor, Q_{11}, is made wide (50 μm) to increase it g_m. Increasing g_m reduces the output impedance of the op-amp so that it can drive resistive loads. The gain of the output buffer is:

$$A_{buffer} = \frac{g_{m11}}{g_{m11} + g_{s11}} = \frac{g_{m11}}{g_{m11} + 0.33g_{m11}} = \frac{3}{4} \tag{4-4}$$

The term g_{s11} is due to the body effect of Q_{11} because the substrate of Q_{11} is grounded but its source is not.

The output buffer reduces the over all gain from 77.1 dB to 74.5 dB. The gain-bandwidth product of op-amp is 10 MHz (Figure 4-3). The capacitor C_1 is 5 pF and is used for dominant pole compensation of the op-amp.

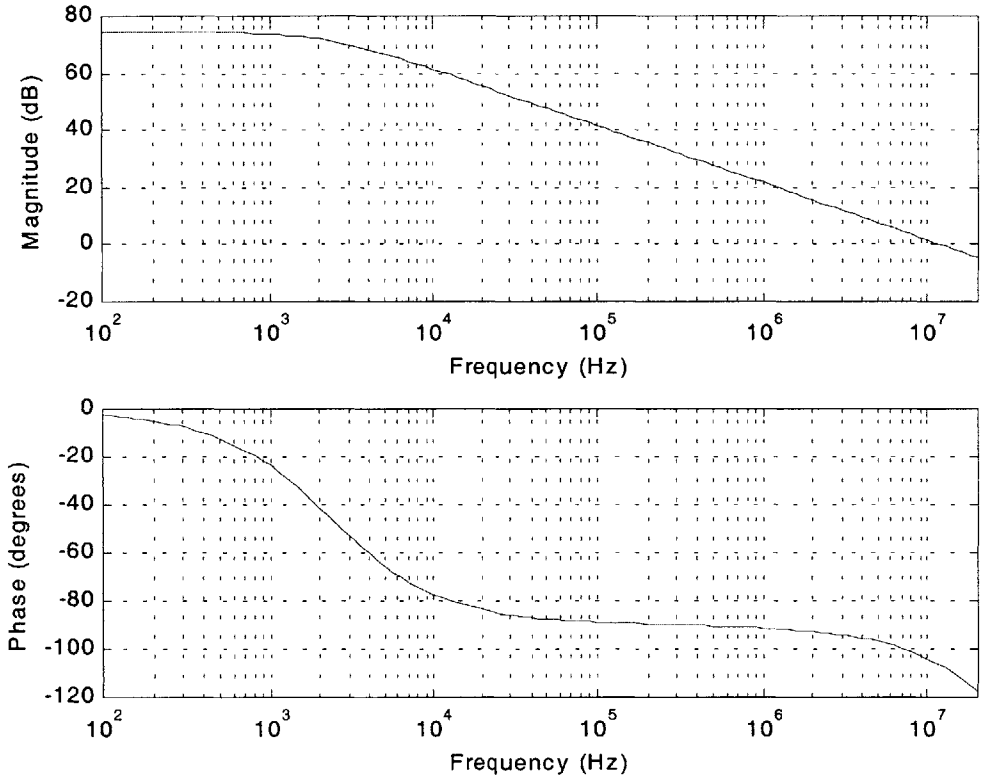

Figure 4-3: Gain and phase of the error amplifier.

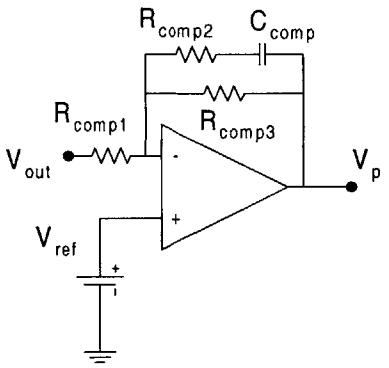

Figure 4-4: The compensator for the voltage control loop is a lag compensator created by using a RC network across the output and negative terminals of the error amplifier.

The RC network across the error amplifier in Figure 4-4 implements the a lag compensator given by:

$$G_c(s)=\left(\frac{R_{comp3}}{R_{comp1}}\right)\frac{(R_{comp2}C_{comp})s+1}{(R_{comp3}+R_{comp2})C_{comp}s+1}=100\frac{(3.6\times10^{-6}s+1)}{(1.6\times10^{-4}s+1)} \qquad (4\text{-}5)$$

This achieved by setting R_{comp1} equal to 39.1 kΩ, R_{comp2} equal to 90 kΩ, R_{comp3} equal to 3.91 MΩ and C_{comp} equal to 40 pF.

4.2.2 Current sense amplifier

The current sense amplifier in Figure 4-5 takes the voltage across R_{sense} and converts it to a ground referenced voltage V_{csa}. The amplifier, A_i, adjusts the gate voltage of Q_{11} so that V_{in+} and V_{in-} are equal. Since V_{in+} equals V_{in-}, which equals V_{out}, the current through R_1 is:

$$I_{sense}=\frac{V_{sense}-V_{out}}{R_1} \qquad (4\text{-}6)$$

This current flows through Q_{11} and the resistor R_2. The output voltage V_{csa} equals:

$$V_{csa}=R_2\frac{V_{sense}-V_{out}}{R_1}=\left(\frac{R_2}{R_1}R_{sense}\right)I_L \qquad (4\text{-}7)$$

From Chapter 2, R_{sense} is 0.15 Ω. R_2 is 50 kΩ and R_1 is 10 kΩ so that the overall gain of the current sense amp is 0.75 Ω.

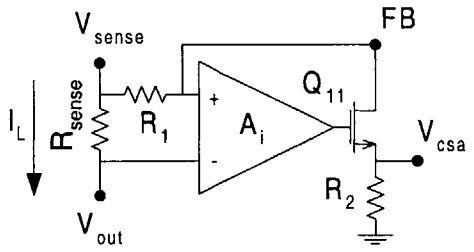

Figure 4-5: The current sense amplifier takes the voltage across R_{sense} and produces a ground referenced voltage, V_{csa}, that is proportional to the inductor current I_L.

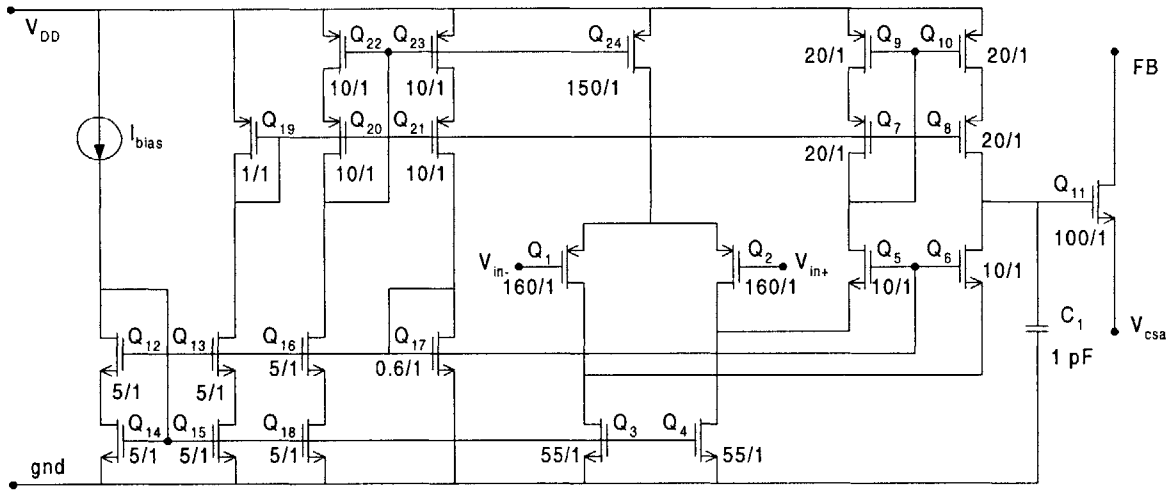

Figure 4-6: Schematic of the current sense amplifier. A folded cascode op-amp like the one used in the error amplifier drives the output transistor Q_{11}.

The amplifier, A_i, that drives transistor Q_{11} is the same folded cascode op-amp used in the error amplifier except that there is no output buffer (Figure 4-6). The current source I_{bias} is increased to 7.5 μA to increase the transconductance of Q_1. The gain-bandwidth product of the folded cascode amplifier is [14]:

$$GBW = \frac{g_{m1}}{C_1} \tag{4-8}$$

The transconductance of Q_1 is 0.61 mA/V and C_1 is 1 pF making the GBW of the current sense amplifier is 97 MHz.

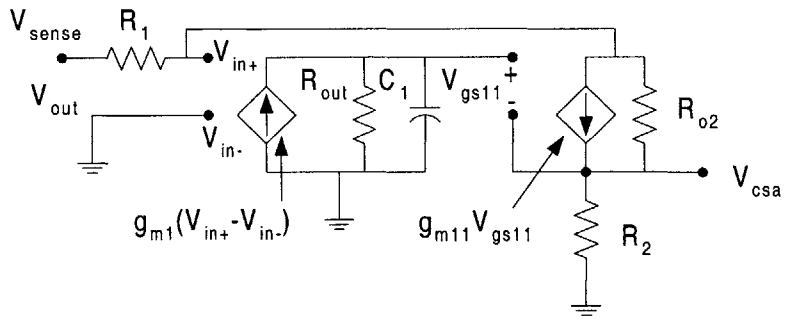

Figure 4-7: Linearized small signal model of the current sense amplifier.

The closed loop bandwidth of the current sense amplifier can be obtained by analyzing its linearized small signal model (Figure 4-7). Equating the voltages at the gate of Q_{11}:

$$(V_{in+} - V_{in-})g_{m1}Z_{out} = V_{gs11} + V_{csa} \tag{4-9}$$

Z_{out} is the parallel combination of R_{out} and C_1. Under closed loop control the output voltage is held constant. Therefore V_{in-}, which equals V_{out}, is a small signal ground. The current through R_1 must equal the current through R_2:

$$\frac{V_{sense} - V_{in+}}{R_1} = \frac{V_{csa}}{R_2} \tag{4-10}$$

Solving for V_{in+} we get:

$$V_{in+} = V_{sense} - \frac{R_1}{R_2}V_{csa} \tag{4-11}$$

The output voltage of the current sense amplifier, V_{csa}, in terms of V_{gs11} is:

$$V_{csa} = g_{m11}R_2V_{gs11} \tag{4-12}$$

Substituting in for V_{in+} and V_{gs11} the voltage at the gate of Q_{11} is:

$$\left(V_{sense} - \frac{R_1}{R_2}V_{csa}\right)g_{m1}Z_{out} = \left(1 + \frac{1}{g_{m11}R_2}\right)V_{csa} \tag{4-13}$$

The term $g_{m11}R_2$ is equal to:

$$g_{m11}R_2 = \sqrt{2\mu_n C_{ox}\left(W_{11}/L_{11}\right)I_{D11}}R_2 = 0.111R_2\sqrt{\frac{R_{sense}}{R_1}I_L} \tag{4-14}$$

The term $\left(1+\frac{1}{g_{m11}R_2}\right)$ varies from 1.3 to 1.08 as IL varies from 30 to 300 mA. Therefore the following approximation is made:

$$\left(1+\frac{1}{g_{m11}R_2}\right)\approx 1 \tag{4-15}$$

The output voltage of the current sense amplifier reduces to:

$$V_{csa}=\left(V_{sense}-\frac{R_1}{R_2}V_{csa}\right)g_{m1}Z_{out} \tag{4-16}$$

This can be modeled in the standard feedback configuration in Figure 4-8. The feedback factor, R_1/R_2, equals 0.2. The closed loop bandwidth of the current sense amplifier is equal to its gain-bandwidth product times the feedback factor or 19.4 MHz.

The switching frequency of the converter is 1.5 MHz. Therefore the first 12 harmonics of the inductor current are within the amplifier's bandwidth. Figure 4-9 shows an ADICE simulation of the current sense amplifier. The inductor current is 190 mA with 56 mA of peak-to-peak current ripple (L_O = 10 µH). The output of the current sense amplifier, V_{csa}, is compared to 0.75 Ω × I_L, which is what the amplifier would produce if its bandwidth were infinite. V_{csa} lags the ideal sense waveform by 14 ns due to its finite bandwidth. However, the 14 ns of delay produce negligible extra phase in the control loop and so does not adversely affect the stability of the converter.

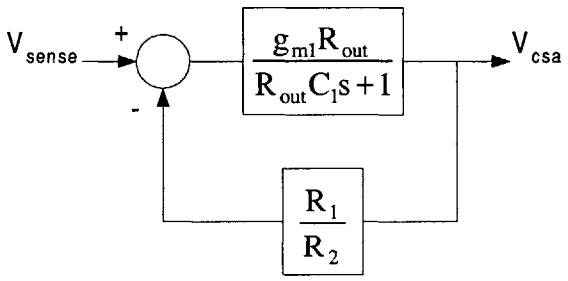

Figure 4-8: Closed loop block diagram of the current sense amplifier.

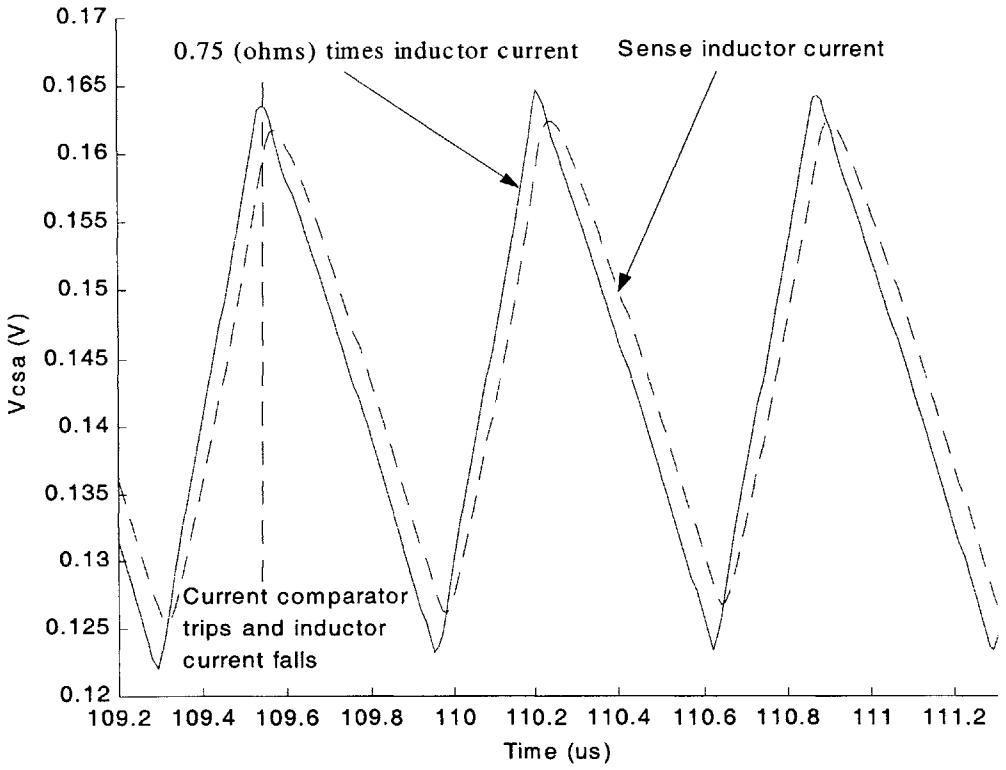

Figure 4-9: ADICE simulation comparing the sensed inductor current, V_{csa}, to the inductor current multiplied by the DC gain of the current sense amplifier (0.75 Ω).

The transition from a positive slope to a negative slope is rounded, which is also due to the current sense amplifier's finite bandwidth. The inductor current rises with a constant slope until the current comparator trips high. The rounded transition of V_{csa} occurs after the inductor current begins to fall and does not affect the trip point.

4.2.3 Slope compensation and voltage biasing

The slope compensation voltage ramp is generated by charging a capacitor with a constant current source. When the sum of the compensation ramp and sensed inductor current exceeds V_p, the current comparator trips and turns off the PMOS device. The compensation ramp is no longer needed after the pass transistor turns off. $V_{discharge}$ is tied to the output of the gate drive, P_{DR}. When P_{DR} goes high and the PMOS device turns off, the capacitor will discharge

through a transistor. The voltage across the capacitor will rise at the beginning of the next cycle when the clock resets the RS-latch and P_{DR} goes to ground.

Figure 4-10 shows the schematic of the slope compensation ramp generator. I_{bias} is 1.8 μA. This current is mirrored to the capacitor, C_{ramp}, by two current mirrors. Transistors with small widths are used for the current mirrors since the current through mirror branches is small. In order for transistors Q_1-Q_4 to stay in the saturation region of operation, their drain to source voltages must be greater than:

$$V_{effi} = \sqrt{\frac{2I_{Di}}{\mu_i C_{ox}\left(W/L_i\right)}} \tag{4-17}$$

V_{eff} of the Q_1-Q_2 is 0.12 V and 0.11 V for Q_3-Q_4.

The compensation ramp is added to the sum sensed inductor current and bias voltage, V_{csa}, through a resistor divider network consisting of R_3 and R_4 (Figure 4-11). R_3 is 100 kΩ and R_4 is 300 kΩ. The resistors are in parallel with R_2 (50 kΩ) and reduce the gain of the current sense amplifier to $4.44 \times R_{sense}$. This can be remedied by making R_1 9 kΩ so that current sense gain is still $5 \times R_{sense}$.

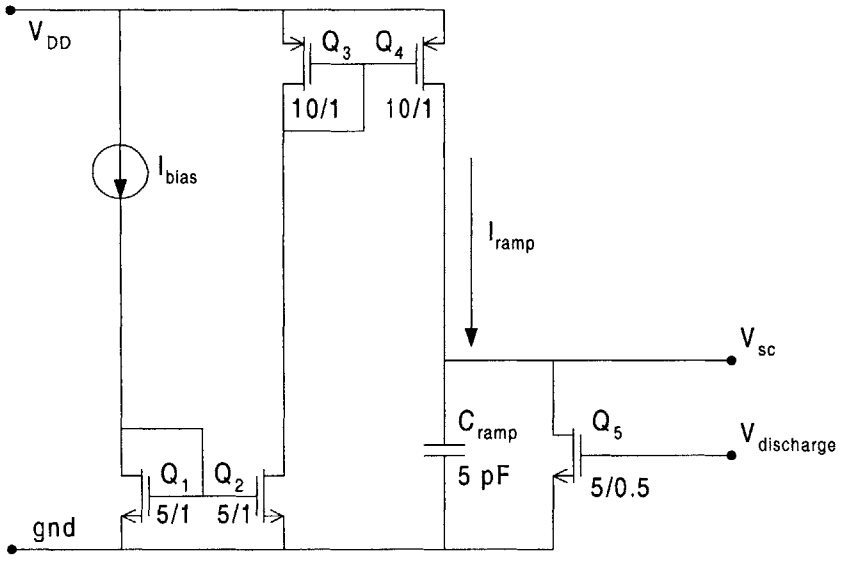

Figure 4-10: Schematic of the slope compensation circuit. The compensation ramp is generated by charging capacitor, C_{ramp}, with a constant current source I_{ramp}.

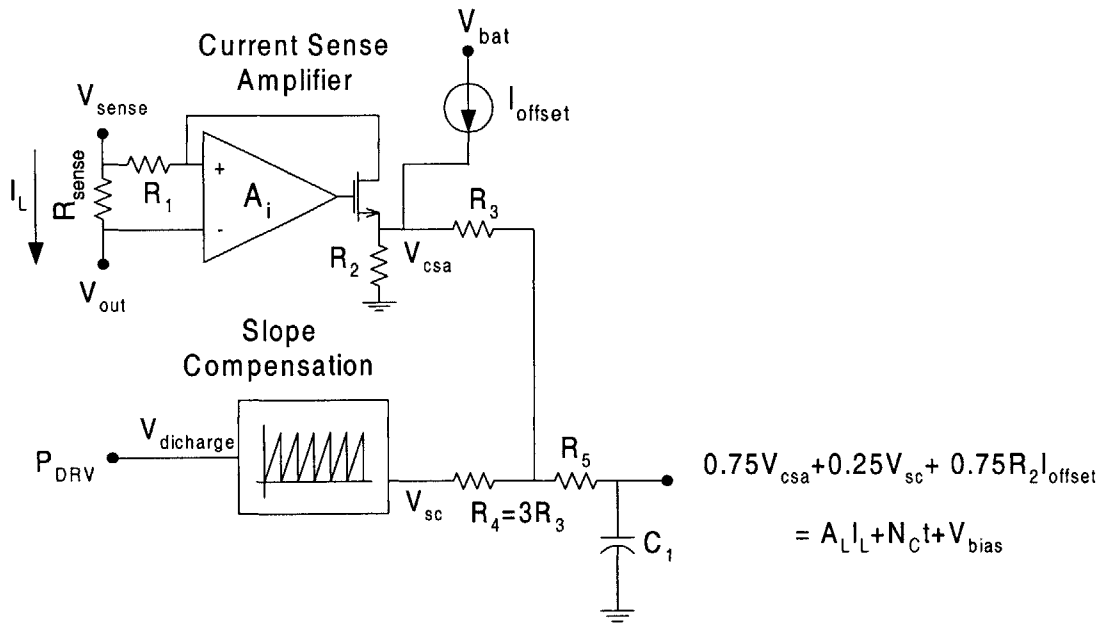

Figure 4-11: Addition of the compensation ramp and the sensed inductor current is accomplished through the resistor divider network R_3-R_4. R_3 is 100 kΩ and R_4 is 300 kΩ. The current source, I_{offset}, produces a bias voltage to prevent the transistors in the error amp from leaving saturation region of operation.

The resistor divider is followed by a low pass filter consisting of R_5 and C_1. The low pass filter is needed to reduce the thermal noise generated by the resistors R_3 and R_4. The bandwidth of the filter is 100 MHz, which is much higher than the closed loop bandwidth of the current sense amplifier (19.4 MHz). Therefore it can be ignored during normal circuit operation.

The 7.5 μA current source, I_{offset}, flows through the parallel combination of R_2 and sum of R_3 and R_4, and produces a bias voltage equal to 333 mV. Consequently, V_{csa} is shifted upward by 333mV. From Section 4.2.2, the current through resistor R_1 is:

$$I_{sense} = \frac{V_{sense} - V_{out}}{R_1} \tag{4-18}$$

The amplifier, A_i, in the current sense amp adjusts the gate voltage of Q_{11} so that the drain current through Q_{11} is equal to I_{sense}. In other words, Q_{11} becomes a current source that pours I_{sense} into R_2. The result is that V_{csa} now equals:

$$V_{csa} = (R_2 \| (R_3 + R_4))(I_{sense} + I_{offset}) = \left(\frac{R_2 \| (R_3 + R_4)}{R_1} R_{sense} \right) I_L + 333mV \quad (4\text{-}19)$$

The output of the low pass filter is:

$$0.75\left(\frac{R_2 \| (R_3 + R_4)}{R_1} R_{sense} \right) I_L + 0.75(333mV) + 0.25V_{sc} = A_L I_L + N_C t + V_{bias} \quad (4\text{-}20)$$

The overall gain from inductor current, I_L, to the sensed inductor voltage V_L is:

$$V_L = 0.75\left(\frac{R_2 \| (R_3 + R_4)}{R_1} \right) R_{sense} I_L = 0.5625 I_L = A_L I_L \quad (4\text{-}21)$$

A_L of 0.5625 is the current gain used in Chapter 3. N_C was set to 9×10^4 V/s in Section 3.4.2. This requires that the slope of V_{ramp} be 3.6×10^5 V/s.

$$\frac{dV_{Cramp}}{dt} = \frac{I_{ramp}}{C_{ramp}} = 3.6\times10^5 V/s \quad (4\text{-}22)$$

This is accomplished by setting I_{ramp} equal to 1.8 μA and C_{ramp} equal to 5 pF. The bias voltage, V_{bias}, is 250 mV and is higher than the minimum output voltage of the error amplifier ($V_{ds,sat}$ = 0.18 V).

An ADICE simulation of the current sense amplifier, slope compensation circuit and adder network is shown in Figure 4-12. The current through the inductor is 300 mA with 56 mA of peak-to-peak ripple. V_{csa} should be 0.75 Ω × I_L + 333 mV or 555 mV with 42 mV of peak-to-peak voltage ripple. This matches the simulation result well.

The middle plot of Figure 4-12 shows the slope compensation voltage rising up to a peak of 154 mV. The duty cycle at 300 mA and a 3.6 V battery voltage is 0.38, which corresponds to an on-time of 254 ns. The slop of the voltage ramp is 3.6×10^5 V/s. The slope compensation voltage should rise to a peak of only 91 mV. The cause of error is the small fraction of I_{offset} that flows through R_4 into C_{ramp}. The extra current raises the slope to 6.1×10^5 V/s, making N_C increase from 9×10^4 V/s to 1.5×10^5 V/s. The decay rate for perturbations in the inductor current change from $(-0.352)^n$ to $(-0.073)^n$ if L_O is 3.76 μH and from $(0.2)^n$ to $(0.4)^n$ if L_O is 12 μH. This is when

the battery voltage is 2.9 V (worst case scenario). The perturbations are still well damped and since the slope of the compensation does not affect the gain-bandwidth product of the converter's transfer function, the deviation in the slope has little effect on the closed loop performance of the converter.

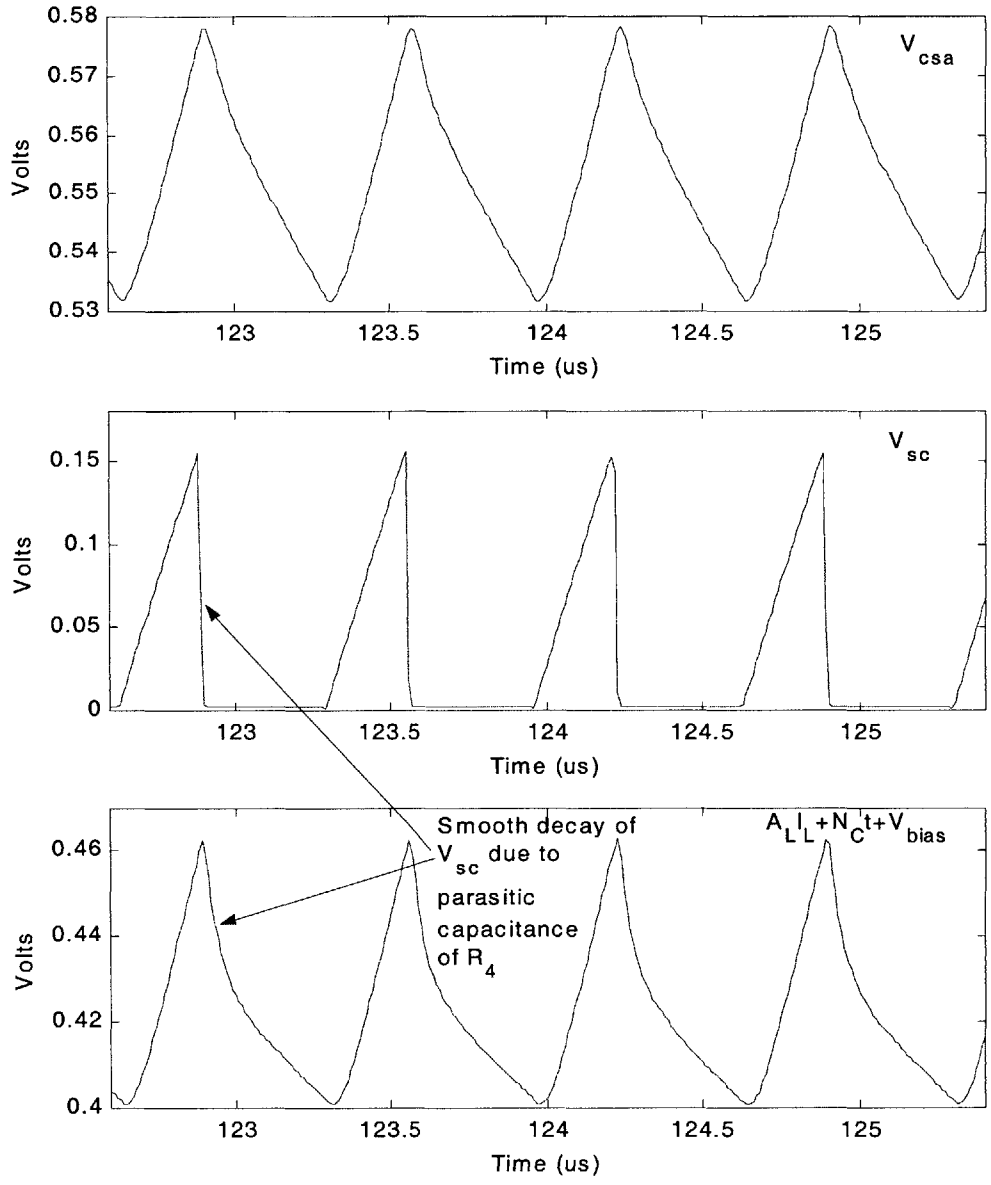

Figure 4-12: ADICE simulation of the current sense amplifier, the slope compensation circuit and resistive adder network.

The bottom plot shows the output of the resistor adder network. The steady state voltage should be ¾(555 mV) = 416 mV. The minimum voltage from the adder is steady state value minus half the ripple current times 0.5625 Ω or 400 mV. The steady state and minimum match the simulation result well. The peak voltage should be equal to the average voltage plus half the ripple current times 0.5625 Ω plus a quarter of the slope compensation voltage or 470 mV. The actual peak is only 463 mV. Additionally, when the slope compensation voltage is discharged, the voltage at the output of the resistor adder network should suddenly drop by 38 mV. This does not happen. Instead the voltage decreases with a steep slope and then smoothly transitions to a falling slope that is equal to ¾ of the falling slope V_{csa}. The cause of the discrepancy in the peak voltage and the voltage drop is due to the parasitic capacitance of the resistor R_4. R_4 is a polysilicon resistor that is laid on top of the silicon substrate with a layer of oxide separating the two. This creates parasitic capacitance from the polysilicon layer to the substrate. Since R_4 is a very large resistor it takes up a large area on the chip and thus its parasitic capacitance is significant. The RC time delay decreases the voltage added by the slope compensation circuit and also smoothes out the fall in the slop compensation voltage when $V_{discharge}$ goes high.

4.3 Decision stage

The decision making part of the control IC consists of the current comparator, the current limiter, the clock and the RS-latch. The clock used in the simulations is a SPICE pulsed voltage source with a duty cycle of 10%. The actual clock for the buck converter will come from the mixed signal IC in the cell phone. At the start of a cycle, the clock goes high, resetting the RS-latch. Q goes to 0 turning on the PMOS pass transistor. If $A_L I_L + N_C t + V_{bias}$ exceeds V_p at any point in time during the switching cycle, Q goes to 1. This turns off the PMOS pass transistor and turns on the NMOS synchronous rectifier. The current limiter circuit is a comparator that operates in parallel to the current comparator via the OR-gate. The current limiter provides instantaneous current limiting. If $0.75I_L + V_{bias}$ exceeds I_{lim} then the current limiter trips and sets Q to 1.

4.3.1 Current comparator

The high frequency buck converter requires a very fast comparator. The comparator architecture consists of a pre-amplification stage, decision stage and output buffer stage [15]. The schematic of the comparator is shown in Figure 4-13.

The pre-amplification stage consists of Q_1-Q_6. The gain from input voltages to the currents I_{o1} and I_{o2} are:

$$I_{o1} = \frac{kg_{m1}}{2}(V_{in+} - V_{in-}) + \frac{kI_{D17}}{2} \tag{4-23}$$

$$I_{o2} = \frac{kg_{m1}}{2}(V_{in-} - V_{in+}) + \frac{kI_{D17}}{2} \tag{4-24}$$

The faster I_{o1} and I_{o2} differ from one another, the faster the comparator decides to go high or low. This is achieved by making the kg_{m1} large so that small differences in V_{in+}-V_{in-} will result in large differences in I_{o1} and I_{o2}. The transconductance of Q_1 is made large by making the width of Q_1 100 μm and setting I_{D1} to 30 μA. I_{bias} is 5 μA. This current is mirrored and doubled to 10 μA through Q_{14} and Q_{15}. Q_{17} is made six times wider than Q_{16} so that I_{D17} is 60 μA. The gain from input voltage to I_{o1} and I_{o2} is further increased by using current mirrors, consisting of Q_3-Q_6. The width of Q_5 is 5 μm and the width of Q_3 is 2 μm making the current mirror gain, k, 2.5. Plugging in these values, the gain from input voltages to the currents I_{o1} and I_{o2} is now:

$$I_{o1} = 0.265\,{}^{mA}\!/_{V}\,(V_{in+} - V_{in-}) + 0.075\text{mA} \tag{4-25}$$

$$I_{o2} = 0.265\,{}^{mA}\!/_{V}\,(V_{in-} - V_{in+}) + 0.075\text{mA} \tag{4-26}$$

The decision circuit consists of transistors Q_7-Q_{10}. The decision circuit works as follows. At the beginning of the cycle, V_p (tied to V_{in-}) is much larger than $A_L I_L + N_C t$ (tied to V_{in+}). I_{o1} is much larger than I_{o2}. The voltage at the drain of Q_9 is:

$$V_{D9} = V_{DD} - \left(V_{tp} + \sqrt{\frac{2I_{o1}}{\mu_p C_{ox}\left(W_9/L_9\right)}} \right) \tag{4-27}$$

Therefore, transistors Q_8 and Q_9 are on. Since transistor Q_8 is on, the gate voltages of Q_7, Q_{10} and Q_{12} are all shorted to V_{DD}, turning them off. In addition, since transistor Q_9 is on, Q_{11} mirrors I_{01}. This current flows through Q_{13}. The gate to source voltage of Q_{13} is:

$$V_{gs13} = V_{tn} + \sqrt{\frac{2I_{o1}}{\mu_n C_{ox}\left(W_{13}/L_{13}\right)}} \tag{4-28}$$

This turns on the output buffer transistor, Q_{14}, and forces the output of the comparator low.

As $A_L I_L + N_C t$ increases, the current through I_{o2} increases and the drain voltage of Q_{10} decreases. Similarly, the current through I_{o1} decreases making the drain voltage of Q_9 increase. The comparator starts to switch states when the source to drain voltage of Q_8 equals V_{tp}. This occurs when Q_8 leaves the linear region and moves into the saturation region:

$$I_{o2} = \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_8 \left(V_{DD} - V_{D8} - V_{tp}\right)^2 = I_{o1} \tag{4-29}$$

In other words when I_{o2} equal I_{o1} or $A_L I_L + N_C t$ equals V_p, the comparator switches state.

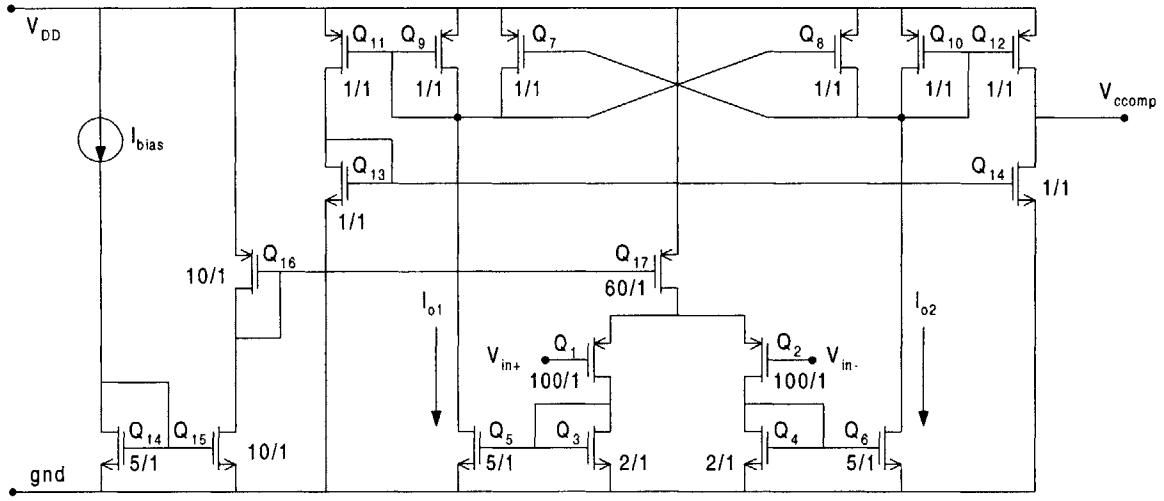

Figure 4-13: Schematic of the current comparator.

When the source to drain voltage of Q_8 equals V_{tp}, Q_7 turns on and starts to carry some of I_{o1}.The current through Q_9 decreases, which starts to reduce the source to gate voltage of Q_8 and Q_9. When $V_{sg8} = V_{sg9}$ falls below V_{tp}, Q_8, Q_9, Q_{11}, Q_{13} and Q_{14} shut off. Q_{10} is now fully on and carries all of I_{o2}. Since the gate of Q_{12} is tied to the gate to Q_{10}, Q_{12} turns on and the comparator goes high.

4.3.2 Current limiter

The current limiter compares the voltage at the output of the current sense amplifier, V_{csa}, to current limit set by the I_{lim} pin and trip high whenever V_{csa} exceeds I_{lim}. V_{csa} is $0.75\Omega \times I_L + 333$ mV. The current limit is set by making I_{lim} equal to $0.75\Omega \times I_{max} + 333$ mV, where I_{max} is the maximum peak inductor current desired.

The comparator used for current limiting is similar to the current comparator except that the current through the input transistors Q_1 and Q_2 have been reduced to 15 μA each. This reduces the transconductance of the preamplifier and slows down the comparator. The current limiter does not need to be as fast as the current comparator. The current comparator must go from high to low within 10 ns so that it does not add significant phase delay to the control loop. The current limiter bypasses the control loop and can thus be slower. Reducing the current to Q_1 and Q_2 to 15 μA also reduces the power consumption in the comparator by a factor of 2. Figure 4-14 shows the current limiter and OR-gate in one schematic. The current limiter is tied to one of the inputs of the OR-gate. The output the current comparator is tied to node V_{cmp}.

4.3.3 RS-latch

The RS-latch is created by using two 2-input NOR gates. The output of each NOR gate is fed back to one of the input pins of the other NOR gate (Figure 4-15). The logic for the RS-latch is shown in Table 4-2.

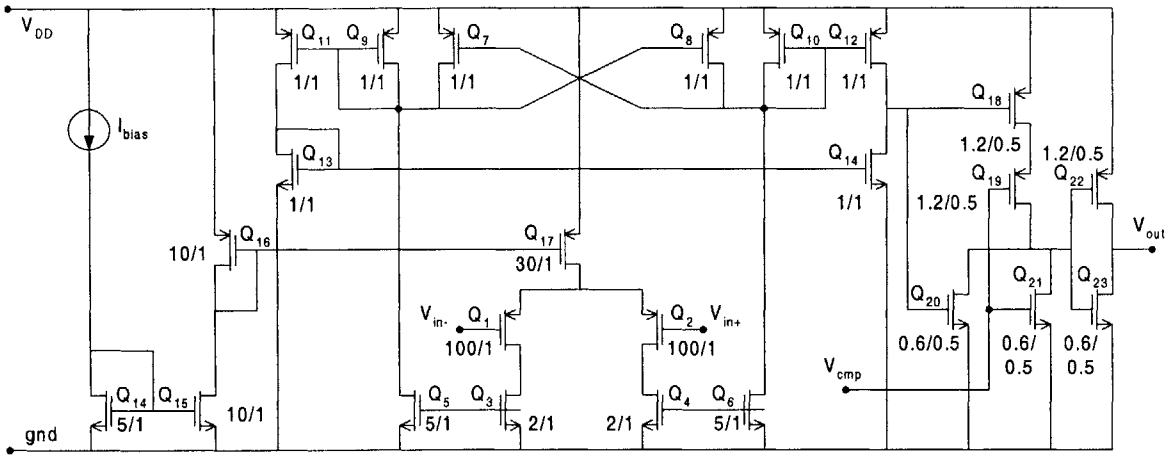

Figure 4-14: Schematic of the current limiter and OR-gate. The current comparator is connected to the V_{cmp} terminal of the OR-gate.

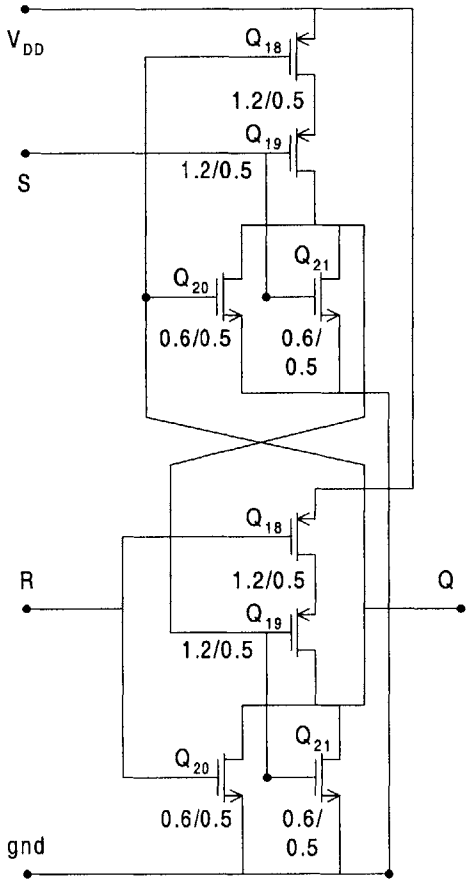

Figure 4-15: Schematic of the RS-latch.

Table 4-2: RS-latch logic

R	S	Q
0	0	0
0	1	1
1	0	0
1	1	0

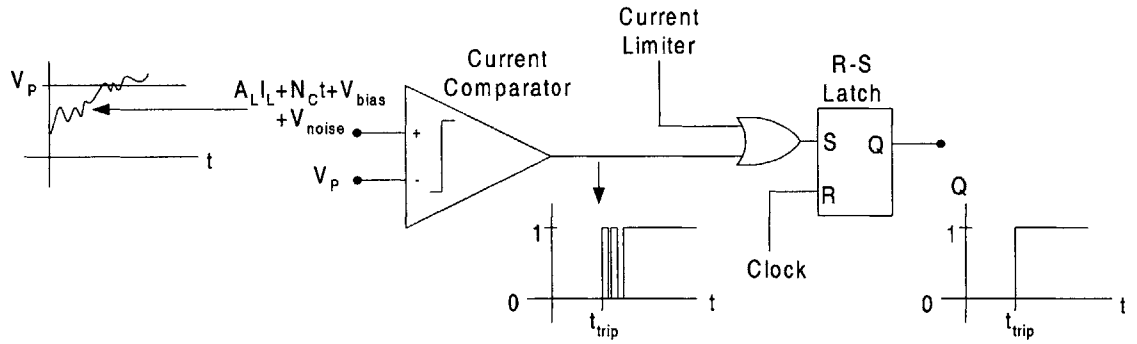

Figure 4-16: Once S sets Q to 1, Q stays at 1 even though the output of the comparator may swing high and low due to noise at the input of the current comparator.

At the beginning of a cycle, the clock trips high. The width of the clock is only 66 ns or 10% of the period. Referring to Table 4-2, S can set Q to 1 only after the clock goes low (R goes to 0) so that the minimum duty ratio is 10%. Once S sets Q to 1, Q stays at 1 until R resets it to 0. Therefore, if S suddenly goes to 0 after it goes high, the output of the RS-latch is unaffected. This can occur if there is noise at the inputs of the current comparator (Figure 4-16). Since Q stays high once S goes to 1, no hysteresis is needed in the comparators.

The ADICE simulation results of the decision stage are shown in Figure 4-17 and 4-18. Figure 4-17 shows the transition of output of the RS-latch, Q, from low to high after $A_LI_L+N_Ct+V_{bias}$ exceeds V_p. As soon as the current comparator reaches 1.8 V, S and Q go high. The total delay from input of the current comparator to Q is 9 ns. Figure 4-18 shows the transition of Q when the current limiter trips high. I_{lim} was set to 0.7 V, corresponding to an I_{max} of 490 mA. The total delay from the input of the current limiter to Q is 16.6 ns.

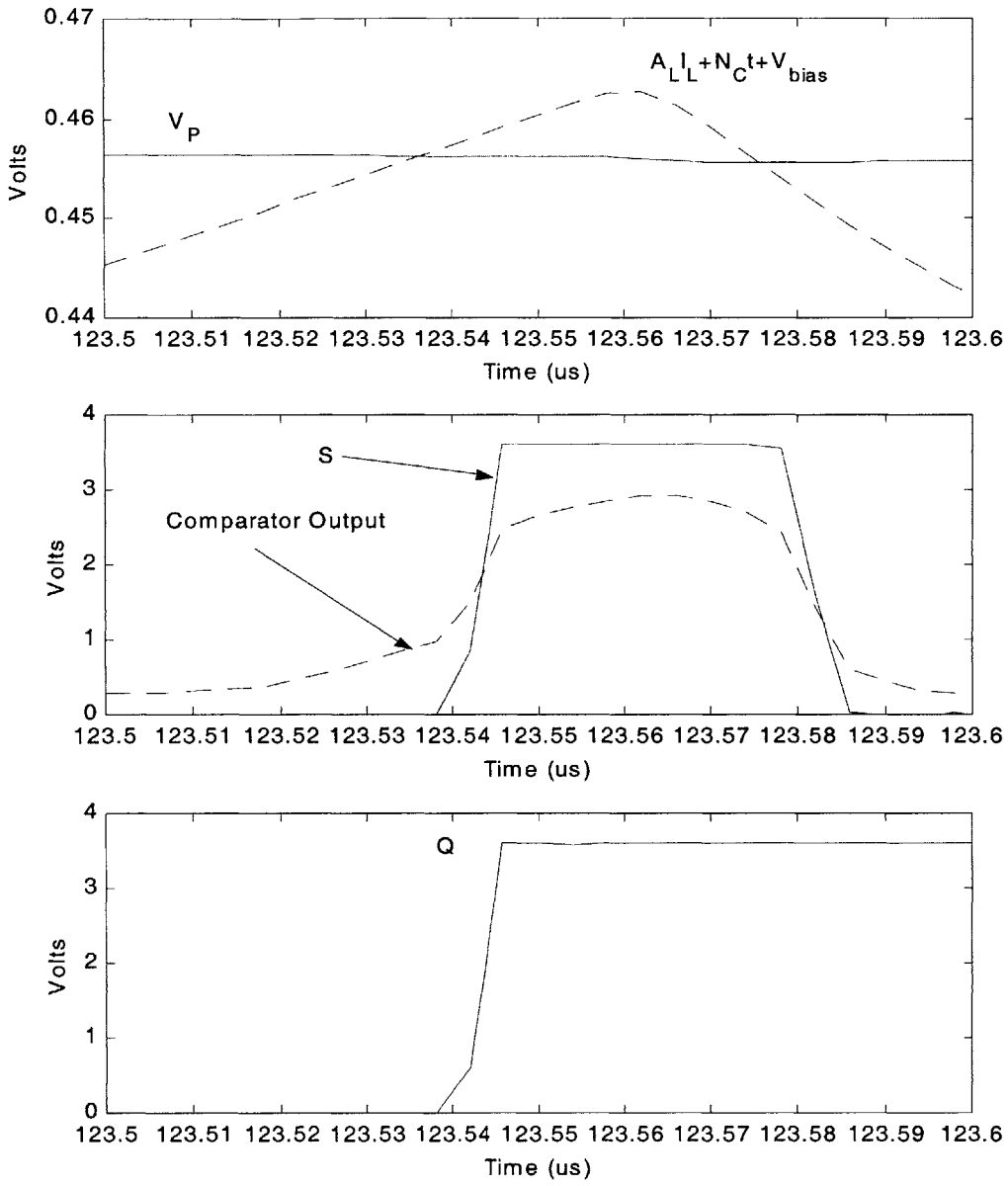

Figure 4-17: ADICE simulation of the current comparator. When $A_L I_L + N_C t + V_{bias}$ exceeds V_p, the current comparator trips high setting S to 1. S then sets Q to 1. The total delay from the input of comparator to Q is only 9 ns. Notice that when $A_L I_L + N_C t + V_{bias}$ falls below V_p and the comparator trips low, Q stays high and the pass transistor stays off letting the inductor current decay until the end of the cycle.

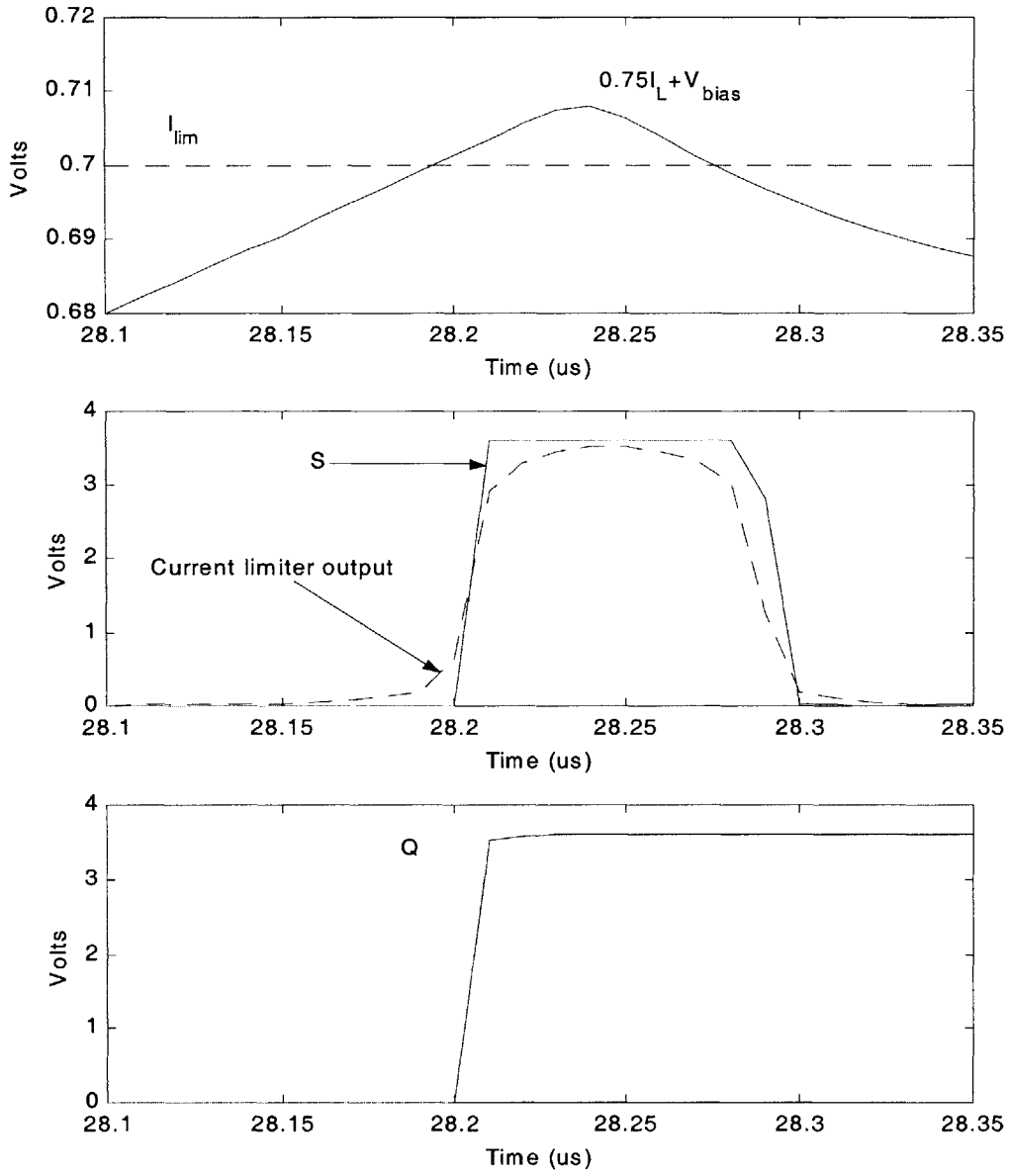

Figure 4-18: ADICE simulation of the current limiter. When $0.75I_L+V_{bias}$ exceeds I_{lim}, the current limiter trips high setting S to 1. S then sets Q to 1. The total delay from the input of comparator to Q is only 16.6 ns. As in the case of the current comparator Q stays high even when the comparator trips high and the inductor current decays until the end of the cycle.

4.4 Drive stage

4.4.1 Drive stage circuits

The final components of the control IC are the shoot-through protection circuit (STP) and the gate drives. The two components are analyzed together because the output of the gate drives, P_{DR} and N_{DR}, are fed back to the STP via the P_{gate} and N_{gate} terminals, respectively. A high level block diagram of the STP and gate drive circuitry is shown in Figure 4-19. The STP consists of a AND gate-OR gate pair. Both logic gates have one input tied to the output of the RS-latch, Q. The second input of the OR gate is tied to the output of the gate drive that turns on the NMOS synchronous rectifier. The second input of the AND gate is tied to the output of the gate drive that turns on the PMOS pass transistor. Also shown in Figure 4-19 are the time delays associated with each sub-circuit. The time delays of the logic gates, τ_{d1} and τ_{d2}, are on the order of 1 ns. The time delays for the gate drives, τ_{d3} and τ_{d4} will vary with the input capacitance of the power MOSFETs used. The schematic of the STP is shown in Figure 4-20.

The output of the STP consists of very small transistors (W = 1.2 μm/L = 0.6 μm). If a single inverter was used as the gate drive it would have be very large in order to drive the power MOSFETs (C_{in} ~ 100-200 pF). The large inverter would also have a fairly large input capacitance (~ 5 pF). If the STP had to drive this inverter the delay would be too large. The time delay for the an inverter to drive a captive load, C_{load}, is equal to [15]:

$$t_{delay} = (R_n + R_p)(C_{out} + C_{load}) \tag{4-30}$$

Where t_{delay} is the sum of the delays of the inverter going high to low and low to high. R_n and R_p are the MOSFET drain to source resistance of the NMOS and PMOS transistors, respectively. R_n and R_p are on the order of 10 kΩ, for the output transistors of the STP circuit. This results in a delay of 100 ns to turn the gate drive on and off if the gate drive were a single inverter with 5 pF of input capacitance. The large gate drive inverter would have R_n and R_p on the order of 10 to 100

Ω and would add an additional delay of 2 to 20 ns. This is significant delay considering that the switching period is 666 ns.

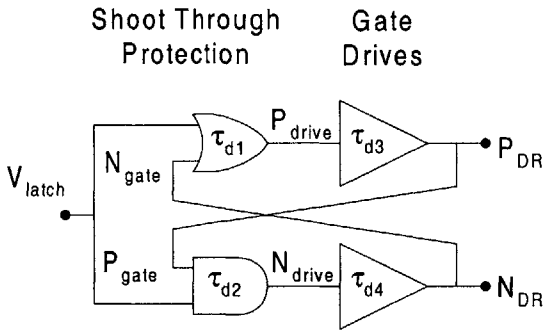

Figure 4-19: The shoot-through protection circuit consists of an AND-gate and an OR-gate that have one of their input tied to the output of the RS-latch at the terminal V_{latch}. The output of the gate drives, P_{DR} and N_{DR}, are fed back to the terminals P_{gate} and N_{gate}, respectively, to prevent both power MOSFETs from turning on.

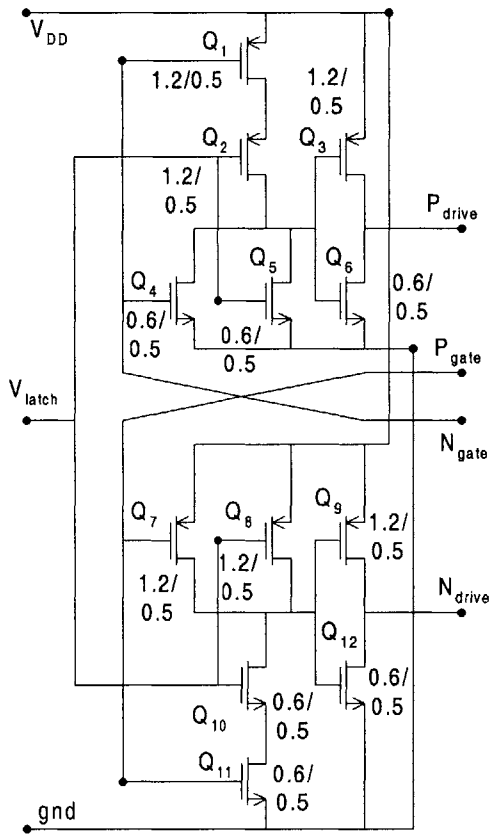

Figure 4-20: Schematic of the shoot-through protection circuit.

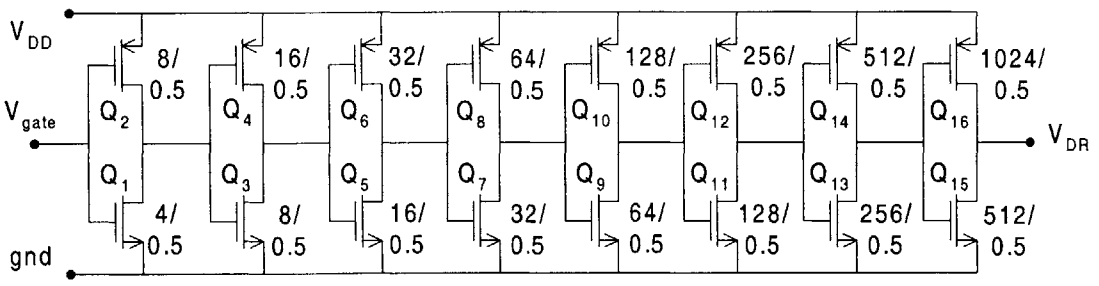

Figure 4-21: Schematic of the gate drive. The cascade of increasing larger inverters reduces the overall gate delay of the gate drive.

The gate drives are instead series of eight CMOS inverters (Figure 4-21). Each successive inverter is twice as wide as the one preceding it. The output transistors of the STP circuit drive an inverter that is 6.66 time larger. The input capacitance of Q_1 and Q_2 of the gate drive are on the order of 10 fF, resulting in a delay of only 0.2 ns. The first inverter drives next one that has twice as much input capacitance. However, since R_{n1} and R_{p2} are smaller than those of STP output transistors, the delay of the first inverter does not increase significantly. By having the STP drive a slightly larger transistor, which in turns drives a slightly larger transistor, and so on, the sum of the t_{delay} of each inverter is less than total gate delay of one single large inverter. This significantly reduces the time delay in the gate drives.

4.4.2 Drive stage operation

The STP-gate drive combination works as follows. At the end of the cycle, Q, P_{DR} and N_{DR} are all 1 so that the pass transistor is off and the synchronous rectifier is off. P_{drive}, N_{drive}, P_{gate} and N_{gate} are also at logic 1. When the next cycle begins, the clock resets the RS-latch and Q goes to 0. After time τ_{d2}, N_{drive} goes low and after time $\tau_{d2}+\tau_{d4}$, N_{gate} also goes low as the synchronous rectifier turns off. Since Q and N_{gate} are both 0, P_{drive} goes low at time $\tau_{d2}+\tau_{d4}+\tau_{d1}$. After another τ_{d3} seconds the pass transistor turns on and P_{gate} goes to 0. All the terminals in Figure 4-19 are 0 and the pass transistor turns on $\tau_{d1}+\tau_{d3}$ seconds after the synchronous rectifier turns off. At some point later in the cycle, say time τ_o, either the current comparator or the current limiter will trip

and set Q to 1. At time $\tau_o + \tau_{d1}$ P_{drive} will go high. After another τ_{d3} seconds the pass transistor turns off and P_{gate} goes to 1. Since Q and P_{gate} are now both 1, N_{drive} goes high at time $\tau_o + \tau_{d1} + \tau_{d3} + \tau_{d2}$. After another τ_{d4} seconds the synchronous rectifier turns on and N_{gate} goes to 1. All the terminals in Figure 4-19 are 1 and the synchronous rectifier turns turn on $\tau_{d2} + \tau_{d4}$ seconds after the pass transistor off. This sequence is summarized in Table 4-3.

The drive stage was simulated in ADICE and the results shown in Figures 4-22, 4-23 and 4-24. The Si1555DL SPICE models provided by Vishay Siliconix was used in the simulation. The input capacitance of the Si1555DL NMOS transistor is 84 pF and is 154 pF for the Si1555DL PMOS transistor. The threshold voltages for the NMOS and PMOS power transistors are 0.9 V and –1 V, respectively.

Figure 4-22 shows the turn-on sequence of the buck converter when the NMOS synchronous rectifies turn off and the PMOS pass transistor turns on. The simulation follows the expected result from Table 4-3. The delay times, however, are not well defined. For instance, N_{drive} starts to go low after Q starts to go low but both reach 0 V at the same time. The case is similar with N_{DR} and P_{drive}. The total delay from the time Q starts to low to the time P_{DR} reaches 2.6 V (PMOS starts to turn on) is 16 ns, while the NMOS synchronous rectifier turns off (reaches 0.9) 5 ns before the PMOS pass transistor starts to turn on.

Table 4-3: Turn-on and Turn-off sequence for the power MOSFETs.

Time	0^-	0^+	τ_{d2}	$\tau_{d2}+\tau_{d4}$	$\tau_{d2}+\tau_{d4}$ $+\tau_{d1}$	$\tau_{d2}+\tau_{d4}$ $+\tau_{d1}+\tau_{d3}$	τ_o	$\tau_o+\tau_{d1}$	$\tau_o+\tau_{d1}$ $+\tau_{d3}$	$\tau_o+\tau_{d1}+$ $\tau_{d3}+\tau_{d2}$	$\tau_o+\tau_{d1}+$ $\tau_{d3}+\tau_{d2}+\tau_{d4}$
Q	1	0	0	0	0	0	1	1	1	1	1
P_{drive}	1	1	1	1	0	0	0	1	1	1	1
P_{gate}	1	1	1	1	1	0	0	0	1	1	1
N_{drive}	1	1	0	0	0	0	0	0	0	1	1
N_{gate}	1	1	1	0	0	0	0	0	0	0	1

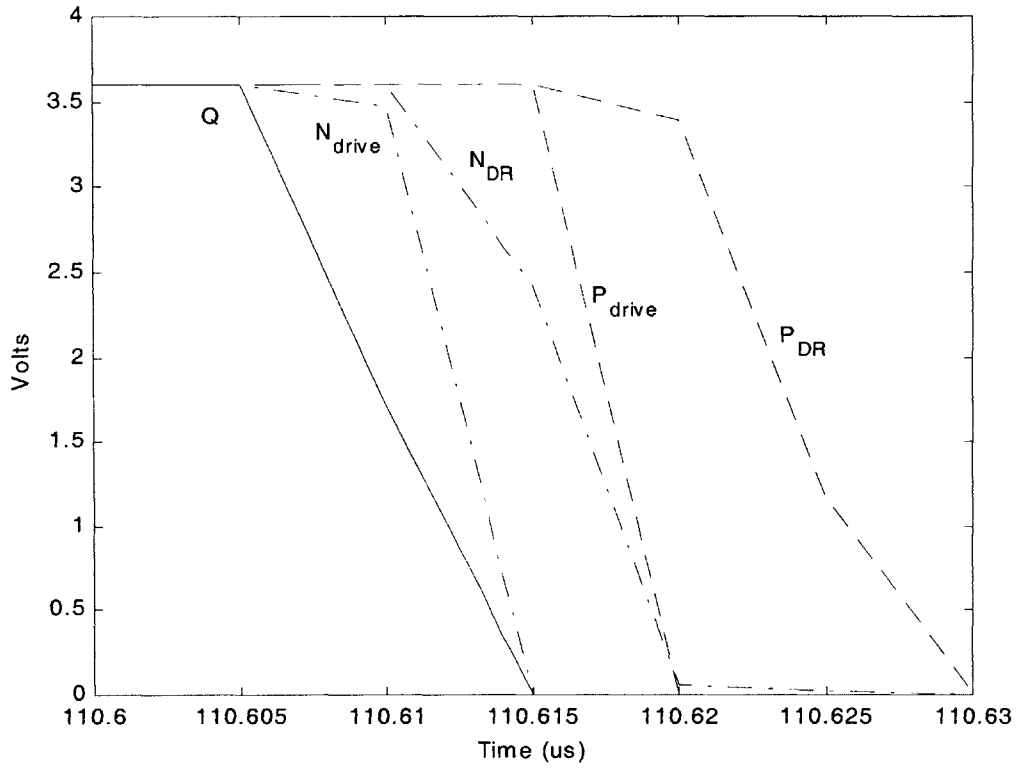

Figure 4-22: Turn-on sequence for the buck converter in which the NMOS synchronous rectifier turns off and the PMOS pass transistor turns on. There is a 16 ns delay from the time Q starts to go low to time the pass transistor starts to turn on (P_{DR} decreases to 2.6 V). The synchronous rectifier turns off (N_{DR} decreases to 0.9 V) 5 ns before the pass transistor starts to turn on.

Figure 4-23 shows the turn-off sequence of the buck converter when the pass transistor turns off and the synchronous rectifier turns on. The time it takes for P_{drive} to go high after Q goes high is negligible. P_{drive} is the output of an OR gate that consists of very small transistors, which make the delay of the OR gate extremely small. Once P_{drive} goes high, P_{DR} starts to rise. N_{drive} goes high when P_{DR} reaches 1.2 volts. Since N_{drive} is the output of a fast AND-gate, it goes high before the PMOS pass transistor fully turns off (reaches 2.6 V). This is due to large input capacitance of the pass transistor. N_{DR} starts to rise as soon as N_{drive} goes high and reaches 0.9 V 6 ns after the PMOS device turns off. The total delay from the time Q starts to go low to time synchronous rectifier starts to turn on is 21 ns.

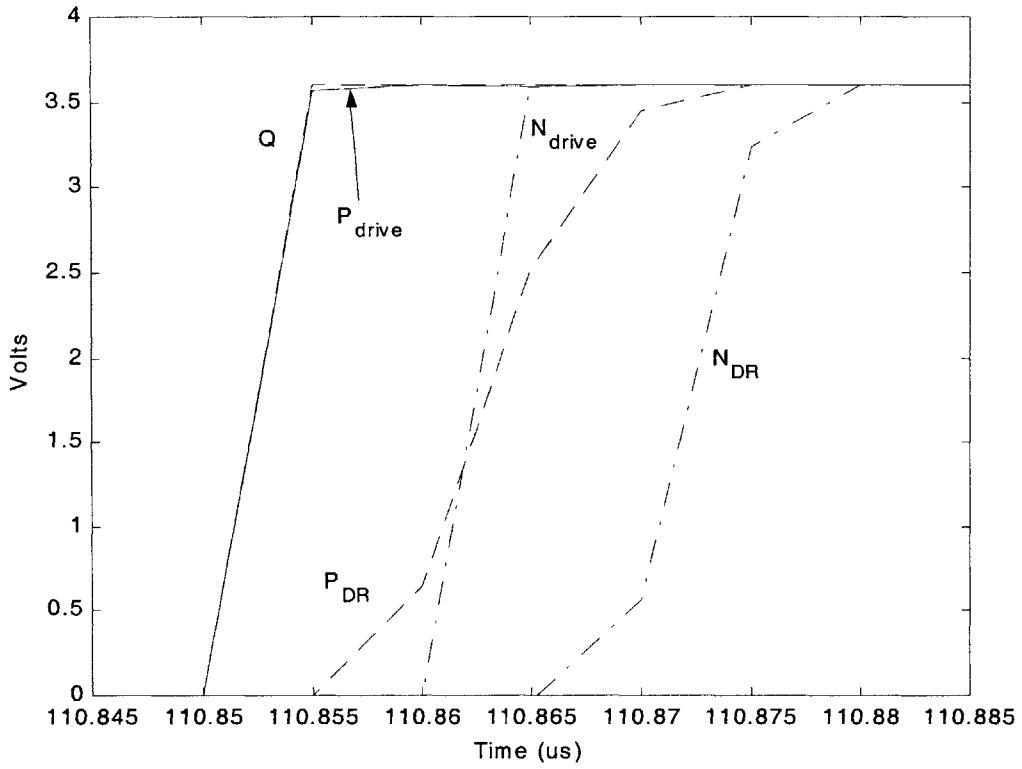

Figure 4-23: Turn-off sequence for the buck converter in which the PMOS pass transistor turns off and the NMOS synchronous rectifier turns on. There is a 21 ns delay from the time Q starts to go high to time the synchronous rectifier starts to turn on (N_{DR} increases to 0.9 V). The pass transistor turns off (P_{DR} increases to 2.6 V) 6 ns before the synchronous rectifier starts to turn on. Notice that N_{drive} starts to go high after PDR starts to go high but reaches V_{bat} before P_{DR}. This is because the N_{drive} terminal is the output of an AND gate with very small transistors that transition from low to high very rapidly. The P_{drive} follows Q with almost no delay for the same reason. The OR-gate of the STP circuit consists of small transistors that switch rapidly.

Figure 4-24 shows turn-on and turn-off sequence of the power MOSFETs along with the resulting voltage across the schottky diode. The schottky conducts only for a short period of time when both power MOSFETs are off. The forward voltage drop when the diode is on is only 300 mV. The forward voltage shows up negative in Figure 4-21 because the anode of the diode is at ground and forward voltage is defined as the voltage across the anode to the cathode of the diode. The SPICE model of schottky diode used here is the ZHCS400 from Zetex.

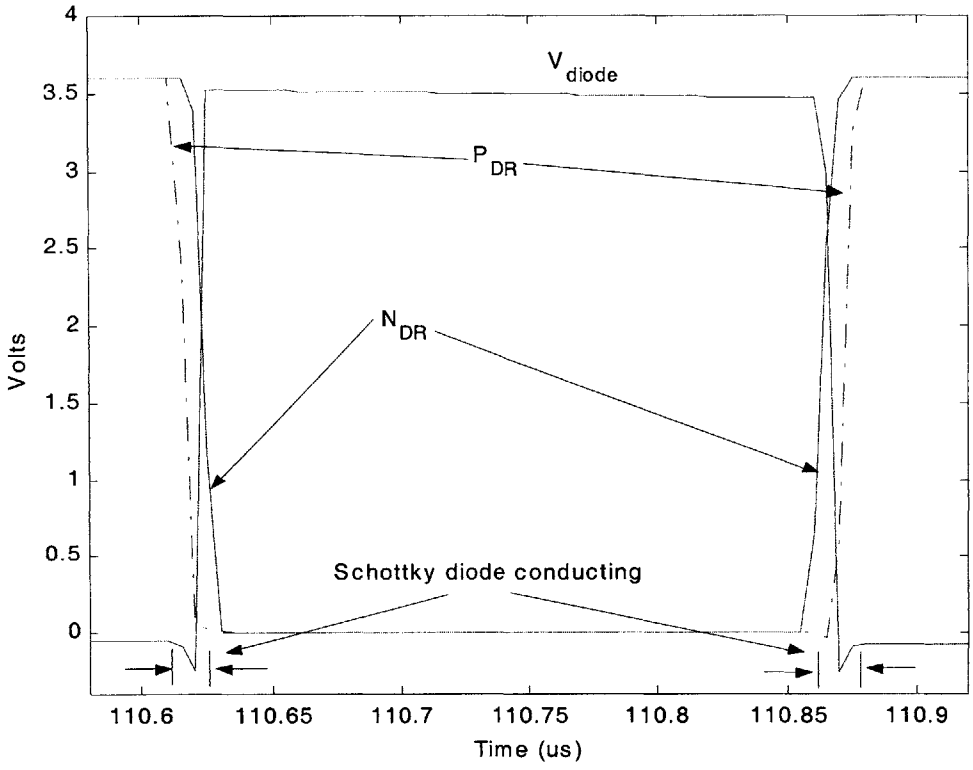

Figure 4-24: Turn-on and turn-off sequence of the power MOSFETs and the corresponding voltage across the schottky diode. The schottky diode turns on for a brief period of time during the turn-on and turn-off sequences when both power MOSFETs are off. The forward voltage drop is only 300 mV.

4.5 Power consumption in the control IC

The power consumption in the control IC needs to be calculated before the total efficiency of the closed loop buck converter can be determined. The power consumption in the analog circuits (amplifiers and comparators) is computed by multiplying V_{bat} by the sum of the currents through all the branches of the circuit, denoted as I_{tot}. The power dissipated in the digital circuits (RS-latch, STP and gate drives) is computed by multiplying by V_{bat} the average current into the transistors [15]:

$$P_{diss} = V_{bat} I_{avg} = V_{bat} \frac{C_{tot} V_{bat}}{T_{sw}} = C_{tot} V_{bat}^2 f_{sw} \tag{4-31}$$

C_{tot} is the sum of the all the capacitances in the transistor (C_{gs}, G_{gd}, C_{ds}, C_{bs}...).

The power dissipated in resistors R_1, R_2, R_3 and R_4 due to the current I_{sense} through the current sense amplifier is equal to:

$$P_{sense} = \left(\frac{R_{sense} I_L}{R_1}\right)^2 (R_1 + R_2 \| (R_3 + R_4)) = 1.484 \times 10^{-5} \left(I_{out}^2 + \frac{\Delta I_{p-p}^2}{12}\right) W \qquad (4\text{-}32)$$

The maximum output current is 300 mA and maximum ripple current is 120 mA (using a 4.7 μH inductor). The maximum power dissipated is only 1.353 μW.

The power consumption of the control IC is calculated for V_{bat} of 3.6, 2.9 and 5.1 V and is summarized in Table 4-4. The total power consumption of IC is 3.631 mW when is V_{bat} 3.6 V. This is just over 10% of output power when the output current is 30 mA and is only 1% of output power when the output current is 300 mA. The power dissipated at V_{bat} of 2.9 V is 78% of the power consumption at 3.6 V while the power dissipation at 5.1 V is 1½ times larger. The extra power dissipated at 5.1 V does not matter since the battery is being charged and the charging source is providing power to the battery and the converter. Therefore, the power consumption in the IC when battery voltage is 3.6 V is an upper bound for efficiency calculations.

Table 4-4: Power consumption in the control IC.

Circuit	I_{tot} (μA)	C_{tot} (pF)	P_{diss} at 3.6 V	P_{diss} at 2.9 V	P_{diss} at 5.1 V
Error amplifier	135	-	0.486 mW	0.391 mW	0.742 mW
Current sense Amp.	180	-	0.648 mW	0.522 mW	0.990 mW
Slope compensation	5.4	-	0.019 mW	0.015 mW	0.029 mW
I_{offset}	7.5	-	0.027 mW	0.021 mW	0.042 mW
Current comparator	360	-	1.296 mW	1.043 mW	1.980 mW
Current limiter	180	-	0.648 mW	0.522 mW	0.990 mW
RS-latch	-	-	0.758 μW	0.491 μW	1.770 μW
Shoot-thru protect.	-	.039	1.458 μW	0.946 μW	3.400 μW
Gate drive (NMOS)	-	.075	0.253 mW	0.164 mW	0.590 mW
Gate drive (PMOS)	-	13	0.253 mW	0.164 mW	0.590 mW
I_{sense} (I_{out} =300 mA)	5	-	1.353 μW	1.353 μW	1.353 μW
Total P_{diss}. (mW)	-	-	3.631 mW	2.843 mW	5.959 mW

5 Simulation Results and Analysis

5.1 Overview

The buck converter and its control IC were simulated in ADICE to test their performance. The control system requirements tested are: steady state error and peak overshoot in the output voltage during step changes in output current. The input filter was tested for input current ripple attenuation. The tests were simulated for different values of input voltage, input and output filter inductors, temperature and variation in the compensator and IC process parameters.

The complete circuit simulated in ADICE is shown in Figure 5-1. The input and output filter capacitors, C_I and C_O, are modeled with their parasitic inductances and resistances. The input and output filter inductors, L_I and L_O, are modeled only with their DC resistances. From Chapter 2, the SRF of L_I is 100 while the SRF of L_O is 38 MHZ. Since the SRF is more than 25 times the switching frequency, the affects of the inter-winding capacitance can be ignored. The power MOSFETs, Q_1 and Q_2, used are the Si1555DL PMOS and NMOS devices. The spice models for these are available from Vishay Siliconix. The spice model for the schottky diode, D1, is for the ZHCS400 from Zetex. The ESR (~ 5-10 mΩ) of damping capacitor, C_D, is not included because it is much smaller than the damping resistance R_D (0.68-1.5 Ω). The ESL for the damping capacitor is not included due to convergence problems in the simulations. From section 2.3.3, the ESL of the damping capacitor is only 600 pF. At 1.5 MHz, it adds only 9 mΩ of impedance to the damping leg. Therefore, even if the ESL of the damping capacitor were included it would have little affect on the circuit operation. The battery is a SPICE voltage source. No battery impedance is included because that is the worst case scenario for the input filter. A SPICE current source, I_{out}, is used to model the DSP. The values for all the sources and passive components used for the different tests are summarized in Table 5-1.

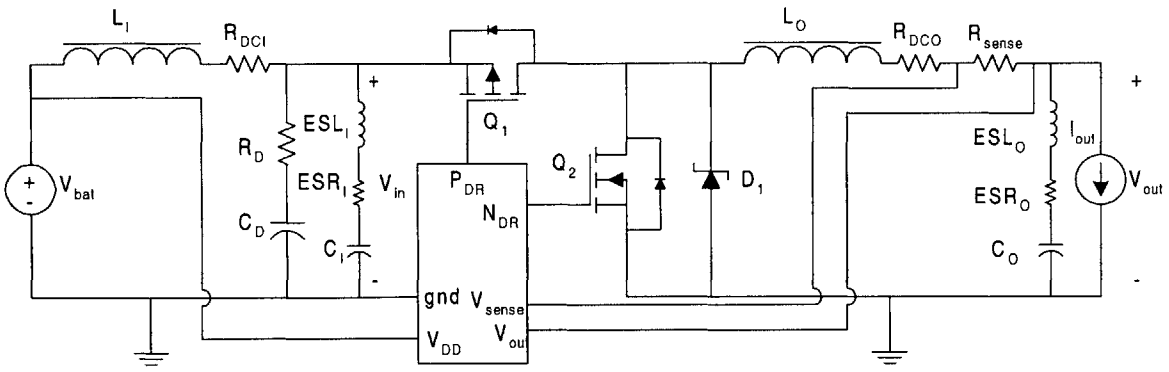

Figure 5-1: Synchronous buck converter and control IC used in the ADICE simulations. The input and output filter components are shown with their relevant parasitic elements.

Table 5-1: Component Values used in ADICE simulations

Component	Value
V_{bat}	2.9V, 3.6, 5.1V
L_I	1 μH
R_{DCI}	0.16 Ω
R_D	1 Ω
C_D	10 μF
ESL_I	600 pH
ESR_I	0.002 Ω
C_I	1 μF
L_O	4.7 μH, 10 μH
R_{DCO}	0.075 Ω
R_{sense}	0.15 Ω
ESL_O	633 pF
ESR_O	0.002 Ω
C_O	10 μF
I_{out}	30-300 mA

5.2 Output voltage response to step changes in output current

The most important task for the buck converter is to regulate the output voltage in the face of rapid and large changes in load current. The changing load current has the largest effect on the output voltage because if the converter cannot track the current, any difference between the current need by the DSP and the current provided by converter will come from the output filter capacitor. This can cause large swings in the output voltage.

As a result the buck converter's control system is required to maintain the output voltage at 1.2 with a steady state error of less than 1% (±12 mV). The voltage overshoot to a step in output current from 30 to 300 mA in 9 μsec should be no more than 5% (± 60 mV) and should settle back to within 1% of 1.2 volts is less than 20 μsec after the step.

5.2.1 Output voltage response for different output filter inductors

Figure 5-2 shows the output voltage response to step change in current for 4.7 μH and 10 μH output filter inductors. The output current and the current through the inductors is shown in Figure 5-3. The positive step occurs at 100 μsec and ends 9 μsec later. The negative step starts at 140 μsec and ends at 149 μsec. The simulation was done at a battery voltage of 3.6 V, IC junction temperature of 25° C and with nominal process models for the L46 CMOS process. The compensator pole and zero locations are also at their nominal locations.

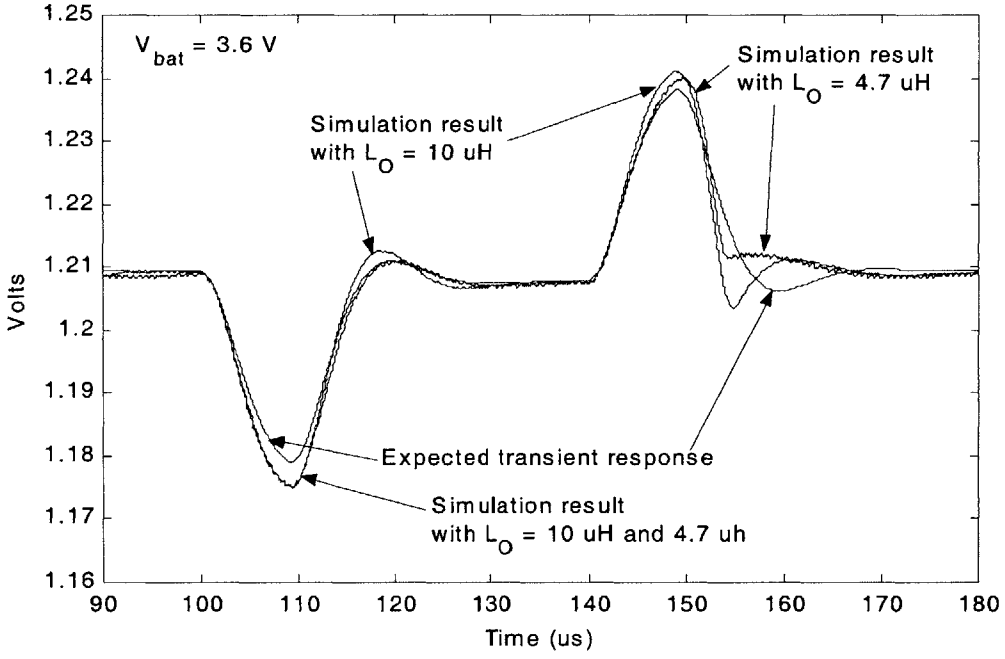

Figure 5-2: Output voltage transient response for L_O = 4.7 μH and 10 μH and V_{bat} = 3.6 V.

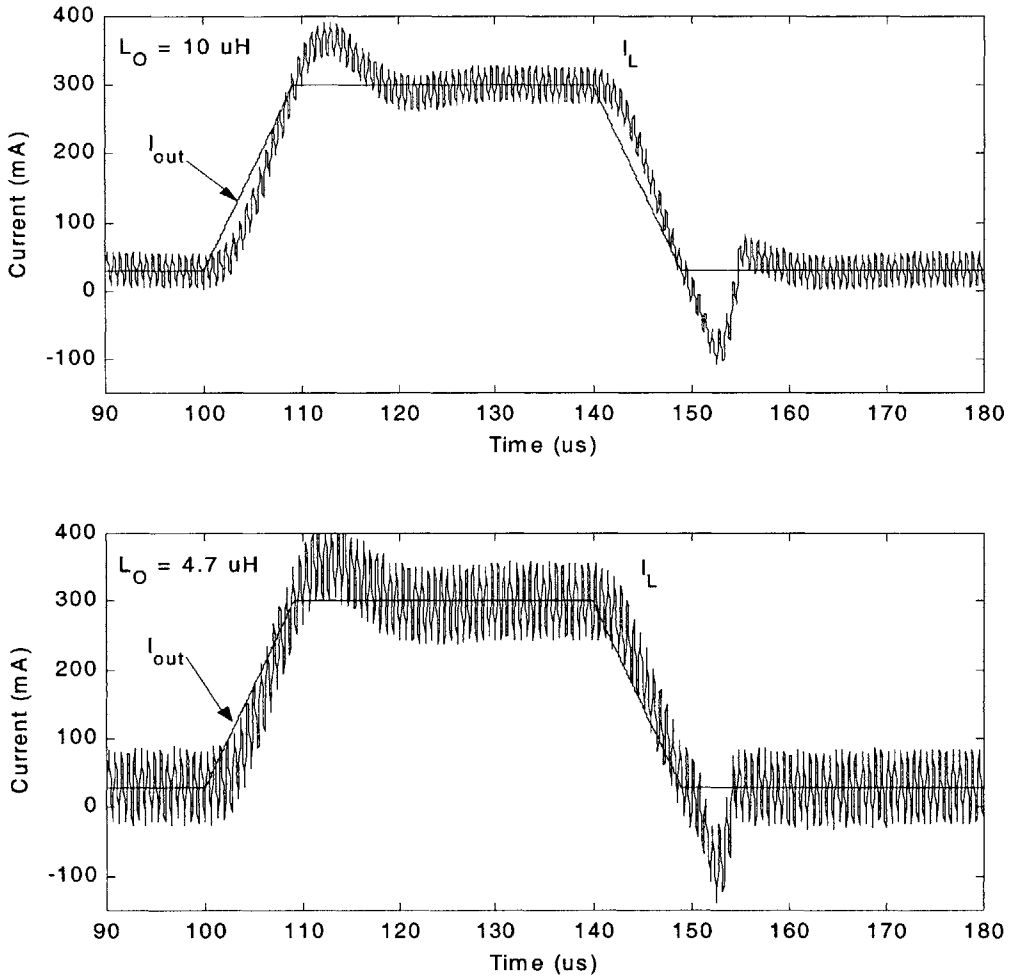

Figure 5-3: Inductor current for L_O = 10 μH and 4.7 μH during the step changes in I_{out}.

The steady state voltage for the converter from Section 3.4 is:

$$v_{out} = v_{ref} + \frac{1}{G_o}(v_{offset} - A_L i_{out}) \tag{5-1}$$

The offset voltage is 9.5 mV, AL is 0.5625 Ω and the DC gain of the compensator is 100. So for 30 mA of output current the steady state value of V_{out} should be 1.2093V and at an output current of 300 mA the steady state output voltage should be 1.2078 V. The simulation results show a steady state voltage of 1.209 V when I_{out} is 30 mA and 1.2075 V when I_{out} is 300 mA (Figure 5-4). The expected and simulated results are in good agreement at both output currents.

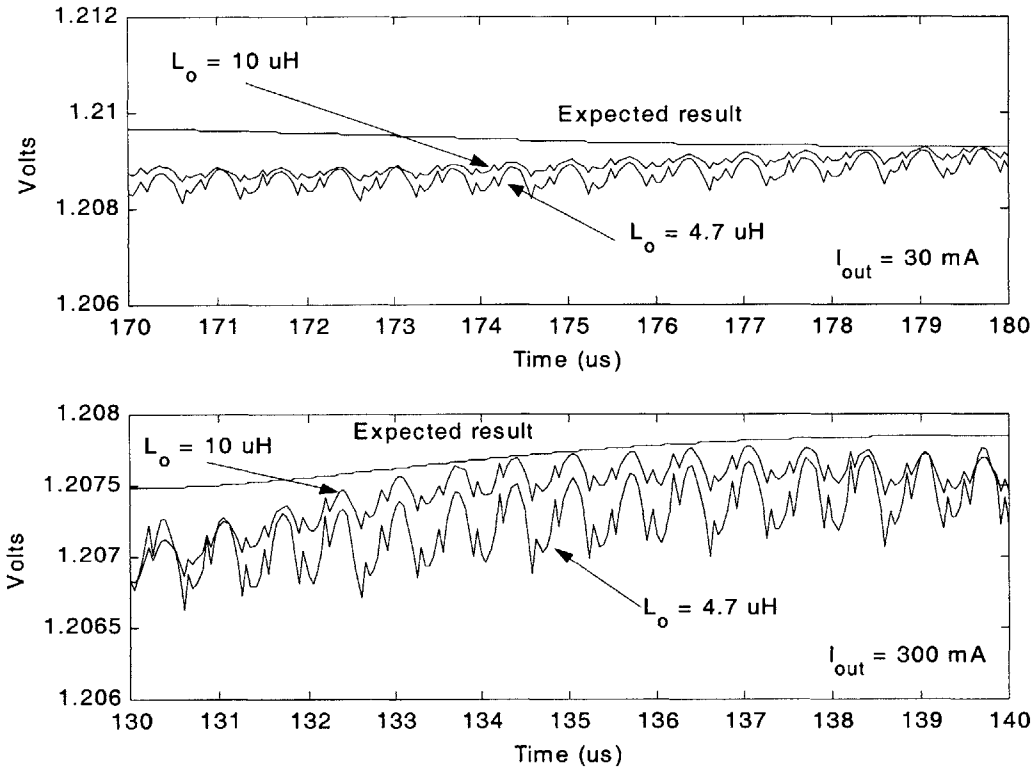

Figure 5-4: Steady-steady output voltage for I_{out} = 30 mA and 300 mA.

The peak-to-peak ripple voltage is only 0.21 mV in the converter with a 10 μH inductor and is 0.43 mV in the converter a 4.7 μH inductor. This is half of the expected ripple voltage of 0.43 mV and 0.921 mV for the 10 μH and 4.7 μH inductors, respectively. The discrepancy is due to the 633 pH of parasitic inductance of the output filter capacitor. The ESL of C_O causes a discontinuity in the ripple voltage, as seen in Figure 5-4, that reduces the overall magnitude by a factor of 2.

The ADICE simulations in Figure 5-2 show a slightly larger overshoot of the output voltage than predicted. The expected undershoot should be only 1.8% of 1.2 V or 1.1788 V. The simulations results are very close to this. The minimum output voltage during the step change in I_{out} is 1.175 V or 2.1% of 1.2 V. When the output current falls from 300 mA to 30 mA, the output voltage should not rise above 1.238 V (3.2 %). The output voltage rises to a peak of 1.241 V in

the simulation of the converter with a 10 μH inductor and rises to 1.24 V for a 4.7 μH inductor. These translate to 3.41 % and 3.33 % undershoot, respectively which is within the 5% overshoot requirement.

Notice that the output voltage response for the converter with 4.7 μH and 10 μH inductors are nearly identical even though the inductance is different by more than a factor of 2. This is to be expected since the gain-bandwidth product of the converter is independent of the inductor size. The variation in the inductance does not affect the high frequency dynamics of the converter near crossover and thus do not affect the closed loop response. The minor discrepancies are due to second-order effects not modeled in Chapter 3.

The discrepancy in the output voltage between the expected and simulation results when the current drops from 300 to 30 mA is not due to errors in modeling but in the implementation of the current sensing. The current sense amplifier creates a ground-referenced voltage that is proportional to the inductor current. However this is true only when the inductor current is positive (flows from the power stage to the output filter capacitor). If the inductor current goes negative the voltage across the terminals of the amplifier, Ai, is negative. Ai goes low turning of the pass transistor Q_{11}. The current sense amplifier effectively shuts off.

The peak overshoot of the output voltage occurs right at the end of the output current drop at 149 μsec (Figure 5-5). The inductor current undershoots and goes negative turning off the current sense amplifier. The current comparator trips when the following condition is reached:

$$1.2V + G_c(s)(1.2V - v_{out}) = V_{bias} + N_c t + A_L i_L \quad (5\text{-}2)$$

The term on the left is the output of the error amplifier/compensator and the term of the left is sum of the current sense amplifier and slope compensation (with bias voltage). This can be rearranged to:

$$G_c(s)\left(1.2V - v_{out} + G_c(s)^{-1}(V_{offset} - A_L i_L - N_c t)\right) = G_c(s)(1.2V - V_{out} - A_S i_L - V_1) = 0 \quad (5\text{-}3)$$

V_{offset} is 1.2 V – V_{bias}. $v_{out} - A_S i_L - V_1$ can be thought of as the effective output voltage of the converter from the standpoint of the error amplifier.

While the inductor current is negative the output voltage is larger than reference voltage by some ΔV. The difference between the positive and negative terminals of the error amplifier should be:

$$1.2V - v_{out} - A_S i_L - V_1 = -\Delta V - A_S i_L - V_1 = -\Delta V + A_S |i_L| - V_1 \qquad (5\text{-}4)$$

However, the actual difference between the positive and negative terminals of the error amplifier is $-(\Delta V+V_1)$ which is larger in magnitude. The error amplifier thinks the output voltage is larger than expected and drives the compensator harder to make the output voltage equal the reference voltage. This is why the output voltage falls faster in the ADICE simulation results than expected. When the inductor current goes positive again the current sense amplifier turns on and the control loop works as normal.

The output voltage of the converter with the 4.7 μH falls rapidly later than output voltage of the converter with the 10 μH. This is because the ripple current in the former is larger than in the latter. The larger ripple current means that the inductor current stays positive for a longer period of time so the current sense amplifier is on longer. The larger ripple current also means that the peak of the inductor current goes into positive territory faster. This translates to shorter period time for the current sense amplifier to be off and the output voltage of the converter with a 4.7 μH inductor does fall as low as the converter with a 10 μH inductor (Figure 5-5). For the 4.7 μH inductor simulation, the output voltage is 1.212 V when the current sense amplifier turns on and the control loop acts as normal. Since the output voltage is only 4 mV above the its steady state value, the error signal is small and the control loop slowly reduces the output voltage back to the steady state value of 1.2093 V. In the 10 μH simulation the output voltage is 1.203 V when the inductor current goes positive again. This is smaller than the steady state value so the control loop raises the output voltage back up to 1.2093 V with a small overshoot.

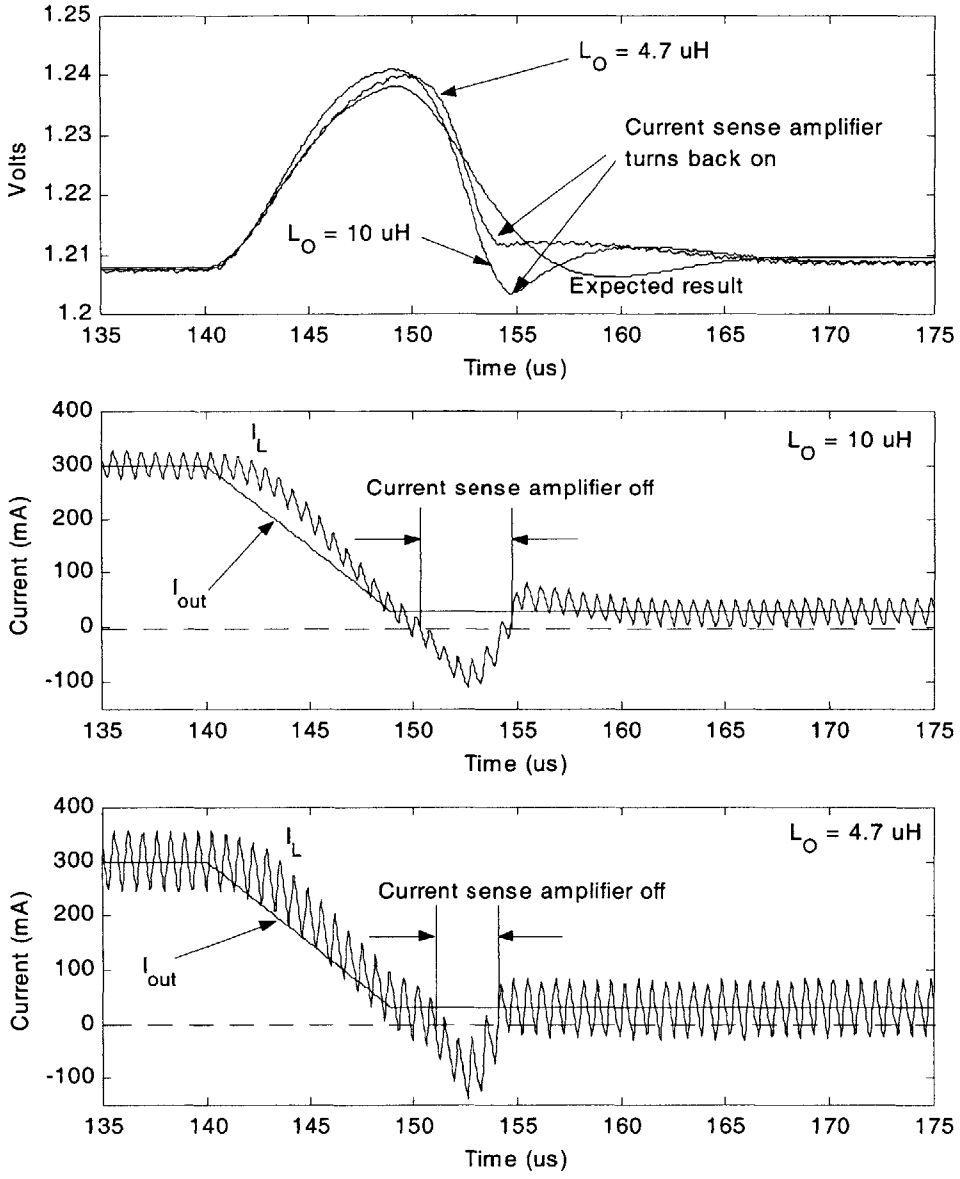

Figure 5-5: Top: Output voltage response when I_{out} steps down from 300 mA to 30 mA in 9 μsec. Middle: Inductor current in the converter with L_O = 10 μH during the step in I_{out}. Bottom: Inductor current in the converter with L_O = 4.7 μH during the step in I_{out}.

The output voltage transient responses for L_O of 4.7 μH and 10 μH were also simulated at 2.9 V and 5.1 V. The battery voltage is 2.9 V when it is fully discharged. When a three cell NiMH battery is being charged the voltage can rise up to 5.1 V. The simulation results are shown in Figures 5-6 and 5-7.

For V_{bat} of 2.9 V the steady state voltage is 1.209 V when I_{out} is 30 mA and 1.2072 V when I_{out} is 300 mA. The expected steady state voltages for I_{out} of 30 and 300 mA are 1.2093 V and 1.2078 V respectively. The simulations closely match the expected result. The minimum voltage during a positive step change is output current is 1.175 V for a 4. 7 μH inductor and 1.174 V for a 10 μH inductor. This translates to undershoot in the output voltage of 2.1% and 2.2 %, slightly larger than the 1.8% expected. The peak overshoot for the 4.7 μH inductor is 1.24 V (3.3%) and the peak overshoot for the 10 μH inductor is 1.242 V (3.5%) while the expected result is 3.2%.

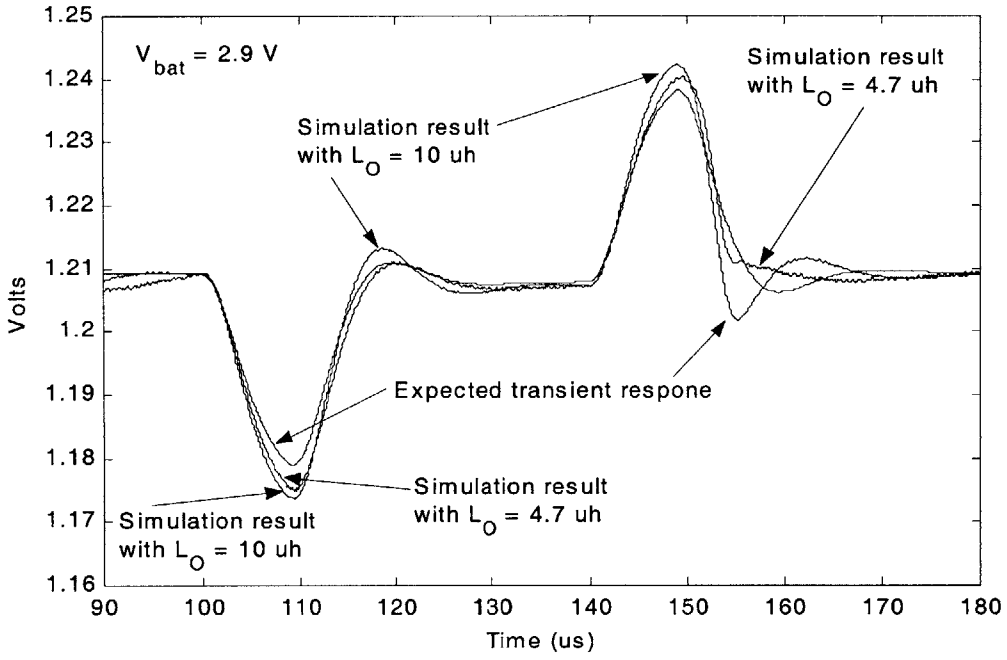

Figure 5-6: Output voltage transient response for L_O = 4.7 μH and 10 μH and V_{bat} = 2.9 V.

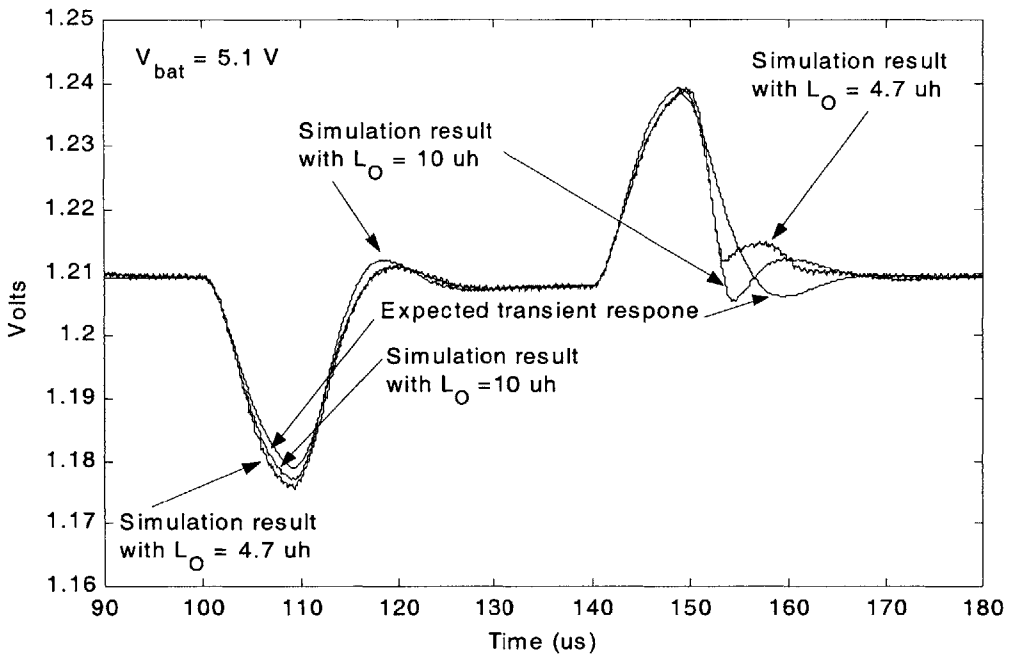

Figure 5-7: Output voltage transient response for L_O = 4.7 μH and 10 μH and V_{bat} = 5.1 V.

The output voltage transient response at 5.1 V is very similar to the voltage response at 2.9 V and 3.6 V. The steady state voltage is 1.2094 V when I_{out} is 30 mA and 1.2078 V when I_{out} is 300 mA. The peak undershoot in output voltage for the 4.7 μH inductor is 1.176 V (2 %) while the peak overshoot for the 10 μH inductor is 1.177 V (1.9 %). The peak overshoot of the output voltage for the 4.7 μH inductor and the 10 μH inductor is 1.239 V (3.25%).

5.2.2 Output voltage response for different battery voltages

It is important to verify that the output voltage transient response does vary significantly as the battery voltage changes. The battery voltage is nominally 3.6 V but can go as low as 2.9 V when it is fully discharged. The battery voltage can be as high as 5.1 V when it is being charged. The battery voltage varies by almost a factor of 2. The output voltage transient responses in Figure 5-2, 5-6 and 5-7 have been rearranged in Figures 5-8 and 5-9 to show the variation in the output voltage transient response for a fixed inductor value and for entire battery voltage range.

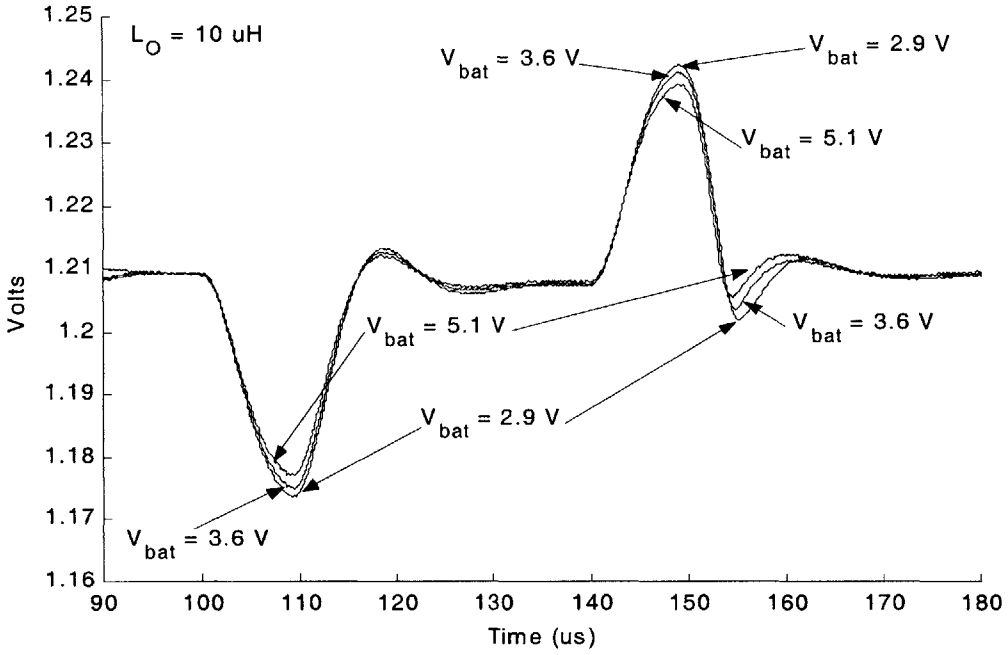

Figure 5-8: Output voltage transient response for L_O = 4.7 μH and V_{bat} = 2.9 V, 3.6 V and 5.1 V.

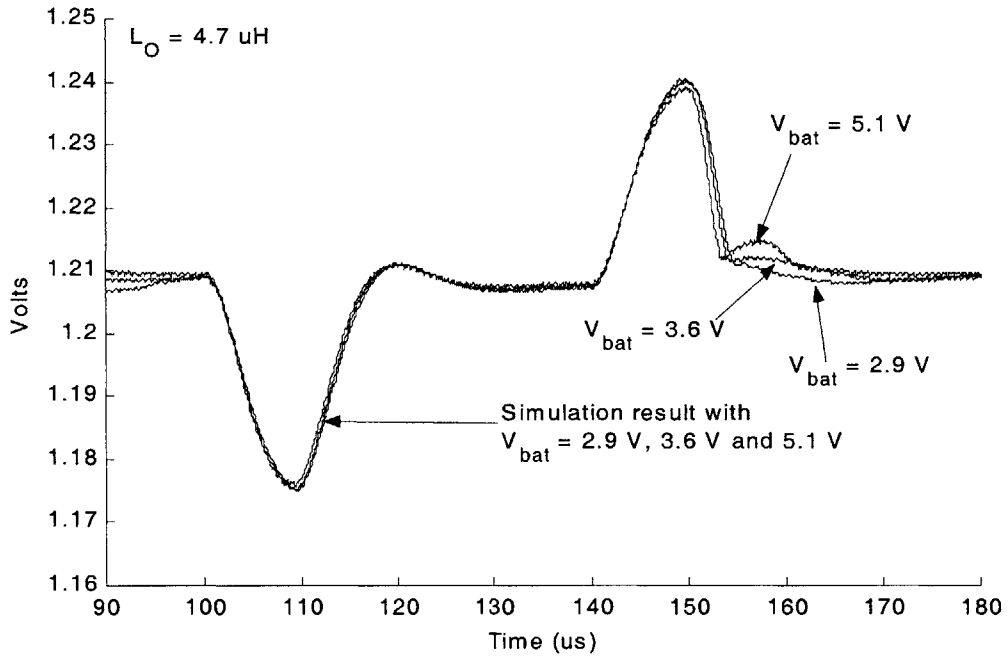

Figure 5-9: Output voltage transient response for L_O = 4.7 μH and 10 μH and V_{bat} = 5.1 V.

In chapter 3, transient response of the output voltage was predicted to be independent of input voltage because the gain-bandwidth product of the converter did not vary with V_{bat}. Figures 5-9 and 5-10 show that this is true. For L_O equal to 10 μH, the transient responses for the positive step change in current at different battery voltages are identical except that the peak undershoots vary slightly (Figure 5-8). The peak undershoot at 2.9 V is 1.174 while at 5.1 V the peak undershoot is 1.177 V. This is only a 3 mV (0.25 %) difference in the peak undershoot of the output voltage. The case is similar with the negative step change starting at 140 μsec. The peak overshoot at 2.9 V is 1.242 V while it only 1.239 V at a battery voltage of 5.1 V.

The variation in the output voltage response for different battery voltages is extremely small when the output filter inductor is 4.7 μH. The peak undershoot and overshoot vary by less than 1 mV as V_{bat} varies from 2.9 V to 5.1 V.

During the negative step change in output current (t = 140 – 180 μsec), the output voltage falls much more rapidly than expected as explained in the previous section. In Figure 5-8 the transient response at a battery voltage of 5.1 V falls the least while the transient response falls the most. This is because the ripple voltage is higher as the battery voltage increases. From Section 2.3.1 the peak-to-peak ripple current in the inductor is:

$$\Delta I_{p-p} = \frac{(1-D)TV_{out}}{L_O} \tag{5-5}$$

As the input voltage rises, the duty ratio, D, decreases, making the ripple current larger. The larger the ripple current the less time the current sense amplifier is off and the output voltage transient response does not fall as low during the negative step change in output current.

5.2.3 Output voltage response over temperature and process variations

So far the output voltage transient response has been simulated with junction temperature of the control IC at 25° C and with the nominal process models for TSMC's L46 0.25 μm CMOS process. However the closed loop converter is expected to meet performance specifications over

all temperature and process variations. The control IC of the converter is required to operate at junction temperatures from -40° C to 125° C while the power stage, input and output filters operate at maximum temperatures of 85° C.

There are two process variation models designated as FNFPFRFC and SNSPSRSC. The FNFPFRFC model is for fast NMOS transistors, fast PMOS transistors, "fast" resistances and "fast" capacitances. The NMOS and PMOS transistors are faster because their transconductance are larger than nominal. The resistances and capacitance are faster in the sense that they are smaller than nominal and any RC time constants are shorter. Since the transconductance of the transistors is relative to the mobility of their carrier species and mobility increases as temperature decreases, simulating at low temperature and with the FNFPFRFC process model represents one extreme of the process and temperature variation.

Similarly, the SNSPSRSC process model is for slow NMOS transistors, slow PMOS transistors, "slow" resistances and "slow" capacitances. The transconductances of the transistors is reduced making them slower. The resistors and capacitors are larger than their nominal value so any RC time constants are now much longer. Since the resistances increase with temperature and mobility/transconductance decrease with temperature, simulations done with the SNSPSRSC and at high temperature represent the other extreme of the process and temperature variation.

The output voltage transient response was simulated at the two process/temperature extremes: SNSPSRSC/125° C and FNFPFRFC/-40° C. The results are shown in Figure 5-10 along with the transient response at the nominal process and 25° C. The battery voltage is 3.6 V and the output filter inductor is 10 μH. The simulations were done with the compensator pole and zero at their nominal locations. In other words the RC network used for the compensator transfer function was not modified by the process and temperature variations for the purpose of this simulation.

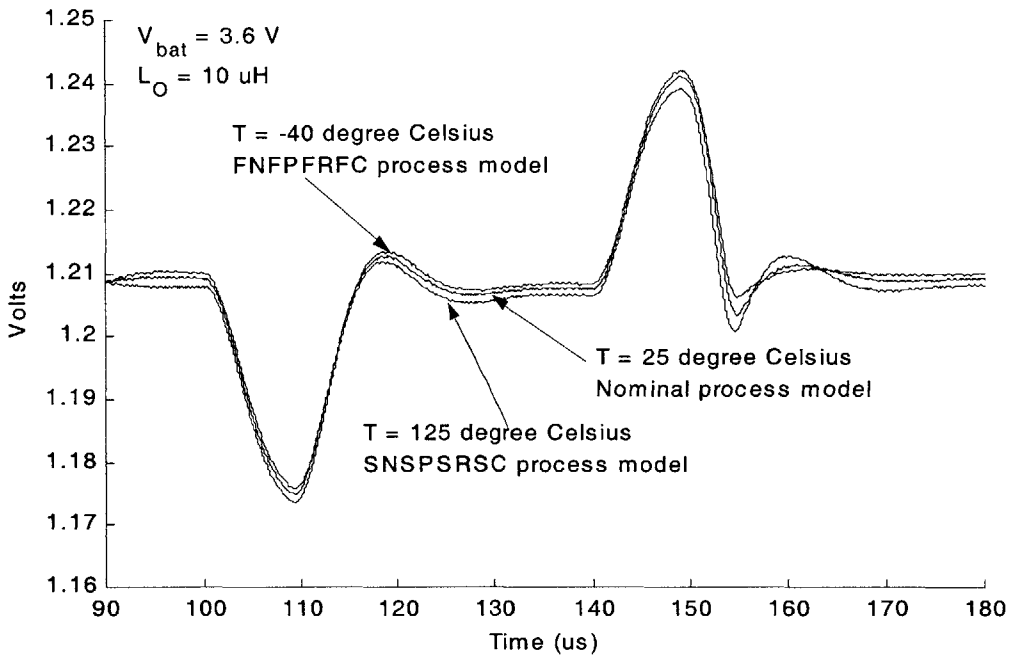

Figure 5-10: Output voltage transient response at different process/temperature extremes with V_{bat} = 3.6 V and L_O = 10 μH.

The simulation results show remarkably little variation in the transient response over process and temperature extremes. The only discrepancy is that the voltage response at the FNFPFRFC/-40° C extreme is shifted slightly above the nominal voltage response and voltage response at the SNSPSRSC/125° C extreme is shifted slightly lower than the nominal response. The steady state voltage at 30 mA of output current is 1.209 V nominally, 1.21 V for the FNFPFRFC/-40° C extreme and 1.2078 V for the SNSPSRSC/125° C. At 300 mA of output current the steady state voltages are 1.2075V, 1.2084 V and 1.2065 V for the nominal, FNFPFRFC/-40° C and SNSPSRSC/125° C simulations, respectively. The peak undershoot and overshoot of the output voltage differ by only 3 mV from the FNFPFRFC/-40° C and SNSPSRSC/125° C process/temperature extremes.

The shift in the voltage responses means the steady state error depends on temperature and process variations. The steady state output voltage is given by:

$$v_{out} = v_{ref} + \frac{1}{G_o}(v_{offset} - A_L i_{out}) \tag{5-6}$$

The offset voltage, v_{offset}, is equal to 1.2 V – 0.75(R1||(R2+R3)I_{offset}. For nominal conditions, I_{offset} is 7.5 μA and (R1||(R2+R3) is 44.44 kΩ and the offset voltage is 950 mV. For the SNSPSRSC/125° C process/temperature extreme, the resistors increase more than the transconductance of the current source, I_{offset}, decrease so that (R1||(R2+R3)I_{offset} is larger and the offset voltage reduces to 800 mV. For the FNFPFRFC/-40° C process/temperature extreme, the resistors decrease in value more than the transconductance of the current source, I_{offset}, increases so that (R1||(R2+R3)I_{offset} is smaller an the offset voltage is increases to 1.017 V.

The rest of the control IC does not affect the control loop significantly at the temperature and process extremes. The gain-bandwidth product of the error amplifier is 10 MHZ at nominal process conditions. At the SNSPSRSC/125° C process/temperature extreme the gain-bandwidth product can be reduced by 30% to 7 MHZ. Since the bandwidth of the voltage control loop is only 50 KHz, the variation in dynamics of the error amplifier does not affect the closed loop transient response. Similarly the bandwidth of the current sense amplifier will be reduced from 19.44 MHz to 13.6 MHz. Thus only the first nine harmonics of the switching frequency are within the bandwidth of the current sense amplifier. In Figure 4-9 the affect of the finite bandwidth of the current sense amplifier led to a rounding of the edges of the triangular inductor current. The reduced bandwidth, due to the SNSPSRSC/125° C process/temperature extreme, means that the sensed waveform will have more rounded edges. Since the rounded edges of the sensed inductor current do not affect the control loop, the reduced bandwidth of the current sense amplifier does not affect transient performance. Finally the delay from the time the current comparator trips high or low to the time the MOSFETs turn on or off is 35 ns. Even if this doubled due the process and temperature variations, the delay would reduce the phase margin by only 0.035° at the unity gain crossover frequency of 80 kHz.

5.2.4 Output voltage response with variation in the compensator

The pole and zero of the compensator, $G_c(s)$, are created using a RC network across the negative and output terminals of the error amplifier. The resistors have a tolerance of ±20% and the capacitor has a tolerance of ±30%. The tolerances are due to process variations and temperature affects. The resistors, however, can be matched to within 1% of one another.

The compensator pole and zero are equal to inverse of the product of the resistors and capacitor. The RC product varies from 56% to 156% of their nominal value. Therefore when the RC products are 56% of their nominal value, the pole and zero locations are pushed out to 178% of their nominal location. When the RC products are 156% of their nominal value, the pole and zero locations are pushed back to 64% of their nominal location.

Figure 5-11 shows the simulation result of the output voltage transient response with the compensator pole and zero at 64% of their nominal location, battery voltage of 3.6 V and a 10 μH output filter inductor. With the pole and zero at a lower frequency the control bandwidth is reduced. The voltage control loop cannot act as fast which leads to a larger overshoot in the output voltage. The steady state error, however, is unaffected because the DC gain of the compensator is the quotient of two resistors. The peak undershoot is predicted to be 1.1715 V (2.38%). The simulation shows a peak undershoot in output voltage of 1.1675 (2.7%), which is only 4 mV lower. The peak overshoot in output voltage is 1.2458 V (3.82%) and 1.2487 (4.06%) for the expected transient response and the simulation result, respectively.

Figure 5-12 shows the simulation result of the output voltage transient response with the compensator pole and zero at 178% of their nominal location with the battery voltage at 3.6 V and a 4.7 μH output filter inductor. Now that the pole and zero are at a higher frequency the control bandwidth is increased. The voltage control loop reacts much faster leading to a smaller overshoot in the output voltage. The peak undershoot is predicted to be 1.189 V (0.92%). The ADICE simulation shows a peak undershoot in output voltage of 1.1855 (1.21%), a difference of

only 3.5 mV lower. The peak overshoot in output voltage is 1.228 V (2.33%) and 1.229 (2.42%) for the expected transient response and the simulation result, respectively. The simulation results are in good agreement with the expected transient responses.

The simulation results for the variations in the compensator are shown in Figure 5-13. As predicted from chapter 3, the variation in the compensation resistors and capacitor result in the largest variation in the output voltage transient response. The peak undershoot can be anywhere from 1.21% to 2.7 % of the 1.2 V while the peak overshoot can be anywhere from 2.42% to 4.06% of 1.2 V. The peak overshoot and peak undershoot are within 5% of 1.2 V even with variations in the compensation resistors and capacitor. All transient responses settle to within 1% of 1.2 volts within 20 μsec of the current step and the steady state error is at most 9.4 mV or 0.783%.

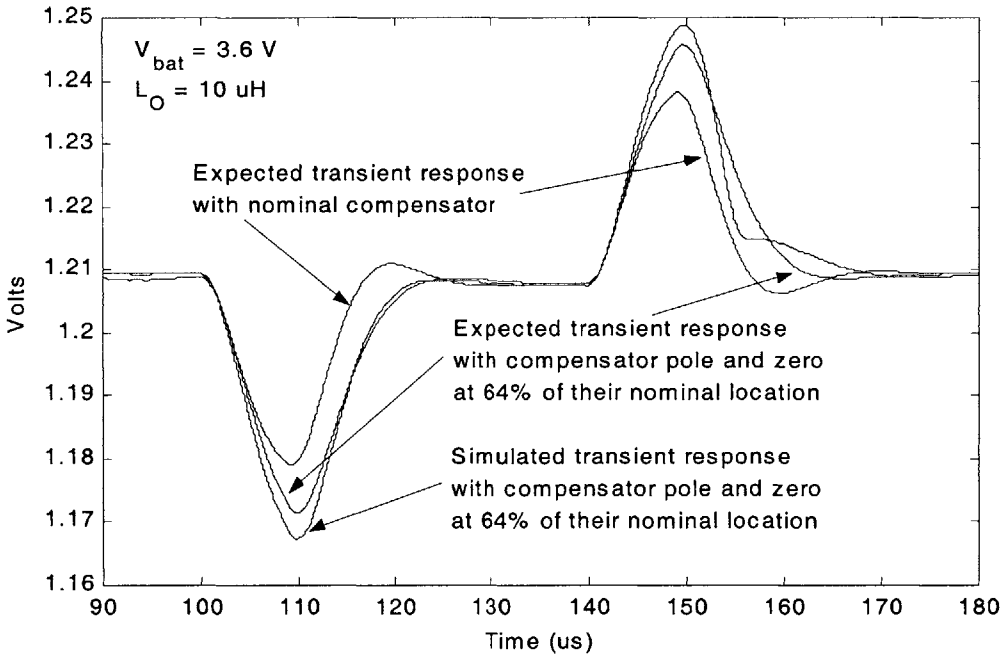

Figure 5-11: Output voltage transient response with compensator pole and zero at 64% of their nominal value.

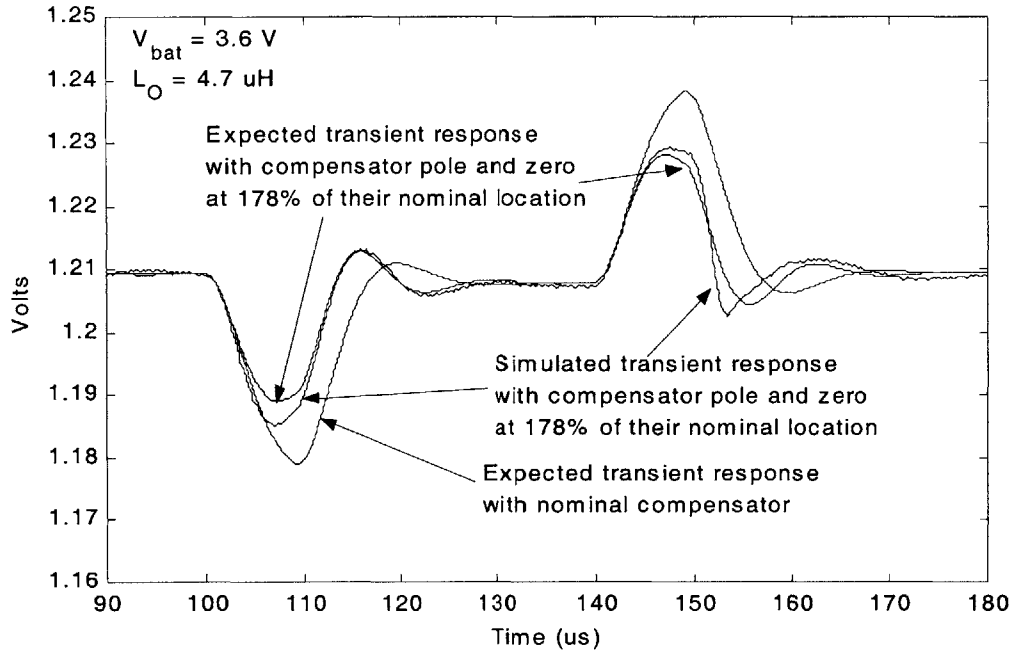

Figure 5-12: Output voltage transient response with the compensator pole and zero at 178% of their nominal location.

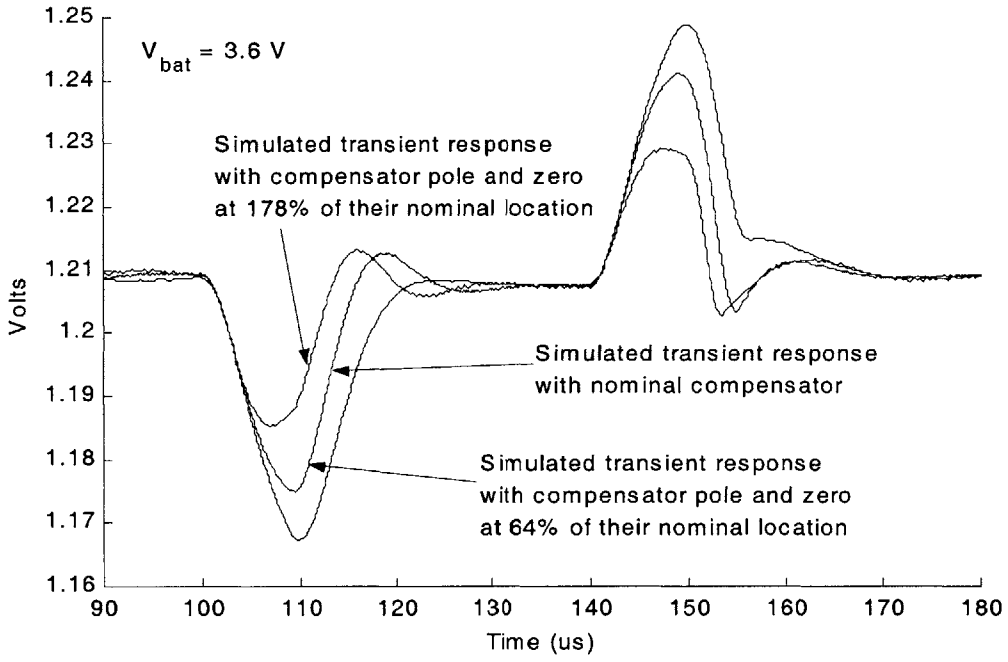

Figure 5-13: Output voltage transient response across the range of the compensator pole and zero location.

5.3 *Input filter performance*

5.3.1 Input current sourcing

With the input filter in Figure 5-1, the battery supplies only the DC current DI_{out} to the buck converter while the input filter capacitor sources the ripple current. The formula for the duty ratio of a buck converter including component resistance is:

$$D = \frac{V_{out} + (R_{dsn} + R_{DCO} + R_{sense})I_{out}}{V_{bat} - (R_{dsp} + R_{DCI} - R_{dsn})I_{out}} \tag{5-7}$$

For the Si1555DL power MOSFETs, R_{dsn} = 0.47 Ω and R_{dsp} = 0.67 Ω. R_{sense} is 0.15 Ω, R_{DCO} is 0.075 Ω and R_{DCI} is 0.16 Ω. The duty ratios when the battery voltage is 2.9 V, 3.6 V and 5.1 V at 300 mA of output current are 0.504, 0.403 and 0.282 respectively.

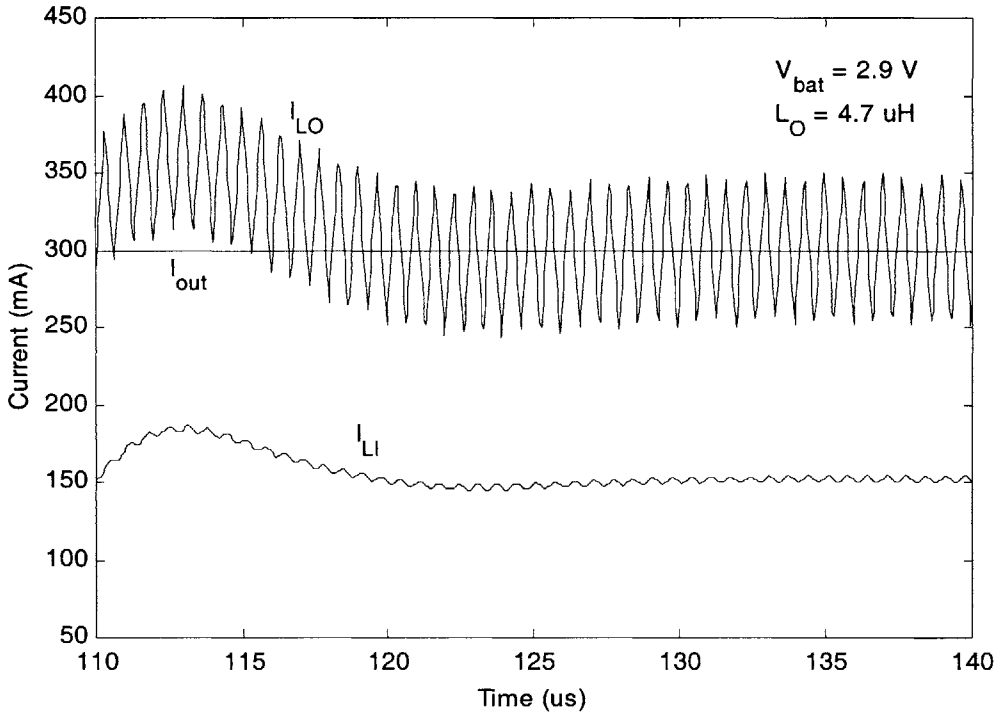

Figure 5-14: Current in the input and output filter inductors for L_O = 4.7 μH and V_{bat} = 2.9 V.

The current through the input filter inductor should be 151 mA when the battery voltage is 2.9 V. In Figure 5-14, the ADICE simulation of the current through the input filter inductor, I_{LI}, is 152 mA, which matches the predicted result. When the battery voltage is 3.6 V I_{LI} should be 121 mA. This is verified in Figure 5-15 where I_{LI} is 120 mA. When the battery is at its peak voltage of 5.1 V the current through the input filter inductor should be only 84.6 mA. The ADICE simulation in Figure 5-16 shows 83 mA of input current, which closely agrees with expected results.

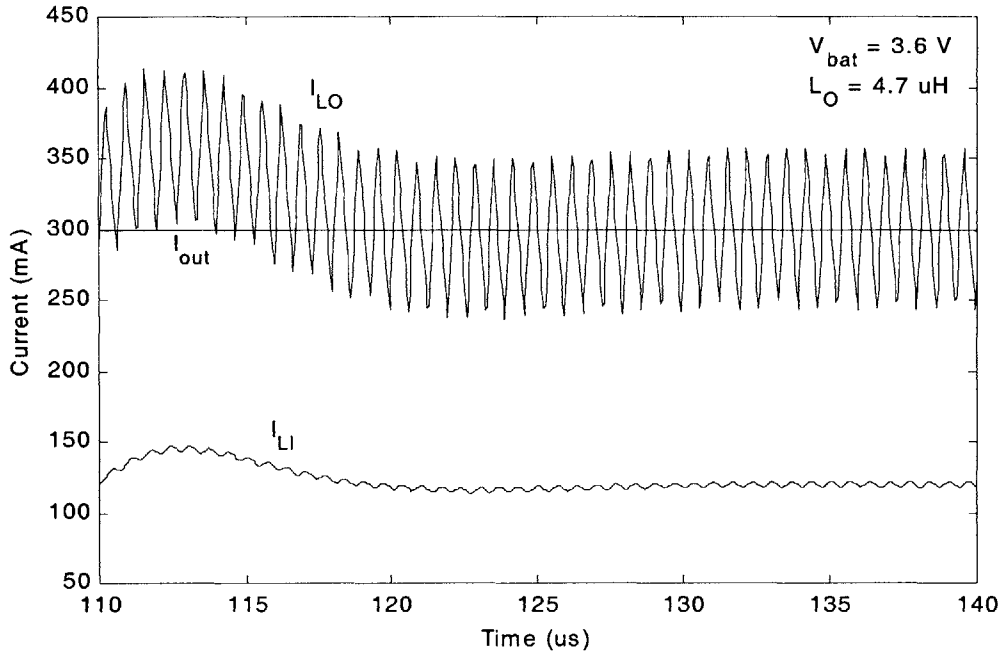

Figure 5-15: Current in the input and output filter inductors for $L_O = 4.7$ µH and $V_{bat} = 3.6$ V.

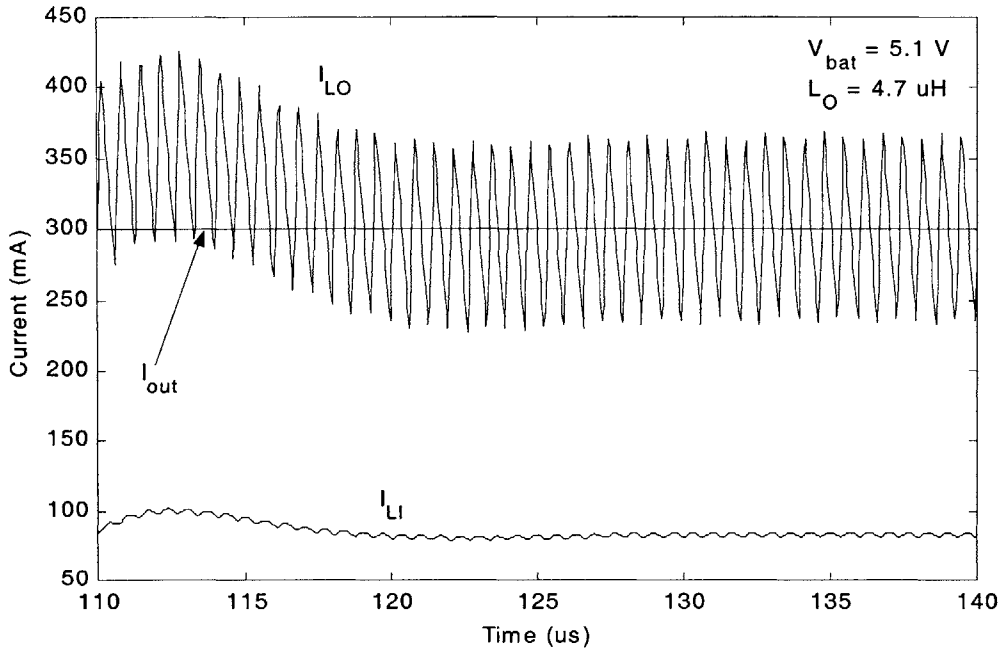

Figure 5-16: Current in the input and output filter inductors for $L_O = 4.7$ μH and $V_{bat} = 5.1$ V.

5.3.2 Input current ripple attenuation

Figures 5-14 through 5-16 show the current through the input filter inductor equal to DI_{out} with a small ripple current. The main purpose of the input filter is to reduce the ripple current from the battery to the power stage. The highest peak current occurs when the battery voltage is 5.1 V, the output current is 300 mA and a 4.7 μH output filter inductor is used. The peak output filter inductor current, $I_{out} + \frac{1}{2}\Delta I_{p\text{-}p,max}$, should be 361 mA, which is close to 363 mA peak current in Figure 5-16. The ripple current is equal to:

$$I_{ripple} = \frac{Z_c \parallel Z_d}{Z_c \parallel Z_d + Z_l} I_{peak} = \frac{0.1\Omega}{0.1\Omega + 0.96\Omega} 361\text{mA} = 3.7\text{mA} \qquad (5\text{-}8)$$

The ripple current should be 3.7 mA peak-to-peak. Figure 5-17 zooms in on the input filter inductor current in Figure 5-16. The ripple current in the ADICE simulation is slightly less at 3.2 mA peak-to-peak.

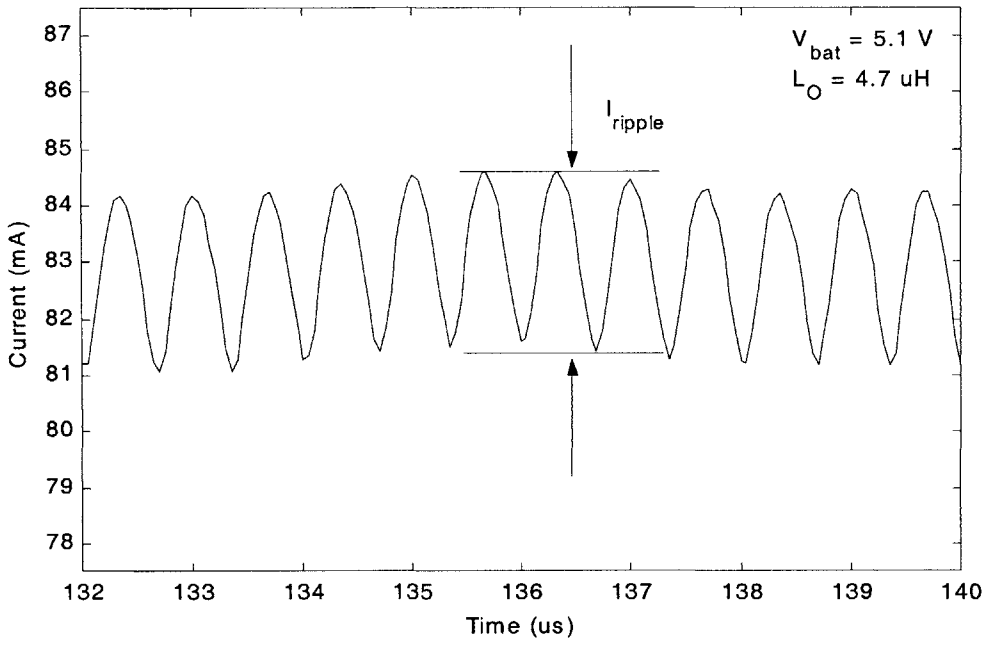

Figure 5-17: Ripple current in the input filter inductors for L_O = 4.7 μH and V_{bat} = 5.1 V.

5.4 Efficiency of the closed loop buck converter

Figure 5-18 shows the calculated efficiency of the closed loop buck converter for the three choices of power MOSFETs. The battery voltage is 3.6 V and the inductor used in the efficiency calculations is the 10 μH RL-1608-S10 .The other components used to calculate the efficiency are the ones used for the ADICE simulations and are listed in Table 5-1.

The converters using the Si1555DL and Si1303/4DL power MOSFETs have efficiencies greater than 70% for the entire 30 mA to 300 mA output current range, with peak efficiencies of 84.61 % and 84.87 %, respectively. The Si3585DV with its larger input capacitance and smaller on-stage resistance is more than 70% efficient when the output current is greater than 55 mA. The Si3585DV MOSFETs would still be a more suitable choice if the converter is expected to source 200-300 mA of current to the DSP most of the time. The efficiency the buck converter with the Si3585DV MOSFET pair stays above 85% in that current range whereas for the other two MOSFET pairs the efficiency drops in the 200-300 mA range.

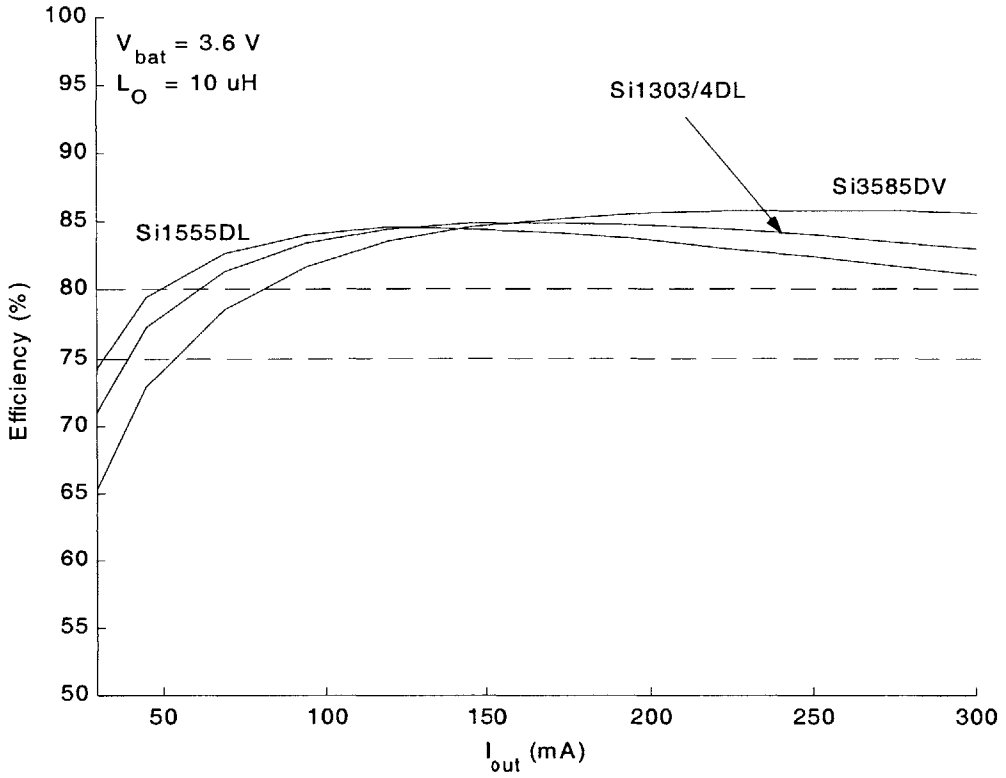

Figure 5-18: Efficiency of the closed loop buck converter for different power MOSFETs taken over the entire output current range.

The efficiency at 30 mA and 300 mA and the peak efficiency are listed in Table 5-2. The efficiencies of the converter can be misleading some times. At 30 mA of output current the converter with the Si1555DL MOSFETs is almost 9% more efficient than a converter using the Si3585DV MOSFETs. Since output power is only 36 mW, the converter using the Si3585DV MOSFETs consumes only 5.5 mW more than a converter with the Si1555DL MOSFETs. The efficiency of the Si3585DV converter is only 4.6% more efficient than the Si1555DL converter at 300 mA. However, since the output power is 360 mW, the Si1555DL converter consumes 24 mW more than the Si3585DV converter. Therefore when comparing efficiencies over a range of output power it is important to take note of amount of power lost at given operating points, and how much time is spent at these operating points.

Table 5-2: Peak efficiency and efficiency at minimum and maximum output current.

Power MOSFET	Peak efficiency	Efficiency at 30 mA	Efficiency at 300 mA
Si1555DL	84.61 % @ 120 mA	74.3 %	81 %
Si1303/4DL	84.87 % @ 170 mA	71.1 %	83 %
Si3585DV	85.77 % @ 250 mA	65.5 %	85.6 %

6 Conclusion

The design of a high frequency buck converter, and its control IC, suitable for cell phone power applications has been presented. The converter is able to operate over the entire voltage range of the cell phone battery (2.9 V – 5.1V) and can easily supply the 30 mA – 300 mA of current, at an output voltage of 1.2 V, that the cell phone DSP requires. A synchronous rectifier replaces the buck converter's free-wheeling diode to achieve greater efficiency at the low output voltage. The output filter produces a peak-to-peak output voltage ripple of 0.2 to 0.4 mV, which is an order of magnitude smaller than the 5 mV requirement. An input filter is included in the design to reduce EMI generated by the converter power stage. The input filter can reduce the converter current ripple of up to 376 mA peak-to-peak down to anywhere between 1.75 mA and 7.5 mA, a reduction of two orders of magnitude. All the elements in the input filter, output filter and power stage are surface mount components to save space.

The losses in power stage, input filter, output filter and control IC were analyzed to determine the overall efficiency of the converter. The target efficiency for the buck converter was 70% with a minimum of 50% over the 30 mA to 300 mA output current range. The buck converters using the Si1555DL and Si1303/4DL power MOSFETS and the 10 μH RL-1608-S10 inductor were found to over 70% efficient of the entire output current range an more than 80% efficient above 60 mA. Their peak efficiencies were just under 85% at output currents of 120 mA for the Si1555DL MOSFETs and 170 mA for the Si1303/4DL. A buck converter with the same inductor but using the Si3585DV power MOSFETs was at least 65% efficient and was more than 70% efficient above 55 mA of output current. The converter is more than 85% efficient when the output current is between 160 mA and 300 mA making it more suitable for DSP applications that continuously draw larger amounts of current.

The control IC for the converter was designed using the transistor models from TSMC's 0.25 μm CMOS process. The operation of the buck converter with its control IC was verified in

Analog Devices' SPICE simulator ADICE. The IC implemented current-mode control of the converter. Current-mode control provided a fast transient response to rapid changes in the output current. The transient response was found to independent of the input voltage and output filter inductor variation and varied very little over temperature and process variations. The greatest variation in the transient response of the converter was due to the large tolerances in the resistors (±20%) and capacitor (±30%) that set the pole and zero locations of the compensator. The compensator was therefore designed to meet transient and steady state error requirements in the presence of large variation in the location of its pole and zero. The peak overshoot in output voltage when the output current rose from 30 mA to 300 mA step in 9 μsec was no more that 4%. The output voltage settled backed to within 1% of 1.2 V in less than 20 μsec. The steady state error in output voltage was at most 10 mV, which is within the ±1% steady state error requirement.

The next step towards introducing a switching power supply for the cell phone DSP is to verify the closed loop performance of the discrete components used in the power stage, input and output filters using an off the shelf control IC. Once that is done the IC presented here can be fabricated and tested. Once the IC and the discrete components work together successfully a complete switching power supply will be ready for use in a cell phone.

7 References

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8 Appendix A: Losses in MOSFETs

This section covers the formulas used to calculate MOSFET switching, capacitive and conduction losses for a buck converter with a PMOS high-side switch, an NMOS low-side switch and anti-parallel schottky diode for synchronous rectification, as shown in Figure 8-1. The switch model and waveforms used is from pages 545 – 550 of [13]. The inductor is modeled as an ideal current source. I_L is equal to $I_0 - \frac{1}{2}I_{ripple,p\text{-}p}$ when the low-side switch is turned off and the high-side switch is turned on. It is equal to $I_0 + \frac{1}{2}I_{ripple,p\text{-}p}$ when the high-side switch is turned off and the low side switch is turned on to account for the ripple current through the inductor.

The parasitic capacitances of the MOSFETs are assumed to be of the form:

$$C_i = \frac{C_{i0}}{\sqrt{1 + V_{DS}/V_{i0}}} \tag{8-1}$$

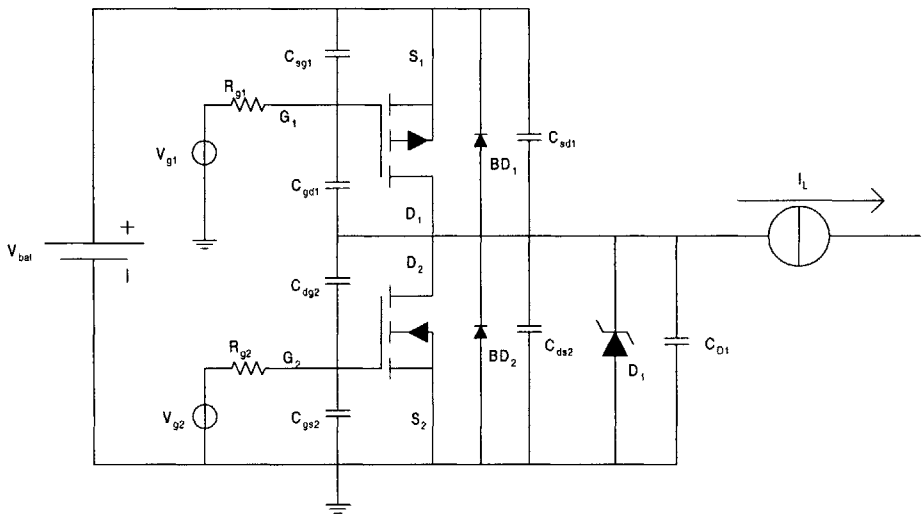

Figure 8-1: Loss model for voltage driven complementary MOSFET pairs in a synchronously rectified buck converter.

C_{i0} is the capacitance at $V_{DS} = 0$. The capacitance for the schottky diode does not fit that model and the energy dissipated has to be calculated numerically. The input capacitance C_{iss} is defined as $C_{gs} + C_{gd}$ at $V_{DS} = 0$. The output capacitance, C_{oss} is defined as $C_{gd} + C_{ds}$ at $V_{GS} = 0$.

8.1 High side switching losses

The power dissipated in the switching transitions of the high-side PMOS transistor when it is turned on is:

$$P_{high-side,on} = f_{sw}\left[\frac{1}{2}I_L T_1 (V_{bat} + 2V_{D1}) + I_L V_{hd} T_2\left(\alpha^2 - \alpha\beta T_2 + \frac{\beta^2 T_2^2}{3} - 1\right)\right] \quad (8\text{-}2)$$

Where T_1 is the time it takes for the current through the high-side switch to go from 0 to I_L,

$$T_1 = R_{g1} C_{issp} Ln\left(\frac{V_{gh1} - V_{th1}}{V_{gh1} - V_{s1}}\right) \quad (8\text{-}3)$$

T_2 is the time it takes for the voltage across the PMOS switch to go to zero:

$$T_2 = \frac{1}{\beta}\left[\alpha - \sqrt{1 + \frac{I_L R_{ds1,on}}{V_{hd}}}\right] \quad (8\text{-}4)$$

and:

$$\alpha = \sqrt{1 + \frac{V_{bat} + V_{D1}}{V_{hd}}} \quad (8\text{-}5)$$

$$\beta = \frac{(V_{gh1} - V_{s1})}{2V_{hd} R_{g1} C_{gd0}} \quad (8\text{-}6)$$

The power lost during high side turn off transition is:

$$P_{high-side,off} = f_{sw}\left[I_L V_{hd} T_3\left(\sigma^2 - \sigma\delta T_3 + \frac{\delta^2 T_3^2}{3} - 1\right) + \frac{1}{2} I_L T_4 (V_{bat} + 2V_{D1})\right] \quad (8\text{-}7)$$

$T_3 = \frac{1}{\delta}(\alpha - \sigma)$ is the time it takes for the voltage across the PMOS switch to rise from 0 to V_{bat} + V_{D1}. $T_4 = R_{g1}C_{issp}Ln\left(\frac{V_{s1}}{V_{th1}}\right)$ is the time it takes for the current through the PMOS switch to fall to zero. For T_1 and T_4, C_{issp} is the input capacitance when V_{DS} = V_{bat} + V_{D1}. For the above formulas:

$$\sigma = \sqrt{1 + \frac{I_L R_{ds1,on}}{V_{hd}}} \tag{8-8}$$

$$\delta = \frac{V_{s1}}{2V_{hd}R_{g1}C_{gd0}} \tag{8-9}$$

8.2 Low side switching losses

The NMOS switch has a much smaller switching loss due to the fact that its drain to source voltage is at equal to the negative of the forward voltage of the schottky diode (-0.3V – -0.4V) because the diode is conducting when the low-side switch is turned on and off. The input capacitance is considered to be constant and equal to C_{issn0}. The time it takes for the NMOS to carry the load current I_L is $T_5 = R_{g2}C_{issn0}Ln\left(\frac{V_{gh2} - V_{th2}}{V_{gh2} - V_{s2}}\right)$. Once the low-side switch is carrying full output current, the schottky turn off and the power dissipated is:

$$P_{low-side,on} = f_{sw}I_L V_{D1}T_5 \tag{8-10}$$

The turn-off switching losses are similar to the turn-on loss. $T_6 = R_{g2}C_{issn0}Ln\left(\frac{V_{s2}}{V_{th2}}\right)$ is the time it takes for the current through the NMOS to go to zero. It is assumed that the voltage across the diode equals it forward voltage as soon as current starts to flow through it. The power lost in the turn off transition is:

$$P_{low-side,off} = f_{sw}I_L V_{D1}T_{13} \tag{8-11}$$

8.3 Capacitive turn-on losses

High-side and low-side capacitive turn-on losses are calculated by multiplying the total energy stored in the capacitance times the switching frequency.

$$P_{cap.} = f_{sw}\int_{V_{min}}^{V_{max}} C_{oss}(V_{DS})V_{DS}dV_{DS} \tag{8-12}$$

V_{min} is assumed to be 0V when the MOSFET is on. For the PMOS, $V_{max} = V_{bat} + V_{D1}$, while for the NMOS, $V_{max} = V_{bat}$. Computing the above integral, the turn off losses for the MOSFETs are:

$$P_{high-side,cap.} = 2f_{sw}C_{osspo}V_{h0}^2\left(A^3/3 - A + 2/3\right) \tag{8-13}$$

$$P_{low-side,cap.} = 2f_{sw}C_{ossn0}V_{l0}^2\left(B^3/3 - B + 2/3\right) \tag{8-14}$$

Where,

$$A = \sqrt{1 + \frac{V_{bat} + V_{D1}}{V_{h0}}} \tag{8-15}$$

$$B = \sqrt{1 + \frac{V_{bat}}{V_{l0}}} \tag{8-16}$$

8.4 Gate drive losses

Gate drive losses are determined empirically from the gate charge vs. gate to source voltage plots on the MOSFET data sheets.

8.5 Conduction Losses

The total conduction loss is the just the square of the rms current through the MOSFETs times their on-state resistance.

$$P_{conduction} = \left[I_0^2 + \frac{1}{12}\left(\frac{(1-D)V_0}{Lf_{sw}}\right)^2\right]\left(DR_{ds1,on} + (1-D)R_{ds2,on}\right) \tag{8-17}$$

9 Appendix B: Inductor loss testing

This appendix illustrates the method used to measure inductor loss. The surface mount power inductors used for the output filter were tested to determine their average power loss over one switching cycle. Due to the complex and nonlinear nature of the core loss in the inductor, it is best to experimentally verify that the loss is small. Three 10 μH surface mount power inductors were tested, the RL-1608-S10 from Renco, the SMPI20 from Wilco and the DS1608C from Coilcraft.

The test setup is shown in Figure 9-1. It consists of the power stage of the buck converter driving the inductor and a resistive load R_L. The power stage consists of the Si1555DL power MOSFETs and the B0520WS schottky diode. The power stage is driven using the TPS2812 gate drive chip from Texas Instruments. The load, R_L, consists of a 3.3 Ω resistor in series with a 0-50 Ω potentiometer. A function generator produces a square wave that is fed into the input pin of the TPS2812. The duty ratio of the square wave is adjusted, typically between 0.34 and 0.38, until the average voltage across R_L is 1.2 V. Since R_L varies from 3.3 to 53.3 Ω, the inductor can be tested with load currents from 22.5 mA to 363 mA.

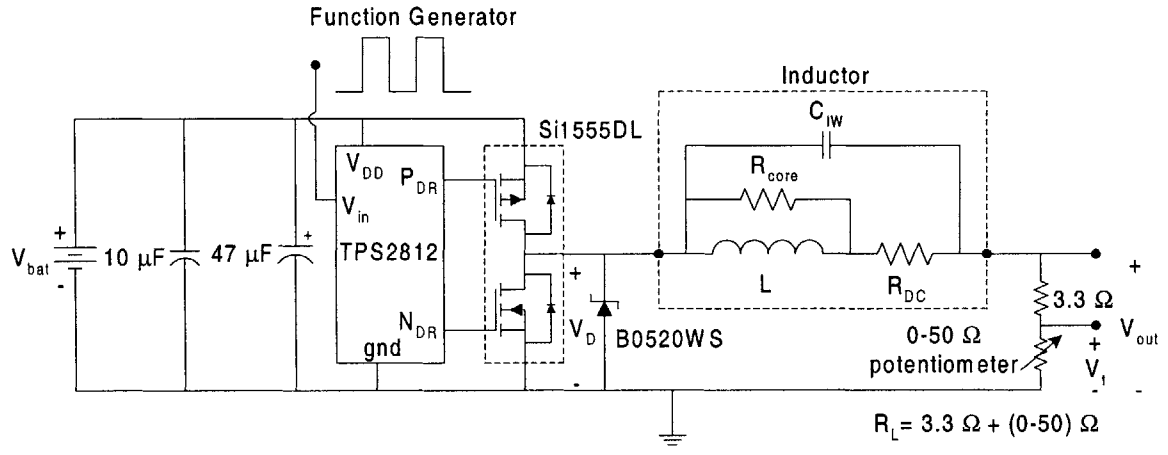

Figure 9-1: Test setup for measure average inductor power loss.

The average power in the inductor is defined as:

$$P_{avg} = \frac{1}{T}\int_{T}(V_D - V_{out})\frac{V_{out}}{R_L}dt \tag{9-1}$$

The voltage across the diode, V_D, and the load resistor, V_{out}, was measured using a LeCroy LC57A 1 GHz oscilloscope. The oscilloscope is capable of taking the difference between V_D and V_{out} and multiplying that difference by V_{out}. Using the cycle-to-cycle average function on the scope the power per unit resistance lost in the inductor can be determined:

$$P_{avg}R_L = \frac{1}{T}\int_{T}(V_D - V_{out})V_{out}dt \tag{9-2}$$

To find the load resistance the voltage across the potentiometer, V_t, is taken. The current through the load resistance can be found using:

$$I_{out} = \left\langle \frac{V_{out} - V_t}{3.3\Omega} \right\rangle \tag{9-3}$$

The <> symbol stands for the average of a variable of time. The load resistance can be than determined by:

$$R_L = 3.3\Omega + \frac{V_t}{I_{out}} \tag{9-4}$$

With the power per unit resistance lost in the inductor and the load resistance known the loss in the inductor can now be determined. The potentiometer resistance can be varied so that the loss over the 30 mA to 300 mA current range of the converter can be found.

10 Appendix C: MATLAB code

```
function [Y] = Ploss(X)
 'function Ploss computes the various losses in the power MOSFETs of a buck converter'

I_o = X(1);
g_fs1 = X(2);
g_fs2 = X(3);
T_o1 = X(4);
T_o2 = X(5);
C_issh = X(6)*1e-12;
C_issoh = X(7)*1e-12;
C_gdo = X(8)*1e-12;
C_ossoh = X(9)*1e-12;
C_issol = X(10)*1e-12;
C_ossol = X(11)*1e-12;
R_dsonh = X(12);
R_dsonl = X(13);
V_t1 = X(14);
V_t2 = X(15);
V_hd = X(16);
V_ho = X(17);
V_lo = X(18);
E_gateh = X(19);
E_gatel = X(20);

V_o = 1.2;
f_sw = 1.5e6;
alpha = .9;
beta = .9;
I_lkg = .0002;
I_delta = .06;
T = 50;
Rgh = 10;
Rgl = 10;
V_gh = 3;
V_d2 = .32;
V_bat = 3.6;
E_diode = 1.4e-9;

D = V_o/V_bat;
Rdsh = R_dsonh*(1+(T-25)/T_o1);
Rdsl = R_dsonl*(1+(T-25)/T_o1);
tau1 = Rgh*C_issh;
tau2 = Rgh*C_issoh;
I1 = I_o - I_delta/2;
I2 = I_o + I_delta/2;
V_s1 = V_t1 + I1/g_fs1;
```

```
V_s2 = V_t2 + I2/g_fs2;
A = (1+(V_bat+V_d2)/V_hd)^.5;
B = (V_gh - V_s1)/(2*V_hd*Rgh*C_gdo);
C = (1+(I1*Rdsh)/V_hd)^.5;
E = V_s2/(2*V_hd*Rgh*C_gdo);

T_1 = tau1*log(V_gh/(V_gh-V_t1));
T_2 = tau1*log(V_gh/(V_gh-V_s1)) - T_1;

T_4 = (A-C)/B;
T_5 = tau2*log((V_gh-V_s1)/(V_gh*(1-alpha)));

E_2 = .5*I1*(V_bat + 2*V_d2)*T_2;
E_4 = I1 * T_4 *V_hd*(A^2 - A*B*T_4 + ((B*T_4)^2)/3 -1);


Y(1) = T_1+T_2+T_4+T_5;
Y(2) = (E_2 + E_4)*f_sw;

T_6 = tau2*log(V_gh/V_s2);
T_7 = (A-C)/E;
T_8 = tau1*log(V_s2/V_t1);

E_7 = I2 * T_7 * V_hd*(C^2 + C*E*T_7 + ((E*T_7)^2)/3 -1);
E_8 = .5*I2*(V_bat + 2*V_d2)*T_8;

Y(3) = T_6+T_7+T_8;
Y(4) = (E_7 + E_8)*f_sw;

tau3 = Rgl *C_issol;

T_9 = tau3*log(V_gh/(V_gh - V_t2));
T_10 = tau3*log(V_gh/(V_gh - V_s2)) - T_9;
T_11 = tau3*log(1/(1-beta));

E_10 = I2*V_d2*T_10;

Y(5) = T_9+T_10+T_11;
Y(6) = f_sw*E_10;


T_12 = tau3*log(V_gh/V_s1);
T_13 = tau3*log(V_gh/V_t2) - T_12;

E_13 = I1*V_d2*T_10;

Y(7) = T_12+T_13;
Y(8) = f_sw*E_10;


G = (1 + (V_bat + V_d2)/V_ho)^.5;
```

```
H = (1 + V_bat/V_lo)^.5;


E_outh = 2*C_ossoh*(V_ho)^2 * (G^3/3 - G + 2/3);
E_outl = 2*C_ossol*(V_lo)^2 * (H^3/3 - H + 2/3);

Y(9) = f_sw*E_gateh;
Y(10) = f_sw*E_gatel;
Y(11) = f_sw*E_outh;
Y(12) = f_sw*E_outl;
Y(13) = f_sw*E_diode;

K = (I_o)^2 + (I_delta)^2/12;


Y(14) = K*D*Rdsh;
Y(15) = K*(1-D)*Rdsl;
Y(16) = (1-D)*V_d2*I_lkg;

Y(17) = Y(2) + Y(4) + Y(6) + Y(8)+ Y(9)+ Y(10) + Y(11) + Y(12) + Y(13) + Y(14)+ Y(15) +
Y(16);
Y(18) = 100*Y(17)/(X(1)*V_o);
```

```
function [m, n, o, p, q, r, s, t, u, v, w, x, y, z] = Sploss(u)
'function Sploss calculates the losses for a particular pair of power MOSFETs and converts losses
from watts to milliwatts'

D = [u 3 2.05 187.5 200 324 432 153 243 250 175 .28 .16 1 .9 .371 .62 .844 4e-9 2.9e-9];
'D = [u .6 .645 167 167 313 480 253 667 223 361.5 .21 .16 1.2 1.16 .308 .744 1.3 4.546e-9 2.04e-
9];'
'D = [u .5 .75 250 200 120 260 177 314 182.7 182.7 .69 .355 .9 1 .2 .41 .334 2.67e-9 1.72e-9];'
Y = Ploss(D);
m = Y(2)*1000;
n = Y(4)*1000;
o = Y(6)*1000;
p = Y(8)*1000;
q = Y(9)*1000;
r = Y(10)*1000;
s = Y(11)*1000;
t = Y(12)*1000;
u = Y(13)*1000;
v = Y(14)*1000;
w = Y(15)*1000;
x = Y(16)*1000;
y = Y(17)*1000;
z = Y(18);
```

```
'Script Mosloss.m plots losses computed using Sploss as functions of output current'

for i = 1:161
   I = .030+ (i-1)*.003;
   iout(i) = I*1000;
   op(i) = 1.2*I*1000;
   [m(i) n(i) o(i) p(i) q(i) r(i) s(i) t(i) u(i) v(i) w(i) x(i) y(i) z(i)] = Sploss(I);
end


figure(1)
subplot(2,1,1)
plot(iout,m)
hold on
plot(iout,n,'--')
xlabel('I_o (mA)')
ylabel('Power loss (mW)')
title('High side turn on (solid) and turn off (dashed) switching losses')
axis([30 300 0 6]);
subplot(2,1,2)
plot(iout,q)
hold on
plot(iout,r,'--')
hold on
xlabel('I_o (mA)')
ylabel('Power loss (mW)')
title('High side (solid) and low side (dashed) gate drive losses')
axis([30 300 0 10]);


figure(2)
subplot(2,1,1)
plot(iout,s)
hold on
plot(iout,t,'--')
Hold on
plot(iout,u,'-.')
xlabel('I_o (mA)')
ylabel('Power loss (mW)')
title('High (solid), Low (dashed) side and Schottky (dash-dot) capacitive losses')
axis([30 300 0 5]);
subplot(2,1,2)
plot(iout,v)
hold on
plot(iout,w,'--')
xlabel('I_o (mA)')
ylabel('Power loss (mW)')
title('High side (solid) and Low side (dashed) conduction loss')
axis([30 300 0 15]);
```

```
figure(3)
hold on
plot(iout,z,'--')
hold on
plot(iout,300/7*op./op,'-')
xlabel('I_o (mA)')
ylabel('%')
title('Percentage loss for Si3585DV (dashed) and Si1304DL/TP0101T (dash-dot) MOSFET
Pairs')
axis([30 300 0 100]);
```

```
'Ifilterloss.m computes power loss in the output filter'

Rdc = .16;
Rp = .050;
L = 1e-5;
f = 1.5e6;
Vo = 1.2;
D = .41;
dI = (1-D)*Vo/(L*f);

I1 = [.0251 .0448 .0685 .0933 .119 .145 .172 .198 .224 .251 .277 .303 .325];
Io = [.03:.01:.3];
figure(1)
Ploss_rdc = D^2*(Io.*Io)*Rdc;
plot(1000*Io,1000*Ploss_rdc,'k')
hold on
axis([30 300 0 4])
xlabel('Output current (mA)')
ylabel('Power loss (mW)')
figure(2)
Ploss_rp = ((1-D)*D^2*(Io.*Io)+D*((1-D)^2*(Io.*Io)+dI^2/12))*Rp;
plot(1000*Io,1000*Ploss_rp,'k')
hold on
axis([30 300 0 1])
xlabel('Output current (mA)')
ylabel('Power loss (mW)')
figure(3)
Ploss_if = Ploss_rdc+Ploss_rp;
Pout = 1.2*Io;
plot(1000*Io,100*Ploss_if./Pout,'k')
hold on
axis([30 300 0 4])
xlabel('Output current (mA)')
ylabel('Power loss (%)')
```

```
'Buckdynamics.m computes performance of compensator to step changes in input voltage and
output current'
V_in = 2.9;
V_ref = 1.2;
L = .376e-5;
```

```
C = 1e-5;
Nc = 90000;

f = 1.5e6;
T = 1/f;
Rp = .67;
Rn = .47;
Rlo = .075;
Rli = 0.16;
Rs = .15;
rx = (Rp + Rs + Rlo)/L;
ry = (Rn + Rlo)/L;
A=[0  1/C
  -1/L  0];

B=[0  -1/C
  1/L 0];

C1=[ 1    0
   0    1];

 D1=[0    0
  0    0];

I_o = .3;
D = (V_ref+I_o*(Rn+Rlo+Rs))/(V_in - I_o*(Rp+Rli-Rn));
Ravg = D*(Rp+Rs)+(1-D)*Rn+Rlo;
ai = 3.75;
Al = ai*Rs;
wsq = 1/(L*C);
sigma = 2*Nc*L+(1-2*D)*Al*V_in;

a = 2*Nc*L/(sigma*wsq);
b = 2*Al*f*V_in/(sigma*wsq);
c = 2*L*f*V_in/sigma;
d1 = -2*Al*L*f*V_in/sigma;
d2 = Nc*L/(Al*V_in*f);
e = D*(2*Nc*L-Al*D*V_in)/sigma;

Den_Plant = [a b 1];
[p] = roots(Den_Plant)

Num_VpVc = c*[1];
Num_IoVc = d1*[d2 1];
Num_ViVc = e*[1];

Plant_VpVc = tf(Num_VpVc,Den_Plant)
Plant_IoVc = tf(Num_IoVc,Den_Plant)
Plant_ViVc = tf(Num_ViVc,Den_Plant)

comp_num = 100*[3.6e-6 1];
```

```
comp_den = [1.6e-4 1];
comp_filter = tf(1,[1]);
Compensator = series(tf(comp_num,comp_den),comp_filter);
Loop_gain = series(Compensator,Plant_VpVc);
CLsys = feedback(Loop_gain,1);
[Gm,Pm,Wcg,Wcp] = margin(CLsys);

tloadstep = [7e-5:5e-8:1.8e-4];
for i = 1:600
  iloadstep(i) = .03;
end
for i = 601:780
  iloadstep(i) =  .03+(i-600)*.0015;
end
for i = 780:1400
  iloadstep(i) = .3;
end
for i = 1401:1580
  iloadstep(i) = .3-(i-1400)*.0015;
end
for i = 1580:2201
  iloadstep(i) = .03;
end

tstep = [0:5e-8:1.4e-4];
for i = 1:800
  vstep(i) = 3.6;
end
for i = 801:880
  vstep(i) = 3.6-(i-800)*.0075;
end
for i = 881:1800
  vstep(i) = 3;
end
for i = 1801:1880
  vstep(i) = 3+(i-1800)*.0075;
end
for i = 1880:2801
  vstep(i) = 3.6;
end



Foward_path = tf([1],Den_Plant);
Feedback_path = Num_VpVc*Compensator;
CL = feedback(Foward_path,Feedback_path);
loadstep = series(tf(Num_IoVc,[1]),CL);
[vo tls] = lsim(loadstep,iloadstep,tloadstep);


Foward_path = tf([1],Den_Plant);
```

```
Feedback_path = Num_VpVc*Compensator;
CL1 = feedback(Foward_path,Feedback_path);
loadstep1 = series(tf(Num_ViVc,[1]),CL);
[vo1 tls1] = lsim(loadstep1,vstep,tstep);



figure(1)
bode(Plant_VpVc,{1e2,1e8})
hold on
bode(Loop_gain,{1e2,1e8})
figure(2)
subplot(2,1,1)
plot(tloadstep*1e6,1000*iloadstep,'k')
axis([90 180 0 350])
xlabel('Time (us)');
ylabel('I_{out} (mA)');
subplot(2,1,2)
plot(tls*1e6,1.2095+vo,'k')
hold on
xlabel('Time (us)');
ylabel('V_{out} (V)');
axis([90 180 1.16 1.25])


figure(3)
subplot(2,1,1)
plot(tstep*1e6,vstep,'k')
axis([20 140 2.5 4])
xlabel('Time (us)');
ylabel('V_{in} (V)');
subplot(2,1,2)
plot(tls1*1e6,1.209+vo1,'k')
hold on
axis([20 140 1.195 1.22])
xlabel('Time (us)');
ylabel('V_{out} (V)');
```

'Ifilterdynamics.m Calculates input impedance of the close loop buck converter and output impedance of the input filter. Uses parameters from buckdynamics.m. Buckdynamics.m should be run before Ifilterdynamics.m.'

```
Li = 1e-6;
Rl = .16;
Cd = 1e-5;
Rd = 1;
Ci = 1e-6;

Z1 = tf([Li Rl],[1]);
Z2 = tf([Cd*Rd 1],[Cd 0]);
```

```
Z3 = tf([1],[Ci 0]);

A = series(series(Z2,Z3),Z1);
B = series(Z1,Z2)+series(Z2,Z3)+series(Z1,Z3);

Io = .3;
Vo = 1.2;
Zslf = Vo/(Io*D^2);
a1 = (Al - D*Nc*T/Io)*C;
a2 = (1-2*D)*Al/(2*Nc*L);
a3 = Al*Vo/(2*Nc*L);
num1 = c*(tf([a1 a2],[1]) + Compensator);
den1 = tf([a b 1],[1])+c*Compensator;
Yin = ((1-a3)*num1/den1 + a3);
Zin = -Zslf/Yin;


[mag4 phase4 w4] = bode(Zin,{1e2,1e8});
for i = 1:length(mag4)
  m4(i) = (mag4(1,1,i));
end
[mag1 phase1 w1] = bode(A/B,{1e2,1e8});
for i = 1:length(mag1)
  m1(i) = (mag1(1,1,i));
end
```