Biasing Techniques for Linear Power Amplifiers

by

Anh Pham

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Author _____
Department of Electrical Engineering and Computer Science
May 2002

Certified by _____
Charles G. Sodini
Professor of Electrical Engineering and Computer Science
Thesis Supervisor

Accepted by _____
Arthur C. Smith, Ph.D.
Chairman, Committee on Graduate Students
Department of Electrical Engineering and Computer Science

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Abstract

Power amplifiers with conventional fixed biasing attain their best efficiency when operate at the maximum output power. For lower output level, these amplifiers are very inefficient. This is the major shortcoming in recent wireless applications with an adaptive power design; where the desired output power is a function of the bit-error rate, channel characteristics, modulation schemes, etc. Such applications require the power amplifier to have an optimum performance not only at the peak output level, but also across the adaptive power range.

An adaptive biasing topology is proposed and implemented in the design of a power amplifier intended for use in the WiGLAN (Wireless Gigabits per second Local Area Network) project. Conceptually, the adaptive biasing circuitry senses the input signal, scales appropriately, then takes the average. The result dc signal is used to moderate the biasing current for the power transistors. The bias level is; therefore, a function of the input signal. By selecting the appropriate scaling factor, the biasing current can be adjusted to improve the efficiency across a wide range of operating power levels.

The power amplifier that was designed, has two stages with a nominal gain of 17.3dB. The output at 1-dB compression point is 20dBm. Both stages employ the adaptive biasing technique. The peak efficiency is 35% at 19dBm output power while the mid-range operation efficiency shows a significant improvement from conventional fixed biasing. Operating at 5.8GHz center frequency, the amplifier also exhibits good linearity with –56.66dBc and –58.11dBc, 2^{nd} and 3^{rd} harmonics, respectively, at maximum output power.

Acknowledgements

The work presented in this thesis could not have happened without the help and support of many people. First, I would like to thank Professor Charles Sodini for providing me with this research opportunity. His guidance is instrumental and his intuition approach to technical problems is intriguing. I am also greatly indebted to all of my colleagues in the H. S. Lee and C. G. Sodini research groups. Don Hitko vast knowledge and experience in circuit design are essential to the completion of this thesis work. Todd Sepke is always patient and helpful with design tools and other computing issues. I found solutions for a lot of the problems during our countless coffee break discussions. I would like to thank Andy Wang for his help on system issues that I often ran into during the course of this thesis. Andrew Chen and Mark Peng seem to know all the tricks to get things done around MIT, and are willing to offer their assistance. Andrew is the photographer for all the photos presented in this thesis. I greatly appreciate all the groups' members for making our office a friendly and supportive research environment.

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Vickram Vathulya at Philips Research USA introduced me to integrated power amplifier design and shared his industry "how-to" experience many times thereafter. I would like to thank Philips Research USA, especially Satyen Mukherjee and Tirdad Sowlati, for giving me the opportunity to design power amplifiers for GSM and CDMA cellular phones.

Marilyn Pierce helps me greatly with all the deadlines and administrative requirements that I often overlook. I greatly appreciate her dedication.

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And there is Ha, who is always there for me.

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1 Introduction

Because of the explosion of wireless PDAs (Personal Digital Assistant) use, we are now living in a "mobile" information era where information from every corner of the world is available at the touch of a fingertip regardless of our location. However, current wireless systems are too costly and limited to exploit this vast amount of information. What we need is not merely a wireless connection, but a fast, efficient, and reliable wireless connection.

Every wireless system employs one or multiple power amplifiers, and it is usually the case that the performance of a wireless system is determined by the linearity and efficiency of its power amplifiers. However, current linear power amplifiers are very inefficient. They are the most power "hungry" block in a wireless system, and they consume many times the combined power of the rest of the transceiver circuitry. Not only do they severely reduce the battery lifetime, but they also degrade the performance of adjacent circuitries by releasing tremendous amounts of heat. The need for an efficient linear power amplifier has been the focus of much industrial and academic research in the past decade.

Moreover, although power amplifiers have been used since the early days of transistors, there is no comprehensive documentation of its biasing techniques. Thorough knowledge of various biasing topologies and the tradeoff between them will greatly help power amplifier designers.

Motivated by the above challenges, this thesis focuses on high efficiency biasing techniques for power amplifiers. Three power amplifiers, each uses a different biasing topology, are designed and simulated to study and compare the three biasing circuits. In addition, an innovative adaptive biasing topology is proposed. An adaptive biasing power amplifier is designed, fabricated, and tested to demonstrate the proposed concept.

The remainder of this chapter presents an overview of the thesis. We will begin by reviewing specific issues in biasing, efficiency, and SOC (System On Chip) that often challenge power amplifier designers. As the thesis is part of the ambitious WiGLAN project, a brief introduction of the WiGLAN is presented to explain the challenges and requirements for the power amplifier design. The chapter concludes with a detailed outline of the thesis.

1.1 Power Amplifier Biasing

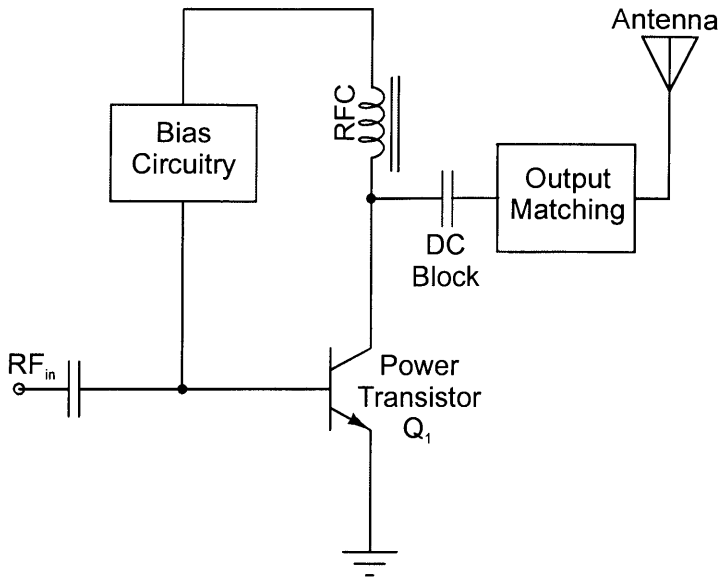

Figure 1-1: Basic Power Amplifier Circuit

Figure 1-1 shows a basic power amplifier circuit with the power transistor connected to the supply via an RF choke (RFC). The output matching circuit transforms the output impedance to the 50Ω antenna load. The goal is to provide the bias circuitry for the power transistor. Much of the amplifier operating conditions and performance depend largely on this biasing circuit.

The collector current of a power transistor is usually in the range of hundreds of milliamps. Therefore, any emitter degeneration resistor is undesirable*. The use of the RF choke allows the collector to connect directly to the supply voltage with minimal loss. In order to achieve high efficiency, the biasing circuitry should consume as little power as possible. Also, its impedance should be large so that it does not load the RF circuit and reduce the gain.

1.2 Efficiency

Assume transistor Q_1 in Figure 1-1 is biased with a fixed quiescent current I_q and voltage V_q. The set (V_q, I_q) is usually called the transistor's biasing point. When an RF input is applied, the collector current and voltage swing around their respective biasing points. Figure 1-2 shows an example of the collector current and voltage waveforms under sinusoidal excitation.

* with the exception of ballast resistor to avoid thermal runaway.

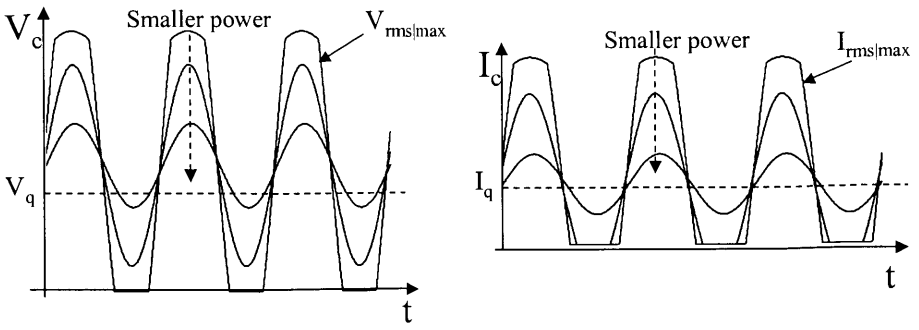

Figure 1-2: Collector Voltage and Current Waveforms

Let $I_{rms|\max}$, and $V_{rms|\max}$ be the largest root mean square value for the collector current and voltage, respectively. Assume a lossless matching network, the maximum rms (root mean square) output power is given by

$$P_{\max} = V_{rms|\max} I_{rms|\max} \tag{1-1}$$

Under the bias condition of V_q and I_q, the supply power is

$$P_{dc} = V_q I_q \tag{1-2}$$

Therefore, the maximum attainable efficiency is

$$\eta = \frac{P_{\max}}{P_{dc}} = \frac{V_{rms|\max} I_{rms|\max}}{V_q I_q} \tag{1-3}$$

Depending on the current and voltage waveforms as well as their relative phases, the maximum efficiency could be anywhere from 0 to a theoretically ideal value of 100 percent.

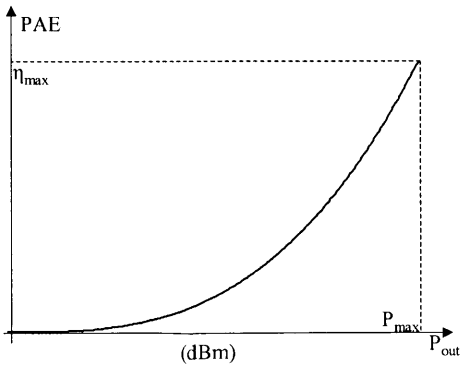

Figure 1-3: Typical Power Amplifier Efficiency Curve

When a smaller input is applied, the voltage and current swings are smaller, and the output power is smaller than P_{max}. However, since the bias points V_q, and I_q are fixed, the supply power stays constant regardless of the input. Therefore, the power amplifier efficiency drops at lower output levels. Figure 1-3 shows a typical PAE (Power Added Efficiency) versus output power curve. The power amplifier is most efficient when operating at its maximum designed output power.
Power amplifiers with this type of efficiency curves work fine for fixed output power applications. However, they pose a significant shortcoming for adaptive power systems, where the output power varies depending on the channel condition.

1.3 Fully Integrated Power Amplifier Issues

With the advanced development of semiconductor and integrated circuit technologies, system on chip (SOC) is now the favored possibility. However, power amplifiers remain a sticky issue for integrated circuit systems. Designers face two main challenges for fully integrated power amplifiers. First, as the technology scales, both supply voltages and transistor breakdown voltages become smaller. For the same output power, the current increases as the voltage decreases. Designers now have to work with much higher currents that make them more vulnerable to parasitic and series resistor loss. Second, spiral on-chip inductors are too lossy for matching networks, especially output matching networks where RF power is high. Overcoming these challenges will require much more research and innovations.

1.4 The WiGLAN Project

The power amplifier designed in this thesis is intended for use in the ongoing WiGLAN (Wireless Gigabit per Second Local Area Network) project in the Microsystems Technology Laboratory (MTL) at MIT. Using the ISM (Industry Scientific and Medical) band at 5.8GHz with 150MHz bandwidth, the project calls for a design of a wireless network with 1 Gigabit per second throughput. In order to achieve such a high speed, an adaptive modulation scheme utilizing multiple OFDM (Orthogonal Frequency Division Modulation) channels with up to 256-QAM (Quadrature Amplitude Modulation) is used. Such a modulation scheme requires a power amplifier with extremely high linearity.
Moreover, in order to maximize battery lifetime, the WiGLAN also adapts the transmitting power based on the distance to receivers and environment conditions. Power adaptation poses yet another challenge to the power amplifier designs. As discussed earlier, conventional power amplifiers are very inefficient at lower output levels. Therefore, innovative biasing techniques are required to improve low level operation efficiency.

1.5 Thesis Overview

The rest of the thesis is divided into two parts. The first part, Chapter 2-5, provides relevant background and detailed theoretical analysis for power amplifiers. Chapter 2 reviews useful RF terminologies and nonlinearities. Chapter 3 discusses the conducting power amplifier modes,

Class-A, AB, B, and C. Detailed operation of each mode is studied to determine the tradeoff between gain, efficiency, and linearity. In Chapter 4, three fixed power amplifier biasing topologies as well as the proposed adaptive biasing technique are presented. For each topology, details of the bias setting mechanism, as well as effects on gain, linearity and efficiency of the overall amplifying stage are discussed and compared. Chapter 5 goes over the step-by-step design of a class-A power amplifier. Extra efforts are given to demonstrate and clarify the difference between power match and conjugate match in power amplifier design.

The second part of the thesis, Chapter 6-9, is devoted to the practical designs of power amplifiers to validate the observation of the four biasing topologies studied in Chapter 4. In Chapter 6, a 5.8GHz, 20dBm class-A power amplifier is designed using the step-by-step procedure from Chapter 5. The power amplifier has four versions, each using one of the four biasing techniques discussed in Chapter 4. Simulation results of the design are presented and discussed in Chapter 7.

The adaptive biasing version of the power amplifier is fabricated in the IBM SiGe 6HP BiCMOS process. Chapter 8 explains the fabrication, test board, and measurement setups for the power amplifier. Measurement results are provided in Chapter 9. Chapter 10 concludes the thesis and discusses further research topics on the subject.

2 Nonlinearities and Power Link Budget

This chapter reviews some general nonlinearity and RF terminologies. Most of these terminologies, in general, apply for all gain blocks. For simplicity, however, they are addressed here in the context of a power amplifier.

Power amplifiers are usually designed for a certain set of specifications such as output power, efficiency, and linearity. However, power amplifier designers often have to design their PA to work with a certain given set of receiver characteristics and channel link to produce a certain required bit-error-rate output. In such cases, designers have to start from the receiver output, work their way back through the receiver chain and the channel link to derive the acceptable specifications for the power amplifier. Therefore, familiarity with receiver characterizations as well as the channel link is certainly helpful for power amplifier designers. The last part of this chapter addresses this connection and suggests a rough estimation for the power link budget of a transceiver.

2.1 Distortion

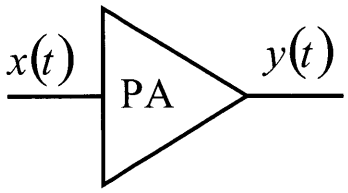

Figure 2-1: Power Amplifier Model

Power amplifiers are usually nonlinear, which results in unintended signals with frequencies outside of the band of operation. These out-of-band signals can cause significant interference to other channels. In order to study the nonlinearity, we use a polynomial series to model the power amplifier as suggested by Razavi [1]. For simplicity, we restrict our analysis to fifth order distortion and assume that higher order distortions are negligible.

Let $y(t)=\alpha_1 x(t)+\alpha_2 x(t)^2+\alpha_3 x(t)^3+\alpha_3 x(t)^4+\alpha_5 x(t)^5$ be the output when an input $x(t)$ is applied to the power amplifier as shown in Figure 2-1.

2.1.1 Harmonics

If a sinusoidal $x(t)=A\cos(\omega t)$ is applied to the power amplifier, then the output is given by

$$y(t)=\alpha_1 A\cos(\omega t)+\alpha_2\left(A\cos(\omega t)\right)^2+\alpha_3\left(A\cos(\omega t)\right)^3 +\alpha_4\left(A\cos(\omega t)\right)^4+\alpha_5\left(A\cos(\omega t)\right)^5 \tag{2-1}$$

Expanding the high order terms using trigonometric identities, we can rewrite the output in terms of dc, fundamental and harmonic components. Please refer to Appendix A for detail calculation; the result is listed here in Table 2-1. The second column contains the dc, fundamental and harmonic terms. The coefficients for these terms are in the third column.

Table 2-1: Power Amplifier Output in Response to a Single Tone Input

Output Components		Coefficients
DC	1	$\frac{1}{2}\alpha_2 A^2+\frac{3}{8}\alpha_4 A^4$
Fundamental	$\cos(\omega t)$	$\alpha_1 A+\frac{3}{4}\alpha_3 A^3+\frac{5}{8}\alpha_5 A^5$
2nd Harmonic	$\cos(2\omega t)$	$\frac{1}{2}\alpha_2 A^2+\frac{1}{2}\alpha_4 A^4$
3rd Harmonic	$\cos(3\omega t)$	$\frac{1}{4}\alpha_3 A^3+\frac{5}{16}\alpha_5 A^5$
4th Harmonic	$\cos(4\omega t)$	$\frac{1}{8}\alpha_4 A^4$
5th Harmonic	$\cos(5\omega t)$	$\frac{1}{16}\alpha_5 A^5$

Because of the nonlinear behavior, the output contains integer multiples of the input frequency. These higher frequency components are called harmonics. To minimize interference to other bands, these harmonics components should be suppressed as much as possible. FCC (Federal Communications Commission) Part 15 specifies the rules regarding harmonics signals of a transmitting system.

2.1.2 1-dB Compression

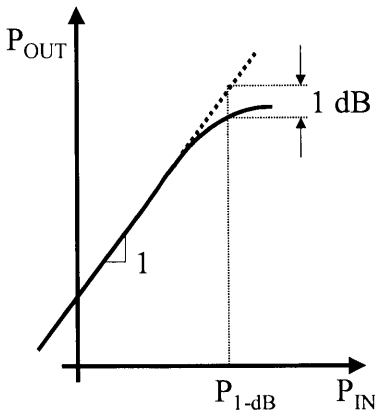

Figure 2-2: 1-dB Compression Point

From Table 2-1, the above amplifier has a fundamental gain of $\alpha_1 A + \frac{3}{4}\alpha_3 A^3 + \frac{5}{8}\alpha_5 A^5$, where A is the input amplitude. In low power operation, where A is small, $\alpha_1 A$ is much larger than $\frac{3}{4}\alpha_3 A^3 + \frac{5}{8}\alpha_5 A^5$. In this case, the fundamental gain is approximately $\alpha_1 A$. On the logarithmic-scale plot, the output power versus input power curve has a slope of 1 at low power levels. As A increases, $\frac{3}{4}\alpha_3 A^3 + \frac{5}{8}\alpha_5 A^5$ increases faster than $\alpha_1 A$. Therefore, as the input power rises to a certain level, $\frac{3}{4}\alpha_3 A^3 + \frac{5}{8}\alpha_5 A^5$ is no longer negligible compare to $\alpha_1 A$. If α_3 and α_5 are negative, the gain starts leveling off when A is sufficiently large. In other words, the gain is "compressed" from its extrapolated linear value. The 1-dB compression point is defined as the input power level where the gain drops by 1-dB as shown in Figure 2-2.
An important observation from the fundamental term coefficient is that only the odd power terms in the polynomial series (α_3 and α_5 in this case) affect the fundamental gain.

2.1.3 IIP_3 and Intermodulation Products

When a signal with two different frequency components $x(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)$ is applied to the power amplifier, the output exhibits multiple mixings of the two frequencies called intermodulation products (IM). Using the same power amplifier model,

$$y(t)=\alpha_1\left(A_1\cos(\omega_1 t)+A_2\cos(\omega_2 t)\right)+\alpha_2\left(A_1\cos(\omega_1 t)+A_2\cos(\omega_2 t)\right)^2$$
$$+\alpha_3\left(A_1\cos(\omega_1 t)+A_2\cos(\omega_2 t)\right)^3+\alpha_4\left(A_1\cos(\omega_1 t)+A_2\cos(\omega_2 t)\right)^4 \quad (2\text{-}2)$$
$$+\alpha_5\left(A_1\cos(\omega_1 t)+A_2\cos(\omega_2 t)\right)^5$$

For simplicity, we assume here that the two tones have the same amplitude, i.e. $A_1 = A_2 = A$. Expanding the series, besides the familiar dc, fundamental and high-order harmonics components with frequencies ω_1, $2\omega_1$, $3\omega_1$, $4\omega_1$, $5\omega_1$, ω_2, $2\omega_2$, $3\omega_2$, $4\omega_2$, and $5\omega_2$, we also have intermodulation components between the two input frequencies. Again, detailed calculation is presented in Appendix A. The result is listed here in Table 2-2. The first column represents the output frequency components. The top row shows represents the amplitude. The grid contains the respective coefficients. A "–" represents a zero.

Table 2-2: Power Amplifier Output in Response to a Two-Tone Input

	$\alpha_1 A$	$\alpha_2 A^2$	$\alpha_3 A^3$	$\alpha_4 A^4$	$\alpha_5 A^5$
1 (dc)	–	1	–	9/4	–
ω_1, ω_2	1	–	9/4	–	25/4
$2\omega_1$, $2\omega_2$	–	1/2	–	2	–
$3\omega_1$, $3\omega_2$	–	–	1/4	–	25/16
$4\omega_1$, $4\omega_2$	–	–	–	1/8	–
$5\omega_1$, $5\omega_2$	–	–	–	–	1/16
$\omega_1 \pm \omega_2$	–	1	–	3	–
$2\omega_1 \pm \omega_2$, $\omega_1 \pm 2\omega_2$	–	–	3/4	–	25/8
$2\omega_1 \pm 2\omega_2$	–	–	–	3/4	–
$3\omega_1 \pm \omega_2$, $\omega_1 \pm 3\omega_2$	–	–	–	1/2	–
$3\omega_1 \pm 2\omega_2$, $2\omega_1 \pm 3\omega_2$	–	–	–	–	5/8
$4\omega_1 \pm \omega_2$, $\omega_1 \pm 4\omega_2$	–	–	–	–	1/16

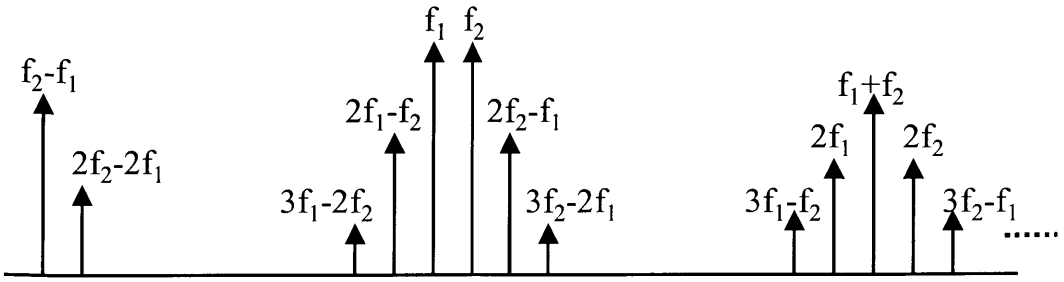

Figure 2-3: Two-Tone Test Output Spectral Density

Of particular interest are the third-order and fifth-order IMs with frequencies $(2\omega_1 - \omega_2)$, $(2\omega_2 - \omega_1)$, $(3\omega_1 - 2\omega_2)$, and $(3\omega_2 - 2\omega_1)$ because when ω_1 and ω_2 are close enough, these third-order and fifth-order products could fall in the band of interest. The rest of the intermodulation products are usually further away from the operating band that receiver filters easily suppress them. At low power level when A is small, $\alpha_3 A^3$ is much larger than $\alpha_5 A^5$. Therefore, on the logarithmic-scale plot versus the input power, the power of these third-order IMs has a slope of 3 because their amplitudes are proportional to A^3. Analogously, the power of the fifth order IMs has a slope of 5 as shown in Figure 2-4.
Power amplifier linearity is usually specified by IIP_3 (input third intercept point), which is defined as the input power where the third-order IM power is as large as the fundamental.

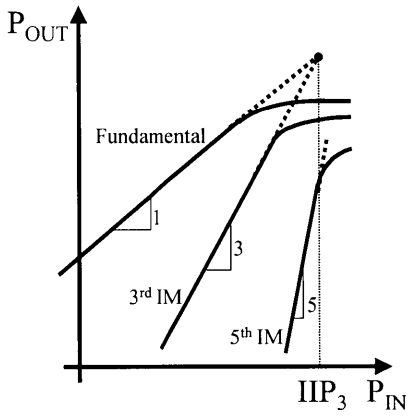

Figure 2-4: Input Third Intercept Point

2.2 Receiver Sensitivity and Bit-Error-Rate (BER)*

Receiver sensitivity is defined as the minimum signal power at the receiver antenna that can produce an acceptable signal to noise ratio. To calculate the sensitivity, we start with the noise figure equation

$$NF = \frac{SNR_{in}}{SNR_{out}} = \frac{P_{rx\_ant} / \left(P_{rs\_noise} * BW \right)}{SNR_{out}} \qquad (2\text{-}3)$$

where

P_{rx_ant} is the receiving signal power at the antenna,

P_{rs_noise} is the source resistance noise power per unit bandwidth, assume conjugate match at the input, $P_{rs\_noise} = kT = -174 dBm/Hz$,

BW is the total bandwidth,

* The work in Sections 2.2, 2.3, and 2.4 is co-authored with Andy Wang

SNR_{out} is the signal to noise ratio at the output of the receiving chain.

Rearrange the terms,

$$P_{rx\_ant} = NF * SNR_{out} * P_{rs\_noise} * BW \tag{2-4}$$

By definition, P_{rx_ant} is the receiver sensitivity S_0 when SNR_{out} is smallest. In dB terms,

$$S_0 = \underbrace{\underbrace{-174dBm/Hz + NF_{dB}}_{in-band-white-noise} + 10\log BW}_{total-noise-floor} + SNR_{out|\min} \tag{2-5}$$

Given a specific communication channel with a certain bandwidth and receiver noise figure, we can use equation (2-5) to calculate the sensitivity from the minimum signal-to-noise ratio. However, the minimum signal-to-noise ratio is often given in terms of bit-error-rate (BER), which is defined as the average number of erroneous bits observed at the output of the receiver divided by the total number of bits received in a unit time.

Let E_b be the bit energy,
R be the data rate (i.e. 1Gb/s),
N_0 be the white Gaussian noise power spectral density.

Then the total signal power is $R * E_b$, and the total noise power is $BW * N_0$. Therefore,

$$SNR_{out} = \frac{P_{signal}}{P_{noise}} = \frac{R * E_b}{BW * N_0} = \frac{R}{BW}\left(\frac{E_b}{N_0}\right) \tag{2-6}$$

E_b/N_0 directly relates to the bit-error-rate. Depends on modulation types and coding schemes, we can readily use BER versus E_b/N_0 curves to determine E_b/N_0 from a given value of BER. A typical BER versus E_b/N_0 plot for a Gaussian and a Rayleigh channel is shown in Figure 2-5.

From equation (2-5), replace $SNR_{out|\min}$ with equation (2-6)

$$S_0 = \underbrace{-174dBm/Hz + NF_{dB}}_{in-band-white-noise} + 10\log R + 10\log\left(\frac{E_b}{N_0}\right) \tag{2-7}$$

Since E_b/N_0 is determined for a given BER, equation (2-7) allows us to directly calculate the receiver sensitivity based on BER. One interesting observation from the equation is that sensitivity is independent of bandwidth when expressed in terms of E_b/N_0.
Table 2-3 shows some example values for receiver sensitivity of typical receiver specifications. The values are calculated for two channel types, Gaussian and Rayleigh channels.

Table 2-3: Example Values for Receiver Sensitivity

	Receiver Sensitivity S_0	
Specification	Gaussian Channel	Rayleigh Channel
Receiver Noise Figure $NF_{dB} = 6dB$ Data Rate R=1Gbit/s (256-QAM) Bit-Error-Rate BER=10^{-3}	-71 dBm	-54 dBm
Receiver Noise Figure $NF_{dB} = 6dB$ Data Rate R=1Mbit/s (4-QAM) Bit-Error-Rate BER=10^{-3}	-101 dBm	-84 dBm

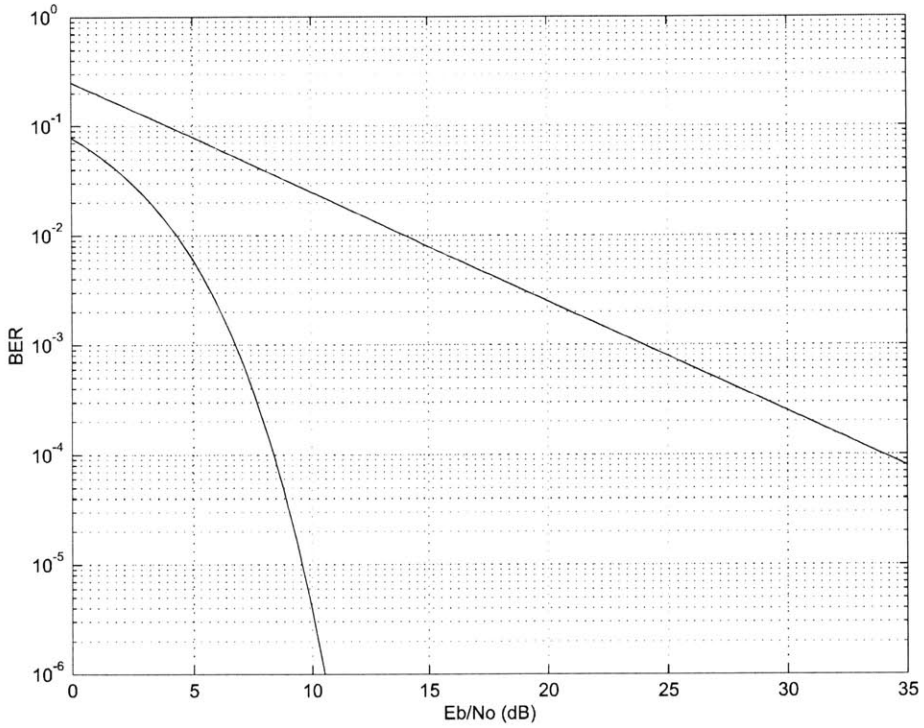

Figure 2-5: BER Curves for Gaussian and Rayleigh Channels

Courtersy of Andy Wang M.S. Thesis [2]

2.3 Path Loss

Signals propagating through free space experience a power loss proportional to the square of the distance. However, in a typical wireless LAN environment, there are walls, furniture, moving objects, reflecting surfaces, ... For these environments, the exponential proportionality constant is larger than 2, with experimental measurement values for a typical office setting between 3 and 4. The power loss also depends on the signal frequency as given in the following equation.

$$L_{ave} = -10\log\left(\frac{\lambda^2}{(4\pi)d^n}\right) \tag{2-8}$$

with

$\lambda = c/f$ is the signal wavelength in meter,

d is the distance between transmitter and receiver in meter,

n is the path loss exponent.

Table 2-4: Path Losses at Various Distances for Typical Wireless Standards

	$d = 1m$	$d = 10m$	$d = 100m$
Blue Tooth (f_0 = 2.4 GHz)	29 dB	59 dB	89 dB
802.11a (f_0 = 5.3 GHz)	36 dB	66 dB	96 dB
WiGLAN (f_0 = 5.8 GHz)	36.7 dB	66.7 dB	96.7 dB

2.4 Power Link Budget

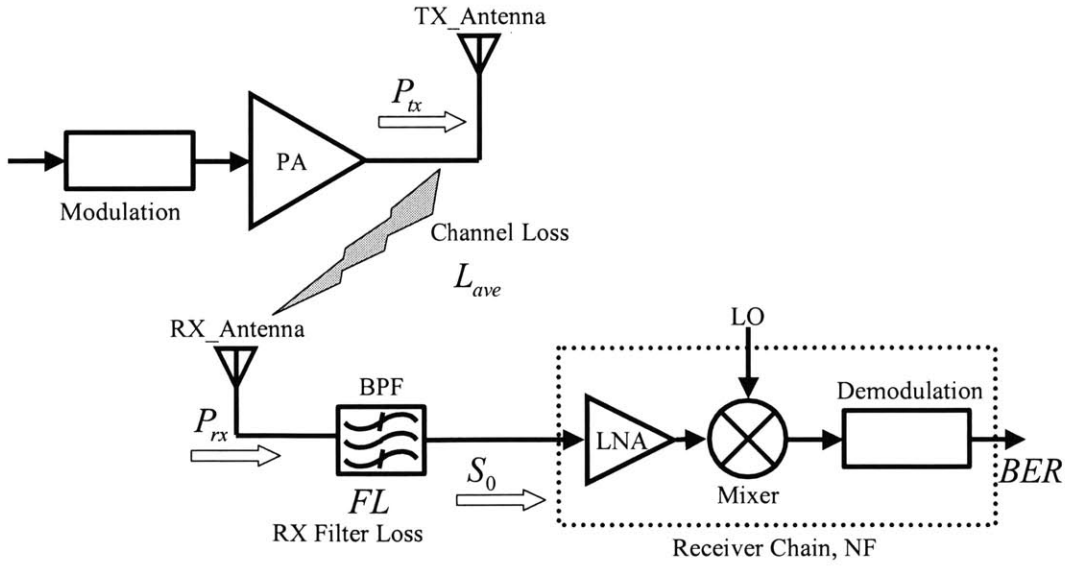

Figure 2-6: Transceiver Block Diagram for Power Link Budget

We can use our knowledge of power amplifier and receiver characteristics to plan the power link budget for the WiGLAN. Consider the block diagram for the WiGLAN transceiver as shown in Figure 2-6 where

P_{tx} is the transmitter power,

L_{ave} is the average path loss,

FL is the receiver filter loss,
S_0 is the receiver sensitivity,
NF is the total noise figure of the receiver chain,

$$P_{tx} = P_{rx} + L_{ave} = S_0 + FL + L_{ave} \tag{2-9}$$

Replacing the terms on the right from equations (2-7) and (2-8).

$$P_{tx} = \underbrace{-174 + NF + 10\log R + 10\log\left(\frac{E_b}{N_0}\right)}_{\text{Receiver Sensitivity}} + \underbrace{FL}_{\text{Filter Loss}} + \underbrace{10\log\left(\frac{\lambda^2}{(4\pi)d^n}\right)}_{\text{Path Loss}} \tag{2-10}$$

Given the data rate R, bit error rate (in terms of E_b/N_0), and the distance d, equation (2-10) relates the transmitting power P_{tx} to the receiver noise figure NF.

Table 2-5: Typical Required Transmitting Power for the WiGLAN PA in Rayleigh Channel

	Required Transmitting Power P_{tx}		
Specification	$d = 1m$	$d = 10m$	$d = 100m$
Receiver Noise Figure $NF_{dB} = 6dB$ Data Rate R=1Gbit/s (256-QAM) Bit-Error-Rate BER=10^{-3} Filter Loss $FL = 3dB$	-14.3 dBm	15.7 dBm	45.7 dBm
Receiver Noise Figure $NF_{dB} = 6dB$ Data Rate R=1Mbit/s (4-QAM) Bit-Error-Rate BER=10^{-3} Filter Loss $FL = 3dB$	-44.3 dBm	-14.3 dBm	15.7 dBm

3 Conducting Power Amplifiers

Power amplifiers are divided into classes based on their output waveform shapes and relative phases. However, the actual implication of the power amplifier classes is related to the three main figure-of-merits: gain, linearity, and efficiency. Before discussing power amplifier classification, we shall first review the definitions for gain, efficiency, and linearity.

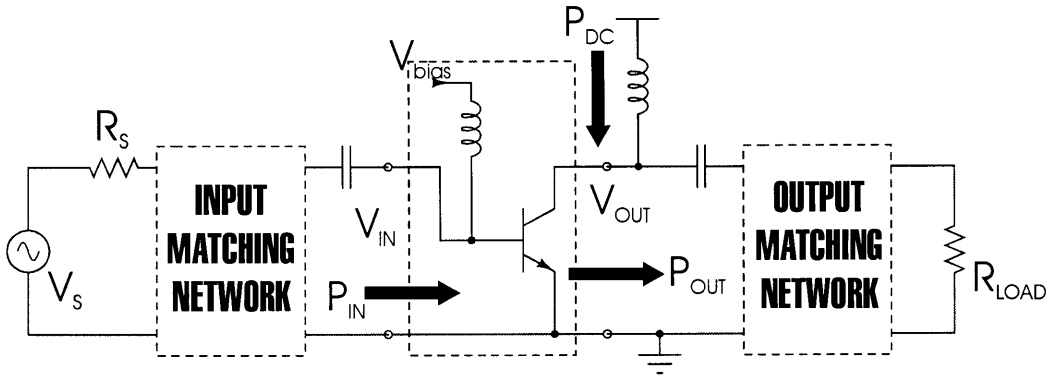

Figure 3-1: A 2-Port Model of An Inductively Coupled Power Amplifier

Consider a simple power amplifier as a two-port network in Figure 3-1. The dc supply is connected via an RFC (Radio Frequency Choke). Such a supply configuration is called inductively coupled. Assume that both input and output matching networks are lossless. The power amplifier gain is simply

$$G = \frac{P_{out}}{P_{in}} \tag{3-1}$$

Where P_{in} is the input power, and

P_{out} is the output power.

Power added efficiency (PAE) is defined as

$$\eta = \frac{P_{out} - P_{in}}{P_{dc}} \tag{3-2}$$

Where P_{dc} is the dc supply.

Usually when the gain is large, P_{out} is much larger than P_{in}, then efficiency is loosely defined as P_{out}/P_{dc}.

Power amplifier linearity is usually specified by the input third order intercept product IIP_3 as discussed in chapter 2. Intuitively speaking, a power amplifier is perfectly linear if its response to a single frequency input signal contains no other frequency components besides the input frequency.

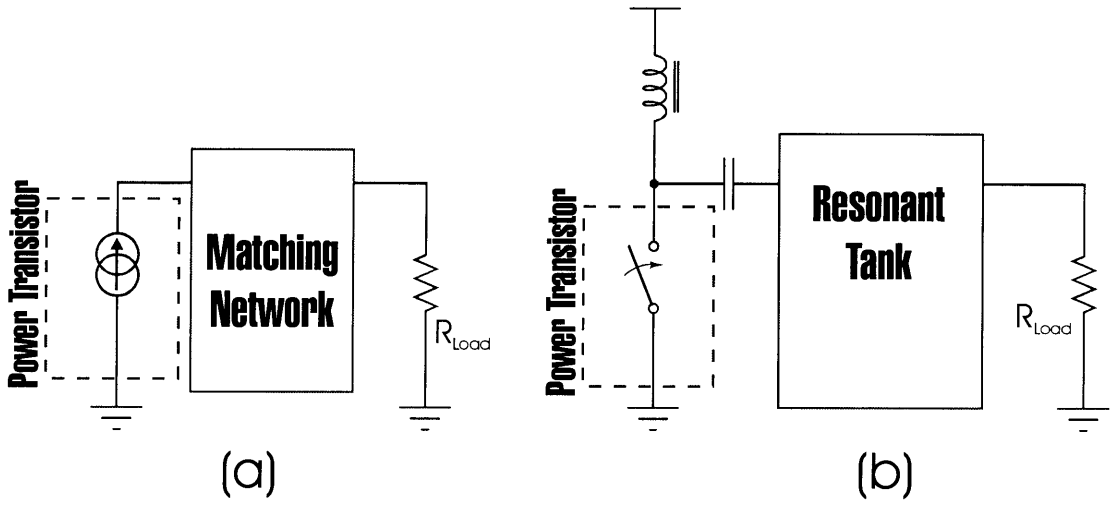

Figure 3-2: Equivalent Power Amplifier Models for (a) Conducting Classes and (b) Switching Classes

There are two main types of power amplifier classes: the conducting classes and the switching classes as shown in Figure 3-2. In conducting-class power amplifiers, the transistor acts as a current source generator driving a resistive load. Depending on the current waveforms, conducting-class power amplifiers can be very linear. Switching-class power amplifiers, on the other hand, use the transistor as a switch. They rely on a resonant tank network to store energy and switch the transistor on and off to divert the stored energy to RF output power. Because of the switching nature operation, switching-class power amplifiers are extremely nonlinear and unsuitable for the type of quadrature amplitude modulation employed by the WiGLAN. Therefore, we will limit our discussion here to conducting-class power amplifiers where good linearity is inherited.

3.1 Class-A

A power amplifier operates in class-A mode when its power transistors are on for the entire period of the input signal. Therefore, a class-A amplifier is said to have a 360° conduction angle.

Assume there is a base-emitter voltage $V_{be(on)}$, above which the transistor is on, and below which the transistor is off. In order for the amplifier to operate in class-A mode, the transistor has to be biased with a base voltage V_{bias} such that the base voltage V_b is larger than $V_{be(on)}$ during the entire period. In such case, the transistor output voltage and current waveforms are pure sinusoidal as shown in Figure 3-3.

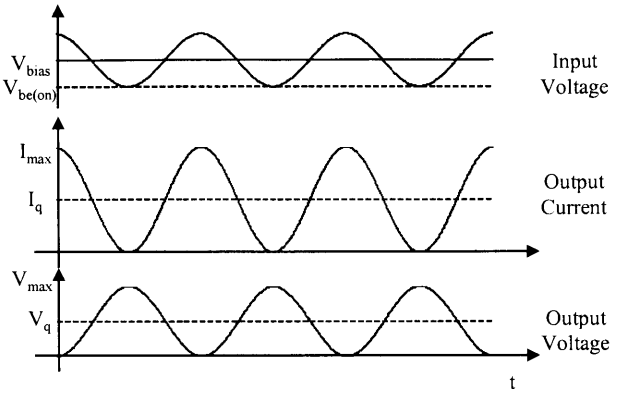

Figure 3-3: Waveforms of A Class-A Power Amplifier

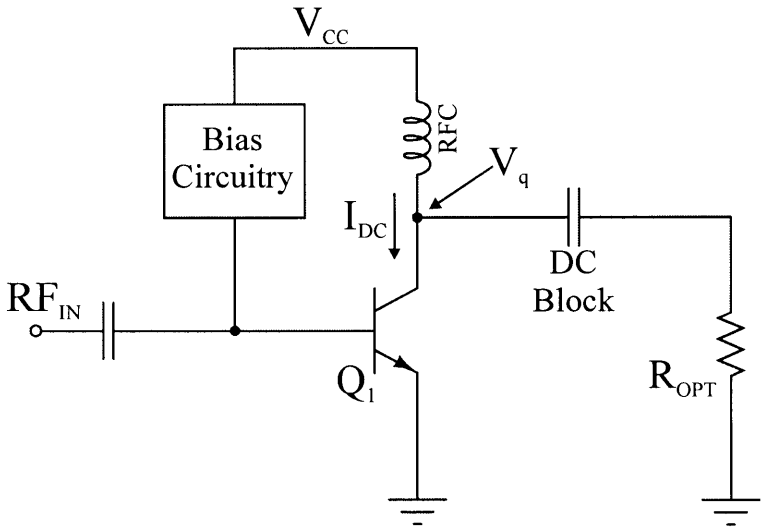

Figure 3-4: Power Amplifier Circuits for Calculating Output Power and DC Power

The power amplifier in this case is biased with a quiescent collector current $I_q = I_{DC}$ and voltage $V_q = V_{CC}$. At maximum output power, the collector voltage and current waveforms swing across the entire available linear range of 0 to $I_{\max}$, and 0 to $V_{\max}$, respectively, where $I_{\max} = 2I_q = 2I_{DC}$ and $V_{\max} = 2V_q = 2V_{CC}$. Therefore, the maximum linear rms output power is

$$P_{out|\max} = I_{rms}V_{rms} = \frac{I_{\max}}{2\sqrt{2}}\frac{V_{\max}}{2\sqrt{2}} = \frac{I_{DC}V_{CC}}{2} \tag{3-3}$$

The dc supply power is constant and given by

$$P_{dc} = I_{DC}V_{CC} \tag{3-4}$$

Therefore, the maximum achievable efficiency for an inductively coupled class-A power amplifier is

$$\eta = \frac{P_{out|\max}}{P_{dc}} = 50\% \tag{3-5}$$

Note that because of the coupled inductor, the collector voltage can swing higher than the supply voltage. In effect, it doubles the maximum linear voltage swing. For class-A power amplifier without the coupled inductor, the maximum efficiency is 25%.

Assuming the collector current and voltage are perfectly sinusoidal, class-A power amplifier output waveforms contain nothing but the original frequency of the input drive. Therefore, class-A mode is perfectly linear.

3.2 Reduced Conduction Angle Mode, Class-AB, B and C

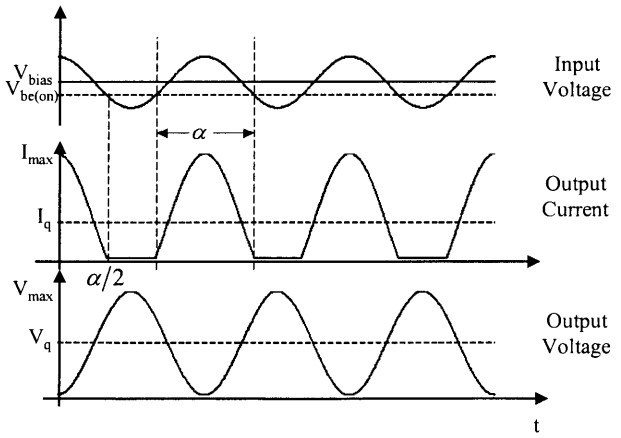

Figure 3-5: Waveforms of A Reduced Conduction Angle Amplifier

In order to improve efficiency, power amplifiers can be biased at a lower quiescent point compare to that of a class-A as shown in Figure 3-5. The idea is to use an RF drive large enough to swing the transistor into conducting. Therefore, a class-B amplifier requires a higher drive than a class-A amplifier operating in the same output power condition.

Table 3-1: Modes of Operation

	Quiescent Base Bias Point ($V_{bias} - V_{be(on)}$)	Quiescent Collector Current (I_q)	Conducting Angle
Class -A	$\frac{V_{in\_\max}}{2}$	$\frac{I_{\max}}{2}$	2π
Class-AB	$0 - \frac{V_{in\_\max}}{2}$	$0 - \frac{I_{\max}}{2}$	$\pi - 2\pi$
Class-B	0	0	π
Class-C	< 0	0	$< \pi$

From Figure 3-5 we can see that the transistor base is biased at a low enough voltage that the transistor enters cut-off for a certain interval in each period. The result is a clipped sinusoidal output current. The transistor is only on for an angle $\alpha < 360^\circ$. Therefore, this mode of operation is called reduced conduction angle mode. Depend on their conduction angles; power amplifiers are categorized into different classes. Class-A power amplifiers have a 360° conduction angle. Class-B operates with a 180° conduction angle. Class-AB falls somewhere in between with a conduction angle between 180° and 360°. Class-C conduction angle is reduced further to less than 180°. Table 3-1 lists different modes of operations for conducting power amplifiers, their respective biasing conditions as well as their conduction angles.

Compared to class-A amplifiers, reduced conduction angle amplifiers trade gain for efficiency. As discussed earlier, amplifiers operate in this mode have lower bias points, and rely on a larger RF drive to swing them into conducting. Therefore, reduced conduction angle amplifiers have less gain compare to their class-A counterparts. In order to see how this improves the efficiency, we can calculate the output and dc power of the amplifier based on the current and voltage waveforms in Figure 3-5.

First, we should find the expression for the collector current I_c in terms of $I_{\max}$ and the conduction angle α. The collector output current in Figure 3-5 can be written as

$$I_c = \begin{cases} I_q + (I_{\max} - I_q)\cos\theta & -\frac{\alpha}{2} < \theta < \frac{\alpha}{2} \\ 0 & otherwise \end{cases} \tag{3-6}$$

Where

$$\cos(\alpha/2) = -\frac{I_q}{I_{\max} - I_q} \tag{3-7}$$

Or

$$I_q = \frac{I_{\max}\cos(\alpha/2)}{\cos(\alpha/2)-1} \tag{3-8}$$

Substituting I_q from equation (3-8) into equation (3-6),

$$I_c = \begin{cases} \dfrac{I_{\max}\left(\cos\theta-\cos(\alpha/2)\right)}{1-\cos(\alpha/2)} & -\dfrac{\alpha}{2}<\theta<\dfrac{\alpha}{2} \\ 0 & \textit{otherwise} \end{cases} \tag{3-9}$$

Next, the dc current is simply the average of I_c. Therefore,

$$I_{dc} = \frac{1}{2\pi}\int_{-\pi}^{\pi} I_c\,d\theta = \frac{1}{2\pi}\int_{-\frac{\alpha}{2}}^{\frac{\alpha}{2}} \frac{I_{\max}\left(\cos\theta-\cos(\alpha/2)\right)}{1-\cos(\alpha/2)}\,d\theta \tag{3-10}$$

Or

$$I_{dc} = \frac{1}{2\pi}\frac{I_{\max}}{\left(1-\cos(\alpha/2)\right)}\left(\sin\theta-\theta\cos(\alpha/2)\right)\Big|_{-\frac{\alpha}{2}}^{\frac{\alpha}{2}} \tag{3-11}$$

Which simplifies to

$$I_{dc} = \frac{I_{\max}}{2\pi}\left(\frac{2\sin(\alpha/2)-\alpha\cos(\alpha/2)}{1-\cos(\alpha/2)}\right) \tag{3-12}$$

The dc supply power is then given by

$$P_{dc} = I_{dc}V_{dc} = \frac{V_{\max}}{2}\frac{I_{\max}}{2\pi}\left(\frac{2\sin(\alpha/2)-\alpha\cos(\alpha/2)}{1-\cos(\alpha/2)}\right) \tag{3-13}$$

To find the maximum fundamental output power, we first determine the magnitude of the fundamental current I_{f_0}, which is simply

$$I_{f_0} = \frac{1}{\pi}\int_{-\pi}^{\pi} I_c\cos\theta\,d\theta = \frac{1}{\pi}\int_{-\frac{\alpha}{2}}^{\frac{\alpha}{2}} \frac{I_{\max}\left(\cos\theta-\cos(\alpha/2)\right)}{1-\cos(\alpha/2)}\cos\theta\,d\theta \tag{3-14}$$

Or

$$I_{f_0} = \frac{I_{\max}}{\pi\left(1-\cos\left(\alpha/2\right)\right)}\left(\frac{\theta+\frac{\sin\left(2\theta\right)}{2}}{2}-\sin\theta\cos\left(\alpha/2\right)\right)\Bigg|_{-\frac{\alpha}{2}}^{\frac{\alpha}{2}} \tag{3-15}$$

Equation (3-15) simplifies to

$$I_{f_0} = \frac{I_{\max}}{2\pi}\left(\frac{\alpha-\sin\alpha}{1-\cos\left(\alpha/2\right)}\right) \tag{3-16}$$

Therefore, the maximum fundamental output power is

$$P_{\max} = \frac{I_{f_0}}{\sqrt{2}}\frac{V_{\max}}{2\sqrt{2}} = \frac{V_{\max}}{4}\frac{I_{\max}}{2\pi}\left(\frac{\alpha-\sin\alpha}{1-\cos\left(\alpha/2\right)}\right) \tag{3-17}$$

From equations (3-13) and (3-17) the efficiency is given as

$$\eta = \frac{P_{\max}}{P_{dc}} = \frac{1}{2}\left(\frac{\alpha-\sin\alpha}{2\sin\left(\alpha/2\right)-\alpha\cos\left(\alpha/2\right)}\right) \tag{3-18}$$

Figure 3-6 plots both the efficiency η and maximum output power versus conduction angle α. This graph was originally reported by Steve Cripps [3]. As expected, class-A mode shows an ideal efficiency of 50%. The efficiency increases as the conduction angle reduced. For a class-B amplifier, $\alpha = \pi$ yields a maximum possible efficiency of $\eta = \pi/4 = 78.54\%$. The efficiency continues to increase as the conduction angle is reduced further into class-C mode.

This plot shows a very interesting point. Between class-A and class-B modes, the maximum fundamental output power is approximately constant while the efficiency improves from $1/2$ to $\pi/4$. When the conducting angle is reduced further into class-C mode, the efficiency increases and approaches a perfect 100% when the conduction angle reaches 0°. However, the efficiency improvement is accompanied by a substantial reduction in the fundamental output power. In modern technologies, especially integrated circuits, power usually comes as a premium. Therefore, integrated circuit power amplifiers rarely operate in class-C mode because of the low maximum output power.

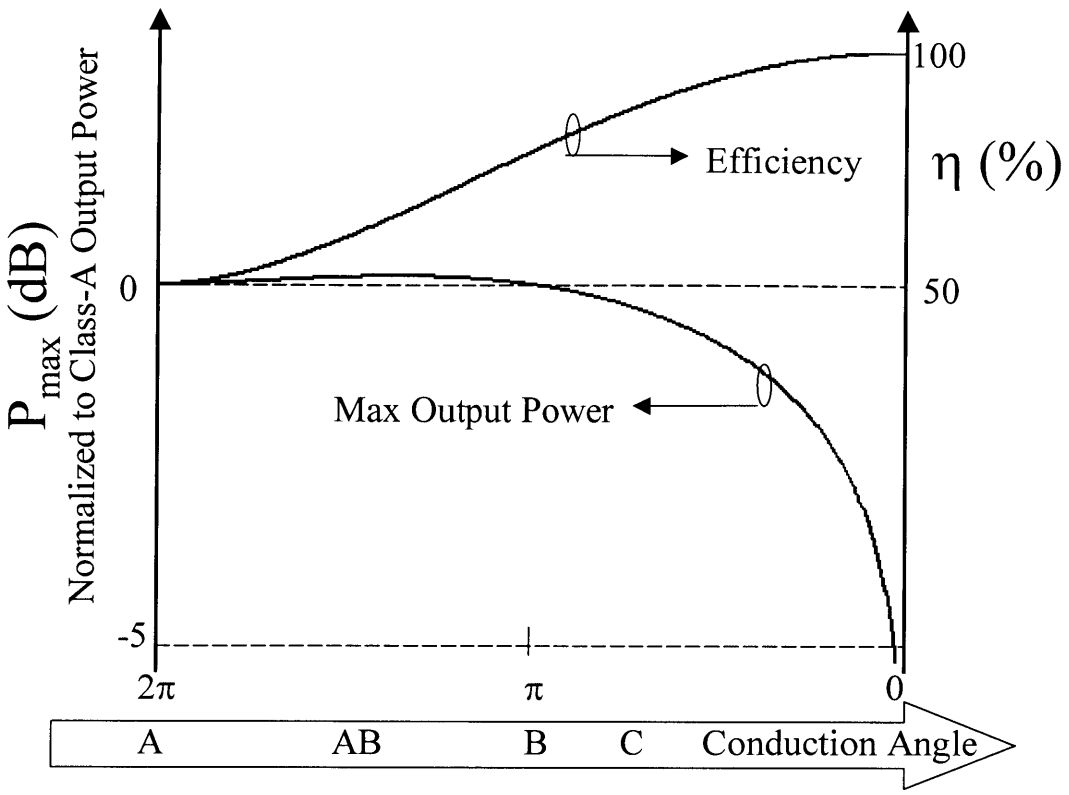

Figure 3-6: Efficiency and Maximum Output Power (Normalized to Class-A) vs. Conduction Angle

By making amplifiers more efficient with reduced conduction angle modes, we not only give up gain but linearity as well. Clipping effects on the output current waveforms introduce nonlinearities at the output. We can analyze these nonlinearities quantitatively by calculating the high order harmonics components of the output currents. The n^{th} order harmonics can be written as,

$$I_{nf_0} = \frac{1}{\pi}\int_{-\pi}^{\pi} I_c \cos(n\theta)d\theta = \frac{1}{\pi}\int_{-\alpha/2}^{-\alpha/2} \frac{I_{\max}\left(\cos\theta - \cos(\alpha/2)\right)}{1-\cos(\alpha/2)}\cos(n\theta)d\theta \qquad (3\text{-}19)$$

Using the above expression, we can determine the harmonic components of the output current as functions of the conducting angle. Results of the dc and the first five harmonics components are listed in Table 3-2.

Table 3-2: DC and Harmonics Components of Output Currents in Reduced Conduction Angle Operation Modes

	Expression	Class-A $\alpha = 2\pi$	Class-AB $\alpha = 3\pi/2$	Class-B $\alpha = \pi$
DC	$\frac{I_{max}}{2\pi}\left(\frac{2\sin(\alpha/2)-\alpha\cos(\alpha/2)}{1-\cos(\alpha/2)}\right)$	$\frac{I_{max}}{2}$	$\frac{I_{max}(3\pi+4)}{2\pi(2+\sqrt{2})}$	$\frac{I_{max}}{\pi}$
Fundamental	$\frac{I_{max}}{2\pi}\left(\frac{\alpha-\sin\alpha}{1-\cos(\alpha/2)}\right)$	$\frac{I_{max}}{2}$	$\frac{I_{max}(3\pi+2)}{2\pi(2+\sqrt{2})}$	$\frac{I_{max}}{2}$
Second	$\frac{I_{max}}{3\pi}\frac{(1-\cos\alpha)\sin(\alpha/2)}{(1-\cos(\alpha/2))}$	0	$\frac{I_{max}}{3\pi(1+\sqrt{2})}$	$\frac{2I_{max}}{3\pi}$
Third	$\frac{I_{max}}{6\pi}\frac{(1-\cos\alpha)\sin\alpha}{(1-\cos(\alpha/2))}$	0	$\frac{-I_{max}}{3\pi(2+\sqrt{2})}$	0
Fourth	$\frac{I_{max}}{60\pi}\frac{(5\sin(3\alpha/2)-3\sin(5\alpha/2))}{(1-\cos(\alpha/2))}$	0	$\frac{2I_{max}}{15\pi(1+\sqrt{2})}$	$-\frac{2I_{max}}{15\pi}$
Fifth	$\frac{I_{max}}{60\pi}\frac{(3\sin(2\alpha)-2\sin(3\alpha))}{(1-\cos(\alpha/2))}$	0	$\frac{-I_{max}}{15\pi(2+\sqrt{2})}$	0

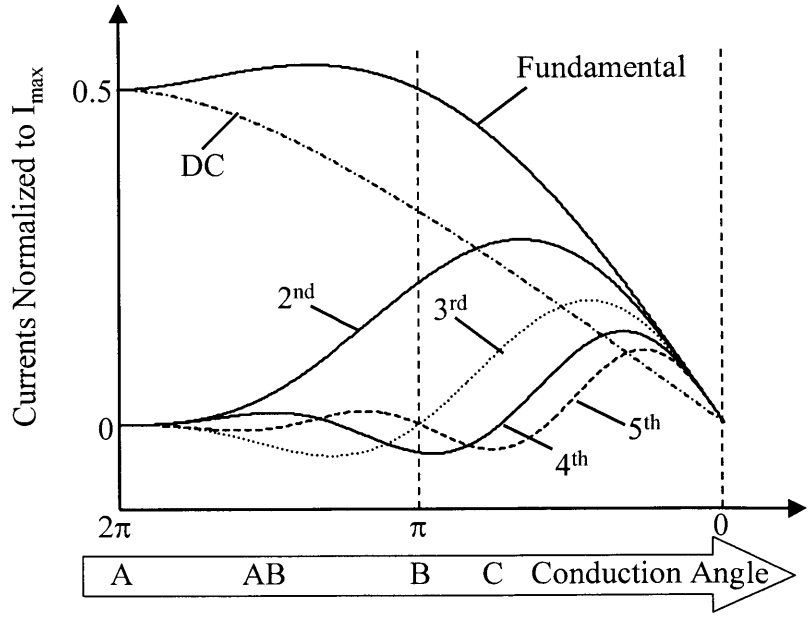

Figure 3-7: DC and Harmonics Components of The Output Current

A plot of the current components, based on the above calculation and the original idea from Steve Cripps [4], is shown in Figure 3-7. The fundamental current curve confirms our earlier

observation that between class-A and class-B conditions, the fundamental output power is approximately constant. As we reduce the conducting angle, the dc current decreases which explains the efficiency improvement. This is accompanied by the increases in harmonics. The second harmonics dominates throughout the conducting angle range. One interesting observation is that between class-A and class-B conditions, only the second harmonic is substantial, all the higher order harmonics are small. Therefore, by biasing the amplifier toward class-B condition in a differential configuration we can significantly improve the efficiency while suffer little setback in linearity.

4 Biasing Techniques

In this chapter, we will study three different fixed biasing topologies: current mirror network, diode-connect, and cascode current mirror. We analyze each topology by addressing the following questions:

- How does it work? We will discuss the role of each component in the biasing circuit, and ultimately derive the expression to determine the power transistor quiescent current.
- What are the effects of the biasing circuit on the gain, linearity, and efficiency of the amplifier stage and how do we control these effects? By answering this question, we can show the tradeoff in optimizing the circuit for a specific performance requirement.

Finally, we will look at the proposed adaptive biasing topology and study how it improves the efficiency of the overall power amplifier stage.

4.1 Current Mirror Network

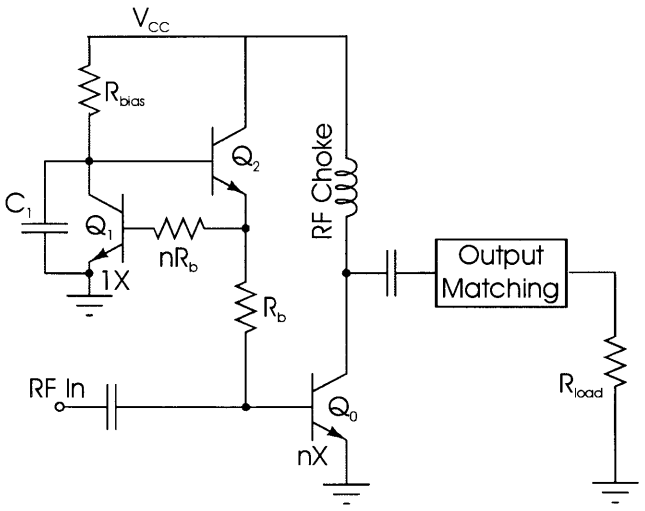

Figure 4-1: Current Mirror Biasing

4.1.1 How does it work?

Luo and Sowlati [5] reported a very popular power amplifier biasing circuitry is shown in Figure 4-1. This conventional biasing technique uses the power transistor Q_0 as part of a current mirror network. Transistors Q_0 and Q_1 form a $1:n$ current mirror network based on their size ratio. Transistor Q_2 provides base current correction for this current mirror network. The base resistors R_b and nR_b provide negative feedback to set Q_0's collector current. To see how this feedback mechanism works, consider the base-emitter loop equation across Q_0 and Q_1 as shown in Figure 4-2.

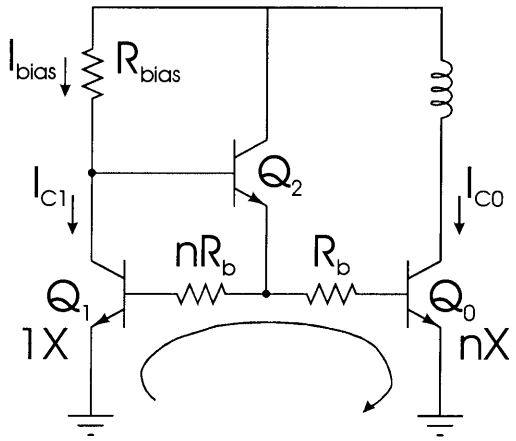

Figure 4-2: Base-Emitter Voltage Loop

$$V_{be0} + \frac{I_{c0}}{\beta} R_b = V_{be1} + \frac{I_{c1}}{\beta} nR_b \tag{4-1}$$

where

V_{be0} and V_{be1} are Q_0 and Q_1 base-emitter voltage, respectively,

$I_{c0} = I_{s0} \exp\left(\frac{V_{be0}}{V_T}\right)$ and $I_{c1} = I_{s1} \exp\left(\frac{V_{be1}}{V_T}\right)$ are Q_0 and Q_1 collector currents,

β is the dc current gain of the transistors.

An obvious solution for the above equation is $I_{c0} = nI_{c1}$ where $V_{be0} = V_{be1}$. Consider, however, the case when V_{be0} drops below V_{be1}. The voltage across resistor R_b will increase which forces more current into transistor Q_0's base. This extra base current increases Q_0's collector current by a factor of β which, in turn raises V_{be0} back up.

Similarly, when V_{be0} rises above V_{be1}, the voltage across R_b is smaller. This leads to smaller base and collector currents for Q_0, which reduces V_{be0}. Therefore, Q_0 collector current I_{c0} is always set at nI_{c1}. By choosing the appropriate scaling ratio between the two transistors Q_0 and

Q_1, we can set the quiescent collector current for the power transistor Q_0 while minimizing the current consumption by the biasing network.

Resistor R_{bias} sets the dc collector current for Q_1. Ignore the base current and the voltage drops across the base resistors, we have

$$I_{c1} \approx I_{bias} = \frac{\left(V_{CC} - 2V_{BE(on)}\right)}{R_{bias}} \tag{4-2}$$

Therefore, Q_0 collector current is determined by

$$I_{c0} = \frac{n\left(V_{CC} - 2V_{BE(on)}\right)}{R_{bias}} \tag{4-3}$$

The bypass capacitor C_1 is used to short out any RF signal might present at transistor Q_1's collector preventing the current I_{bias} from being modulated by the RF signal.

4.1.2 Effects on gain, linearity, and efficiency

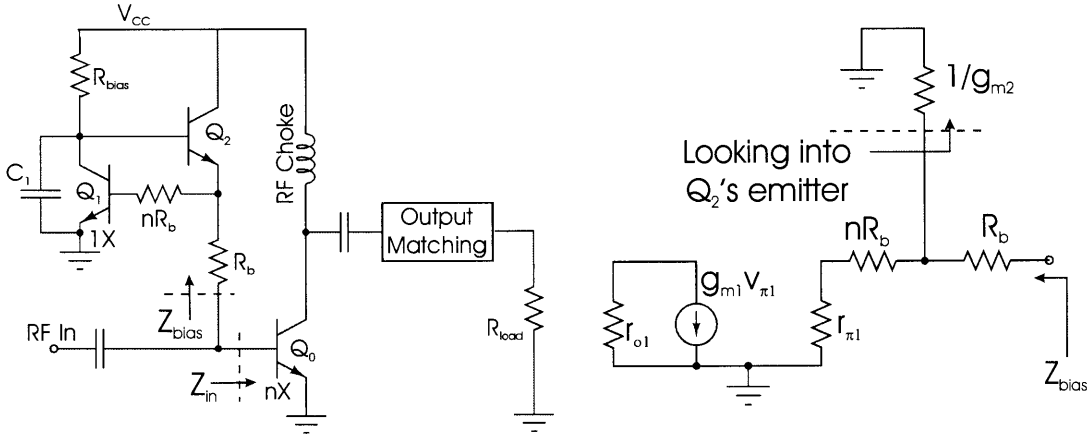

Figure 4-3: Small Signal Equivalent Circuit for Conventional Biasing

Let Z_{bias} and Z_{in} be the small signal equivalent resistances of the biasing circuit and the power transistor, respectively, as shown in Figure 4-3. Depending on the resistance ratio Z_{bias}/Z_{in}, a certain portion of the RF signal splits into the biasing circuit, thereby reduces the gain of the amplifier stage. To minimize the biasing circuit's effect on gain and linearity Z_{bias} has to be much larger than Z_{in}.

Assuming that the bypass capacitor C_1 is large enough so that Q_1's collector is at ac ground, from the equivalent small signal circuit for the biasing circuitry in Figure 4-3, we can determine Z_{bias} as

$$Z_{bias} = R_b + (1/g_{m2}) \| (nR_b + r_{\pi 1}) \tag{4-4}$$

Typically, $1/g_{m2}$ is much smaller than $nR_b + r_{\pi 1}$. Therefore, equation (4-4) simplifies to

$$Z_{bias} = R_b + 1/g_{m2} \tag{4-5}$$

The quiescent collector current of transistor Q_2 is the sum of the two base currents of transistors Q_0 and Q_1.

$$I_{c2} = I_{b0} + I_{b1} \tag{4-6}$$

Rewrite in terms of Q_0's collector current and the current ratio n.

$$I_{c2} = \left(\frac{n+1}{n^2}\right) I_{c0} \tag{4-7}$$

Combine equations (4-5) and (4-7)

$$Z_{bias} = R_b + \frac{kT}{qI_{c2}} = R_b + \frac{n^2}{(n+1)} \cdot \frac{kT}{qI_{c0}} \tag{4-8}$$

By selecting the appropriate value for the base resistor R_b and the current ratio n, we can make sure that Z_{bias} is much larger than Z_{in} so that the biasing circuit does not affect the RF drive signal feeding to Q_0's base. However, there is a limit of how big R_b can be. The base current of a power transistor could be several milliamps. If we make R_b too big, the energy loss due to R_b is significant. In addition, the voltage drop across R_b could reduce the overall voltage headroom and invalidate the initial assumption of negligible base resistance voltage.

With regard to efficiency, the biasing circuit should consume as little energy as possible. By increasing the scaling ratio n of the current mirror, we can reduce the current used in the biasing circuit. However, the dependency of Q_0's collector current on process variation in R_{bias}, R_b and Q_1 is also scaled by n. Therefore, there is a tradeoff between reducing the current needed for the biasing circuit and keeping the process variation tolerable.

4.2 Diode-Connect

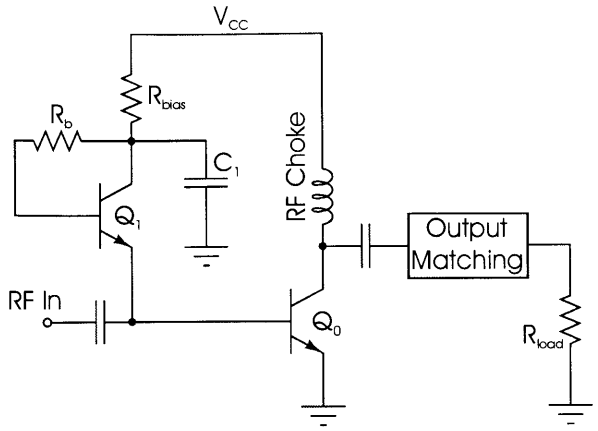

Figure 4-4: Diode-Connect Biasing

4.2.1 How does it work?

Kawamura, et al, [6] proposed diode-connect biasing circuit shown in Figure 4-4. Transistor Q_1 is diode-connected with a series base resistor R_b. Ignore Q_1's base current, the current through R_{bias} is

$$I_{bias} = \frac{V_{CC} - 2V_{BE(on)}}{R_{bias}} \tag{4-9}$$

I_{bias} is the base dc current of transistor Q_0. Therefore, Q_0's collector current is determined by

$$I_{c0} = \beta\left(\frac{V_{CC} - 2V_{BE(on)}}{R_{bias}}\right) \tag{4-10}$$

The bypass capacitor C_1 is used to short out any RF signal at transistor Q_1's collector preventing the current I_{bias} from being modulated by the RF signal.

4.2.2 Effects on gain, linearity, and efficiency

Again, let Z_{in} and Z_{bias} be the equivalent input resistances of the biasing circuit and power amplifier, respectively.

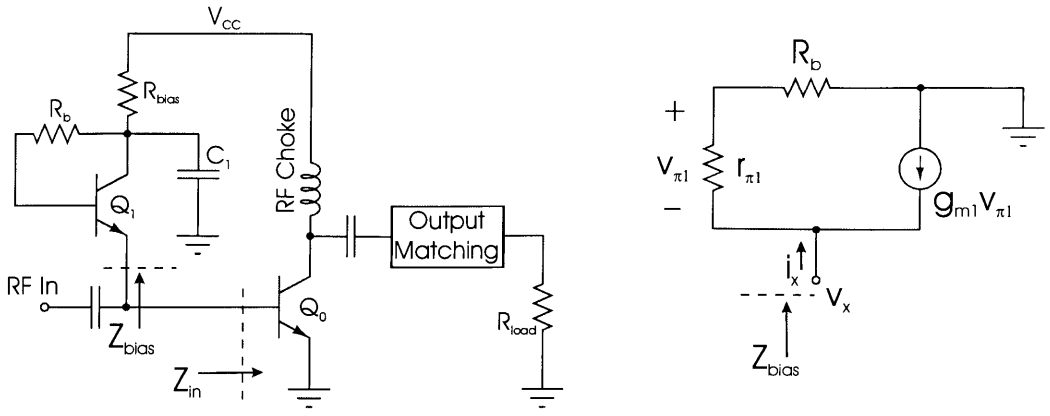

Figure 4-5: Small Signal Equivalent Circuit for Diode-Connect Biasing

Assuming that the bypass capacitor C_1 is large enough so that Q_1's collector is at ac ground, the small signal circuit for the biasing circuitry is shown in Figure 4-5. To find Z_{bias} we apply a test voltage to Q_1's emitter. Kirchoff current law at Q_1's emitter gives

$$I_x = \frac{V_x}{r_{\pi 1} + R_b} + g_{m1}\frac{r_{\pi 1} V_x}{r_{\pi 1} + R_b} \tag{4-11}$$

Or

$$I_x = \frac{(1+\beta)V_x}{r_{\pi 1} + R_b} \tag{4-12}$$

Therefore

$$Z_{bias} = \frac{V_x}{I_x} = \frac{r_{\pi 1} + R_b}{1+\beta} \approx \frac{1}{g_{m1}} + \frac{R_b}{\beta} \tag{4-13}$$

Q_1's collector current is simply Q_0's base current. Therefore, equation (4-13) can be rewritten as

$$Z_{bias} = \frac{\beta kT}{qI_{c0}} + \frac{R_b}{\beta} \tag{4-14}$$

From equation (4-14), we can see that by selecting an appropriate value for R_b we can make Z_{bias} sufficiently larger than Z_{in} to make sure that the biasing circuit does not affect the gain of the amplifying stage.

The biasing circuit does not consume any extra current beside the base current for the power transistor. Therefore, it does not affect the overall efficiency of the amplifying stage.

4.3 Cascode Current Mirror

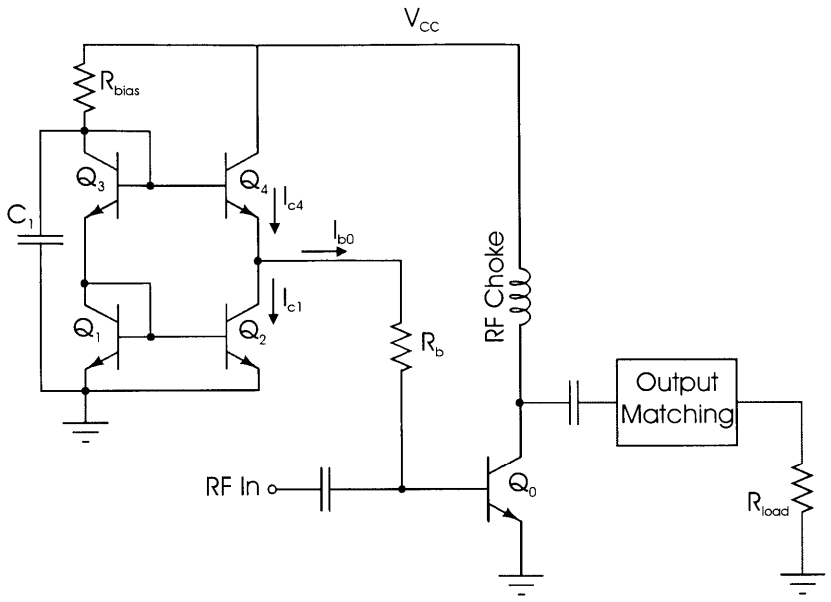

Figure 4-6: Cascode Current Mirror Biasing

4.3.1 How does it work?

In the biasing scheme shown in Figure 4-6, transistors Q_1, Q_2, Q_3, and Q_4 form a cascode current mirror network. Q_0 is biased by tapping off Q_2's collector with a series resistor R_b. The current through R_{bias} is the given by

$$I_{bias} = \frac{V_{CC} - 2V_{BE(on)}}{R_{bias}} \tag{4-15}$$

The bypass capacitor C_1 is used to short out any RF signal at transistor Q_3's collector preventing the current I_{bias} from being modulated by the RF signal. Ignore the base currents, we have

$$I_{c1} = I_{c3} = I_{c2} = I_{bias} \tag{4-16}$$

From Kirchoff current law for Q_2's collector node,

$$I_{c4} = I_{c2} + I_{b0} \tag{4-17}$$

Or

$$I_{c4} = I_{bias} + \frac{I_{c0}}{\beta} \tag{4-18}$$

Assume the voltage across R_b is negligible,

$$V_{be1} + V_{be3} = V_{be4} + V_{be0} \tag{4-19}$$

Replacing V_{be} in equation (4-18) with their corresponding collector currents,

$$V_t \ln\left(\frac{I_{c1}}{I_s}\right) + V_t \ln\left(\frac{I_{c3}}{I_s}\right) = V_t \ln\left(\frac{I_{c4}}{I_s}\right) + V_t \ln\left(\frac{I_{c0}}{I_s}\right) \tag{4-20}$$

Combine equations (4-16), (4-18), and (4-20)

$$V_t \ln\left(\frac{I_{bias}}{I_{s1}}\right) + V_t \ln\left(\frac{I_{bias}}{I_{s3}}\right) = V_t \ln\left(\frac{I_{bias} + I_{c0}/\beta}{I_{s4}}\right) + V_t \ln\left(\frac{I_{c0}}{I_{s0}}\right) \tag{4-21}$$

Assume that transistors Q_1, Q_2, Q_3, and Q_4 have the same emitter area, and let n be the emitter size ratio between transistors Q_0 and Q_1, equation (4-21) reduces to

$$I_{bias}^2 = \frac{I_{c0}}{n}\left(I_{bias} + \frac{I_{c0}}{\beta}\right) \tag{4-22}$$

Solve for I_{c0} and replacing I_{bias} with equation (4-15),

$$I_{c0} = \frac{\left(\sqrt{\beta^2 + 4n\beta} - \beta\right)}{2} I_{bias} = \frac{\left(\sqrt{\beta^2 + 4n\beta} - \beta\right)}{2} \frac{\left(V_{cc} - 2V_{BE(on)}\right)}{R_{bias}} \tag{4-23}$$

By selecting the appropriate values for resistor R_{bias} and transistor area ratio n we can set the bias condition for the power transistor Q_0.

4.3.2 Effects on gain, linearity, and efficiency

Again, assuming that the bypass capacitor C_1 is large enough so that Q_3 's collector is at ac ground, the small signal circuit for the biasing circuitry in is shown in Figure 4-7. We can immediately write the equivalent resistance as

$$Z_{bias} = R_b + 1/g_{m4} \tag{4-24}$$

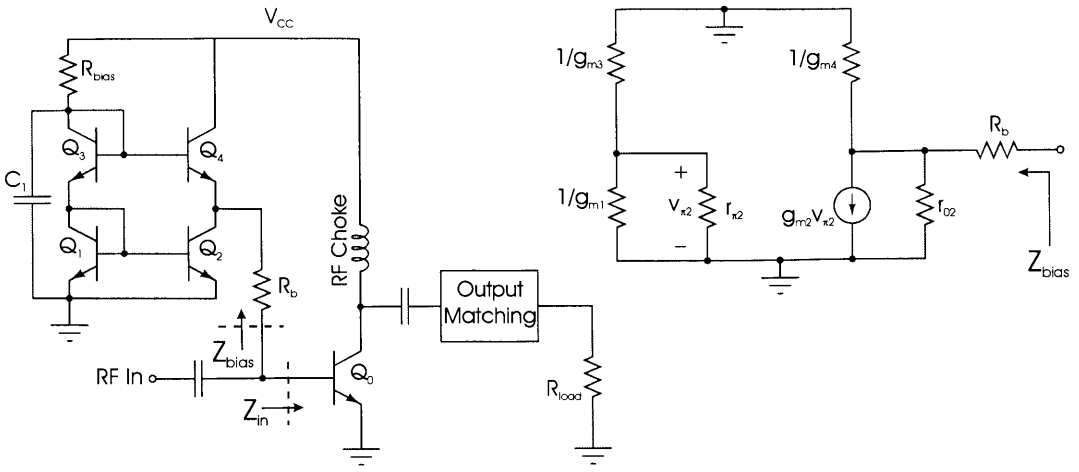

Figure 4-7: Small Signal Equivalent Circuit for Cascode Current Mirror Biasing

Q_4's collector current is simply the sum of Q_2's collector and Q_0's base currents. We can relate Q_2's collector current to that of Q_0's as shown in equation (4-23).

$$Z_{bias} = R_b + \frac{kT}{q(I_{c2} + I_{b0})} = R_b + \frac{kT}{q\left(\frac{2I_{c0}}{\left(\sqrt{\beta^2 + 4n\beta} - \beta\right)} + \frac{I_{c0}}{\beta}\right)} \tag{4-25}$$

As usual, we would like to have Z_{bias} much larger than Z_{in} to minimize the biasing circuit effects on the stage gain. By choosing appropriate values for resistor R_b we can make Z_{bias} much larger than Z_{in}. Making the transistors ratio n larger reduces the power consumed by the biasing circuit, and therefore, increases the overall efficiency of the stage. However, as the case in the conventional current mirror biasing, there is a tradeoff in making R_b and n large.
When R_b is too big, the energy loss due to R_b is significant. In addition, the voltage drop across R_b could substantially reduce the overall headroom.
The dependency of Q_0's collector current on process variation in R_{bias}, R_b and Q_1 is also scaled by n. We should make n as large as possible while keeping the process variation tolerable.

4.4 Adaptive Biasing

4.4.1 The Concept

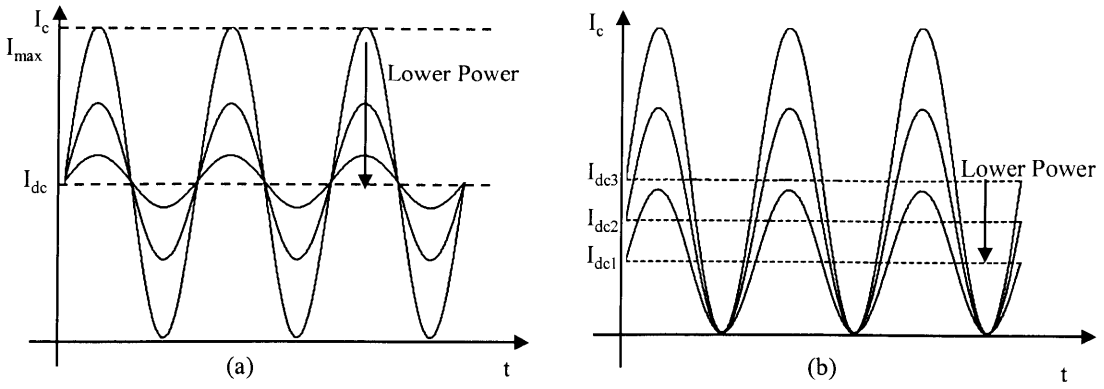

Figure 4-8: Collect Current in Fixed Biasing (a) and Adaptive Biasing (b)

As discussed in section 1.2, power amplifiers with fixed biasing schemes are inefficient at low output levels, where the collector current does not swing across the full available linear range of I_{max} as shown in Figure 4-8a. Therefore, a logical way to improve the efficiency at low levels operation is to use adaptive biasing where the biasing current I_{dc} changes such that the collector current always utilizes its maximum available linear range as shown in Figure 4-8b.

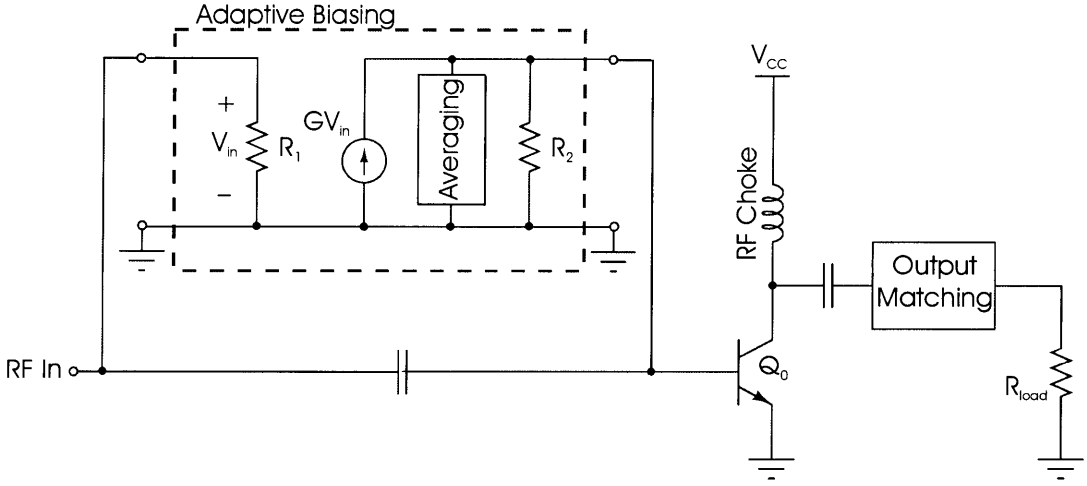

Figure 4-9: Adaptive Biasing Circuit Concept

Figure 4-9 shows this adaptive biasing concept as a two-port network. The input port with resistance R_1 senses the RF input voltage. This input voltage is transformed to a current output with a transconductance G. The current is then averaged and fed into the base of the power transistor Q_0. The output resistance is R_2. As usual, we want both R_1 and R_2 large so that they do not load the RF drive and reduce the gain of the amplifying stage.

4.4.2 How does it work?

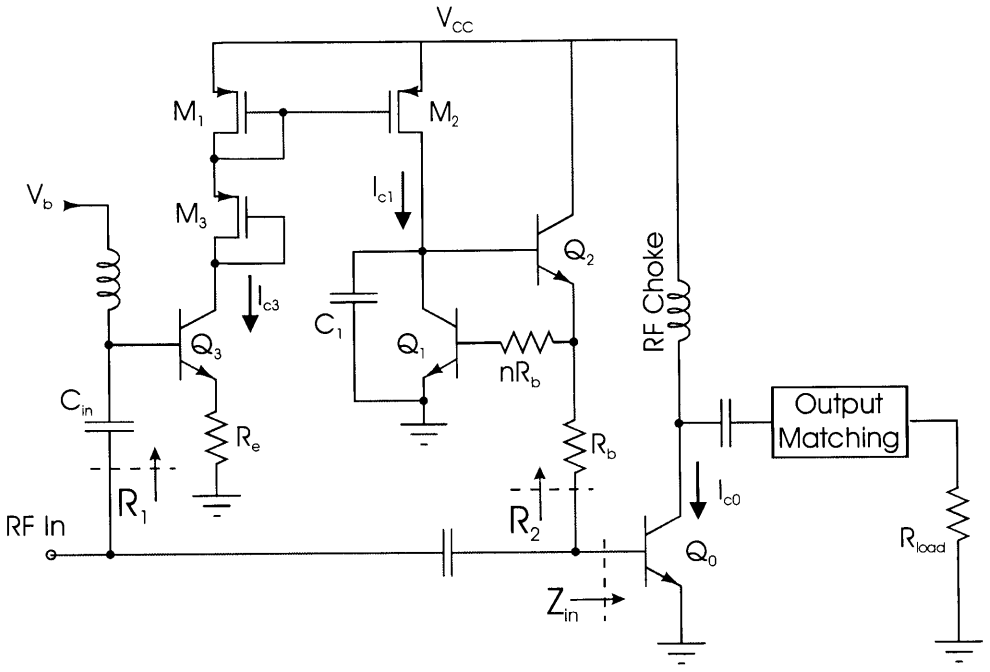

Figure 4-10: Adaptive Biasing

Figure 4-10 shows a circuit implementation for the adaptive biasing scheme. The power transistor Q_0 is used in a current mirror configuration with Q_1 in the familiar conventional biasing discussed in section 4.1. However, instead of the resistor R_{bias} providing a fixed biasing current, we have the PMOS M_2 generating a current proportional to the RF input level. To see how the biasing current changes based on the input level, let's start from the RF In node.

Transistor Q_3 is used as a common emitter with an emitter degeneration resistor R_e and a PMOS load of M_1 and M_3. The RF input voltage modulates Q_3's collector current, which is the same as the drain currents of M_1 and M_3. This modulated current is then mirrored to M_2 and fed to the averaging circuit consisting of the bypass capacitor C_1 and transistors Q_1 and Q_2. The end result is an adaptive dc collector current for Q_1, which sets the collector current for the power transistor Q_0.

When there is no RF input, Q_3's base voltage V_b sets the initial biasing current.

$$V_b = V_{be(on)} + I_{c3}R_e \tag{4-26}$$

Or

$$I_{c3} = \frac{V_b - V_{be(on)}}{R_e} \tag{4-27}$$

Let m be the scaling ratio of M_1 and M_2 PMOS current mirror. Then

$$I_{c1} = mI_{c3} \tag{4-28}$$

As before, n is the scaling ratio of Q_1 and Q_0 current mirror.

$$I_{c0} = nI_{c1} \tag{4-29}$$

Combine equations (4-27), (4-28), and (4-29) we have the equation determining the initial biasing current for the power transistor Q_0.

$$I_{c0} = n \cdot m \cdot \left(\frac{V_b - V_{be(on)}}{R_e} \right) \tag{4-30}$$

Therefore, by selecting the appropriate values for V_b, R_e, n, and m we can set the initial idling current for transistor Q_0. We can generate multiple adapting currents for multiple stages by adding more branches to the PMOS current mirror involving M_1.

4.4.3 Effects on gain, linearity, and efficiency

Again, let R_1 and R_2 be the input and output small signal equivalent resistances of the two-port adaptive biasing as shown in Figure 4-10. Also, let Z_{in} be the equivalent resistance looking into the base of the power amplifier Q_0. To minimize the effects of the biasing circuit on the stage gain, we want both R_1 and R_2 much larger than Z_{in}. We already calculated R_2 from equation (4-5) in section 4.1. The result is repeated here.

$$Z_{bias} = R_b + 1/g_{m2} \tag{4-31}$$

As discussed in section 4.1 we can make R_2 large by making R_b arbitrary large. However, when R_b is too big, we will loose headroom dues to the voltage drops across R_b. The energy loss dues to R_b is also significant in this case and might affect the overall efficiency.

To calculate R_1, let's look at the equivalent small signal circuit of transistor Q_3 as shown in Figure 4-11. Apply a test voltage to Q_3's base, we have

$$V_x = r_{\pi 3} I_x + \left(1 + g_{m3} r_{\pi 3}\right) I_x R_e \tag{4-32}$$

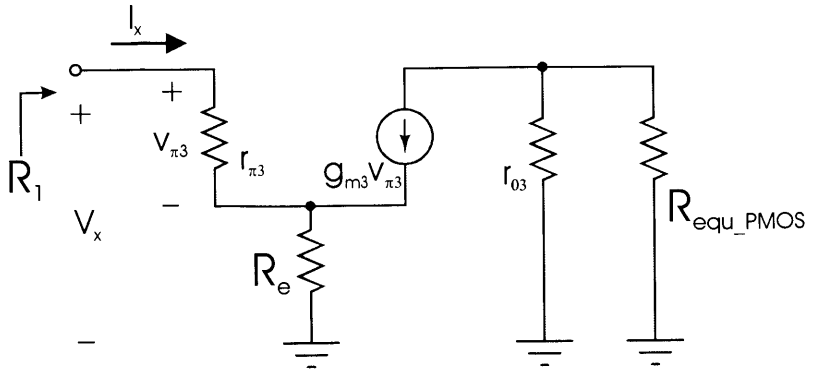

Figure 4-11: Small Signal Equivalent Circuit for Adaptive Biasing

Or

$$R_1 = \frac{V_x}{I_x} = r_{\pi 3} + (1+\beta)R_e \tag{4-33}$$

From equation (4-33), we can select the appropriate value for R_e such that R_1 is significantly larger than Z_{in}.

4.4.4 The Averaging Circuit

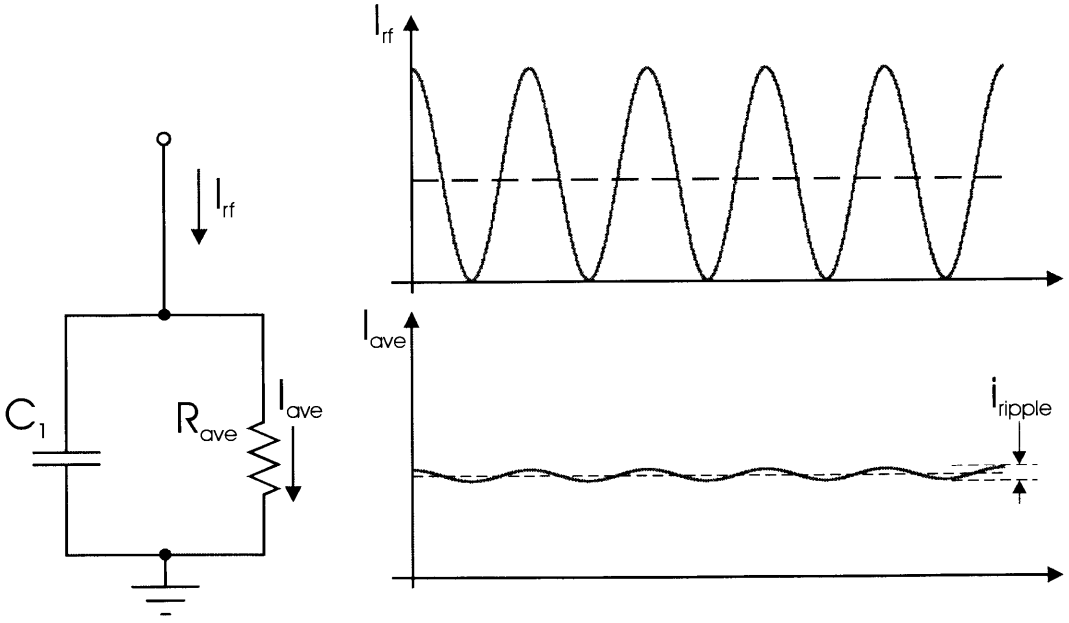

Figure 4-12: R-C Averaging Circuit

At the heart of this adaptive biasing idea is the averaging circuit consisting of the parallel combination of capacitor C_1 and resistor R_{ave} as shown in Figure 4-12. For the specific adaptive biasing schematic in Figure 4-10, R_{ave} is the equivalent resistance of the bipolar Q_0, Q_1, and Q_2 current mirror setup.

The time constant $\tau = R_{ave}C_1$ sets two deciding factors for the averaging circuit. First, it determines the amount of ripples of the averaged current I_{ave}. This is a basic one-pole system where the current amplitude rolls off 6dB/dec after the pole at $f_p = \frac{1}{R_{ave}C_1}$. Figure 4-13 shows a set of Bode responses of the averaging circuit for different pole frequencies.

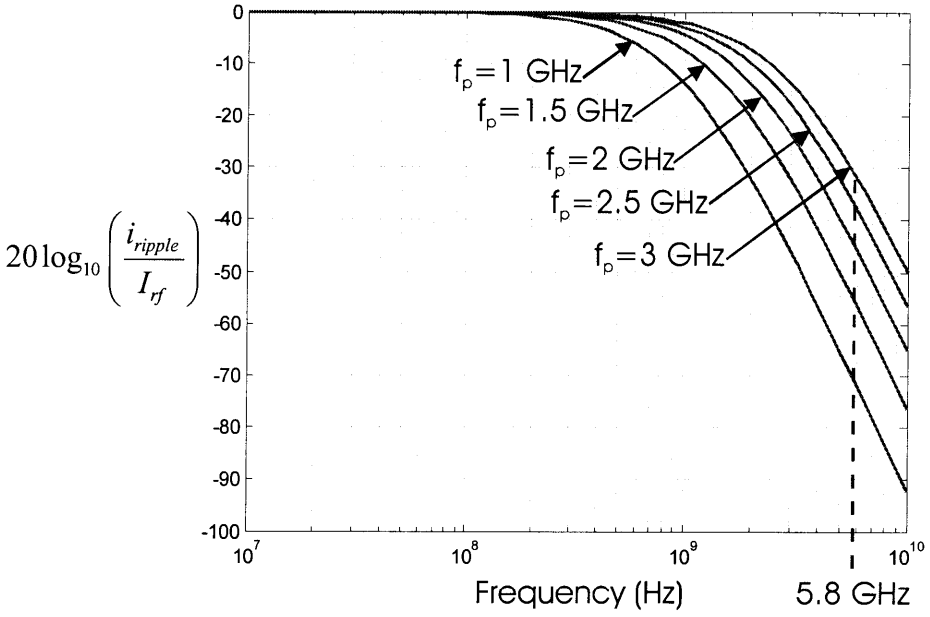

Figure 4-13: Ripple Attenuation of the Averaging Circuit with Different Pole Location

The vertical axis shows the amount of ripple attenuation in dB versus frequency on the horizontal axis. Ideally we want the averaged current I_{ave} to be pure dc, which means infinite ripple attenuation. For practical design, we assume that 2% ripple is tolerable. That is

$$\frac{i_{ripple}}{I_{rf}} = \frac{i_{ripple}}{2I_{ave}} = 0.01 \qquad (4\text{-}34)$$

On the logarithmic scale, this is equivalent to 40dB attenuation. From Figure 4-13, a pole at 2GHz provides 45dB attenuation at the operating frequency of 5.8GHz. Obviously, better ripple attenuation can be achieved by moving the pole closer to zero. However, moving the pole closer to zero also slows down the circuit, which brings us to the second effect of the time constant $\tau = R_{ave}C_1$ on the averaging circuit.

The time constant $\tau = R_{ave}C_1$ also determines how fast the adaptive current tracks the change in RF input voltage. Let's look at an example waveform of a QAM system as shown in Figure 4-14. Let T_S be the symbol period and T_C be the carrier period.

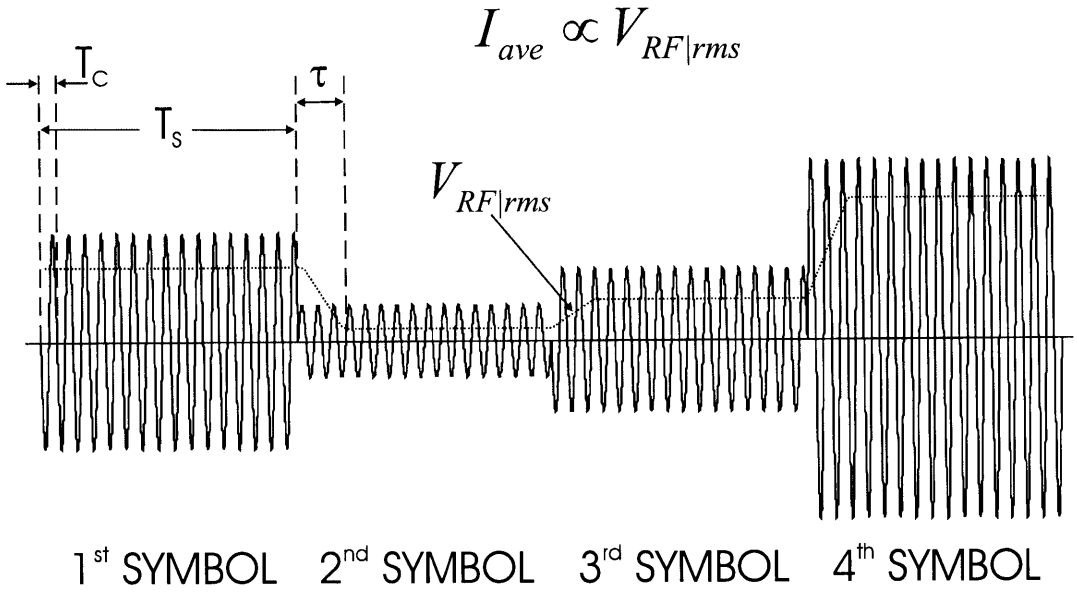

Figure 4-14: Example of 256-QAM Waveform with Symbol Period T_S, Carrier Period T_C, and Averaging Time Constant τ

We would like the averaging circuit to response fast enough to track the symbol amplitude. That means the time constant τ is much smaller than the symbol period T_S. In addition, we want the averaging circuit response to be much slower than the carrier frequency so that the biasing current stays constant over the whole symbol. Collectively, we need

$$T_C << \tau << T_S \tag{4-35}$$

T_C is readily given from the carrier frequency f_0, while T_S can be calculated from the data rate and levels of QAM. Suppose the modulation is 256-QAM, and the data rate is 100 Megabit per second. There are 8 symbols in 256-QAM. Therefore, the symbol rate is

$$S = \frac{10^8}{8} = 12.5 \text{ Mega-Symbols/sec} \tag{4-36}$$

Then the symbol period is simply

$$T_S = \frac{1}{S} = 80ns \tag{4-37}$$

In general for n-QAM, and data rate of R bits per second

$$T_S = \frac{\log_2 n}{R} \tag{4-38}$$

In summary, for a system using n-QAM, f_0 carrier frequency, data rate R bits per second, the averaging circuit should be designed such that

- The ripple attenuation on the Bode plot at the carrier frequency f_0 is better than 40dB
- The time constant $\tau = R_{ave}C_1$ satisfies the condition $\frac{1}{f_0} << \tau << \frac{\log_2 n}{R}$

5 Designing a Class-A Power Amplifier

5.1 Optimal Load and Output Matching Network

For power amplifiers, optimal loads are often different than the conjugate match of the output impedance. Circuit designers who are not familiar with power amplifier design usually find this difference very confusing. Section 5.1.1 is devoted to clarifying the difference between the familiar conjugate match and power match using in power amplifier design. Section 5.1.3 gives detailed explanations of why it is important to use the power match criteria in designing matching networks for power amplifiers.

5.1.1 Conjugate Match vs. Power Match

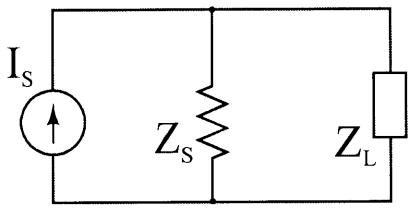

Figure 5-1: Current Generator with Impedance Z_S Delivers Power to Load Z_L

Consider a generator with impedance Z_S delivers power to the load Z_L as in Figure 5-1. It is well known that maximum power delivery occurs when Z_L and Z_S are conjugate matched. That is

$$Z_L = Z_S^* \tag{5-1}$$

However, as Steve Cripps mentioned in his book [7], the above result is only true for ideal generators. For practical devices, especially for output current generator of a transistor, there are physical limits, both in terms of the current it can supply, as well as the voltage it can sustain across its terminals. Consider, for example, a current generator that can supply a maximum

current of 500mA with an output resistance of 50Ω. Using the conjugate match rule, a load of 50Ω will yield maximum output power. However, the voltage appearing across the generator terminals would be 25V. If the current generator were the output of an integrated circuit transistor, it is likely that this would exceed the voltage rating of the device. Moreover, the transistor voltage would be limited by the available dc supply.

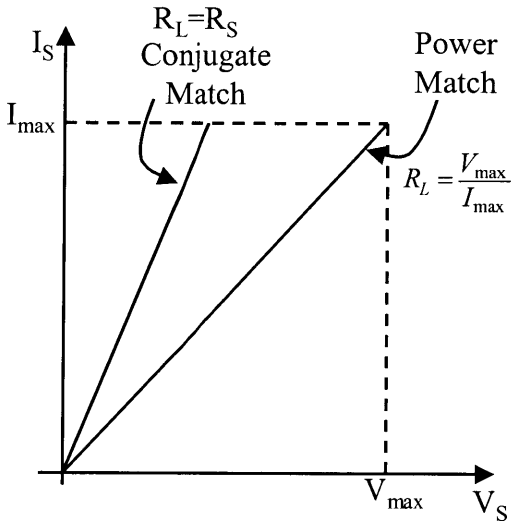

Figure 5-2: Conjugate Match Yields Less Power than Power Match

In generators with such limits, the maximum power transfer occurs when $R_L = \frac{V_{max}}{I_{max}}$ as demonstrated in Figure 5-2.

The difference between conjugate match and power match is also very important in designing matching networks, which will be addressed in section 5.1.3.1.

5.1.2 Optimal Load

Consider an inductively coupled power amplifier with load impedance R_{opt} as shown in Figure 5-3. Assume the transistor is biased with a quiescent collector current I_{dc}. Under sinusoidal excitation, the collector voltage and current are also sinusoidal with the average values of V_{cc} and I_{dc}, respectively. Clearly for optimum power match,

$$R_{opt} = \frac{V_{cc}}{I_{dc}} \tag{5-2}$$

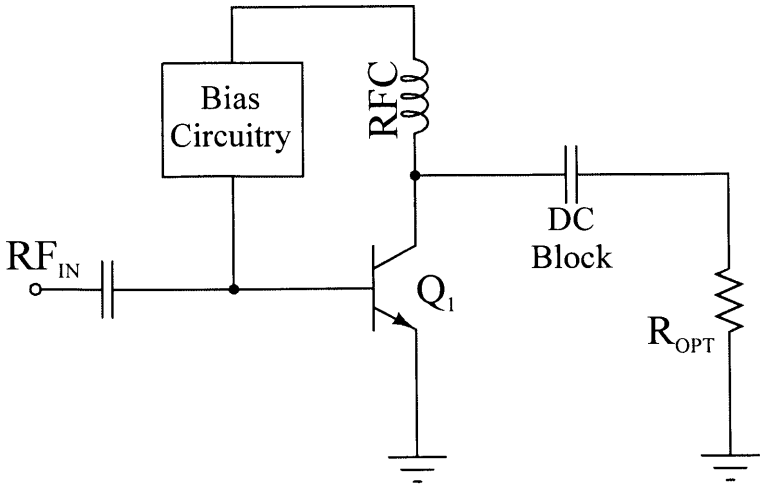

Figure 5-3: Power Amplifier Optimal Load

Under the power-matched condition, the current and voltage swing over their maximum linear range from 0 to $I_{\max}$, and 0 to $2V_{cc}$, respectively. Figure 5-4 shows both the collector voltage and current at the maximum linear output power. We can write the expression for the maximum rms output power as

$$P_{out\_\max} = \frac{\left(\frac{V_{cc}}{\sqrt{2}}\right)^2}{R_{opt}} = \frac{V_{cc}^2}{2R_{opt}} \tag{5-3}$$

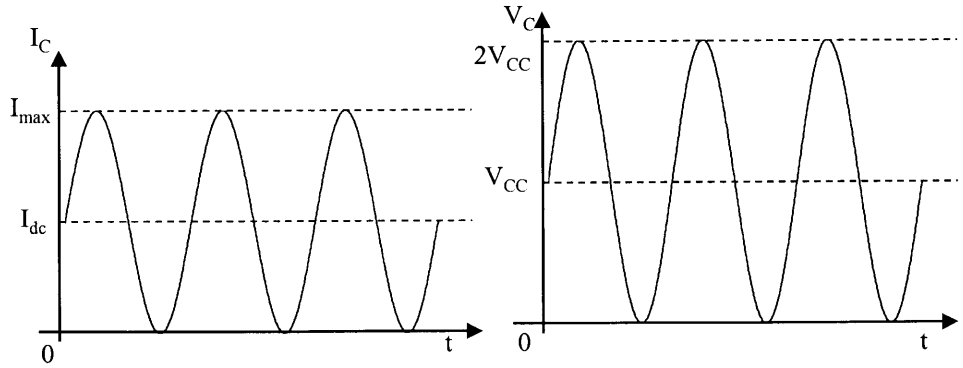

Figure 5-4: Maximum Linear Collector Current and Voltage Waveforms

Therefore, R_{opt} is determined by the maximum output power $P_{out\_\max}$ and the supply voltage V_{cc}.

$$R_{opt} = \frac{V_{cc}^2}{2P_{out\_\max}} \tag{5-4}$$

In practice, the transistor will saturate before the collector voltage reaches zero. Therefore, the maximum linear peak-to-peak voltage should be $2\left(V_{cc}-V_{ce\_sat}\right)$. Then,

$$R_{opt}=\frac{\left(V_{cc}-V_{ce\_sat}\right)^2}{2P_{out\_\max}} \tag{5-5}$$

To prevent the transistor from entering saturation, we should "overestimate " V_{ce_sat} in calculating the optimal load resistance.

5.1.3 Matching Networks

5.1.3.1 Power Contours and Mismatched Circles

Depending on the frequency range, matching networks of lumped reactance elements (i.e. inductors and capacitors) or transmission lines are used to transform the antenna impedance (usually 50Ω) to R_{opt}. However, due to component variation as well as different operating frequencies (within the signal bandwidth), loads different than R_{opt} are often presented at the transistor output. These load mismatches reduce the output power and degrade the amplifier performance. If we can determine a certain set of impedances on the Smith chart, where the power reduction due to load mismatch is less than a certain value, say 0.5-dB, then we can design the matching network such that possible mismatches are confined into this 0.5-dB area. Therefore, we are interested in determining a contour of impedances with constant power reduction. These contours give us targeting zones to design matching networks. The work presented here in this section is a detailed derivation from the original power contour graphs by Steve Cripps [8].

First, lets approach the problem using conventional load mismatch. Figure 5-5 shows an ideal voltage source with a source resistance R_{opt} driving a conjugate-matched load and a mismatched load.

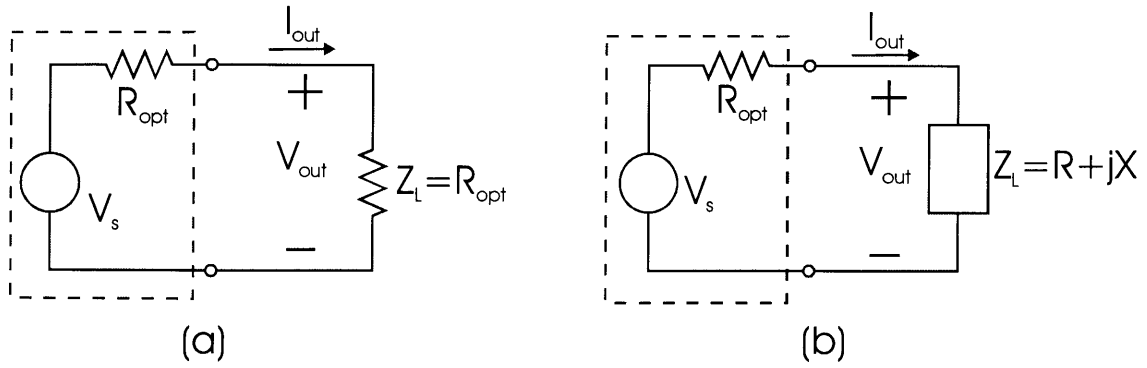

Figure 5-5: Ideal Voltage Source Driving (a) an Optimal Load and (b) a Mismatched Load

In the first case, when the source is driving a conjugate-matched load $Z_L = R_{opt}$, the maximum rms power delivered is

$$P_{\max} = \frac{1}{2} V_{out} I_{out} = \frac{1}{2} \cdot \frac{V_s}{2} \cdot \frac{V_s}{2R_{opt}} = \frac{V_s^2}{8R_{opt}} \tag{5-6}$$

In the second case, when a mismatched load of $Z_L = R + jX$ is presented at the output. The real power transferred to this load is

$$P_L = \frac{1}{2}\mathrm{Re}\left(V_{out} I_{out}^*\right) = \frac{1}{2}\mathrm{Re}\left(\frac{(R+jX)V_s}{\left(R_{opt}+R+jX\right)} \cdot \frac{V_s}{\left(R_{opt}+R+jX\right)^*} \right) = \frac{V_s^2 R}{2\left(\left(R_{opt}+R\right)^2 + X^2\right)} \tag{5-7}$$

We are interested in mismatched loads that reduce the output power by a factor of m (for clarity, use m=2 which correspond to 3-dB power reduction). That is

$$P_L = \frac{P_{\max}}{m} \tag{5-8}$$

Replace the terms in equation (5-8) by equations (5-6) and (5-7)

$$\frac{V_s^2 R}{2\left(\left(R_{opt}+R\right)^2 + X^2\right)} = \frac{V_s^2}{8mR_{opt}} \tag{5-9}$$

or

$$\left(R-(2m-1)R_{opt}\right)^2 + X^2 = \left(4m^2-4m\right)R_{opt}^2 \tag{5-10}$$

On the Smith chart, these mismatched loads form a family of circles with radius $\sqrt{\left(4m^2-4m\right)R_{opt}^2}$ and center at $\left((2m-1)R_{opt}, 0\right)$ as shown in Figure 5-6.

Again, the above approach ignores the current $I_{\max}$ and voltage $V_{\max}$ limits of the transistor current generator. Lets revisit the problem using the power match condition.

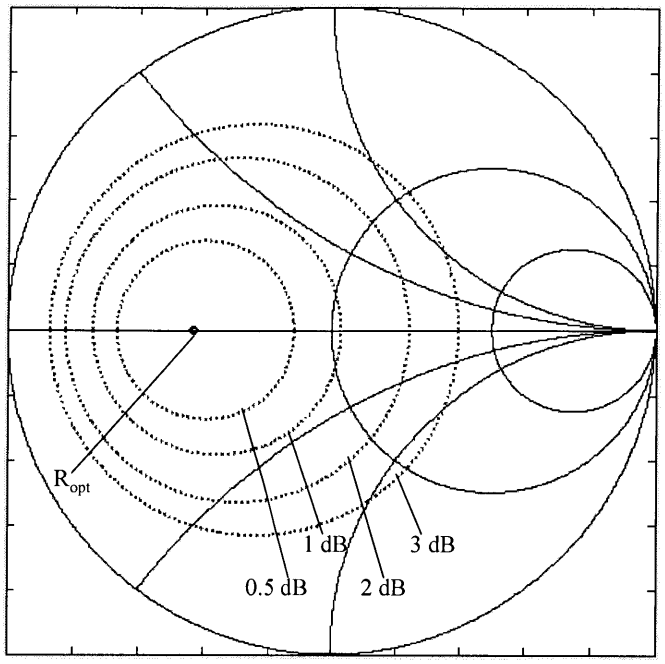

Figure 5-6: Mismatched Circles

Figure 5-7 shows two resistive terminations $\frac{R_{opt}}{m}$, and mR_{opt} that result in an output power of $\frac{P_{opt}}{m}$. Consider the load $\frac{R_{opt}}{m}$, when the current reaches its limit $I_{\max}$, the voltage is $\frac{V_{\max}}{m}$. Therefore, while keeping the current at $I_{\max}$ we can increase the voltage by adding a series reactance $\pm jX$ to the load, without changing the power. In other words, the point $\frac{R_{opt}}{m}$ can be extended into a continuous arc segment of constant power if some series reactance is added to the load. That is

$$Z = \frac{R_{opt}}{m} \pm jX \tag{5-11}$$

Obviously, the limit occurs when $|Z|_M = R_{opt}$, where the voltage reaches its maximum permissible value $V_{\max}$. The limiting reactance values can be computed as follow.

$$\left| \frac{R_{opt}}{m} \pm jX_M \right| = R_{opt} \tag{5-12}$$

Solve for X_m,

$$X_M = \pm R_{opt}\sqrt{1-\frac{1}{m^2}} \tag{5-13}$$

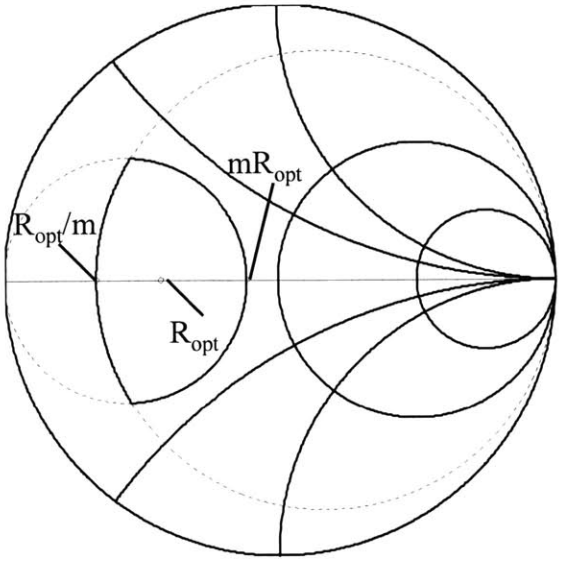

Figure 5-7: Power Mismatched Resistive Terminations

Similarly, for the load mR_{opt}, when the voltage reaches its limit $V_{\max}$, the current is $\frac{I_{\max}}{m}$. Shunt susceptance $\pm jB$ can be added to this load conductance to extend this load point to another arc segment of constant power.

$$Y = \frac{1}{mR_{opt}} \pm jB \tag{5-14}$$

The current reaches its maximum $I_{\max}$ when $|Y|_M = \frac{1}{R_{opt}}$.

Solving for B_M, we write

$$\left|\frac{1}{mR_{opt}} \pm jB_M\right| = \frac{1}{R_{opt}} \tag{5-15}$$

or

$$B_M = \pm \frac{1}{R_{opt}} \sqrt{1 - \frac{1}{m^2}} \tag{5-16}$$

The two arc segments define a constant $\frac{P_{opt}}{m}$ power contour. It is simple to show that the contour is indeed closed, that is $X_M = \frac{1}{Y_M}$.

Start with Y_M, we write

$$\frac{1}{Y_M} = \frac{1}{\frac{1}{mR_{opt}} \pm jB_M} = \frac{\frac{1}{mR_{opt}} \mp jB_M}{\left(\frac{1}{R_{opt}}\right)^2} = \frac{R_{opt}}{m} \mp jR_{opt}\sqrt{1 - \frac{1}{m^2}} \tag{5-17}$$

Substitute equation (5-13) into the above equation,

$$\frac{1}{Y_M} = \frac{R_{opt}}{m} \pm jX_M = Z_M \tag{5-18}$$

Figure 5-8 shows a family of these power contours with mismatched circles superimposed on the Smith chart. We can see that power contours set tighter targeting areas as expected.

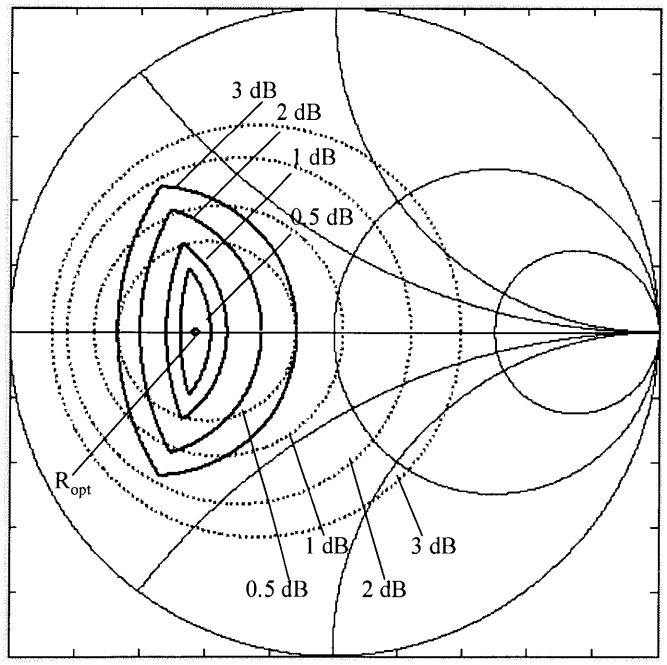

Figure 5-8: Mismatched Circles vs. Power Contours

This graph is a replica of the power contour graph by Steve Cripps [9]

5.1.3.2 Low-pass Matching Sections

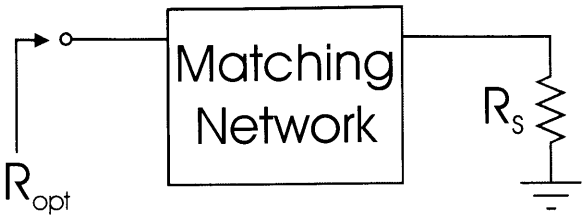

Figure 5-9: Impedance Matching

Figure 5-9 shows a typical impedance matching design for power amplifiers. The matching circuit transforms the antenna impedance R_s (typically 50Ω) to a different impedance R_{opt}. For RF power transistor, it is usually the case that R_{opt} is resistive and smaller than R_s. For such matching problems, a very simple and popular design is a low-pass L-C section as shown in Figure 5-10.

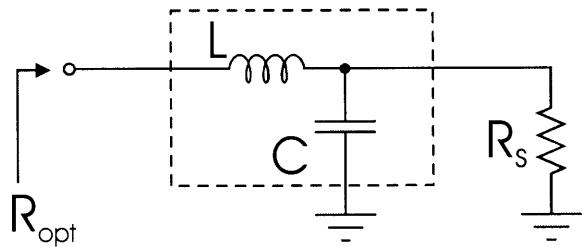

Figure 5-10: L-C Matching Section

If the reader is familiar with the Smith chart, this is a simple case of matching a resistive load $R_{opt} < 50\Omega$ to the 50Ω center. A series inductor L can be added to move along the constant resistance circle $R = R_{opt}/50$ to the constant conductance $G = 1$ circle. A parallel capacitor is then added to rotate to the center along the constant conductance $G = 1$ circle as shown in Figure 5-11.

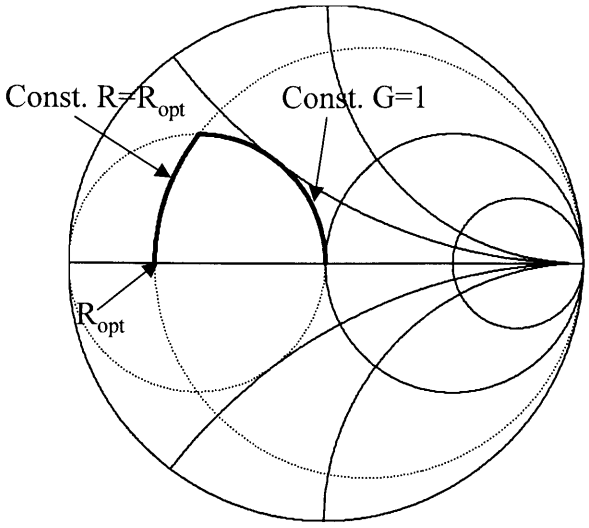

Figure 5-11: L-C Matching Using Smith Chart

Otherwise, using linear circuit techniques, the equivalent impedance Z_{eq} can be written as

$$Z_{eq} = j\omega L + \frac{R_s\left(\frac{1}{j\omega C}\right)}{R_s + \frac{1}{j\omega C}} \tag{5-19}$$

Simplify the right-hand side,

$$Z_{eq} = j\omega L + \frac{R_s\left(1 - j\omega R_s C\right)}{1 + \left(\omega R_s C\right)^2} = \frac{R_s}{1 + \left(\omega R_s C\right)^2} + j\omega\left(L - \frac{R_s^2 C}{1 + \left(\omega R_s C\right)^2}\right) \tag{5-20}$$

Since $Z_{eq} = R_{opt}$, equating the real and imaginary terms gives

$$R_{opt} = \frac{R_s}{1 + \left(\omega R_s C\right)^2} \tag{5-21}$$

and

$$L = \frac{R_s^2 C}{1+(\omega R_s C)^2} \tag{5-22}$$

From the above assumption that $R_{opt} < R_s$, solve for C in equation (5-21)

$$C = \frac{1}{\omega}\sqrt{\frac{1}{R_s R_{opt}} - \frac{1}{R_s^2}} \tag{5-23}$$

Then we can rewrite equation (5-22) in terms of R_{opt},

$$L = R_{opt} R_s C \tag{5-24}$$

Theoretically, an L-C section can transform the resistive load R_s to any optimal resistive load $R_{opt} < R_s$. However, the larger the transformation ratio $m = R_s / R_{opt}$, the narrower the bandwidth of the matching circuit. Figure 5-12 shows the frequency response curves of a single L-C section for five different values of the transformation ratio m. Usually a good rule of thump is to keep the ratio of each section less than 10 by adding more sections if necessary.

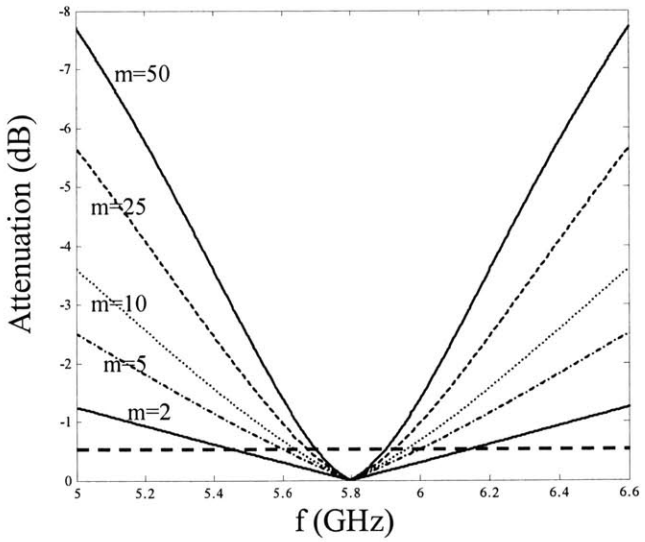

Figure 5-12: Frequency Response of an L-C Matching Section for Different m Ratios

Moreover, for a multiple-section network, the transformation ratio of each section should be the same to maximize the overall bandwidth. For example, let's look at a two-section network for an R_s to R_{opt} transformation via an intermediary R_{int}. For both transformation ratios to be the same,

$$\frac{R_s}{R_{int}} = \frac{R_{int}}{R_{opt}} \tag{5-25}$$

Or

$$R_{int} = \sqrt{R_s R_{opt}} \tag{5-26}$$

For practical designs, the matching network frequency response should fit in a "target area" on the Smith chart. In simulation, this target area can be determined by the power match contour for a specific performance as shown in Figure 5-8. In practice, a load-pull setup provides the same contours for the power amplifier in measurement.

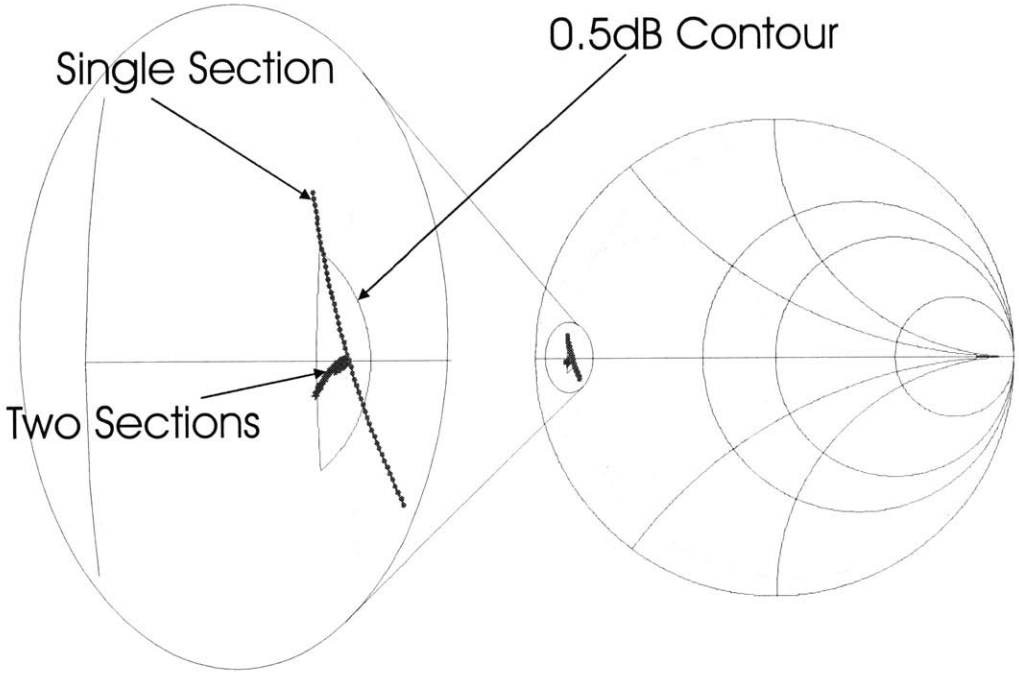

Figure 5-13: Single and Double L-C Matching Sections Bandwidths

Figure 5-13 shows the frequency response for two different matching networks for a 50Ω to 4Ω transformation. One network consists of a single L-C section while the other has two sections. The target area is defined by the 0.5-dB power contour at 5.8GHz center frequency and 150MHz bandwidth. We can see that the one section network frequency response curve does not fit in the target area while the two-section network fits in nicely.

5.1.3.3 Harmonic Shorts

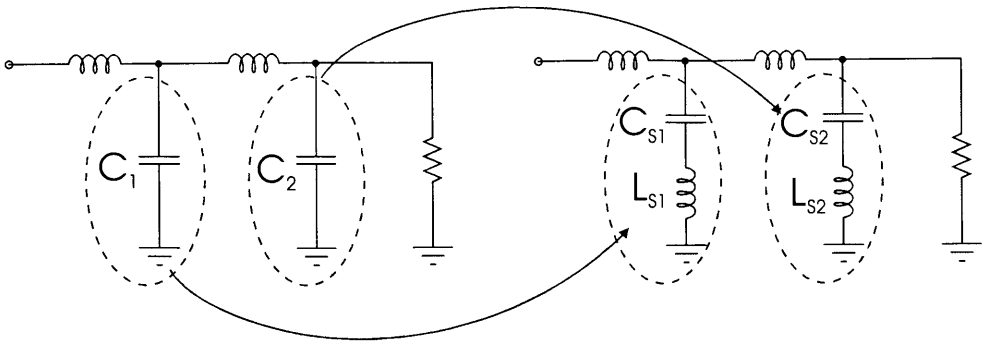

Figure 5-14: Replacing Parallel Capacitors with Equivalent Harmonics Shorts

Harmonic shorts are series L-C circuits that resonate at integer multiples of the frequency of interest. Harmonic shorts can be added to the output matching network to improve the power amplifier linearity performance. Consider a two-section output matching network as shown in Figure 5-14, we can replace capacitor C_1 with a second order harmonic short L_{s1} and C_{s1}. The equivalent impedance of the series L_{s1} and C_{s1} is the same as C_1. In addition, L_{s1} and C_{s1} resonate at $2f_0$. That is

$$j\omega_0 L_{s1} + \frac{1}{j\omega_0 C_{s1}} = \frac{1}{j\omega_0 C_1} \tag{5-27}$$

and

$$L_{s1}C_{s1} = \frac{1}{(2\omega_0)^2} \tag{5-28}$$

Solve for L_{s1} and C_{s1} we have

$$L_{s1} = \frac{1}{3\omega_0^2 C_1} \tag{5-29}$$

and

$$C_{s1} = \frac{3}{4}C_1 \tag{5-30}$$

By adding this second order harmonic short, we can eliminate the second order harmonic component from the output signal. Similarly, C_2 can be replaced with a third order harmonic short L_{s2} and C_{s2} to short out the third order harmonic.

In general, a capacitor C of an L-C matching section can be replace by an n^{th}-order harmonic short L_{sn} and C_{sn}. Then

$$j\omega_0 L_{sn} + \frac{1}{j\omega_0 C_{sn}} = \frac{1}{j\omega_0 C} \tag{5-31}$$

and

$$L_{sn} C_{sn} = \frac{1}{(n\omega_0)^2} \tag{5-32}$$

Solve for L_{sn} and C_{sn} we have

$$L_{sn} = \frac{1}{(n^2 - 1)\omega_0{}^2 C} \tag{5-33}$$

and

$$C_{sn} = \frac{(n^2 - 1)}{n^2} C \tag{5-34}$$

5.2 Transistor Size and Biasing Point

From the collector current plot in Figure 5-4, the transistor should be able to handle an average current of I_{dc} and a peak current of $I_{\max}$. To minimize transistor parasitic as well as die area, we should choose the smallest transistor that can handle the aforementioned currents. A good way to do this is using the familiar f_T versus current density plot as shown in Figure 5-15. These plots are readily available in the "Model Guide" handbook of the process technology. For optimal performance, the transistor should be sized such that the maximum operating collector current is about 90 percent of its maximum f_T current value. That is

$$I_{\max} = 90\%\left(I_{f_T \max} * Area\right) \tag{5-35}$$

where $I_{f_T \max}$ is the peak f_T current density of the transistor.

From Figure 5-4 we can relate the maximum output power and $I_{\max}$.

$$P_{out\_\max} = \frac{V_{cc}\left(I_{\max}/2\right)}{2} \tag{5-36}$$

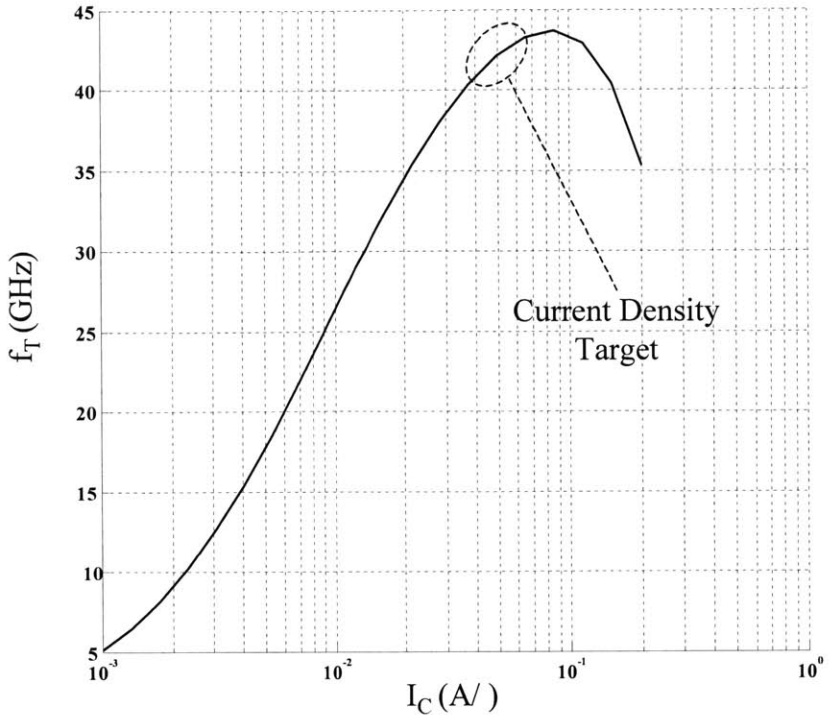

Figure 5-15: BJT f_T Curve

Combine equation (5-35) and (5-36)

$$Area = \frac{1}{90\%}\left(\frac{4P_{out\_\max}}{V_{cc}I_{f_T\max}}\right) \tag{5-37}$$

Once the appropriate transistor size is determined, the next step is to set its bias condition. Biasing techniques are subjects of great research interest and the main focus of this thesis. They are discussed in details in Chapter 4.

5.3 Gain and Multiple Stages

Follow sections 5.1 and 5.2, we can complete the design of the first stage for a power amplifier that satisfies the requirements for output power, and gain variation. The next step is to make sure that we have enough gain. It is fairly easy to calculate the gain G_1 of our first stage, either by hand using the transistor parameters and load conditions, or computer simulations. If our first stage gain is less than specification, we can repeat steps in sections 5.1 and 5.2 to design a second stage. The only differences now are the second stage output power is $P_{\max} - G_1$, and the load is the first stage input impedance instead of the antenna.

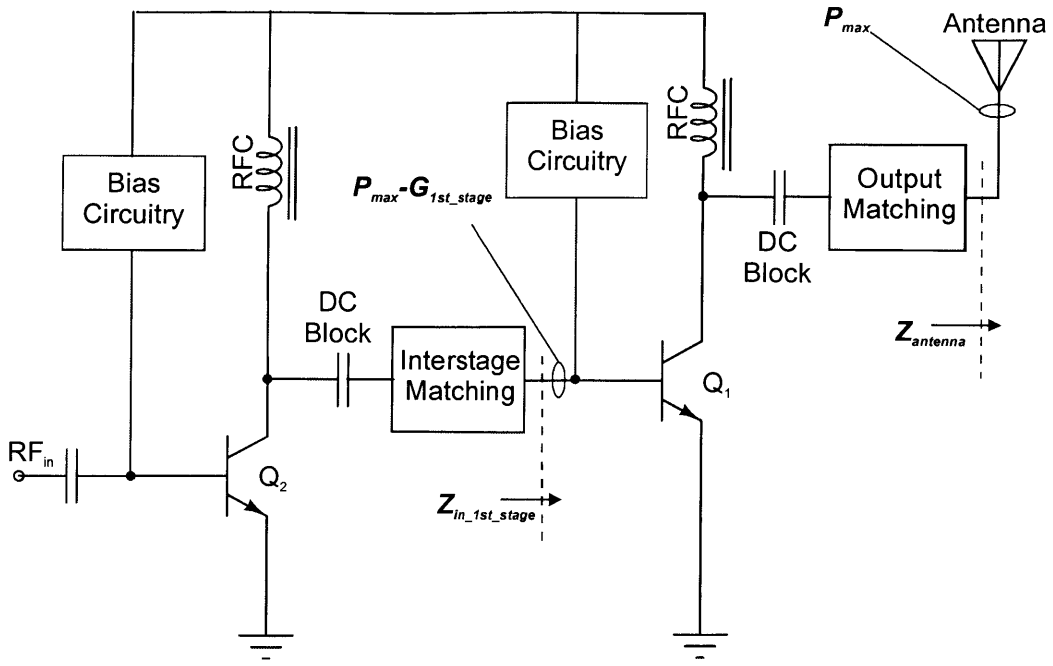

Figure 5-16: Two-Stage Power Amplifier

Using the same methodology, we can keep adding more stages until the overall gain meets the gain requirement. A two-stage power amplifier with each stage's output power and load impedance is shown in Figure 5-16.

There is a general strategy to partitioning gain among multiple stages. Figure 5-17 shows an example of a three-stage amplifier with the dc, input, output power and gain of each stage labeled.

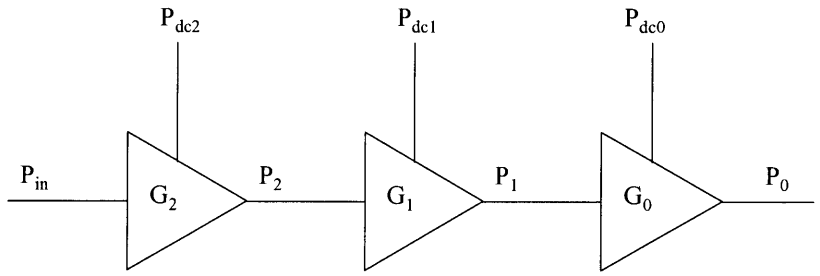

Figure 5-17: Gain Partitioning in Multiple Stages

The combine efficiency can be written as

$$\eta = \frac{P_0}{P_{dc0} + P_{dc1} + P_{dc2}} \tag{5-38}$$

Invert the efficiency and replace the output power as the product of the input power and gains.

$$\frac{1}{\eta} = \frac{P_{dc0}}{P_0} + \frac{P_{dc1}}{G_0 P_1} + \frac{P_{dc2}}{G_1 G_0 P_2} \tag{5-39}$$

Rewrite the right-hand side in terms of efficiency.

$$\frac{1}{\eta} = \frac{1}{\eta_0} + \frac{1}{G_0 \eta_1} + \frac{1}{G_1 G_0 \eta_2} \tag{5-40}$$

Equation (5-40) shows that the last stage efficiency has the most significant impact on the overall efficiency since each stage efficiency is scaled by the gain product of all the stages behind it. Therefore, the strategy is to sacrifice gain for efficiency in the last stages and make up the gain in the early stages.

6 Power Amplifier Design Example for WiGLAN

6.1 Specification

The specification for the power amplifier is tailored to the adapting modulation scheme of the WiGLAN. The amplifier also has to satisfy the ISM band regulation in terms of maximum output power, and harmonics power levels. The 6HP SiGe BiCMOS is the process of choice because it offers transistors with suitable speeds, and well-established technology files. Table 6-1 gives the specification for the desired power amplifier.

Table 6-1: WiGLAN Power Amplifier Specification

Maximum Output Power	$P_{0\max}$	20	dBm
Power Dynamic Range	ΔP_0	$0 \sim 20$	dBm
Center Frequency	f_0	5.8	GHz
Bandwidth	Δf	150	MHz
Gain	G	≥ 16	dB
Gain Variation	ΔG	≤ 0.5	dB
Second-order Harmonic		≤ -40	dBc
Third-order Harmonic		≤ -50	dBc
Supply Voltage	V_{CC}	1.6	V
SiGe 6HP BiCMOS Process	f_T	~ 48	GHz

6.2 Determine R_{opt}

Equation (5-5) gives the expression for R_{opt}. To guarantee the transistor operates in the forward-active region at its maximum output range, we use 0.4V for V_{ce_sat}. In addition, to compensate

for the loss in the output matching network, we will use $P_{out-\max}$ of 21dBm (126mW) in the calculation for R_{opt}.

$$R_{opt} = \frac{\left(V_{cc} - V_{ce\_sat}\right)^2}{2P_{out\_\max}} = \frac{(1.6-0.4)^2}{2 \cdot 0.126} = 5.72\Omega \tag{6-1}$$

6.3 Output Matching Network

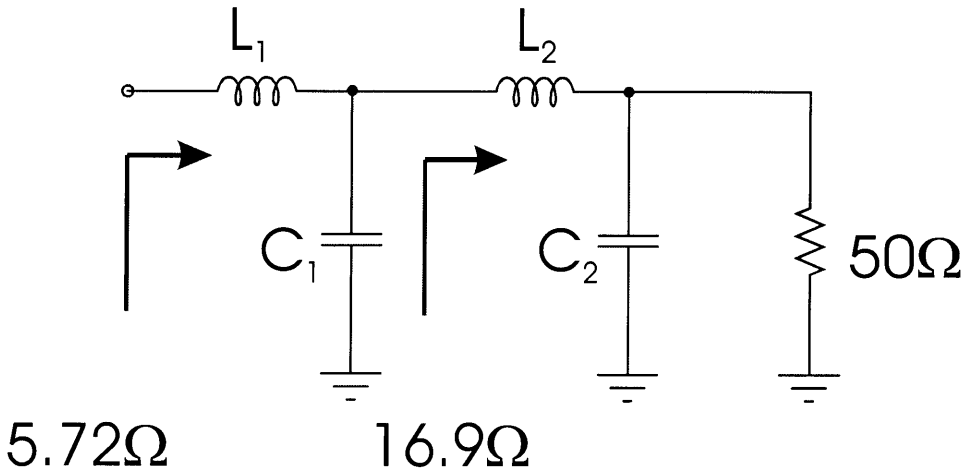

Figure 6-1: 2-Section L-C Low-Pass Matching Network

Given the calculated value for R_{opt}, the output matching network has to transform the antenna load of 50Ω to 5.72Ω. A two low-pass L-C section as shown in Figure 6-1 seems to be a reasonable choice given the wide bandwidth of $150MHz$. From equation (5-26), the intermediate resistance value should be

$$R_{int} = \sqrt{R_s R_{opt}} = \sqrt{50 \cdot 5.72\Omega} = 16.9\Omega \tag{6-2}$$

Using the formulas from equations (5-23) and (5-24) for each section, using operating frequency of $5.8GHz$.

$$C_1 = \frac{1}{\omega}\sqrt{\frac{1}{R_{int}R_{opt}} - \frac{1}{R_{int}^2}} = 2.27pF \tag{6-3}$$

$$L_1 = R_{opt}R_{int}C_1 = 219pH \tag{6-4}$$

$$C_2 = \frac{1}{\omega}\sqrt{\frac{1}{R_{antenna}R_{int}} - \frac{1}{R_{antenna}^2}} = 0.77pF \tag{6-5}$$

$$L_2 = R_{int}R_{antenna}C_2 = 649pH \tag{6-6}$$

The output matching network will be implemented on a printed circuit board to avoid lossy on-chip inductors. The power amplifier will be fabricated on chip, and then packaged before mounted on the printed circuit board for testing. With the packaging approach, there is a series inductor at the transistor collector L_{cw} induced by the bond-wire and package lead. Usually, L_{cw} is in the order of $1nH$ for a single pad with one-millimeter long bond-wire. In addition, we need a capacitor C_{cp} to block the dc current to the load. We can incorporate these two components into our matching network. Assume that the RFC is large enough so that at the operating frequency it is an open circuit. Then, we can design for the series L_{cw} and C_{cp} to be equivalent to L_1 in our L-C matching sections.

$$\omega L_1 = \omega L_{cw} - \frac{1}{\omega C_{cp}} \tag{6-7}$$

From equation (6-4), we have $L_1 = 219pH$. Also, the estimated value for L_{cw} is $1nH$. Then from (6-7), the coupling capacitor C_{cp} is calculated as

$$C_{cp} = \frac{1}{(L_1 + L_{cw})\omega^2} = 0.62pF \tag{6-8}$$

In addition, we can insert harmonics shorts into the matching network as discussed in section 5.1.3.3. We replace C_1 with an equivalent series 2nd harmonic resonant tank L_{s2} - C_{s2}, and C_2 by the 3rd harmonic resonant tank L_{s3} - C_{s3}. Figure 6-2 shows the matching network from Figure 6-1 with the package inductor, and harmonic shorts modifications.

The expression for L_{s2}, C_{s2}, L_{s3}, and C_{s3} are given in equations (5-33) and (5-34).

$$L_{s2} = \frac{1}{(2^2 - 1)\omega_0^2 C_1} = 110pH \tag{6-9}$$

$$C_{s2} = \frac{(2^2 - 1)}{2^2}C_1 = 1.7pF \tag{6-10}$$

$$L_{s3} = \frac{1}{(3^2 - 1)\omega_0^2 C_2} = 122pH \tag{6-11}$$

$$C_{s3} = \frac{(3^2 - 1)}{3^2} C_2 = 0.68pF \tag{6-12}$$

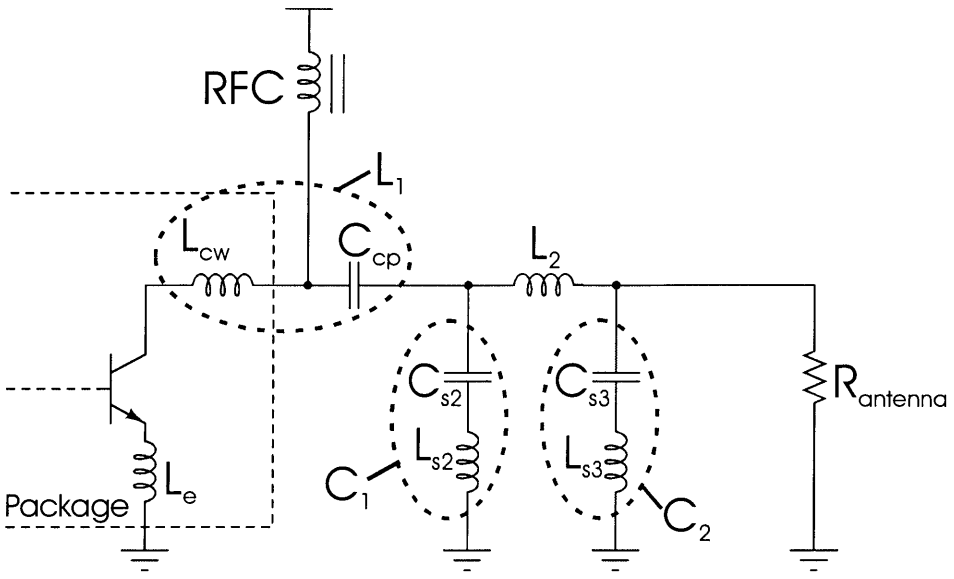

Figure 6-2: Output Matching Network with Packaging Parasitic Inductor

6.4 Output Stage Transistor Size

From equation (5-36), again use 21dBm for $P_{out-\max}$ to compensate for the output matching loss, we can find the maximum current the transistor has to sustain is

$$I_{\max} = \frac{4P_{out\_\max}}{V_{cc}} = \frac{4 \cdot 0.126}{1.6} A = 315mA \tag{6-13}$$

An f_T simulation of a 0.8μm x 48μm double stripes NPN transistor of the SiGe 6HP process gives a maximum f_T of $48GHz$ with an I_c current of $82mA$. Therefore, we need 4 parallel 0.8μm x 48μm double stripes NPN transistors for the output stage.

6.5 Output Stage Gain and Impedance

With the gain requirement of at least 16dB, we will probably need more than one stage. As discussed earlier in section 5.3, we should trade off the gain in the output stage for efficiency and make up the gain in the early stages to improve the overall efficiency. Therefore, we should bias the output stage deep into class-AB. We will set the quiescent collector current to 25% of the class-A current. Class-A collector current is simply half the maximum current calculated above; therefore,

$$I_q = \frac{1}{4} I_{class\_A} = \frac{1}{4} \cdot \frac{I_{\max}}{2} = 40mA \tag{6-14}$$

Now we can look at the small signal circuit model to calculate the gain and input impedance for this stage. Figure 6-3 shows equivalent circuit for the power transistor with inductive emitter degeneration. L_e represents the wire-bond and lead inductors from packaging. We will discuss the size and effects of this inductor in detail shortly.

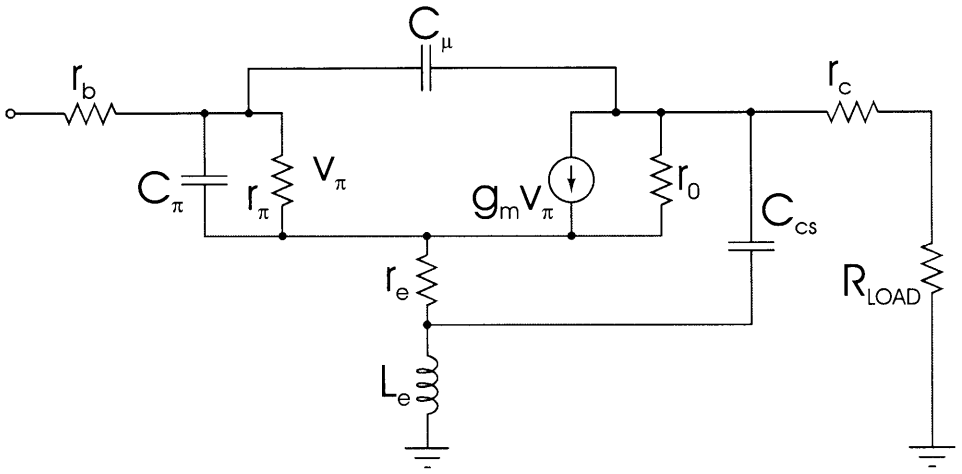

Figure 6-3: Equivalent Small Signal Model with Emitter Wire-Bond Inductor

Table 6-2 lists the model parameters for a 0.8μm x 48μm double stripes NPN from the SiGe 6HP technology. Using this circuit model with the collector quiescent current of $40mA$, we can find the gain and equivalent input impedance of this stage. The calculation is rather involved and tedious. The detail derivation and algebraic result is presented in Appendix B.

Table 6-2: Device Parameter for NPN transistor, SiGe 6HP

0.8μm x 48μm double stripes NPN		
Model Parameters	Value	Unit
β_0	85	-
r_b	2.25	Ω
r_c	3.36	Ω
r_e	0.19	Ω
V_A	70	V
C_π	692.64	fF
C_μ	362.4	fF
C_{cs}	317.44	fF

Figure 6-4 shows a graphical result of the gain and input impedance as a function of the inductance L_e.

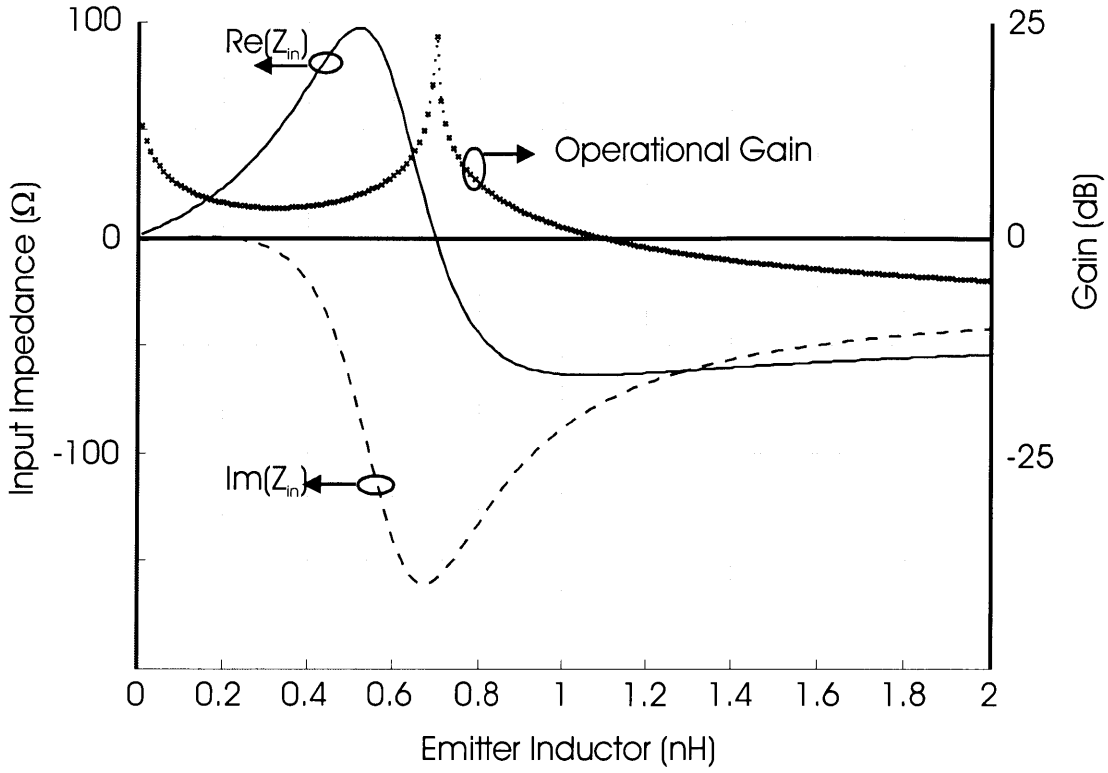

Figure 6-4: Gain and Input Impedance vs. Emitter Degeneration

Start from no emitter degeneration inductor, the input reactance changes little with small inductance, and become capacitive when we keep increasing L_e. The input resistance increases significantly as we first add inductor into the emitter. When L_e is sufficiently large, however, the resistance starts decreasing and becomes negative. This causes by the collector to substrate capacitor C_{cs} acting as a current feedback. When the inductor is large enough, the feedback current raises the emitter voltage above the input voltage, and creates the negative input resistance. This condition is undesirable for two reasons. First, it is unstable. Second, the highly capacitive input impedance makes it difficult to design proper matching.

Therefore, to achieve reasonable and stable gain, the emitter degeneration inductor should be as small as possible. We can control this inductor value by using parallel down-bond wires from multiple emitter contact pads. In this design, we will use ten emitter contact pads for the output stage power transistor. Assuming each bond wire has a $1nH$ inductance, using ten pads gives us an estimated value for L_e of $100pH$. From Figure 6-4, the gain and input impedance of the designing stage are determined.

$$G_0 = 5.91dB \tag{6-15}$$

$$Z_{in} = (9.7597 - j0.1523)\Omega \tag{6-16}$$

6.6 Output Stage Biasing

6.6.1 Fixed Biasing Topologies

Having determined the bias condition, we are now ready to design the biasing circuit. For each biasing technique presented in Chapter 4, all circuit components are derived in terms of the biasing current I_q and impedance Z_{bias}. For this output stage, $I_q = 40mA$. Typically, the impedance Z_{bias} is initially designed to be ten times Z_{in}, which is $(9.7597 - j0.1523)\Omega$ in this case. The final value for Z_{bias} might varies somewhat when the amplifier is tuned for optimal gain, linearity, and efficiency performance. For comparison purpose, each of the three fixed biasing topologies presented in Chapter 4 is designed for the same Z_{bias}.

6.6.2 Adaptive Biasing Topology

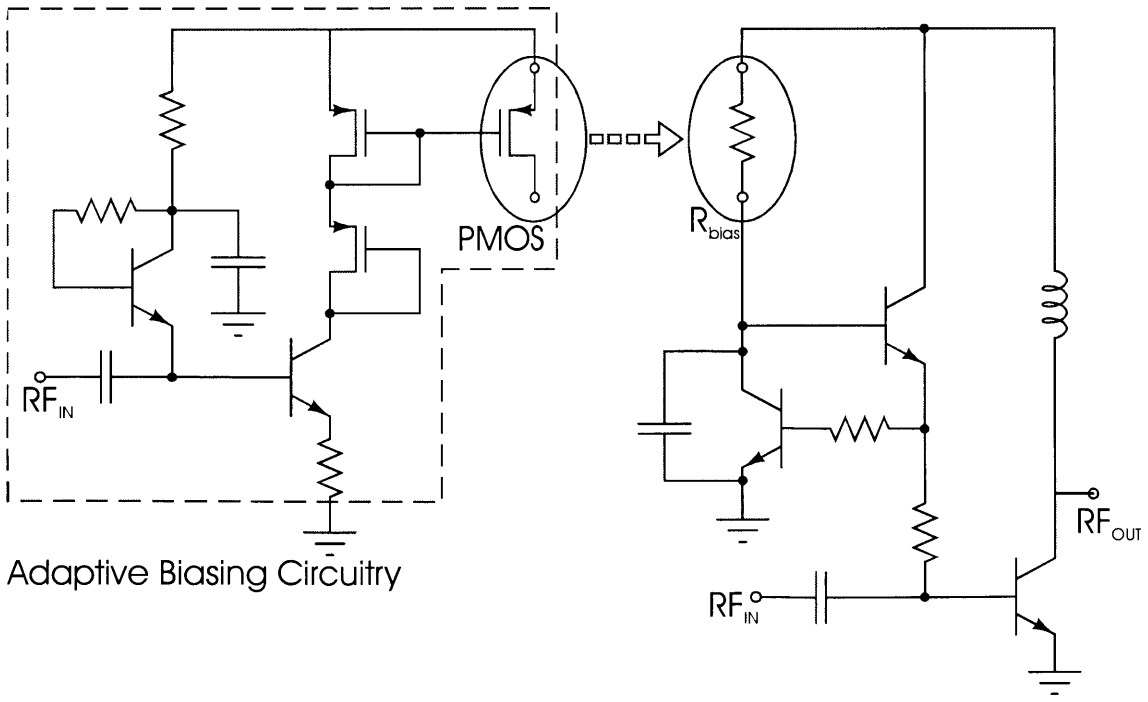

Figure 6-5: Replacing the Conventional Biasing Resistor with the Adaptive-Current PMOS in the Adapting Biasing Scheme

The adaptive biasing version of the power amplifier is improvised from the conventional biasing circuit. Recall that each conventional fixed biasing has a resistor R_{bias} that acts as a current source to set the fixed biasing condition. We can replace this resistor with the current-adapting PMOS transistor from the adaptive biasing circuitry as shown in Figure 6-5.

6.7 Driver Stage

The output stage provides a gain of about 6dB. We need to add a driver stage to meet the total gain requirement of at least 16dB. As discussed in Section 5.3, we can repeat the same set of procedure for the driver stage design. The driver stage should have a maximum output power of 14 dB, while its load is the output stage Z_{in}.

Appendix C shows the full schematics for the complete two-stage power amplifier designs.

7 Simulation Results

7.1 Gain, Efficiency, and Linearity Performance

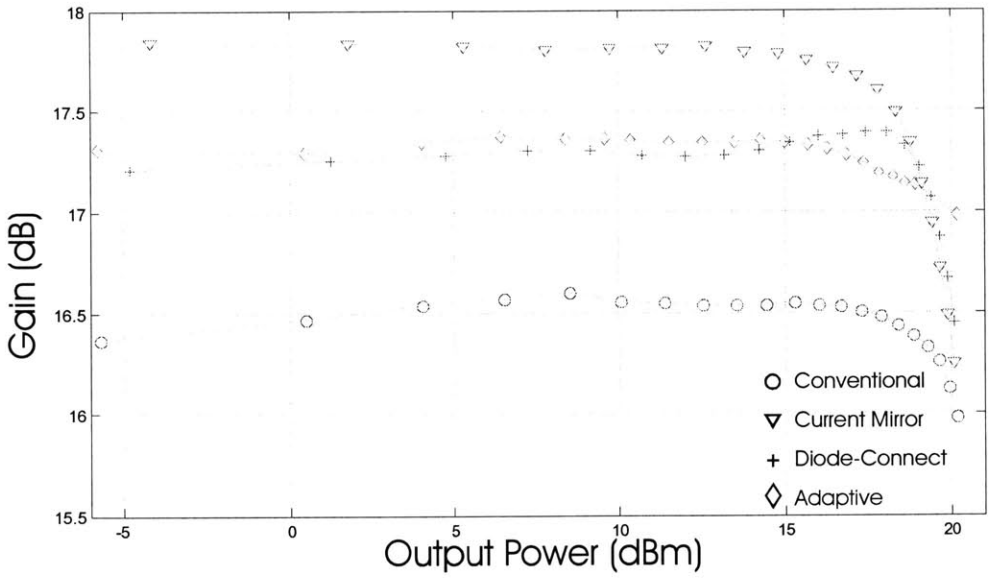

Figure 7-1: Gain vs. Output Power Curves for PAs with Four Different Biasing Topologies

The gain curves of the designed power amplifiers are presented in Figure 7-1. All four biasing topologies provide almost the same gain for a two-stage power amplifier. The diode-connect power amplifier enters saturation later than the other three amplifiers where the gain starts rolling off around 17dBm of output power. A simple explanation for this is the slightly higher voltage headroom in the diode-connect biasing topology, where the current through the inserted base resistor is smaller compared to the other three biasing topologies. The diode-connect base current is related to $\frac{I_{c0}}{\beta^2}$ while the other base currents is related to $\frac{I_{c0}}{\beta}$. The smaller current

leads to a smaller voltage drop across the resistor and higher available voltage swing for the input RF signal at the base of the power transistor.

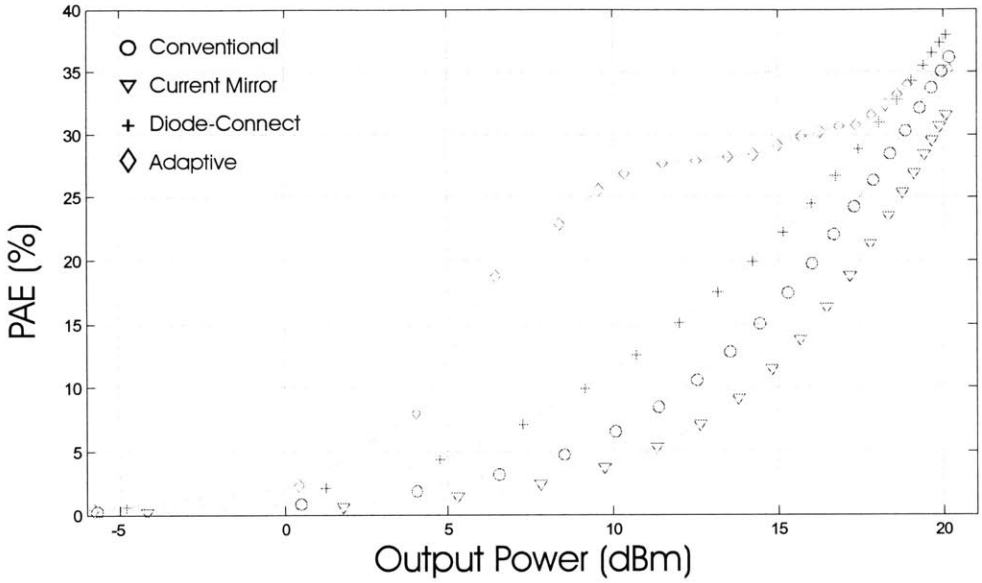

Figure 7-2: Power Added Efficiency Curves vs. Output Power

Figure 7-2 shows the efficiency curves for the four versions of the designed power amplifier. As expected, the adaptive biasing version shows dramatic improvement at low-power operation. The improvement is most noticeable in mid-power range. At very low power levels, the extra power consumed by the biasing circuitry itself is comparable to the output power. Therefore, the efficiency is not upgraded. At very high power levels, where the current already starts clipping (due to class-AB operation), an increase in biasing current does not improve the efficiency.

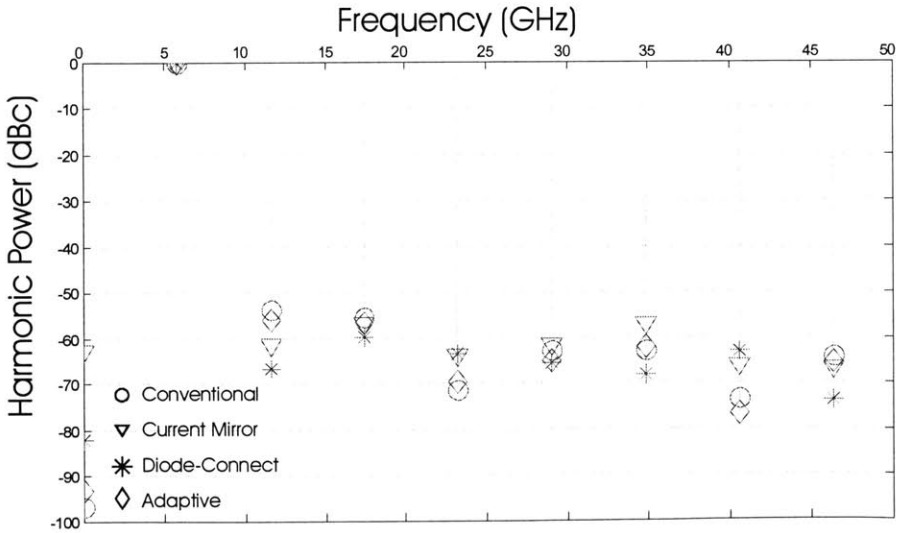

Figure 7-3: Output Spectral Density (normalized to the carrier) at Maximum Output Power

Figure 7-3 shows the output spectral density for the four biasing power amplifier versions. Since they all operate in the same biasing condition, and have the same output matching network, which also performs as a filter, the output spectral density is expected to be similar. With the resonant shorts for 2nd and 3rd order harmonics inserted in the output matching, the corresponding harmonics are drastically attenuated.

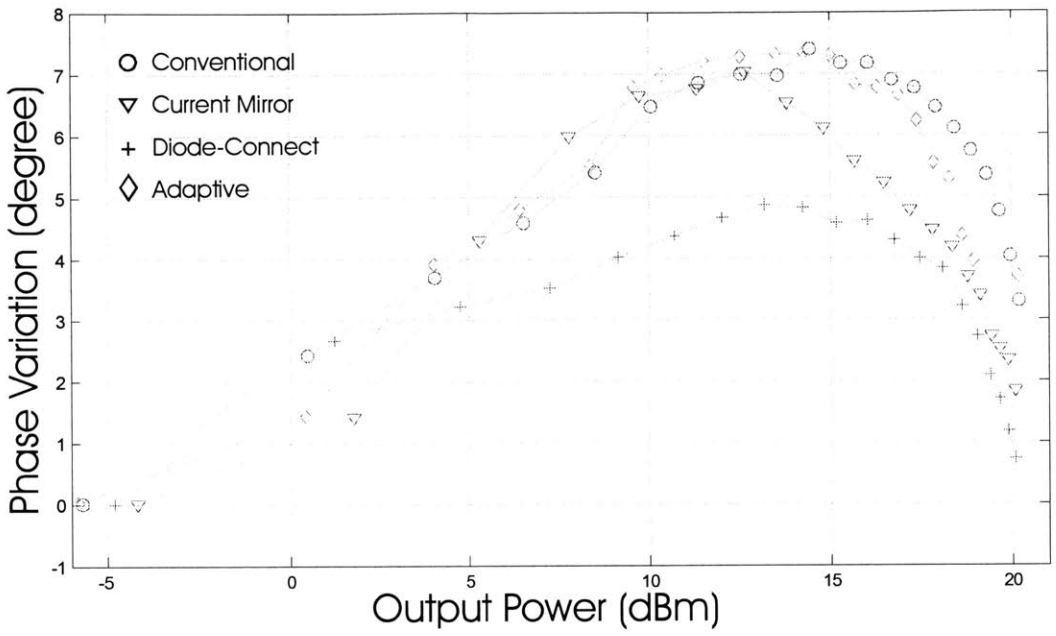

Figure 7-4: Phase Variation across the Output Power Range

Finally, Figure 7-4 shows the phase variation across the output power range. The variation represents the added phase noise due to the power amplifier. How much of this variation is tolerable is beyond the focus of this thesis. For power amplifiers used in commercial cellular phones, a variation of less than 10° is acceptable.

7.2 Layout

The adaptive power amplifier was fabricated using the IBM 6HP SiGe BiCMOS process. The input matching network was incorporated on chip with spiral inductor. The final chip size is 1mm x 1.2mm. There are 26 bond-pads, 7 of which are signal and supply pads. The rest are ground bonds to reduce emitter degeneration inductors.

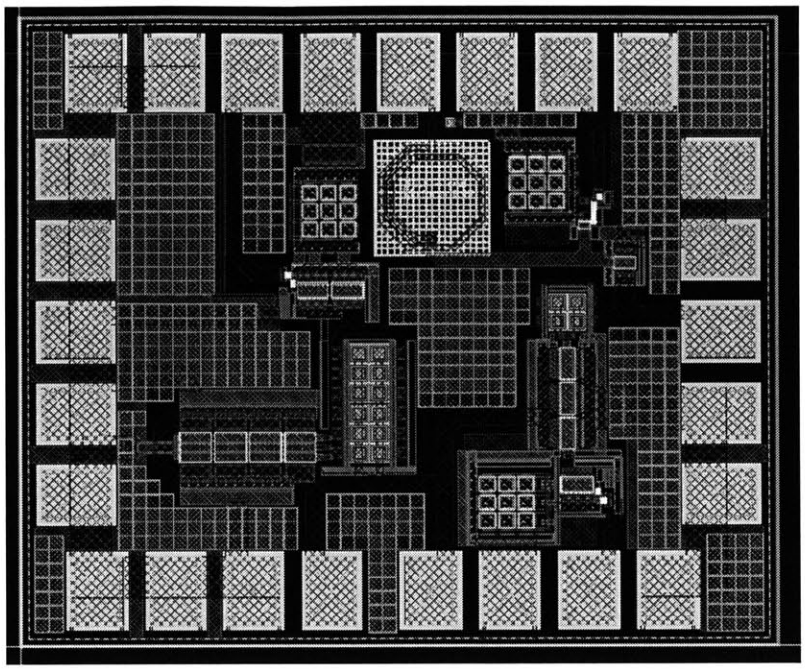

Figure 7-5: Adaptive Biasing Power Amplifier Layout

8 Measurement Procedure and Results

8.1 Die Photo and Packaging

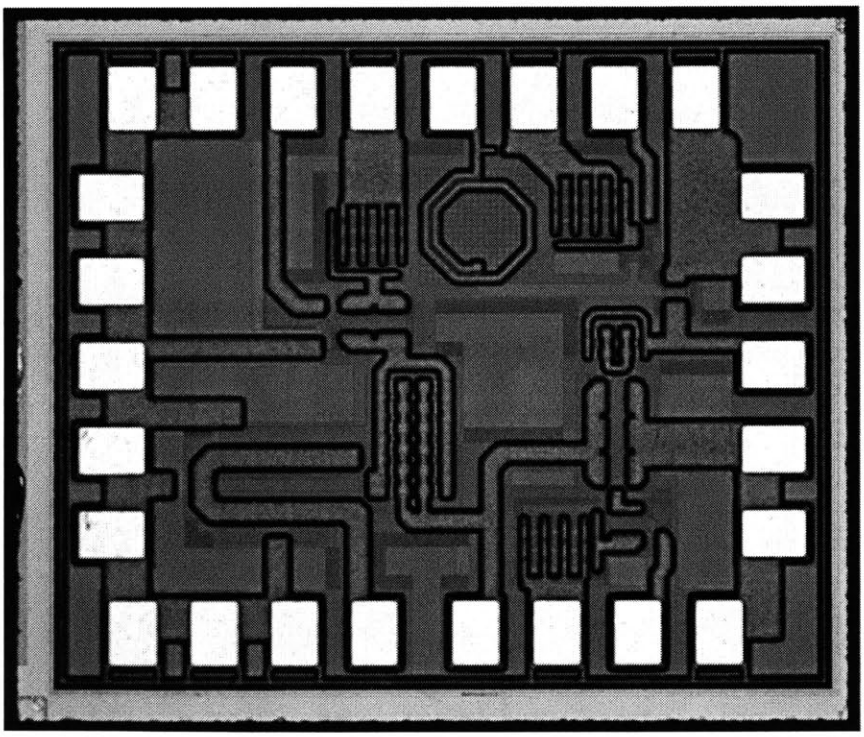

Figure 8-1: Power Amplifier Die Photo

The chip is mounted on a package by MSI (Mini-Systems, Inc). The package is an 8-pin surface mount metal/glass sidewall (model number 5C8M-12) with ground paddle for short ground wire bonds.

8.2 Test Board

The test board is fabricated on the 60 mil thickness GML1000 board material to ensure good RF performance. The GML1000 has a dielectric constant of 3.05, and a loss tangent of 0.005. The board is single layer with bottom ground plane. The output matching network is designed on the PCB using co-planar wave line inductors and surface mount capacitors. There are three ports: RF in, RF out and DC supply, all with SMA connectors.

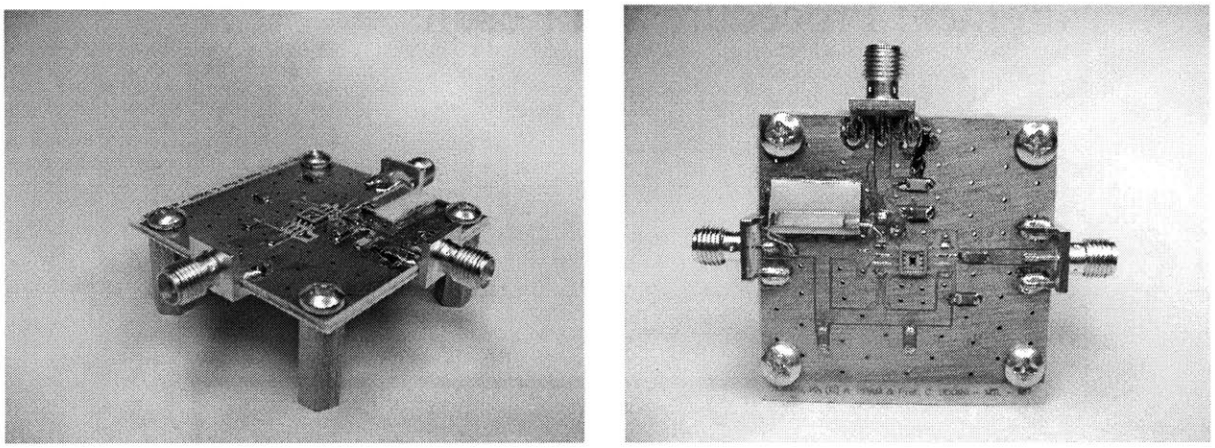

Figure 8-2: Test Board Photos

8.3 Measurement Setup

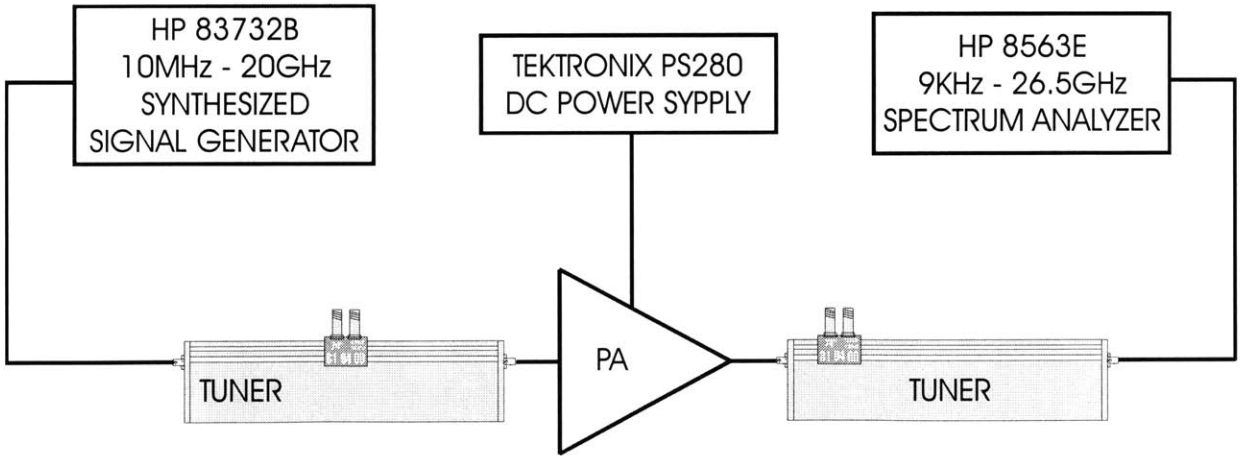

Figure 8-3: Measurement Setup

Figure 8-3 sketches the test setup. The TEKTRONIX PS280, capable of 3 amperes current between 0 and 5 volts, supplies the dc power for the PA. The input is drawn from the HP 83732B Signal Generator, which can generate signals from 10MHz to 20GHz of up to 20dBm. The output is connected to the HP 8563E Spectrum Analyzer. The HP 8563E has the range of 9KHz to 26.5GHz, which allows the measurement of up to the fourth harmonic of the

fundamental carrier of 5.8GHz. The HP 8563E can take up to 1W (30dBm) input power, therefore, there is no need for an attenuator between the power amplifier output and the spectrum analyzer.

8.4 Results

The first assembled test board shows strong oscillation at around 1.8GHz. On the first attempt to stop the oscillation, the output matching network is bypassed. The power amplifier output goes straight to a manual tuner. The tuner setting is adjusted to vary the load presented to the power amplifier. A systematic sweep of the tuner setting fails to provide a stable load for the power amplifier. On the second attempt to stop the oscillation, a R-C feedback is inserted around the output stage. Ideally, we want to put this R-C between the collector and base of the power transistor Q_0. However, Q_0's base is inaccessible. Instead, the R-C feedback is inserted between Q_0 and Q_3 as shown in Figure 8-4.

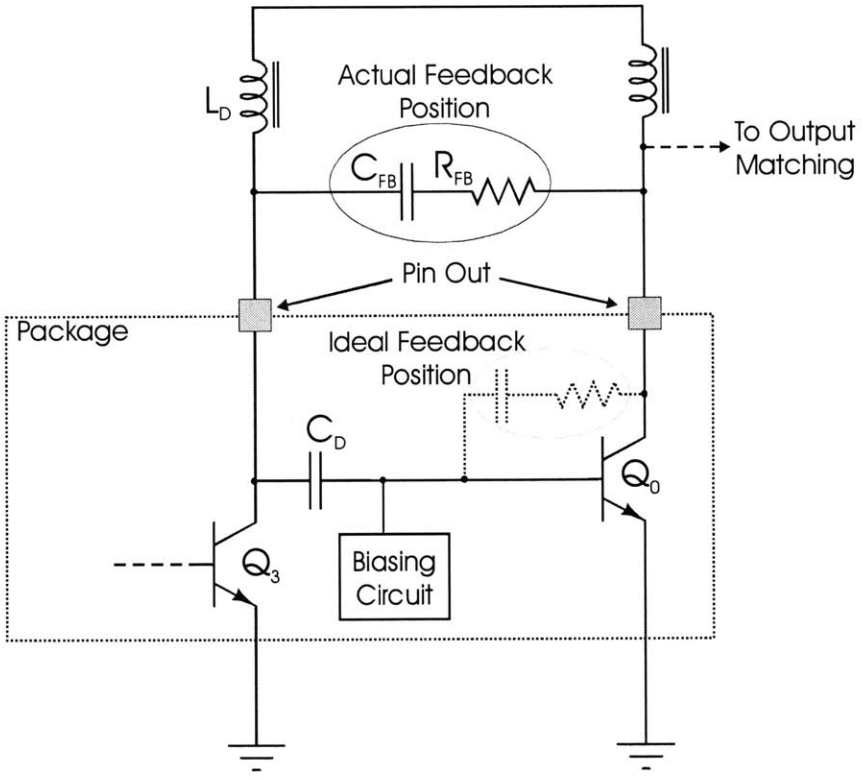

Figure 8-4: Negative Feedback to Reduce Gain and Stop Oscillation

With $R_{FB} = 100\Omega$, and $C_{FB} = 10pF$, the feedback does stop the oscillation. Figure 8-5 shows the measurement results of this setup. Both the gain and efficiency are lower than simulation results. There are two causes for the lower than expected gain. First, the negative R-C feedback reduces the gain to stop oscillation. Second, the feedback network affects both the inter-stage matching L_D - C_D, as well as the output matching network. Therefore, the gain is suffered from these mismatches.

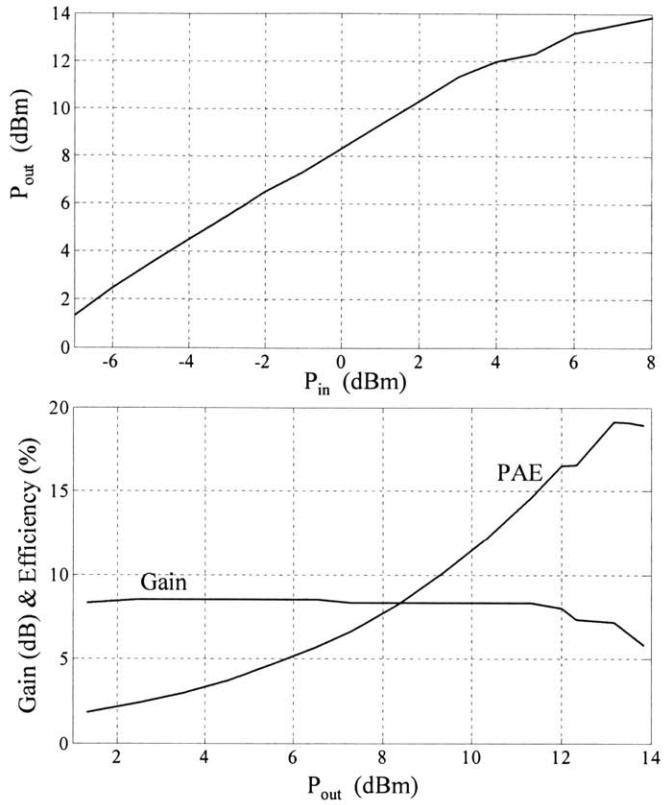

Figure 8-5: Measurement Results for Power Amplifier with R-C Feedback

A second test board is assembled with better care. A piece of copper tape is used as a lid for the chip package. More bypass capacitors are used along the dc power supply line. Package leads are soldered to solder-pads in shorter distances. The efforts are surprisingly rewarding. The power amplifier shows no oscillation across the frequency range. Figure 8-6 shows the measurement results. The efficiency performance is close to the simulation results. However, the gain is about 5dB lower than expected. There are two possible causes for the discrepancies. First, the on-chip input matching network does not provide a good match. A quick S-parameter measurement of the input port confirms this theory. The reflection coefficient S_{11} is in fact flat up to 6GHz. Second, there might be a mismatch at the output matching network as well since it is designed based on the estimated wire-bond and lead inductor values. A complete load-pull measurement is necessary for perfect output and input matches.

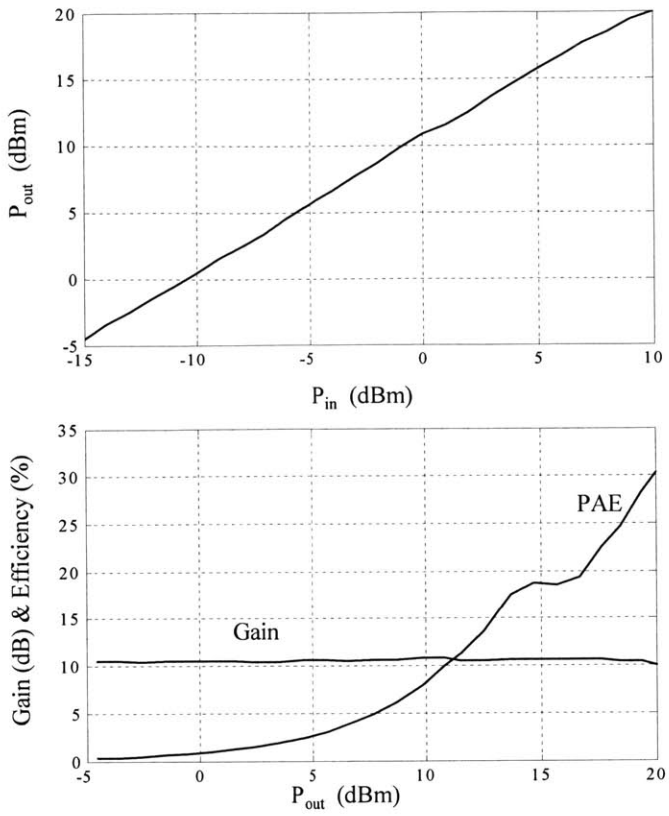

Figure 8-6: Second Assembled PA without Feedback Measurement Results

9 Conclusion

Three fixed biasing techniques have been studied and employed in the design of a 5.8GHz power amplifier. Among the three, the diode-connect biasing topology shows the best overall performance. It shows a higher efficiency across the whole power range than that of the conventional and current mirror biasing. While the overall gain of the three topologies is almost the same, the diode-connect biasing provides a wider linear gain because of its low series base resistance current.

In addition, an adaptive biasing technique is proposed and demonstrated in the fabrication of the designed power amplifier. The biasing circuit senses the RF input voltage, converts it to current, averages then scales it appropriately to provide the biasing currents for the amplifying stages. The result is a significant improvement in the mid-power range efficiency, which is very useful for systems with adaptive power scheme.

There are many future research topics in power amplifiers.

First, there is the fully integrated issue for power amplifiers as discussed in Section 1.3. The two main problems here are the lossy on-chip inductors and the low breakdown voltage as technology scales. Aoki, et al, [10] proposed a distributed active-transformer architecture to overcome these problems. Another way to overcome the lossy inductor and low breakdown voltage problems is to use multiple power amplifiers with a power combiner proposed by Hayashi, et al, [11]. The demonstrated combiner was fabricated on PC board. However, for high frequencies, the dimensions are small enough for on-chip combiner.

Second, the proposed adaptive biasing topology improves efficiency by changing only the current swing. Efficiency could be improved further by the voltage swing as well. To adapt both the voltage and current swing, we need to vary the load. This is possible by using multi-tap transformers.

Appendix A. Harmonics Calculation

Trigonometric identities

$$\cos^2(a)=\frac{1+\cos(2a)}{2}$$

$$\cos^3(a)=\frac{3}{4}\cos(a)+\frac{1}{4}\cos(3a)$$

$$\cos^4(a)=\frac{3}{8}+\frac{1}{2}\cos(2a)+\frac{1}{8}\cos(4a)$$

$$\cos^5(a)=\frac{5}{8}\cos(a)+\frac{5}{16}\cos(3a)+\frac{1}{16}\cos(5a)$$

$$\cos(a)\cos(b)=\frac{1}{2}\cos(a+b)+\frac{1}{2}\cos(a-b)$$

Power amplifier transfer function

$$y(t)=\alpha_1 x(t)+\alpha_2 x^2(t)+\alpha_3 x^3(t)+\alpha_4 x^4(t)+\alpha_5 x^5(t)$$

Single tone input

$$x(t)=\cos(\omega t)$$

Power amplifier output in response to a single tone input

$$y(t)=\alpha_1 A\cos(\omega t)+\alpha_2 A^2\cos^2(\omega t)+\alpha_3 A^3\cos^3(\omega t)+\alpha_4 A^4\cos^4(\omega t)+\alpha_5 A^5\cos^5(\omega t)$$

Using trigonometric identities for the nonlinear terms

$$y(t)=\left(\frac{1}{2}\alpha_2 A^2+\frac{3}{8}\alpha_4 A^4\right)+\left(\alpha_1 A+\frac{3}{4}\alpha_3 A^3+\frac{5}{8}\alpha_5 A^5\right)\cos(\omega t)+\left(\frac{1}{2}\alpha_2 A^2+\frac{1}{2}\alpha_4 A^4\right)\cos(2\omega t)$$
$$+\left(\frac{1}{4}\alpha_3 A^3+\frac{5}{16}\alpha_5 A^5\right)\cos(3\omega t)+\frac{1}{8}\alpha_4 A^4\cos(4\omega t)+\frac{1}{16}\alpha_5 A^5\cos(5\omega t)$$

Two-tone input

$$x(t) = A\cos(\omega_1 t) + A\cos(\omega_2 t)$$

Power amplifier output in response to a two-tone input

$$\begin{aligned} y(t) = {} & \alpha_1 A\left[\cos(\omega_1 t) + \cos(\omega_2 t)\right] + \alpha_2 A^2\left[\cos^2(\omega_1 t) + 2\cos(\omega_1 t)\cos(\omega_2 t) + \cos^2(\omega_2 t)\right] \\ & + \alpha_3 A^3\left[\cos^3(\omega_1 t) + 3\cos^2(\omega_1 t)\cos(\omega_2 t) + 3\cos(\omega_1 t)\cos^2(\omega_2 t) + \cos^3(\omega_2 t)\right] \\ & + \alpha_4 A^4\left[\begin{array}{c}\cos^4(\omega_1 t) + 4\cos^3(\omega_1 t)\cos(\omega_2 t) + 6\cos^2(\omega_1 t)\cos^2(\omega_2 t) + \\ +4\cos(\omega_1 t)\cos^3(\omega_2 t) + \cos^4(\omega_2 t)\end{array}\right] \\ & + \alpha_5 A^5\left[\begin{array}{c}\cos^5(\omega_1 t) + 5\cos^4(\omega_1 t)\cos(\omega_2 t) + 10\cos^3(\omega_1 t)\cos^2(\omega_2 t) + \\ +10\cos^2(\omega_1 t)\cos^3(\omega_2 t) + 5\cos(\omega_1 t)\cos^4(\omega_2 t) + \cos^5(\omega_2 t)\end{array}\right] \end{aligned}$$

Using trigonometric identities for the nonlinear terms

$$\begin{aligned} y(t) = {} & \left(\alpha_2 A^2 + \frac{3}{4}\alpha_4 A^4\right) + \left(\alpha_1 A + \frac{3}{4}\alpha_3 A^3 + \frac{5}{8}\alpha_5 A^5\right)\left[\cos(\omega_1 t) + \cos(\omega_2 t)\right] \\ & + \left(\frac{1}{2}\alpha_2 A^2 + \frac{1}{2}\alpha_4 A^4\right)\left[\cos(2\omega_1 t) + \cos(2\omega_2 t)\right] + \left(\frac{1}{4}\alpha_3 A^3 + \frac{5}{16}\alpha_5 A^5\right)\left[\cos(3\omega_1 t) + \cos(3\omega_2 t)\right] \\ & + \frac{1}{8}\alpha_4 A^4\left[\cos(4\omega_1 t) + \cos(4\omega_2 t)\right] + \frac{1}{16}\alpha_5 A^5\left[\cos(5\omega_1 t) + \cos(5\omega_2 t)\right] \\ & + 2\alpha_2 A^2\cos(\omega_1 t)\cos(\omega_2 t) + 3\alpha_3 A^3\left[\frac{1}{2} + \frac{1}{2}\cos(2\omega_1 t)\right]\cos(\omega_2 t) + 3\alpha_3 A^3\cos(\omega_1 t)\left[\frac{1}{2} + \frac{1}{2}\cos(2\omega_2 t)\right] \\ & + 4\alpha_4 A^4\left[\frac{3}{4}\cos(\omega_1 t) + \frac{1}{4}\cos(3\omega_1 t)\right]\cos(\omega_2 t) + 4\alpha_4 A^4\cos(\omega_1 t)\left[\frac{3}{4}\cos(\omega_2 t) + \frac{1}{4}\cos(3\omega_2 t)\right] \\ & + 6\alpha_4 A^4\left[\frac{1}{2} + \frac{1}{2}\cos(2\omega_1 t)\right]\left[\frac{1}{2} + \frac{1}{2}\cos(2\omega_2 t)\right] + 5\alpha_5 A^5\left[\frac{3}{8} + \frac{1}{2}\cos(2\omega_1 t) + \frac{1}{8}\cos(4\omega_1 t)\right]\cos(\omega_2 t) \\ & + 5\alpha_5 A^5\cos(\omega_1 t)\left[\frac{3}{8} + \frac{1}{2}\cos(2\omega_2 t) + \frac{1}{8}\cos(4\omega_2 t)\right] \\ & + 10\alpha_5 A^5\left[\frac{3}{4}\cos(\omega_1 t) + \frac{1}{4}\cos(3\omega_1 t)\right]\left[\frac{1}{2} + \frac{1}{2}\cos(2\omega_2 t)\right] \\ & + 10\alpha_5 A^5\left[\frac{1}{2} + \frac{1}{2}\cos(2\omega_1 t)\right]\left[\frac{3}{4}\cos(\omega_2 t) + \frac{1}{4}\cos(3\omega_2 t)\right] \end{aligned}$$

The output simplifies to

$$
\begin{aligned}
y(t) = & \left(\alpha_2 A^2 + \frac{9}{4}\alpha_4 A^4\right) + \left(\alpha_1 A + \frac{9}{4}\alpha_3 A^3 + \frac{25}{4}\alpha_5 A^5\right)\left[\cos(\omega_1 t) + \cos(\omega_2 t)\right] \\
& + \left(\frac{1}{2}\alpha_2 A^2 + 2\alpha_4 A^4\right)\left[\cos(2\omega_1 t) + \cos(2\omega_2 t)\right] + \left(\frac{1}{4}\alpha_3 A^3 + \frac{25}{16}\alpha_5 A^5\right)\left[\cos(3\omega_1 t) + \cos(3\omega_2 t)\right] \\
& + \frac{1}{8}\alpha_4 A^4\left[\cos(4\omega_1 t) + \cos(4\omega_2 t)\right] + \frac{1}{16}\alpha_5 A^5\left[\cos(5\omega_1 t) + \cos(5\omega_2 t)\right] \\
& + \left(\alpha_2 A^2 + 3\alpha_4 A^4\right)\left[\cos((\omega_1 + \omega_2)t) + \cos((\omega_1 - \omega_2)t)\right] \\
& + \left(\frac{3}{4}\alpha_3 A^3 + \frac{25}{8}\alpha_5 A^5\right)\left[\cos((2\omega_1 + \omega_2)t) + \cos((2\omega_1 - \omega_2)t) + \cos((2\omega_2 + \omega_1)t) + \cos((2\omega_2 - \omega_1)t)\right] \\
& + \frac{1}{2}\alpha_4 A^4\left[\cos((3\omega_1 + \omega_2)t) + \cos((3\omega_1 - \omega_2)t) + \cos((3\omega_2 + \omega_1)t) + \cos((3\omega_2 - \omega_1)t)\right] \\
& + \frac{3}{4}\alpha_4 A^4\left[\cos((2\omega_1 + 2\omega_2)t) + \cos((2\omega_1 - 2\omega_2)t)\right] \\
& + \frac{5}{16}\alpha_5 A^5\left[\cos((4\omega_1 + \omega_2)t) + \cos((4\omega_1 - \omega_2)t) + \cos((4\omega_2 + \omega_1)t) + \cos((4\omega_2 - \omega_1)t)\right] \\
& + \frac{5}{8}\alpha_5 A^5\left[\cos((3\omega_1 + 2\omega_2)t) + \cos((3\omega_1 - 2\omega_2)t) + \cos((2\omega_1 + 3\omega_2)t) + \cos((2\omega_1 - 3\omega_2)t)\right]
\end{aligned}
$$

Appendix B. Gain and Input Impedance Calculation

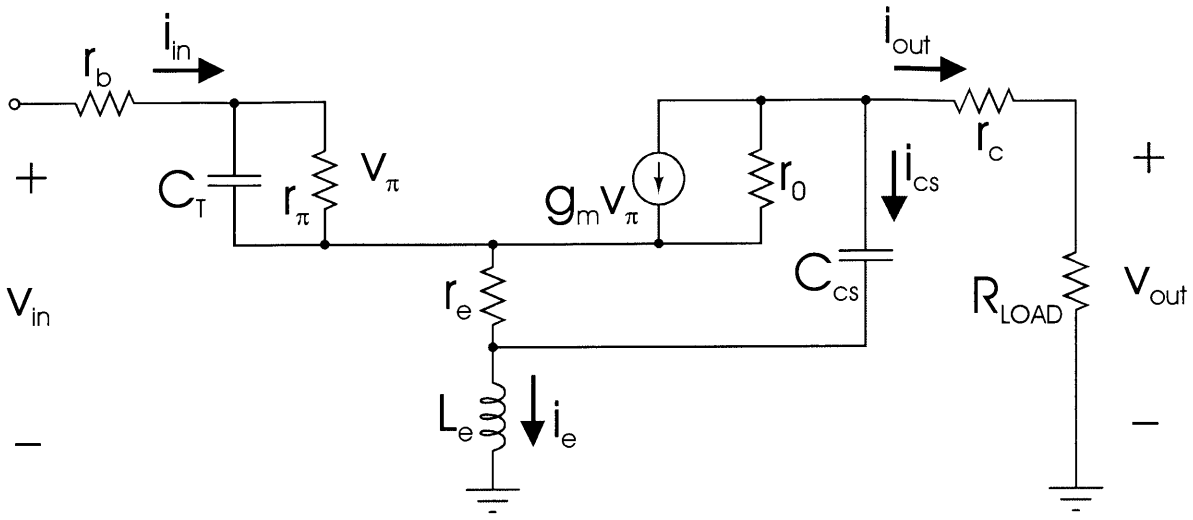

Figure B-1: Small Signal Model for Output Stage Gain and Impedance Calculation

Define impedances as followed:

$$Z_{out} = r_c + R_{LOAD}$$

$$Z_e = j\omega L_e$$

$$Z_\pi = r_\pi \| C_T = \frac{r_\pi}{1 + j\omega C_T r_\pi}$$

$$Z_{cs} = \frac{1}{j\omega C_{cs}}$$

Kirchoff Voltage and Current Laws:

$$i_{in} = i_{out} + i_e$$

$$i_{cs} = \frac{Z_{out} i_{out} - Z_e i_e}{Z_{cs}}$$

$$v_{in} = (r_b + Z_\pi) i_{in} + r_e (i_e - i_{cs}) + Z_e i_e$$

$$\frac{Z_{out}i_{out} - r_e\left(i_e - i_{cs}\right) - Z_e i_e}{r_0} + g_m Z_\pi i_{in} + i_{cs} + i_{out} = 0$$

Solve for i_{out}

$$i_{out} = \frac{v_{in}}{\dfrac{\left(r_b + Z_\pi + r_e\left(\dfrac{Z_{cs}+Z_e}{Z_{cs}}\right) + Z_e\right)\left(\dfrac{Z_{out}+Z_e+r_0}{r_0} + \dfrac{r_e}{r_0}\left(\dfrac{Z_{out}+Z_{cs}+Z_e}{Z_{cs}}\right) + \dfrac{Z_{out}+Z_e}{Z_{cs}}\right)}{\dfrac{Z_e}{r_0} + \dfrac{r_e}{r_0}\left(\dfrac{Z_{cs}+Z_e}{Z_{cs}}\right) - g_m Z_\pi + \dfrac{Z_e}{Z_{cs}}} - r_e\left(\dfrac{Z_{out}+Z_{cs}+Z_e}{Z_{cs}}\right) - Z_e}$$

Therefore, the voltage gain is

$$\frac{v_{out}}{v_{in}} = \frac{R_{LOAD}}{\dfrac{\left(r_b + Z_\pi + r_e\left(\dfrac{Z_{cs}+Z_e}{Z_{cs}}\right) + Z_e\right)\left(\dfrac{Z_{out}+Z_e+r_0}{r_0} + \dfrac{r_e}{r_0}\left(\dfrac{Z_{out}+Z_{cs}+Z_e}{Z_{cs}}\right) + \dfrac{Z_{out}+Z_e}{Z_{cs}}\right)}{\dfrac{Z_e}{r_0} + \dfrac{r_e}{r_0}\left(\dfrac{Z_{cs}+Z_e}{Z_{cs}}\right) - g_m Z_\pi + \dfrac{Z_e}{Z_{cs}}} - r_e\left(\dfrac{Z_{out}+Z_{cs}+Z_e}{Z_{cs}}\right) - Z_e}$$

Appendix C. Schematics

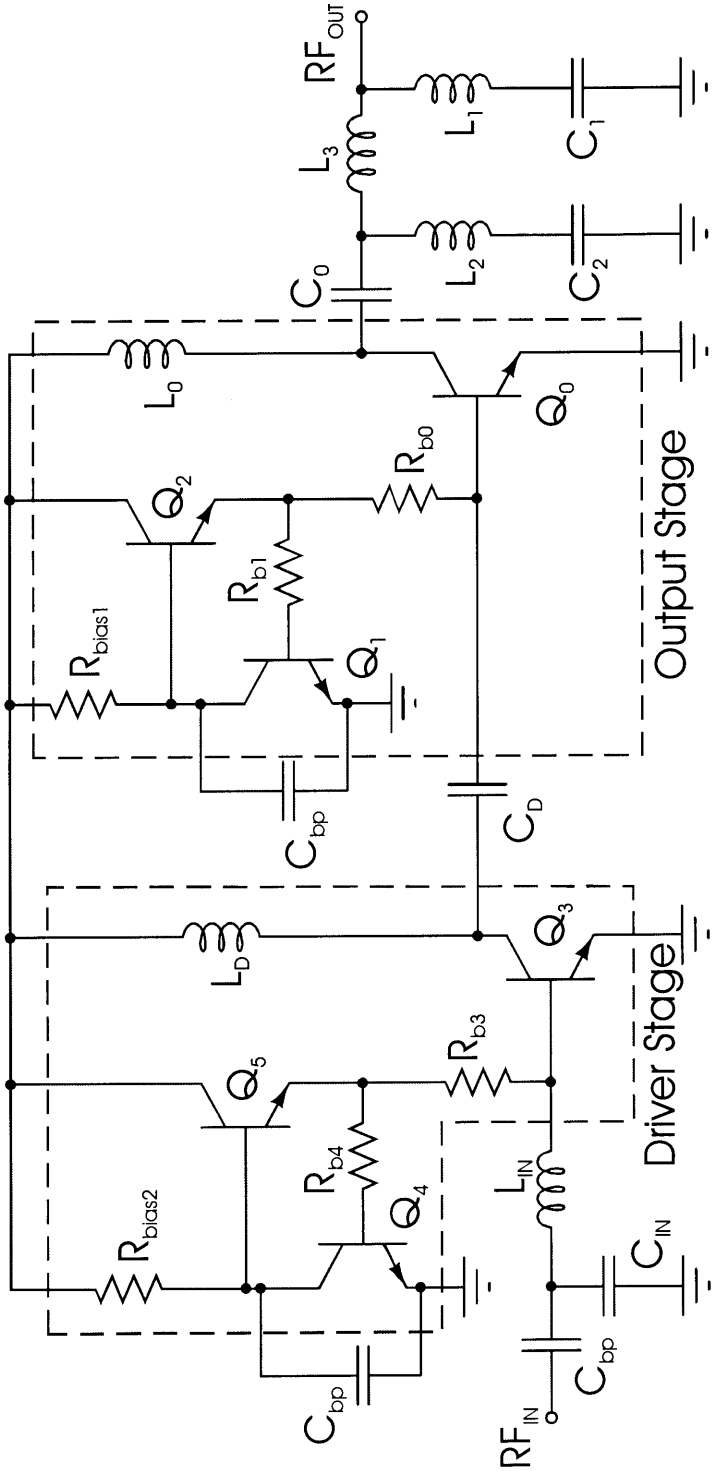

Figure C-1: Schematics for Conventional Biasing Power Amplifier

Table C-1: Component Values – Conventional Biasing Power Amplifier

Component	Value	Description
Q_0	4x (0.8μm x 48μm double stripes)	Output-Stage Power Transistor
Q_1	3x (0.8μm x 4μm double stripes)	Output-Stage Bias Transistor
Q_2	3x (0.8μm x 4μm double stripes)	Output-Stage Bias Transistor
Q_3	1x (0.8μm x 24μm double stripes)	Driver-Stage Power Transistor
Q_4	1x (0.8μm x 2μm double stripes)	Driver-Stage Bias Transistor
Q_5	1x (0.8μm x 2μm double stripes)	Driver-Stage Bias Transistor
L_0	8 nH	Output Matching Inductor
L_1	112 pH	Output Matching Inductor
L_2	110 pH	Output Matching Inductor
L_3	649 pH	Output Matching Inductor
L_D	700 pH	Inter-Stage Matching Inductor
L_{IN}	1.5 nH	Input Matching Inductor
C_0	0.62 pF	Output Matching Capacitor
C_1	0.68 pF	Output Matching Capacitor
C_2	1.7 pF	Output Matching Capacitor
C_D	1.5 pF	Inter-Stage Matching Capacitor
C_{IN}	0.22 pF	Input Matching Capacitor
C_{bp}	10 pF	Bypass Capacitor
R_{bias1}	45 Ω	Output-Stage Bias Resistor
R_{b0}	15 Ω	Q_0's Series Base Resistor
R_{b1}	240 Ω	Q_1's Series Base Resistor
R_{bias2}	40 Ω	Driver-Stage Bias Resistor
R_{b3}	20 Ω	Q_3's Series Base Resistor
R_{b4}	240 Ω	Q_4's Series Base Resistor

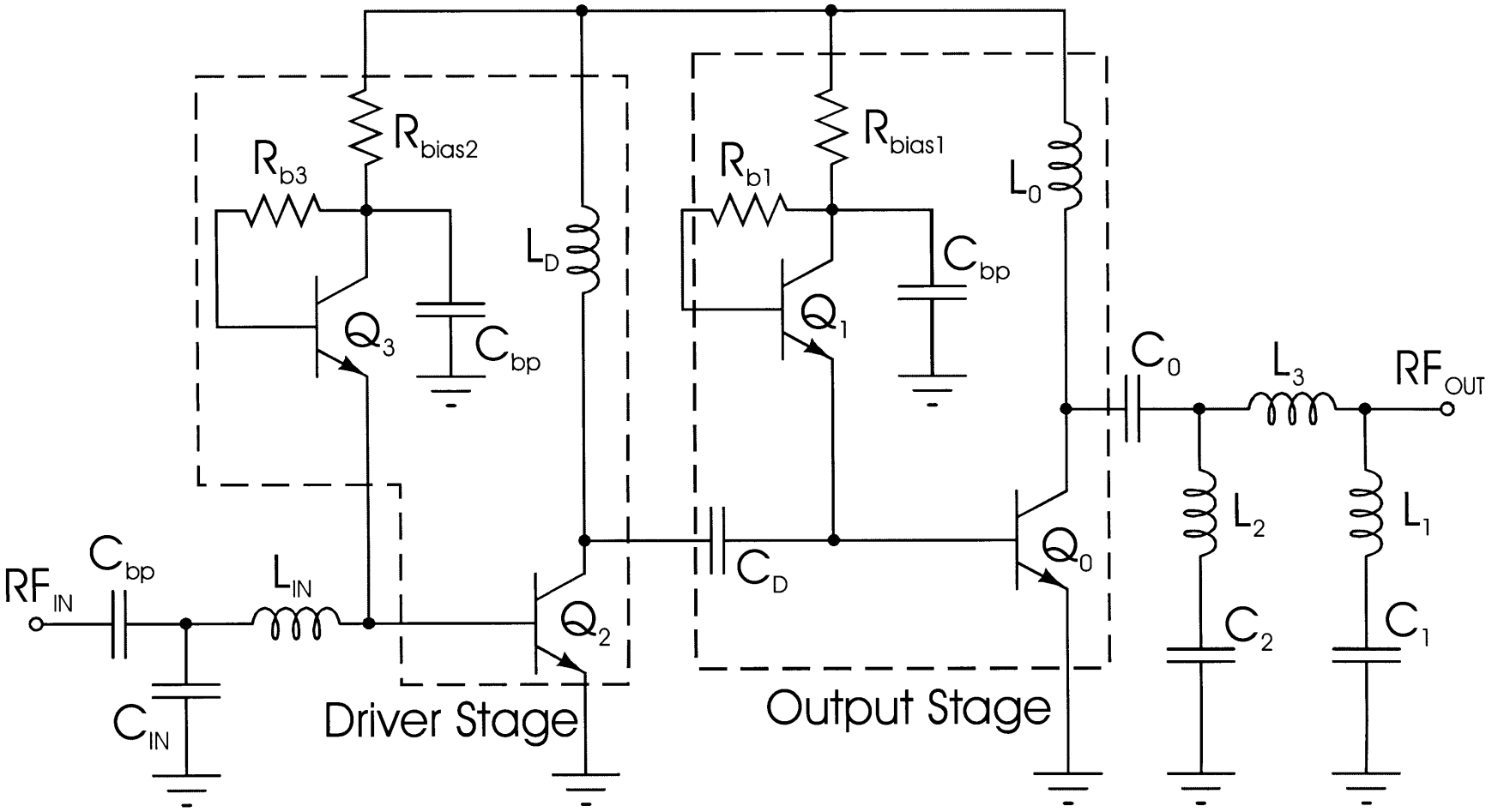

Figure C-2: Schematics for Diode-Connect Biasing Power Amplifier

Table C-2: Component Values – Diode-Connect Biasing Power Amplifier

Component	Value	Description
Q_0	4X (0.8μm x 48μm double stripes)	Output-Stage Power Transistor
Q_1	2X (0.8μm x 24μm double stripes)	Output-Stage Bias Transistor
Q_2	1X (0.8μm x 24μm double stripes)	Driver-Stage Power Transistor
Q_3	1X (0.8μm x 4μm double stripes)	Driver-Stage Power Transistor
L_0	8 nH	Output Matching Inductor
L_1	112 pH	Output Matching Inductor
L_2	110 pH	Output Matching Inductor
L_3	649 pH	Output Matching Inductor
L_D	700 pH	Inter-Stage Matching Inductor
L_{IN}	1.32 nH	Input Matching Inductor
C_0	0.62 pF	Output Matching Capacitor
C_1	0.68 pF	Output Matching Capacitor
C_2	1.7 pF	Output Matching Capacitor
C_D	1.5 pF	Inter-Stage Matching Capacitor
C_{IN}	0.15 pF	Input Matching Capacitor
C_{bp}	10 pF	Bypass Capacitor
R_{bias1}	45 Ω	Output-Stage Bias Resistor
R_{b1}	300 Ω	Q_1's Series Base Resistor
R_{bias2}	40 Ω	Driver-Stage Bias Resistor
R_{b3}	650 Ω	Q_3's Series Base Resistor

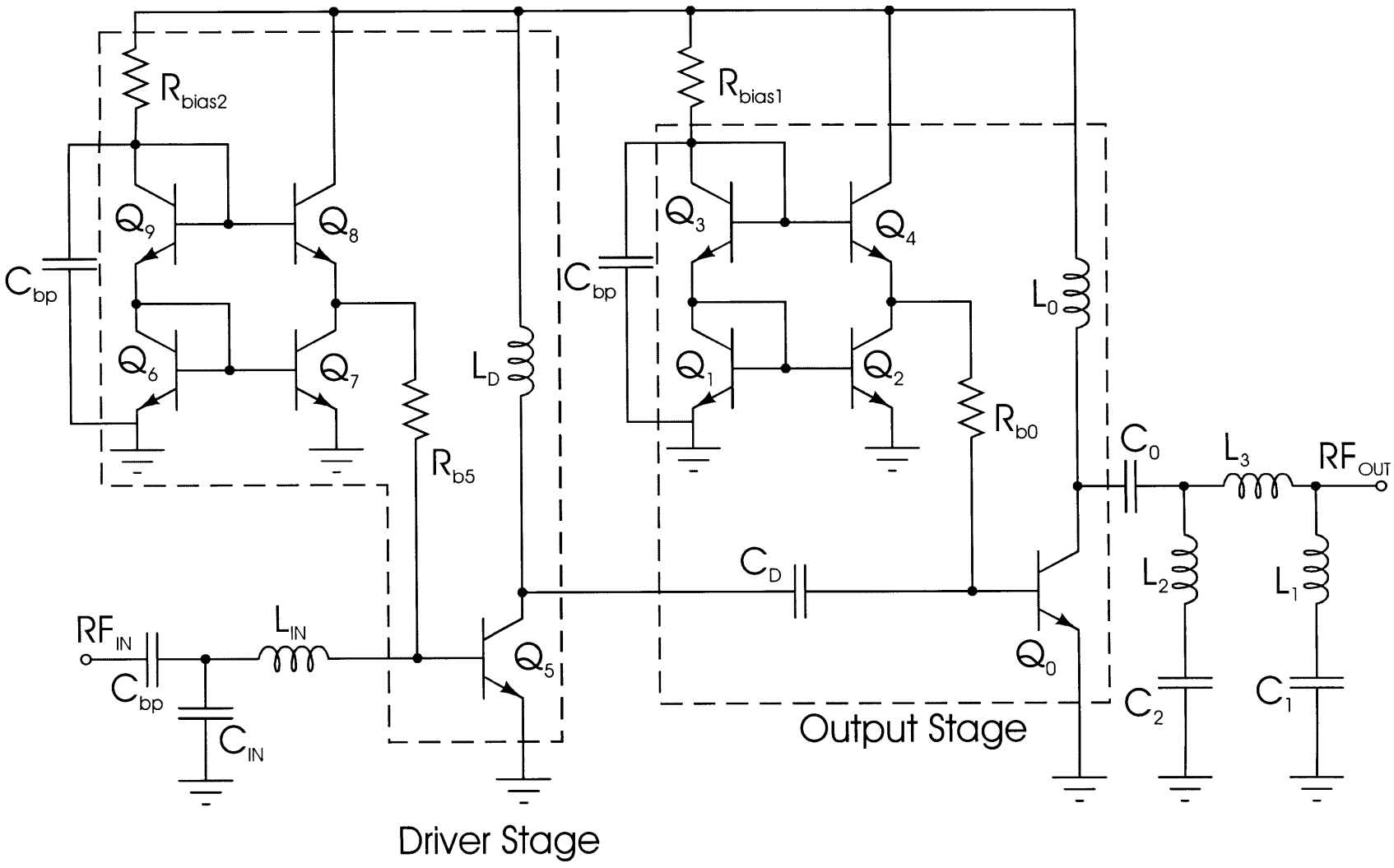

Figure C-3: Schematics for Cascode Current Mirror Biasing Power Amplifier

Table C-3: Component Values – Cascode Current Mirror Biasing Power Amplifier

Component	Value	Description
Q_0	4X (0.8μm x 48μm double stripes)	Output-Stage Power Transistor
Q_1	1X (0.8μm x 24μm double stripes)	Output-Stage Bias Transistor
Q_2	1X (0.8μm x 24μm double stripes)	Output-Stage Bias Transistor
Q_3	1X (0.8μm x 24μm double stripes)	Output-Stage Bias Transistor
Q_4	1X (0.8μm x 24μm double stripes)	Output-Stage Bias Transistor
Q_5	1X (0.8μm x 24μm double stripes)	Driver-Stage Power Transistor
Q_6	1X (0.8μm x 2.5μm double stripes)	Driver-Stage Bias Transistor
Q_7	1X (0.8μm x 2.5μm double stripes)	Driver-Stage Bias Transistor
Q_8	1X (0.8μm x 2.5μm double stripes)	Driver-Stage Bias Transistor
Q_9	1X (0.8μm x 2.5μm double stripes)	Driver-Stage Bias Transistor
L_0	8 nH	Output Matching Inductor
L_1	112 pH	Output Matching Inductor
L_2	110 pH	Output Matching Inductor
L_3	649 pH	Output Matching Inductor
L_D	700 pH	Inter-Stage Matching Inductor
L_{IN}	0.67 nH	Input Matching Inductor
C_0	0.62 pF	Output Matching Capacitor
C_1	0.68 pF	Output Matching Capacitor
C_2	1.7 pF	Output Matching Capacitor
C_D	1.5 pF	Inter-Stage Matching Capacitor
C_{IN}	0.17 pF	Input Matching Capacitor
C_{bp}	10 pF	Bypass Capacitor
R_{bias1}	45 Ω	Output-Stage Bias Resistor
R_{b0}	10 Ω	Q_0's Series Base Resistor
R_{bias2}	55 Ω	Driver-Stage Bias Resistor
R_{b5}	30 Ω	Q_5's Series Base Resistor

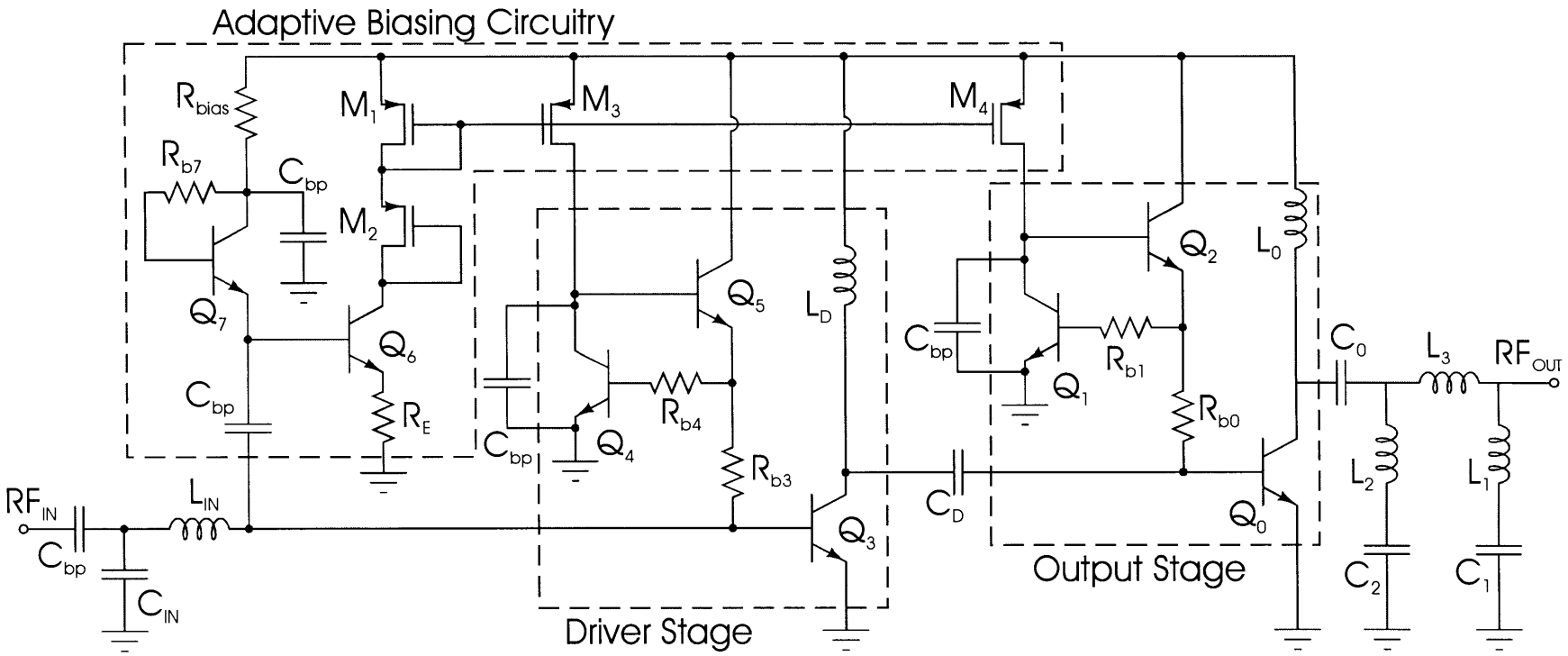

Figure C-4: Schematics for Adaptive Biasing Power Amplifier

Table C-4: Component Values – Adaptive Biasing Power Amplifier

Component	Value	Description
Q_0	4x (0.8μm x 48μm double stripes)	Output-Stage Power Transistor
Q_1	3x (0.8μm x 4μm double stripes)	Output-Stage Bias Transistor
Q_2	3x (0.8μm x 4μm double stripes)	Driver-Stage Power Transistor
Q_3	1x (0.8μm x 24μm double stripes)	Driver-Stage Power Transistor
Q_4	1x (0.8μm x 2μm double stripes)	Driver-Stage Power Transistor
Q_5	1x (0.8μm x 2μm double stripes)	Driver-Stage Power Transistor
Q_6	1X (0.8μm x 12μm double stripes)	Driver-Stage Power Transistor
Q_7	1X (0.8μm x 2μm double stripes)	Driver-Stage Power Transistor
M_1	1X (0.8μm x 1.2μm)	Input Sensor PMOS Load
M_2	1X (0.8μm x 1.2μm)	Input Sensor PMOS Load
M_3	2X (0.8μm x 4.8μm)	Driver-Stage PMOS Current
M_4	10X (0.8μm x 12μm)	Output-Stage PMOS Current
L_0	8 nH	Output Matching Inductor
L_1	112 pH	Output Matching Inductor
L_2	110 pH	Output Matching Inductor
L_3	649 pH	Output Matching Inductor
L_D	700 pH	Inter-Stage Matching Inductor
L_{IN}	1.24 nH	Input Matching Inductor
C_0	0.62 pF	Output Matching Capacitor
C_1	0.68 pF	Output Matching Capacitor
C_2	1.7 pF	Output Matching Capacitor
C_D	1.5 pF	Inter-Stage Matching Capacitor
C_{IN}	0.27 pF	Input Matching Capacitor
C_{bp}	10 pF	Bypass Capacitor
R_{b0}	15 Ω	Q_0's Series Base Resistor
R_{b1}	240 Ω	Q_1's Series Base Resistor
R_{b3}	20 Ω	Q_3's Series Base Resistor
R_{b4}	240 Ω	Q_4's Series Base Resistor
R_{bias}	40 Ω	Adaptive Biasing Resistor
R_{b7}	600 Ω	Q_7's Series Base Resistor
R_E	25 Ω	Adaptive Current Setting Resistor

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