Bandgap Current Source

by

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Abstract

Most analog circuits require reference voltages and currents that do not vary with power supply voltage and temperature. The typical solution to this problem is the 1.2V bandgap voltage reference. However, producing non-integer multiples of this voltage, or a bandgap current reference from this voltage source, requires an operational amplifier. The use of an op-amp leads to increased power consumption and design complexity.

The focus of this research is to develop a simple low-power current reference that is independent of temperature and power supply voltage. We have developed a novel bandgap core circuit that produces a bandgap referenced output current directly without an operational amplifier. The same core circuit can also be used to generate arbitrary non-integer multiples of bandgap voltage.

A prototype 2-terminal bandgap current source has been designed and fabricated emplying only 4 MOS transistors and 2 parasitic PNP transistors in a standard 0.35μm CMOS technology. Although it is clear that the design has not yet been optimized, initial results show temperature and power-supply independence comparable with commercial standards.

Thesis Supervisor: Hae-Sung Lee
Title: Professor of Electrical Engineering

Acknowledgments

Thank you to the family and friends who stood by me, the labmates who put up with my neverending stream of questions, the advisor who was willing to teach me, the brothers who took care of me even when I was sick, and the God whose love they exhibited towards me.

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Chapter 1

Introduction

1.1 Background

A voltage or current source is an essential block of many circuits. For example, in A/D converters this source would be used as a comparative reference. For a given analog input level, an ideal A/D converter will always give the same digital output, independent of external conditions such as temperature and power-supply level. Thus it would make sense to use a source reference that does not depend on these two factors. Many analog circuits also require biasing that does not depend on these factors.

1.2 Typical Solution

Most analog circuit textbooks [1, p.345] cover the design of a bandgap voltage source that is temperature independent and in some implementations, power-supply independent as well. The bandgap source relies on the well-characterized and effectively linear dependencies of base-emitter voltage (negative dependence) and thermal voltage (positive dependence) on temperature. Using resistors to ratio each component's effect on the output voltage, these two temperature dependencies are cancelled, creating a temperature-independent 1.2V supply.

A temperature-independent current reference can be created from the bandgap voltage source, typically using an op-amp. If necessary, this current reference can then be used to create non-integer multiples of the original 1.2V supply.

Figure 1-1 shows a typical bandgap current source design which uses an op-amp and resistor to generate a current source using the bandgap voltage, V_{out}, as a reference. Note that the temperature dependence of resistor R_2 must be taken into account in the resistor ratio x.

This design is not suitable for low-power applications because power is wasted in biasing the op-amp and the three transistor columns used to set up the bandgap voltage. Another problem is that this is a three-terminal device, which adds to design complexity.

1.3 Thesis Motivation

Our goal is to design a simple low-power current source that is independent of temperature and power-supply. To meet the desired goal of simplicity, our design should use as few transistors as possible (and therefore should not require op-amps). We will also pay careful

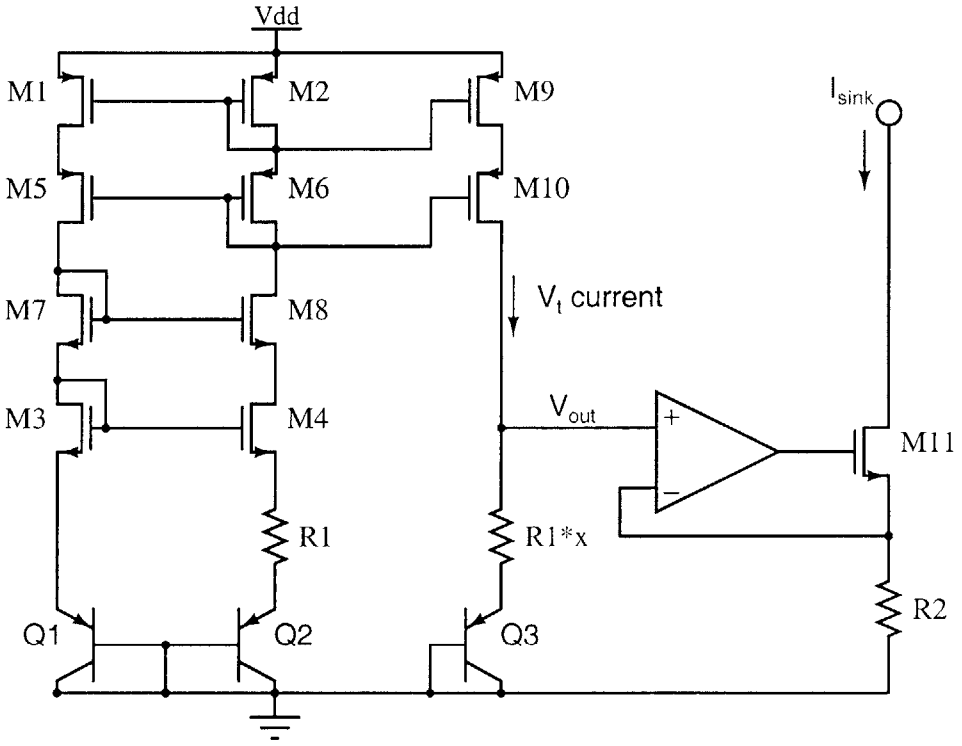

Figure 1-1: Typical bandgap current source [1, Fig. 4.50].

attention to the use of biasing current to minimize power consumption requirements. For simplicity of usage, a two-terminal implementation is being sought.

Chapter 2

Topology

The basic design is shown in Figure 2-1. M_1 and M_2 act as a current mirror. R_2 and R_3 are the same size. The saturation current of Q_2 is larger than that of Q_1 by a factor S. Start-up circuitry is not shown.

Note that this is a two-terminal device that uses no op-amps in the design. Also, no bias current is wasted because all transistors are in the path of I_{sink}.

The gate-source voltages for M_3 and M_4 are equal because they have the same drain current (from the M_1/M_2 current mirror). It is assumed that Early effect can be neglected due to long channel-lengths. Thus, the voltage across both R_2 and R_3 will be equivalent to the base-emitter voltage of Q_1 and so these two resistors will carry the exact same quantity of current.

The current through R_1 is a function of the difference between the base-emitter voltages of Q_1 and Q_2. Thus this current is ΔV_{BE} dependent. In a BJT:

$$V_{BE} = V_T \ln(I_C/I_S)$$

Note that Q_1 and Q_2 have different saturation currents. Let:

$$S = I_{S2}/I_{S1}$$

From the current mirror:

$$I_{C1} + I_{R3} = I_{C2} + I_{R2}$$

But since R_2 and R_3 are equivalent and have the same voltage (V_{BE1}) across them:

$$I_{R2} = I_{R3}$$

And so:

$$I_{C1} = I_{C2}$$

Thus:

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = V_T \ln(\frac{I_{C1} I_{S2}}{I_{C2} I_{S1}}) = V_T \ln S$$

Thus the current that is proportional to ΔV_{BE} is also proportional to thermal voltage, V_T. Since $V_T = kT/q$, the ΔV_{BE} current is also proportional to absolute temperature (PTAT).

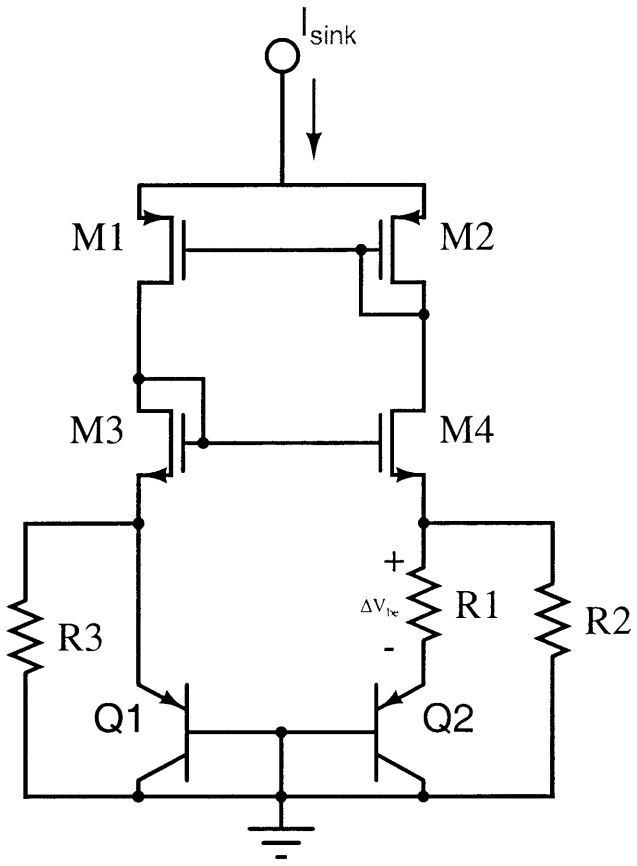

Figure 2-1: Base design for simple low-power bandgap current source.

Let K be the resistor ratio needed to cancel out temperature coefficients.

$$K = \frac{R_2}{R_1}$$

Then the amount of current sunk by this circuit is determined only by the value of the unit resistor R_1:

$$\begin{aligned} I_{sink} &= 2\left(\frac{V_{BE1}}{R_2} + \frac{\Delta V_{BE}}{R_1}\right) \\ &= 2\left(\frac{V_T \ln(I_{C1}/I_{S1})}{KR_1} + \frac{V_T \ln S}{R_1}\right) \\ &= \frac{2V_T}{KR_1} \ln\left(\frac{V_T \ln S}{I_{S1} R_1}\right) + \frac{2V_T}{R_1} \ln S \end{aligned} \tag{2.1}$$

It can be seen that, to a first approximation, none of the parameters depend on V_{DD} and that current can be set by determining R_1 (and therefore R_2) to solve the transcendental equation above for the desired value of current.

2.1 Implementation of Resistor Ratio

Resistor ratio K is set by bypassing sections of resistor R_1 via MOS switches M_5 - M_{12} (Figure 2-2).

2.2 Startup Condition

As is typical for self-biased circuits [1, p.326], this topology has two stable states of operation - the desired state and a zero-current state. The node voltages that make the zero-current state possible are shown in Figure 2-3.

Startup circuitry was not included on-chip to minimize complications from extra components. Because every major node of the circuit was connected to a pin, any necessary startup circuitry could be connected externally.[1]

2.3 Stability

Because self-biasing circuits rely on feedback, care must be taken not to create an unstable loop.

Suppose a positive disturbance is introduced at the gate of M_4. This disturbance increases V_{GS4}, which increases I_{D4}. The increase in I_{D4} is mirrored through M_1/M_2, increasing the gate voltage of diode-connected M_3. However, the gate of M_3 is shorted to the gate of M_4, and so a positive feedback loop is created. For this feedback loop to be stable,

$$\left|\frac{\Delta V_{G3}}{\Delta V_{G4}}\right| < 1$$

[1] It turned out that any small disturbance pushed the circuit out of the zero state and so startup circuitry was not needed for lab testing.

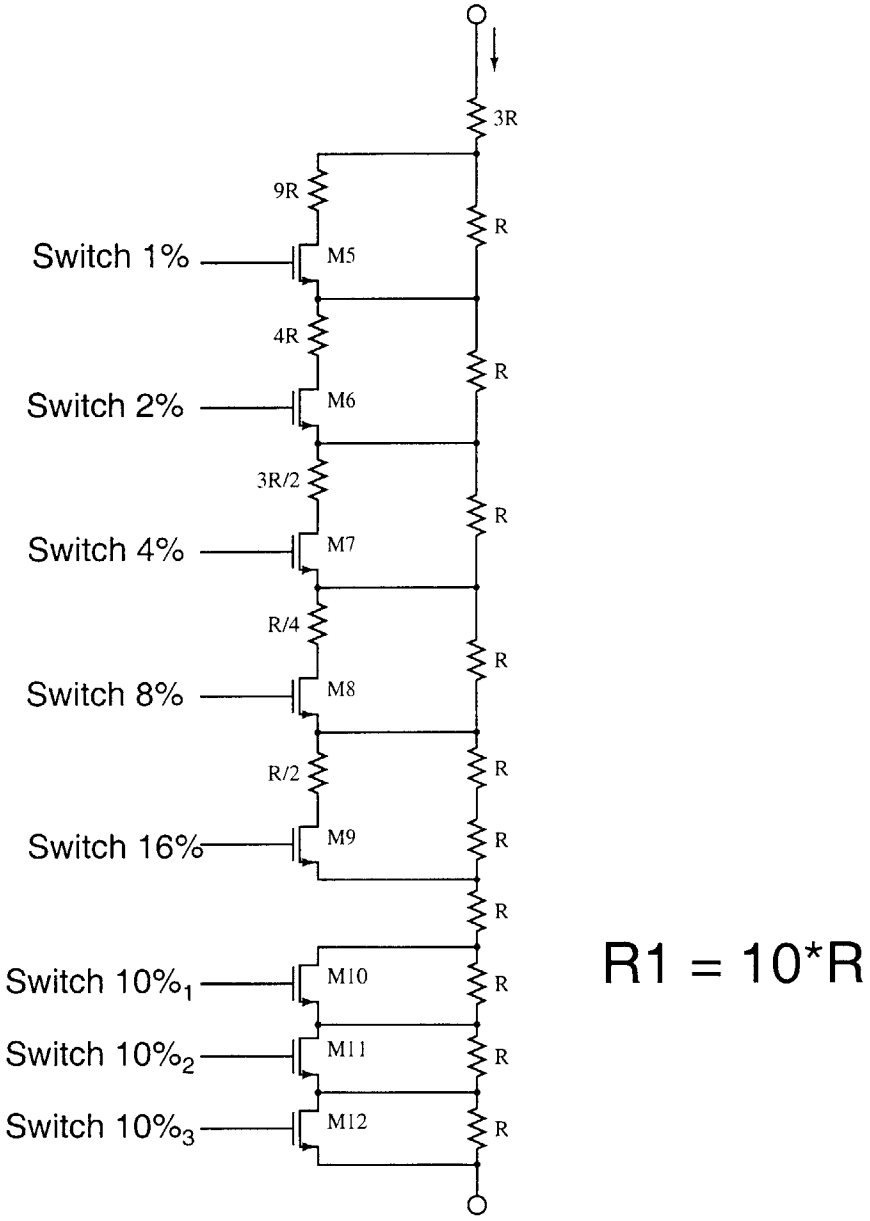

Figure 2-2: Sub-circuitry used to vary R1, and therefore resistor ratio K.

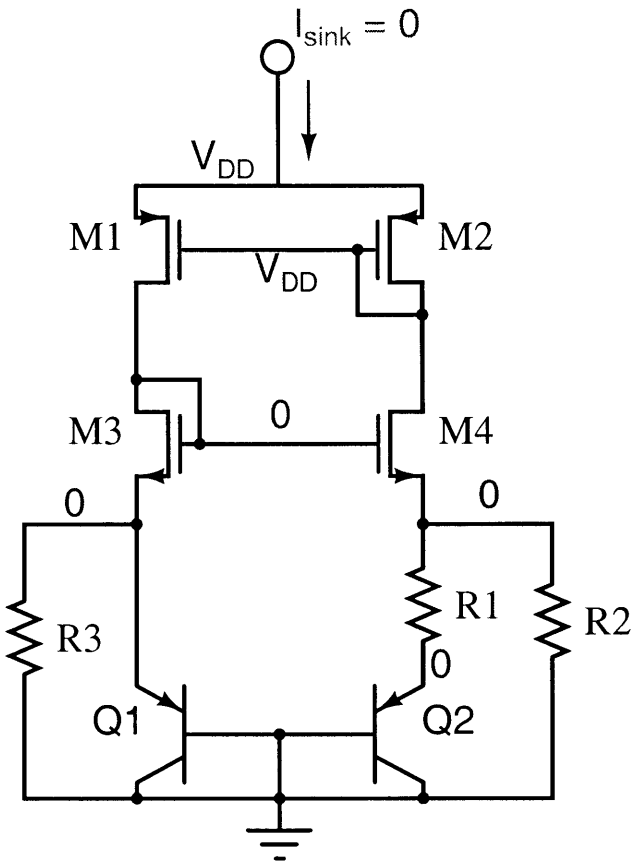

Figure 2-3: Node voltages for zero-current state.

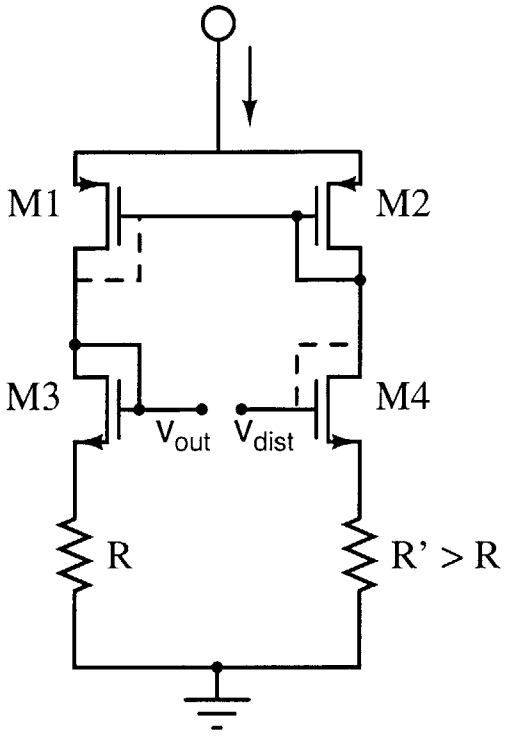

Figure 2-4: Feedback stability analysis. Dotted lines indicate alternate configuration.

Consider the circuit shown in Figure 2-4, which is a modified form of Figure 2-1.

$$g_m = \frac{qI_C}{kT}$$

Because of current mirror M_1/M_2

$$I_{C1} = I_{C_2} \Longrightarrow g_{m1} = g_{m2}$$

Comparing Figure 2-4 with the original Figure 2-1, it is clear that:

$$R = g_m^{-1} || R3$$

$$R' = (g_m^{-1} + R_1) || R_2$$

But

$$R_2 = R_3$$

therefore

$$R' > R$$

Let M_2 and M_4 be diode connected as shown. If a disturbance V_{dist} is applied to the gate of M_4 (effectively a common-source amplifier with source degeneration R')

$$V_{out} = I_{C1}\left(g_m^{-1} + R\right) = V_{dist}\frac{g_m}{1 + g_m R'}\left(g_m^{-1} + R\right)$$

and so we meet our stability condition

$$\left|\frac{\Delta V_{G3}}{\Delta V_{G4}}\right| = \frac{V_{out}}{V_{dist}} = \frac{1 + g_m R}{1 + g_m R'} < 1$$

However, if the circuit is rearranged such that, instead of M_2 and M_3, M_1 and M_4 are diode-connected (see dotted lines in Figure 2-4), then the gain of the positive feedback loop is greater than unity, causing the circuit to be unstable. In practice, such a circuit would most likely latch upon startup.

Chapter 3

Simulation

The circuit was simulated using model file data downloaded from the MOSIS website as part of the TSCM 0.35μm 2-poly process design kit. This data was formatted for the Spectre simulator, and so Spectre was used for simulations. This choice was also appropriate because of Spectre's native support for temperature sweeps.

3.1 Ideal Resistors

Initial simulations were done using ideal resistors (no temperature dependence). Results for a resistor ratio K=25kΩ/4.1kΩ and a BJT saturation current ratio S=20 are shown in Figure 3-1.

As can be seen in the Cadence graphs, the V_T component of I_{sink} increased with temperature, while the V_{BE} component decreased with temperature. The sum of these two components created a 100μA current source which was temperature independent until about 100^{o}C.

A sweep of V_{DD} (Figure 3-2) gave an output impedance of better than 100 kΩ (in other words, an output admittance of less than 10 μS). This output impedance came from the increase of the V_T component of I_{sink} [1]. Also note that turn-on voltage for this circuit was approximately V_{on}=2V.

3.2 Poly2 Resistors

Simulation with modelled Poly2 resistors (TC_F=1070ppm) required a resistor ratio, K, of approximately 25kΩ/2kΩ to create temperature independence. The lower required value of R_1 can be explained as follows: the resistance of poly2 increases with temperature, which, as seen from equation 2.1 would make the TC_F of I_{sink} more negative. To cancel this decrease, we need to have a larger PTAT component of current, and thus R_1 must be decreased appropriately.

[1] Why?

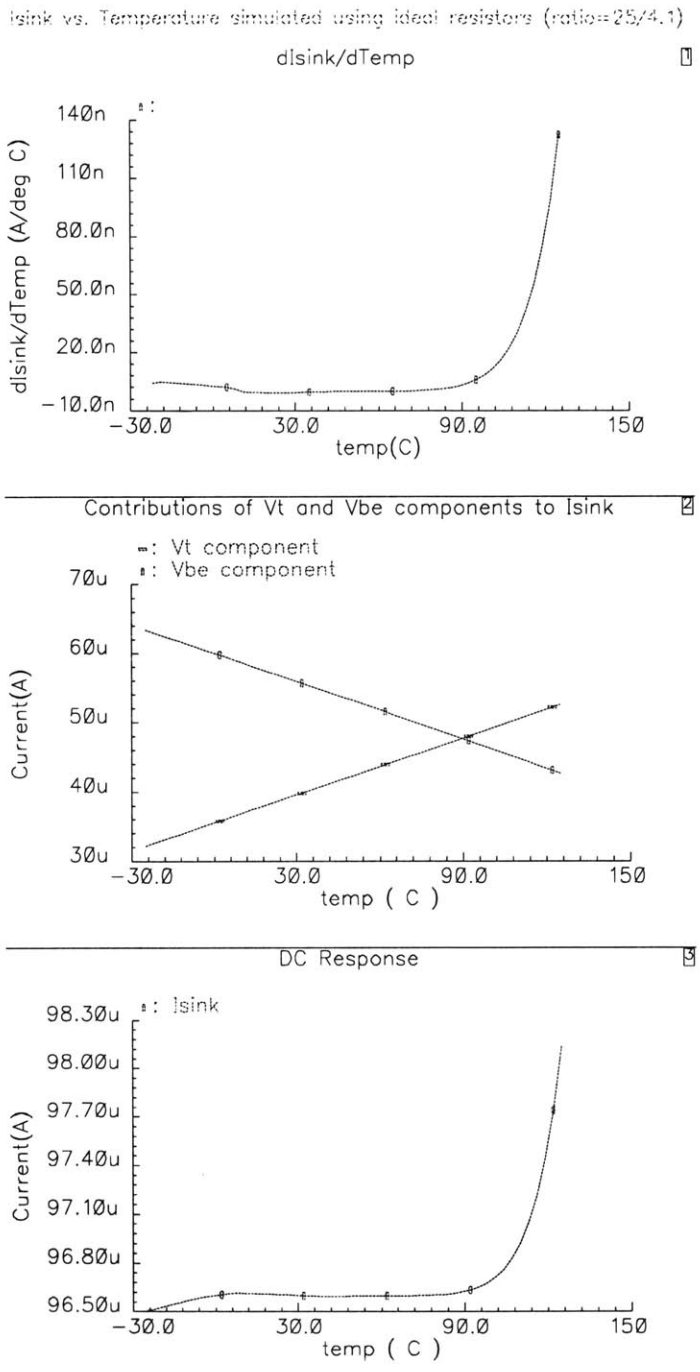

Figure 3-1: Simulation sweep of I_{sink} vs. temperature (using ideal resistors).

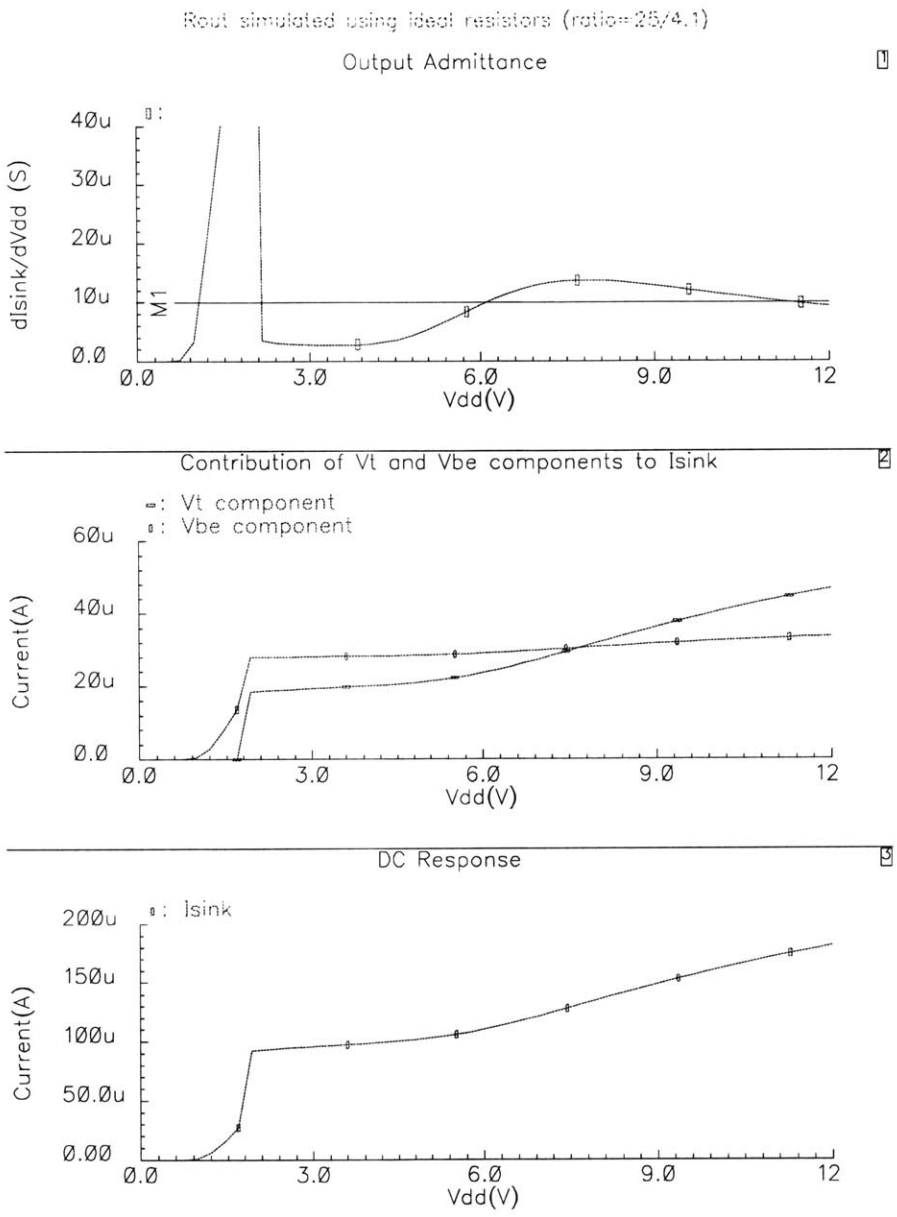

Figure 3-2: Simulation sweep of I_{sink} vs. voltage applied (using ideal resistors).

Chapter 4

Layout

The test circuit was fabricated via MOSIS using TSMC's 0.35um process. The complete layout is shown in Figure 4-1

4.1 MOS Transistors

Because the operation of this circuit relies on the precise cancellation of components, matching is of absolute importance.

To achieve this matching, the MOS transistors were laid-out in cross-coupled pairs of transistor fingers [2, p.435]. The PMOS current mirror transistors, M_1 and M_2, were laid out in the pattern d_1-s-d_2-s-d_1-s-d_2-s-d_1 / d_2-s-d_1-s-d_2-s-d_1-s-d_2, where the source was shared between the two transistors (Figure 4-2).

Dummy transistors were included on the ends of each row so that each MOS finger would be as uniform as possible.

The NMOS voltage mirror transistors, M_3 and M_4, were laid out in a similar format (Figure 4-3). However, because M_3 and M_4 have electrically distinct source nodes, this layout was a bit more complicated, and folded gate configurations were used for the unit transistor (as opposed to simple fingers).

4.2 Resistors

Resistors were created in the Poly2 layer as an interdigitated array of resistor sections (Figure 4-4). Polysilicon was chosen because its sheet resistance (48.6Ω/sq) was high enough to allow for reasonable geometries of kΩ-range resistors and because its temperature dependency was well-characterized (process specifications state 1070 ppm).

An attempt was made to layout all resistor sections around a common centroid. In each resistor segment, resistors were connected in alternating directions to cancel thermoelectric effects (mismatch due to thermal gradients) [2, p.240,251]. Dummy resistors were used to ensure uniform etching of all electrically significant resistor segments.

The unit resistor was 3.75 squares, which gave a unit resistance of

$$R = 3.75sq * 48.6\Omega/sq = 182.25\Omega$$

R_2 and R_3 each consisted of 122 of these unit resistors in series (22kΩ). R_1 consisted of 13 of these units in series $R_{1,max} = 2.4k\Omega$, 3 of which were typically bypassed by MOS

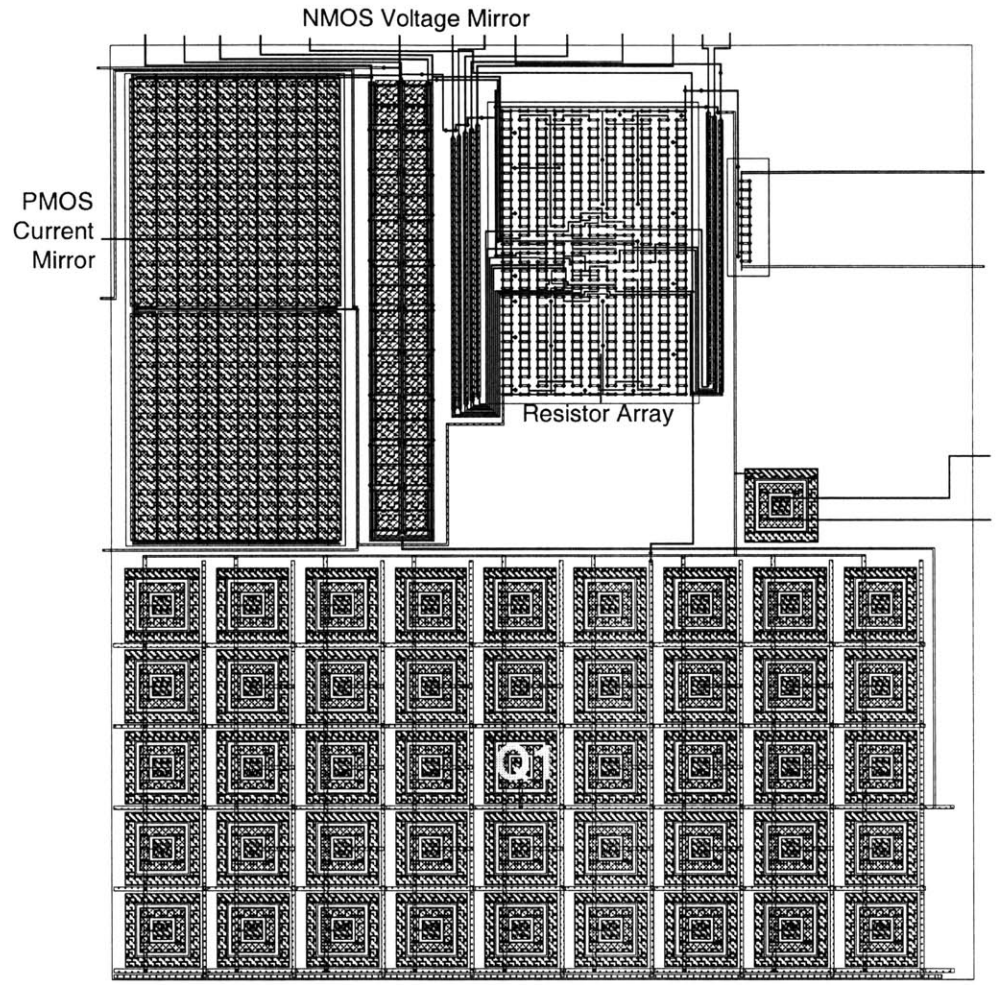

Figure 4-1: Complete layout.

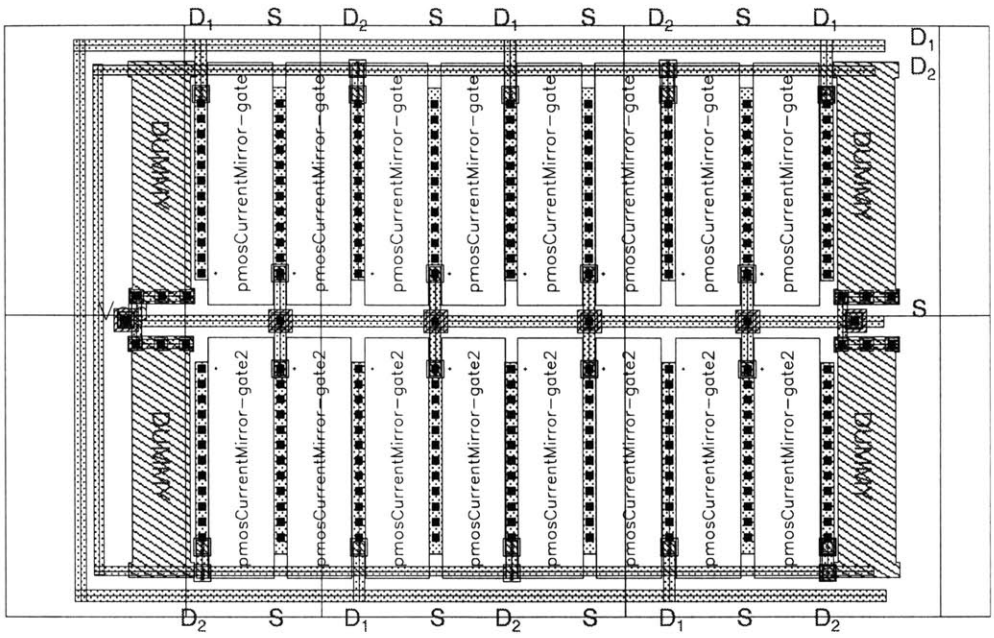

Figure 4-2: Layout of PMOS current mirror transistors, M1 and M2. The gates of these transistors are tied together (not shown).

switches. Other MOS switches were used to open alternate current paths, decreasing R_1 in increments of 1, 2, 4, 8, and 16%. The total set of MOS switches allowed a test range for the resistor ratio, K, of 69%-130% of the baseline value.

4.3 BJTs

Q_1 is a unit BJT. Q_2 is 20 of these unit BJTs in parallel, arranged around Q_1 on the layout. Dummy BJTs were placed to make sure that all BJTs used in the circuit were surrounded by other BJTs on all sides in the layout.

4.4 Test structures

An extra BJT and a 10-unit resistor chain were included on the chip as test structures.

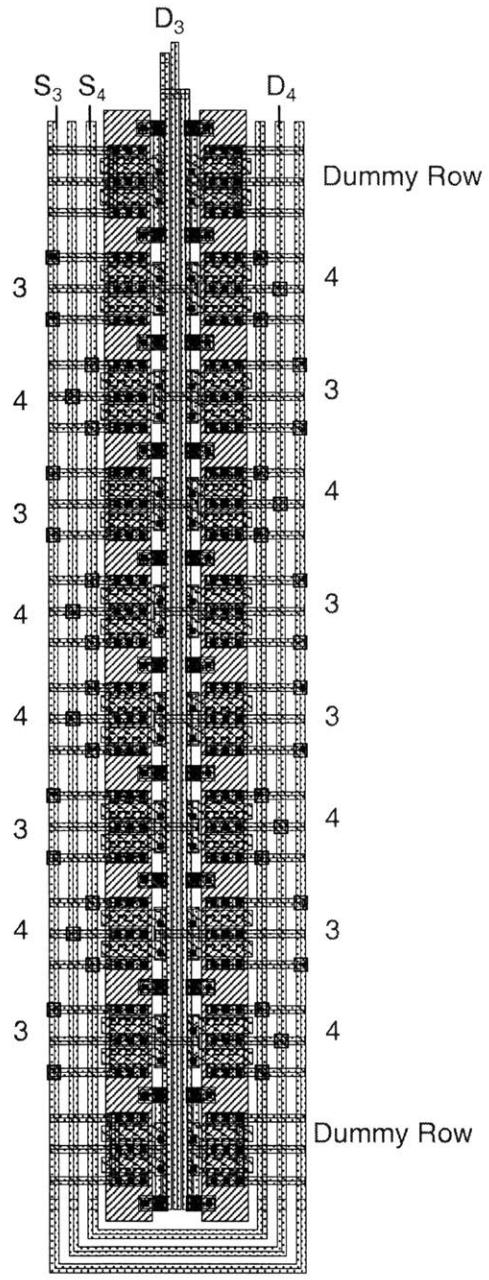

Figure 4-3: Layout of NMOS voltage mirror transistors, M3 and M4.

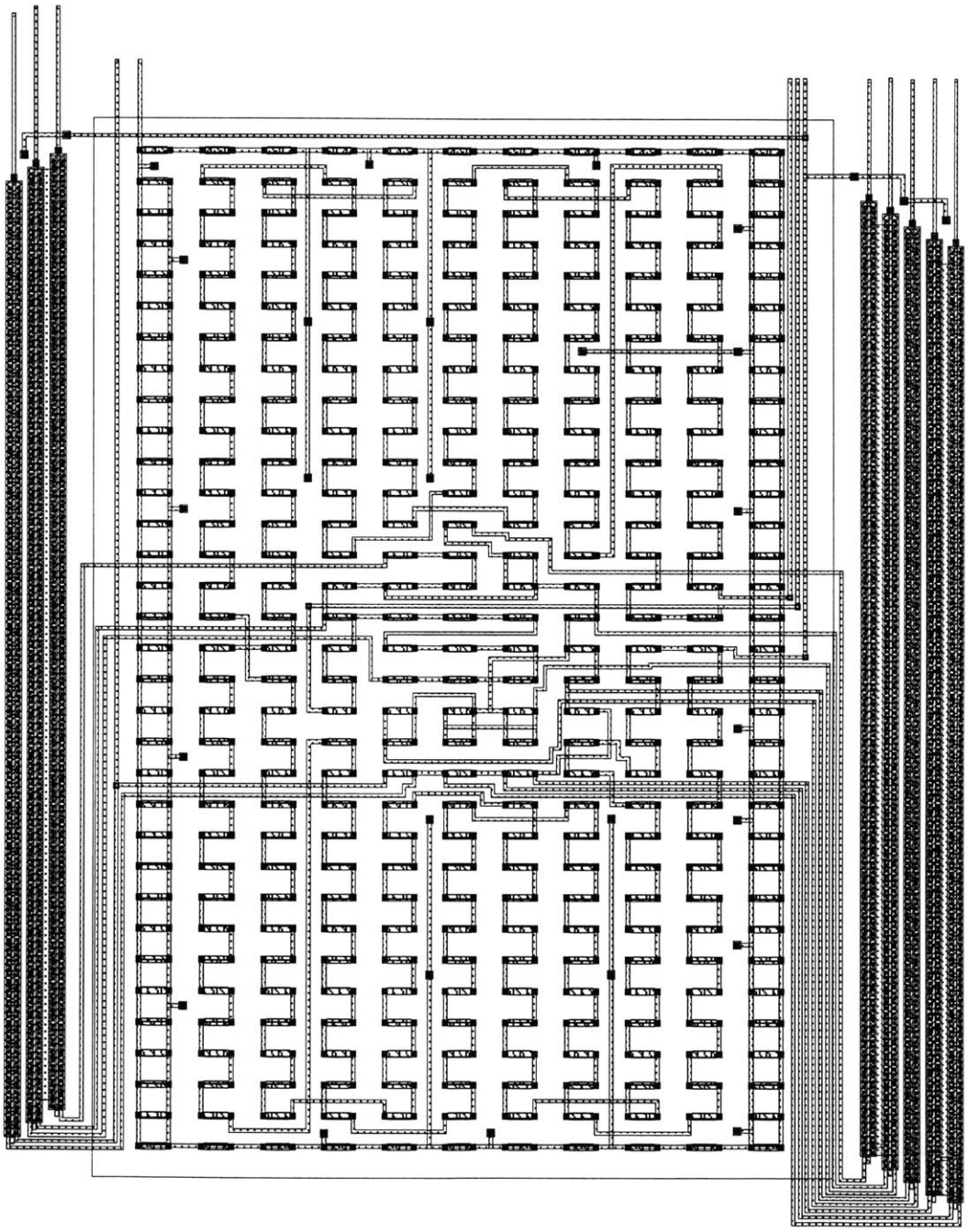

Figure 4-4: Resistor array and MOS bypass switches.

Chapter 5

Testing

5.1 Setup

In an effort to create a low-cost test setup, a "Hot/Cold Snack Box" from Sharper Image (model #SI712BLU) was used. This box used a Peltier device and could establish a temperature environment of 10^oC - 50^oC. Because this box created a lot of electrical noise, data was only taken during passive cooling/heating phases; in other words, the box was turned off once it reached a temperature extreme, then data was taken as the box temperature settled back to room temperature.

The instruments used to take the test data were a Keithley M1321 Thermocouple and an HP 4140B pA Meter. The two instruments were controlled using a computer running LabView 5 through a modified version of code that was originally written by Ching-Chun (Ginger) Wang.

The schematic for the test setup can be seen in Appendix B. Because electrostatic discharge (ESD) protection for the MOS bypass switches (M_5 - M_{12}) was unfortunately neglected in the layout design, external capacitors and resistors were used.[1]

5.2 Results

The test BJT had a DC current gain β=6 and a saturation current of 2x10^{-17}A. The test 10-unit resistor had a resistance of 3kΩ which gives us a fabricated unit resistance of 300 Ω (expected value was R=182.25 Ω).

Results from a sweep of applied voltage are shown in Figure 5-1. The chip had a turn-on voltage of about 2V, at which point it exhibited an output resistance of

$$R_{out} = \frac{3.19V - 2.19V}{89.7\mu A - 86.9\mu A} = 350k\Omega$$

Also note that the positive feedback caused hysteresis, where the applied voltage would have to drop slightly below the turn-on voltage of 2V (down to about 1.5V) to get the device to turn off.

Next a temperature sweep was done to test the temperature dependence of the current source. Results for different resistor ratios are shown in table 5.1.

[1] Protection diodes, also shown in the schematic, will be added before future testing is done.

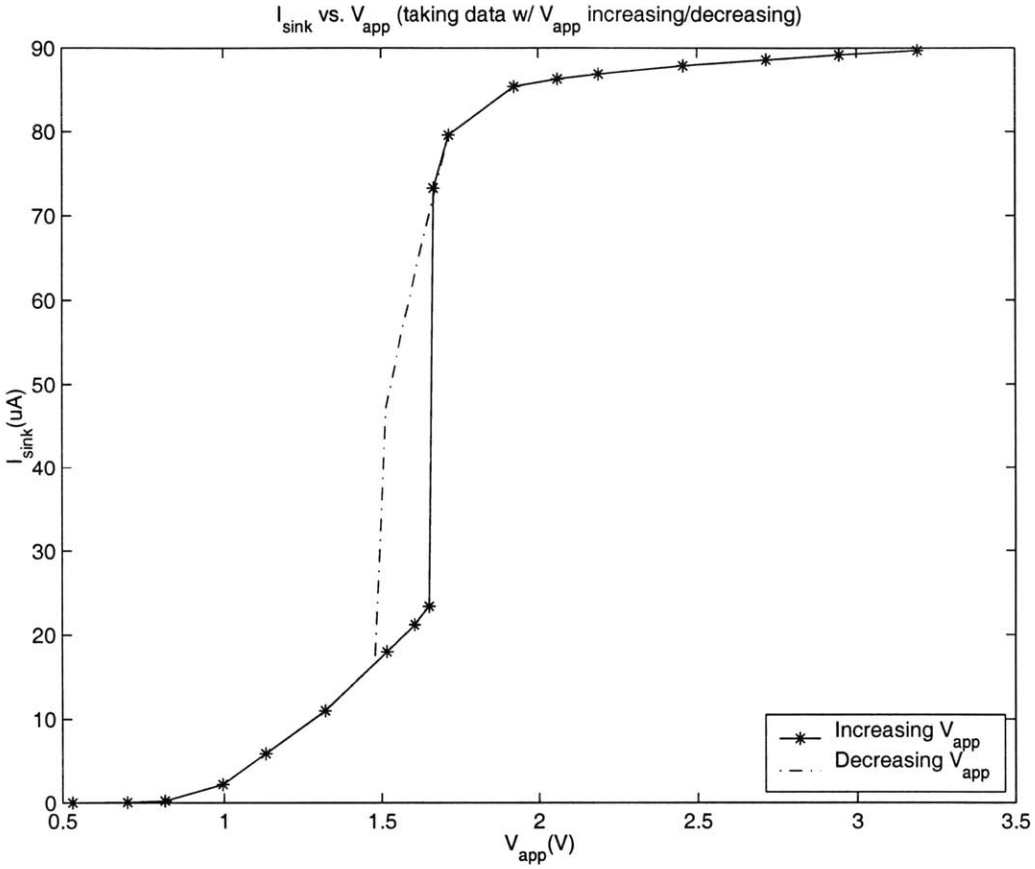

Figure 5-1: Chip 2 - Isink vs. Vapp.

Table 5.1: Temperature sensitivity for different resistor ratios

Resistor Ratio (% of k=122/10)	Temperature Coefficient (ppm/^{o}C)
100%	417
130% (all gates grounded)	113

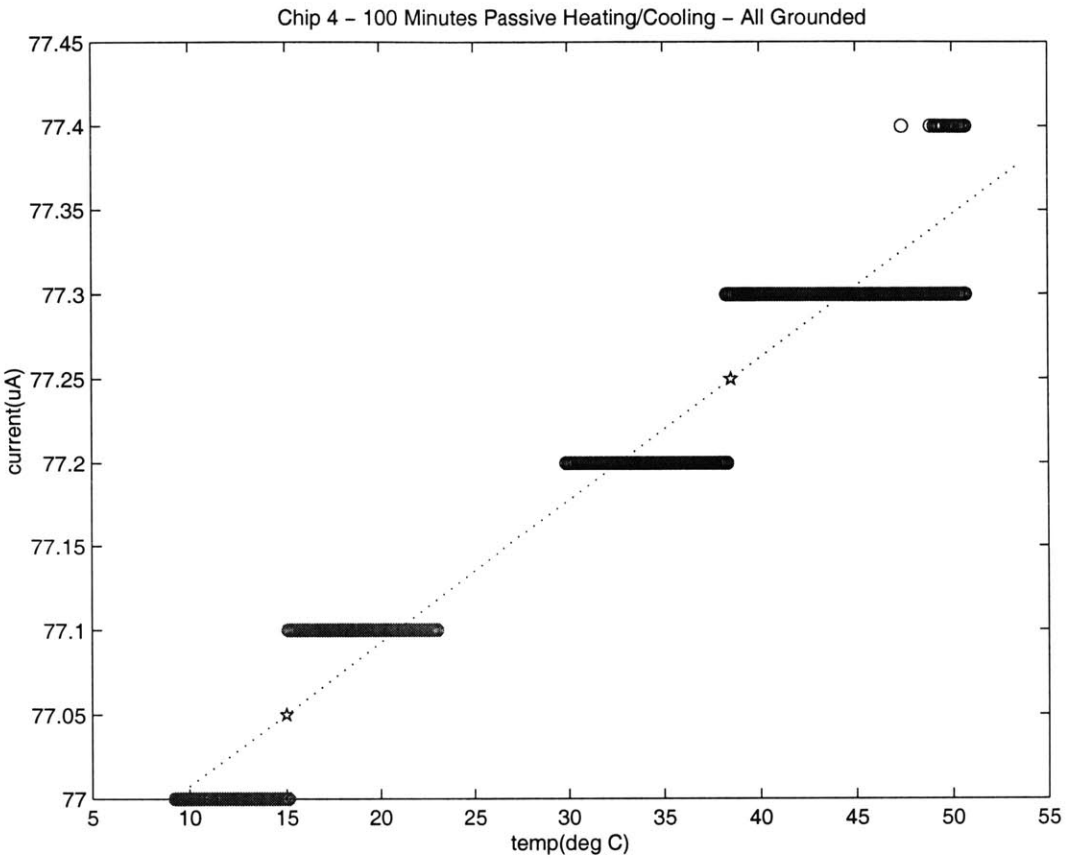

Figure 5-2: Chip 4 - Temperature sensitivity = 113 ppm/deg C

The circuit exhibited the most temperature independence when the gates of all the MOS switches were grounded (R_1 at maximum). Plots for this configuration are shown in figure 5-2.

Using the box method to characterize the chip's temperature sensitivity gives us the following:

$$TC_F = \frac{I_{sink,max} - I_{sink,min}}{\Delta T I_{sink}} = \frac{77.3\mu A - 77.1\mu A}{(38^oC - 15^oC)77\mu A} * 10^6 ppm = 113 ppm/^oC$$

A summary of results appears in table 5.2.

Table 5.2: Summary of results for bandgap current source

Parameter	Magnitude
Output Current (I_{sink})	77μA
Turn-On Voltage (V_{on})	2V
Temperature Coefficient (TC_F)	113 ppm/^{o}C
Tested Temperature Range	10^{o}C - 50^{o}C
Output Impedance (R_{out})	350 kΩ
BJT Saturation Current Ratio (S)	20
Optimum Resistor Ratio (K)	122/13

Chapter 6

Conclusion

A prototype 2-terminal bandgap curent source was designed and fabricated using only 4 MOS transistors and 2 parasitic PNP transistors in a standard 0.35μm CMOS technology.

The baseline current of this circuit was 77μA. This is lower than expected in simulations, most likely because the fabricated unit resistance was much higher than the simulated (extracted) resistance. One cause of this discrepancy is the lack of accounting for contact resistance in the extraction rules. Given that each resistor segment was only 3.75 squares, neglecting the contacts significantly underestimates the value of the resistor.

The circuit exhibited a temperature coefficient of 113 ppm/^{o}C. Commercial bandgap references typically have dependencies of 25-50 ppm/^oC. Considering that the circuit exhibited the least temperature dependence when R_1 was greatest, it is likely that the most efficient resistor ratio was not implemented. Future chips should allow for a much larger value of R_1.

Power-supply voltage independence was also exhibited. Output impedance was approximately 350 kΩ.

6.1 Difficulties Encountered

Extracting BJT data from the layout proved to be difficult because the BJT extraction rules in the design kit from MOSIS were incomplete. The completed rules are documented in Appendix C.

A limitation of using the pA meter was that it had an accuracy of only 3 significant digits. With this level of accuracy, measuring a temperature coefficient close to commercial levels would have required either a) a test environment with a wider temperature range (not practical), or removal of the baseline current before I_{sink} was measured by the ammeter. A PCB implementing the second solution, with a current source in parallel with the ammeter, is shown in Appendix B. However, this solution has yet to be implemented.

A mistake was made in that no electrostatic discharge protection (ESD) was included for the gates of the MOS switches (M_5 - M_{12}). During testing, 5 chips were blown. In every failed chip, the gate of M_{12} appeared to be shorted. It is not certain why this particular gate was the most vulnerable to failure.

6.2 Future Work

Potential revisions of the layout should include ESD protection for the gates of the MOS switches, and should allow for a higher resistor ratio.

In order to get higher accuracy, future measurements will use an external current source to cancel out the baseline current, as seen in the schematic of Figure B-1.

Appendix A

Full Schematic

This is the full schematic as verified with the extracted data of the complete layout.

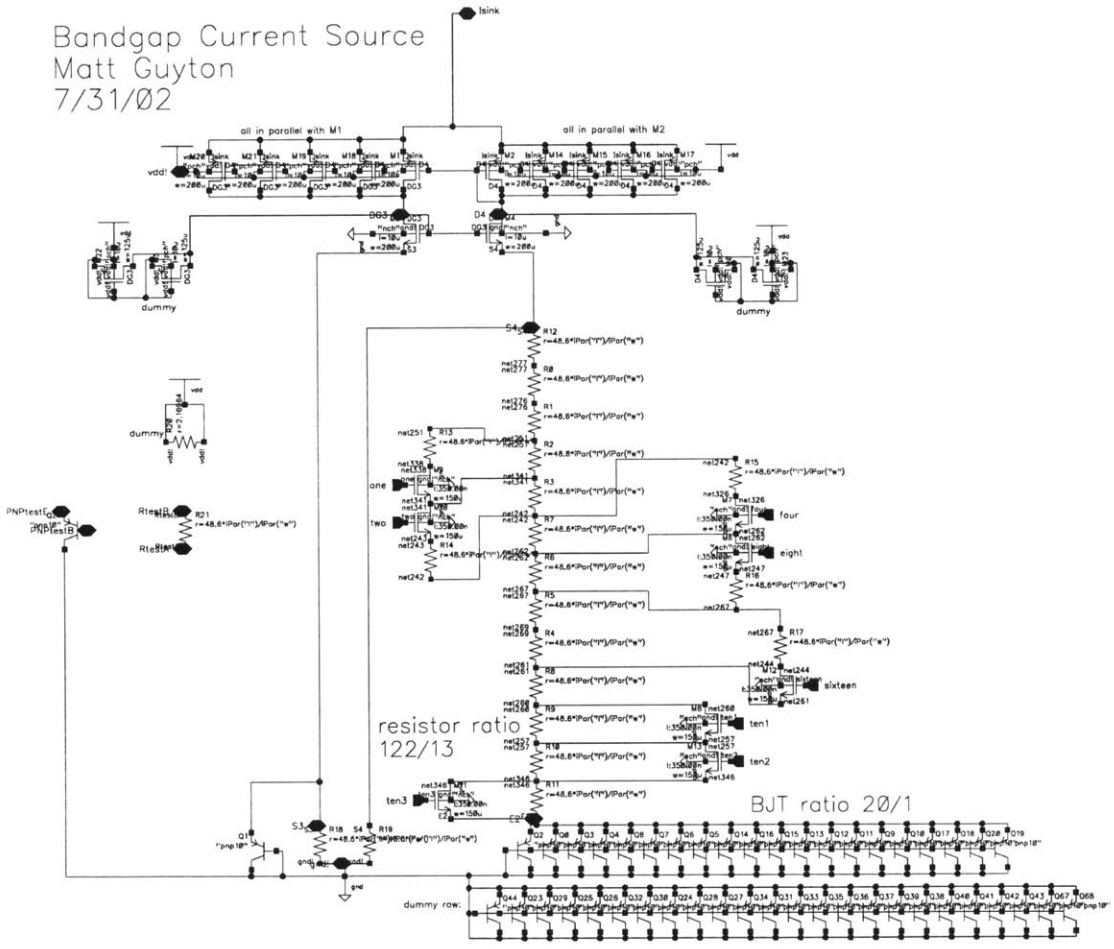

Figure A-1: Complete schematic.

Appendix B

PC Board

For future testing of the bandgap current circuit, a printed circuit board (PCB) has been designed. It implements 2 ideas that have not yet been tested - protection diodes for the gates of the MOS switches (M_5 - M_{12}), as well as having a current source in parallel with the ammeter to remove the baseline current.

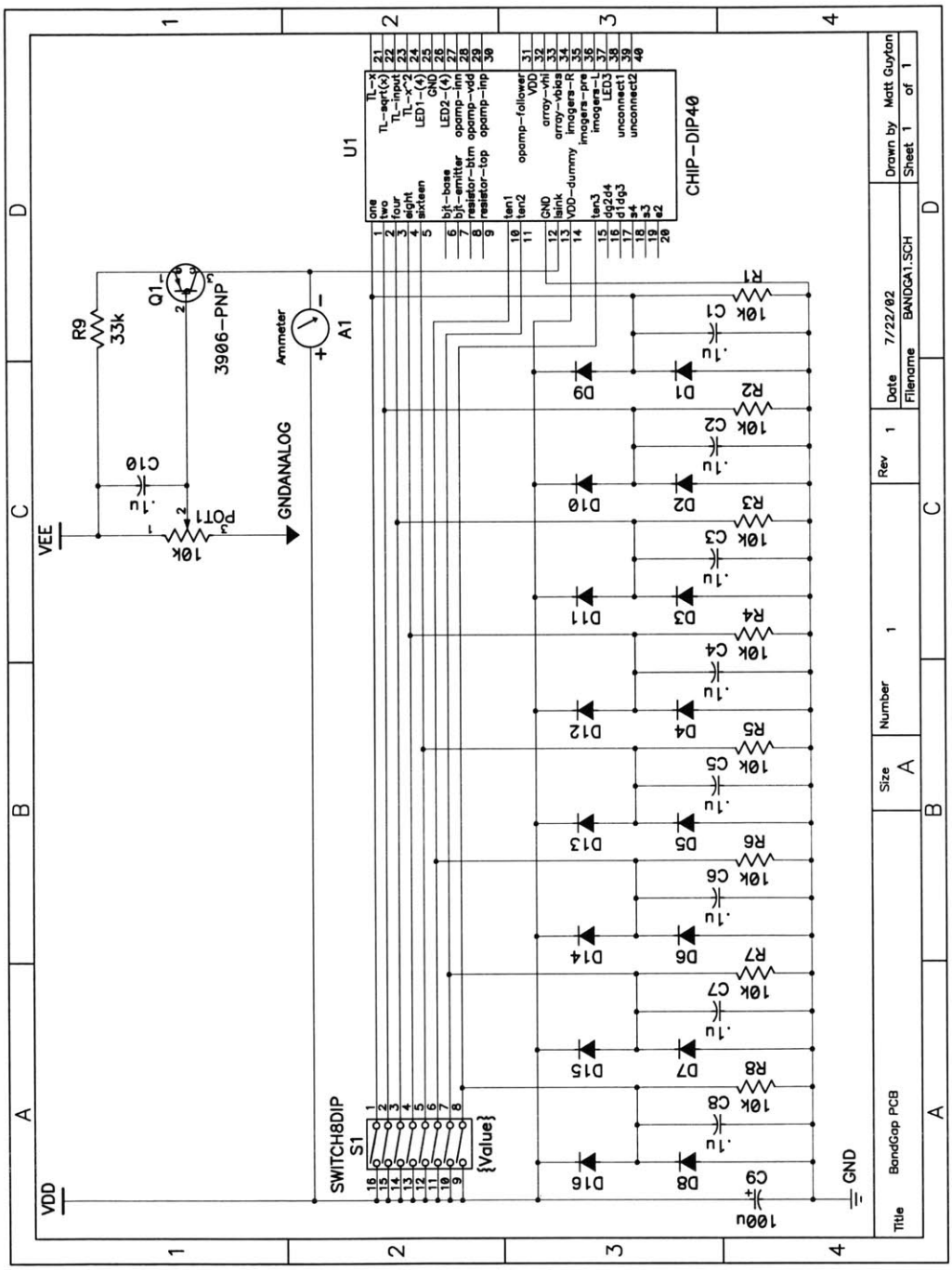

Figure B-1: Test setup - printed circuit board schematic. Note that pins 21-40 of the DIP are part of a different project.

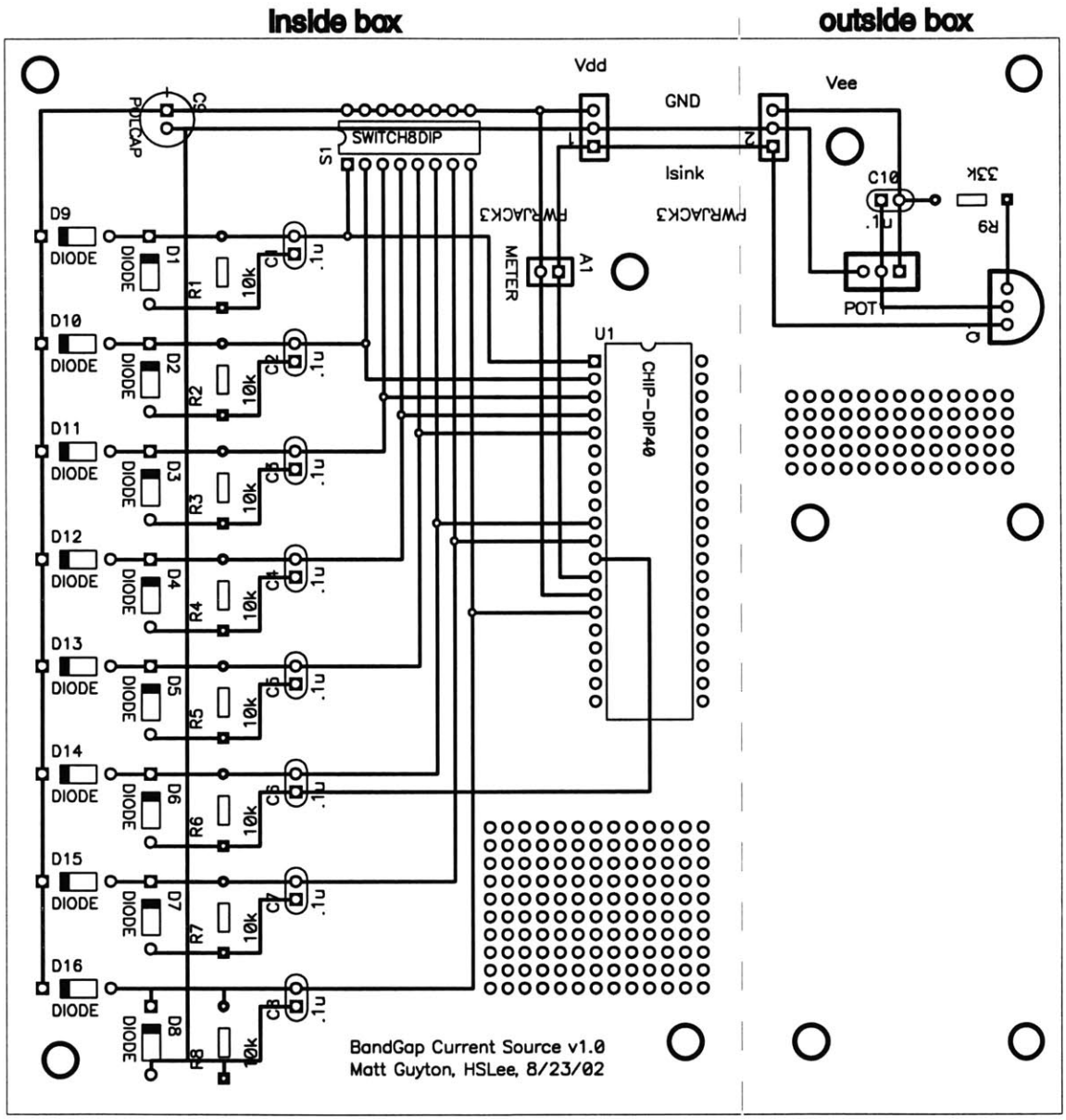

Figure B-2: Test setup - printed circuit board layout. Board is split. Everything to right of DIP40 package placed outside temperature controlled environment.

Appendix C

BJT Extraction From Layout

Getting DIVA to extract the BJT's from the layout proved difficult because the TSMC .35μm design kit came with incomplete rules for this extraction. Glenn Jennings at MOSIS was particularly helpful in debugging this problem. His correspondence is included below.

```
 On Tue, 18 Dec 2001 mcguyton@MIT.EDU wrote:

 [ I'm using your 2p4m .35um TSMC process in Cadence.
 [ I can't get vertical PNPs to extract as anything (only the metal is
 [ extracted).  Even if I make a cellview containing only your
 [ parameterized pcell\pnp, the extraction doesn't recognize it as a BJT!
 [ I can get resistors, PMOS, and NMOS to extract correctly.
 [
 [ The error message is "WARNING - no devices available to which
 [ properties can be added."  Sometimes it says "parameters" instead of
 [ "properties".
 [
 [ How can I get this to extract correctly?

OK, this one first.  Make a copy of the original file
  cmosp35.3.0/dfII_lib/cmosp35/divaEXT.rul

and do some editing to the copy as follows:

locate this line:

   pnpEmitter=geomGetTexted(pdiff "device" "emit" "emitter")
                                  ^^^^^^^^

and change it to:

   pnpEmitter=geomGetTexted(pdiff ("device" "all") "emit" "emitter")


locate all of the following lines, and unmask them:

; extractDevice(pnpVertical (sub "C") (pnpBase "B") (pnpEmitter "E")
```

```
;                "pnp ivpcell cmosp35")
; saveRecognition(pnpVertical "nwell")

; sub=geomOr(sub subDevices)
; sub=geomStamp(sub pohmic)
; nwell=geomStamp(nwell geomCat(nohmic  nohmicPnpBase) error)
; pnpBase=geomStamp(pnpBase nohmicPnpBase)
; pnpEmitter=geomStamp(pnpEmitter pdiff)

; emitterAreaVertical=measureParameter(area (pnpVertical over pnpEmitter)
;                                       1.0e-02)
; baseAreaVertical=measureParameter(area (pnpVertical) 1.2755102e-03)
; saveProperty(pnpVertical "model" "pnp")
; saveParameter(emitterAreaVertical "area")
; saveParameter(baseAreaVertical "areab")
```

This should get you a little farther as far as extraction is concerned.
Next is this one:

```
 [ I can't get vertical PNPs (a pcell included with the design kit) to
 [ pass DRC.  I'm using them diode-connected and so the base (Nwell) is
 [ connected to the collector (substrate).  It seems that to pass DRC,
 [ all Nwells have to be connected to Vdd, otherwise I get the error
 [ "substrate soft connected".  If the base and collector are shorted, it
 [ is not possible to satisfy this rule.
 [
 [ How can I do to fix this?  It doesn't seem like NWells should have to
 [ be tied to Vdd to pass DRC...
```

This kind of softconnect "error" has to be interpreted by the
designer. In this case, since it is a PNP structure, you should
simply disregard it. I fear that tweaking the DRC file to make this
suprious flag go away, would cause more problems than it solved.

Regards,
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