Active Filter Techniques for Reducing EMI Filter Capacitance
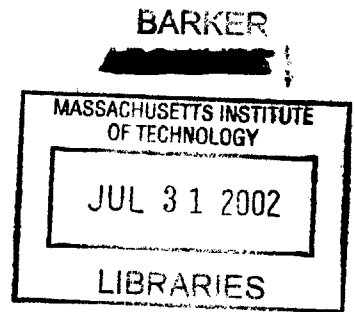
by

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Abstract

Switching power converters are widely used due to their excellent efficiency, but they inherently generate ripple. Passive low-pass LC filters have been traditionally employed to meet ripple and EMI specifications [1]. These passive filters can contribute considerably to the volume and weight of a power converter. In particular, capacitors can become relatively large in order to meet strict ripple specifications. This is detrimental to cost and reliability of these passive EMI filters. For these reasons, capacitors in EMI filters can pose a considerable design challenge. Active circuit techniques can substantially reduce passive EMI filter capacitor requirements. This thesis investigates using active circuitry to mitigate the challenges of designing with large capacitors on three fronts: reducing capacitance in EMI filters, reducing damping capacitance, and reducing capacitance cost.

A significant reduction of the passive EMI filter capacitor can be achieved by active ripple filters. This thesis investigates a hybrid passive/active filter topology that achieves ripple reduction by injecting a compensating voltage ripple across a series filter element. Both ripple feedforward and feedback are employed. The design of sensor, amplifier, and injector circuitry for this application is explored. The experimental results demonstrate the feasibility and high performance of the new approach, and illustrate its potential benefits.

The damping capacitor can easily become the dominant capacitance of the system. By using signal-level transistors, the needed capacitance can be greatly reduced. A feedback system using current sense and current drive is explored in this thesis. Test results demonstrate an improvement by a factor of a thousand.

Active techniques can also reduce the cost of capacitor in EMI filters, by enhancing the performance of low cost capacitors. This work applies active techniques to the input EMI filter of a commercial automotive motor drive system. Initial evaluation has demonstrated the feasibility of this approach. More work will be required to further evaluate the details of active filter system to this commercial application.

Thesis Supervisor: David J. Perreault
Title: Active Filter Techniques for Reducing EMI Filter Capacitance

1.1 Motivation

Switching power converters inherently generate ripple, and typically require input and output filtration to meet ripple and EMI specifications, (e.g., Fig 1.1). Passive LC low-pass filters have traditionally been employed to achieve the necessary degree of ripple attenuation [1]. The capacitors in these passive filter components often account for a large portion of filter size and cost [1-4]. Furthermore, the temperature and reliability limitations of filter capacitors can present a significant design constraint.

Take for example a commercial application, which uses a 1-kilowatt inverter for automotive electro-hydraulic power steering. The input filter for this switching inverter requires three electrolytic capacitors and two inductors. The capacitors account for approximately 75% of the filter volume, and a rough estimate suggests that they attribute to more than 60% of the cost. Furthermore, there is the question of the lifetime of these large electrolytic capacitors when they are subjected harsh environmental conditions (e.g. vibration and wide temperature ranges). Coupled with strict EMI requirements shown in Fig 1.1, techniques to reduce the required capacitance become attractive.

An alternative to the conventional passive filtering approach is to use a hybrid passive/active filter [2-10]. In this approach, a small passive filter is coupled with an active electronic circuit to attenuate the ripple. The passive filter serves to limit the ripple to a level manageable by the active circuit and to attenuate ripple components that fall beyond the bandwidth of the active circuit. The active filter circuit cancels or suppresses the low-frequency ripple components that are most difficult to attenuate with a passive low-pass filter. Essentially, the cut-off the LC filters needs to be placed well below the
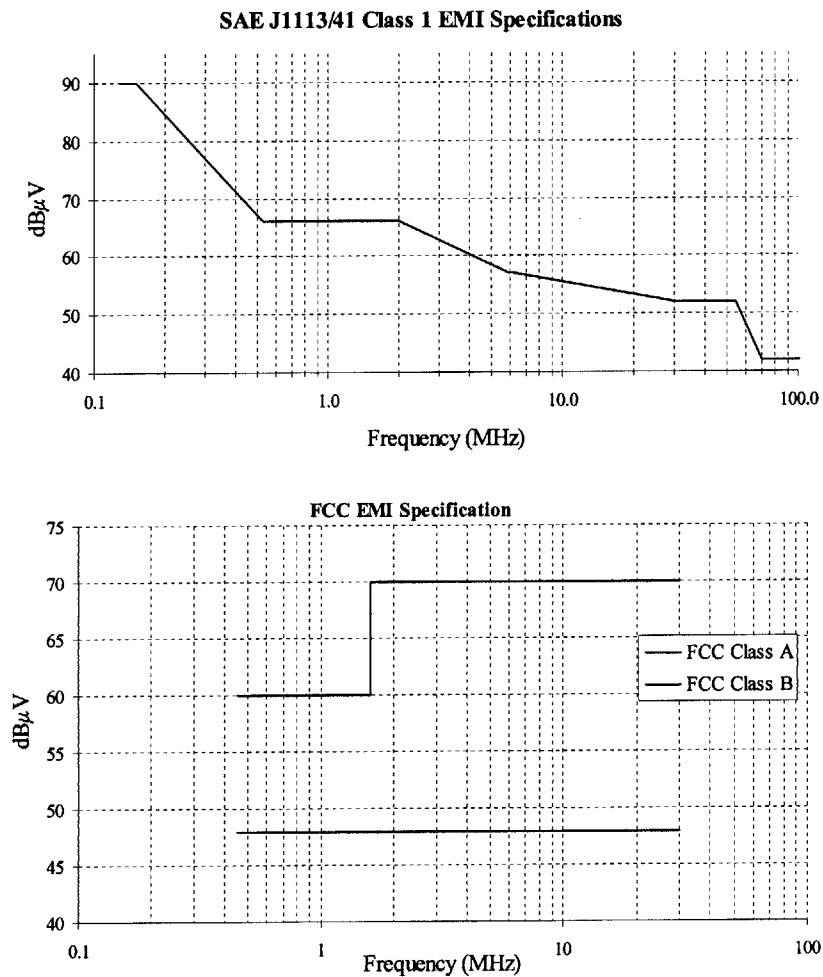
Figure 1.1 Various EMI specifications: (from top to bottom) SAE J1113/41 Class1 Automotive conducted EMI specification for narrowband signals. FCC conducted EMI limits. The voltage is measured across a 50Ω LISN impedance.

frequencies that are to be attenuated, which make the components large. By using active circuitry to provide a fair amount of attenuation, less attenuation is required from the passive filter. This permits a substantial reduction in the passive filter size, with potential benefits in converter size, weight, and cost.

Active filters may be characterized by whether they inject ripple voltages [3,7] or currents [2,4-10] to achieve ripple reduction. Controls governing the ripple correction can be derived through either feedforward [2,9,10] or feedback [5-8]. Feedforward controlled filters sense a ripple component and inject its inverse, while feedback controlled filters suppress ripple via high-gain feedback loop, see Fig 1.2. Combinations of these mechanisms are also possible (see [3,4] for example), and there are a wide variety of means for implementing the sensing and injection functions.

This thesis focuses on active filter techniques that minimize the required capacitance in filters. A hybrid active/passive topology is introduced that achieves ripple reduction by injecting an opposing voltage in series with the voltage ripple source. This
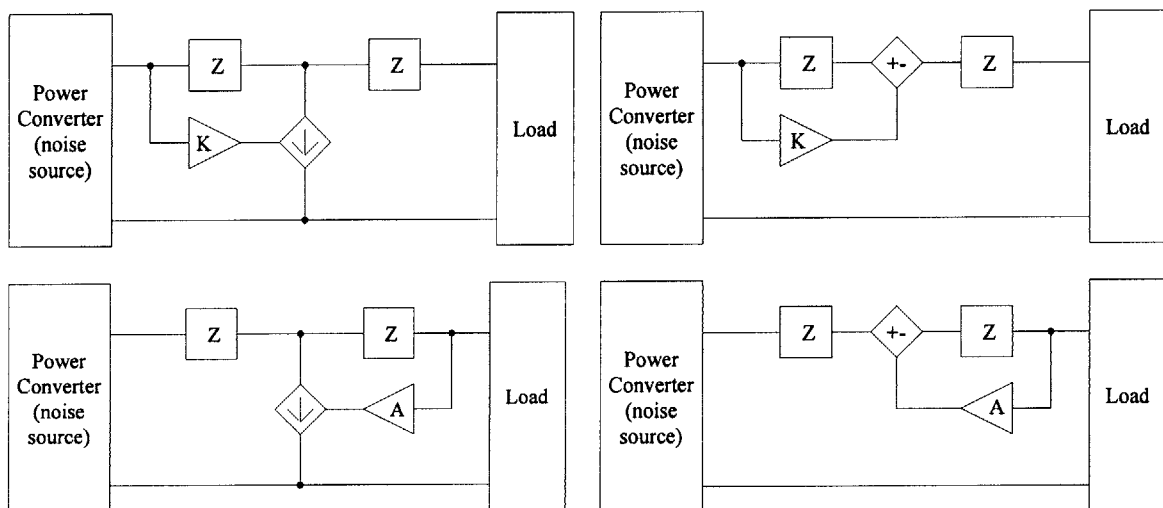
Figure 1.2 Various active ripple filter topologies (clockwise from top left): Current ripple filter using feedforward control. Voltage ripple filter using feedforward control. Current ripple filter using feedback control. Voltage ripple filter using feedback control.

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is effective in minimizing the size of EMI capacitors needed. A second hybrid active/passive technique uses a current amplification topology to reduce the needed filter damping capacitor. Finally, the use of feedback active filters to reduce the filter capacitor size in PWM motor drives is explored.

1.2 A Feedforward/Feedback Active Ripple Filter

Figure 1.3 illustrates an active ripple filter topology using both feedforward and feedback. This topology operates by injecting ripple voltage to oppose the ripple voltage appearing across the buck capacitor C_{buck}. Essentially this technique mimics a voltage divider. The voltage ripple is divided between the active voltage source and the output. If the voltage source perfectly duplicates the voltage ripple then the output voltage will be ripple free. The injector design is challenging since it must accurately generate the desired ac injection voltage while carrying the full dc converter current. The injection signal is based on a superposition of easily-measured feedforward and feedback voltage ripple signals. Implementing the control design is also a challenging task. The transfer function from the ripple source to the output is given by equation 1.1 for a feedforward gain of $K(s)$.

$$\frac{V_{out}(s)}{V_{ripple}(s)} = 1 - K(s) \qquad (1.1)$$
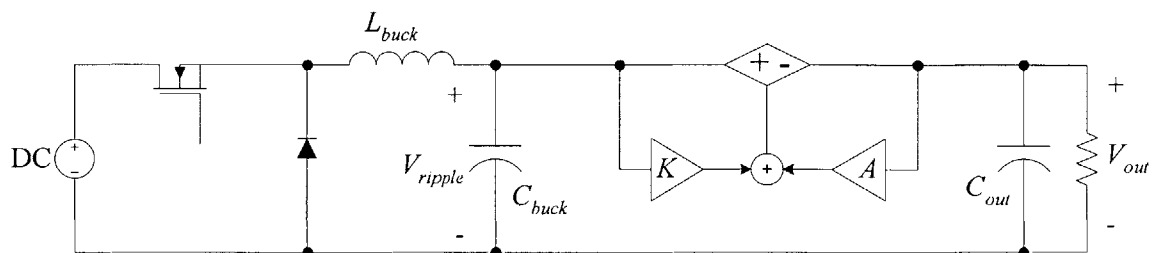
Figure 1.3 Feedforward / feedback voltage ripple filter used in combination with a passive filter at the output of a buck converter. The hybrid passive/active filter enables a reduction in the size of the passive filter components.

For a perfect feedforward path gain of unity, the ripple at the output would be zero. However, due to gain and phase accuracy limitations in the components, feedforward cancellation alone cannot fully attenuate the ripple. Considering the feedback path alone, the ripple source to output transfer function is:

$$\frac{V_{out}(s)}{V_{ripple}(s)} = \frac{1}{1 + A(s)} \tag{1.2}$$

The ripple at the output becomes small as the magnitude of gain A(s) becomes large. In the feedback case, stability considerations limit the achievable feedback suppression. Combining feedforward and feedback takes best advantage of the injector circuitry and maximizes ripple attenuation. This thesis will explore this active/passive filter technique in detail. It will be shown that the proposed structure is attractive in cases where it is desirable to minimize the passive filter capacitance, C_{out}.

1.3 Active Damping

Figure 1.4 illustrates how filter damping is often implemented. In many cases, passive components used to implement filter damping can be larger than the primary filter elements themselves. For instance, the capacitor value used in a shunt damping leg is
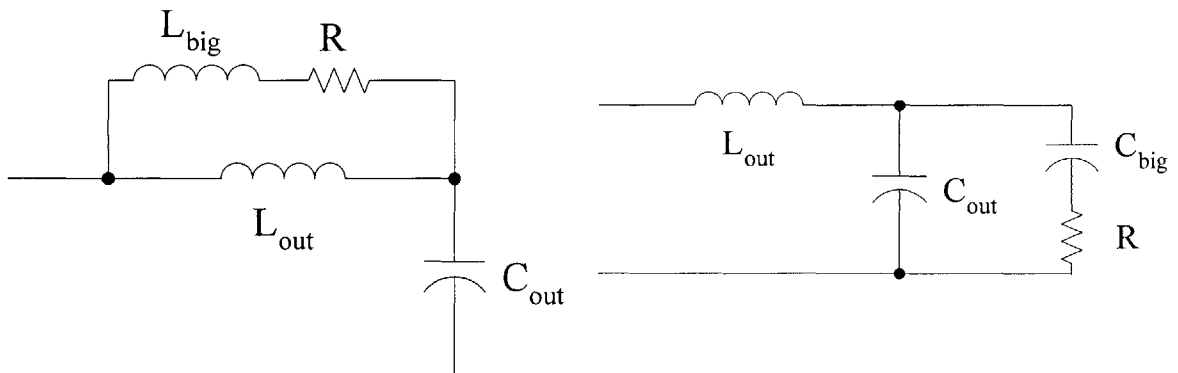
Figure 1.4 Illustrates common damping topologies (from left to right): series damping and shunt damping. The series damping topology employs an inductor and resistor. The DC current component flows through the output inductor. At higher frequencies the current flows through the resistor because the bypass inductor is smaller than the output inductor. The shunt damping approach uses a capacitor and resistor. At DC there is no voltage across the resistor. At AC frequencies near the corner frequency ripple flows through the resistor.

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usually an order of magnitude larger than the value of the filter capacitor [1]. Active

damping, in which active circuits are used to realize the desired damping characteristics, is

an attractive approach for reducing passive component size.

Realizing active damping for a shunt damping leg suggest topologies where a

damping capacitor is actively enhanced. Just as with active ripple filters, this can be

accomplished in a variety of feedback topologies: current-sense/current-drive, voltage-

sense/current-drive, current-sense/voltage-drive, and voltage-sense/voltage-drive (Figure

1.5). This thesis investigates the use of the current-sense/current-drive topology for

damping. It will be shown that the required size of the damping capacitor is greatly

$$Z_{eq} = Z_c \parallel \frac{Z_c}{A(s)}$$

$$Z_{eq} = Z_c[1 + A(s)]$$

$$Z_{eq} = Z_c \parallel \frac{1}{A(s)}$$

$$Z_{eq} = \frac{Z_c}{1 + A(s)}$$
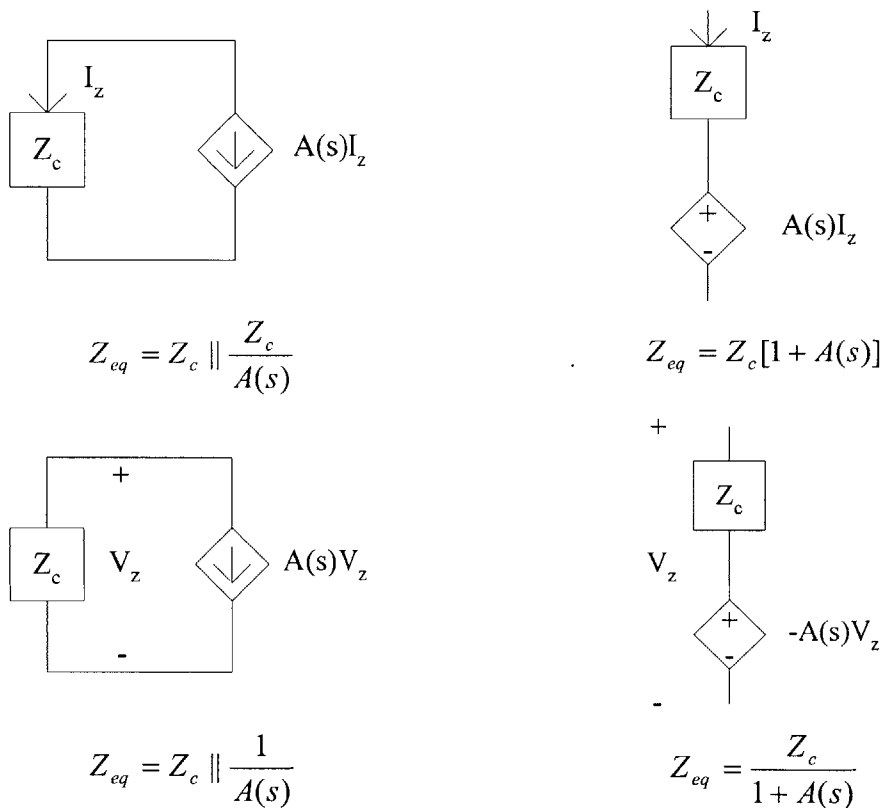
Figure 1.5 Various impedance reduction topologies (clockwise from top left): Current sense-Current Drive. Current sense-Voltage drive. Voltage sense-Current drive. Voltage sense-Voltage drive.

reduced by the active circuitry.

1.4 Feedback Active Filtering

Capacitors contribute significantly to the cost of EMI ripple filter. High frequency demands further exacerbate this cost. In other words, the cost to capacitance ratio increases for high frequency capacitors. For instance, ceramic capacitors are extremely expensive due to their excellent high frequency performance. Filter designs still rely on relatively large ceramic capacitors in order to meet strict EMI specifications at high frequencies, which add to filter cost. This makes ceramic capacitors a prime target for active techniques.

Active topologies are used in conjunction with low frequency capacitors to mimic the performance of high frequency ceramic capacitors at a fraction of the cost. Since the hybrid filter must replace an expensive ceramic, cost considerations severely constrain the design of the hybrid filter. The active ripple filter uses feedback control. Similar to active damping, the various topologies is shown in Figure 1.5. These active techniques are applied to a full production, commercial PWM motor drive. The thesis will explore the primary technical challenges and proposed topologies.

1.5 Thesis Objective and Organization

The thesis is organized as follows: The following two chapters of the thesis explore the design of the active ripple filter illustrated in Fig 1.3. Chapter 2 addresses the design of transformer-based voltage injectors and sensors. Chapter 3 explores the design of feedforward and feedback control circuitry for this approach. Active damping techniques are addressed in Chapter 4. Chapter 5 of the thesis describes the application of the proposed scheme to the output filter of a buck converter, and experimentally

compares the performance of the approach to that achievable with a conventional passive filter. Chapter 6 explores the implementation of active ripple filter to PWM motor drives. Finally, Chapter 7 offers a conclusion to the work.

2.1 Introduction

This chapter considers the design of voltage injectors for active ripple filters. The injector circuit (represented as a controlled voltage source in Fig. 1.1) must meet a number of challenging requirements. First, the injector must carry the full dc output current with minimal losses. Second, the injector must provide both isolation and sufficient input impedance for the active electronics. Finally, it must be able to replicate the injector signal with high fidelity. For the given constraints, a transformer proves to be an ideal choice for a voltage injection mechanism. Advantages of a transformer-based injector include minimal dc losses and inherent galvanic isolation (for coupling to control circuitry.) Furthermore, for an ideal transformer the voltage appearing on the primary
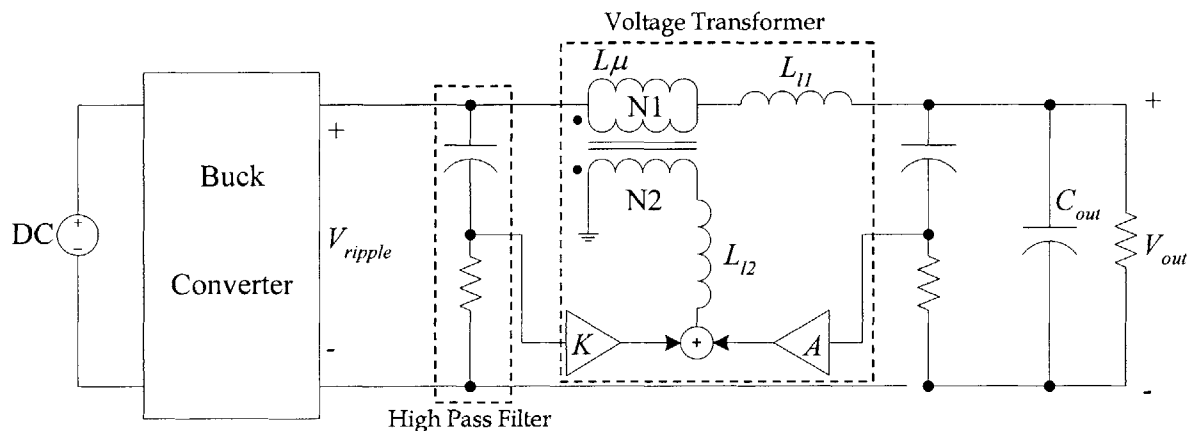
Figure 2.1 Hybrid Active/Passive Filter implementation using a single-magnetic component voltage injector. Voltage is sensed with an op amp via a high pass filter. Voltage is injected using a voltage transformer; the significant transformer parasitics are shown. L_μ is the magnetizing inductance, and L_{l1} and L_{l2} represent the leakage inductances.

side is a perfectly scaled version of the voltage on the secondary side. This thesis

considers two different voltage injector implementations that address these challenges.

2.2 Single Magnetic Component Voltage Injector

Figure 2.1 illustrates one possible transformer-based injector, including the

relevant transformer parasitics. A primary challenge is handling the large dc current in

the system. In this case, the dc current of the converter passes through the magnetizing

inductance of the transformer. This requires that the core be properly sized and gapped

to prevent saturation under this heavy bias condition. The transformer magnetizing

inductance L_μ and turns ratio must also be selected such that the transformer presents

sufficient impedance so that the signal-level amplifier is not loaded. The amplifier

circuitry is required to generate an ac voltage of magnitude:

$$V_{circuit} = \frac{N_2}{N_1}\left|V_{ripple}\right| \tag{2.1}$$

and a current of magnitude:

$$I_{circuit} = \frac{N_1}{N_2}\frac{\left|V_{ripple}\right|}{\omega_{ripple}L_u} \tag{2.2}$$

where L_μ is the magnetizing inductance measured on the transformer's primary side,

$\left|V_{ripple}\right|$ is the magnitude of the ripple to be cancelled, and ω_{ripple} is the fundamental

frequency of the ripple.

The first step in designing a transformer voltage injector is calculating the

required magnitizing inductance (and hence transfomer core size), which is determined

by the output current and dissipation limits of the amplifer circuitry. The transformer

turns ratio is used to match the voltage and current drive levels of the amplifier to those

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required for voltage ripple cancellation. To maximize amplifier use and minimize injector size, the turns ratio should be selected to fully utilize the available amplifier voltage and current swing. For example, the amplifier in the prototype system has an output voltage limit of +/- 6 V, and a current limit of +/- 100 mA. To suppress a 2.4 volt peak-to-peak ripple voltage, a turns ratio of 1:5 is selected. Given a 125 KHz fundamental ripple frequency, a magnetizing inductance of 5 µH is selected so that the current drive capability of the amplifier is not exceeded. The magnetizing inductance determines many of the characteristics of the transformer.

The transformer must be properly designed for the calculated magnetizing inductance, which depends on four parameters (as in an inductor): the number of turns (*N*), flux density (*B*), core area (*A$_c$*), and current (*I*).

$$L_\mu = \frac{NBA_c}{I} \qquad (2.3)$$

The number of turns, *N*, is determined by core characteristics. The saturation flux, *B*, and core area, *A$_c$*, is a factor of the type of core chosen and the material. The current, *I*, is given by the particular application (the maximum current should be used) and therefore is set. Although not represented in equation 2.3, window size is a very important parameter. All of the windings must be able to fit in the core. Each of these parameters are inter-related, thus a list of possible cores choices can be generated and evaluated for use.

The core material is selected in the second design step. It is determined by numerous factors; including cost, core loss characteristics, magnetic saturation limit, and permeability. Neglecting cost, high frequency core losses are the primary factor.

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Excessive core loss will generate heat and more importantly cause the transformer to greatly deviate from its ideal behavior. In the prototype, a 3F3-ferite core was selected for excellent performance at high frequencies. The core material in turn determines what flux will saturate the material (B_{sat}). As the flux in the core approaches B_{sat}, the permeability decreases, the inductance decreases, and the core losses increase. Therefore, the transformer should be designed to operate less than the saturation flux density. The prototype has been designed with a B_{max} of 0.3 T.

From equation 2.3, having determined B_{max} and I a list of cores can be generated by varying N and A_c. The number of turns, N, and core area, A_c, is not completely independent. The core size if determined by numerous factors, one of which is window size. The window size must be able to accommodate both the primary and secondary turns. The size of the wire is determined by the amount of current that the wires carry. As a rule of thumb, the maximum current density should not exceed 500 A/cm^2. Otherwise, there will be excessive losses and heating due to the resistance of the wire. The prototype system has a maximum of 14 A through the primary and 100 mA through the secondary. Therefore, 14 awg wire is used for the primary and 22 awg wire for the secondary (wire data is readily available [14]). The minimum window area needed is the number of turns of the primary wire times the cross-sectional area of the primary wire plus the number of turns of the secondary wire times the area of the secondary wire, all multiplied by a factor to account for the limited packing factor of wire in the window. As a rule of thumb, the total wire cross-sectional area should be multiplied by a factor of 1.5 to 2 to get the required window area; again, packing factor estimates are available [14]. By searching through a list of available core areas, a list of corresponding number of

turns, N, is determined. A set of viable cores is narrowed from this larger list by checking if all the windings are able to fit in the core window. To fully determine the characteristics of a core the gap size needs to be extracted.

The maximum flux sets the gap size. The amount of flux through a core is dependent on the number of turns, current, core area, permeability, and mean core length. The core area, permeability, and mean core length can be incorporated into one parameter denoted as A_L, representing the number of nH per turn squared. Thus the flux is determined by N, I, and A_L. The flux B in terms of A_L is given below:

$$B = \frac{NIA_L}{A_C} \tag{2.4}$$

The B_{max} and I are predetermined and a set of A_c with corresponding N was found previously, thus A_L can be determined. This provides a set of possible cores with a given N, core area, and gap size. A_L and A_C are inter-related.

When selecting a particular core the tradeoff between gap size and core size must be considered. Equation 2.4 shows a couple of interesting relationships. For a given number of ampere-turns, the core area can be reduced if the B_{max} is increased. Alternatively, the core area can also be decreased if A_L is decreased. This has the downside of increasing the leakage inductance which has detrimental affects on the
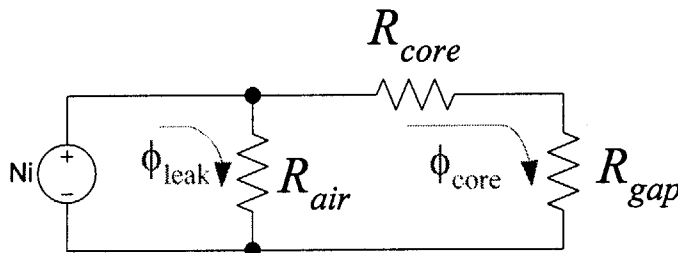
Figure 2.2 A magnetic circuit representation of leakage inductance in a transformer. Flux is represented by current and reluctance is represented by resistance. As the gap increases, the resistance increases and more flux will travel through the air, causing more leakage.

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system performance (discussed later). The increase in leakage inductance with reduced

A_L (and larger air gap) is illustrated by the magnetic circuit in Fig. 2.2. A_L is decreased by

decreasing the core permeability or increasing the air gap. As the gap increases, its

resistance to flux increases, therefore causing a larger percentage of flux to bypass the

core. Percentage leakage inductance is directly related to the fraction of flux that

bypasses the core. Given the relationships of the main parameters, tradeoffs between

different selections can be made.
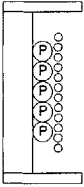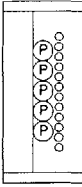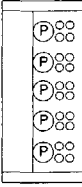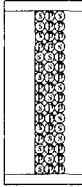
Leakage inductances in the transformer affect the controls of the filter and

therefore play an important part in the design. The use of feedforward ripple cancellation

requires that the ripple be both sensed and injected with great accuracy. Therefore, the

injector must have negligible magnitude attenuation and phase shift for the frequency

range of interest: any phase or magnitude error will greatly degrade the performance of

the feedforward control. The signal fidelity of an ideal transformer is perfect. However,

transformer parasitics [11,12] (illustrated in Fig. 2.3) can limit the injector performance.

Experimental results have verified that the primary-to-secondary shunt capacitance,

C_{shunt}, can be neglected for converters operating at up to several hundred kilohertz,

because it does not affect the behavior of the injector for the frequency range of interest.
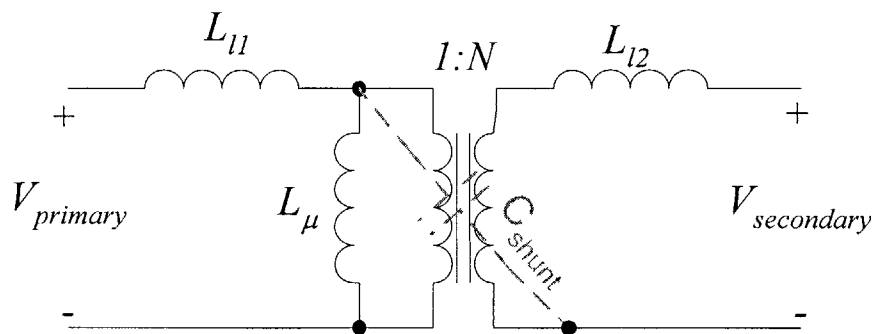
Figure 2.3 A transformer model including parasitics. The parasitics can cause magnitude and phase errors.

However, the secondary side (amplifier-side) leakage inductance, L_{l2}, forms a voltage divider with the magnetizing inductance reflected to the secondary side, resulting in a magnitude error. A transformer design that minimizes percentage leakage inductance is advantageous.

Leakage inductance also affects the stability of the feedback control. Stability is the major factor limiting achievable attenuation. The injector transformer is in the feedback loop, so any phase lag added by the transformer can greatly decrease stability. An ideal transformer adds zero phase lag, but the parasitic inductance on the primary side (injection), L_{l1}, plays a surprisingly important role in the stability of the system. As will be described in chapter 4, L_{l1} and the output capacitor, C_{out}, form a 2nd order low-pass filter, and the phase shift associated with this parasitic filter can affect the stability of the feedback control. As a result, the transformer design should also minimize L_{l1} to ease the constraints on the control design.

Topology	Primary Over Secondary	Secondary Over Primary	Interleaved Secondary Over Primary	Litz Wire
Description				
Manufacturing Difficulty	Low	Low	Medium	High
$L\mu$ (μH)	4.92	4.86	4.82	4.68
L_{l1} (μH)	0.13	0.12	0.04	0.07
L_{l2} (μH)	0.34	0.75	2.45	0.78

Table 2.1 Characteristics of different transformer winding topologies. The description row illustrates the winding geometry, showing half of the bobbin. The large circles represent the primary winding and the smaller circle represents the secondary.

It is advantageous for both feedforward and feedback control to minimize the

leakage inductances, which depends on two factors: winding geometry (as mentioned

above) and core gap length. Reducing gap size will reduce the leakage inductance, but

it substantially increases transformer size. For a given current, magnetizing inductance,

and maximum allowable flux density, there is a direct relationship between A_L

(inductance factor, nH/turns^2) and core area, A_{core}:

$$A_{core} = \frac{I_{\mu,max}\sqrt{L_\mu A_L}}{B_{max}} \tag{2.7}$$

A_L is inversely proportional to the gap length, which typically correlates with leakage

inductance. Thus, there is a tradeoff between the leakage inductance and the core size.

Leakage inductance can be further reduced by finding a beneficial winding geometry.

Various winding geometries are investigated in this thesis, bearing in mind the

constraint of manufacturing ease. Leakage inductance stems from imperfect coupling,

where the flux generated by one set of windings does not link the other set of windings.

Winding topologies that have the windings close together are advantageous. Topologies

where the windings are interleaved and placed on the same magnetic component are

Impedance at the primary side with the secondary side shorted	Impedance at the secondary side with the primary side open	Impedance at the primary side with the secondary side open
$Z_3 = L_{l2} + L_{l2}/N^2$	$Z_2 = L_{l2} + N^2 L_\mu$	$Z_1 = L_{l1} + L_\mu$

Figure 2.4 A method for measuring leakage inductance. Three measurements are made (as illustrated n the three columns). The magnetizing inductances and both leakage inductances can be estimated from these measurements.

investigated further. Table 2.1 illustrates the experimental evaluation of a number of possible winding arrangements. The winding geometries and corresponding leakage inductances are show. The leakage inductances can be calculated from various measurements on the primary and secondary side, as illustrated in Fig. 2.4. After comparing several geometries, while keeping implementation ease in mind, an interleaved primary over secondary winding method was selected for the prototype, as this resulted in a low value of L_{l2}.

Given these relationships various tradeoffs must be made in the core selection. For instance, the prototype injector could be implemented using a RM14 core with a relatively small gap and low leakage. Given the required primary side inductance and current following equations illustrate some of the previous tradeoffs:

$$L = A_L N^2 \tag{2.5}$$

$$L = \frac{A_{core}^2 B_{max}^2}{I_{max}^2 A_L} \tag{2.6}$$

A RM12/I core was selected with an area of 146 mm^2. A standard gapped core with an A_L value of 315 nH was chosen, resulting in four primary turns and twenty secondary turns. This results in a primary side leakage (L_{l1}) of 0.156 µH (3.4%). The secondary side leakage (L_{l2}) is 2.3 µH (2.5%). The corresponding attenuation of 0.98 is calculated from equation 2.4.

$$Attenuation = \frac{N^2 L_u}{L_{l1} + N^2 L_u} = \frac{V_{out}}{V_{in}} \tag{2.8}$$

To the extent that this attenuation is known and repeatable, it can be compensated for in the control design.

2.3 Two Magnetic Component Voltage Injector

An alternative method for implementing the injector is to use a bypass inductor in parallel with a high-frequency transformer, as illustrated in Fig. 2.5. In this approach, the bypass inductor, which is implemented with a gapped core and wound with large-gauge wire, serves as the dc bypass element. This function is accomplished by the magnetizing inductance L_μ in the previous case. The high-frequency transformer is implemented with a much smaller ungapped core using small-gauge wire. This element serves as the means for voltage injection. The relative winding resistances determine the dc current sharing between the inductor and the transformer, while the ac characteristics are determined by the relative inductances. This topology essentially de-couples the inverse relationship between leakage inductance and core size.

The design of the inductor and transformer is similar to the previous design of the transformer. In the bypass inductor implementation, the smallest core area should be selected because the inductor leakage inductance does not affect the filter performance. The transformer implementation is also the same except it must be implemented with an ungapped core to keep overall performance comparable to the single-core
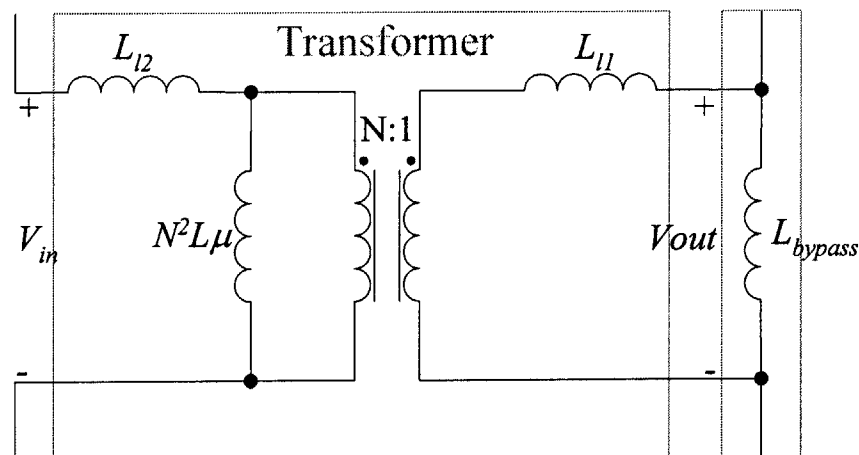
Figure 2.5 An injector implementation that uses a bypass inductor in parallel with a high-frequency transformer. The significant transformer parasitics L_μ, L_{l1}, and L_{l2} are also represented.

implementation. Furthermore, the magnetizing inductance must be at least ten times that

of the bypass inductor, which remains at 5μH. This is due to the AC performance; at the

frequencies of interest the parallel AC impedance of the bypass inductor and the

magnetizing inductance must equal 5μH. Once again the winding topology is important

in minimizing parasitic inductances[1] (see table 2.2), which affect performance. The

attenuation of the voltage injected with this approach may be calculated as:

$$Attenuation = \frac{N^2 L_u}{N^2 L_u + L_{l2}} \left(\frac{L_{DC}}{L_{l1} + L_{DC}} \right) = \frac{V_{out}}{V_{in}} \tag{2.9}$$

By minimizing the leakage inductances, L_{l1} and L_{l2}, the attenuation is minimized. It

should be noted that in the previous case, only L_{l2} caused a magnitude error in the

injected signal. In the two-core approach, L_{l1} also causes a magnitude error because it

forms a voltage divider with the bypass inductor. This approach can thus lead to a larger

magnitude error.

A prototype ac transformer (with a 50μH L_μ) was wound on a non-gapped RM5

core, while the bypass inductor (5μH) was wound on a gapped RM10 core. The

combined volume of the inductor and transformer is 4884 mm^3. The single-core design

has a volume of 8340 mm^3. The two-component approach thus yields almost a 50%

reduction in total volume. The ac transformer magnetizing inductance L_μ is *50 μH*, L_{l1}

leakage is 0.148 μH (or 0.4%) and the L_{l2} leakage inductance is 1.32μH (or 0.15%). This

is much lower than in the previous design. However, the attenuation is increased to 0.92,

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1 The previous method of measuring parasitic inductances is not accurate in this case. Due to the increase in
the number of turns, the shunt capacitance is larger. When the secondary side is shorted, a capacitive
component appears on the primary side impedance. The previous method assumes no capacitance. To
measure leakage, the attenuation from primary to secondary must be measured by driving the transformer

Topology	Primary Over Secondary	Secondary Over Primary	Interleaved Secondary Over Primary
Description			
Manufacturing Difficulty	Low	Low	Low
L_μ (μH)	38.83	41.36	48.23
L_{l1} (μH)	.15	2.75	-2.8*
L_{l2} (μH)	1.32	2.77	-1.06*

* Not a negative inductance. Due to measurement errors. Larger shunt capacitance affects measurement models.

Table 2.2 Characteristics of different winding topologies. The figures illustrate the winding geometry. (Half the bobbin is shown.) The primary and secondary wire sizes are the same. The primary is denoted with a P and secondary with a S.

as compared to 0.98 yielded by the single-core design. The example confirms a volume versus gain tradeoff with the two magnetic component implementation in comparison to the single magnetic component implementation.

2.4 Conclusion

Transformer based implementations are well suited to the design challenges of a voltage injector. A primary constraint is handling the large DC current in the system without significant dissipation. Two implementations were introduced that overcame this constraint. The first passes the DC current through the magnetizing inductance of the injection transformer. The second uses a discrete bypass inductor. The voltage injector must also isolate the active circuitry from the power system; transformers naturally achieve galvanic isolation. For control considerations, the voltage injector should have high

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with an AC source and measuring the open circuit secondary side voltage. Attenuation = $N*L_\mu/Z_2$; Z_1 and Z_2 can be measured from the method above.

fidelity. Different winding topologies are investigated to minimize parasitics that affect system operation. A simplified design procedure was introduced to design the proposed transformer:

Step1: Determine the desired voltage ripple to be canceled. Determine the maximum current and voltage of the active circuitry.

Step 2: Determine the turns ratios and inductance from equations 2.1 and 2.2.

Step 3: Select the core material base on individual constraints, including high frequency performance of the material. Material selection determines the maximum core flux.

Step 4: Use equations 2.5 and 2.6 (with the constraints of current, inductance, and maximum flux) to generate a list of possible core sizes, turns, and gap sizes. With the relationship of gap size (and hence core size) and transformer leakage inductance in mind, select an appropriate core.

Step 5: Choose a winding topology that will minimize parasitic leakage inductances. A few geometries with representative results are given.

3.1 Introduction

The design of the active circuit is greatly dependent upon the frequency band over

which the active filter must operate. For a dc/dc converter, the frequencies of interest

include the fundamental switching frequency and beyond. Achieving significant

attenuation at very high frequencies (e.g., beyond 10 MHz) is difficult and is better

handled with purely passive attenuation. The example power converter considered in

this thesis has a fundamental switching frequency of 125 KHz. Therefore, its pass band

should include 100 KHz and beyond.

For a multi-stage amplifier implementation, minimizing the number of stages is

beneficial in terms of cost and reliability, and facilitates the design of the feedforward

and feedback controller. Feedforward control depends on the ability to amplify signals

with high fidelity. Each amplifier stage introduces noise and parasitic capacitance, which

distorts to the feedforward signal. The feedback controller needs to have a stable loop
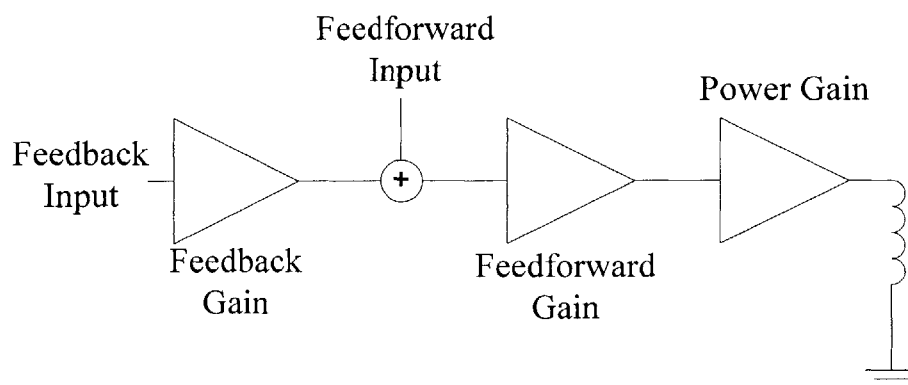
Figure 3.1 A block diagram representation of the multistage amplifier. A three-stage amplifier structure is employed, comprising a feedback stage, a feedforward stage, and an output (power gain) stage.

response. Adding additional stages adds gain, but at the penalty of adding poles due to both amplifier dynamics and parasitic capacitances between stages. These parasitic poles can contribute to phase shifts near the unity gain crossover frequency, hurting phase margin (stability). Thus, the design objective is to achieve the necessary gain and bandwidth using as few amplifier stages as is practical. The design considered here is implemented with a three-stage amplifier structure: a power gain stage, a feedforward stage, and a feedback stage (see Fig 3.1). A high-speed buffer, LM6121, is used to implement the power gain stage. It is able to provide +/- 100 mA of current with +/- 6 volt output swing at a bandwidth of 50 MHz. This particular component was chosen because of its large bandwidth. Smaller bandwidths would lead to distortion caused by the dominant pole.

3.2 Feedforward Control Implementation

To obtain a three-stage design, the feedback-summing junction and the feedforward gain stage, illustrated in Fig. 3.1, are combined. The feedforward controller must be implemented with exact gain, minimal phase shift, and low distortion over the frequency range of interest. The desired gain of the feedforward path is equal to the injector turns ratio divided by the attenuation caused by the transformer parasitics:

$$Gain_{single} = \frac{N^2 L_u + L_{l1}}{NL_u} \tag{3.1}$$

$$Gain_{two} = \frac{N^2 L_u + L_{l2}}{NL_u} (\frac{L_{l1} + L_{DC}}{L_{DC}}) \tag{3.2}$$

This way, the feedforward gain can be used to compensate the magnitude error due to transformer attenuation. In the prototype system, the single-core injector transformer
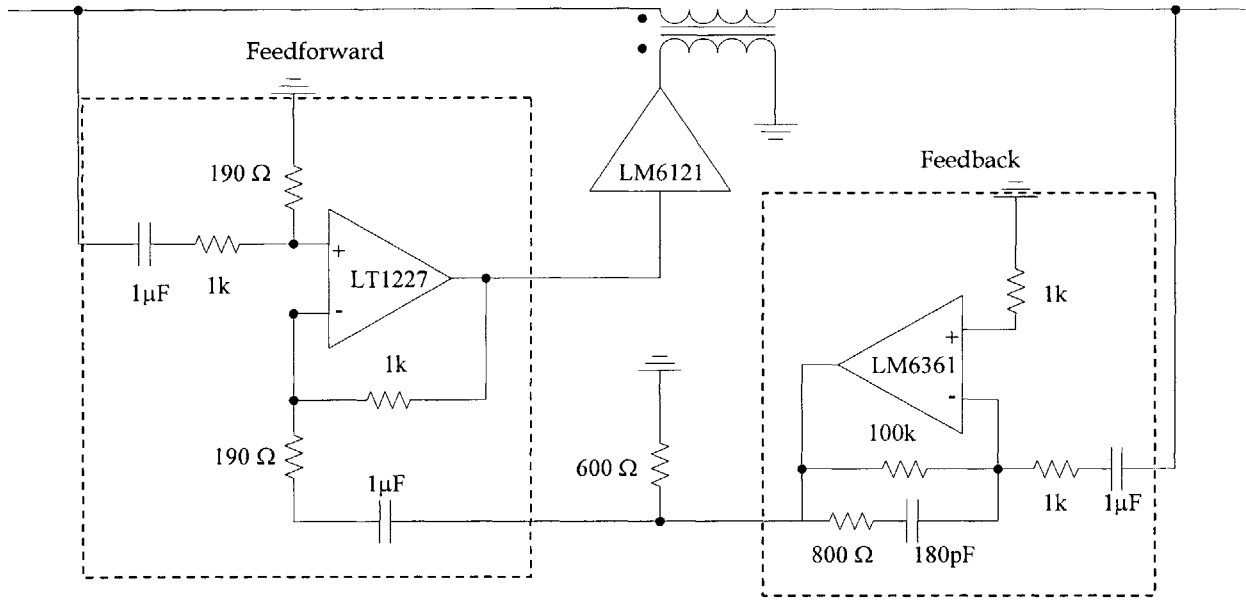
Figure 3.2 A three-stage amplifier implementation of control. (From top to bottom and left to right.) The first stage provides the power gain to drive the injector transformer. The second stage serves as the feedforward gain and the summing point for the feedback control. The last stage is the feedback gain with minor-loop compensation.

requires a feedforward gain of 5, while the two-component injector requires a gain of 5.2, since its attenuation is larger. It is important to note that manufacturing variations can make this gain compensation challenging, particularly for the two-component implementation. The prototype amplifier design, illustrated in Fig. 3.2, uses readily available discrete components.

3.2.1 Design of Summing Amplifier Using a Current Feedback Op-Amp

A current-feedback op amp is used for the feedforward gain because it achieves the necessary gain, bandwidth, and slew-rate requirements for this application. The feedforward op amp also acts as a summer, which allows this stage to incorporate the feedback control signal. Current feedback op amps offer several advantages over the traditional voltage feedback op amps, but the design is more constrained. First, current feedback op-amps do not have a gain-bandwidth product limit. In other words, the -3 dB

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point does not vary much as the closed loop gain is varied, unlike voltage feedback op-amps in which bandwidth decrease with an increase in closed-loop gain. Second, current feedback op-amps typically have a larger slew rate. These advantages come with the penalty of an increase in design difficulty. Therefore, the use of these op-amps in the prototype is limited to basic gain configurations using a purely resistive feedback loop. Capacitive feedback networks are possible, but the compensation is difficult. A further constraint requires the feedback resistor to be set by the capacitance in the load of the current feedback op-amp. Although there is no gain-bandwidth limit, the bandwidth is slightly degraded with increasing gain. Thus, in the stage which combines the feedforward and feedback signals it is advantageous to make the gain for feedforward and feedback signals the same (equal to the desired feedforward gain); a separate gain stage will be added for the feedback control.

Several basic op-amp summing topologies are available for the stage which combines the feedback and feedforward control signals. Possible configurations include a: non-inverting summing amplifier (eqn 3.3), inverting summing amplifier (eqn 3.4) or a difference amplifier (eqn 3.5) (see Fig 3.3).

$$V_{out} = (\frac{R_f}{R} + 1)(\frac{R_{feedback}}{R_{feedback} + R_{feedforward}} V_{feedback} + \frac{R_{feedforward}}{R_{feedforward} + R_{feedback}} V_{feedforward})$$ (3.3)

$$V_{out} = \frac{R_f}{R_{feedback}} V_{feedback} + \frac{R_f}{R_{feedforward}} V_{feedforward}$$ (3.4)

$$V_{out} = (\frac{R_{feedback}}{R_2})(\frac{R_{feedforward}}{R_{feedward} + R_1}(1 + \frac{R_{feedback}}{R_2})V_{feedforward} - V_{feedback})$$ (3.5)

Each of these topologies has its limitations. In the non-inverting configuration, the loop gain, which affects the bandwidth, is set by the R_f term. From eqn 3.3, the loop gain of

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the op-amp is attenuated by the feedforward and feedback resistors; therefore the loop

gain needs to be larger for a given gain. Increasing the loop gain will decrease the

bandwidth. For the inverting configuration, the feedback and feedforward resistor is set

by R_f for a given gain. Thus the input impedance for both the feedforward and feedback

path is constrained to a relatively low value. For the prototype system, a difference

amplifier is implemented. The difference amplifier allows the feedforward and feedback

gain to be equal with out attenuating the loop gain. Although the feedback input

impedance is set by R_f, this configuration allows the feedforward input impedance to be

set independently. This topology is advantageous because it provides this extra degree of

freedom.

3.2.2 Design Procedure

The design procedure for the difference amplifier is as follows: The first step is to

determine the load capacitance of the difference amplifier, which corresponds to the input

capacitance of the power gain stage and parasitic capacitance. This capacitance

determines the value of feedback resistor. The estimated input capacitance of the

LM6121 power gain amplifier is about 3.5 pF. The number is rounded up to about 10 pF,
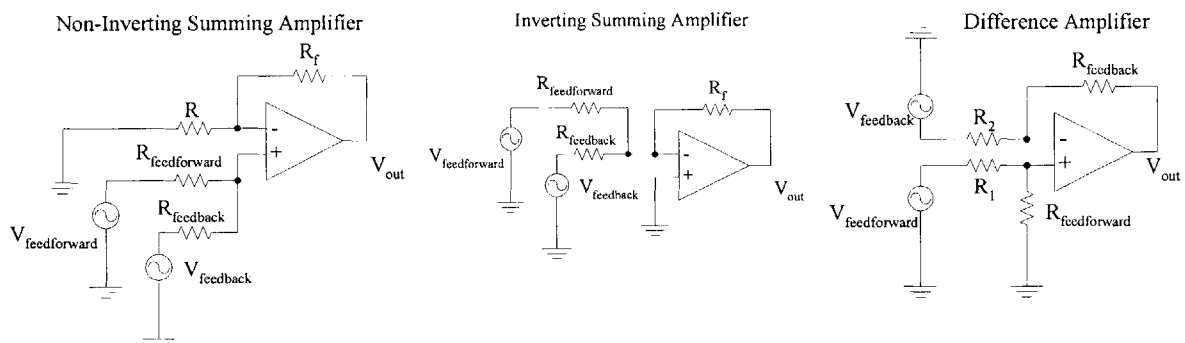
Figure 3.3 Various summing topologies (from left to right): non-inverting summing amplifier, inverting summing amplifier, and difference amplifier. In the non-inverting configuration the bandwidth is reduced. The inverting summing amplifier has low input impedance. The difference amplifier has low feedback input impedance.

to account for board and layout capacitance. From the data sheet, this results in a 1K feedback resistor.

Next, the feedback resistances can be determined, which affect the input impedances of the difference gain block. The input impedance for the feedforward input is $R_1 + R_{feedforward}$. The input impedance of the feedback stage is R_2. The input impedance of the feedforward signal determines the size of the capacitance needed to sense the signal; more will be mentioned about this later. The prototype uses the minimum feedback resistance of 1K. Therefore R_1 and R_2 are 190 ohms; and $R_{feedback}$ is 1K.

Finally, care must be taken to ensure that the power supplies are stiff. In other words, the amplifier power supply voltages must be constant with varying signal amplitudes and frequencies. This can be easily accomplished by placing decoupling capacitors across the power supply very close to the amplifier. In the prototype a large-valued tantalum capacitor is used in parallel with a small ceramic capacitor.

3.3 Feedforward Control Analysis

There are two main limitations that dominate the feedforward system: non-exact gain compensation and nonzero amplifier output resistance. Due to parameter variations of the inductor and transformer, the feedforward gain cannot completely compensate for the magnitude error. Assuming zero phase error, the percentage error in magnitude corresponds directly to the percentage of residual ripple. For example, a 10% magnitude error results in a 10% residual ripple. The phase error is also proportional to the residual ripple. The nonzero output impedance of the power gain stage, R_{out}, causes a phase error, because it forms a high pass filter with the magnetizing inductance on the secondary side of the transformer (see fig 3.4):

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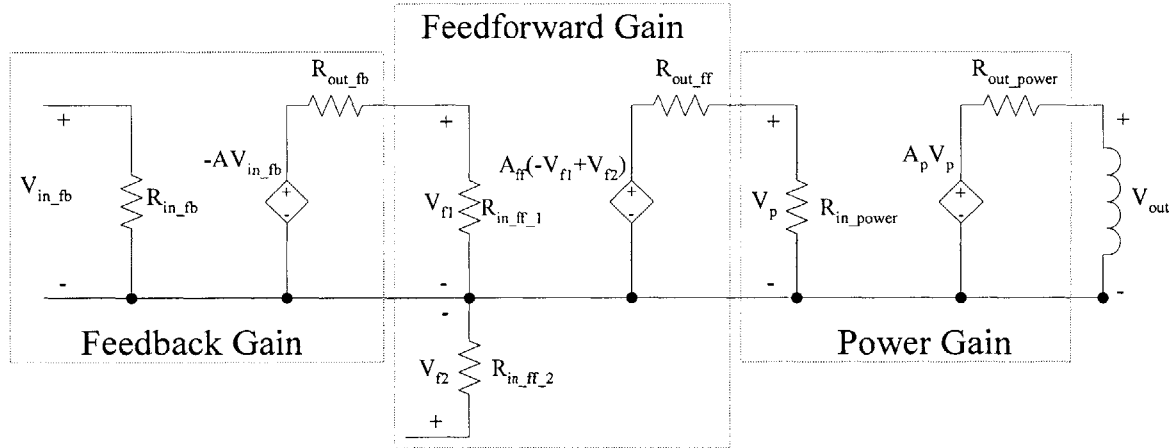
Figure 3.4 The three stage amplifier with input and output impedances. There is a significant voltage divider between the feedback gain and the feedforward gain stages. A high pass filter is formed at the output.

$$\frac{V_{transformer}}{V_{circuit}} = \frac{sN^2 L_u}{R_{out} + sN^2 L_u} \tag{3.6}$$

For perfect gain, the percent residual ripple depends on the phase error ϕ in the following manner:

$$\%V_{residual} = 100 * \sqrt{(1 - \cos\phi)^2 + \sin^2\varphi} \tag{3.7}$$

The pole associated with the output resistance and magnetizing inductance is at 6.4 KHz in the prototype. Although it is well below the fundamental frequency, there is a slight phase shift of three degrees at the switching frequency. This results in a maximum 95% ripple cancellation by the feedforward system, as per eqn 3.7. The corresponding
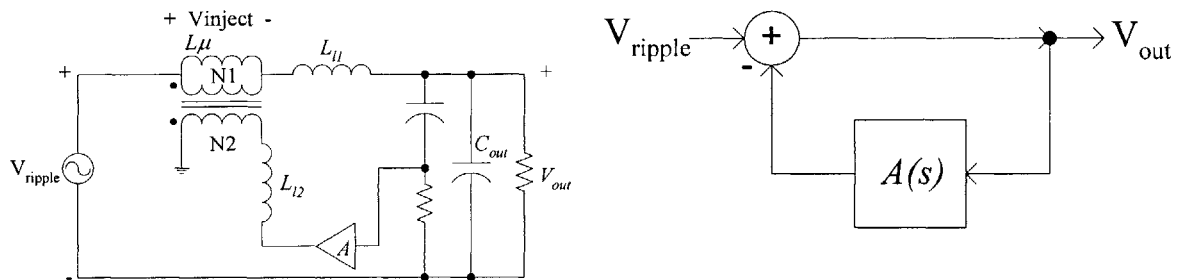
Figure 3.5 The left diagram shows the circuit representation of the feedback loop. The diagram on the right depicts a block representation of the proposed feedback loop. The performance of the feedback controller is directly proportional to the gain, $A(s)$.

magnitude error is negligible given knowledge of the transformer parasitics. Therefore it

is these errors in magnitude and phase that prevent perfect ripple nulling.

3.4 Feedback Controller

Figure 3.5 shows the proposed feedback system. The design of the feedback

controller is not only dependent on the switching frequency, but also on the stability of

the control loop. The effectiveness of feedback control is directly dependent upon gain.

Thus maximizing gain, without instability, is most desirable. As mentioned in section

2.2, the injector transformer leakage inductance L_{ll} and the output capacitor C_{out} form a

low-pass filter, illustrated in Fig. 3.6. This two-pole filter causes an additional -180

degree phase shift from V_{inject} to V_{sense}. Neglecting damping and assuming that the buck

capacitor is nearly ac ground, the following equation gives the transfer function from the

injected voltage to sensed voltage:

$$H_{injector}(s) = \frac{V_{sense}(s)}{V_{inject}(s)} = \frac{-1}{1+(L_{ll}C_{out})s^2} \tag{3.8}$$

The higher the unity-gain crossover frequency of the loop gain, the larger the attenuation
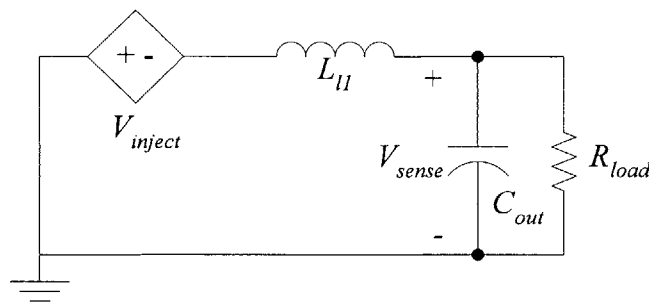
Figure 3.6 A circuit represention of the voltage injector loaded with the output capacitor. The voltage source represents the injected signal on the voltage transformer internal to the leakage inductance. To simplify the analysis the buck capacitor and the damping due to R_{load} has been neglected. The feedback signal is sensed across the output capacitance.

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will be across the frequency range of interest. However, if the −180 degree phase shift

occurs at or before the unity-gain crossover, then the system will be unstable. The

parasitic low-pass filter in the prototype occurs at around 1.5 MHz, therefore restricting

the gain across the frequencies of interest, in this case from 125 KHz to 1MHz.

The narrow frequency range is insufficient for this application. To overcome this

limitation, a small inductive element, L_{comp}, is added between the sense point and the

load, see Fig. 3.7. In the prototype system this was implemented as a small magnetic

bead. This results in the addition of two zeros after the two poles:

$$H_{comp\_inj}(s) = \frac{V_{sense}(s)}{V_{inject}(s)} = \frac{-(L_{comp}C_{out})s^2 - 1}{s^2(L_{comp} + L_{l1})C_{out} + 1} \tag{3.9}$$

If L_{comp} is much smaller than L_{l1} then the zeros occur just after the poles. Therefore the

phase of the system approaches −180 degrees (never reaching it due to damping) and then

returns to zero degrees. Figure 3.8 shows the frequency response of $H_{comp\_inj}(s)$ for the

prototype system.

The attenuation of the ripple will be greatly degraded at the frequency where the

Figure 3.7   A circuit represention of the voltage injector loaded with the output capacitor and series compensating inductor. The voltage source represents the injected voltage. To simplify the analysis, the buck capacitor and the damping due to R_{load} has been neglected. The feedback signal is sensed between the two inductors.
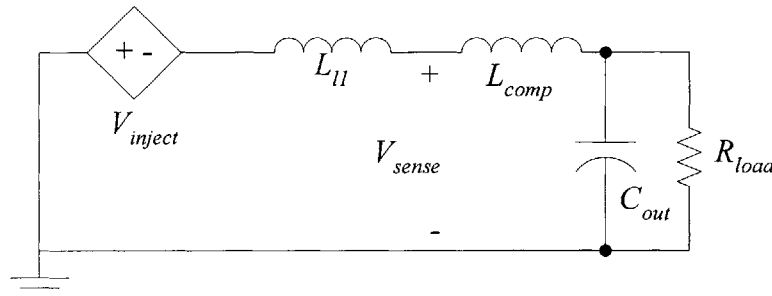
minimum of the magnitude response occurs. Furthermore, the ripple at this frequency is greater with feedback filtering than without. This is because not only is the magnitude at a minimum but the phase is nearly –180 degrees, which makes the gain, $A(s)$, a negative number less than one, thus causing the attenuation to become less than one. These poorly damped pole and zero pairs make the design of the feedback control loop difficult.

One solution is to add additional series or shunt damping. In either case, resistive damping needs to be added on the load side of V_{sense} of Fig. 3.7, thereby allowing a damping term for both the zero and the pole. A shunt damping leg is chosen for this particular application because it can be easily and inexpensively implemented with a

Bode Plot of Compensated Injector

Phase Response of Compensated Injector
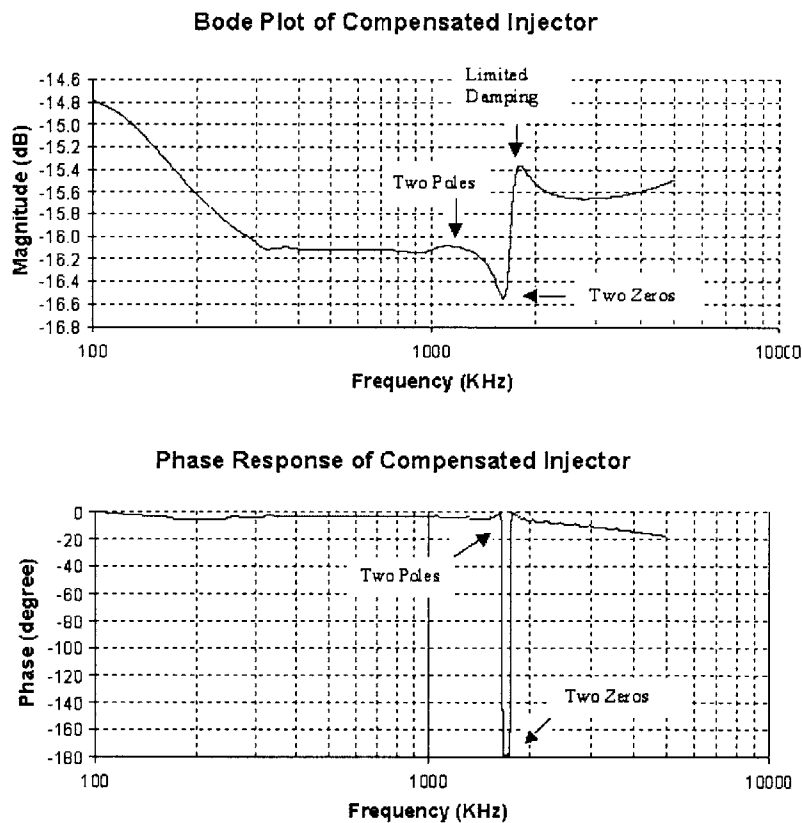
Figure 3.8 The transfer function from injected to sensed voltage. The two poles are due to the low-pass filter formed by $L_{ll}+L_{comp}$ and C_{out} adds a –180° phase shift. L_{comp} adds the two zeros and C_{out} brings the phase back to 0°. The magnitude shows peaking near the poles and zeros of the system, which is due to limited damping.

capacitor and resistor. Simulations demonstrate that a 1 μF capacitor in series with a 0.5 Ω resistor provides ideal damping. The implementation of the damping leg uses a 0.22 Ω resistor instead of a 0.5 Ω to account for the ESR of the 1 μF capacitor. A series damping topology would require an inductor in parallel with a resistor. The inductor would be required to withstand the large bias current, thus making it large. This problem is similar to the one faced in the design of the transformer. As will be discussed in the following chapter, both damping schemes can also be implemented with a simple active circuit.

3.4.1 Feedback Gain Amplifier

The feedback amplifier block needs to be designed with large gain and bandwidth, to maximize the effectiveness of the feedback controller. Furthermore, an op-amp with a basic, second-order frequency response with a dominant pole will facilitate the stability and compensation design. It is for this reason that a current feedback op amp was not chosen to implement the feedback block. The current feedback op-amp has a large, negative phase shift with small amplitude attenuation when it reaches its bandwidth. This particular response is indicative of either a time delay or a large number of poles at frequencies slightly beyond the -3dB bandwidth. A high-frequency voltage-feedback op amp, LM6361, is used for the feedback amplifier because it has a predictable attenuation and phase shift.

The overall topology of cascading the feedforward stage and the feedback stage

leads to a tradeoff between feedback gain and feedforward signal noise. This relationship

stems from the input impedance of the difference amplifier. The feedback gain block has

non-zero output impedance, which forms a voltage divider with the input impedance of

the difference amplifier as illustrated in Fig 3.4. The difference amplifier has relatively

small input impedance, 190 ohms, therefore the attenuation is significant. Thus the

maximum gain of the added feedback gain stage is limited, and consequently the gain of

the feedback loop is limited. Based on PSPICE simulations, the maximum open loop

gain in the proposed configuration is around 100. In order to increase the input

impedance the feedback resistor must be increased on the difference gain block. For

current feedback op-amps, this increases the noise in the signal. The added noise only
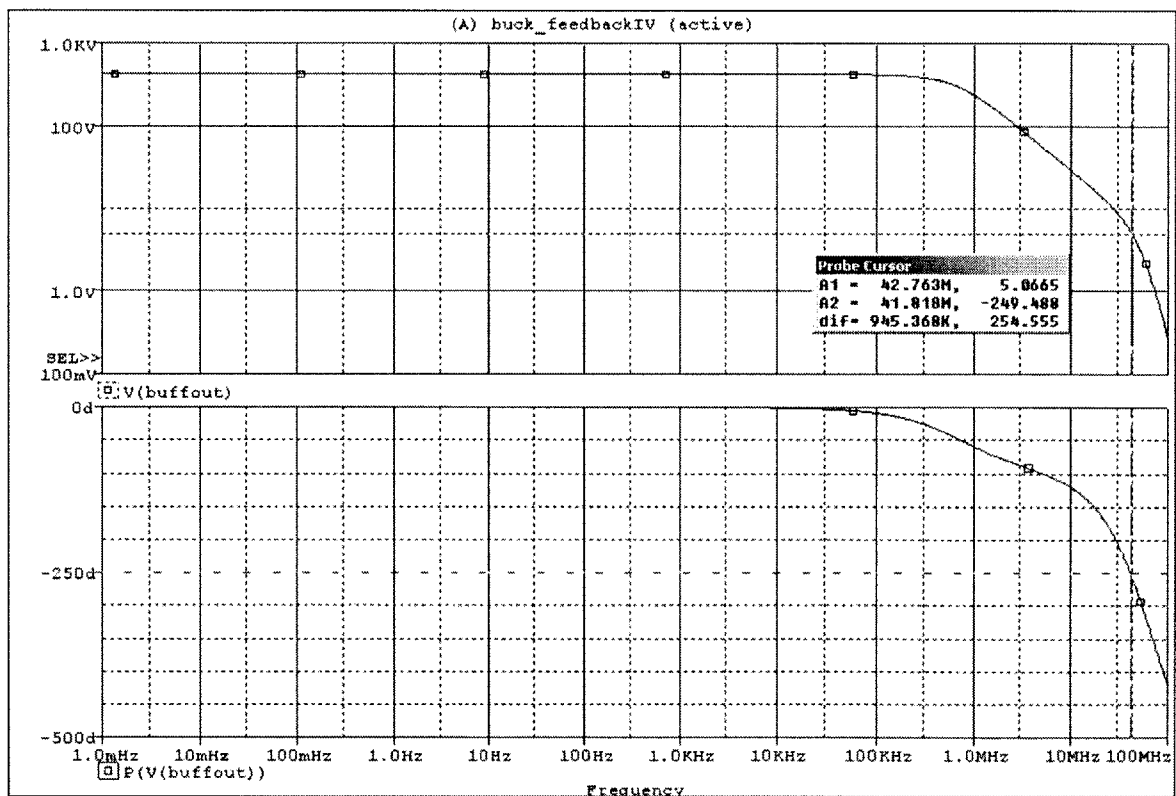
Figure 3.9 Simulation of the open loop frequency response of the multi-stage amplifier. The unity gain cross over of 42 MHz and phase of –250 degrees is shown.

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affects the feedforward controller because it relies on high signal fidelity. On the other

hand, the noise in the feedback control is reduced by the loop gain. Even with this

relationship, the cascade provides some advantages in minimizing the number of stages.

The prototype attempts to minimize feedforward noise and therefore has a maximum

overall feedback gain of 100.

3.4.2 Compensation Design Procedure

A compensator must be added to ensure feedback loop stability, which can be

implemented as minor loop compensation. Phase margin serves as a measure for the

degree of stability. Phase margin is defined as 180 degrees minus the phase at unity gain

cross over. As a rule of thumb, the phase margin should be at least 45 degrees.

Figure 3.10 (Clockwise from top left) Various compensation techniques. Gain Compensation. Lag Compensation. Lead Compensation. Minor Loop Compensation.

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The first step in selecting a unity gain frequency is to determine the frequency response of the open loop system. Assume for now that the transformer and output capacitor add no phase shift, so the phase is primarily due to the multi-stage amplifier. Any phase error due to the passive components can be accommodated by a larger phase margin. The frequency 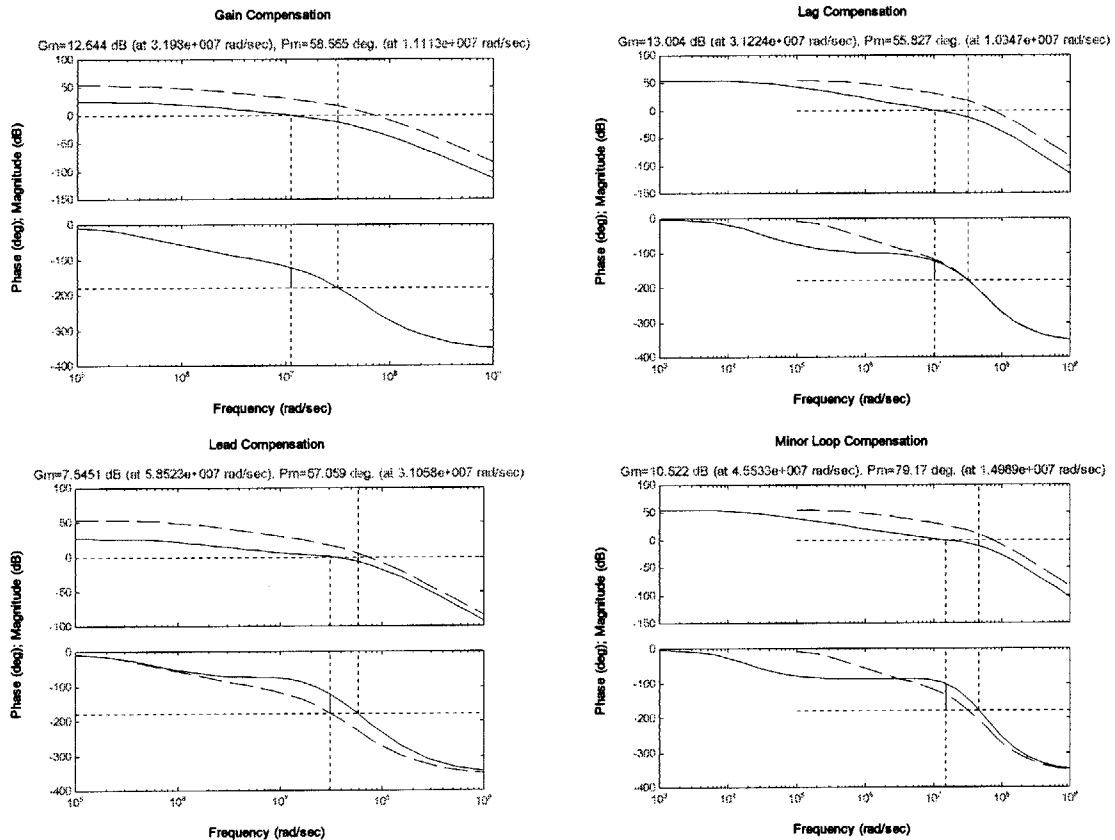response can be measured experimentally, simulated, or approximated from the data sheets. From simulations (see Fig 3.9), the unity gain frequency is around 40 MHz and has a phase of −250 degrees, which makes the closed-loop system unstable. The loop can be stabilized if the open loop gain is shaped by a compensator.

The next step is to select a compensation method that allows the system to meet the determined crossover frequency and phase margin. The feedforward gain stage, power gain stage, and the transformer have a combined gain of approximately one and marginal phase shift below 10 MHz. Therefore, the entire system will be stable if the feedback gain block is designed with a unity gain crossover of 10 MHz and a phase margin of at least 85 degrees (this is the phase margin of the feedback stage alone). After the unity gain frequency has been selected, the problem reduces to the compensation of a single op-amp. Below is a list of possible compensation methods and their tradeoffs, see Fig. 3.10:

Gain compensation – Reduce the gain across all frequencies without affecting phase

Advantages - Easy to implement

Disadvantages – Gain is reduced across the frequency range of interest.

Lag compensation – A zero is followed by a pole. The gain at frequencies beyond the pole is decreased allowing the frequency response to cross over sooner. The zero is added to offset the negative phase shift added by the pole.

Advantages – Only lose high frequency gain

Disadvantages – Adds a small amount of negative phase

Lead compensation – A pole is followed by a zero. Adds a phase bump.

Advantages – Increases the phase at crossover

Disadvantages – Increases the crossover frequency, which may affect high frequency noise.

As a rule of thumb, the maximum phase bump is around 60 degrees. Therefore, it may be
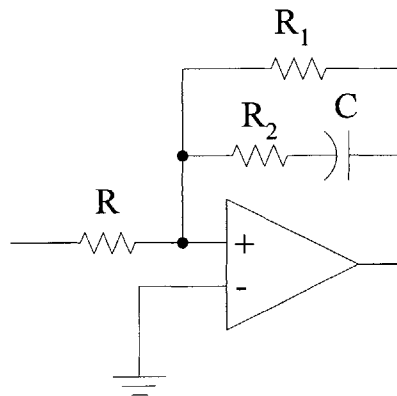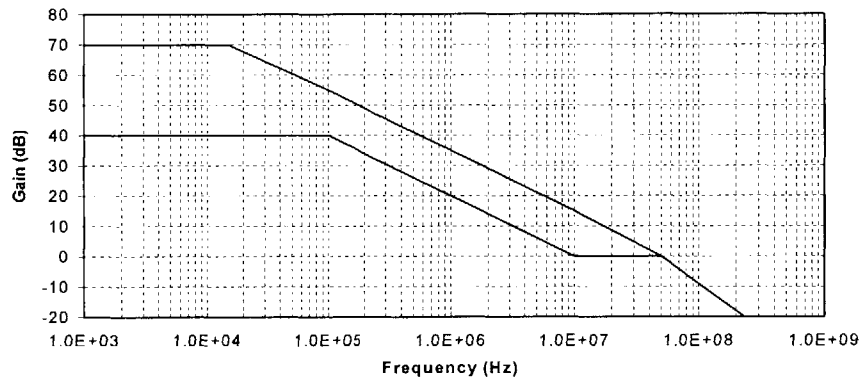
Figure 3.11 Op-amp implementation of minor loop feedback. The gain vs. frequency of the amplifier in open loop configuration verses minor loop configuration is shown.

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necessary to decrease the gain in order to meet phase margin specifications.

Minor loop compensation – Compensation is added to the feedback network of the op-amp.

Advantages – A combination of lead and lag compensation can be implemented

Disadvantages – More difficult to implement.

The prototype uses minor loop compensation. For minor loop compensation the

frequency response can be approximated by plotting the lower value of the open loop

transfer function and the feedback impedance. The feedback impedance has a resistor in

parallel with a series connection of a resistor and a capacitor (see fig 3.11). The impedance

has a zero followed by a pole. The lower curve has a pole followed by a zero followed by a

pole as the frequency increases (see fig 3.11). This forms a lag-lead compensator.

Intuitively, at lower frequencies the gain is set by R_1. As the frequency increases, the

capacitor impedance decreases, which causes the feedback impedance to decrease. Thus

the gain decreases. The minimum gain is reached when the capacitor shorts leaving R_1 in

parallel with R_2. As the frequency is further increased, the op-amp bandwidth is reached

and the gain is further reduced. The placement of the zero and pole are related. Placing a

zero right at the crossover frequency has the advantage of maintaining the crossover while

adding a slight phase bump. Knowing that the frequency response will crossover with a

slope of 20 dB per decade, the position of the pole can be determined. With a gain of 100

and a zero at 10 MHz the pole must be placed at 100 KHz (from eqn. 3.10)

$$\frac{\omega_{zero}}{\varpi_{pole}} = \frac{Gain}{Slope_{crossover}}$$

(3.10)

Equations 3.11 and 3.12 relate the pole and zero to the component values. The value of R_1

was determined by the maximum gain.

$$\frac{1}{R_1 C} = 2\pi\omega_{zero} \tag{3.11}$$

$$\frac{1}{(R_1 + R_2)C} = 2\pi\omega_{pole} \tag{3.12}$$

The component values used in the prototype are illustrated in Fig. 3.2.

With compensation and damping, the gain can be increased: the unity gain

crossover frequency extends past 1.5 MHz. The small ferrite bead (Fair-rite bead number

2673021801) used as the compensation inductance in the prototype not only adds the

needed inductance but extra resistive damping. This allows the unity gain frequency to

occur at 10 MHz. Minor loop compensation is used to further increase stability. The gain

of the prototype system is 50 at 125 KHz and decreases 20 dB per decade. Since the gain

is not infinite, the feedback controller is not able to completely eliminate the ripple.

3.5 Summary

The design of the feedforward and feedback controls is dominated by their

individual characteristics. In the feedforward case, the output signal must be precise. The

feedback controller must have large gain within the bounds of system stability. The design

considerations for each controller is based its respective single characteristic. The design

considerations for each of these stages have been considered in detail, and the design of a

prototype controller has been addressed.

4.1 Introduction

A lossless low-pass filter is easily implemented with an LC (inductor,capacitor)

filter, see Fig 4.1. These filters roll off at 40 dB/decade above the cutoff frequency (or

knee). The frequency response, shown in Fig 4.1, shows a large peak, which indicates that

the output of this filter will oscillate at that frequency. This resonance occurs when the

impedance of the inductor is equal to the negative of the impedance of the capacitor (occurs

at the corner frequency of the filter, $\omega = \frac{1}{\sqrt{LC}}$). The peaking can be reduced by adding

resistance to the filter, which provides damping. As illustrated in Fig. 4.2, either parallel or

series damping may be used. For parallel damping, the system becomes well damped for

damping resistances near to or less than the characteristic impedance in eqn 4.1, while for

series damping the system becomes well damped for resistances similar to or greater than
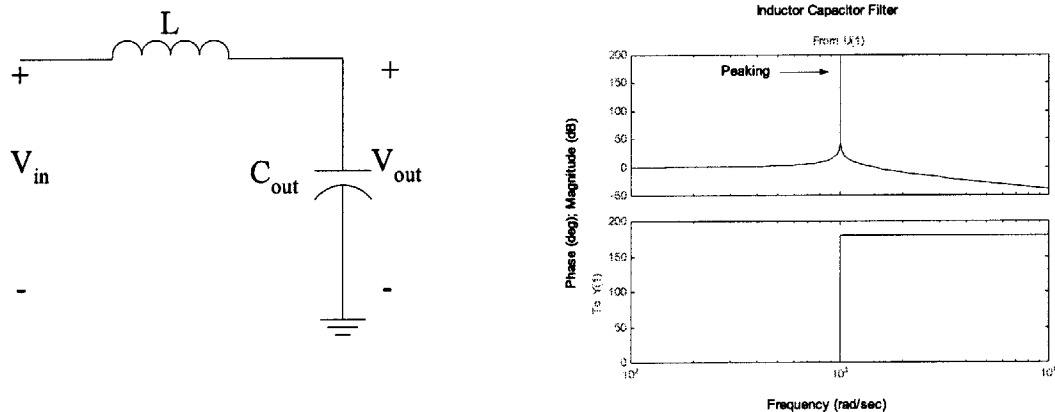
Figure 4.1 The figure on the left shows a standard L-section inductor capacitor filter. The figure on the right shows the frequency response of the filter. The peaking depicts the frequency in which the filter will oscillate. The larger the magnitude of the peaking the longer it takes the oscillations to die out.
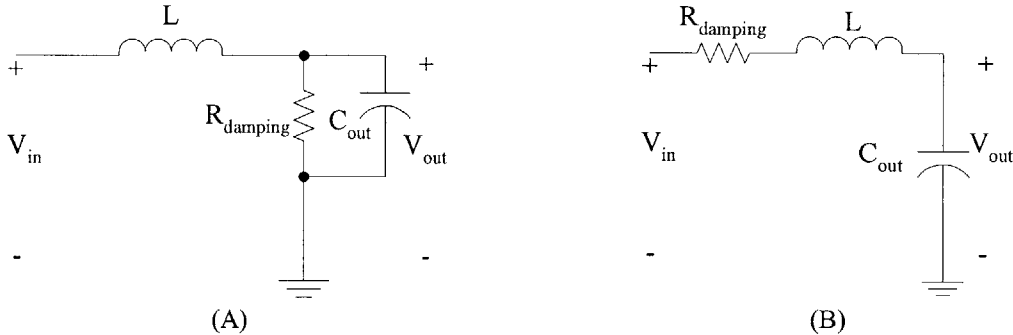
Figure 4.2 LC filters with passive resistor damping. (A) a parallel implementation. (B) a series damping implementation. The major drawback of these approaches is the dc power dissipation.

the characteristic impedance.

$$Zo = \sqrt{\frac{L}{C}} \tag{4.1}$$

One major drawback of this damping approach is the large dc power losses in the damping resistors. The DC losses can be eliminated by adding reactive components[1]. For example, in the parallel damping approach a capacitor is added in series with the parallel damping resistor to block the DC voltage. As illustrated in Fig. 4.3A, the damping leg capacitor must have substantially greater capacitance than the main filter capacitor, so that
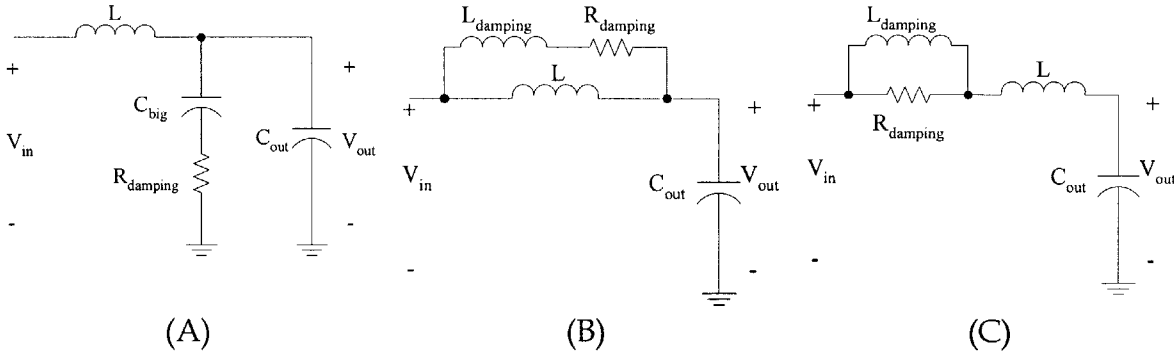
Figure 4.3 Figure (A) is a parallel damping scheme with a blocking capacitor to reduce DC losses. The Damping capacitor is an order of magnitude larger than the output capacitor. (B) Shows a series damping scheme with a parallel inductor, L, to reduce the DC losses. The filtering provided by L is degraded by the damping leg. (C) Depicts an alternative series damping topology. The damping inductor must be sized to handle the large DC current.

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the damping leg appears resistive at the corner frequency of the LC filter. Similarly, an inductance can be used to eliminate dc losses in a series path damping leg, as illustrated in Fig. 4.3 B, 4.3C. In all cases, the reactive damping components need to be sized so that the damping leg impedance is resistive at the corner frequency of the LC filter. Therefore, the sizing of the reactive damping component is a major design constraint.

The passive components used for series and shunt damping schemes can be larger than the filter elements themselves. Thus, active damping techniques are an attractive approach for reducing passive component size. Active circuity can be applied to both the series and parallel damping configuration. A series damping element can be implemented with a transformer in conjunction with a gain stage [13], see Fig. 4.4. Since the damping element must lie outside of the feedback loop, the injection transformer (in the active filter system of chapter 2-3) cannot be reused for this purpose. Hence, the series damping topology was not chosen for the filter considered here due to its complexity and its need to place an additional transformer in the dc power path. The parallel damping configuration

$$Z_{eq} = Ls \parallel A(s)$$

(A)   (B)   (C)
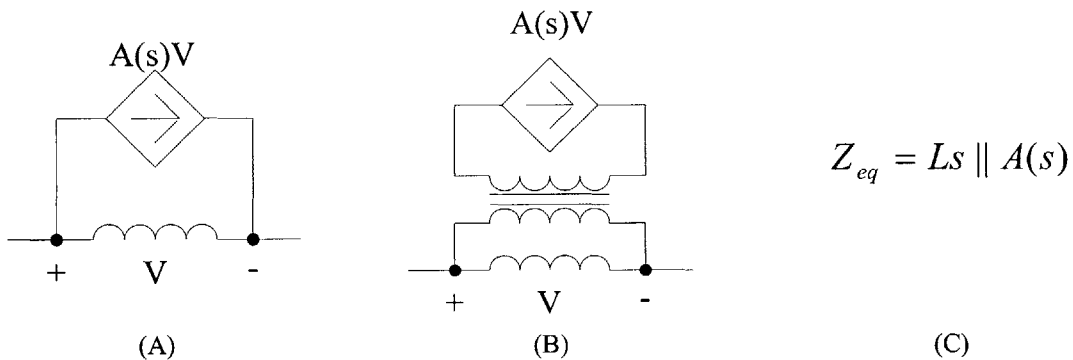
Figure 4.4 One possible series damping implementation. (A) shows a current source in parallel with a voltage-controlled current source. (B) shows a transformer implementation of the voltage controlled current source. The magnetizing inductance of the transformer serves as the by pass inductor. (C) is the equivalent impedance of the damping configuration.

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does not have the difficulty of dealing with the dc current.

An active parallel damping topology uses a capacitance to limit the dc power dissipation. Essentially, an active shunt damping scheme requires a topology where the damping capacitor is enhanced. Just as with active ripple filters, this can be accomplished in a variety of topologies: current-sense/current-drive, voltage-sense/current-drive, current-sense/voltage-drive, and voltage-sense/voltage-drive. The above topologies rely on feedback control to enhance the capacitor. Hence, careful consideration must be given to closed loop stability. The implementation must take care to minimize the number of poles and negative phase shifts near the unity gain crossover. Similar to the previous feedback design, minimizing the number of active gain stages is desirable. Therefore, the active damping circuit considered here uses a single gain stage.

4.2 Active Damping Design Considerations

The thesis introduces the current-sense/current-drive active damping circuit illustrated in Fig. 4.5(b). A single transistor topology allows for implementation ease and
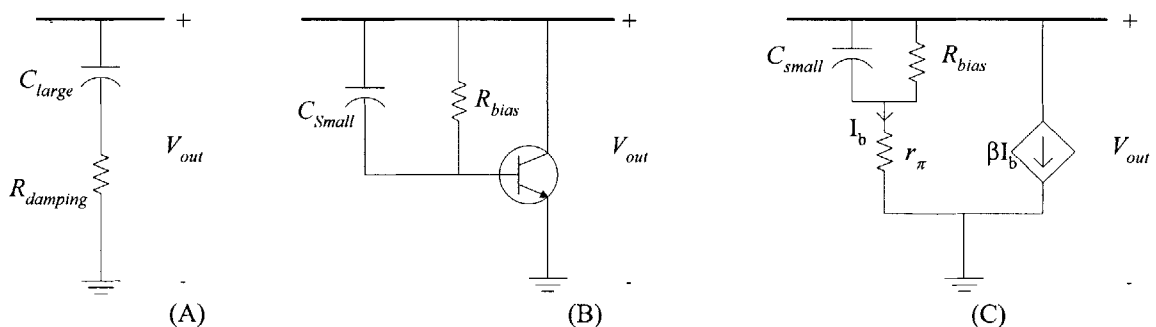

Figure 4.5 (A) A conventional passive shunt damping circuit. (B) The proposed active damping circuit. (C) A small-signal model of the active damping circuit. The transistor allows C_{small} to replace C_{large}, since the current that flows through C_{small} is magnified by the beta of the transistor. The input resistance r_{Π} of the transistor serves as the damping resistor.

loop stability. In this topology, the current that flows into through the capacitor C_{small} is

amplified by a current gain, β. Fig. 4.5(c) shows the small-signal model of the transistor

input resistance r_π is in series with the capacitor C_{small}. The effective shunt impedance thus

becomes:

$$Z_{equivalent} = \frac{R_\pi + \dfrac{1}{sC_{small}}}{\beta + 1} \tag{4.2}$$

The overall impedance is reduced by $\beta+1$. In other words the capacitance in increased by

$\beta+1$, thus $C_{eq} = (\beta+1)C_{small}$ and $R_{eq} = r_\pi/(\beta+1)$.

The single transistor implementation guarantees the stability of the closed loop.

Assuming that the inductor is an open circuit at the frequencies of interest, the open loop

frequency response contains one zero and two poles, see Fig 4.6. The phase shift of this

system will never reach 180 degrees. The frequency response can be approximated by

equation 4.3 based on the assumption that $R_{bias} \gg R_\Pi \gg R_{load}$ and $C_{load} \gg C_{small} \gg C_\Pi$.
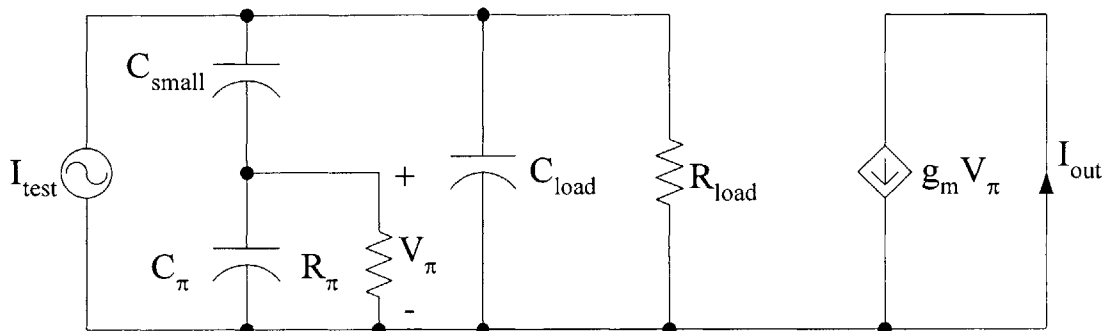
Figure 4.6 Open loop model of active damping circuit. The relevant parasitic transistor capacitacnces are shown; along with the load capacitor and resistor. At low frequencies the gain of the circuit is small. The gain increases in the midrange frequencies. As high frequencies the gain decreases again. At high frequencies the system behaves like a single pole topology.

$$\frac{I_{out}}{I_{test}} = \frac{\dfrac{R_\pi}{R_{bias}} R_{load} (1 + sR_{bias} C_{small}) g_m}{s^2 R_{load} R_\pi C_{load} C_{small} + s R_{load} C_{load} + 1} \tag{4.3}$$

If the C_{small} is made too large, complex conjugate poles will result, which caused peaking in the frequency response of the system, the very thing that the active damping system attempts to remove. Equation 4.4 constrains the maximum value of C_{small} to:

$$C_{small} < \frac{R_{load} C_{load}}{4 R_\pi} \tag{4.4}$$

Meeting this constraint on C_{small} will ensure that the feedback loop is unconditionally stable.

The first step in active damping design is finding the bias current. I_c is a major design parameter, and determines the damping resistance of the proposed single transistor implementation. The effective damping resistance is approximately $1/g_m = V_t/I_c$. This sets the bias current requirement I_c of the transistor, and the dissipation. Simulations can readily show the needed damping resistance. It reveal that 0.6 ohms is the largest resistance acceptable for a fair amount of damping. Thus the G_m must be 5/3, which require about 45mA of bias current, I_c.

Determining the capacitance is the second step, which depends on the corner frequency of the LC filter. In this system experimental results reveal that the corner frequency is around 800 KHz. The damping capacitor, C_{small}, shorts the base and collector together; therefore making the impedance of the damping leg equal to the damping

resistance. The frequency at which this occurs can be approximated by open circuit techniques. Essentially, this frequency is approximated by an RC time constant. The resistance that C_{small} sees is equal to:

$$R_{bias} \parallel R_{\pi} + G_m R_{load} (R_{bias} \parallel R_{\pi}) + R_{load} \qquad (4.5)$$

The prototype uses a 1nF capacitor for C_{small}, which must not exceed the capacitance specified by Eqn. 4.4.

The next step is to choose the needed transistor. Power dissipation limits the maximum bias current, I_c. Assuming that the bias current dominates the output signal current, the power dissipation of the damping circuit is the bias current times the dc bus voltage. The amount of power dissipation determines the type of transistor needed and the heat sink. The dissipation limit of a transistor is readily available from the data sheet. For instance, a TO-92 package has a maximum power dissipation of 0.82 watts at an ambient temperature of 25°C. For the prototype, the power dissipation is about 0.65 watts. Since damping is required for only lower frequencies (e.g. the corner frequency of the LC filter), a low-end transistor will suffice. This particular implementation uses a 2N2219 transistor with a beta of about 100. A 50 kΩ resistor is employed to bias the transistor into the linear region. The package is more than sufficient in handling the power dissipation requirements.

4.3 Design Procedure

Step 1: Find the damping resistance. Use simulations or calculations to determine

the maximum resistance allowable to damp the LC network. This resistance

corresponds to the $1/G_m$ of the transistor amplifier.

Step 2: Find the damping capacitance needed. Again, use simulations or

calculations to determine the minimum capacitance required to enable

sufficient damping. The capacitance found corresponds to the β times C_{small}.

Step 3: Check the power dissipation of the circuit. If it is too large then decrease the

bias current and increase C_{small}.

Step 4 Check the frequency response of the damping circuit. C_{small} must be less

than the value specified by equation 4.4. If it is too large, then decrease

C_{small}, increase the bias current, and change the type of transistor packaging

(or add a heat sink).

4.4 Initial Test Results

T he initial test results show that the active damping leg performed comparably to

the passive damping leg around the corner frequency of the LC filter (see Fig 4.7). For

frequencies below the knee, less than 200 kHz, the active damping leg has a larger

impedance than the passive damping leg. This is also true of frequencies greater than the

corner frequency, above 3 MHz. The performance of the active damping leg for

frequencies above and below the corner frequency is inconsequential to its overall

performance. The only thing that matters is its performance at the frequency of the knee of

the LC filter. Experimental results show similar performance over this region. Therefore

the active damping leg is comparable to a passive damping leg implemented with a 0.22 Ω

resistor and a 1μF capacitor.

4.5 Summary

Active circuits can be used to reduce the size of capacitors in shunt damping legs.

In a passive design, damping capacitors are typically an order of magnitude larger in

capacitance than the main capacitor. There are various feedback topologies available for

active damping; the one investigated here senses current and injects current. A

straightforward single-transistor implementation is possible in this case that achieves
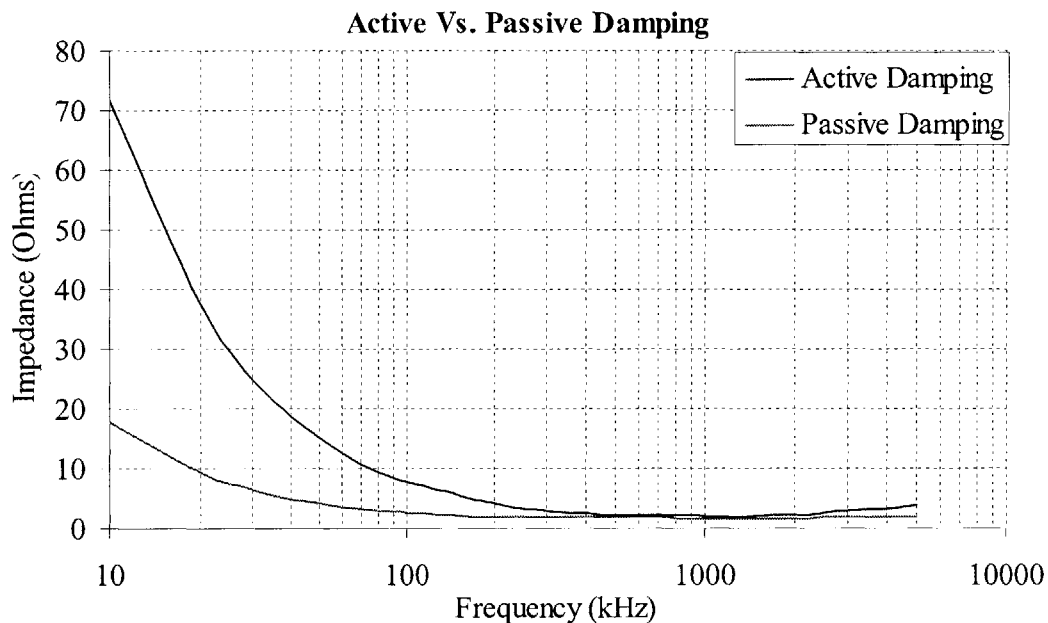
Figure 4.7 Shows a comparison of impedances between the active and passive damping topologies. The performance of the damping leg is only affected by its behavior at the frequency of interest. This corresponds to the knee of the LC filter. For this system it is around 800kHz. For the frequency of interest, the active damping leg is comparable to the passive damping leg. The passive damping leg has a lower impedance above and below the frequency of interest.

adequate performance and stability. In the topology, the bias current determines the

damping resistor. The maximum current is constrained by the power dissipation.

Furthermore, the reduced capacitor must be large enough to damp at the knee of the filter,

but if the capacitor becomes too large then the active damping feedback loop develops

peaking. The substantial reduction in capacitance that is achieved comes with the cost of a

slight increase in power dissipation.

5.1 Introduction

This chapter presents the experimental evaluation of the proposed active filter

technique in the output filter of a dc/dc converter. The effectiveness of the active

circuitry is evaluated in detail. In addition, it is compared to entirely passive filters

having the same size and ripple performance.

5.2 Test Setup

The proposed hybrid passive/active filter technique has been applied to the design

of an output filter for a 230 watt buck converter operating at 14 V output from a 42 V

nominal input (Fig. 5.1). The fundamental switching frequency is 125 KHz. The buck

converter power stage utilizes a 1.4 µH inductor and 20 µF primary output capacitor and

operates in discontinuous conduction mode under average current mode control. The

primary inductor and capacitor of the buck converter must remain as passive components,

since the magnitude of the current ripple in the primary filter stage is too large for the
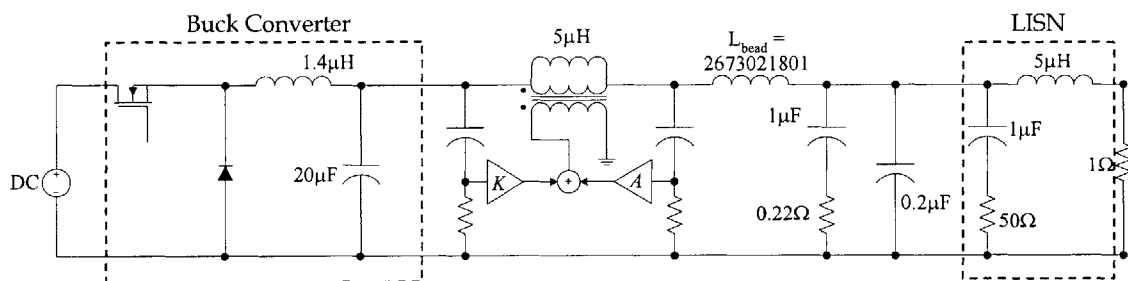
Figure 5.1 The test setup for the hybrid filter. The active filter is used in conjunction with a small passive output filter. The output filter consists of a 0.2 µF capacitor in parallel with a damping leg comprising a 0.22 Ω resistor and a 1 µF electrolytic capacitor.

active techniques considered in this thesis. Instead, active filtering is applied to the secondary filter stage, where the ripple is still above EMI specifications but within the realm of the power limitations of the active component.

A structural view of the output filter and test setup is shown in Fig. 5.1. The passive components of the hybrid filter comprise a 0.2 µF ceramic capacitor and a damping leg made up of a 1 µF electrolytic capacitor and a 0.5 Ω resistor. As described previously, this passive damping leg can be replaced with an active circuit and a significantly smaller capacitor (not shown in Fig 5.1). Tests of the system were conducted using conventional EMI test procedures [15]. A Line Impedance Stabilization Network (LISN) was placed between the load and the output filter for measurement of EMI performance. The LISN passes power frequency signals to the load, while acting as a known impedance at ripple frequencies. The voltage across the 50 ohm LISN resistor is used as the metric for output ripple performance. In other words, the input impedance of the LISN is the load resistance at DC and approaches 50 Ω at high frequencies. Tests described here were performed using a 1 Ω load.

Passive Only Vs. Hybrid
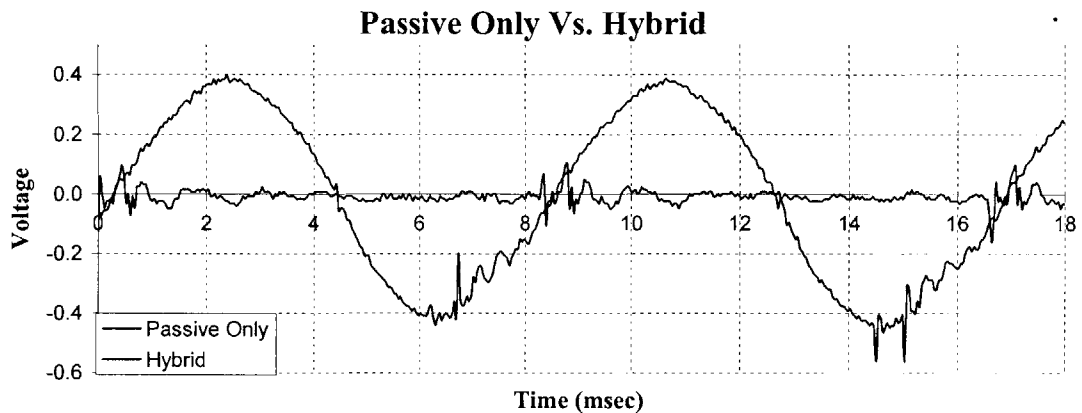
Figure 5.2 The experimental test results for a 125 KHz buck converter. Voltage ripple measured at the LISN is shown both with and without active injection. The peak-to-peak ripple is greatly reduced by the active circuit.

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Passive Filter vs. Hybrid Active/Passive Filter
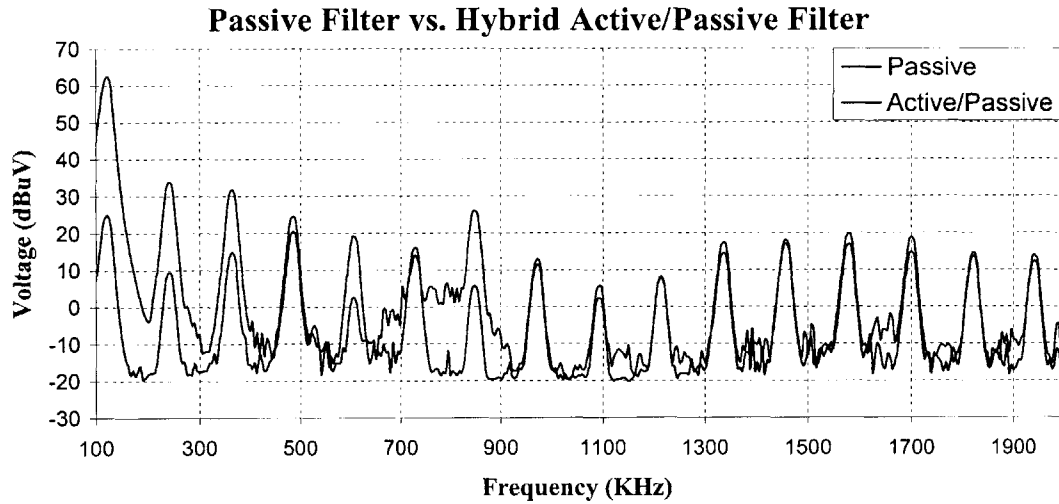
Figure 5.3 Ripple spectra measured at the output of the LISN for both the hybrid active/passive filter and a passive filter of the same size. The hybrid filter achieves a 35 dBμV attenuation of the fundamental ripple frequency as compared to passive components alone.

5.3 Experimental Results and Evaluation

The performance of the hybrid filter is determined by first taking measurements without injection from the active filter element. Essentially, the 5 μH magnetizing inductance of the injector transformer and the 0.2 μF output capacitor form a conventional LC low-pass filter. Measurements were then taken with the active filter in operation. Figure 5.2 illustrates the dramatic improvement in output voltage ripple performance that is achieved through the use of the active circuitry. The spectral measurements of Fig. 5.3 indicate that the use of active injection provides almost 35 dB reduction in fundamental ripple voltage and results in the largest component across frequency being 25 dB lower in magnitude.

As mentioned previously, the best results are achieved with feedforward and feedback control used together, as illustrated in Figs. 5.3 and 5.4. Individually, the feedforward and feedback controls above are able to achieve about 20 dB ripple attenuation, corresponding to about 10% residual ripple. The amount of attenuation

attainable for feedforward is limited by phase and magnitude error. The feedforward control has very slight magnitude and phase errors, but it is enough to significantly limit feedforward ripple cancellation. For the feedback control, stability considerations limit achievable feedback gain and ripple attenuation. The ripple around 700 KHz is greater with feedback ripple cancellation than without, reflecting deterioration in filter performance in this region due to ripple *amplification* by the feedback. The increase in ripple from feedback control in the region is compensated by the feedforward control. Therefore, as illustrated in Fig. 5.3, the combination of the two control systems yields a superior result over either one alone. At mid-range frequencies the feedforward controller compensates for the limitations of the feedback controller, and at still higher frequencies only passive filtering is effective. These two complementary control schemes allow for the maximum usage of the injector, which is the largest component in the filter.
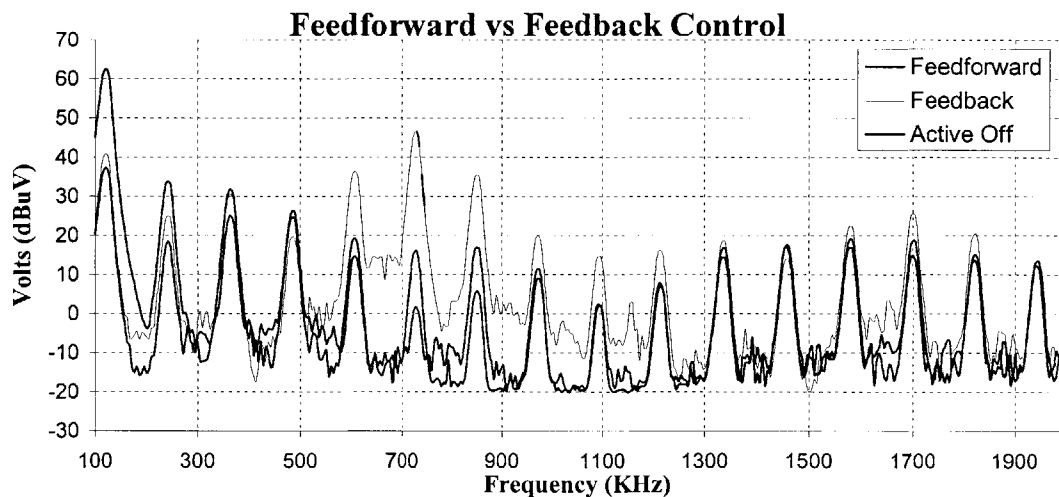

Figure 5.4 Ripple spectra measured at the output of the LISN for feedforward and feedback control used individually. The measurement with the active filter off is offered for comparison. Each control technique has its own performance limitations. The feedback control actually performs worse than no active filtering at certain frequencies.

5.4 Design of a Comparison Passive Filter

In order to compare the benefits of hybrid filters to conventional passive filter

design methods, a passive filter meeting the same ripple specification is designed using

the 5 μH magnetizing inductance of the injector. The larger passive filter requires a 20

μF capacitor to meet the same flat ripple specification across frequency (ripple ≤ 25

dBμV across frequency). Relative performance of the hybrid filter and the large passive

filter is shown in Fig. 5.5. Therefore, the hybrid filter allows a 20 μF capacitor to be

replaced with a 0.2 μF capacitor with no degradation in performance. This corresponds

to a factor of 100 reduction in the required filter capacitance utilizing the hybrid

active/passive approach presented here.

Furthermore, experiments have demonstrated that the active damping circuitry

presented in chapter 4 provides identical performance to the purely passive damping leg.

Fig. 5.6 shows the performance of the system with and without active damping. Without
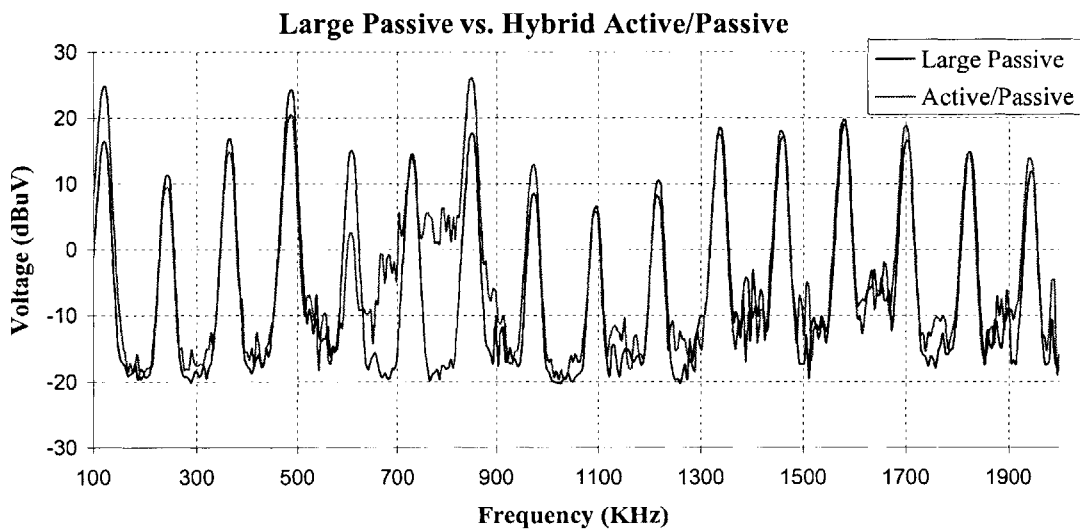
Figure 5.5 LISN voltage spectra of the hybrid active/passive filter and a large passive filter with a 20 μF capacitor. The plots indicate that both the hybrid filter and the large passive filter both meet a flat 25 dBμV ripple specification across frequency.

Active Damping Vs. No Damping
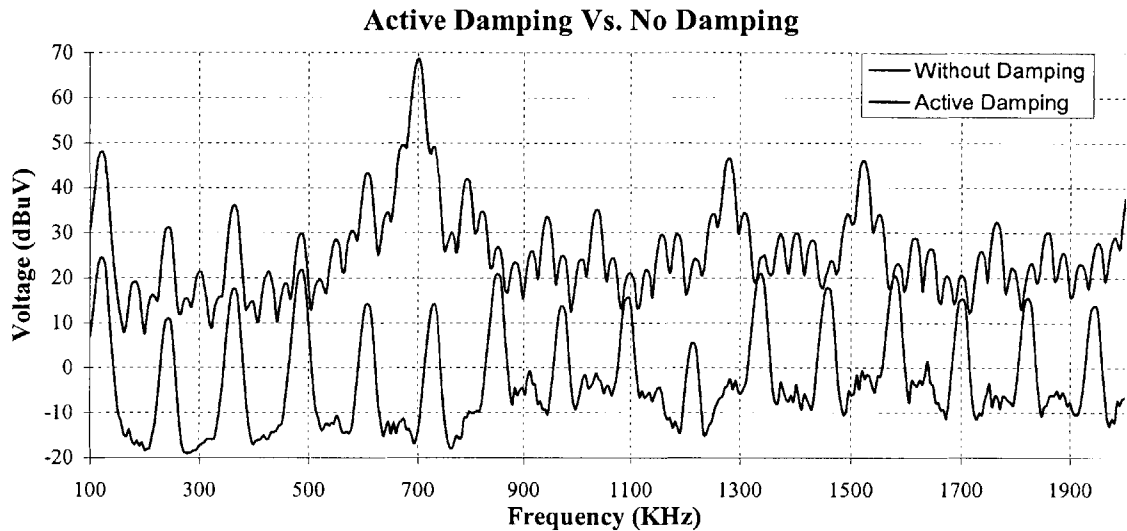
Figure 5.6 LISN voltage spectra of the hybrid filter system with active damping and without damping. The system with out any damping is unstable. This is indicated in the figure by the large peak at 700 KHz. The active damping stabilizes the system.

the active damping circuit operational the system is unstable. Fig. 5.7 goes on to compare the performance between active and passive damping circuits. From the 5.7, the results are nearly identical. Therefore the active damping circuit provides a reduction in damping capacitance by a factor of 1000. Essentially, a simple, single-transistor circuit is capable of making a 1nF capacitor behave like a 1μF capacitor. The benefit of the proposed approach is that by introducing simple, signal-level active circuitry, the passive filter capacitance can be dramatically reduced for the same level of performance.

5.5 Design of a Complete Active Filter

The efficiency of the active filter is of great concern because it is dissipative in nature, unlike conventional passive filters. If the losses in the active circuitry greatly decrease the efficiency of the converter then the approach will not be worthwhile. To evaluate the impact of efficiency, additional voltage regulators are added to the active/hybrid filter to supply the power for the active filter components. This allows a

complete and accurate measurement of efficiency for a self sufficient active filter implementation. The voltage regulators can draw the power from either the 42 volt or 14 volt bus. The prototype uses two 14 volt to 6 volt regulators because they were readily available; the 42 volt bus could also have been used. Switching regulators are required because the signal level amplifiers have been designed to have a 0 DC voltage, which requires both positive and negative voltage. The prototype is implemented with the NME1205, switching regulator which has an isolated output that allows for positive and negative voltages. The structure of the system is illustrated in Fig. 5.9.

It is also possible to use a single (positive) supply amplifier configuration, as illustrated in Fig. 5.8. Amplifiers designed with a single supply have a non zero DC voltage. This would require a blocking capacitor in series with the amplifier and the secondary side of the transformer (see Fig 5.8), because at DC the transformer is a short circuit. The blocking capacitor and the magnetizing inductor form a second order high pass filter, with the following transfer function:
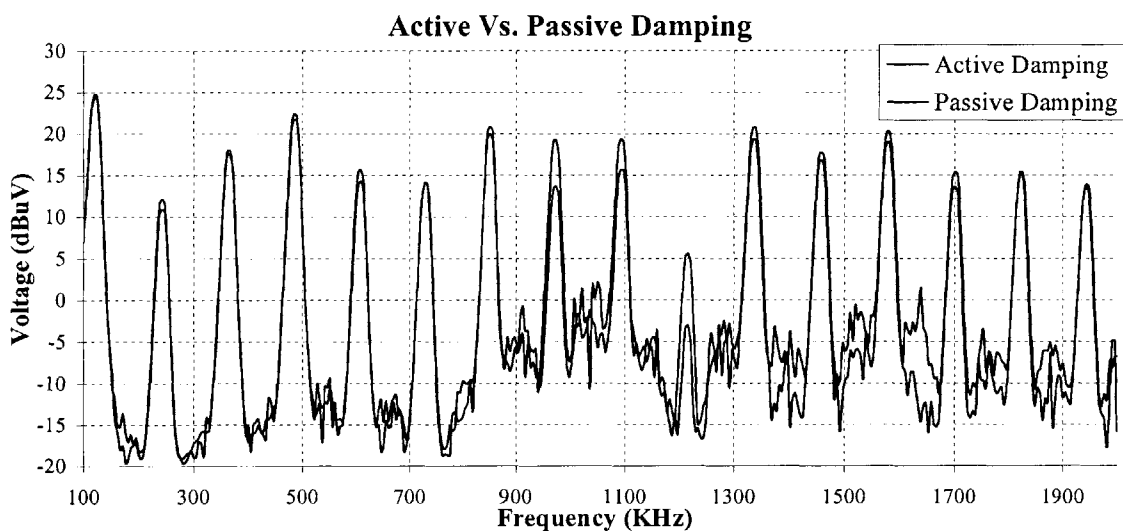

Figure 5.7 LISN voltage spectra of the hybrid filter with active and passive damping. The plots indicate that the active and passive damping topologies have similar performance.

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$$\frac{V_{secondary}}{V_{amplifier}} = \frac{s^2}{s^2 + s\dfrac{R_{out}}{L_{magnetizing}} + \dfrac{1}{L_{magnetizing}C_{blocking}}} \qquad (5.1)$$

In order to minimize phase and magnitude error the pole pair must be at least an order of magnitude below the switching frequency of the converter. For a secondary side magnetizing inductance of 125 μH, this requires a 1.3 μF capacitor, making it the largest capacitor of the active filter.

To minimize capacitance, a dual-supply amplifier configuration is used, implemented with switching regulators. They are more efficient than the alternative, linear regulators. However, switching regulators are relatively costly and generate more electrical noise than linear regulators. The noise can be significantly reduced by adding some additional small, passive filters. If the size of the filter needed for the regulators are larger than the ones being replaced, then the active system is futile. Fortunately, the regulators only need 0.1 μF filter capacitor on the output and a small inductor on the input (see Fig 5.9). Since the regulators have a small bias current, a ferrite bead is used
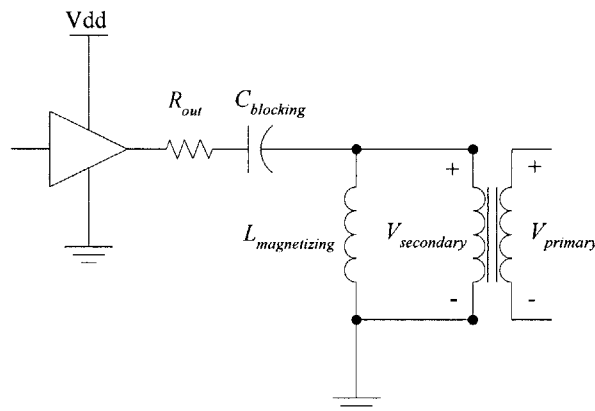
Figure 5.8 An additional blocking capacitor is needed at the output stage of the amplifier if a single supply amplifier configuration is used (resulting in a DC bias voltage is not equal to zero). The output impedance of the high speed buffer, R_{out}, blocking capacitor, and magnetizing inductance of the transformer forms a second-order low pass filter. If the poles of filter are near the frequencies of interested they will cause magnitude and phase errors.

to implement the input inductor. It is important to note that the regulators draw power from the "noisy" 14V side of the filter. Therefore, noise added by these components is filtered out by the hybrid filter. If the regulators draw power from the "quiet" 14V side then the added noise will be directly injected into the load. The design of the regulators does not pose a fundamental challenge to the performance of the overall hybrid filter. That is, the experimental results have verified that the hybrid filter gives identical performance whether deriving power from the buck converter and deriving power from another power source. It should be noted that the power supplies for the active circuitry are a significant consideration. Availability of existing logic supplies to the power the active circuitry make the active filtering approach much more attractive.

The prototype with self-contained power supply represents an accurate measure of the overall efficiency of the hybrid filter. From testing, the overall regulators take the noisy 14 volts and supply a nearly steady +/- 6V. In many applications, separate generation of the signal-level voltages is not necessary; it is included here for completeness. Experimental results show that the average current drawn from the "noisy" 14V bus by the active elements is slightly less than 100mA. This corresponds to 1.4 Watt of power dissipation. If the active damping is also used, then the power
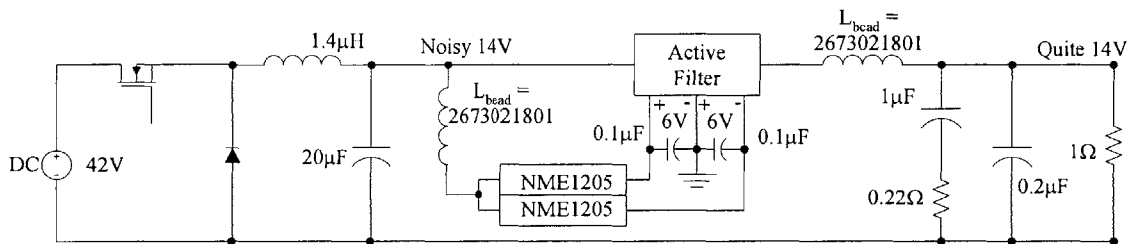
Figure 5.9 Switching regulators are incorporated into the hybrid active filter as a power source. Power for the active circuitry of the filter is derived from the DC/DC converter. The entire hybrid system is self-contained. The system power is drawn from the noisy 14V side, so any noise created by the regulators is dealt with by the active filter. The passive filters components required by the switching regulators are insignificant in comparison to the rest of the EMI filter.

dissipation increases to 2 watts. This corresponds to only 0.9% of the total output power. Thus, the active circuitry does not dramatically affect the efficiency of the overall system.

5.6 Summary

The hybrid active/passive filter and active damping was applied to a 125KHz switching buck converter. The active/passive filter was able to reduce the fundamental switching-frequency noise by 35dB. The active filter allows a $0.2\mu F$ capacitor to replace a $20\mu F$ capacitor for the same EMI performance, which corresponds to a 100 times reduction in capacitance. The active damping technique does even better. It allows a reduction of the damping inductor by a factor of a 1000: a 1nF capacitor is able to replace a $1\mu F$ capacitor. The overall system was found to consume only 0.9% of the rated converter output power. Therefore, by paying a small price in overall efficiency the hybrid filter and active damping techniques are able to dramatically reduce the capacitance needed in EMI filters.

6.1 Introduction

Traditional input EMI filter design places a capacitor in parallel with the DC voltage

supply to provide a low-impedance shunt path for high-frequency currents. EMI

specifications, such as SAE J1113/41, require the capacitor to be able to shunt current over

a wide frequency range. To achieve low impedance at higher frequencies various types of

capacitors are placed in parallel. Large-capacitance electrolytic capacitors are used to shunt

lower EMI frequencies and provide voltage holdup. For mid-range frequencies, smaller

tantalum or ceramic capacitors are employed. Small ceramic capacitors are used for high

EMI frequencies. The relative cost per capacitance is typically higher for capacitors that

perform better at higher frequencies. Large-valued electrolytics are used because of their

low cost and high energy storage densities, but they have poor high frequency performance.

On the other hand, ceramic capacitors have excellent high frequency performance, but are
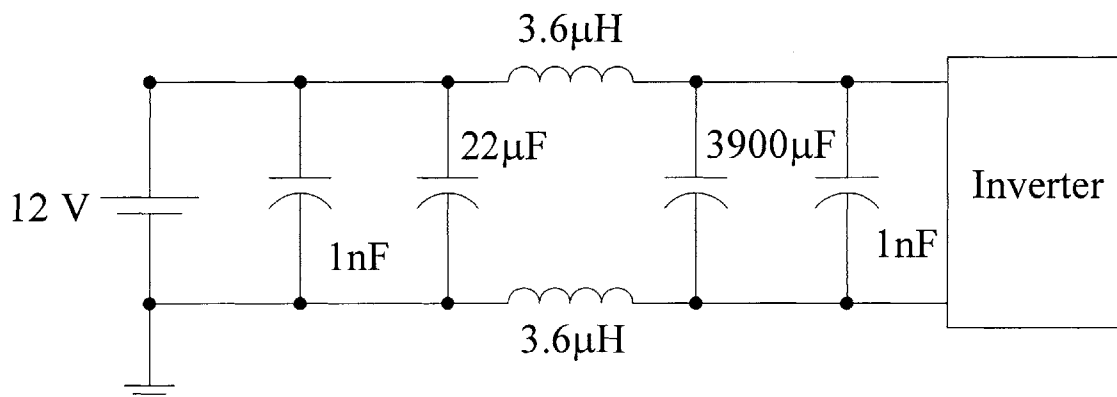
Figure 6.1 Passive input filter for an automotive Electorhydraulic electronic power steering module. Current ripple is generated by an inverter connected to a three phase brushless motor. The passive filter contains a large electrolytic filter in parallel with the inverter. In addition, it has a large, expensive ceramic capacitor in parallel with the battery.

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used sparingly due to cost.

The particular filtering application considered in this chapter is an input EMI filter for an automotive electro-hydraulic power steering (EHPS) pump motor. This application uses an inverter to convert DC voltage into three phase AC to drive a brushless motor for the EHPS system. The electrical motor replaces the belt-drive for a hydraulic fluid pump, and allows for more efficient operation of the power steering system. The inverter has a fundamental switching frequency of 10 KHz and a peak (transient) input current of 70 amps steady-state average input current on the order of 35 amps. The baseline passive input filter and inverter package was produced by a major automotive supplier for a line of European cars. The entire system must follow SAE EMI specifications.

The production version, (passive) input filter is illustrated in Fig. 6.1. It uses a filter structure with a 3900 μF electrolytic capacitor at the input to the inverter and a 22μF ceramic capacitor at the supply interface. Separating the two capacitors are two 3.6 μH inductors providing both common mode and differential mode filtering. In addition to the electrolytic capacitor at the inverter input there is a small ceramic (1nF) capacitor in parallel with it for higher frequencies. The same is true of the large-valued ceramic capacitor (22μF). An approximate cost breakdown of this filter is illustrated in Table 6.1. The high-valued ceramic capacitor cost about the same as the large electrolytic capacitor

Passive Component	Cost For Quantities of 1000 (US dollars)	Volume (inches^2)
3900 μF Electrolytic Capacitor	$ 2	1.37
22 μF Ceramic Capacitor	$ 2	0.02
3.6 μH Inductor	$ 3	0.6

Table 6.1 Gives the cost break down of the components in the passive input EMI filter of the EHPS system. The cost per unit is based on estimated cost attained for quantities of 1000 units. The volume of each component is provided for relative magnitude.

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though it is physically much smaller. (The breakdown price may not scale to high volumes, but for comparison purposes the thesis uses available cost figures for quantities of 1000.) Active filtering techniques are applied to this passive filter in an effort to achieve improvements over the cost of the production model.

The large ceramic capacitor is a prime candidate for active techniques due to its high cost and reduced ripple-carrying requirement. Other passive components, such as inductors, may also be reduced by active circuit techniques; such techniques will not be explored here. The feasibility of applying active circuit techniques to a capacitor is dependent on the ripple current the capacitor must carry. Simulations can provide an easy estimate of the current magnitude. The inverter and motor drive can be modeled as a square-wave current source at the switching frequency of the inverter, 10 KHz (see Fig 6.2). The worst-case condition for the power steering unit occurs when the motor becomes locked in position. Designing for this, the inverter is modeled as a 10 KHz current source pulsing with 50 percent duty ratio from 0 to 70 amps. The power constraint of signal level amplifiers forbids the direct replacement of the electrolytic capacitor with an active filter. Simulations show the ripple current of the electrolytic capacitor to be 40 amps peak to peak (see Fig 6.3). It is interesting to note that even the passive filter can only sustain this level
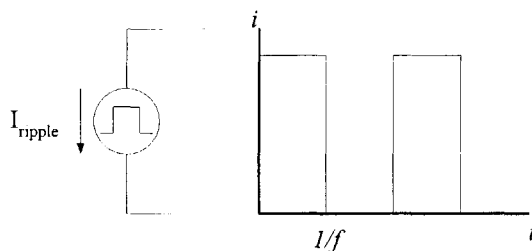
Figure 6.2 The inverter and motor drive is modeled as a square wave current source. The frequency of the square wave is 10KHz, the switching frequency of the inverter. The peak current amplitude is 70 amps, which is the worst case condition for the system.

under transient conditions; the steady-state limit of the electrolytic capacitor is only on the order of 15A rms. The high-value ceramic capacitor has a ripple current of 0.9 amps under this condition (see Fig 6.4). Although this is still a significant amount of current, the high value ceramic capacitor is a prime target for active filtering.

6.2 Active Filter Design Considerations

In this system, cost is the major design constraint. In order for the active filter to be a commercially viable replacement for the capacitor, the entire active filter must cost under $2. The active filter must also have limited power dissipation for efficiency considerations. Unlike passive components, active circuits have inherent power dissipation. Excess power dissipation impacts cost, due to the need for more elaborate heat management techniques and component technologies. Furthermore active component power dissipation will

Current of Large Electrolytic Capacitor
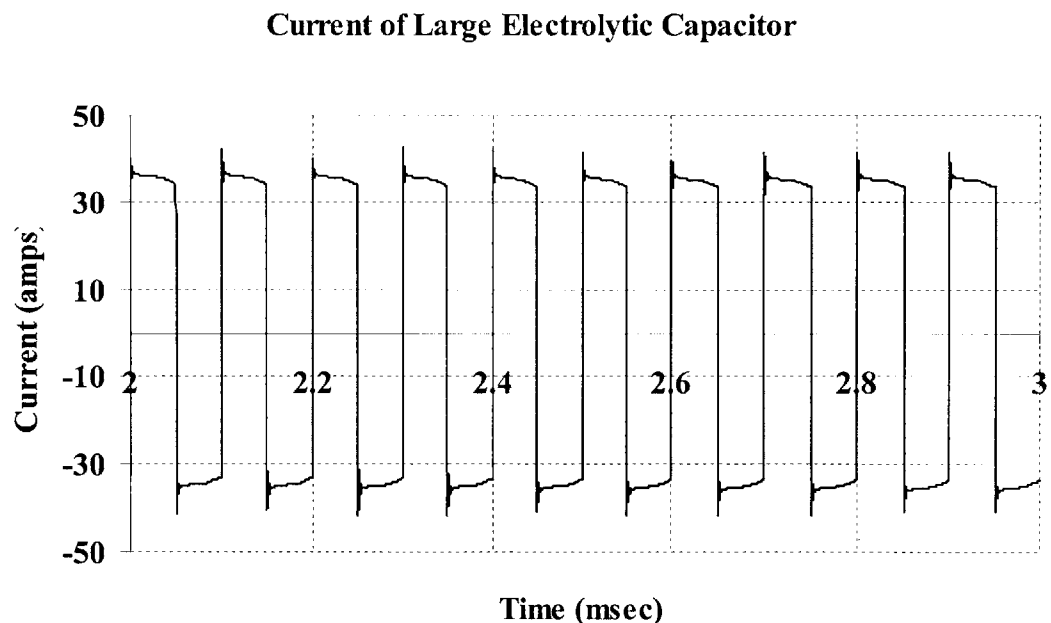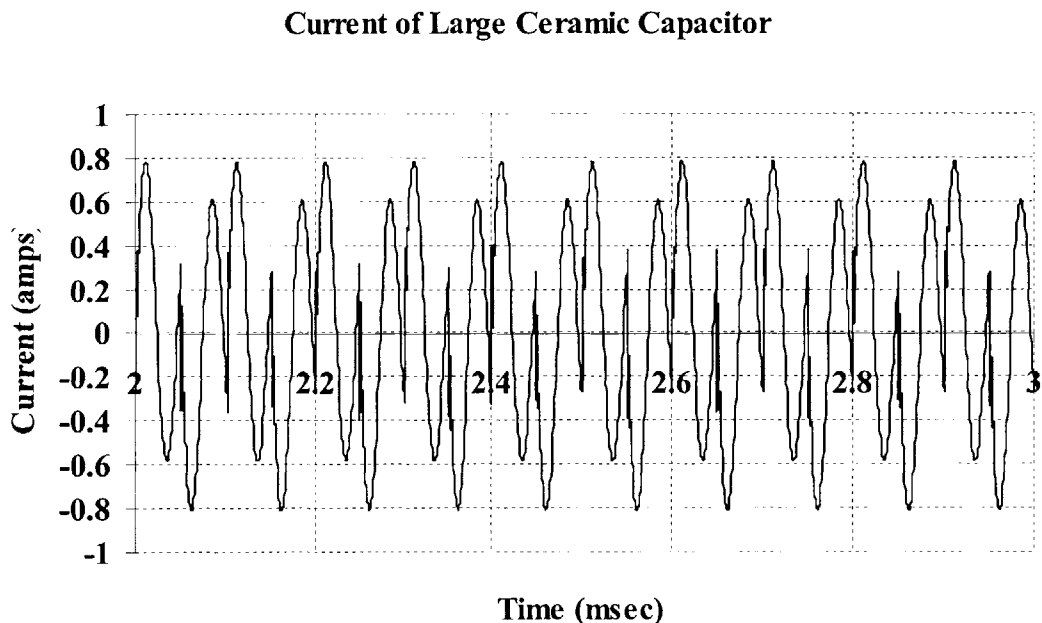

Figure 6.3 Simulation of the maximum ripple current that is shunted through the 3900μF electrolytic capacitor. The electrolytic capacitor must be able to handle a maximum peak to peak current ripple of 80 amps. The current magnitude is too large for active filtering techniques.

adversely affect the overall efficiency of the inverter. A further constraint is the active

filter system must use the available 14V power supply. Other power supply requirements

would increase the cost substantially. Given these constraints, the design of the active

filter is quite interesting and challenging.

Based on these limitations, many design choices can be made that affect the

design regardless of the chosen topology. The severe cost constraint allows the use of only

lower-end, minimal cost transistors, such as the 3904 and 3906. These transistors are

standard signal level transistors in a TO-92 package. A reasonable power limit for the

package would require each one to dissipate less than a third of a watt. Therefore, it may

be necessary to parallel several transistors together. Simulations show that the 22uF

capacitor has a peak current ripple of 0.9 amps. The bias current alone (for a class A stage)

Current of Large Ceramic Capacitor

Time (msec)

Figure 6.4 Simulation of the maximum ripple current that is shunted through the 22 μF ceramic capacitor. The electrolytic capacitor must be able to handle a maximum peak to peak current ripple of 0.8 amps. Active filtering techniques may be applied to the ceramic capacitor.

would result in 14 watts of power dissipation, making it impossible to directly implement the active filter with signal-level transistors and a class-A output stage. More importantly, it would not make the system cost effective. Surprisingly, a saving factor lies in the SAE J1113/41 specification. The specification only stipulates the EMI ripple from 150 KHz onward. The majority of the ripple is due to the fundamental switching frequency of the inverter, which occurs at 10 KHz; the magnitude of the frequency spectrum of the ripple at 100 KHz and beyond is significantly less than the 10 KHz component. If the active components are able to reject the 10 KHz signal and pass signals 100 KHz and beyond, then the magnitude of the ripple to be handled by the active circuit is greatly reduced. Therefore, with appropriate design an active approach can lead to a viable alternative.

The design of the sensing filter proves to be a primary challenge of this system. The ideal sensing filter would have a sharp cutoff, essentially going from high attenuation to high gain within decade. Such a sharp cutoff would require a high order sensing filter, which adds complexity and cost, and makes it more difficult to attain a stable feedback loop. Loop compensation may be added for higher sensing filter stability, but this adds complexity and oscillations may occur due to non-linearities. (Nonlinearities, such as saturation, cause the loop gain of the feedback system to decrease for certain input magnitudes, which can drives the system unstable.) These factors make it difficult to use a sensing filter with an order higher than one. One possible solution is to use non linear compensation, but this is beyond the scope of this thesis. Therefore, only non-compensating sensing filters are considered. Unfortunately, a first order sensing filter does not provide enough separation between the pass band and stop band. That is to say that, the

filter is unable to attenuate the 10 KHz signal within the power limitations of the low power transistors, while still providing adequate gain at 100 KHz and beyond.

One approach for overcoming these limitations is to place a medium-sized electrolytic capacitor in parallel with the active filter. The low cost of electrolytics makes this a viable solution. Electrolytic capacitors have poor performance at higher frequencies, where their ESL (equivalent series inductance) causes them to behave like inductors. By placing an electrolytic capacitor larger than 22 μF in parallel with the active filter, the lower frequency currents, including the 10 KHz fundamental, will be shunted from the active filter (see Fig 6.5). At higher EMI frequencies , where the electrolytic capacitor begins to behave like an inductor, the active filter takes over and shunts the high-frequency currents from the load. The much higher frequency currents that fall beyond the bandwidth of active circuit can be filtered by a small ceramic capacitor.

6.3 Amplifier Design Considerations

Essentially the active filtering problem can be thought of as replacing a passive capacitor with an active circuit having the same or lower impedance over the high
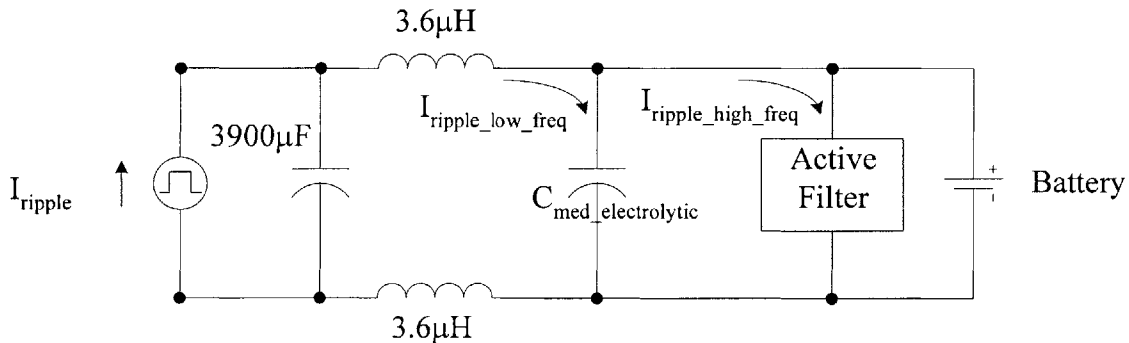

Figure 6.5 A medium sized electrolytic capacitor (22μF) is placed in parallel with the active filter in order to reduce the current magnitude that the active filter shunts. The large passive filter has a poor frequency response, therefore it will shunt the lower frequency component of the current ripple. The higher frequency ripple components are handled by the active filter.

frequency range. To replace the existing capacitor with a hybrid filter, the active circuitry

can be used to enhance a significantly smaller capacitor. Various active enhancement

topologies were investigated in the context of active damping (Chapter 5). Two topologies

for active filtering in this application are investigated in this thesis. The first is a voltage

sense – current drive topology. The second is a voltage sense – voltage drive

configuration. Some of the advantages and possible disadvantages of each will be

addressed. Both topologies use a sensing filter, implemented with small passive

components, to select the frequencies processed with the active amplifier. Transistors are

employed for signal and power gain, and both topologies use feedback control. With any

feedback system, the tradeoff between gain and stability is the primary performance

limitation. The larger the gain the more the active circuitry enhances the capacitor,

therefore allowing for a smaller passive component. The upper limit on the amount of gain

achievable is set by the stability of the system. As mentioned previously, the stability is

highly dependent upon the sensing filter.

6.3.1 Voltage Sense – Current Drive Topology

The system uses a current to voltage gain, also known as a transconductance

amplifier. Although the transconductance amplifiers can have high bandwidths, the main
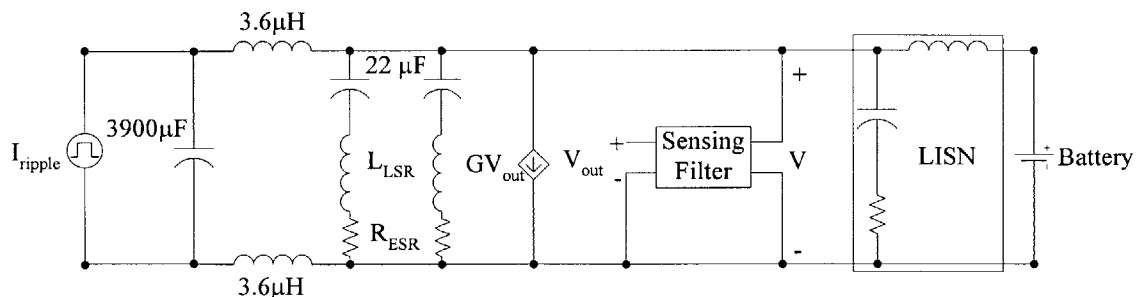
Figure 6.6 Simulation model of the hybrid filter. This model is used to determine the maximum current ripple that will flow through the active filter. From simulations the needed bias current is determined.

drawback in this application is the large DC bias current. The needed DC bias is set by the

ripple magnitude which the active filter shunts. Circuit simulations readily determine the

needed bias currents. The hybrid filter is modeled by two 22uf electrolytic capacitors

including parasitics, a passive sensing filter, and an ideal transconductance amplifier. (see

Fig 6.6) Simulations show that the active component must shunt a maximum peak ripple

of 200 mA. Therefore the current drive stage of the transconductance amplifier must be

bias at 250 mA. Although such currents are not uncommon in power electronics, it posses

significant difficulty for signal level amplifiers. The challenge of a large bias current stems

from issues of power dissipation and the general design of large bias currents on signal

level transistors.

The amount of power dissipation that a transistor is equipped to handle is dependent

upon the packaging and cooling method. The cost constraint limits the cool schemes to

heat sink cooled. Being further constrained to low-end transistors, a single transistor

cannot handle such large bias levels. The TO-92 package cannot handle the power

requirements and the 3904 and 3906 cannot handle the large current magnitude. Therefore
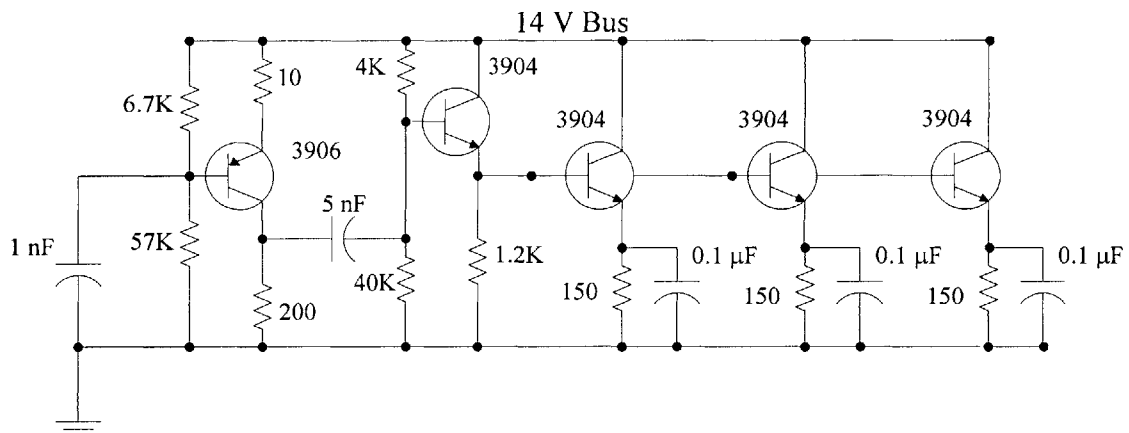
Figure 6.7 The active filter circuit with integrated sensing filter. Three emitter followers are used as the current driving stage. A second emitter follower stage is used to increase the input impedance of the driving stage. A common base stage is employed for added gain.

multiple transistors used in parallel to evenly distribute the bias current and dissipation. The prototype uses three 3904, npn transistors with a bias current of 85 mA and a power dissipation of .225 watts (see Fig 6.7). The maximum power dissipation for these transistors is .625 watts. To reduce the power dissipation the voltage dropped across the transistors is divided by a resistor in the emitter. The configuration is commonly called emitter follower stage. The voltage to current gain of the output stage is increased by adding a bypass capacitor across each resistor. Although each of the three emitter follower circuits dissipates about 1.2 watts, the transistor handles only a quarter of that. The use of an emitter follower with bypass capacitors for the output stage allows the system to stay within the power limits of the small signal transistors, while providing voltage to current gain.

It was found experimentally that the large bias current causes difficulties in the performance of the transconductance amplifier. According to hand calculations and simulations, the gain of the prototype should be greater than forty and have a bandwidth of at least 10 MHz. When the system is actually implemented (Fig.6.7) the gain and bandwidth are far from the predicted values. The maximum measured gain is ten and the bandwidth is 2 MHz. Even after layout parasitics and temperature rise has been accounted for in simulation, the actual values are greatly different from the predicted values. When the bias current is decreased to signal level values of less than 10 mA, the predicted and actual values matched. This indicates the inherent difficulty of designing high biased current circuits using standard signal level techniques and components. The exact difficulty of designing with signal level transistors with large bias currents is not addressed

in this work, but may relate to limitations of the assumption (e.g. low-level injection) used to develop the small-signal models for transistors.

6.3.2 Voltage Sense – Voltage Drive

By moving to a voltage sense-voltage drive topology, the issues of designing with large bias currents can be avoided, but at the expense of increased peak currents. The output stage can be implemented with a standard push-pull stage. A push-pull circuit has no bias current, but it does have a dead zone. In the dead zone the output voltage is zero if the input voltage is within the thermal voltage of the transistor. A small bias current is passed through both push-pull transistors in order to eliminate the dead zone. The two transistors are biased with emitter followers, which have the extra benefit of increasing the input impedance to the drive stage (see Fig. 6.8). One concern of a push-pull output stage is maintaining bias stability. In this configuration, it is possible for the current to increase without bound. Placing resistors in the emitters of the push-pull transistors is one solution. The emitter resistors serve to limit the amount of current follow (see Fig 6.8). The output
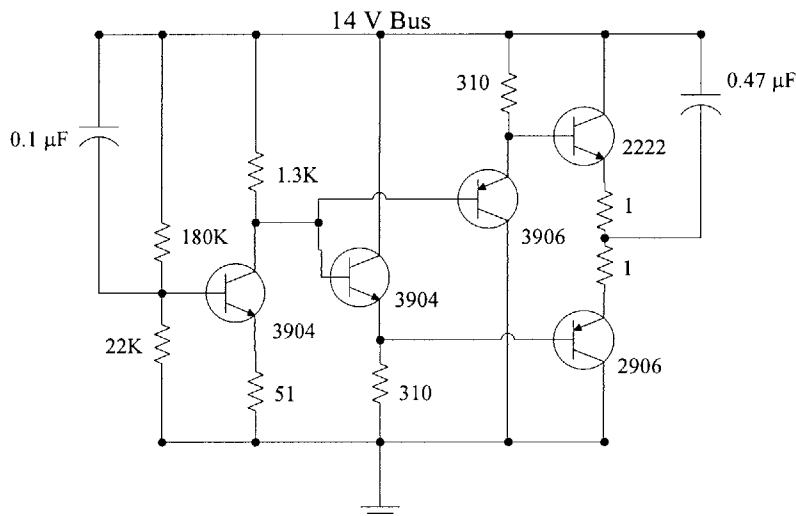

Figure 6.8 The voltage sense-voltage drive active filter circuit with integrated sensing filter. A push pull implements the voltage drive stage. This topology greatly reduces the needed bias current. A second emitter follower stage is used to increase the input impedance of the driving stage. A common emitter stage is employed for added gain.

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stage does not provide any voltage gain. Rather, it serves as a voltage buffer and a power

gain stage.

The voltage sense-voltage drive topology has the drawback of increased peak

current, which affects the bandwidth of the system. Simulation can facilitate the prediction

of the peak current needed. The hybrid system is modeled as a sensing filter with lead

compensation, two 22 μF electrolytic capacitors, and an ideal voltage gain driving a load

capacitor (see Fig 6.9). Simulations show that the peak current has increased to 500mA.

The 3904 and 3906 transistors are not designed to handle these peak currents. Fortunately,

the 2222 and 2906 can accommodate these current magnitudes. In addition, these

transistors cost the same and have the same packaging. The tradeoff is that the 2222 and

2906 have a lower unity beta bandwidth than the 3904 and 3906. This is due to the larger

parasitic capacitances of the 2222 and 2906. Furthermore, the topology needed for the

voltage amplifier has a lower bandwidth than the one for the transconductance amplifier.

The common emitter stage in the voltage amplifier has the unfortunate miller effect which

multiplies capacitances by the gain of the system. The bandwidth limitation may become a

definite issue in the voltage sense-voltage drive topology.

The tradeoffs of the voltage sense-voltage drive over the voltage sense-current drive
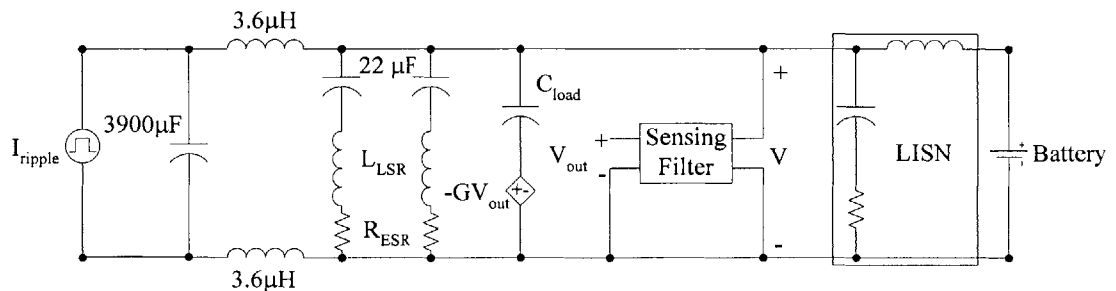
Figure 6.9 Simulation model of the hybrid filter. This model is used to determine the peak current ripple that will flow through the active filter. From simulations the needed transistors can be determined.

topology lies in the output stage. The push pull output stage of the voltage sense voltage drive case allows for a substantial decrease in the needed bias current. This leads to relative ease in design and, more importantly, a substantial reduction in power dissipation. The tradeoff is the increase in the peak ripple current magnitude. Different transistors were required to deal with this issue. It also has the additional drawback of having a lower bandwidth.

6.4 Summary

This chapter enumerated some of the possible difficulties of applying active filtering technologies to a commercial motor drive application. Although may of technical challenges are similar, more constraints are added because the active filter must replace a $2 passive component. Several possible approaches where introduced and briefly analyzed illustrating some of the tradeoffs. There is still a significant amount of work left to be done. First and foremost: given the power limitations and cost constraints, what are appropriate design procedures? Relating to which, there needs to be further work investigating different sensing filter designs and compensation methods. Moreover, the issues of designing signal level transistors with large bias currents needs to be looked at closely. A set of guidelines and design solutions need to be developed. The optimal solution to the difficult problem of active filters for motor drives still remains to be developed, and is left for future work.

7.1 Introduction

EMI filters are an integral part of switching power converters. Capacitors substantially contribute to the overall size, cost, and reliability of these EMI filters. This thesis focuses on reducing filter capacitors in EMI filters, reducing damping capacitors, and introducing the application of active techniques to reduce EMI capacitor cost in motor drives.

For all of these applications, signal-level active components are used to enhance the performance of small passive components. These low power circuits are unable to handle highly dissipative applications. Therefore, active circuit techniques are usually applied to later filter stages. At these subsequent stages, the EMI ripple is greatly reduced but still significant enough to warrant the use of relatively large passive capacitors.

7.2 Active Filtering

A hybrid passive/active filter topology that achieves ripple reduction by injecting a compensating voltage ripple across a series filter element is used. Both ripple feedforward and feedback are employed in the design. The design of injector, amplifier, and senor circuitry suitable for the application are investigated. This work demonstrated that, at least in some applications, active filtering techniques can reduce the needed filter capacitance by a factor of 100.

The primary challenge in the proposed filtering technique lies in the design of the voltage injector. The injector circuit must satisfy several difficult challenges. First, there must be minimal DC losses. The injector resides in the DC path of the converter; thus any DC loss would be detrimental to efficiency. Second, the injector must provide isolation between the power converter and the signal-level circuitry. Finally, the feedforward control relies on an injector with high signal fidelity. Transformer-based circuits prove to be the most viable solution. This work illustrates the design procedure and tradeoffs of several transformer circuits, giving careful consideration to parasitics.

As illustrated in Chapter 3, the feedforward and feedback controls are implemented with standard discrete amplifiers. Feedforward control relies on precise gain to inject the inverse of the voltage ripple. Provisions must be made in the design of the feedforward controller insure an accurate gain. Conversely, feedback systems rely on an inexact but large gain to reduce the voltage ripple within a closed loop. Feedback loop stability is the most important factor in the design of such systems. A compensator is employed to shape the loop to maximize gain and stability. Chapter 3 investigates circuit topologies which optimize the feedforward and feedback controller.

This thesis has provided a proof-of-concept for a series voltage ripple filter. There are still issues that need to be resolved before this technology can be brought to light in industry. The prototype introduced in this work is by no means optimized. Further work is still needed to explore the minimum cost, volume, and maximum lifetime of such a system. Additional circuit design can improve the performance of the controller. The feedforward system can be further optimized for precision and the feedback system can be maximized for gain. Never the less, this thesis demonstrates the

viability of the system.

7.3 Active Damping

The capacitors used for damping EMI filters is usually an order of magnitude larger than the main EMI filter capacitor. The damping leg needs a large capacitor to block DC voltage, while making the damping leg appear resistive at the corner frequency of the EMI filter. Chapter 4 demonstrated that, at least in some cases of interest, active topologies are able to reduce the damping capacitor size up to a factor of one thousand.

The proposed active damping implementation only requires a single low-end, signal level transistor. The topology introduced uses a current sense-current drive feedback configuration. Once again, the stability of the system is the primary design challenge. The loop transfer function shows that the stability places an upper limit on the size of the capacitor that this technique can replace. The other main limitation is the slight increase in power dissipation. Despite this, the experimental results demonstrate the feasibility and high performance of the new approach, and illustrate its potential benefits.

This work explores only one possible topology. More work is needed to investigate the countless topologies available and the tradeoffs of each. One particular area of interest is topologies which reduce power dissipation.

7.4 Active Motor Drive Filters

This work also introduces the application of active techniques to a commercial EMI filter. In the application, an electric motor powered by the automotive voltage supply is used to drive the hydraulic pump of an automotive electro-hydraulic power steering (EHPS) system. The system was produced by a major automotive supplier for a

line of European automobiles. Active filtering techniques are considered for the input EMI filter in an attempt to reduce the overall filter cost.

A significant portion of the cost is due to the capacitors of the filter. The filter contains two main capacitors: a 3900 μF electrolytic and a 22 μF ceramic. Since the ceramic capacitor nearly costs the same as the electrolytic, it is cost effective to target the ceramic capacitor. Also, the power dissipation considerations prevent the replacement of the electrolytic capacitor. Designing for commercial applications places a heavy constraint on cost. In fact, cost is the primary design challenge. The second most difficult challenge is power dissipation. Two configurations are introduced: a voltage sense-current drive topology and a voltage sense-voltage drive topology. Some of the tradeoffs are also illustrated in chapter 6.

A significant amount of work still needs to be done in this area. Investigations of the two topologies are in a preliminary stage. Further detailed testing and evaluation is needed before any conclusion can be drawn. Furthermore, the scope of future research need not be limited to the two proposed topologies. At the very least, a concise design procedure needs to be developed, illustrating the benefits and tradeoffs of several topologies. Although much work has been completed, there are still significant challenges that need to be addressed before this becomes a commercially viable technique.

7.5 Summary

It is demonstrated that the proposed active filtering approach is most effective in cases where it is desirable to minimize the amount of capacitance in the filter. Experimental data has verified that active filter techniques can reduce the main capacitor

size by about a factor of 100. Tests have also demonstrated that active damping can reduce damping capacitor size a thousand times. This work has also proposed means to reduce EMI filter cost in motor drives. In all these cases, a capacitance reduction of a significant factor is possible with active techniques, without impacting ripple performance.

[1] T.K. Phelps and W.S. Tate, "Optimizing Passive Input Filter Design," *Proceedings of Powercon 6,* May 1979, pp. G1-1 - G1-10.

[2] M. Zhu, D.J. Perreault, V. Caliskan, T.C. Neugebauer, S. Guttowski, and J.G. Kassakian, "Design and Evaluation of an Active Ripple Filter with Rogowski-Coil Current Sensing," *IEEE PESC Record,* Vol. 2, 1999, pp. 874 -880.

[3] S. Feng , W. A. Sander, and T. Wilson, "Small-Capacitance Nondissipative Ripple Filters for DC Supplies," *IEEE Transactions on Magnetics,* Vol. 6, No. 1, March 1970, pp. 137-142.

[4] D.C. Hamill "An Efficient Active Ripple Filter for Use in DC-DC Conversion," *IEEE Transactions on Aerospace and Electronic Systems,* Vol. 32, No. 3, July 1996, pp. 1077-1084.

[5] N.K. Poon, J.C.P. Liu, C.K. Tse, and M.H Pong, "Techniques for Input Ripple Current Cancellation: Classification and Implementation," *IEEE Transactions on Power Electronics,* Vol. 15, No. 6, November 2000, pp. 1144-1152.

[6] J. Walker, "Designing Practical and Effective Active EMI filters," *Proceedings of Powercon 11,* 1984, I-3 pp. 1-8.

[7] L.E. LaWhite and M.F. Schlecht, "Active Filters for 1 MHz Power Circuits With Strict Input/Output Ripple Requirements," *IEEE Transactions on Power Electronics,* Vol. PE-2, No.4, October 1987, pp. 282-290.

[8] T. Farkas and M.F. Schlecht, "Viability of Active EMI Filters for Utility Applications, " *IEEE Transactions on Power Electronics,* Vol. 9, No. 3, May 1994, pp. 328-337.

[9] M.S. Moon and B.H. Cho, "Novel Active Ripple Filter for the Solar Array Shunt Switching Unit, " *Journal of Propulsion and Power,* Vol. 12, No. 1, January-February 1996, pp. 78-82.

[10] P. Midya and P.T. Krein, "Feed-forward Active Filter for Output Ripple Cancellation," *International Journal Electronics,* Vol. 77, No. 5, pp. 805-818.

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[11] L.R. Casey, A. Goldberg, and M.F. Schlecht, "Issues Regarding the Capacitance of 1-10 MHz Transformers," *Proceedings IEEE APEC*, 1988, pp. 352 –359.

[12] A. Goldberg, J.G. Kassakian, and M.F. Schlecht, "Issues Related to 1-10-MHZ Transformer Design," *IEEE Transactions on Power Electronics,* Vol. 4, No. 1, January 1989, pp. 113-123.

[13] V. Vlatkovic, D. Borojevic, and F.C. Lee, "Input Filter Design of Power Factor Correction Circuits," *IEEE Transactions on Power Electronics*, Vol. 11, No. 1 , January 1996, pp. 199 –205.

[14] J. Kassakian, M. Schlecht, and G. Verghese, *Principles of Power Electronic.* Reading Massachusettes: Addison-Wesley, 1992.

[15] SAE EMI Test Methods and Standards Committee (1994) Electro-magnetic compatibility – component test procedure – Part 42 – conducted transient emissions, *SAE Standard SAE J1113/42*, July, Society of Automotive Engineers, Warrendale, PA, USA.