Fabrication of Ultra-thin Strained Silicon on Insulator

by

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B.S., Electrical Engineering (2001)

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Submitted to the Department of Electrical Engineering and Computer Science in Partial Fulfillment of the Requirements for the Degree of Master of Science in Electrical Engineering

at the

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ABSTRACT

MOSFETs fabricated on ultra-thin strained silicon on insulator (SSOI) substrates combine the mobility enhancements of strained silicon with the superior scalability of ultra-thin body or double-gate device structures. Fabrication of 13 nm-thick strained Si directly on SiO_2 is demonstrated by a bond and etch-back method. A double etch-stop technique has been developed to enable thickness control sufficient to achieve a final uniform silicon thickness. Strain is preserved in the strained silicon on insulator structures after rapid thermal annealing. Such ultra-thin layers will enable research on strained Si double-gate and ultra-thin body MOSFETs.

Thesis Supervisor: Judy L. Hoyt

Title: Associate Professor of Electrical Engineering and Computer Science

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INTRODUCTION AND MOTIVATION

1.1 Introduction and Motivation

Fundamental limits to CMOS scaling are rapidly approaching as devices are scaled into the sub-50 nm regime. Until recently, reductions in channel length and gate oxide thickness have allowed the fabrication of devices with increasing speed and density. Unfortunately, this type of scaling will soon reach fundamental limits imposed by source-to-drain tunneling leakage and quantum mechanical tunneling through the gate oxide. Therefore, new methods and materials for CMOS device fabrication must be investigated to allow continued device improvement.

Both novel materials and new device structures have been investigated to improve device performance. Work on strained silicon surface channel MOSFETs

has shown notable mobility enhancements of up to 1.8x for NMOS devices [1]. Significant mobility enhancements also exist for PMOS at low vertical effective field, but the enhancement is degraded in the vertical effective field range where state-of-the-art devices are operated [2]. In addition to novel materials, alternate device structures may also be used to continue scaling. Ultra-thin body and double-gate MOSFETs provide improved electrostatic integrity and the ability to be scaled to the shortest of channel lengths. Therefore, strained silicon in combination with an ultra-thin body or double-gate device design is one promising combination to allow continued device improvements past the limits of traditional bulk silicon MOSFETs. The purpose of this work is to determine the feasibility of fabricating strained silicon ultra-thin layers directly on insulator. This will enable the future fabrication of devices such as ultra-thin body and double gate strained silicon MOSFETs as shown in figure 1.1.

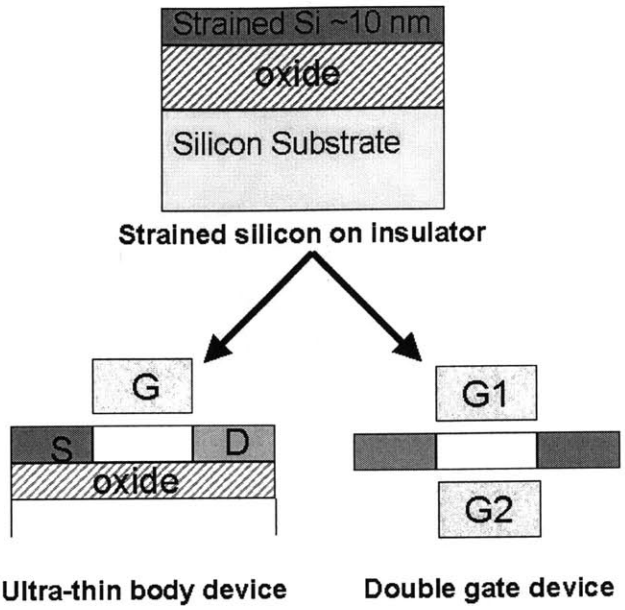


Figure 1.1 – Strained silicon on insulator substrates will enable the fabrication of ultra-thin body and double gate strained silicon MOSFETS. This will combine the benefits of novel device design with the mobility enhancements of strained silicon.

1.2 Benefits of Strained Silicon

Due to biaxial tensile strain in the silicon channel, strained silicon MOSFETs show notable mobility enhancements over bulk silicon MOSFETs. In order to correctly induce the strain in thin strained silicon layers, a controlled epitaxial growth is necessary.

1.2.1 Lattice Mismatch and Strain in Si and SiGe Films

High quality strained silicon layers can be formed by the growth of silicon on a relaxed SiGe layer. Germanium has a lattice constant of 5.646Å. This is 4.1% larger than the silicon lattice constant of 5.431Å as shown schematically in figure 1.2.

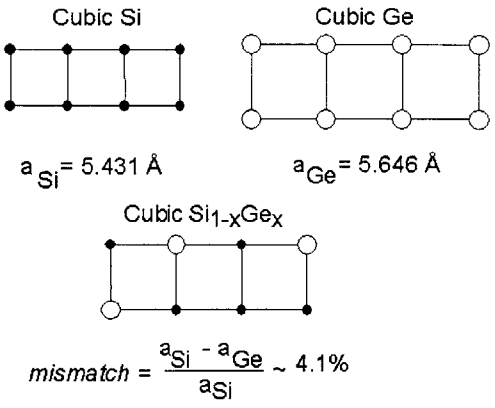


Figure 1.2 – Germanium has a lattice constant of 5.646Å. This is 4.1% larger than the silicon lattice constant of 5.431Å. This difference in lattice constant is key to the successful growth of strained Si or SiGe films.

Due to the lattice mismatch between crystalline silicon and crystalline germanium, if the silicon film is sufficiently thin, silicon grown on relaxed SiGe will stretch in the in-plane direction to match the larger lattice of the SiGe, and thus exhibit biaxial tensile strain as seen in figure 1.3. The amount of strain in the silicon is dependent on the germanium fraction in the relaxed SiGe. Fully strained silicon grown on $Si_{.70}Ge_{.30}$, will have 1.2% strain. As the Ge fraction increases, the lattice constants become more mismatched and the strain in the silicon will also increase. Conversely, if thin layers of SiGe are grown on crystalline silicon, the SiGe will exhibit biaxial compression since the lattice constant will match the in-plane lattice parameter of the underlying silicon, as shown in figure 1.3.

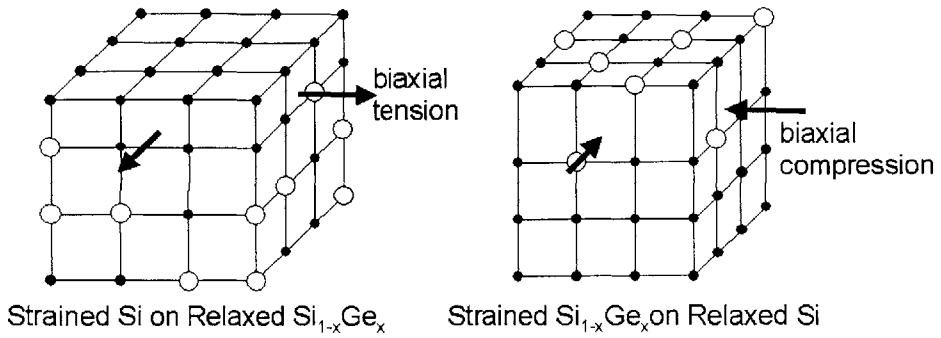


Figure 1.3 – Thin silicon films grown on relaxed SiGe will adhere to the larger SiGe lattice and exhibit biaxial tensile strain. However, thin SiGe grown on crystalline Si will adhere to the smaller silicon lattice and exhibit biaxial compression.

Only a limited thickness of strained material can be grown without strain relaxation. The strained film will begin to relax when it becomes more energetically favorable to form dislocations. This thickness is the critical thickness of the film.

1.2.2 Electron and Hole Mobility Enhancement in Strained Si

Tensile strain in the silicon channel leads to benefits for MOSFET operation due to increased mobility of both electrons and holes. The biaxial tensile strain causes splitting in the conduction band. The typical six-fold degenerate conduction band of the relaxed silicon splits into two-fold and four-fold degenerate bands when the silicon is strained. Since electrons have a lower energy in the two-fold degenerate band, they will preferentially occupy this band, leading to a higher mobility [1]. Bulk strained silicon MOSFETS, as shown schematically in figure 1.4, exhibit large mobility enhancements due to the biaxial tensile strain.

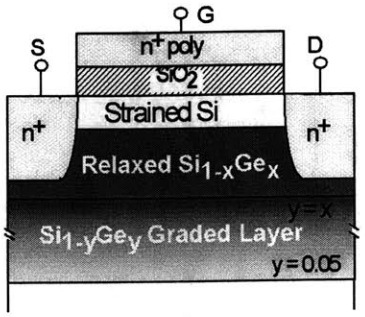


Figure 1.4 – Schematic representation of bulk strained silicon MOSFET device. Channel region is comprised of strained silicon grown on a relaxed SiGe virtual substrate. After Rim, et al. IEDM 1995 – [2].

Electron mobility enhancements of up to 1.8X for n-MOSFETs have been achieved as shown in figure 1.5 [1].

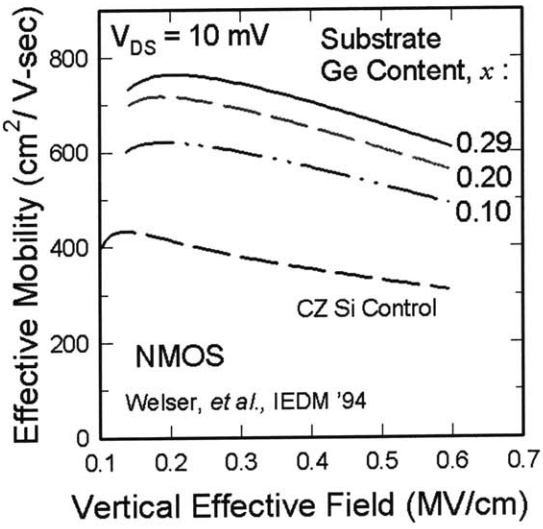


Figure 1.5 – Effective mobility versus vertical effective field for NMOS bulk strained silicon on SiGe device. All strained silicon samples have enhanced mobility compared to the silicon control. After Welser, et al., [1].

The mobility is plotted as a function of the vertical effective field (E_{eff}), which is related to the inversion charge density and thus the gate overdrive according to [3]:

$$E_{eff} = \left(\frac{1}{\varepsilon}\right) * (Q_b + \eta * Q_{inv}) \qquad \text{eq. 1.1}$$

where ε is semiconductor relative dielectric constant [4], Qb is the bulk charge, Qinv is the inversion charge, and η is a fitting parameter of 1/2 for electrons and 1/3 for holes [5,6]. Electron mobility increases with increasing strain in the silicon, but this effect saturates at approximately 30% germanium [1]. A peak mobility of over 750cm^2/V*sec is observed for nMOS strained silicon devices on relaxed $Si_{.70}Ge_{.30}$ virtual substrate.

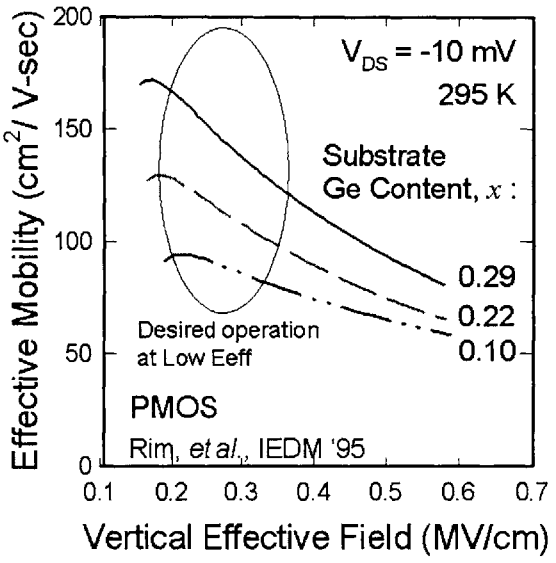


Figure 1.6 – PMOSFET mobility versus vertical effectice field. The largest enhancement is shown at low E_{eff}. After Rim, et al., [2].

Similar to the electron mobility enhancement observed for NMOS devices, mobility enhancements proportional to the strain in the silicon channel have also been demonstrated for holes. Therefore, higher hole mobilities are achieved when the silicon channel is grown on SiGe with high germanium fraction. Unlike electrons

the mobility enhancement for holes does not saturate at 30% germanium. The hole mobility continues to increase until about 60% Ge is incorporated into the relaxed SiGe layer. Although large enhancements are observed at low vertical effective field, the enhancement diminishes at high effective fields as seen in figure 1.6 [2].

In addition to mobility enhancements, strained silicon provides the benefit of having the same chemical properties as silicon. This allows the use of standard silicon CMOS processes to fabricate devices with enhanced mobility. Most importantly, high quality gate oxides can be grown on strained silicon [7].

1.3 Silicon on Insulator (SOI) MOSFETs

Silicon on insulator (SOI) is an emerging technology offering numerous advantages in device performance. These advantages make SOI an attractive technology for the continued scaling of MOSFETs. However, the fabrication of fully depleted SOI devices that fully utilize the advantages of SOI presents challenges.

1.3.1 Advantages of SOI

Devices fabricated on SOI provide many performance advantages. The buried oxide acts as isolation from the substrate. Thus, active devices are isolated from parasitic substrate effects. This isolation from the substrate makes latch-up virtually impossible. It also makes SOI transistors more resistant to radiation effects because electron/hole pairs are generated primarily in the silicon substrate and are isolated from the active devices. In many SOI devices, the source and drain regions extend fully to the buried oxide. This minimizes the junction surface area, leakage

current, and junction capacitance. Implications of these reduced parasitics include improved speed, lower power dissipation, and reduced short channel effects. It is possible to achieve near ideal sub-threshold behavior (i.e. 60mV/dec) in SOI devices. While devices fabricated in SOI do have many advantages, there are some disadvantages such as increased self heating, increased hot carrier effects, and lower breakdown voltages. Most of these disadvantages can be eliminated by operation of the transistor at low voltage [8-10].

1.3.2 Fabrication of Silicon on Insulator Layers

There are three major competing methods for SOI formation: wafer bonding and etch back [11,12], hydrogen induced delamination [13] and SIMOX [14-16] as shown schematically in figure 1.7a-c respectively. Each method has both advantages and disadvantages in process complexity and material quality.

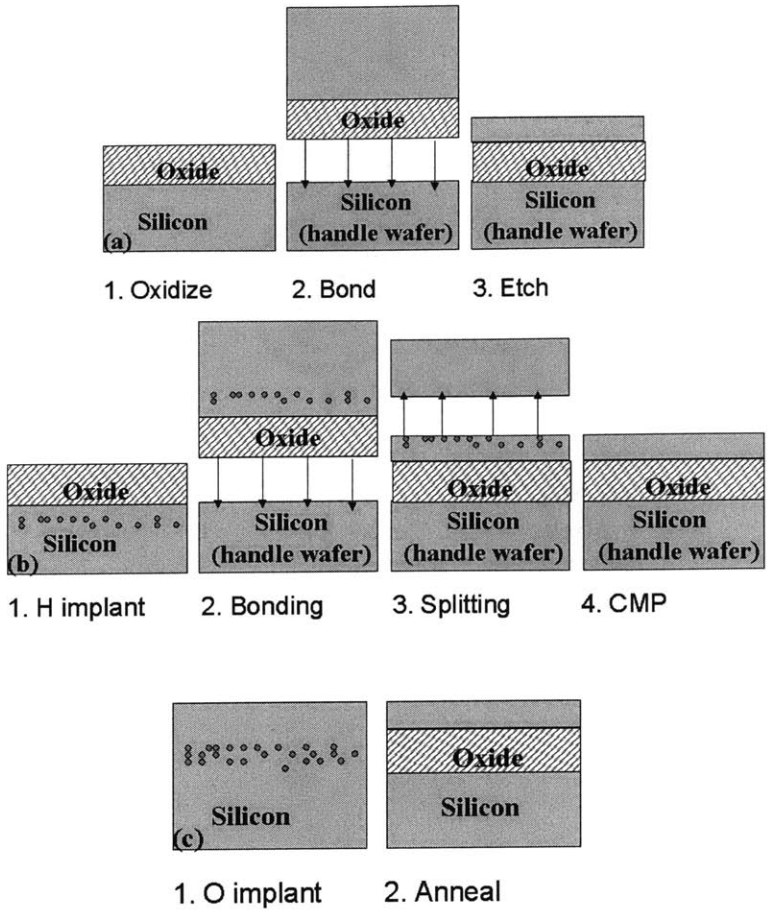


Figure 1.7 – Buried oxide formation by varying methods: (a) waferbonding and etchback [11,12], (b) Smart-cut [13] and (c) SIMOX [14-16]

The first and most traditional method of SOI formation is wafer bonding and etch back. In this method, SOI formation begins with the oxidation of a silicon donor wafer. The donor wafer is bonded to a handle wafer and then thinned back. Etch stops become necessary to achieve acceptable across-wafer thickness uniformity. This method is shown schematically in Figure 1.7a. The second method for buried oxide formation is "smart-cut" or hydrogen induced delamination. This method relies on the deep implantation of a large dose of hydrogen into the donor wafer before bonding. After ion implantation, the oxidized, implanted wafer is bonded to a silicon handle wafer. During annealing, micro-cavity formation causes splitting in the ion-

implanted wafer at the peak of the hydrogen implant. CMP is used to remove surface roughness. Since the implant determines the depth of splitting, this method produces uniform thickness in the transferred silicon layer (figure 1.7b). The third method of SOI formation, SIMOX, also relies on ion implantation but in a very different manner. In this technique, a buried oxide is formed by implanting a high dose of oxygen into the substrate. With subsequent high temperature annealing at 1320C for at least 6 hours, SiO_2 is formed at the implanted layer and the silicon re-crystallizes above this layer (figure 1.7c). While this method is successful, it is limited by the quality of the oxide formed and the high thermal budget required to form the oxide.

1.3.3 Fully Depleted SOI MOSFETs

Fully depleted SOI structures such as ultra-thin body or double-gate devices provide many benefits for the sub-50 nm regime. "Fully depleted" implies that the depletion region extends through the entire transistor body and will not extend with additional gate bias. Two examples of fully depleted SOI MOSFETs are the ultra thin body MOSFET and the double gate MOSFET as shown schematically in figure 1.8.

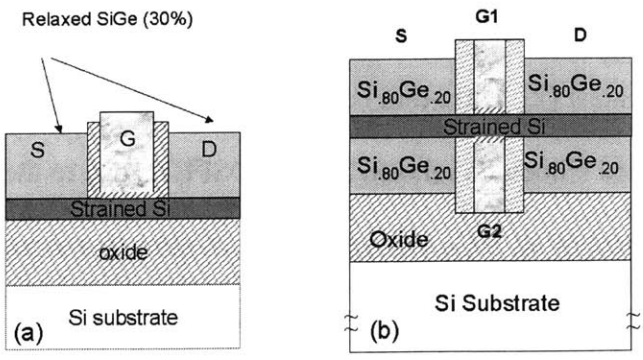


Figure 1.8 – Schematic representation of (a) ultra thin body and (b) double gate MOSFETS with strained silicon channel layers.

It is well known that devices fabricated in SOI provide the benefit of reduced parasitic capacitance allowing for high-speed operation with minimal power dissipation. Ultra-thin body SOI devices have the added benefit of improved electrostatic integrity and suppression of short channel effects, and thus can be scaled to the shortest channel lengths [17-19]. The possibility of using lower doping in ultra-thin films is very attractive due to an increase in mobility and a reduction in the V_t roll off [8]. Ultra-thin or double-gate structures enable a reduction in bulk charge and Eeff. This is shown in the following calculations for the vertical field that applies in the case of holes [3]:

$$E_{eff} = \left(\frac{1}{\varepsilon}\right) * \left(Q_b + \left(\frac{1}{3}\right) * Q_{inv}\right)$$

$$= 0.5\ MV/cm\ for\ Q_{inv} = 10^{13}\ cm^{-2}\ and\ Q_b = 0$$

In strained silicon holes exhibit a maximum mobility enhancement at low vertical effective fields. Thus, double-gate and ultra-thin body MOSFETs when combined with strained silicon will allow greater mobility enhancements for p-MOSFETs by allowing device operation at lower effective fields where the hole mobility enhancement is greatest [2]. Ultra-thin body strained silicon devices also provide benefits over strained silicon on relaxed SiGe MOSFETS due to the elimination of germanium. Removal of all SiGe during creation of ultra-thin strained silicon directly on insulator layers eliminates the problems associated with the presence of Ge, such as Ge diffusion into the Si, limited thermal budget, and enhanced dopant diffusion.

1.4 Material Constraints Due to Thin Strained Si Film

In order to combine the benefits of fully depleted SOI with those of strained silicon, thin strained silicon on insulator substrates must be fabricated with high material quality.

It has been shown that the electron and hole mobility of thin unstrained SOI MOSFETs is independent of film thickness when the silicon thickness is greater than 50 nm [20]. However, with further reduction in silicon thickness below 10 nanometers, severe mobility degradation can be observed due to material and interface quality [21]. Ultra-thin silicon n-MOSFET mobilities of 210 $cm^2/V*s$, 260 $cm^2/V*s$, and 650 $cm^2/V*s$ were observed for silicon thicknesses of 3 nm, 5 nm, and 45 nm respectively [22]. This places tight requirements on the silicon thickness of SOI layers to avoid degradation of device performance. Since the thickness of the device layer in thin SOI has this type of impact, across wafer thickness uniformity must be carefully controlled to avoid mobility variation across the wafer. Due to critical thickness constraints of epitaxial growth, the thickness of strained silicon films is limited. For example, at 30% germanium in the underlying relaxed SiGe, the critical silicon thickness is about 150A. After silicon loss due to cleaning and device fabrication, the final channel thickness will be very thin and small variations may have a large influence on device behavior.

As this silicon film is aggressively scaled, the short-range variation in film thickness (roughness) also becomes critical. SOI thickness variation down to a

couple of atomic layers can have a significant impact on mobility and threshold voltage in ultra-thin (less than 4 nm) relaxed SOI MOSFETs due to surface roughness scattering [22,23]. Therefore, the short-range roughness should be minimized. This type of roughness is best characterized by root mean square (RMS) roughness values obtained via atomic force microscopy (AFM) and by transmission electron microscopy (TEM).

Coulomb scattering at the back interface of the silicon with the buried oxide can also lead to a decrease in the mobility of electrons and holes in the thin silicon channel. Thus, the quality of the backside interface is very important [24]. There are two approaches to backside interface formation as shown in figure 1.9.

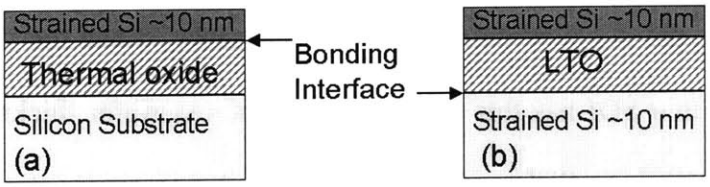


Figure 1.9 – Bonding interface location using (a) silicon bonded directly to thermally oxidized handle wafer (b) LTO deposited and CMP'd on strained silicon wafer then bonded to CZ silicon handle wafer

The first approach is to create a high quality thermal oxide that can be directly bonded to the strained silicon layer. This gives the benefit of providing a high quality buried oxide layer, but places the bonding interface and any contaminates from bonding at the back interface of the silicon channel. The second approach is to deposit low temperature oxide (LTO) on the silicon surface and then bond the wafer.

This will place the bonding interface far from the channel layer, but necessitates the use of a lower quality deposited oxide.

In addition to creating thin, uniform layers with low roughness, it is also important to consider how the strain in the silicon will be affected by layer transfer and annealing. Strained silicon is traditionally grown on thick relaxed SiGe layers. Due to the lattice mismatch between SiGe and Si, biaxial tensile strain is induced in the thin silicon layer. The main concern in fabricating strained silicon on insulator is whether the strain will relax when the strain-inducing SiGe is removed.

Another critical issue for SSOI MOSFETs is channel doping. Fully depleted SOI device structures also enable reduction of channel doping compared to bulk MOSFETs. In order to enjoy the full benefits of strain enhancement, channel-doping concentration must be kept below 5 x 10^{18} cm^{-3} to operate at low vertical effective field [25]. Therefore, use of SOI is advantageous.

1.5 Previous Implementations of Strained Silicon on Relaxed SiGe on Insulator

There have been previous attempts to combine the advantages of strained silicon and SOI. Previous implementations have relied on the formation of the SiGe layer on insulator and the re-growth of a strained silicon layer for the channel. In contrast, this work demonstrates the transfer of a thin strained silicon layer directly to insulator, thus eliminating the intermediate SiGe layer entirely. These two implementations are shown in figure 1.10.

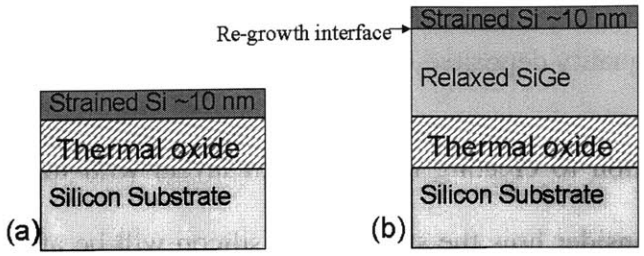


Figure 1.10 – Use of epitaxial heterostructures to combine the benefits of strained silicon and SOI technologies (a) strained silicon directly on insulator fabricated in this work and (b) strained silicon on SiGe on insulator fabricated in previous work. Strained Si directly on insulator enables fabarication of ultra-thin body MOSFET, while the structure in (b) does not.

Cheng et al. at MIT developed a "smart-cut" type process for the transfer of relaxed, epitaxial SiGe to an oxidized substrate. Due to the implant depth of hydrogen, the transferred SiGe layers are relatively thick, ~630 nm with 20-25% Ge. If desired, these SiGe layers can be thinned via CMP before the growth of the ~15 nm strained silicon channel layer [26]. Tezuka et al. has demonstrated another method for fabrication of strained silicon on insulator using an intermediate SiGe layer. This process involves the growth of a SiGe layer on an SOI substrate. During thermal oxidation of SiGe, the Ge atoms are rejected and condensed, forming a SiGe layer of higher Ge fraction on insulator. Layers with up to 56% Ge have been demonstrated, but these layers are not fully relaxed. Therefore, an apparent Ge fraction of 24% is observed by Raman analysis [27,28]. Devices fabricated in such strained silicon on SiGe on insulator layers demonstrate mobility enhancements comparable to those of strained silicon bulk MOSFETs [29,30].

1.6 Directions for This Work – Creation of Ultra-thin Strained Silicon Directly on Insulator Substrates

The prospect of combining strained silicon with ultra-thin body or double gate MOSFETs motivates the creation of thin strained silicon on insulator. Previous implementations of strained silicon on insulator have relied on the transfer of thick,

epitaxial SiGe onto and oxidized handle wafer followed by a re-growth of strained silicon [26]. Although this configuration does offer some benefits over strained silicon on a SiGe substrate, it does not enable the fabrication of ultra-thin body strained Si MOSFETs. In addition, strained Si/relaxed SiGe on insulator structures do retain all the problems associated with the Ge underneath the channel, such as Ge diffusion into the Si, limited thermal budget, and enhanced dopant diffusion. In this work, thin strained silicon layers were fabricated directly on insulator, entirely eliminating the SiGe from the final structure. Such layers were investigated for material quality, thickness uniformity, and strain behavior. The key question in fabricating strained silicon directly on insulator is whether the strain in the silicon will remain after the strain-inducing SiGe layer is removed and how the strain will be affected by thermal cycling which is required for MOSFET fabrication.

Chapter 2

FORMATION OF STRAINED SILICON ON INSULATOR

The prospect of combining the benefits of strain induced mobility enhancement and reduction of short channel effects from ultra-thin body or double-gate device design motivates the formation of thin strained silicon on insulator layers. This chapter describes the design and fabrication of ultra-thin strained silicon on insulator. First, a description of the growth of an epitaxial heterostructure designed for layer transfer including two etch stop layers is presented. Next, the bonding and etch back processes are described. Finally, the thin strained silicon on insulator layer is characterized for uniformity and strain in the transferred material is verified.

2.1 Introduction

Strained silicon on insulator was formed in this work using a flip, bond, and etch technique. An epitaxial heterostructure including two built in etch stop layers and with strained silicon on top is grown via ultra-high vacuum chemical vapor deposition (UHVCVD). This epitaxial wafer is flipped and bonded to an oxidized handle wafer. Grinding removes 500 um of the initial substrate. Selective etching removes the remaining layers to leave only the layers of interest (figure 2.1).

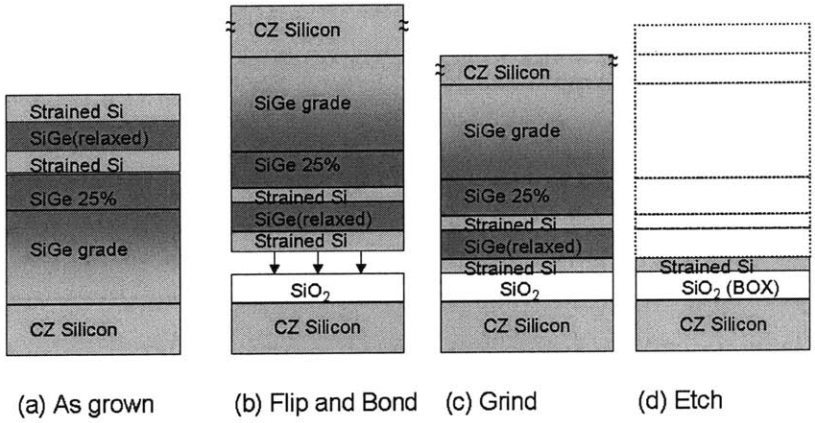


Figure 2.1 – Basic process for SSOI formation via flip bond and etch-back technique. An epitaxial heterostructure is (a) grown and then (b) flipped and bonded to an oxidized handle wafer. Finally the un-needed layers are removed by (c) grinding and (d) and selective etching.

2.2 Epitaxial Growth

All epitaxial material used in this work was grown by M. Lee and A. Pitera in the Department of Materials Science and Engineering at MIT. A compositionally graded SiGe buffer layer was deposited by ultra-high vacuum chemical vapor deposition (UHVCVD) on a 4 inch p- <100> CZ silicon substrate with a grading rate

of 10% Ge / μm and a final germanium content of 29%. A two μm-thick layer of fully relaxed $Si_{0.71}Ge_{0.29}$, then caps this buffer layer. The $Si_{0.71}Ge_{0.29}$ layer has a large RMS roughness of ~10 nm due to the strain fields in the graded buffer layer. This "crosshatch" is shown via Nomarski micrograph in figure 2.2.

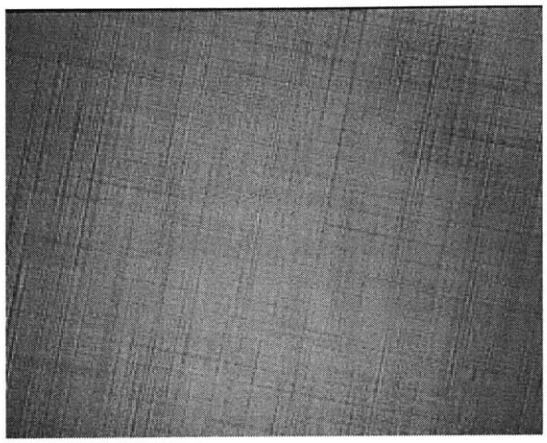


Figure 2.2 – Nomarski micrograph of SiGe graded buffer layer with crosshatch evident on the surface. Crosshatch is formed due to strain fields in the graded buffer layer.

The crosshatch can also be observed by atomic force microscopy (AFM) imaging as shown in figure 2.3. After the growth of a graded buffer layer, the crosshatched surface of the SiGe is very rough. In this scan an RMS roughness of ~9 nm is observed.

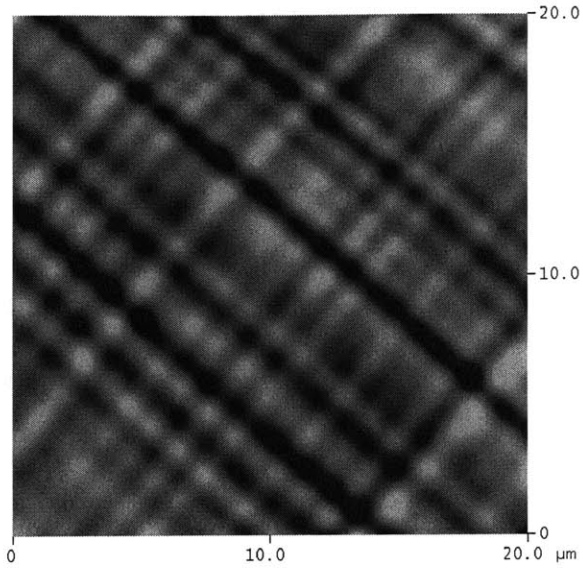


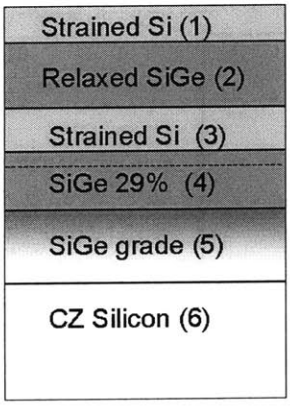
Image Statistics

Img. Z range	58.862 nm
Img. Mean	0.165 nm
Img. Raw mean	1.371 µm
Img. Rms (Rq)	9.095 nm
Img. Ra	7.349 nm
Img. Rmax	58.802 nm
Img. Srf. area	400.15 µm²
Img. Prj. Srf. area	400.00 µm²
Img. Srf. area diff	0.037 %

Fig. 2.3 - AFM scan of relaxed SiGe surface. Roughness analysis shows an RMS roughness of ~9 nm on a 20um square scan. This roughness is typical of SiGe relaxed buffer layers.

Chemical mechanical polishing (CMP) removes ~1 um of the $Si_{0.71}Ge_{0.29}$ cap layer. This eliminates the crosshatch reducing surface roughness [31-34]. A post CMP clean is necessary to remove contaminates such as potassium, sodium, and metals from the wafer surface. A full explanation of post-CMP cleaning and contamination data can be found in Appendix A. A typical post-CMP clean before epitaxial re-growth consists a double piranha clean of 5 minutes H_2O_2:H_2SO_4 (1:3), 15-second HF dip, and 5 minutes H_2O_2:H_2SO_4 (1:3). This double piranha clean is followed by a modified RCA as follows: 10 minute H_2O_2:H_2SO_4 (1:3) + 15 second

HF dip + 15 minute H_2O:H_2O_2:HCL + SRD. After cleaning, remaining epitaxial layers are grown to form the "as grown heterostructure" shown in figure 2.4. This re-growth consists of approximately 200 nm of relaxed $Si_{0.71}Ge_{0.29}$, a thin ~10 nm strained Si etch stop layer, and a 150 nm relaxed $Si_{0.71}Ge_{0.29}$ layer separating the Si etch stop from the 15 nm-thick strained silicon channel. Since less than 300 nm of material is re-grown after CMP, the resulting roughness is limited [32]. All epitaxial material was grown by M. Lee and A. Pitera in the Department of Materials Science and Engineering at MIT.



#	Material	Thickness	Use
1	Strained Si	~13 nm	Channel
2	SiGe Relaxed	~150 nm	Induce strain
3	Strained Si	~10 nm	Etch Stop
4	SiGe 29% (relaxed)	~1um	Induce strain --- CMP interface
5	SiGe grade	~2-3um	Contains etch stop of 22% Ge
6	CZ Si	~550um	Initial substrate

Figure 2.4 - As grown epitaxial heterostructure for creation of ultra thin strained silicon directly on insulator via a bond and double etch stop process.

2.3 Bonding

Bonding of SiGe is nontrivial due to crosshatch on the SiGe wafer. Two approaches to the formation of buried oxide dependent on planarization method are shown in figure 2.5.

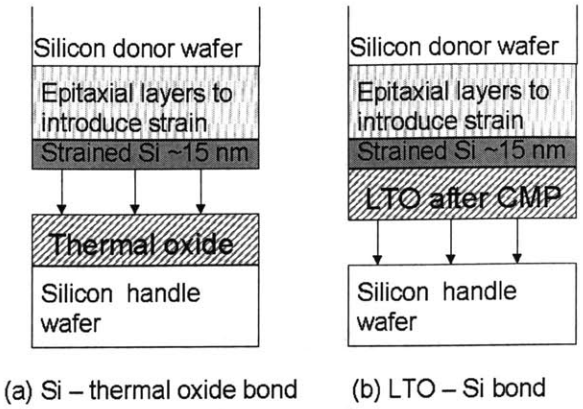


Figure 2.5 – Two bonding methods based on planarization method. (a) Strained silicon epitaxial wafer is bonded directly to a handle wafer with thermal oxide (b) LTO is deposited on the epitaxial wafer and CMP is used to smooth the surface before bonding to a CZ silicon wafer.

The first method is to grow thermal oxide on the handle wafer and bond the epitaxial wafer directly to the thermal oxide. This provides the processing benefit of fewer process steps, and therefore, fewer opportunities to accumulate particles on the wafer that will cause void formation during bonding. Wafers with significant crosshatch, such as those with high Ge content or without CMP during growth, will exhibit RMS roughness that is too large to enable reliable bonding. Therefore, a second method was also used in this work for the formation of the buried oxide. This method involves depositing low temperature oxide (LTO) onto the epi wafer, planarizing the LTO via chemical mechanical polishing (CMP) and then bonding to a handle wafer.

Wet chemistries remove particles and activate the surface before bonding. A typical surface preparation is 10 minutes H_2O_2:H_2SO_4 (1:3), DI rinse, 3-second HF dip, DI rinse, 7 minute H_2O:H_2O_2:HCL (5:1:1), DI rinse, 5 minute H_2O_2:H_2SO_4 (1:3)

followed by a DI rinse and 10 minute spin-rinse-dry (SRD) cycle. H_2O_2:H_2SO_4 is substituted for the typical H_2O:H_2O_2:NH_4OH (SC1) during RCA activation process to reduce the loss of Si from the strained silicon channel layer.

Bonds are established at room temperature. The bonded pair is annealed in nitrogen ambient for 3 hours at 400°C followed by 1 hour at 600°C. In figure 2.6, the difference in void density is evident between a wafer including and a wafer omitting the low temperature annealing step.

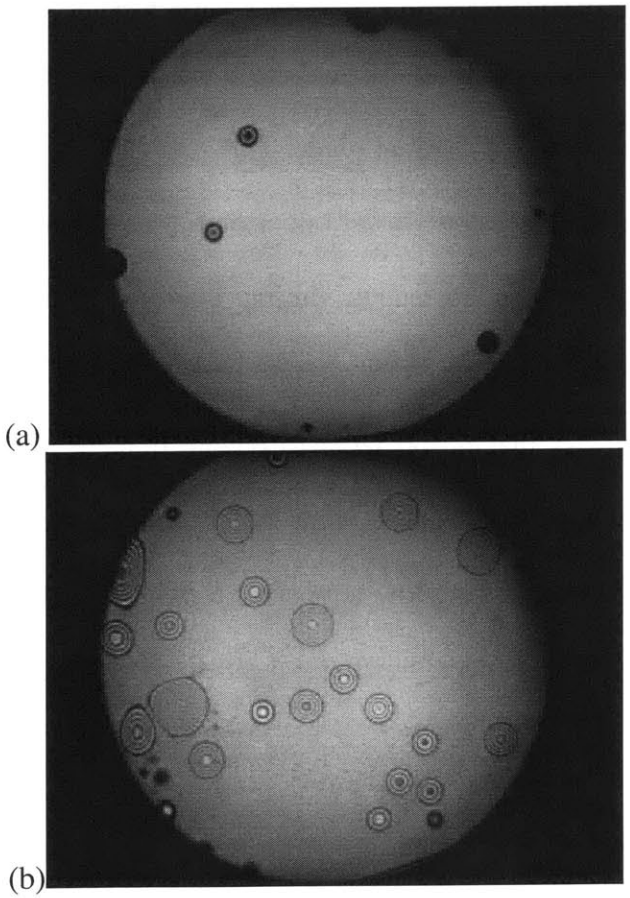


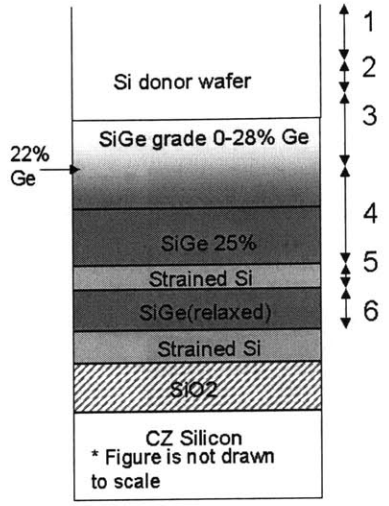
Figure 2.6 – IR camera images of voids after wafer bonding and annealing, illustraing how bonding results depend on annealing conditions. (a) Annealing including a low temperature step for diffusion of trapped gasses from the interface to limit void formation. (b) Annealing without low temperature step results in void formation.

The low-temperature annealing step allows gasses trapped at the bonding interface to diffuse from the bonding interface so voids will not form when the sample is annealed at higher temperatures. The subsequent higher temperature anneal is used to increase bond strength. After annealing bond strengths were measured using a simple razor blade test. In this test, a razor blade is inserted between the wafers at the bonding interface. This causes de-bonding of the two wafers. The crack propagation over time can be measured and compared to a control wafer. In this work, bond strengths comparable to CZ Si bonded to thermal oxide using the same bonding procedure and anneal are achieved.

2.4 Grind and Etch back

After bonding, the donor substrate is removed by wafer grinding. Grinding and Dicing Services Inc. (GDSI, Sunnyvale, CA) completed all wafer grinding. Wafer grinding removes ~500 μm of the silicon donor wafer, resulting in a total thickness variation (TTV) of 5 - 10 μm across a four inch wafer. After grinding, CMP in the MIT Microsystems Technology Laboratory is used to remove the grinding-induced roughness from the wafer surface. This CMP step removes approximately 1 um of silicon. After CMP, the wafer is completely hydrophobic whereas before CMP water would wet in a pattern of the grinding due to deep groves in the silicon. The thickness non-uniformity induced by grinding is removed by the series of selective etches, leaving only 13 nm of strained silicon directly on oxide. The entire process is summarized in figure 2.7.

The series of selective etches begins with tetra-methyl ammonium-hydroxide (TMAH). TMAH selectively etches Si and stops at 22% Ge. This first etch stop is based on the germanium fraction and is located in the SiGe graded buffer layer [35]. TMAH highlights stress patterns in the SiGe films; therefore, CMP is used to reduce the surface roughness after TMAH. After observing a necessary two hour stabilization time, a mixture of $HF:H_2O_2:CH_3COOH$ (1:2:3) selectively etches the remaining SiGe layer and stops on the 10 nm-thick strained Si etch stop layer [36]. A selectivity of 23:1 (SiGe:Si) is observed for this etch with a SiGe etch rate of 40.3 nm/min. This selectivity is adequate to stop on the thin etch stop layer. A TMAH dip removes the 10 nm-thick strained Si etch stop layer. $HF:H_2O_2:CH_3COOH$ or $H_2O:H_2O_2:NH_4OH$ is then used to etch the final 150 nm-thick SiGe layer. $H_2O:H_2O_2:NH_4OH$ is preferred because the etch rate of SiGe is 2.7 nm/min, over 10 times slower than the etch rate in $HF:H_2O_2:CH_3COOH$, allowing for a more controlled etch while still offering an adequate selectivity of 18:1 (SiGe:Si).



Step #	Removal Method	to remove	to stop on
1	grinding	500 um Si	desired thickness
2	CMP	~1um Si	removal of grinding roughness
3	TMAH	~50 um Si	22% Ge in buffer layer
4	$HF:H_2O_2:CH_3COOH$	~ 1 um SiGe	Si etch stop
5	TMAH	100 A etch stop layer	SiGe
6	$H_2O:H_2O_2:NH_4OH$	~1500A SiGe	Si channel

Figure 2.7 – Grind and etch back process. Dual etch etop layers are used to improve across wafer thickness uniformity.

2.5 Material Characterization

Various strained silicon on insulator (SSOI) layers were fabricated to investigate material properties such as across wafer thickness uniformity, strain, and roughness. XTEM micrographs are also presented.

2.5.1 Layer Structures of Interest

Three layer structures have been investigated and fabricated as seen in figure 2.8.

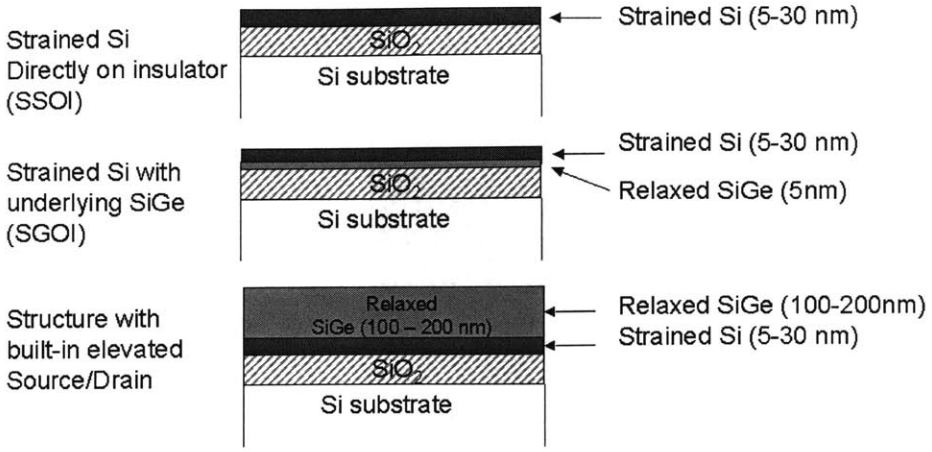


Figure 2.8 – Layer structures of interest. (a) strained silicon directly on insulator (b) strained silicon with thin intermediate SiGe layer on insulator (c) strained silicon on insulator with relaxed SiGe above the silicon.

The first structure of interest, shown in figure 2.8a, consists of a thin strained silicon layer directly on insulator. This structure is very appealing for fabrication of ultra-thin body MOSFETs because it eliminates many of the problems associated with the presence of germanium such as enhanced dopant diffusion and germanium diffusion into the channel region. Even though it is not beneficial to have germanium present for most device purposes, the presence of a SiGe layer could have an effect on the strain behavior of thin strained silicon films. Therefore, the second structure of interest is strained silicon on insulator with an intermediate SiGe layer. The third structure consists of a thin strained silicon layer with a 150 nm-thick SiGe layer above the silicon channel. This structure is of interest for fabrication of ultra-thin body devices where slots would be etched in the SiGe to form a gate region. This would allow the material that induced the strain to remain in all regions of the wafer except the small gate regions, as seen in figure 2.9. The SiGe raised source/drain regions could help maintain the strain in the silicon layer during processing and eliminate implanting directly into the 10 nm-thick strained silicon layer for source/drain doping.

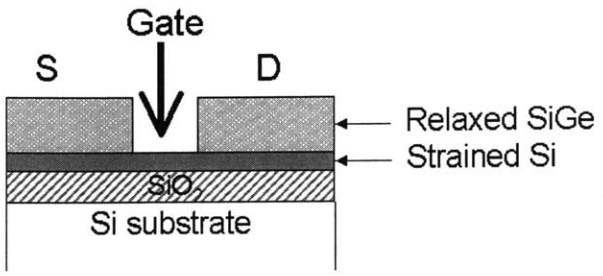


Figure 2.9 – Slot etching in strained silicon with overlying SiGe for gate region in UTB device. This structure allows the SiGe which induced the strain in the silicon to serve as raised source/drain regions.

2.5.2 SIMS and XTEM Analysis of Layer Structures of Interest

Secondary Ion Mass Spectrometry (SIMS) was used to confirm the existence of silicon and SiGe layers after transfer and etching. Ihab Abdelrihim of National Semiconductor completed this analysis. Figure 2.10 shows such an analysis for strained silicon directly on insulator during two key points in the process: just before reaching the strained silicon etch stop and after the removal of the strained silicon etch stop. It is important to note that the germanium has not significantly diffused into the etch stop or channel layers. Due to the presence of a buried oxide layer, charging effects were seen in these samples. These charging effects will shift the apparent Ge fraction, but relative step sizes in Ge fraction will remain accurate.

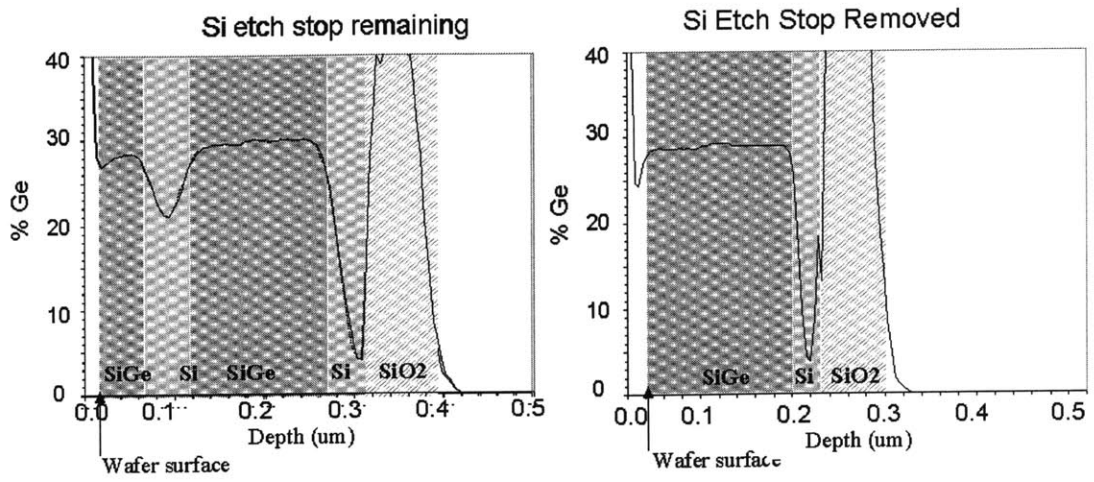
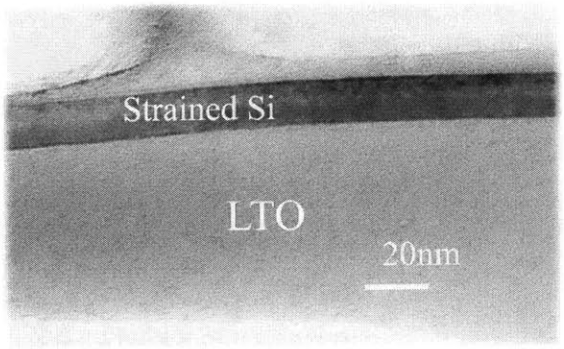
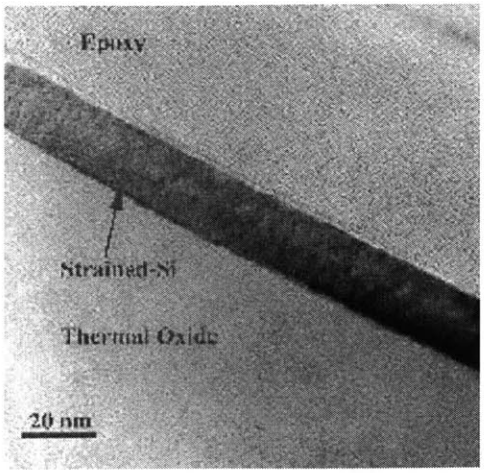


Figure 2.10 – SIMS analysis completed at National Semiconductor

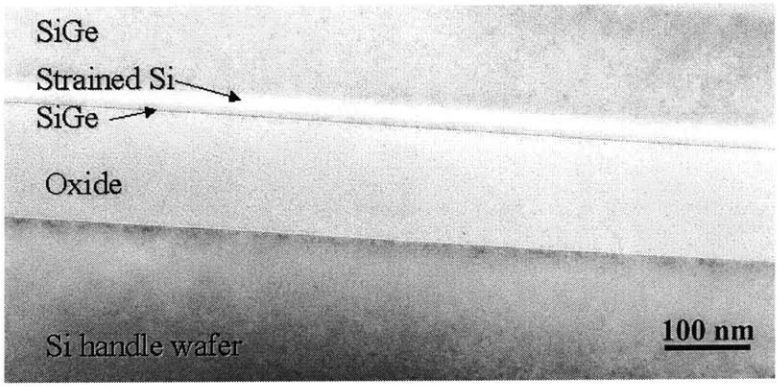
Very thin layers cannot be accurately measured via SIMS. Therefore, cross section transmission electron microscopy (XTEM) is used to evaluate the final strained silicon on insulator structures. In the strained silicon directly on insulator, a final silicon thickness of 13 nm is achieved as seen in figure 2.11.



(a)



(b)



(c)

Figure 2.11 – XTEM of strained silicon on insulator structures. (a,b) strained silicon directly on insulator (c) strained silicon on insulator with intermediate SiGe layer. XTEM courtesy of J. Li and D. Anjum of University of Virginia. The apparent bowing in (a) is due to thin-foil effects associated with the XTEM sample preparation.

Figure 2.11 shows three XTEM micrographs of strained silicon directly on insulator and strained silicon on insulator with intermediate SiGe layer. J. Li and D. Anjum prepared the XTEM samples by conventional Ar^+ ion milling at 6 KeV. The zone axis is (110). The curved interface in Fig. 2.11 is an artifact of Ar^+ Ion-milling. The smooth silicon/oxide interface seen in the XTEM images is promising for fabrication of devices in the thin SSOI wafers but it should be noted that XTEM samples only a small area of the interface.

2.5.3 Raman Analysis for Strain Determination

Raman analysis at 325 nm excitation wavelength was used to analyze the strain present in the transferred silicon films. This analysis was completed at IBM Microelectronics Division by N. Klymko with the assistance of K. Rim. The three layer structures presented in Section 2.5.1 were used to investigate the strain relaxation when the strain is maintained by different mechanisms. In all cases, the strain is induced by growth of Si on a relaxed SiGe layer. The silicon layers remain fully strained after the film transfer process in spite of the 700°C one hour anneal for bonding. A complete discussion of strain in thin silicon on insulator films and annealing is presented in chapter 4.

2.5.4 Across Wafer Thickness Uniformity

Thickness uniformity of thin SSOI layers is of great concern for the fabrication of ultra-thin body strained silicon MOSFET devices. A nanospec reflectometry measurement tool was calibrated to estimate film thickness using SIMS and TEM data. This technique worked well for film thicknesses above 100 nm, but the use of a scaling factor is necessary below this thickness. To determine the correct scaling factor for thin films, the Nanospec measurements of film thickness were compared to film thickness via TEM. A constant value is then subtracted from the measured film thickness. This error is most likely due to interference of the back interface of the buried oxide. While these film thicknesses should be representative, due to the method of measurement they will contain some

error. The use of a double etch stop for SSOI fabrication allowed substrates to be fabricated with thickness uniformity comparable to the as grown epitaxial layers. In all cases, the Si film was thinnest near the flat, as expected from the growth method. During epitaxial growth, wafers are placed in the UHVCVD reactor with the flat away from the gas source. Thus, the as grown films will be slightly thicker away from the flat, as is seen in the transferred silicon layers. A final thickness uniformity standard deviation of 3.6% is observed on the 14 nm-thick strained silicon directly on insulator sample (figure 2.12).

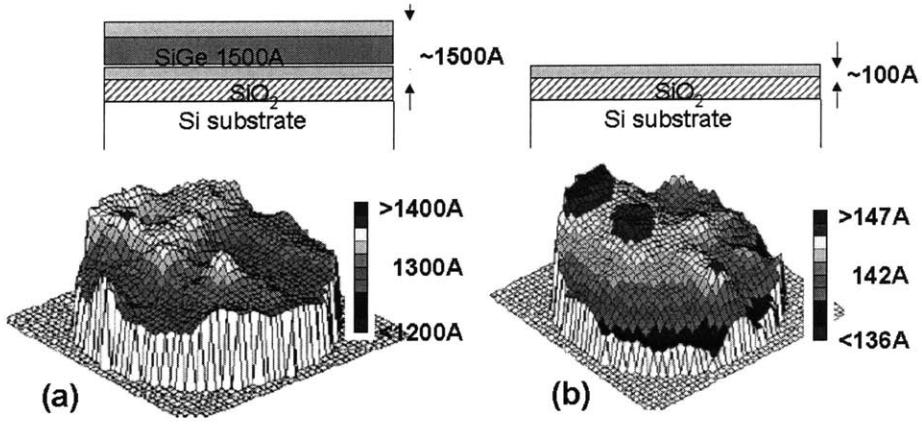


Figure 2.12 – Final across wafer thickness uniformity mapping. Thickness uniformity is believed to be limited by the initial epitaxial growth not by the film transfer process.

2.5.5 AFM Roughness Analysis

Surface roughness is also important for device fabrication in ultra-thin strained silicon on insulator layers. AFM samples of the SSOI substrates show an average RMS roughness of 0.92 nm. A three-dimensional AFM image of the silicon surface is seen in figure 2.13.

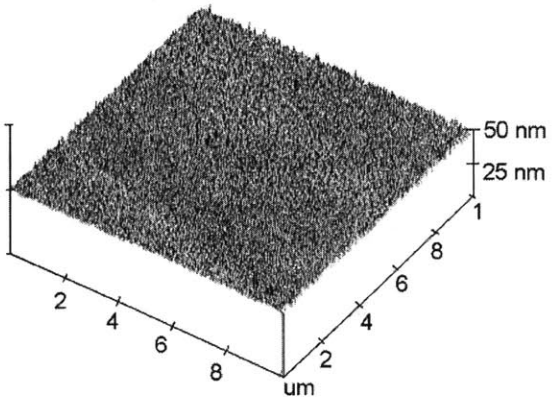
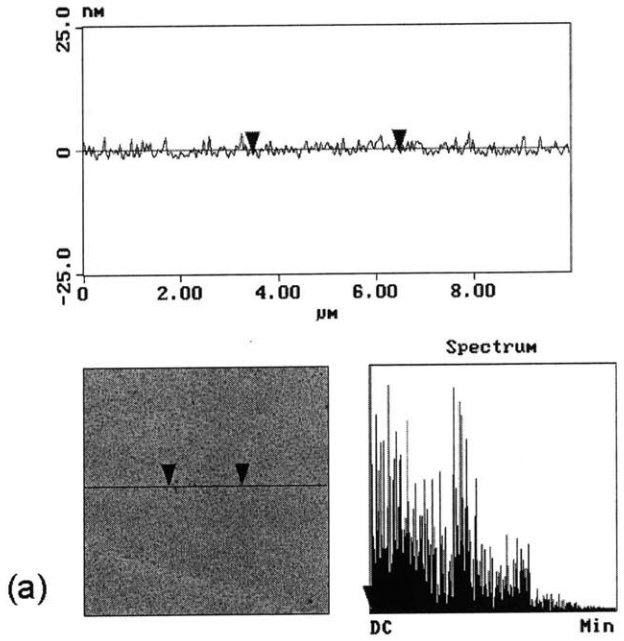


Figure 2.13 – Three dimensional AFM image of silicon surface in an ultra-thin strained silicon on insulator wafer. The average RMS roughness measured was 0.92 nm.

It is important to notice the roughness of the silicon film is short-range roughness, unlike the crosshatch-induced roughness seen for SiGe samples, which typically has a spatial period of ~ 100 to 1000 nm. A line scan comparison of the surface roughness seen on the silicon surface compared to a 25% SiGe wafer with crosshatch is seen in figure 2.14.



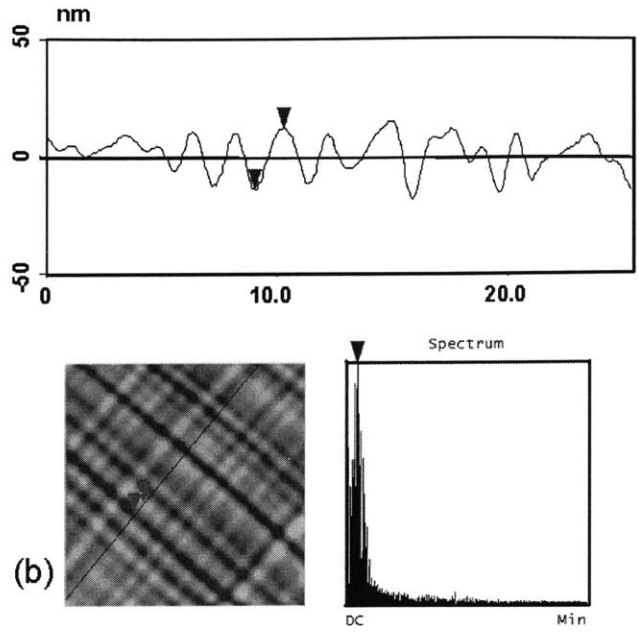


Figure 2.14 – Comparison of short-range roughness seen on the ultra-thin strained silicon on insulator surface (a) compared to the long range roughness (crosshatch) of as grown SiGe (b).

The roughness seen on the SSOI sample is due to the etching process. Optimization of the etching process could further reduce the 0.92 nm roughness. While this roughness is not extremely high, it should be further reduced for optimum device performance.

2.6 Summary and Conclusions

A bond and etch back technique for the fabrication of 13 nm-thick strained silicon directly on insulator has been developed. The use of a double etch stop allows the transfer of a thin strained silicon layer with across-wafer thickness uniformity comparable to the as grown epitaxial layers. Surface roughness of ~1 nm was achieved. Alternative etches are required for the reduction of this roughness to an acceptable level. Raman analysis confirms strain remains in the thin silicon layers after the removal of the SiGe that induced the strain. Ultra-thin strained silicon on

insulator substrates are promising for the fabrication of ultra-thin body and double-gate strained Si MOSFETs.

Chapter 3

SELECTIVE ETCHING OF SIGE AND STRAINED SI

3.1 Introduction

Selective etches are necessary to form SSOI by silicon film transfer. There are multiple constraints to be considered when choosing an appropriate etch chemistry, including etch rate, selectivity, and resulting surface quality. For creation of SSOI, the etch rate must be high enough to etch the thick layers in a reasonable time, the selectivity must allow the use of etch stop layers as thin as 100A, and the resulting surface must be suitable to MOSFET fabrication.

3.2 Selective Etching of SiGe to Stop on Si

SiGe can be selectively removed from Si using $HF:H_2O_2:CH_3COOH$ or $H_2O:H_2O_2:NH_4OH$. The selectivity of these etches is caused by the rapid oxidation of

germanium by H_2O_2. Hydrogen peroxide is a good oxidizer of germanium, but it is not a good agent for the removal of the germanium oxide from the wafer surface. Therefore, either HF or NH_4OH is added to the solution. Either water or acetic acid can be added to the etchants in order to tune the etch rate and selectivity [36,38]

3.2.1 Etching of SiGe with HF:H_2O_2:CH_3COOH

A highly concentrated solution of HF:H_2O_2:CH_3COOH (1:2:3) exhibits a high selectivity when etching SiGe and stoping on Si due to the more rapid oxidation of germanium than silicon. This room temperature etch requires a 120 minute set time for etch rate stabilization. Without allowing the necessary set time, both the etch rate and selectivity are greatly reduced. The etch rate is approximately 5-7 times higher after a 120 minute set time, this is due to the time needed for the reaction between H_2O_2 and CH_3COOH. Parker *et al.* has shown that H_2O_2 reacts with acids such as CH_3COOH to form peroxy acids, but the reaction (as shown below) is slow, even for readily soluble acids such as acetic acid. The reaction between H_2O_2 and CH_3COOH follows [37]:

$$2\ CH_3COOH + 2\ H_2O_2 \rightarrow 2\ CH_3COOOH + 2H_2O$$

This allows a reaction to occur ionizing the Ge atoms as follows [36,37]:

$$Ge + 2CH_3COOOH + 2e^- \rightarrow Ge^{+2} + 2\ CH_3COO^- + OH^-$$

The electrons needed in this reaction cause the etch rate to be slightly higher for n-type vs. p-type material. For the material doping to have an effect, the doping levels must be in the order of at least $10^{17} - 10^{18}$ cm^{-3} [36]. Therefore, for most practical uses the doping of the sample will not impact the etching. The etch rate when etching SiGe in $HF:H_2O_2:CH_3COOH$ increases exponentially with Ge content. As the Ge content increases, the number of exposed Ge surface atoms also increases allowing the oxidation to occur more easily.

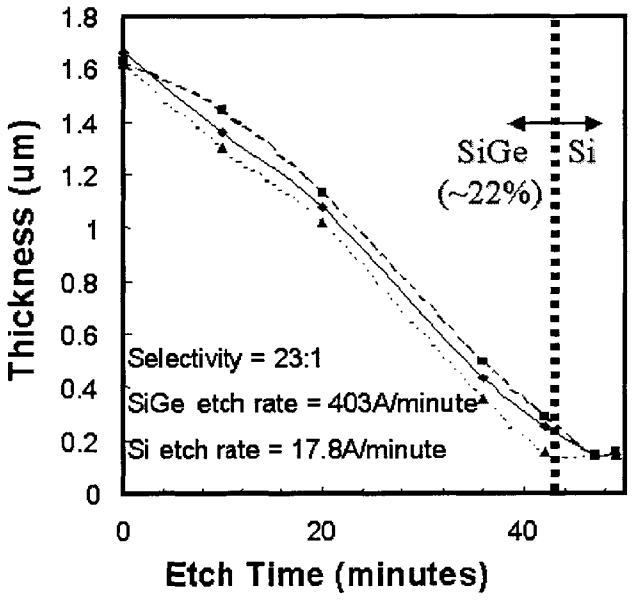


Figure 3.1 - $HF:H_2O_2:CH_3COOH$ etch chart. $HF:H_2O_2:CH_3COOH$ selectively etches SiGe and stops on Si with a selectivity of 23:1.

A selectivity of 1100:1 (SiGe:Si) has been demonstrated by Carns for films with 60% germanium [36]. In this work, thick (~1.5 um) relaxed, single crystal $Si_{.75}Ge_{.25}$ films were etched to stop on thin ~10 nm-thick strained silicon etch stop layers as seen in figure 3.1. The etch rate of $Si_{.71}Ge_{.29}$ in $HF:H_2O_2:CH_3COOH$ (1:2:3) is

observed to be 403 Å/minute while the etch rate of silicon is only 17.8 Å/minute. The selectivity of $Si_{.71}Ge_{.29}$:Si is 23:1. This selectivity allows thin strained silicon layers, <100A, to be used as etch stops.

3.2.2 Etching of SiGe with H_2O:H_2O_2:NH_4OH

Although, HF:H_2O_2:CH_3COOH provides excellent selectivity, the etch rate is excessively high and it is not selective to oxide. For many processing applications the SiGe films will need to be selectively masked and etched. For this reason, many other chemicals have been investigated, including H_2SO_4, H_3PO_4, HNO_3, and N_4OH. Only NH_4OH when combined with H_2O and H_2O_2 provides selectivity to etch SiGe with respect to Si and SiO_2 [38]. For etching of thin SiGe layers, a more controllable etch than HF:H_2O_2:CH_3COOH is needed. To meet both of these needs, H_2O:H_2O_2:NH_4OH (5:1:1, 80C) provides a slower etch rate, while still providing adequate selectivity to both Si and SiO_2. This is the same chemistry commonly used for the first step (SC1) of a pre-diffusion clean.

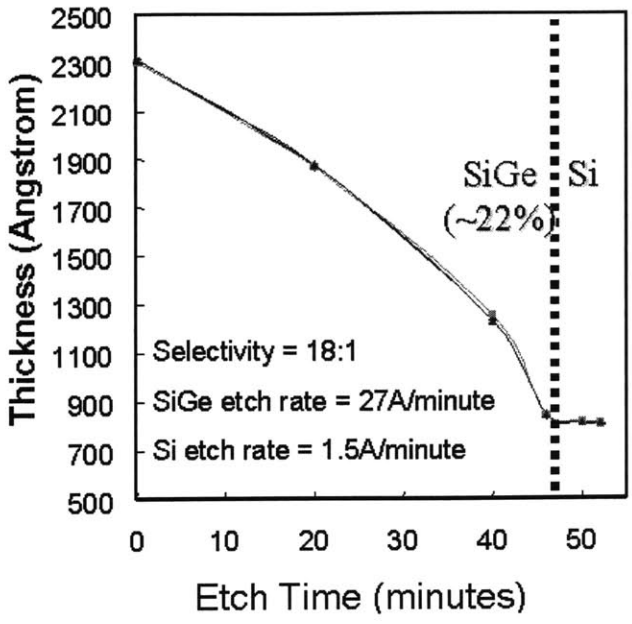


Figure 3.2 - H_2O:H_2O_2:NH_4OH etch chart. H_2O:H_2O_2:NH_4OH selectively etches SiGe and stops on Si with a selectivity of 18:1.

The etch rate of $Si_{.75}Ge_{.25}$ in H_2O:H_2O_2:NH_4OH (5:1:1) is observed to be 27A/minute while the etch rate of silicon is only 1.5A/minute. H_2O:H_2O_2:NH_4OH (5:1:1) has a selectivity of 18:1 ($Si_{.75}Ge_{.25}$:Si) as seen in figure 3.2. This selectivity is exponentially proportional to the Ge fraction. These etch rates are in agreement with those observed by others [38].

3.3 Selective Etching of Si to Stop on SiGe

Anisotropic etching of Si for micro-electromechanical systems (MEMS) purposes has been studied in detail over the past decade. Tetramethylammonuim hydroxide - $(CH_3)_4NOH$ (TMAH), and KOH are two popular etches providing reasonable etch rates and selectivity, but both are known to roughen the silicon surface.

3.3.1 Etch Characteristics of TMAH

A great amount of research has been completed to characterize etching characteristics of TMAH. The dependence of the etch rate and resulting surface on factors such as concentration, temperature, and agitation have been documented [39-43]. One key property of TMAH is an extremely high selectivity to oxide. While this can be a benefit for ease of masking, when etching blanket films, native oxide can inadvertently mask small areas. Therefore, an HF dip prior to etching is necessary to remove native surface oxide. The etch rate of silicon in TMAH is also highly dependent on the concentration, as shown in figure 3.3.

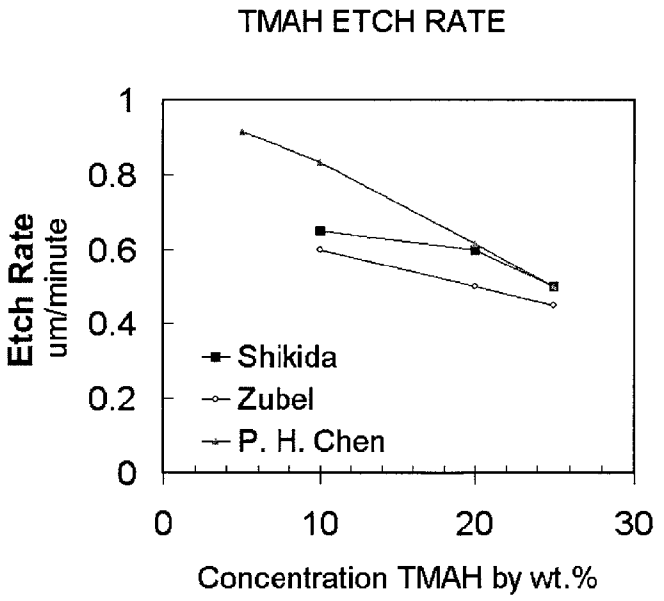


Figure 3.3 – Silicon etch rate dependence on TMAH concentration [40-41, 43].

For example, a silicon etch rate using 10% by weight TMAH is approximately 33% greater than that obtained using 25% by weight TMAH. Therefore, in order to keep a

constant, predictable etch rate, a reflux condenser is used. As the name implies, a reflux condenser will condense vapors which would typically evaporate into the air and return it to the etching solution, keeping the concentration more constant in the etch bath. For all etching temperatures, the etch rate of TMAH drops as the TMAH concentration is increased above 8% by weight. The maximum etch rate of TMAH occurs at about 4-5% by weight.

Although a maximum etch rate occurs for low TMAH concentrations, it may not be favorable to use such concentrations for silicon etching because of surface roughness. For TMAH concentrations below 20% by weight pyramids, called hillocks, bounded by the <101> ledges near the {111} planes will form. There is a positive correlation between the dissolved silicon in the etch solution and hillock formation. At high silicon content the {101} plane is etched slower than the {100}. Thus, as the TMAH concentration decreases the dissolved silicon content increases. The pyramids disappear for TMAH concentrations above 20% by weight and can be adverted by refreshing the etchant during silicon removal [41]. A silicon wafer surface etched for a long period in TMAH is displayed in figure 3.4. The non-uniformity of the surface is readily observed.

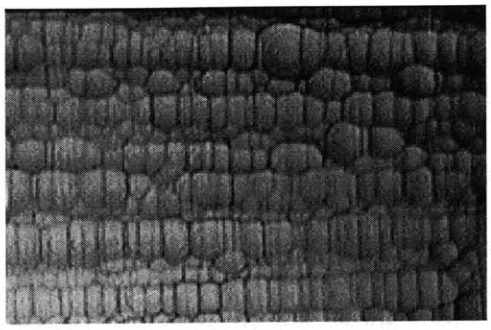


Figure 3.4 – TMAH etching induced surface non-uniformity shown for a silicon wafer etched in TMAH for 4 hours, removal of ~100μm.

TMAH, being an organic etchant, must be cleaned after etching in order to ensure organic compounds are removed from the wafer surface. A typical post-TMAH clean would include Piranha, followed by SC1 to remove organics.

3.3.2 Advantages and Disadvantages of vs. TMAH

KOH is another silicon etch that selectively etches silicon and stops on SiGe. Much like TMAH, KOH is has a high etch rate that can be modulated by concentration (figure 3.5) [39-40, 42, 44-47].

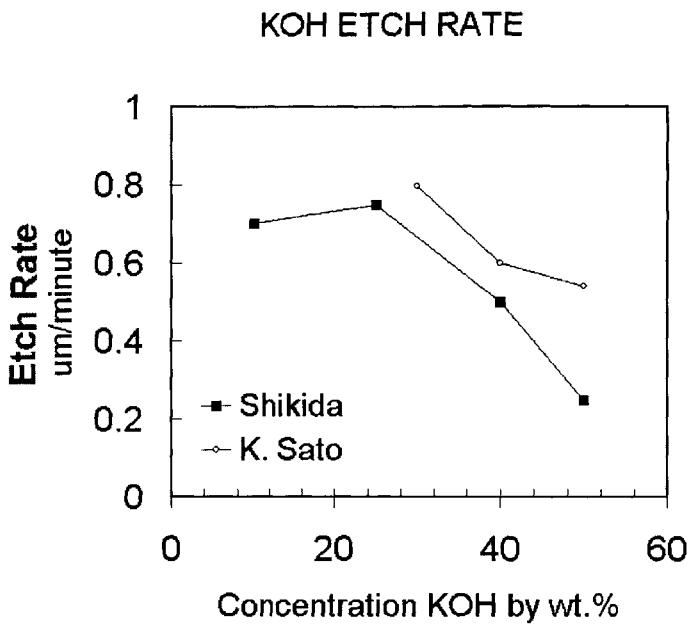


Figure 3.5 – Silicon etch rate in KOH with varying KOH concentrations [40,44]

KOH is much less expensive than TMAH, making it a financially attractive option for many fabrication needs, but it is less CMOS compatible than TMAH. KOH is an inorganic compound that is not fully CMOS compatible due to mobile alkali metal ion contamination from the potassium. Therefore, if KOH is used, extensive cleans must follow to remove contamination. A typical clean for KOH contamination removal would consist of Piranha (H_2O_2:H_2SO_4) followed by a full RCA. KOH also exhibits surface roughness dependencies similar to those of TMAH, as the concentration of KOH decreases the roughness increases for long etches. Although the same dependence exists, silicon samples etched in KOH with etch depths of 43-85 um exhibit four times less roughness than comparable etch depths in TMAH [40].

3.3.3 Addition of IPA for Reduction of Silicon Surface Roughness

Isopropyl alcohol (IPA) can be used as an additive to TMAH and KOH solutions to improve surface roughness when etching 10-100 μm of silicon films [43]. Previous work on roughness dependence was completed using long, timed

etches removing 10-100 μm of silicon, and may not directly apply to the removal of very thin ~10 nm thick strained silicon layers. In order to determine an appropriate etch to remove thin etch stop layers of strained Si and stop on SiGe, various mixtures of TMAH, KOH and IPA were used to etch ~10 nm of strained silicon on relaxed SiGe wafers. AFM measurements of RMS roughness and mean roughness before and after etching are summarized in table 3.6.

Etchant	Etch Time	RMS (nm)		Mean Roughness (nm)	
		with IPA (1:1)	no IPA	with IPA (1:1)	no IPA
None	n/a		0.875		0.543
KOH (10%)	1 min.	0.786	1.578	0.499	1.142
KOH (25%)	1 min.	0.870	1.060	0.677	0.765
TMAH (25%)	1 min.	0.849	1.162	0.547	1.007

Figure 3.6 – Roughness comparison of KOH and TMAH with varying IPA ratios.

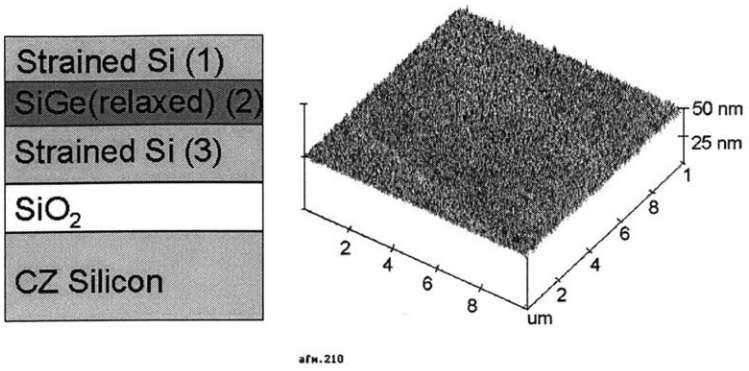
This data shows that 10% by weight KOH mixed in a 1:1 mixture with IPA provides the best surface quality. In all cases, the samples with IPA have a lower surface roughness.

3.4 AFM Evaluation of Surface Roughness Using Selective Etches for SSOI Formation

Surface roughness induced scattering is a concern in the fabrication of ultra-thin body MOSFETs. Since the roughness of the thin Si film will affect device performance, the evolution of the surface roughness during etch back was studied by AFM. AFM sample sizes ranged from 1-10 square um. The focus of the study is on the short-range non-uniformity. Short-range non-uniformity will have a greater effect on device properties than long-range non-uniformity. Results of this study are summarized in figure 3.7.

The roughness of the as grown material will be the roughness associated with the back side of the Si channel after bonding occurs. As grown epitaxial layers, such as those used to fabricate surface channel MOSFETs, (with a CMP step during the growth and limited re-growth) exhibit an RMS roughness of approximately 0.5 nm. This is mainly due to the residual crosshatch inherent to relaxed SiGe films.

The processing method and etches used to create SSOI affect the surface roughness. Grinding leaves the surface with large non-uniformities and deep scratch marks. This roughness (fig 3.6) is so large it must be removed by CMP. After grinding, TMAH is used to selectively etch the Si substrate and stop at 22% Ge. TMAH is known to roughen Si surfaces along crystalline planes and highlight stress patterns. The cross-hatched stress pattern is highlighted by the TMAH leaving a very rough surface. This roughness is removed by CMP. Next, $HF:H_2O_2:CH_3COOH$ is used to etch to the strained Si etch stop. Upon reaching the etch stop, an RMS roughness of 1.13 nm is observed. TMAH is used to remove this thin etch stop layer. This slightly roughens the surface to 2.6 nm. The final 1500A of SiGe can be removed using either $HF:H_2O_2:CH_3COOH$ or $H_2O:H_2O_2:NH_4OH$. $H_2O:H_2O_2:NH_4OH$ is preferred due to the slower etch rate and a higher quality surface. H_2O: H_2O_2: NH_4OH reduces the prior roughness to 0.92 nm versus $HF:H_2O_2:CH_3COOH$ with an RMS of 2.7 nm.



Location of Measurement	RMS (nm)
At Si etch Stop (1)	1.13
After TMAH removal of etch stop (2)	2.60
At channel using $HF:H_2O_2:CH_3COOH$ (3)	2.15
At Channel using $H_2O:H_2O_2:NH_4OH$ (3)	0.92

Figure 3.7. – Evolution of RMS roughness during SSOI formation

Key points in the surface evolution can also be seen via Nomarski microscope inspection. In figure 3.8 (a) the deep grinding-induced groves are seen. These scratch marks follow the pattern created from mechanical grinding with a diamond blade. In figure 3.8 (b), the highly crosshatched surface from the initial long TMAH etch is seen. In the final two pictures little cross-hatch remains visible. There are however, some small defects which can be seen in both (c) and (d) of figure 3.8.

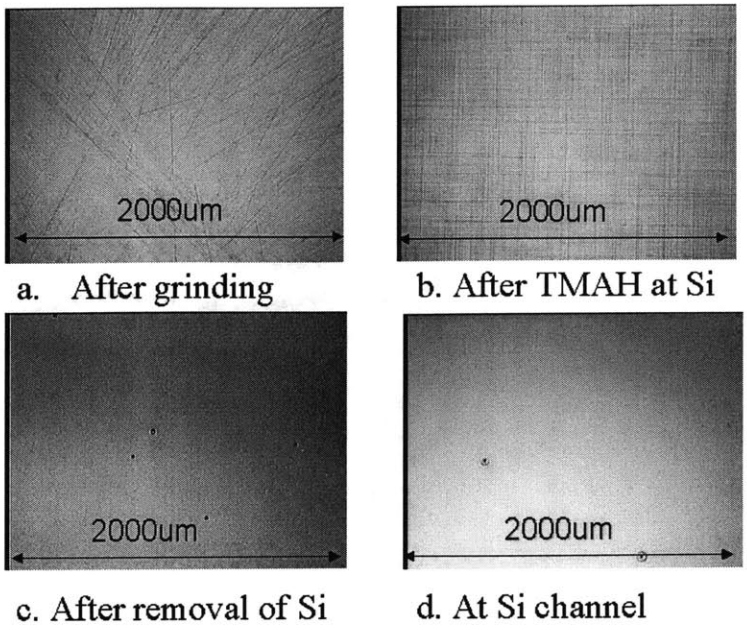


Figure 3.8 – Nomarski microscope pictures of wafer surface at (a), a fter grinding (b) at 22% Ge in the grade after TMAH Si etch (c) After SiGe etch to stop on Si etch stop and removal of the Si etch stop by TMAH (d) after final SiGe etch to stop on strained silicon channel layer

3.5 Summary and Conclusions

Various etches for removing Si on SiGe have been investigated to find suitable etches for creation of strained silicon on insulator layers. For this application, it is crucial to have high selectivity to allow stopping on thin etch-stop layers, and low RMS roughness in the resulting films. For SiGe etching both $HF:H_2O_2:CH_3COOH$ and $H_2O:H_2O_2:NH_4OH$ provide reasonable etch rates and selectivities. Both TMAH and KOH have suitable selectivity for etching of silicon to stop on SiGe, but roughen the surface of the SiGe film. With the addition of IPA to the KOH and TMAH, the roughness can be reduced by a factor of two. While this should improve the resulting roughness of the final SSOI layer from the ~1 nm RMS observed, further studies are needed to produce layers with suitable RMS roughness for device fabrication. Such work may include investigation of new wet etches as well as dry etches.

Chapter 4

STRAIN RELAXATION IN THIN STRAINED SILICON ON INSULATOR FILMS

4.1 Introduction

Raman spectroscopy can be used as a method of measuring strain in silicon and SiGe films by relying on laser excitation of atoms in the crystalline lattice [48-54]. Distinct photon modes of these crystalline lattices will emit varying radiation levels that can be collected and analyzed. Each excitation mode will produce a peak when plotted versus the wave number. Strain is then determined by measuring the shift of the SiGe or strained Si peak location from a reference silicon peak. In this work, strain is analyzed for thin strained silicon on insulator samples after the transfer process and after annealing. For device fabrication, thin strained silicon on insulator layers must be able to withstand the high temperature steps necessary for oxide formation and dopant activation. Therefore, strained silicon on insulator samples were subjected to rapid thermal annealing conditions typical for MOSFET fabrication. The maintenance of the

strain after annealing is promising for the future fabrication of MOSFETs in ultra-thin strained silicon on insulator layers.

4.2 Raman Spectroscopy

For this work, UV Raman provided the advantage of reduced excitation wavelength and thus, reduced penetration depth. Since the 325 nm laser's extinction depth is quite small, this excitation wavelength enables measurement of the ultra-thin strained silicon film without interference effects from the underlying silicon substrate [48-50,52]. All Raman spectroscopy was completed at IBM Microelectronics Division with the assistance of N. Klymko and K. Rim.

4.3 Raman Spectroscopy for Determination of Strain

Raman measurements can be used to determine germanium content and strain in $Si_{1-x}Ge_x$ and Si films [53-54]. The three major peaks of interest (silicon, SiGe, and strained silicon) are shown in figure 4.1. Each peak is measured separately due to the short extinction depth of the UV laser. The SiGe peak in figure 4.1 is fully relaxed $Si_{.71}Ge_{.29}$ and the silicon is fully strained. Increasing the biaxial tensile strain in the silicon will move the silicon peak closer to the SiGe peak. Increasing the Ge fraction will shift the SiGe peak further from the Si reference peak.

The unstrained silicon peak occurs at approximately 521 cm^{-1}. By scanning a CZ silicon wafer immediately before scanning the films of interest, this peak can

be used as a reference peak for the strained silicon or SiGe film measurements. The use of this reference peak enables the determination of precise wave number shifts, eliminating error introduced by drift of the Raman machine.

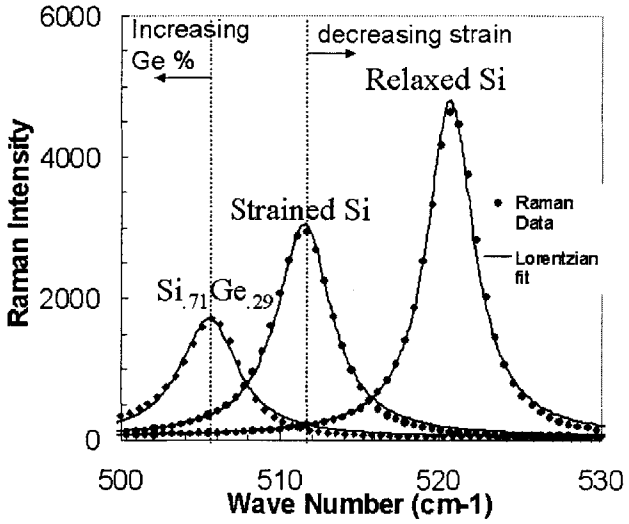


Figure 4.1 – UV Raman spectra for strained silicon on relaxed silicon. Lorentzian fit is shown as the solid line and data appears as points.

After Raman spectra are collected and background noise is subtracted out, the resulting curves can be fit by a simple Lorentzian function of the form:

$$\frac{A*\left(\frac{1}{pi}\right)*\left(\frac{g}{2}\right)}{\left((x-u)^2+\left(\frac{g}{2}\right)\right)^2} \qquad (4.1)$$

where A is the amplitude, u is the mean, and g is the half width. The extracted mean peak position, u, is used to calculate the shift in wave number. For all

layers of interest, the wave-number shift ($\Delta\omega$) will be related to the bulk (unstrained) silicon peak and defined as:

$$\Delta\omega = \omega_{\text{silicon (bulk)}} - \omega_{\text{measured}}. \qquad (4.2)$$

If the strain state of the SiGe film is known, wave-number shift values can be used to determine the apparent germanium fraction. The Raman peak shift of SiGe is linearly related to the Ge fraction [55]. Therefore, for fully relaxed films the Ge fraction (x) can be determined from [55]:

$$x = 0.030\ \Delta\omega \qquad (4.3)$$

Raman spectroscopy is an important method for determining strain in silicon layers. Similar to the case of SiGe films, the apparent Ge fraction is often used to describe the strain level in strained silicon films. In this case, the apparent germanium fraction corresponds to the germanium fraction necessary to produce the resulting amount of strain in the silicon when the silicon is grown pseudomorphically on the SiGe. For strained silicon the apparent germanium fraction can be calculated by [55,56]:

$$x = 0.0331\ \Delta\omega. \qquad (4.4)$$

The stress in the layer can be calculated using the wavenumber shift of strained silicon from the bulk, relaxed silicon [51,55]:

$$\sigma = 2.49\ \Delta\omega\ (\text{kbar}) \qquad (4.5)$$

where σ is the stress and $\Delta\omega$ is the shift in wave number. The strain, ε, in the layer can be calculated from the stress, σ, using Hooke's Law. When this equation is combined with equation 4.4 the strain can be calculated from the wave number shift as follows [51, 55]:

$$\varepsilon = 1.38 \times 10^{-3} \Delta\omega \qquad (4.6)$$

Where ε is the strain and $\Delta\omega$ is the wave number shift.

4.4 Strain in as Transferred SSOI Films

Raman analysis at 325 nm-excitation was used to analyze the strain present in the thin strained silicon directly on insulator films.

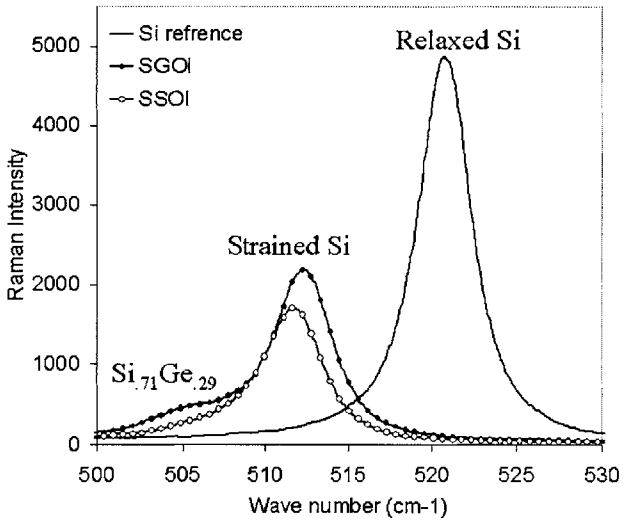


Figure 4.2 – Raman analysis of SSOI after film transfer shows that the film remains fully strained for both 13 nm-thick strained silicon directly on insulator and 13 nm-thick strained silicon on insulator with intermediate 5 nm-thick SiGe layer.

The Si peak at 521 cm^{-1} provides a reference for the strained Si peak at 512 cm^{-1}. Using the equations presented in section 4.3, the strain in the silicon and the apparent germanium fraction were calculated from the Raman spectra. Assuming the silicon is fully strained, the peak shift ($\Delta\omega$) of 9 wavenumbers corresponds to a strain of 1.24%. Using equation 4.4, this corresponds to the strain induced by the growth of silicon on relaxed $Si_{0.77}Ge_{0.29}$. To confirm the Raman strain measurements, RBS analysis was used to determine the actual germanium fraction of the SiGe film as shown in figure 4.3.

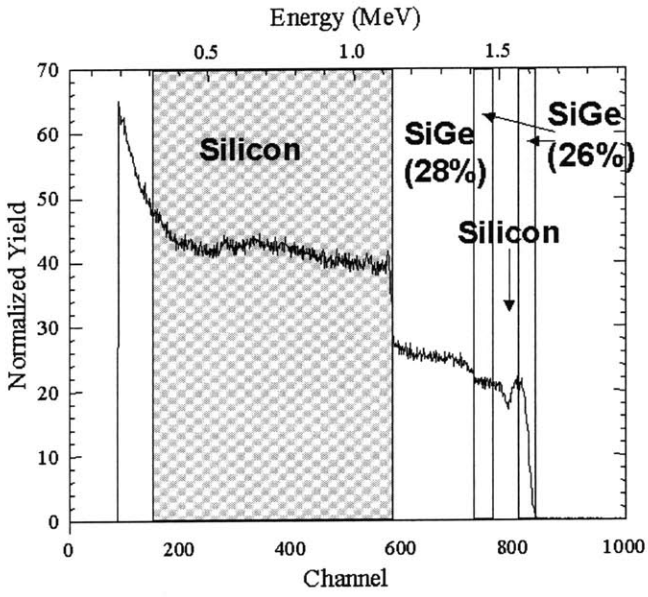


Figure 4.3 – RBS analysis shows the Ge fraction of 28% +/- 1%. This corresponds to the apparent Ge fraction extracted from Raman spectra. RBS analysis courtesy C. Ni Chleirigh.

From the RBS data, a germanium fraction of 28% is observed. A slight decrease in the Ge fraction to 26% is observed at the re-growth interface. Since the amount of material grown during the re-growth is limited this film is expected to

be slightly strained, i.e. it is not thick enough to relax. Therefore, the silicon will be strained to the 28% underlying SiGe layer. The apparent Ge fraction from Raman is equal to the actual Ge fraction found by RBS within the limits of the measurements (+/- 1%). Therefore, it appears that the bond to the SiO_2 has maintained the as-grown crystalline structure and the strain is not degraded in the process of transferring the thin strained Si film.

4.5 RTA Study of SSOI Under Typical S/D Anneals

Rapid thermal annealing of SSOI and strained silicon on insulator with intermediate SiGe was completed using conditions suitable for source/drain anneals. Blanket films of ~13 nm-thick SSOI and strained silicon on insulator with an underlying thin SiGe layer were subjected to the following annealing conditions: 600C for 10 seconds, 800C for 10 seconds, and 950C for 1 second. Raman data (figure 4.4) was fit using Lorentian functions after subtracting out background noise.

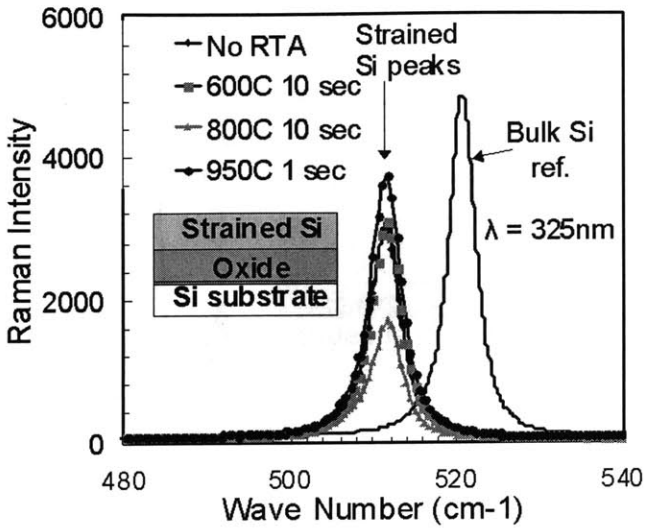


Figure 4.4 - Raman analysis of 13 nm-thick strained silicon directly on insulator using 325 nm excitation shows the strained Si peak at 512 cm^{-1}. The shift from the relaxed Si peak at 521 cm^{-1} corresponds to a strain of 1.2%, in agreement with the strain in the as-grown film prior to layer transfer. In addition, no shift in the strained Si peak is observed after RTA.

For the strained Si directly on insulator two peaks are observed: a Si peak at 521 cm^{-1} and a strained Si peak at 512 cm^{-1}. This shift of 9 wave numbers corresponds to approximately 1.2% strain, the amount of strain induced in Si grown on 29% SiGe. No shift in the strained silicon peak at 512 cm^{-1} is observed after annealing. If the strain in the film were relaxing during annealing, this peak would shift towards the silicon reference peak at 521cm^{-1}. Since no shift is observed, it can be concluded that the strained silicon films remain fully strained both before and after rapid thermal annealing.

The Raman spectra for strained silicon on insulator with a very thin underlying SiGe layer is shown in figure 4.5.

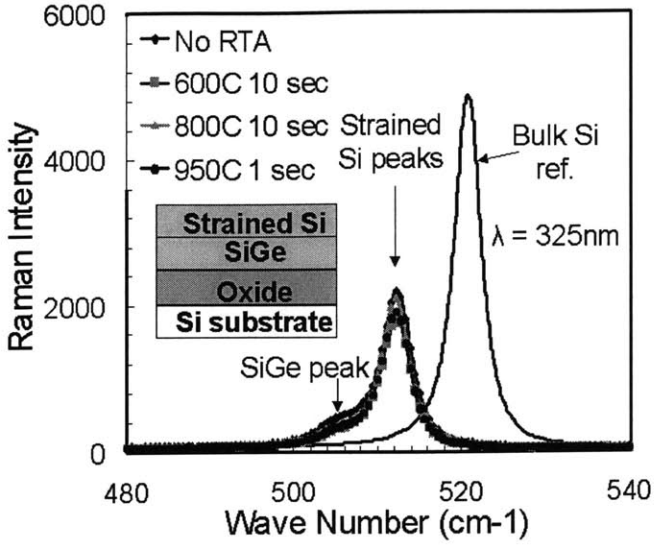


Figure 4.5 - Raman analysis of 13 nm-thick strained silicon on insulator with intermediate 5 nm-thick SiGe layer using 325 nm excitation shows the strained Si peak at 512 cm^{-1}. The shift from the relaxed Si peak at 521 cm^{-1} corresponds to a strain of 1.2%, in agreement with the strain in the as-grown film prior to layer transfer. The SiGe peak appears as a small shoulder on the strained silicon peak. In addition, no shift in the strained Si peak is observed after RTA.

For strained silicon with underlying SiGe, there are three peaks observed: silicon, SiGe, and strained silicon at 521 cm^{-1}, 506 cm^{-1}, and 512 cm^{-1} respectively. The relative intensity of the peaks varies due to the integration time and thickness of the layer. The location of the peaks again suggests that the samples silicon has remained equally strained after all annealing conditions.

4.6 Summary and Conclusions

It is very encouraging for MOSFET fabrication that no relaxation of the strained silicon film was observed during thermal cycling after the removal of the strain-inducing SiGe. The particular properties of the bonding interface contribute to maintaining the strain of thin SSOI layers. The Si-SiO_2 bonded interface is strong enough to maintain the 1.2% strain in the silicon film. The film is also below the critical thickness. If a film is below the critical thickness, it is energetically

favorable for the film to remain strained rather than relax [57-59]. The critical thickness of strained silicon on $Si_{.75}Ge_{.25}$ is ~175A, much greater than the 13 nm-thick strained silicon layer analyzed in this work [60]. These two properties allow the film to remain strained after the removal of the SiGe that originally induced the strain into thesilicon.

Chapter 5

ULTRA-THIN STRAINED SILICON ON INSULATOR MOSFETS

5.1 Introduction

Ultra-thin strained silicon on insulator (SSOI) combines the advantages of strained silicon with ultra-thin body device design. In this work ultra-thin SSOI MOSFETs were fabricated using a simple one-mask process. Transistor behavior was observed, but the drain current (I_d) was significantly reduced compared to the bulk silicon control devices. This can be attributed to very large series resistance in the SSOI devices. Simulations of the source/drain ion implants were completed to explain the series resistance in the ultra-thin SSOI devices. It has been concluded that the simple process and source/drain dopant implants used were not optimal for ultra-thin silicon.

5.2 Ring MOSFET Fabrication process

5.2.1 Basic Fabrication Process

Multiple SSOI substrates were fabricated using the flip, bond, and etch method discussed in chapter two. A one-mask MOSFET process developed by Mark Armstrong was used to fabricate simple devices [61]. The mask used in this process was designed by Ingvar Aberg. The first step in the MOSFET fabrication process is gate stack deposition. After an RCA clean, approximately 300 nm of low temperature oxide (LTO) is deposited at 400°C to form the gate oxide. Next, a 50 nm-thick polysilicon gate layer is deposited by LPCVD at 560°C. The backside of the wafer is then etched to remove the polysilicon, LTO, and epitaxial layers (if applicable) so that a good contact can be made to the substrate. The gate stack is then patterned with the "one level MOSFET" mask using a contact aligner. The gate stack was etched in an Applied Materials Precision 5000 to leave only 10 nm of LTO covering the source and drain regions. The remaining 10 nm-thick oxide is removed using buffered oxide etchant (BOE). The BOE also etches the LTO laterally resulting in undercutting of the polysilicon. A 20 second BOE dip provides a 100 nm of LTO undercut. The wafer is then implanted with Arsenic (As) using 4 rotations at 7-degree tilt for a total dose of $4x10^{15}cm^{-2}$. After As ion implantation, the source and drain dopants are activated via rapid thermal annealing. A metal layer consisting of a 50 nm Titanium burrier layer and a 100 nm Aluminum layer is then deposited to form contacts. These devices rely on a thick gate oxide to break metal between the source, gate, and drain regions in the device. The final step for device formation is a sinter in 60%/40% mixture of N_2 and H_2 at 400°C. Further details of this process are found in appendix C. A schematic representation of this process is shown in figure 5.1.

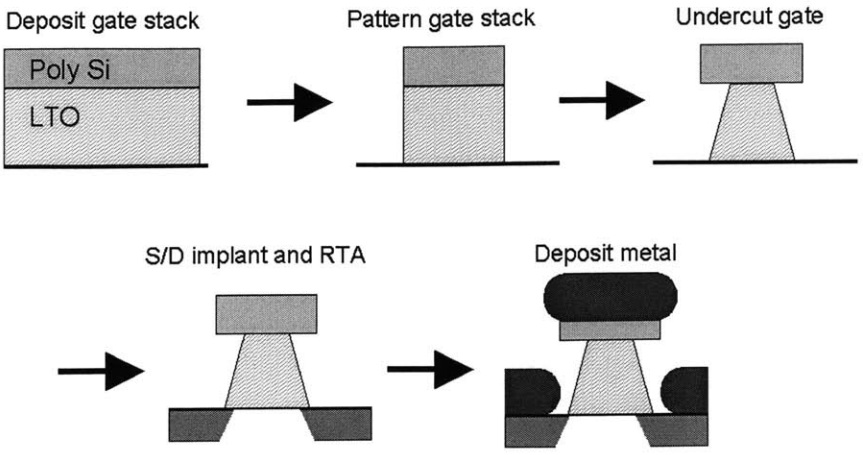


Figure 5.1 – Schematic of short flow process for one mask - level ring MOSFETs. Figure after C. Leitz [62].

5.2.2 Mask for One Level MOSFETs

The mask used for the one level MOSFETS is shown in figure 5.2. This mask contains ring devices with an isolation ring. All devices have gate lengths between 50-500 um. Long (3 mm length) lines of varying widths down to 5 um are also present on the top right corner of the die for SEM and TEM analysis.

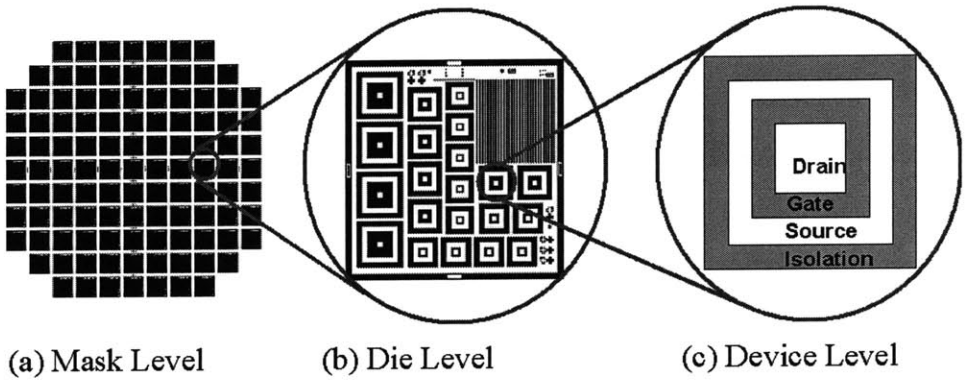


Figure 5.2 – Mask layout for single mask ring MOSFETs. This mask (a) contains many die (b) with multiple ring structure MOSFETs. The source, gate, drain, and isolation rings are labeled in (c).

5.2.3 Key Issues for Ring MOSFET Fabrication

While the basic process for fabricating one level MOSFET devices is relatively quick and simple, there are key steps that must be carefully monitored. The one mask process relies on a thick gate oxide to break the gate, source and drain metal. In order for this metal to break properly, the thickness of the gate oxide as well as the metal thickness must be well controlled. A standard gate stack of 350 nm is sufficient to cleave a 150 nm metal layer. If the gate stack thickness is significantly reduced the total metal thickness must also be reduced. The undercut of the LTO gate oxide in these devices is also critical to ensure the metal will not bridge the source/drain and gate regions.

The second key step for the successful fabrication of one-level MOSFETs is the implantation and activation of source/drain dopants. To correctly implant these regions, the LTO undercut length and angle must be controlled. If the undercut is too great, the dopants will not reach the edge of the gate. Thus, there will not be any overlap between the gate and the source/drain regions which will lead to increased series resistance. The second key issue is the dopant implant conditions. The implant must successfully dope both the source/drain regions and gate. The use of *in-situ* doped polysilicon would eliminate the need for one implant to dope both the source/drain and the gate. For the one mask process to be successful on strained silicon, the implant activation anneal must also be kept below a critical temperature to prevent strain relaxation in the thin silicon layer.

5.3 Mobility Extraction from Ring MOSFETs

While the one mask process is not suitable for fabrication of state-of-the-art devices, it is useful for basic device characterization of bulk devices including mobility extraction. The MOSFET layout and the key dimensions used for mobility extraction are shown in figure 5.3.

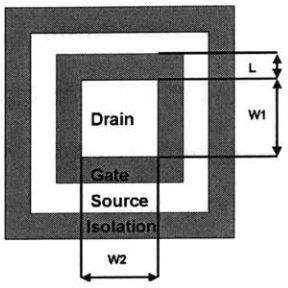


Figure 5.3 – Layout and key dimensions of one level ring MOSFET

Following the work of Armstrong and Leitz [61,62], and using these dimensions, the area and geometry factor (G) can be calculated. The geometry factor replaces W/L in current equations due to the ring configuration. The geometry factor is calculated using the following equation:

$$G = \frac{L}{2W_1 + 2W_2} \qquad \text{eq. 5.1}$$

The area is calculated using the following equation:

$$A=2(L-2\Delta L)(2L+W_1+W_2) \qquad \text{eq. 5.2}$$

where $2\Delta L$ is the linewidth shrink due to over-etching and undercutting of the gate during fabrication.

Ring MOSFET parameters				
Parameter	Device 1	Device 2	Device 3	Device 4
L	500 µm	200 µm	100 µm	50 µm
W1	250 µm	250 µm	250 µm	250 µm
W2	250 µm	250 µm	250 µm	250 µm
G	0.24	0.138	0.0813	0.0447
A	0.015 cm^2	0.0036 cm^2	0.0014 cm^2	0.0006 cm^2

Figure 5.4 – Device parameters for one level MOSFETs with varying gate lengths. From Armstrong [61].

Mobility, µ, is extracted in the linear regime where the current is defined as follows:

$$I_d = \frac{W}{L} u_{eff} * C_{ox}(V_{gs} - V_t)V_{ds} \qquad \text{eq. 5.3}$$

Due to the ring MOSFET configuration, W/L is replaced with the geometry factor G as follows:

$$I_d = G * u_{eff} * C_{ox}(V_{gs} - V_t)V_{ds} \qquad \text{eq. 5.4}$$

where I_d is the drain current, G is the geometry factor, V_{gs} is the gate to source voltage, V_t is the threshold voltage, V_{ds} is the drain to source voltage, and C_{ox} is the oxide capacitance. This equation can be rearranged to express mobility as a function of parameters extracted from standard measurements as follows:

$$u_{eff} = \frac{I_d * G}{C_{ox}(V_{gs} - V_t)V_{ds}} \qquad \text{eq. 5.5}$$

Since this expression for effective mobility was derived from the linear regime of MOSFET operation, it is only valid for $V_{ds} << V_{gs}$. During device measurement, a V_{ds} value of 0.1V was used. Once the mobility is known it can be plotted versus V_{gs}-V_t, but it is more standard to show mobility versus vertical effective field. The vertical effective electric field (E_{eff}) can be expressed as:

$$E_{eff} = \frac{Q_b + \eta Q_{inv}}{\varepsilon_s} \qquad \text{eq. 5.6}$$

Where Q_b is the bulk charge, Q_{inv} is the inversion charge, η is a fitting parameter, and ε_s is the permitivity of the substrate. The fitting parameter, η, is defined as 1/3 for holes and 1/2 for electrons. From electric field continuity at an interface, ε_s and ε_{ox} may be related as follows:

$$E_s \varepsilon_s = E_{ox} \varepsilon_{ox} \qquad \text{eq. 5.7}$$

From Gauss' law we also can relate the electric field in the silicon, at the Si-SiO_2 interface, to the bulk and inversion charge as follows:

$$E_s = \frac{Q_{inv} + Q_b}{\varepsilon_s} \qquad \text{eq. 5.8}$$

Using the continuity equation (eq. 5.7) and expression from Gauss' law (eq. 5.8) the expression for the effective field can be approximated as follows:

$$E_{eff} = \frac{E_{ox}\varepsilon_{ox} - Q_{inv} + \eta Q_{inv}}{\varepsilon_s} \qquad \text{eq. 5.9}$$

To further simplify the effective field calculation, approximations for the inversion charge and effective field in the oxide are used. The approximations are as follows:

$$Q_{inv} = C_{ox}(V_{gs}-V_t) \qquad \text{eq. 5.10}$$

$$E_{ox} = V_{gs}/t_{ox} \qquad \text{eq. 5.11}$$

Using these approximations, the vertical effective field can be expressed as follows:

$$E_{eff} = \frac{C_{ox}(V_t + \eta(V_{gs} - V_t))}{\varepsilon_s} \qquad \text{eq. 5.12}$$

From equations 5.5 and 5.12, approximate values for mobility and effective field can be calculated from CV and I_d-V_g measurements.

5.4 Device Results

Ultra-thin strained silicon on insulator NMOSFETs were fabricated using the one mask process. Bulk silicon and strained silicon on $Si_{.75}Ge_{.25}$ wafers were used as control samples. In order to ensure that the strain was not degraded in the strained silicon samples, a limited thermal budget was used for all devices. In the ultra-thin SSOI sample, the strained silicon is only 15 nm-thick at the beginning of the process; therefore, all cleaning times were slightly shortened to reduce silicon loss and Piranha replaced SC1 during the pre-LTO clean as documented in appendix C.

5.4.1 XTEM of SSOI Device

Cross section transmission electron microscopy (XTEM) was used to view a cross-section of the device structure. Due to the large size of actual ring MOSFET devices, TEM samples were prepared from narrow SEM/TEM lines. TEM images confirm that the thin strained silicon channel layer was not lost during MOSFET processing, at least on some fraction of the wafer. A cross-section TEM micrograph is shown in figure 5.5.

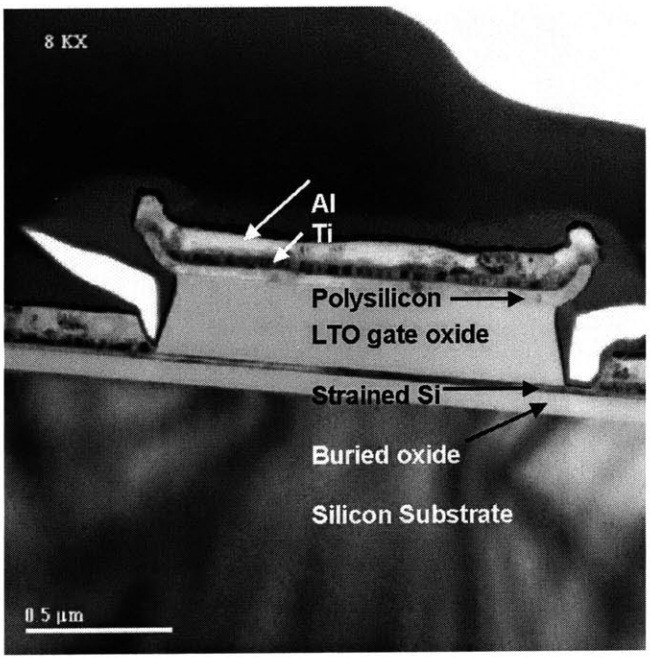


Figure 5.5 XTEM of SSOI device structure (XTEM bars, not an actual device) showing thin SSOI layer and the gate, source, and drain. XTEM courtesy of Xiaoman Duan of National Semicondutor. The TEM sample was prepared using a focused ion beam technique.

In this TEM image, a thin strained silicon channel layer is seen directly below the gate oxide and in the source-drain regions thus confirming that this layer was not removed from this portion of the wafer during the MOSFET fabrication. The TEM also suggests that the polysilicon experienced considerable stress during processing,

causing it to curl in the edge regions when the LTO gate oxide was etched to undercut the polysilicon.

In addition to confirming the presence of a strained silicon channel layer, XTEM was also used to examine the SSOI material more closely in key areas of the device. Figure 5.6 and 5.7 show the region under the LTO gate and in the source/drain respectively.

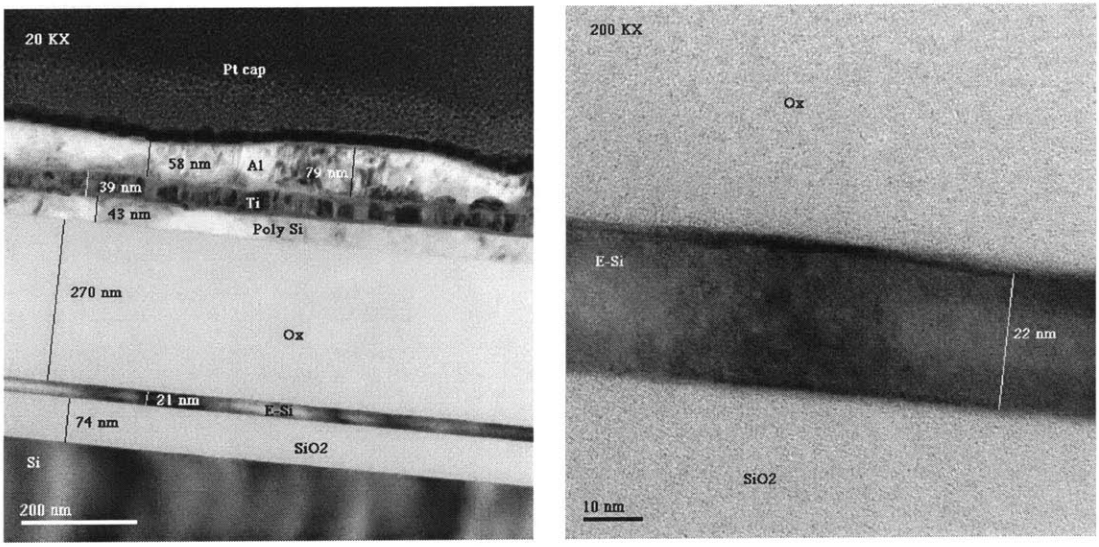


Figure 5.6 – XTEM of gate region of device. XTEM courtesy of Xiaoman Duan of National Semiconductor.

The gate stack seen in figure 5.6 consists of a 270 nm-thick gate oxide, a 43 nm-thick polysilicon layer, a 39 nm-thick titanium barrier layer and a 58 nm-thick aluminum layer on top of a 21nm-thick strained silicon layer on insulator.

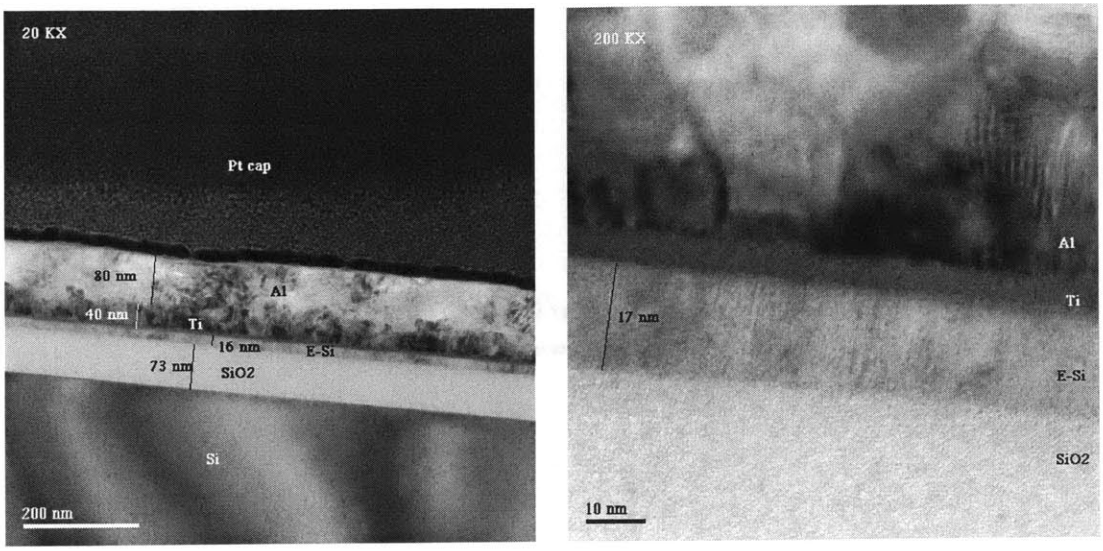


Figure 5.7– XTEM of source drain region of device. XTEM courtesy of Xiaoman Duan of National Semiconductor.

In the source/drain regions, the stack consists only of the deposited metals on top of the thin strained silicon layers. Here the silicon is slightly thinner than in the region under the gate due to etching for gate stack formation and subsequent cleaning steps which both remove silicon.

5.4.2 Determination of Buried Oxide Layer Presence

The first and most important step in analyzing the electrical behavior of SSOI devices is the confirmation of the presence of buried oxide layer in any given device on the wafer. It is possible that during fabrication and processing, the thin strained silicon layer could be etched away in certain regions of the wafer, effectively leaving the gate oxide to be deposited directly onto the buried oxide layer as shown in figure 5.8b.

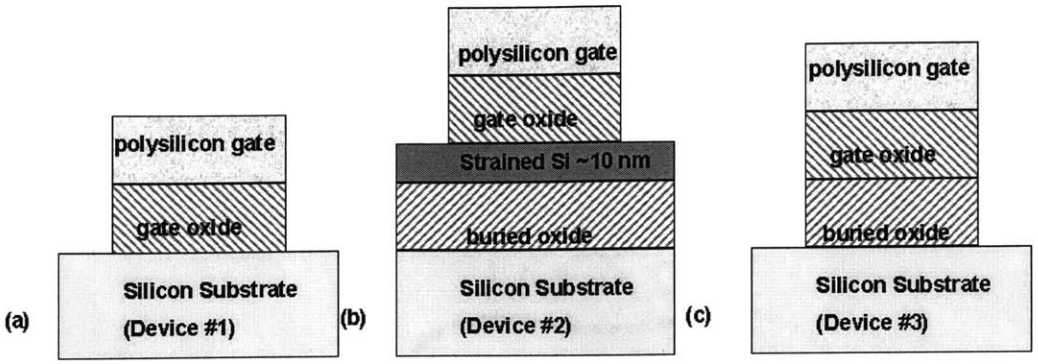


Figure 5.8 – There are three potential device structures that could be relevant in this experiment: (a) the silicon control structure (device#1) (b) the ultra-thin strained silicon on insulator device (device#2) and (c) device fabricated from SSOI if silicon layer is accidentally removed in processing before gate oxide deposition (device#3).

There are three potential device structures relevant to this experiment. The first structure is the silicon control device structure as seen in 5.8a. This device consists a silicon substrate with the gate oxide and polysilicon patterned to form the gate stack referred to as device#1. The second potential structure is the strained silicon on insulator device as seen in figure 5.8b. This device consists of a buried oxide and a thin strained silicon layer with the gate oxide and polysilicon patterned above these layers. This device will be referred to as device#2. The final device structure is an undesired structure that could occur if the strained silicon layer is accidentally etched away before gate oxide deposition as seen in figure 5.8c referred to as device#3. While etching the gate oxide, the buried oxide will also be etched thus exposing the silicon substrate. These devices are summarized in figure 5.9.

Devices for electrical measurements		
Device number	Starting material	comments
Device #1	CZ silicon	silicon control device
Device #2	SSOI	channel will form in 13 nm-thick silicon
Device #3	overetched SSOI	channel will form in silicon substrate
Device #4	strained silicon	bulk strained silicon on SiGe control

Figure 5.9 – Table of devices measured. The channel of device #1 and #3 will be in the silicon substrate while the channel for device#2 will be in the 13-nm thick silicon on insulator layer. Device#4 consisting of strained silicon on SiGe will be used for mobility comparisons.

In order to determine whether the SSOI wafers were over-etched to form the structure in 5.8b, IV characteristics between the drain and the substrate were performed by sweeping the drain voltage from –10V to 10V while holding the substrate at ground. If the buried oxide layer is not present, this measurement will produce diode characteristics of the drain-substrate P-N junction. If the oxide is present, there will not be a current path from the drain to the substrate.

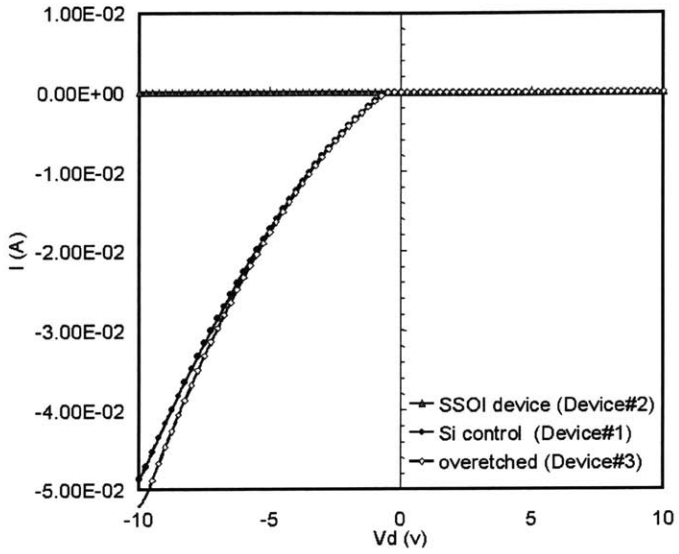


Figure 5.10 – Presence of thin silicon layer confirmed by measuring IV characteristics between drain and substrate. Good SSOI devices (device#2) show little leakage. Silicon control and overetched SSOI devices (device#1 and device#3) show diode characteristics of the drain-substrate junction.

These IV measurements were performed on three wafers. A silicon control wafer (device#1) and two devices from the "SSOI" wafer (device#2 and device#3). The results are shown in figure 5.10. Device#3 was over-etched and does not have a strained silicon layer. Device#3 displays diode-like characteristics similar to the silicon control. Device#2, the SSOI device, did not show current flow. Therefore, it is concluded that there was a thin strained silicon layer and a buried oxide was present during processing and measurement.

5.4.3 IV Results for SSOI and Si Wafers

IV characteristics were measured for the three devices described in section 5.4.2. The wafers were a silicon control wafer(device#1), a strained silicon on insulator wafer (device#2), and an over-etched device (device#3) where the channel will form in the bulk silicon substrate. For these measurements the drain voltage was swept from 0 to 7V and the gate voltage was stepped from 0 to 15 volts. The substrate and the source were both grounded for IV measurements. The IV characteristics from the silicon control (device#1)and over-etched devices (deivce#3) are shown in figure 5.11. IV characteristics for devices from the properly etched SSOI device (device#2) are shown in figure 5.12.

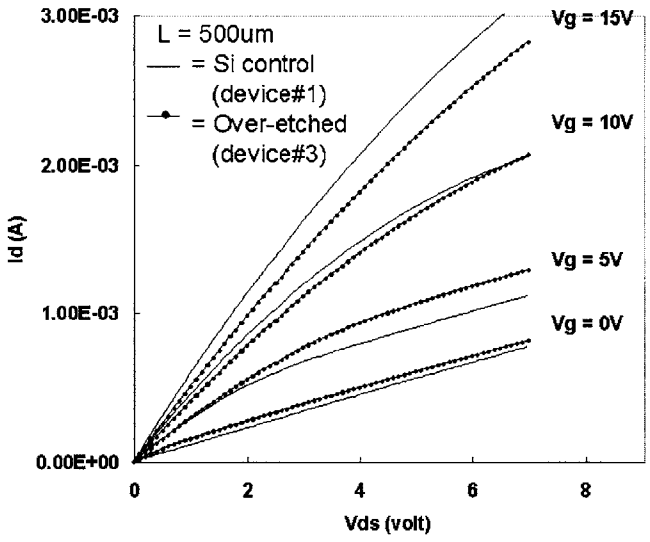


Figure 5.11 – I_d vs. V_{ds} for a ring MOSFETs with gate length of 500um. Device#3 was over-etched leaving the silicon substrate to be measured. Therefore, this device and the silicon control exhibit very similar IV characteristics.

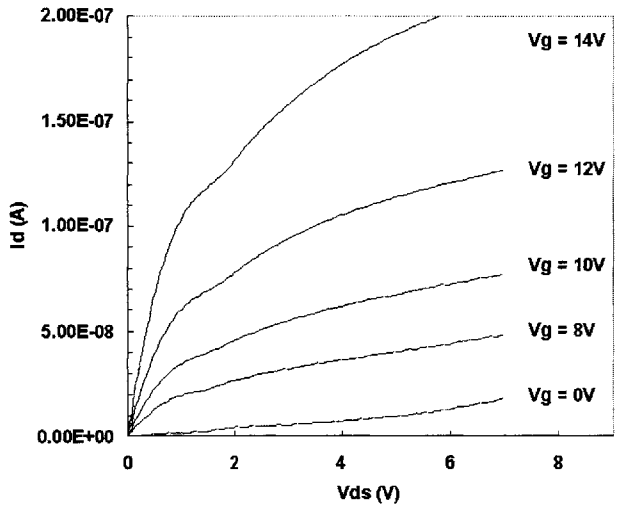


Figure 5.12 – I_d vs. V_{ds} for a properly etched SSOI ring MOSFET (device#2) with gate length 500um. In this thin SSOI device, the current is severly degraded compared to the bulk silicon control sample, due to series resistance effects.

For the devices where the channel is formed in the thin strained silicon layer(device#2), the current is severely reduced compared to the silicon control. The IV characteristics for both the silicon control and the SSOI devices are not optimal, but both are functional devices. As expected for device#3, where the thin strained silicon layer did not remain and no buried oxide was present, the IV characteristics were nearly identical to the silicon control. This is due to the channel forming in the silicon substrate.

5.4.4 CV results for SSOI and Si wafers

High frequency capacitance was measured as a function of gate voltage for the silicon control devices, strained silicon on insulator devices (device#2), and overetched devices (device#3). For the measurement, the drain, source, and body were all tied to the low voltage and the gate was tied to the high voltage. The gate voltage was swept from –15V to 15V in 0.25V steps at a frequency of 100Khz. CV characteristics for the ring MOSFETs are seen in figures 5.13 and 5.14.

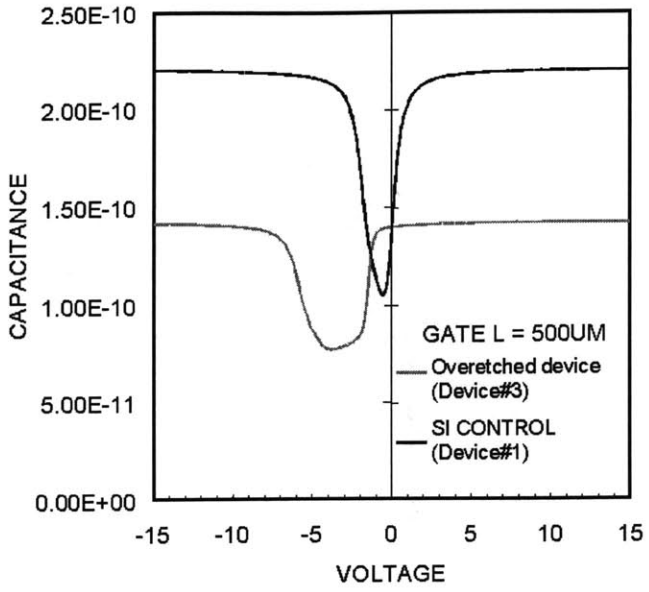


Figure 5.13 – High frequency CV ring MOSFET with gate length of 500 um. The D factor in these measurements is less than 0.3. Device#3 was overetched so the channel is in the silicon substrate. In this device the gate oxide will consist of the combination of the deposited gate and the etched burried oxide. This accounts for the shift in maximum capacitance between the two silicon devices.

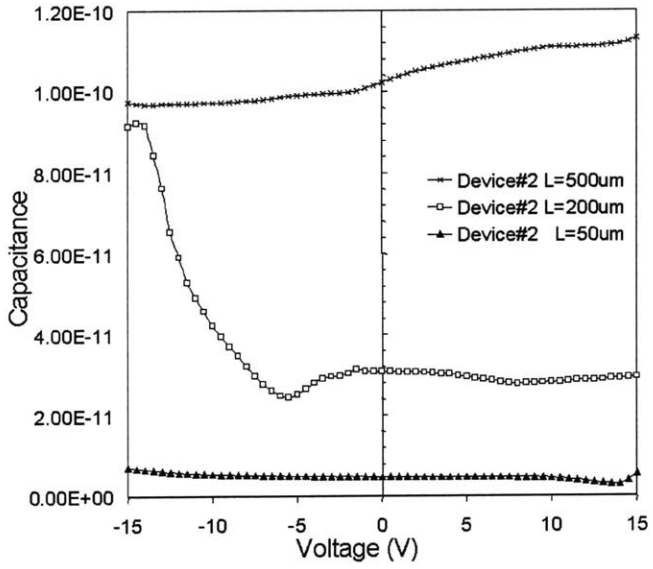


Figure 5.14 - High frequency CV for SSOI MOSFETS (device#2). The D factor in these measurements is very high, between 1-10. Both the value and the shape of the measured capacitance varied greatly between devices. No correlation was found between CV shape or value and device size. Useful CV data could not be extracted from these SSOI devices.

The oxide thickness for the silicon and over-etched devices can be calculated from the CV curves using the permitivity of the material and the effective area of the device. For the silicon control device (device#1) an oxide thickness of 235.4 nm was calculated, but for the over-etched device (device#3) a thickness of 364.7 nm was calculated. This large discrepancy in oxide thickness is expected because silicon device formed on the over-etched SSOI sample will have the buried oxide and gate oxide in the gate stack. The target gate oxide thickness was 250 nm. In the silicon control device the oxide thickness extracted from CV is 235 nm. The buried oxide thickness targeted during SSOI formation was 100 nm +/- 25 nm due to CMP non-uniformity. In (device#3) the gate oxide consists of the sum of these two layers with an estimated thickness of 350 nm. This is very near the value extracted thickness from CV of 364 nm. The CV for SSOI device (device#2) had an extremely high D factor. Therefore, the measurements were not reproducible and varied greatly in value and shape from device to device. Due to the lack of meaningful CV data, the gate oxide thickness for SSOI devices cannot be calculated from the CV measurement.

5.4.5 Mobility Extraction

Electron mobility was calculated as a function of vertical effective field using the approximations and equations presented in section 5.3. The apparent mobility for strained silicon on SiGe control devices (device#4), silicon control (device#1), and strained silicon on insulator (device#2) devices are shown in figure 5.15

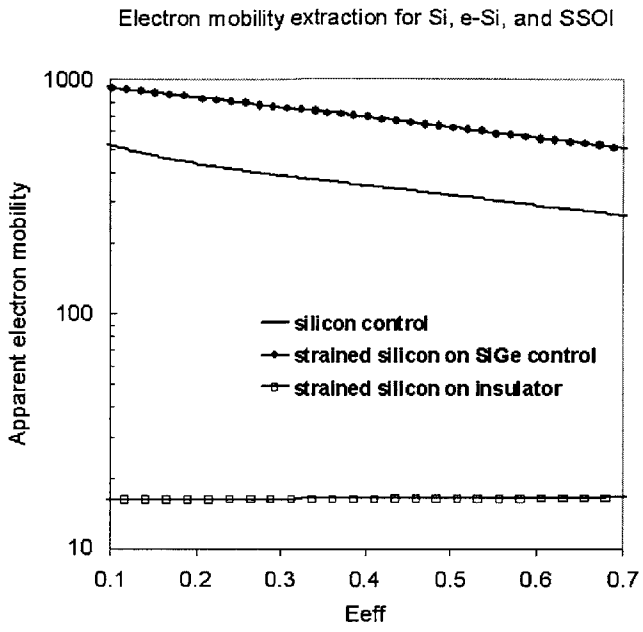


Figure 5.15 – Apparent electron mobility versus effective field for a strained silicon on $Si_{0.25}Ge_{0.75}$ wafer (device#4), a silicon control wafer (device#1), and an SSOI device with an apparent Ge fraction of 29% (device#2). Mobility enhancement is seen for the strained silicon control wafer, but severe apparent mobility degredation is seen for SSOI devices.

The electron mobility of the silicon control device, calculated using the equations in section 5.3, closely agreed with the universal mobility. As expected, a mobility enhancement is seen for the strained silicon control. If the SSOI devices retained their strain and other effects do not dominate the mobility, then the mobility of the strained silicon control and the strained silicon on insulator devices should be similar. Unfortunately, the apparent mobility of the strained silicon on insulator devices is severely degraded by almost two orders of magnitude compared to the silicon control. The observed low current is due to high series resistance. If the high series resistance significantly degrades Id, the mobility calculated and plotted in figure 5.15 is only an apparent mobility, not the true mobility of the electrons in the silicon channel.

5.4.6 Source to Drain Resistance Extraction

The resistance components of a MOSFET are shown in figure 5.16. Extraction of the source to drain resistance for varying gate lengths allows the series resistance effects to be examined.

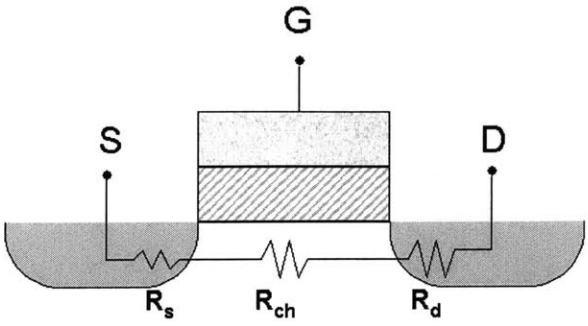


Figure 5.16– A MOSFET with source, channel, and drain resistances.

If series resistance dominates the behavior of the device, then the current will not vary linearly with gate length. Source to drain resistance extraction for varying gate length devices shows the silicon control devices are not dominated by series resistance while the SSOI devices are. For the silicon control devices, the resistance varies linearly with gate length as seen in figure 5.17.

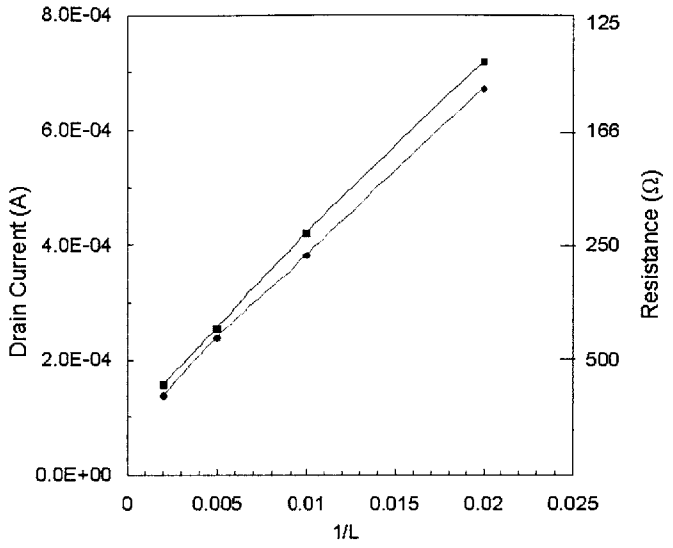


Figure 5.17 – Drain to source resistance extraction for the bulk silicon control devices. Resistance varied by gate length, therefore the resistance of the device is not dominated by a source/drain to channel series resistance.

Figure 5.16 shows the series resistance does not dominate these silicon devices. The calculated source to drain resistance varied from 110Ω for 50um devices to 540Ω for the 500um device. However, in the strained silicon on insulator devices, the gate length had no effect on the resistance of the device and the resistance values were extremely high. Resistances on the order of 0.1MΩ - 100MΩ were observed. This is nearly the resistance of an open contact, but since IV characteristics can be measured, it is not an open circuit. In the device TEM it is also evident that there is a continuous silicon film from the S/D to the channel regions, thus dispelling the idea the metal has pulled the silicon atoms from the channel to form a silicide. The formation of open metal contacts is of greater concern for films with thicknesses below 5 nm. While it is not an open circuit, the series resistance is extremely high and the resistance did not vary with the gate length. This suggests that series resistance between the source/drain regions (R_s and R_d) dominates the electrical characteristics of these devices.

Based on the source/drain ion implant conditions, the sheet resistance of the SSOI film in the source/drain regions can be estimated from the following equation:

$$R_s = \frac{1}{q * C_e * \mu} \qquad \text{eq. 5.13}$$

where R_s is the sheet resistance, q is the charge of an electron, C_e is the integrated dose, and u is the mobility. Using TSUPREM simulations of the ion implant conditions, an integrated dose of $3.93X10^{15}cm^{-2}$ and $9.96X10^{12}$ cm^{-2} was present in the source-drain regions of the silicon control and SSOI devices respectively. Section 5.5 discusses these simulations in detail. For this order of magnitude calculation the mobility in the layers was assumed to be equal. Placing these numbers into the R_s equation yields a sheet resistance of 3.68Ω/□ for the silicon control and 1255Ω/□ for the SSOI. The ratio of R_{ext} for SSOI and a silicon control is in the range of 10^3 to 10^5. The ratio of sheet resistance for the devices is ~300. This implies that the Rs of the source/drain account for a large portion, though not all, of the measured resistance. The remaining resistance could be due to the shadowed region between the drain and channel as seen in figure 5.18. The resistance values calculated assume a constant doping through the source/drain regions For the SSOI devices there may exist a small region between the gate and the source and drain where the doping is even lower than the $9.96x10^{12}$ cm^{-2} due to the overhang and shadowing of the poly gate. This would greatly increase the resistivity of this region.

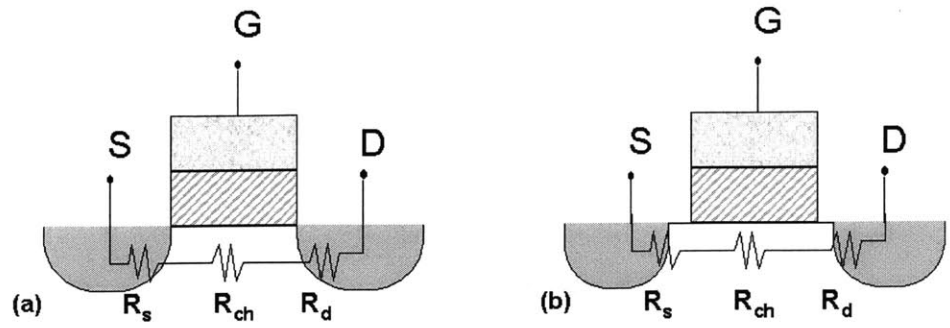


Figure 5.18 – Source to drain resistance is cauculated assuming the dopants are distributed evenly from the drain to the gate region as seen in (a). If the dopants do not reach the near gate region (b) then the source to drain resistance will be much greater.

Further calculations of the series resistance needed to degrade the current from the levels of the silicon control to the SSOI devices were made by placing a resistor in series with a transistor as seen in figure 5.19.

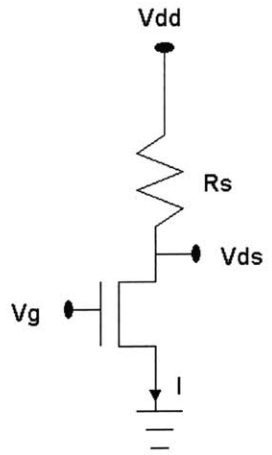


Figure 5.19– Circuit for order of magnitude extraction of series resistance to degrade I_d from ~1x10^{-3} A as seen in the silicon control to ~4x10^{-8} A as seen in SSOI device.

For this order of magnitude calculation, the current was estimated as follows:

$$I = k * (V_{gs} - V_t - \frac{V_{ds}}{2}) * V_{ds} \qquad \text{eq. 5.14}$$

For the silicon control device the threshold voltage was approximately 0V and the current was ~1E-3A for a gate voltage of 5 volts and a drain voltage of 5 volts. Substituting these numbers into the equation for current and solving for k extracts a value of 8E-5. For the silicon control device it is assumed that $V_{ds}=V_{dd}$. For the SSOI device, a Vds value must be extracted to determine the voltage dropped across the series resistor. Therefore, the current value for an SSOI device with the same gate voltage and drain voltage is substituted into the current equation yielding:

$$4E-8 = 8E-5*(5-\frac{V_{ds}}{2})*V_{ds}. \qquad \text{Eq. 5.15}$$

Solving this equation gives a Vds value of 0.1V. Therefore, 4.9V of the applied voltage is dropped across the series resistor. Using ohm's law, a series resistance of 1.2E8 Ω is calculated. This simple order of magnitude calculation yields a resistance value near that extracted from the SSOI device measurements. Therefore, it is assumed that series resistance dominates the electrical behavior of the SSOI device and that the observed "mobilities" are meaningless.

5.4.7 Explanations for Degraded SSOI Device Performance

As shown in the previous section, the series resistance of the SSOI devices is extremely high. This is most likely due to the ion implant conditions selected. If the implant energy was not selected properly, the implant peak may not have been located in the thin silicon layer. The implant conditions are discussed in more detail in section 5.5. Also, if the implant does not extend into the region under the poly gate, then a high resistance path will separate the source and drain regions from the channel. This resistance could account for the degraded drain current. If this series resistance dominates the electrical characteristics then the mobility for the strained silicon on insulator cannot be accurately extracted.

Although it will not have as large of an effect as the series resistance, surface roughness could also degrade the mobility of electrons in the thin strained silicon on insulator film. It is impossible to measure this effect in these devices given the high series resistance. The surface roughness of the SSOI channel layer is approximately 1 nm. This roughness should be reduced for better device performance.

5.5 Simulations of Source/Drain Implant Conditions

From the device results shown previously, it is clear the one level strained silicon on insulator MOSFETs had extremely high series resistance. The implant that was used for fabrication of these SSOI devices was not optimal. Past bulk devices fabricated by C. Leitz and M. Lee used an implant of 35KeV As with four 90-degree rotations at a 7-degree tilt for a total dose of $4X10^{15}cm^{-2}$. Simulations of this implant show it is not optimal for ultra-thin body devices. Figure 5.20 shows the TSUPREM simulation of this implant.

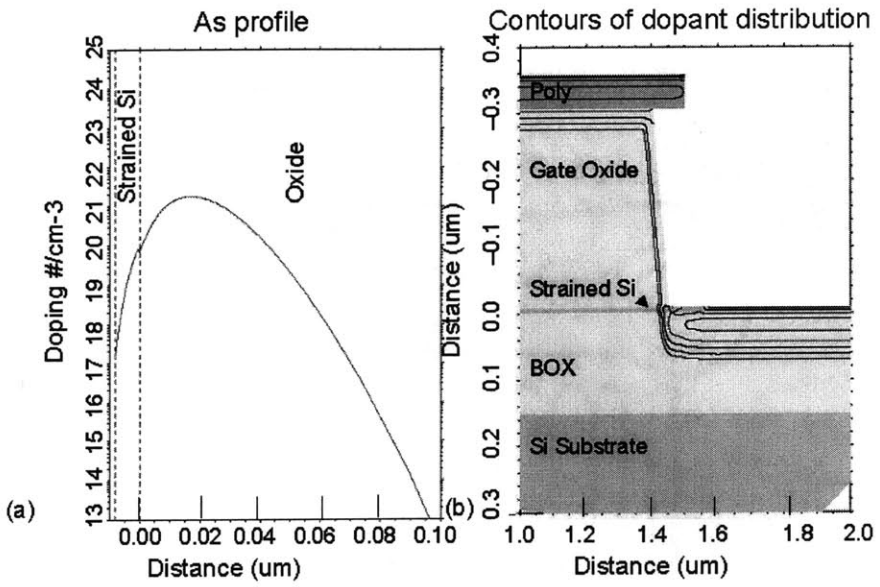


Figure 5.20– TSUPREM simulation of 35KeV, 7 degree tilt As implant with a total dose of $4X10^{15}$ cm^{-2} used for one mask ring MOSFET. This implant is not optimal for ultra-thin strained silicon on insulator device fabrication due to the loss of dopants to the oxide. An integrated dose of $9.96X10^{12}$ cm^{-2} is present in the thin silicon layer.

As seen in this figure, the majority of the dopants are implanted deep into the oxide instead of remaining in the thin silicon layer. The silicon layer contains an integrated dose of $9.96X10^{12}$ cm^{-2} compared to the total dose of $4X10^{15}$ cm^{-2}. Therefore, the dose in the thin silicon layer is much lower than desired. However, it is important to note that the doping is adequately distributed throughout the poly gate.

Since the implant described above was not adequate for doping the ultra-thin strained silicon source/drain regions, further implant simulations are necessary. First, an implant energy that will place the dopants in the thin strained silicon layer must be determined. Implant energies from 35 KeV down to 5 KeV were simulated. One-dimensional simulations using the fitted Monte Carlo data tables in TSUPREM of these implants are shown in figure 5.21.

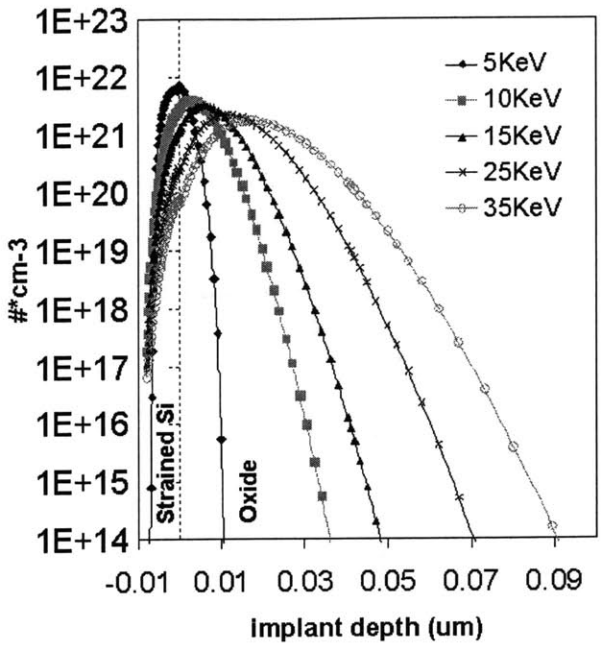


Figure 5.21 – Concentration dependence on implant energy for As implant with a total dose of $4X10^{15}$ cm^{-2}. Lower energy implants allow a higher percentage of dopants to remain in the strained silicon channel region. Higher implant energies result in most of the dopant atoms being implanted into the burried oxide layer.

The simulations show that a low energy implant is necessary. Even at the lowest commercially available energy of 5KeV, nearly half of the dopant atoms are implanted too deep and are located in the oxide instead of the silicon layer.

After completing one-dimensional simulations to determine a correct implant energy, two-dimensional simulations were completed to analyze the device structure. TSUPREM simulations were completed using an implant energy of 5 KeV with the previous 7-degree tilt condition used in the fabrication of the one-mask devices as shown in figure 5.22.

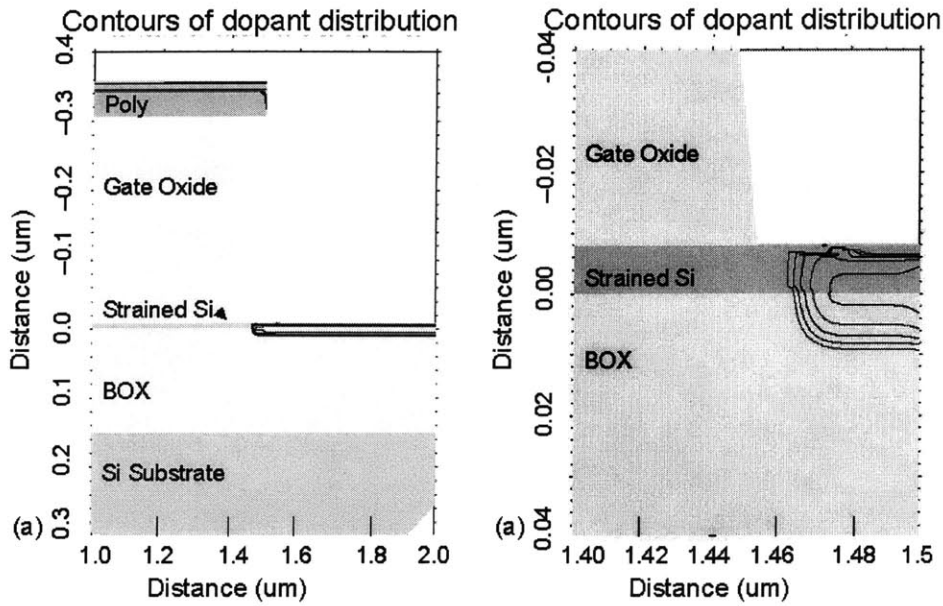


Figure 5.22 –Implant of As at 5 KeV , 7 degrees tilt for a total dose of $4x10^{15}$ cm^{-2}. This implant gives better dopant concentration in the silicon layer, but does not adequately reach regions under the gate overhang.

As can be seen in figure 5.22, lowering the implant energy from 35KeV to 5KeV gives better dopant concentration in the silicon layer. However, under closer examination, it is still not an optimal implant. Due to the 0.1μm overhang of the poly and the shape of the undercut oxide, a small, undoped region exists between the channel and implanted source/drain regions. This will increase the series resistance of the devices.

A series of implant tilt angles were simulated to eliminate the undoped region between the source/drain and gate. These implants had tilt angles ranging from 5 degrees to 35 degrees. The 35-degree simulation results are shown below in figure 5.23.

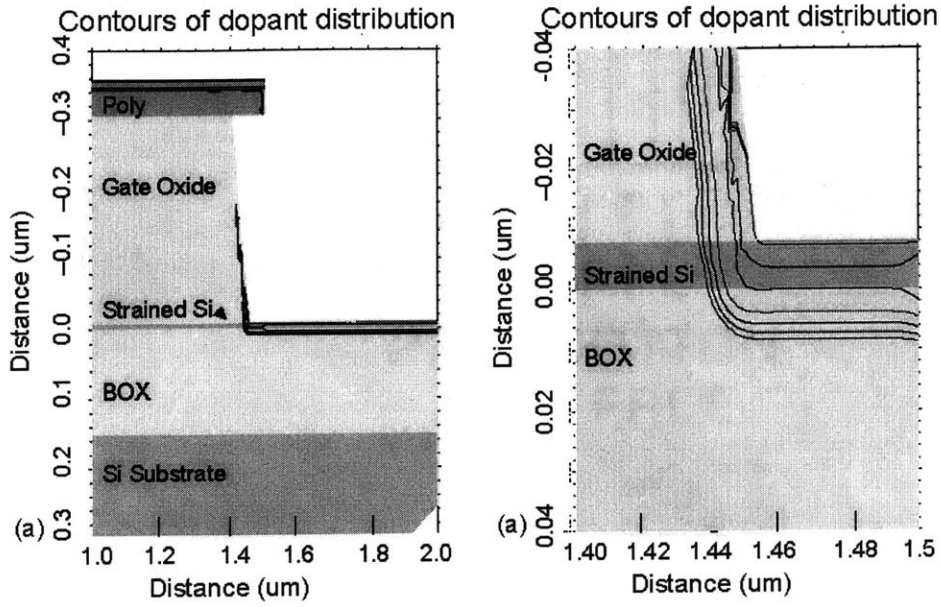


Figure 5.23 - Implant of As at 5 KeV using tilt of 35 degrees from the surface normal. This implant gives better dopant concentration in the silicon layer and adequately reachs regions under the gate overhang.

As with the previous 5 KeV, 7-degree implant, this implant gives reasonable dopant concentrations in the source/drain regions. By increasing the tilt of the implant dopants are able to reach the edge of the gate. While this implant is suitable for the source/drain implant it is not adequate for doping the gate. Therefore, an additional implant is needed for polysilicon doping or *in-situ* doped polysilicon could be used. Without one of these two options the device will suffer from polysilicon gate depletion.

5.6 Summary and Conclusions

Ultra-thin SSOI NMOSFETS were fabricated using a one-mask ring MOSFET design. These devices exhibited transistor-like characteristics, but suffered from suppressed current levels and high series resistance. TSUPREM-4 simulations of the device show that the implant used was not optimal for the thin body structure due to loss of dopants in the buried oxide. Further simulations show that a decrease

in the implant energy from 35 KeV to 5 KeV will allow more dopants to be implanted in the silicon layer resulting in adequate source drain doping levels. An increase in the tilt of the wafer during implant will allow the dopants to be implanted in the undercut region and therefore form a low resistance path from the channel to the source and drain.

Chapter 6

SUMMARY

The goal of this work has been to create ultra-thin SSOI, while maintaining the strain in the silicon layer. A wide variety of experiments were performed to analyze the SSOI fabrication process, to determine if the stain remains in ultra-thin SSOI layers, and to test the SSOI device performance. As a result of these experiments, the fabrication of 13 nm-thick strained silicon directly on insulator has been successfully demonstrated. The fabrication of SSOI wafers is promising for the future fabrication of state-of-the-art devices combining the mobility enhancements of strained silicon and the improved scalability and performance of fully depleted SOI.

6.1 Summary

In this work, ultra-thin strained silicon directly on insulator layers were fabricated using a flip, bond and etch process. This process relies on the use of dual etch stops to achieve across wafer uniformity. For SSOI creation, it is crucial to have selective etches with high selectivity to allow the use of thin etch stop layers and low RMS roughness in the resulting films. Selective Si and SiGe etches were

characterized for use in this process. Two suitable etchants for etching of SiGe to stop on Si are $HF:H_2O_2:CH_3COOH$ and $H_2O:H_2O_2:NH_4OH$. The selectivity of both etches is due to the rapid oxidation of germanium by H_2O_2. The selectivity of these etches is approximately 20:1. Due to the high etch rate, $HF:H_2O_2:CH_3COOH$ is used to etch large amounts of SiGe while $H_2O:H_2O_2:NH_4OH$ is used for a more controlled etch. $H_2O:H_2O_2:NH_4OH$ has a much lower etch rate with a comparable 18:1 etch rate and $H_2O:H_2O_2:NH_4OH$ does not roughen the surface a much as $HF:H_2O_2:CH_3COOH$. TMAH was primarily used to etch Si and stop on SiGe, but KOH is another possible silicon etch. With the addition of IPA to the KOH and TMAH etches the resulting surface roughness can be reduced by a factor of two. While this should improve the resulting roughness of the final SSOI layer from the current ~1 nm RMS observed, further studies are needed to produce layers with suitable RMS roughness for device fabrication.

The strained silicon on insulator layers were characterized to determine material quality, thickness uniformity, and strain behavior. The thickness of the strained silicon layers transferred was approximately 13 nm. Currently, such layers have a RMS roughness near 1 nm. UV Raman analysis confirms that the strain remains after the removal of the SiGe layer that originally induced the strain. The observed strain remains unchanged during RTAs typical of source drain activation anneals in MOSFET processes. The particular properties of the bonding interface contribute to maintaining the strain of thin strained silicon on insulator layers. The $Si\text{-}SiO_2$ bonded interface is strong enough to maintain the 1.2% strain in the silicon film. The film is also below the critical thickness. Therefore, it is energetically favorable for the film to remain strained rather than relax via dislocation formation. These two properties allow the film to remain strained after the removal of the SiGe that originally induced the strain into the silicon. Due to the maintenance of this strain, such ultra-thin strained silicon on insulator structures are promising for the fabrication of ultra-thin body or double-gate strained Si MOSFETs.

The creation of ultra-thin SSOI substrates allows the fabrication of devices, combining the advantages of strained silicon on insulator with ultra-thin body device design. In this work, ultra-thin strained silicon on insulator devices were fabricated using a simple one-mask process. These devices exhibit MOSFET behavior, but suffer from high series resistance and therefore reduced current levels. Drain currents were suppressed by four orders of magnitude from the silicon control devices. TSUPREM simulations were completed to model the fabrication process. It has been concluded that the one level ring MOSFET process as well as the implants were not optimal for the ultra-thin silicon. While these devices did not enable the measurement of mobility, they do show that devices can be fabricated in the thin strained silicon layers that exhibit MOSFET characteristics. Therefore, a more optimal process should be investigated to improve the device performance.

6.2 Contributions

The contributions of this work are:

- Completed bonding experiments to compare bonding with LTO planarization layer and direct bonding to oxidized handle wafer. It was concluded that for low Ge content wafers with limited re-growth and negligible crosshatch both methods are acceptable. For wafers with larger roughness the LTO planarization layer is necessary for bonding.

- Developed an annealing procedure to minimize formation of voids from trapped gas during bonding. Anneal includes both a low temperature step of 400°C to allow diffusion of trapped gas and a higher temperature step for increased bond strength.

- Demonstrated bond strengths of epitaxial wafers for SSOI formation equal to the bond strengths of silicon control samples, thus showing film delamination due to bond strength will not be an issue for SSOI formation.

- Characterized SiGe etches including $HF:H_2O_2:CH_3COOH$ and $H_2O:H_2O_2:NH_4OH$ for etching of SiGe to stop on silicon. Both etches are adequate for etching of SiGe layers to stop on very thin strained silicon layers, but need to be optimized to limit surface roughness. $HF:H_2O_2:CH_3COOH$ provides the benefit of a higher etch rate, but roughens the surface more than $H_2O:H_2O_2:NH_4OH$. Both etches have a selectivity of ~20:1.

- Characterized KOH and TMAH etches for etching of silicon to stop on SiGe and the effect of IPA ratio on the resulting surface roughness. KOH (10% by wt.) in a 1:1 ratio with IPA exhibited the overall lowest surface roughness with about a factor of 2 improvement from TMAH (25% by wt.).

• Developed a process for strained silicon layer transfer based on epitaxial growth, bonding and etch back including dual etch stop layers. Selective etches allow Si and SiGe layers to serve as etch stops.

• Fabricated 13 nm-thick strained silicon on insulator layers with good across wafer thickness uniformity and RMS roughness ~ 1 nm.

• Demonstrated via UV Raman that silicon remains fully strained after layer transfer process including the removal of SiGe that induced the strain. This proves the SiGe underlying layer is not necessary to maintain the strain in the silicon layer. Samples of strained silicon directly on insulator and strained silicon on thin SiGe on insulator exhibit same amount of strain as transferred and after annealing

• Demonstrated that ultra-thin strained silicon on insulator layers remain fully strained after rapid thermal annealing of SSOI layers at 900C for 1 second.

• Fabricated ring MOSFET devices on strained silicon on insulator wafers exhibiting transistor-like characteristics, but with drain current greatly reduced from the silicon control, due to series resistance effects.

• Completed TSUPREM-4 simulations showing the source drain implant used in UTB MOSFETS was not optimal. An As implant of low energy and high tilt is needed for these devices. An As implant of 5 KeV and 35-degree tilt was shown to be adequate for source/drain doping.

• Completed contamination studies with TXRF and SIMS for post-CMP cleaning procedures. From these studies it can be concluded that a post CMP clean is necessary. A clean on double piranha + full RCA + HF dip will remove metallic and mobile ion contaminates to an acceptable level. The final HF dip is crucial for the removal of Na and K.

6.3 Suggestions for Future Work

In discussions about the properties of strained silicon on insulator films areas in need of further research have been mentioned. Some suggestions of possible future work are listed below.

- While layers with uniform thickness have been fabricated, RMS surface roughness remains a key issue. The development of a dry etch or use of optimal etch scheme to reduce surface roughness is needed. The use of sacrificial oxidation and HF removal could also be used to reduce roughness.

- Investigation of the use of smart-cut would also be a potential solution to minimize surface roughness. Smart-cut would eliminate etching through the graded buffer layer. This method would allow layers with higher Ge fraction and more strain to be more easily investigated.

- The addition of additional CMP steps during the etch-back process for reduction of roughness should also be considered. CMP could be used either to remove the silicon etch stop or directly after etch stop removal, leaving only a small amount of film to be etched before reaching the silicon channel.

- In order to fully demonstrate the benefits of strained silicon on insulator, devices must be fabricated and analyzed.

- In order to understand the relation of critical thickness to the strain in SSOI, a critical thickness study is needed. SSOI substrates fabricated with varying strained silicon thickness from 15-nm to 50-nm will allow Raman comparisons of the strain level. Comparing these samples before film transfer, after transfer, and after

annealing could be used to determine the dependence of strain relaxation on film thickness.

- Experiments to understand how the oxide/silicon interface affects the strain in strained silicon films. The use of other insulators for the buried insulator layer could also be investigated.

- Further Raman studies could be completed to fully understand strain relaxation (or lack thereof) in thin strained silicon on insulator films.

- Fabrication of strained silicon on insulator layers with high apparent Ge fraction and therefore higher strain levels to maximize the mobility enhancements for both electrons and holes.

- Development of an in-situ smoothing etch during epitaxial growth for elimination of crosshatch on SiGe virtual substrates. This would eliminate the need to CMP and clean the wafers therefore eliminating the contamination concern and reducing the time of growth.

- While bonding was shown for 30% SiGe substrates, substrates with higher Ge content will exhibit a larger thermal mismatch and more crosshatch. Therefore, bonding experiments for high Ge content should be completed.

- In other work, it has been shown that hole mobility is increased in a dual layer structure. The UTB device design will allow greater hole mobility due to operation at low Eeff, but the transfer of a dual layer structure could provide largest mobility enhancements for both electrons and holes.

- As the strained silicon thickness is further reduced from the current 13-nm thick films cleaning procedures to reduce the loss of silicon will need to be developed.

- The interface of silicon to deposited oxide can contain a large amount of fixed charge. In these devices there will be two silicon – oxide interfaces. One from the buried oxide and one from the top gate oxide. A study of fixed charge at the back interface dependent on the bonding interface would allow an optimal bonding procedure for device fabrication to be developed.

Appendix A

POST-CMP CONTAMINATION STUDY

SiGe graded buffer layers grown on silicon substrates exhibit large roughness due to crosshatch formed during growth. A graded buffer layer of 25% will have a peak to valley roughness of approximately 11 nm. Therefore, in order to form uniform, bondable SiGe heterostructures SiGe virtual substrates are subjected to CMP to reduce roughness before re-growth of the final epitaxial layers. In this study, contamination from CMP is quantified and contamination reduction after cleaning is demonstrated.

A.1 CMP Process and Post-CMP Clean

A post CMP clean is completed for removal of particles and contaminates from the wafer surface. For this work, CMP was completed at Polishing Solutions, an external vendor. The first step of cleaning, completed by the vendor, consisted of a mega-sonic solution of dilute H2O:H2O2:H2SO4 (SC1) followed by a spin rinse dry (SRD). Further cleaning was completed at MIT to further reduce the contamination levels. The cleaning consisted of a double piranha post-CMP clean of 5 minutes H_2O_2:H_2SO_4 (1:3), 15-second HF dip, and 5 minutes H_2O_2:H_2SO_4 (1:3). A modified RCA was then completed as follows: 10 minute H_2O_2:H_2SO_4 (1:3) + 15

second HF dip + 15 minute H_2O:H_2O_2:HCL + SRD. This procedure is summarized in figure A.1. The H_2O_2:H_2SO_4 removes organics and replaces the typical SC1 solution of H_2O:H_2O_2:NH_4OH to reduce material loss. The H_2O:H_2O_2:HCL removes metallic and mobile ion contaminates. The complete cleaning procedure is summarized in figure A.1.

step	Chemical	ratio	time	temperature
0	*dilute H_2O: H_2O_2: H_2SO_4	---	---	---
1	H_2O_2:H_2SO_4	1:3	5 min	reaction determined
2	H_2O:HF	50:1	15 sec	room temperature
3	H_2O_2:H_2SO_4	1:3	5 min	reaction determined
4	DI water SRD	n/a	5 min	n/a
5	H_2O_2:H_2SO_4	1:3	10 min	reaction determined
6	H_2O:HF	50:1	15 sec	room temperature
7	H_2O:H_2O_2:HCL	5:1:1	15 min	80 C
8	H_2O:HF	50:1	15 sec	room temperature
9	DI water SRD	n/a	5 min	n/a

* Proprietary meagasonic clean completed at CMP vendor site

Figure A.1 – Post CMP cleaning procedure.

A.2 TXRF Analysis for Metal Contamination

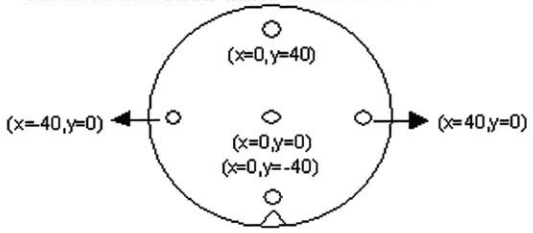
One bare silicon 6" wafer and two SiGe virtual substrates (25% Ge) wafers were submitted to the Microcontamination Lab at National Semiconductor for TXRF analysis to determine surface trace metal contamination. The bare Si wafer and one SiGe virtual substrate were cleaned separately before TXRF analysis using the procedure outlined in section A.1 but with step 9 the final HF dip omitted. The second SiGe wafer was only cleaned using the dilute SC1 + SRD at the CMP vendor site. The wafers were analyzed at five spots to give statistically meaningful data. Each sampling spot encompasses about a 10 mm diameter surface area for analysis and the analysis samples at most a depth of 100 angstroms. The 6" bare Si wafer was analyzed for Na, Mg, Al, P, S, Cl, K, Ca, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Zn, Br by TXRF. Due to spectral overlaps from Ge, light element analysis (Na, Mg, Al) using

the W-M beam could not be performed for the wafers with a SiGe layer. TXRF data is shown in figures A.2 and A.3.

TXRF WAFER SURFACE METALLIC CONTAMINATION MONITORING

Quantitative Analysis of Bare Si Wafer

All concentration units are E10 Atoms/cm^2.



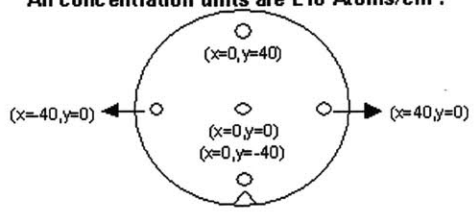
	Slot #1 Bare Si + clean									
	x	y	x	y	x	y	x	y	x	y
Element	0	0	40	0	0	40	-40	0	0	-40
Na	<71		<71		<71		<71		<71	
Mg	<42		<42		<42		<42		<42	
Al	<55		<55		<55		<55		<55	
S	2627		2426		2490		1948		1808	
Cl	645		655		673		607		674	
K	<3		<3		<3		<3		<3	
Ca	<2		<2		<2		<2		<2	
Ti	<0.7		<0.7		<0.7		<0.7		<0.7	
V	<0.4		<0.4		<0.4		<0.4		<0.4	
Cr	<0.3		<0.3		<0.3		<0.3		<0.3	
Mn	<0.2		<0.2		<0.2		<0.2		<0.2	
Fe	0.5		0.5		0.6		0.5		0.8	
Co	<0.1		<0.1		<0.1		<0.1		<0.1	
Ni	0.4		0.4		0.4		0.5		0.5	
Cu	<0.3		<0.3		<0.3		<0.3		<0.3	
Zn	<0.4		<0.4		<0.4		<0.4		<0.4	
Br	85		92		109		106		83	

Figure A.2 – TXRF analysis on Si control wafer after clean. Analysis completed by Craig Seeley of National Semiconductor.

TXRF WAFER SURFACE METALLIC CONTAMINATION MONITORING

Quantitative Analysis of SiGe Wafers

All concentration units are E10 Atoms/cm².



	Slot #15 CMP SiGe + clean										Slot #25 CMP SiGe w/o clean									
	x	y	x	y	x	y	x	y	x	y	x	y	x	y	x	y	x	y	x	y
Element	0	0	40	0	0	40	-40	0	0	-40	0	0	40	0	0	40	-40	0	0	-40
S	2508		2461		3000		2559		2349		1176		1042		984		854		1095	
Cl	382		383		374		381		401		90		92		87		112		233	
K	<3		<3		<3		<3		<3		<3		<3		<3		<3		<3	
Ca	<2		<2		<2		<2		<2		17		52		42		35		184	
Ti	<0.7		<0.7		<0.7		<0.7		<0.7		<0.7		<0.7		<0.7		<0.7		27.2	
V	<0.4		<0.4		<0.4		<0.4		<0.4		<0.4		<0.4		<0.4		<0.4		<0.4	
Cr	<0.3		<0.3		<0.3		<0.3		<0.3		<0.3		<0.3		<0.3		<0.3		0.7	
Mn	<0.2		<0.2		<0.2		<0.2		<0.2		<0.2		<0.2		<0.2		<0.2		0.7	
Fe	<0.1		<0.1		1.0		0.5		0.8		0.6		0.6		0.4		0.6		11.7	
Co	<0.1		<0.1		<0.1		<0.1		<0.1		<0.1		<0.1		<0.1		<0.1		<0.1	
Ni	0.7		0.7		0.7		0.7		0.7		0.8		0.8		0.7		0.9		0.5	
Cu	<0.3		<0.3		<0.3		<0.3		0.5		<0.3		<0.3		<0.3		<0.3		<0.3	
Zn	<0.4		<0.4		<0.4		<0.4		<0.4		16.2		37.3		22.2		14.9		21.9	
Br	44		24		42		37		43		23		23		18		<2		<2	

Figure A.3 – TXRF analysis on SiGe wafer before and after cleaning. Analysis completed by Craig Seeley of National Semiconductor.

The bare Si and SiGe wafers all had detectable levels of S, Cl and Br. Trace levels of Fe and Ni were evident on all wafers. The SiGe wafer after CMP without clean had notable increases in contamination from Ca and Zn when compared to the wafer with the cleaning step. Furthermore, the analysis spot near the flat (0, -40) had detectable and/or higher concentrations of Ca, Ti, Cr, Mn, Fe, and Zn. Notable reductions were shown in contamination levels after cleaning.

A.3 SIMS Analysis for Na and K Contamination at National Semiconductor

One bare silicon 6" wafer and two SiGe (25% Ge) 6" wafers were submitted to National Semiconductor and Thanas Budri completed the SIMS analysis for Na and K contamination. The bare Si wafer and one of the SiGe wafers were cleaned

before analysis using the procedure outlined in section A.1 omitting step 9, the final HF dip. The second SiGe wafer was only cleaned using the dilute SC1 + SRD at the CMP vendor site.

SIMS analysis was performed using O2+ as primary ions with Oxygen leak to enhance the ion yields. CEA RBS calibrated standards in Si are measured in order to quantify the results. The matrix effects related to Ge (25%) content are taken into account during quantification. The results are summarized below in figure A.4:

Element	Si+ clean	SiGe + clean	SiGe
K39	3.0e9atoms/cm2	7.3e9atoms/cm2	1.5e10atoms/cm2
Na23	2.0e10atoms/cm2	9.4e10atoms/cm2	3.7e12atoms/cm2

Figure A.4 – Integrated dose calculations for Si and SiGe wafers. Analysis completed by Thanas Budri at National Semiconductor.

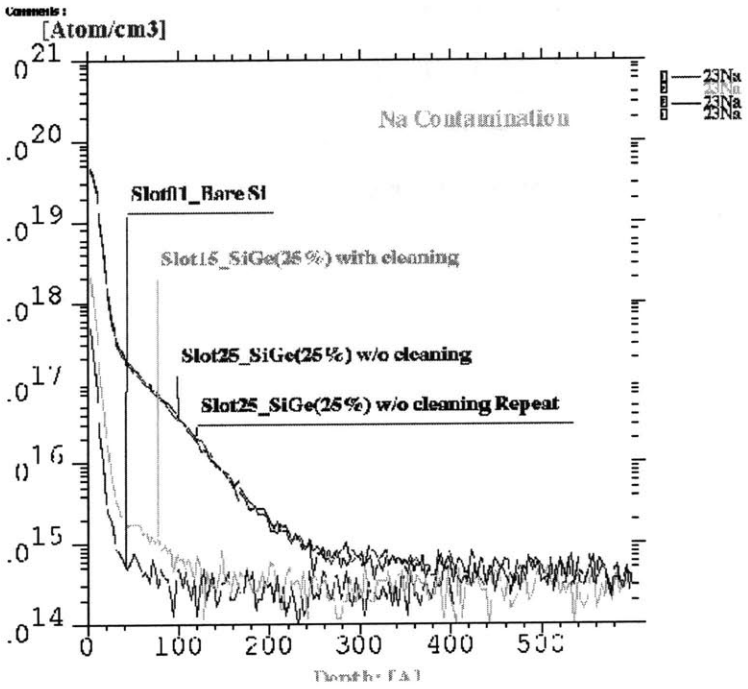


Figure A.5 – SIMS analysis of Si and SiGe wafers for Na contamination. Analysis completed by Thanas Budri of National Semiconductor.

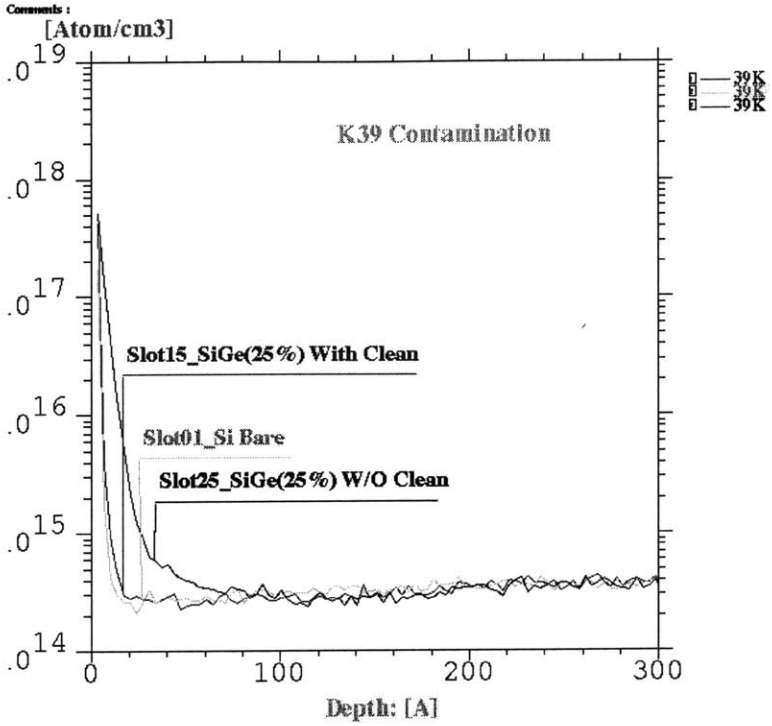


Figure A.6 – SIMS analysis of Si and SiGe wafers for K contamination. Analysis completed by Thanas Budri of National Semiconductor.

From the SIMS analyzed data elevated Na23 contamination levels are shown from the SiGe wafer without further cleaning upon return from the CMP vendor. In case of K39 there is a detected increased contamination by 50% in the SiGe sample without the clean compared to the cleaned wafer.

A.4 SIMS Analysis for Na and K Contamination at Charles Evans and Associates

SIMS analysis for Na and K was also conducted at Charles Evans and Associates (CEA). The wafers analyzed were one silicon control + full clean as described in A.1, one SiGe wafer after CMP + full clean, and one SiGe wafer directly after epitaxial growth. It is important to realize that these wafers received a final HF dip. The CMP wafers again have slightly elevated contamination levels

compared to the silicon control , but the absolute contamination level is in a more acceptable range as seen in the following figures.

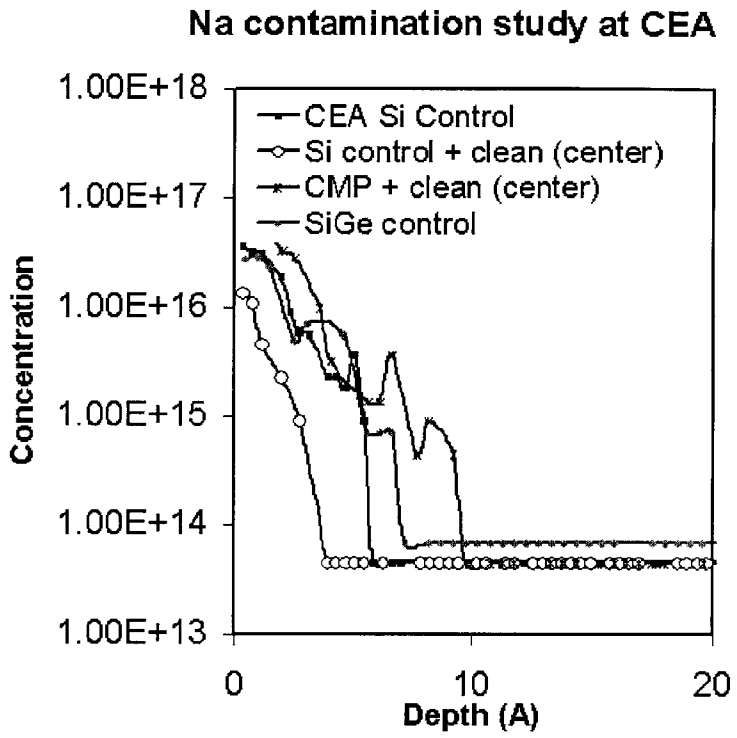


Figure A.7– SIMS analysis of Si and SiGe wafers for Na contamination. Analysis completed at CEA.

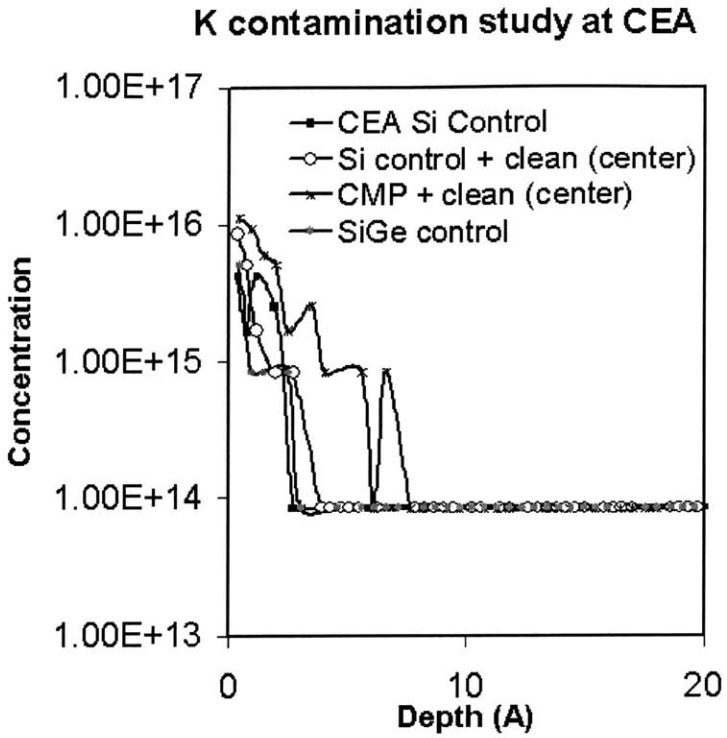


Figure A.8– SIMS analysis of Si and SiGe wafers for K contamination. Analysis completed at CEA.

Summary of Na and K levels:

Wafer	Na (cm-2)	K (cm-2)
CEA blank	7.81E+08	8.61E+07
Si control + clean	1.97E+08	1.02E+08
Si control + clean (R/2)	2.41E+08	1.32E+08
CMP SiGe + clean	2.61E+09	7.07E+08
CMP SiGe + clean (R/2)	1.52E+09	2.68E+08
SiGe control	7.41E+08	5.67E+07

Figure A.9 – Integrated dose calculations of Na and K for Si and SiGe wafers. SIMS completed at Charles Evans.

A.5 Summary

From these 3 studies it is clear the post CMP clean is needed for reduction contamination levels. The HF dip at the end also is key to the success of the clean. There are differences in the absolute value of Na and K contamination seen from National and CEA. There are two differences in the wafers and clean which could account for this discrepancy. First, the wafers for National were subject to CMP at a later time with a run for another customer. Potentially there is contamination from the other customer or at Polishing Solutions since the time of the first CMP run which contained the wafer sent to CEA for analysis. The second potential difference is the clean for the wafers sent to National did not include the final HF dip that was used for the wafers sent to CEA.

When the clean is completed carefully it should be acceptable to place a limited number of wafers from CMP into the epi tool due to the absolute levels of metallic and Na and K contamination, but the levels will need to be re-confirmed on a periodic basis.

Appendix B

BONDING FOR BURRIED OXIDE FORMATION

Formation of ultra-thin strained silicon on insulator layers relies on bonding epitaxial wafers either directly to thermal oxide or with a deposited planarization layer such as low temperature oxide (LTO). This appendix summarizes the bonding of strained silicon for layer transfer.

B.1 Deposited Low Temperature Oxide for Bonding

B.1.1 Experimental Procedure

LTO was deposited and densified on p- prime CZ silicon and strained silicon wafers. Thermal oxide was grown on p- prime CZ silicon wafers to serve as handle wafers. The LTO donor wafers were subjected to different CMP parameters (time, rotation, down force, back pressure) to determine an optimal CMP procedure. A split was done to have 2 each of 5, 10, 20, and 30 seconds. There was also a wafer that was subjected to CMP for 10sec on each 90-degree rotation and one that had no CMP as summarized in figure B.1.

Wafer #	CMP time (seconds)
Bond5	5
bond10	10
bond20	20
bond30	30
AFM5	5
AFM10	10
AFM20	20
AFM30	30
sicmp	20
sinocmp	0
sige	20

CMP table settings	
settings	value
Table	25
Quill	50
Down force	4
Slurry	150
rate	~12.5A/sec

Figure B.1 – CMP conditions for LTO bonding study

Film thickness and uniformity were measured before and after CMP. The wafers were cleaned in the CMP room with the PVA sponges. A post CMP clean of Piranha (yellow), HF dip (yellow 50:1), Piranha (green) was used to re-enter the clean room. Before bonding, an activation process of either Piranha + HF or standard RCA with extra HF dip at the end was used. All wafers were spin-dried and bonded using fusion.aba program in the Evaligner bonder in TRL. The purpose of this experiment was to measure the effect of time on removal rate, uniformity, and surface roughness. This experiment will also to determine the effect of wafer bow on bonding.

B.1.2 Affect of Wafer Bow on Bonding

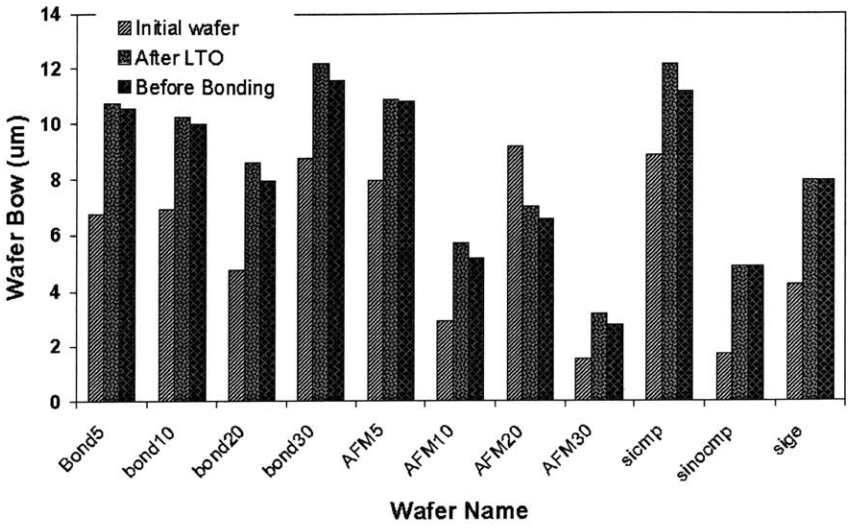


Figure B.2 – Wafer bow due to deposition of LTO. Measurements taken before LTO deposition, after LTO deposition, and after CMP.

On average bow increased with deposition of LTO and then slightly decreased with CMP.Wafer Bow before bonding was on average less than 12 um. This was not a significant enough bow to affect the bonding.

B.1.3 Effect of CMP Conditions on Uniformity, Removal, and RMS Roughness

While the CMP conditions did not greatly affect the wafer bow for bonding, CMP conditions greatly affect the uniformity of the LTO after CMP. For successful bonding both long and short-range uniformity are important. Ultimately, unless gross long-range non-uniformity is present the short-range roughness will dominate the bonding. This is due to the ability of the wafers to bow to accommodate the long-range thickness differences. To test the affect of CMP on the thickness uniformity a set of 9 wafers were subjected CMP with down force of 1, 2, and 4 and back pressure combinations of 3, 4, and 5. As seen in figure B.3 and B.4 the removal rate and

thickness deviation were greatly affected by the changes in these two key CMP parameters.

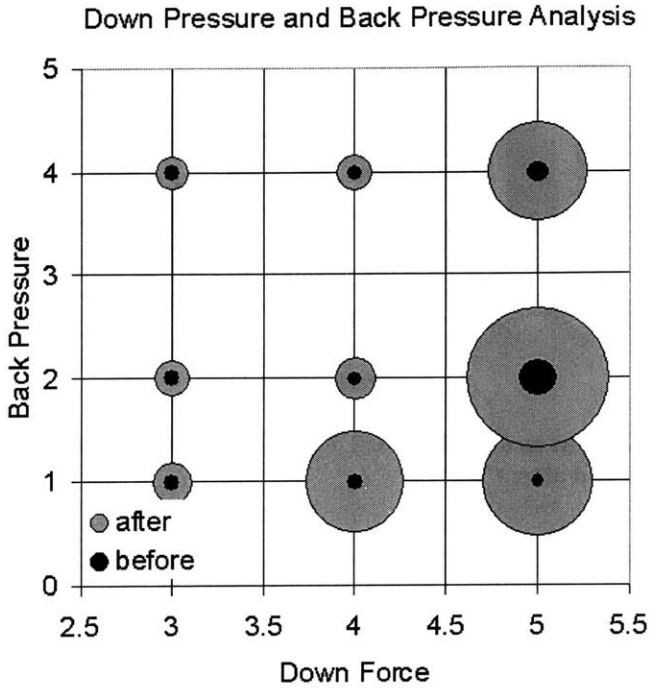
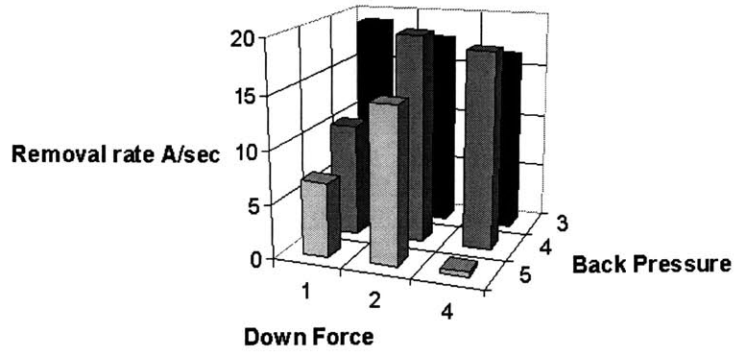


Figure B.3 – Thickness deviation due to changes in back pressure and down force. Smaller light circle shows the thickness deviation before CMP, larger dark circle shows the LTO thickness deviation after CMP. From these results an optimal range of operation can be determined.

The area of black inner circle represents the standard deviation in thickness before CMP. The area of dark gray outer circle represents the standard deviation in thickness after CMP. As seen in figure B.3, there is a distinct regime of operation where the thickness uniformity is most optimal.



	1	2	4
5	6.9525	14.62025	0.4825
4	10.4785	19.4105	18.25925
3	19.177	17.726	16.5105

Figure B.4 – LTO removal rate dependence on downforce and back pressure. Removal rates increase as the back pressure decreases and down force increases.

From the removal rate and uniformity measurements an optimal down force and backpressure can be chosen based on the uniformity and removal rate desired.

B.1.3 AFM study of Short-range Non-uniformity

Not only does the long-range non-uniformity affect the bonding, short-range non-uniformity also plays a key factor. Atomic force microscopy (AFM) was used to find the roughness dependence on the above parameters. These results are summarized in figure B.5.

AFMRESULTS bow - um roughness - nm			
		initial wafers	with LTO
CMP time: 5 seconds			
	Mean Roughness (top)	0.81	0.622
	Mean Roughness (left)	0.451	0.642
	Mean Roughness (middle)	0.627	0.701
	Mean Roughness (right)	0.178	0.888
	Mean Roughness (bottom)	0.656	0.932
	Bow	10.88	10.79
CMP time: 10 seconds			
	Mean Roughness (top)	0.426	0.754
	Mean Roughness (left)	0.51	0.918
	Mean Roughness (middle)	0.433	0.718
	Mean Roughness (right)	0.99	1.89
	Mean Roughness (bottom)	0.622	0.796
	Bow	5.71	5.2
CMP time: 20 seconds			
	Mean Roughness (top)	0.833	0.857
	Mean Roughness (left)	0.294	0.463
	Mean Roughness (middle)	1.129	0.692
	Mean Roughness (right)	0.416	0.401
	Mean Roughness (bottom)	0.797	0.51
	Bow	7.01	6.6
CMP time: 30 seconds			
	Mean Roughness (top)	0.532	0.709
	Mean Roughness (left)	0.645	0.579
	Mean Roughness (middle)	0.874	0.812
	Mean Roughness (right)	0.89	2.368
	Mean Roughness (bottom)	1.03	0.579
	Bow	3.15	2.8

Figure B.5 – AFM data for LTO roughness before and after CMP for bonding

B.2 Comparison of LTO-Si, Thermal-Si, and Oxide-oxide Bonding

Three bonding methods were investigated including LTO bonded to silicon, LTO bonded to thermal oxide, and Silicon-to-thermal-oxide as shown in figure B.6. To determine the best bonding procedure for strained silicon wafers.

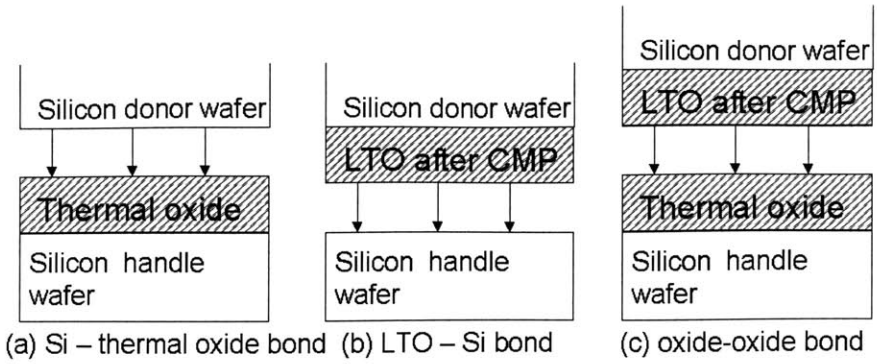


Figure B.6 – Schematic representation of three bonding methods investigated

A summary of the matrix used for this study is shown in figure B.7.

Wafer #	Type	Thickness	Densify T	Densify Time	CMP (sec)	neal Temp	Prep		handle #	type	Thickness
Test of Si-SiO2 bond											
1	thermal	500A	no	no	no	400	P+HF+SC2+P		1	CZ Si	n/a
2	thermal	1500A	no	no	no	400	P+HF+SC2+P		2	CZ Si	n/a
3	thermal	3000A	no	no	no	400	P+HF+SC2+P		3	CZ Si	n/a
Test of Si-LTO bond											
4	LTO	1500	800	1	30	400	P+HF+SC2+P		4	CZ Si	n/a
5	LTO	1500	800	1	60	400	P+HF+SC2+P		5	CZ Si	n/a
6	LTO	3000	800	1	30	400	P+HF+SC2+P		6	CZ Si	n/a
7	LTO	3000	800	1	60	400	P+HF+SC2+P		7	CZ Si	n/a
Thermal-Thermal CMP test											
8	thermal	1500	no	no	no	400	RCA+HF		8	Thermal	500
9	thermal	1500	no	no	30	400	RCA+HF		9	Thermal	500
10	thermal	1500	no	no	60	400	RCA+HF		10	Thermal	500
11	thermal	3000	no	no	no	400	RCA+HF		11	Thermal	500
12	thermal	3000	no	no	30	400	RCA+HF		12	Thermal	500
13	thermal	3000	no	no	30	400	RCA+HF		13	Thermal	500
LTO Densification											
14	LTO	1500	700	1	45	400	RCA+HF		14	Thermal	500
15	LTO	1500	700	2	45	400	RCA+HF		15	Thermal	500
16	LTO	1500	700	3	45	400	RCA+HF		16	Thermal	500
17	LTO	1500	700	12	45	400	RCA+HF		17	Thermal	500
18	LTO	1500	800	1	45	400	RCA+HF		18	Thermal	500
19	LTO	1500	800	3	45	400	RCA+HF		19	Thermal	500
20	LTO	1500	800	5	45	400	RCA+HF		20	Thermal	500
21	LTO	1500	800	12	45	400	RCA+HF		21	Thermal	500
22	LTO	1500	850	0.5	45	400	RCA+HF		22	Thermal	500
23	LTO	1500	850	1	45	400	RCA+HF		23	Thermal	500
24	LTO	1500	850	3	45	400	RCA+HF		24	Thermal	500
25	LTO	1500	900	0.5	45	400	RCA+HF		25	Thermal	500
26	LTO	1500	900	1	45	400	RCA+HF		26	Thermal	500
Handle for SiGe											
27	SiGe	n/a	n/a	no	no	400	RCA+HF		27	Thermal	500
									28	Thermal	1500
									29	Thermal	3000

Figure B.7 – Bonding experiment to differentiate methods of bonding.

From this extensive matrix, it was determined that the best bonding occurred for silicon wafers bonded directly to the thermally oxidized handle wafers. This bonding can only occur for low Ge fraction wafers where the crosshatch is minimal. This study also showed a dependence of void formation on oxide thickness. If the oxide thickness was below 500-1000A bonding would produce many voids.

B.3 Summary and Conclusions

Bonding of epitaxial wafers is necessary for SSOI formation by layer transfer. Bonding options vary dependent on choice of planarization method. For most optimal bonding virtual substrates should be subjected CMP during growth to reduce crosshatch making it easier to establish good bonds. If the epitaxial wafers exhibit roughness in excess of ~5A an LTO planarization layer becomes necessary. CMP conditions can greatly affect the removal of LTO and therefore should be carefully controlled. Bonding has been shown via both methods and therefore SSOI materials can be fabricated.

Appendix C

SHORT FLOW MOSFET FABRICATION SEQUENCE

C.1 Ring MOSFET Fabrication

The following table outlines the process and machines used for the fabrication of one level MOSFETs. The MTL fabrication facilities were used for this processing.

Process step	Description	MTL tool	MTL lab
Gate Stack Deposition			
1	Short rca clean for reduced Si and SiGe loss	rca hood	ICL
1(a)	10 min green piranha	rca hood	ICL
1(b)	30s standard HF dip	rca hood	ICL
1(c)	15min SC-2	rca hood	ICL
2	LPCVD 3000A LTO deposition, at 400C recipe LTO 400, 58min	Tube 6C	ICL
3	LPCVD 500A polysilicon deposition at 560C	Tube6A	ICL
Backside clear			
4	HMDS deposition	HMDS	ICL
5	Coat frontside & hardbake resist prebake 115C postbake 130C	Coater6	ICL
6	Native oxide strip BOE, 5s	oxide	ICL
7	Etch Backside polysilicon recipe POLY_STD	AME5000	ICL
8	BOE etch backside LTO 20-30s	oxide	ICL
9	Ash photoresist 120s	asher	ICL

Device Patterning			
10	HMDS Deposition	HMDS	ICL
11	Photoresist Coat	Coater6	ICL
	with prebake only		
	at 115C		
12	Exposure with MOBIL	Stepper2	ICL
	Mask		
13	Photoresist Develop	Developer	ICL
14	Postbake Resist	Coater6	ICL
15	Etch frontside	AME5000	ICL
	polysilicon		
16	Check LTO thickness	UV1280	ICL
17	Etch frontside LTO	AME5000	ICL
	30s, poly_std recipe		
18	Ash resist	asher	ICL
	standard recipe, 120s		
19	BOE undercut of	oxide	ICL
	polysilicon		
	4s for 300A undercut		
Source/Drain Implantation			
20	Implant source/drain/gate	outside vendor	
21	Post-implantation	Premetal	ICL
	piranha clean		
	blue premetal 60s,green		
	premetal 60s, no HF dip		
22	RTA at 1000C for 1s	RTA2	ICL
Metallization			
23	Pre-metallization piranha	Premetal	ICL
	clean, 60s green premetal		
	20s HF dip		
24	500A Ti/1000A Al at zero	e-beam	ICL
	tilt		
25	1um Al on backside	e-beam	ICL
26	400C sinter in H2/N2 for	Tube A3	TRL
	30min		

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