A New Power Combining and Outphasing Modulation System for High-Efficiency Power Amplification

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A New Power Combining and Outphasing Modulation System for High-Efficiency Power Amplification

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Abstract---**This paper describes a new power combining and outphasing system that provides both high efficiency and linear output control. Whereas conventional outphasing systems utilize two power amplifiers, the system introduced here combines power from four or more amplifiers. The proposed technique overcomes the loss and reactive loading problems of previous outphasing systems. It provides ideally lossless power combining, along with resistive loading of the individual power amplifiers over a very wide output power range. A conceptual development illustrating the operating principles of the system is provided, along with a representative design, detailed analysis, and supporting simulations. The relation of the proposed technique to multi-level resistance compression is also described. It is anticipated that the new power combining and outphasing modulation approach will find widespread use in applications where both high linearity and high efficiency are desired.**

I. Introduction

Radio-frequency (RF) power amplifiers are important in numerous applications, including RF communications, medical imaging, industrial heating and processing, and dc-dc power conversion among many others. Power amplifiers (PAs) are often required to provide *linear* amplification, which encompasses the ability to dynamically control the RF output power over a wide range. This becomes particularly challenging when wide-bandwidth control of the output is required. It is also often desired to maintain high efficiency across a wide range of output power levels, such that high average efficiency can be achieved for highly modulated output waveforms. Simultaneously achieving both of these requirements – wide-bandwidth linear amplification and high average efficiency – has been a longstanding challenge, and is the goal of this paper.

One concept that has been explored for achieving both linear operation and high efficiency is that of *outphasing*. This technique, which originated in the 1930's [1], is also sometimes referred to as "Linear Amplification with Nonlinear Components" or LINC [2]. In conventional outphasing, a desired output signal is decomposed into two constant-amplitude signals which can be summed to provide the desired output (Fig. 1). Because the two signals are of constant amplitude, they can be synthesized with highly-efficient PAs including partially- and fully-switched-mode designs such as classes D [3-5], E [6,7], F [8-10], E/F [11] and current-mode D [12], Inverse F [13], Φ [14,15], etc. (These amplifiers can be made highly efficient in part because they needn't have the capability to provide linear output control.) Combining the two constant-amplitude outputs in a power combining network enables the net output amplitude to be controlled via the relative phase of the two constituent components.

A key consideration with outphasing is how the power combining is done, particularly because many high-efficiency power amplifiers are highly sensitive to load impedance, and their performance and efficiency can heavily degrade due to interactions between the power amplifiers [16-18]. One conventional approach is to use an isolating combiner, as illustrated in Fig. 2 [19]. An isolating combiner provides constant (resistive) loading impedance to each PA independent of the outphasing angle, eliminating any interactions. A consequence of this, however, is that each PA operates at a constant output power level. Power that is not delivered to the output must instead be delivered elsewhere, usually to an "isolation" resistor. This leads to a rapid degradation of efficiency as output power is decreased, diminishing the attractiveness of this approach [19]. This problem can be partially offset by recovering power not delivered to the output through a rectifier [20-22].

A different conventional approach is to use a lossless combiner, such as the classic Chireix combiner [1,16,17,19,23], Fig. 3, or related methods [24-26]. Benefits of the Chireix combining technique, which is non-isolating, include the fact that the combiner is ideally lossless, and that the real components of the effective load admittances seen by the individual power amplifiers vary with outphasing (and power delivery) such that power amplifier conduction losses can be reduced as output power reduces. However, the reactive portions of the effective load admittances are only zero for at most two outphasing angles, and become large outside of a limited power range. This limits efficiency, due both to loss associated with added reactive currents and to degradation of power amplifier performance with (variable) reactive loading [16-18]. It has been observed that the challenges with power combining are a principal reason that outphasing is not a more dominant architecture in RF applications [27].

A goal of the present work is to overcome the limitations of previous outphasing systems. A new power combining and outphasing modulation system is introduced that overcomes the loss and reactive loading problems of previous outphasing approaches. It provides ideally lossless power combining, along with nearly resistive loading of the individual power amplifiers over a very wide output power

range, enabling high average efficiency to be achieved even for large peak-to-average power ratios (PAPR).

Section II of the paper presents a conceptual development to illustrate the operating principles of the system, and also explores the related concept of multi-level resistance compression. Section III presents an example implementation of this new approach, along with detailed analysis and supporting simulations. Section IV describes additional implementations and design possibilities with the proposed system. Finally, Section V concludes the paper.

II. CONCEPTUAL DEVELOPMENT

In this section we provide a conceptual framework to facilitate understanding of the proposed power combining and outphasing system. In addition to illustrating the operating principles of the system, this section explains how implementations of the proposed power combining and outphasing system can be synthesized. As a first step, this section treats a seemingly-unrelated problem – the development of multi-stage resistance compression networks. It is then shown how the design and behavior of multi-stage compression networks can be used for synthesis of lossless power combiners and outphasing control laws.

A. Multi-Stage Resistance Compression

As a route to illustrating the design and behavior of the proposed outphasing system, we first present a brief treatment of multi-stage resistance compression networks. Resistance Compression Networks (RCNs) are a class of lossless interconnection networks for coupling a source to a set of matched (but variable) resistive loads [22, 30, 31]. One basic RCN and its operating characteristic are shown in Fig. 4. As the resistances R_o in Fig. 4 vary together over a range geometrically-centered on X, the input impedance of the network is resistive and varies over a much smaller range than R_o varies. In particular, it can be shown that the input impedance is resistive at the operating frequency and is a function of the load resistance [22, 30, 31]:

$$R_{in} = f(R_o) = \frac{R_o^2 + X^2}{2R_o} \quad \textbf{(1)}$$

As the load resistances R_o vary over the range $[X/b, bX]$, the input resistance varies over the range $[X,kX]$, where k and b are related as

$$b = k + \sqrt{k^2 - 1} \quad and \quad k = \frac{1+b^2}{2b} \quad \textbf{(2)}$$

Because the input impedance is resistive and varies over a much smaller range than the matched load resistances R_o, RCN networks are advantageous in applications such as resonant rectifiers and dc-dc converters [22, 30, 31].

Multi-stage RCNs offer the possibility of even smaller input resistance variations (or wider load resistance ranges) than single-stage designs. Here we present for the first time the design of a multi-stage RCN to provide an input resistance that deviates less than a specified peak amount away from a desired median input resistance value, and determine the load resistance range over which this can be accomplished. In particular, we consider the design of the multi-stage resistance compression network shown in Fig. 5. We will subsequently show how this RCN relates to the proposed outphasing system.

Suppose we would like to design the RCN of Fig. 5 to provide an input resistance $R_{in,2}$ within $\pm\Delta R$ of a desired median value $R_{in,2,med}$ over as wide a range R_o as possible. To do this we select a value k_2 (stage 2 input resistance ratio) of:

$$k_2 = \frac{R_{in,2,med} + \Delta R}{R_{in,2,med} - \Delta R} \quad \textbf{(3)}$$

and select a stage two reactance magnitude of

$$X_2 = \frac{2R_{in,2,med}}{k_2 + 1} \quad \textbf{(4)}$$

which yields:

$$R_{in,2,med} = \frac{k_2 + 1}{2} X_2 \quad and \quad \Delta R = \frac{k_2 - 1}{2} X_2 \,. \quad \textbf{(5)}$$

Next we consider selecting the stage one reactance magnitude X_1 to provide compression into a range that makes best use of the second stage. The effective resistance $R_{in,1}$ seen at the inputs of the first stage has a minimum value of X_1, so to maximize the R_o range over which we achieve the desired compression we select:

$$X_1 = \frac{1}{b_2} X_2 \quad \textbf{(6)}$$

where b_2 is determined from k_2 as per **(2)**. $R_{in,1}$ has a maximum value of k_1X_1 where we find the operating range over which the desired degree of compression is achieved from:

$$R_{in,1,\max} = k_1 X_1 = b_2 X_2 \quad \textbf{(7)}$$

We then get the desired degree of compression over an operating range of R_o in $[X_1/b_1, b_1X_1]$ where b_1 is determined from **(2)** and **(7)**.

Figure 6 shows how the input resistance $R_{in,2}$ varies as a function of load resistance R_o when compression network values are selected as described above. Selection of the compression network reactances as described provides this characteristic, which compresses resistance to a much greater extent than is possible in a single-stage compression network. For example, one can achieve resistance compression of the input resistance to within ±2.5% of the desired median value over a 12:1 ratio in load resistance R_o with this technique. Similar levels of performance can be obtained using other types [30,31] of compression stages. Moreover, even greater levels of resistance compression (or similar resistance deviations over wider ranges of load resistance) can be achieved with more stages.

We will find it useful in the following section to know the load voltages $V_A - V_D$ in terms of the drive voltage V_L. It can be shown that the following relation holds for these voltages:

$$\begin{bmatrix} V_A \\ V_B \\ V_C \\ V_D \end{bmatrix} = V_L \frac{\sqrt{R_o^2 + X_1^2}}{2\sqrt{\left(\frac{R_o^2 + X_1^2}{2R_o}\right)^2 + X_2^2}} \begin{bmatrix} e^{-j\phi}e^{-j\theta} \\ e^{j\phi}e^{-j\theta} \\ e^{-j\phi}e^{j\theta} \\ e^{j\phi}e^{j\theta} \end{bmatrix} \quad \textbf{(8)}$$

where

$$\theta = ATAN\left(\frac{2R_o X_2}{R_o^2 + X_1^2}\right) \quad \textbf{(9)}$$

and

$$\phi = ATAN\left(\frac{X_1}{R_o}\right). \quad \textbf{(10)}$$

The phase relationship of these voltages is illustrated in Fig. 7.

B. Synthesis of Power Combiners and Control Laws

Here we show how the design and behavior of multi-stage compression networks can be used for synthesis of power combiners and outphasing control laws. Consider the two-stage RCN shown in Fig. 5. Suppose we take this network, and change the sign of every reactance and resistance. This is equivalent to taking the network of Fig. 5 and applying type 1 time-reversal duality and then applying type 3 time reversal duality [32,33]. Neglecting the impact upon the natural response of the circuit, the sinusoidal steady-state behavior of such a circuit would have all current flow directions reversed, while preserving voltage relationships in the circuit, thus yielding reversed power flow (i.e. from the – now negative – resistors to the voltage source V_L. The ratio of the voltage V_L to the current flowing *into* V_L would be that of $R_{in,2}$ of the original compression circuit, which is close to the value $R_{in,2,med}$. Likewise, the voltages at the now-negative resistors would be as described in **(8),** and currents proportional to these voltages would flow into the network (i.e., the apparent impedances seen looking into the network ports to which the negative resistances are connected would be resistive with values $|R_o|$.)

To develop a power combining and outphasing system, we take advantage of the above observations. In particular, we replace the source V_L in Fig. 5 with a load resistance $R_L = R_{in,2,med}$ and replace the resistors R_o with voltage sources (or power amplifiers in practice). This leads directly to the system of Fig. 8. Controlling the phases of the sources to match their behavior in the original two-stage resistance compression network, we can then obtain power control over a wide range while preserving nearly resistive loading of the sources (see Section III). While these substitutions do not lead to precise duality between RCNs and the proposed power combining and outphasing system, this approach nonetheless provides a means to develop effective outphasing and power combining systems such as described in Section III.

III. THE NEW OUTPHASING SYSTEM

This section describes the proposed new outphasing system, and provides a detailed analysis of its behavior along with supporting examples. In this section we focus on defining the key system elements and analyzing system behavior.

A. System Structure and Control Law

Figure 8 shows an embodiment of the proposed system. Whereas conventional outphasing systems utilize two power amplifiers, the system proposed here combines power from four or more amplifiers[1]. (Here we treat the case with four power amplifiers; extensions to more than four amplifiers are treated in Section IV.) In Fig. 8, the power amplifiers are modeled as ideal voltage sources; it is recognized, however, that practical power amplifiers may not act as ideal sources when the effective loading impedance deviates from the ideal [18]. The power combiner of Fig. 8 has five ports: four connecting to the power amplifiers and one connecting to the load. It is (ideally) lossless, comprising reactive elements having specified reactances at the operating frequency.

We begin by describing how the reactances in the new combiner may be selected. The reactance magnitude X_2 of the combiner is selected close to the load resistance R_L. In particular, we may specify a number k equal to or slightly greater than 1 (e.g., $k = 1.05$) and determine X_2 as:

$$X_2 = R_L \frac{2}{k+1} \quad \textbf{(11)}$$

We then select reactance magnitude X_1 in terms of X_2 and k, for example as:

$$X_1 = \frac{X_2}{k + \sqrt{k^2 - 1}} \quad \textbf{(12)}$$

Thus, for example, with $R_L = 50\ \Omega$, we may choose $X_2 = 48.78\ \Omega$ and $X_1 = 35.60\ \Omega$ at the operating frequency of the system.

We now analyze the behavior of the network of Fig. 8, and develop a set of relations for controlling the output by outphasing of the sources. The relationship between the source voltages and input currents of the network of Fig. 8 can be shown to be that of **(13)** below, where we define $\gamma = R_L/X_1$ and $\beta = X_2/X_1$. In vector notation we can express this as:

$$\vec{I} = Y \cdot \vec{V} \quad \textbf{(14)}$$

Here we propose a relative phase relationship among the four sources. (The phases may also be adjusted *together* by an additional angle to control the absolute phase of the output.) While other possibilities exist, the following relationship among the sources is proposed:

$$\begin{bmatrix} V_A \\ V_B \\ V_C \\ V_D \end{bmatrix} = V_S \begin{bmatrix} e^{-j\phi}e^{-j\theta} \\ e^{j\phi}e^{-j\theta} \\ e^{-j\phi}e^{j\theta} \\ e^{j\phi}e^{j\theta} \end{bmatrix} \quad \textbf{(15)}$$

where V_S is the amplitude of the sources and φ and θ are the control angles used for outphasing. The relationship among the sources is shown graphically in Fig. 7. (Also, see the relation of the phases to that of the multi-level RCN in **(8)**.)

[1] Outphasing using more than two amplifiers has been previously proposed (e.g., [34, 35]), but not in a manner that yields both resistive loading and lossless combining as sought here.

$$\begin{bmatrix} I_A \\ I_B \\ I_C \\ I_D \end{bmatrix} = X_1^{-1} \begin{bmatrix} \gamma + j(1-\beta) & -\gamma + j\beta & \gamma & -\gamma \\ -\gamma + j\beta & \gamma - j(\beta+1) & -\gamma & \gamma \\ \gamma & -\gamma & \gamma + j(\beta+1) & -\gamma - j\beta \\ -\gamma & \gamma & -\gamma - j\beta & \gamma + j(\beta-1) \end{bmatrix} \cdot \begin{bmatrix} V_A \\ V_B \\ V_C \\ V_D \end{bmatrix} \quad \textbf{(13)}$$

$$Y_{eff,A} = X_1^{-1}(\gamma - \gamma\cos(2\phi + 2\theta) - \gamma\cos(2\phi) + \gamma\cos(2\theta) - \beta\sin(2\phi)) \quad \textbf{(16)}$$
$$+ jX_1^{-1}(1 - \beta - \gamma\sin(2\phi + 2\theta) - \gamma\sin(2\phi) + \gamma\sin(2\theta) + \beta\cos(2\phi))$$

$$Y_{eff,B} = X_1^{-1}(\gamma - \gamma\cos(2\theta - 2\phi) - \gamma\cos(2\phi) + \gamma\cos(2\theta) + \beta\sin(2\phi)) \quad \textbf{(17)}$$
$$+ jX_1^{-1}(-1 - \beta - \gamma\sin(2\theta - 2\phi) + \gamma\sin(2\phi) + \gamma\sin(2\theta) + \beta\cos(2\phi))$$

$$Y_{eff,C} = X_1^{-1}(\gamma - \gamma\cos(2\theta - 2\phi) - \gamma\cos(2\phi) + \gamma\cos(2\theta) + \beta\sin(2\phi)) \quad \textbf{(18)}$$
$$- jX_1^{-1}(-1 - \beta - \gamma\sin(2\theta - 2\phi) + \gamma\sin(2\phi) + \gamma\sin(2\theta) + \beta\cos(2\phi))$$

$$Y_{eff,D} = X_1^{-1}(\gamma - \gamma\cos(2\phi + 2\theta) - \gamma\cos(2\phi) + \gamma\cos(2\theta) - \beta\sin(2\phi)) \quad \textbf{(19)}$$
$$- jX_1^{-1}(1 - \beta - \gamma\sin(2\phi + 2\theta) - \gamma\sin(2\phi) + \gamma\sin(2\theta) + \beta\cos(2\phi))$$

To characterize system behavior, we find the *effective* admittance seen by each source for the stipulated phase relationships **(15)**. The effective admittance at a combiner input port is the complex ratio of current to voltage at the port *with all sources active*. The effective admittances represent the admittances "seen" by the sources when they are operating under outphasing control. Combining **(13)** and **(15)** and manipulating them, expressions for the effective admittances at the four combiner input ports can be found as **(16)**, **(17)**, **(18)**, and **(19)**.

It is readily observed that the effective admittances seen by sources A and D are complex conjugates, as are those seen by sources B and C. Moreover, the expressions all have many individual terms in common.

We next propose an outphasing control strategy for realizing a desired output power while preserving desirable (nearly resistive) loading of the sources. Without loss of generality, we will consider synthesis of a zero-phase referenced output voltage at the load; we may adjust the load phase by common adjustments to all of the power amplifier phases. To synthesize a zero-phase load voltage of amplitude $V_{L,ref}$, or equivalently a "commanded" cycle-average power $P_{cmd} = (V_{L,ref})^2/(2R_L)$, we define an intermediate variable r_o:

$$r_o = \frac{2V_S^2}{P_{cmd}} \quad \textbf{(20)}$$

and pick our control angles θ and φ in terms of r_o as follows:

$$\theta = ATAN\left(\frac{2r_oX_2}{r_o^2 + X_1^2}\right) \quad \textbf{(21)}$$

$$\phi = ATAN\left(\frac{X_1}{r_o}\right) \quad \textbf{(22)}$$

It will be appreciated that other useful control selections of θ and φ are possible. Nevertheless, as will be seen, this control law provides monotonic output control and desirable loading of the individual power amplifiers over a wide operating range. (Again, note the relation of **(20)** – **(22)** to **(8)** – **(10)**).

B. System Attributes and Demonstration

Here we demonstrate the attributes of the proposed power combiner and outphasing system. As an example we consider a system having V_s = 1 V, R_L = 50 Ω and a design value k = 1.05 (resulting in X_2 = 48.78 Ω and X_1 = 35.60 Ω). Figure 9 shows plots of the control angles φ and θ versus "commanded" power, as per **(20)** – **(22)**, while Fig. 10 shows actual output power vs. commanded power. As can be seen, the actual power increases monotonically from zero with commanded power, and matches the commanded power well over the range shown. (At higher commanded power levels the actual power achieved saturates at approximately 0.31 W.) Because the output power is a smooth, monotonic function of command down to zero power, the nonlinearity can be readily addressed through predistortion or other means. This result demonstrates that the new outphasing scheme can smoothly control output power over a wide range down to zero power (at least when the PAs act as ideal sources).

Also of practical importance are the effective impedances seen by the individual power amplifiers across the control range. Figure 11 shows the real and imaginary components of the effective impedances at the four combiner input ports as a function of the commanded cycle-average output power P_{cmd} (as per **(16)** – **(19)**). Figure 12 shows the same information as magnitude and phase of the effective admittances. These plots illustrate key characteristics of the system (also, see captions for information about behavior outside of the plotted range). First, it can be seen that the input admittance at each port is highly conductive (phase close to zero) over a wide range of power commands, and that the susceptive component of the admittance is never large on an absolute scale. This represents a nearly-ideal

loading characteristic for many kinds of power amplifiers: the susceptive portions of the effective admittances loading the power amplifiers are small and the conductive components of the admittances are closely matched and scale up with desired power delivery. At very low commanded powers (below the range illustrated in Figs. 11 and 12), the admittances do increase and become susceptive (becoming entirely susceptive at zero commanded power). However, as the source currents and power drawn in this range are small, this nonideality will be tolerable in many applications. These results demonstrate that the proposed power combiner and outphasing system can meet the goal of providing wide-range power control at high efficiency while preserving desirable loading characteristics of the individual power amplifiers.

A key advantage of the new system is that the susceptive portion of admittance loading the power amplifiers is substantially smaller than with conventional Chireix combining, as illustrated in Fig. 13. One can achieve smaller susceptive loading over a specified power range with the proposed outphasing system than one can with a Chireix combiner. Likewise, for a specified allowable magnitude of susceptive loading one can operate over a greater power range with the proposed system than one can with a Chireix combiner.

C. Model Validation

To validate the above results, the system of Fig. 8 was simulated in LTSPICE with the proposed control law at a frequency of 10 MHz. The example V_s = 1 V, R_L = 50 Ω and X_2 = 48.78 Ω and X_1 = 35.60 Ω was used. Positive reactances were implemented with inductors (566.6 nH for X_1 and 776.4 nH for X_2), while negative reactances were implemented with capacitors (447 pF for X_1 and 326.27 pF for X_2). The effective admittances at the four power amplifier ports and the power were calculated numerically for a range of operating points. The simulation results were found to match the theory within the numerical precision of the simulation. As an example of this, Fig. 14 shows the analytical curves showing the effective admittance $Y_{eff,C}$ along with values computed numerically based on simulations. Simulation matched theory equally well for the other effective admittances.

D. Efficiency Impact

As with Chireix power combining, the influence of the proposed approach on power amplifier efficiency depends on the PA topology and operation. Nevertheless, it is clear that the ability to maintain highly conductive (resistive) loading of the PAs is generally desirable, as susceptive (reactive) loading corresponds to current which is conducted by the PA and induces loss but which does not contribute to RF power delivery. *Power Factor* k_p is a widely-used measure of how well the power delivery capability of a source (such as a power amplifier) is utilized [36]. This measure was adopted in the original paper by Chireix [1], and we exploit it for the same purpose here[2].

For power transfer at a single port, power factor is defined as [36]:

$$k_p = \frac{P}{S} = \frac{P}{V_{rms} I_{rms}} \tag{23}$$

where P is real (or average) power delivered at the port, and S is the "apparent" power associated with root-mean-square (rms) voltage and current at the port. For power transfer with sinusoidal voltage and current into an admittance Y_{eff} at a port, the expression for power factor can be simplified to:

$$k_p = \frac{\mathrm{Re}\{Y_{eff}\}}{|Y_{eff}|} = \cos(\angle Y_{eff}). \tag{24}$$

In a system having N ports through which power is transferred (such as the four PA input ports in the system of Fig. 8 or the two PA ports of a Chireix system), we can define a *net power factor* k_p having the same interpretation in terms of loss and source utilization:

$$k_{p,net} = \frac{\sum_{j=1}^{N} P_j}{\sum_{j=1}^{N} S_j} = \frac{\sum_{j=1}^{N} P_j}{\sum_{j=1}^{N} V_{rms,j} I_{rms,j}} \tag{25}$$

For power transfer with sinusoidal waveforms, identical voltage amplitudes at the N ports, and effective admittances loading the individual ports, this simplifies to:

$$k_{p,net} = \frac{\sum_{j=1}^{N} \mathrm{Re}\{Y_{eff,j}\}}{\sum_{j=1}^{N} |Y_{eff,j}|} \tag{26}$$

where $Y_{eff,j}$ is the effective admittance loading the j^{th} port.

Figure 15 plots the net power factor vs. output power for four Chireix systems (including designs from Fig. 3) and for two systems of the type proposed here (designed with different values k, and including the design of Figs. 10-12.) Note that the power axis is plotted in dB to capture the behavior over a wide power range. It can be seen that the new architecture yields much better power factor than is achievable with a Chireix combiner. With the proposed architecture, one can realize smaller deviation from unity power factor for a given power range, or a wider power range for an allowable minimum power factor. This arises directly from the ability of the proposed architecture to provide more nearly resistive loading of the PAs across power, as illustrated in Fig. 13.

To underscore the impact of the new architecture on efficiency, we consider behavior with ideal saturated Class B power amplifiers. While Class B amplifiers are not switched-mode in nature, high peak efficiencies (approaching ideal performance) have been reported even at microwave frequencies [23, 37], and the impact of loading on PA efficiency is readily determined for Class B operation. Starting from the analytical formulation in [16], it is easily shown that the efficiency of an ideal saturated class B amplifier is

[2] Power factor is calculated in equation 18 and plotted in Figs. 4 & 5 of [1]. Owing to the symbol selected by Chireix, this calculation has sometimes been confused with efficiency. While it is related to efficiency, power factor should instead be recognized as a measure of how well ohmic loss is minimized in power delivery, with k_p = 1 being the best that can be achieved.

$$\eta = \frac{\pi}{4} \cdot k_p = \frac{\pi}{4} \cdot \frac{\mathrm{Re}\{Y_{eff}\}}{|Y_{eff}|} \quad \textbf{(27)}$$

where k_p is the load power factor, and Y_{eff} is the load impedance presented to the PA. Extending this to a system of outphased class B PAs with either a Chireix combiner or the new combiner, one finds a system efficiency of:

$$\eta = \frac{\pi}{4} \cdot k_{p,net} . \quad \textbf{(28)}$$

Thus, for ideal saturated Class B PAs, efficiency is proportional to net power factor, with a scaling coefficient of $\pi/4 \approx 0.785$. The curves of Fig. 15 therefore directly illustrate how efficiency varies with output power in the case of ideal saturated Class B amplifiers[3]. The improvement of the proposed architecture in terms of loading and power factor directly translates into an efficiency benefit.

To illustrate the *average* efficiency benefit of the proposed combining and outphasing approach, we consider the (normalized) output power probability density function shown in Fig. 16(top) for a representative WLAN signal. This signal has a peak-to-average power ratio (PAPR) of 9.01 dB. Fig. 16(bottom) shows the average efficiencies that would be realized for this power distribution with ideal Class B PAs and the different combiners of Fig. 15. Of the Chireix combiners, the combiner having a peak in power factor near -13 dB yields the best average efficiency (50.1%), while the better of the two "new architecture" combiners provides a much higher efficiency (69%) – an almost 19% improvement in efficiency. It may be concluded that – at least for some cases of interest – substantial efficiency improvements can be realized with the architecture proposed here.

E. Power Combiner Efficiency

In computing efficiency, the previous section focused on losses incurred in the power amplifiers, while assuming that the combiner itself is truly lossless. A concern with any power combining system is the efficiency of the combiner itself. While ideally lossless, the parasitic resistances of actual passive components in the combiner of Fig. 8 may contribute a degree of loss which cannot be neglected in some cases. (The same is true of a Chireix combiner.) Here we consider the impact of losses on power combiner efficiency. We treat only losses owing to the power combiner, and do not consider any combining-related losses that may accrue in the power amplifiers themselves (e.g., owing to variations in effective impedance at the power combiner input ports, as treated in the previous section).

To model non-idealities of the passive components in the combiner of Fig. 8, we assume that each branch in the combiner network has a series resistance such that every branch has the same quality factor $Q = |X|/R_s$. To estimate the losses and efficiency degradation owing to these parasitic resistances, we adopt a method that has been previously employed in matching networks [28,29]: the circuit currents are calculated assuming no loss (i.e., assuming the resistances are zero); the losses and circuit efficiency are then calculated based on the losses induced by the calculated currents flowing through the parasitic resistances. This method thus assumes that the branch currents are not significantly affected by the presence of small resistances [28,29].

Using the above method, in can be shown that the loss in the combiner can be calculated as:

$$P_{loss,av} = \frac{1}{2Q} \vec{V}^H \left[Y^H W Y \right] \vec{V} \quad \textbf{(29)}$$

where V and Y are defined as in **(13)** and **(14)**, ^{H} is the Hermetian operator (conjugate transpose) and W is defined in **(29A)**, shown below.

The fractional loss fl = (1-efficiency) of the combiner can be similarly calculated as:

$$fl = 1 - \eta = \frac{1}{Q} \cdot \frac{\vec{V}^H \left[Y^H W Y \right] \vec{V}}{\vec{V}^H Y \vec{V}} \quad \textbf{(30)}$$

The fractional loss is thus inversely proportional to the quality factor of the branch impedances in the combiner network, and depends on the operating point.

To validate the above formulation and to illustrate the efficiency potential of the proposed power combining system, the fractional loss of an example system was calculated using the result **(30)** and compared to numerical results from LTSPICE. The example V_s = 1 V, R_L = 50 Ω, f = 10 MHz, X_2 = 48.78 Ω and X_1 = 35.60 Ω is again used. Positive reactances were implemented with inductors (566.6 nH for X_1 and 776.4 nH for X_2), while negative reactances were implemented with capacitors (447 pF for X_1 and 326.27 pF for X_2)), and parasitic resistances added for Q = *100* of each branch element. Both analytical and simulation results are shown in Fig. 17. As can be seen, the simulation results confirm the analytical formulation. The small mismatch between the theoretical curve and the simulated results can be attributed to the assumption made in the analysis that the small resistive losses do not affect the current waveforms. Moreover, it can be seen that the loss owing to power combining is small over a wide operating range (<5% over the plotted range for Q = *100*). As fractional loss (or percentage loss) is inversely proportional to branch quality factor, we can see that combining loss is expected to be manageable even at relatively low quality factors, and can be made quite low if high-quality-factor components are used.

F. Example System Simulation and Comparison

To better illustrate the value of the proposed architecture and its use with switched-mode power amplifiers, simulation of a complete power amplifier system is presented here, along with comparison to a Chireix-based outphasing system. Among the important potential applications of the proposed approach are high-efficiency, high-power HF and VHF amplifiers for industrial, scientific, and medical applications. Applications such as medical imaging (MRI), industrial processing and heating rely on multi-kW amplifiers at frequencies in the range of 13.56 – 128 MHz. Here we consider the performance of 3 kW, 27.12 MHz power amplifier systems based on

[3] An approximately proportional relation between power factor and efficiency would also be expected for class C operation in many cases [16].

$$W = \begin{bmatrix} |X_1|+|X_2| & |X_2| & 0 & 0 \\ |X_2| & |X_1|+|X_2| & 0 & 0 \\ 0 & 0 & |X_1|+|X_2| & |X_2| \\ 0 & 0 & |X_2| & |X_1|+|X_2| \end{bmatrix} \quad \textbf{(29A)}$$

750 W E/F_{odd} switched-mode rf power amplifiers. Time-domain simulations are carried out in LTSPICE using the models described below.

Figure 18 shows the structure of the E/F_{odd} [11] power amplifier used in the simulations; this topology is a variant of the "current-mode class D" amplifier [12]. The power amplifier operates from an input voltage V_{in} = 125 V, leading to peak device voltages of approximately 400 V. The device model used roughly approximates the characteristics of ARF521 RF Power MOSFETs (and ARF475FL push-pull pairs). The switch model includes $R_{ds\text{-}on}$ = 0.1 Ω (on-state resistance), C_{oss} = 80 pF (output capacitance) and R_{oss} = 0.3 Ω (output capacitance series resistance). The choke inductors are 10 μH with 0.3 Ω ESR. The tank capacitor C_T = 96.1 pF, while the resonant inductor is realized as the primary-referred magnetizing inductance of the transformer L_T = 195.6 nH. The transformer also has primary and secondary winding resistances such that the magnetizing inductance has a quality factor Q_T = 150 as seen from either winding.

For simulation of the new architecture, a transformer turns ratio of N_p:N_s = 3.16:1 is used. The combiner of Fig. 8 is used, with a load resistance of 50 Ω and reactance values X_1 = 35.6 Ω and X_2 = 48.78 Ω (as in the design illustrated in Fig. 13). Positive reactances are implemented with inductors (208.95 nH for X_1 and 286.3 nH for X_2), while negative reactances are implemented with capacitors (164.9 pF for X_1 and 120.3 pF for X_2). Each branch of the combiner includes parasitic series resistance for branch quality factors of Q = 150. Based on the author's experience with designs at similar power levels and frequencies [15,38], it is expected that the networks and component quality factors described above can be practically realized.

For simulation of conventional Chireix outphasing, 1500 W PAs are formed by operating pairs of the inverters described above synchronously (with the same timing) and combining their outputs using an interphase transformer, as illustrated in Figure 19. (The interphase transformers suppress any circulating currents between the PAs owing to instantaneous voltage differences.) The interphase transformers are considered as ideal, except for having 0.47 Ω winding resistances, which yield a 0.1 dB insertion loss (2.3% loss). The two pairs of PAs are outphased using a Chireix combiner having X_c = 13.6 Ω and supply a load resistance R_L = 13 Ω (corresponding to one of the Chireix designs of Fig. 13). To achieve the correct matching, the PAs have transformer turns ratios of N_p:N_s = 3.16:1.41.

Several conclusions may be drawn based on the simulations of the two systems. First, while the two systems perform similarly near full power, the proposed architecture provides much higher efficiencies at reduced power levels. Figure 20 shows the drain efficiency vs. output power for both the new system and the Chireix system. It is readily apparent that the proposed architecture is superior at low power levels (e.g., >12% higher efficiency at 300 W output (-10 dB re full power), increasing to >20% higher efficiency at -12.5 dB). The difference in efficiency arises both due to the higher reactive currents in the Chiriex architecture (lower power factor) as described earlier, and because the greater reactive loading on the Chireix PAs at low power levels causes them to lose zero-voltage switching, resulting in substantial capacitive discharge loss.

Figure 21 shows the device drain-to-source voltages at 300 W output power (-10 dB re full power) for both the Chireix and proposed systems. (Only one device voltage in each PA is shown; the other is identical, but shifted by a half cycle. Likewise, voltages for only two of the Chireix PAs are shown, as the other two PAs have identical waveforms.) It can be seen that zero-voltage switching (ZVS) has been lost at turn on for half of the devices in the Chireix system at this output power. (Moreover, the switch body diodes are forced to conduct in the other half of the devices.) By contrast, desired operation with zero-voltage switching is well maintained in the proposed system owing to the reduced reactive loading. In addition to the efficiency implications, loss of ZVS can often lead to EMI and gate drive challenges in practice (e.g., see [22,30]). The proposed architecture is advantageous in that it maintains desirable switching conditions down to far lower power levels than is possible in a Chireix system.

A further conclusion that can be drawn from the simulations is that the new architecture can operate over a much wider power range than the Chireix system with the selected switching PA. While an outphasing system driven from ideal sources can modulate power down to zero, E/F_{odd} switching amplifiers do not behave as ideal sources, especially under reactive loading [18]. In particular, the PA output voltage amplitudes are different for inductive vs. capacitive loading, such that the PA output waveforms differ (see the mismatch in drain voltage waveforms for the Chireix system in Fig. 21, for example). This in turn causes outphasing cancellation to become imperfect, leading to a minimum deliverable output power. Indeed, the plots of Fig. 20 show the efficiency vs. output power over the complete outphasing range for each system. The Chireix system in this example has a minimum output power of 161 W, corresponding to a ~19:1 or 12.7 dB achievable power range. By contrast, the proposed architecture has a minimum output power of 26.4 W, corresponding to a ~113:1 or 20.6 dB power range. Because the proposed architecture provides more resistive loading over a broader power range than with Chireix combining, it better matches the desired loading characteristics of the power amplifiers, leading to higher performance. While this aspect is highly dependent on the power amplifier topology and

characteristics [18], it may be expected that the more highly resistive loading achievable with the proposed architecture will be a substantial advantage in many other implementations as well.

Finally, it is observed from the simulations that the proposed system behaves as predicted based on idealized models of the power amplifiers, except for operation at extreme low powers (as described above.) It can be concluded that the proposed approach is suitable for use with E/F_{odd} switching power amplifiers, and it may be expected to be effective with many other kinds of power amplifiers as well, even considering that they do not act as ideal sources.

IV. DESIGN OPPORTUNITIES

It will be appreciated that a wide variety of high-performance power combining and outphasing systems can be synthesized through the approach described in the previous sections. This includes designs based on multi-stage cascades of various types of compression network structures (such as those in [30,31]). For example, a three-level structure designed similarly (using 8 sources) would yield even wider-range power control for a given susceptive loading of the sources. Likewise, using the topological dual of the RCN in Fig. 4 in a multi-stage design would likewise be effective as the basis for a combiner. Moreover, one could combine different types of base RCN circuits to construct effective combiners. (Note that for some types, all of the sources and/or loads may not be referenced to common potentials, so one may elect to use transformers or baluns to provide coupling.) Finally, use of transformations such as topological and / or time-reversal duality transformations will yield other versions of the proposed system.

Numerous other circuit opportunities also present themselves. The reactances in Fig. 8 are specified only at a single frequency, and one may choose to implement them with single inductors or capacitors as appropriate. However, one may also use higher-order reactive networks. These may be selected to block or conduct dc and/or higher-order harmonics, or to present desired impedances (e.g., for combining and outphasing) at additional frequencies. Likewise, while the development has been described in terms of lumped parameter elements, it will be appreciated that distributed elements (e.g., based on transmission-line networks) can also be used.

There is also flexibility of design within a combiner structure and control law. For instance, the main design example in section III utilized a value of design parameter k of 1.05. Different values of k may be selected based on system design goals and requirements, such as the desired operating range and load sensitivities of the power amplifiers. For example, Figure 22 shows the influence of design parameter k on the effective admittance $Y_{eff,A}$ in a system with the combiner of Fig. 8 and control laws **(20)** – **(22)**. It can be seen that higher values of k provide a higher upper bound in achievable power delivery, but also result in greater phase variations over the operating range.

In realizing an outphasing power amplifier, one must both compute phase angles for a desired output level (e.g., according to **(20) – (22)**) and generate rf drive signals for the power amplifiers having the desired phase (e.g., using one or more phase modulators to adjust the phase of a reference rf signal appropriately). Conventional methods can be directly applied in realizing these functions. However, another method can also be used to directly realize phase angle computation and phase modulation in the proposed power amplifier system. Consider the case of the power amplifier system of Fig. 8 and the related RCN system of Fig. 5. For the system of Fig. 5, the phases of the voltages V_A-V_D have phase relationships as specified in Fig. 7 and **(8)** to **(10)**, which are identical to the control law specified in **(20) – (22)**, if the load resistances are replaced by r_o in **(20)**. Thus, if one were to construct an RCN as in Fig. 5 which was driven by an rf signal having a desired output phase, and load it with resistors controlled as per **(20)**, the voltages across the load resistors would provide signals with the desired phases for driving the power amplifiers. One could realize the controlled resistors with voltage-controlled resistors (e.g., using MOSFETs) or through switched-resistor networks, for example, and adjust the resistances via a control system. One would thereby directly realize both phase angle computation and phase modulation in one step. It should be recognized that one could implement the actual RCN network, use equivalent components (e.g., using simulated inductors), or build an analog or digital circuit having the same response characteristics as the RCN. Using this technique, one can thus directly realize both control computations and phase modulation.

V. CONCLUSION

This paper describes a new power combining and outphasing system that provides greatly improved performance characteristics. Whereas conventional outphasing systems utilize two power amplifiers, the system introduced here combines power from four or more amplifiers. The proposed technique overcomes the loss and reactive loading problems of previous outphasing systems. It provides ideally lossless power combining, along with resistive loading of the individual power amplifiers over a very wide output power range, enabling high average efficiency to be achieved even for large peak-to-average power ratios.

Section II of this document presents a conceptual development that illustrates the operating principles of the system. The relation of the proposed technique to multi-level resistance compression is also described. Section III presents a key embodiment of this new approach, along with detailed analysis and supporting simulations. Section IV describes additional design possibilities with the proposed system, and also illustrates how circuit control and phase modulation can be realized. It is anticipated that the new power combining and outphasing modulation system will find widespread use in applications where both high linearity and high efficiency are desired.

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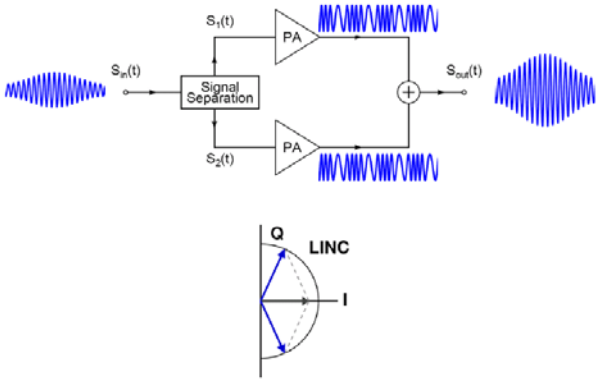

Fig. 1 The conventional outphasing architecture, also known as the LINC architecture. A variable envelope output is created as the sum of two constant-envelope signals by outphasing of the two constant envelope signals.

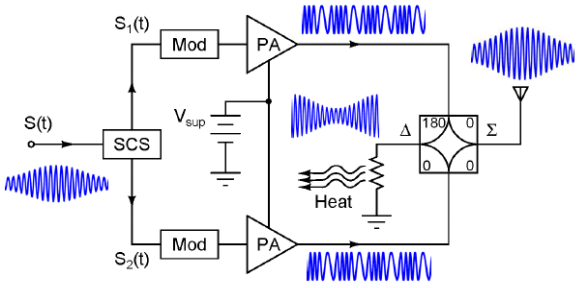

Fig. 2 The conventional outphasing architecture implemented with an isolating combiner. A portion of the total constant output power from the PAs is delivered to the output (at the sum port of the combiner); the remainder is delivered to the difference port and is lost as heat in the isolation resistor. In some implementations, power not delivered to the output is instead recovered back to the dc supply via a rectifier.

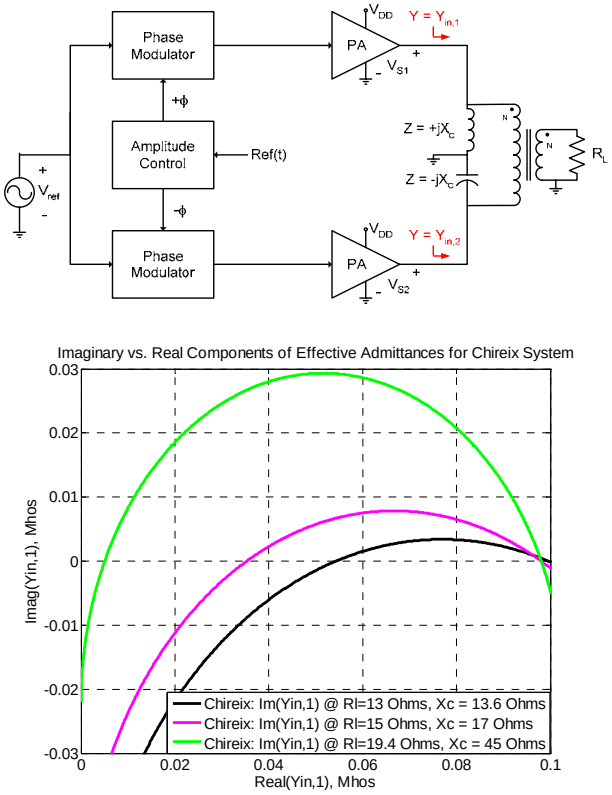

Fig. 3 (top): The conventional outphasing architecture implemented with one version of a Chireix combiner. The Chireix combiner is lossless but nonisolating. The impedances $+jX_C$, $-jX_C$ are to compensate for the effective reactive loading on the PAs due to interactions between them. Because the effective reactive loading due to PA interactions depends on operating point (outphasing angle), compensation is imperfect over most of the operating range. This can lead to loss of efficiency and PA degradation when operating over wide ranges. (bottom): Imaginary vs. Real components of the effective admittance $Y_{in,1}$ seen by PA 1 across the outphasing range for three design cases (of R_L, X_C). $Y_{in,2}$ is the complex conjugate of $Y_{in,1}$. Significant deviation from resistive loading is observed. Similar deviations are found for other Chireix designs.

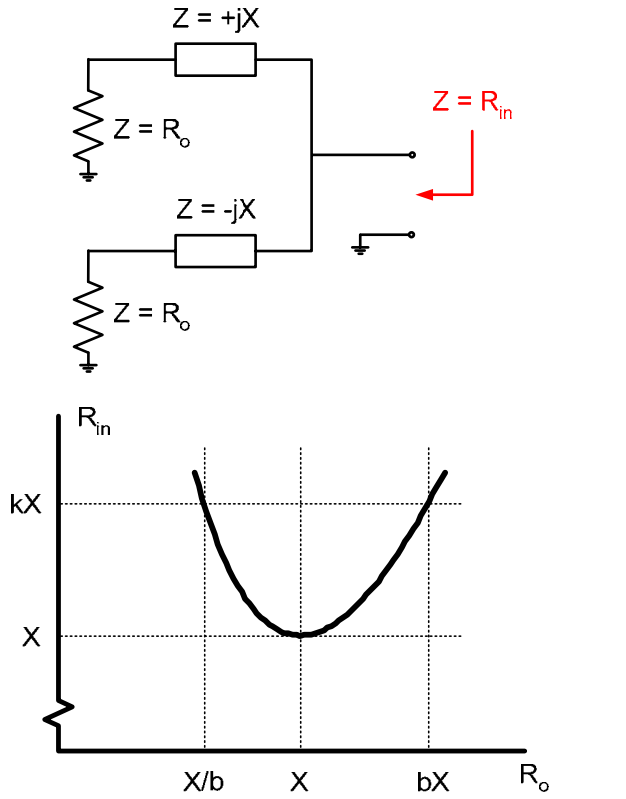

Fig. 4 (top) A basic resistance compression network (RCN) and (bottom) its resistive input impedance R_{in} as a function of the matched load resistance value R_o. As the resistances R_o vary together over a range geometrically-centered on X, the input impedance is resistive and varies over a much smaller range than R_o. RCN networks have application to resonant dc-dc converters and rectifiers [30,31] and to energy recovery in power amplifiers [22] among other uses.

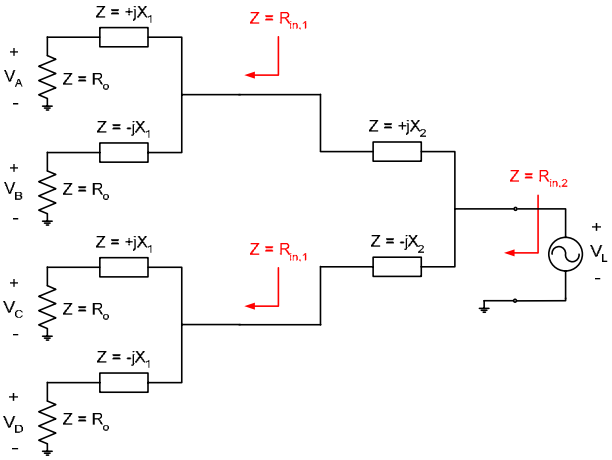

Fig. 5 A multi-stage resistance compression network based on a cascade of the single-stage RCN network in Fig. 4. A source V_L driving the network is also shown. The input resistance $R_{in,2}$ varies much less than the matched load resistances R_o.

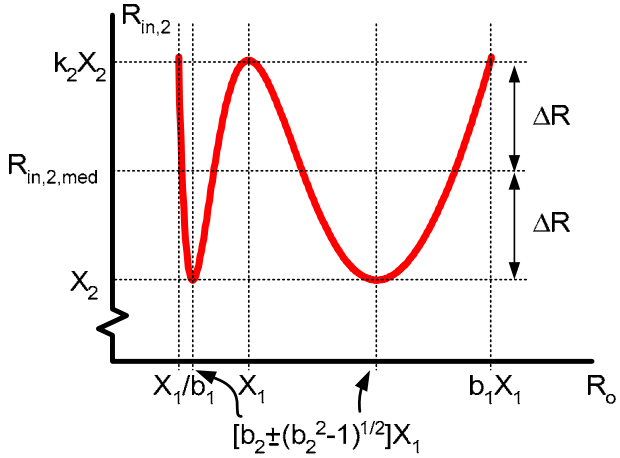

Fig. 6 Resistive input impedance $R_{in,2}$ as a function of the matched load resistance value R_o for the two-stage compression network of Fig. 5. Selection of the compression network reactances as described provides this characteristic, which compresses resistance to a greater extent than is possible in a single-stage compression network design. For example, one can achieve resistance compression of the input resistance to within ±2.5% of the desired median value over a 12:1 ratio in load resistance values R_o with this technique.

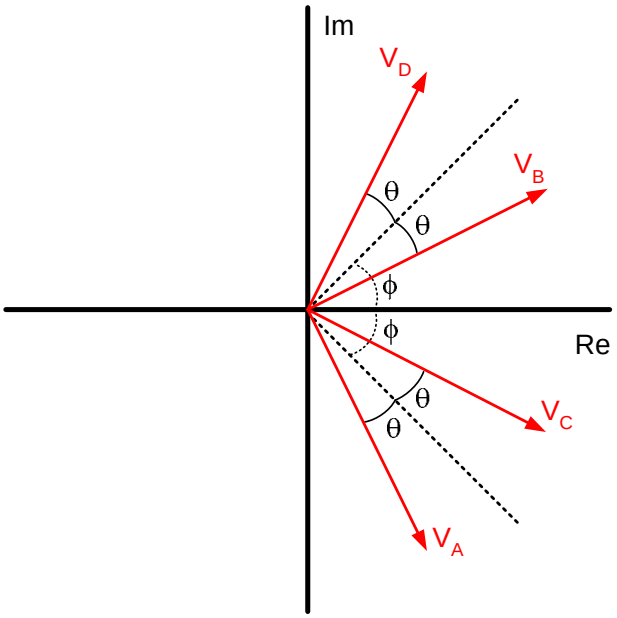

Fig. 7 Phasor diagram showing the relationship among the phase voltages. The outphasing control angles φ and θ are used to regulate output power while maintaining desirable loading of the sources.

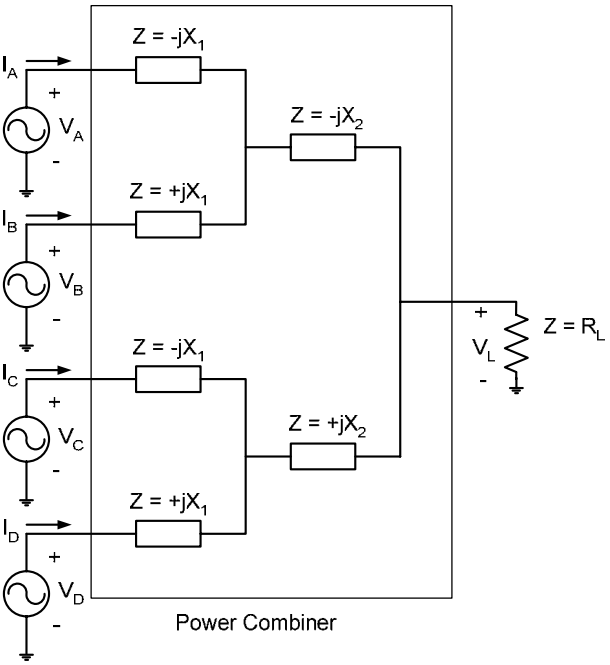

Fig. 8 An example implementation of the proposed outphasing architecture. This implementation employs four power amplifiers (as compared to two in conventional outphasing); the power amplifiers are illustrated as ideal voltage sources in this figure for analysis purposes. The power combiner is ideally lossless, and comprises reactive elements with specified impedances at the operating frequency. The combiner has five ports: four for the power amplifier inputs and one for the load.

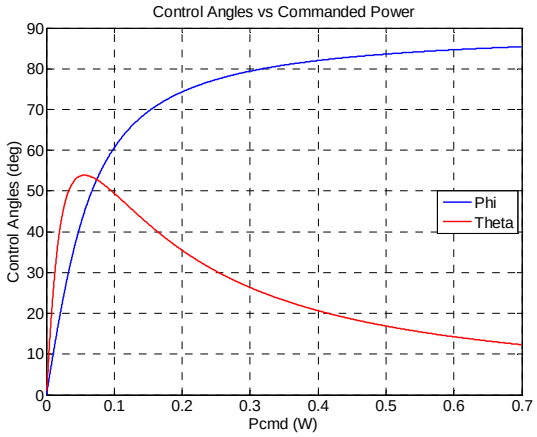

Fig. 9 Plot showing the outphasing control angles vs. commanded output power according to **(20)** to **(22)** for the example system (V_s = 1 V, R_L = 50 Ω, X_2 = 48.78 Ω and X_1 = 35.60 Ω).

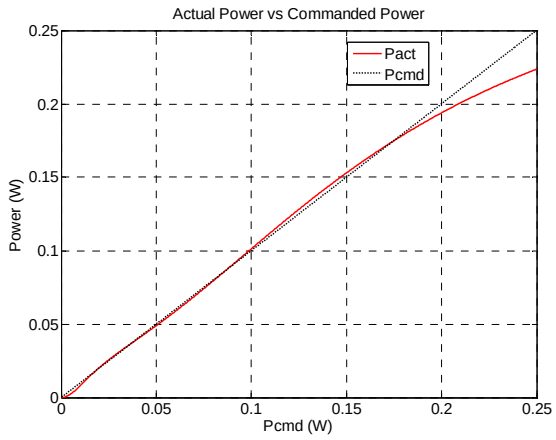

Fig. 10 Actual output power vs. commanded power for the example system (V_s = 1 V, R_L = 50 Ω, X_2 = 48.78 Ω and X_1 = 35.60 Ω). The actual power increases monotonically from zero with commanded power, and matches the commanded power well over the range shown. At higher commanded power levels the actual power achieved saturates at approximately 0.31 W.

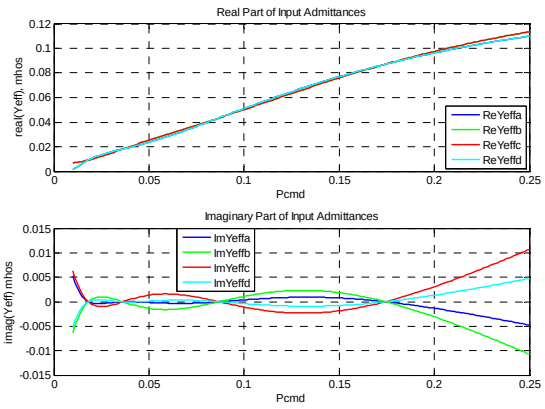

Fig. 11 Real and imaginary components of the effective admittances at the four power combiner input ports plotted as a function of the power command P_{cmd}. The plots are shown for the example R_L = 50 Ω, X_2 = 48.78 Ω and X_1 = 35.60 Ω over a commanded power range of [0.01,0.25] W. It can be seen that the imaginary components are small compared to the real components over a wide range (i.e., highly conductive input admittances). Below the range shown, as commanded power goes to zero, the real parts of the admittances go to zero, while the imaginary parts go to +/- 0.028 Mhos. (The real parts of $Y_{eff,A}$ and $Y_{eff,D}$ briefly go negative for P_{cmd} < ~0.00875 W, with a minimum negative real component of ~-0.0026 Mhos. This indicates power transfer from sources B and C to A and D over this range.) As P_{cmd} is increased above the range shown, real components of the admittances saturate at values in the range 0.15 – 0.16 Mhos, with imaginary parts saturating to values in the range of [-0.075, 0.075] Mhos.

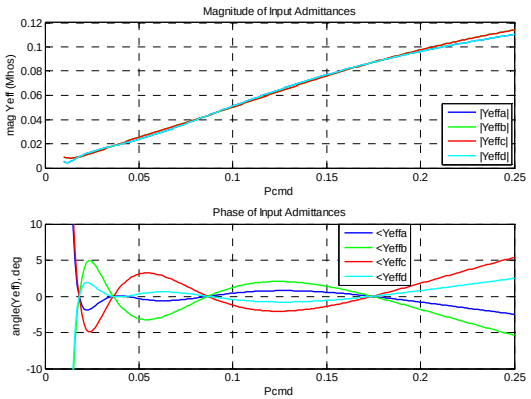

Fig. 12 Magnitude and phase of the effective admittances at the four power combiner input ports, plotted as a function of the power command P_{cmd}. Plots are shown for the example R_L = 50 Ω, X_2 = 48.78 Ω and X_1 = 35.60 Ω over the commanded power range of [0.01,0.25] W. It can be seen that the input admittance is highly conductive (phase close to zero) over a wide range As commanded power goes to zero below the range shown, the admittance magnitudes increase to a maximum of ~0.28 Mhos, and the phases go to +/- 90°. As commanded power increases above the range shown, input admittance magnitudes saturate to values below ~0.18 Mhos, with phases in the range of [-25°, 25°].

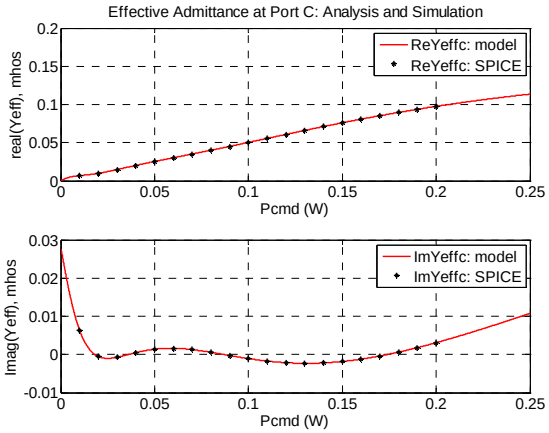

Fig. 14 Real and imaginary components of the effective admittance $Y_{eff,c}$ for the example V_s = 1 V, R_L = 50 Ω, f = 10 MHz, X_2 = 48.78 Ω and X_1 = 35.60 Ω. Both analytical results and numerical results computed from LTSPICE *.ac* simulations are shown. For simulation, positive reactances were implemented with inductors (566.6 nH for X_1 and 776.4 nH for X_2), while negative reactances were implemented with capacitors (447 pF for X_1 and 326.27 pF for X_2). The simulation results confirm the analytical formulation.

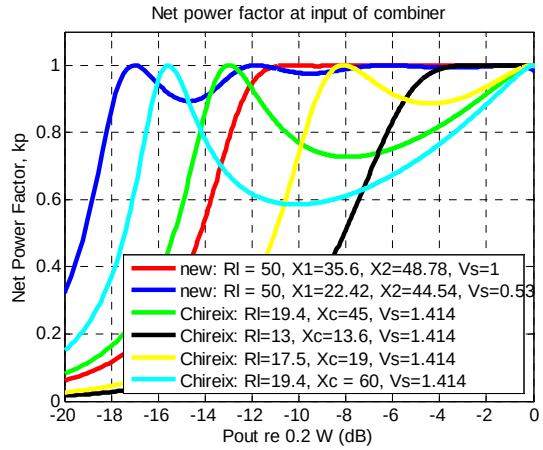

Fig. 15 Net power factor as a function of normalized output power for four Chireix systems and for two systems of the proposed architecture. It can be seen that the proposed power combining and outphasing system provides nearly ideal power factor across a wide power range.

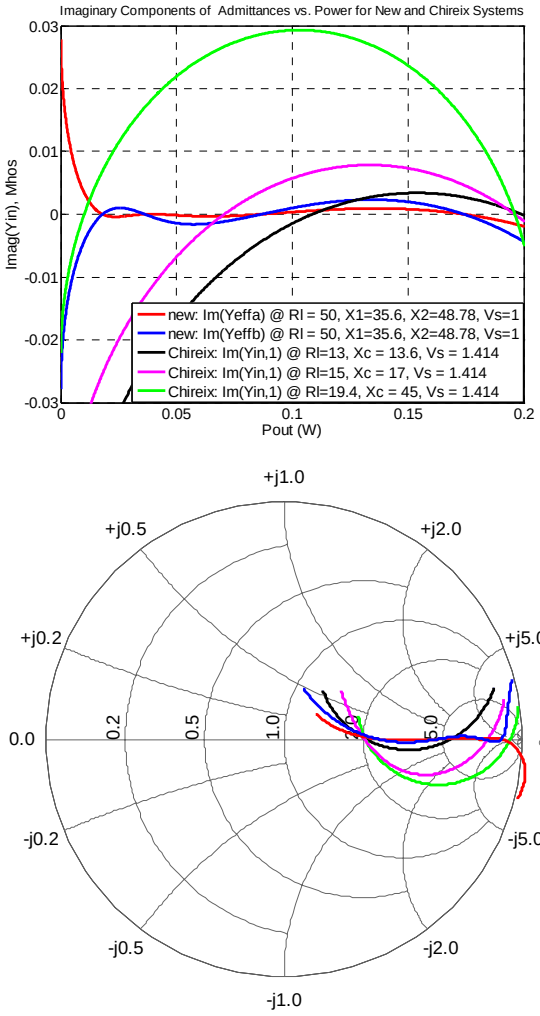

Fig. 13 (top): This figure compares the imaginary components of admittances of the new power combiner and outphasing system of Fig. 8 to that of the Chireix system of Fig. 3 as a function of total output power. Three example designs of the Chireix system are shown. The Chereix systems are shown for a factor of sqrt(2) higher input voltage to account for the fact that a Chireix system only has two PAs. With this normalization, the same total power is achieved in the two systems with each PA seeing similar real components of admittance. It can be seen that the new power combining and outphasing system yields much smaller reactive loading than the Chireix combiner over a wide power range. (For reference, the real part of the admittances for P_{out} = 0.2 W are each approximately 0.1 Mho.) (bottom): This figure shows the loci of reflection coefficients associated with these effective admittances on a Smith chart. The loci for the new combiner (red and blue traces) are much closer to ideal than those of the Chereix combiners.

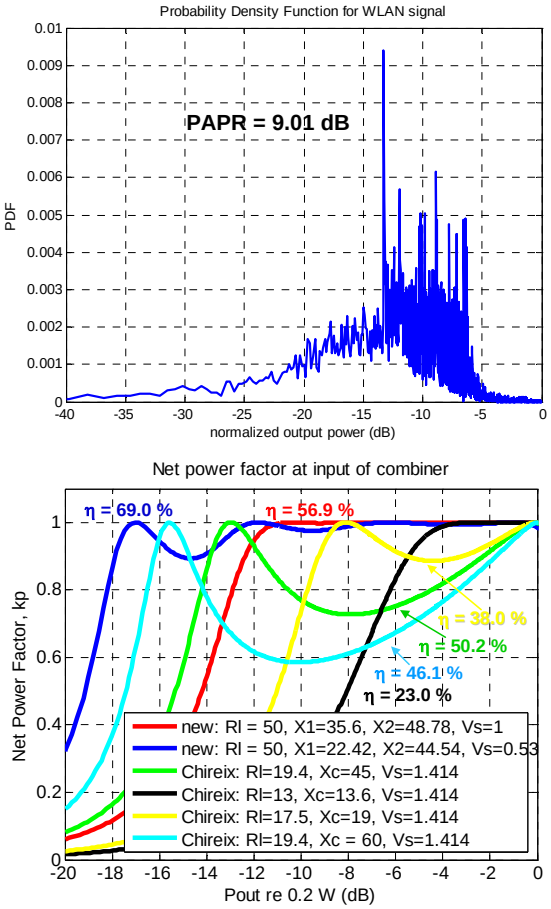

Fig. 16 (top): Normalized output power probability density function for a representative WLAN signal having a 9.01 dB PAPR. (bottom): Net power factor vs. normalized output power for four Chireix systems and two systems of the proposed architecture. For ideal saturated class B amplifiers, efficiency is 0.785 times the net power factor. The average efficiency of each system with ideal saturated class B amplifiers for the WLAN signal is also indicated. The Chireix systems provide 23.0%, 38.0%, 50.1% and 46.1% average efficiency, respectively. The two systems of the proposed architecture provide 56.9% and 69.0% average efficiency, respectively.

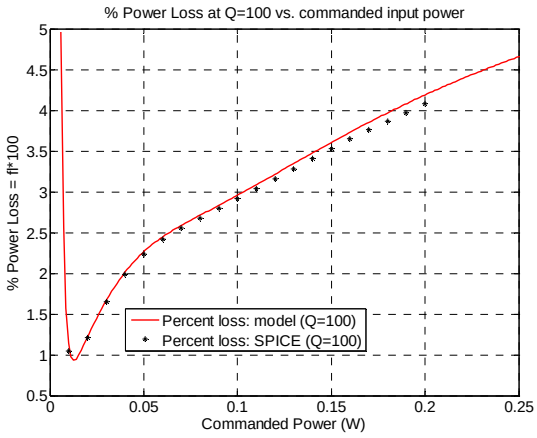

Fig. 17 Percentage power loss in the combiner ($100 \cdot fl$) for the example V_s = 1 V, R_L = 50 Ω, f = 10 MHz, X_2 = 48.78 Ω and X_1 = 35.60 Ω for component quality factors Q = 100. Both analytical results and numerical results computed from LTSPICE *.ac* simulations are shown. For simulation, positive reactive impedances were implemented with inductors with series resistors (566.6 nH, 0.356 Ω for X_1 and 776.4 nH, 0.488 Ω for X_2), while negative reactive impedances were implemented with capacitors with series resistors (447 pF, 0.356 Ω for X_1 and 326.27 pF, 0.488 Ω for X_2). The simulation results confirm the analytical formulation.

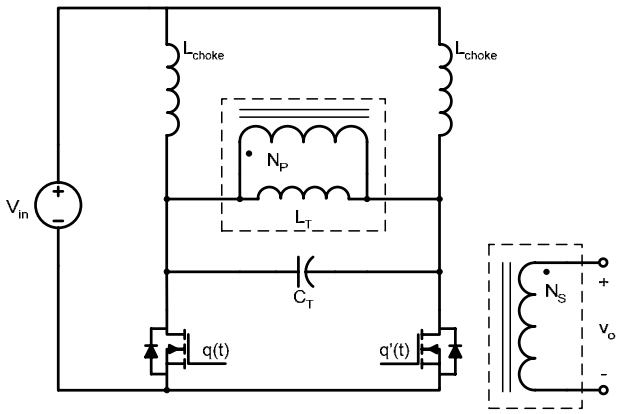

Fig. 18 This figure shows the E/F_{odd} power amplifier used in the example system simulations. The power amplifier is designed to operate at 27.12 MHz at an input voltage of 125 V and at output powers up to 750 W. The tank capacitor C_T = 96.1 pF is selected in conjunction with the 80 pF device capacitance to be at resonance with the primary-referred magnetizing inductance of the transformer L_T = 195.6 nH.

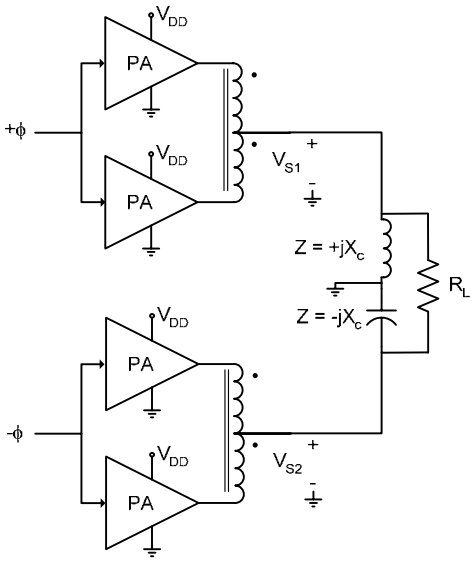

Fig. 19 Implementation of the Chireix outphasing system. Each of the two outphased sources is constructed of from a pair of power amplifiers (of the type in Fig. 18) operated synchronously, with their outputs combined through interphase transformers. The Chireix combiner has X_c = 13.6 Ω and the load resistance R_L = 13 Ω (corresponding to one of the Chireix designs of Fig. 13).

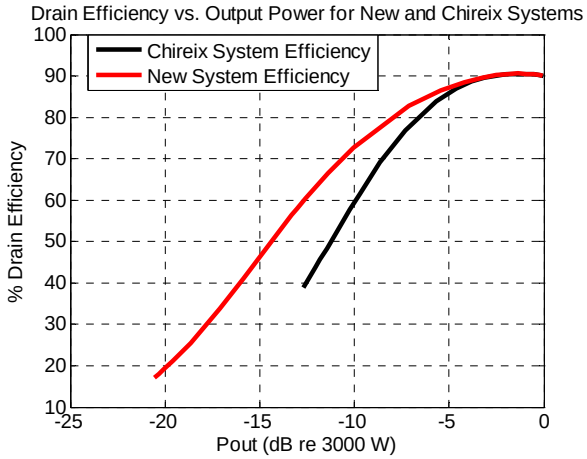

Fig. 20 Drain efficiency vs. output power for the both the new outphasing system and the Chireix system. Efficiency is plotted over the entire outphasing range, such that this plot also indicates the output power operating ranges of the power amplifier systems.

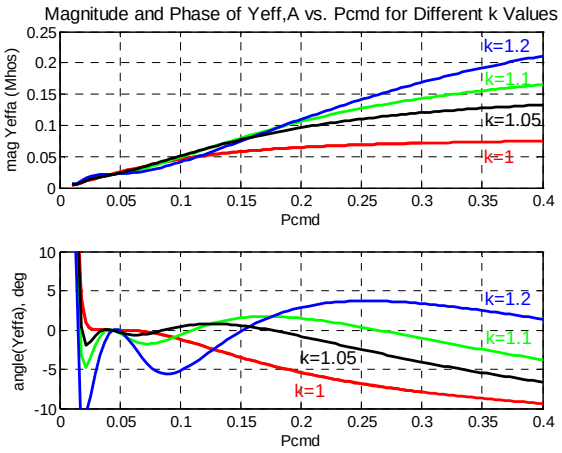

Fig. 22 This figure shows plots of the effective admittance $Y_{eff,A}$ in the combiner of Fig. 8 and control laws **(20)** – **(22)** for different values of design parameter *k*. It can be seen that higher values of *k* provide a higher upper bound in achievable power delivery, but also result in greater phase variations over the operating range.

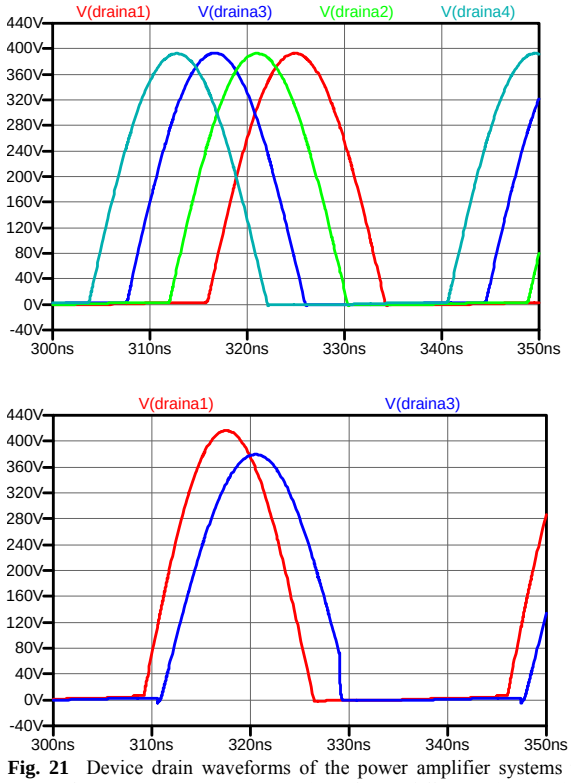

Fig. 21 Device drain waveforms of the power amplifier systems when operated at 300 W output power (-10 dB re full power): (top) new outphasing system; (bottom) Chireix system. Only one device voltage in each PA is shown; the other is identical, but shifted by a half cycle. Likewise voltages for only two of the Chireix PAs are shown, as the other two PAs have identical waveforms. It can be seen that the new outphasing system provides the desired voltage waveforms for the PA, while the Chireix system has lost zero-voltage turn-on for some devices (as indicated by waveform truncation near 330 ns).