# Ge Photodetectors for Si Microphotonics

Hsin-Chiao Luan

B. S. in Ceramic Engineering, Magna Cum Laude
University of Washington, 1995

Submitted to the Department of Materials Science & Engineering
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

February, 2001

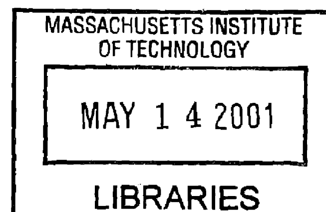
© Massachusetts Institute of Technology, 2001. All Rights Reserved.

Author ..................................................................
Department of Materials Science & Engineering
January 12, 2001

Certified by ..................................................................
Lionel Cooper Kimerling
Thomas Lord Professor of Materials Science & Engineering
Thesis Supervisor

Accepted by ..................................................................
Carl V. Thompson
Stavros Salapatas Professor of Materials Science & Engineering
Chair, Department Committee on Graduate Students
Department of Materials Science & Engineering

Science



# Ge Photodetectors for Si Microphotonics

by

Hsin-Chiao Luan

Submitted to the Department of Materials Science & Engineering
on January 12, 2001, in partial fulfillment of the requirements for
the degree of Doctor of Philosophy

## ABSTRACT

This thesis demonstrates the integration of pure Ge near-infrared photodetectors on Si. Ge epilayers were grown directly on Si by a two-step ultra-high-vacuum/chemical-vapor-deposition (UHV/CVD) process. This work conclusively proves that threading-dislocation densities in the Ge epilayers, measured both by plan-view transmission electron microscopy and etch-pit-density (EPD) counting, were reduced by cyclic thermal annealing. Additionally, Ge mesas with no threading dislocations as measured by EPD were also demonstrated. The removal of threading-dislocations can be attributed to the thermal stress induced dislocation glide and reactions. Using the annealed Ge epilayers grown on Si, p-i-n Ge photodetectors with maximum responsivities of 770 mA/W at 1.3 μm were fabricated. Finally, to allow the integration of Ge epilayers in Si microelectronic processing, the protection and passivation of Ge was investigated. The passivation was provided by the oxidation of Si epilayers grown on Ge. Capacitance-voltage characteristics of metal-oxide-semiconductor devices demonstrated the high quality of the passivation with the measured interface state density of $4 \times 10^{11}$ $cm^{-2}eV^{-1}$.

Thesis Supervisor: Lionel Cooper Kimerling
Title: Thomas Lord Professor of Materials Science & Engineering

# Acknowledgements

I would like to thank Professor Kimerling for his encouragement, guidance and inspiration. Kim is a wonderful thesis advisor. Working with Kim is always fun, challenging and rewarding. I am eternally grateful to him.

I would also like to thank Professor Jesus del Alamo for teaching the best device physics class. He has also provided invaluable advice throughout the last few years in our weekly SRC lunch meetings. I am deeply appreciative of that. I learned a lot about thinking like a materials scientist from taking Professor Sam Allen's class and reading his book. I also gained a lot of ideas about dislocations from talking to him. I would not have solved a lot of those dislocation problems without his help. I also need to express my appreciation to Professor Gene Fitzgerald. Gene is the kind of professor who spends a lot a time talking to students about any thing related to a student's life. He is always keen on research problems. I learned a lot about thinking critically from him.

Members of the EMAT group have enriched my life at MIT. Anu provided a lot of encouragement at times when my research went totally wrong. I would not have survived without our weekly conversation. I am also grateful for the huge amount of time she spend reviewing draft of this thesis. Jurgen gave me my first research problem that became the background of a lot of what I have included in this thesis. He gave me a heart warming wedding gift when Shingshing and I married each other on a cold New England winter day. I will always cherish that. Wada san shared a lot of his experience in semiconductor research with me. He took the role of my thesis advisor when Kim was not around. "Doo moo arigatoogozaimasu." My research is a continuation of Laura Giovane's thesis. I learned how to run our CVD from working with her and the need for growing Ge on Si came from the conclusion of her thesis. Over the last few years, we continued to work on several papers together. We have been a great team and I thank Laura for all her effort. I would also like to thank Desmond and Kidoo for being the most valuable research partners. Desmond, Kidoo and I started our PhD program in the same year. We have worked closely together on the Si microphotonics project and the result of our team is great. Desmond and Kidoo have brilliant plans for the future of Si microphotonics, and I wish them the best. Anand and Douglas have been my best buddies in the office. I have a lot of books and I have to confess that my books takes up too much space. I thank Anad and Douglas for all their understanding and constant encouragement. I would also like to thank Thomas Chen for his music and messages of life, Kevin for always being ready to lend a hand with experiments, Sajan for his French and Indian language lessons, Michal for sharing her life experiences on our trip to the Bell Labs, Xiaoman for getting me started with tripod polisher, Yutaka for sharing his TEM tricks, Kenichiro for his DLTS measurements, Nori for teaching me Kanseiben, Sang and Song for my first lesson in defects in semiconductors, Meghan and Jessica for helping with dislocation experiments, Pascal for sharing his knowledge in wafer bonding, Meyer for helping me learn about dislocations and wine, Mindy for helping me improve my writing skills and Ann for sharing her friendship.

My friends at the Universita degli Studi "Roma Tre" are the best research collaborators one can have. Lorenzo Colace, Gianlorenzo Masini, and Gaetano Assanto worked with me from 8AM to 8PM (sometimes 9PM) for two weeks on those Ge photdetectors. I learned so much from them. Working with them was like having my own personal tutors on optoelectronics. Beside helping me with measurement of photodetectors, they also demonstrated their technique at making the best home cooked Italian food. Without their hands-on demo, I would have never learned the art of Ragu sauce, Gelato, Spaghetti alla Carbonara, Prosciutto etc.... and that buffalo mozerella

A lot of good friends at MIT also provided a lot of help. Tom Langdo shared a lot of his experience with CVD with me. Our discussion about CVD is the key to fixing those challenging problems that kept we awake many nights. Vicky, Mat, Andy Kim, Mike all shared their knowledge about heteroepitaxy. Vab, Andy Wei and Keith gave me a lot of help. Minha, Chris, Stefan, Steve, Mat, Kidoo, and Tom are the best study group.

MTL and CMSE staff provided a lot of help. Mike Frongillo runs the best TEM lab. Vicky Diadiuk has always been supportive of my CVD project. Paul McGrath, Kurt Broderick, Joe DiMaria, Joe Walsh and Tom Takacs provided invaluable assistance at the most desperate times.

My undergraduate advisors gave me a lot of help. Professor Tom Pearsall taught my first class in optoelectronics. He took time to teach me how to use a curve tracer, a monochrometer and an MBE system while I was an undergraduate student. He helped me with graduate school applications by going through research papers published by professors at several universities and explaining the details to me. No undergraduate advisor could have been more helpful than Tom. Professor Mehmet Sarikaya spent his invaluable time teaching me some of those finer things about TEM. Professor Allen Miller trusted me and gave me admission to the MSE program at UW. Professor C. C. Lee at NTIT taught my first Intro to the MSE class. Without their willingnes to spend a little more time with me while I was an undergrad, I might have never found my way to MIT.

I would not have survived MIT without the help from my family. Martha, Betty, Peter, Henry, William, Bear, and Annie all have lent their hands at the hardest time. My parents gave me the opportunities to pursue my dream. They have supported my decision all the way. No words can described my gratitude to them. I would only hope the completion of this thesis would put more smiles on their faces. Finally, I would like to thank Shing-shing for her constant support and encouragement. This thesis is dedicated to her.

# Table of Contents

**1** Introduction ..... 17
1.1 Motivation ..... 17
1.2 Outline of thesis ..... 18
**2** Materials selection and design considerations ..... 21
2.1 Overview ..... 21
2.2 Integration of near-infrared photodetectors on Si ..... 21
2.3 Literature review ..... 23
2.4 Requirements for photodetectors for Si microphotonics ..... 29
2.5 Materials selection ..... 30
2.6 Effect of threading-dislocations on the performance of photodiodes ..... 40
2.7 Design of microphotonic photodiodes ..... 53
**3** Direct epitaxial growth of high quality Ge epilayers on Si ..... 55
3.1 Overview ..... 55
3.2 Introduction ..... 55
3.3 Experimental procedure ..... 64
3.4 Results and discussion ..... 65
3.5 Conclusion ..... 94
**4** Ge photodetectors integrated on Si ..... 95
4.1 Overview and introduction ..... 95
4.2 Experimental procedure ..... 95
4.3 Results and discussion ..... 100
4.4 Conclusion ..... 120
**5** Passivation of Ge epilayer surface ..... 123
5.1 Overview ..... 123
5.2 Introduction ..... 123
5.3 Experimental procedure ..... 125
5.4 Results and discussion ..... 127
5.5 Conclusion ..... 134
**6** Summary and future work ..... 135

6.1 Summary of thesis ....... 135
6.2 Future Work ....... 135
**Bibliography** ....... 143

# List of Figures

Figure 1.1: A schematic of an application of Si microphotoinc technology: WDM photodetector receiver..........17
Figure 2.1: Integration challenge of photodetectors grown on a thick buffer-layer. Depending on the thickness of the buffer layer, the photodetectors would typically be at least a few microns away from the transistor level. [5]..........32
Figure 2.2: A possible scheme for the integration of Ge photodetectors with Si MOSFETs and high dielectric contrast Si and $Si_3N_4$ waveguides. Selective area growth of Ge allows the selective introduction of Ge into the Si substrate and therefore achieves large scale integration of microphotonic and microelectronic components..........33
Figure 2.3: Calculated absorption coefficient of SiGe as a function of strain and composition at 1300 nm [5]..........35
Figure 2.4: Band structure of Si calculated by Chelikowsky and Cohen [224]..........36
Figure 2.5: Band structure of Ge calculated by Chelikowsky and Cohen [224]..........37
Figure 2.6: The effect of biaxial strain on the band structure of Ge..........38
Figure 2.7: The ratio of Ge intrinsic carrier concentration to the InGaAs intrinsic carrier concentration as a function of temperature..........45
Figure 2.8: Typical behavior of sensitivity versus bit-rate plot of a p-i-n receiver. At high bit-rate the contribution of shot-noise become less important..........46
Figure 2.9: Carrier drift velocity of electrons and holes in Ge calculated using equation 2.13..........49
Figure 2.10: 3-dB bandwidth of a p-i-n junction photodiode as a function of depletion width, mobility and bias voltage..........51
Figure 3.1: (a) Plan-view TEM and (b) cross-sectional TEM pictures of Ge epilayers grown at 600°C..........67
Figure 3.2: a) Plan-view TEM and (b) cross-sectional TEM pictures of Ge epilayers grown at 600°C after annealing..........68
Figure 3.3: Calculated normalized dislocation velocity in Ge epilayers grown on Si as a function of $T_L$ during cyclic annealing, assuming the system is relaxed at $T_H$ = 900°C. The

calculated dislocation velocity has a peak at about $T_L = 830°C$. An optimized cyclic thermal annealing process should have a $T_L$ close this temperature. ................................71
Figure 3.4: Cross-sectional TEM picture of Ge epilayer grown on Si by two-step UHV/CVD process after cyclic thermal annealing between $T_H = 900°C$ and $T_L = 780°C$. ........72
Figure 3.5: Cross-sectional TEM pictures of Ge grown on Si at 600°C annealed in a rapid-thermal annealing furnace for 60 seconds at (a) 650°C, (b) 750°C, (c) 850°C, and (d) 930°C. ..........................................................................................................................73
Figure 3.6: EPD pictures of Ge epilayers grown on Si at 600°C after cyclic thermal annealing between 900°C and 780°C. (a) Thickness = 552 nm, (b) Thickness = 1252 nm, (c) Thickness = 2480 nm, (d) Thickness = 3889 nm. ......................................................76
Figure 3.7: Correlation between threading-dislocation densities measured by EPD and plan-view TEM. The correlation between measurements by EPD and TEM is very good except for the measurement of sample 9A10...................................................................77
Figure 3.8: Picture of sample 6A etched by the EPD etching solution. The picture is taken using an optical microscope.........................................................................................79
Figure 3.9: EPD results of Ge selectively grown on patterned $SiO_2$/Si wafers followed by annealing. (a) EPD picture of a sample annealed at 900°C for 10 min. (b) EPD picture of a sample cyclically annealed between 900°C and 100°C ten times....................................81
Figure 3.10: Average EPD vs. width of selective area growth squares............................81
Figure 3.11: Electron diffraction pattern for a diamond cubic structure when the [110] axis is aligned to the electron beam. ..........................................................................................82
Figure 3.12: Cross-sectional TEM pictures for the Burgers vector analysis of sample 6A. These pictures are two beam bright field images with five reflecting conditions: (a) $g = [2\bar{2}0]$, (b) $g = [2\bar{2}2]$, (c) $g = [\bar{2}22]$, (d) $g = [004]$, (e) $g = [004]$................85
Figure 3.13: Cross-sectional TEM pictures for the Burgers vector analysis of sample 6AC. These pictures are two beam bright field images with four reflecting conditions: (a) $g = [2\bar{2}0]$, (b) $g = [004]$, (c) $g = [2\bar{2}2]$, (d) $g = [2\bar{2}\bar{2}]$ ........................................86
Figure 3.14: Comparison of reaction kinetic model for threading-dislocation density reduction to experimental data..................................................................................92
Figure 4.1: Schematic of the MSM photodetectors. ........................................................97
Figure 4.2: Schematic of the mesa Ge/Si heterojunction photodetector...........................97

Figure 4.3: Schematics of n-i-p Ge photodiode on p-Si substrate and p-i-n Ge on n-Si substrate. ........98
Figure 4.4: SIMS profiles of (a) the Ge n-i-p diode (on $p^+$ Si substrate) and (b) the Ge p-i-n diode (on $n^+$ Si substrate)........99
Figure 4.5: Current-voltage characteristics (positive voltage on Ge) of mesa Ge/Si diodes made with Ge grown on p-Si treated by 20 post-growth thermal annealing cycles between 900°C and 780°C. ........100
Figure 4.6: Band-diagram of Ge/Si heterojunction diode grown on p-Si substrate. .......101
Figure 4.7: Short circuit spectral responsivity of mesa heterojunction photodetectors made from Ge grown on Si treated with different post-growth annealing treatments. A responsivity enhancement due to cyclic annealing is clearly demonstrated.........101
Figure 4.8: . Responsivity at 1300 nm versus applied bias voltage (positive voltage applied on Ge) of mesa heterojunction photodetectors made from Ge grown on Si treated with different post-growth annealing. Annealed samples reach maximum responsivity at lower bias voltages........102
Figure 4.9: Photocurrent response of a heterojunction photodetector made from Ge grown on Si followed by 20 annealing cycles (6AC20). ........104
Figure 4.10: The relationship between pulse width (FWHM) and -3dB frequency assuming a hyperbolic secant$^2$ time dependence. ........104
Figure 4.11: Photocurrent response of MSM devices at 1300 nm versus applied bias (symbols). The lines are fitted based on the Hecht model [193]. Cyclic thermal annealed samples reach maximum responsivity at lower bias voltages. ........106
Figure 4.12: Photocurrent response of MSM devices illuminated by 100 ps pulses at 1.32 μm. The photodiodes were fabricated from Ge grown on Si treated by 20 annealing cycles (6AC20). In the inset, the pulse width dependence on the inverse of the electric field is plotted: the symbols are experimental data, the solid line is a linear fit. An electron mobility of 3500 $cm^2/V$-s was estimated from this experiment. ........107
Figure 4.13: Calculated equilibrium band diagram of Ge/Si p-i-n diodes for (a) n-i-p Ge diode on p-Si substrates, and (b) p-i-n Ge diode on n-Si substrate. Continuous lines refer to calculated band diagram for substrates of resistivities of 1 Ω-cm. Dashed lines refer to calculated band diagram for substrates of resistivities of 0.01 Ω-cm........110

Figure 4.14: Calculated reverse dark current densities for Ge/Si p-i-n diodes with different substrate doping type and density. Curves differ for the surface recombination velocity at the Si/Ge interface used in the calculations. ....................112
Figure 4.15: Calculated 1300 nm responsivity of Ge/Si p-i-n diodes as a function of the substrate doping. ....................113
Figure 4.16: Measured dark current versus voltage for mesa p-i-n Ge/Si diodes grown on: (a) p-Si and $p^+$-Si substrates, (b) n-Si and $n^+$-Si substrates. For the $p^+$-Si case, the inferred diode ideality factor is 1.2 and the saturation current density at 0 V is 2 mA/cm2. The reverse current at 1 V is 20 mA/cm2. ....................115
Figure 4.17: Measured photocurrent-voltage characteristics of mesa p-i-n Ge/Si diodes at 1300 nm. ....................117
Figure 4.18: Calculated 1300 nm responsivity of Ge/n-Si p-i-n diodes as a function of the substrate doping considering the diffusion of dopant from the n-Si substrate. ....................117
Figure 4.19: Measured short circuit spectral responsivity of a mesa p-i-n Ge photodiode fabricated on $p^+$-type Si. ....................118
Figure 4.20: Responsivity of n-i-p Ge (4 μm) / $p^+$-Si photodiode with and without $SiO_2$ anti-reflection coating. ....................120
Figure 5.1: (a) Cross sectional TEM micrograph of a Si epilayer grown on the Ge epilayer. (b) Cross sectional TEM micrograph of a Si epilayer grown on Ge, with $SiO_2$ grown by thermal oxidation as the topmost layer. ....................128
Figure 5.2: Capacitance-voltage characteristics of $SiO_2$/Si/Ge/$p^+$-Si structure. ....................129
Figure 5.3: High frequency C-V curve measured at 300K and 77K. ....................130
Figure 5.4: Comparison of measured C-V curve (1 MHz) and calculated C-V curve. ...131
Figure 5.5: Measured interface state density as a function of surface potential. ....................133
Figure 6.1: Geometry for the reduction of threading-dislocations by gliding to mesa sidewalls ....................136
Figure 6.2: Vertical coupling of Ge photodiode with Si waveguide. Ge photodiode is on top of the Si waveguide. ....................138
Figure 6.3: Vertical coupling of a Ge photodiode with Si or $Si_3N_4$ waveguide. Ge photodiode is under the waveguide. ....................139

Figure 6.4: Design of a vertical p-i-n Ge photodiode grown on Si integrated with a $Si_3N_4$ waveguide. ....................................................................................................................140
Figure 6.5: Design of a lateral p-i-n Ge photodiode grown on Si integrated with a $Si_3N_4$ waveguide. ....................................................................................................................141
Figure 6.6: Depletion width of an $n^+$-p Ge diode as a function of voltage and doping concentration....................................................................................................................142

# List of Tables

Table 3.1: Annealing parameters and characterization results of samples grown by two-step UHV/CVD process with the first step at 350°C and the second step at 600°C.................................. 65
Table 3.2: Annealing parameters and characterization results of samples grown by two-step UHV/CVD process with the first step at 350°C and the second step at 900°C.................................. 66
Table 3.3: Annealing parameters and characterization results of samples annealed at different TL. The threading-dislocation density decreases as TL approaches 830°C.................................... 72
Table 4.1: Annealing parameters and characterization results of samples used for making MSM and Ge/Si heterojunction detectors. Samples were grown by two-step UHV/CVD process with the first step at 350°C and the second step at 600°C. ...................................................................... 96

# Chapter 1

# Introduction

## 1.1 Motivation

Si microphotonics [1], the optical analog to Si microelectronics, is the integration of optoelectronic components on Si substrates using process technologies that are compatible with Si microelectronic technology. Successful development of Si microphotonic technology can bring the advantage of optics to the Si platform and dramatically improve our information processing capability and deliver the benefit of optoelectronic technology at a much lower cost. Figure 1.1 shows an application of Si microphotonic technology: a wavelength-division-multiplexing (WDM) photodetector receiver. In this application, Si or $Si_3N_4$ waveguides, waveguide ring-resonators, Ge photodetectors and Si microelectronics are all integrated on a Si chip. In more sophisticated applications, light emitters, and optical modulators can also be integrated on Si.

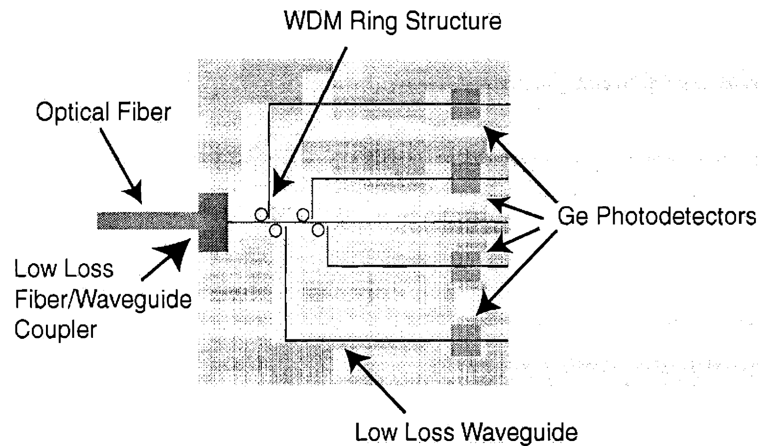



**Figure 1.1:** A schematic of an application of Si microphotoinc technology: WDM photodetector receiver.

Optical waveguides [4], optical modulators [3], photodetectors [5], light emitters [2], and optical amplifiers are the key components for Si microphotonic systems. This thesis investigates the integration of Ge p-n junction photodiodes on Si[1]. The goal is to develop processing technologies that allows the direct integration of high quality Ge epilayers on Si, and to provide an understanding of the materials properties for the design of integrated Ge photodiodes.

## 1.2 Outline of thesis

In chapter 2, design issues related to the integration of near-infrared photodiodes on Si are discussed. Based on the consideration of the performance metrics of photodiodes and a discussion of the effect of threading-dislocations on the operation of photodiodes, Ge is selected as the most reasonable material for the integration of near-infrared photodiodes on Si for Si microphotonic applications.

Chapter 3 describes the direct epitaxial growth of Ge on Si. Based on a careful literature review, a two-step ultra-high-vacuum/chemical-vapor-deposition (UHV/CVD) process is designed for the growth of Ge epilayers directly on Si. The threading-dislocations in Ge epilayers are reduced by cyclic thermal-annealing process. The threading-dislocations in the as-grown and annealed Ge epilayers were studied extensively by transmission-electron-microscopy (TEM). Based on the TEM study, the mechanism for the reduction of threading dislocations in Ge epilayers is discussed.

1. Many devices can be used as photodetectors. This thesis focuses on the p-n junction photodiodes.

Chapter 4 describes the performance of Ge photodiodes integrated on Si. The beneficial effect of cyclic thermal-annealing on the electrical properties of Ge epilayers grown on Si is illustrated by the improved performance of metal-semiconductor-metal (MSM) Ge photodetectors and Ge/Si heterojunction photodiodes. Next, the properties of Ge p-i-n photodiodes are investigated and the role of misfit-dislocations at the Ge/Si interface is discussed. Finally, p-i-n Ge photodiodes made from Ge epilayers grown on Si with responsivity of 770 mA/W at 1300 nm is discussed.

Chapter 5 describes the development of a process technology for the passivation and protection of the Ge epilayer surface. Protection of Ge epilayer in Si wafer cleaning chemistry is provided by a thin-smooth Si epilayer grown on the Ge epilayer. Passivation for the Ge surface is provided by the oxidation of Si epilayer grown on Ge. Capacitance-voltage (C-V) characteristics of the metal-oxide-semiconductor (MOS) devices made this way demonstrate the good quality of the interface between the thermally grown silicon oxide and Ge.

Finally, Chapter 6summarizes this thesis work and concludes with suggestions for future development of Si microphotonic technology.

# Chapter 2

# Materials selection and design considerations

## 2.1 Overview

This chapter first presents the reason for investigating the integration of near-infrared photodetectors on Si. A literature review of the work carried out in this field is then presented, followed by a justification for the selection of pure Ge as the material for integrating near-infrared photodiodes on Si. Finally, the effect of threading-dislocations on the operation of photodiodes is discussed leading to the conclusion that Ge photodiodes are the best short term solution for Si microphotonic receivers.

## 2.2 Integration of near-infrared photodetectors on Si

Integration of optoelectronic devices on Si substrates has been an active research field for many years. There are several reasons: 1) Si substrates cost less and are mechanically stronger and thermally more conductive compared to InP and GaAs substrates. InP and GaAs substrates are currently used for making optoelectronic devices. If reliable and efficient LEDs, lasers and photodetectors can be made using Si wafers as substrates, the cost for these components can be reduced. 2) Si microelectronic technology provides the highest level of integration. Integration of optoelectronic devices with Si microelectronic devices can significantly improve the ability of integrated circuits (IC). Recent commercial developments in system on a chip (SOC), fiber to the home (FTTH), and fiber to the building (FTTB) concepts can all benefit from the successful development of Si based optoelectronic integrated circuit (OEIC) technology [6]. Application examples include fiber to the home receivers, on-chip optical clock distribution, and some high speed optical data transfer between Si chips.

Photodetectors and optical receivers are important components in optical networks. Photodetectors are not only used at the receiving end, they are also used as optical power monitoring devices. For networks operating in the first optical window of modern silica optical fibers (~850 nm), low cost Si detectors could be used. However, for operation in the second window (~1300 nm) and the third window (~1550 nm), InGaAs[2] or Ge photodiodes are needed [7]. The lattice constant of Ge and $In_{0.53}Ga_{0.47}As$ are very different from that of Si. $In_{0.53}Ga_{0.47}As$ and Ge photodiodes are therefore typically made on lattice matched substrates such as InP and Ge substrates. There are a lot of benefits to be gained if near-infrared photodiodes operating from 1300 nm to 1550 nm can be integrated on Si with Si microelectronics.

The integration of near-infrared photodiodes on Si has been pursued by several research groups. The key challenge is the lattice mismatch between Si (Si lattice constant = 0.543 nm) and semiconductor materials that are sensitive to light in the range of 1300 nm to 1550 nm ($In_{0.53}Ga_{0.47}As$ lattice constant = 0.587 nm; Ge lattice constant = 0.565 nm). This lattice mismatch causes two major problems when one deposits $In_{0.53}Ga_{0.47}As$ or Ge epilayers on Si: (1) the introduction of high densities of misfit-dislocations and threading-dislocations in the epilayer, and (2) high surface roughness due to island growth. High surface roughness causes difficulties in process integration. High threading-dislocation densities can degrade device performance and compromise device reliability.

2. The International Union of Pure and Applied Chemistry (IUPAC) recommends the use of GaInAs instead of InGaAs. In this thesis, InGaAs is used because most papers and books use InGaAs. For the same reason, this thesis use units typically used in text books in semiconductors physics rather than SI units.

Misfit-dislocations are introduced to relax the lattice mismatch between the epilayer and the Si substrate and are typically confined to the interface between the epilayer and the Si substrate. If one makes devices (for example photodetectors) far away from the epi-substrate interface, problems associated with the misfit-dislocations can be avoided. Threading-dislocations are the by-product of the introduction of misfit-dislocations and do not relax lattice-mismatch strain. Threading-dislocations are left in the epilayers because dislocations cannot end in a crystal. Dislocations have to either form a loop or terminate at a free surface. Since the epilayer surface is always the nearest free surface to the epi-substrate interface, these threading-dislocations typically thread from the epi-substrate interface to the epilayer surface. Since devices are usually built close to the epilayer surface, these threading-dislocations cannot be easily avoided. Threading-dislocations can reduce carrier lifetime, carrier mobility and compromise device reliability. Discussion of the effect of threading-dislocations on the electrical properties of semiconductors is reviewed in section 2.6. To integrate high performance $In_{0.53}Ga_{0.47}As$ or Ge near-infrared photodetectors on Si, it is necessary to solve problems related to threading-dislocations and surface roughness. Section 2.3 reviews works related to the integration of near-infrared photodetectors on Si.

## 2.3 Literature review

Luryi and co-workers pioneered the integration of Ge photodetectors directly on Si by molecular-beam-epitaxy (MBE) [8]. To prevent island growth and minimize the effect of misfit-dislocations, they introduced a SiGe graded-buffer layer between the Ge epilayer and the Si substrate. Their transmission-electron-microscope (TEM) pictures revealed a high density (above $10^9\ cm^{-2}$) of threading-dislocations in the Ge layer. These Ge/Si

photodetectors demonstrated a 40% external quantum-efficiency at a wavelength of 1450 nm and a dark current of 50 $mA/cm^2$. They did not report quantum efficiency at 1550 nm. Kastalsky, Luryi and co-workers later improved the materials quality by introducing a "glitche-grading" region between the Ge layer and the Si substrate [9]. The "glitche-grading" buffer was a combination of the graded-buffer layer and the "glitche" layer. The "glitche" region was a Ge(50 nm)/$Si_{0.3}Ge_{0.7}$(10 nm) superlattice. Their TEM measurement showed a reduction in threading-dislocation density to the $5x10^7$ $cm^{-2}$ range. Their capacitance-voltage measurement showed a depletion width of about 0.15 μm. The measured leakage current density was 0.4 $mA/cm^2$ due to the reduced threading-dislocation density and the reduction in depletion width[3].

To further reduce the leakage current density, Luryi and Pearsall suggested the use of strained-layer $Si_{1-x}Ge_x$/Si superlattice (SLS) as the active absorption layer in near-infrared photodetectors integrated on Si [10]. This idea is based on the bandgap calculations by People [11]. According to People's calculation, strained $Si_{1-x}Ge_x$ alloys coherently grown on Si have a much smaller bandgap compared to relaxed $Si_{1-x}Ge_x$ alloys [12]. This calculation was later experimentally verified by Lang and co-workers [13]. Using strained-layer $Si_{1-x}Ge_x$/Si superlattice with $x > 0.35$, materials with bandgap lower than 1300 nm and 1550 nm can be grown essentially dislocation free on Si. Strained-layer $Si_{1-x}Ge_x$/Si superlattice photoconductors [14], waveguide p-i-n photodiodes [15], and avalanche waveguide photodiodes [16] [17] with good photoresponse at 1300 nm were demonstrated. The photoresponse at 1550 nm was very low. The disadvantage of strained-layer $Si_{1-x}Ge_x$/Si superlattice material is its low absorption coefficient. With

3. Total leakage current due to carrier generation in the depletion region of a p-n junction is proportional to the depletion region width.

$x = 0.6$, the absorption coefficient is only about 21 $cm^{-1}$ at 1300 nm [16] [13]. Because of the low absorption coefficient, detectors made from strained-layer $Si_{1-x}Ge_x$/Si superlattice need a long absorption length to provide a reasonable quantum-efficiency. For example, with a 300 μm long waveguide geometry and $x = 0.6$ an external quantum-efficiency of 10% at 1300 nm was measured [15]. The quantum efficiency at 1550 nm was about 2% and the measured leakage current density was 7 mA/$cm^2$. Note that the leakage current density for strained-layer $Si_{1-x}Ge_x$/Si superlattice photodiodes is not much lower compared to that of Ge/Si photodiodes earlier reported by Kastalsky and Luryi. Etch-pit-density measurement of threading-dislocations revealed a density of about $10^4$ $cm^{-2}$. When strained-layer $Si_{0.5}Ge_{0.5}$/Si superlattice photodiodes were measured at normal incidence, only 1% external quantum efficiency at 1300 nm was measured with a leakage current density of 60 mA/$cm^2$ at a reverse bias voltage of 7 V [18]. Strained-layer $Si_{1-x}Ge_x$/Si superlattice photodiodes were later integrated with Si rib waveguide [19] [20] [21] [22]. Other strained-layer $Si_{1-x}Ge_x$/Si superlattice based photodiodes have also been reported [23] [24] [25] [26] [27] [28] [29]. All of these photodiodes require a long waveguide geometry to achieve reasonable quantum efficiencies at 1300 nm and 1550 nm.

The limitation of strained-layer $Si_{1-x}Ge_x$/Si superlattice is the low absorption coefficient and the thickness of each strained-layer. The limitation on absorption coefficient can be solved by adding more Ge into the $Si_{1-x}Ge_x$ layer. However adding more than 60% of Ge brings the critical-thickness below 10 nm. Although the use of strained-layer superlattice allows the growth of many pairs of strained-$Si_{1-x}Ge_x$/Si on Si. The total critical-thickness of the strained-layer superlattice is still limited by the critical-thickness of the average concentration of the SiGe/Si superlattice layers. One way to solve these problems is to go

beyond the SiGe binary system and work with the SiGeC ternary system. The idea is that by adding elements (such as C) with lattice constant smaller than Si, the lattice mismatch between SiGe alloy and Si can be compensated [30]. Typically for every 1% of C added, lattice-mismatch due to about 8% of Ge can be compensated [31]. Normal incidence $Si_{0.25}Ge_{0.6}C_{0.15}$ p-i-n photodiodes with 80 nm of active SiGeC layer have been reported [32]. The external quantum efficiency at 1.3 μm was about 1% and the leakage current density was 7 $mA/cm^2$. The threading-dislocation density was estimated to be below $10^8$ $cm^{-2}$ and the absorption coefficient was 10 $cm^{-1}$ at 1550 nm and 340 $cm^{-1}$ at 1300 nm [33] [34]. $Ge_{1-x}C_x$ photodiodes have also been reported [35] [36]. The addition of C was found to reduce the leakage current and improve the ideality factor. With 590 nm of heavily doped p-$Ge_{0.902}C_{0.008}$ (2.7 x $10^{18}$ $cm^{-3}$) on n-Si ($10^{14}$~$10^{15}$ $cm^{-3}$), the measured external quantum efficiency at 1300 nm was 2.2% and the leakage current density was 1.4 $mA/cm^2$.

It is clear from the above review that SiGe strained-layer superlattice and SiGeC based photodiodes provide very little improvement from the Ge/Si approach first demonstrated by Luryi and Kastasky in terms of external quantum efficiency and leakage current. Although the use of SiGe strained-layer superlattice does reduce the threading-dislocation densities in the epilayers, the absorption coefficient is much lower. Also, the reduction in threading-dislocation density did not help reducing the leakage current density.

Another approach to the integration of near-infrared photodiodes on Si is the integration of InGaAs photodiodes on Si. InGaAs photodiodes made on InP are efficient, fast and of low leakage current [37] [70]. The challenge is the 8% lattice mismatch between $In_{0.53}Ga_{0.47}As$ (lattice matched to InP with bandgap at 1650 nm) and Si that guaranteed a

high density of threading-dislocations in the InGaAs epilayer grown on Si. Despite this challenge, InGaAs epilayers have been grown on Si using various techniques and InGaAs photodiodes have been integrated on Si [38] [39] [40] [41] [42] [43]. For example, Razeghi and co-workers demonstrated InP/InGaAs(4 μm)/InP(1 μm)/GaAs(1 μm) p-n diffused-junction photodiodes on Si with 88% external quantum efficiency at 1300 nm and 92% external quantum efficiency at 1550 nm and a leakage current density of 1 mA/cm$^2$ at -1 V [38]. This performance is much better compared to that produced by the SiGe and SiGeC approach. The excellent quantum-efficiency can be understood in terms of InGaAs's high absorption-coefficient at 1300 nm and 1550 nm (>10$^4$ cm$^{-1}$). The much lower leakage-current density compared to those of SiGe SLS photodiodes is probably due to the use of diffused junction rather than mesa structures. The threading-dislocation densities in InGaAs epilayers grown on Si are typically on the order of 10$^8$ cm$^{-2}$ range [43]. This might explain the much higher leakage current density compared to that of InGaAs photodetectors made on InP (typically in the range of 16 μA/cm$^2$).

To completely eliminate threading-dislocations, InGaAs/InP structures can be bonded to Si substrates. The InP substrates can be etched by HCl, leaving behind InGaAs on Si. The final products are threading-dislocation free InGaAs/InP structures on Si: a perfect material for making near-infrared photodiodes on Si [44] [45] [46] [47] [48]. Near-infrared InGaAs photodiodes integrated on Si by wafer bonding typically have 100% quantum efficiency and leakage current density similar to that of InGaAs photodiodes grown on InP. Wafer bonding technique, however, still requires the handling of InP substrates. InP substrates are fragile and expensive compared to Si wafers. Wafer bonding, unlike selective area epitaxy, does not provide the possibility of selective introduction of InGaAs material on Si in designated small areas. The introduction of III-V

compound into a Si processing line is also an issue to be resolved. All the elements in InGaAs are dopants in Si. Cross contamination is an issue to be considered if III-V compound semiconductors are to be introduced into the Si processing line.

Another possible solution is to go back to the Ge/Si approach. Compared to SiGe and SiGeC, Ge has an absorption coefficient that is almost comparable to that of InGaAs in the range of 1300 nm to 1550 nm. Considering the fact that the commercial applications of SiGe BiCMOS technology have already been demonstrated, the intoduction of Ge into the Si processing technology raises less issues related to cross contamination. It is also well known that Ge can be grown selectively on patterned $SiO_2$/Si substrates [49]. The key challenge is the epitaxial growth of flat-Ge epilayers on Si with low surface roughness and low threading-dislocation densities. Samavedam and co-workers have integrated Ge p-n junction photodiodes on thick (> 10 μm) optimized SiGe graded buffer-layers grown on Si [54] [55]. The optimized SiGe graded buffer-layer technology includes an intermediate chemo-mechanical-polishing (CMP) and regrowth step. High quality Ge film with threading-dislocation densities of $2 \times 10^6$ $cm^{-2}$ was achieved on Si. The p-n junction was defined by in-situ doping and mesa etching. The mesa side-wall was passivated by a thin layer of PECVD $SiO_2$. The measured external quantum efficiency was 12.6% at 1300 nm, the leakage current density was 0.22 $mA/cm^2$ at -1 V with a depletion region of 0.24 μm. Samavedam's work demonstrated that high quality Ge photodiodes can be integrated on Si if the threading-dislocation density is low and the mesa side-wall is passivated. The challenge of this graded-buffer technology is the integration of the 10 μm thick SiGe graded-buffer with the planar Si CMOS technology. If Ge of similar quality can be grown directly on Si, process integration of Ge photodiodes with Si CMOS technology would be much simpler.

Colace and co-workers demonstrated that Ge epilayers with low root-mean-square surface roughness (~ 0.5 nm) can be grown on Si using a two-step CVD process [51] [52] [53]. Colace and co-workers demonstrated metal-semiconductor-metal photodetectors with their Ge epilayers. The measured external quantum-efficiency was 12.6% at 1.3 μm. As will be discussed in Chapter 3, Ge epilayers grown on Si using this two-step process have a threading-dislocation density on the order of $10^9$ cm$^{-2}$. The threading-dislocation density, however, can be reduced to the mid $10^6$ cm$^{-2}$ level by cyclic thermal-annealing [56] [57]. Selectively grown Ge mesas on Si with no threading-dislocation after cyclic annealing were also demonstrated. Details will be discussed in Chapter 3. Applying this improved Ge epilayer on Si, Ge photodiodes with external quantum efficiency of 52% at 1.32 μm and 20% at 1.55 μm have been demonstrated with 1 μm of Ge [58] [59]. The leakage current density was 30 mA/cm$^2$.

This section provided a short review of the integration of the near-infrared photodetectors on Si. Two conclusions can be drawn from this literature review: (1) Materials with high absorption coefficients are the key to high quantum efficiency. (2) Materials with the lowest threading-dislocation densities do not always make the best photodetectors. Surface passivation is also important. More details regarding these points will be discussed later in this thesis. The following section will first provide a discussion of the requirements for integrated photodetectors for Si microphotonics.

## 2.4 Requirements for photodetectors for Si microphotonics

Si microphotonic technology is the integration of optoelectronic components on Si substrates using process technologies that are friendly to Si microelectronic technology.

An important feature of Si microphotonic technology is the use of high index contrast waveguide systems such as the $Si/SiO_2$ and $Si_3N_4/SiO_2$ (core/cladding) systems. The high optical confinement in these waveguide systems allows the fabrication of a high density of micron-size waveguide bends, waveguide splitters and wave-length-division (WDM) multiplexing filters on Si [4] [60]. Another important feature of Si microphotonic technology is the process compatibility with Si based microelectronic technology. These two features, the high integration density and Si process compatibility, ensure the large scale integration of microelectronic and microphotonic devices on Si.

Based on the above discussion, the requirements for the integration of photodetectors for Si microphotonics are: (1) Si microelectronic process compatibility. (2) Capability for large scale integration with microelectronic technology and waveguide technology. (3) High photodetector performance. The following section will discuss the materials selection for the integration of photodetectors for Si microphotonic technology.

## 2.5 Materials selection

### 2.5.1 Process Compatibility with Si technology

Current Si microelectronic technology is based on the Si CMOS and Cu interconnect technologies. An important feature of the current Si microelectronic technology is the use of chemo-mechanical polishing (CMP) for the planarization of every layer of transistors and interconnects. Examples can be found in the shallow trench isolation (STI) process and the damascene and dual damascene processes [61] [62]. Another important feature of Si microelectronic technology is its intolerance to cross-contamination. For simple process integration of microphotonic technology with microelectronic technology,

microphotonic technology must provide a close resemblance to the Si CMOS technology and introduce little cross-contamination problems.

Among the materials discussed in section 2.3, InGaAs photodetectors made on Si provide the best performance in terms of high quantum efficiency and low leakage current. InGaAs, indeed, is the ideal material for making near-infrared photodetectors [37] [70]. However, introduction of InGaAs into the Si process raises serious concern regarding cross-contamination. All the elements in InGaAs are dopants in Si. The equilibrium partial pressure of As related species such as $As_4$ or $As_2$ is in the range of 1 atm to 10 atm at the temperature range of 700°C to 900°C [63]. Annealing of InGaAs at high temperature can result in significant As loss and change in surface stoichiometry. This feature would limit InGaAs to the back-end Si processing technology and make process integration difficult.

SiGe, SiGeC and Ge, on the other hand, do not pose serious cross-contamination problems. SiGe based BiCMOS technology has been developed for commercial applications [61]. A more important question is related to the melting temperature of SiGe alloys. The melting temperature of Si is 1415°C. For Ge, it is 937°C. Si and Ge are completely soluble both in liquid phase and solid phase. There is, therefore, no eutectic point in the binary SiGe phase diagram. The melting temperature of SiGe, therefore, decreases monotonically with the addition of Ge. The introduction of pure Ge would limit the annealing temperature of any later processing to temperature below 937°C.

### 2.5.2 Capability for large scale integration

To allow the large scale integration of Si microphotonic components with Si microelectronic devices, each microphotonic component including the photodetectors must be small. This is the reason why high dielectric contrast waveguide systems such as $Si/SiO_2$ and $Si_3N_4/SiO_2$ systems are selected for the Si microphotonic waveguide devices. The photodetector technology must also allow large scale integration.

Giovane studied the integration of near-infrared photodetectors grown on graded buffer layers with poly-Si waveguides [5]. Figure 2.1 shows a schematic to illustrate this integration scheme. Using graded buffer layers, the photodetector is several microns above the transistor level.

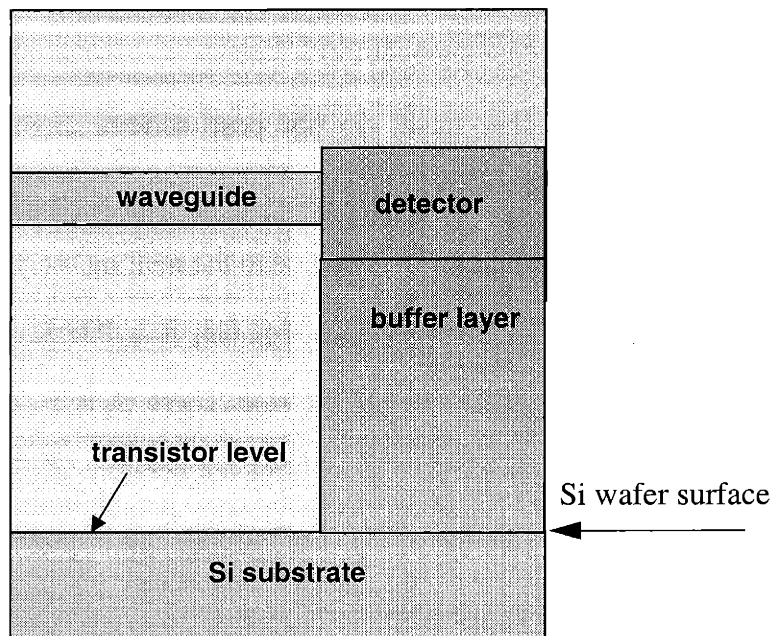



**Figure 2.1:** Integration challenge of photodetectors grown on a thick buffer-layer. Depending on the thickness of the buffer layer, the photodetectors would typically be at least a few microns away from the transistor level. [5].

Another possible way to integrate microphotonic photodetectors with Si microelectronic is selective area growth. By selective area growth, semiconductor materials that are sensitive to 1300 nm and 1550 nm light can be selectively introduced into the Si substrates. The selective area growth of Ge on patterned $SiO_2/Si$ wafer has been demonstrated [56] [65]. With selective area growth, planar integration of Si MOSFET and Ge photodetectors can be achieved. Figurer 2.2 shows a schematic to illustrate this point.

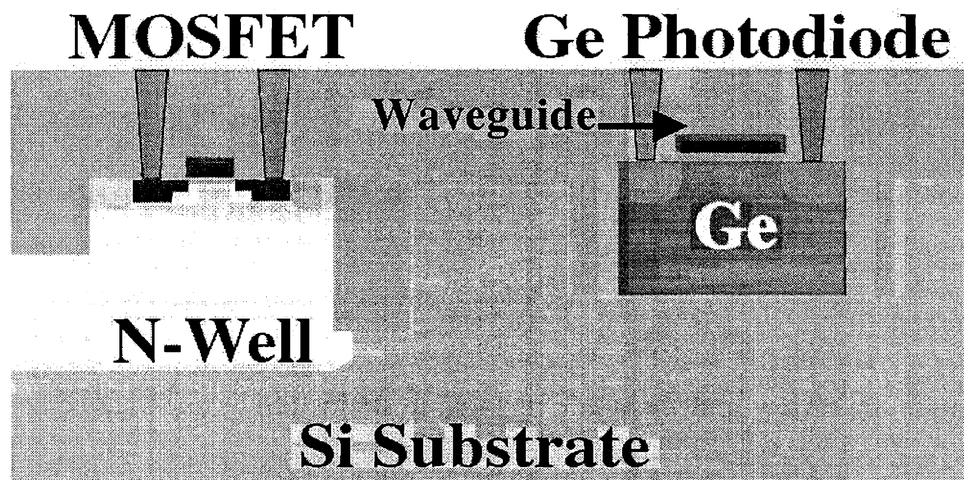



**Figure 2.2:** A possible scheme for the integration of Ge photodetectors with Si MOSFETs and high dielectric contrast Si and $Si_3N_4$ waveguides. Selective area growth of Ge allows the selective introduction of Ge into the Si substrate and therefore achieves large scale integration of microphotonic and microelectronic components.

### **2.5.3** Photodiode performance

The performance of a photodiode is described by its quantum efficiency, leakage current and speed. A high performance photodiode for Si microphotonic applications must provide high quantum efficiency, low leakage current and high speed at a small bias voltage. The photodiode should also be small to allow large scale integration. The smaller the photodiode, the higher the density of integration.

The quantum efficiency ($\eta$) of a photodiode can be described by the following equation.

$$\eta = \eta_o \cdot (1 - \exp(-\alpha d)) \cdot \varepsilon \tag{2.1}$$

$\eta_o$ is the optical coupling efficiency and represents the percentage of the input optical power that is coupled into the active region of the photodiode. $\alpha$ is the absorption coefficient of the active region of the photodiode, $d$ is the distance that the light travels in the active region and $\varepsilon$ is the collection efficiency of the optically generated carriers in the photodiode. To make small and efficient photodiodes (about the size of a few microns), the absorption coefficient must be high ($\sim 10^4$ $cm^{-1}$). Both InGaAs and Ge have high absorption coefficient at 1300 nm and 1550 nm. This is the main reason for the much higher quantum efficiencies of InGaAs and Ge photodiodes integrated on Si compared to those of SiGe photodiodes.

According to the review in Section 2.3, research in strained SiGe superlattice and SiGeC materials show that these materials have small absorption coefficient in the 1300 nm to 1550 nm range. It is interesting to find out if there is a possibility to engineer SiGe superlattices with much higher absorption coefficient by exploring a wide range of strain and Ge fraction space. The absorption coefficient of SiGe materials as a function of strain and Ge fraction has been calculated by Giovane [64]. Figure 2.3 shows the calculated absorption coefficient at 1.3 μm.

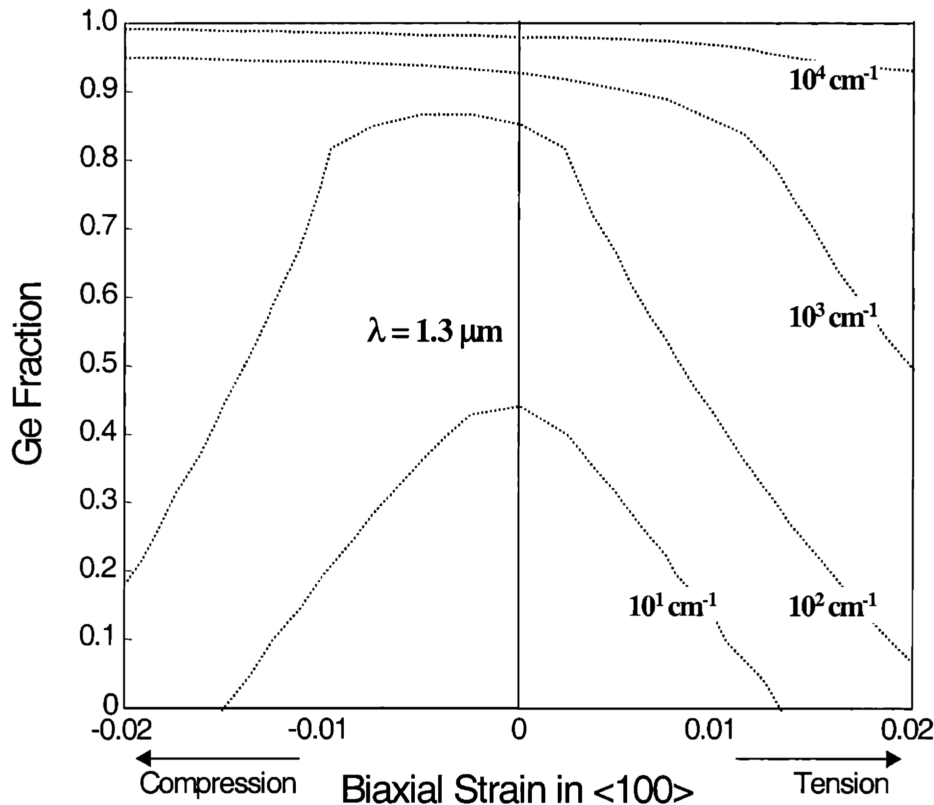



**Figure 2.3:** Calculated absorption coefficient of SiGe as a function of strain and composition at 1300 nm [5].

Figure 2.3 shows that compressive strain can pull down the iso-absorption contour for $\alpha = 10^2$ cm$^{-1}$ while pushing the iso-absorption contour for $\alpha = 10^4$ cm$^{-1}$ up. The reason for this behavior lies in the band structure of Si and Ge [66]. Figures 2.4 and 2.5 show the band diagrams of Si and Ge respectively.

Both Si and Ge are indirect band gap materials. The edge of the Si conduction band is close to the X-valley (<100> directions). The edge of the Ge conduction band is at the L-valley (<110> directions). One major difference between the Si and Ge band structure, however, is that Ge conduction band has a Γ-valley that is very close to the conduction

band edge. This Γ-valley provides a mechanism for electrons in the valence band to absorp optical power easily and be promoted into the conduction band. This is a two-particle process and is essentially the mechanism that gives direct band-gap semiconductor materials such as InGaAs their high absorption coefficient ($10^4$ $cm^{-1}$). This kind of absorption process is more difficult in Si because in the Si band structure, the Γ-valley is quite distant from the valence band edge. Most of the optical absorption in Si, therefore, requires electrons at the valence band edge to be promoted to the X-valley. This process requires a photon, an electron and a phonon for momentum conservation. Since this is a three-particle process and is less efficient compared to direct transitions, this process only gives low absorption coefficient for photons with energy close to the band edge.

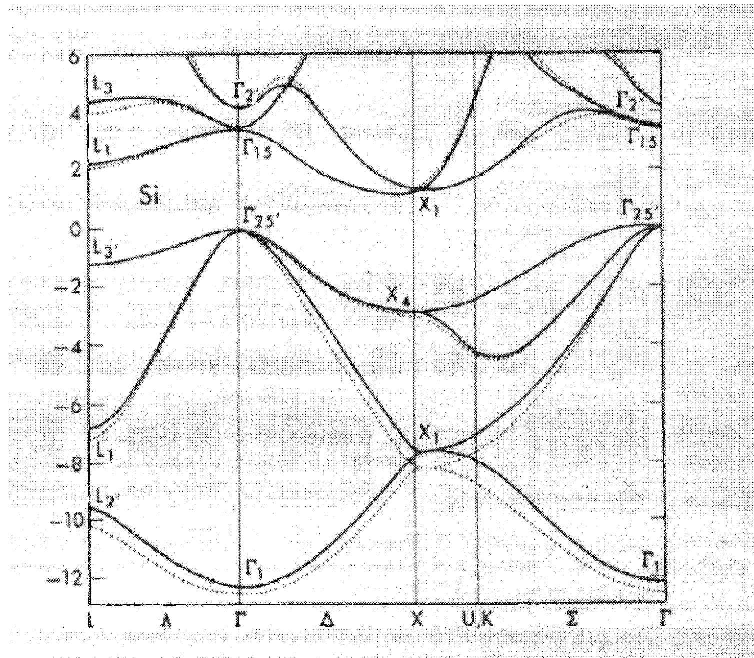



**Figure 2.4:** Band structure of Si calculated by Chelikowsky and Cohen [224].

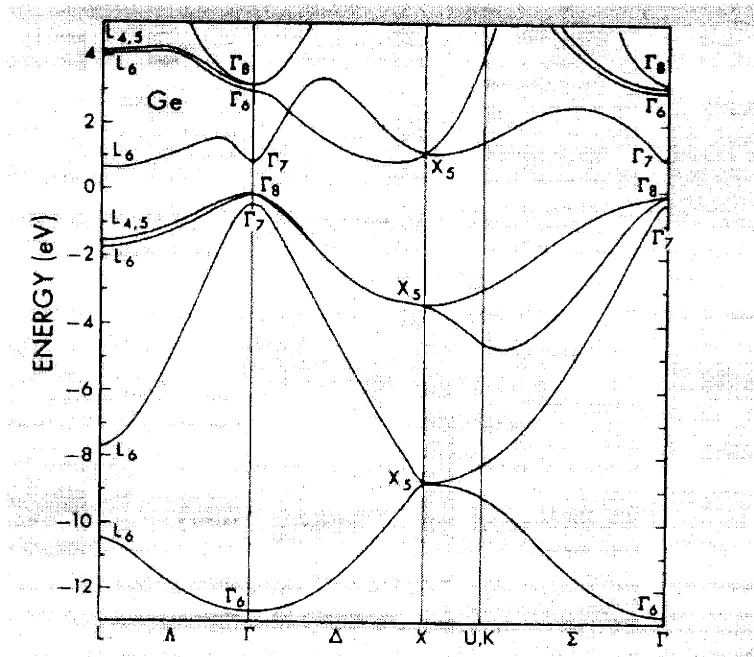



**Figure 2.5:** Band structure of Ge calculated by Chelikowsky and Cohen [224].

The effect of strain on the band structure can be estimated using deformation-potential theory [67] [68] [69]. Figure 2.6 shows how the Γ-valley, X-valley and L-valley in the Ge band structure change with biaxial strain in the (001) plane. The biaxial strain in the (001) plane squeeze the diamond cubic unit cell of Ge into a tetragonal unit cell. Because the Poisson ratio of Ge is less than 0.5, the volume of the unit cell is reduced when compressive biaxial strain is applied. The volume of the unit cell is enlarged when tensile biaxial strain is applied. The change in symmetry causes splitting of the light-hole and the heavy-hole states in the valence band. In the conduction band, the biaxial strain splits the X-valley and shifts the L-valley and Γ-valley. The X-valley splits into the X-valley that represents the [100] and [010] directions and the Z-valley that represents the [001] direction. The X-valley is pulled down due to the compressive biaxial strain. This is the reason why compressive strain can reduce the band gap of Ge and SiGe alloys. This is also

the reason why the iso-absorption contour for $\alpha = 10^2$ cm$^{-1}$ in Figure 2.3 is pulled down by the application of compressive strain. The shift of the Γ-valley can be calculated using the following formula:

$$\Delta E = D\frac{\Delta V}{V} \tag{2.2}$$

where $\Delta E$ is the change in the Γ-valley band edge energy, $D$ is the hydrostatic deformation potential, $V$ is the volume and $\Delta V$ is the change in volume. Since the hydrostatic deformation potentials for the Γ-valley of Ge and SiGe are negative, compressive strain in the (001) plane pushes the Γ-valley up. This is the reason why compressive strain can push the iso-absorption contour for $\alpha = 10^4$ cm$^{-1}$ up as seen in Figure 2.3.

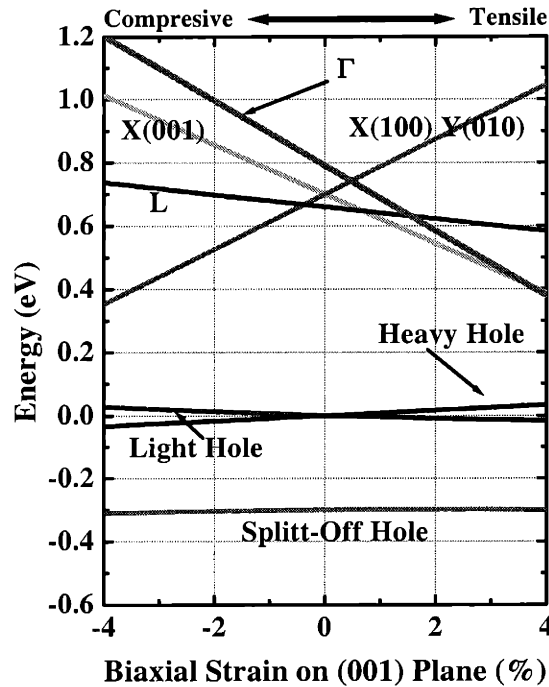



**Figure 2.6:** The effect of biaxial strain on the band structure of Ge.

Figure 2.3 and Figure 2.6 show that the only way to obtain high absorption coefficient using the SiGe alloy system is to use relaxed or tensile strained alloys with high Ge fraction. Adding Si or C into Ge increases the band gap and decreases the absorption coefficient [32]. Strain relaxed or tensile strained pure Ge is the best choice for integrating efficient near-infrared photodiodes on Si.

This section presented the basis for the selection of the semiconductor material to be used as the active region in the photodetectors for Si microphotonic technology. InGaAs provides a high absorption coefficient but is more difficult for process integration with Si microelectronic devices due to cross contamination problems. InGaAs, therefore, should be reserved for the integration of discrete near-infrared photodetectors on Si until cross contamination problems can be solved. SiGe strained layer superlattices and SiGeC alloys are quite compatible with Si processing technology. These materials, however, do not have high enough absorption coefficient at 1300 nm and 1550 nm. The reason for the low absorption coefficient has been discussed in detail in this section. The absorption coefficient of SiGe and SiGeC alloys is not expected to be high enough unless a high percentage of Ge is present. To provide the high absorption coefficient while staying within the SiGe system, pure Ge is the best choice. Selective epitaxial growth of pure Ge on patterned $SiO_2$/Si wafers allows the selective introduction of Ge onto the Si substrate. This makes the integration scheme illustrated in Figure 2.2 possible and provides the potential for the large scale integration of Si microphotonic technology with Si microelectronic technology. The challenge is the threading-dislocations that are almost inevitable when Ge is grown on Si. Section 2.6 will evaluate the effect of threading-dislocations on photodetector performance. It will be shown that threading-dislocations are not fatal to the performance of photodetectors and need not be

completely eliminated. In Chapter 3, it will be demonstrated that it is possible to grow Ge on Si with no threading-dislocations by a combination of cyclic thermal annealing and selective area growth.

## 2.6 Effect of threading-dislocations on the performance of photodiodes

### 2.6.1 Leakage current and noise

Leakage current, or dark current, is the current that flows through a photodiode even without the injection of photons. Leakage current is, therefore, a source of noise in an optical receiver. Noise in a receiver can degrade signal-to-noise (S/N) ratio and increase bit-error-rate (BER). Leakage current is also a source of power dissipation. For large scale integration, it is necessary to control power dissipation due to leakage current. This section first discusses the sources of leakage current and the correlation between threading-dislocation density and leakage current. Next a comparison of the leakage current of Ge and InGaAs photodiodes is presented. At the end of this section, the sensitivity analysis of a photodiode receiver will be presented. It will be shown that at high bit-rate, leakage current is not a dominant source of noise. The reason for reducing leakage current is therefore limited to the need to control power dissipation.

A thorough discussion of leakage current in photodiodes has been presented by Pearsall and Pollack [70]. The sources of leakage current are: (1) diffusion current, (2) bulk generation current, (3) surface leakage current and (3) tunneling current. Diffusion current is due to the diffusion of thermally-generated minority-carriers into the depletion region from the surrounding undepleted p and n region [71]. Bulk generation current is due to the defect-assisted thermal generation in the depletion region [72]. Surface leakage is caused

by carrier generation at the surface depletion region close to the metallurgical p-n junction [73]. Tunneling current is due to band-to-band transitions or trap assisted transitions at high electric field and is typically important for avalanche photodetectors. For photodiodes made from heteroepitaxial layers that have a high density of threading-dislocations, bulk generation is the most important source of leakage current. For photodiodes that have unpassivated p-n junctions, surface leakage current is also important. Passivation of Ge epilayer surface for the control of surface leakage current will be discussed in Chapter 5.

Dislocations are known to increase leakage current of p-n junction diodes. For example, using in-situ transmission-electron-microscopy (TEM) studies, Ross and co-workers have reported an increase in leakage current as the density of misfit dislocations in a metastable SiGe p-n junction diode was increased due to thermal annealing [74]. Kozodoy and co-workers also showed that threading-dislocations in GaN p-n junction diodes can cause an increase in leakage current [75]. The correlation between threading-dislocation density and leakage current in SiGe p-i-n diodes has been studied by Giovane and co-workers [76]. They showed that the contribution of threading-dislocations on the leakage current can be estimated knowing the number of traps per length of dislocations ($N_{TD}$) and calculating the defect state density ($N_T$) using the following formula:

$$N_T = N_{TD} \cdot N_D \tag{2.3}$$

where $N_D$ is the threading-dislocation density. If the capture cross section ($\sigma_n$) of defect states related to threading dislocations is known, the minority-carrier lifetime can be estimated by

$$\tau = \frac{1}{\sigma_n \cdot \upsilon_{th} \cdot N_D \cdot N_{TD}} \quad (2.4)$$

where $\upsilon_{th}$ is the thermal velocity. Knowing the minority-carrier lifetime, the leakage current density due to carrier generation at threading-dislocation related defect states can be estimated by the following:

$$J_{gen} = \frac{q \cdot n_i \cdot w}{\tau} = q \cdot n_i \cdot w \cdot \sigma_n \cdot \nu_{th} \cdot N_D \cdot N_{TD} \quad (2.5)$$

where $W$ is the depletion width, and $n_i$ is the intrinsic carrier concentration. Using Equations 2.3, 2.4 and 2.5, leakage current in a Ge photodiode with threading-dislocations can be evaluated if the capture cross section and defect density per dislocation length is known. Currently there are no reports on these values. For a rough estimate, values for Si and SiGe alloys can be used. From Kimerling and co-workers, in Si $N_D = 10^6 cm^{-1}$ [77] [78]. The effective capture cross section for threading-dislocations in $Si_{0.7}Ge_{0.3}$ alloys has been measured using deep-level-transient-spectroscopy (DLTS) ($\sigma_n = 4 \times 10^{-12} cm^2$ ) [79]. Using these values and $\upsilon_{th} = 1.17 \times 10^7 (cm/s)$ at 300K, $n_i = 2.4 \times 10^{13} cm^{-3}$ for Ge, the leakage current due to carrier generation at defect states related to threading-dislocations can be calculated:

$$J(A/cm^2) = 1.8 \times 10^{-4} (A/cm) \cdot w \cdot N_D \quad (2.6)$$

This calculation shows that the leakage current per length of threading dislocation in pure Ge is 180 μA/cm. Assuming that the depletion width is 1 μm and the threading-dislocation density is $2 \times 10^7$ $cm^{-2}$, the leakage current density calculated using Equation 2.6 is 360 $mA/cm^2$. This value is much larger compared to that reported in reference 59 (50 $mA/cm^2$) [59]. This suggests that the activity of threading-dislocations in

Ge can be quite different from that in SiGe alloy. Calculation by Equation 2.6, therefore, should be used as an upper limit in the estimation of leakage current and noise.

An application of Equation 2.5 and a comparison of the leakage current in Ge and $In_{0.53}Ga_{0.47}As$ is in order here. The purpose is to compare the difference in leakage current here and later estimate how this difference affects the noise in a photodetector receiver. We will use the following equation for the comparison of leakage current in p-i-n photodiodes.

$$J_{leakage} = J_{diff} + J_{gen} = qn_i^2\left(\frac{D_p}{N_d W_C} + \frac{D_n}{N_a W_C}\right) + \frac{q \cdot n_i \cdot w}{\tau_n} \tag{2.7}$$

where $D_p$ is the diffusion coefficient of holes, $D_n$ is the diffusion coefficient for electrons, $N_d$ is the doping concentration in the heavily doped n-region, $N_a$ is the doping concentration in the heavily doped p-region and $W_C$ is the distance from the edge of the intrinsic region to the interface between the heavily doped region and the metal contact. For the comparison of the leakage current, the most important parameter is the ratio of the intrinsic carrier concentration,

$$\frac{n_{i-Ge}}{n_{i-InGaAs}} \tag{2.8}$$

While other parameters depend on the materials quality and doping concentration, the intrinsic carrier concentration is intrinsic to the material. The intrinsic carrier concentration ($n_i$) can be described by the following formula [72]

$$n_i = 4.9 \times 10^{15}\left(\frac{m_{de}m_{dh}}{m_0^2}\right)^{3/4} T^{3/2} e^{-E_g/2kT} \tag{2.9}$$

where $m_{de}$ is the density-of-state effective mass of electrons, $m_{dh}$ is the density-of-state effective mass of holes, $m_0$ is the electron rest mass, $T$ is the temperature, $E_g$ is the band gap and $k$ is the Boltzmann constant. For Ge, at room temperature, $m_{de}= 0.226$, $m_{dh}= 0.292$ and $E_g= 0.66eV$. For $In_{0.53}Ga_{0.47}As$, $m_{de}= 0.046$, $m_{dh}= 0.224$ and $E_g= 0.748eV$[80]. Figure 2.7 shows the calculated $\frac{n_{i-Ge}}{n_{i-InGaAs}}$ as a function of temperature. The intrinsic carrier concentration of Ge is 50 times larger than that of InGaAs at room temperature. This is due to the smaller band gap and much heavier electron effective mass of Ge. In well designed InGaAs or Ge p-i-n photodiodes with low defect density the leakage current is limited by the diffusion current. In these cases, the leakage current of a Ge photodiode can be about 2500 times higher than that of an InGaAs photodiode. In cases where the defect density is high and the generation current is larger than the diffusion current, the carrier lifetime for both Ge and InGaAs would be in the similar range. Assuming that the depletion width is the same, the leakage current of a Ge photodiode would be about 50 times larger than that of an InGaAs photodiode. Combining the lower leakage current density with the much higher absorption coefficient of $In_{0.53}Ga_{0.47}As$ at 1300 and 1550 nm, $In_{0.53}Ga_{0.47}As$ is a much better material for making near-infrared photodiodes.

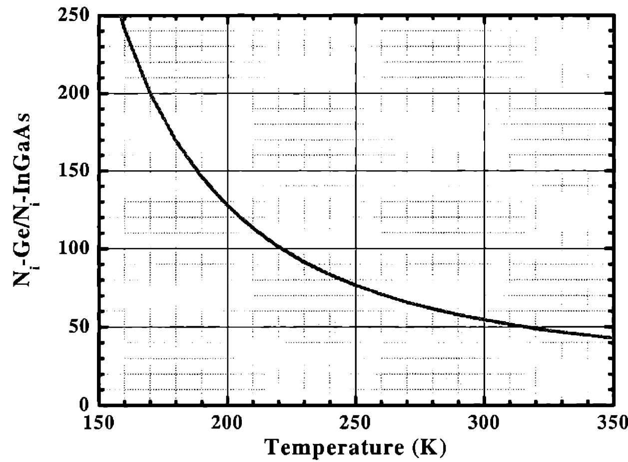



**Figure 2.7:** The ratio of Ge intrinsic carrier concentration to the InGaAs intrinsic carrier concentration as a function of temperature.

We are now ready to discuss the effect of leakage current on noise, bit-error-rate and sensitivity. Complete discussions of the sensitivity of photodiode receivers can be found in several book chapters [81] [82]. Here, only the main conclusion is presented. Bit-error-rate (BER) is defined as the ratio between the number of errors that occur in the transmission of information divided by the number of bits that are transmitted. Receiver sensitivity is the optical power required at the optical input of a photodiode receiver to achieve a certain BER (typically $10^{-9}$ or $10^{-12}$). With increasing noise level, the S/N decreases and the BER increases. To maintain the same BER, the required optical power increases and the receiver sensitivity degrades (that is, higher optical power is needed to achieve the same BER). A photodiode receiver typically has two devices: a p-i-n photodiode for photon detection and a field-effect-transistor (FET) for signal amplification. The sources of noise are shot-noise ($\langle i_T^2 \rangle$), thermal-noise ($\langle i_R^2 \rangle$), channel-noise ($\langle i_c^2 \rangle$), and $1/f$ noise ($\langle i_f^2 \rangle$). At low bit-rate, shot-noise is important:

$$\langle i_T^2 \rangle \propto 2q(I_g + I_D)B \tag{2.10}$$

where $I_g$ is the FET gate leakage, $I_D$ is the dark current (or leakage current) of the photodiode and $B$ is the bit-rate. At high bit-rate, the channel noise is important

$$\langle i_c^2 \rangle \propto C_T^2 B^3 \tag{2.11}$$

where $C_T$ is the total input capacitance of the photodiode and the amplifier FET. Because the channel-noise is proportional to $B^3$, channel-noise is the dominant noise source at high bit-rate. Figure 2.8 shows a typical calculated sensitivity versus bit-rate plot. The detail of the sensitivity to bit-rate plot depends on the characteristics of the photodiode and the FET amplifier. Figure 2.8 should only be viewed as a way to improve understanding.

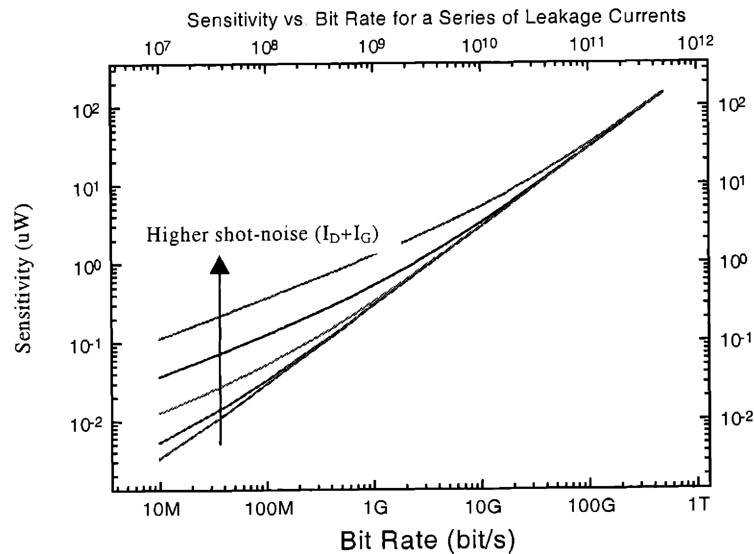



**Figure 2.8:** Typical behavior of sensitivity versus bit-rate plot of a p-i-n receiver. At high bit-rate the contribution of shot-noise become less important.

An important feature of Figure 2.8 is that the effect of shot-noise on sensitivity is less significant at higher bit-rate. This is because the channel-noise is proportional to $B^3$. Therefore, one can expect that leakage current from a photodiode plays a less significant role as the speed of the optical link increases. As concluded by Bowers and Burrus, for a p-i-n/FET receiver with a leakage current of 10 μA, the leakage current causes less than 1 dB reduction in sensitivity [37]. Also, as pointed out by Pearsall, Pollack and Forrest, it is more important to reduce the capacitance of a photodiode at high bit-rate rather than controlling leakage current [70] [82]. One way to reduce the photodiode capacitance is to reduce the area of the photodiode. Reducing the area of a photodiode also has the effect of reducing the total leakage current. From Equation 2.6, the upper bound of leakage current density in a Ge photodiode with a depletion width of 1 μm and a threading-dislocation density of $2 \times 10^7$ $cm^{-2}$ is 360 mA/$cm^2$. A typical high speed photodiode has a diameter of 100 μm. The total leakage current is 28 μA. Ge epilayers on Si with much lower threading-dislocation densities have been demonstrated and will be discussed in Chapter 3 [56]. Measured leakage current density is also much lower than our calculated upper bound. We can therefore conclude that the leakage current in a Ge photodiode made from Ge epilayers grown on Si is low enough for making sensitive high-speed p-i-n receiver. Threading-dislocations are not a major source of noise and sensitivity degradation. The reason for reducing leakage current in Ge photodiodes used in Si microphotonics systems is therefore to control the power dissipation rather than to improvement the sensitivity.

### **2.6.2** Carrier Mobility and Speed

The speed of a photodetector is controlled either by RC delay or carrier transit time through the depletion region; whichever is slower. For a well designed photodetector, the

speed is limited by the carrier transit time ($t_r$). The 3-dB frequency (that is, speed) of a photodetector is given by

$$f_{3dB} = \frac{2.4}{2\pi t_r} \cong \frac{0.4 v_d}{W} \tag{2.12}$$

where $v_d$ is the drift velocity of photo-generated carriers in the depletion region and $W$ is the depletion width [72]. The velocity of the photo-generated carriers can be related to the carrier mobility ($\mu$) by the following model [71]

$$v_d = \mp \frac{\mu\varepsilon}{1 + \left|\frac{\mu\varepsilon}{v_{sat}}\right|} \tag{2.13}$$

where $\varepsilon$ is the electric field and $v_{sat}$ is the saturation drift velocity of the carriers. Figure 2.9 shows the relationship between drift velocity and electric field for Ge with electron mobility of 3900 $cm^2/V$-s and hole mobility of 1900 $cm^2/V$-s calculated from equation 2.13. Figure 2.9 demonstrates that, at high electric field, both electrons and holes travel at the saturation drift velocity. At low electric field, the drift velocity is almost proportional to the electric field and Equation 2.13 is reduced to

$$v_d = \mp\mu\varepsilon \tag{2.14}$$

For carriers with lower mobility, higher electric field is needed to obtain saturation drift velocity. Since threading-dislocations are known to reduce carrier mobility, photodiodes made from materials grown by heteroepitaxy might not provide high enough speed performance. In the rest of this section, the effect of threading-dislocations on carrier mobility are reviewed and the possibility of making high speed photodiodes using dislocated materials is considered. It will be shown that threading-dislocations have very little effect on room-temperature mobility and speed.

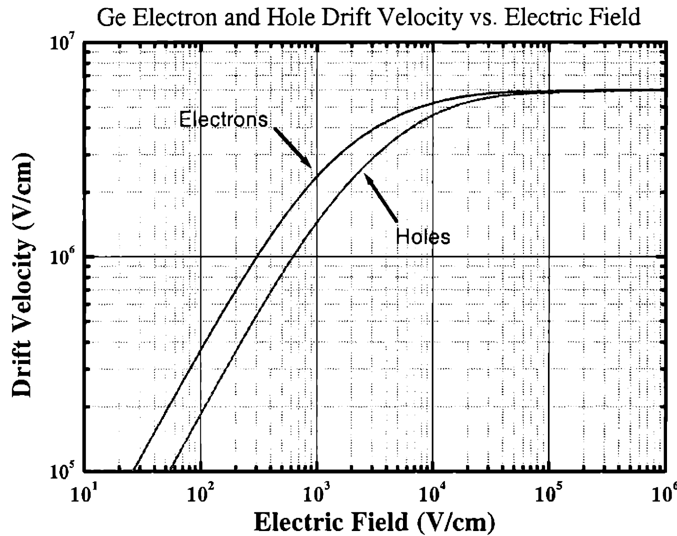



**Figure 2.9:** Carrier drift velocity of electrons and holes in Ge calculated using equation 2.13.

The effect of dislocations on the carrier mobility has been reported in the early days of semiconductor research [83] [84] [85]. It was thought that dislocations with edge component act like acceptor centers. Dislocation related acceptor centers can capture electrons and become negatively charged. Around the dislocation line, there is a space-charged region that scatters carriers and reduce carrier mobility. Similar models have been used to explain the effect of threading-dislocations on carrier mobility in III-V compounds grown on Si [86], SiGe systems on Si [87] [88] [89] [90], and GaN on $Al_2O_3$ [91] [92] [93]. For the purpose of integrating near-infrared photodiodes on Si, the work on III-V materials grown on Si and the study of SiGe systems are relevant. Bartels and co-workers found that InP and GaAs grown directly on Si have high densities of threading dislocations ($1\sim2\times10^8$ cm$^{-2}$). At room temperature, they found that carrier mobility is almost unaffected by dislocation scattering [86]. Electron mobility as high as

3600 $cm^2/V$-s (InP) and 3800 $cm^2/V$-s (GaAs) were reported. Ismail reported that in SiGe systems, electron mobility becomes sensitive to threading-dislocations when their density exceeds $3x10^8$ $cm^{-2}$ [89] [90]. The room-temperature electron mobility is reduced by 10% at a threading-dislocation density of $3x10^8$ $cm^{-2}$ and reduced by 50% at a threading-dislocation density of $10^{11}$ $cm^{-2}$. All these reports show that threading-dislocations below the level of $10^8$ $cm^{-2}$ do not significantly affect electron mobility. Measurement of electron mobility in Ge grown directly on Si also supports this finding [59].

It is interesting to estimate the effect of reduced carrier mobility on the speed of photodiodes. The goal of this analysis is to show that even with a reduction in carrier mobility, it is still possible to make high speed photodiodes. The hole mobility of Ge is 1900 $cm^2/V$-s. Assuming a 90% reduction in hole mobility, this would give a hole mobility of 190 $cm^2/V$-s. This kind of reduction in mobility is larger than experimentally reported reduction reviewed earlier. Assume the depletion width is about 1 μm and the applied voltage is 1 V, the electric field is $10^4$ V/cm. Using equation 2.13, we have a hole drift velocity of $1.4x10^6$ cm/s. Using equation 2.12, the 3-dB frequency is 5.8 GHz. The 3-dB frequency of a p-i-n photodiode as a function of depletion width and hole mobility is shown in Figure 2.10. This calculation shows that even with a 90% reduction in hole mobility, Ge photodiodes running at GHz are still possible. We can conclude that the effect of threading-dislocations on mobility does not seriously degrade the speed of photodiodes.

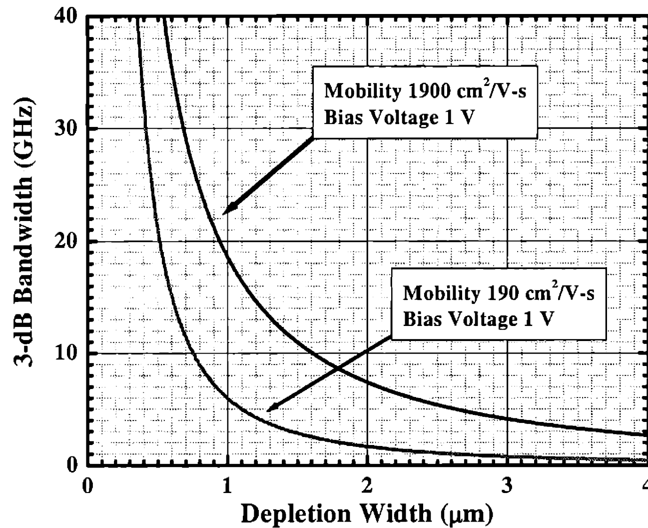



**Figure 2.10:** 3-dB bandwidth of a p-i-n junction photodiode as a function of depletion width, mobility and bias voltage.

### **2.6.3** Device reliability

Dislocations are known to cause sudden failure of laser diodes [94] [95]. The mechanism for this sudden failure has been attributed to recombination enhanced defect reactions [96]. Since a photodiode's device structure is similar to that of a laser diode, it is important to consider the effect of threading-dislocations on photodiode reliability. If threading-dislocations are fatal to photodiode operation as suspected by Lafontaine and co-workers [27], threading-dislocations should be completely eliminated. On the other hand, if threading-dislocations do not cause sudden failure of photodiodes, some residual threading-dislocations can be tolerated.

The reliability of photodiodes has been reported [97] [98] [99] [100]. There has been little evidence of sudden failure of photodiodes. Failure of photodiodes, rather, is characterized

by a slow increase in leakage current. When the leakage current becomes so high that the S/N ratio is too low, the BER can become so high that the optical communication link ceases to function [99]. Several mechanisms account for the failure of photodiodes [100]: (1) Local avalanche breakdown at the p-n junction at the surface. (2) Electrode reaction the with semiconductor that shorts the p-n junction. (3) Breakdown of dielectric film between the electrode and the semiconductor. (4) Microplasma generation at current concentration sites related to defects. Among the four possible failure mechanisms of photodiodes, microplasma generation is most likely related to threading-dislocations. As experimentally demonstrated in InP avalanche photodiodes, recombination centers (related to threading-dislocations) revealed by electron-beam-induced-current (EBIC) imaging at 0 V become a strong generation site at high reverse bias (-30 V) [97]. These recombination centers are found to be related to Fe decorated dislocations. Defects that generate such a microplasma can cause current concentration. When the current density is too high, the p-n junction can be destroyed by local melting.

Based on the above discussion, decorated threading-dislocations can be possible sites of photodiode failure at high reverse voltage. To avoid failure related to microplasmas, it is important to prevent contamination of the depletion region of photodiodes. This can be easily achieved in epitaxially grown devices. Another possibility is to design the p-n junction so the current flows at almost vertical angle to the threading-dislocation lines. This prevents the local concentration of current flow through threading-dislocation lines. However, the most effective way to prevent failure might be to design high performance photodetectors that operate at small bias voltage. It will be shown in chapter 4 that high performance Ge photodiodes operating at low bias voltage can be integrated on Si.

Threading-dislocations are, therefore, not fatal to the operation of photodiodes and need not be completely eliminated.

## 2.7 Design of microphotonic photodiodes

Based on the previous discussion, photodiodes for Si microphotonic technology should be designed with the following guidelines. These guidelines are relevant to the design of both normal-incidence photodiodes and waveguide photodiodes.

1. High quantum efficiency: To achieve high quantum efficiency, we must have high waveguide/photodiode coupling efficiency and use materials with high absorption coefficient at 1300 nm and 1550 nm. A coupling efficiency of 100% is desirable. An absorption coefficient in the range of high $10^3$ cm$^{-1}$ to low $10^4$ cm$^{-1}$ is necessary. An absorption coefficient higher than $10^5$ cm$^{-1}$ might result in lower quantum efficiency due to surface recombination.
2. High speed: To achieve high speed, we should make sure that the distance that photogenerated carriers need to travel is short. For a speed of 1 Gbit/s at a bias voltage of 0.5 V, the distance should be smaller than 4 μm. For a speed of 10 Gbit/s at the same low bias voltage, the distance should be smaller than 1 μm. We also need to design photodiodes with small capacitance so that the speed is not limited by RC delay.
3. Low leakage current: To achieve low leakage current, we must have small depletion volume, good surface passivation and low defect density. For high speed optical link in the Gbit/s range, a total leakage current of 10 μA is low enough for a discrete photodiode. For large scale integration of photodiodes, it is necessary to make the leakage current as low as possible to reduce power dissipation.
4. High reliability: To achieve high reliability, we must design photodiodes that can operate at low bias voltage. We also need to improve materials quality. It is especially important to make sure that any dislocations left in the photodiode are not decorated by metal contaminant.

5. High Si microelectronic integration capability: To achieve high level integration, the photodiode must be small and the technology must not cause cross contamination problems in Si processing.

The epitaxial growth of high quality Ge epilayers with threading-dislocation density as low as $8 \times 10^{6}\ cm^{-2}$ with high absorption coefficient at 1300 nm and 1550 nm will be discussed in Chapter 3. It will be also shown that Ge mesas with no threading-dislocations can be grown on Si by selective epitaxy. Performance of Ge photodiodes made with Ge epilayers grown on Si will be discussed in Chapter 4. It will be shown that highly efficient Ge photodiodes can be integrated on Si using epi-technology described in Chapter 3. Chapter 5 will discuss the passivation of Ge surface. It will be shown that passivation of Ge can be done by thermal oxidation of Si epilayer grown on Ge.

# Chapter 3

# Direct epitaxial growth of high quality Ge epilayers on Si

## 3.1 Overview

This chapter discusses the epitaxial growth of Ge epilayers on Si. A literature review of the work in the field of threading-dislocation reduction is first presented. That is followed by a discussion of the experimental procedure for the deposition of high quality Ge epilayers on Si. Finally, the effect of several processing parameters on the threading-dislocation density in Ge grown on Si is discussed. This chapter provides conclusive evidence that high-quality Ge epilayers with low threading-dislocation densities can be grown directly on Si without the use of buffer layer structures.

## 3.2 Introduction

Heteroepitaxy of Ge on Si is a research topic of significant technological importance. A particularly important application is the integration of Ge photodetectors with Si or $Si_3N_4$ waveguides and Si based electronic devices for the distribution and detection of optical signal at wavelengths of 1300 nm and 1550 nm on Si. Silicon-based optoelectronic integrated circuits (OEIC), or Si microphotonic systems, offer a potential solution to the limitation of metal interconnect. High-quality Ge epilayers on Si can also be used for the integration of Ge-based transistors on Si. The epitaxial growth of high-quality Ge on Si, however, is difficult due to the 4% lattice mismatch between Ge and Si. This lattice mismatch causes two major problems when Ge is epitaxially grown on Si: (1) the introduction of high densities of misfit-dislocations and threading-dislocations in the

epilayer, and (2) high surface-roughness due to island growth. High surface-roughness causes difficulties in process integration. High densities of threading-dislocations can increase the leakage current of p-n junctions. In this chapter, a technology for the heteroepitaxy of high-quality Ge epilayers on Si with low surface-roughness and low threading-dislocation density is presented. This technology allows the selective epitaxial growth of Ge directly on Si wafers with patterned $SiO_2$ mask and therefore provides an opportunity for large scale integration of Ge photodiodes with Si microelectronics.

### **3.2.1** Origin of threading-dislocations

In lattice mismatched systems such as the Ge/Si system, misfit-dislocations develop during the growth to relax the lattice mismatch between the Ge epilayer and the Si substrate. These misfit-dislocations relax the lattice mismatch between Ge and Si by introducing extra half planes of atoms. These misfit-dislocations are confined to the interface between the Ge epilayer and the Si substrate and are energetically stable when the Ge thickness is larger than the critical thickness for misfit-dislocation formation [101] [102] [103] [104].

Threading-dislocations are the by-products of the formation of misfit-dislocations and do not relax strain due to lattice mismatch. Threading-dislocations are left in the epilayers because dislocations cannot end in a crystal and have to either form a loop or terminate at a free surface. Since the epilayer surface is the nearest free surface to the epi-substrate interface, these threading-dislocations typically thread from the epi-substrate interface to the epilayer surface. Since devices are usually built close to the epilayer surface, these threading-dislocations can easily affect the performance of devices built on epilayers.

Therefore, the reduction of threading-dislocation densities in epilayers grown on lattice mismatched substrate is important.

### 3.2.2 Methods for threading-dislocation reduction

Several methods have been developed for the reduction of threading-dislocation densities in lattice-mismatched epilayers:

1. Growth of thick constant composition buffer layer: Sheldon and co-workers found that in InAs/GaAs, GaAs/Ge/Si, GaAs/InP, and InAs/InP heterostructures, the threading-dislocation density is inversely proportional to the epilayer thickness [105]. Tachikawa and Yamaguchi later showed that for film thickness below 10 μm, the threading-dislocation density is inversely proportional to film thickness [106]. For film thickness larger than 50 μm, they found that the threading-dislocation density is exponentially proportional to the film thickness. The mechanism for the reduction of threading-dislocations is thought to be the annihilation and coalescence of dislocations.
2. Growth of graded buffer layer: Fitzgerald and co-workers demonstrated that by growing SiGe relaxed graded buffer layers on Si at high temperature, high quality relaxed epilayers with 0~100% Ge can be grown on Si [107] [108] [109]. Their idea is that by preventing massive dislocation nucleation, interaction and multiplication events that increase threading-dislocations can be reduced. This is done by staying within the low mismatch region with the introduction of each grading layer. Each grading layer therefore introduces a small number of new dislocations while providing the strain to glide dislocations out of the edge of the substrate.
3. Strained layer superlattices: Strained layer superlattices are essentially several low-misfit layers on top of each other. The idea is that strain can act as a barrier to the vertical movement of threading dislocations [110].
4. Low temperature Si buffer layer: For the heteroepitaxial growth of SiGe on Si, several groups have reported that the insertion of a low-temperature

molecular-beam-epitaxy (MBE) grown Si buffer can dramatically reduce the threading-dislocation density in the SiGe layer. The mechanism for this improvement is not clear [111] [112] [113] [114] [115]. It has been suggested that point defects in a low-temperature Si buffer layer can trap the dislocations [116].

5. Growth interruption and cyclic thermal annealing: Several groups have reported that growth interruption and in-situ annealing can reduce threading-dislocation densities in GaAs grown on Si [117] [118] [119]. Cyclic thermal annealing has also been reported to be effective in reducing threading-dislocation densities.
6. Growth on patterned substrates: Epitaxial growth on patterned substrates has been shown to reduce the overall threading-dislocation density. In small misfit systems, epitaxial growth on small patterns reduce the misfit-dislocation densities and dislocation interactions and therefore the threading-dislocation densities [120] [121]. Growth in small areas also reduces the distance the threading-dislocations need to travel before they reach the side edges of the epilayer [122] [123].
7. Epitaxial necking, conformal growth, epitaxial lateral overgrowth and pendeo-epitaxy: If threading-dislocations thread to the epilayer surface at a certain direction, it is possible to reduce the threading-dislocation density by blocking threading-dislocations using amorphous materials such as $SiO_2$ and $Si_3N_4$. Epitaxial necking [124] [125], conformal growth [126], epitaxial lateral overgrowth [127] [128], and pendeo-epitaxy [129] are methods based on this idea.
8. Compliant substrate: If threading-dislocations can thread into the substrate rather than into the epilayer, epilayer with essentially no threading-dislocations can be obtained. This has been reported by the application of the compliant substrate technology [130] [131]. By introducing a thin-compliant layer on the substrate by wafer bonding or by thinning of SOI wafer, several research groups have reported epilayers with very low threading-dislocation densities [132] [133] [134].

As discussed in Chapter 2, for large-scale integration of Ge photodetectors on Si, a technology for selectively introducing high-quality Ge epilayers on Si is necessary. For

simple process integration with Si microelectronic technology, it is ideal to reduce threading-dislocations in small selectively-grown Ge mesas by a simple thermal annealing process. It will be demonstrated in Sections 3.3 and 3.4 that this can be accomplished.

### **3.2.3** High lattice-mismatched systems: Ge/Si, GaAs/Si

Heteroepitaxy of Ge on Si has been studied by several groups. Tsaur and co-workers found that by using vacuum-evaporation to deposit Ge on Si, they could deposit smooth Ge films on Si by heating the substrate to 550°C [135]. However, increading the deposition temperature to 650°C resulted in increased roughness of the Ge film. Their best threading-dislocation density was about $10^8$ $cm^{-2}$ as measured by TEM. Twins were also found in the Ge film. Kuech and co-workers reported the growth of Ge on Si by chemical-vapor-deposition (CVD) and physical-vapor-deposition (PVD) at a substrate temperature of 500°C [136] [137]. However, high densities of threading-dislocations and twins in the Ge films were reported. Ishii and co-workers reported the selective area growth of Ge on Si by CVD using $SiO_2$ as a mask material [138]. Fukuda and co-workers reported that in-situ thermal annealing at 680°C can reduce threading-dislocations in Ge grown on Si by MBE at 600°C [139] [140]. Baribeau and co-workers reported the growth of Ge on Si with threading-dislocation density as low as $5 \times 10^6$ $cm^{-2}$ using MBE growth at 610°C and post-growth cyclic thermal annealing at 700°C [141] [142]. They also reported that Ge on Si with similar quality can be obtained by a two-step MBE growth procedure without thermal annealing. The first layer was grown at 500°C (~200 nm) and the second layer was grown at 700°C (~1.5 μm). They reported a threading-dislocation density of $5 \times 10^6$ $cm^{-2}$ as measured by the FWHM of the Ge (004) Bragg reflection rocking curve. Rapid thermal chemical vapor deposition of Ge on Si has been reported by Ozturk and co-workers [143]. Their experiment showed that the Ge CVD process is

surface reaction limited at temperatures below 450°C and is mass transport limited at temperature above 450°C. Using UHV/CVD, Cunningham and co-workers reported similar growth behavior [144]. They also reported that at growth temperatures below 350°C, Ge growth occurs in a two-dimensional, layer-by-layer mode. Above 375°C, growth occurs as three-dimensional island growth [145]. Later, they also reported non-selective Ge growth on $SiO_2$ by UHV/CVD with the flow of $GeH_4/B_2H_6$/He mixture [146]. Kvam and Namayar reported the growth of Ge on Si by flowing $GeCl_4$ at growth temperatures from 985°C to 1060°C [147]. This growth temperature is higher than the melting temperature of Ge (939°C). They reported a threading-dislocation density of $8 \times 10^6$ $cm^{-2}$ measured by plan-view TEM. Malta and co-workers reported the MBE growth of Ge on Si at a growth temperature of 900°C [148] [149]. The threading-dislocation density measured by etch-pit-density counting (EPD) is in the low $10^5$ $cm^{-2}$ range. It is clear from these reports that none of the research done till now provides a systematic report on the selective area growth of Ge on Si with low threading-dislocation density. There has also been no report on the study of threading-dislocation densities in UHV/CVD grown Ge on Si. UHV/CVD is the tool used for epitaxial growth in the SiGe BiCMOS technology.

A system that is very similar to the Ge/Si heteroepitaxial system is the heteroepitaxial growth of GaAs on Si. The lattice mismatch between GaAs and Si is also about 4%, which is very similar to that between Ge and Si. A review of the work in the heteroepitaxy of GaAs on Si is therefore very helpful in understanding the Ge/Si system. A large number of papers have been written regarding the heteroepitaxy of GaAs on Si. Many methods have been applied to reduce threading-dislocation densities in GaAs grown on

Si [150] [151] [152] [153]. Here we focus on summarizing the reduction of threading-dislocations in GaAs on Si by thermal-annealing processes.

Fan and co-workers reported the reduction of threading-dislocations in GaAs grown on Si by the cyclic interruption of the vapor phase growth process. During the interruption, the samples were cooled down to room temperature and heated back to the growth temperature [154]. The GaAs was grown on a Si wafer covered with 0.15 μm of Ge buffer layer. They suggested that the thermal mismatch between GaAs and Si during temperature-cycling can cause stress-induced dislocation movement and form dislocation loops. By repeating the process several times, most of the threading-dislocations form loops and the top epilayer surface can be free of threading-dislocations. However, they did not report the final threading-dislocation density. Early reports of GaAs growth on Si typically included a Ge buffer layer. Akiyama and co-workers reported the direct epitaxial growth of GaAs on Si by a two-step process [155]. In this two-step process, GaAs growth was first initiated at a low temperature of 450°C. After a suitable thickness of LT-GaAs was grown, the temperature was raised to conventional GaAs growth temperature. Lee and co-workers reported the growth of GaAs on Si by a two-step MBE growth procedure and the reduction of threading-dislocations by post-growth thermal-annealing [156]. Using cross-sectional TEM, they showed that post-growth annealing of GaAs grown on Si at 850°C under arsenic overpressure for 15 minutes can reduce the threading-dislocation density from about $10^9$ cm$^{-2}$ to $10^7$ cm$^{-2}$ range. Okamoto and co-workers reported high quality GaAs on Si obtained by a combination of the application of in-situ thermal cycling (between 300°C and 900°C) and the insertion of an InGaAs/GaAs superlattice [118]. They reported etch-pit-density (EPD) of 1.4 x $10^6$ cm$^{-2}$ by KOH etching. Itoh and co-workers later reported that similar EPD (2 x $10^6$ cm$^{-2}$) can be obtain in GaAs grown on Si by

in-situ thermal-annealing along [157]. In a series of papers, Yamaguchi and co-workers also demonstrated the reduction of threading-dislocation density in GaAs grown on Si by in-situ cyclic thermal-annealing [119] [158] [159]. Their measurement of threading-dislocation density was done by EPD using KOH etching. Their EPD measurements were calibrated by plan-view TEM. They showed that better GaAs quality can be obtained by increasing annealing temperature. They proposed a chemical reaction-kinetic model to explain their results. The lowest EPD reported was $2\sim3\text{x}10^6$ $cm^{-2}$. Similar results have also been reported by several other research groups [160] [161] [162] [163] [164]. One way to further improve the materials quality is to combine selective area growth and cyclic thermal-annealing. Yamaguchi and co-workers reported that an average EPD lower than $10^6$ $cm^{-2}$ in selectively grown GaAs square mesas (10 μm width) can be achieved after cyclic thermal-annealing [165]. Chand and Chu reported that post growth patterning and annealing can eliminate dark line defects in patterns smaller than 15 μm x 15 μm [166]. Karam and co-workers also reported similar reduction in threading-dislocation density by selective area growth and thermal annealing [167]. A more interesting report is by Yamaichi and co-workers [168]. They reported that by patterning $SiO_2$ deposited on GaAs/Si, similar reduction in threading-dislocation density can be achieved after annealing. Their optical microscopic images showed that most of the threading-dislocations are gettered at the edge of the $SiO_2$ pattern.

Based on the above discussion, it appears that thermal annealing combined with strained-layer superlattice and patterning (or selective area growth) can produce GaAs on Si with threading-dislocation densities as low as $10^6$ $cm^{-2}$. Most of these reports relied on EPD (by KOH etching) for measurement of threading-dislocation densities. EPD by KOH

etching, however, has not been know to accurately reveal the threading-dislocation density. Using EPD by KOH etching, threading-dislocation densities as low as $10^3$ cm$^{-2}$ in GaAs grown on Si have been reported by Fischer and co-workers [169] [170]. The accuracy of these reports was later questioned by other research groups [150]. For example, Ishida and co-workers found that there is a discrepancy between EPD (~$10^3$ cm$^{-2}$) and plan-view TEM counted threading-dislocation densities (~$10^7$-$10^8$ cm$^{-2}$) [171]. They showed that the results could be reconciled by including some small etch-pits that only show up in optical microscopy under high magnification. This report demonstrated that it is very important to verify EPD measurement of threading-dislocation densities carefully. Shimizu and co-workers did a series of experiments and measured the threading-dislocation densities in GaAs on Si by both EPD and plan-view TEM [172]. In the range of $10^6$~$10^7$ cm$^{-2}$, they found that EPD typically gives measurements about a factor of two less than that by plan-view TEM. Using a model developed by Stirland and co-workers, they attributed this difference to the resolution of the imaging method of EPD [173]. Similar results have also been reported by Stirland [174]. Based on the discussion above, we conclude that GaAs on Si with threading-dislocation densities in the $10^6$ cm$^{-2}$ range can be obtained and thermal-annealing is effective in reducing threading dislocations. Thermal-annealing, therefore, should be considered as a way of achieving high quality Ge epilayers on Si. Also, to ensure accuracy, it is very important to measure the threading-dislocation density carefully.

## 3.3 Experimental procedure

A hot wall UHV/CVD was used for Ge heteroepitaxy on Si. The base pressure of the UHV/CVD chamber is 3 x $10^{-9}$ Torr. The substrates were 4" p-type Si (001) wafers with resistivity in the range of 0.5-2 Ω–cm. For the selective area growth experiments, similar p-type Si (001) wafers were oxidized in a typical oxidation furnace and then patterned using photolithography. The oxide thickness was 1 μm. Square windows with sides ranging from 10 μm to 100 μm were etched in silicon oxide by buffered oxide etch solution (BOE). The sides of the squares were aligned to the <100> directions. Before heteroepitaxy, plane Si and patterned $SiO_2$/Si wafers were cleaned in Piranha solution ($H_2SO_4 : H_2O_2 = 3 : 1$) for 10 minutes. Next, the native oxide was removed by dipping the wafers in aqueous HF solution (HF : $H_2O$ = 1 : 5) for 15 seconds. Heteroepitaxy of Ge on Si was initiated at 350°C with a flow of 10 sccm of $GeH_4$ (15% in Ar). The total pressure during Ge heteroepitaxy was 15 mTorr. After 30 nm of Ge was deposited on Si, the furnace temperature was raised to 600°C or 900°C and approximately 1 μm of Ge was deposited on Si. Finally, the wafers were cyclically annealed between a high annealing temperature ($T_H$) and a low annealing temperature ($T_L$) in the same furnace used for the Ge epitaxy. For rapid thermal annealing (RTA) experiments, 1 cm x 1 cm square pieces were cut and annealed in a rapid thermal annealing furnace.

Samples were examined using cross-sectional TEM, plan-view TEM, atomic-force-microscopy (AFM) and etch-pit density counting (EPD). For EPD, the etchant was a mixture of $CH_3COOH$ (67 ml), $HNO_3$ (20 ml), HF (10 ml) and $I_2$ (30 mg). An optical microscope was used to image the etch-pits. We calibrated the optical-microscope magnification using a microscope stage micrometer. In cases where the resolution of the optical microscope was too low to reveal the etch-pits, AFM was

used. AFM was also used to verify the results when optical microscopes revealed no etch-pits in some selectively grown Ge sections on patterned $SiO_2/Si$. For TEM experiments, JEOL 2000FX and JEOL 2010 transmission-electron-microscopes were used. We calibrated the magnification using a diffraction grating replica. For Burgers vector analysis, the image orientation was calibrated by $MoO_3$ platelets.

## 3.4 Results and discussion

### 3.4.1 High quality Ge epilayers on Si

The wafers are specular after epitaxial growth of Ge on Si. There is no cross-hatch pattern. The root-mean square surface roughness as measured by AFM for samples grown at 600°C is about 1~2 nm. For samples grown at 900°C, the root-mean square surface roughness is about 15 nm. Cyclic thermal annealing does not increase the surface roughness much.

**Table 3.1: Annealing parameters and characterization results of samples grown by two-step UHV/CVD process with the first step at 350°C and the second step at 600°C.**

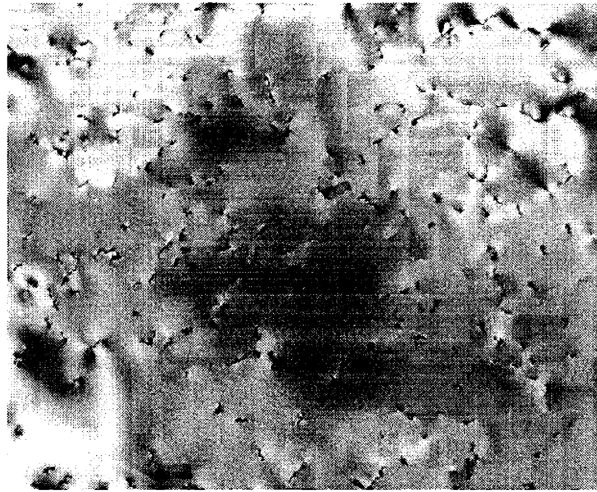
| Sample ID | 6A | 6A10 | 6A100 | 6AC |
|---|---|---|---|---|
| $T_H$(°C)/Time(min) | NA | 900°C/10min | 900°C/100min | 900°C/10min |
| $T_L$(°C)/Time(min) | NA | 100°C/10min | 100°C/100min | 100°C/10min |
| Number of Annealing Cycles | NA | 1 | 1 | 10 |
| Threading-dislocation Density by TEM ($cm^{-2}$) | $(9.5\pm0.4)x10^8$ | $(7.9\pm0.6)x10^7$ | $(7.8\pm0.5)x10^7$ | $(5.2\pm0.6)x10^7$ |
| Threading-dislocation Density by EPD ($cm^{-2}$) | $(8.7\pm0.2)x10^8$ by AFM | $(4.9\pm0.1)x10^7$ | $(4.8\pm0.1)x10^7$ | $(3.7\pm0.1)x10^7$ |
| EPD/TEM | 0.91 | 0.62 | 0.62 | 0.71 |

**Table 3.2: Annealing parameters and characterization results of samples grown by two-step UHV/CVD process with the first step at 350°C and the second step at 900°C.**

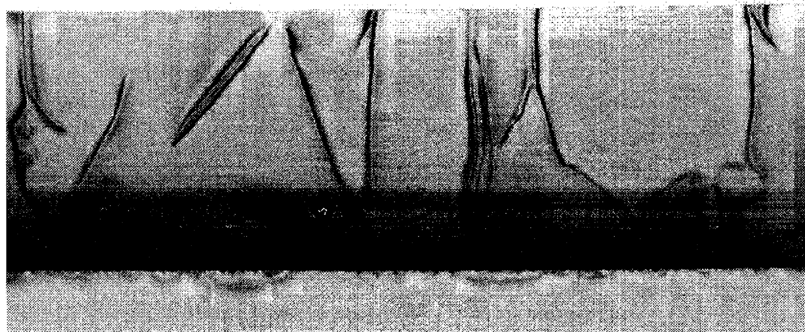
| Sample ID | 9A | 9A10 | 9A100 | 9AC |
|---|---|---|---|---|
| $T_H$(°C)/Time(min) | NA | 900°C/10min | 900°C/10min | 900°C/10min |
| $T_L$(°C)/Time(min) | NA | 100°C/10min | 100°C/10min | 100°C/10min |
| Number of Annealing Cycles | NA | 1 | 1 | 10 |
| Threading-dislocation Density by TEM ($cm^{-2}$) | $(1.6\pm0.1)\times10^8$ | $(1.3\pm0.1)\times10^8$ | $(9.8\pm0.2)\times10^7$ | $(5.7\pm0.4)\times10^7$ |
| Threading-dislocation Density by EPD ($cm^{-2}$) | $(1.0\pm0.1)\times10^8$ | $(4.2\pm0.1)\times10^7$ | $(5.8\pm0.1)\times10^7$ | $(3.9\pm0.1)\times10^7$ |
| EPD/TEM | 0.63 | **0.32** | 0.59 | 0.68 |

Table 3.1 shows a summary of the annealing parameters and measurements of threading-dislocation densities in Ge deposited on Si at 600°C. Table 3.2 shows a summary of the annealing parameters and measurements of threading-dislocation densities in Ge deposited on Si at 900°C. All samples have about 1 μm of Ge on Si. Both measurements by plan-view TEM and EPD are reported in Tables 3.1 and 3.2. For both TEM and EPD measurements, we sampled dislocations in at least twelve 10 μm x 10 μm square areas and took the average. The error-bar is the 95% confidence interval of the average. The measurements by EPD typically give smaller error-bars because it is easier to have a large number of samples by EPD. More discussion on the comparison of EPD and TEM measurements will appear in Section 3.4.5. Tables 3.1 and 3.2 clearly show that cyclically annealed samples have lower threading-dislocation densities compared to samples annealed for 100 minutes. This fact shows that increasing the number of annealing cycles is more effective in reducing threading-dislocation densities than increasing the annealing time at $T_H = 900°C$. Figures 3.1 (a) and 3.1 (b) show the plan-view and cross-sectional TEM pictures of Ge epilayers grown at 600°C. Figures 3.2

(a) and (b) show the pictures for samples grown at 600°C after annealing (sample 6AC). A comparison of Figures 3.1 and 3.2 clearly shows that annealing can reduce threading-dislocation density. Since samples grown at 600°C have lower surface roughness compared to samples grown at 900°C, experiments described in the following sections were all conducted with samples grown at 600°C.

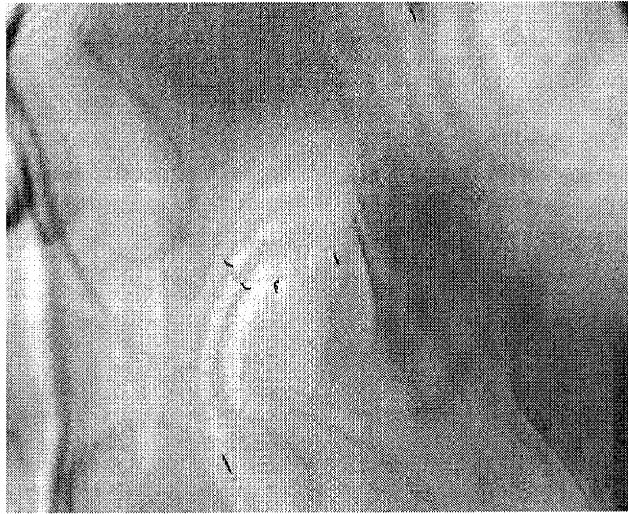


(a)



(b) 0.5μm

**Figure 3.1:** (a) Plan-view TEM and (b) cross-sectional TEM pictures of Ge epilayers grown at 600°C.



(a)

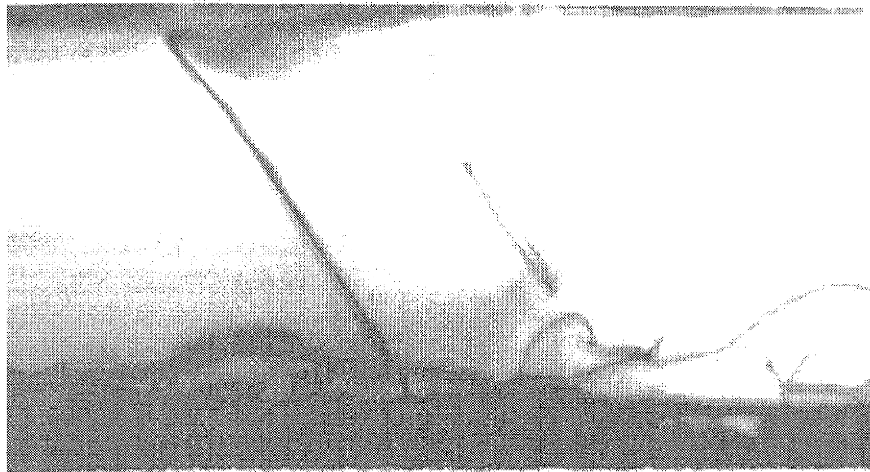



**Figure 3.2:** a) Plan-view TEM and (b) cross-sectional TEM pictures of Ge epilayers grown at 600°C after annealing.

As will be discussed in Section 3.4.7, the threading-dislocations in the annealed samples have Burgers vectors of the form $\frac{a}{2}[101]$, $\frac{a}{2}[10\bar{1}]$, $\frac{a}{2}[01\bar{1}]$ or $\frac{a}{2}[011]$. These are glissile-dislocations that can glide in Ge under thermal-stress. Similar to the GaAs/Si system, the thermal expansion coefficient of Ge and Si are quite different. The mechanism for the reduction of threading-dislocations by cyclic thermal annealing can therefore be understood in terms of the thermal stress induced dislocation glide and annihilation mechanism proposed by Yamaguchi and co-workers [119]. Dislocation movement in heterepitaxial films due to thermal stress has been observed by Stach and co-workers using real-time TEM studies[227]. A detailed discussion regarding the mechanism for the reduction of threading-dislocations can be found in Section 3.4.8.

### **3.4.2** Optimization of the cyclic thermal annealing process

If we assume that the thermal-stress induced dislocation glide and annihilation is the mechanism for threading-dislocation reduction by cyclic thermal annealing, a process optimization scheme can be proposed based on the optimization of dislocation glide-velocity. By increasing the dislocation glide-velocity, the distance that a threading-dislocation travels during one annealing cycle increases, therefore, increasing the probability of dislocation annihilation events and leading to an enhancement in the threading-dislocation density reduction rate.

Dislocation glide-velocity can be described by the following formula [175]

$$V_{dislocation} = V_o \cdot \sigma_{exc} \cdot \exp\left(-\frac{E_v}{kT}\right) \quad (3.1)$$

where $V_{dislocation}$ is the dislocation velocity, $V_o$ is a constant, $\sigma_{exc}$ is the excess stress driving dislocation motion, $E_v$ is the energy barrier to dislocation glide, $k$ is the

Boltzmann constant and $T$ is the temperature. In cyclic thermal annealing treatment, samples of Ge epilayers on Si are first annealed at a high annealing temperature $T_H = 900°C$ and then the temperature is dropped to a low annealing temperature ($T_L$). Because the melting temperature of Ge is 939°C, it is reasonable to assume that the whole Ge/Si structure is relaxed at $T_H = 900°C$. As the temperature is dropped to $T_L$, the thermal stress between Ge epilayers and Si is induced due to the difference in coefficients of thermal expansion (CTE) between Ge and Si. This thermal stress ($\sigma_t$) can be described by the following formula

$$\sigma_t = (\alpha_{Si} - \alpha_{Ge}) \cdot (T_H - T_L) \cdot \frac{2 \cdot (1 + \nu)}{(1 - \nu)} \cdot \mu \tag{3.2}$$

where $\alpha_{Si}$ and $\alpha_{Ge}$ are the CTEs of Si and Ge, $\nu$ is the Possion ratio, and $\mu$ is the Young's modulus. The excess stress is the thermal stress minus the dislocation line tension stress. Since dislocation line tension stress is not strongly related to temperature and is much smaller compared to the thermal stress, we have an expression of the dislocation velocity as the following,

$$V_{dislocation} \propto (\alpha_{Si} - \alpha_{Ge}) \cdot (T_H - T_L) \cdot \exp\left(-\frac{E_v}{kT}\right) \tag{3.3}$$

Equation 3.3 shows that there are two processes that control the dislocation velocity: the thermal stress and the dislocation-glide energy-barrier. Thermal stress increases as $T_L$ decreases. Dislocation-glide energy-barrier, on the other hand, prevents dislocation glide at low temperatures. Due to this tradeoff, there is an optimal temperature that gives the highest dislocation velocity. Data necessary for the estimation of dislocation velocity in Ge has been published [176]. Figure 3.3 shows the calculated normalized-velocity of dislocations in Ge epilayers on Si as a function of $T_L$ assuming that the system is relaxed at $T_H = 900°C$. Based on Figure 3.3, an optimized cyclic thermal annealing process should

have a $T_L$ at about 830°C. We have performed experiments with $T_H = 900°C$ and $T_L = 100°C$, 675°C and 780°C. An experiment at $T_L = 830°C$ was not performed due to the limitation of our three-zone annealing furnace. Table 3.3 summarizes the results. The threading-dislocation density decreases as $T_L$ approaches 830°C. This verifies our dislocation velocity optimization strategy and provides evidence for the dislocation glide and annihilation mechanism. Figure 3.4 shows a cross-sectional TEM picture of sample 6AC7.

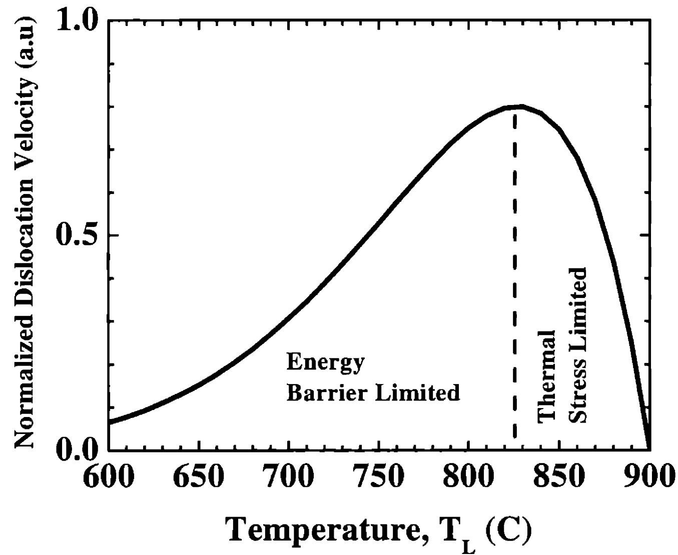



**Figure 3.3:** Calculated normalized dislocation velocity in Ge epilayers grown on Si as a function of $T_L$ during cyclic annealing, assuming the system is relaxed at $T_H = 900°C$. The calculated dislocation velocity has a peak at about $T_L = 830°C$. An optimized cyclic thermal annealing process should have a $T_L$ close this temperature.

**Table 3.3: Annealing parameters and characterization results of samples annealed at different $T_L$. The threading-dislocation density decreases as $T_L$ approaches 830°C**

| Sample ID | 6AC | 6AC6 | 6AC7 |
|---|---|---|---|
| $T_H$(°C)/Time(min) | 900°C/10min | 900°C/10min | 900°C/10min |
| $T_L$(°C)/Time(min) | 100°C/10min | 675°C/10min | 780°C/10min |
| Number of Annealing Cycles | 10 | 10 | 10 |
| Threading-dislocation Density by TEM ($cm^{-2}$) | $(5.2\pm0.6)x10^7$ | $(4.2\pm0.1)x10^7$ | $(2.7\pm0.1)x10^7$ |
| Threading-dislocation Density by EPD ($cm^{-2}$) | $(3.7\pm0.1)x10^7$ | $(3.1\pm0.1)x10^7$ | $(2.1\pm0.1)x10^7$ |
| EPD/TEM | 0.71 | 0.74 | 0.78 |

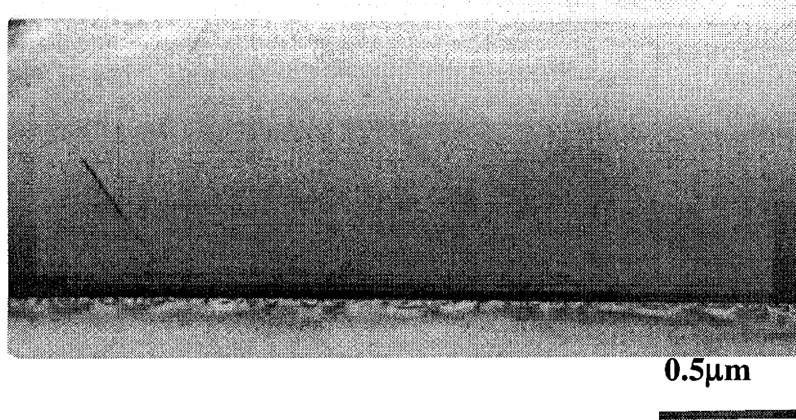



**Figure 3.4:** Cross-sectional TEM picture of Ge epilayer grown on Si by two-step UHV/CVD process after cyclic thermal annealing between $T_H = 900°C$ and $T_L = 780°C$.

### 3.4.3 Effect of high annealing temperature

To understand the limitation of the thermal annealing process, we studied the $T_H$ necessary for the reduction of threading-dislocation densities. The purpose is to find the lowest $T_H$ that is effective in reducing threading-dislocation densities. For this experiment, samples grown at 600°C were used. Square samples (1 cm x 1cm) were

cleaved from a wafer with Ge grown on Si similar to that used for samples 6A10, 6A100, 6AC, 6AC6, and 6AC7. These square samples were then annealed in a rapid thermal annealing furnace at four different temperatures (650°C, 750°C, 850°C and 930°C) for 60 seconds. After annealing, cross-sectional TEM samples were prepared and examined. These TEM pictures are shown in Figure 3.5. From these pictures it is clear that annealing at temperatures higher than 750°C is necessary to effectively reduce threading-dislocations. Tamura and co-workers reported that annealing temperature higher than 900°C is necessary to reducing threading-dislocation densities in GaAs grown on Si [177]. Our experiment shows a similar trend.

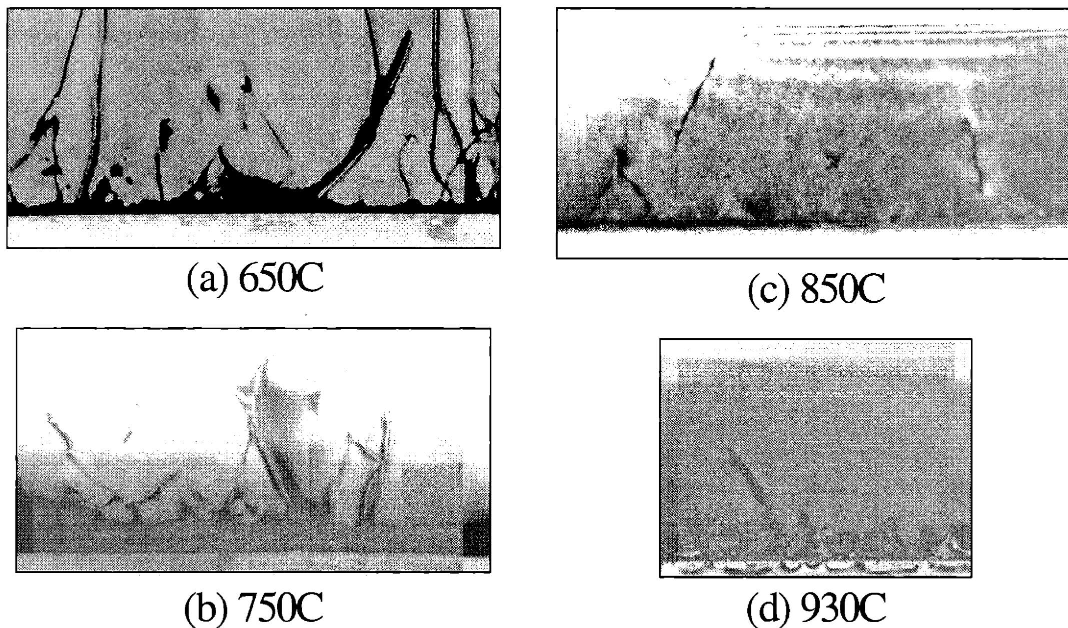
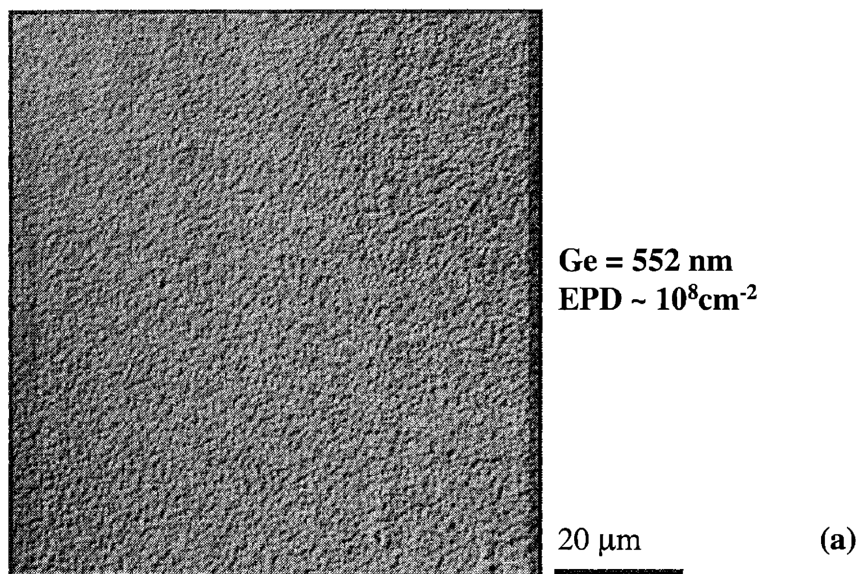


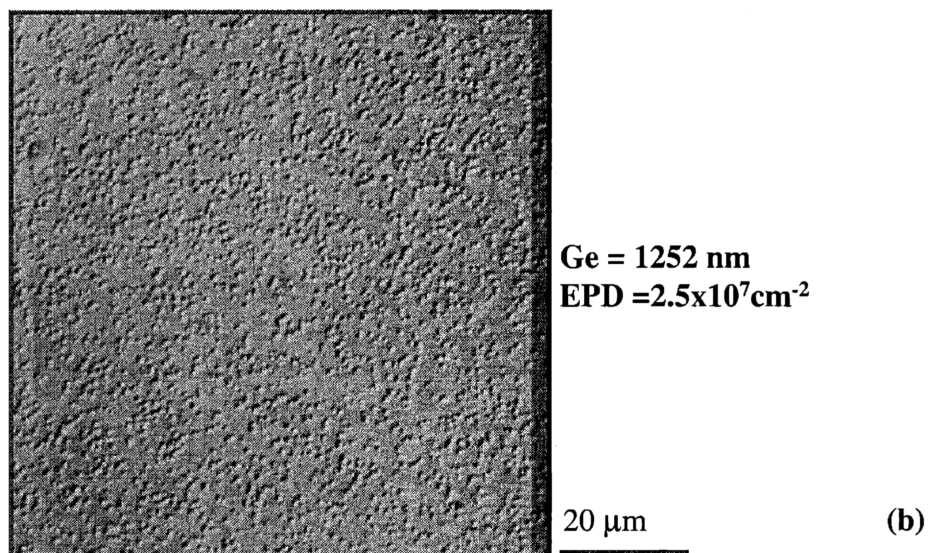

**Figure 3.5:** Cross-sectional TEM pictures of Ge grown on Si at 600°C annealed in a rapid-thermal annealing furnace for 60 seconds at (a) 650°C, (b) 750°C, (c) 850°C, and (d) 930°C.

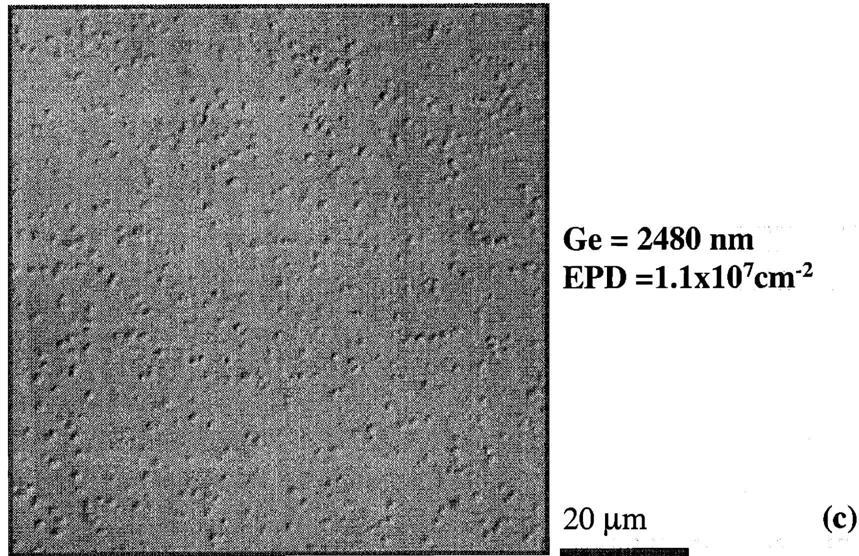
### 3.4.4 Effect of Ge epilayer thickness

The proposal of thermal stress induced dislocation glide and annihilation as the mechanism for the reduction of threading-dislocations suggests that an increase in Ge epilayer thickness can result in lower threading-dislocation densities after thermal annealing. This is because the thermal strain energy increases as the Ge epilayer thickness increases. Therefore, threading-dislocations in thicker Ge film have higher driving force to overcome barriers for dislocation motion. To verify this point, samples with four different Ge epilayer thicknesses were grown at 600°C and cyclically annealed between 900°C and 780°C for 10 cycles. Annealed samples were then etched in the EPD solution described in section 3.3 for 10 seconds. The film thickness of each film was measured by chemical etching and surface profilometry.

Figure 3.6 summarizes the results. The threading-dislocation density in Ge epilayers grown on Si after thermal annealing is lower in thicker Ge film. This indicates that an increase in Ge epilayer thickness is effective in increasing driving force for threading-dislocation reduction. It is interesting to examine the distribution of threading-dislocations in Figure 3.6. EPD pictures of samples with lower threading-dislocation densities (that is, Figure 3.6 (b), (c) and (d)) reveal that threading-dislocations are clustered together after annealing. Dislocation clusters are especially visible in Figure 3.6 (d). Details regarding the effect of dislocation clustering on the effectiveness of annealing for reducing threading-dislocations will be discussed in Section 3.4.8. Another interesting feature to note in Figure 3.6 is the circular shape of each etch-pit which makes it easier to distinguish closely spaced etch-pits as opposed to the elogated etch-pits revealed by KOH etching of GaAs [119].


Ge = 552 nm
EPD ~ 10^8cm^-2
20 μm
(a)


Ge = 1252 nm
EPD =2.5x10^7cm^-2
20 μm
(b)



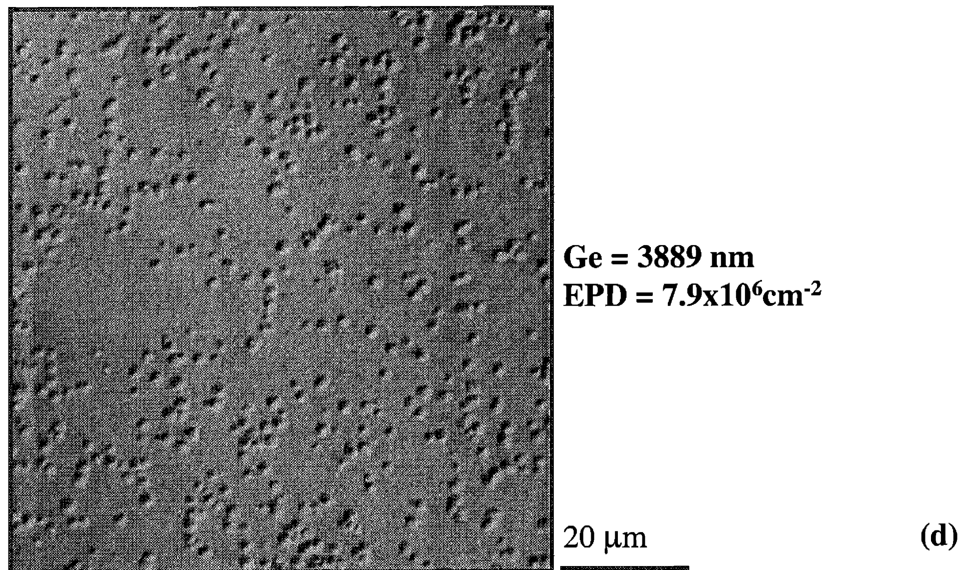




**Figure 3.6:** EPD pictures of Ge epilayers grown on Si at 600°C after cyclic thermal annealing between 900°C and 780°C. (a) Thickness = 552 nm, (b) Thickness = 1252 nm, (c) Thickness = 2480 nm, (d) Thickness = 3889 nm.

### **3.4.5** Verification of threading-dislocation density measurements

In section 3.2.3, we have discussed the problem related to the EPD measurement of threading-dislocation densities in GaAs grown on Si using KOH etching. To ensure proper

threading-dislocation density measurements, we have used both PV-TEM and EPD for the measurement. These data are summarized in Tables 3.1, 3.2 and 3.3. Figure 3.7 shows the correlation between EPD and PV-TEM measurements. The correlation between PV-TEM and EPD measured threading-dislocation densities is very good except for the measurement from sample 9A10. The EPD measurement of threading-dislocation density in sample 9A10 is much lower than that measured by PV-TEM. This is also evident in the EPD/TEM ratio reported in Tables 3.1 and 3.2. Compared to other samples reported in Tables 3.1 and 3.2, the EPD/TEM ratio for sample 9A10 is much lower. This discrepancy can be attributed to some unrevealed threading-dislocations in EPD pictures of sample 9A10. The EPD/TEM ratio for sample 6A is higher compared to those of other samples in Tables 3.1 and 3.2. This is due to the fact that AFM is used to image sample 6A as the resolution of optical microscopy is insufficient to reveal those etch-pits.

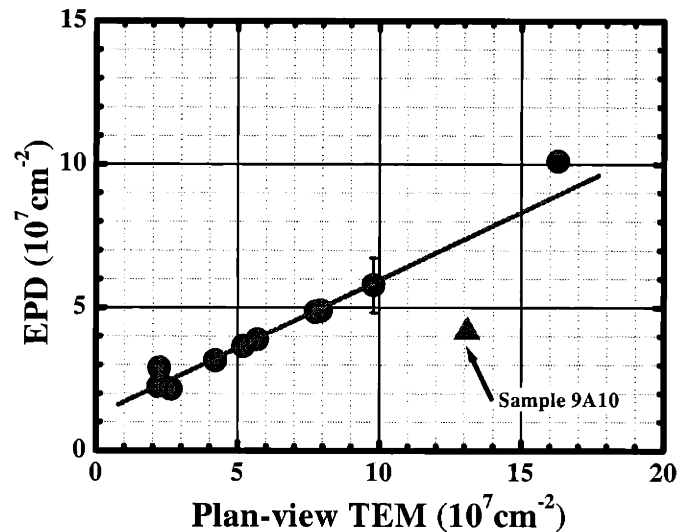



**Figure 3.7:** Correlation between threading-dislocation densities measured by EPD and plan-view TEM. The correlation between measurements by EPD and TEM is very good except for the measurement of sample 9A10.

The EPD/TEM ratio can be attributed to the resolution limit of the optical microscope. If two etch-pits overlap each other, it become difficult to resolve individual pits. The modeling of EPD/TEM ratio considering the overlapping can be estimated by a statistical model proposed by Stirland and co-workers[173].

$$\frac{EPD}{N_d} = \frac{[1 - \exp(-\pi N_d r^2)]}{\pi N_d r^2} \tag{3.4}$$

$N_d$ is the threading-dislocation density which in our case is the density measured by TEM. $r$ is the "etching resolution" parameter defined as the closest distance at which two similar etch-pits can be distinguished. Using data reported in Tables 3.1, 3.2 and 3.3 and Equation 3.4, we estimated that the "etching resolution" of our EPD technique is about 0.6~1 μm which is very close to what can be estimated from Figure 3.6.

Figure 3.7 shows that the accuracy of threading-dislocation density measured by EPD is sufficient at densities in the low $10^7$ $cm^{-2}$ range. In this range, EPD also provides a larger sampling area compared to TEM. For samples with lower dislocation densities, it is therefore reasonable to measure the dislocation density by EPD. However, in some cases this can bring disaster. For example, Figure 3.8 shows an EPD picture of sample 6A taken by an optical microscope. From plan-view TEM study, we know that this sample has a threading-dislocation density of about $10^9$ $cm^{-2}$. Lacking the required resolution, the density of etch-pits in optical microscope picture (Figure 3.8) is 8 x $10^5$ $cm^{-2}$. However, there is a huge amount of small features in the background. Using AFM, these features show up as etch-pits. The density of etch-pits revealed by AFM is about $10^9$ $cm^{-2}$. Therefore, it is important to check the dislocation-density measurements carefully. Discussion in this section suggests the use of TEM for measurements when dislocation

density is high (EPD > 4 x $10^7$ $cm^{-2}$) and the use of EPD when the dislocation density is low (EPD < 3 x $10^7$ $cm^{-2}$). It is always a good idea to check the EPD measurement with TEM when in doubt. Cases like sample 9A10 can show up sometimes. In cases where very low densities are measured by EPD, it is important to check the dislocation density by both AFM and optical microscopy. It is always a good idea to check with TEM before publication.

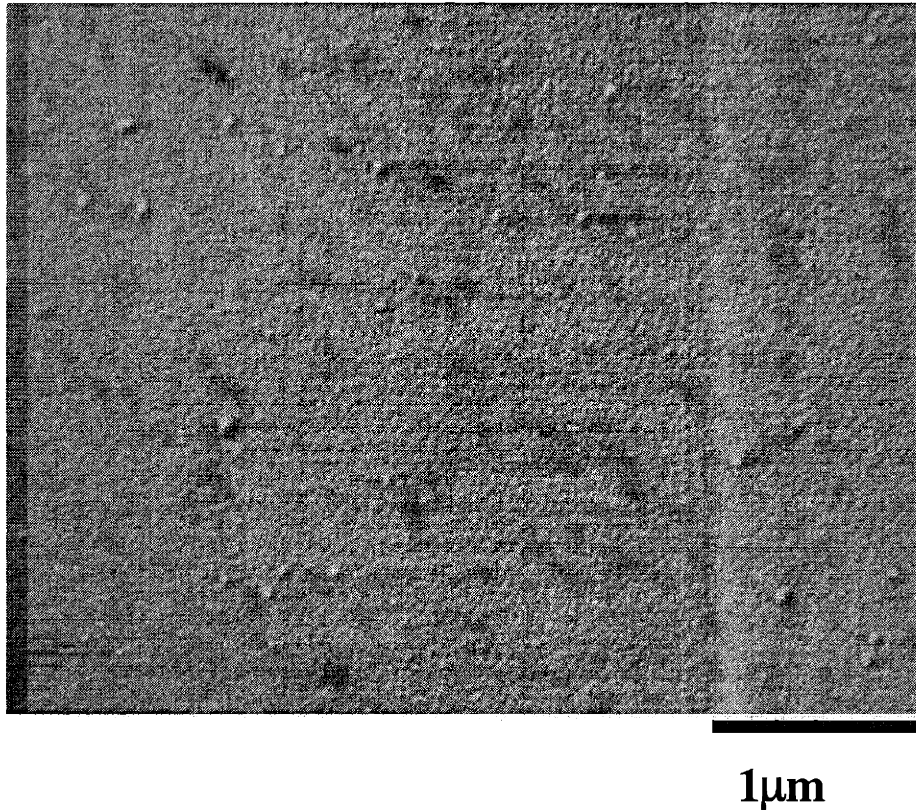



**Figure 3.8:** Picture of sample 6A etched by the EPD etching solution. The picture is taken using an optical microscope.

**3.4.6** Selective area growth and the effect of mesa size on threading-dislocation density

In discussion in sections 3.4.1 and 3.4.2, it was suggested that the mechanism for threading-dislocation density reduction is dislocation glide and annihilation. If these threading-dislocations can glide under thermal stress, it is possible to further reduce the threading-dislocation density by gliding threading-dislocations to dislocation sinks. Mesa side walls are effective dislocation sinks. Reduction of threading-dislocations by gliding them to mesa sidewalls have been suggested by several research groups [165] [122] [123].

We deposited small Ge mesas on Si by the selective growth of Ge on patterned $SiO_2$/Si wafers. We then used EPD to estimate the threading-dislocation densities in Ge selectively grown on patterned $SiO_2$/Si wafers. Figure 3.9 (a) shows the EPD result of two selectively grown Ge mesas after 10 minutes of annealing at $T_H = 900°C$. The average EPD is $(4.3 \pm 0.2) \times 10^7$ $cm^{-2}$. Figure 3.9 (b) shows the EPD result of two selectively grown Ge mesas cyclically annealed between $T_H = 900°C$ and $T_L = 100°C$ 10 times. The average EPD is $(2.3 \pm 0.2) \times 10^6$ $cm^{-2}$. Of particular interest, one of the Ge mesas in Figure 3.9 (b) is without threading-dislocation. Many threading-dislocation free Ge mesas were found in our samples. This result was also verified by AFM. The ability of our EPD counting technique to detect a reduction in threading-dislocation density with increasing number of annealing cycles validates its effectiveness in resolving etch-pits in selectively grown Ge mesas. We also studied the dependence of the threading-dislocation density in small Ge mesas as a function of mesa-sidewall width. The average threading-dislocation density decreased with the decrease of mesa-sidewall width as shown in Figure 3.10, which is similar to the prediction of models described by Yamaguchi and Beltz [165] [122]. Experiments described in this section have been repeated and verified four times.

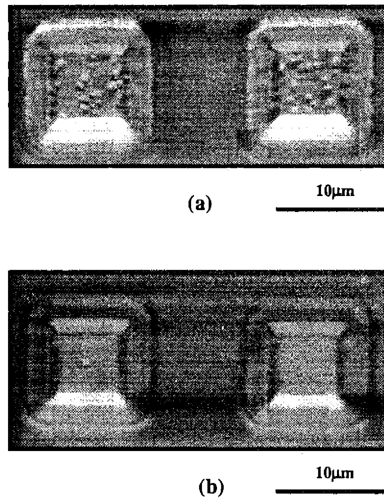



**Figure 3.9:** EPD results of Ge selectively grown on patterned $SiO_2$/Si wafers followed by annealing. (a) EPD picture of a sample annealed at 900°C for 10 min. (b) EPD picture of a sample cyclically annealed between 900°C and 100°C ten times.

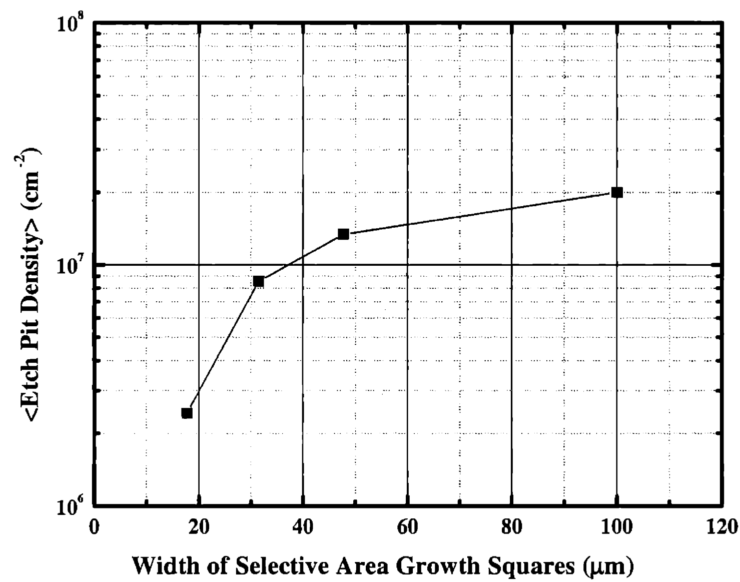



**Figure 3.10:** Average EPD vs. width of selective area growth squares.

### 3.4.7 Burgers vector analysis

To understand the mechanism for the reduction of threading-dislocations, it is important to analyze the Burgers vector in the Ge epilayer. This can be done by taking TEM pictures using two-beam diffraction technique and $g \cdot b$ analysis [95] [163] [178] [179]. To assist the interpretation of TEM pictures taken for the $g \cdot b$ analysis, Figure 3.11 shows the electron diffraction pattern of a diamond cubic structure when the [110] axis is aligned to the electron beam.

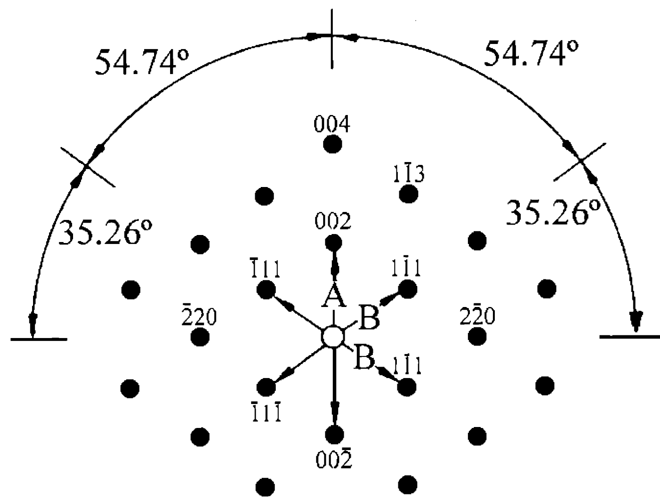
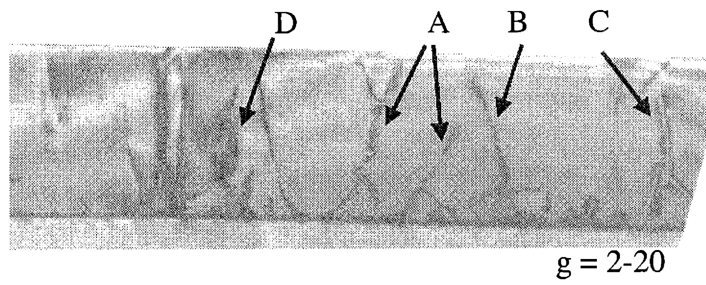



**Figure 3.11:** Electron diffraction pattern for a diamond cubic structure when the [110] axis is aligned to the electron beam.

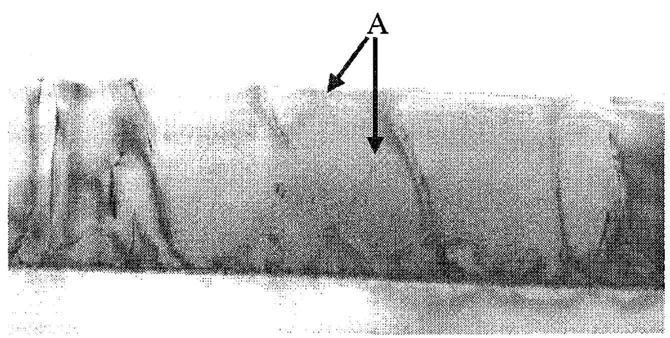
There are two types of threading-dislocations in systems such as the epitaxial growth of Ge on Si. The pure-edge dislocations have Burgers vectors of the form $\pm\frac{a}{2}[1\bar{1}0]$ or $\pm\frac{a}{2}[110]$. Using the $g \cdot b$ criterion, these dislocations are invisible at $g = \pm(004)$. There is no resolved shear stress for these pure-edge dislocations under biaxial stress in the (001) plane [178]. These pure-edge dislocations therefore cannot glide due to thermal stress caused by thermal mismatch between Ge and Si and are "sessile dislocations". The 60°

"mixed" dislocations have Burgers vector of the form $\pm\frac{a}{2}[101]$ , $\pm\frac{a}{2}[10\bar{1}]$, $\pm\frac{a}{2}[01\bar{1}]$ or $\pm\frac{a}{2}[011]$. Using the $g \cdot b$ criterion, these dislocations are invisible at $g= \pm(1\bar{1}1)$ and $g= \pm(\bar{1}11)$. These mixed dislocations can glide under thermal stress and are "glissile dislocations".

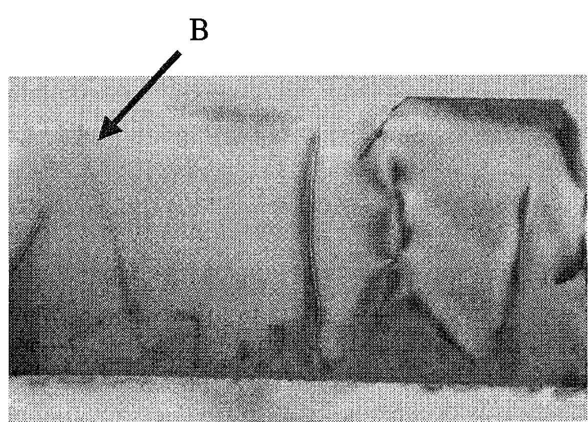
Figure 3.12 shows the TEM pictures for the Burgers vector analysis of sample 6A. This is a sample grown at 600°C without post growth annealing. Dislocation A is invisible in Figure 3.12 (a) ($g = [2\bar{2}2]$). Dislocation B is invisible in Figure 3.12 (b) ($g = [\bar{2}22]$). These two dislocations are therefore glissile-dislocations. Dislocation C is invisible in Figure 3.12 (c) and dislocation D is invisible in Figure 3.12 (d) ($g = [004]$). These dislocations are therefore sessile-dislocations. The as-grown Ge on Si, therefore, has a high density of both sessile and glissile threading-dislocations. Figure 3.13 shows the TEM pictures for the Burgers vector analysis of sample 6AC. This is a sample grown at 600°C and cyclically annealed between 900°C and 100°C ten times. The dislocations shown in these pictures look very similar to dislocations shown in Figure 3.2 (b) and Figure 3.4. Threading-dislocations in annealed samples typically have the same geometry. These dislocations are invisible at either $g = [2\bar{2}2]$ of $g = [2\bar{2}\bar{2}]$ and are therefore glissile-dislocations. More than ten cross-sectional TEM samples of annealed Ge epilayers have been examined. All the threading-dislocations observed showed the same behavior. Since the threading-dislocation density is low in annealed samples, cross-sectional TEM pictures cannot sample a lot of threading-dislocations. Therefore, we cannot rule out the existence of sessile threading-dislocations in annealed samples. However, we can conclude that the threading-dislocations in the annealed samples are mostly glissile threading-dislocations. In the as-grown samples, there is a high density of both glissile and sessile threading-dislocations.



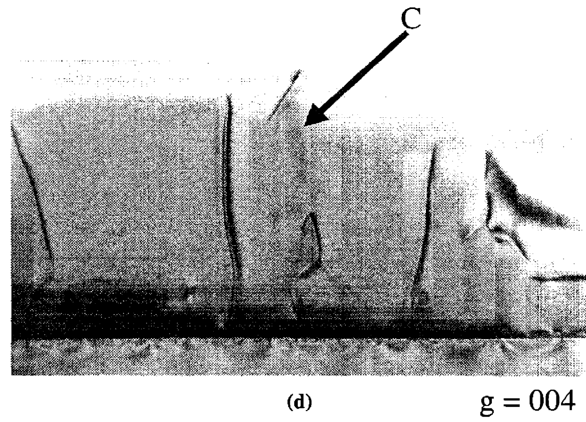

(a)




(b)




(c)



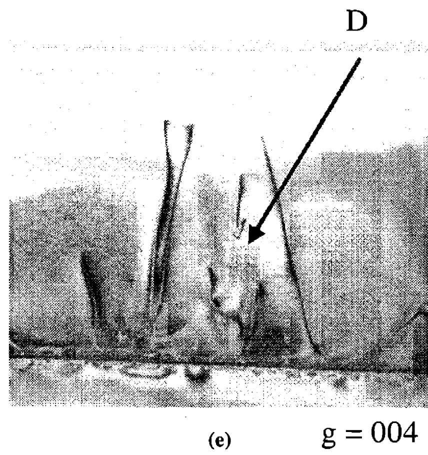




**Figure 3.12:** Cross-sectional TEM pictures for the Burgers vector analysis of sample 6A. These pictures are two beam bright field images with five reflecting conditions: (a) $g = [2\bar{2}0]$, (b) $g = [2\bar{2}2]$, (c) $g = [\bar{2}22]$, (d) $g = [004]$, (e) $g = [004]$.

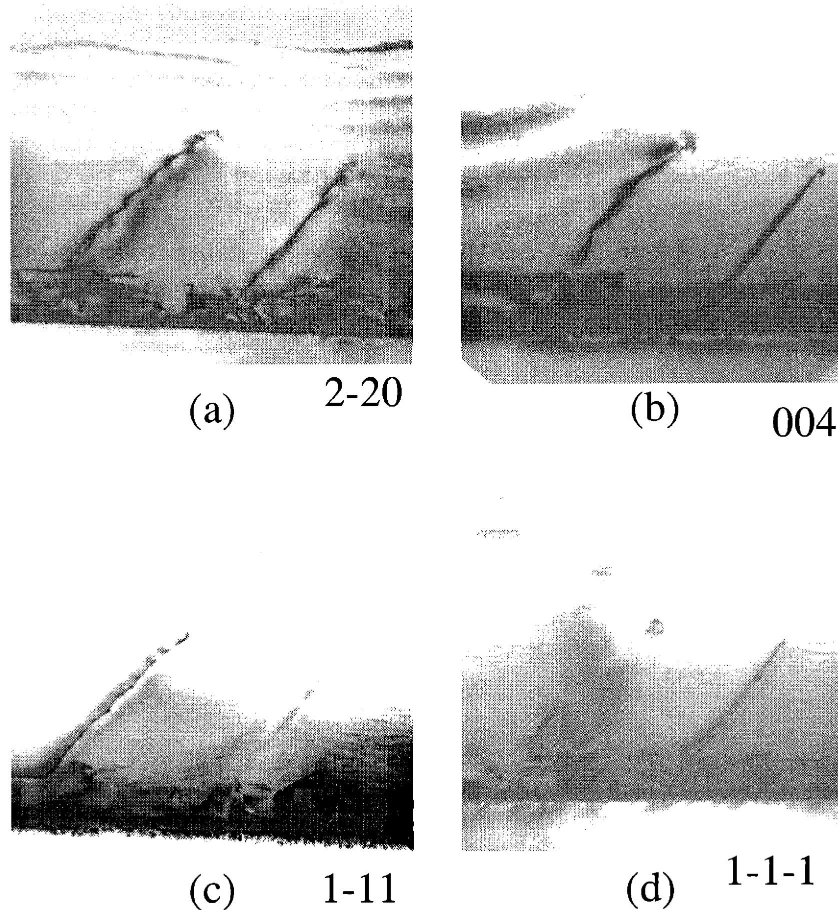



**Figure 3.13:** Cross-sectional TEM pictures for the Burgers vector analysis of sample 6AC. These pictures are two beam bright field images with four reflecting conditions: (a) $g = [2\bar{2}0]$, (b) $g = [004]$, (c) $g = [2\bar{2}2]$, (d) $g = [222]$.

**3.4.8** Mechanism for the reduction of threading-dislocations by cyclic thermal annealing

The mechanism for the reduction of threading-dislocations in Ge grown on Si by cyclic thermal annealing has been proposed by Yamaguchi and co-workers [119]. They proposed that the thermal stress between Ge and Si described by equation 3.2 can cause 60° dislocations to glide. Their TEM examination revealed that 60° (glissile) dislocations were mainly observed in the as-grown sample while pure-edge (sessile) dislocations were mainly observed in the annealed samples. They did not explain if they studied

misfit-dislocations or threading-dislocations. Based on the TEM observation, they proposed the thermal stress induced dislocation glide and dislocation reaction as the model for threading-dislocation reduction. This mechanism, however, cannot be easily justified based on their TEM observation.

As already discussed in section 3.4.7, pure-edge dislocations cannot glide under biaxial stress due to thermal mismatch between GaAs (or Ge) and Si because there is no resolved shear stress [178]. Two glissile (60°) dislocations can react and form one pure-edge (sessile) dislocation according to the following dislocation reaction.

$$\frac{a}{2}[10\bar{1}] + \frac{a}{2}[0\bar{1}1] = \frac{a}{2}[1\bar{1}0] \quad (3.5)$$

If reaction 3.5 is the reaction responsible for the reduction of threading-dislocations as proposed by Yamaguchi, reduction of density from $\sim 10^9$ cm$^{-2}$ to $10^7$ cm$^{-2}$ cannot be explained easily. This is because equation 3.5 can only provide a 50% reduction in dislocation density and the product is a sessile pure-edge dislocation that cannot glide. Both Fitzgerald and Harris have suggested that the reaction described by equation 3.5 produces permanent dislocations that are virtually impossible to eliminate [120] [150]. To allow the reduction of threading-dislocations, they suggested that reactions described by equation 3.5 should be avoided. Knall and co-workers have reported a case where reactions like equation 3.5 dominated the process in GaAs grown on Si after annealing [179]. They found that very little dislocation reduction could happen under this condition.

Our experiments with cyclic thermal annealing of Ge grown on Si showed that a reduction of threading-dislocation density from $10^9$ cm$^{-2}$ to $10^7$ cm$^{-2}$ is possible. We have calibrated

our threading-dislocation density measurements carefully and are very confident with the experiment. The Burgers vector analysis described in section 3.4.7 clearly demonstrated that the threading-dislocations in Ge after cyclic thermal annealing are mostly glissile dislocations. Judging from these facts, reaction 3.5 cannot be the mechanism behind the reduction of threading-dislocation density. The proposal that sessile pure-edge dislocations are virtually permanent and cannot be removed is not justified by our experiment. There must be a mechanism for the removal of sessile pure-edge threading dislocations.

There are several possible mechanisms for the removal of sessile pure-edge threading dislocations. One possible explanation is that these sessile threading-dislocations can climb. If the distance between two sessile threading-dislocations with opposite Burgers vectors can be reduced by dislocation climb so that annihilation reactions are possible, reduction of sessile threading-dislocations can happen. The deformation-mechanism map of the Ge crystal published by Ashby shows that dislocation climb is a possible deformation-mechanism when the temperature is close to the melting point [180]. However, climb is only possible if there is a resolved shear stress. Since there is no resolved shear stress on sessile threading-dislocations, it is not likely that these dislocations can climb. Also, if climb is a possible mechanism for the reduction of sessile threading-dislocations formed by Equation 3.5, one would expect to find a lot of sessile threading-dislocations after annealing. This is, however, not the case. All the threading-dislocations we examined are found to be glissile threading-dislocations. There must be some mechanism that allows the transformation of sessile threading-dislocations back into glissile threading-dislocations after the reaction of Equation 3.5.

One possible mechanism is that a sessile threading-dislocation can split into two glissile dislocations by the following reaction:

$$\frac{a}{2}[1\bar{1}0] = \frac{a}{2}[10\bar{1}] + \frac{a}{2}[0\bar{1}1] \tag{3.6}$$

Reaction described by equation 3.6 is the reverse of equation 3.5. Based on the $b^2$ criteria, this is not an energetically favorable reaction. However, if another reaction can happen and generate two more glissile dislocations:

$$\frac{a}{2}[\bar{1}10] = \frac{a}{2}[\bar{1}01] + \frac{a}{2}[01\bar{1}] \tag{3.7}$$

The combination of Equation 3.6 and 3.7 is

$$\frac{a}{2}[1\bar{1}0] + \frac{a}{2}[\bar{1}10] = nil \tag{3.8}$$

The reaction of Euqation 3.8 is an energetically favorable reaction and can cause a reduction in threading-dislocation density. If thermal annealing can provide enough driving force to overcome the energy barrier for Equations 3.6 and 3.7, the removal of sessile dislocations can be explained. The energy barrier for reactions of Equations 3.6 and 3.7, however, is likely to be very high. The energy per length of a dislocation ($E_d$) can be described by

$$E_d \cong \frac{\mu b^2}{4\pi(1-\nu)} \tag{3.9}$$

where $\mu$ is the shear modulus, $b$ is the magnitude of the Burgers vector, and $\nu$ is the Poisson ratio [182]. Using values typical for semiconductors such as Si, Ge and GaAs, the energy per length of a dislocation is on the order of 10 eV/nm. This is a very high energy barrier that cannot be overcome easily even at the melting temperature of Ge. An early calculation of the strength of sessile dislocations by Stroh showed that reaction like

Equation 3.6 would only happen under high stress and high temperature [181]. We already know that there is no resolved shear stress on sessile threading-dislocations. Therefore, it is unlikely that the reduction of sessile threading-dislocations can be explained by this mechanism.

A much simpler way to resolve this issue might be to consider a wide range of possible interactions between threading-dislocations rather than focusing only on reactions represented by Equation 3.5. Speck and co-workers have considered all the possible interactions between threading-dislocations in cubic semiconductor structures [183] [184] [185]. The interaction between sessile and glissile threading-dislocations can be described by equations similar to the following:

$$\frac{a}{2}[1\bar{1}0] + \frac{a}{2}[01\bar{1}] = \frac{a}{2}[10\bar{1}] \tag{3.10}$$

Equation 3.10 points out that the product of the interaction between a sessile dislocation and a glissile dislocation can be a glissile dislocation. This reaction is energetically favorable under the $b^2$ criteria. Compared to the two other mechanisms discussed before, it is not necessary to have resolve shear stress on sessile threading-dislocations for this mechanism to work. The reaction of Equation 3.10 does not require the sessile threading-dislocations to move. Reactions similar to that represented by equation 3.10 provide the best explanation to the removal of sessile threading-dislocations.

To explain why the threading-dislocations in the annealed samples are mostly glissile threading-dislocations, we need to consider all the reactions among threading-dislocations. This can be done with the help of Table 1 in reference 183. According to Speck and co-workers, there are 12 possible Burgers vectors in the cubic

semiconductor structure. Among the 12, 8 are for glissile dislocations and 4 are for sessile. There are therefore 144 possible reactions between these different dislocations. The ratio between the number of reactions that would produce glissile dislocations to the number of reactions that would produce sessile dislocations is 4.5. This means after reactions between threading-dislocations, assuming random distribution, the product of the reactions is 4.5 times more likely to be glissile threading-dislocations than sessile threading-dislocations. This explains why most of the threading-dislocations in the annealed samples are glissile-dislocations.

A summary of the mechanism is in order here. According to the discussion in this section, the reduction of threading-dislocations due to thermal cycling can be explained by the following. Due to the difference of coefficient of thermal expansion between Ge and Si, there is a thermal stress on the (001) plane when there is a temperature change. This thermal stress can be described by Equation 3.2. This thermal stress can push glissile threading-dislocations to glide. When two glissile threading-dislocations with opposite Burgers vectors are close to each other, they can annihilate according to reactions similar to the following:

$$\frac{a}{2}[10\bar{1}] + \frac{a}{2}[\bar{1}01] = nil \tag{3.11}$$

Reactions between glissile dislocations also can produce sessile dislocations by reactions similar to that described by Equation 3.5. These sessile dislocations are unlikely to glide or climb under thermal stress. These sessile dislocations, however, are not permanent dislocations. A glissile dislocation can react with a sessile dislocation according to reactions similar to that described by equations 3.10. Reactions 3.5, 3.10 and 3.11 all result in reduction of threading-dislocations.

Our explanation of threading-dislocation reduction by thermal stress induced dislocation glide and reaction suggests the modeling of the process by a "reaction kinetic" approach. This approach has been used by Yamaguchi and co-workers, Kroemer and co-workers, and more recently by Speck and co-workers to explain threading-dislocation reduction [187] [151] [186]. The idea is that any process that promote lateral movement of threading-dislocations can results in dislocation reactions. Since dislocation reactions cause reduction in dislocation density, the process can be described by

$$\frac{d\rho}{dn} = -k \cdot \rho^2 \tag{3.12}$$

where $\rho$ is the dislocation density, $n$ is the parameter that results in lateral movement of dislocations (in our case, number of annealing cycles), and $k$ is the reaction rate constant. The solution of equation 3.12 can be integrated easily. A comparison of this model with experimental data presented in this chapter is shown in Figure 3.14.

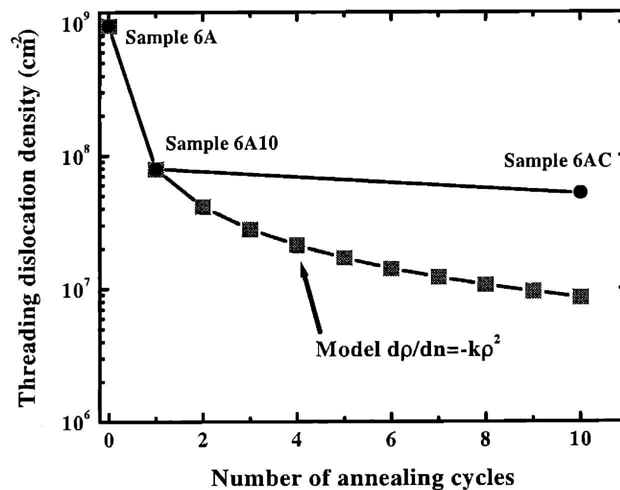



**Figure 3.14:** Comparison of reaction kinetic model for threading-dislocation density reduction to experimental data.

Figure 3.14 shows that the prediction of the model does not fit the experimental results. The rate of threading-dislocation reduction is reduced after the first annealing cycle. Several explanations are possible here. During cyclic thermal annealing, the stress due to thermal mismatch pushes the dislocations to move back and forth. Therefore, a dislocation can only react with dislocations along it's path. Once these dislocations are gone, there are no more dislocations for further reaction and the reduction rate decreases. Another explanation is that threading-dislocations form clusters after annealing. Clusters of dislocations can be seen clearly in Figure 3.6. These clusters of threading-dislocations are probably pile-ups of glissile and sessile threading-dislocations that cannot react with each other. Once these clusters of dislocations are formed, no more reactions between dislocations are possible.

One last question regarding the mechanism for threading-dislocation reduction is how to reconcile the difference between experiments presented in this chapter and the work done on GaAs grown on Si. Report by Knall and co-workers clearly showed that thermal annealing has little effect in reducing threading-dislocation density in their experiment [179]. However, there is a large literature suggesting otherwise. We believe the discrepancy in the literature regarding effect of thermal annealing on the reduction of threading-dislocations in GaAs grown on Si is due to the fact that GaAs is a compound semiconductor. While for Ge the annealing temperature is the main factor controlling the dislocation reduction process, for GaAs there are other factors to consider. For example, Deppe and co-workers showed that annealing of GaAs/Si at 680°C can be very effective in reducing threading-dislocations if the annealing atmosphere is $ZnAs_2$ [188]. Without $ZnAs_2$, there is no effect. Tamura and co-workers showed that for GaAs/Si structure, when annealed in a rapid thermal annealing furnace by putting two wafers front-to-front, only

annealing at temperatures above 900°C can results in serious reduction in threading-dislocation density [189]. Takagi and co-workers showed that if one anneals GaAs/Si structures at 950°C for too long, the threading-dislocation density would actually increase [190]. They attributed this effect to solution hardening due to Si diffusion from the substrate into GaAs. Apparently the situation for GaAs/Si system is much more complicated compared to the Ge/Si system. Judging from the data in the literature, it can be concluded that thermal annealing is effective in reducing threading-dislocations in GaAs grown on Si. Nevertheless, it is important to control the temperature, annealing time, and furnace atmosphere carefully for this system.

## 3.5 Conclusion

This chapter provided conclusive evidence that high-quality Ge epilayers can be grown directly on Si without the insertion of a complicated buffer layer structure. It was also shown that selective area growth of Ge on Si with no threading-dislocations can be done easily. This provides an opportunity for the integration of high performance Ge photodiodes on Si. In the next chapter, the potential of high-quality Ge epilayers grown on Si for the integration of Ge photodiodes on Si is discussed.

# Chapter 4

# Ge photodetectors integrated on Si

## 4.1 Overview and introduction

This chapter discusses the performance of photodetectors made from Ge grown on Si by epitaxial technology described in Chapter 3. A review of the work related to the integration of near-infrared photodetectors on Si can be found in Chapter 1 and is therefore not repeated here. This chapter begins with a discussion of the processing steps for making Ge photodetectors on Si using Ge epilayers grown by technologies described in Chapter 3. Three kinds of photodetectors were made: metal-semiconductor-metal (MSM) photodetectors, Ge/Si heterojunction photodetectors, and p-i-n Ge photodetectors. The performance of these photodetectors as a function of the materials quality is discussed. N-i-p Ge photodiodes with responsivity as high as 770 mA/W have been integrated on Si.

## 4.2 Experimental procedure

Ge epilayers were grown on Si by the technique described in Section 3.2. In short, the Ge epilayers were grown on Si using a two-step UHV/CVD process. The threading-dislocations in the Ge epilayers were reduced by cyclic thermal annealing between 900°C and 780°C. Threading-dislocation densities were measured by plan-view transmission electron microscopy (plan-view TEM). A complete report regarding the effect of cyclic thermal annealing on the reduction of threading-dislocation densities has Chapter 3. Table 4.1 summarizes the growth parameters and characterization results of samples used for experiments reported in this chapter.

**Table 4.1: Annealing parameters and characterization results of samples used for making MSM and Ge/Si heterojunction detectors. Samples were grown by two-step UHV/CVD process with the first step at 350°C and the second step at 600°C.**

| Sample ID | 6A | 6AC5 | 6AC20 |
|---|---|---|---|
| Cyclic annealing temperatures (°C) | NA | 900/780 | 900/780 |
| Number of annealing cycles | 0 | 5 | 20 |
| Threading-dislocation density ($cm^{-2}$) | $(9.5\pm0.4)x10^{8}$ | $(2.7\pm0.1)x10^{7}$ | $(1.6\pm0.1)x10^{7}$ |
| Mobility-lifetime product ($cm^2/V$) | $7x10^{-8}$ | $2x10^{-7}$ | $3x10^{-6}$ |

Ge epilayers (1μm grown on (001) p-Si, 0.5-2 Ω-cm) treated with three different post-growth annealing treatments (samples 6A, 6AC5, 6AC20) were used to fabricate metal-semiconductor-metal (MSM) photodetectors to study the effect of post-growth annealing on the photodetector performance. MSM photodetectors were made by lithographic definition of silver metal evaporated onto the Ge epilayers. Figure 4.1 shows a schematic of the structure of the MSM photodetectors. The spacing between metal contacts was 10 μm. After the metal deposition, no thermal treatments were performed to avoid inter-diffusion and alloying. Mesa Ge/Si heterojunction diodes with area ranging from 4 x $10^{-4}$ $cm^2$ to 0.1 $cm^2$ were also fabricated by photolithography and wet chemical etching of Ge epilayers. Ohmic contacts were formed by evaporation of contact metal, photolithagraphy and chemical etching. Figure 4.2 shows a schematic of the structure of the mesa Ge/Si heterojunction diodes. The Ge epilayers used for mesa diodes were the same as those used for MSM photodetectors.

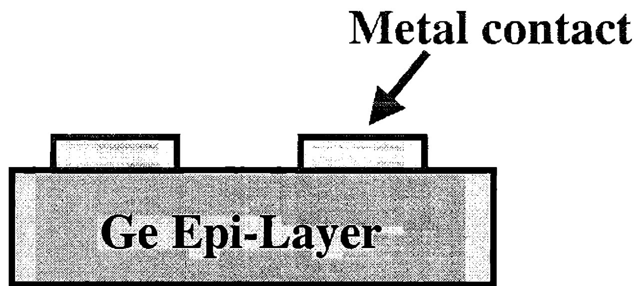



**Figure 4.1:** Schematic of the MSM photodetectors.

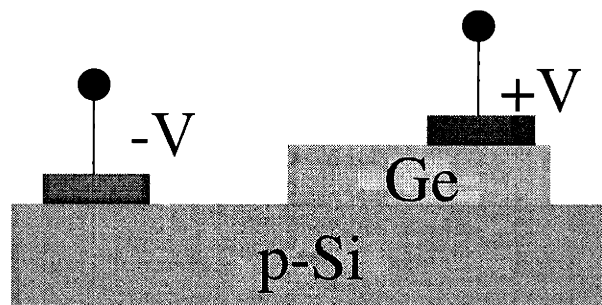



**Figure 4.2:** Schematic of the mesa Ge/Si heterojunction photodetector.

For the fabrication of p-i-n Ge photodiodes on Si, p-type and n-type Si substrates with different doping concentrations were used for Ge growth. The substrates were p-type and n-type Si (100) wafers with resistivities in the range of 0.008-0.02 Ω-cm for the heavily doped substrates and 0.5-2 Ω-cm for the lightly doped substrates. Changing the substrate type and doping concentration has no negative effect on the epitaxial growth of Ge on Si. The Ge epilayers were grown using epitaxial growth procedure similar to that described in Chapter 3. After epitaxy, wafers were cyclically annealed between 900°C and 780°C 20 times to reduce threading-dislocations. For the formation of the p-i-n structure, we introduced dopants in the Ge surface by ion implantation. For p-i-n Ge diodes on n-Si, we ion implanted the Ge surface with $4 \times 10^{15}$ $cm^{-2}$ of $BF_2$ at 30 keV at a tilt of 7°. For n-i-p

Ge diodes on p-Si, phosphorous was implanted at 30 keV with a dose of 4 x $10^{15}$ $cm^{-2}$ at a tilt of 7°. After ion implantation, dopant activation was accomplished by an anneal at 600°C for 5 minutes. Figure 4.3 shows the schematics of the p-i-n Ge photodetector. The secondary ion mass spectrometry (SIMS) profiles of n-i-p Ge diodes on $p^+$-Si and p-i-n Ge diodes on $n^+$-Si are shown in Figure 4.4 (a) and (b), respectively. Finally, by photolithography and wet chemical etching we fabricated mesa structures with areas ranging from $4x10^{-4}$ $cm^2$ to 0.1 $cm^2$. Ohmic contacts were formed by evaporation of contact metal.

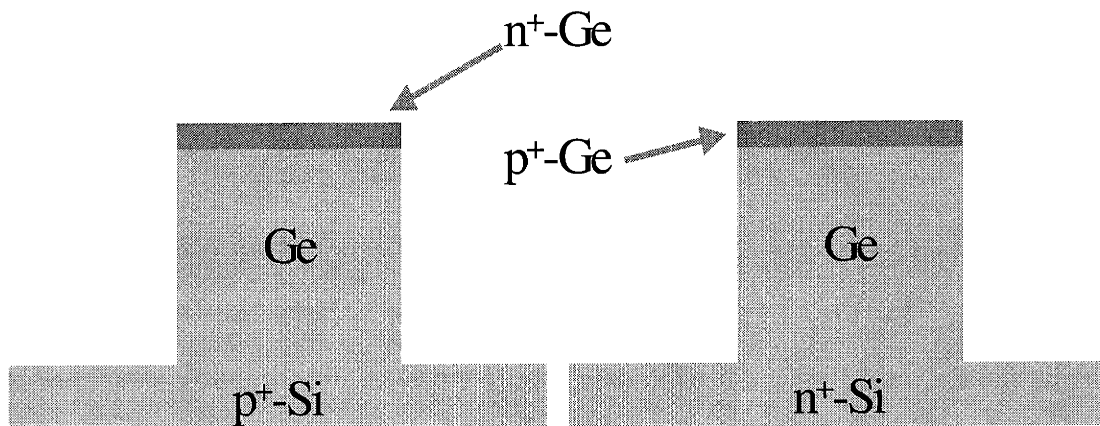
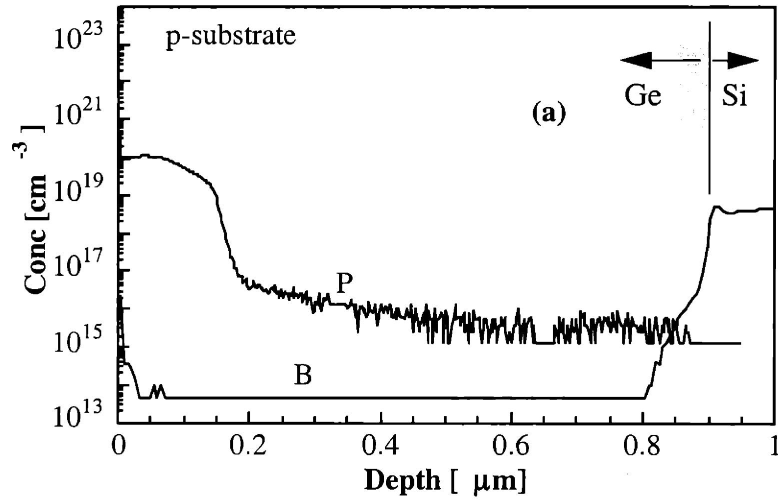



**Figure 4.3:** Schematics of n-i-p Ge photodiode on p-Si substrate and p-i-n Ge on n-Si substrate.



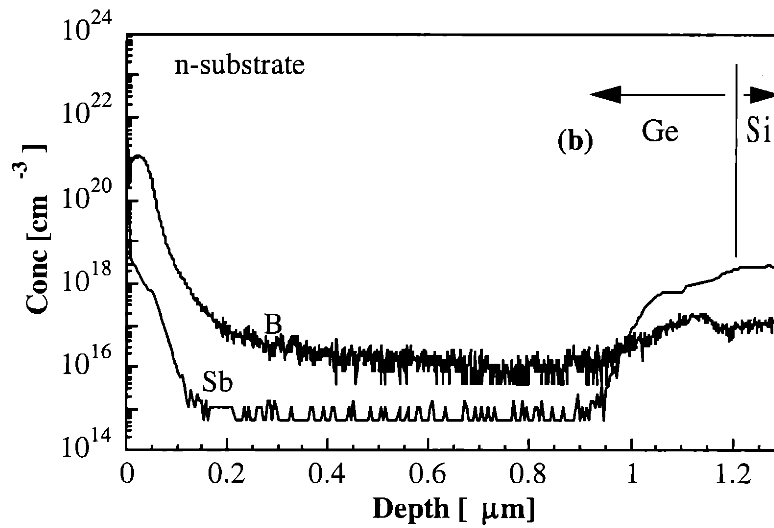




**Figure 4.4:** SIMS profiles of (a) the Ge n-i-p diode (on $p^+$ Si substrate) and (b) the Ge p-i-n diode (on $n^+$ Si substrate).

## 4.3 Results and discussion

### 4.3.1 Effect of threading-dislocation densities on photodetector performance

Mesa Ge/Si heterojunction diodes with area ranging from 4 x $10^{-4}$ to 0.1 $cm^2$ were characterized. Figure 4.5 shows the current-voltage plot of a Ge/Si heterojunction diode made from sample 6AC20. The devices exhibited well pronounced rectifying current-voltage characteristics with a saturated reverse current density of about 30 $mA/cm^2$ at 1 V at room temperature. Figure 4.6 shows the band-diagram of a Ge/Si heterojunction diode grown on p-type Si substrate. This band-diagram is calculated using a one dimensional finite difference simulator [195]. The energy gap difference between Si and Ge is accounted for by a valence band discontinuity of 0.36 eV and a conduction band discontinuity of 0.1eV reported by Di Gaspare and co-workers [225]. The band-diagram and current-voltage characteristic is as expected for this kind of heterojunction [226].

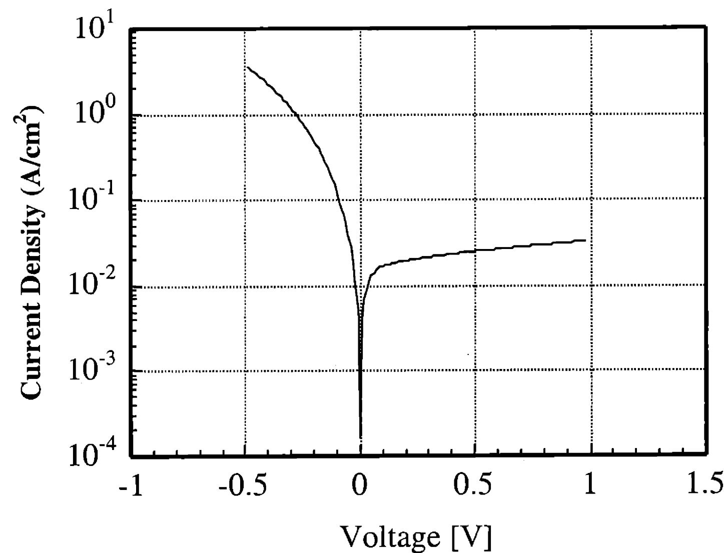



**Figure 4.5:** Current-voltage characteristics (positive voltage on Ge) of mesa Ge/Si diodes made with Ge grown on p-Si treated by 20 post-growth thermal annealing cycles between 900°C and 780°C.

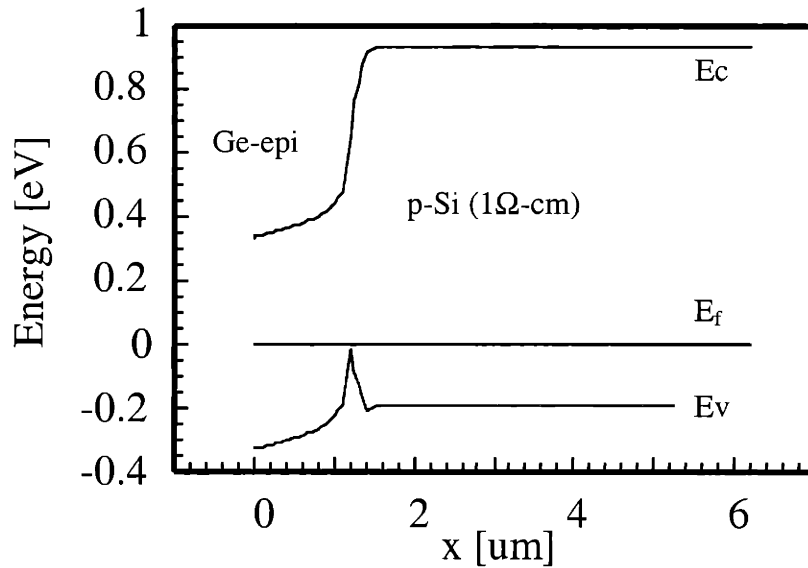



**Figure 4.6:** Band-diagram of Ge/Si heterojunction diode grown on p-Si substrate.

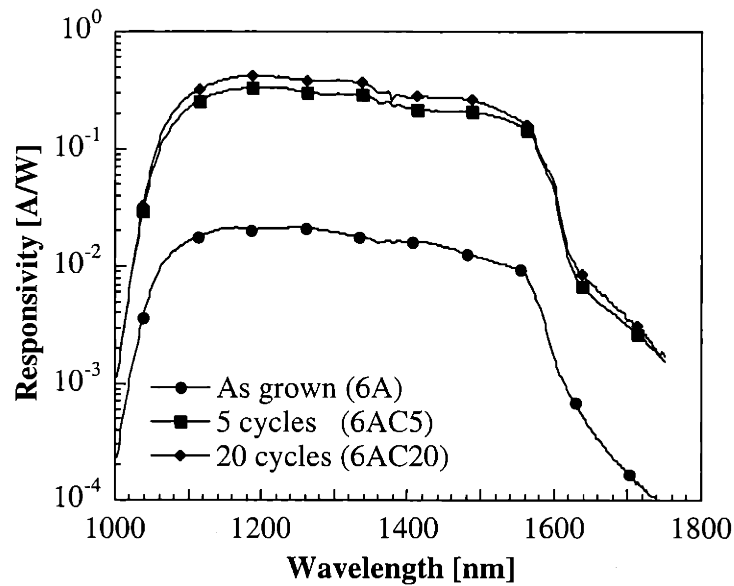



**Figure 4.7:** Short circuit spectral responsivity of mesa heterojunction photodetectors made from Ge grown on Si treated with different post-growth annealing treatments. A responsivity enhancement due to cyclic annealing is clearly demonstrated.

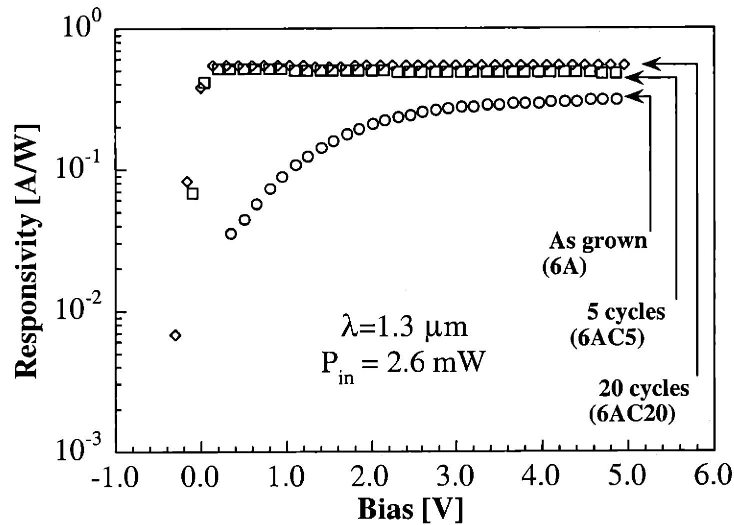



**Figure 4.8:** . Responsivity at 1300 nm versus applied bias voltage (positive voltage applied on Ge) of mesa heterojunction photodetectors made from Ge grown on Si treated with different post-growth annealing. Annealed samples reach maximum responsivity at lower bias voltages.

Ge/Si heterojunction diodes made from all three samples showed good photo-response in the near-infrared as shown in Figure 4.7. Measurements were taken in short circuit with monochromatic light intensity of 0.1 mW/cm$^2$. The detectors were illuminated through the Si substrate. A large improvement in the short-circuit photocurrent was measured from the annealed samples (sample 6AC5 and 6AC20) with responsivity close to 300 mA/W at 1300 nm as compared to that measured from the as-grown sample (sample 6A). The photo-response improved when the photodiodes were reverse biased, as shown in Figure 4.8. Both Figures 4.7 and 4.8 demonstrate a remarkable improvement of photo-response from the as-grown samples (sample 6A) to the annealed samples (sample 6AC5 and 6AC20). The responsivities of the annealed samples reach saturation (i.e. almost complete collection of the photo-generated carriers) well before the as-grown samples. The saturated responsivity of the best sample was 550 mA/W at 1300 nm. Assuming Fresnel

reflection losses of 36% and taking into account the absorption length (1 μm), the calculated internal and external quantum efficiencies were 95% and 52%, respectively.

The response speed of the mesa diode was measured by recording the photo-generated current by a train of 1320 nm, 100 ps light pulses produced by a Nd:YAG laser mode-locked at 100 MHz. The devices were biased through a 50 Ω resistor and AC decoupled by a 100 pF capacitor. The trace of a photodiode with a mesa area of $4 \times 10^{-4}$ cm$^2$ made from a Ge/Si film that was cyclically annealed 20 times (sample 6AC20) measured at a bias voltage of 4 V is plotted in Figure 4.9. The measured capacitance of this photodiode is 9.4 pF. Despite some ringing due to parasitic inductance, an 850 ps FWHM pulse duration was estimated. The relationship between pulse width (FWHM) and -3dB frequency assuming a hyperbolic secant$^2$ time dependence has been discussed by Bowers and Burrus(Figure 4.10) [37]. According to Figure 4.10, a 850 ps FWHM pulse represents a -3dB frequency of about 350 MHz. The pulse width decreased with the inverse square root of the applied bias. Devices with larger areas showed proportionally longer response times suggesting that the response speed is limited by the device capacitance rather than carrier drift time. Decreasing the device capacitance by reduing the device area should reduce response time and improve the -3dB frequency.

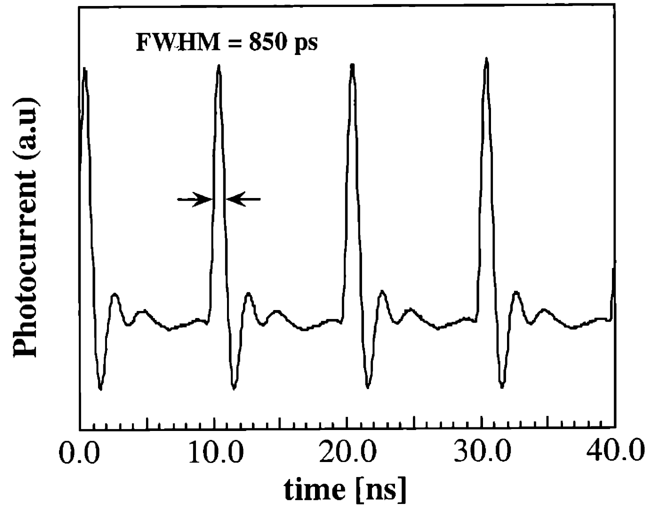



**Figure 4.9:** Photocurrent response of a heterojunction photodetector made from Ge grown on Si followed by 20 annealing cycles (6AC20).

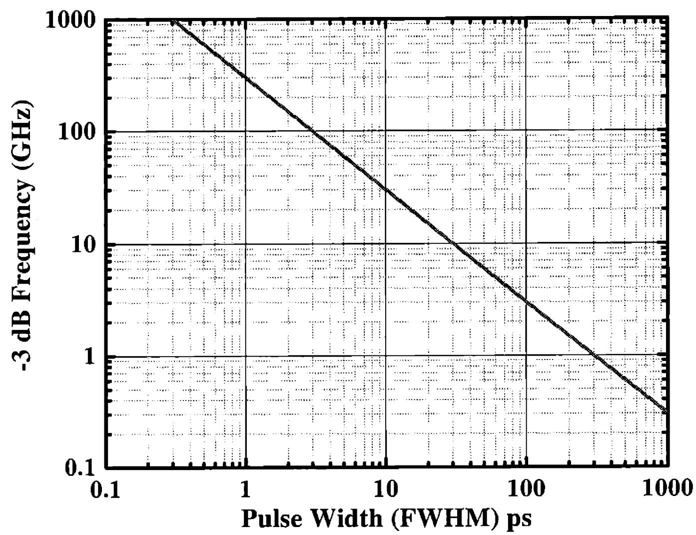



**Figure 4.10:** The relationship between pulse width (FWHM) and -3dB frequency assuming a hyperbolic secant$^2$ time dependence.

To single out the effect of the Ge epilayer quality on the optoelectronic characteristics of our devices, we fabricated metal-semiconductor-metal (MSM) planar interdigitated photodetectors. Silver electrodes spaced 10 μm apart were defined by standard optical lithography on a 100 x 500 μm region. Contacts were passivated by a photoresist layer. The MSM devices were illuminated at 1300 nm and the photocurrent was collected as a function of the bias applied to the structure (Figure 4.11 symbols). A dramatic improvement in the collection efficiency at low bias is observed after thermal annealing. The experimental data are well fitted by a simple one-parameter (mobility-lifetime product) model based on the Hecht formula adapted to a non-uniform field distribution (Figure 4.11, solid lines) [191] [192] [193]:

$$J_{ph} = q\Phi\alpha L(E)\left(1 - \exp\left(\frac{-d}{L(E)}\right)\right) \tag{4.1}$$

where $J_{ph}$ is the collected photocurrent, $q$ is the electron charge, $\Phi$ is the photon flux, $\alpha$ is the absorption coefficient, $E$ is the electric field, $L(E) = \mu\tau E$ is the drift length, $\mu$ is the carrier mobility, $\tau$ is the carrier lifetime, and $d$ is the distance between electrodes. The measured mobility-lifetime product is reported in Table 4.1 and compared to the number of threading-dislocations estimated in different samples. Despite the small number of data points, a clear correlation among the threading-dislocation density and the mobility-lifetime product is apparent.

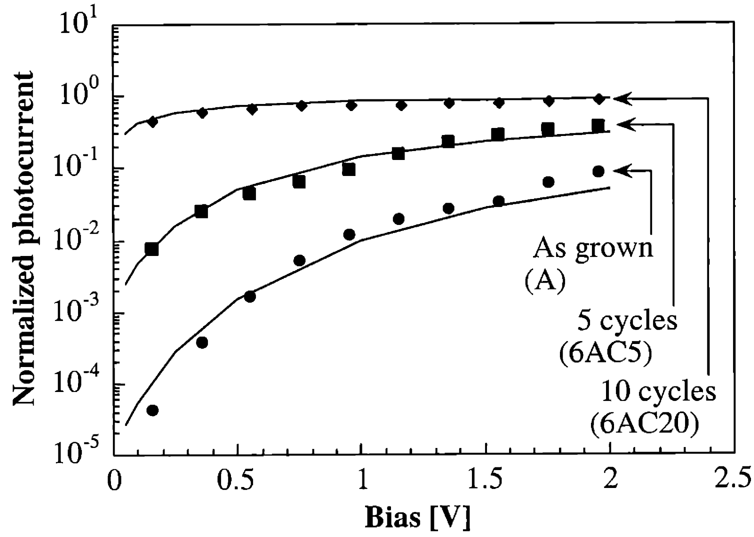



**Figure 4.11:** Photocurrent response of MSM devices at 1300 nm versus applied bias (symbols). The lines are fitted based on the Hecht model [193]. Cyclic thermal annealed samples reach maximum responsivity at lower bias voltages.

The MSM photodetector was also employed to measure the mobility of free carriers in the Ge film. The reduction in photocurrent pulse width versus applied bias was recorded in response to 100 ps light pulses at 1320 nm. Figure 4.12 shows the results from the sample with 20 annealing cycles (6AC20) at different biases. In the inset, the pulse width is plotted versus the inverse average electric field. The relationship between the pulse width and the inverse of the average electric field can be described by equation 2.12 and equation 2.14.

$$FWHM \propto t_r \propto \frac{W}{\mu} \cdot \frac{1}{\varepsilon} \tag{4.2}$$

From the slope of the linear fit, a mobility of 3500 $cm^2/Vs$ can be inferred. This value compares well with those reported for undoped Ge with negligible scattering at impurity sites.

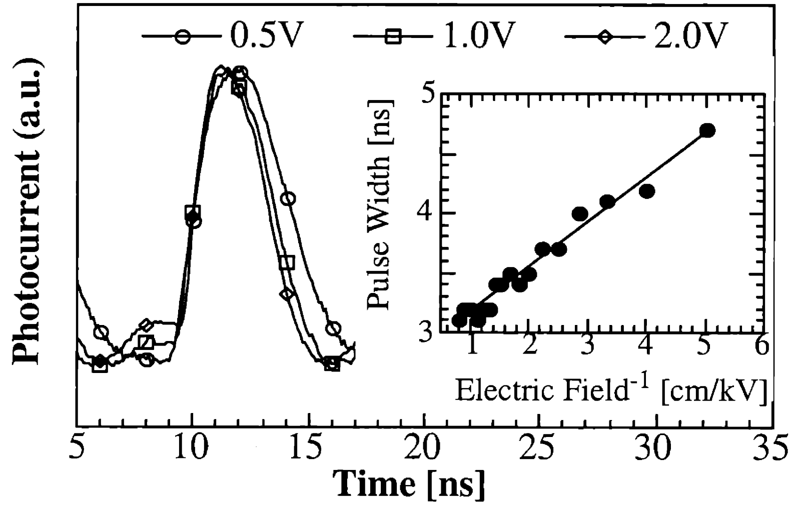



**Figure 4.12:** Photocurrent response of MSM devices illuminated by 100 ps pulses at 1.32 μm. The photodiodes were fabricated from Ge grown on Si treated by 20 annealing cycles (6AC20). In the inset, the pulse width dependence on the inverse of the electric field is plotted: the symbols are experimental data, the solid line is a linear fit. An electron mobility of 3500 $cm^2/Vs$ was estimated from this experiment.

In this section the performance of photodetectors based on epitaxial Ge grown on Si substrates using UHV/CVD followed by cyclic thermal annealing was discussed. The beneficial effect of the post-growth thermal annealing on the electrical properties of the Ge epilayers, due to the reduction of threading-dislocation densities, is confirmed by the dramatic enhancement of the performance of the photodetectors.

### 4.3.2 Performance of Ge p-i-n heterojunction photodetector

The purpose of this section is to discuss the effect that Si substrate doping and misfit dislocations at the Ge/Si interface have on the operation of Ge p-i-n heterojunction

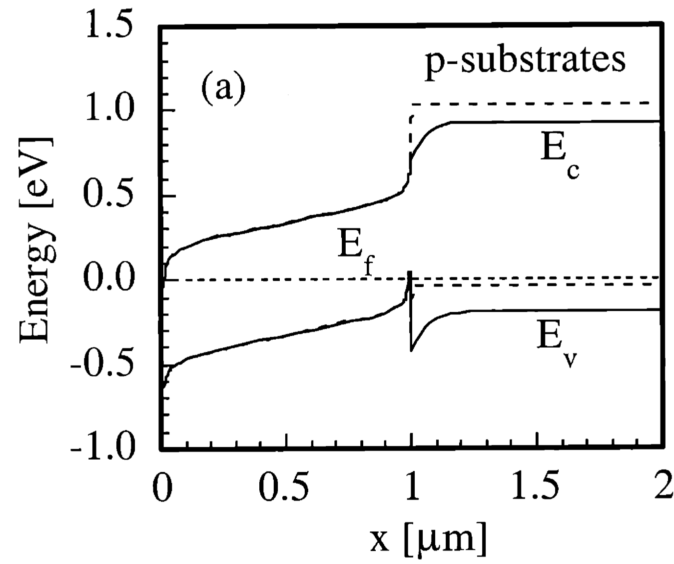
photodetectors. The Ge/Si heterojunctions can be modeled on the same grounds of the work of Milnes and co-workers [194] [226]. Based on a series of careful measurements of the I-V characteristics of Ge/Si heterojunctions, they proposed that the band alignment in Ge/Si heterojunction-diodes is modified significantly by acceptor-like interface defect-states in the forbidden gap due to the lattice mismatch between Ge and Si. As a consequence, both band bending and recombination of excess minority carriers were expected at the Ge/Si interface. Taking advantage of such physical ansatz, we numerically solved the pertinent Poisson and continuity equations using a one dimensional finite difference simulator [195]. According to Di Gaspare and co-workers, the energy gap difference between Si and Ge can be accounted for by the valence band discontinuity (0.36 eV) and the conduction band discontinuity (0.1 eV). These are used as the basis for the description of the band alignment between Ge and Si. The acceptor-like states at the Ge/Si heterojunction are modeled by the addition of a narrow distribution of p-type dopants in the charge contribution in the Poisson equation, and by a surface recombination velocity at the interface for the recombination/generation in the continuity equation. Thickness and height of the defect distribution were chosen in order to produce a net charge concentration equivalent to a surface state density of $5 \times 10^{13}$ $cm^{-2}$. Such a density is an estimation obtained from the difference in bond density on the free semiconductors surfaces ($\Delta N_s$): for the Ge/Si (100) case this is approximately equal to 8% of the surface bond density of Si. The surface recombination velocity ($S$) due to the defects is

$$S = \sigma v_{th} \Delta N_s \tag{4.3}$$

where $\sigma$ is the capture cross section and $v_{th}$ is the thermal velocity. For a typical value for capture cross section of about $10^{-14}$ $cm^2$, we obtain a surface recombination velocity of about $10^6$ cm/s [196]. The n-i-p structure is formed by a thin heavily doped $n^+$-Ge layer,

an intrinsic Ge layer (1 μm) and a p-Si substrate. The p-i-n structures are formed by a thin heavily doped $p^{+}$-Ge layer, an intrinsic Ge layer (1 μm) and a n-Si substrate.

Based on the above description, in Figure 4.13 (a) and (b) we plot the calculated equilibrium band diagrams for Ge/Si heterojunctions on p-Si and n-Si substrates, respectively. Calculations for two different resistivities (1 and 0.01 Ω-cm) are shown for both p-Si and n-Si substrates. It is apparent (Figure 4.13 (a)) that the built-in electric field in the Ge film maintains its orientation throughout the film thickness of n-i-p Ge diode on p-type Si. The situation for p-i-n Ge diode on n-type Si, on the other hand, is quite different. In this case (Figure 4.13 (b)), a pair of back-to-back diodes is formed due to the presence of acceptor-like interface states at the Ge/Si heterojunction.



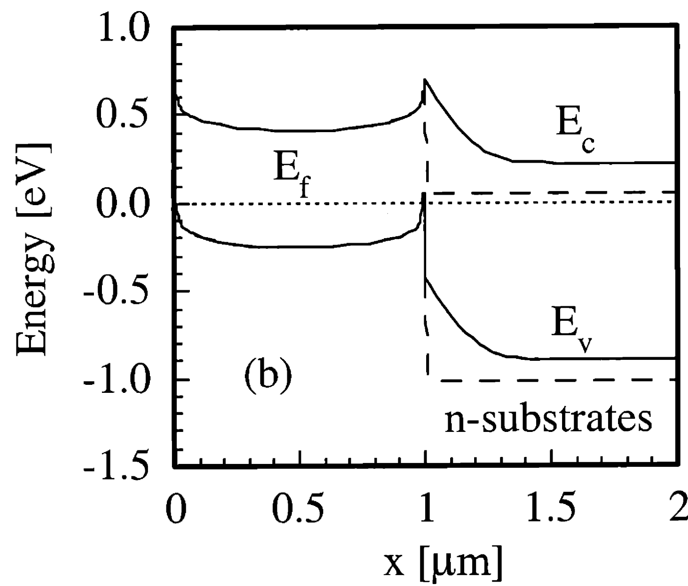
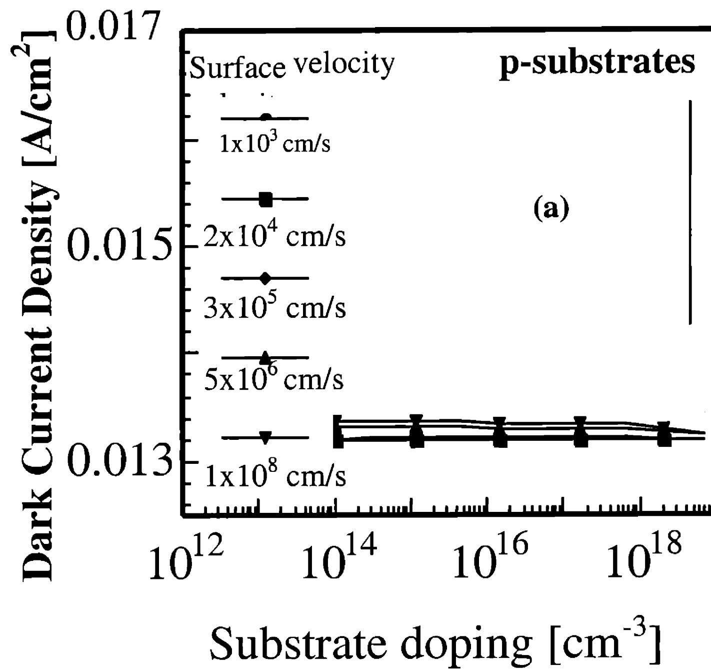




**Figure 4.13:** Calculated equilibrium band diagram of Ge/Si p-i-n diodes for (a) n-i-p Ge diode on p-Si substrates, and (b) p-i-n Ge diode on n-Si substrate. Continuous lines refer to calculated band diagram for substrates of resistivities of 1 Ω-cm. Dashed lines refer to calculated band diagram for substrates of resistivities of 0.01 Ω-cm.

Especially important is the barrier in the conduction band at the Ge/Si interface which can significantly affect the optoelectronic characteristics of the device. Comparing Figure 4.13 (a) and (b), we expect free carriers generated in the Ge film (either by thermal generation or optical excitation) to flow more easily in n-i-p Ge diodes integrated on p-Si than in p-i-n Ge diodes integrated on n-Si. To select the best substrate/layer combination we calculated the dark current and responsivity dependence on substrate resistivity and type. Figure 4.14 (a) and (b) display the calculated dark current at reverse bias of 1 V versus doping for the case of both p-Si and n-Si substrates. In both cases, a set of curves differing by the surface recombination velocity used in the calculation is presented to demonstrate the sensitivity of dark current on surface recombination velocity. As shown in Figure 4.14 (a), the current in n-i-p Ge diodes exhibits almost no dependence on surface recombination velocity and substrate doping concentration. The behavior of p-i-n devices is, on the other hand, quite different. Two regions of operation are clearly visible in Figure 4.14 (b). At high Si resistivity, the barrier in the conduction band at the Ge/Si interface (continuous line in Figure 4.13 (b)) prevents the applied reverse bias to extend into Ge. This impedes the extraction of the thermally generated carriers. Therefore, the calculated leakage current density for p-i-n Ge diodes on lightly doped n-Si is low. As the substrate doping is increased (lower Si substrate resistivities), however, barrier width and height at the Ge/Si interface are reduced (dashed line in Figure 4.13 (b)), the heterojunction is readily depleted by the applied voltage, and generation through defect-states (surface recombination velocity) becomes responsible for the increasing leakage current.



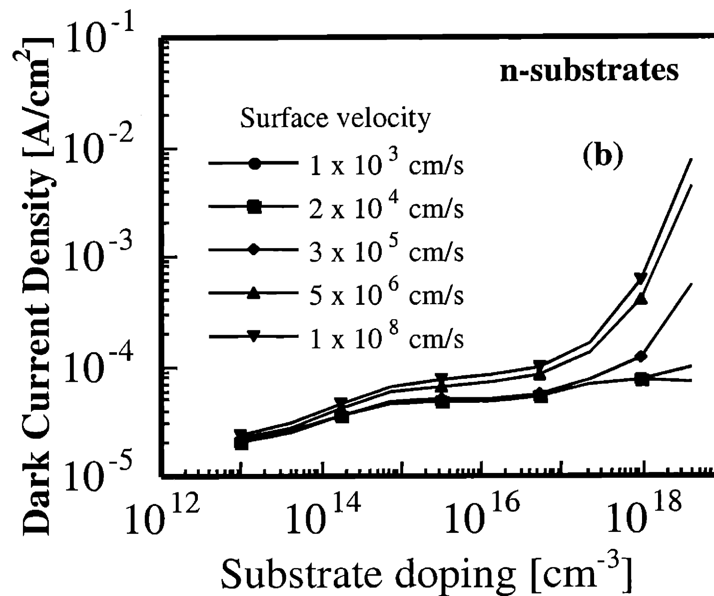




**Figure 4.14:** Calculated reverse dark current densities for Ge/Si p-i-n diodes with different substrate doping type and density. Curves differ for the surface recombination velocity at the Si/Ge interface used in the calculations.

The simulated responsivity at 1300 nm as a function of substrate resistivity is shown in Figure 4.15. Again, n-i-p Ge diodes show ideal behavior with an ability to fully collect photogenerated carriers, regardless the substrate resistivity and applied (reverse) bias voltage. On the other hand, the barrier at the Si/Ge interface in p-i-n diodes impedes the collection of photogenerated carriers: in this case, an increase in substrate doping (or a larger applied bias) helps to reduce the barrier height and increase the responsivity. It is clear from our simulation that n-i-p diodes are preferred for their better performance.

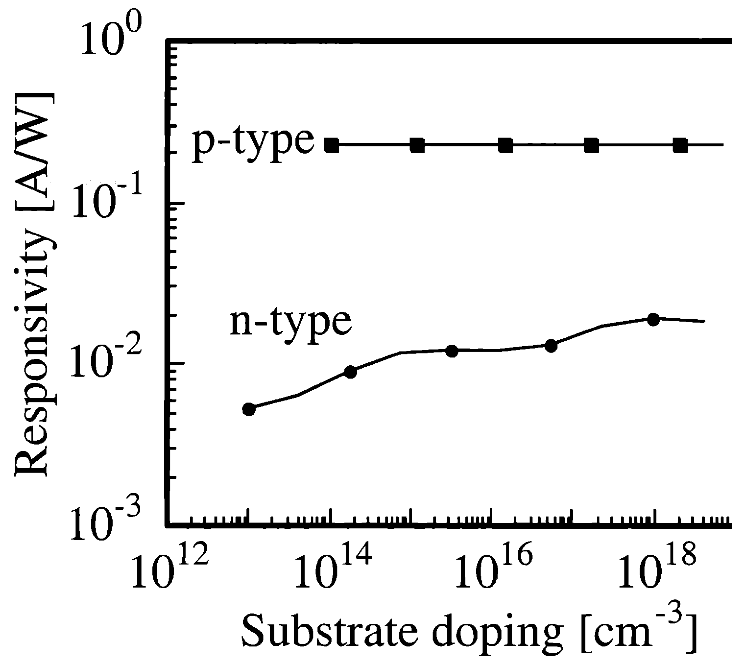
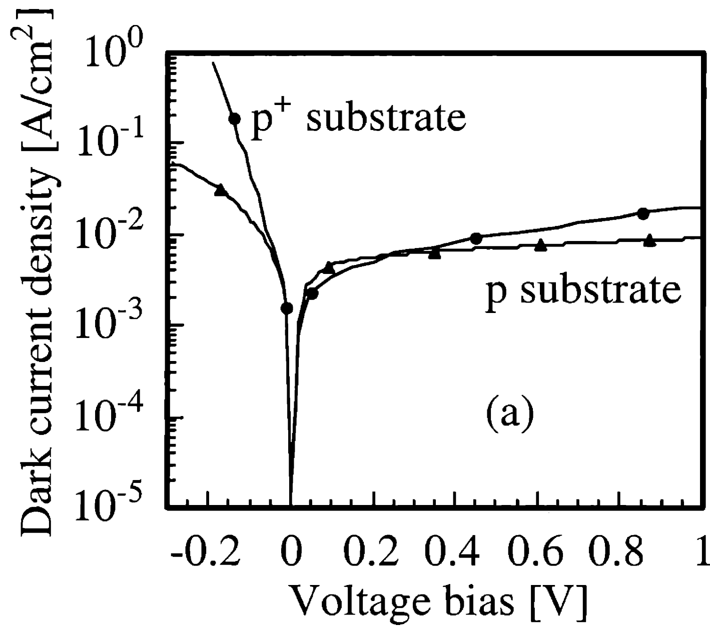



**Figure 4.15:** Calculated 1300 nm responsivity of Ge/Si p-i-n diodes as a function of the substrate doping.

For the electronic and optoelectronic characterization of p-i-n Ge diodes on n-Si substrates and n-i-p Ge diodes on p-Si substrates, we have selected substrate types and doping according to the analysis discussed above. The goal is to make photodiodes with high near-infrared responsivities at small reserve bias voltage and low reverse dark currents. For simplicity, we refer to diodes made on n-Si as n-diode, on $n^+$-Si as $n^+$-diode, on $p^+$-Si as $p^+$-diode and on p-Si as p-diode. Figure 4.16 shows the measured current-voltage characteristics of diodes grown on n-type and p-type Si. The diameter of the diodes reported here is 1.3 mm. All devices exhibited a well-pronounced rectifying response, with reverse current values and direction dependent on the substrate type (positive voltage applied to Ge). For $p^+$-diodes, we measured a reverse current density of 20 $mA/cm^2$ at a reverse bias of 1 V. However, from the forward characteristic at 0 V, a reverse current density lower than 2 $mA/cm^2$ can be estimated (Figure 4.16 (a)). This discrepancy is probably due to surface leakage. This proposal is supported by a study of the leakage current in $Si_{0.75}Ge_{0.25}$ p-n junction diodes by Giovane [5]. In Giovane's experiment, the leakage current in mesa isolated $Si_{0.75}Ge_{0.25}$ p-n junction diodes passivated by a thin PECVD $SiO_2$ become dominated by surface leakage current when the diode diameter is less than 3 mm. The threading-dislocation densities in $Si_{0.75}Ge_{0.25}$ p-n junction diodes studied by Giovane are similar to the densities in our Ge diodes. Since our Ge p-i-n junction diodes are smaller and are not passivated by $SiO_2$, we would expect surface leakage current to play a major role. The importance of controlling the surface is also supported by the experiment by Samavedam, where he reported a much reduced leakage current when mesa Ge p-n junction diodes grown on SiGe graded buffer layers are passivated by PECVD $SiO_2$ [55]. An introduction of a passivation process is expected to improve the reverse characteristics of $p^+$ diodes.



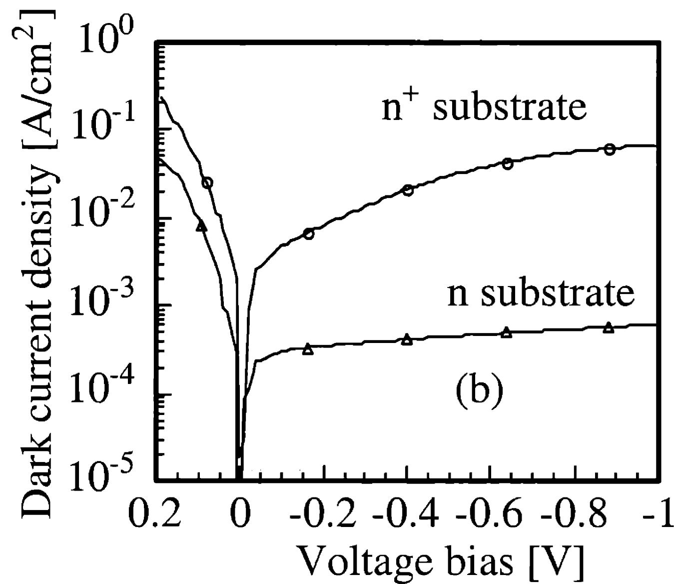




**Figure 4.16:** Measured dark current versus voltage for mesa p-i-n Ge/Si diodes grown on: (a) p-Si and $p^+$-Si substrates, (b) n-Si and $n^+$-Si substrates. For the $p^+$-Si case, the inferred diode ideality factor is 1.2 and the saturation current density at 0 V is 2 mA/cm$^2$. The reverse current at 1 V is 20 mA/cm$^2$.

In Figure 4.17 we show the measured 1300 nm responsivities of n-, p-, $p^+$- and $n^+$-diodes. As expected from the above discussions, the photocurrent is slightly dependent on the doping level of the substrate for the p-diodes, while it increases significantly with the substrate conductivity in n-diodes. The responsivity of $n^+$-diodes is comparable to the responsivity exhibited by the $p^+$-diodes. This does not agree with the simulation presented in Figure 4.15. However, when the out diffusion of dopant from the substrate (see SIMS profiles in Figure 4.4) is taken into account, the simulation agrees with our experiment. Figure 4.18 shows the calculated responsivity at 1300 nm of Ge p-i-n photodiodes integrated on n-Si substrate as a function of the substrate doping. The out diffusion of n-type dopants from the n-Si substrate results in much lower barrier at the interface due to a partial compensation of the defect charges and therefore an improvement in responsivity. It is worth emphasizing that the photocurrent of the $p^+$-diode saturates to the maximum value even in short circuit. The slightly larger saturated response of $n^+$-diodes can be attributed to their thicker intrinsic Ge layer with respect to that of the $p^+$-diode (Figure 4.4). When this difference is taken into account, and assuming an absorption coefficient of $10^4$ $cm^{-1}$ and reflection losses of 36%, an internal collection efficiency of 90% can be inferred for both the $n^+$-diode and $p^+$-diode. However, despite comparable responsivities of $n^+$- and $p^+$- diodes, the much lower dark current density of $p^+$- diodes makes them more attractive.

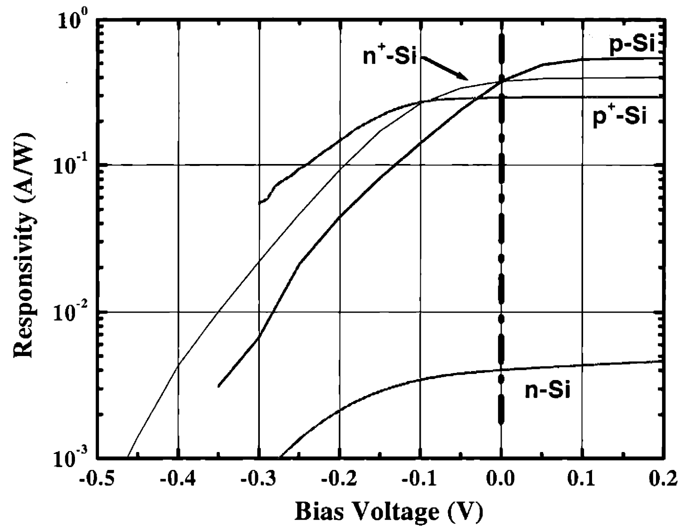



**Figure 4.17:** Measured photocurrent-voltage characteristics of mesa p-i-n Ge/Si diodes at 1300 nm.

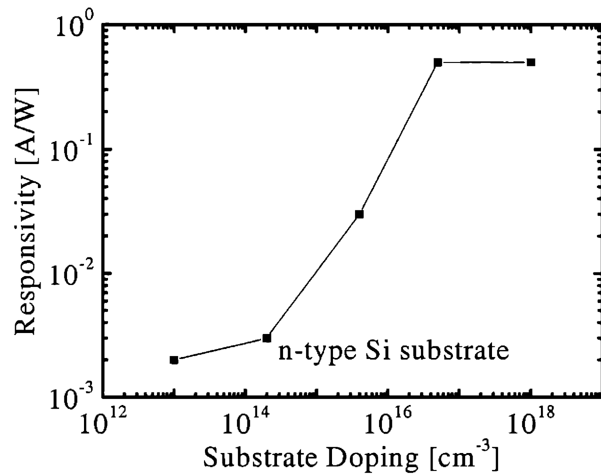



**Figure 4.18:** Calculated 1300 nm responsivity of Ge/n-Si p-i-n diodes as a function of the substrate doping considering the diffusion of dopant from the n-Si substrate.

Figure 4.19 shows the spectral responsivity of a $p^+$-diode in short circuit measured by exposing to a monochromatic light intensity of 0.1 mW/cm$^2$. The wavelength dependence of the measurement system has been corrected. Measured responsivities at 1300 nm and 1550 nm are 0.3 A/W and 0.2 A/W, respectively. A further improvement can be expected as the thickness of the Ge active layer is increased and appropriate antireflection coatings are adopted.

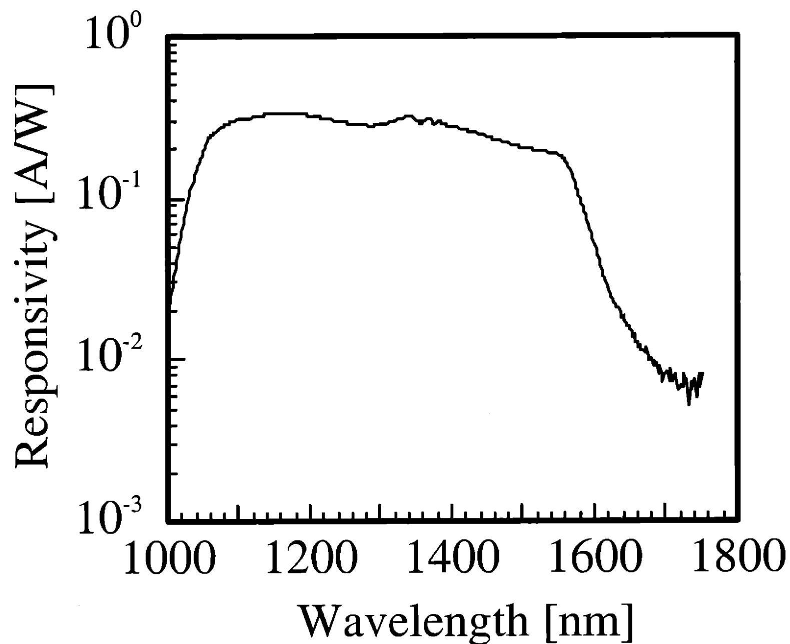



**Figure 4.19:** Measured short circuit spectral responsivity of a mesa p-i-n Ge photodiode fabricated on $p^+$-type Si.

In order to quantify the photoresponse speed of our p-i-n photodiodes, we recorded the photocurrent generated by a train of 100 ps light pulses at 1.32 μm produced by a Nd:YAG laser mode-locked at 100 MHz. The devices were biased through a 50 Ω resistor

and AC decoupled through a 100 pF capacitor. A minimum pulse duration of 800 ps FWHM was measured with the aid of a sampling scope. This represents a -3dB frequency of 380 MHz. Since devices with smaller areas exhibited proportionally faster responses, we can conclude that the speed was limited by the intrinsic capacitance.

### **4.3.3** Performance of n-i-p Ge (4 μm)/$p^+$-Si photodiodes

Discussion in section 4.3.2 pointed out that by increasing Ge thickness and including an anti-reflection (AR) coating, the responsivity of n-i-p Ge integrated on $p^+$-Si substrates can be improved. Including an anti-reflection coating enhances the light coupling efficiency. Increasing the Ge thickness increases the amount of light absorped by Ge and increases the number of electrons and holes generated by photons in Ge.

In this section, the performance of n-i-p Ge (4 μm) on $p^+$-Si is presented. The Ge thickness is increased to 4 μm to absorp a lot of light. Figure 4.20 shows the responsivity vs. voltage characteristics of n-i-p Ge (4 μm) on $p^+$-Si. Without the AR coating, the maximum responsivity measured was 550 mA/W, with AR (220 nm of $SiO_2$) coating it was 770 mA/W at 1300 nm. For these n-i-p diodes with 4 μm of Ge, about 0.1 V of reverse bias is necessary to achieve the maximum responsivity. This indicates that the built-in electric field is not enough to deplete the whole Ge section and a small voltage is necessary to collect all the photogenerated carriers. The measured responsivities for these n-i-p Ge/Si photodiodes are as good as those reported for Ge avalanche photodetectors operating at a multiplication factor of M~10 made by diffusion of dopants into pure Ge wafers [197] [198] [199] [200] [201] [202] [203].

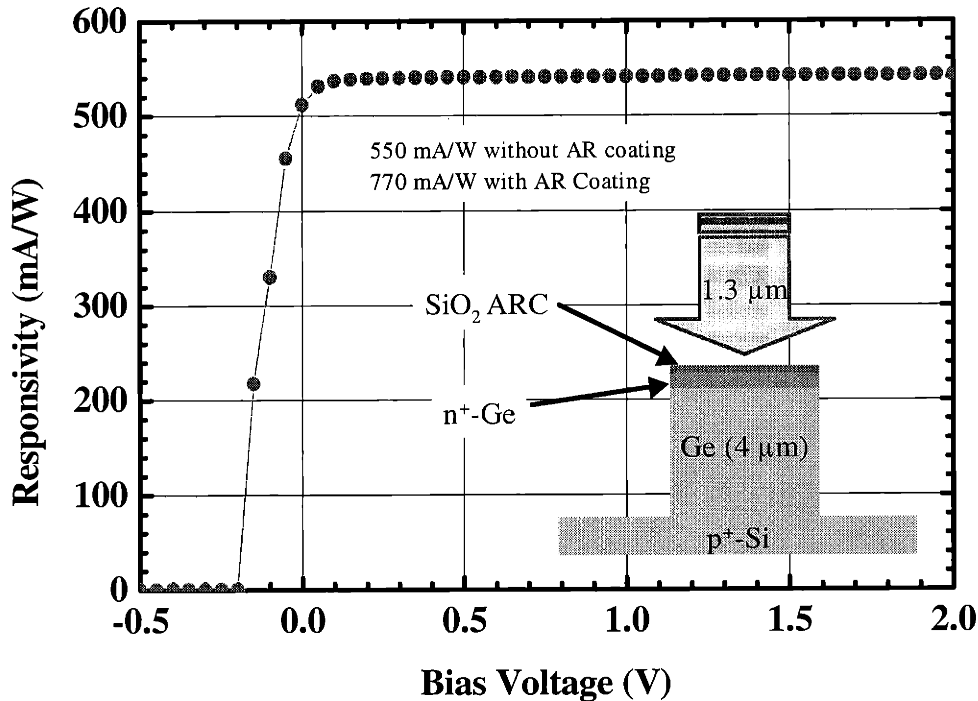



**Figure 4.20:** Responsivity of n-i-p Ge (4 μm) / $p^+$-Si photodiode with and without $SiO_2$ anti-reflection coating.

## 4.4 Conclusion

This chapter presented evidences that the improvement in Ge epilayer quality due to cyclic thermal annealing translates to improvement in performance of Ge photodetectors made on Si. The best performance measured was obtained from an n-i-p Ge/$p^+$Si photodiodes with responsivity as high as 770 mA/W at a reverse bias voltage of 0.1 V and wavelength of 1.3 μm. This proves that highly efficient Ge photodiodes can be integrated on Si using technology described in Chapter 3. The two remaining challenges are the control of surface leakage current and the integration of Si or $Si_3N_4$ waveguides with the

Ge photodiodes. The control of surface leakage current is discussed in chapter 5. The integration of Ge photodiodes with waveguides is described in chapter 6.

# Chapter 5

# Passivation of Ge epilayer surface

## 5.1 Overview

This chapter discusses the protection and passivation of Ge epilayers. The reason for studying the passivation of Ge epilayers is to reduce the surface leakage current. This chapter starts with a review of the work related to the passivation of Ge. That is followed by a description of the experimental procedure. The passivation is done by the thermal oxidation of Si epilayers grown on Ge. The quality of the passivation is characterized by the capacitance-voltage characteristics of the metal-oxide-semiconductor devices. This chapter provides evidence that high quality passivation of the Ge surface can be achieved by the thermal oxidation of Si epilayers grown on Ge.

## 5.2 Introduction

To achieve large scale integration of Ge photodiodes with Si microelectronics, it is important to develop technologies for the protection and passivation of a Ge epilayer. The protection of Ge in Si processing is important because Ge is known to have a very high etch rate in the SC-1 clean of the RCA clean solutions [204]. Passivation of the Ge surface is important because surface leakage current can be the dominant source of leakage current as the size of p-n junction diode becomes smaller [205]. A general discussion of surface leakage current can be found in the text book by Muller and Kamins [206]. To reduce surface leakage current, it is important to reduce the density of generation-recombination sites at the surface, and prevent the formation of inversion-charge or depletion regions close to the location where the p-n junction meets the surface dielectric film.

The passivation of Ge surfaces for the reduction of surface-leakage current in Ge avalanche photodiodes has been reviewed by Kaneda [203]. The goal of their experiments was to make sure that the Ge surface is not in inversion at 0V. They reported that CVD $SiO_2$ on Ge can produce an interface state density as low as $10^{12}$ $cm^{-2}eV^{-1}$ and is a good passivation for $p^+$-n diffused-junction diodes. The measured high-frequency capacitance-voltage (C-V) characteristics showed significant hysteresis. For $n^+$-p diffused-junction diodes, they proposed the use of a CVD $Si_3N_4/SiO_2$ double-layer structure [207]. Another proposal for the reduction of surface leakage current in Ge p-n junction diodes is the oxidation of sputtered Si film on Ge by Chikao and co-workers [208]. Because the band gap of Si is much higher than that of Ge, they proposed that the generation current at the interface between $SiO_2$ and Si can be much smaller compared to the interface between $SiO_2$ and Ge. They did not report any experimental results.

A review of the passivation of Ge surfaces, either by the oxidation of Ge or by the deposition of dielectric materials on Ge, has been published by Meiners and Wieder [209]. These two methods typically do not provide adequate passivation of the Ge surface. A more effective way to passivate the Ge surface is the method proposed by Vitkavage and co-workers [210] [211] [212] [213] [214] [215]. In this method, a thin pseudomorphic Si layer (on the order of 1 nm) is first deposited on Ge at 350°C. Following the Si deposition, $SiO_2$ was deposited at 300°C. Both Si and $SiO_2$ were deposited by plasma-enhanced CVD (PECVD) process. They measured almost ideal C-V characteristics and reported an interface state density of $3x10^{10}$ $eV^{-1}cm^{-2}$. This idea has also been applied to the passivation of GaAs and InGaAs [216] [217] [218] [219] [220]. All these reports

described methods based on the deposition of a thin pseudomorphic Si layer and the deposition of $SiO_2$ or $Si_3N_4$ film by plasma-enhanced CVD or photon-enhanced CVD.

In Si microelectronic technology, the gate oxide is typically grown by thermal oxidation. CVD $SiO_2$ is usually of lower quality compared to thermal oxide and is usually not used as a gate oxide. If Ge passivation can be done by thermal oxidation rather than low-temperature PECVD, the integration of Ge photodiode process with Si CMOS process can be more flexible. However, it is usually necessary to clean the wafers in RCA clean solutions before thermal oxidation. The etch-rate of Ge in RCA clean solutions is quite high [204]. It is therefore necessary to provide a protection layer for the Ge epilayer if Si wafers coated with Ge epilayers were to be cleaned in RCA clean solutions. One nanometer of pseudomorphic Si does not provide enough protection of Ge in the RCA clean bath. In this chapter, we report the passivation of Ge epilayers, grown on Si using UHV/CVD, by the thermal oxidation of Si (50 nm) epilayers deposited on the Ge epilayers.

## 5.3 Experimental procedure

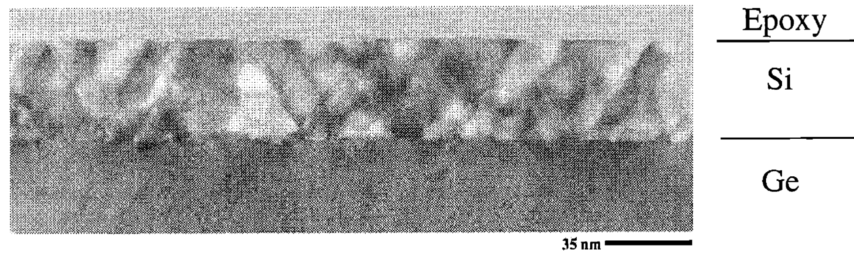
Heavily doped p-type Si wafers (0.008-0.02 Ω-cm) were used as substrates for Ge heteroepitaxy. The growth of the Ge epilayer was done by a procedure similar to that reported in Chapter 3. After about 1 μm of Ge was deposited on Si at 600°C, the $GeH_4$ flow was terminated and the Si layer growth was carried out in-situ immediately by interrupting the flow of $GeH_4$ while commencing the flow of $SiH_4$. The Si deposition temperature was maintained at about 600°C and 20 sccm of $SiH_4$ was flowed for 1 hour. At the end of this process, about 50 nm of Si was deposited. Because the Si CVD process

at 600°C is limited by surface reaction, the Si epilayer surface is flat with low surface-roughness similar to that of the Ge epilayer. After epitaxy, the Si/Ge/$p^+$-Si structure was cyclically annealed between 900°C and 780°C 10 times. The Si/Ge/$p^+$-Si structure was then cleaned in the RCA clean solutions. The Si layer can protect the Ge epilayer in the RCA clean chemistry. The etch rate of Si in the SC-1 clean solution of the RCA clean, which consists of $NH_4OH$, $H_2O_2$ and $H_2O$, has been calibrated by Jackson [221]. After cleaning, the silicon layer was oxidized by thermal oxidation in a conventional, atmospheric oxidation furnace by flowing dry $O_2$ at 850°C for 185 minutes. At the end of the oxidation process the whole structure was annealed in dry Ar at 850°C for 30 minutes to reduce fixed oxide charge density. This oxidation process produced about 21 nm of $SiO_2$.

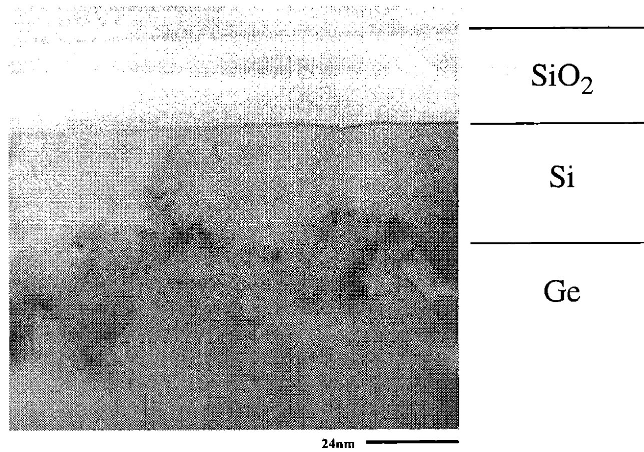
MOS structures were fabricated by thermally evaporating aluminum through a shadow mask. The quality of the oxide/semiconductor interface was characterized by measuring the capacitance-voltage (C-V) characteristics of the MOS structure. The use of $p^+$-Si substrate ensures that the junction capacitance at the Ge-epilayer/$p^+$-Si-wafer heterojunction does not affect the C-V characteristics. The back side of the sample is fully metallized to reduce parasitic capacitance. The C-V measurements were carried out in the dark and the gate voltage was swept only after a steady-state condition was reached. The sweep rate was slower than 0.5 V/s. Measurements were done at 1 MHz to 300 Hz and from room-temperature (300 K) to liquid-nitrogen temperature (77 K). The structure of the $SiO_2$/Si/Ge interface was studied by cross-sectional TEM and high-resolution TEM.

## 5.4 Results and discussion

Figure 5.1 (a) shows a cross-sectional TEM micrograph of a thin Si epilayer grown on Ge epilayer. This figure demonstrates that the interface between Ge and Si is quite flat. Since the thickness of the Si layer is much larger than the critical thickness for the introduction of misfits dislocations in Si grown on Ge, dislocations are visible in the Si layer. Figure 5.1 (b) is a cross-sectional TEM micrograph of the structure shown in Figure 5.1 (a) after thermal oxidation. The $SiO_2$/Si interface is flat. The interface between the remaining Si epilayer and Ge, however, is not. There are V-shaped defects at the Si/Ge interface. These are probably due to the thermal mismatch between Si and Ge. The distinction between Si and Ge is also not clear. This is probably due to inter-diffusion between Si and Ge at high temperature. TEM studies at lower magnification showed that the threading-dislocation density in the Ge epilayer was not reduced by cyclic thermal annealing and thermal oxidation. The threading-dislocation density remains on the order of $10^9$ $cm^{-2}$.




(a)




(b)

**Figure 5.1:** (a) Cross sectional TEM micrograph of a Si epilayer grown on the Ge epilayer. (b) Cross sectional TEM micrograph of a Si epilayer grown on Ge, with $SiO_2$ grown by thermal oxidation as the topmost layer.

Although the interface structure between Si and Ge is not perfect, the electrical properties of the MOS structure is adequate for this application. Figure 5.2 (a) shows the measured capacitance-voltage (C-V) characteristics. Accumulation, depletion and inversion regimes are clearly visible. There is no detectable hysteresis in the 1 MHz C-V curve. The hysteresis is typically thought to be caused by slow interface states on the insulator side of the interface [216] [213]. The lack of hysteresis in this system could be an indication of the high quality of the $SiO_2$/Si interface. The difference in the accumulation capacitance measured at 1 MHz and 500 Hz, however, suggests that there are slow interface states

close to the valence band edge that cannot follow the 1 MHz measurement signal. These states might be related to the region within the Si layer between the $SiO_2$ layer and Ge.

The characteristic time to form an inversion layer at the surface of an MOS system biased to inversion is of the order of $2N_a\tau_0/n_i$, where $\tau_0$ is the minority carrier lifetime [206]. We were able to measure inversion capacitance at 500 Hz. This indicates that the minority carrier lifetime is on the order of $10^{-8}$~$10^{-7}$ s. Minority carrier lifetime in this range is expected for Ge with threading-dislocation density on the order of $10^9$ $cm^{-2}$. The accumulation capacitance and the inversion capacitance are quite similar. This shows that there is little oxide leakage current. The flat band voltage for this sample is -2 V. This is measured from a plot of $1/(C_{hf}/C_{ox})^2$ as a function of gate-voltage [213]. From the analysis of depletion capacitance as a function of the bias voltage, the doping concentration in the Ge epilayer was estimated to be about 1.3 x $10^{17}$ $cm^{-2}$.

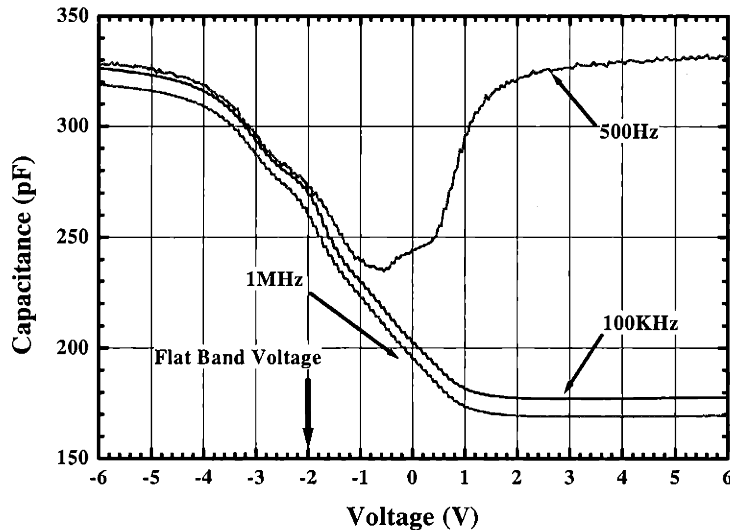



**Figure 5.2:** Capacitance-voltage characteristics of $SiO_2$/Si/Ge/$p^+$-Si structure.

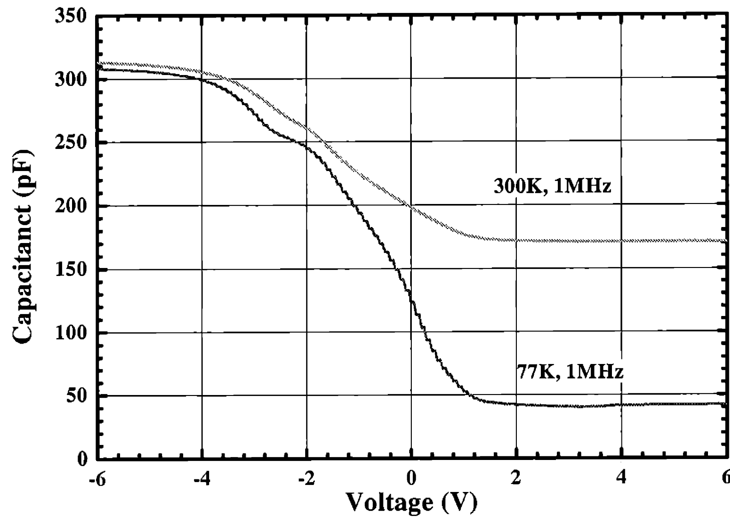



**Figure 5.3:** High frequency C-V curve measured at 300K and 77K.

Figure 5.3 shows the high-frequency C-V curve at 1 MHz measured at 300K and 77K. The accumulation capacitances measured at 300K and 77K are similar. This suggests that real accumulation has occurred and the Fermi level is not pinned by the interface [209] [223].

For further analysis, Figure 5.4 compares the C-V curve measured at 1 MHz to the theoretical C-V curve. The theoretical C-V was calculated assuming perfect interface between $SiO_2$ (21 nm)and Ge ($N_A = 1.3 \times 10^{17}$ $cm^{-2}$) with no insertion of the Si layer. The flat band voltage of the calculated C-V curve is shifted to the measured value (-2 V). The measured C-V curve is stretched out along the gate voltage axis. This suggests that the interface has traps that can respond to dc gate voltage [222].

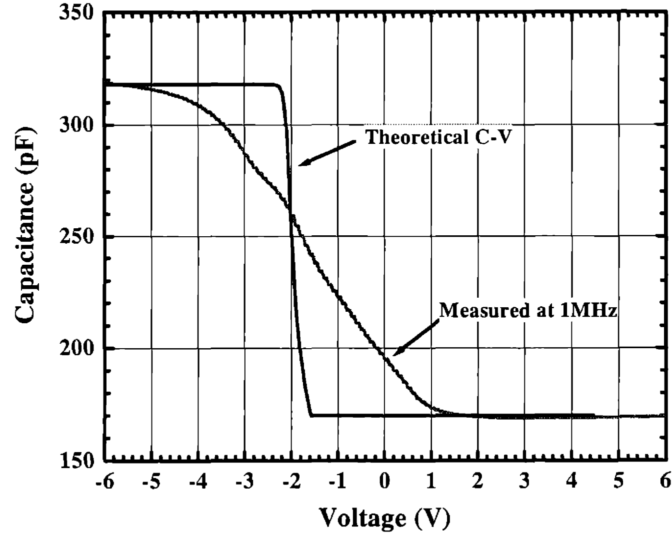



**Figure 5.4:** Comparison of measured C-V curve (1 MHz) and calculated C-V curve.

To estimate the interface state density, we applied Berglund's method and used

$$D_{it} = \frac{C_{ox}}{q}\left(\frac{C_{lf}/C_{ox}}{1 - C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1 - C_{hf}/C_{ox}}\right) \qquad (5.1)$$

where $D_{it}$ is the interface state density, $C_{ox}$ is the oxide capacitance, $C_{lf}$ is the low-frequency capacitance and $C_{hf}$ is the high-frequency capacitance. The surface potential ($\phi_S$)is calculated by

$$\phi_S = \int_{V_{FB}}^{V_{G2}}\left(1 - \frac{C_{lf}}{C_{ox}}\right)dV_G \qquad (5.2)$$

where $V_{FB}$ is the flat-band voltage, and $V_G$ is the gate-voltage.

Figure 5.5 shows the measured interface state density as a function of surface potential. Berglund's method is used instead of Terman's method because Terman's method requires the comparison of the measured and theoretically calculated C-V curve. The Si layer between $SiO_2$ and Ge makes the accurate calculation of the theoretical C-V curve difficult. Berglund's method, on the other hand, allows the estimation of interface state density using only the measured capacitances without further assumption. The sample that received cyclic thermal annealing has a lower interface state density compared to the sample that did not receive cyclic thermal annealing. The lowest interface state density measured is about $4 \times 10^{11}$ $cm^{-2}eV^{-1}$. This is quite low considering the fact that the thin Si layer between Ge and $SiO_2$ is quite defective. The calculated surface potential range is about 0.7 eV. This is quite large considering that the Ge band gap is 0.66 eV at room temperature. Nevertheless, it is clear that the Fermi level can swing from the Ge valence band edge to the Ge conduction band edge.

In chapter 4, it was suggested that the interface between Ge and Si has acceptor-like interface states. These interface states at the Ge/Si interface can pin the Fermi level to the valence band. Figure 5.5, on the other hand, clearly shows that the Fermi level can be swept from the valence band all the way to the conduction band in the presence of Si/Ge interface. An explanation to this contradiction might be that the Ge/Si interface studied in Chapter 4 is decorated by oxygen and carbon. Oxygen and carbon contamination at the epi/wafer interface is typical and has been confirmed by SIMS profiling for our samples. Different from the epi/wafer interface, the Si-epi/Ge-epi interface is not contaminated by oxygen and carbon. This is because the Si layer is grown in-situ in the UHV/CVD chamber. The fact that the misfit dislocations at the Si-epi/Ge-epi interface are not

decorated by oxygen and carbon might be the reason why the pinning effect reported in chapter 4 is not seen in the MOS structures reported here.

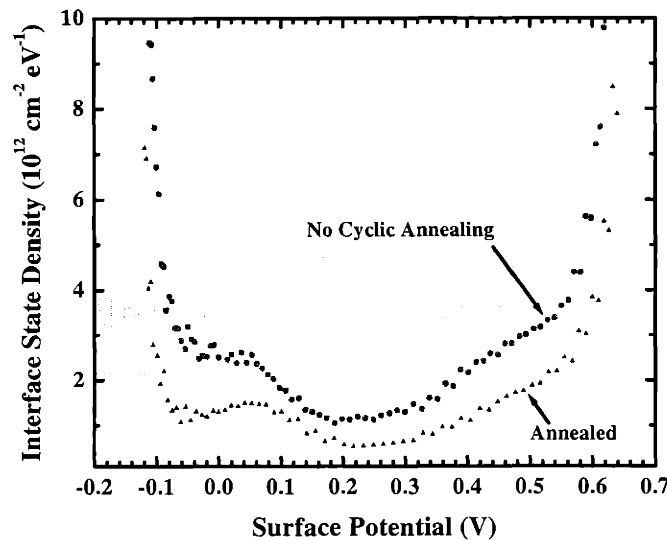



**Figure 5.5:** Measured interface state density as a function of surface potential.

It is important to determine whether this technology for the protection and passivation of Ge epilayers is useful. From the TEM pictures, we know that the Si layer was effective in protecting the Ge epilayer. This definitely shows that the in-situ grown Si can improve the stability of the system and protect Ge in the RCA clean solutions. The C-V characteristics of the MOS devices shows that the surface potential can be swept from the conduction band to the valence band. This clearly demonstrates that the $SiO_2$/Si interface is of high quality. Surface leakage current reduction using the gated-diode structure can certainly be applied [205]. The flat-band voltage can be shifted by using metals other than Al for contacts on the $SiO_2$ and therefore avoid the inversion charge at 0 bias voltage. The major

disadvantage of the procedure described in this chapter is that the ability for the reduction of threading-dislocation density by cyclic thermal annealing is lost when the Ge surface is covered by Si. The reason for the high threading-dislocation density left after annealing in the case with Si epilayer on Ge, as compared to the experiment discussed in Chapter 3 where there is no Si epilayer, can be explained by the blocking of dislocation movement by the surface Si epilayer. To solve this problem, it might be necessary to carry out in-situ cyclic thermal annealing before the deposition of Si.

The lowest interface state density reported in this chapter is $4 \times 10^{11}\ cm^{-2}eV^{-1}$. From the low hysteresis of the C-V curve, we know that the $SiO_2$/Si interface state density is low. It is therefore, reasonable to suggest that extra interface states are due to the defects in the Si layer and the Si-epi/Ge-epi interface. To further reduce the interface state density, it might be necessary to reduce the defects in the Si layer. This can be done by calibrating the oxidation rate and reduce the Si layer thickness to below the critical thickness by oxidizing much of the Si layer. To prevent the V-shape defects, low temperature oxidation at the Si growth temperature might be necessary.

## 5.5 Conclusion

This chapter presented evidence that a high quality passivation of Ge can be done by the thermal oxidation of an Si epilayer grown in-situ on Ge. Interface state density as low as $4 \times 10^{11}\ cm^{-2}eV^{-1}$ was achieved and the surface potential can be swept from the valence band to the conduction band.

# Chapter 6

# Summary and future work

## 6.1 Summary of thesis

This thesis presents conclusive evidence that thermal annealing can reduce threading-dislocation density in Ge grown directly on Si, and hat thermal annealing of small Ge mesas selectively grown on Si can provide virtually perfect Ge material on Si. This work demonstrates that it is possible to measure threading-dislocation density by both plan-view TEM and EPD techniques. The reduction of threading-dislocations can be attributed to the thermal stress induced dislocation glide and annihilation. Threading-dislocations related to the pure-edge dislocations (sessile dislocations) that were thought to be permanent dislocations were found to be removable. This thesis also presents conclusive evidence that high performance Ge photodiodes can be integrated on Si using direct epitaxial growth. The beneficial effect of the thermal annealing process on the performance of Ge photodiodes is clearly demonstrated. As a first step towards the integration of Ge photodiodes with Si microelectronic technology, thesis provides evidence that the passivation of Ge epilayer can be accomplished by the thermal oxidation of Si epilayers grown on Ge. This Si epilayer on Ge provides adequate protection of Ge in Si wafer cleaning chemistry.

## 6.2 Future Work

This thesis provided the basic materials technology for the direct integration of Ge photodetectors on Si. While there are many interesting topics related to the study of defects in Ge, the focus of future work should be on the development of a fully integrated

photodetector receiver for Si microphotonics. The main challenge is to design a process for the integration of Si or $Si_3N_4$ waveguides with Ge photodiodes and Si microelectronics. Focusing on the Ge photodiodes, the goals are to have integrated photodiodes with high quantum efficiency, high speed, low leakage current, high reliability and high Si microelectronic process compatibility. Here are some suggestions on how to accomplish these goals:

1. Materials Design: Ge with almost zero threading-dislocation density can be integrated on Si by the combination of selective area growth and cyclic thermal annealing. The limit of this process, however, is that the selectively grown Ge square mesas need to be on the order of 10 μm in width. For some applications, this might be too small. The solution to this challenge is simple. Since dislocations glide along the <110> directions, it is only necessary to have the distance between mesa sidewalls short along the <110> directions as shown in Figure 6.1 .

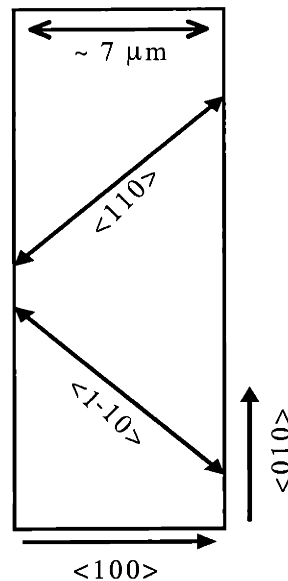



**Figure 6.1:** Geometry for the reduction of threading-dislocations by gliding to mesa sidewalls.

Another challenge is related to the melting temperature of Ge and the annealing temperature necessary for threading-dislocation reduction. The melting temperature of Ge is 939°C. This is lower than some processing temperatures in current Si CMOS technology. A solution to this challenge is to add a small fraction of Si into Ge to increase the melting temperature. The limit of this solution is the reduction in the absorption coefficient with the addition of Si. The limit of annealing temperature requires some more experiments. Based on experiments presented in this thesis, it should be possible to reduce threading-dislocations by annealing at temperature as low as 850°C.

2. Process Compatibility: The key characteristics of current Si CMOS technology is its planar structure. Using planar structure allows the high density integration of transistors, many layers of metal interconnects and the possibility of three dimensional integration. It is desirable to integrate Ge photodiodes with Si CMOS technology using processes that preserves the planar structure. Selective epitaxial growth of Ge is a good start. Planarization processes should be researched to take full advantage of the planar integration scheme.

3. Optical Design: To have highly efficient Ge photodiodes, it is important to improve the optical coupling efficiency. In Si microphotonic systems, this means that we want to couple as much optical power from the waveguide into the Ge photodiode as possible. The coupling of optical power between waveguide and photodiodes for the Si microphotonic systems has been discussed by Desmond Lim in his PhD thesis to some extent [60]. Considering the process capability of typical thin film deposition processes, vertical coupling is much easier than butt coupling. To preserve planar geometry using

vertical coupling, two structures are possible. Vertical coupling with Ge photodiode on top of the Si waveguide is shown in Figure 6.2.

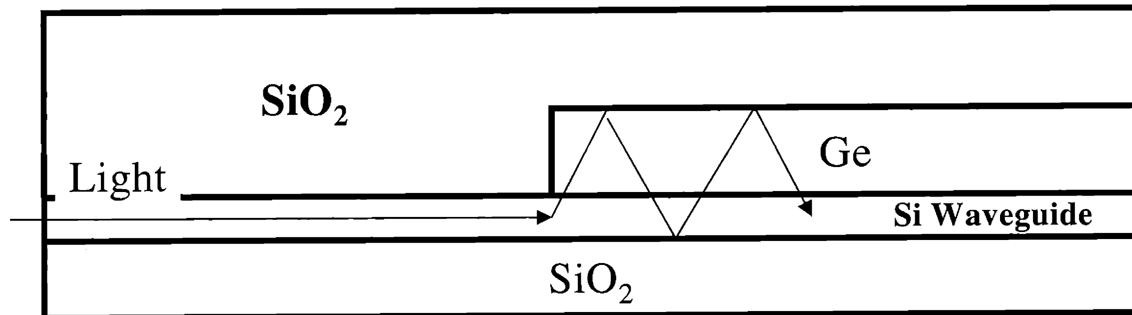



**Figure 6.2:** Vertical coupling of Ge photodiode with Si waveguide. Ge photodiode is on top of the Si waveguide.

The geometry shown in Figure 6.2 allows high-efficiency optical coupling between Si waveguide and Ge photodiode. This is because the index difference at the $SiO_2$/Si and $SiO_2$/Ge interface helps the reflection and therefore allows the light to be guided in the Ge and Si layers. Planarity of the structure can be maintained by depositing a thick $SiO_2$ on top of Ge and polishing the $SiO_2$ layer. However, to allow the single crystal growth of Ge, Si-on-insulator (SOI) wafers are necessary. The thickness of Ge has to be about 1 $\mu$m for the thermal annealing process to be effective in reducing threading-dislocation density. It is not clear if this is acceptable for integration with Si CMOS process.

One way to get around this limit is to have the waveguide on top of the Ge photodiode as shown in Figure 6.3. This is similar to the structure described in Figure 2.2.

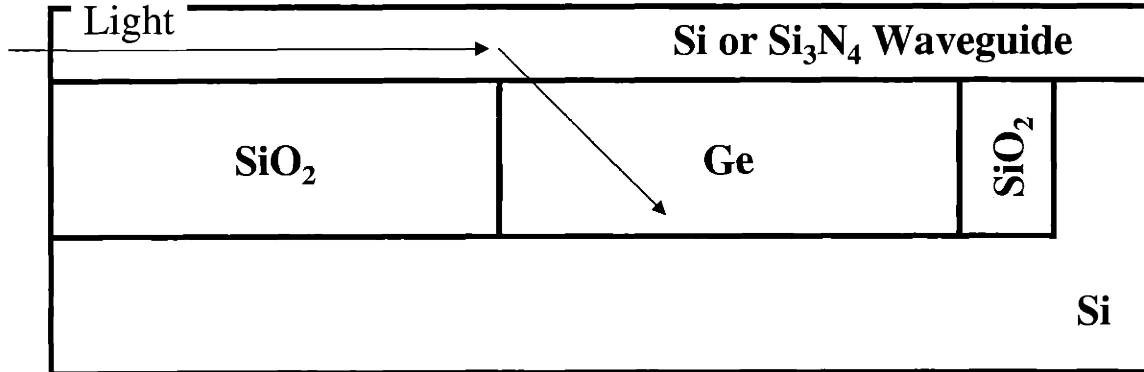



**Figure 6.3:** Vertical coupling of a Ge photodiode with Si or $Si_3N_4$ waveguide. Ge photodiode is under the waveguide.

The advantage of the structure shown in Figure 6.3 is that it preserves the planar structure on the wafer surface. Both Si or $Si_3N_4$ waveguide can be used in this geometry. Simulation shows that when light is coupled into the Ge photodetector, the light travels at about 45 degree angle. This increases the absorption length by a factor of the square root of two. With 1 μm of Ge and an absorption coefficient of $10^4$ $cm^{-1}$, 75% of the light can be absorped. With 2 μm of Ge, 94% of the light can be absorped. If the absorption coefficient is lower than $10^4$ $cm^{-1}$ as in the case of Ge at the wavelength of 1550 nm, it is necessary to improve optical coupling efficiency. To further enhance the optical coupling efficiency, an SOI wafer can be used. This would provide a thin $SiO_2$ layer under the Ge photodiode and reflect light back into the Ge photodiode. The use of SOI wafer, of course, adds to the compexity of the process.

4. Device Design: An efficient photodiode should have a high carrier collection efficiency at relatively small bias voltage. To achieve high carrier collection efficiency,

design of the doping profile in the photodiode is important. Figure 6.4 shows the design of a vertical p-i-n Ge photodiode integrated with a $Si_3N_4$ waveguide. The advantage of this structure is that it is possible to grow the p-i-n structure by in-situ doping. If diffused (or implanted) junction is more desirable, this vertical structure needs only one diffusion (or implantation) step. The disadvantage is that the contact to the $p^+$-Si needs a via through the $SiO_2$ layer on the side. If this is not done correctly, the series resistance can be high and results in high RC delay. In-situ Boron doping is known to degrade the selectivity of Ge growth on $SiO_2$. Some CVD studies might be necessary to resolve this issue.

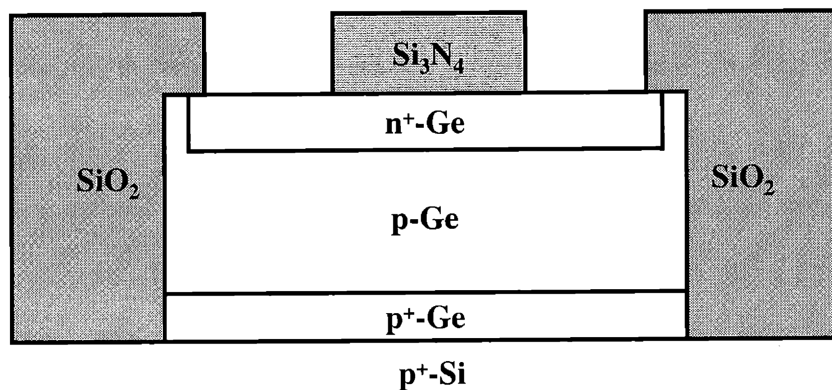



**Figure 6.4:** Design of a vertical p-i-n Ge photodiode grown on Si integrated with a $Si_3N_4$ waveguide.

Another possible structure is the lateral p-i-n structure shown in Figure 6.5. This structure is similar to the structure shown in Figure 2.2 The advantage of this structure is that the structure is similar to MOSFET. Both contacts to the $p^+$-Ge and $n^+$-Ge can be formed from the top. The lateral p-i-n structures have much smaller junction capacitance compared to the vertical p-i-n structure. The disadvantage is that two diffusion (or implantation) steps are needed.

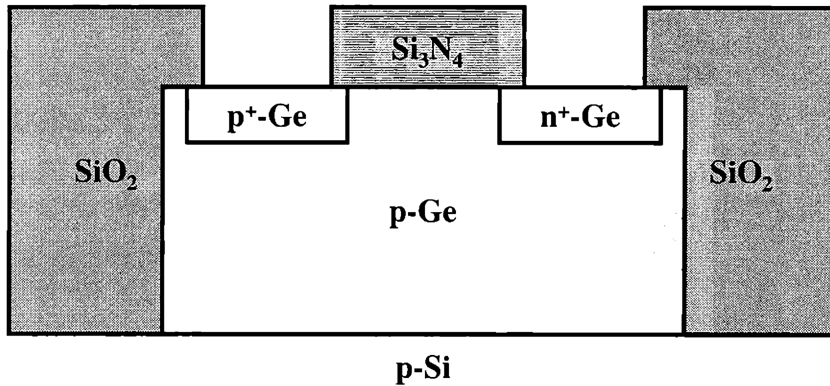



**Figure 6.5:** Design of a lateral p-i-n Ge photodiode grown on Si integrated with a $Si_3N_4$ waveguide.

To collect all the carriers and achieve high speed operation, it is important to have the depletion region covering the whole Ge epilayer. This can be done by making sure that the lightly doped p-Ge region has low enough doping concentration. Figure 6.6 shows the calculated depletion width of an $n^+$-p diode. If the doping concentration in the lightly doped region can be kept below 1 x $10^{16}$ $cm^{-3}$, it should be possible to deplete 1 $\mu$m of Ge with a small reverse bias voltage and therefore ensure a fast and efficient photodiode.

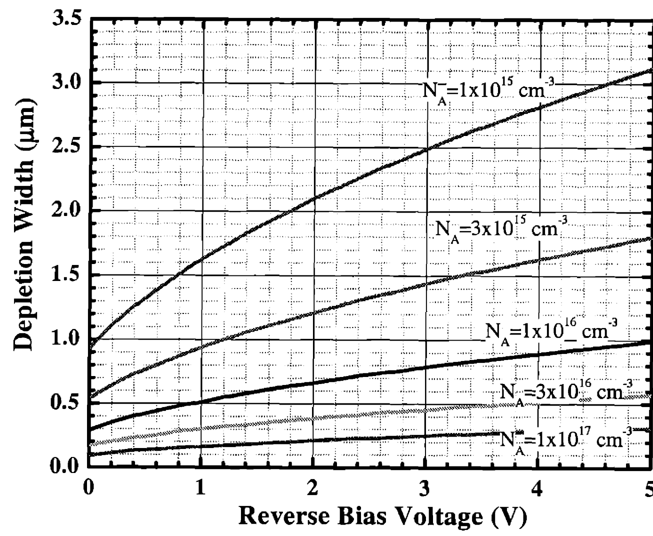



**Figure 6.6:** Depletion width of an $n^+$-p Ge diode as a function of voltage and doping concentration.

# References


[1] L. C. Kimerling, "Silicon microphotonics," *Applied Surface Science*, **159**, 8 (2000).

[2] B. Zhen, J. Michel, F. Y. G. Ren, D. C. Jackson, J. M. Poate, and L. C. Kimerling, "Room temperature sharp line electroluminescence $\lambda$=1.54 μm from an erbium-doped silicon light-emitting diode," *Applied Physics Letters*, **64**, 2842 (1994).

[3] D. R. C. S. Lim, *Device integration for silicon microphotonic platforms,* Ph. D. Thesis, Massachusetts Institute of Technology, 2000.

[4] K. K. Lee, *Transmission and routing of optical signals and on-chip waveguides for Si microphotonics*, Ph. D. Thesis, Massachusetts Institute of Technology, 2001.

[5] L. M. Giovane, *Strain-balanced silicon-germanium materials for near IR photodetection in silicon-based optical interconnects,* Ph. D. Thesis Massachusetts Institute of Technology, 1997.

[6] A. E. White, "Wavelength division multiplexing (WDM) has arrived," *Optics & Photonics News*, March 2000, 27 (2000).

[7] D. R. Goff, *Fiber optic reference guide: Apratical guide to the technology,* Boston: Focal Press, Second Edition, 1999.

[8] S. Luryi, A. Kastalsky, and J. C. Bean, "New infrared detector on a silicon chip," *IEEE Transactions on Electron Devices*, **31**, 1135 (1984).

[9] A. Kastalsky, S. Luryi, J. C. Bean, T. T. Sheng, "Single-crystal Ge/Si infrared photodetector for fiber-optic communications," *Proceedings of the First International Symposium on Silicon Molecular Beam Epitaxy,* p. 406, (1985).

[10] S. Luryi, T. P. Pearsall, H. Temkin, J. C. Bean, "Waveguide infrared photodetectors on a silicon chip," *IEEE Electronics Device Letters*, **EDL-7**, 104, (1986).

[11] R. People, "Indirect bandgap of coherently strained $Ge_xSi_{1-x}$ bulk alloys on (001) silicon substrate," *Physical Review,* **B32**, 1405 (1985).

[12] R. People, "Physics and applications of $Ge_xSi_{1-x}$/Si strained layer heterostructures," *IEEE Journal of Quantum Electronics*, **QE-22**, 1696 (1986).

[13] D. V. Lang, R. People, J. C. Bean and A. M. Sergent, "Measurement of the bandgap of $Ge_xSi_{1-x}$/Si strained layer heterostructures," *Applied Physics Letters*, **47**, 1333 (1985).

[14] H. Temkin, J. C. Bean, T. P. Pearsall, N. A. Olsson, and D. V. Lang, "High photoconductive gain in GeSi/Si strained layer superlattice detectors operating at $\lambda$=1.3 μm," *Applied Physics Letters,* **49**, 155 (1986).

[15] H. Temkin, T. P. Pearsall, J. C. Bean, R. A. Logan, and S. Luryi, "GeSi strained layer superlattice waveguide photodetectors operating near 1.3 mm," *Applied Physics Letter,* **48**, 963, (1986).

[16] H. Temkin, A. Antrasyan, N. A. Olsson, T. P. Pearsall, and J. C. Bean, "GeSi rib waveguide avalanche photodetectors for 1.3 mm operation," *Applied Physics Letters*, **49**, 809 (1986).

[17] T. P. Pearsall, H. Temkin, J. C. Bean, and S. Luryi, "Avalanche gain in $Ge_xSi_{1-x}$/Si infrared waveguide detectors," *IEEE Electron Device Letters*, **EDL-7** 330 (1986).

[18] F. Y. Huang, X. Zhu, M. O. Tanner, and K. L. Wang, "Normal-incidence strained-layer superlattice $Ge_{0.5}Si_{0.5}/Si$ photodiodes near 1.3 μm," *Applied Physics Letters*, **67**, 566 (1995).

[19] V. P. Kesan, P. G. May, E. Barrous, and S. S. Iyer, "Integrated waveguide-photodetector using Si/SiGe multiple quantum wells for long wavelength applications," **IEDM-90**, 637 (1990).

[20] V. P. Kesan, P. G. May, G. V. Treyz, E. Bassous, S. S. Iyer, and J. M. Halbout, "Integrated rib waveguide-photodetector using $Si/Si_{1-x}Ge_x$ multiple quantum wells for long waveglengths," *Materials Research Society Symposium Proceedings*, **220**, 483 (1991).

[21] A. Splett, T. Zinke, K. Petermann, E. Kasper, H. Kibbel, H. J. Herzog, and H. Presting, "Integration of waveguides and photodetectors, in SiGe for 1.3 μm operation," *IEEE Photonics Technology Letters*, **6**, 59 (1994).

[22] B. Li, G. Li, E. Liu, Z. Jiang, J. Qin, and X, Wang, "Monolithic integration of a SiGe/Si modulator and multiple quantum well photodetector for 1.55 μm operation," *Applied Physics Letters*, **73**, 3504, (1998).

[23] T. P. Pearsall, E. A. Beam, H. Temkin, J. C. Bean, "Ge-Si/Si infra-red, zone-folded superlattice detectors," *Electronics Letters*, **24**, 685 (1988).

[24] B. Jalali, A. F. J. Levi, F. Ross, and E. A. Fitzgerald, "SiGe waveguide photodetectors grown by rapid thermal chemical vapour deposition," *Electronics Letters*, **28**, 269 (1992).

[25] B. Jalali, L. Naval, and A. F. J. Levi, "Si-based receivers for optical data links," *Journal of Lightwave Technology*, **12**, 930 (1994).

[26] C. Li, Q. Yang, H. Wang, J. Zhu, L. Luo, J. Yu, Q. Wang, Y. Li, J. Zhou, C. Lin, "$Si_{1-x}Ge_x/Si$ resonant-cavity-enhanced photodetectors with a silicon-on-oxide reflector operating near 1.3 μm," *Applied Physics Letters*, **77**, 157 (2000).

[27] H. Lafontaine, N. L. Rowell, S. Janz, and D. X. Xu, "Growth of undulating $Si_{0.5}Ge_{0.5}$ layers for photodetectors at $\lambda$=1.55 μm," *Journal of Applied Physics*, **86**, 1287 (1999).

[28] S. Janz, J. M. Baribeau, D. J. Lockwood, J. P. McCaffrey, S. Moisa, N. L. Rowell, D. X. Xu, H. Lafontaine, M. R. T. Pearson, "$Si/Si_{1-x}Ge_x$ photodetectors using three-dimensional growth modes to enhance photoresponse at $\lambda$=1550 nm," *Journal of Vacuum Science and Technology A*, **18**, 588 (2000).

[29] T. Yoshimoto, S. G. Thomas, K.L. Wang, and B. Jalali, "SOI waveguide GeSi avalanche pin photodetector at 1.3 μm wavelength," *IEICE Trans. Electron.*, **E81-C**, 1667 (1998).

[30] J. Mi, P. Warren, P. Letourneau, M. Judelewicz, M. Gaihanou, M. Dutoit, C. Dubois, and J. C. Dupuy, "High quality $Si_{1-x-y}Ge_xC_y$ epitaxial layers grown on (100) Si by rapid thermal chemical vapor deposition using methylsilane," *Applied Physics Letters*, **67**, 259 (1995).

[31] K. Brunner, O. G. Schmidt, W. Winter, K. Eberl, G. Gluck, U. Konig, "SiGeC: band gaps, band offsets, optical properties and potential applications," *Journal of Vacuum Science & Technology B*, **16**, 1701, (1998).

[32] F. Y. Huang, "Normal-incidence epitaxial SiGeC photodetector near 1.3 μm wavelength grown on Si substrate," *Applied Physics Letters*, **69**, 2330 (1996).

[33] F. Y. Huang, S. G. Thomas, M. Chu, K. L. Wang, "Epitaxial SiGeC/Si photodetector with response in the 1.3 - 1.66 μm wavelength range," **IEDM-96**, 665 (1996).

[34] F. Y. Huang, K. Sakamoto, K. L. Wang, P. Trinh, and B. Jalali, "Epitaxial SiGeC waveguide photodetector grown on Si substrate with response in the 1.3 - 1.55 μm wavelength range," *IEEE Photonics Technology Letters*, **9,** 229 (1997).

[35] X. Shao, S. L. Rommel, B. A. Orner, J. Kolodzey, P. R. Berger, "A p-$Ge_{1-x}C_x$/n-Si heterojunction diode grown by molecular beam epitaxy," *IEEE Electron Device Letters*, **18**, 411 (1997).

[36] X. Shao, S. L. Rommel, B. A. Orner, H. Feng, M. W. Dashiell, R. T. Troeger, J. Kolodzey, and P. B. Berger, "1.3 μm photoresponsivity in Si-based $Ge_{1-x}C_x$ photodiodes," *Applied Physics Letters*, 72, 1860 (1998).

[37] J. E. Bowers, C. A. Burrus, "Ultrawide-band long-wavelength p-i-n photodetectors," *Journal of Lightwave Technology*, **LT-5**, 1339 (1987).

[38] M. Razeghi, F. Omnes, R. Blondeau, Ph. Maurel, M. Defour, O. Acher, E. Vassilakis, G. Mesquida, J. C. C. Fan and J. P. Salerno, "A high quantum efficiency GaInAs-InP photodetector-on-silicon substrate," *Journal of Applied Physics*, **65**, 4066 (1989).

[39] N. A. Papanicolaou, G. W. Anderson, A. A. Iliadia, A. Christou, "Lattice mismatched InGaAs on silicon photodetectors grown by molecular-beam epitaxy," *Journal of Electronic Materials*, **22**, 201 (1993).

[40] T. Sasaki, T. Enoki, M. Tachikawa, M. Sugo, H. Mori, "InAlAs/InGaAs metal-semiconductor-metal photodiodes heteroepitaxially grown on Si substrates," *Applied Physics Letters*, **64**, 751, (1994).

[41] A. Bartels, E. Peiner, G. P. Tang, R. Klockenbrink, H. H. Wehmann and A. Schlachetzki, "Performance of InGaAs metal-semiconductor-metal photodetectors on Si," *IEEE Photonics Technology Letters*, **8**, 670 (1996).

[42] H. H. Wehmann, G. P. Tang, R. Klockenbrink, and A. Schlarchetzki, "Dark-current analysis of InGaAs-MSM-photodetectors on silicon substrates," *IEEE Transactions on Electron Devices*, **43**, 1505 (1996).

[43] E. Peiner, H. H. Wehmann, H. Iber, S. Mo, G. P. Tang, A. Bartels, A. Schlachetzki, A. Koch, K. Dettmer, "High-quality $In_{0.53}Ga_{0.47}As$ on exactly (001)-oriented Si grown by metal-organic vapour-phase epitaxy," *Journal of Crystal Growth*, **172**, 44 (1997).

[44] F. E. Ejeckam, C. L. Chua, Z. H. Zhu, Y. H. Lo, M. Hong, R. Bhat, "High-performance InGaAs photodetectors on Si and GaAs substrates," *Applied Physics Letters*, **67**, 3936 (1995).

[45] A. R. Hawkins, T. E. Reynolds, D. R. England, D. I. Babic, M. J. Mondry, K. Streubel and J. E. Bowers, "Silicon heterointerface photodetector," *Applied Physics Letters*, **68**, 3692 (1996).

[46] B. F. Levine, A. R. Hawkins, S. Hiu, B. J. Tseng, C. A. King, L. A. Gruezke, R. W. Johnson, D. R. Zolnowski, and J. E. Bowers, "20 GHz high performance planar Si/InGaAs p-i-n photodetector," *Applied Physics Letters*, **70**, 2449 (1997).

[47] B. F. Levine, A. R. Hawkins, S. Hiu, B. J. Tseng, J. P. Reilley, C. A. King, L. A. Gruezke, R. W. Johnson, D. R. Zolnowski, J. E. Bowers, "Characterization of waver bonded photodetectors fabricated using various annealing temperatures and ambients," *Applied Physics Letters*, **71**, 1507 (1997).

[48] B. F. Levine, C. J. Pinzone, S. Hui, C. A. King, R. E. Leibenguth, D. R. Zolnowski, D. V. Lang, H. W. Krautter and M. Geva, "Ultralow-dark-current wafer-bonded Si/InGaAs photodetectors," *Applied Physics Letters*, **75**, 2141 (1999).

[49] H. Ishii, Y. Takahashi, and J. Muroda, "Selective Ge deposition on Si using thermal decomposition of $GeH_4$," *Applied Physics Letters*, **47**, 863 (1985).

[50] L. Colace, G. Masini, and G. Assanto, "Ge-on-Si approaches to the detection of near-infrared light," *IEEE Journal of Quantum Electronics*, **35**, 1843 (1999).

[51] L. Colace, G. Masini, F. Galluzzi, G. Assanto, G. Capellini, L. Di Gaspare, and F. Evangelisti, "Ge/Si (001) photodetector for near infrared light," *Solid State Phenomena*, **54**, 55 (1997).

[52] L. Colace, G. Masini, F. Galluzzi, G. Assanto, G. Capellini, L. Di Gaspare, E. Palange, and F. Evangelisti, "Near infrared light detectors based on UHV-CVD epitaxial Ge on Si (100)," *Materials Research Society Symposium Proceedings*, **486**, 193 (1998).

[53] L. Colace, G. Masini, F. Galluzzi, G. Assanto, G. Capellini, L. Di Gaspare, E. Palange and F. Evangelisti, "Metal-semiconductor-metal near-infrared light detector based on epitaxial Ge/Si," *Applied Physics Letters*, **72**, 3175 (1998).

[54] S. B. Samavedam, M. T. Currie, T. L. Langdo, S. M. Ting, and E. A. Fitzgerald, "High quality germanium photodiodes on silicon substrates using an intermediate chemical mechanical polishing step," *Materials Research Society Symposium Proceedings*, **486**, 187 (1998).

[55] S. B. Samavedam, M. T. Currie, T. A. Langdo, and E. A. Fitzgerald, "High-quality germanium photodiodes integrated on silicon substrates using optimized relaxed graded buffers," *Applied Physics Letters*, **73**, 2125 (1998).

[56] H. C. Luan, D. R. Lim, K. K. Lee, K. M. Chen, J. G. Sandland, K. Wada and L. C. Kimerling, "High-quality Ge epilayers on Si with low threading-dislocation densities," *Applied Physics Letters*, **75**, 2909 (1999).

[57] H. C. Luan, D. R. Lim, L. Colace, G. Masini, G. Assanto, K. Wada, and L. C. Kimerling, "Germanium photodetectors for silicon microphotonics by direct epitaxy on silicon," *Materials Research Society Symposium Proceedings*, **607** (2000).

[58] G. Masini, L. Colace, G. Assanto, H. C. Luan, K. Wada and L. C. Kimerling, "High responsivity near infrared Ge photodetectors integrated on Si," *Electronics Letters*, **35**, 1467 (1999).

[59] L. Colace, G. Masini, G. Assanto, H. C. Luan, K. Wada and L. C. Kimerling, "Efficient high-speed near-infrared Ge photodetectors integrated on Si substrates," *Applied Physics Letters*, 76, 1231 (2000).

[60] D. R. Lim, *Device integration for silicon microphotonic platforms*, Ph. D. Thesis, Massachusetts Institute of Technology, 2000.

[61] T. Taur, T. H. Ning, *Fundamentals of modern VLSI devices*, Cambridge: Cambridge University Press, 1998.

[62] C. Y. Chang, and S. M. Sze, *ULSI technology*, New York: McGraw-Hill, 1996.

[63] S. K. Ghandhi, *VLSI fabrication principles: Silicon and Gallium Arsenide*, New York: Wiley, 1994.

[64] L. M. Giovane, H. C. Luan, L. C. Kimerling, "Strained SiGe materials for high quantum efficiency photodiodes at λ=1.3 to 1.55 μm," *Materials Research Society Symposium Proceedings*, **607** (2000).

[65] M. Sugiyama, T. Morikawa, T. Tatsumi, T. Aoyama, and F. Sato, "A 1.3-um operation Si-based planar P-I-N photodiode with Ge absorption layer using strain-relaxing selective epitaxial growth technology," *Extended abstract of the 1998 International Conference on Solid State Devices and Materials*, 384, (1998).

[66] J. R. Chelikowski, and M. L. Cohen, "Nonlocal pseudopotential calculations for the electronic structure of eleven diamond and zinc-blend semiconductors," *Physics Review B*, **14**, 556 (1976).

[67] C. G. Van de Walle, R. M. Martin, "Theoretical calculations of heterojunction discontinuities in the Si/Ge system," *Physical Review B*, 34, 5621 (1989).

[68] C. G. Van de Walle, "Band lineups and deformation potentials in the model-solid theory," *Physical Review B*, 39, 1871 (1989).

[69] C. G. Van de Walle, "Strain effects on the valence-band structure of SiGe," in E. Kasper ed., *Properties of Strained and Relaxed Silicon Germanium*, INSPEC, 1995.

[70] IT. P. Pearsall and M. A. Pollack, "Compound semiconductor photodiodes," in *Semiconductors and semimetals*, R. K. Williardson and A. C. Beer, Eds., vol. 22, *Lightwave communication technology, Part D, Photodetectors*, W. T. Tsang, vol. Ed. New York: Academic, 173 (1985).

[71] J. A. del Alamo, *Integrated microelectronic devices: physics and modeling*, Massachusetts Institute of Technology, unpublished.

[72] S. M. Sze, *Physics of semiconductor devices*, 2nd Edition, New York: Wiley (1981).

[73] R. S. Muller, T. I. Kamins, Device electronics for integrated circuits, 2nd Edition, New York: Wiley (1986).

[74] F. M. Ross, R. Hull, D. Bahnck, J. C. Bean, L. C. Peticolas, and C. A. King, "Changes in electrical device characteristics during the in situ formation of dislocations," *Applied Physics Letters*, **62**, 1426 (1993).

[75] P. Kozodoy, J. P. Ibbetson, H. Marchand, P. T. Fini, S. Keller, J. S. Speck, S. P. DenBaars, and U. K. Mishra, "Electrical characterization of GaN p-n junctions with and without threading dislocations," *Applied Physics Letters*, **73**, 975 (1998).

[76] L. M. Giovane, H. C. Luan, A. M. Agarwal, and L. C. Kimerling, "Correlation between leakage current density and threading-dislocation density in SiGe p-i-n diode grown on relaxed graded buffer layers," *Applied Physics Letters*, (2000).

[77] L. C. Kimerling, J. R. Patel, J. L. Benton, and P. E. Freeland, *Institute of Physics Conference Series*, **59**, 401 (1981).

[78] J. R. Patel, and L. C. Kimerling, *Crystal Research and Technology*, **16**, 187 (1981).

[79] P. N. Grillot, S. A. Ringel, E. A. Fitzgerald, G. P. Watson and Y. H. Xie, *Journal of Applied Physics*,**77**, 3248 (1995).

[80] L. A. Coldren and S. W. Corzine, *Diode lasers and photonic integrated circuits*, New York: Wiley (1995).

[81] G. Keiser, *Optical fiber-communication*, 2nd Edition, New York: McGraw-Hill (1991).

[82] S. R. Forrest, "Sensitivity of avalanche photodetector receivers for high-bit-rate long-wavelength optical communication systems," in *Semiconductors and semimetals*, R. K. Williardson and A. C. Beer, Eds., vol. 22, L*ightwave communication technology, Part D, Photodetectors*, W. T. Tsang, vol. Ed. New York: Academic, 329 (1985).

[83] W. T. Read, "Theory of dislocations in germanium," *Philosophical Magazine*, **45**, 775 (1954).

[84] W. T. Read, "Scattering of electrons by charged dislocations in semiconductors," *Philosophical Magazine*, **46**, 111 (1954).

[85] B. Podor, "Electron mobility in plastically deformed germanium," *Physca Status Solidi*, **16**, K167 (1966).

[86] A. Bartels, E. Peiner and A. Schlachetzki, "The effect of dislocations on the transport properties of III/V-compound semiconductors on Si," *Journal of Applied Physics*, **78**, 6141 (1995).

[87] D. Monroe, Y. H. Xie, E. A. Fitzgerald, P. J. Silverman, and G. P. Watson, "Comparison of mobility-limiting mechanisms in high-mobility $Si_{1-x}Ge_x$ heterostructures," *Journal of Vacuum Science & Technology B*, **11**, 1731 (1993).

[88] K. Ismail, F. K. LeGoues, K. L. Saenger, M. Arafa, J. O. Chu, P. M. Mooney, and B. S. Meyerson, "Identification of a mobility-limiting scattering mechanism in modulation-doped Si/SiGe heterostructures," *Physical Review Letters*, **73**, 3447 (1994).

[89] K. Ismail, "Effect of dislocations in strained Si/SiGe on electron mobility," *Journal of Vacuum Science & Technology B*, **14**, 2776 (1996).

[90] K. Ismail, "Correlation between dislocations and electron transport properties in Si/SiGe," *Solid State Phenomena*, **47-48**, 409 (1996).

[91] H. M. Ng, D. Doppalapudi, T. D. Moustakas, N. G. Weimann and L. F. Eastman, "The role of dislocation scattering in n-type GaN films," *Applied Physics Letters*, **73**, 821 (1998).

[92] N. G. Weimann, L. F. Eastman, D. Doppalapudi, H. M. Ng, and T. D. Moustakas, "Scattering of electrons at threading dislocations in GaN," *Journal of Applied Physics*, **83**, 3656 (1998).

[93] I. Lo, K. Y. Hsieh, S. L. Hwang, L. W. Tu, W. C. Mitchel and A. W. Saxler, "Effect of threading dislocations on electron transport in $In_{0.24}Ga_{0.76}N$/GaN multiple quantum wells," *Applied Physics Letters*, **74**, 2167 (1999).

[94] S. L Yellen, A. H. Shepard, R. J. Dalby, J. A. Baumann, H. B. Serreze, T. S. Guido, R. Soltz, K. J. Bystrom, C. M. Harding and R. G. Waters, "Reliability of GaAs-based semiconductor diode lasers: 0.6-1.1 μm," *IEEE Journal of Quantum Electronics*, **29**, 2058 (1993).

[95] O. Ueda, *Reliability and degradation of III-V optical devices*, Boston: Artech House (1996).

[96] L. C. Kimerling, "Recombination enhanced defect reactions," *Solid-State Electronics*, **21**, 1391 (1978).

[97] F. Capasso, P. M. Petroff, W. B. Bonner, S. Sumski, "Investigation of microplasmas in InP avalanche photodiodes," *IEEE Electron Device Letters*, **EDL-1**, 27 (1980).

[98] H. Sudo, and M. Suzuki, "Surface degradation mechanism of InP/InGaAs APD's," *Journal of Lightwave Technology*, **6**, 1496 (1988).

[99] R. H. Saul, F. S. Chen, and P. W. Shumate, "Reliability of InGaAs photodiodes for SL applications," *AT&T Technical Journal*, **64**, 861 (1985).

[100] M. Fukuda, *Optical semiconductor devices*, New York: Wiley (1999).

[101] E. A. Fitzgerald, "Dislocations in strained-layer epitaxy: theory, experiment and applications," *Materials Science Reports*, **7**, 87 (1991).

[102] R. Beanland, D. J. Dunstan, P. J. Goodhew, "Plastic relaxation and relaxed buffer layers for semiconductor epitaxy," *Advances in Physics*, **45**, 87 (1996).

[103] S. C. Jain, A. H. Harker and R. A. Cowley, "Misfit strain and misfit dislocations in lattice mismatched epitaxial layers and other systems," *Philosophical Magazine A*, **75**, 1461 (1997).

[104] S. C. Jain, M. Willander, J. Narayan, R. Van Overstraeten, "III-nitrides: growth, characterization, and properties," *Journal of Applied Physics*, **87**, 965 (2000).

[105] P. Sheldon, K. M. Jones, M. M. Al-Jassim, B. G. Yacobi, "Dislocation density reduction through annihilation in lattice-mismatched semiconductors grown by molecular-beam epitaxy," *Journal of Applied Physics*, **63**, 5609 (1988).

[106] M. Tachikawa and M. Yamaguchi, "Film thickness dependence of dislocation density reduction in GaAs-on-Si substrates," *Applied Physics Letters*, **56**, 484 (1990).

[107] E. A. Fitzgerald, Y. H. Xie, M. L. Green, D. Brasen, A. R. Kortan, J. Michel, Y. J. Mii, and B. E. Weir, "Totally relaxed $Ge_xSi_{1-x}$ layers with low threading dislocation densities grown on Si substrates," *Applied Physics Letters*, **59**, 811 (1991)

[108] S. B. Samavedam, and E. A. Fitzgerald, "Novel dislocation structure and surface morphology effects in relaxed Ge/Si-Ge(graded)/Si structures," *Journal of Applied Physics*, **81**, 3108 (1997).

[109] M. T. Currie, S. B. Samavedam, T. A. Langdo, C. W. Leitz, and E. A. Fitzgerald, "Controlling threading dislocation densities in Ge on Si using graded SiGe layers and chemical-mechanical polishing," *Applied Physics Letters*, **72**, 1718 (1998).

[110] The literature on this topic is extensive; see, for example see references in R. Beanland, D. J. Dunstan, P. J. Goodhew, "Plastic relaxation and relaxed buffer layers for semiconductor epitaxy," *Advances in Physics*, **45**, 87 (1996).

[111] H. Chen, L. W. Guo, Q. Cui, Q. Hu, Q. Huang, and J. M. Zhoi, "Low-temperature buffer layer for the for growth of a low-dislocation-density SiGe layer on Si by molecular-beam-epitaxy," *Journal of Applied Physics*, **79**, 1167 (1996).

[112] K. K. Linder, F. Z. Zhang, J. S. Rieh, P. Bhattacharya, and D. Houghton, "Reduction of dislocation density in mismatched SiGe/Si using a low-temperature Si buffer layer," *Applied Physics Letters*, **70**, 3224 (1997).

[113] K. K. Linder, F. C. Zhang, J. S. Rieh, P. Bhattacharya, "Characterization of mismatched SiGe grown on low temperature Si buffer layers by molecular beam epitaxy," *Journal of Crystal Growth*, **175**, 499 (1997).

[114] J. H. Li, C. S. Peng, Y. Wu, D. Y. Dai, J. M. Zhou, and Z. H. Mai, "Relaxed $Si_{0.7}Ge_{0.3}$ layers grown on low-temperature Si buffers with low threading dislocation density," *Applied Physics Letters*, **71**, 3132 (1997).

[115] C. S. Peng, Z. Y. Zhao, H. Chen, J. H. Li, Y. K. Li, L. W. Guo, D. Y. Dai, Q. Huang, J. M. Zhou, T. T. Sheng, C. H. Tung, "Relaxed $Ge_{0.9}Si_{0.1}$ alloy layers with low threading dislocation densities grown on low-temperature Si buffers," *Applied Physics Letters*, **72**, 3160 (1998).

[116] T. Ueno, T. Irisawa, Y. Shiraki, A. Uedono, S. Tanigawa, "Low temperature buffer growth for modulation doped SiGe/Ge/SiGe heterostructures with high hole mobility," *Thin Solid Films*, **369**, 320 (2000).

[117] J. C. C. Fan, B. Y. Tsaur, R. P. Gale, F. M. Davis, "Reducing dislocations in semiconductors utilizing repeated thermal cycling during multistage epitaxial growth," US Patent 4632712 (1986).

[118] H. Okamoto, Y. Watanabe, Y. Kadota, and Y. Ohmachi, "Dislocation reduction in GaAs on Si by thermal cycles and InGaAs/GaAs strained-layer superlattice," *Japanese Journal of Applied Physics*, **26**, L1950 (1987).

[119] M. Yamaguchi, A. Yamamoto, M. Tachikawa, Y. Itoh and M. Sugo, "Defect reduction effects in GaAs on Si substrates by thermal annealing," *Applied Physics Letters*, **53**, 2293 (1988).

[120] E. A. Fitzgerald, "The effect of substrate growth area on misfit and threading dislocation densities in mismatched heterostructures," *Journal of Vacuum Science and Technology B*, **7**, 782 (1989).

[121] E. A. Fitzgerald, Y. H. Xie, D. Brasen, M. L. Green, J. Michel, P. E. Freeland, and B. E. Weir, "Elimination of dislocations in heteroepitaxial MBE and RTCVD $Ge_xSi_{1-x}$ grown on patterned Si substrates," *Journal of Electronic Materials*, **19**, 949, (1990).

[122] G. E. Beltz, M. Chang, M. A. Eardley, W. Pompe, A. E. Romanov, J. S. Speck, "A theoretical model for threading dislocation reduction during selective area growth," *Materials Science and Engineering*, **A234-236**, 794, (1997).

[123] X. G. Zhang, P. Li, G. Zhao, D. W. Parent, F. C. Jain, and J. E. Ayers, "Removal of threading dislocations from patterned heteroepitaxial semiconductors by glide to sidewalls," *Journal of Electronic Materials*, **27**, 1248 (1998).

[124] E. A. Fitzgerald, and Naresh Chand, "Epitaxial necking in GaAs grown on pre-patterned Si substrates," *Journal of Electronic Materials*, **20**, 839 (1991).

[125] T. A. Langdo, C. W. Leitz, M. T. Currie, E. A. Fitzgerald, A. Lochtefeld, D. A. Antoniadis, "High quality Ge on Si by epitaxial necking," *Applied Physics Letters*, **76**, 3700, (2000).

[126] O. Parillaud, E. Gil-Lafon, B. Gerard, P. Etienne and D. Pribat, "High quality InP on Si by conformal growth," *Applied Physics Letters*, **68**, 2654 (1996).

[127] S. Nakamura, M. Senoh, S. Nagahama, N. Iwasa, T. Yamada, T. Matsushita, H. Kiyoku, Y. Sugimoto, T. Kozaki, H. Umemoto, M. Sano, K. Chocho, "InGaN/GaN/AlGaN-based laser diodes with modulation-doped strained-layer superlattices," *Japanese Journal of Applied Physics Part 2-Letters*, **36**, L1568, (1997).

[128] S. Nakamura, M. Senoh, S. Nagahama, N. Iwasa, T. Yamada, T. Matsushita, H. Kiyoku, Y. Sugimoto, T. Kozaki, H. Umemoto, M. Sano, K. Chocho, "InGaN/GaN/AlGaN-based laser diodes with modulation-doped strained-layer superlattices grown on an epitaxially laterally overgrown GaN substrate," *Applied Physics Letters*, **72**, 211 (1998).

[129] T. Gehrke, K. J. Linthicum, E. Preble, P. Rajagopal, C. Ronning, C. Zorman, M. Mehregany, R. F. Davis, "Pendeo-epitaxial growth of gallium nitride on silicon substrate," *Journal of Electronic Materials*, **29**, 306 (2000).

[130] F. E. Ejeckam, M. L. Seaford, Y. H. Lo, H. Q. Hou, and B. E. Hammons, "Dislocation-free InSb grown on GaAs compliant universal substrates," *Applied Physics Letters*, **71**, 776 (1997).

[131] F. E. Ejeckam, Y. H. Lo, S. Subramanian, H. Q. Hou and B. E. Hammons, "Lattice engineered compliant substrate for defect-free heteroepitaxial growth," *Applied Physics Letters*, **70**, 1685 (1997).

[132] Z. Yang, J. Alperin, W. I. Wang, S. S. Iyer, T. S. Kuan, F. Semendy, "In situ relaxed $Si_{1-x}Ge_x$ epitaxial layers with low threading dislocation densities grown on compliant Si-on-insulator substrates," *Journal of Vacuum Science and Technology B*, **16**, 1489 (1998).

[133] F. Y. Huang, M. A. Chu, M. O. Tanner, K. L. Wang, G. D. U'Ren, and M. S. Goorsky, "High-quality strain-relaxed SiGe alloy grown on implanted silicon-on-insulator substrate," *Applied Physics Letters*, **76**, 2680 (2000).

[134] Y. H. Luo, J. L. Liu, G. Jin, K. L. Wang, C. D. Moore, M. S. Goosky, C. Chih, K. N. Tu, "Low-dislocation relaxed SiGe grown on an effective compliant substrate," *Journal of Electronic Materials*, **29**, 950 (2000).

[135] B. Y. Tsaur, M. W. Geis, J. C. C. Fan, and R. P. Gale, "Heteroepitaxy of vacuum-evaporated Ge films on single-crystal Si," *Applied Physics Letters*, **38**, 779 (1981).

[136] T. F. Kuech, M. Maenpaa, S. S. Lau, "Epitaxial growth of Ge on <100> Si by a simple chemical vapor deposition technique," *Applied Physics Letters*, **39**, 245 (1981).

[137] M. Maenpaa, T. F. Kuech, M. A. Nicolet, S. S. Lau, D. K. Sadana, "The heteroepitaxy of Ge on Si: A comparison of chemical vapor and vacuum deposited layers," *Journal of Applied Physics*, **53**, 1076 (1982).

[138] H. Ishii, Y. Takahashi, and J. Murota, "Selective Ge deposition on Si using thermal decomposition of $GeH_4$," *Applied Physics Letter*, **47**, 863 (1985).

[139] Y. Fukuda, and Y. Kohama, "Effect of in situ thermal annealing on crystaline quality of Ge layers grown by molecular beam epitaxy on Si (100)," *Japanese Journal of Applied Physics*, **26**, L597 (1987).

[140] Y. Fukuda, Y. Kohoma, M. Seki, and Y. Ohmachi, "Dislocation reduction in MBE-grown Ge on Si (001) by in situ thermal annealing," *Japanese Journal of Applied Physics*, **27**, L1591 (1988).

[141] D. C. Houghton, J. M. Baribeau, P. Maigne, T. E. Jackman, I. C. Bassignana, C. C. Tan, R. Holt, "Ge and GeSi heteroepitaxy on Si (100) by MBE," *Materials Research Society Symposium*, **77**, 411 (1987).

[142] J. M. Baribeau, T. E. Jackman, D. C. Houghton, P. Maigne, and M. W. Denhoff, "Growth and characterization of Si1-xGex and Ge epilayers on (100) Si," *Journal of Applied Physics*, **63**, 5738 (1988).

[143] M. C. Ozturk, D. T. Grider, J. J. Wortman, M. A. Littlejohn, Y. Zhong, D. Batchelor, and P. Russell, "Rapid thermal chemical vapor deposition of germanium on silicon and

silicon dioxide and new applications of Ge in ULSI technologies," *Journal of Electronic Materials*, **19**, 1129 (1990).

[144] B. Cunningham, J. O. Chu, and S. Akbar, "Heteroepitaxial growth of Ge on (100) Si by ultrahigh vacuum, chemical vapor deposition," *Applied Physics Letters*, **59**, 3574 (1991).

[145] S. Akbar, J. O. Chu, B. Cunningham, "Heteroepitaxial growth of germanium on silicon by UHV/CVD," US Patent 5259918 (1993).

[146] S. Akbar, J. O. Chu, B. Cunningham, G. Fitzgibbon, and S. Ratanabanyarat, "Nonselective germanium deposition by UHV/CVD," US Patent 5286334 (1994).

[147] E. P. Kvam and F. Namavar, "Reduced dislocation density in Ge/Si epilayers," *Applied Physics Letters*, **58**, 2357 (1991).

[148] D. P. Malta, J. B. Posthill, R. J. Markunas, T. P. Humphreys, "Low-defect-density germanium on silicon obtained by a novel growth phenomenon," *Applied Physics Letters*, **60**, 844 (1992).

[149] D. P. Malta, J. B. Posthill, R. J. Markunas, T. P. Humphreys, and N. R. Parikh, "Low-defect-density Ge on Si for large-lattice-mismatched semiconductor integration and strain-engineered devices," *Materials Research Society Symposia Proceedings*, **263**, 491 (1992).

[150] J. S. Harris, S. M. Kock, and S. J. Rosner, "The nucleation and growth of GaAs on Si," *Materials Research Society Symposia Proceedings*, **91**, 3 (1987).

[151] H. Kroemer, T. Y. Liu and P. M. Petroff, "GaAs on Si and related systems: problems and prospects," *Journal of Crystal Growth*, **95**, 96 (1989).

[152] J. C. C. Fan and J. M. Poate Ed., *Heteroepitaxy on Si*, Materials Research Society Symposia Proceedings, **67** (1986).

[153] J. C. C. Fan, J. M. Phillips, B. Y. Tsaur, *Heteroepitaxy on Silicon II*, Materials Research Society Symposia Proceedings, **61** (1987).

[154] J. C. C. Fan, B. Y. Tsaur, R. P. Gale, F. M. Davis, "Reducint dislocations in semiconductors utilizing repeated thermal cycling during multistage epitaxial growth," US Patent 4632712 (1986).

[155] M. Akiyama, Y. Kawarada, K. Kaminishi, "Growth of single domain GaAs layer on (100)-oriented Si substrate by MOCVD," *Japanese Journal of Applied Physics Part 2-Letters*, **23**, L843 (1984).

[156] J. W. Lee, H. Shichijo, H. L. Tsai, and R. J. Matyi, "Defect reduction by thermal annealing of GaAs layers grown by molecular beam epitaxy on Si substrates," *Applied Physics Letters*, **50**, 31 (1987).

[157] Y. Itoh, T. Nishioka, A. Yamamoto, and M. Yamaguchi, "GaAs heteroepitaxial growth on Si for solar cells," *Applied Physics Letters*, **52**, 1617 (1988).

[158] M. Yamaguchi, M. Tachikawa, Y. Itoh, M. Sugo, and S. Kondo, "Thermal annealing effects of defect reduction in GaAs on Si substrates," *Journal of Applied Physics*, **68**, 4518 (1990).

[159] M. Yamaguchi, "Dislocation density reduction in heteroepitaxial III-V compound films on Si substrates for optical devices," *Journal of Materials Research*, **6**, 376 (1991).

[160] N. Hayafuji, M. Miyashita, T. Nishimura, K. Kadoiwa, H. Kumabe, T. Murotani, "Effect of employing positions of thermal cyclic annealing and strained layer superlattice on defect reduction in GaAs on Si," *Japanese Journal of Applied Physics*, **29**, 2371 (1990).

[161] A. Ackaert, P. Demeester, L. Buydens, G. Coudenys, and P. Van Daele, "Selective MOVPE growth of GaAs on Si and its applications to LEDs," *Journal of Crystal Growth*, **107**, 822 (1991).

[162] T. Marshner, W. Stoltz, E. O. Gobel, F. Phillipp, M. Muller and J. Lorberth, "Improvements in the heteroepitaxial growth of GaAs on Si by MOVPE," *Materials Science and Engineering*, **B21**, 266 (1993).

[163] N. Y. Jin-Phillipp, F. Phillipp, T. Marschner, W. Stoltz, E. O. Gobel, "Transmission electron microscopy study on defect reduction in GaAs on Si heteroepitaxial layers grown by metalorganic vapor phase epitaxy," *Journal of Crystal Growth*, **158**, 28 (1996).

[164] Y. Takano, M. Hisaka, N. Fujii, K. Suzuki, K. Kuwahara, and S. Fuke, "Reduction of threading dislocations by InGaAs interlayer in GaAs layers grown on Si substrates," *Applied Physics Letters*, **73**, 2917 (1998).

[165] M. Yamaguchi, M. Tachikawa, M. Sugo, S. Kondo, and Y. Itoh, "Analysis for dislocation density reduction in selective area grown GaAs films on Si substrates," *Applied Physics Letters*, **56**, 29 (1990).

[166] N. Chand, and S. N. G. Chu, "Elimination of dark line defects in GaAs-on-Si by post-growth patterning and thermal annealing," *Applied Physics Letters*, **58**, 74 (1991).

[167] N. H. Karam, V. Haven, S. M. Vernon, N. El-Masry, E. H. Lingunis and N. Haegel, "Selective area epitaxy of GaAs on Si using atomic layer epitaxy by LP-MOVPE," *Journal of Crystal Growth*, **107**, 129 (1991).

[168] E. Yamaichi, T. Ueda, Q. Gao, C. Yamagishi, and M. Akiyama, "Method to obtain low-dislocation-density regions by patterning with $SiO_2$ on GaAs/Si followed by annealing," *Japanese Journal of Applied Physics*, **33**, L1442 (1994).

[169] R. Fischer, D. Neuman, H. Zabel, H. Morkoc, C. Choi, N. Otsuka, "Dislocation reductions in epitaxial GaAs on Si (100)," *Applied Physics Letters*, **48**, 1223, (1986).

[170] R. Fischer, H. Morkoc, D. A. Neumann, H. Zabel, C. Choi, N. Otsuka, M. Longerbone, L. P. Erickson," *Journal of Applied Physics*, **60**, 1640 (1986).

[171] K. Ishida, M. Akiyama, and S. Nishi, "Misfit and threading dislocations in GaAs layers grown on Si substrates by MOCVD," *Japanese Journal of Applied Physics*, **26**, L163 (1987).

[172] M. Shimizu, M. Enatsu, M. Furukawa, T. Mizuki and T. Sakurai, "Dislocation-density studies in MOCVD GaAs on Si substrates," *Journal of Crystal Growth*, **93**, 475 (1988).

[173] D. J. Stirland, "The relationship between etch pit density and dislocation density for (001) GaAs," *Journal of Crystal Growth*, **79**, 493 (1986).

[174] D. J. Stirland, "Quantitative defect etching of GaAs on Si: Is it possible?" *Applied Physics Letters*, **53**, 2432 (1988).

[175] R. Hull, J. C. Bean, D. Bahnck, J. L. J. Peticolas, K. T. Short, and F. C. Unterwald, "Interpretation of dislocation propagation velocities in strained $Ge_xSi_{1-x}$/Si (100) heterostructures by the diffusive kink pair model," *Journal of Applied Physics*, **70**, 2052 (1991).

[176] E. Kasper Ed., *Properties of strained and relaxed Silicon Germanium*, INSPEC:London (1995).

[177] M. Tamura, Y. Yodo, T. Saitoh, J. Palmer, "Rearrangement of misfit dislocations in GaAs on Si by post-growth annealing," *Journal of Crystal Growth*, **150**, 654 (1995).

[178] N. A. El-Masry, J. C. Tarn, and N. H. Karam, "Interactions of dislocations in GaAs grown on Si substrates with InGaAs-InGaAsP strained layer superlattices," *Journal of Applied Physics*, 64, 3672 (1988).

[179] J. Knall, L. T. Romano, B. S. Krusor, D. K. Biegelsen, and R. D. Bringans, "Threading dislocations in GaAs grown with free sidewalls on Si mesas," *Journal of Vacuum Science and Technology B*, **12**, 3069 (1994).

[180] M. F. Ashby, "A first report on deformation mechanism maps," *Acta Metallurgica*, 20, 887 (1972).

[181] A. N. Stroh, "The strength of Lomer-Cottrell sessile dislocations," *Philosophical Magazine*, **1**, 489 (1956).

[182] J. P. Hirth and J. Lothe, *Theory of dislocations*, New York:McGraw-Hill (1968).

[183] J. S. Speck, M. A. Brewer, G. Beltz, A. E. Romanov, and W. Pompe, "Scaling laws for the reduction of threading dislocation densities in homogeneous buffer layers," *Journal of Applied Physics*, **80**, 3808 (1996).

[184] A. E. Romanov, W. Pompe, G. Beltz, and J. S. Speck, "Modeling of threading dislocation density reduction in heteroepitaxial layers: I. Geometry and crystallography," *Physica Status Solidi*, (b) **198**, 599 (1996).

[185] A. E. Romanov, W. Pompe, G. Beltz, and J. S. Speck," Modeling of threading dislocation density reduction in heteroepitaxial layers: II. Effective dislocation kinetics," *Physica Status Solidi*, (b) **199**, 33 (1997).

[186] A. E. Romanov, P. Pompe, G. E. Beltz, and J. S. Speck, "An approach to threading dislocation "reaction kinetics"," *Applied Physics Letters*, **69**, 3342 (1996).

[187] M. Yamaguchi, A. Yamamoto, M. Tachikawa, Y. Itoh, and M. Sugo, "Defect reduction effects in GaAs on Si substrates by thermal annealing," *Applied Physics Letters*, **53**, 2293 (1988).

[188] D. G. Deppe, N. Holonyak, K. C. Hsieh, D. W. Nam, and W. E. Plano, "Dislocation reduction by impurity diffusion in epitaxial GaAs grown on Si," *Applied Physics Letters*, **52**, 1812 (1988).

[189] M. Tamura, T. Yodo, T. Saitoh, J. Palmer, "Rearrangement of misfit dislocations in GaAs on Si by post-growth annealing," *Journal of Crystal Growth*, **150**, 654 (1995).

[190] Y. Takagi, H. Yonezu, Y. Hachiya, and K. Pak, "Reduction mechanism of threading-dislocation density in GaAs epilayer grown on Si substrate by high-temperature annealing," *Japanese Journal of Applied Physics*, **33**, 3368 (1994).

[191] R. S. Crandall, "Modeling of thin film solar cells: uniform field approximation," *Journal of Applied Physics*, **54**, 7176 (1983).

[192] V. Chu, J. P. Conde, D. S. Shen, and S. Wagner, "Photocurrent collection in a Schottky barrier on an amorphous silicon-germanium alloy structure with 1.23 eV optical gap," *Applied Physics Letters*, **55**, 262 (1989).

[193] L. Colace, G. Masini, F. Galluzi, G. Assanto, G. Capellini, L. Di Gaspare, E. Palange, and F. Evangelisti, "Metal-semiconductor-metal near-infrared light detector based on epitaxial Ge/Si," *Applied Physics Letters*, **72**, 3175 (1998).

[194] W. G. Oldham, and A. G. Milnes, "Interface states in abrupt semiconductor heterojunctions," *Solid State Electronics*, **7**, 153 (1964).

[195] P. A. Basore, D. A. Clugston, "PC1D version 4 for windows: from analysis to design," 25th IEEE Photovoltaic Specialists Conference, Washington DC, May (1996).

[196] G. K. Wetheim, and G. L. Pearson, "Recombination in plastically deformed germanium," *Physical Review*, **107**, 694 (1957).

[197] T. Kaneda, H. Fukuda, T. Mikawa, Y. Banda, and Y. Toyama, "Shallow-junction $p^+$-n germanium avalanche photodiodes (APD's)," *Applied Physics Letters*, **34**, 866 (1979).

[198] S. Kagawa, T. Kaneda, T. Mikawa, Y. Banba, and Y. Toyama, "Fully ion-implanted $p^+$-n germanium avalanche photodiodes," *Applied Physics Letters*, **38**, 429 (1981).

[199] T. Kaneda, S. Kagawa, T. Mikawa, Y. Toyama and H. Ando," An $n^+$-n-p germanium avalanche photodiode," *Applied Physics Letters*, **36**, 572 (1980).

[200] O. Mikami, H. Ando, H. Kanbe, T. Mikawa, T. Kaneda, Y. Toyama, "Improved germanium avalanche photodiodes," *IEEE Journal of Quantum Electronics*, **QE-16**, 1002 (1980).

[201] T. Mikawa, S. Kagawa, T. Kaneda, T. Sakurai, H. Ando, and O. Mikami, "A low-noise $n^+np$ germanium avalanche photodiode," *IEEE Journal of Quantum Electronics*, **QE-17**, 210 (1981).

[202] S. Kagawa, T. Mikawa, T. Kaneda, "Germanium avalanche photodiodes in the 1.3 μm wavelength region," *Fujitsu Science and Technology Journal*, **18**, 397 (1982).

[203] T. Kaneda, "Silicon and germanium avalanche photodiodes," in *Semiconductors and semimetals*, R. K. Williardson and A. C. Beer, Eds., vol. 22, *Lightwave communication technology, Part D, Photodetectors*, W. T. Tsang, vol. Ed. New York: Academic, 173 (1985).

[204] K. Koyama, M. Hiroi, T. Tatsumi, and H. Hirayama, "Etching characteristics of $Si_{1-x}Ge_x$ alloy in ammoniac wet cleaning," *Applied Physics Letters*, **57**, 2202 (1990).

[205] C. J. Kircher, "Comparison of leakage currents in ion-implanted and diffused p-n junctions," *Journal of Applied Physics*, **46**, 2167 (1975).

[206] R. S. Muller, T. I. Kamins, *Device electronics for integrated circuits*, New York:Wiley (1986).

[207] K. Shuzo, F. Hirokazu, "Semiconductor device," Japan Patent 53163159.

[208] K. Chikao, K. Masayuki, O. Tadatoshi, M. Yasuaki, "Light receiving semiconductor device," Japan Patent 55072362.

[209] L. G. Meiners, and H. H. Wieder, "Semiconductor surface passivation," *Materials Science Reports*, **3**, 139 (1988).

[210] D. J. Vitkavage, G. G. Fountain, R. A. Rudder, S. V. Hattangady, and R. J. Markunas, "Gating of germanium surfaces using pseudomorphic silicon interlayers," *Applied Physics Letters*, **53**, 692 (1988).

[211] G. Lucovsky, S. S. Kim, D. V. Tsu, G. G. Fountain, and R. J. Markunas, "The effects of subcutaneous oxidation at the interfaces between elemental and compound semiconductors and $SiO_2$ thin films deposited by remote plasma enhanced chemical vapor deposition," *Journal of Vacuum Science and Technology B*, **7**, 861 (1989).

[212] G. G. Fountain, S. V. Hattangady, R. A. Rudder, R. J. Markunas, G. Lucovsky, S. S. Kim, and D. V. Tsu, "Evidence for the occurrence of subcutaneous oxidation during low temperature remote plasma enhanced deposition of silicon oxide films," *Journal of Vacuum Science and Technology A*, **7**, 576 (1989).

[213] D. J. Vitkavage, G. G. Fountain, S. Hattangady, R. A. Rudder, R. J. Markunas, "Semiconductor device having a semiconductor substrate interfaced to a dissimilar material by means of a single crystal pseudomorphic interlayer," US Patent 5168330.

[214] S. V. Hattangady, G. G. Fountain, R. A. Rudder, M. J. Mantini, D. J. Vitkavage and R. J. Markunas, "Interface engineering with pseudomorphic interlayers: Ge metal-insulator-semiconductor structures," Applied Physics Letters, **57**, 581 (1990).

[215] S. V. Hattangady, M. J. Mantini, G. G. Foundtain, R. A. Rudder and R. J. Markunas,"The role of an ultrathin silicon interlayer at the $SiO_2$-Ge interface," *Journal of Applied Physics*, **71**, 3842 (1992).

[216] H. Hasegawa, M. Akazawa, H. Ishii, and K. Matsuzaki, "Control of compound semiconductor-insulator interfaces by an ultrathin molecular-beam epitaxy Si layer," *Journal of Vacuum Science and Technology B*, **7**, 870 (1989).

[217] J. L. Freeouf, J. A. Silberman, S. L. Wright, S. Tiwari, and J. Batey, "Spectroscopic and electrical studies of GaAs metal-oxide-semiconductor structures," *Journal of Vacuum Science and Technology B*, **7**, 854 (1989).

[218] J. L. Freeouf, D. A. Buchana, S. L. Wright, T. N. Jackson, J. Batey, B. Robinson, A. Callegari, A. Paccagnella, and J. M. Woodall, "Studies of GaAs-oxide interface with and without Si interlayer," *Journal of Vacuum Science and Technology B*, **8**, 860 (1990).

[219] J. L. Freeouf, D. A. Buchanan, S. L. Wright, T. N. Jackson, and B. Robinson, "Accumulation capacitance for GaAs-$SiO_2$ interfaces with Si interlayers," *Applied Physics Letters*, **57**, 1919 (1990).

[220] Z. Wang, D. M. Diatezua, D. G. Park, Z. Chen, H. Morkoc, A. Rockett, "Plasma nitridation of thin Si layers for GaAs dielectrics," *Journal of Vacuum Science and Technology B*, **17**, 2034 (199).

[221] K. M. Jackson, "Summary of wet etch rates for RCA, piranha and hot phosphoric processing," personal communication, unpublished.

[222] D. K. Schroder, *Semiconductor material and device characterization*, New York: Wiley (1998).

[223] Y. Wada and K. Wada, "Nearly ideal characteristics of GaAs metal-insulator-semiconductor diodes by atomic layer passivation," *Journal of Vacuum Science and Technology B*, **12**, 3084 (1994).

[224] J. R. Chelikowski, and M. L. Cohen, "Nonlocal pseudopotential calculations for the electronic structure of eleven diamond and zinc-blend semiconductors," *Physical Review B*, **14**, 556, (1976).

[225] L. DiGaspare, G. Capellini, C. Chudoba, M. Sebastiani, and F.Evangelisti, "Low energy yields spectroscopy determination of bans offsets: application to the epitaxial Ge/Si(100) heterostructure", *Applied Surfave Science*, **104-105**, 595, (1996).

[226] B. L. Sharma and R. K. Purohit, *Semiconductor heterojunctions*, Pergamon:Oxford (1974).

[227] E. A. Stach, U. Dahmen, and W. D. Nix, "Real time observations of dislocation-mediated plasticity in the epitaxial Al(011)/Si(100) thin film system," *Materials Research Society Conference Proceedings*, **578** (2000).

[228] G. P. Watson, D. G. Ast, T. J. Anderson, B. Pathangey, "The barrier to misfit dislocation glide in continuous, strained, epitaxial layers on patterned substrates," *Journal of Applied Physics*, **74**, 3103 (1993).