Electrical Reliability of RF Power GaAs PHEMTs

by

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Submitted to the Department of Electrical Engineering and Computer Science
In Partial Fulfillment of the Requirements for the Degree of Master of Science in
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Abstract

GaAs pseudomorphic high-electron mobility transistors (PHEMTs) have great potential for RF power applications. A major concern with these devices is their gradual degradation that occurs as a result of biasing the device at high voltages for extended periods of time. Although previous research has linked the electrical degradation to impact ionization and hot carrier effects, the details of the underlying physical mechanisms are not known. In this thesis, we seek to provide fundamental physical understanding of the electrical degradation in these devices, and to then suggest design strategies that mitigate these effects. In our study, experimental RF power PHEMTs (non-commercial devices provided by our sponsor, Mitsubishi Electric) were electrically stressed at room temperature. During stressing, the devices were characterized at frequent intervals. Our general results showed several forms of degradation, the most significant changes being in the drain resistance (R_D increases), the source resistance (R_S decreases and then saturates), and the threshold voltage (V_T decreases). We then performed several stressing experiments under different conditions and on devices of different geometries. From our experiments on both the PHEMTs and on specialized test structures, our general findings are that there are three independent mechanisms affecting the three regions of the device: the source, the drain and the gate. The decrease in R_S can be explained by an increase in sheet carrier concentration on the source side. The increase in R_D can be attributed to ohmic contact degradation and possibly a decrease in sheet carrier concentration on the drain side. The decrease in V_T can be explained by charge modulation underneath the gate—most likely, hot holes generated by impact ionization neutralizing trapped electrons in the AlGaAs layer.

Thesis Supervisor: Jesús A. del Alamo
Title: Professor of Electrical Engineering

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1 Introduction

1.1 Introduction to GaAs PHEMTs

GaAs Pseudomorphic High-Electron Mobility Transistors (PHEMTs) have been gaining popularity for use in RF power applications for wireless systems. Because of their high frequency response, GaAs PHEMTs are significant devices for power amplification in cell phones, base stations, and satellite communication systems. However, major reliability issues in these devices need to be addressed before they can realize their full potential in such applications.

The devices studied in this research are called pseudomorphic HEMTs, as the layers forming the active structure of the device are grown with slightly different lattice constants (introducing strain in the channel layer). In PHEMTs, InGaAs (rather than GaAs) is used for the channel material, as the introduction of indium increases the electron mobility [1]. Figure 1-1 shows a sketch of a PHEMT structure. In this schematic, the undoped channel layer lies between two very thin highly-doped layers (shown as dashed lines), which are each separated by an undoped "spacer" layer. The thin "supply" layers provide the carriers that form the 2D-electron gas in the channel, and the "spacer" regions ensure that the 2DEG is separated from any ionized donors in the supply layers.

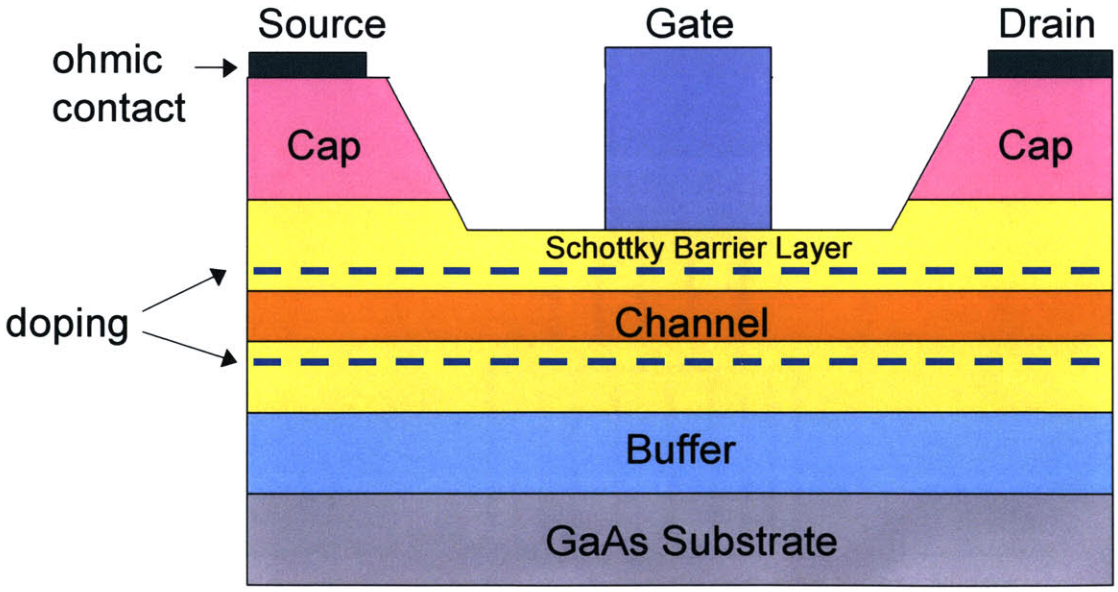

Figure 1-1: Sketch of double-heterojunction pseudomorphic HEMT structure on GaAs substrate.

1.2 Motivation

Electrical degradation is a major concern in RF power GaAs PHEMTs. The high-power device applications (as mentioned in the previous section) require severe and prolonged biasing conditions, which cause the devices to gradually degrade over time. High currents and electric fields cause several degradation and failure mechanisms to occur [2, 3].

This research seeks to explore the long-term degradation of a specific type of PHEMTs as a result of electrical stressing, as seen by [4] and [5]. This type of degradation is most significantly characterized by an increase in drain resistance, though changes in the drain current have also been observed. These forms of degradation may not be catastrophic, but it does affect the use of the device in its intended applications, as can be seen in Figure 1-2. This figure shows the I-V characteristics of a PHEMT before and after an electrical stressing experiment performed at room temperature (which consists of biasing the device at high voltages and high current for a significant period of time). Although in this case the current has increased from its in initial value, it is obvious that the low-field resistance has increased significantly. This represents a serious problem in power applications. Gaining a fundamental physical understanding of the mechanisms behind this degradation is the first goal of the research in this thesis. The next goal is to find solutions to the degradation problem in the form of device design improvements (such as fabrication process modifications, surface treatments, etc).

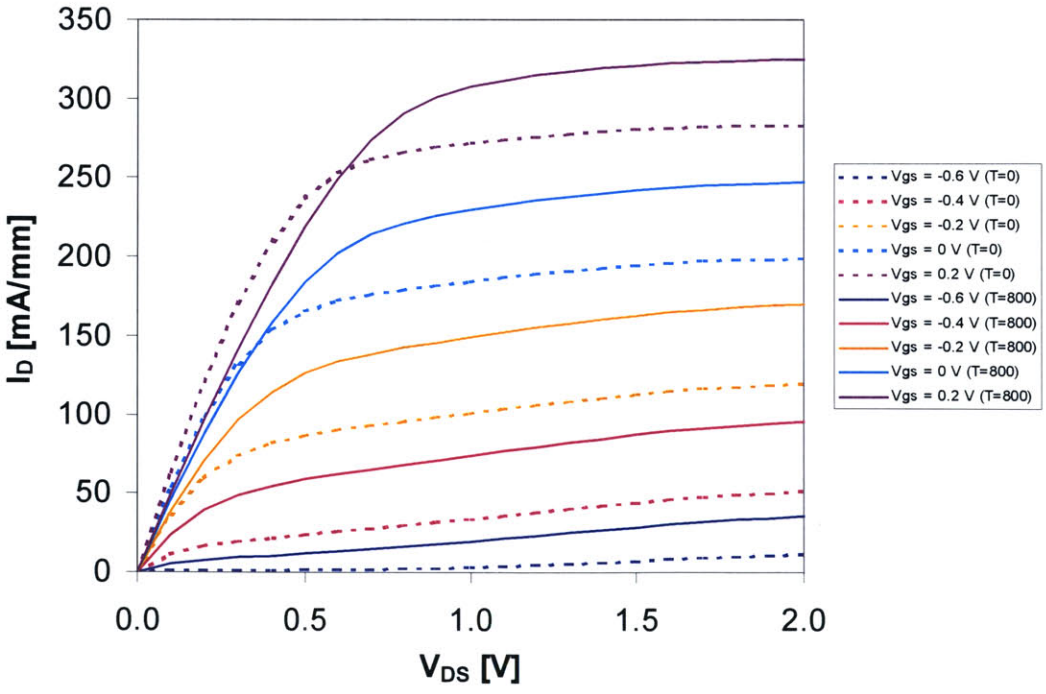

Figure 1-2: I_D vs. V_{DS} curves of a PHEMT, before and after electrical stressing. For 800 minutes, the device was biased at a constant I_D = 450 mA/mm while $V_{DGo}+V_T$ was stepped from 6.0 V to 7.4 V.

1.3 PHEMT Reliability: State-of-the art

Previous studies have found that GaAs PHEMTs undergo hot-electron induced degradation as a result of electrical stressing [4-6]. This manifests itself in various ways, but mostly what has been observed is an increase in the drain parasitic resistance and changes in the drain current. Some devices have exhibited an increase in drain current (due to a decrease in threshold voltage) as a result of hot-electron stressing [7-9], while others have shown the opposite effect [4, 10, 11]. Still others showed an initial increase in drain current followed by a decrease with prolonged stressing [5]. To explore this issue, studies in [3, 5, 6] examined different behaviors of PHEMT stability under various types of accelerated DC stresses. As explained in [3] and [5], the degradation behavior of PHEMTs varies with the relative amount of cumulative stress on the device; mild stressing for shorter periods of time tends to incur an expansion in output power (i.e. an I_D increase), whereas more aggressive and/or extended stressing tends to produce output power degradation.

The increase of the off-state breakdown voltage of PHEMTs with stressing (also referred to as off-state "breakdown walkout") is another observation that has been investigated [11-13]. This improvement in off-state breakdown was observed to be permanent, and in [12] was attributed to a reduction in surface leakage current between the drain and the gate. Additional studies showed that this phenomenon had a strong dependence on surface process conditions [13]. It was also shown in [11] that hot-electron trapping in the passivation layer (leading to electric field relaxation near the drain edge of the gate) was responsible for the off-state breakdown increase. This explanation is consistent with the observed increase in drain resistance seen in these devices.

The reduction of impact-ionization [3] and a permanent increase in the on-state three-terminal gate-drain breakdown voltage have also been reported [14]. Experimental studies exploring this phenomenon also indicated that a build-up of negative charge in the gate-drain region (which thereby induced a wider depletion region and reduced electric field) could be responsible for this. Further studies explored the effect of on-state breakdown walkout on the degradation of device characteristics, in attempt to use the increase in the breakdown voltage to alleviate premature avalanche breakdown and improve device reliability [15].

1.4 Outline of Thesis

This thesis will be organized in the following manner. Chapter 2 will describe the experimental stress and measurement setup used to perform stressing experiments on PHEMTs. The

characterization suite used to monitor the various device figures of merit is described in detail. The biasing scheme utilized to stress these devices is also explained. This chapter concludes with preliminary bias-stressing results, which serves to give us an indication of appropriate stressing conditions for our future experiments.

In Chapter 3, we will show the general results of these bias-stressing experiments, and from this will find indications of at least three separate forms of degradation. We will also go through the various types of additional degradation experiments that were performed in an attempt to isolate all the different mechanisms involved. Such experiments include variations in bias stressing current, tests for degradation recovery, examining differences in device geometry, and observing the effects of the atmosphere on device degradation. This chapter is concluded with a summary of all the findings from the PHEMT degradation experiments.

Chapter 4 contains a description of our stressing experiments performed on Transmission Line Model (TLM) structures. The TLMs have the same material structure as the PHEMTs, but no gate has been fabricated on them. Thus, at low fields a TLM behaves just like an integrated resistor (at high fields, the current saturates due to velocity saturation). Their simplicity in structure allows us to analyze their degradation more easily, so that we can better isolate the degradation mechanisms. Light-emission experiments are also performed, and a summary of the findings of the TLMs is given.

In Chapter 5, the various results from both the PHEMT and TLM degradation experiments are discussed. The degradation observed in the TLMs is correlated with degradation behavior observed in the PHEMTs, and are related to physical causes. The results of our stressing experiments are also correlated with observations reported in the literature.

Finally, in Chapter 6, the conclusions of this work are presented with all the identified degradation mechanisms. This section also contains some suggestions for further work in this research topic.

2 Experimental

2.1 Introduction

This chapter first describes the experimental GaAs PHEMTs that were studied in this research. The details of the experimental setup and the measurement suite for characterizing these devices are then described. The methods for electrically stressing the devices are also explained.

2.2 Device Technology

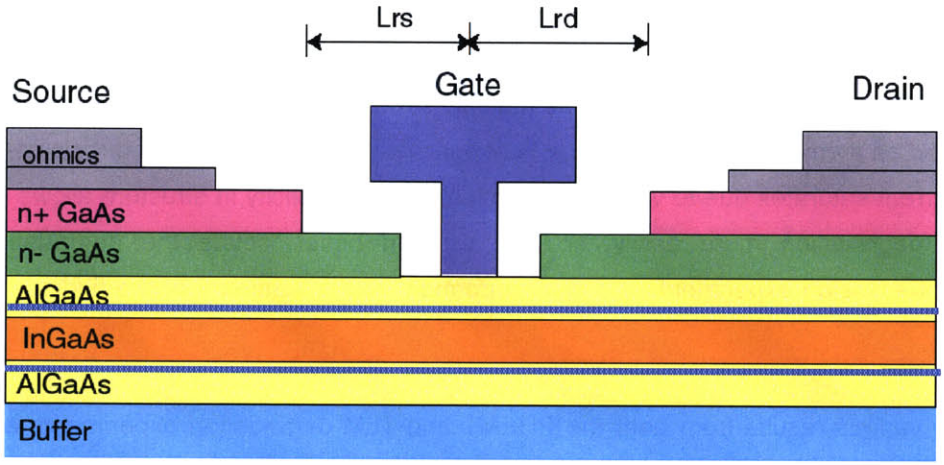

Figure 2-1: Schematic cross-section of GaAs PHEMT under study.

A schematic cross-section of the device under study is shown in Figure 2-1. These PHEMTs are non-commercial devices that were designed and fabricated by Mitsubishi Electric. The active channel is made of InGaAs, which is sandwiched between two thick layers of undoped AlGaAs. Within each intrinsic AlGaAs layer, there is a thin heavily-doped AlGaAs electron supply layer, which provide the carriers in the channel. The device has a double-recessed T-gate structure of length L_g = 0.25 μm. The gate width of these devices is W_g = 100 μm (2 fingers of 50 μm each), though other widths are available.

A typical virgin device has a current-gain cutoff frequency f_T around 40-50 GHz. A typical value for the drain resistance is R_D = 0.72 Ω-mm, while the source resistance is R_S = 0.54 Ω-mm. The threshold voltage V_T is nominally –0.66 V, and the drain current at V_{GS} = 0 V and V_{DS} = 1.2 V is I_{Dss} = 210 mA/mm. The drain current near the knee voltage (V_{GS} = 0.8 V, V_{DS} = 1.0 V), is I_{Dn1} = 470 mA/mm. At V_{DS} = 1.2 V, and at a drain current of I_D = 250 mA/mm, the

transconductance is g_{m2} = 440 mS/mm and the output conductance is g_{o2} = 13 mS/mm. The off-state breakdown voltage is $BV_{DG,off}$ = 15 V.

2.3 Stress and Measurement Setup

To study the degradation of PHEMTs we developed a stress and measurement setup, which enables us to stress the device under a variety of conditions, while monitoring its key figures of merit. We first developed a comprehensive suite of electrical measurements to fully characterize the device *without* introducing any degradation. This characterization suite is an automated program (written in HP VEE), and was designed to be a reproducible and reliable means of evaluating device performance during electrical stress degradation.

We then developed several automated bias-stressing programs (also written in HP VEE) to stress the devices for extended periods of time, while using the characterization suite to characterize the device at frequent intervals. This flow of events is shown schematically in Figure 2-2. After an initial burn-in measurement (optional) is performed, the device undergoes several cycles of characterization and bias stressing. In this manner, we were able to thoroughly evaluate the device performance before and throughout the electrical degradation experiments.

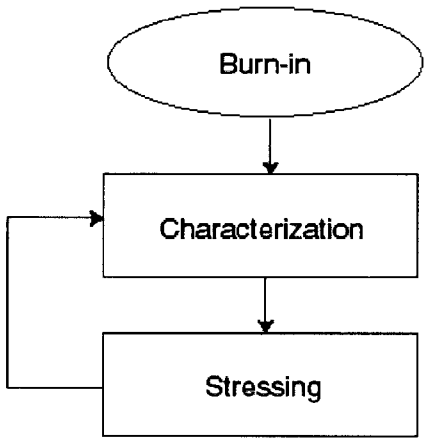

Figure 2-2: Flowchart illustrating the *in-situ* characterization of the device in a stressing experiment.

2.3.1 Experimental Set-up

A schematic picture of our stress and measurement setup can be found in [16]. The device is probed on a Cascade Microtech probe station, using Picoprobe GSG 150 microwave probes. A chamber encloses the chuck and test area containing the probes and sample, which provides shielding from light and also allows gases (such as N_2, forming gas) to be pumped into the chamber. A Windows OS PC running HP VEE controls an HP 4155A Semiconductor Parameter

Analyzer, which is used to stress the device as well as characterize it. A bias-tee is placed on the gate of the device, in order to reduce any oscillations in the DC signal.

Once this entire setup is in place, the external series resistance of the system is measured and its value (typically ~0.5 ohm) is input into the test program (this must be done before running the test program in order to correctly calculate the values of resistance from the measurements). Once the probes come down on the device, the test program is executed and all measurements are taken without lifting the probes. All data obtained from the test program are automatically written into individual text files (one for each set of measurements), while the key device parameters that are extracted are stored in one separate summary file.

2.3.2 The Characterization Suite

The characterization suite consists of several different comprehensive measurements, but is conservative in terms of the maximum current and voltage applied, so as not to damage the device in any way. The test suite obtains the output, transfer, and subthreshold characteristics of the device under test, in addition to extracting several key device parameters (including source and drain resistances, transconductance, output conductance, threshold voltage, and off-state breakdown voltage). After performing several repeated characterization trials on a variety of virgin devices, it was confirmed that only minimal degradation was introduced by the characterization suite. We will now go over the individual measurements performed and the all figures of merit obtained in this test suite.

2.3.2.a Output Characteristics

A set of I-V curves is obtained by sweeping V_{DS} from 0 to 2 V, while stepping V_{GS} from –1.0 V to 0.2 V (in 0.2 V intervals). A typical set of I-V characteristics is shown in Figure 2-3.

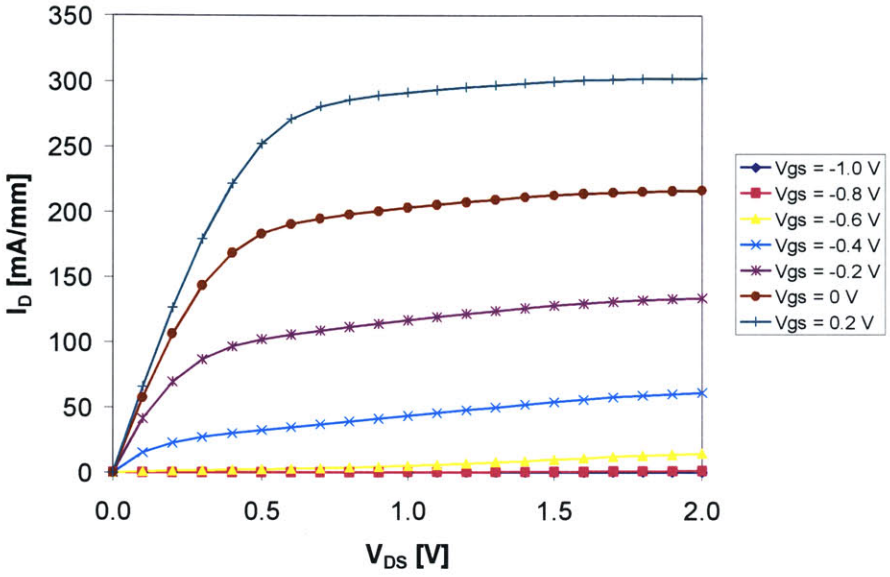

Figure 2-3: Output Characteristics of a standard-parameter, undegraded PHEMT.

2.3.2.b Resistance Measurements

The measurement schemes for the different resistances are taken from [16]. The drain resistance R_D is measured by injecting I_G = 5 mA/mm into the gate and setting up I_D = -I_G so that no current goes through the source. R_D is then calculated as V_{DS}/I_G, minus the external series resistance R_{Dext} (measured previously during the setup calibration). Equation 2.1 illustrates this calculation.

$$R_D = \left.\frac{V_{DS}}{I_G}\right|_{I_G=-I_D=5\,\text{mA/mm}} - R_{Dext} \qquad (2.1)$$

The source resistance R_S is then measured by injecting the same gate current (I_G = 5 mA/mm), but setting I_D = 0 so that all current flows through the source. R_S is then given by:

$$R_S = \left.\frac{V_{DS}}{I_G}\right|_{I_G=-I_S=5\,\text{mA/mm}} \qquad (2.2)$$

The total resistance R_{DS} is measured by injecting I_D = 5 mA/mm into the drain and keeping the gate floating, so all current flows through the source. R_{DS} is then calculated as:

$$R_{DS} = \left.\frac{V_{DS}}{I_D}\right|_{I_D=-I_S=5\text{ mA/mm}} - R_{Dext} \tag{2.3}$$

Note that in all these calculations, the external series resistance is modeled as occurring solely at the drain side of the device (hence it is referred to as R_{Dext}). We neglect R_{Sext} because there are four contacts to the source in our coplanar ground-signal-ground probing configuration. Also, the parasitic resistance on the gate does not impact the extraction of these resistances.

Once these three resistances are obtained, the program then extracts the channel resistance R_{ch} using the following formula:

$$R_{ch} = R_{DS} - R_S - R_D \tag{2.4}$$

2.3.2.c Transfer Characteristics

The transfer characteristics are obtained by sweeping V_{GS} from –0.8 to 0.3 V (using a 10 mV step-size) while keeping V_{DS} constant at 1.2 V. At each value of V_{GS}, the drain current I_D is measured and the transconductance g_m is calculated as follows:

$$g_m(V_{GS}) = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=1.2\text{ V}} \tag{2.5}$$

A sample set of transfer characteristics is shown in Figure 2-4.

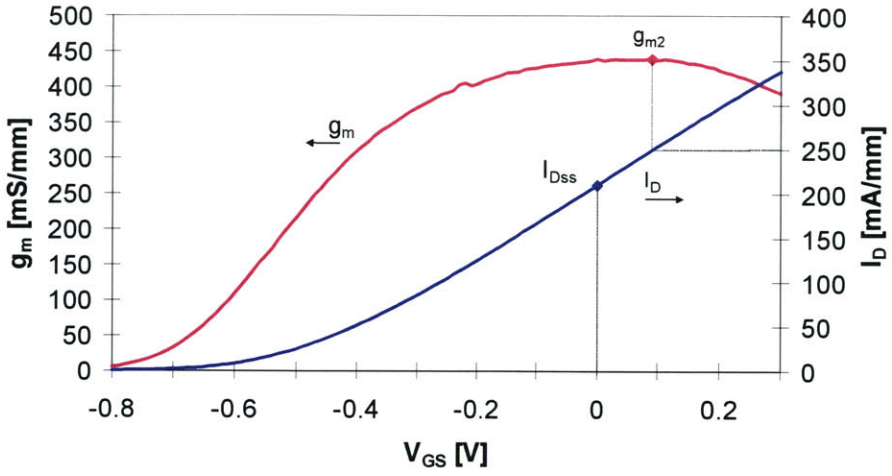

Figure 2-4 Transfer Characteristics of an undegraded PHEMT.

From these data, I_{DSS} (the drain current at V_{GS} = 0) and the transconductances at specified bias points (g_{m1}, at I_D = 108 mA/mm and g_{m2}, at I_D = 250 mA/mm) are also extracted. For the latter calculations, linear interpolation is done between data points in order to obtain a more accurate value.

2.3.2.d Drain Current near knee voltage

We perform a measurement of the drain current at V_{GS} = 0.8 V and V_{DS} = 1.0 V (near the knee voltage). This figure of merit (named I_{Dn1}) gives an indication of the RF figure of merit I_{max}.

2.3.2.e Threshold Voltage

We extract the extract the threshold voltage of the device in the linear regime. The definition of the threshold voltage is as follows:

$$V_T(V_{DS}) = V_{GS}\big|_{I_D=1\ \text{mA/mm}} - \frac{V_{DS}}{2} \qquad (2.6)$$

To measure the threshold voltage, V_{DS} is held constant at 0.1 V, while V_{GS} is swept from –0.8 to –0.4 V (using a 10 mV step-size). The threshold voltage is then taken as the (linearly interpolated) V_{GS} value corresponding to I_D = 1 mA/mm, after subtracting the correction factor of $V_{DS}/2$ (see Figure 2-5 for illustration of extraction.)

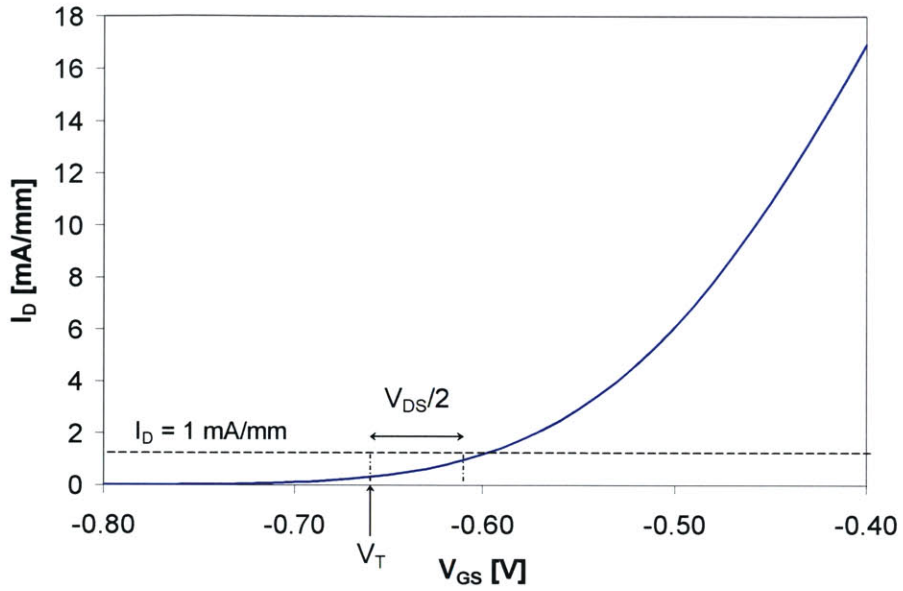

Figure 2-5: Extraction of Threshold Voltage.

2.3.2.f Output Conductance

The output conductance g_o is defined as:

$$g_o(V_{GS}) = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{DS}=1.2\text{ V}} \tag{2.7}$$

The output conductance is measured at V_{DS} = 1.2 V, at two different gate voltages, corresponding to specified bias points (g_{o1} is measured at a V_{GS} corresponding to I_{D1} = 108 mA/mm, and g_{o2} at a V_{GS} corresponding to I_{D2} = 250 mA/mm).

Aside from g_{o1} and g_{o2}, additional measurements of output conductance are later performed as part of a kink measurement (see Section 2.3.2.g below).

2.3.2.g Kink-related Measurement

In order to observe any kinks present in the output characteristics of the device, a measurement is performed that extracts the output conductance over a range of drain voltages. While keeping V_{GS} constant at 0 V, V_{DS} is swept from 0 V to 3.5 V. The output conductance is calculated for each value of V_{DS}, thus creating a g_o vs. V_{DS} curve. From this data, the program searches for a local minimum and a local maximum. If these are found, it calculates the difference and reports that value for the "kink."

2.3.2.h Subthreshold Characteristics

To obtain the subthreshold characteristics, V_{GS} is swept from –1.5 to 0.2 V, while V_{DS} is stepped from 0.2 to 1.2 V, in intervals of 0.2 V. Figure 2-6 shows typical results of this measurement.

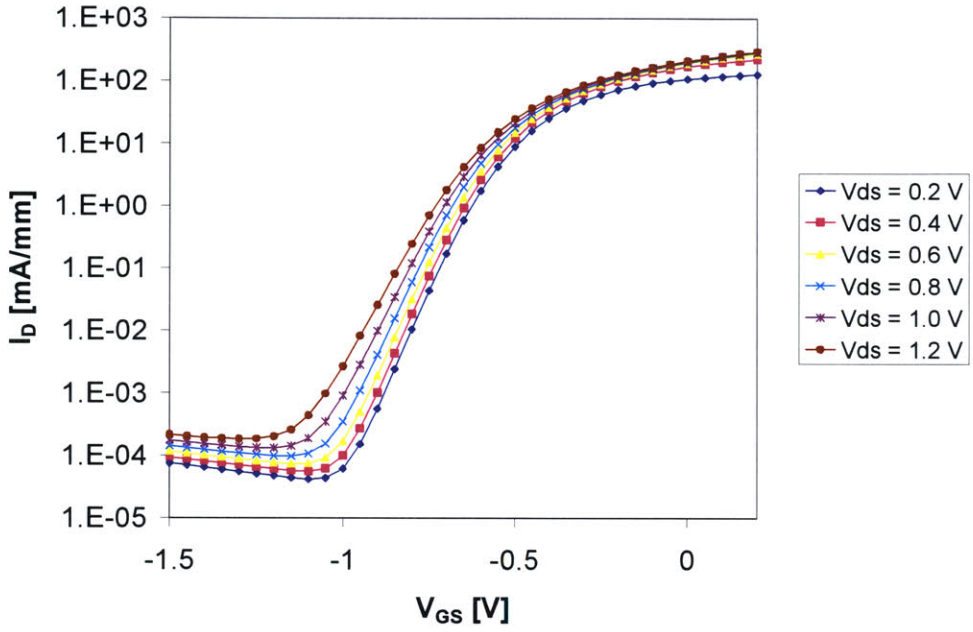

Figure 2-6: Semi-log plot of subthreshold characteristics.

From this data, the test program extracts the inverse subthreshold slope, S, for V_{DS} = 0.2 V and V_{DS} = 1.2 V. S is defined as:

$$S(V_{DS}) = \left(\frac{\partial(\log_{10} I_D)}{\partial V_{GS}} \right)^{-1} \Bigg|_{I_D = 0.1\,\text{mA/mm}} \tag{2.8}$$

Typical values for S at V_{DS} = 0.2 V and V_{DS} = 1.2 V are 90 mV/decade and 105 mV/decade, respectively.

The subthreshold characteristics are also used to quantify the shift in threshold voltage due to different drain voltages. The relative amount of drain-induced barrier lowering (DIBL) is obtained by computing the threshold voltage at two different values of V_{DS}, and then taking the difference and dividing by the corresponding difference in V_{DS}:

$$DIBL = \frac{V_T(1.2\,\text{V}) - V_T(0.2\,\text{V})}{1\,\text{V}} \tag{2.9}$$

In this calculation, the threshold voltage is computed using Equation 2.6, but without subtracting correction term of $V_{DS}/2$, as is common in the logic MOSFET world.

2.3.2.i Off-State Breakdown Voltage

Using the drain-current injection technique [17], the off-state breakdown voltage BV_{DG} is measured. A current of I_D = 0.1 mA/mm is injected into the drain, while V_{GS} is swept from 0 to –3.5 V. BV_{DG} is then the drain-to-gate voltage corresponding to the maximum V_{DS} (see Figure 2-7).

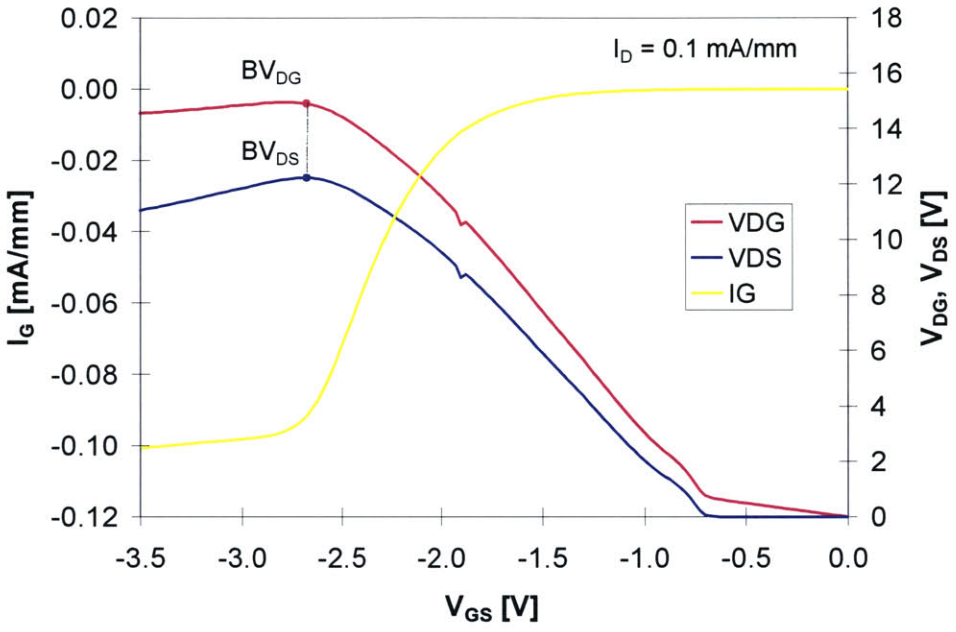

Figure 2-7: Measurement of the off-state breakdown voltage.

2.3.3 Burn-in Measurement

Although we employ low currents and voltages in the characterization suite, there are still small changes in certain parameters upon performing several characterization trials on a new device. It is unknown exactly where this phenomenon comes from, but it is suspected that the extraction of the off-state breakdown voltage (likely the most severe measurement) is partially responsible. To address this "aging effect," we followed Mitsubishi's suggestion to implement a burn-in measurement prior to initial device characterization in a degradation experiment. This burn-in was designed to quickly exhaust the initial transients that occur with repeated measurements on a new device. Without changing the probe configuration, we set up a two-terminal reverse-bias current between the gate and drain for a short period of time (I_{GD} = -10 mA/mm for 20 seconds). This is done by explicitly setting I_G equal to –10 mA/mm and $I_D = -I_G$ = 10 mA/mm (thus keeping the source floating). Figure 2-8 illustrates the results of this burn-in test on a virgin device.

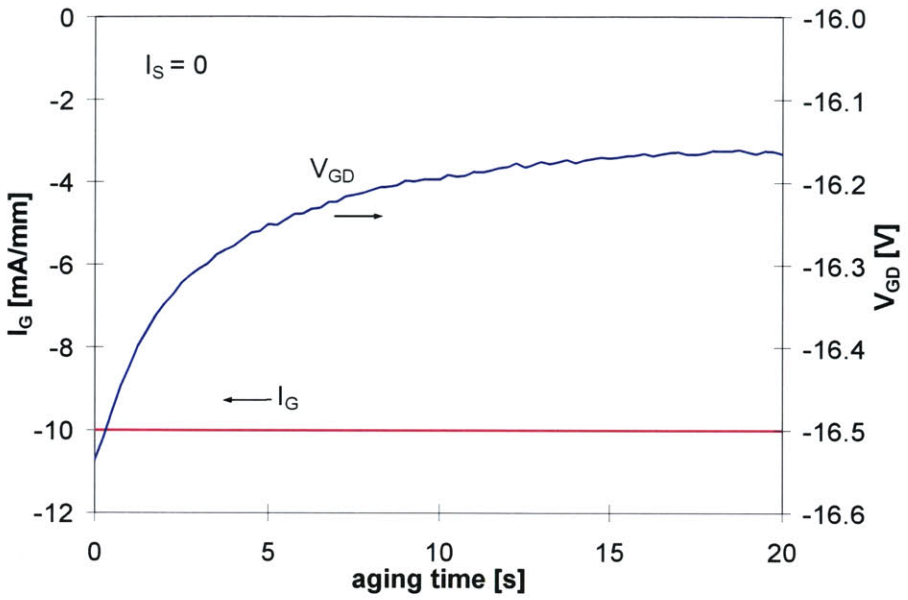

Figure 2-8: Results of burn-in measurement on a virgin PHEMT.

As one can see from this figure, V_{GD} tends to stabilize after a few seconds of injecting reverse gate current. To observe the effect of this new burn-in measurement, 100 consecutive characterization trials were performed on two identical virgin devices, one after performing the burn-in, and one without it. Figure 2-9 and Figure 2-10 illustrate the evolution of some key parameters in both devices. For accurate comparison, the measured data from each device have been normalized to their respective initial values.

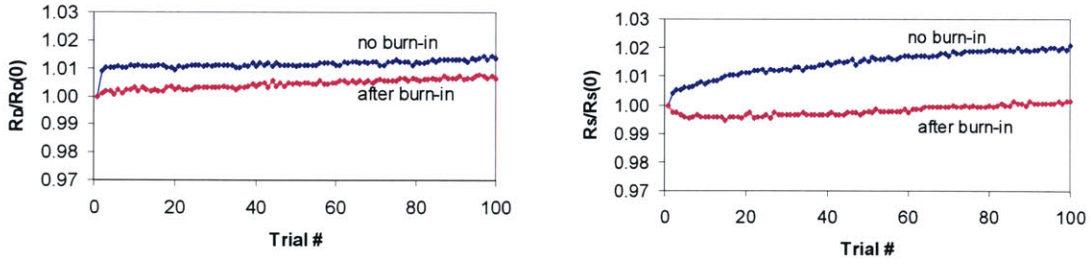

Figure 2-9: Drain Resistance (left) and Source Resistance (right) vs. test trial number, with and without burn-in.

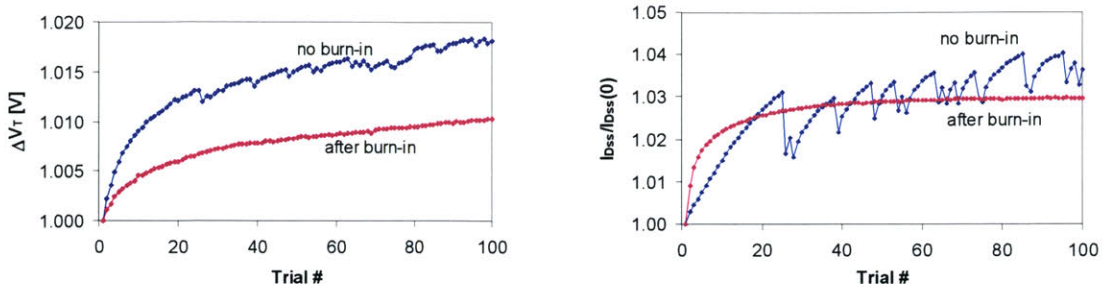

Figure 2-10: Threshold Voltage (left) and Drain Current at V_{GS} = 0 (right) vs. test trial number, with and without burn-in.

From these figures one can see that in either case, the effects of the characterization suite are quite small (usually less than 2% change). Nevertheless, one can clearly see that once the burn-in measurement is performed, the device is less susceptible to further residual changes arising from the characterization suite.

2.4 Electrical Stressing Methodology

Since previous research [3-6, 18] has linked impact ionization with electrical degradation in PHEMTs, we have chosen a stressing scheme that, to the first order, keeps the impact-ionization rate constant. As described in [19], this consists of stressing at a constant drain current I_D and constant $V_{DGo}+ V_T$, where V_{DGo} is the intrinsic drain-to-gate voltage drop (excludes external resistances such as R_D). In order to enhance experimental productivity, $V_{DGo}+V_T$ is initially set at a relatively high voltage and then stepped up in regular time intervals.

Our early experiments were done without an initial burn-in, and implemented a stressing current of I_D = 250 mA/mm, with $V_{DGo}+V_T$ stepped up from 5.0 V in 0.25 V every 100 minutes. Figure 2-11 shows the results from such an experiment. As one can see, at these biasing conditions, little degradation is observed; the drain resistance decreases slightly by 4%, and the source resistance decreases by 14%. We did not observe any increase in drain resistance before the device burned out after 2000 minutes of stressing (when $V_{DGo}+V_T$ was stepped up to 10 V).

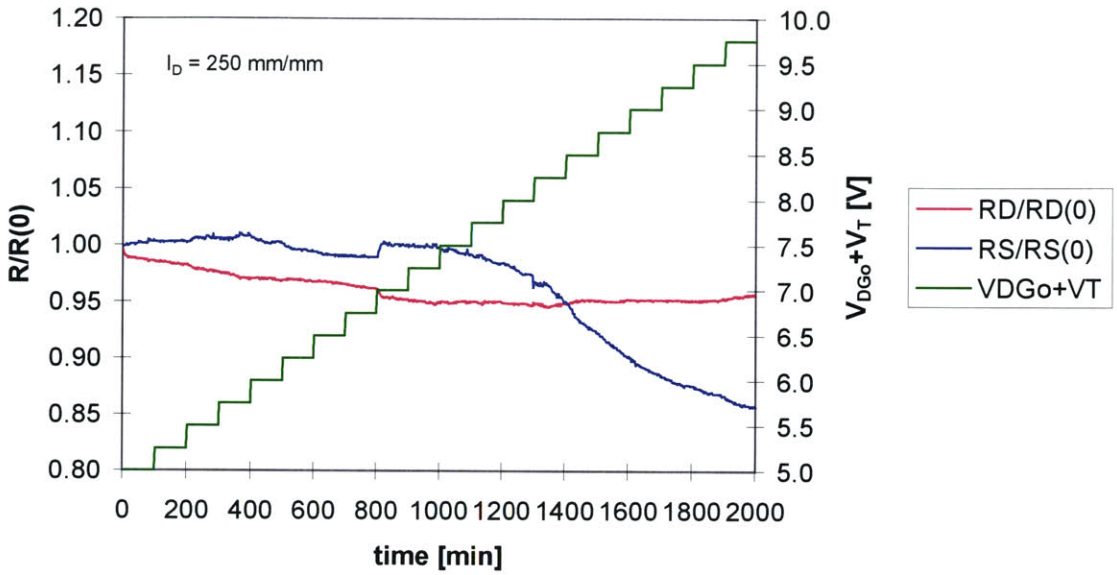

Figure 2-11: Normalized drain and source resistances, as a function of time stressed at I_D = 250 mA/mm.

From this we concluded that we need high currents in addition to high voltages to degrade the device in a reasonable time frame and to observe an increase in R_D. The stressing experiments were then changed to use the conditions of I_D = 400 mA/mm and $V_{DGo}+V_T$ starting at 6.0 V (and increasing in 0.2 V intervals every 100 minutes). We performed one such experiment on a device identical to the one in the previous experiment. Then, we ran an identical degradation test on an identical device, after performing the burn-in measurement as described in the previous section. Figure 2-12 illustrates the main results of each new experiment, namely the normalized values of R_D and R_S as a function of time.

From Figure 2-12, it can be clearly seen that the transient decreases in both R_D and R_S are much shorter after the implementing the burn-in. In any case, from this graph one can clearly see that such severe biasing conditions (I_D = 400 mA/mm, $V_{DGo}+V_T$ > 6 V) are appropriate for observing degradation in these devices in a reasonable length of time.

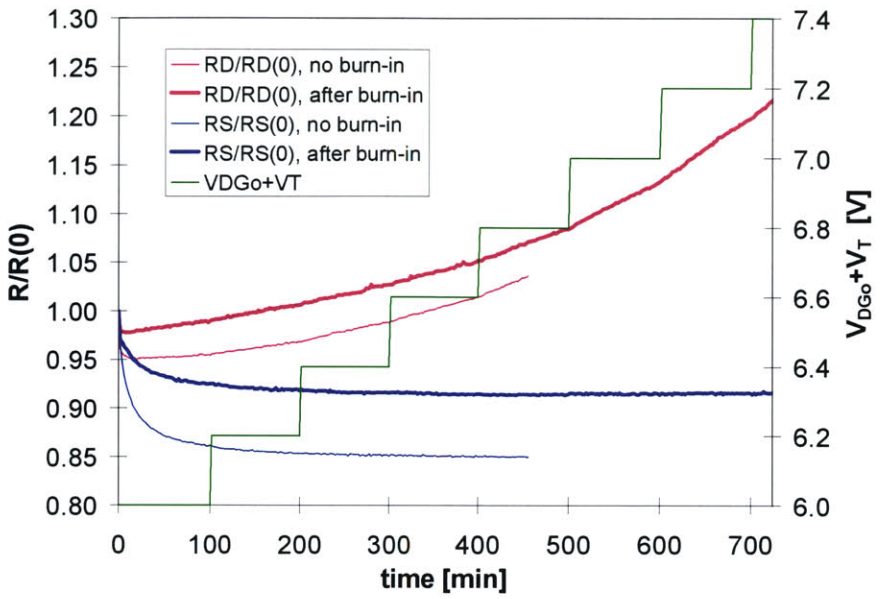

Figure 2-12: Normalized drain and source resistances, as a function of time stressed at I_D=400 mA/mm.

2.5 Conclusions

We have determined that the automated test suite developed to characterize RF power PHEMTs is a benign and reproducible set of measurements, thus making it suitable for evaluating device performance during electrical stressing experiments. Although slight changes do arise upon repeated characterizations of a virgin device, the initial burn-in measurement is effective in exhausting most of these changes in a very short period of time. The burn-in measurement, along with selected biasing conditions are then used as a basis for performing stressing experiments in the PHEMTs, the results of which will be discussed in the next chapter.

3 Degradation of PHEMTs

3.1 Introduction

This chapter describes the degradation of PHEMTs, as observed from our bias stressing experiments. The initial, general results are first presented, followed by results pertaining to several additional degradation experiments. Finally, a summary of the findings from all the different PHEMT stressing experiments is given.

3.2 Initial Experiments: Overall Results

3.2.1 General Observations

Figure 3-1 and Figure 3-2 show the overall results of typical degradation experiment performed on a standard-parameter device (Lrd = 0.5μm, Lrs=0.4μm).

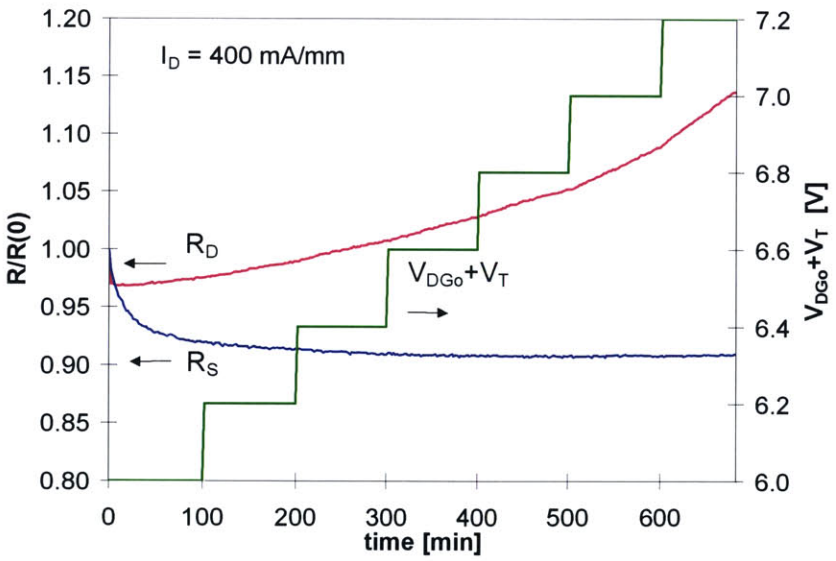

Figure 3-1: Time evolution of normalized R_D and R_S, for voltage step-stress experiment performed on standard-parameter device.

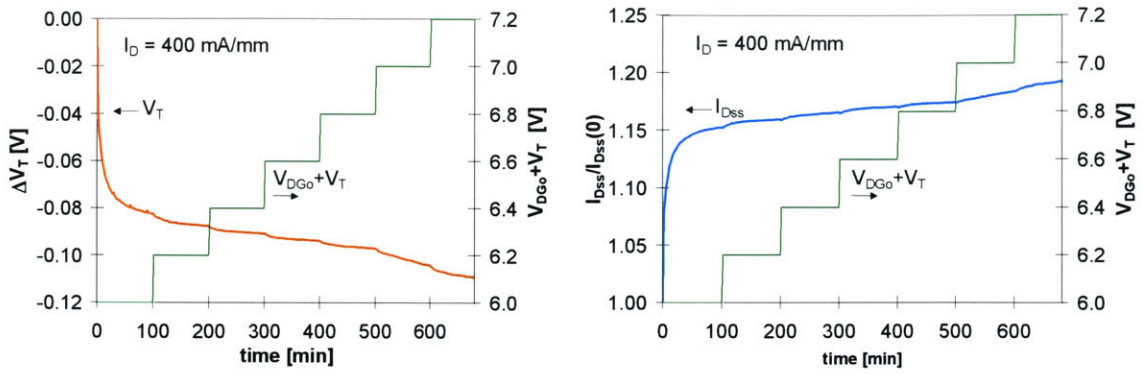

Figure 3-2: Time evolution of the change in V_T (left) and normalized I_{Dss} (right), for voltage step-stress experiment performed on standard-parameter device.

The main observations are that, after initial short transients, R_D increased while R_S decreased and saturated (Figure 3-1). V_T decreased, producing a corresponding increase in I_{Dss} (Figure 3-2). The changes in R_D, R_S and V_T look quite different from each other. These three figures of merit were the main parameters that were observed to degrade as a result of bias stressing. Other parameters (such as g_m, g_o, DIBL, and S) remained relatively unaffected by bias stressing (see Figure 3-3 and Figure 3-4). However, catastrophic breakdown (burnout) occurred after several hours of stressing, when the bias voltages became very high (corresponding to a V_{DS} of about 8 or 9 V). This device in particular broke down after 682 minutes of stressing. In our experiments, the only sign of burnout was a dramatic drop in the off-state breakdown voltage immediately before (seen in Figure 3-5).

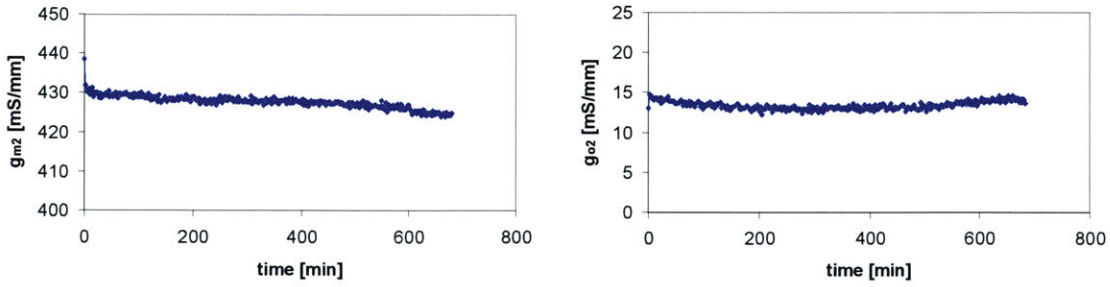

Figure 3-3: Time evolution of g_{m2} (left) and g_{o2} (right), during voltage step-stressing experiment at constant I_D = 400 mA/mm.

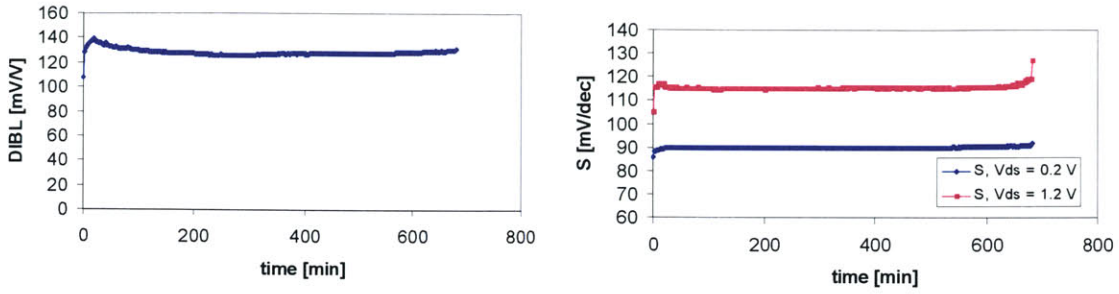

Figure 3-4: Time evolution of DIBL (left) and S (right), during voltage step-stressing experiment at constant I_D = 400 mA/mm.

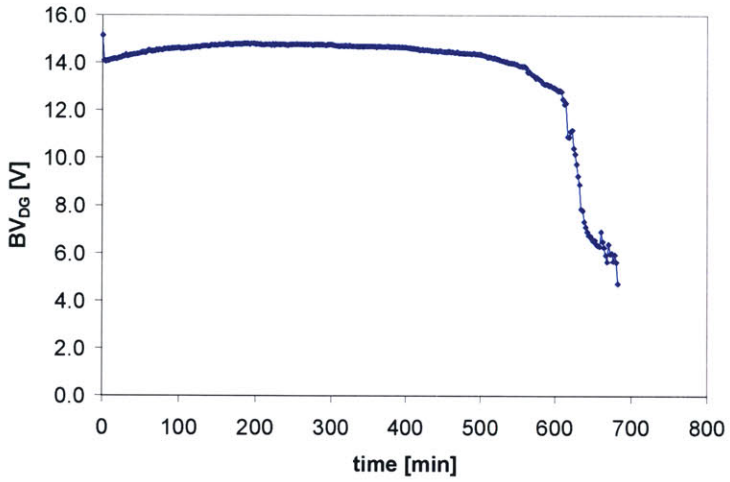

Figure 3-5: Time evolution of $BV_{DG,off}$ during voltage-step stressing experiment at constant I_D = 400 mA/mm.

3.2.2 Observation of Impact Ionization

As mentioned previously, it is suspected that impact ionization and hot-electron effects play a major role in the degradation of PHEMTs [3-6, 18]. To observe these effects, it is necessary to perform measurements at high voltages (V_{DS} > 5 V). However, we could not implement such severe measurements in the characterization suite, since doing so would introduce significant degradation. If such high-voltage measurements were to be implemented, they could only be performed at a few instances during the stressing experiment. Thus, during certain stressing experiments, we occasionally measured the I-V characteristics using a larger range of V_{DS} (up to V_{DS} = 5 V). Figure 3-6 below illustrates the output characteristics measured on a PHEMT, before and after 10 minutes of stressing at constant I_D = 400 mA/mm, constant $V_{DGo}+V_T$ = 6.0 V. As once can see from this graph, at high gate voltages (V_{GS} = 0.6 V, 0.8 V), impact-ionization effects are initially present around high drain voltages (V_{DS} > 4.5 V, 4.0 V, respectively). But after 10 minutes

of stressing, these effects are diminished somewhat (the onset of impact-ionization effects occurs at higher V_{DS}).

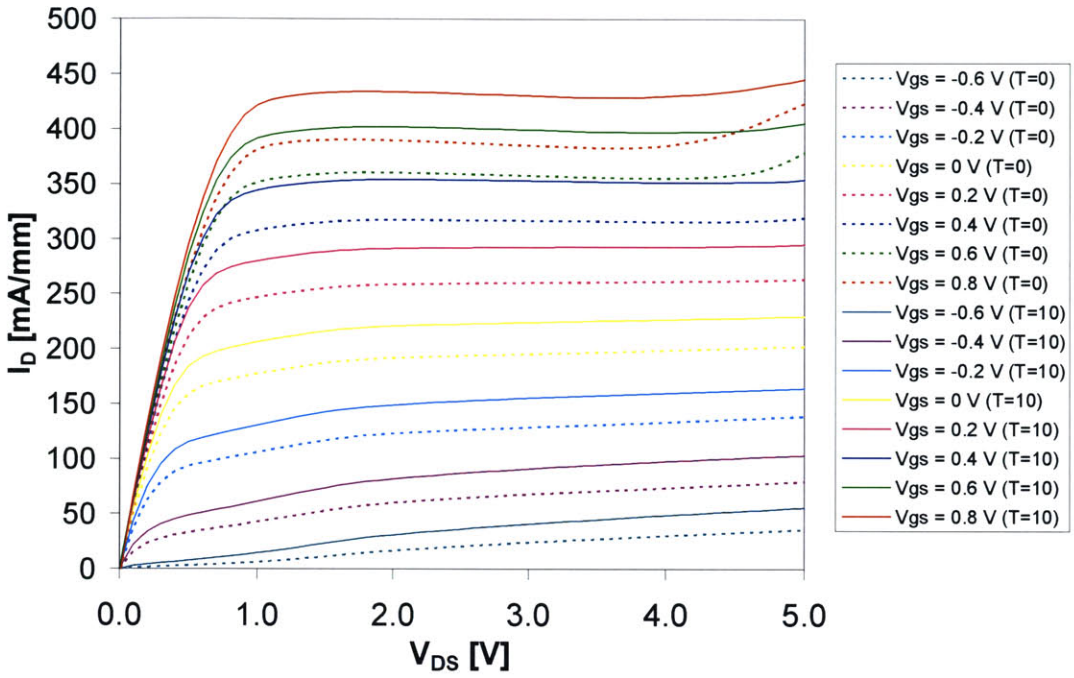

Figure 3-6: Output characteristics of a PHEMT, before (dashed lines) and after (solid lines) 10 minutes of stressing at constant $V_{DGo}+V_T = 6.0$ V.

From this data, we suspected that high-V_{DS} stressing could be causing a decrease in hot-electron effects such as impact ionization. So we decided to monitor the amount of impact ionization in this experiment by observing the behavior of I_G versus V_{GS} in the hot-electron regime (at high values of V_{DS}). Since this type of measurement is somewhat aggressive (and will most likely cause some device degradation), this measurement was only performed at a few points in a stressing experiment. Figure 3-7 below shows the data obtained from the same device, after 10 minutes and 200 minutes of stressing at $I_D = 400$ mA/mm, $V_{DGo}+V_T = 6.0$ V.

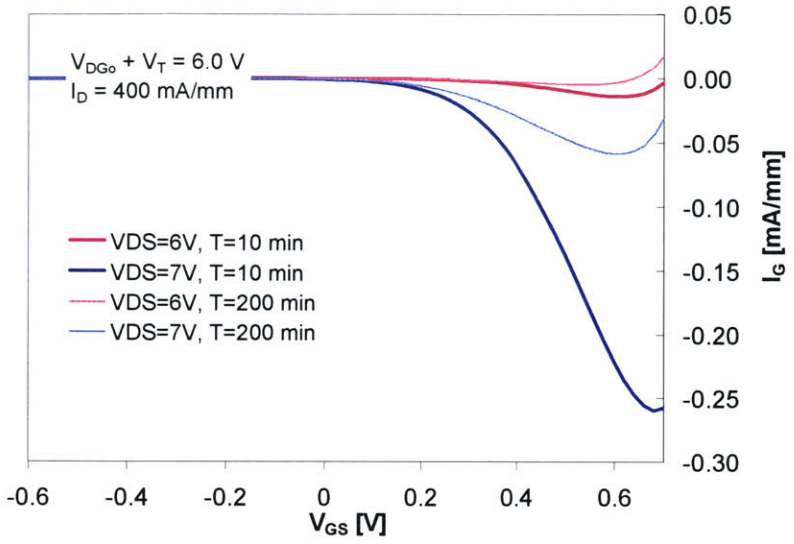

Figure 3-7: I_G vs. V_{GS} curves, after 10 minutes and 200 minutes of stressing at constant $V_{DGo}+V_T$ = 6.0 V.

First of all, the presence of the classic "bell-shaped" curve of I_G vs V_{GS} confirms the presence of impact ionization during our high-V_{DS} stressing [20]. In addition to this, these data also indicate a decrease of impact ionization within the first few hours of stressing. This could possibly be due to a reduction of the maximum electric field between the gate and drain [6], [15].

From our initial results, it appears that the amount of impact ionization tends to decrease with high-voltage stressing, and that the degradation of R_D tends to accelerate at higher bias voltages (higher $V_{DGo}+V_T$). However, the actual dependence of the degradation rate on impact ionization was not clear. It also appeared that there are at least three different degradation mechanisms (manifested in the increase in R_D, decrease in R_S, and decrease in V_T). In order to investigate the role of impact ionization in device degradation, and to isolate all the mechanisms involved, we performed several additional degradation experiments. These are detailed in the next section.

3.3 Further Degradation Experiments

3.3.1 Effects of Higher Stressing Current

It is known that the impact ionization rate has a linear dependence on the drain current [21]. In other words, if we increase I_D by a certain factor (while keeping the same $V_{DGo}+V_T$), then the impact ionization rate will increase by the same factor. Therefore, if the device degradation is mostly due to impact ionization, then the degradation rate should increase in direct proportion to the stressing current. In order to test this, we began performing experiments using a higher stressing current and observing how the degradation responded.

Overall, our experiments showed that the degradation is *not* linearly dependent on the stressing current. First of all, as mentioned previously in Section 2.4, we saw virtually no degradation of R_D at a stressing current of I_D = 250 mA/mm (Figure 2-11). However, we saw very significant degradation at 400 mA/mm (Figure 2-12). Even more interesting, at high enough current levels, if we just increase the drain stressing current by a small amount, the degradation rate of R_D increases quite dramatically. This is illustrated in Figure 3-8, which shows the results of stressing experiments performed on two identical standard-parameter devices. Aside from the fact that the stressing current was 400 mA/mm in once case and 450 mA/mm in the other, the stressing conditions were otherwise identical (V_{DGo} + V_T was stepped up from 6.0 V in 0.2 V intervals every 100 minutes).

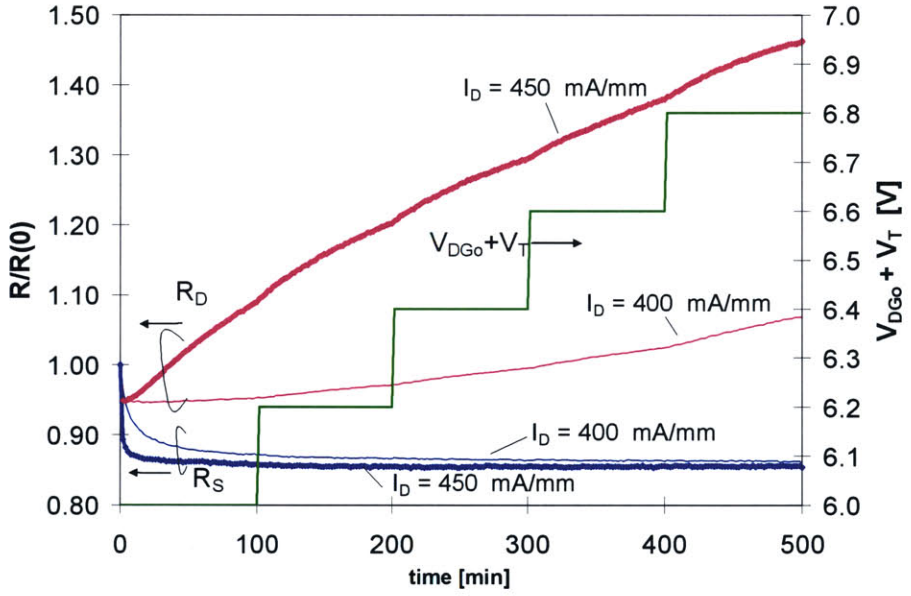

Figure 3-8: Normalized drain and source resistances, as a function of stressing time.

As one can clearly see, the degradation of R_D is much more severe as a result of a mere 11% increase in stressing current. One can also note that the time evolution of R_S (but not the total amount of change) is significantly affected; a higher stressing current prompts a much faster decrease.

To look more closely into the impact of a higher stressing current, the behavior of other key figures of merit are examined as well. Figure 3-9 and Figure 3-10 illustrate the time evolution of some other individual parameters (normalized to their initial values).

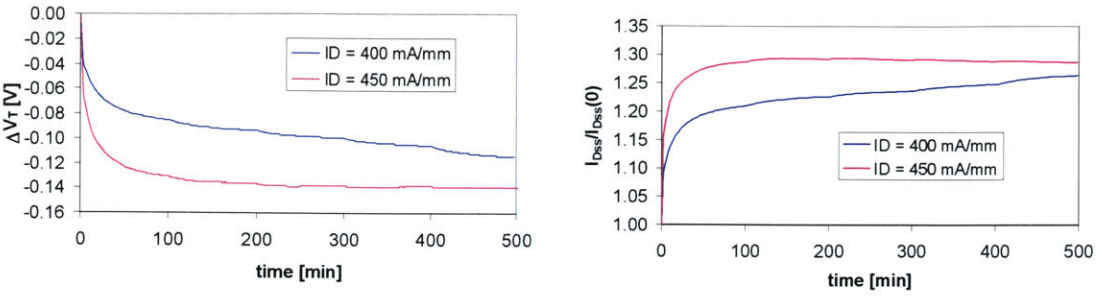

Figure 3-9: Change in V_T (left) and normalized I_{Dss} (right) as a function of stressing time.

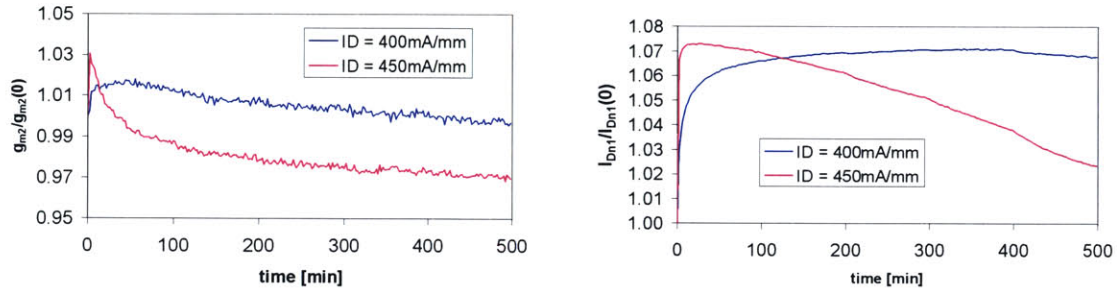

Figure 3-10: Normalized g_{m2} (left) and I_{dn1}, (right) as a function of stressing time.

As one can see, the major consequences of using a higher stressing current are quicker time evolution (and hence the ability to observe advanced stages of degradation much earlier). This is especially apparent in I_{Dss} and I_{Dn1} (refer back to Figure 3-9 and Figure 3-10). After 500 minutes of stressing at I_D = 400 mA/mm, I_{Dss} has increased to 26% of its initial value and is still continuing to (slowly) increase. However, after only about 250 minutes of stressing at I_D = 450 mA/mm, I_{Dss} has already increased to about 30% of initial value and has then begun to decrease. This effect is even more obvious at higher V_{GS}; if we look at the behavior of I_{Dn1}, we see that with the higher stressing current, I_{Dn1} begins to decrease quite sharply, almost immediately after the stressing has begun. In contrast, when stressing at 400 mA/mm, it took about 400 minutes of stressing before we observed a decrease in I_{Dn1}.

The accelerated degradation at higher stressing current may be resulting directly from the higher gate voltages applied to the device. Figure 3-11 and Figure 3-12 below illustrate the values of V_{GS}, V_{DS}, and I_G during stressing for both experiments. As one can see, a 450 mA/mm stressing current involves applying a higher gate voltage, which increases significantly with stressing (as I_{Dn1} degrades, a higher V_{GS} is needed to keep the stressing current constant). The resulting gate current follows similar behavior. In contrast, with a stressing current of 400 mA/mm, the gate voltage and gate current remained relatively constant throughout the experiment.

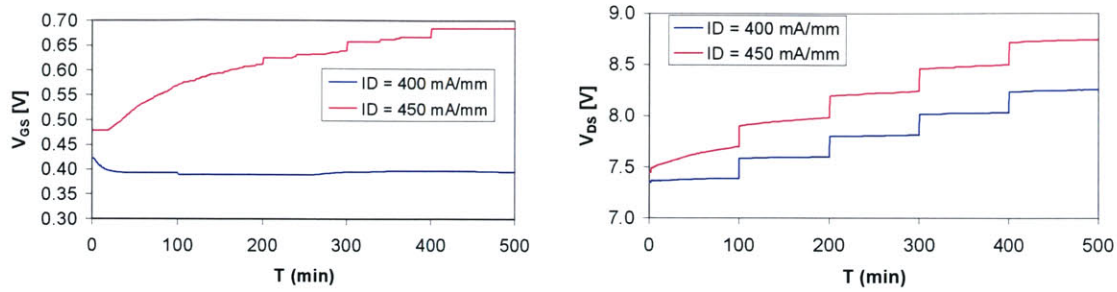

Figure 3-11: Gate bias voltage (left) and drain bias voltage (right), as a function of stressing time.

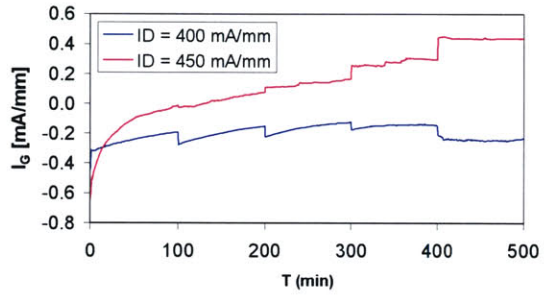

Figure 3-12: Gate current as a function of stressing time.

Since much insight was gained into seeing the results of degradation experiments at different current levels, we decided to try experiments that would step I_D (while keeping $V_{DGo}+V_T$ constant). As expected, our initial experiments showed that there was virtually no degradation happening at drain currents less than 300 mA/mm, so subsequent stressing experiments were begun at 325 mA/mm. One experiment involved keeping $V_{DGo}+V_T$ constant at 6.4 V and stepping up the drain current from 325 mA/mm (in steps of 25 mA/mm every 50 minutes). Figure 3-13 illustrates the results of this experiment.

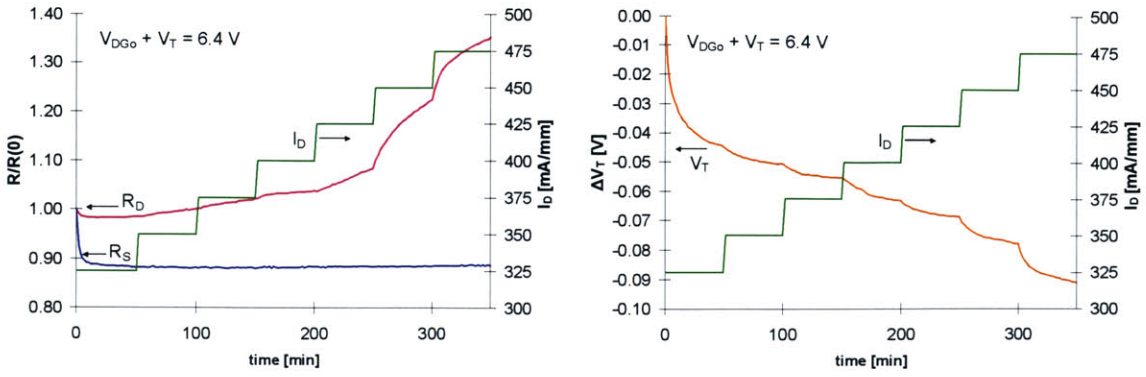

Figure 3-13: Normalized R_D and R_S (left) and change in V_T (right) as a function of stressing time.

From the left graph it becomes even more obvious that the degradation of R_D is not linearly dependent on I_D. Moderate degradation is observed from 350 mA/mm to 400 mA/mm (and the degradation rate is more or less constant throughout each of these intervals). However, at 425 mA/mm, R_D begins to increase more quickly, and then at 450 mA/mm experiences a very dramatic increase (which tends to saturate in time). The experiment ended after 350 minutes of stressing, because a 500 mA/mm drain current could not be obtained (upon increasing V_{GS}, the device burned out).

Concerning the behavior of other figures of merit, one can see that after the initial decrease, the source resistance remains constant, despite a changing I_D. In contrast, the threshold voltage continues to shift as I_D increases.

To summarize our experiments with varying stressing currents, we have found the R_D degradation rate to have a superlinear dependence on I_D, thus suggesting that impact ionization may not be the only mechanism behind R_D degradation. Regarding the source resistance, the initial decrease happens faster as I_D increases, but afterwards it saturates and is unaffected by I_D. The decrease in V_T is also accelerated by higher stressing currents.

3.3.2 Recovery Experiment

In initial experiments, we observed that after periods of stressing followed by several hours of being unstressed, noticeable "recovery" transients in V_T (and I_{Dss}) were observed, but not in R_D or R_S. This thus confirms the change in V_T is independent of the mechanisms behind the degradation of R_D and R_S. We then wanted to test the extent of the recovery of the changes in V_T (if we left a degraded device unbiased for a longer period of time, after a much longer period of stressing, would the shifts in V_T and I_{Dss} still be recovered?). So in the I_D = 400 mA/mm stressing experiment discussed above in Section 3.3.1, the stressing was voluntarily stopped after 500 minutes. The DUT was left unbiased for a period of four days (~ 100 hours), after which then the stressing experiment was resumed. Figure 3-14 illustrates the evolution of R_D, R_S, and V_T throughout this experiment.

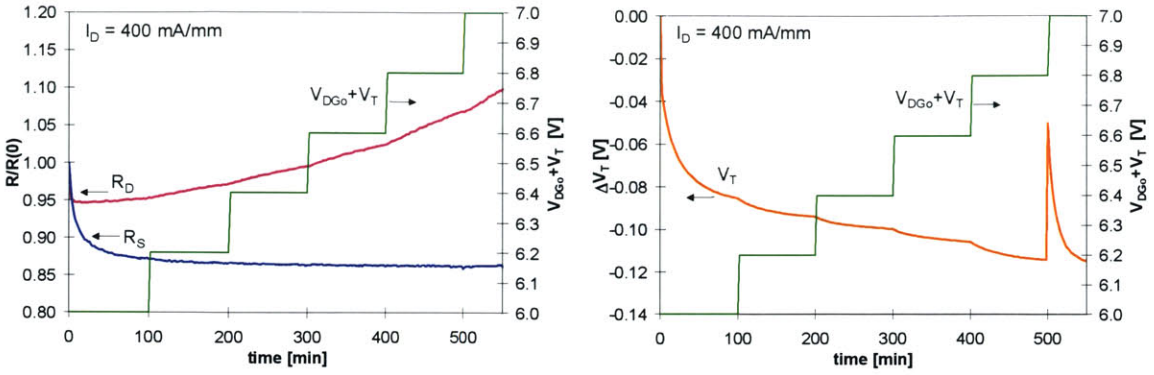

Figure 3-14: Normalized R_D and R_S (left) and change in V_T (right), as a function of stressing time. After 500 minutes, stressing was paused for four days and and then resumed.

First of all, it is obvious from the above figure that there is almost complete recovery of the downward shift in V_T (only the sharp drop in the first 10 minutes of stressing is not recovered). These results are consistent with the findings of Meneghesso et al, which found that the downward shift in threshold voltage observed in PHEMTs subjected to hot-electron stressing can be "fully recovered" after ~100 hours of storage at room temperature with no applied bias [8] .

A pause in stressing also had an effect on other parameters, namely on I_{Dss}, I_{Dn1} and g_{m2} (see Figure 3-15 and Figure 3-16). There were no significant effects on the other figures of merit.

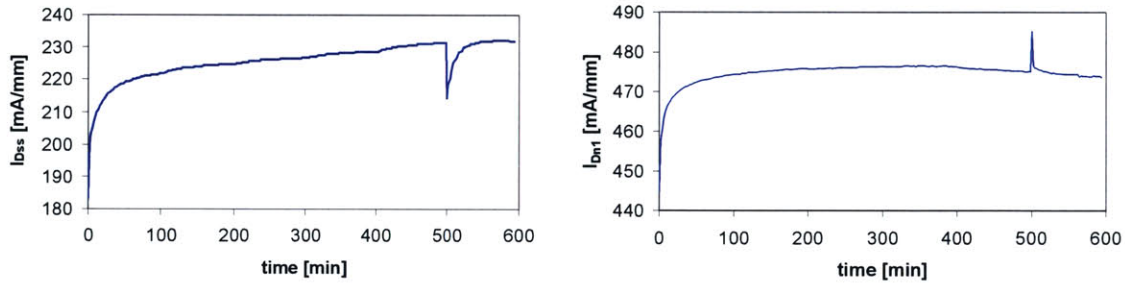

Figure 3-15: I_{Dss} (left) and I_{dn1} (right), as a function of stressing time in recovery experiment.

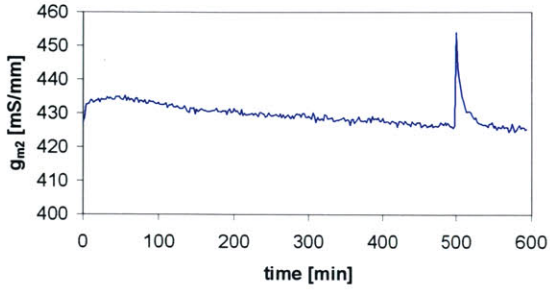

Figure 3-16: g_{m2}, as function of stressing time.

First of all, from Figure 3-15 (left graph), we also observe a significant recovery of I_{Dss}, which makes sense given the relationship between V_T and drain current. However, if we look at the behavior of I_{Dn1} (right graph) we see that interestingly, the drain current actually *increases* upon a pause in stressing, despite the increase in V_T. This appears to have something to do with the change in transconductance (see Figure 3-16) that occurs after the long period of unbiased storage. This thus suggests that the changes in drain current, especially at high voltages are not *entirely* due to shifts in the threshold voltage.

We can also observe this phenomenon by examining the data from the I_D = 450 mA/mm stressing experiment; from looking at the behavior of V_T and I_{Dss} (Figure 3-9) we can see that they pretty much "track" each other throughout the experiment. However, the behavior of I_{Dn1} (Figure 3-10) clearly does not follow V_T; I_{Dn1} obviously degrades much faster than I_{Dss}. Thus, so far we see that for low voltages ($V_{GS} \leq 0$), the change in I_D is mostly dominated by the shift in V_T (attributed in [8] to trapped charge modulation in the active channel under the gate) while at higher V_{GS}, another degradation mechanism becomes much more significant.

3.3.3 Effect of Drain-Gate Gap (Lrd)

Since we wanted to explore the role of impact ionization in device degradation, we decided to compare the degradation behavior of devices with different geometries in the gate-drain region. We know that if the extent of the drain-gate gap (Lrd) becomes smaller, then for a given bias voltage, the peak electric field is larger in the drain-gate region, which therefore increases impact ionization.

Thus we performed a set of step-stressing experiments on PHEMTs of differing drain-gate gaps (different values of Lrd). In this set of experiments, we examined devices in which all device dimensions (Lrs, Lsd, Lgd, etc) were identical, except for Lrd. The specs of the devices tested (along with a few nominal figures of merit) are detailed in Table 1 below:

Table 1: PHEMT device parameters and initial data for Lrd experiments.

Device Design	Chip	Lrs [um]	Lrd [um]	$BV_{DG,off}(0)$ [V]	$R_D(0)$ [Ω-mm]	$R_S(0)$ [Ω-mm]	$V_T(0)$ [V]
No. 10	11	0.4	0.3	11.7	0.66	0.57	-0.64
No. 2*	10	0.4	0.5	15.1	0.72	0.54	-0.66
No. 9	10	0.4	0.7	17.4	0.80	0.57	-0.66
No. 8	10	0.4	0.9	19.8	0.84	0.54	-0.66

* standard-parameter device

First of all, without any degradation, one can see that as Lrd increases, the off-state breakdown voltage increases. This is expected since there for larger Lrd, the peak electric field for a given bias voltage will be smaller. Also, from the table one can see that as Lrd increases, R_D increases. This is also expected since for a larger Lrd, the recess region is longer. $R_S(0)$ and $V_T(0)$ are relatively unaffected by the extent of Lrd, as expected.

Figure 3-17 illustrates a graph of the normalized drain resistance as function of stressing time for all four devices. As one can see, devices with longer Lrd did not experience significantly different R_D degradation rates; the relative R_D degradation experienced by each device was similar (all remained within ~3% of each other). This suggests that impact ionization is not entirely responsible for R_D degradation. It is interesting to note that the change in R_D scales with $R_D(0)$ (i.e., the longer the recess, the bigger $R_D(0)$, and the bigger the change in R_D). This suggests some kind of surface effect.

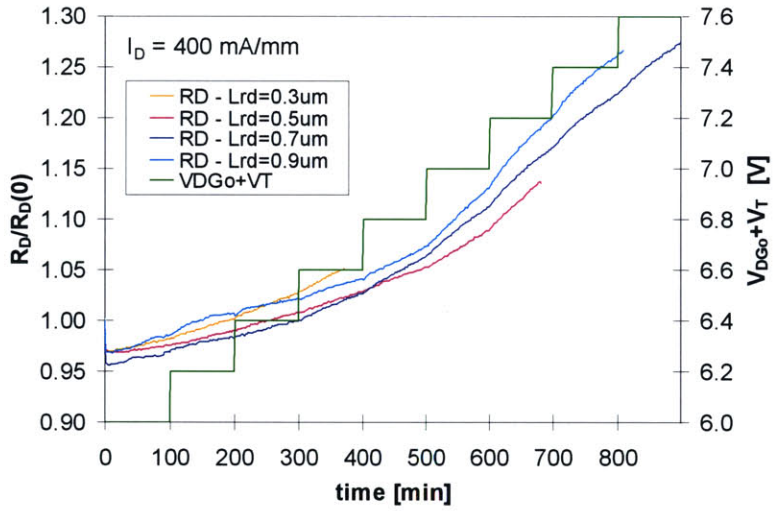

Figure 3-17: Time evolution of R_D (normalized to initial values) for voltage step-stress experiments, performed on four different devices with different values of Lrd.

However, if one looks at the evolution of the threshold voltage shift in these devices (Figure 3-18), one can see that in this case the size of the drain-gate gap does have a significant effect. Here, as Lrd decreases, the V_T shift happens faster. This is consistent with the idea that the shift in V_T is due to hot holes (generated by impact ionization) becoming trapped underneath the gate, as discussed in [6] and [20].

If we now examine degradation occurring on the source side of the device, we find that R_S is somehow correlated with Lrd. Figure 3-19 shows the time evolution of R_S (normalized to the

minimum values) for all four devices in the first 300 minutes of stressing. One can see that as Lrd decreases, the transient change in R_S becomes much slower.

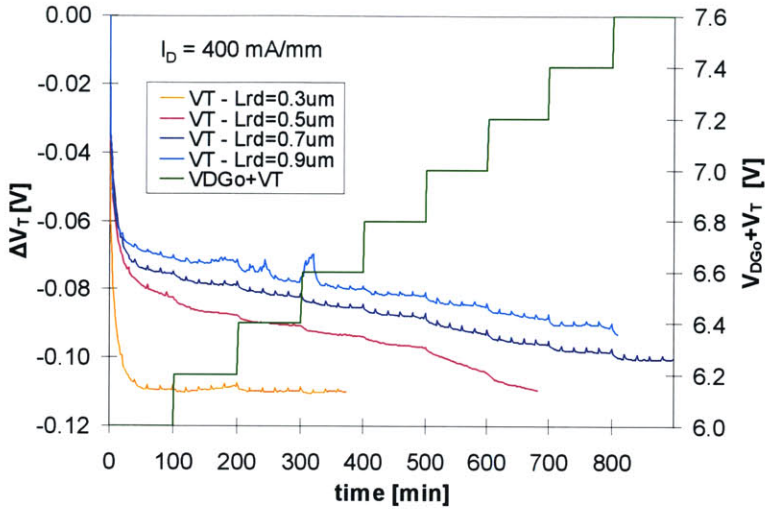

Figure 3-18: Time evolution of change in V_T for voltage step-stress experiments performed on four different devices with different values of different Lrd.

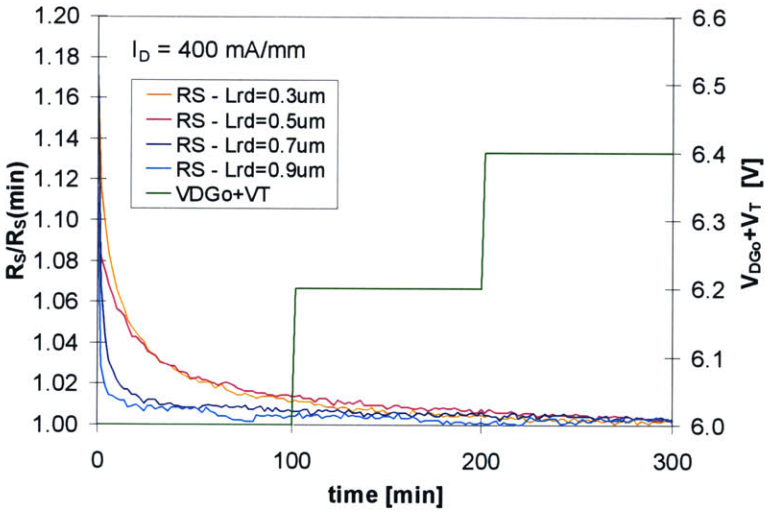

Figure 3-19: Time evolution of normalized R_S for voltage step-stress experiments performed on four different devices with different values of Lrd.

The behavior of the off-state breakdown voltage with stressing (Figure 3-20) is puzzling. Initially the breakdown voltage is proportional to Lrd (see Table 1), but it decreases significantly within the first few minutes of stressing. As one can see from Figure 3-20, this decrease is more dramatic for longer values of Lrd. After this initial decrease, $BV_{DG,off}$ for all devices remains more or less

constant for a long period of time. However, immediately before catastrophic breakdown, devices with shorter Lrd experience a sharp drop in $BV_{DG,off}$, whereas devices with longer Lrd do not.

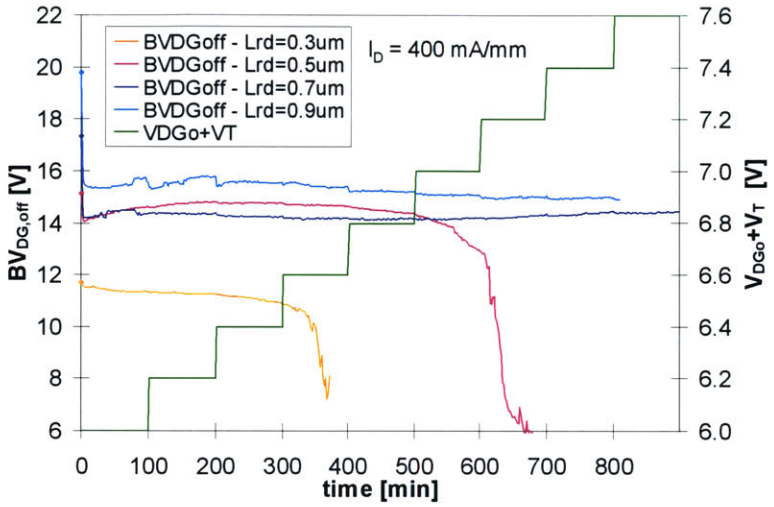

Figure 3-20: Time evolution of $BV_{DG,off}$ for voltage step-stress experiments performed on four different devices with different values of Lrd.

In summary, the experiments with varying Lrd strongly suggest that the changes occurring on the source and under the gate are related to impact-ionization. On the other hand, the picture of degradation on the drain side of the device seems to be more complicated; the behavior of R_D and V_T in these experiments seems to imply that impact ionization plays a much lesser role on the drain side of the device than it does in the gate region. This alludes to the possibility that there is another, separate degradation mechanism localized in the drain region that is affecting R_D.

3.3.4 Effect of Source-Gate Gap (Lrs)

In order to examine the effect of Lrs on device degradation, identical step-stressing experiments were performed on three additional PHEMTs (with identical dimensions except for the source-gate gap Lrs). The specs of these devices tested are detailed in Table 2 below:

Table 2: PHEMT device parameters and initial data for Lrs experiments.

Device Design	Chip	Lrs [um]	Lrd [um]	$BV_{DG,off}(0)$ [V]	$R_D(0)$ [Ω-mm]	$R_S(0)$ [Ω-mm]	$V_T(0)$ [V]
No. 13	10	0.2	0.5	14.1	0.73	0.48	-0.64
No. 2*	10	0.4	0.5	15.1	0.72	0.54	-0.66
No. 12	10	0.6	0.5	15.3	0.72	0.64	-0.66
No. 11	10	0.8	0.5	15.4	0.74	0.73	-0.67

Without degradation, the main effect of changing Lrd is on the source resistance—as Lrs increases, $R_S(0)$ increases. $BV_{DG,off}$, $R_D(0)$, and $V_T(0)$ are relatively unaffected by changing Lrs.

Figure 3-21 illustrates the time evolution of normalized R_D for all four devices. As expected, the degradation behavior of R_D is nearly identical for all devices (Lrd is constant). Figure 3-22 shows the evolution of the change in V_T with stressing. Since Lrs is different, the electric field between the gate and source is different for each device, which thus affects the measurement of V_T. However, by comparing the V_T behavior in Figure 3-22 with that in Figure 3-18, one can see that rate of change in V_T is not greatly affected by Lrs (as it is by Lrd).

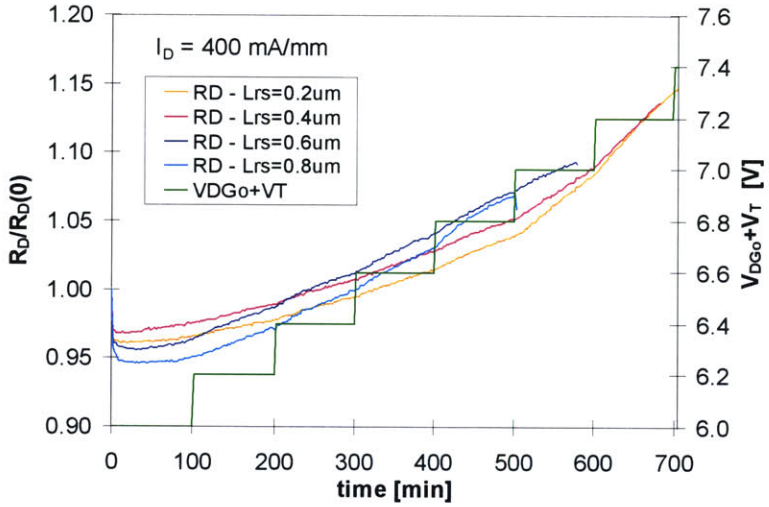

Figure 3-21: Time evolution of normalized R_D for voltage step-stress experiments, performed on four different PHEMTs with different values of Lrs.

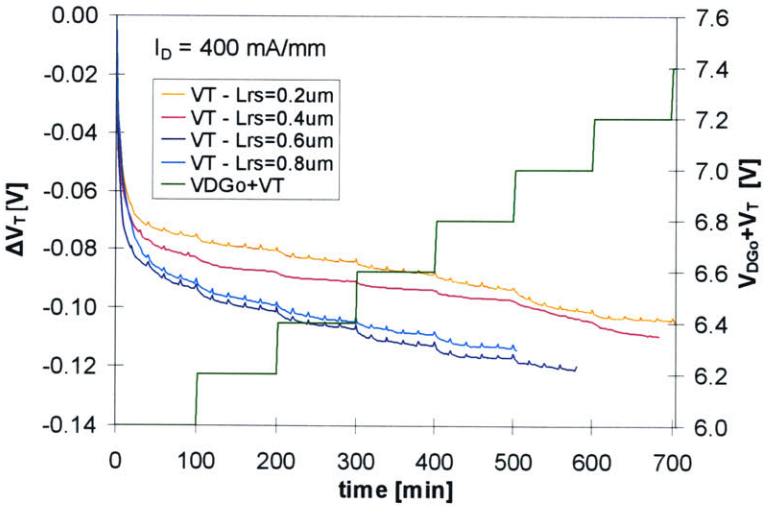

Figure 3-22: Time evolution of ΔV_T for voltage step-stress experiments performed on four different PHEMTS with different values of Lrs.

Figure 3-23 shows the time evolution of R_S (normalized to the minimum values) with stressing. As one can see from this graph, the transient behavior of R_S is unaffected by the length of the source-gate gap. It is interesting to note however, that the change in R_S scales with the nominal value. This suggests a surface-related degradation mechanism.

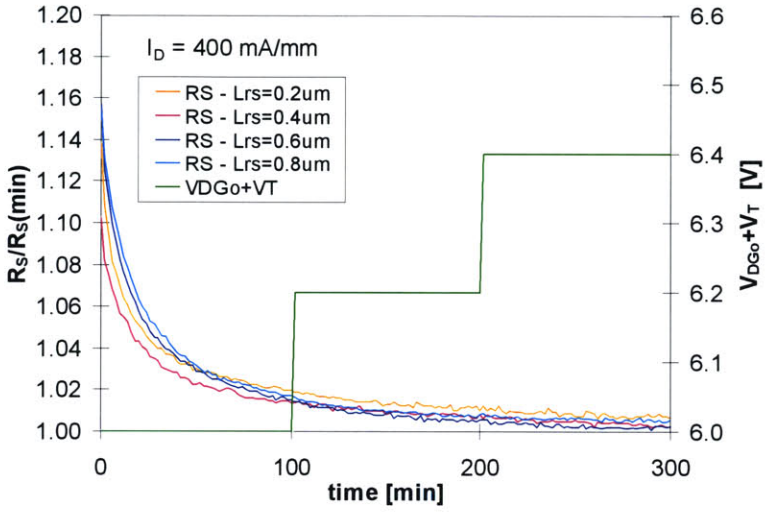

Figure 3-23: Time evolution of normalized R_S for voltage step-stress experiments performed on four different PHEMTs with different values of Lrs.

A more interesting result of this experiment is the impact of Lrs on the breakdown behavior of the device. Figure 3-24 illustrates the time evolution of the breakdown voltage for all four devices. As one can see from this graph and from Table 2, devices with shorter values of Lrs take longer to reach catastrophic breakdown. This suggests the possibility that there might be some surface reaction occurring at the source side of the device that is negatively affecting the breakdown characteristics. This is certainly possible since in [22] it is shown that for PHEMTs, the electrostatic interaction of the source can seriously affect $BV_{DG,off}$.

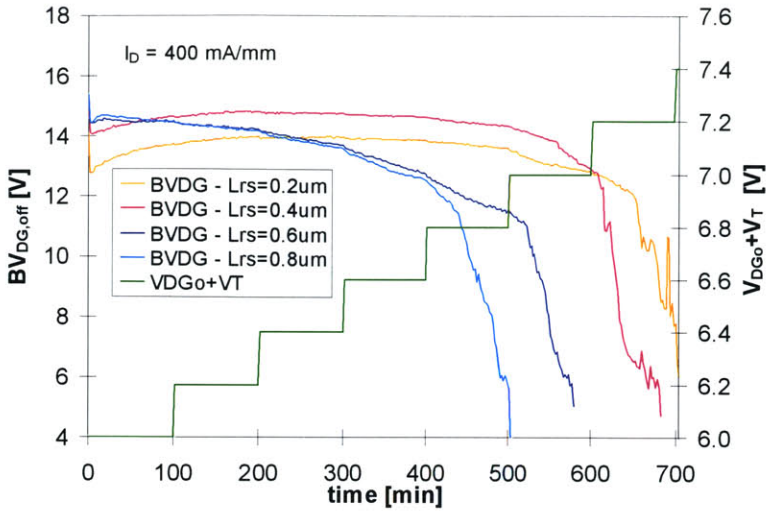

Figure 3-24: Time evolution of $BV_{DG,off}$ for voltage step-stress experiments performed on four different PHEMTs with different values of Lrs.

In summary, the experiments with varying Lrs suggest that the changes occurring on the source, drain and under the gate are not strongly dependent on the size of the source-gate gap. These results are consistent with our previous observation that impact-ionization (which is dependent on Lrd, not Lrs) is closely related to the changes in R_S and V_T. However, the behavior of the off-state breakdown voltage is significantly affected by the extent of Lrs, which is a phenomenon that remains to be explored more thoroughly.

3.3.5 Effect of Atmosphere

Since the previous experiments suggested the possibility of surface-type degradation mechanisms, we decided to investigate how degradation is affected by the atmosphere. Specifically, if there was a surface oxidation reaction occurring, then the presence of oxygen and/or moisture in the environment would have a significant effect on device degradation.

In order to explore this effect, we performed step-stressing experiments in a nitrogen environment. Figure 3-25 shows results from two identical experiments (performed on identical devices), in which one experiment was done in air, the other in nitrogen. The main observations are that in a nitrogen environment, the R_D degradation rate is slower, but the change in R_S is relatively unaffected. This thus suggests that the presence of oxygen and/or moisture accelerates degradation on the surface of the drain region.

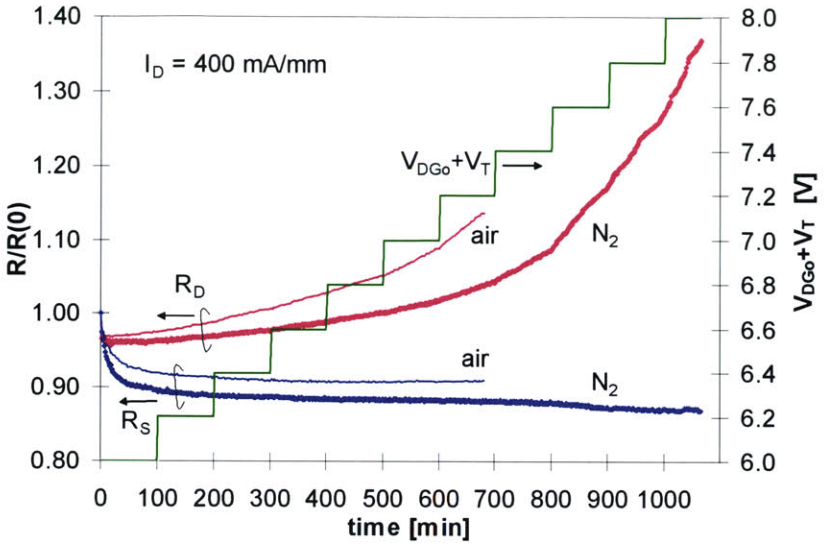

Figure 3-25: Time evolution of R_D and R_S, for voltage step-stressing experiments done in air and nitrogen environments.

Figure 3-26 illustrates the time evolution of the change in threshold voltage for the same experiments. As one can see, the initial behavior of V_T is relatively unaffected by a change in atmosphere. This is consistent with the idea that the V_T shift relates to charge modulation underneath the gate (and not surface effects).

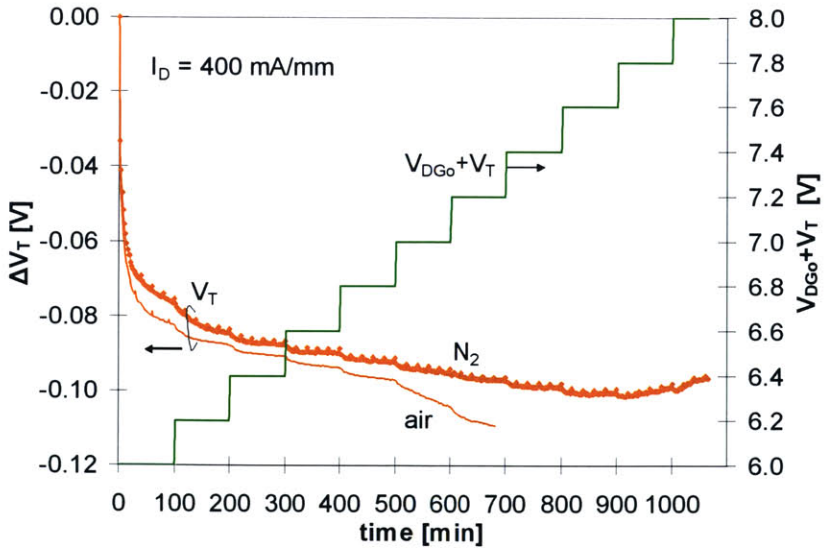

Figure 3-26: Time evolution of ΔV_T, for voltage step-stressing experiments done in air and nitrogen environments.

We can also see how the atmosphere affects degradation by looking at some other figures of merit. Figure 3-27 illustrates the time evolution of BV_{DG} for the same set of experiments. Although

the initial behavior of BV_{DG} is relatively unaffected by the atmosphere, the burnout of the device is delayed in a nitrogen environment. Thus, stressing in a nitrogen environment somehow allows the observation of an advanced regime of degradation at higher stressing voltages. This suggests that the absence of oxygen/moisture somehow supresses certain degradation effects that cause the device to burnout.

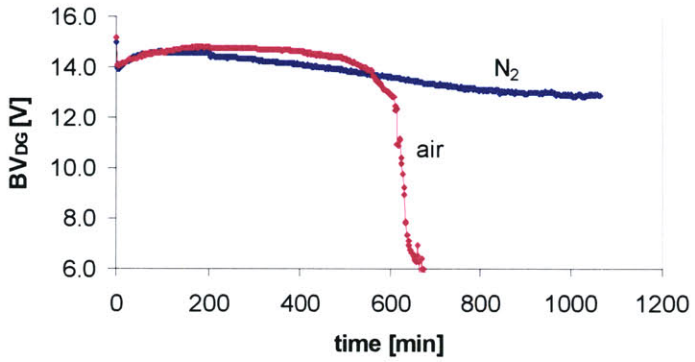

Figure 3-27: Time evolution of BV_{DG}, for voltage step-stressing experiments done in air and nitrogen environments.

The graphs of Figure 3-28 illustrate the changes in I_{Dss} and I_{Dn1}. In stressing done in air, most of what is seen is an increase in drain currents. However, in a nitrogen environment we were able to see a decrease in both I_{Dss} and I_{Dn1} at higher stressing voltages. This suggests that at this stage, the degradation on the drain side of the device is overpowering the effect of V_T shift (which tends to increase the drain current).

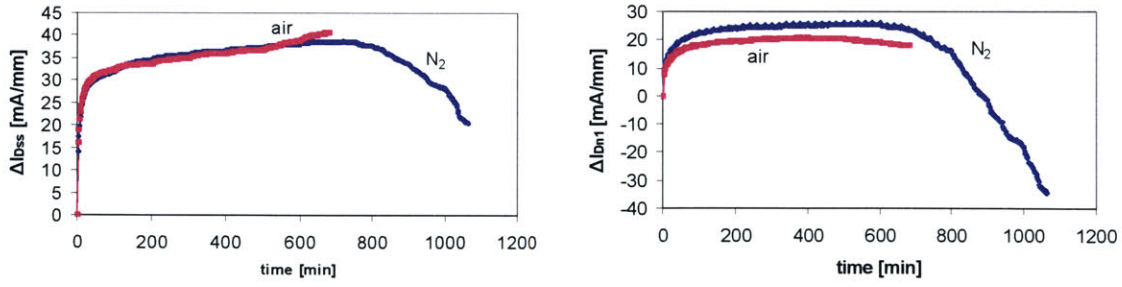

Figure 3-28: Time evolution of ΔI_{Dss} (left) and ΔI_{Dn1} (right), for voltage step-stressing experiments done in air and nitrogen environments.

3.4 PHEMTs: Summary of Findings

Our overall results shown that the main effects of electrical stressing are an increase in R_D, a decrease in V_T and a decrease in R_S. Additional experiments have revealed that the changes in R_D, R_S, and V_T are uncorrelated with one another. The increase in R_D was found to be not entirely due to impact ionization, and was accelerated by the presence of oxygen and/or moisture in the environment and high currents. This degradation was permanent and not recoverable. One possible mechanism is a surface oxidation in the gate-drain region.

The decrease in V_T is closely related to impact ionization, and was found to be recoverable with extended room-temperature storage at zero bias. A likely mechanism is holes (generated by impact ionization) neutralizing trapped electrons in DX centers under the gate [6], [8].

Regarding the decrease in R_S, its time evolution was found to be accelerated by higher stressing currents, but was apparently slowed by impact ionization. A possible mechanism is some kind of surface effect in the source region.

Because there are various degradation mechanisms involved (and several device parameters to look at) it is difficult to isolate each of the degradation phenomena and examine them independently. It would be useful to examine devices that are very similar in structure to PHEMTs, but are less complicated to study. Stressing experiments were thus performed on such special test structures, the details of which are described in the next chapter.

4 Degradation of TLMs

4.1 Introduction

In order to obtain a clearer picture of degradation mechanisms occurring in the PHEMTs, we decided to examine the degradation of Transmission-Line Model (TLM) structures. A TLM has essentially the same structure of a PHEMT, but without a gate. For the first type of TLM studied, the n+ GaAs cap has been removed, but no gate had been fabricated (leaving just a wide recess exposing the n- GaAs layer). Figure 4-1 shows a schematic cross-section of this type of TLM. Different TLMs with different lengths as defined in this picture were fabricated.

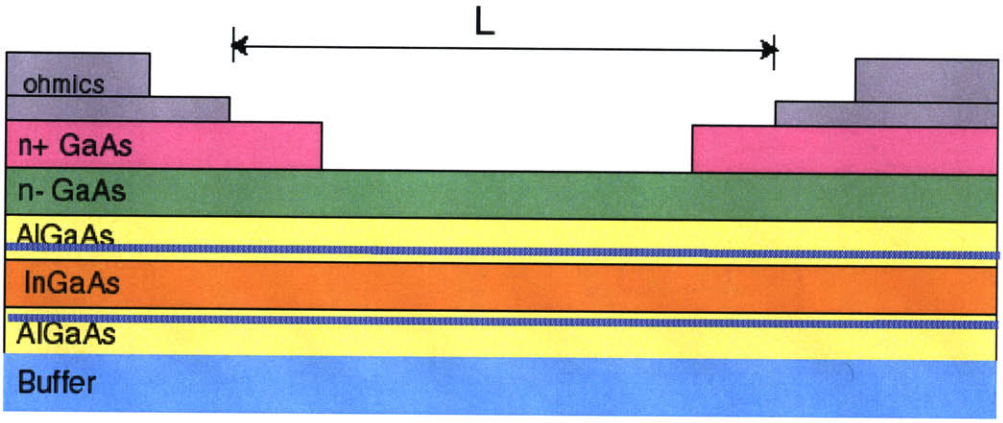

Figure 4-1: Schematic cross-section of TLM under study.

Since TLMs do not have a gate, the current is linear on the voltage (ohmic behavior) for low fields. At high fields however, the current saturates due to velocity saturation. Thus TLMs can be characterized by just two figures of merit: the low-field resistance R, and the saturation current I_{sat}. Being less complicated than PHEMTs, but having similar structure, they are ideal devices to study degradation.

4.2 Measurement and Characterization

4.2.1 Experimental Setup

In performing characterization and stressing experiments on the TLMs, the same general setup as with the PHEMTs was employed (Cascade Microtech probe station, HP 4155A, automation via HP VEE). However, for probing the structures we use four DC probes (two probes are used to contact each pad). Our measurements are performed using the Kelvin measurement technique: two probes are used to apply a voltage V_A between the source and drain, whereas the other two

probes are used in VMU mode (zero current) to monitor the actual voltage drop V_D across the TLM. In this manner we eliminate the effect of any external resistances (such as probe resistance) on our measurements.

4.2.2 TLM Characterization

To characterize the TLM, the applied voltage V_A is stepped up (in intervals of 0.05 V) while the current I_D and the actual voltage drop V_D are measured. The maximum value of V_A applied is chosen to be high enough to observe saturation in I_D, but not so high that it causes significant degradation. The I-V characteristics of the TLM are then obtained by plotting I_D versus V_D (Figure 4-2 shows typical results for a 2 μm virgin TLM).

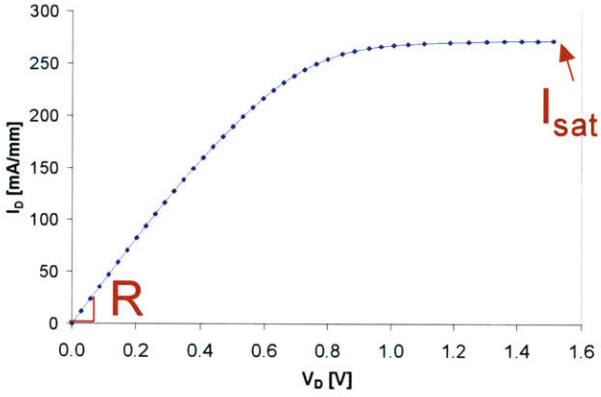

Figure 4-2: I-V Characteristics of a virgin 2 μm TLM.

Since there is no gate present, there are only two figures of merit that can be obtained from a TLM: the low-field resistance R, and the saturation current I_{sat} (due to velocity saturation). The resistance R is defined as the slope of I_D vs. V_D at $V_D = 0$. There is some ambiguity in the definition of I_{sat}, and so it is simply taken at the value of the current at the maximum resulting value of V_D (which is usually around 1.5 V for a 2 μm TLM). In the case shown above in Figure 4-2, R is found to be 2.43 ohm-mm and I_{sat} is 272 mA/mm.

4.2.3 TLM Stressing Methodology

In our stressing experiments on the TLMs, the applied voltage V_A is adjusted by our stressing program in order to keep the intrinsic voltage drop V_D constant throughout a given interval. As with the PHEMTs, the TLMs are characterized periodically throughout the experiments (I-V characteristics, R and I_{sat} are measured every two minutes of stressing). In a typical degradation

experiment, we begin stressing the TLM at V_D = 5.0 V and step it up by 0.25 V every 50 minutes (again, in order to accelerate the degradation).

4.3 Overall Results of TLM Stressing

Figure 4-3 below shows a typical set of results of this experiment on a 2 μm TLM. Disregarding the very short initial increase in Isat, there appear to be two main degradation regimes. Initially, R decreases and I_{sat} increases (Regime 1). But after about 150 minutes of stressing, R starts to increase while I_{sat} remains constant (Regime 2).

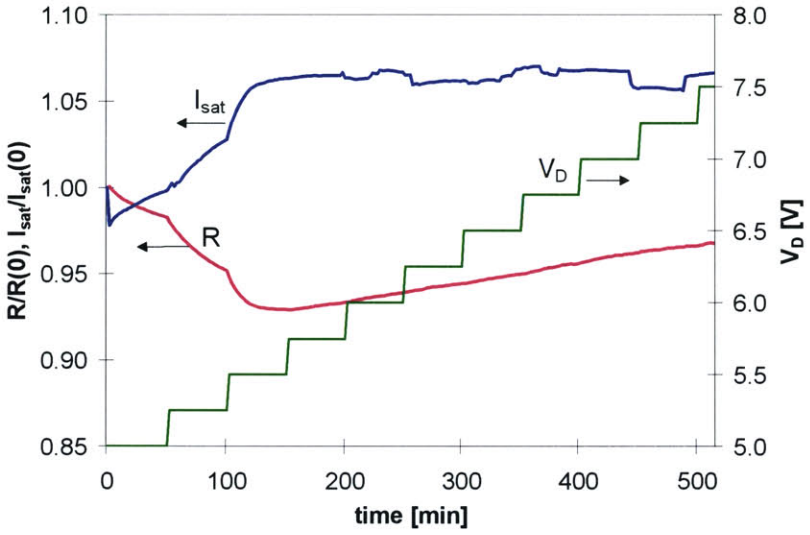

Figure 4-3: Time evolution of normalized R and I_{sat} during a step-stress experiment of a 2 μm TLM.

We can get a better idea of what is happening if we consider the equations for the normalized low-field resistance R and the saturation current I_{sat}:

$$R = 2R_c + \frac{L}{\mu_e q n_s} \tag{4.1}$$

$$I_{sat} = q n_s v_{sat} \tag{4.2}$$

Here, R_C is the contact resistance on each side, L is the length of the TLM, μ_e is the electron mobility, n_s is the sheet carrier concentration, and v_{sat} is the saturation velocity.

From these equations it is clear that any change in I_{sat} (as in Regime 1) indicates a change in sheet carrier concentration n_s. If R increases while I_{sat} remains constant (as in Regime 2), this indicates an increase in the contact resistance R_c.

To obtain a more quantitative analysis, we can perform some simple algebra to look at the time evolution of the separate components (R_c and R_{sheet}) of R. First we note that at t = 0 (before any degradation), we have:

$$R(0) = 2R_C(0) + \frac{L}{q\mu_e n_s(0)} \tag{4.3}$$

By subtracting Eq. 4.3 from Eq. 4.1, making substitutions, and solving for R_C we get:

$$R_C(t) = \frac{1}{2}\left[R(t) - [R(0) - 2R_C(0)]\frac{I_{sat}(0)}{I_{sat}(t)} \right] \tag{4.4}$$

We know R and I_{sat} as functions of time, so given the value of $R_C(0)$, we can obtain the value of R_C as a function of time. Furthermore, once we have R_C we can then extract the value of the sheet resistance:

$$R_{sheet}(t) = \frac{W}{\mu_e q n_s} = \left(\frac{W}{L}\right)\left(R(t) - 2R_C(t)\right) \tag{4.5}$$

For our calculations, we assume a value of $R_c(0)$ = 0.65 ohm-mm, which was suggested based on experiments done by Mitsubishi [23]. The graphs in Figure 4-4 illustrate the time evolution of the contact resistance and the sheet resistance extracted in this manner (this procedure adapted from [16]).

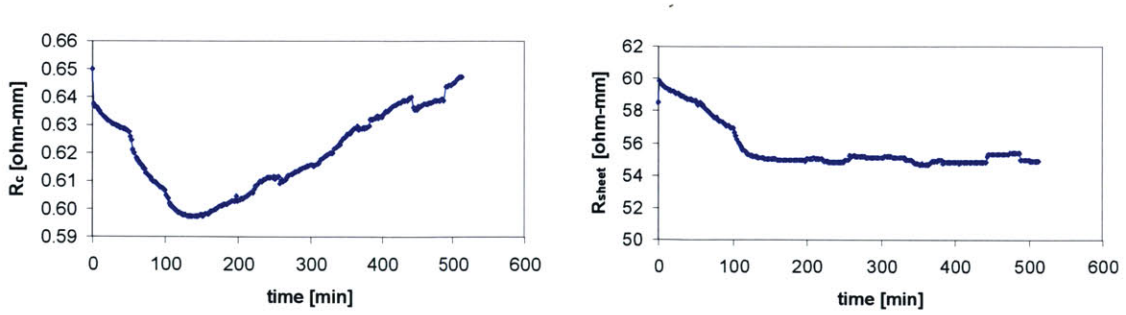

Figure 4-4: Time evolution of extracted R_c and R_{sheet} for voltage-step stress experiment on 2 μm TLM.

As shown in these graphs, the degradation of R can be separated into different regions of the TLM. In the beginning stages of stressing, R_c and R_{sheet} decrease. But after 150 minutes of

stressing, R_c begins to increase and R_{sheet} remains constant. Thus, as we suggested earlier, the first regime of degradation can be explained by an increase in sheet carrier concentration (which might correlate with the reduction in R_S observed in the PHEMTs). The second regime suggests a direct degradation of the ohmic contact resistance.

4.4 Further TLM experiments

4.4.1 Bias Reversal Experiments

Our TLM experiments described in the previous section suggest that an increase in sheet carrier concentration was responsible for the decrease in the low-field resistance R in the first regime. We thus would like to isolate the location of the n_s increase (if it was occurring uniformly across the TLM, or if it was perhaps localized to one side). In this case, we decide to perform a bias-reversal experiment, particularly one that examined the first regime of degradation (in which R decreases). Thus we performed an experiment in which the TLM was stressed at V_D = 5.0 V for a short time (100 minutes), before stressing at a V_D = -5.0 V. Figure 4-5 below shows the results of this experiment.

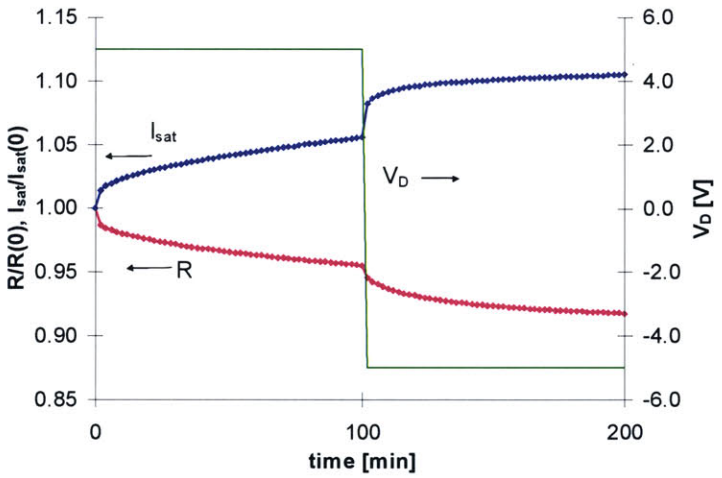

Figure 4-5: Time evolution of R and I_{sat} in bias-reversal experiment in 1st regime.

From this graph, one can see that under V_D = 5.0 V, R decreases and begins to saturate. Upon flipping the polarity, one can note two things: (1) I_{sat} increases rather sharply, and (2) R begins to decrease at a faster rate (before saturating again). These two facts suggest that n_s must be increasing preferentially on one side (if the n_s increase had been uniform, then flipping the stressing voltage would not have a significant effect). From this test alone we cannot determine on which side (the "source" or "drain") the sheet carrier concentration is increasing. However, we

hypothesize that the increase in n_s is localized on the source side, since its time evolution correlates quite well with the R_S decrease observed in the PHEMTs.

After this experiment, we also wanted to see if we could isolate the location of the contact degradation, which supposedly was responsible for the increase in the low-field resistance R in the second regime. We hypothesized that only the drain contact (or the contact into which the electrons are flowing) was being degraded. In order to confirm this idea, we performed another bias reversal experiment, this time in the second regime of degradation (in which R increases). In this experiment the TLM was stressed at a higher voltage (V_D = 6.0 V) for a longer time (1000 minutes), and then stressed at V_D = -6.0 V for another 1000 minutes. Figure 4-6 illustrates the time evolution of R and I_{sat} throughout this experiment.

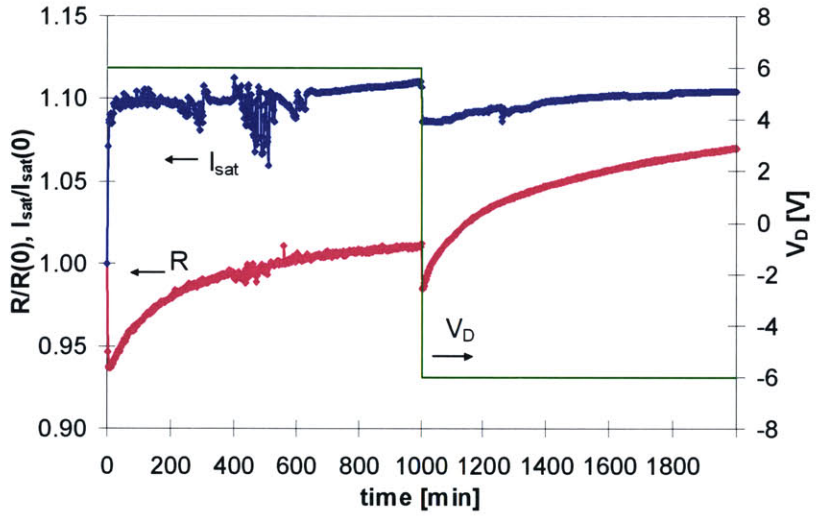

Figure 4-6: Time evolution of R and I_{sat} for bias-reversal experiment in 2nd regime.

As one can see from Figure 4-6, in the first phase the R degradation began to saturate, but then switching the polarity of the stressing voltage resulted in significant additional degradation. In addition, I_{sat} did not change significantly throughout the experiment (< 2%). From these results, we can deduce that in the first phase, only one of the ohmic contacts degrades, and upon polarity reversal the other one degrades.

Like with the other bias reversal experiment, at this point we cannot tell whether it is the drain or source contact that is being degraded with stressing. We only speculate that it is the drain contact, since it is the one that gets bombarded by hot electrons. However, a TLM structure with a terminal connected to the center of wide-recess (TLM-4, described in Section 4.5.1) will allow

us to monitor the contact resistance of each side, and hence will allow us to resolve this issue and also the issue with the sheet resistance.

Another significant observation that was noted in this experiment (and in other degradation experiments) was that impact ionization appears to decrease within the first few hours of stressing. Figure 4-7 shows extensive I-V characteristics taken at three points in the first phase of the experiment. As one can see from the graph, before any stressing, there is noticeable impact ionization present at high V_D. However, after 400 minutes of stressing, these effects disappear. Apparently, the first hours of stressing causes a major decrease of impact ionization in the TLMs. This is consistent with the decrease in impact ionization observed in the PHEMTs (see Section 3.2.2 of this report).

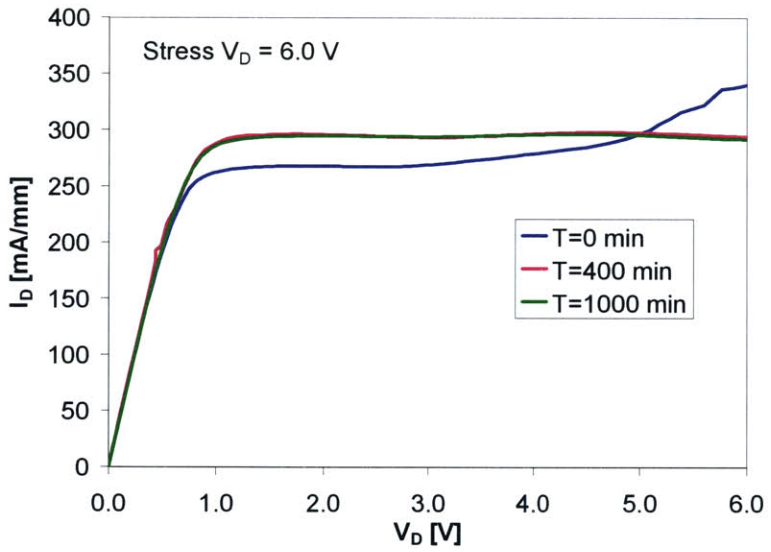

Figure 4-7: Extensive I_D-V_D characteristics of 2 μm TLM before and after stressing at V_D = 6.0 V.

4.4.2 Recovery Experiment

Now that degradation phenomena in the TLMs have been somewhat isolated, it is also desirable to know whether or not the degradation in these structures is permanent. In order to test if any of the changes in R or I_{sat} were recoverable, experiments were performed in which the TLMs were left unbiased at room temperature after a period of electrical stressing.

First of all, to test degradation recovery in the first regime, the experiment of Figure 4-5 was used—after 200 minutes of total stressing, the stressing was paused for 32 hours before resuming. The device was stressed for an additional 200 minutes. Figure 4-8 shows the results of

this experiment. As one can see, an extended pause in stressing did not affect R or I_{sat}. Thus we can conclude that the decrease in R in the first regime is not recoverable with room-temperature storage at zero bias.

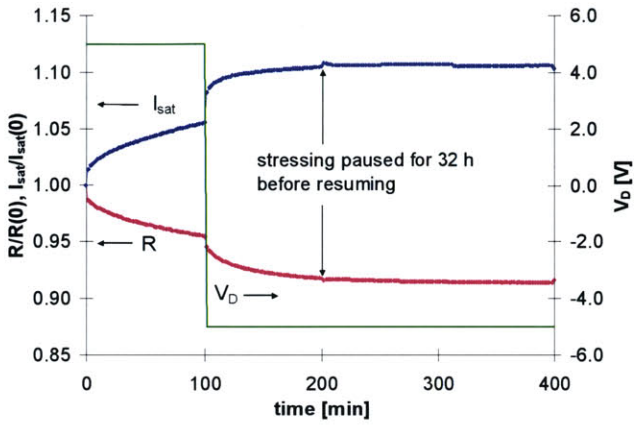

Figure 4-8: Time evolution of normalized R and I_{sat} during a recovery experiment in 1st regime.

To see if the degradation in the second regime was recoverable, a step-stress experiment identical to that of Figure 4-3 was performed on an identical 2 μm TLM. The device was stressed from V_D = 5.0 V to 6.5 V (in 0.25 intervals, every 50 minutes). Then the stressing voltage was immediately set to 0 V and kept there for 390 minutes (6.5 hours), while R and I_{sat} continued to be monitored periodically. Finally, V_D was set back to 6.5 V and was kept there for several more hours. Figure 4-9 illustrates the time evolution of R and I_{sat} throughout this experiment.

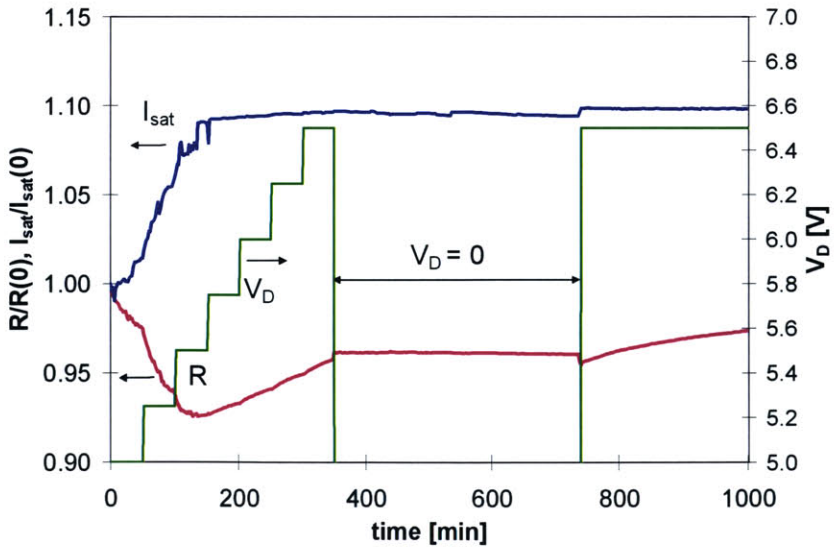

Figure 4-9: Time evolution of normalized R and I_{sat} during a step-stress experiment of a 2 μm TLM. After 350 minutes, the stressing was paused for 6.5 hours and then resumed.

As one can see from this figure, the degradation of both R and I_{sat} due to stressing are permanent. The absence of any recoverable degradation mechanism in the TLMs (which have no gate) is consistent with our association of the recoverable V_T shift in the PHEMTs to the intrinsic region underneath the gate.

4.4.3 Light Emission Experiments

Although we have identified an increase in n_s and an increase in R_C, the apparent decrease of impact ionization and the simultaneous increase in current observed in both the PHEMTs and TLMs remains a mystery. One possible explanation for these phenomena was that the current distribution across the width of the device is non-uniform initially, but it somehow becomes more uniform with stressing. Also, the formation and/or destruction of local hot-spots along the width of the TLM (as observed in [15] in PHEMTs) could possibly explain this and also the strange behavior of the off-state breakdown voltage. To look further into this issue, we decided to perform light emission experiments on the TLMs, in cooperation with Professor Mark Somerville of Olin College.

The reason for studying light-emission is the fact that AlGaAs/InGaAs PHEMTs have been observed to emit light when biased in the impact ionization regime [24]. Previous studies have demonstrated that the electroluminescence observed in AlGaAs/GaAs HEMTs is due to the recombination of channel electrons with holes generated by impact ionization [25]. Thus by observing the evolution of light-emission in TLM structures, we can then literally get a picture of impact ionization occuring across a TLM (which can be then correlated to the impact-ionization profile in a PHEMT). For these experiments, the simplicity of the TLM structure (no gate, only one bias voltage) makes the experiments much less complicated and easier to analyze.

The light-emission experiments were performed using a Cascade Microtech probe station connected to two Keithley voltage supplies, an astronomical grade CCD sensor, and a PC running LabView (to automate the data acquisition). Due to limitations with the setup, a four-probe Kelvin measurement on the TLM was not possible. As a consequence, the applied voltage that was stepped included any external voltage drops occurring over the cables and the probe resistance).

The stressing conditions for our first light-emission experiment (on a 2 μm TLM) were similar to the TLM step-stressing experiments described in Section 4.3. In this particular experiment, the applied voltage was initially set at 5 V for 67 minutes, and then periodically stepped up in 0.25 V intervals (left graph of Figure 4-10). Photographs were taken at various points throughout the

stressing experiment, most frequently at the beginning of stressing. From each picture we were then able to obtain several key figures of merit, including the total light emission (sum of all pixel values in the image). The right graph of Figure 4-10 shows the total light emission as a function of stressing time (each data point corresponds to data from one picture).

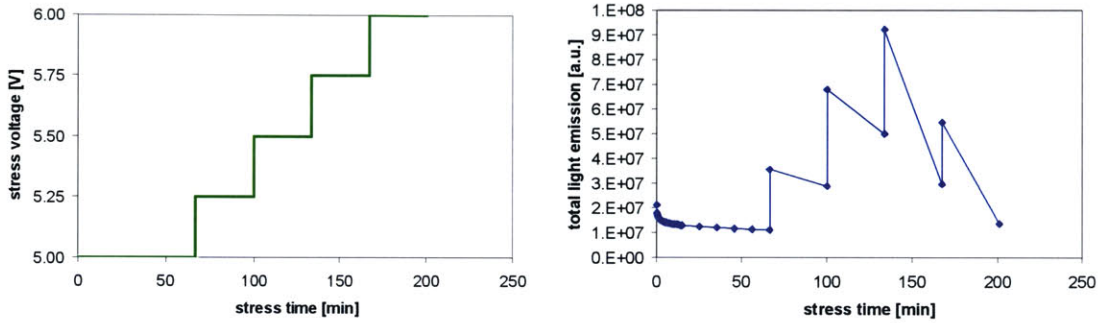

Figure 4-10: Applied stressing voltage (left) and total light emission (right) vs. stressing time for light-emission experiment on a 2 µm TLM.

As one can see from these graphs, the total light emission decreases with stressing (it only increases upon an increase of the stressing voltage). By the end of the experiment (209 minutes of stressing), the total light emission has become less than the initial value. This behavior correlates with our previous observations that showed a decrease in impact ionization and hot-electron effects as a result of stressing.

Throughout the stressing experiment, the stressing current flowing through the TLM was also monitored. With these data, we were then able to generate a plot of the total light emission versus the measured drain current (Figure 4-11). As one can see, the total light emission is roughly proportional to the amount of current. With this in mind, we can then say that the light-emission picture gives a rough indication of the current distribution in the TLM.

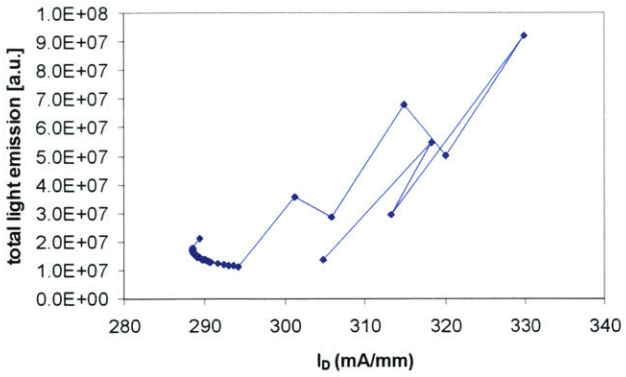

Figure 4-11: Total light-emission vs. stressing current in TLM step-stress experiment.

In order to fully understand the light-emission behavior, it is necessary to examine the actual light-emission photographs taken during this experiment. There are several pictures; three of the photographs are shown on the next page. Figure 4-12 is an image taken at the start of the experiment (at stress voltage of 5 V, with only 0.04 seconds of stressing). Figure 4-13 is an image taken after 67 minutes of stressing (at a stress voltage of 5 V). Figure 4-14 is an image taken at end of the experiment (at a stress voltage of 6 V, after 209 minutes of stressing). From these images we can see that stressing causes the light emission to spread out over the width of the TLM, while its overall intensity decreases. Furthermore, we see that the light intensity is initially concentrated in the center, whereas after stressing, it becomes concentrated at the ends.

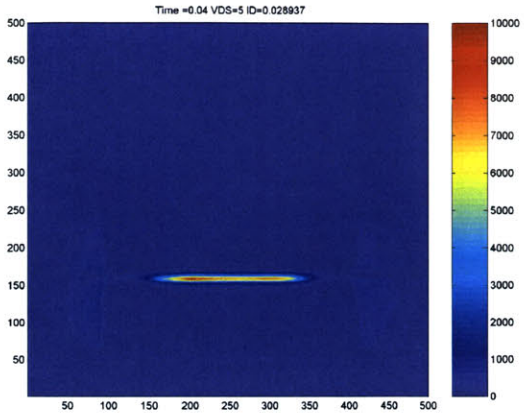

Figure 4-12: Light-emission photograph taken at start of TLM step-stressing experiment (at a stress voltage of 5 V).

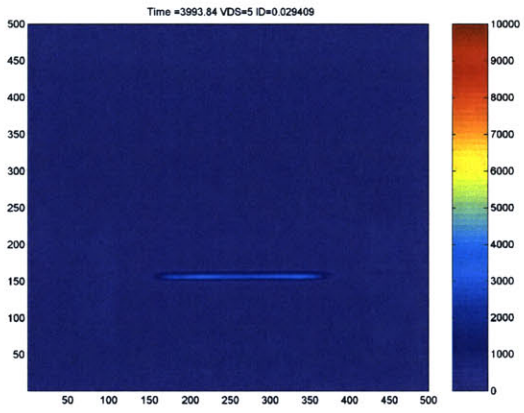

Figure 4-13: Light-emission photograph taken 67 min after start of TLM step-stressing experiment (at a stress voltage of 5 V).

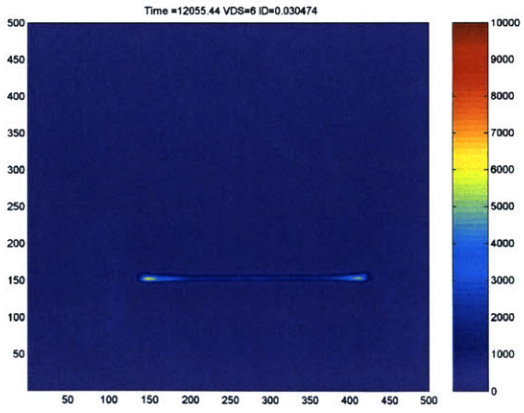

Figure 4-14: Light-emission photograph taken at end of TLM step-stressing experiment (at a stress voltage of 6 V).

The distribution of light intensity along the width of the TLM can be observed more clearly by summing up the pixel values over each column of the image, and plotting them across the width of the TLM. This was done in MATLAB for each photograph. Figure 4-15 shows such light-emission profiles for the three images shown previously (corresponding to before, during, and after the stressing experiment). Again, the key observations from this graph are that, with stressing (1) the light emission spreads out in width, (2) the peaks of light intensity shift from the center to the edges, and (3) the overall amount of light emission decreases.

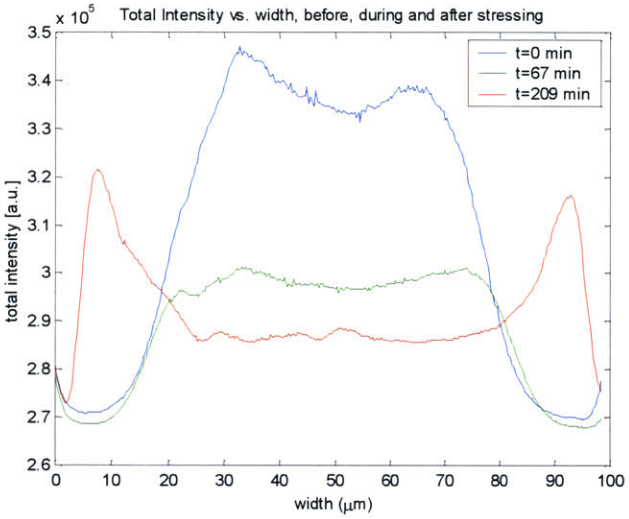

Figure 4-15: Light-emission profile along the width of the TLM, before (blue), during (green) and after (red) the TLM step-stressing experiment.

To obtain a more comprehensive picture of the "spreading" of the light emission across the width of the TLM, we can utilize a mesh grid in MATLAB in order to see how the light-emission profile evolves in time. We can compile the profiles from each photograph (as a function of width) together in a color contour plot in order to plot this data as a function of stressing time. For the regions of time in between data points, the values are interpolated. Since fewer pictures were taken in the later portion of the experiment, this data is best viewed in two sets, one for the first 67 minutes of stressing (stressing at a constant voltage of 5 V), and one for the remainder of the experiment (starting at constant voltage of 5.25 V, and stepped up regularly to 6 V). Figure 4-16 illustrates the two graphs illustrating this. Note that in the right graph, the 3 discontinuities at t = 101, 134 and 167 minutes arise from the instances where the stressing voltage was stepped up.

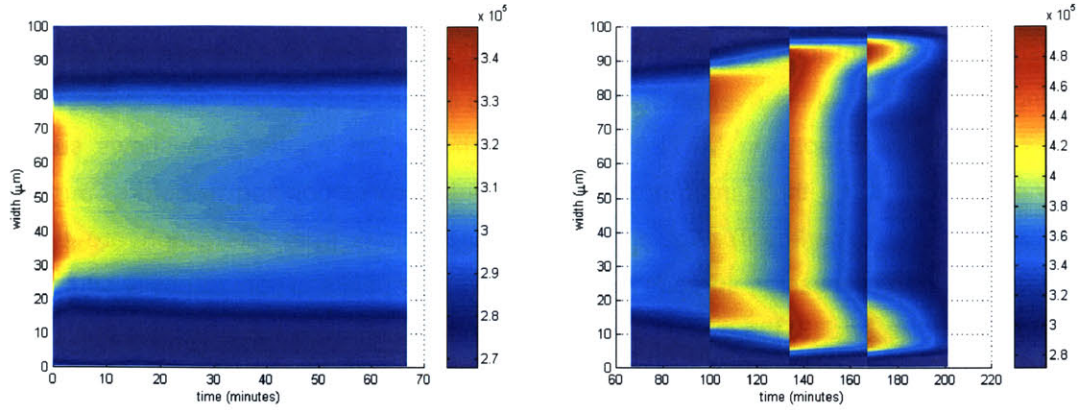

Figure 4-16: Mesh plot illustrating the time evolution of light-emission profiles for the first 67 minutes (left) and for the remaining 142 minutes (right) of the TLM step-stressing experiment.

From the left graph one can clearly see that in the first part of the experiment (constant stressing at 5 V), the light emission profile initially peaked in the center gradually decreases in intensity and becomes more uniform. In the second part of the experiment (right graph) one can see that the the light emission decreases and continues to spreads out with constant voltage stressing (the emitted intensity only increases at the periodic instances where the stressing voltage is stepped up). From these two graphs, we can see that the light emission has spread from covering the center ~55 μm to almost covering the entire width (~ 90 μm). The correlation between light-emission and current suggests that the current flow is initially restricted to the center, but then spreads out and concentrates at the edges. As one can observe from the right figure, the width of the new hot-spots formed at the edges are about ~5-10 μm each. Such effects occurring over such large dimensions (few microns) suggest that the mechanism behind this phenomenon might not be electronic but rather might possibly be related to the temperature distribution along the width of the TLM.

4.4.4 Effect of Atmosphere

Considering the fact that the stressing environment had a significant effect on device degradation in PHEMTs, we also wanted to see how this factor played a role in the degradation of TLMs. Recall that in Section 3.3.5, it was found that the electrical stressing of PHEMTs in nitrogen resulted in less degradation than stressing in air. We thus wanted to see if similar behavior also occurred in the TLMs.

To explore this issue, we performed step-stressing experiments in a nitrogen atmosphere. Figure 4-17 below shows results from two identical step-stressing experiments (performed on identical devices), in which one experiment was done in air (same experiment as Figure 4-3), the other in nitrogen.

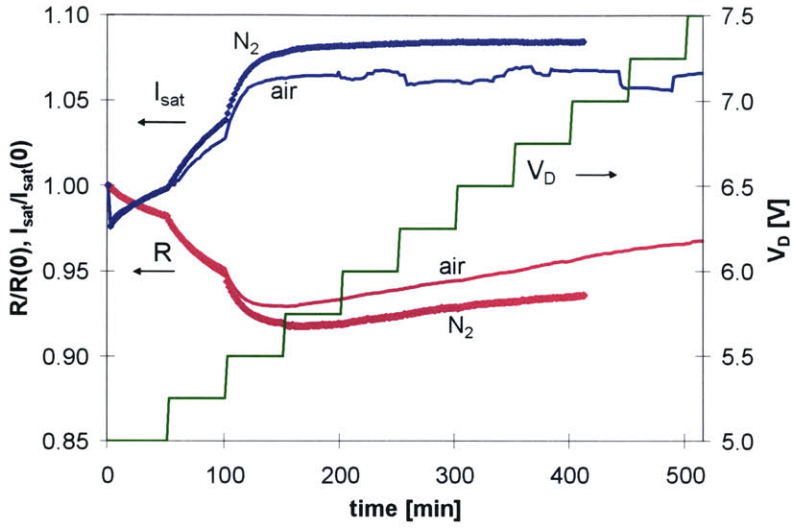

Figure 4-17: Time evolution of normalized R and I_{sat} for voltage step-stressing experiments done in air and nitrogen environments, on a 2 μm TLM.

In the first regime (less than 150 minutes of stressing), there seems to be no effect as a result of the change in environment; the decrease in R is unaffected, and the increase in I_{sat} is only slightly affected. In the second regime, one can see that there is less R degradation. However, this difference is small compared to the difference in R_D degradation seen in PHEMTs, when comparing results of stressing performed in nitrogen and air. In other words, stressing in a nitrogen environment seems to have much more of an effect on the degradation of PHEMTs than it does in the degradation of TLMs. This hints at the possibility that the R_D degradation in PHEMTs (which is accelerated by the presence of oxygen and/or moisture) may be concentrated in an region of the device that is not present in the TLMs (i.e. in an area of exposed AlGaAs, between the drain and the gate).

4.5 Other TLM structures

From the previous sections, one can see how we were able to obtain key insight from studying degradation in standard TLM structures. This led us to create additional test structures, which were especially designed to enable us to isolate the location of the degradation mechanisms more accurately. The first type of new device (TLM-4), is like the original structure, except it has an additional contact used to monitor the voltage midway between the source and drain. In another set of new structures (TLM-5), various TLMs were fabricated, which are all identical except that the distance between the edges of the ohmic & n+ GaAs were different. The details of degradation experiments performed on these new structures is outlined next.

4.5.1 "Tapped" TLM structure (TLM-4)

The first type of new test structure we designed is laid out in Figure 4-18. This device is referred to as a "tapped" TLM structure, since it allows us to "tap," or monitor, the voltage at the midpoint of the device.

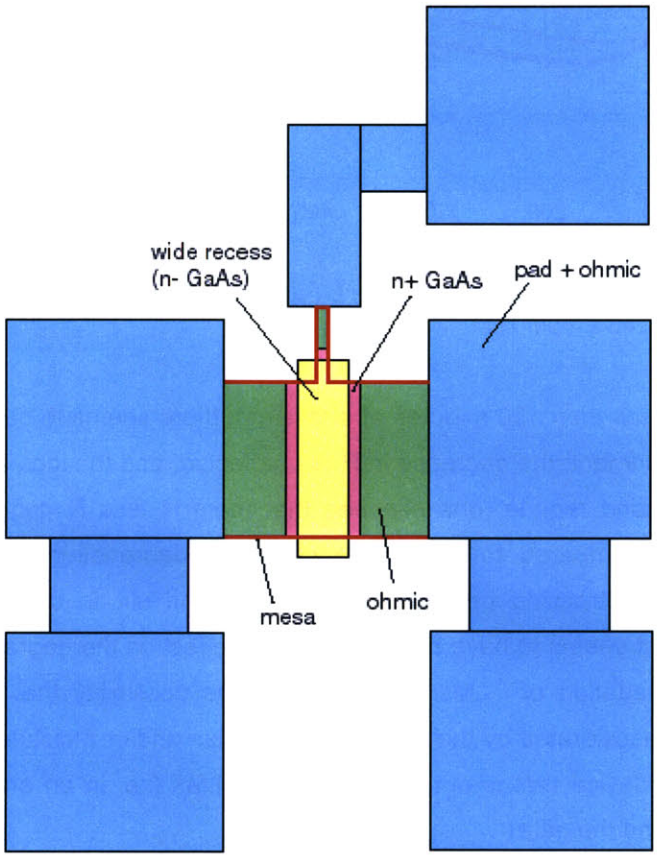

Figure 4-18: Layout view of "tapped" TLM structure, illustrating extra contact to center of device.

Using this structure in this manner, we can extract the resistance of each side of the device and thus decompose the total resistance R into "source" and "drain" resistances. This was desired, since we realized that from our bias reversal experiments alone (see Section 4.4.1) it was impossible to determine whether the changes in the total resistance were due to mechanisms occurring on the source side or on the drain side. Thus, a step-stressing experiment on this "tapped" TLM was performed, throughout which the source and drain resistances were measured as well as the total resistance and saturation current. Figure 4-19 shows the time evolution of total resistance R and I_{sat} for a step-stressing experiment performed on such a device, of length L = 7 μm. Because this type of structure is much longer, the stressing voltages were chosen to be significantly higher (starting at 9 V).

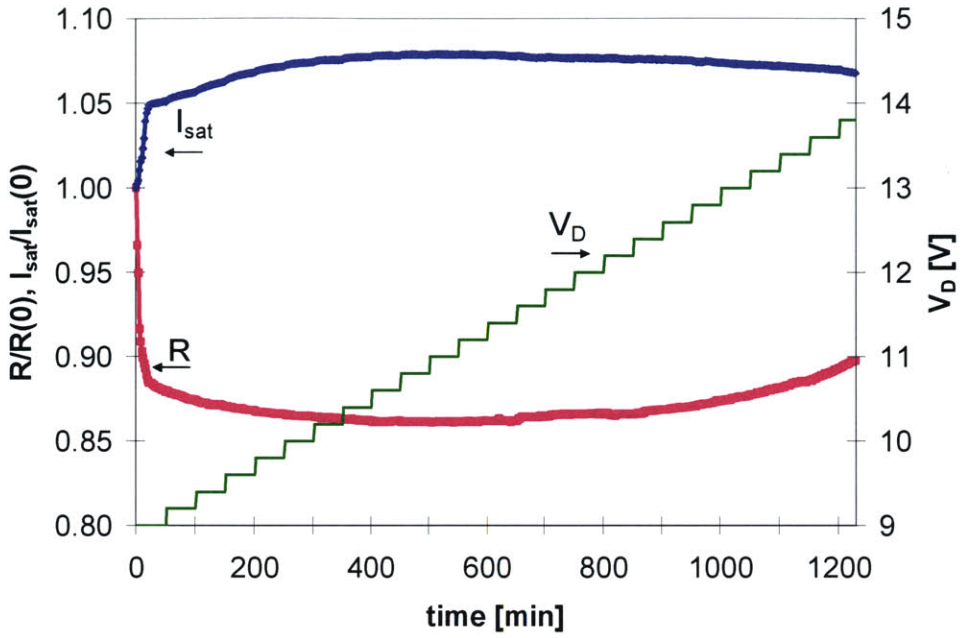

Figure 4-19: Time evolution of normalized R and I_{sat} in a step-stressing experiment on a 7μm "tapped" TLM.

As one can see from Figure 4-19, the behavior is similar to our earlier experiments on the standard TLMs. In the first regime (here, T < 600 minutes), R decreases and I_{sat} increases; in the second regime (after 600 minutes), R increases and I_{sat} remains more or less constant.

Figure 4-20 shows the time evolution of the R_S and R_D extracted from this experiment. First of all, from this graph it is quite clear that in the first regime, R_S decreases much more significantly than R_D. This agrees with our previous suggestion that the decrease in R in the first regime is due to an increase in sheet carrier concentration localized on the source side of the device. In the second regime, the increase in R_D appreciably outweighs the increase in R_S. This verifies our other assumption that the increase in R in the second regime is due to the degradation of the drain ohmic contact. These observations are consistent with the behavior observed in PHEMTs as described in Chapter 3. A detailed comparison will be carried out in Chapter 5.

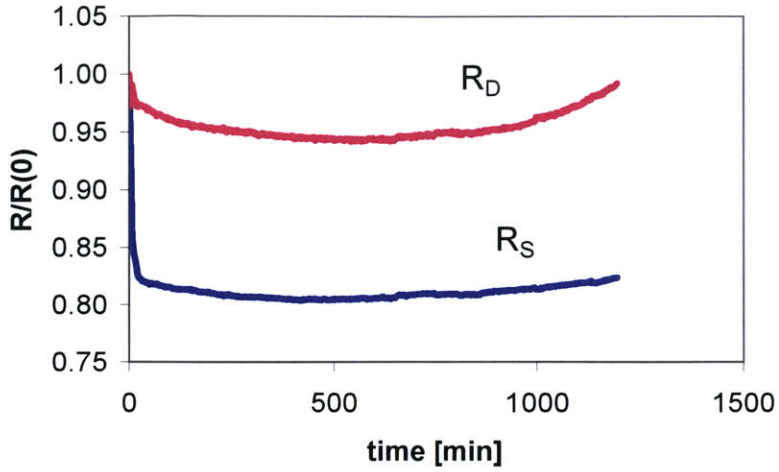

Figure 4-20: Time evolution of extracted drain resistance and source resistance, for a step-stressing experiment on a 7μm "tapped" TLM.

4.5.2 Effect of ohmic contact separation (TLM-5)

Although we can now ascertain that the degradation is occurring on the drain ohmic contact, we cannot determine its exact location (whether it is on the ohmic metal, the surface of the exposed n+ GaAs, or elsewhere). To address this we studied a set of TLMs in which the extent of the wide recess was the same (L_2 = 0.8μm) but had different values for the distance between the ohmic contacts (L_1 = 1.6μm, 2.0μm, and 2.4μm). In this way, we could isolate degradation occurring on top surface of exposed n+GaAs (determined by L_1-L_2) from degradation occurring at edge of n+GaAs and/or at edge of ohmic metal. Figure 4-21 illustrates the results from identical step-stressing experiments peformed on the three devices in this set.

As one can see from this figure, the only main difference amongst the three devices is the time to burnout—as expected, devices with longer L will take a longer time to burnout since they can sustain a higher electric field. However, by comparing the behavior of R and I_{sat}, one cannot really see an appreciable difference in the degradation behavior between the three devices. It thus seems like the device degradation occuring on both the source and the drain is not affected by the extent of the n+ GaAs ledge (and thus must be localized either on the exposed n- GaAs, or closer to the ohmic contacts).

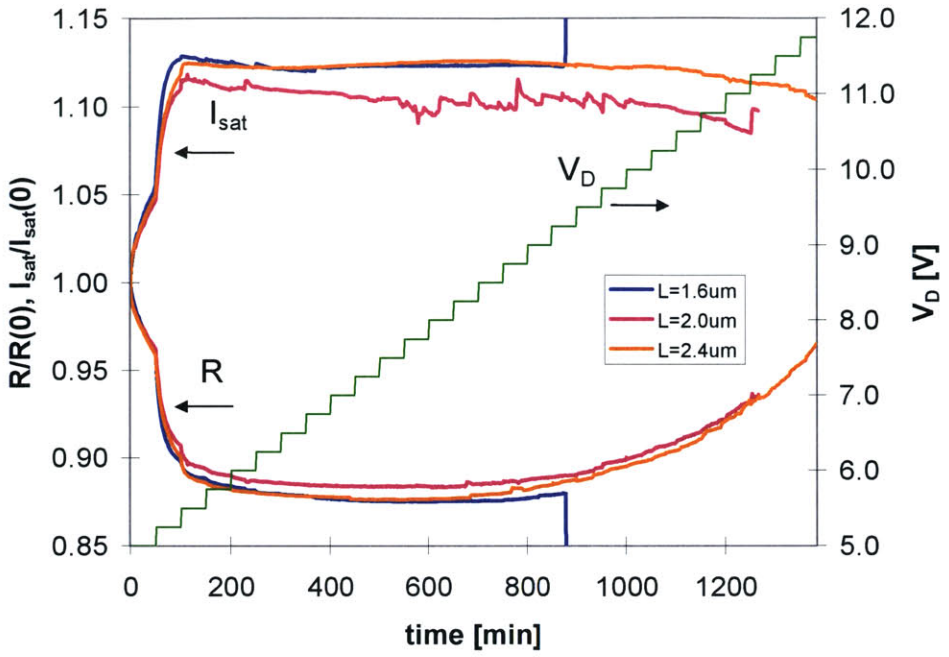

Figure 4-21: Time evolution of R and Isat for step-stressing experiment on three TLMs (of type TLM-5) of different lengths.

4.6 TLMs: Summary of Findings

In summary, we have found that we can separate the degradation behavior of TLMs into two regimes. In Regime 1, the resistance decreases and the saturation current increases. This is attributed to an increase in sheet carrier concentration localized on the source side of the device. In Regime 2, the resistance increases due to the degradation of the drain ohmic contact, which is slightly worsened by the presence of oxygen and/or moisture in the air. Neither of these degradation phenomena are recoverable with room-temperature unbiased storage at room temperature.

In all our various different stressing experiments, we have observed the presence of impact ionization, which decreases with stressing. This is confirmed from light emission experiments, where we have also observed that the current distribution along the width of the TLM dramatically changing with stress. In the next chapter, we will present a more detailed analysis correlating the observations from the TLM experiments to our findings in the PHEMTs.

5 Discussion

5.1 Introduction

This chapter contains a comparison of the results obtained from the degradation experiments performed on both the TLMs and PHEMTs. A general discussion of these data follows, in which we compare our observations with those seen in the literature. We conclude with a discussion of the physical mechanisms responsible for electrical degradation of PHEMTs.

5.2 Relating TLMs to PHEMTs

As described in the previous chapter, we have observed various degradation phenomena in the TLMs that can be correlated with degradation behavior observed in PHEMTs, as presented in Chapter 4. First of all, in Regime 1 of TLM degradation, we observed an increase in sheet carrier concentration (concluded from the decrease in R and the increase in I_{sat}, as seen in Figure 4-3). Further experiments confirmed that this increase was localized to the source side of the device (see Figure 4-20). It was also found that the increase in n_s was not accelerated by changing the atmosphere to air (see Figure 4-17). All these observations are consistent with the decrease in source resistance seen in PHEMTs. In this case, the decrease in R_S occurred only in the initial stages of degradation (and then saturates), and was unaffected by changing the environment to air.

In Regime 2 of TLM degradation, we saw an increase in contact resistance (gathered from the fact that R increased while I_{sat} remained constant, as seen in Figure 4-3). Additional experiments confirmed that it was the drain contact that sustains most of the damage (see Figure 4-20), and that this degradation is slightly mitigated when stressed in nitrogen as opposed to air (see Figure 4-17). All of these observations are consistent with the increase in the drain resistance observed in the PHEMTs. In this case, the increase in R_D began at a later stage of degradation, and was greatly suppressed by changing the environment from air to nitrogen.

Finally, another observation noted in the TLMs is that there was no recovery of the degradation in either Regime 1 or Regime 2 (see Figure 4-8 and Figure 4-9). This is consistent with the facts that there was no recovery of R_S and R_D in the PHEMTs (see left graph of Figure 3-14), and that the only degradation recovery observed in the PHEMTs was that of the threshold voltage (see right graph of Figure 3-14), which was associated with the presence of a gate (absent in the TLMs).

Table 3 captures a summary of all the above comparisons.

Table 3: A summary of the relation of observations in TLMs to corresponding behaviors in PHEMTs.

Observation in TLMs	***Correlation with PHEMTs***
1^{st} regime: $n_s \uparrow$, on source side (atmosphere independent, saturates)	$R_S \downarrow$ (atmosphere independent, saturates)
2^{nd} regime: $R_C \uparrow$, on drain side (accelerated in air environment)	$R_D \uparrow$ (accelerated in air environment)
No degradation recovery	No recovery in R_D, R_S; V_T recovery

As one can see from this table, the observations seen in the TLMs correlate quite well with analogous degradation phenomena observed in the PHEMTs. Thus we can associate the changes in R_S to an increase in sheet carrier concentration on the source side, and we can associate the increase in R_D with the degradation of the drain ohmic contact. This finding is important because it then allows us to use the simple TLM structures to perform several experiments (light-emission, materials analysis, etc) which are quite difficult to do in PHEMTs.

However, at this point we cannot make the claim that degradation effects seen in the TLMs are entirely responsible for the degradation of R_S and R_D in the PHEMTs; clearly, the presence of a gate complicates things somewhat and will affect the dynamics of the physical mechanisms involved in degradation. This is supported by the fact that data from our PHEMT degradation experiments (such as those discussed in Section 3.3.3 and Section 3.3.5) suggest the presence of surface effects in the drain-gate region (a region with no counter-part in the TLMs) significantly affecting degradation. Thus in order to obtain a better overall idea of all the possible mechanisms that are affecting the PHEMTs, we must look at all of the data obtained, in conjunction with previous observations done in the literature.

5.3 Comparison to Literature

As mentioned in Chapter 1, previous studies in the area of GaAs PHEMT reliability have been carried out, the majority of which explore the effects of hot-electron degradation as a result of high-voltage stressing [4, 5, 7, 10, 18, 20]. We thus sought to compare the findings of our stressing experiments to those in the literature, in order to obtain additional insight into the possible mechanisms behind the degradation.

Regarding the drain resistance, it is already well-known that it increases as a result of electrical stressing. In most papers, the increase in R_D is attributed to a widening of the depletion region

between the gate and drain, as a result of the creation and filling of electron traps in the passivation layer above that area [3, 5, 6, 11, 18]. In this case, it is believed that hot electrons (generated by impact ionization) are injected into the passivation layer in the gate-drain region.

Although this explanation seems valid for the PHEMTs examined in those studies, it does not seem to explain the R_D degradation observed in our devices (as seen in Figure 3-1). The increase in R_D that was observed in the literature was almost always accompanied by an increase in the breakdown voltage [5, 6, 11, 18]. This was because the space-charge widening between the gate and drain in those devices resulted in a reduction of the maximum electric field in that region. In our devices however, we did not observe an increase in $BV_{DG,off}$; we actually observed a decrease, especially at the beginning of stressing and then immediately before burnout (see Figure 3-5). At high voltages, we did observe a decrease in impact-ionization and an alleviation of the current upturn (Figure 3-7 and Figure 3-6, respectively), which was also seen by [6] and does correlate with the decrease in electric field. So in our devices, it appears that the *on-state* breakdown voltage increases as a result of electrical stressing, while the *off-state* breakdown voltage decreases. Also, our experiments indicate that impact ionization was not the primary mechanism behind the R_D increase, and that it was more strongly correlated with stressing current (see Figure 3-13) and the environment surrounding the device (see Figure 3-25). Thus it is apparent that a simple charge-trapping mechanism in the passivation layer cannot explain the R_D degradation in our devices.

From our TLM experiments, we also know that ohmic contact degradation plays an important role in the increase of R_D. However, just by looking at the relative magnitudes of the R degradation in TLMs (up to 13% increase from its minimum value, as seen in Figure 4-6) and the R_D degradation in PHEMTs (up to 53% increase from its minimum value, as seen in Figure 3-8), it seems that the increase in R_D cannot be explained by an increase in contact resistance degradation alone. This is not surprising; recall that in PHEMTs, the presence of a gate creates a pinch-off point and a very high electric field on the drain side, which produces a large amount of hot electrons (which can produce effects that accelerate degradation). This effect is not present in the TLMs, and thus the resistance degradation is less severe. This is also apparent if we compare the results of stressing PHEMTs and TLMs in a nitrogen environment—the degradation of R_D in the PHEMTs was significantly alleviated by the absence of air in the environment (Figure 3-25), whereas the degradation of R in the TLMs was only slightly improved (Figure 4-17). Clearly ohmic degradation is present in the PHEMTs, but it is just one of the mechanisms affecting R_D. There were no reports found in the literature that identified contact degradation as the main cause of the drain resistance increase seen in GaAs PHEMTs.

Since our experiments also indicate the presence of an atmosphere-dependent mechanism affecting R_D (which is accelerated by drain stressing current), we do have strong indications that some kind of surface effects (possibly an oxidation or decomposition reaction) is occurring in the gate-drain region. Such surface effects can create a leakage path between the drain and gate, which might explain the odd changes in off-state breakdown voltage [12]. Previous studies show that GaAs PHEMTs are extremely sensitive to surface conditions; due to the close proximity of the PHEMT channel to the surface, any changes on the surface (such as oxidation reactions) will have strong effects on the gate-drain depletion and on the current-carrying capacity [3]. This can also explain why, in some of our experiments (such those done at higher stressing current of I_D = 450 mA/mm, discussed in Section 3.3.1) we begin to observe a *decrease* in drain current accompanying the dramatic increases in R_D, after prolonged stressing (see behavior of I_{Dss} and I_{Dn1} in Figure 3-9 and Figure 3-10). It appears that at this point, the decrease in current (due to this surface degradation) is overcoming the increase in current that is due to the decrease in V_T, which mostly takes place in the initial stages of stressing.

The shift in the threshold voltage (as seen in Figure 3-2) is another major phenomenon that was always present in our PHEMT degradation experiments. By far, this is the observation that is most similar to what is described in the literature (mostly in [5-9]) and seemed to be the most widely understood. In these studies, a non-permanent decrease of the threshold voltage (and increase of the drain current) was observed after hot-electron stressing. In [8], it was observed that these changes were recoverable after rather long (~100 h) storage at room temperature at no applied bias. This corresponds quite accurately with observations in our experiments; recall our experiment described in Section 3.3.2, in which the shift in the threshold voltage recovered significantly after unbiased storage for an equivalent amount of time (see behavior of V_T in Figure 3-14).

To explain the V_T shift, Meneghesso et al. in [8] present the following theory: hot holes, generated by impact-ionization, acquire enough energy to overcome the AlGaAs/InGaAs energy barrier, and are captured in deep levels in the AlGaAs layer under the gate. This neutralizes the trapped electrons, and this modulation of charge is what causes V_T to decrease. Further analysis done in [6, 8] relating ΔI_D and g_m demonstrated that the observed increase in I_D can be fully attributed to the reduction in V_T. This type of analysis was also done for our devices. Figure 5-1 illustrates a graph illustrating the relation between g_m and the changes in I_D and V_T for the first 100 minutes of a PHEMT stressing experiment. One can see that for $V_{GS} < 0$, ΔI_D is equal to the product of g_m and $-\Delta V_T$, which verifies that the increase in I_D at low gate voltages is solely due to the V_T shift. It appears that another mechanism affects I_D at higher V_{GS} (as mentioned in Section 3.3.2).

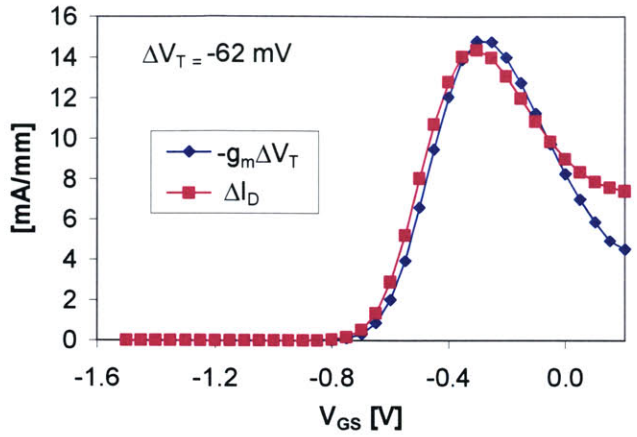

Figure 5-1: ΔI_D and $-g_m \Delta VT$ as a function of V_{GS}. ΔI_D and g_m have been calculated at V_{DS} =0.2 V. ΔI_D is the change in current after 100 minutes of stressing at constant I_D = 400 mA/mm , $V_{DGo}+V_T$ = 6.0 V.

In addition to the reports mentioned above, there were also reports of an *increase* in threshold voltage (and/or a decrease in current) with stressing [4, 10, 11]. At first this may seem contradictory, but in [3] and [5] it is explained that the relative amount of stressing will greatly determine what kind of degradation is observed. This is illustrated well in [5], where it is reported that as the bias stressing voltage is increased (or the stress time made longer) the increase in drain current tends to vanish, and the change in drain current eventually becomes negative. This idea correlates with the observations from our experiments; in the initial stages of stressing, we always observed an increase in drain current (as seen in Figure 3-2). However, if the stressing was severe and/or prolonged (such as in the experiments at I_D = 450 mA/mm discussed in Section 3.3.1, or the prolonged experiments done in nitrogen discussed in Section 3.3.5), the increase in drain current saturated and eventually took a downturn (see behavior of I_{Dss} and I_{Dn1} in Figure 3-9 and Figure 3-10, and in Figure 3-28). The explanation for the drain current decrease as described in [4, 11] is similar to the explanation widely given for the drain resistance degradation; it is reported that I_D decreases as a result of increased surface depletion on the extrinsic drain, as a result of hot-electron-induced trap accumulation in the nitride passivation on the drain side of the gate. However, as mentioned previously, this theory does not appear to explain the degradation observed in our devices, and a surface reaction seems more probable.

In our PHEMT stressing experiments, a permanent decrease in source resistance was another major observation (see Figure 3-1). Although slight decreases in R_S have been seen by Canali et al. in [6] and Meneghesso et al. in [8], this phenomenon is not often observed or studied in the literature (as it is not as crucial and worrying as the increase in R_D). In our experiments on both TLMs and PHEMTs, we have attributed the decrease in R_S to be a result of an increase in sheet carrier concentration on the source side of the device. The actual mechanisms for the increase in

n_s are not quite clear; from our experiments we know that this effect scales with the extent of the gate-source gap (see Figure 3-23), which thus suggests some kind of surface effect. However, the decrease in R_S is not dependent on the atmosphere (see Figure 3-25), so it is not likely an oxidation reaction.

In [3], Leoni et al. also observed that GaAs PHEMTs were subject to a quick, permanent increase in channel electron concentration as a result of stressing. The theory behind this phenomenon is that hot carriers are injected into the buffer layer, and these carriers then release their energy to help activate planar dopants below the channel [3]. So if this was the case, then impact ionization (which would generate more hot holes) would accelerate such an increase in carrier concentration. However, in our experiments, we saw that the R_S decrease was actually slowed down by impact ionization (see Figure 3-19), and thus this hot-carrier theory cannot explain the observation seen in our devices.

5.4 Degradation Mechanisms

Our analysis of the data obtained from all our stressing experiments, along with findings from previous GaAs PHEMT reliability studies in the literature, allow us to form theories that identify the degradation mechanisms that are present in GaAs PHEMTs. Although a decrease in source resistance has not been widely explored in previous studies, from our TLM experiments we were able to conclude that the decrease in R_S is due to a permanent increase in sheet carrier concentration concentrated on the source side of the device. Experiments on the PHEMTs suggested that this phenomenon is most likely due to surface effects, which are unaffected by the environment. This degradation was not recoverable.

Concerning the drain side of the device, the degradation mechanisms are a bit more complicated. From the TLM experiments we know that the drain ohmic contact is degrading, and that it is localized to either the ohmic metal or the exposed n- GaAs layer. However, from our PHEMT experiments we also see strong indications of atmosphere-dependent surface effects (perhaps an oxidation reaction) occurring in the gate-drain region. Such effects might be reducing the local sheet carrier concentration, which would explain the increase in drain resistance. This surface effect appears to be separate from the ohmic contact degradation observed in the TLMs. Thus it seems that we can attribute the R_D increase in PHEMTs to both (1) ohmic contact degradation, as a result of hot electron damage, and (2) effects due to a surface oxidation reaction in the gate-drain region.

Relating to the gate, we observe a significant downward shift in the threshold voltage, which in turn causes an increase in drain current. We found the decrease in V_T to be strongly correlated

with impact ionization, and recoverable with prolonged unbiased storage at room temperature. This exact phenomenon has been observed in the literature, and extensive studies have concluded that charge modulation underneath the gate is responsible for the shift in V_T. It is understood that hot holes (generated by impact ionization) de-trap electrons that lie in DX centers underneath the gate (likely in the AlGaAs layer).

In summary, we have identified separate degradation mechanisms associated with the three regions of the PHEMT: the source, the drain and the gate. In the next chapter we will present our overall conclusions and present suggestions for mitigating this degradation and for further research on these issues.

6 Conclusions and Suggestions

6.1 Conclusions

We have a developed a stress and measurement setup to study the electrical degradation of Pseudomorphic High-Electron Mobility Transistors (PHEMTs) and Transmission Line Model (TLM) structures. We have used this setup to perform a series of different experiments on RF power PHEMTs that enabled us to examine the various forms of degradation present.

In our electrical stressing experiments on the PHEMTs, we have observed three main forms of degradation: a permanent increase in the drain resistance, a permanent decrease in source resistance (which saturates in time), and a recoverable decrease in the threshold voltage. We found that impact ionization decreased with stressing, and that it played a much lesser role in drain resistance degradation than previously thought. The increase in R_D was more closely linked to the amount of bias stressing current and to air in the surrounding atmosphere. In contrast, the shift in the threshold voltage was found to be strongly correlated with impact ionization. The rate of decrease in source resistance was also dependent on the stressing current, yet it had a slight inverse relationship with impact ionization.

From our stressing experiments on the TLMs, we were able to identify some of the degradation mechanisms in these structures and then correlate them with analogous mechanisms affecting the PHEMTs. From comparing our overall findings to those in the literature, we were also able to put together physical explanations for different types of degradation occurring in the PHEMTs. Our key conclusions are that there are three independent sets of mechanisms affecting the three regions of the device: the source, the drain, and the gate. This is summarized in Figure 6-1.

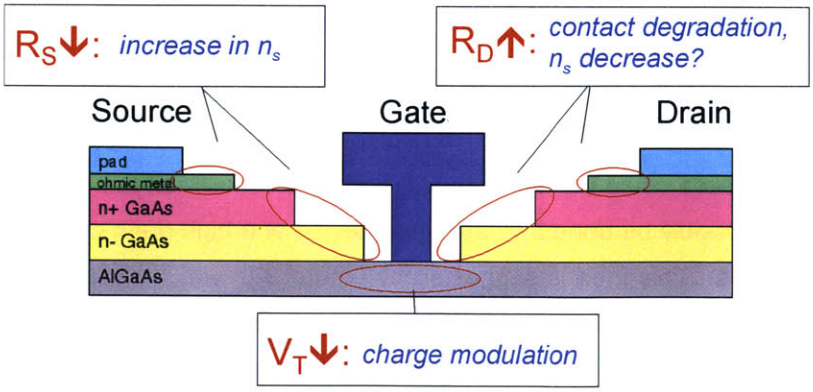

Figure 6-1: A schematic of the top layers of a GaAs PHEMT, illustrating the three main modes of degradation that have been identified in this research.

As shown the figure, the decrease in R_S can be explained by an increase in sheet carrier concentration on the source side of the device. This is likely due to surface effects. The increase in R_D can be attributed to (1) ohmic contact degradation as a result of hot electron degradation, and (2) a possible decrease in sheet carrier concentration on the drain side of the device (owing to an atmosphere-dependent surface reaction). The decrease in V_T can be explained by charge modulation under the gate—most likely, hot holes generated by impact ionization neutralizing trapped electrons in the AlGaAs layer.

6.2 Suggestions

Our research on the reliability of GaAs PHEMTs is still in progress, and there are many studies that should be continued. There are also many additional experiments that can be performed on these devices that will allow us to gain further knowledge concerning the degradation mechanisms. Nevertheless, at this point we can make a few general suggestions to improve the reliability of GaAs PHEMTs.

First of all, because the increase the drain resistance is of most concern in these devices, the primary focus of any possible device design improvements on the PHEMTs will be on mitigating this degradation. Since we have received indications of surface effects occurring in the drain-gate region, then it seems that a surface treatment that can somehow "fix" (i.e., render inert) the surface on the drain-gate region (and prevent chemical reactions from occurring) should alleviate this degradation. Also, since we found that elements in the air (possibly oxygen or moisture) accelerate the degradation of R_D, it is also imperative that the passivation layer on these devices be one that provides adequate protection against the environment (i.e. does not exhibit holes or cracks exposing the surface). To improve the device passivation, new alternative passivation techniques (such as the one described in [26]) can be used, which provides high-density nitride passivation that can offer better hermeticity and thus can improve reliability.

Since the change in threshold voltage is recoverable with unbiased storage at room-temperature, there is not too much concern in addressing this effect. Regarding R_S, a more thorough "burn-in" which exhausts this transient decrease could be implemented, such that R_S will remain stabilized upon further stressing. This can possibly be done by biasing the device at a high drain current for a short period of time (~ 2 minutes). This idea is suggested by Figure 3-8, which illustrates the change of R_D and R_S at a stressing current of I_D = 450 mA/mm. As one can see from this graph, the decrease in R_S happens almost entirely within the first ~10 minutes of stressing. However, it is important to note that within this period, R_D begins to increase. Thus, care must be taken that any source burn-in minimizes any degradation induced on the drain side of the device.

Although we have identified physical mechanisms behind PHEMT degradation, at this point there are a few issues observed in these devices that remain unexplored. One of these is the device burnout behavior (specifically, the decrease of $BV_{DG,off}$, and its dependence on the source-gate gap, Lrs). To examine this issue, the device's off-state breakdown characteristics can be measured at different temperatures, thus allowing us to observe the temperature dependence. This will allow us to determine if the mechanism inducing catastrophic burnout is an avalanche-related mechanism (which has negative temperature dependence).

Also, the behavior of I_{Dn1} with stressing remains a bit mystifying. Since I_{Dn1} gives an indication of the RF parameter I_{max}, it is of key importance in power applications, and thus it is important that its degradation is well understood. Although we can attribute the increase in I_{Dn1} to the V_T shift, and the eventual decrease in I_{Dn1} to the mechanisms behind R_D degradation, there are still some unresolved issues regarding its degradation behavior. Recall that I_{Dn1} was observed to degrade faster than I_{Dss} (Figure 3-9 and Figure 3-10, Figure 3-28), and that the "recovery" behavior of I_{Dn1} was quite puzzling (Figure 3-15). Additional degradation experiments that further examine the time evolution of I_{Dn1} and explain the mechanisms behind its behavior need to be performed.

Another phenomenon that needs further examination is the possible effect of self-heating. In order to see if this is a serious issue in our devices, results from stressing experiments on PHEMTs of varying gate finger widths can be compared (so far, we have tested W_g = 50 μm X 2 = 100 μm, we could also try W_g = 20 μm X 2 = 40 μm). If self-heating is a significant problem, then devices with narrower finger widths should exhibit less degradation (since those devices allow for better heat dissipation).

The specific physical mechanism behind the decrease in source resistance has not been clearly identified. Although surface effects are suspected, the fact that the decrease in R_S is slowed down by impact-ionization and that it is not dependent on the stressing environment demonstrate that its mechanism is quite different from the surface effects occurring on the drain side. Possible materials analysis methods (such as Auger XPS) that examine the device surface before and after stressing can shed some light onto this issue.

With regards to the TLM light emission experiments, it is speculated that the change in current distribution is related to the temperature profile across the width of the device (initially, current flows through the center portion of the device, and as the device heats up, degradation occurs and the current then tends to spread out to the cooler edges). However, the origin of non-uniformity in the current distribution remains puzzling. It is possible that it arises from non-

uniformities in the etching of the n+ GaAs in creating the wide recess. In order to explore this, materials analysis (such as AFM or Auger XPS) is needed to examine the surface of the n- GaAs in the TLMs, both before and after stressing.

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