Precision Hybrid Pipelined ADC

by

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Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy in Electrical Engineering and Computer Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

February 2014

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Abstract

Technology scaling poses challenges in designing analog circuits because of the decrease in intrinsic gain and reduced swing. An alternative to using high-gain amplifiers in the implementation of switched-capacitor circuits has been proposed that replaces the amplifier with a current source and a comparator. The technique has been generalized to zero-crossing based circuits (ZCBC). It has been demonstrated but not limited to single-ended and differential pipelined ADCs, with effective number of bits (ENOB) ranging from 8 bits to 11 bits at sampling rates from 10MS/s to 100MS/s.

The purpose of this project was to explore the use of the ZCBC technique for high-precision ADCs. The goal of the project is a 13-bit pipelined ADC operating at up to 100MS/s. A two-phase hybrid ZCBC operation is used to improve the power-linearity tradeoff of the A/D conversion. The first phase approximates the final output value, while the second phase allows the output to settle to its accurate value. Since the output is allowed to settle in the second phase, the currents through capacitors decay, permitting higher accuracy and power-supply rejection compared with standard ZCBCs. Linearization techniques for the ramp waveforms are implemented. Linear ramp waveforms require less correction in the second phase for given linearity, thus allowing faster operation. Techniques for improving linearity beyond using a cascoded current source are explored; these techniques include output pre-sampling and bidirectional output operation. Current steering is used to minimize the overall delay contributing to the first phase error, known as overshoot error. Overshoot error reduction at the end of the first phase improves the linearity requirements of the final phase. Automated background overshoot reduction is introduced though not included on the prototype ADC. A prototype ADC was designed in 1V, 65nm CMOS process to demonstrate the techniques introduced in this work. The prototype ADC did not meet the intended design goal and achieved 11-bit ENOB at 21MS/s and SFDR of 81dB. The main performance limitations are lack of overshoot reduction in the third pipeline stage in the prototype ADC and mid-range errors, introduced by the bidirectional ramp linearization technique, limiting the attainable output accuracy.

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Acknowledgments

I would like to thank my thesis supervisor Hae-Seung for his guidance and support through the doctoral dissertation process. I am grateful to Jim Roberge, Dave Perreault and Brian Brandt for serving on my committee and especially to Brian Brandt for his isight and feedback in the last year of work. I would not have had the learning experience and shared support and academic life through these years if not for my friends and lab-mates at MIT: Luke Theogarajan, Taylor Barton, Sungwon Chung, Matt Guyton, Sabino Pietrangleo, Johnna Powell, Sunghyuk Lee, Daniel Kumar, Eric Winokur, David He, Albert Chang.

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Chapter 1

Introduction

Modern battery-powered mobile communications devices and wearable devices are becoming increasingly more integrated and demand new power efficient circuit solutions. CMOS technology scaling has been driven by better performance and high power efficiency of digital circuits. Switched-capacitor circuits find a place at the interface between the digital and analog domain in front-end analog signal processing and digitizing system blocks. System component examples of switched-capacitor circuits include filters, pipelined analog-to-digital converters (ADCs), sigma-delta ADCs and digital-to-analog converters. Applications of switched-capacitor circuit blocks can be found in voiceband modems, baseband processing in wireless transceivers, radar and medical imaging devices to name a few.

Easy integration of switched-capacitor circuits in standard CMOS processes for digital circuits has made them widely used since the 1970s [7]. Their performance relies on matching of integrated capacitors in standard CMOS processes, which makes them robust to temperature and aging variations [7]. Switched-capacitor circuits can be used to realize building blocks such as a sample-and-hold (S/H), a gain stage, an integrator etc. Functions such as amplification, integration and subtraction are implemented in switched-capacitor circuits through input sampling and charge-transfer between capacitors. Precise charge-transfer relies on high-performance opamps con-

figured in negative feedback. The opamp requirements are large dc gain to reduce output gain error and unity-gain bandwidth much greater than the bandwidth of the input signal to allow for sufficient output settling.

The realization of high gain opamps in modern nanometer technologies is increasingly difficult [28, 32], especially if power consumption is constrained. Reduced device intrinsic gain with technology scaling limits the achievable gain per stage. Stability issues and the need for increased bandwidth and power become a concern when several gain stages are cascaded [13, 28]. As the feature transistor size is scaled in new processes, the supply voltage has to decrease to ensure reliable device operation. Cascoding is typically used for improved opamp gain, however, at low supply voltages, its use can severely limit the opamp output swing.

New techniques, that address the limitations on amplification and voltage swing, imposed by modern technologies on analog design and take advantage of technology scaling, have been developed. A gain enhancement technique, introduced as correlated level shifting (CLS) in [16], achieves over 60dB gain in $0.18\mu m$ CMOS process using a 30dB gain opamp and allows for rail-to-rail operation. The downside to using CLS is the need for two-phase operation, which ultimately limits the attainable speed and increased power dissipation as the level shifting capacitor loads the opamp during the coarse phase of operation. The combination of open-loop amplification with digital background calibration to trade-off precision in the analog domain with digital signal processing, is demonstrated in [32]. A resolution of 12 bits is attained at 75MS/s in a pipelined ADC with over 60% opamp power reduction in comparison to a conventional feedback opamp implementation. The penalty is continuous background calibration overhead in addition to upgradable memory space, which must track accurately any drift and variations during the conversion operation. There is an inherent trade-off between accuracy and the tracking time constants of the supporting algorithm [32]. Any non-linearity that is not in the gain stage element can limit the applied correction algorithm. In [19] a time-based power-efficient ring-amplifier, which approximates C-

class amplification operation is demonstrated in a 15-bit pipelined ADC at 20MS/s. This work also uses CLS and has the same constraints as [16]. The ring amplifier, though fast and power efficient, used during the coarse phase operation relies on an input offset to create an input-dead zone and condition the class C structure in its proper operating condition and is sensitive to variations during the conversion operation.

A power-efficient approach first introduced as comparator-based switched-capacitor circuits (CBSC) in [15] and then generalized into zero-crossing based circuits (ZCBC) in [4] address the challenges faced by high gain amplifier design in scaled technologies especially at high sampling rates. ZCBC replace the opamp in conventional switched-capacitor circuits with a current source and a zero-crossing detector (ZCD). The technique has been demonstrated but not limited to in single-ended and differential pipelined ADCs [15, 4, 5, 9, 26, 21], with effective number of bits (ENOB) ranging from 8 bits to 11 bits at sampling rates from 10MS/s to 100MS/s.

This work expands on previous architectures, addressing the challenges of ZCB switched-capacitor circuits for high precision applications especially at high sampling rates (up to 100MS/s). A two-phase approach to charge-transfer is used, first published in [21], which combines the strengths of ZCBC and negative-feedback opamp settling operation in addition to using CLS. Cascoding combined with rail-to-rail ZCBC operation is enabled through bidirectional ramp operation of the ZCBC current sources. The delay from the instant at which the virtual ground condition is satisfied in a ZCBC to the instant at which the output voltage is stored on the load capacitor results in an output error, called an overshoot error. Minimizing this delay reduces the overshoot error and improves the output linearity of the ZCB switched-capacitor circuit. A zero-crossing detector (ZCD) signals when the virtual ground condition is satisfied and the current sources are turned off. The ZCB phase output linearity is improved by using current steering to minimize ZCD delay and current source turn-off delay. A test chip for the design of 13-bit 100MS/s pipelined ADC

demonstrates the techniques introduced in this work. In addition, a background calibration technique is introduced though not included on the test chip.

1.1 Summary

Chapter 2 introduces ZCBC in the context of opamp based-switched capacitor circuits in pipelined ADCs. This chapter also provides a brief description of precision limitations in ZCBC, followed by an overview of several published architectures developed to improve precision in ZCBC.

Chapter 3 outlines circuits, which improve output linearity and enable cascoding and rail-to-rail output swing implementation of the ZCBC.

Chapter 4 presents the design and implementation details of a 13-bit 100MS/s pipelined ADC. The chapter starts with a brief description of the first pipeline stage top level design. The first pipeline stage is considered here because its design sets the attainable resolution of the ADC. Next specifics of the design parameters, constraints and implementation choices of the building blocks of the first pipeline stage are detailed.

Chapter 5 presents the pipelined ADC test chip results.

Chapter 6 summarizes the contribution of this thesis and outlines areas of further research.

Chapter 2

Zero-Crossing Based Circuits (ZCBC) Operation and Output Linearity

This chapter starts with a brief introduction to pipelined analog-to-digital converters (ADCs). Next, the multiplying digital-to-analog converter (MDAC) building block of a pipelined ADC stage is introduced in its conventional implementation, followed by a power efficient zero-crossing based (ZCB) implementation. To address non-linearities limiting the ZCB MDAC output precision, three two-phase ZCB topologies are presented. Trade-offs in terms of sampling rate, output linearity and power dissipation are considered for the different topologies.

2.1 Pipelined ADC Background

A pipelined ADC is a cascade of multiple, nearly identical in architecture, stages controlled by the same clock, working sequentially on the input signal to resolve a fraction of the output code. A conceptual block diagram of the n^{th} stage of a pipelined ADC is presented in Figure 2-1. The input voltage V_{IN} is sampled by a sample-and-hold circuit and digitized by an N-bit sub-ADC, U_1 in Figure 2-1. The sub-ADC digital output is then converted back to an analog signal through an N-bit digital-to-analog converter (DAC), U_2 in Figure 2-1. The DAC output is next subtracted from

the sampled input to produce an error voltage between the sampled input signal and its digitized copy. This voltage error is commonly referred to as a residue voltage. The residue is typically amplified (U_3) to the full scale of the input voltage (V_{IN}) (usually determined by the ADC reference voltage) and sampled by the following stage. The gain G of an n^{th} stage in a conventional implementation is $G = 2^{N_n}$. To reconstruct the output code, it is necessary to take into account the amplification between the sub-ADC stages in the pipeline. The digital output of each stage is multiplied by the aggregate gain of the following stages. The digital output of a pipelined ADC can be expressed as:

$$\begin{aligned} D_{out} &= (D_{out}(1)(2^{N_1}) + D_{out}(2))(2^{N_2}) + ... \\ &= \Sigma_{n=1}^{m} \left(D_{out}(n) \Pi_{k=n}^{m} 2^{N_k} \right) \end{aligned}$$

where m is the number of pipeline stages. One reason to choose the residue gain to be a power of 2 is to simplify the digital output reconstruction implementation. In the digital domain multiplication by 2 can be realized simply by bit shifting. The operating rate of a pipelined ADC is limited by the time it takes to make the sub-ADC and DAC conversions and residue amplification. The time it takes for the input signal to propagate through the cascade results in conversion latency which is acceptable in many applications.

The building blocks of an n^{th} stage of a pipelined ADC are: a sample-and-hold, a sub-ADC, a DAC, a subtraction circuit and a residue amplifier as illustrated in Figure2-1. The DAC, subtractor and residue amplification functions are commonly combined into a single switched-capacitor circuit referred to as a multiplying DAC (MDAC). The sub-ADC is typically implemented as, though not limited to, a flash ADC.

Each block of the pipelined ADC contributes errors which accumulate to limit the ADC resolution. Stage errors can be offsets (in the sub-ADC comparators, opamp

or charge injection), capacitor mismatch errors and insufficient residue amplification gain or settling errors. The errors can cause the pipeline stage output voltage to go out of range at the bit transition input values resulting in wide codes at the ADC digital output. Alternatively ADC stage error can scale the gain of the stage producing either wide codes or missing codes at the ADC digital output [28, 6]. The most widespread approach to alleviating the occurrence of wide codes is to use redundancy or over-range protection [30]. Redundancy holds if the gain of the residue amplifier is 2^{M_n} and $M_n < N_n$, which implies that the n^{th} stage output is not amplified to full scale at the bit transition points, allowing room for presence of errors. If redundancy is used, the offset design requirement on the sub-ADC comparators is relaxed, which allows their realization as dynamic latches. Typically the dynamic latch comparators implemented in flash converters are very power efficient and scale well with modern technologies [31]. Thus the sub-ADC represents a small fraction of the power dissipation of the pipelined ADC in contrast to the residue amplification, implemented by the MDAC, which takes up between 50% to 70% of the ADC power budget [39, 32]. Moreover, precise amplification in high resolution (14bits and higher) pipelined ADCs requires opamp gains on the order of $100dB$, which in older technologies could be achieved with a gain boosted two stage topology [32]. Attaining high opamp gain is increasingly difficult and power inefficient in modern nanometer technologies with diminishing device intrinsic gain and supply headroom. Thus there is a need for power-efficient MDAC circuit solutions, which can attain high output precision at high sampling rates.

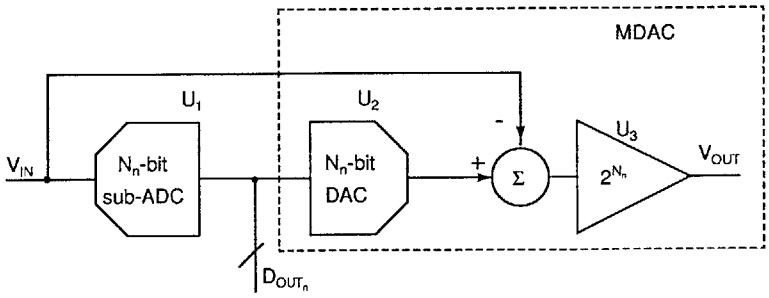
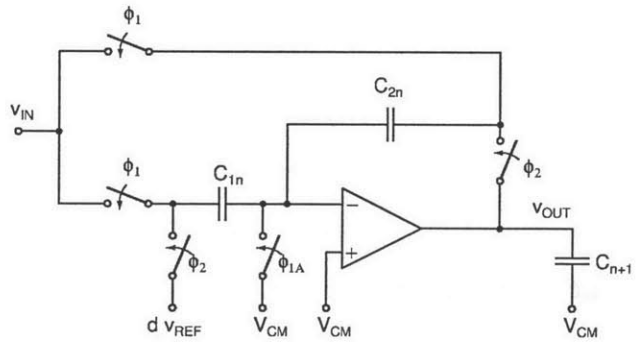


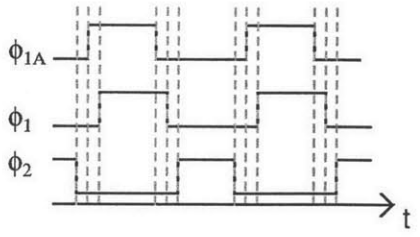
Figure 2-1: Block diagram of an n^{th} stage of a pipelined ADC

2.2 Conventional Switched-Capacitor Circuit Operation

Switched-capacitor circuits are discrete-time circuits. The input and consequently the output of discrete time circuits are valid at discrete (usually periodic) instants of time. In contrast, in continuous time circuits the input and output values of the circuit are valid at all times. Switched-capacitor circuit function is based on two phases of operation: a sampling phase and a charger-transfer or amplification phase. In addition to an input signal, they require a clock signal to control the flow of operation through two clock phases: ϕ_1 and ϕ_2 (illustrated in Figure 2-2b), corresponding to the sampling and charge-transfer phase respectively. The clock phases have to be non-overlapping to ensure no loss of charge during overlapping clock transitions. An example of a switched-capacitor circuit is a multiply-by-two topology (see Figure 2-2a), first introduced in [38] and commonly used to realize a multiplying digital-to-analog converter (MDAC) in a 1bit/stage or 1.5bit/stage pipelined ADC and as such will be used to illustrate the operation of the switched-capacitor circuits in this section. A single-ended implementation of the circuit is assumed for simplicity.



(a) Multiply-by-two switched-capacitor circuit used as MDAC in a pipelined ADC stage.



(b) Timing diagram for a multiply-by-two switched capacitor circuit.

Figure 2-2: Multiply-by-two switched-capacitor circuit used as MDAC in a pipelined ADC stage. It operates on two clock phases ϕ_1 and ϕ_2. Clock phase ϕ_1 controls the input sampling of v_{IN}, while clock phase ϕ_2 controls the charge-transfer phase of operation. At the start of ϕ_2, the bottom plate of C_{1n} is connected to the reference voltage of the pipeline ADC, V_{REF}. The output signal v_{OUT} is valid at the end of ϕ_2.

First the sampling phase is considered. Capacitors C_{1n} and C_{2n} are the input sampling capacitors of an n^{th} stage multiply-by-two circuit of a 1.5bit/stage pipelined

ADC, while capacitor C_{n+1} represents the input sampling capacitor of the subsequent pipelined ADC stage. During the sampling phase (ϕ_1), C_{1n} and C_{2n} are configured as shown in Figure 2-3. By the end of ϕ_1, the input signal v_{IN} is sampled on C_{1n} and C_{2n}. Bottom-plate sampling is commonly used to sample the input signal to minimize input-dependent charge injection. The bottom-plate switch (sw_3) is turned off first by ϕ_{1A} slightly before ϕ_1 transitions and charge $q = (C_{1n} + C_{2n})v_{IN}$ is fixed. The turn-off of $sw3$ defines the sampling instant. On turn off, sw_3 injects charge q_3 into the equivalent input capacitor $C_{eq} = C_{1n} + C_{2n}$, producing a voltage error $v_{sw3} = \frac{q_3}{C_{eq}}$ but both q_3 and therefore v_{sw3} are relatively independent of the input voltage. Suppose sw_3 is implemented as an NMOS switch, with a fast turn-off clock slope, then the channel charge contribution $q_3 \cong \frac{WLC_{ox}(V_{DD}-V_{THN}-V_{CM})}{2}$ injected on C_{eq} is relatively constant independent of input voltage, where V_{DD} corresponds to the high voltage of the clock signal driving $sw3$, C_{ox} and V_{THN} are the oxide capacitance and the threshold voltage of the NMOS device, and V_{CM} is the common mode voltage in the circuit. The clock feed-through voltage error $\mid V_{DD}(\frac{WC_{ov}}{WC_{ov}+C_{eq}}) \mid$ of $sw3$ at C_{eq} is independent of the input voltage and depends on V_{DD} and overlap capacitance C_{ov} of $sw3$. Next sw_1 and sw_2 are turned off on the high to low transition of ϕ_1 and since the bottom plates of C_{1n} and C_{2n} are disconnected already no charge is injected on C_{eq}. In a differential switched-capacitor architecture the constant charge injected by $sw3$ appears as common mode and can thus be suppressed at the output.

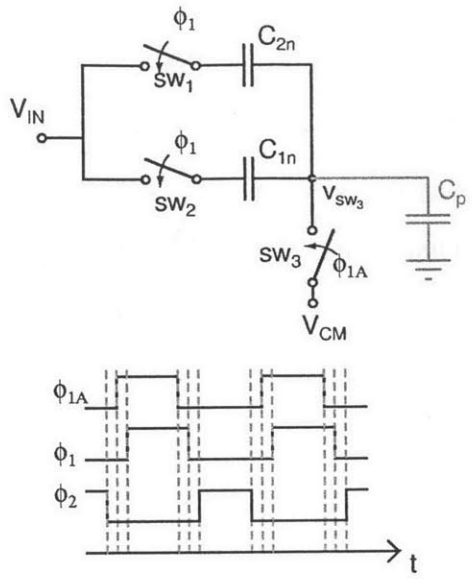
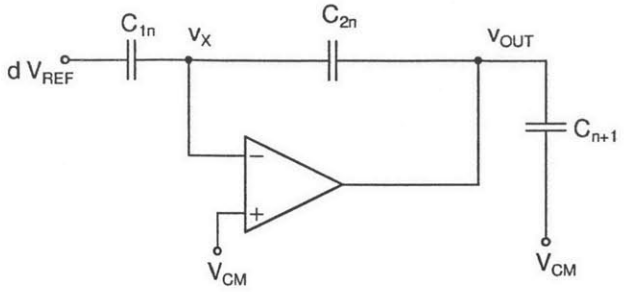


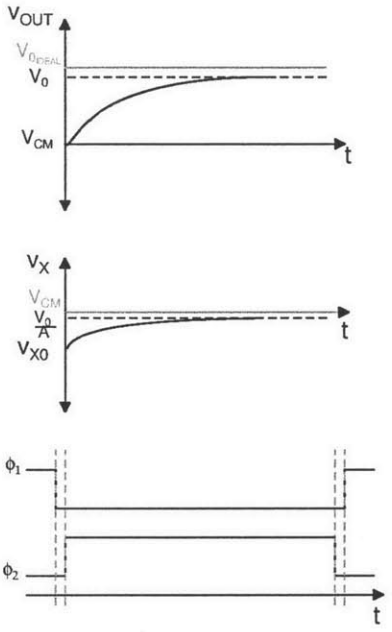
Figure 2-3: Input sampling phase of a multiply-by-two switched-capacitor circuit. Capacitor C_p in gray indicates the parasitic capacitance at node v_{sw3}. Phase notation: ϕ_1 enables the sampling phase, ϕ_2 enables the charge-transfer phase. Switch sw_3 is turned off first by ϕ_{1A}. Next sw_1 and sw_2 are turned off by ϕ_1.

The charge-transfer phase relies on the operation of an opamp, configured in negative feedback through C_{2n} to move the charge on C_{1n} to C_{2n} and exponentially settle the output voltage by the output sampling instant. More specifically, at the start of ϕ_2 (see Figure 2-4a), the top plate of C_{1n} is connected to $d\,V_{REF}$ in a 1.5bit pipelined ADC stage, where d can take on values $[1, 0, -1]$ determined by the output of the sub-ADC of the pipeline stage and V_{REF} is the reference voltage of the ADC. The voltage at the virtual ground node v_X steps instantaneously, disturbing the virtual ground node. In addition at the start of ϕ_2, the top plate of C_{2n} is connected to the output of the opamp v_{OUT}. During ϕ_2, if the opamp has infinite gain, it settles the output voltage v_{OUT} exponentially to its ideal final value v_{O_f} as the voltage at v_X exponentially approaches V_{CM} as shown in Figure 2-4b. If the opamp has finite gain A, and sufficient bandwidth to settle the output voltage to the required accuracy of the ADC stage, the output voltage v_{OUT} settles to its final value v_{OUT_f}, while the opamp input node v_X settles to $V_{CM} - \frac{v_{OUT_f}}{A}$, resulting in output-dependent deviation from the ideal output voltages v_O and V_{CM} at both nodes respectively (see Figure

2-4b). Insufficient gain of the opamp results in a gain error at the output v_{OUT}, which if larger than the accuracy requirement of the pipelined ADC stage, translates into static non-linearity in the ADC digital output [6].



(a) Charge-transfer phase configuration of a conventional multiply-by-two switched-capacitor circuit



(b) Voltage waveforms at the output node v_{OUT} and opamp input node v_X and timing diagram for the charge-transfer phase of a multiply-by-two switched-capacitor circuit. The values in gray indicate the ideal node voltages at the end of ϕ_2, for an opamp of infinite gain. The dashed lines indicate the node voltages at v_{OUT} and v_{IN} for an opamp of finite gain A.

Figure 2-4: Charge-transfer phase operation of a multiply-by-two switched capacitor circuit as used in a pipelined ADC stage

Charge conservation is used to derive the transfer function of the multiply-by-two switched-capacitor circuit of Figure 2-2. If an ideal opamp of infinite gain is assumed,

the following relationship between v_{OUT} and v_{IN} is derived in Appendix A:

$$v_{OUT} = (\frac{C_{1n} + C_{2n}}{C_{2n}})v_{IN} - \frac{C_{1n}}{C_{2n}}dV_{REF}. \tag{2.1}$$

If an opamp of finite gain A is assumed, the voltage at the feedback node is $v_X = V_{CM} - \frac{v_{OUT}}{A}$. The transfer function of the multiply-by-two switched-capacitor circuit for finite opamp gain is also derived in Appendix A as:

$$v_{OUT} = \frac{(\frac{C_{1n}+C_{2n}}{C_{2n}})v_{IN} - \frac{C_{1n}}{C_{2n}}dV_{REF}}{1 + \frac{1}{A\beta}}, \tag{2.2}$$

where β is the feedback factor of the circuit, $\beta = \frac{C_{2n}}{C_{1n}+C_{2n}}$. Finite opamp gain causes gain reduction in the multiply-by-two transfer function, which produces missing codes at the bit decision boundary of the pipelined ADC stage, the number of which is inversely proportional to the opamp gain. The missing codes translate into a static nonlinearity in the pipelined ADC transfer function and limit the attainable ADC resolution[28, 6]. The opamp has to be designed with sufficient gain to satisfy the desired ADC resolution. The gain error referred to the input of the first pipeline stage for an ADC of full scale input V_{FS} and N-bit of resolution has to be $< \frac{1}{2}V_{LSB}$ to ensure no missing codes at the ADC output:

$$\frac{V_{FS}}{2^{N+1}} > \frac{1}{A\beta G},$$

$$A > \frac{2^{N+1}}{\beta G V_{FS}}.$$

As $\beta = \frac{1}{G}$ the opamp gain requirement can be expressed as:

$$A > 2^{N+1}.$$

Thus for a 13-bit ADC, the opamp gain has to be $A > 84dB$. In the presence of opamp input-referred constant offset voltage V_{OS}, the multiply-by-two circuit transfer function can be expressed as:

$$v_{OUT} = \frac{(\frac{C_{1n}+C_{2n}}{C_{2n}})(v_{IN} - V_{OS}) - \frac{C_{1n}}{C_{2n}} dV_{REF}}{1 + \frac{1}{A\beta}}.$$

Circuit techniques, such as auto-zeroing and chopping [12] address constant offset for improved output precision. Research efforts for gain error correction in opamp based switched-capacitor circuits through digital background calibration has been developed and have been used to reduce errors due to low gain [18], open loop amplification [32] and incomplete settling [22]. The proposed techniques rely on continuous background calibration tracking variations during the conversion process and there is a trade-off between the attainable accuracy and the tracking time necessary to complete the algorithm. Open loop amplification relies on a linear sub-DAC operation, while non-linearity apart form the open loop amplifier are present. Furthermore a model for the region of operation of the differential amplifier devices is assumed used in the linearization algorithm. Incomplete settling relies on a first order response of the amplifier with both its input and output starting from from a voltage independent of previous samples and is also code-independent with every conversion step [22].

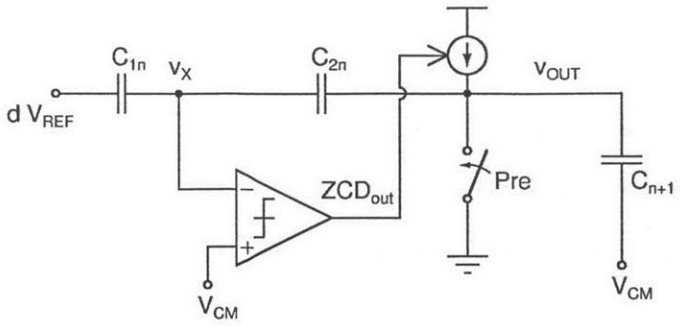
2.3 ZCBC Overview

2.3.1 Single Phase ZCBC

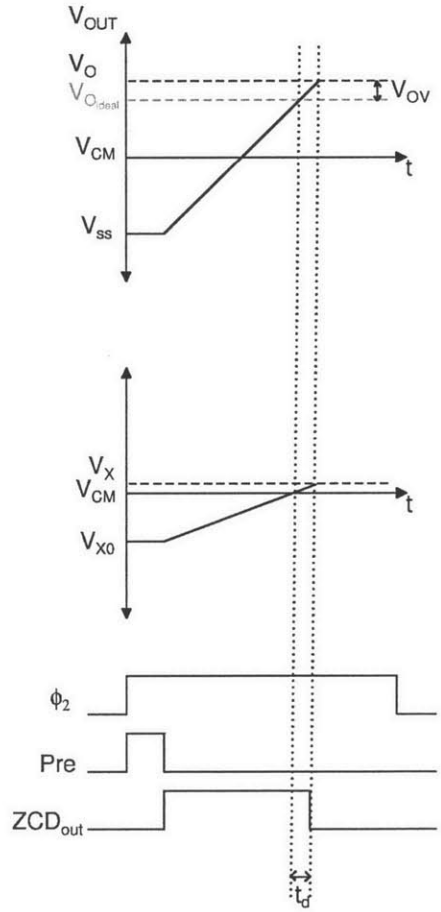
Zero-crossing based switched-capacitor circuits (ZCBC), [15, 4, 5, 26, 9] take advantage of the discrete nature of sampled systems to implement the charge-transfer function in a power efficient way at higher speeds and over a wide range of output accuracies[23].

Both opamp and ZCB switched-capacitor circuits share an identical sampling phase ϕ_1 but differ in the way the charge-transfer phase is performed. In a ZCB switched-

capacitor circuit implementation, the function of the opamp in transferring charge from C_{1n} to C_{2n}, is replaced by a current source charging C_{1n}, C_{2n} and C_{n+1}, and a Zero-Crossing Detector (ZCD) (see Figure 2-5a). At the start of ϕ_2, a preset phase (Pre) resets the output node to a preset voltage (in the case of Figure 2-5a it is ground). In addition, the preset phase ensures that the feedback node v_X starts in this particular case below the virtual ground condition, assuming a PMOS current sources is used to charge up the load capacitors. The timing diagram and output waveforms for the ZCBC charge-transfer operation are shown in Figure 2-5b. The output voltage v_{OUT} ramps towards its ideal final value v_{O_f}, while the feedback node v_X ramps towards V_{CM}. The ZCD detects when the charge from C_{1n} has been transferred to C_{2n}, which occurs at the instant when the voltage at the feedback node V_X crosses V_{CM}. In contrast, the opamp in the conventional switched-capacitor circuit, through negative feedback, forces the virtual ground condition to be $v_X = V_{CM}$.



(a) Charge-transfer ZCB switched-capacitor circuit diagram used as MDAC in a pipeline ADC stage



(b) ZCBC waveforms at the output node v_{OUT} and negative feedback node v_X and timing diagram

Figure 2-5: Conceptual diagram of charge-transfer operation in a ZCB switched-capacitor circuit: a current source and a zero-crossing detector (ZCD) replace the function of an opamp in conventional switched-capacitor circuits. Finite ZCD delay t_d results in an output overshoot error v_{OV} from the ideal output voltage v_O.

For an infinitely fast ZCD and ideal current source of infinite output resistance, the final output voltage V_{OUT} of an MDAC multiply-by-two circuit ZCB implementation is equivalent to the output voltage of an ideal opamp implementation and can be described by Eq. 2.1. A non-ideal ZCD however, has finite delay which results in an overshoot error (v_{OV}) in the output voltage as shown in Figure 2-5b. Next the ZCBC output error is considered starting with ideal components and introducing non-linearities one at a time.

2.3.1.1 Output Voltage Error

Ideally the current source has an infinite output resistance and current value I_{ideal} and the ZCD has an infinitely fast response or a ZCD delay, $t_d = 0$. The output voltage is sampled at the exact instant that the virtual ground condition is satisfied (the voltage at node v_X crosses V_{CM}) such as the transfer function of the circuit is described by Eq. 2.1. The overshoot voltage ($v_{OV} = 0$) in this case is zero. The ideal output voltage (v_O) can be expressed as:

$$v_O(t_0) = \frac{I_{IDEAL}}{C} t_0, \tag{2.3}$$

where t_0 is the zero-crossing instant. If the current source is still assumed ideal (i.e. has infinite output resistance) but the ZCD output response has a finite delay t_d, then the output voltage can be expressed as:

$$\begin{aligned} v_{OUT}(t_0 + t_d) &= \frac{I_{IDEAL}}{C} t_0 + \frac{I_{IDEAL}}{C} t_d \\ &= v_O(t_0) + \frac{I_{IDEAL}}{C} t_d, \end{aligned}$$

where $v_{OV} = \frac{I_{IDEAL}}{C} t_d$ is the overshoot voltage error due to the finite ZCD delay t_d. Note that for a constant ZCD delay t_d, the output overshoot error appears as a constant output error for all output voltages similar to the the input-referred offset

error (V_{OS}) in an opamp based switched-capacitor circuit.

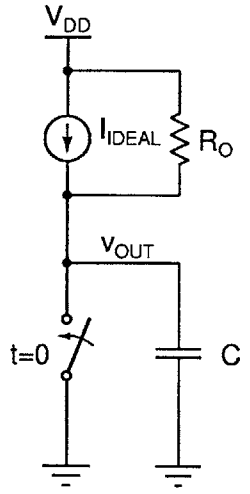


Figure 2-6: Simplified diagram of ZCB circuit ramp current source operation. Current source is modeled as an ideal current source with finite output resistance R_O and capacitor C represents the ZCB circuit load capacitor. $sw1$ is assumed to open at time $t = 0$.

If the current source is no longer assumed ideal, to first order the current source can be modeled as an ideal current source of value I_{IDEAL} in parallel with a finite output resistance, R_O (refer to Figure 2-6). In practice, the current source output resistance is a function of the current, which in turn depends on the output voltage v_{OUT}. Therefore the proposed model is a rough approximation of the current source operation. Applying KCL at node v_{OUT} yields:

$$\begin{aligned} i_C &= I_{IDEAL} + i_{R_O} \\ &= I_{IDEAL} + \frac{V_{DD} - v_{OUT}(t)}{R_O} \end{aligned} \tag{2.4}$$

At a specific output value $v_0 = v_{OUT}(t_0)$, during the ZCD delay (t_d), the voltage change at the ZCBC output v_{OUT} can be assumed to be small relative to the ZCBC full-scale output voltage V_{FS}. To begin with, to first order the output voltage dependence of the current around $v_{OUT} = v_0$, can be neglected. Thus, assuming a constant current around the operating point $v_{OUT} = v_0$ and applying KCL, the current through

the capacitor $i_C(t)$ can be expressed as a function of v_0 as follows:

$$i_C(t) \mid_{v_O} = I_{IDEAL} + \frac{V_{DD} - v_0}{R_O}.$$

The voltage change from time $t_0 = 0$ (the zero-crossing instant) to time $t_f = t_d$ at the ZCBC output v_{OUT} can be expressed as a function of the output voltage value v_0 as follows:

$$\begin{aligned} v_{OV}(t_d) \mid_{v_0} &= \frac{1}{C}\int_0^{t_d}(I_{IDEAL} + \frac{V_{DD} - v_0}{R_O})dt \\ &= \frac{I_{IDEAL}}{C}t_d + \frac{V_{DD}}{CR_O}t_d - \frac{v_0}{CR_O}t_d \\ &= \frac{(I_{IDEAL} + \frac{V_{DD}}{R_O})}{C}t_d - \frac{v_0}{CR_O}t_d. \end{aligned} \tag{2.5}$$

Let $I_{IDEAL} + \frac{V_{DD}}{R_O} = I_0$, then

$$v_{ov}(t_d) \mid_{v_0} = \frac{I_0}{C}t_d - \frac{v_0}{CR_O}t_d \tag{2.6}$$

If the ZCD delay t_d is assumed to be constant with the output voltage v_0, then the first component of Eq. 2.6 is independent of the output voltage v_0, while the second component is output-dependent.

In the analysis above the current, at a fixed output voltage value v_0, is assumed constant as the output voltage changes from instant t_0 when the virtual ground condition is satisfied to t_f when the ZCD output transitions. Next the case of output current dependence on v_{OUT} is included. Remembering the voltage and current relationship for a capacitor $i_C(t) = C\frac{dv_{OUT}(t)}{dt}$ and substituting in Eq. 2.4, the output voltage v_{OUT} as a function of time can be found from the following first order differential equation :

$$C\frac{dv_{OUT}(t)}{dt} = I_{IDEAL} + \frac{V_{DD} - v_{OUT}(t)}{R_O}. \tag{2.7}$$

The solution to Eq. 2.7 is of the form $v_{OUT}(t) = Ke^{st} + P$, where $s = -\frac{1}{R_O C}$ can be found from the homogeneous solution to Eq. 2.7, while $P = I_{IDEAL}R_O + V_{DD}$ and $K = -P$ are found form the particular solution of Eq. 2.7 and the initial condition $v_{OUT}(t = 0^+) = 0$ respectively, when $sw1$ in Figure 2-6 closes. The instant of $sw1$ closing corresponds to the falling edge of the preset signal Pre in Figure 2-5b. It follows that $v_{OUT}(t)$ can be expressed as:

$$v_{OUT}(t) = (I_{IDEAL}R_O + V_{DD})(1 - e^{-\frac{t}{R_O C}}). \tag{2.8}$$

Since the output voltage $v_{OUT}(t)$ of interest for the current source operation is for $t \ll R_O C$, Eq. 2.8 can be approximated by using a Taylor series expansion of the term $e^{-\frac{t}{R_O C}}$: $e^{-\frac{t}{R_O C}} = 1 - \frac{t}{R_O C} + \frac{t^2}{2!(R_O C)^2} + \ldots$. Then $v_{OUT}(t)$ can be approximated including only the first three terms as:

$$\begin{aligned} v_{OUT}(t) &= (I_{IDEAL}R_O + V_{DD})(1 - (1 - \frac{t}{R_O C} + \frac{t^2}{2(R_O C)^2}) \\ &= (I_{IDEAL}R_O + V_{DD})(\frac{t}{R_O C} - \frac{t^2}{2(R_O C)^2}) \\ &= (I_{IDEAL} + \frac{V_{DD}}{R_O})(\frac{t}{C} - \frac{t^2}{2R_O C^2}) \\ &= \frac{I_0}{C}t - \frac{I_0}{2R_O C^2}t^2 \end{aligned} \tag{2.9}$$

If $v_O(t) = \frac{I_0}{C}t$ is the error-free output voltage in this case, then:

$$v_{OUT}(t) = v_O(t) - \frac{I_0}{2R_OC^2}t^2 \tag{2.10}$$

$$= v_O(t) - \frac{(v_O(t))^2}{2I_0R_O} \tag{2.11}$$

$$= v_O(t)(1 - \frac{(v_O(t))^2}{2I_0R_O}) \tag{2.12}$$

The second term in Eq. 2.10 represents the output error due to the finite current source output resistance and it is the error at the output for an infinitely fast ZCD. Differentiating Eq. 4 yields the current $i_C(t)$ through capacitor C as a function of time assuming the approximation made above $t \ll R_OC$:

$$i_C(t) = C\frac{dv_{OUT}(t)}{dt}$$

$$= I_0(1 - \frac{t}{R_OC}). \tag{2.13}$$

Until this point a finite current source output resistance was considered in the analysis leading to Eq. 2.9, assuming an infinitely fast ZCD. For a finite ZCD delay t_d the output voltage can be expressed as:

$$v_{OUT}(t_0 + t_d) = \frac{I_0}{C}(t_0 + t_d) - \frac{I_0(t_0 + t_d)^2}{2R_OC^2}$$

$$= \frac{I_0}{C}t_0 + \frac{I_0}{C}t_d - \frac{I_0t_0^2}{2R_OC^2} - \frac{I_0t_0t_d}{CR_OC^2} - \frac{I_0t_d^2}{2R_OC^2}$$

$$= v_O(t_0) + \frac{I_0}{C}t_d - \frac{I_0t_0^2}{2R_OC^2} - \frac{I_0t_0t_d}{R_OC^2} - \frac{I_0t_d^2}{2R_OC^2}$$

where t_0 is the zero-crossing instant. The output error (ε_{OUT}) can be expressed as a function of the error free output voltage $v_O(t_0) = \frac{I_0t_0}{C}$ as:

$$\varepsilon_{OUT}(v_O(t_0), t_d) = v_{OUT}(t_0 + t_d) - v_O(t_0)$$
$$= \frac{I_0}{C} t_d - \frac{v_O(t_0) t_d}{R_O C} - \frac{(v_O(t_0))^2}{2 R_O I_0} - \frac{I_0 t_d^2}{2 R_O C^2}. \quad (2.14)$$

The first error term in Eq. 2.14 contributes to the overshoot error (v_{OV}) and is due to the ideal current source in the current source model and finite ZCD delay t_d. The second term describes the first order dependence of the overshoot error (v_{OV}) on output voltage due to both the finite resistance R_O of the current source and the finite ZCD delay t_d, under the assumption that the ramp current does not vary by much during t_d. The third term represents a deviation from the ideal output voltage ($v_O(t_0)$) due to the finite current source output resistance R_O and is present even if the ZCD has zero delay as seen in Eq. 2.10. The last term of Eq. 2.14 represents the output voltage error due to the output current dependence on the variation of output voltage during the delay t_d of the ZCD. Note that if the second order terms of Eq. 2.14, are neglected, it reduces to Eq. 2.6. For a constant finite ZCD delay, both the first and last term of Eq. 2.14 are constant for all output voltages, which means that they do not contribute gain error or non-linearity at the output and can be corrected by using offset correcting techniques similar to the ones used in conventional opamp based switched-capacitor circuits. On the other hand, the second and third term are output-dependent errors and contribute to non-linearity at the ZCB switched-capacitor circuit output and will be the focus of the following discussion:

$$v_{OV}(v_O(t_0), t_d) = \frac{I_0}{C} t_d - \frac{v_O(t_0) t_d}{R_O C}. \quad (2.15)$$

The squared term $-\frac{I_0 t_d^2}{2 R_O C^2}$ is only delay dependent and is a lot smaller than the first term $\mid t_d \frac{I_0}{C} \left(\frac{t_d}{2 R_O C} \right) \mid \ll t_d \frac{I_0}{C}$, as $t_d \ll R_O C$ and thus will be neglected. The remaining square term is $\frac{(v_O(t_0))^2}{2 R_O I_0} = \frac{(v_O(t_0))^2}{2 V_A}$, where V_A is the Early voltage of the current source does not contribute an error as it is not delay dependent and the feedback network in

the case of zero delay will cause the zero-crossing to occur at the ideal output voltage value so this term will be neglected.

It has been shown that the output-dependent component of the overshoot error (v_{OV}) is similar to the error due to opamp finite gain in an opamp implementation [36, 6, 17]. The output resistance dependence of the current source on the constant current I_0 can be expressed through the concept of Early voltage V_A as:

$$R_O = \frac{V_A}{I_0}. \tag{2.16}$$

If only the output-dependent component of the overshoot error is considered, the ZCBC output voltage can be derived by adding the output-dependent overshoot error $v_{ov} = -\frac{v_O(t)t_d}{R_O C}$ to the ideal output voltage expressed in Eq. 2.1 to yield:

$$v_{OUT} = \frac{(\frac{C_{1n}+C_{2n}}{C_{2n}})v_{IN} - \frac{C_{1n}}{C_{2n}}dV_{REF}}{1 + \frac{t_d I_0}{V_A C}} \tag{2.17}$$

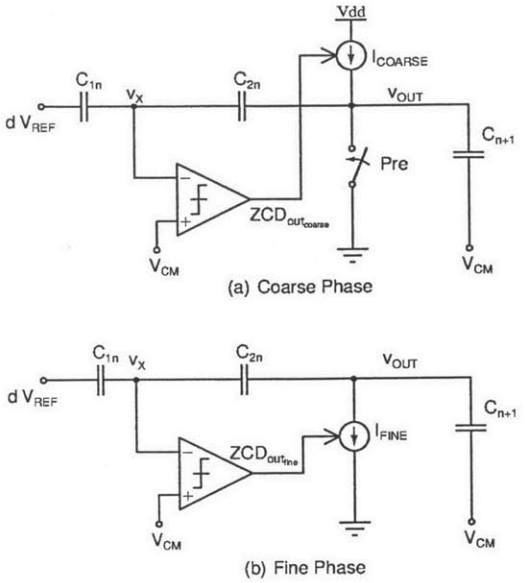
Note that Eq. 2.17 has the same form as Eq. 2.2. Thus, ZCBC output linearity to first order is limited by the output-dependent overshoot error, which has a similar effect as finite opamp gain on output linearity in a conventional opamp based switched-capacitor circuit.

2.3.2 Dual Ramp ZCBC

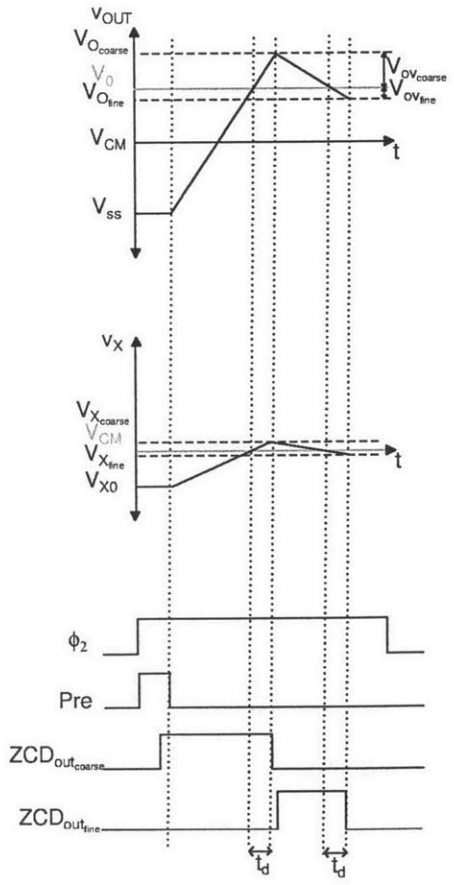
To improve ZCBC output linearity, a dual ramp ZCB switched-capacitor circuit is introduced in [15]. The goal of dual ramp ZCBC is to reduce the ramp current at the zero-crossing instant instant, thus reducing the output overshoot error and output non-lineraity. The concept behind the dual ramp technique is based on a two-phase charge-transfer operation. A fast, coarse ramp is generated to approximate the output voltage during the first phase, followed by a slower fine phase. The fine phase corrects the overshoot error of the coarse phase (Figure 2-7) to arrive at a more accurate estimate of the output value than a single phase ZCBC implementation. The

ideal fine phase current $I_{0_{fine}}$ is only a fraction of the ideal coarse phase current $I_{0_{coarse}}$ and typically of opposite sign of $I_{0coarse}$. At the end of the coarse phase when the ZCD makes its decision, $I_{0_{fine}}$ is turned off and the output voltage estimate is held on the load capacitors C_{1n}, C_{2n} and C_{n+1}. The fine phase current source is then turned on and the output ramps down (Figure 2-7a) to a more accurate approximation of the ideal value v_O as shown in Figure 2-7b. The ZCD output transitions as the voltage at v_X crosses V_{CM} again, which defines the output sampling instant.

As the current $I_{0_{fine}}$ is much smaller than $I_{0_{coarse}}$, the current at the second zero-crossing transition is reduced, resulting in a smaller overshoot error. As demonstrated by Eq. 2.14, the coarse phase output overshoot voltage $v_{OV_{coarse}}$ to first order consists of an output-dependent component and another component invariant with output voltage. The invariant part of $V_{OV_{coarse}}$ if input-referred, can be thought of as an offset voltage in an opmap based circuit and various techniques exist to correct for it at the end of the coarse phase. If constant overshoot correction is used, the fine phase then has to only correct the output-dependent part of the coarse phase overshoot error $v_{ov_{coasre}}$.



(a) Simplified diagram of dual ramp ZCB switched-capacitor circuit used as MDAC in a pipelined ADC stage. It is based on two phases of operation: coarse phase (a) and fine (b) phase



(b) Voltage waveforms at the ZCB circuit output node v_{OUT} and virtual ground node v_X and timing diagram for ϕ_2

Figure 2-7: Simplified dual ramp ZCB switched-capacitor charge-transfer operation based on phases: coarse and fine phase. The ZCD detects the virtual ground condition at the end of each phase.

In the discussion to follow the focus will be on the output-dependent overshoot error at the end of the coarse phase ($v_{ov_{coarse}}$) and at the end of the fine phase ($v_{ov_{fine}}$). In Appendix B, the fine phase overshoot error $v_{OV_{fine}}$ is derived in detail as a function of the ideal output voltage $v_O(t)$ and ZCD delay t_d (assumed to be the same for both phases of charge-transfer operation):

$$v_{OV_{fine}}(v_O(t), t_d) = -\frac{I_{0_{fine}} t_d}{C} - \frac{v_O(t) t_d}{C R_{O_{fine}}} \left(1 - \frac{t_d}{R_{O_{coarse}} C}\right) - \frac{I_{0_{coasre}} t_d^2}{2C^2 R_{O_{fine}}} \left(1 - \frac{t_d}{R_{O_{coarse}} C}\right).$$

The output-dependent overshoot error component $v_{ov_{fine}}$ is then (making the assumption that $R_{O_{coarse}}$ does not vary significantly with the ZCB circuit output voltage v_{OUT}) :

$$v_{ov_{fine}}(v_O(t), t_d) = -\frac{v_O(t) t_d}{C R_{O_{fine}}} \left(1 - \frac{t_d}{R_{O_{coarse}} C}\right).$$

The transfer function for the dual ramp ZCB multiply-by-two switched-capacitor circuit can then be derived by adding the fine phase output-dependent error component $v_{ov_{fine}}(v_O(t))$ to the ideal output transfer function derived in Eq. 2.1:

$$v_{OUT} = \frac{(\frac{C_{1n}+C_{2n}}{C_{2n}}) v_{IN} - \frac{C_{1n}}{C_{2n}} dV_{REF}}{1 + \frac{t_d}{R_{O_{fine}} C} \left(1 - \frac{t_d}{R_{O_{coarse}} C}\right)}.$$

If the Early voltages of both current sources are assumed approximately the same, the transfer function can be re-written as:

$$v_{OUT} = \frac{(\frac{C_{1n}+C_{2n}}{C_{2n}}) v_{IN} - \frac{C_{1n}}{C_{2n}} dV_{REF}}{1 + \frac{t_d I_{0_{fine}}}{V_A C} - \frac{t_d^2 I_{0_{coarse}} I_{0_{fine}}}{V_A^2 C^2}}.$$

As $I_{0_{fine}}$ decreases during the fine phase, $v_{ov_{fine}}$, which is proportional to first order to $I_{0_{fine}}$, is proportionately decreased and the ZCB circuit output linearity improves as well. If the fine phase current $I_{0_{fine}}$ is smaller than the ramp current ($I_{0_{single}}$) in a single phase ZCB multiply-by-two switched-capacitor circuit, the equivalent gain

error in the output voltage is reduced in comparison.

Suppose $\frac{I_{0_{fine}}}{I_{0_{coarse}}} = \frac{1}{H}$, the ZCB circuit full-scale output voltage is $V_{OUT_{FS}}$ and the ZCD delay t_d is the same in both phases of charge-transfer. The coarse phase output-dependent overshoot error ($v_{ov_{coarse}}$) from Eq. 2.14 expressed as:

$$v_{ov_{coarse}}(v_O(t)) = -\frac{v_O(t)t_d}{R_{O_{coarse}}C}. \tag{2.18}$$

Assuming for simplicity and for comparison purposes that $t_d \ll R_{O_{coarse}}C$, $v_{ov_{fine}}$ can be reduced to:

$$v_{ov_{fine}}(v_O(t)) = -t_d\frac{v_O(t)}{R_{O_{fine}}C} = -t_d\frac{v_O(t)I_{0_{fine}}}{V_AC}. \tag{2.19}$$

For simplicity suppose also that the Early voltage V_A of the fine and coarse phase current source devices is the same. Then from Eq. 2.18, Eq. 2.19 and Eq. 2.16 it follows that the output-dependent overshoot error at the end of the fine phase $v_{ov_{fine}}$ is reduced by the ratio H of the coarse ($I_{0_{coarse}}$) to fine ($I_{0_{fine}}$) currents:

$$\begin{aligned}\frac{v_{ov_{coarseMAX}}}{v_{ov_{fineMAX}}} &= \frac{\frac{-t_dV_{OUT_{FS}}}{C(\frac{V_A}{I_{0coarse}})}}{-\frac{2t_dV_{OUT_{FS}}}{C(\frac{V_A}{I_{0fine}})}} \\ &= \frac{I_{0_{coarse}}}{I_{0_{fine}}} \\ &= H.\end{aligned} \tag{2.20}$$

To get a better idea of the trade-offs in terms of output linearity and power dissipation due to the current sources, between single and dual ramp ZCBC implementations for fixed sampling speed, suppose both switched-capacitor circuits operate at the same sampling speed so that $t_{single} = t_{coarse} + t_{fine} = \frac{T_s}{2}$, where T_s is the sampling period, t_{single} is the maximum duration of the single phase charge-transfer and t_{coarse} is the maximum coarse phase duration. Assuming ideal ZCB circuit operation, if the single and dual ramp currents are $I_{0_{single}}$, $I_{0_{coarse}}$ and $I_{0_{fine}}$, respectively, and $v_{ovcoarse_{MAX}}$ and

$v_{ovfine_{MAX}}$ are the maximum coarse phase and fine phase output-dependent overshoot errors respectively, it follows that:

$$\frac{V_{OUT_{FS}}}{\frac{I_{0_{single}}}{C}} = \frac{V_{OUT_{FS}}}{\frac{I_{0_{coarse}}}{C}} + \frac{\mid v_{ovcoarse_{MAX}} \mid}{\frac{I_{0_{fine}}}{C}}. \tag{2.21}$$

Substituting E. 2.20 into Eq 2.21, the relationship between I_{coarse} and I_{single} can be expressed as:

$$\frac{1}{I_{0_{single}}} = \frac{1}{I_{0_{coarse}}} + \frac{\frac{|v_{ovcoarse_{MAX}}|}{V_{OUT_{FS}}}H}{I_{0_{coarse}}}$$

$$I_{0_{coarse}} = I_{0_{single}}\left(1 + \frac{\mid v_{ovcoarse_{MAX}} \mid}{V_{OUT_{FS}}}H\right). \tag{2.22}$$

Substituting $\mid v_{ovcoarse_{MAX}} \mid = H \mid v_{ovfine_{MAX}} \mid$ in Eq. 2.22 if H is fixed, in one extreme $v_{ovfine} \ll \frac{V_{OUT_{FS}}}{H^2}$, then $I_{0_{coarse}} \backsimeq I_{0_{single}}$ and the power dissipation of the current sources (not taking into account ZCD power dissipation) is comparable for both implementations. If $v_{ovfine_{MAX}} = \frac{V_{OUT_{FS}}}{H^2}$, then the coarse current doubles ($I_{0_{coarse}} \backsimeq 2I_{0_{single}}$) and the ramp rate of the coarse phase doubles (assuming C is fixed) compared to the single phase implementation at the same switched-capacitor circuit sampling rate. If $v_{ovfine_{MAX}} > \frac{V_{OUT_{FS}}}{H^2}$, $I_{0_{coarse}}$ will increase significantly in comparison to $I_{0_{single}}$ and the maximum output-dependent error $v_{ovfine_{MAX}}$ will also increase for a fixed H.

Another measure of the output linearity improvement of the dual ramp ZCB circuit over a single phase ZCB circuit is the ratio of the maximum fine phase overshoot $v_{ovfine_{MAX}} = -\frac{V_{OUT_{FS}} t_d I_{0coarse}}{HV_A C}$ (from Eq. 2.20) to the maximum overshoot $v_{ovsingle_{MAX}} = -\frac{V_{OUT_{FS}} t_d I_{0_{single}}}{V_A C}$ in a single phase implementation

$$\frac{\mid v_{ovfine_{MAX}} \mid}{\mid v_{ovsingle_{MAX}} \mid} = \frac{I_{0_{coarse}}}{I_{0_{single}}}\left(\frac{1}{H}\right). \tag{2.23}$$

If $I_{coarse} = HI_{single}$, there is no longer a benefit to using a dual ramp ZCB implemen-

tation as $I_{0_{single}} = I_{0_{fine}}$. Substituting Eq. 2.23 into Eq. 2.22 gives an expression for the improvement in output linearity for a fixed $I_{0_{single}}$, H and ratio $\frac{I_{0_{coarse}}}{I_{0_{single}}}$:

$$\frac{\mid v_{ovfine_{MAX}} \mid}{\mid v_{ovsingle_{MAX}} \mid} H = 1 + \frac{\mid v_{ovfine_{MAX}} \mid}{V_{OUT_{FS}}} H^2$$

$$\mid v_{ovfine_{MAX}} \mid = \frac{\mid v_{ovsingle_{MAX}} \mid}{H(1 - H\frac{\mid v_{ovsingle_{MAX}} \mid}{V_{OUT_{FS}}})}.$$

One downside to the dual ramp ZCB implementation is added complexity of the second phase and power dissipation during the fine phase, contributed by the ZCD and the fine phase current source I_{fine}. The power dissipation contribution of the ZCD in the case of a dynamic ZCD (as used in [4]) roughly doubles due to the ZCD second transition at the end of the fine phase. However, if a preamplifier is used as part of the ZCD architecture then the static power of the ZCD in the dual ramp case increases proportionately to the fine phase duration t_{fine}, assuming the coarse phase is equivalent to a single phase ZCB implementation ($I_{coarse} = I_{fine}$) for fixed load capacitor C. The fine phase current is only a fraction of the coarse phase current and the increase in power dissipation contributed by I_{fine} should not be significant in comparison to a single phase ZCBC of the same ramp current as the coarse phase current ($I_{coarse} = I_{fine}$) for fixed load capacitor C. However, the dual ramp ZCB circuit has to operate at lower speed than its single phase counterpart to allow for the fine phase duration (t_{fine}).

2.3.3 Dual Ramp ZCBC with Correlated Level Shifting (CLS)

A technique to further reduce the output-dependent overshoot error beyond the output linearity improvement introduced by dual ramp ZCBC is described in [17] used in a low-voltage zero-crossing based integrator in a delta-sigma ADC. It combines correlated level shifting (CLS) (similar to the technique in [16] in a 1.5bit per stage

opamp-based pipelined ADC) and dual ramp ZCBC operation. Correlated level shifting is a technique which reduces finite amplification gain error. In dual phase ZCBC's the natural break between the coarse and fine phases allows the implementation of the CLS with no penalty in charge transfer time. The basic principle of the ZCBC CLS technique is the combination of two-phase charge-transfer operation (estimation phase or coarse phase and level shifting phase or fine phase) with an additional output capacitor (C_{CLS} in Figure 2-8) which samples the output at the end of the estimation phase and cancels it from the feedback path during the level shifting phase. Capacitor C_{CLS} is charged in parallel with the load capacitor ($C_{eq} + C_{n+1}$) during the coarse phase. The function of C_{CLS} is to sample the rough output voltage estimate at the end of the coarse phase. During the fine phase, C_{CLS} decouples the ZCB output v_{OUT} from the fine phase current source output v_{CLS}, as shown in Figure 2-8. Thus the fine phase current source output is decoupled from the full-scale ZCBC output voltage. Therefore, the fine current source output voltage swing is only bound the overshoot error, which remains to be corrected by the end of the fine phase. Reduced output swing at the fine current source output node results in reduced current variation and better ZCBC output linearity as demonstrated earlier in Eq. 2.19. The timing diagram and output waveforms for the dual ramp ZCBC with CLS are the same as the ones shown in Figure 2-7b.

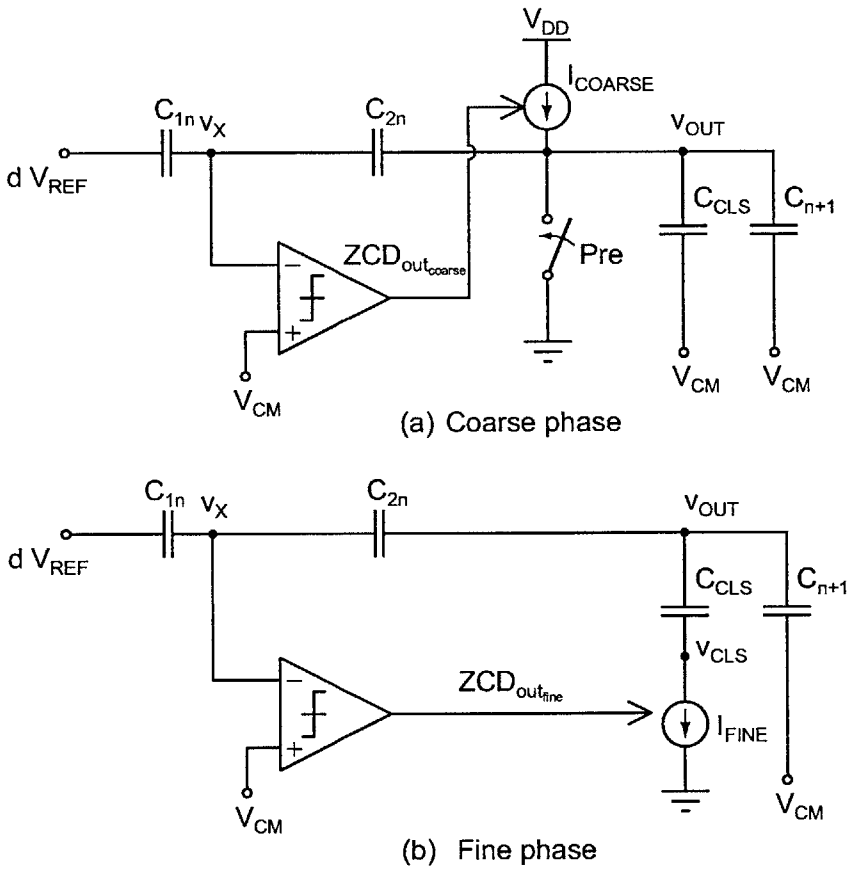


Figure 2-8: Simplified diagram of dual ramp ZCBC with CLS switched-capacitor circuit used as MDAC in a pipeline ADC stage. The coarse phase (top) and fine phase (bottom) of charge-transfer operation is similar to the dual ramp ZCB implementation but for a level shifting capacitor C_{CLS}, which samples the output at the end of the coarse phase and decouples the ZCB circuit output v_{OUT} from the fine phase current output v_{CLS}

The overshoot error at node v_{OUT} at the end of the fine phase is derived in detail in Appendix C, as a function of the ideal output voltage $v_O(t)$ and ZCD delay t_d (assumed to be the same for both phases of charge-transfer operation) :

$$v_{OV_{fine}}(v_O(t), t_d) = -\frac{\gamma I_{fine} t_d}{C_{fine}} - \frac{I_{0_{coarse}} t_d^3}{2R_{O_{coarse}} C_{coarse}^2 R_{O_{fine}} C_{fine}} + \frac{v_O(t) t_d^2}{R_{O_{coarse}} C_{coarse} R_{O_{fine}} C_{fine}}$$

where γ is the voltage divider ratio from node v_{CLS} to the output node v_{OUT}, $\gamma = \frac{C_{CLS}}{C_{eq}+C_{n+1}+C_{CLS}}$, $C_{coarse} = C_{CLS} + C_{n+1} + C_{eq}$ is the load capacitor being charged by I_{coarse} during the coarse phase and $C_{fine} = C_{CLS} \parallel (C_{n+1} + C_{eq})$ is the capacitor being discharged by I_{fine} in Figure 2-8. The fine phase output-dependent error $v_{ov_{fine}}$ is :

$$v_{ov_{fine}}(v_O(t), t_d) = \frac{v_O(t) t_d^2}{R_{O_{coarse}} C_{coarse} R_{O_{fine}} C_{fine}}$$

The transfer function for the dual ramp ZCB multiply-by-two switched-capacitor circuit charge-transfer, can be derived by adding the fine phase output-dependent error component $v_{ov_{fine}}(v_O(t))$ to the ideal output transfer function derived in Eq. 2.1 to yield:

$$v_{OUT} = \frac{(\frac{C_{1n}+C_{2n}}{C_{2n}}) v_{IN} - \frac{C_{1n}}{C_{2n}} dV_{REF}}{1 - \frac{t_d^2}{R_{O_{coarse}} C_{coarse} R_{O_{fine}} C_{fine}}}. \tag{2.24}$$

Substituting the expressions for C_{coarse} and C_{fine} in Eq. 2.24, and assuming the Early voltages for both fine and coarse current sources are approximately the same, the ZCB circuit transfer function becomes:

$$v_{OUT} \simeq \frac{(\frac{C_{1n}+C_{2n}}{C_{2n}}) v_{IN} - \frac{C_{1n}}{C_{2n}} dV_{REF}}{1 - \frac{t_d^2 I_{0_{coarse}} I_{0_{fine}}}{V_A^2 C_{CLS}(C_{n+1}+C_{eq})}}.$$

For the purpose of comparison to the dual ramp ZCB circuit implementation transfer function, the case of $C_{CLS} = C_{n+1} + C_{eq} = C$ is considered, the ZCB circuit transfer function can be re-written as:

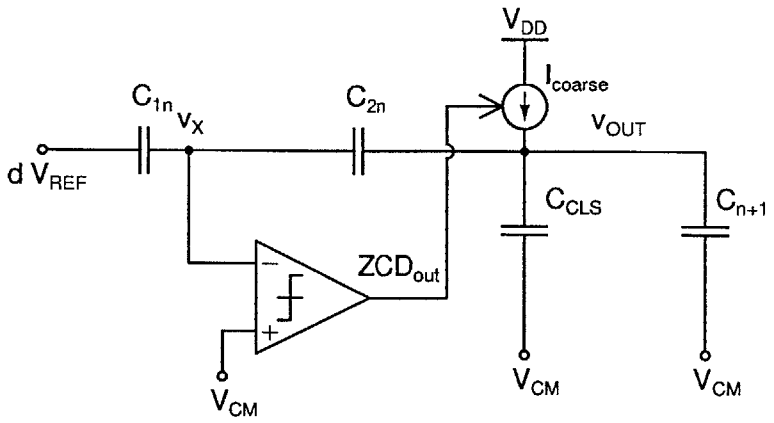
$$v_{OUT} \simeq \frac{(\frac{C_{1n}+C_{2n}}{C_{2n}})v_{IN} - \frac{C_{1n}}{C_{2n}}dV_{REF}}{1 - \frac{t_d^2 I_{0_{coarse}} I_{0_{fine}}}{V_A^2 C^2}}.$$

Note that in comparison to the dual ramp ZCB implementation without CLS, the gain error in the transfer ZCBC function contains only the square term dependent on t_d. The use of CLS therefore reduces the output-dependent overshoot error by $\frac{t_d I_{0_{coarse}}}{HV_A C}$. The downside is added power needed to charge the level shifting capacitor C_{CLS} during the coarse phase. If the level-shifting capacitor C_{CLS} is equal in value to the load capacitor C (as will be discussed further in Chapter 4 and is shown to be an optimal value in Appendix D), the coarse phase current source power doubles compared to the dual ramp implementation.

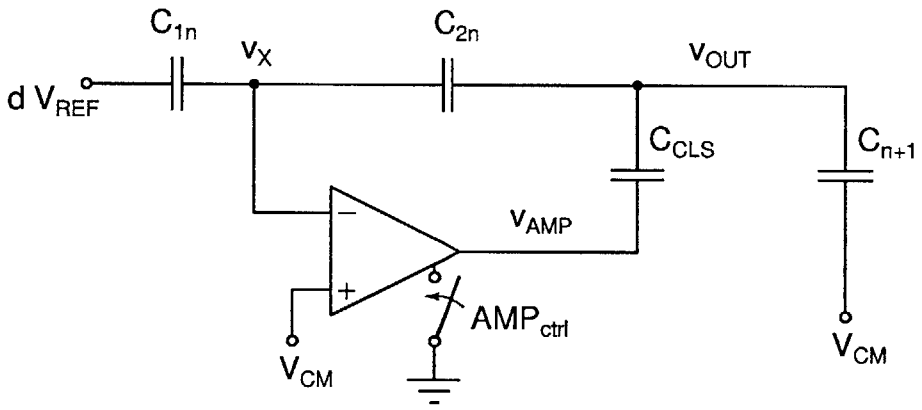
2.4 Hybrid CLS-OpAmp/ZCB Circuit

2.4.1 Architecture Overview

An alternative two-phase architecture, to the dual ramp ZCBC with CLS, is the hybrid CLS-OpAmp/ZCB circuit (Figure 2-9) introduced in [20], where it was implemented in an 11bit 20MHz 1.5bit/stage pipelined ADC. This topology combines the benefits of both ZCB and opamp based switched-capacitor circuits. The hybrid CLS-OpAmp/ZCB technique is also based on a two-phase charge-transfer operation. The first phase produces a power efficient, rough estimate of the virtual ground and output voltages based on ZCB charge-transfer operation. It is identical to the coarse phase of the dual ramp ZCBC (refer to Figure 2-9a). For improved output voltage linearity an additional phase, using an opamp in negative feedback configuration, corrects the coarse phase non-linearity. More specifically, the fine phase (Figure 2-9b) settles the overshoot error incurred at the end of the coarse phase to a more accurate estimate of the output voltage. The output waveform and timing diagram for the hybrid CLS-opamp/ZCB switched-capacitor circuit is shown in Figure 2-10.



(a) ZCB coarse phase of hybrid CLS-opamp/ZCB architecture



(b) Opamp-based phase of hybrid CLS-opamp/ZCD architecture

Figure 2-9: two-phase hybrid CLS-OpAmp/ZCB architecture used as MDAC in a pipelined ADC stage . The coarse phase is equivalent in operation to a single phase ZCB circuit. The fine phase is an opamp-based charge transfer phase. CLS is also used to decouple the opamp v_{AMP} output form the ZCB switched-capacitor circuit output v_{OUT}

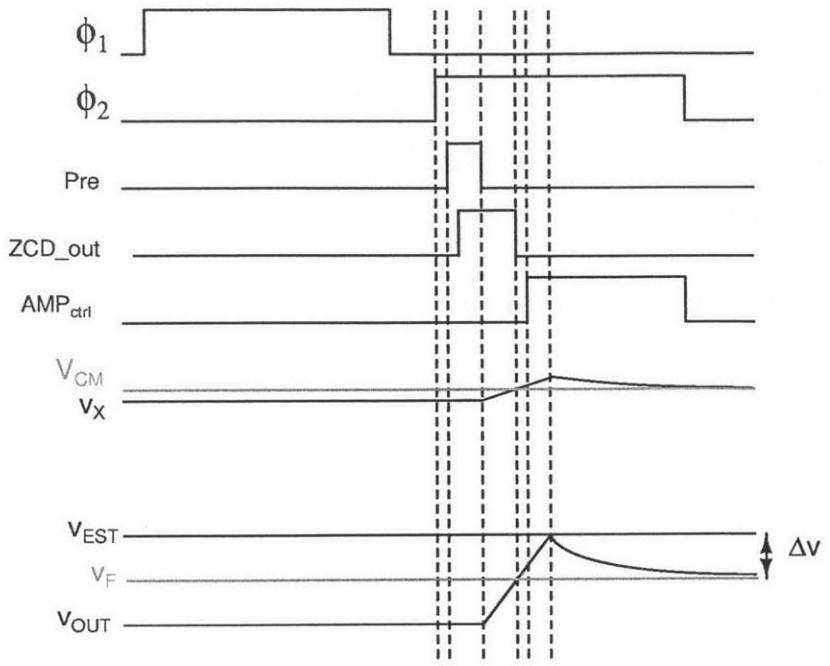


Figure 2-10: Timing diagram and voltage waveforms at the virtual ground node v_X and the ZCB switched-capacitor circuit output v_{OUT} for CLS-OpAmp/ZCBC implementation

To further improve the output voltage accuracy, the CLS technique described in Section 2.3.3 is also implemented in addition to combining ZCB with opamp based charge-transfer operation. The level shifting capacitor C_{CLS} is placed in series with the opamp output v_{AMP} during the fine phase (Figure 2-9b), effectively decoupling v_{AMP} from the switched-capacitor circuit output v_{OUT}. The initial output voltage of the opamp Δv at the beginning of the fine phase is proportional to the difference between the rough estimate v_{EST} and final value v_F of the output voltage v_{OUT}.

2.4.2 Advantages of Hybrid Approach

The advantages of this topology for high precision, high speed switched-capacitor circuits stem from the combination of the power efficiency of ZCBC with the added precision of opamp settling of the error at the virtual ground and output nodes through negative feedback. The use of level shifting capacitor C_{CLS}, combined with a two-phase operation, lessens the gain and swing requirements of the fine phase opamp. The additional opamp phase makes the architecture tolerant of errors limiting ZCBC

precision, especially at higher sampling rates and therefore higher ramp currents. In the context of a high speed, high precision pipeline ADC multiply-by-two switched-capacitor circuit, the errors alleviated by the hybrid CLS-opamp/ZCB topology can be broken down as follows:

- **Voltage reference settling error**

In conventional opamp based charge-transfer operation, the voltage references settle for the duration of the entire charge-transfer phase, which is half the sampling period. In ZCBC the zero-crossing instant is input-dependent in contrast to a conventional opamp-based switched-capacitor circuit, where the sampling instant occurs always at the end of ϕ_2. In single phase ZCBC, the voltage references of the pipelined ADC stage have to settle for the minimum input voltage at node v_X, which translates in time to a small fraction of the sampling period. If the voltage references do not settle, an input-dependent error is introduced, resulting in an output non-linearity.

An opamp based fine phase, following the ZCB charge-transfer phase, allows the voltage reference inputs to settle for the same time as in a conventional opamp based switched-capacitor circuit. In addition, during the fine phase the current through the reference switches decreases exponentially just as in an opamp-based switched-capacitor circuit. In contrast, the reference switches carry the entire ramp current in single phase ZCBC, resulting in input-dependent errors due to switch resistance variation.

- **Output-dependent switch resistance error**

The switches connecting the current source to the feedback capacitor C_{2n} and load capacitor C_{n+1} to the current source during the ZCB phase carry the entire ramp current. The resistance of either switch is dependent on the output voltage as the switch transistor drain or source is directly connected to the output. Current splitting is used [6] to remove series switches in the current path of the current sources and the associated voltage drops and will be discussed in more detail in Chapter 3.

In addition bootstrapping can reduce the switch resistance output dependence. At higher speeds and higher accuracy the total ramp current increases which, results in increased output-dependent voltage drops across the output switches, introducing a nonlinearity at the output.

The current through the output switch decreases as it is settled exponentially by the opamp during the fine phase. The initial value of the current, supplied by the opamp is only a function of the difference between the coarse phase output voltage estimate and the final value, which is significantly smaller than the coarse phase ZCBC current, thus reducing the voltage error across the switch. The exponential decay in current through the output switch reduces even further the contribution of voltage error due to variation in the switch resistance with output voltage and improved the output linearity of the switched-capacitor circuit.

- **Reduced opamp gain and settling requirements**

During the fine phase, the opamp only corrects the output-dependent overshoot error of the coarse ZCBC phase output voltage. The gain and settling requirements of the opamp are therefore reduced by the effective gain of the coarse phase compared to an opamp charge-transfer operation. The gain and settling opamp specifications are discussed in more detail in Chapter 4.

- **Reduced opamp output voltage range**

The opamp is decoupled from the full-swing output of the switched-capacitor circuit and effectively only corrects the output-dependent overshoot error of the coarse ZCB phase. The output swing for the opamp in a hybrid CLS-OpAmp/ZCB topology is therefore much smaller compared to the output swing of a conventional opamp based switched-capacitor circuit implementation as well as an opamp based CLS architecture. Small output swing allows for cascoding, for gain enhancement. Both output swing and choice of opamp topology are discussed in more detail in Chapter 4.

2.4.3 Fine Phase Charge-Transfer

Assuming an ideal opamp with infinite gain, which has fully settled, the change in charge during the fine charge-transfer phase on capacitance $C_{1n} \parallel C_{2n}$ is proportional to the change in the voltage across it:

$$\Delta Q_1 = \frac{C_1 C_2}{C_1 + C_2}[(v_O - V_{REF}) - (v_O + v_{ov} - V_{REF})]$$

where v_O is the ideal output voltage, v_{ov} is the output-dependent overshoot error, $v_O + v_{ov}$ is the final value at the end of the coarse phase (assuming the output independent overshoot error has been corrected) and v_O is the final value at the end the fine phase as the ideal opamp fully settles the coarse phase overshoot error. The change in charge during the fine phase on capacitor C_{n+1} is proportional to the change in the voltage across it:

$$\Delta Q_2 = C_{n+1}[(v_O - VCM) - (v_O + v_{ov} - VCM)].$$

The change in charge during the fine charge-transfer phase on the level shifting capacitor C_{CLS} is proportional to the change in the voltage across it:

$$\Delta Q_3 = C_{CLS}[(V_{CM} + v_{AMP} - v_O) - (V_{CM} - (v_O + v_{ov})]$$

$$\Delta Q_3 = C_{CLS}[(v_O - (V_{CM} + v_{amp_f}) - ((v_O + v_{ov}) - V_{CM})]$$

where v_{amp_f} is the final opamp output voltage with respect to V_{CM}. Charge conservation holds that $\Delta Q_1 + \Delta Q_2 + \Delta Q_3 = 0$:

$$\frac{C_1 C_2}{C_1 + C_2}(-v_{ov}) + C_{n+1}(-v_{ov}) + C_{CLS}(-v_{amp_f} - v_{ov}) = 0$$

$$v_{ov}(\frac{C_1C_2}{C_1+C_2}+C_{n+1}+C_{CLS})=v_{amp_f}C_{CLS}$$

$$\frac{v_{ov}}{v_{amp_f}}=\frac{C_{CLS}}{\frac{C_1C_2}{C_1+C_2}+C_{n+1}+C_{CLS}}. \tag{2.25}$$

Let

$$\gamma=\frac{C_{CLS}}{\frac{C_1C_2}{C_1+C_2}+C_{n+1}+C_{CLS}}, \tag{2.26}$$

then it follows that in the case of an ideal opamp with infinite gain, which settles fully by the end of φ_2 , the final value of the opamp output voltage is:

$$v_{amp_f}=\frac{1}{\gamma}v_{ov}. \tag{2.27}$$

From Eq. 3.12 it is evident that there is a trade-off between γ or the size of the level-shifting capacitor and the opamp voltage swing requirement, which will be discussed in further detail in 4.

2.4.4 Voltage Waveforms

To understand better the linearity limitations of hybrid CLS-OpAmp/ZCBC the output waveforms during the fine charge-transfer phase are described in this section.

To derive the transfer function of the fine opamp-based phase of charge-transfer operation, first the node voltages at the end of the coarse phase and beginning of fine phase will be established. The output voltage at the end of the coarse ZCB phase (see Figure 2-9a) can be described to first order to have the following components from the discussion on error contributions to v_{OUT} in Section 2.3:

$$v_{OUT} = v_O + V_{OV} + v_{ov} \tag{2.28}$$

where v_O is the ideal output voltage and V_{OV} is the constant part of the overshoot error for the case a finite ZCD delay of constant value t_d and constant slope ramp (refer to Eq. 2.14). The output-dependent component of the overshoot voltage error $v_{ov} = f(v_{OUT})$ is a first order approximation of a ZCB circuit with finite current source output resistance and finite ZCD delay of constant value t_d, assuming the current does not vary significantly with output voltage during t_d. The constant part of the overshoot appears as an input-referred offset and can be canceled as discussed previously. In [4, 20], different methods to address the constant overshoot error correction are proposed and are discussed here in more detail in Chapter 4. For simplicity of the analysis below, it is assumed to be corrected, i.e. $V_{OV} = 0$.

The virtual ground condition is not accurately met at the end of the coarse phase due to the non-idealities described above, resulting in an error at the opamp input node v_X. The voltage at v_X at the end of the coarse charge-transfer phase can be expressed as:

$$v_X = VCM + \beta v_{ov}(v_{OUT}) \tag{2.29}$$

where V_{CM} is the voltage at v_X if the virtual ground condition is fully satisfied at the end of the coarse phase and β is the output feedback factor $\beta = \frac{C_{2n}}{C_{1n}+C_{2n}}$ (refer to Figure 2-9b).

Next the fine phase node voltages will be established. At the start of the fine phase ($t = 0^-$) the opamp output starts at V_{CM},

$$v_{AMP}(0^-) = V_{CM}.$$

The opamp output voltage v_{AMP} during the fine phase can be expressed as:

$$v_{AMP}(t) = V_{CM} + v_{amp}(t).$$

The opamp input v_X during the fine charge-transfer phase can be described as:

$$v_X(t) = V_{CM} + v_x(t)$$

and the initial condition at node v_X at the beginning of the fine phase is

$$v_x(0^-) = \beta v_{ov}.$$

The output voltage (assuming $V_{OV} = 0$) can be expressed as:

$$v_{OUT} = v_O + v_{out}(t),$$

with an initial condition at the beginning of the fine phase

$$v_{out}(0^-) = v_{ov}.$$

As all incremental node voltages have been defined during the fine phase of charge-transfer operation, next a small signal model can be derived.

- **Small Signal Model**

The function of the level shifting capacitor C_{CLS}, as already described, is to store the estimate v_{OUT} of the ideal output voltage v_O at the end of the coarse phase. The opamp output voltage $v_{amp}(t)$ during the fine phase depends only on the error v_{ov} between the coarse estimate and the ideal output voltage v_O. Only the voltages $v_x(t)$, $v_{amp}(t)$ and $v_{out}(t)$, affected by the opamp charge-transfer operation are considered below. An equivalent small signal diagram of the fine opamp based charge-transfer phase is shown in Figure 2-11 based on the node voltages defined above.

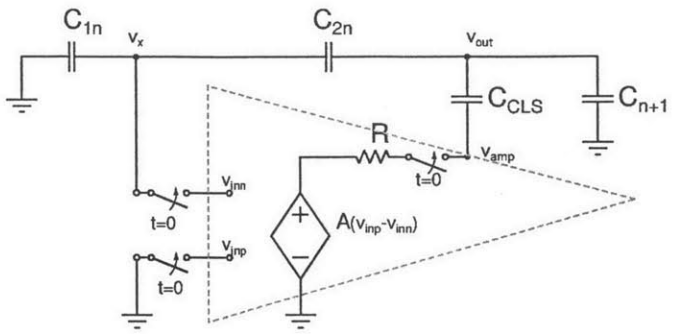


Figure 2-11: Fine phase small-signal diagram. Conventionally a voltage-dependent-voltage source models the function of the opamp

At the instant during the fine phase ($t = 0$) when the opamp is connected in a feedback configuration with capacitors C_{1n}, C_{2n}, C_{CLS} and C_{1n}, the voltage difference $v_{in} = v_{inp} - v_{inn}$ (refer to Figure2-11), where v_{inn} and v_{inp} are the inverting and non-inverting inputs of the opamp respectively, changes instantaneously from 0 to $-\beta v_{ov}$. Note that when the opamp is connected in feedback $v_x = v_{inn}$. The input to the opamp v_{in} at the beginning of the fine phase can be modeled as a unit step function $v_{in}(t)$ = -$\beta v_{ov} u(t)$, where v_{ov} is the output-dependent overshoot error. The voltage waveforms at v_{amp}, v_x, v_{out} can then be represented as superposition of the step responses v'_{amp}, $v'_x(t)$ and $v'_{out}(t)$ of the opamp in feedback configuration with capacitors C_{1n}, C_{2n}, C_{CLS} and C_{1n} with no initial charge on all capacitors and the initial voltages at nodes $v_{amp}(0^-)$, $v_x(0^-)$ and $v_{out}(0^-)$ before the opamp is connected in feedback. Therefore v_{amp}, v_x, v_{out} can be expressed as:

$$v_{amp}(t) = v_{amp}(0^-) + v'_{amp}(t) \tag{2.30}$$

$$v_x(t) = v_x(0^-) + v'_x(t) \tag{2.31}$$

$$v_{out}(t) = v_{out}(0^-) + v'_{out}(t). \tag{2.32}$$

The transfer function from the opamp output voltage to the opamp input can be derived as follows (refer to Figure 2-12):

$$\frac{v'_{amp}(s)}{v'_x(s)} = \frac{A(s)}{1 + \mathrm{KA(s)}} \tag{2.33}$$

where $K = \beta\gamma$ and $A(s) = \frac{A}{1+s\tau}$ is the opamp transfer function (assuming it can be described as a first order system with time constant τ and gain A). Substituting $A(s)$ into Eq. 2.33:

$$\frac{v'_{amp}(s)}{v'_x(s)} = \frac{A}{1 + s\tau + KA} \tag{2.34}$$

$$= \frac{A}{\tau}\left(\frac{1}{\frac{1+KA}{\tau} + s}\right). \tag{2.35}$$

Taking the Laplace transform of the input $v_{in}(t)$ and substituting it in Eq. 2.35, the output voltage $v'_{amp}(s)$ ca be expressed as:

$$v'_{amp}(s) = -\frac{A}{\tau}\left(\frac{1}{\frac{1+KA}{\tau} + s}\right)\left(\frac{-\beta v_{ov}}{s}\right). \tag{2.36}$$

Taking the inverse Laplace transform of Eq. 2.36 yields the opamp output voltage v_{amp} as a function of time during the fine charge-transfer phase:

$$v'_{amp}(t) = -\beta v_{ov}\left(\frac{A}{1 + AK}\right)\left(1 - e^{-\frac{t(1+AK)}{\tau}}\right). \tag{2.37}$$

From and Eq. it follows that $v'_{out} = \gamma v'_{amp} = -\gamma\beta v_{ov}\left(\frac{A}{1+AK}\right)\left(1 - e^{-\frac{t(1+AK)}{\tau}}\right)$. Thus the step repose at node v_{out} is:

$$v'_{out}(t) = -v_{ov}\left(\frac{AK}{1 + AK}\right)\left(1 - e^{-\frac{t(1+AK)}{\tau}}\right). \tag{2.38}$$

The voltage at node v_x is related to the output voltage v_{out} by $v_x = \beta v_{out}$. Therefore

the step repose at node v_x is:

$$v_x'(t) = -\beta v_{ov}(\frac{AK}{1+AK})(1 - e^{-\frac{t(1+AK)}{\tau}}). \tag{2.39}$$

From Eq. 2.30 , Eq. 2.31, Eq. 2.32, and Eq. 2.37, Eq. 2.39 and Eq. 2.38 the fine phase voltages at nodes v_{amp}, v_x, v_{out} can be expressed as:

$$v_{amp}(t) = -\beta v_{ov}(\frac{A}{1+AK})(1 - e^{-\frac{t(1+AK)}{\tau}}) \tag{2.40}$$

$$v_x(t) = -\beta v_{ov}(\frac{1}{1+AK}) + \beta v_{ov}(\frac{AK}{1+AK})e^{-\frac{t(1+AK)}{\tau}}) \tag{2.41}$$

$$v_{out}(t) = v_{ov}(\frac{1}{1+AK}) + v_{ov}(\frac{AK}{1+AK})e^{-\frac{t(1+AK)}{\tau}}) \tag{2.42}$$

and are plotted as a function of time are plotted in Figure 2-15, Figure 2-14, and Figure 2-13 respectively.

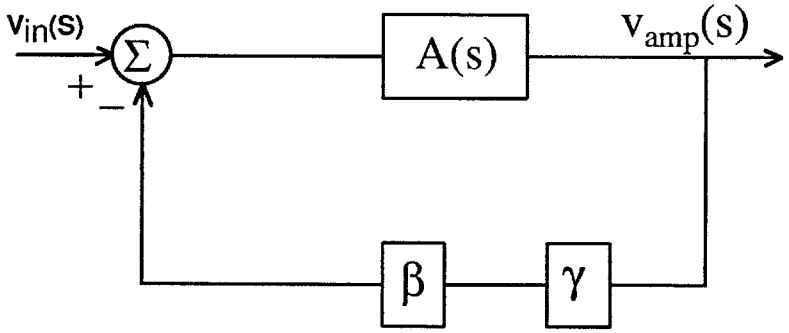


Figure 2-12: Block diagram for the transfer function the opamp input $v_{in}(s)$ to the opamp output voltage $v_{amp}(s)$.

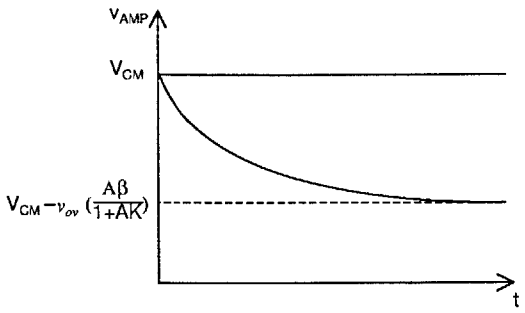


Figure 2-13: Fine charge-transfer phase time waveform at the opamp output node v_{AMP}.

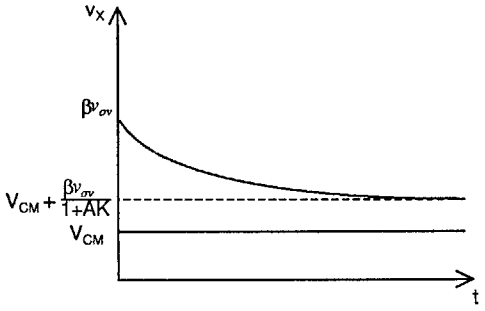


Figure 2-14: Fine charge-transfer phase time waveform at the negative feedback node v_X.

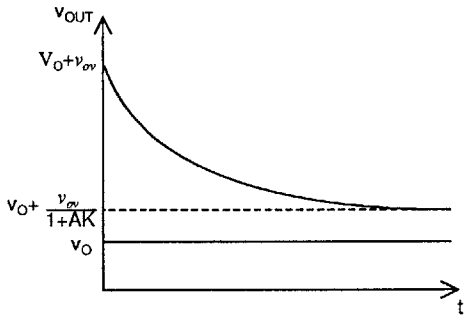


Figure 2-15: Fine charge-transfer phase time waveform at the output node v_{OUT}.

The transfer function for hybrid CLS-OpAmp/ZCBC can be expressed by adding the error $v_{ov} = -\frac{v_O(t)I_0t_d}{V_AC}$ at the output voltage node v_{OUT} to the ideal transfer function From Eq. 2.1 to obtain:

$$v_{OUT} \simeq \frac{(\frac{C_{1n}+C_{2n}}{C_{2n}})v_{IN} - \frac{C_{1n}}{C_{2n}}dV_{REF}}{1+\left(\frac{I_0t_d}{V_AC}\right)\left(\frac{1}{1+A\beta\gamma}\right)}. \tag{2.43}$$

In the above expression it has been assumed that the opamp has settled to the desired accuracy and only the gain error is considered for the purpose of comparison.

2.5 Conclusion

Table 2.1 summarizes the output voltage and gain error for the different ZCB topologies described in this chapter when used in a multiply-by-two switched-capacitor realization of an MDAC in an n^{th} pipelined ADC stage. To simplify the output voltage error comparison, suppose the sampling rate, ZCD delay t_d and load capacitor C are fixed for all topologies. Moreover, suppose all two-phase based topologies use the same coarse ZCB phase with ramp current $I_{0_{coarse}}$. Note also that in the analysis thus far the ZCD delay t_d at the end of the coarse and fine phases has been assumed equal.

The gain error of a single phase ZCB topology is similar in form to the gain error of a conventional opamp based switched-capacitor circuit using negative feedback. One important difference is that the ZCB topology gain error is proportional to the ramp rate and will increase with the ADC sampling rate, while in the conventional opamp based circuit, the gain error is static. The opamp is assumed to have settled to the required accuracy of the multiply-by-two switched-capacitor circuit. The main advantage of ZCBC is their power-efficiency in performing the charge-transfer operation in switched-capacitor circuits [25].

The gain error improves from the single to dual ramp ZCB implementation by a factor of $\frac{I_{0coarse}}{I_0 H}$ if only the linear ZCD delay-dependent error term in Table 2.1 is taken into account. Note that if the sampling rate is fixed, then the coarse phase ramp current has to be larger than the single phase ZCB current, $I_{0_{coarse}} > I_0$. The dual ramp ZCB charge-transfer operation takes advantage of a fast coarse ramp which allows the fine phase current to be reduced by a factor of H since it is used to only correct the output-dependent overshoot error of the coarse phase output. Reduced current during the fine phase ZCD transition results in a decreased output-dependent

overshoot error and therefore improved output linearity by a factor of H. The downside is increased power dissipation, the reasons for which are twofold. The ZCD has to detect the second virtual ground condition during the fine phase. If a dynamic ZCD is used, this results in power increase by a factor of two if the same ZCD is used during both phases. If a preamplifier is needed in the ZCD architecture, then the preamplifier bias current contributes to power dissipation for the entire charge-transfer phase in contrast to single phase ZCBC, where the time, during which, the preamplifier in on is input-dependent. The second source of increased power dissipation comes from of the coarse phase current as discussed in Section 2.3.2, assuming the fine phase current contribution is small. A slower more power-efficient ZCD can be used for the second zero-crossing detection to alleviate the power penalty of dual ramp charge-transfer.

The dual ramp ZCB architecture with CLS eliminates the gain error term linear with respect to the ZCD delay t_d ($\frac{t_d I_{0_{coarse}}}{HV_A C}$), present in the dual ramp ZCB circuit and therefore improves the output linearity of the multiply-by-two circuit. This comes at the expense of larger power dissipation during the coarse phase, necessary to charge the level shifting capacitor C_{CLS}.

In the hybrid CLS-opamp/ZCB architecture, the use of an opamp, in place of a fine ZCB phase, is an improvement in terms of gain error over the dual ramp ZCB topology because the error term $\frac{t_d I_{0_{coarse}}}{HV_A C} - \frac{t_d^2 I_{0_{coarse}}^2}{HV_A^2 C^2}$ is reduced by the loop gain of the circuit $\frac{1}{A\beta\gamma}(\frac{t_d I_{0_{coarse}}}{HV_A C} - \frac{t_d^2 I_{0_{coarse}}^2}{HV_A^2 C^2})$. Compared to dual ramp ZCB circuit with CLS, the linear term of the gain error with respect to the ZCD delay t_d is not eliminated but greatly reduced. Using an opamp during the fine phase comes at a cost of greater power dissipation compared to the power dissipation of the fine phase of a dual ramp ZCB circuit with CLS, which is due to a fine phase current source and the second transition of the ZCD. One important advantage of the hybrid CLS-opamp/ZCB topology is that it reduces errors caused by voltage drops across switches, which contribute to output non-linearity in addition to the overshoot error. The current

through the output switches and reference voltage switches decays exponentially as the output settles and the input to the opamp approaches virtual ground. In the ZCB architectures the current through the switches in the circuit is the entire ramp current and it is even larger for a single phase ZCB circuit by a factor of $\frac{I_{0single}}{I_{0fine}}$ compared to its two-phase counterparts. The opamp based phase only has to settle the output voltage error to a few time constants compared to a conventional opamp-based circuits and as shown in [39], the power efficiency of opamps in switched-capacitor circuits is inversely proportional to the number of settling time constants.

Multiply-by-two, switched-capacitor circuit	Equivalent gain error
Conventional opamp-based	$\frac{v_O}{A\beta}$
Single phase ZCB	$\frac{t_d I_0}{V_A C}$
Two phase ZCB	$\frac{t_d I_{0_{coarse}}}{HV_A C} - \frac{t_d^2 I_{0_{coarse}}^2}{HV_A^2 C^2}$
Tow phase ZCB with CLS	$-\frac{t_d^2 I_{0_{coarse}}^2}{HV_A^2 C^2}$
Hybrid CLS-OpAmp/ZCB	$\frac{\left(\frac{t_d I_{0_{coarse}}}{V_A C}\right)}{A\beta\gamma}$

Table 2.1: Comparison of output voltage error and gain error of a conventional switched-capacitor circuit and the four different ZCB topologies presented in this chapter.

Chapter 3

Techniques for Improved Precision in High Speed ZCBC

This chapter discusses circuit techniques, which improve performance in high speed, high-precision zero-crossing based circuits (ZCBC) in terms of output swing, power efficiency and output linearity. Although the circuit techniques presented here are developed for hybrid CLS-opamp/ZCB pipelined ADCs, they are relevant to other ZCB implementations. The hybrid CLS-opamp/ZCB circuit is based on two phases of charge-transfer operation: a ZCB coarse phase and a slower opamp-based fine phase. The coarse phase output linearity determines the gain and bandwidth requirements of the fine phase opamp. Higher opamp bandwidth requires higher power dissipation during the fine phase. Thus for a power efficient, high precision, high speed two phase charge-transfer operation, it is important to optimize the ZCB phase output linearity.

The two circuit techniques, presented in this chapter, focus on improving the coarse ZCB phase performance. At high output rate, current steering is used in place of turning off the current sources through a switch at the gate of the cascode devices at the end of the ZCB phase, which minimizes the current source turn-off delay and ZCD delay and improves output linearity. A bidirectional ramp technique, introduced in the following section, extends the ZCB phase operating output range,

while it simultaneously allows for current source cascoding in ZCBC to boost output linearity.

3.1 ZCBC Output Sampling

Charge-transfer in an n^{th} ZCB pipelined ADC stage relies on a current source charging a load capacitor. The load capacitor consists of the configuration of the input and feedback capacitors of the n^{th} stage in series connected in parallel to the input sampling capacitors of the $n+1$ stage. A zero crossing detector (ZCD) replaces the function of an opamp in a conventional charge-transfer operation and signals when the virtual ground condition is satisfied. The output of the ADC stage is next sampled on the input capacitors of the subsequent pipeline stage. In an opamp based charger-transfer operation, the current through switches in the switched-capacitor circuit diminishes exponentially as the circuit settles to steady state. In contrast, any switches present in the current source path of the ZCB switched-capacitor circuit carry the entire ramp current at the output sampling instant and contribute voltage errors that limit circuit output linearity.

3.1.1 Background

The charge-transfer phase of an n^{th} stage of a single-ended, single phase ZCB pipelined ADC is shown in Figure 3-1. Current source splitting first demonstrated in a single-ended 8-bit pipelined ADC [4], is used to eliminate the series switch, which connects the feedback capacitor C_{n2} to the output node v_{OUT} in a pipeline ADC stage for and their associated voltage error drops. Output-dependent switch error results from the fact that both the switch resistance as well as current flow through the switch vary with output voltage. Current source splitting consists of replacing a single current source at the output with two current sources. In Figure 3-1: the first current source charges the stage load capacitor ($C_{n1} \parallel C_{n2}$), comprised of the input and feedback capacitors of the n^{th} stage in series. The second current source charges the input

sampling capacitor of the $n+1$ stage (C_{n+1}). Thus each of the two current sources is dedicated to effectively charge a single capacitor and a separate ramp is generated at nodes v_{OUT} and v'_{OUT}. The currents I_1 and I_2 are scaled such that the ramp rates at v_{OUT} and v'_{OUT} are equal. When current source splitting is used $sw1$ has to carry only the mismatch current between I_1 and I_2. The output-dependent switch voltage error is proportional to the difference in the current flowing through the two current sources due to device variation and can be negligible by carefully matching the ramp rates at v_{OUT} and v'_{OUT} and making $sw1$ large. Even though in a hybrid CLS-OpAmp/ZCB topology the fine phase attenuates errors from the coarse phase, the coarse phase linearity limits the overall attainable accuracy of the stage. In addition it sets the accuracy requirement on the fine phase and therefore its power efficiency. The focus of this section is on improving the coarse phase output linearity .

The remaining switches in the current path of the circuit are: the switches at the pipelined ADC reference voltages and the switch at the bottom plate of C_{n+1}. In this section, it is assumed that the resistance of the reference switches is minimized by choosing large width devices to allow sufficient settling of the ADC reference voltages at the output sampling instant. The sizing of the reference switches is less stringent for the charge-transfer phase in a hybrid CLS-opamp/ZCB circuit as the references have the entire duration of ϕ_2 to settle. In addition, the current decreases exponentially through the reference switches during the opamp based fine phase, reducing their final error contribution at the output. The focus in this section is on the switch at the bottom plate of the load capacitor C_{n+1} in addition to minimizing ZCD and current source trun-off delay.

3.1.2 Output Sampling in High Precision, High Speed ZCBC

3.1.2.1 Single phase ZCBC

In previous ZCB pipelined ADC implementations [36, 6, 9, 26], the output sampling instant is defined as the instant at which the ZCD detects the virtual ground condition

and turns off the bottom plate output sampling switch, implemented by $M5$ in Figure 3-1. When $M5$ is switched off, the charge on load capacitor C_{n+1} is fixed and it is not disturbed by the output current source formed by transistors $M1, M2$, which is turned off next. During the short time, when the output current source is still on and $M5$ is turned off, the output current source effectively charges only the parasitic capacitance Cp at v_{OUT}. Next both current sources at v_{OUT} $(M1, M2)$ and v'_{OUT} $(M3, M4)$ are turned off. Switches $M6$ and $M8$ control the turn-on, and $M8$ and $M9$ control the turn-off of the current source cascode devices $M1$ and $M3$, triggered by $P_{CAS_{ctrl}}$ as shown in Figure 3-1 and 3-2.

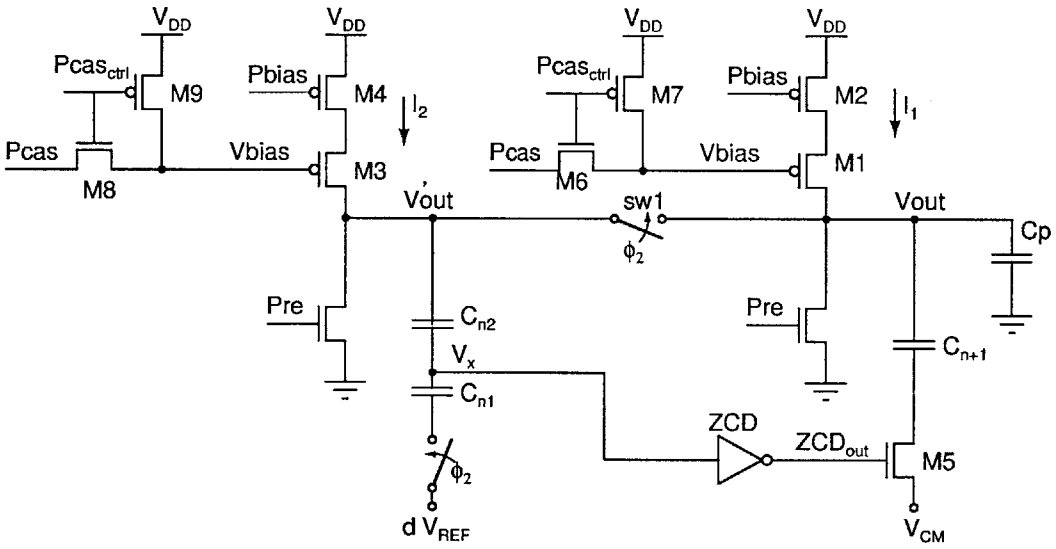


Figure 3-1: Single-ended single phase ZCB charge-transfer phase (ϕ_2) implementation [4]. Bottom plate sampling is used ($M1$) to sample the output on capacitor C_{n+1}.

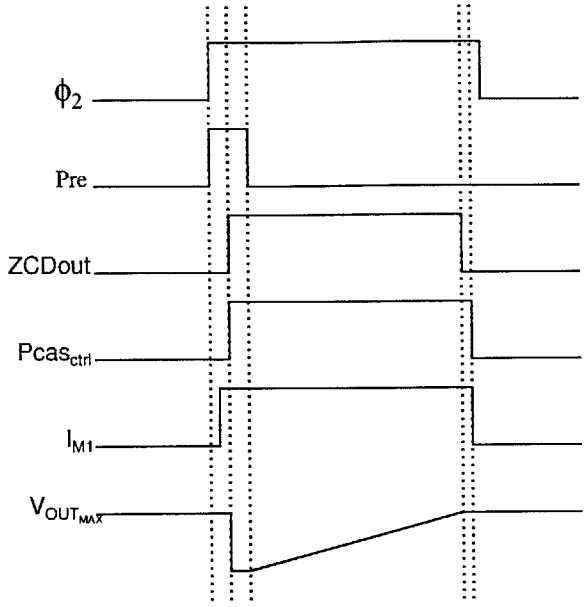


Figure 3-2: Timing diagram for the charge-transfer phase (ϕ_2) of single phase single-ended ZCB implementation

In single phase ZCBC the maximum ramp duration t_{ramp} (which occurs at the maximum output voltage $v_{OUT_{max}}$), is smaller than $\frac{T_s}{2}$ (where T_s is the ADC sampling period) by the duration of the preset phase (Pre) as shown in Figure 3-2. Since the preset phase is much smaller than $\frac{T_s}{2}$, for the purpose of this discussion it is assumed that $t_{ramp} \simeq \frac{T_s}{2}$. As the desired pipelined ADC resolution increases, larger input sampling capacitors are used to lower sampled thermal noise. Larger ZCB circuit load capacitor C requires larger ramp current for the same ramp rate. For example, to reduce the sampled thermal noise by a factor of 2, C_{n1} and C_{n2}, as well as C_{n+1} have to be increased by a factor of 4, which results in a factor of 4 increase in ramp current I at a fixed ramp rate. At higher pipelined ADC sampling rates, for fixed ADC resolution (i.e. fixed C) and ZCBC output range $V_{OUT_{FS}}$, the ramp rate increases, $\frac{dv_{OUT}}{dt} = \frac{V_{OUT_{FS}}}{\frac{T_s}{2}}$. From $\frac{I}{C} = \frac{V_{OUT_{FS}}}{\frac{T_s}{2}}$ it follows that the ramp current I increases inversely proportionately to T_s:

Since $sw1$ only carries mismatch current as discussed previously, the error it contributes can be ignored in this discussion. However, at higher currents, the mismatch current increases. Bootstrapping can be used for $sw1$ in order to minimize the varia-

tion of its switch resistance with output voltage. In contrast to $sw1$, the bottom plate sampling switch $M5$ carries the entire current I_1 of the output current source. The current I_1 varies with the output voltage v_{OUT} due to the finite output resistance of the current sources, which results in voltage variation across $M5$. The variation of I_1 with output voltage by Eq. 4.39 in Section 2.3.1.1 as:

$$I_1(t) = I_0 - \frac{I_0 t}{R_O C_{n+1}}, \tag{3.1}$$

where I_0 is the ideal current of $M1$ and R_O is the current source output resistance. The voltage V_{M5} at the drain of $M5$ is

$$V_{M5} = I_1(t) r_{on}$$

where r_{on} is the on-resistance of transistor $M5$ when operating in triode region. The voltage error ϵ_{M5} in voltage V_{M5} due to the change in I_1 with output voltage can be derived by combining Eq. 3.2 to express the ideal value I_0 of I_1 as $I_0 = \frac{V_{OUT_{FS}} C_{n+1}}{\frac{T_s}{2}}$, and Eq. 3.1:

$$I = \frac{V_{OUT_{FS}} C}{\frac{T_s}{2}}. \tag{3.2}$$

From Eq. 3.2 it follows that at higher ADC resolution and sampling rates, the ramp current increases as do the errors contributed by the voltage drop across switches in the current path.

$$\epsilon_{M5} = -\frac{I_0 t}{R_O C_{n+1}} r_{on} \tag{3.3}$$

$$= -\frac{V_{OUT_{FS}} C_{n+1} t}{\frac{T_s}{2} R_O C_{n+1}} r_{on} \tag{3.4}$$

$$= -\frac{V_{OUT_{FS}} t}{\frac{T_s}{2} R_O} r_{on}. \tag{3.5}$$

From Eq. 3.3 it is clear that ϵ_{M5} can be reduced by decreasing the resistance of $M5$. The switch resistance of $M5$ can be expressed by recalling the resistance of a transistor operating in the triode region :

$$r_{on} = \frac{1}{\mu_n C_{OX} \frac{W}{L}(V_{GS} - V_{TN} - V_{DS})}, \tag{3.6}$$

where μ_n is the transistor channel charge mobility, C_{OX} is the oxide capacitance of the transistor, W and L are the width and length of the transistor and V_{GS},V_{DS} and V_{TH} are the gate source voltage, drain source voltage and transistor threshold voltage respectively. Ignoring the dependence of r_{on} on the voltage across $M5$, ϵ_{M5} is:

$$\epsilon_{M5} = -\frac{V_{OUT_{FS}} t}{\frac{T_s}{2} R_O} \left(\frac{1}{\mu_n C_{OX} \frac{W}{L}(V_{GS} - V_{TN})} \right). \tag{3.7}$$

To reduce ϵ_{M5}, the width of $M5$ can be increased (while keeping minimum length to minimize parasitic capacitance), since the remaining parameters in Eq. 3.7 are fixed. At $t = \frac{T_s}{2}$, ϵ_{M5} is at its maximum and is equal to $\mid \frac{V_{OUT_{FS}} r_{on}}{R_O} \mid$. The downside of increasing the width of $M5$ is that the gate capacitance of $M5$ increases, which requires higher ZCD power dissipation for the same switch turn-off speed. Conversely larger gate parasitic capacitance presents a load to the ZCD and can result in a ZCD delay increase for fixed power dissipation, which in turn diminishes the output linearity of the circuit.

3.1.2.2 Dual Ramp ZCBC

In a dual ramp ZCB pipelined ADC stage, the coarse ZCB phase is equivalent to the one shown in Figure 3-1. The ramp duration in contrast to single phase ZCB implementation is $t_{ramp} = f\frac{T_s}{2}$, where f is a small fraction of $\frac{T_s}{2}$. For fixed load capacitor C and ADC sampling rate this results in a factor of $\frac{1}{f}$ increase in ramp current I during the coarse phase compared to a single phase ZCB implementation. The coarse ramp current I can be expressed as a function of the maximum output voltage $V_{OUT_{FS}}$ as:

$$I = \frac{V_{OUT_{FS}} C}{\frac{T_s}{2} f}. \tag{3.8}$$

In dual ramp ZCBC the ramp current increases at a rate larger by a factor of $\frac{1}{f}$ compared the ramp current increase in single phase ZCBC for fixed $V_{OUT_{max}}$ (refer to Eq. 3.2). It follows that the error due to the resistance of the switch at the bottom plate of C_{n+1} increases proportionately at the end of the coarse phase in a dual ramp ZCBC compared to its single phase counterpart.

In dual ramp ZCBC an approximate value of the output is first stored on the load capacitor and then the final output value is sampled at the end of the charge-transfer phase. The current sources are turned off at the end of the coarse phase, when the ZCD output transitions and the output is stored on the load capacitor C. The fine phase current sources are then turned on at the beginning of the fine phase. The fine phase output current is a fraction of the coarse phase output current and thus the error incurred by the bottom plate sampling switch is a fraction of the switch error at the end of the coarse phase.

The focus of this discussion is on accuracy limitations of the coarse phase. Substituting Eq. 3.8 into Eq. 3.3, the error at the drain of the bottom plate sampling transistor at the end of the coarse phase is:

$$\begin{aligned} \epsilon &= -\frac{\frac{V_{OUT_{FS}} C_{n+1}}{\frac{T_s}{2} f} t}{R_O C_{n+1}} r_{on} \\ &= -\frac{V_{OUT_{FS}} t}{\frac{T_s}{2} f R_O} r_{on} \end{aligned}$$

At $t = \frac{T_s}{2}$, ϵ achieves its maximum value $\mid \frac{V_{OUT_{FS}} r_{on}}{f R_O} \mid$. For fixed ADC resolution, sampling rate and ZCBC output range, the error across the bottom plate sampling switch at the output sampling instant is increased by a factor of $\frac{1}{f}$ compared to the error in a single phase implementation (refer to Eq. 3.3). For the same error as in a

single phase implementation, the width of the sampling transistor has to be increased by $\frac{1}{f}$ compared to its single phase counterpart. Larger width switch device translates into a larger gate parasitic capacitor and an increase in the delay in turning off the current sources, which results in an increase in the output overshoot error. However, in a dual ramp ZCBC the switch voltage error is reduced by the fine phase and the width of the sampling transistor does not have to increase by $\frac{1}{f}$.

An important difference between single phase and dual ramp ZCBC is the effect of turn-off time of the current sources. While in the single phase case the turn-off time is not critical, in the dual ramp implementation it delays the start of the fine phase of charge-transfer operation. The current source devices are designed for small saturation voltage (V_{DSAT}) to maximize the output swing especially at low supply voltages. This results in increased current source device width and gate parasitic capacitance. The larger cascode device gate capacitance will load the analog multiplexer, which switches the cascode voltage from $Pcas$ to V_{DD} (refer to Figure 3-1). This will increase the time constant of the multiplexer for a fixed on-resistance and increase the delay to turn off the current source. The multiplexer switch resistance is proportional to the width of the device for a minimum length device and its gate capacitor loads the ZCD and increases the delay t_d and therefore the output overshoot error. The power increase due to the larger gate capacitance is $P = \frac{1}{2}(V_{DD} - P_{cas})^2 C_{gs} f_s$, where f_s is the ADC sampling rate.

3.1.2.3 Hybrid CLS-OpAmp/ZCBC

Figure 3-3 illustrates the coarse ZCB charge-transfer phase of a hybrid CLS-OpAmp/ZCB pipelined ADC stage. The CLS technique [16] introduces capacitor C_{CLS} to sample the output signal v''_{OUT} at the end of the coarse ZCB phase in order to reduce the amplification gain error at the end of the charge-transfer phase ϕ_2. The output values at v_{OUT} , v'_{OUT} and v''_{OUT} are sampled at the end of the coarse phase. The presence of C_{CLS} further increases the coarse phase ramp current requirement for fixed ADC

sampling rate and resolution in comparison to the ramp current in dual ramp ZCBC. The choice of capacitor value for C_{CLS} will be discussed in more detail in Chapter 4 and is assumed in this discussion to be $C_{CLS} = (C_{n1} \parallel C_{n2}) + C_{n+1}$. In this case the coarse phase ramp current increases by a factor of 2, compared to the coarse phase current in dual ramp ZCBC. The total coarse phase current $I = I_1 + I_2 + I_3$ (refer to Figure 3-3) can be expressed as a function of the full swing output voltage $V_{OUT_{FS}}$ as:

$$I = \frac{V_{OUT_{FS}} 2C}{(\frac{T_s}{2}) f},$$

where $2C = C_{CLS} + (C_{n1} \parallel C_{n2}) + C_{n+1}$ (if $C_{CLS} = (C_{n1} \parallel C_{n2}) + C_{n+1}$). Thus at high ADC resolution and sampling rate, the ramp current increases at a rate larger by a factor of $\frac{2}{f}$ compared to the ramp current in single phase ZCBC and by a factor of 2 compared to the coarse phase current in dual ramp ZCBC. The gate capacitance of the current source devices increases with the the total ramp current I, for fixed device saturation voltage V_{DSAT}. If the ZCD is unchanged in the three ZCB topologies the load at the output of the ZCD increases. As the the gate capacitance of $M1$ and $M3$ increases (in Figure 3-1), the width of devices $M7$ and $M9$ increases for the same time constant $C_{gs_{M1}} r_{on_{M7}}$ and fixed device length. The gate capacitance of $M7$ and $M9$ increases in turn and loads the ZCD. As a result the delay t_d increases for fixed ZCD power dissipation and the overshoot error increases proportionately to t_d.

The voltage error at the drain of $M5$ at the end of the coarse phase and the corresponding voltage error in dual ramp ZCBC are the same because in both implementations the bottom plate switch of C_{n+1} carries current I_1 during the coarse phase, for fixed ramp rate and output range.

At ADC sampling rate of $100MS/s$, the coarse phase maximum ramp duration t_{ramp} is on the order of $1ns$, which translates to a ramp rate $\frac{dvout}{dt} = \frac{1V}{1ns}$ for an output voltage range of $1V$. Suppose 13 bits of resolution at a sampling rate of $100MS/s$ are desired. For a N-bit ADC if the mean-square thermal noise power is equal to the

quantization error noise power, the input sampling capacitor C_{IN} is:

$$C_{IN} = \frac{2^{2N}(12)\,kT}{V_{FS}^2}. \tag{3.9}$$

For a conservative fully differential design, $N = 13.8$ is chosen and from Eq. 3.9, $C_{IN} = 3.4pF$ for an ADC input range of $V_{FS} = 1.75V$. The input sampling capacitor at either input is then $C_1 = 2C_{IN} = 6.8pF$. The equivalent capacitor $C_{11} \parallel C_{21}$ is $1.3pF$, the load capacitor C_2 is $1.7pF$ and the level shifting capacitor C_{CLS} is $3pF$. The total ramp current I during the coarse ZCBC phase equals:

$$I = C\frac{dv_{OUT}}{dt},$$

where $C_{TOT} = (C_{1n} \parallel C_{2n}) + C_{CLS} + C_{n+1} = 6pF$. This results is:

$$I \simeq 6pF\frac{1V}{1n} \simeq 6mA.$$

In the case of $6mA$, the total gate parasitic capacitance of the current sources of $M1, M3$ and $M11$ in $65nm$ CMOS technology for 64 devices in parallel of $W = 4.08\mu m$ and $L = 120nm$ is approximately $0.4pF$. As an example if the switch resistance of the analog multiplexer at the cascode node is 10Ω, the resulting time constant is $4ps$ to turn off the current sources. The gate capacitance of the switch with 10Ω on-resistance is on the order of $\sim 35fF$ from Cadence simulations and presents itself as load to the ZCD and for fixed ZCD bias current increases the delay t_d. Both the switch time constant as well as the ZCD delay increase due to the extra load of $\sim 35fF$ result in an increase in the output overshoot error.

At high ADC resolution and sampling rate, the coarse ramp current increases which requires an increase in the size of $M5$ and $M6$ (refer to Figure 3-3) in order to reduce their voltage error contribution to the output non-linearity. Increased gate parasitic capacitance of the cascode current source devices results in increased delay from the instant at which the virtual ground condition is satisfied to the output sampling instant and increased power dissipation. Increased delay translates to output non-

linearity, which limits the accuracy of the ZCBC charge-transfer phase.

3.1.3 Current Steering

To improve the coarse ZCB phase output linearity, the current through the bottom sampling switches at the sampling instant and the current source turn-off delay must be minimized. One way to achieve this is to use current steering to define the output sampling instant at the end of the coarse phase. In Figure 3-3 current is steered away from the cascode devices $M1, M3$ and $M7$ through switches $M9, M10$ and M_{11} at the cascode nodes $V_{cas}, V_{cas_{CLS}}, V_{cas_f}$ respectively at the end of the coarse phase. The cascode nodes have to swing only by approximately one saturation voltage of the current source devices (V_{DSAT}) to steer most of the current away. In Figure 3-3 the voltage difference between the cascode node V_{cas} of the output current and the cascode device bias voltage V_{BIAS} is the gate to source voltage voltage $V_{GS_{M1}}$ of $M1$, where $\mid V_{GS_{M1}} \mid = \mid V_{BIAS} - V_{cas} \mid = \mid V_{THP} \mid + V_{DSAT}$. When V_{BIAS} drops below $V_{BIAS} - V_{DSAT}$, $\mid V_{GS_{M1}} \mid < \mid V_{THP} \mid$ and the cascode device is turning off.

Once the output voltage has been sampled on the load capacitor C_{TOT}, the current sources are turned off by switching off the cascode devices $M1, M3$ and $M7$ as shown on Figure 3-3 though switch $M12$ for the rest of the charge transfer phase. Subsequently, the current steering switches $M9, M10$ and $M11$ are turned off. Current steering separates the instant of current source turn-off from the start of the fine charge-transfer phase by providing a path for the current away from nodes v_{OUT}, v'_{OUT} and v''_{OUT}, while the current sources are being turned off. Therefore, the turn-off delay of the current source cascode devices does not affect the overshoot error and no longer impedes the start of the fine phase. Alternatively, when current source turn-off determines the output sampling at the end of the coarse phase the turn-off delay of the current sources delays the start of the fine phase and increases the coarse phase overshoot error.

The bottom plate switch $M5$ at the load capacitor C_{n+1} is not turned off until the end of the fine charge-transfer phase. At the end of the coarse phase as the current is steered away form C_{n+1}, the current through $M5$ drops as does the voltage across it. By the end of the fine phase, the opamp settles the coarse phase residual error exponentially and the current through M5 decreases exponentially. The voltage across M5 reduces proportionately to the current. The switch $M5$ can therefore be reduced in size in comparison to the bottom plate sampling switch used in single phase ZCB charge-transfer.

The current source devices $M2, M4, M8$ are biased such that their respective drain to source voltages are minimized to place the devices at the edge of the triode region as in the wide-swing cascode current mirror [2]. In this setup, $V_{cas} = V_{DD} - V_{DSAT}$, where V_{DSAT} is the saturation voltage of the current source devices. For $M9$ to steer away the current from $M1$, the resistance ($r_{on_{M9}}$) of the device in triode region has to satisfy $V_{DD} - \mid V_{THP} \mid - 2V_{DSAT} \leq I_1 r_{on_{M9}} < V_{DD} - 2V_{DSAT}$. For the above example this condition translates to three times the minimum size NMOS device with gate parasitic capacitance of $< 5fF$ in a $65nm$ CMOS process, two orders of magnitude smaller than the gate capacitance of the current source cascode devices in the above example of $0.4pF$. A small size steering switch reduces the capacitance loading the ZCD and thus improves the ZCD delay t_d and the output overshoot error.

The output of the ZCD generates two control signals: the first one is $ZCDout$ to turn on the current steering switches, the second one is $Pcas_{ctrl}$ to turn off the cascode current source devices as shown in Figure 3-3 and Figure 3-4. If the two signal path delays are matched the gate of $M1$ is pulled to V_{DD} as the drain of $M1$ is pulled to ground, turning off the device faster. The path delays, however, are not matched in order to minimize the total delay from the instant at which the virtual ground condition is satisfied to the output sampling instant. Reduced total delay minimizes the output overshoot error, reducing output non-linearity. The total parasitic capacitance at the gate of the cascode devices is large and can increase the

total delay if the paths are matched. Thus, the current steering switches are turned on first and the cascode devices and current sources are subsequently turned off.

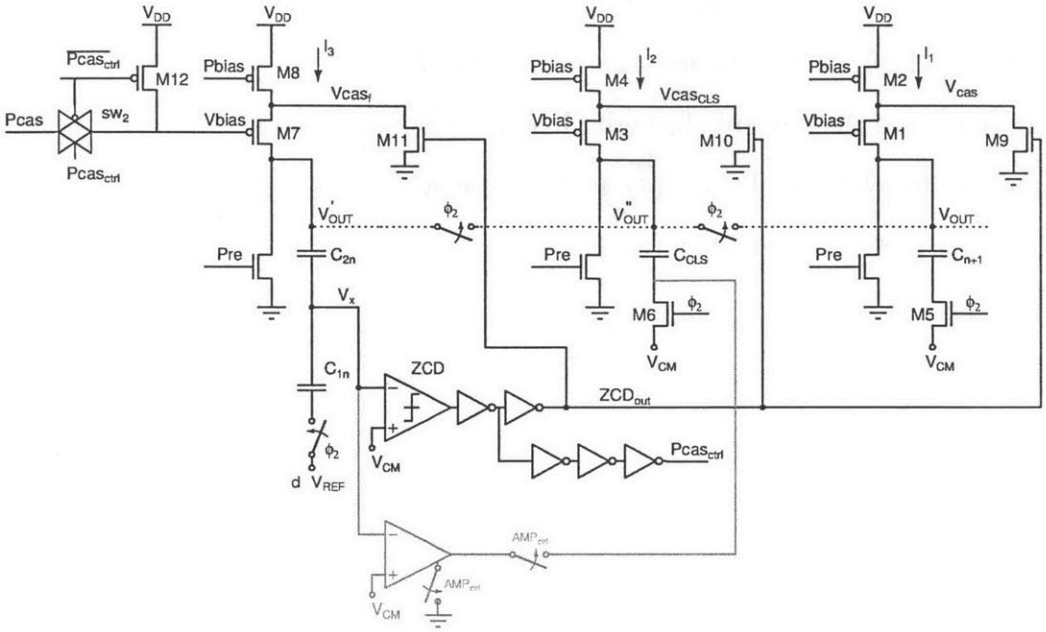


Figure 3-3: Coarse charge-transfer phase implementation of single-ended hybrid CLS-opamp/ZCB circuit, implementing an MDAC in a pipelined ADC stage. Current steering is used instead of bottom plate sampling to sample the output on capacitor C_{n+1}. The current sources comprised of $M1 - M4$ and $M7 - M8$ are turned off.

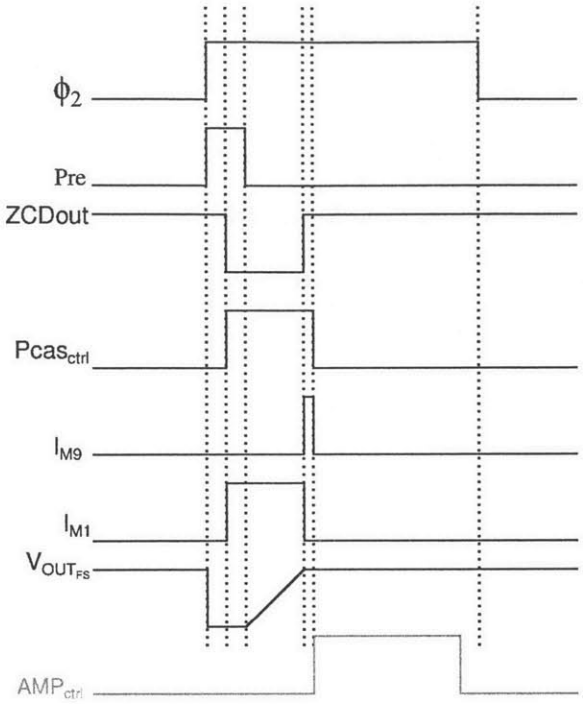


Figure 3-4: Timing diagram for the coarse charge-transfer phase (ϕ_2) of single-ended hybrid CLS-opamp/ZCB circuit, implementing an MDAC in a pipelined ADC stage.

3.2 Bidirectional Ramp ZCBC

3.2.1 Motivation

In ZCB switched-capacitor circuits, exponential output voltage settling is replaced by an output voltage ramp and a zero-crossing detector (ZCD). The ZCD determines the instant at which, the virtual ground condition is fulfilled, which would otherwise be forced by an opamp in feedback, in a conventional switched-capacitor circuit. A positive voltage ramp in a ZCBC is generated by a PMOS current source charging the circuit load capacitor. Alternatively a negative voltage ramp is generated by an NMOS current source discharging the load capacitor. To reduce ZCBC output voltage error, the current source is typically cascoded [14, 36, 6, 17, 9, 26] for improved output resistance. Larger current source output resistance implies smaller current variation and therefore smaller ramp variation with output voltage, which translates to reduced output-dependent error (due to a finite ZCD delay) for a fixed load capacitor. Thus,

cascoding is desired for better ZCB circuit output linearity.

The downside to cascoding is reduced voltage swing at the current source output. Reduced output swing is a disadvantage, especially in deep sub-micron technologies as shrinking supply voltages limit the available operating range of analog circuits. Both output swing and output linearity determine the attainable accuracy and SNR in the design of ZCB switched-capacitor circuits especially in deep-submicron technologies as explained below.

The signal-to-noise ratio (SNR) of a circuit is defined as the ratio of signal power to noise power [10]. For fixed SNR the output voltage range determines the allowed noise level in the circuit. Reduced output swing translates or lower SNR for fixed output noise. To reduce the noise level (assuming thermal noise is dominant), power consumption has to be increased. Therefore, in designing low power precision circuits, optimizing output voltage swing is important since it reduces power consumption. Next, the trade-off between output linearity, output swing and power dissipation is illustrated through an example.

At low supply voltages, in a fully-differential ZCB switched-capacitor circuit, cascode current sources at both differential outputs limit the linear output range to a fraction of the supply voltage (refer to Figure 3-5). The linear output range is defined here as the range of output voltages for which the NMOS and PMOS cascode devices, at the two differential outputs v_{OUTP} and v_{OUTN} respectively, are in saturation. For example, for an upper supply rail (V_{DD}) of $1V$ and current source device saturation voltage (V_{DSAT}) of 150mV (assuming it is the same for both the PMOS and NMOS devices), the available linear output range ($V_{OUT_{FS}}$), constrained by cascoding, is $V_{OUT_{FS}} = VDD - 2(2V_{DSAT}) = 400mV$. The effect of limited output voltage range is considered next for ZCBC in the context of pipelined ADCs.

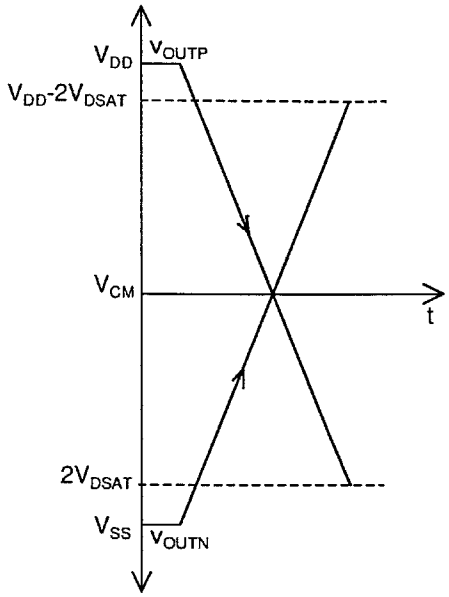


Figure 3-5: Linear output voltage range of a fully-differential ZCB switched-capacitor circuit, limited by the use of cascoded current sources. The lower bound is set by the minimum voltage required to keep the NMOS current source devices in saturation, $2V_{DSAT}$, while the upper bound is set by the minimum voltage drop from the upper rail, at which the PMOS current source devices are in saturation, $V_{DD} - 2V_{DSAT}$.

The output voltage of a pipelined ADC stage can go out of range due to errors, such as stage offsets, BDC offsets, amplification gain error and capacitor mismatch, of which BDC offsets typically dominate. Over-range protection or redundancy is typically implemented to mitigate the effect of stage errors on the ADC transfer function [27]. In the absence of over-range protection, the output of a pipeline stage can exceed the input range of the subsequent stage. This results in missing codes in the ADC transfer function, near the stage bit decision boundaries as is discussed in more detail in [6]. The use of over-range protection results in a reduced available output swing for the pipelined ADC stage. In the typical use of redundancy, the nominal output range sets the value of the reference voltages. The reference voltages in turn set the input voltage. Thus the output voltage range limits the input range especially in deep sub-micron technologies.

Suppose that a pipelined ADC stage has a gain of 4 and worst case input-referred BDC offset of $\pm 20mV$ (it is assumed that the BDC offset dominates the other sources

of offset in the circuit). This causes the output to exceed the nominal range by $V_{OVERR} = \pm 80mV$. Therefore this amount of extra swing needs to be accommodated at the stage output. If the pipelined ADC stage is implemented using a ZCB switched-capacitor circuit and minimum output margin from the rails is assumed, the combined effect of cascoding and this extra output swing both constrain the nominal output range of the circuit. Using the examples above, for a current source device saturation voltage (V_{DSAT}) of $160mV$ and output-referred BDC offset of $\pm 80mV$, the nominal full scale output range of the pipeline stage is $V_{OUT_{FS_n}} = V_{DD} - 2(2V_{DSAT}) - 2 \mid V_{OVERR} \mid = 200mV$. Thus if redundancy is implemented the stage input is limited to $200mV$.

On the other hand, consider the case of a pipeline stage, using a fully-differential ZCB implementation, in which the ramp current sources are not cascoded. Using a current source without cascoding results in a reduction of ZCBC output voltage linearity by the intrinsic gain of the cascode current source device and limits the attainable accuracy at the output of the stage. The output voltage range is then $V_{OUT_{FS}} = V_{DD} - 2V_{DSAT} = 680mV$. Assuming the same output error margin from either rail voltage, as in the example above, of $\pm 80mV$, the nominal output range is $V_{OUT_{FS_n}} = V_{DD} - 2V_{DSAT} - 2 \mid V_{OVERR} \mid = 520mV$. The decrease in output voltage range due to cascoding results in SNR degradation by a factor of $(\frac{560mV}{200mV})^2 = 6.7$. To maintain the SNR when using cascoding, the noise power should decrease by a factor of $(6.7)^2$. If only thermal noise is considered, a decrease in thermal noise power by a factor of $(6.7)^2$ requires an increase in the size of the input sampling capacitors by $(6.7)^2$ and a proportional increase in ramp current and power dissipation. Therefore, for fixed ADC sampling rate, higher operating output voltage range improves the power efficiency of the ADC, especially in high resolution, high speed implementations. While it requires little additional power to improve current source output resistance, and therefore output linearity, cascoding diminishes the overall power efficiency of ZCB switched-capacitor circuits due to the reduced current source output

voltage swing. It is therefore desirable to develop new techniques which improve current source output resistance without trading off output range and power efficiency.

In [24], a ramp generator is described, which uses feedback to linearize the ramp, without limiting output swing. A low voltage, power efficient implementation of the ramp generator is described in [17]. The ramp generator does improve the output linearity, without limiting the available output range of ZCBC and is dynamic (it does not draw static power) and therefore power efficient. However, at higher ramp rates the time constant of the circuit can become comparable to the ramp duration, which results in nonlinearity error at the output, as the circuit does not have enough time to settle to the desired accuracy. It can therefore be difficult to maintain power efficiency at higher switched-capacitor circuit precision and speed.

A method is presented below to improve the output range to near full rail, while allowing output swing room for cascoding and not compromising the linearity of the stage.

3.2.2 Concept

In previous ZCB implementations [15, 5, 17, 20], a unidirectional voltage ramp is generated at the output voltage node for all inputs to the switched-capacitor circuit. The output ramp direction is fixed through the use of fixed preset voltage (typically V_{DD} or V_{SS}) during the preset phase and fixed current source (NMOS or PMOS) during the charge-transfer phase. For simplicity, a single-ended ZCB circuit output voltage ramp is shown in Figure 3-6. The output voltage is preset to one of the rails at the beginning of every charge transfer phase ϕ_2 of the clock. Suppose the output is preset to the negative rail (V_{SS} in Figure 3-6). Next a PMOS current source charges the capacitors to generate a positive going ramp at the ZCB circuit output v_{OUT}. Alternatively, if the output is preset to the positive rail V_{DD}, an NMOS current source charges the capacitors to generate a negative going ramp. A fixed preset voltage and type of current source are used in unidirectional single-ended ZCBC independent of

input voltage [4, 15].

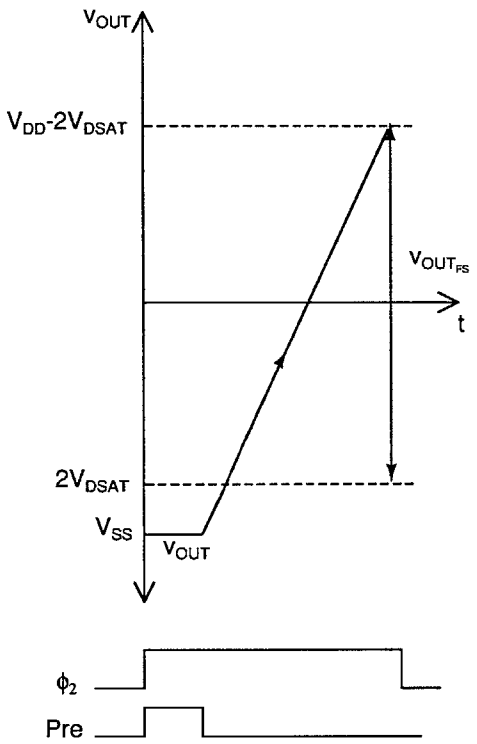


Figure 3-6: Output voltage ramp for single-ended unidirectional ramp ZCB circuit, implemented with a preset voltage V_{SS} and a cascode PMOS current source. The voltage $V_{OUT_{FS}}$ represents the full-swing output voltage range.

In a fully-differential ZCB implementation (refer to Figure 3-5) the positive (v_{OUTP}) and negative (v_{OUT}) outputs are each preset to the opposite rails, V_{SS} and V_{DD}, and corresponding complementary current sources $NMOS$ and $PMOS$ are used during the charge-transfer phase ϕ_2 at each output node respectively [9, 26, 6]. However, for either the v_{OUTP} or v_{OUTN} output voltages, the preset voltage and current source are fixed and therefore the output ramp is unidirectional at either output independent of input voltage polarity.

Next the linear operating voltage range for NMOS and PMOS cascode current sources are considered to gain insight into how the output swing of ZCBC can be extended, while taking advantage of cascoding as a power efficient way to boost their output linearity.

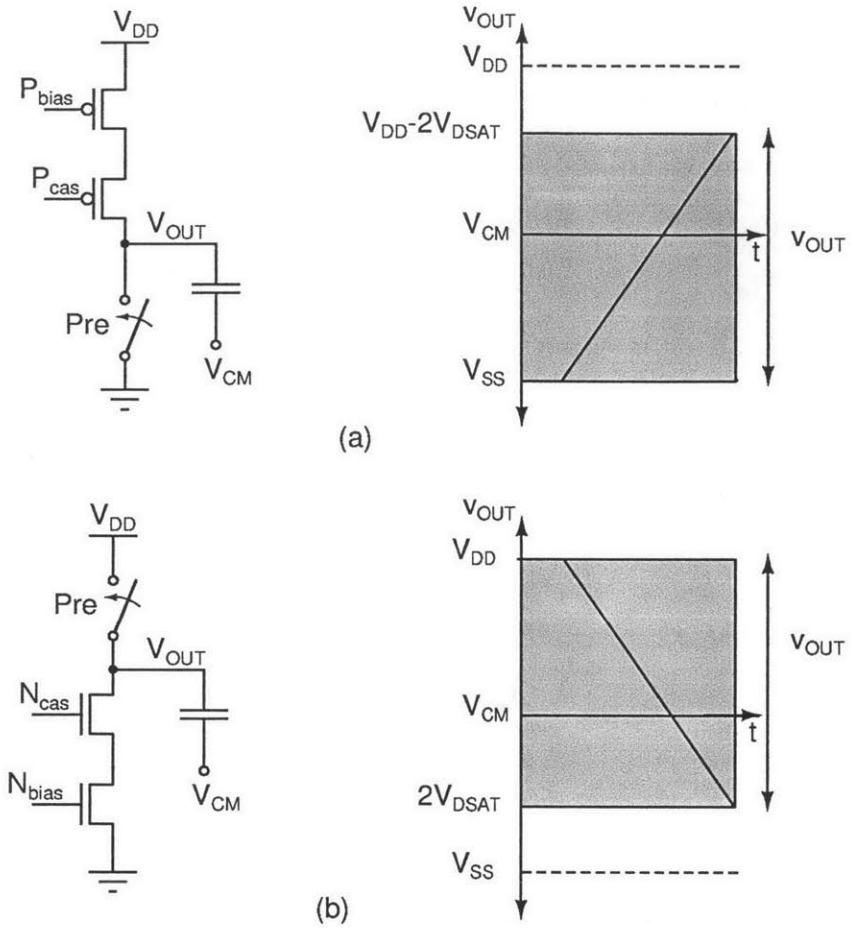


Figure 3-7: Linear operating output voltage range for cascode PMOS (a) and cascode NMOS (b) current source in a ZCB output ramp generation circuit implementation.

A cascode PMOS current source has a linear output voltage range of $[V_{SS}, V_{DD} - 2V_{DSAT}]$ as shown in Figure 3-7, while a cascode NMOS current source has a linear output voltage range of $[2V_{DSAT}, V_{DD}]$. In unidirectional single-ended ZCBC the full-swing output is defined by the overlap, of the linear range of the PMOS and NMOS current sources, which is $[2V_{DSAT}, V_{DD} - 2V_{DSAT}]$ (refer to Figure 3-8(b)). However, a different approach to defining the ZCBC full-swing output range can be taken. Note that the linear operating ranges of both types of current sources combine to a full scale output range. An NMOS cascode current source can be used to generate an output ramp only for output voltages from V_{CM} to V_{DD}, where V_{CM} is the mid-rail voltage (refer to Figure 3-8(a)). Alternatively a PMOS current source can be used to generate an output ramp only for output voltages from V_{SS} to V_{CM}. The

complementary current sources thus generate voltage ramps at the output node of the ZCB switched-capacitor circuit, which cover complementary ranges of output voltages to combine for a full rail to rail output swing. Instead of the overlap, the union of the linear output ranges of both current source types can be thus defined as the ZCBC output range. Therefore the use of both current sources at the output node v_{OUT} in a ZCB switched-capacitor circuit extends its output range to full rail.

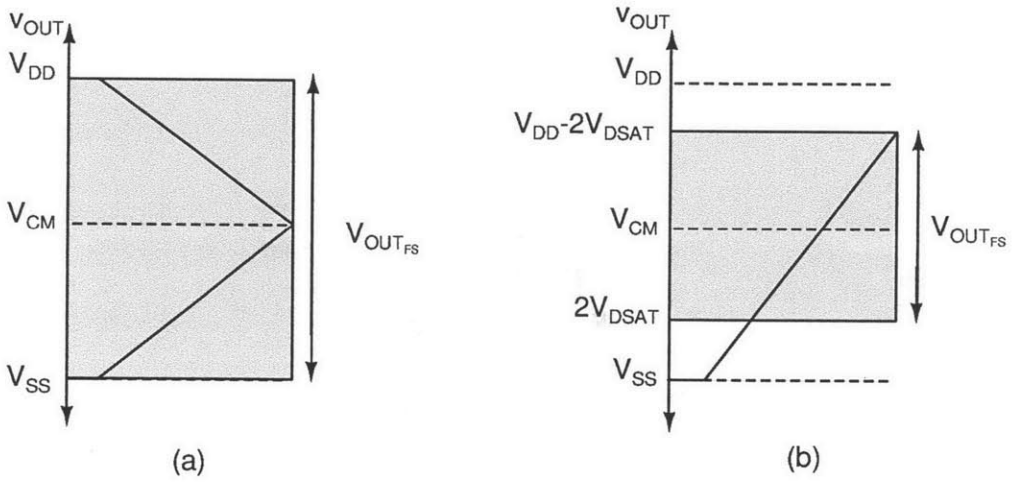


Figure 3-8: Linear output range $V_{OUT_{FS}}$ for single-ended (a) bidirectional ramp ZCBC and (b) unidirectional ramp ZCBC

3.2.3 Practical Implementation

In a fully-differential ZCB implementation, both types of current sources are present at each of the differential outputs (v_{OUTP} and v_{OUTN}) as shown in Figure 3-9. The presence of both types of current sources at either output provides the capacity to generate output ramps of opposite polarity, making the ZCB circuit bidirectional with respect to its output ramp. Only one type of current source (NMOS or PMOS) is enabled for any input range. The activated current source, during the charge-transfer clock phase ϕ_2, generates an output voltage ramp, sweeping only half of the output range: from V_{DD} to VCM, for an NMOS current source or from V_{SS} to V_{CM} for a PMOS current source respectively. To determine the appropriate current source and preset voltage to be selected, before the beginning of ϕ_2 for every clock cycle, it is

necessary to establish if the output voltage falls within the range of voltages form V_{DD} to V_{CM} or V_{SS} to V_{CM}. The decision to determine which half of the output range the output belongs to can be made by a single comparator at the input at the end of the sampling phase ϕ_1, for a fixed input. In a pipeline ADC stage $n+1$ additional comparators are required where n is the number of stage BDCs.

In the context of a ZCB pipelined ADC stage, an additional bit (refer to Figure 3-9) must be resolved by the sub-ADC of the stage to establish if $V_{OUTP} > V_{CM}$ and $v_{OUTN} < V_{CM}$ or $v_{OUTP} < V_{CM}$ and $v_{OUTN} > V_{CM}$ for a fixed input. Based on the additional bit, defined as an output-sign bit, the respective preset voltage and current source are enabled during ϕ_2. The sub-ADC of the pipeline stage resolves the output-sign bit to be 1 in Figure 3-9, which corresponds to a positive output voltage $v_{OUTP} > V_{CM}$ and a negative output voltage $v_{OUTN} < V_{CM}$.

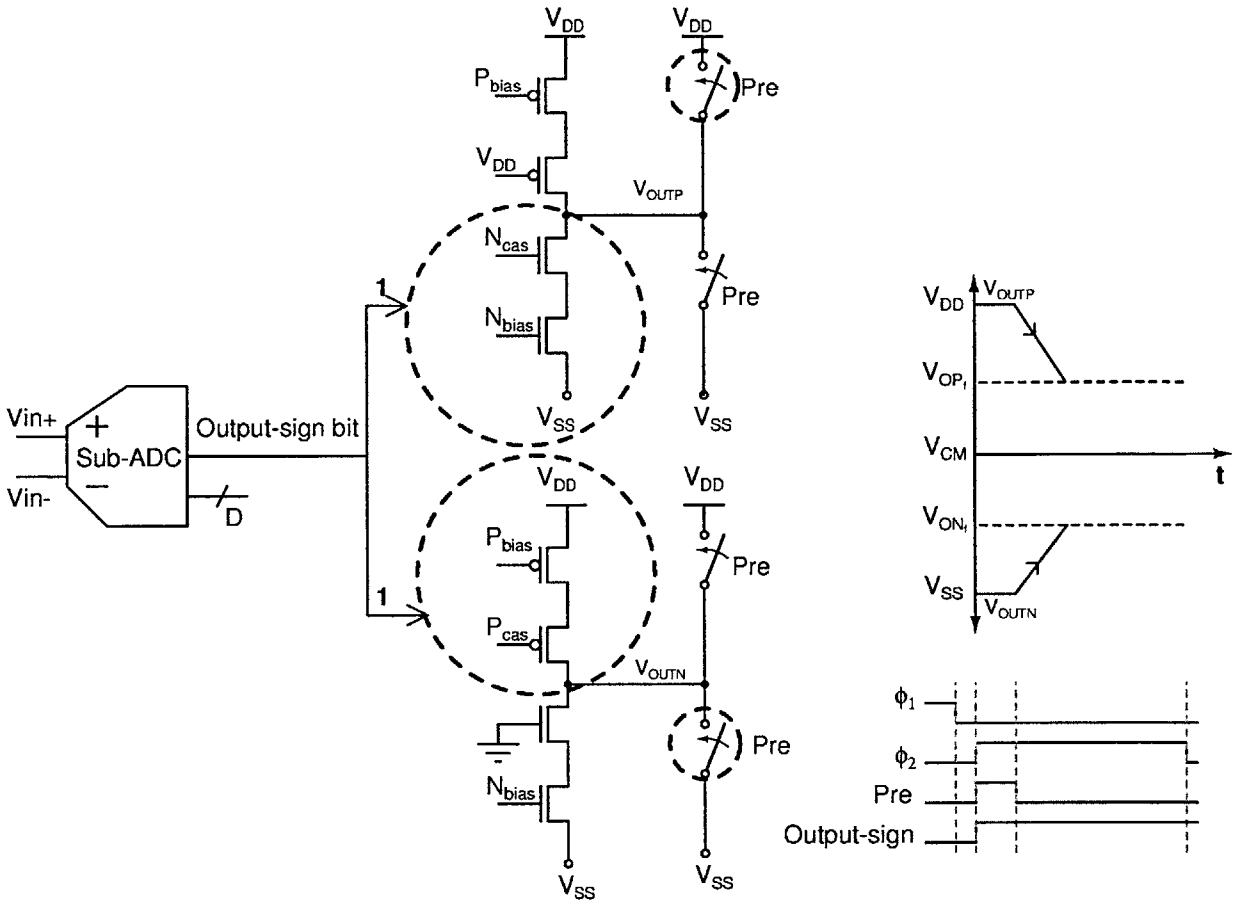


Figure 3-9: Fully-differential bidirectional ramp ZCB implementation used in a pipelined ADC. The output sign bit is resolved to be 1, which corresponds to $v_{OUTP} > VCM$, and $V_{OUTN} < VCM$.

In Figure 3-9, during the preset phase *Pre*, if the positive output V_{OUTP} is preset to V_{DD}, the negative output V_{OUTN} is preset to V_{SS}. The NMOS current source is enabled at v_{OUTP} and generates a negative going output ramp by discharging the output from V_{DD} to the final output voltage value V_{OP_f}. The PMOS current source is enabled at v_{OUTN} and generates a positive output ramp by charging the output from V_{SS} to the final output voltage value V_{ON_f}.

If the output sign bit is incorrect due to offset in the output-sign bit decision comparator, the selected preset voltage and current source pair is also incorrect. In the case of an incorrect output sign bit if the offset error of the output-sign BDC is positive,the output ramp exceeds half of the output operating range. This, however, does not interfere with the function of the circuit as long as the outputs are within

$2V_{DSAT}$ from either rail. An incorrect output-sign bit decision is more likely for inputs around the sign bit decision boundary V_{CM}, corresponding to outputs close to V_{CM} (Figure 3-10).

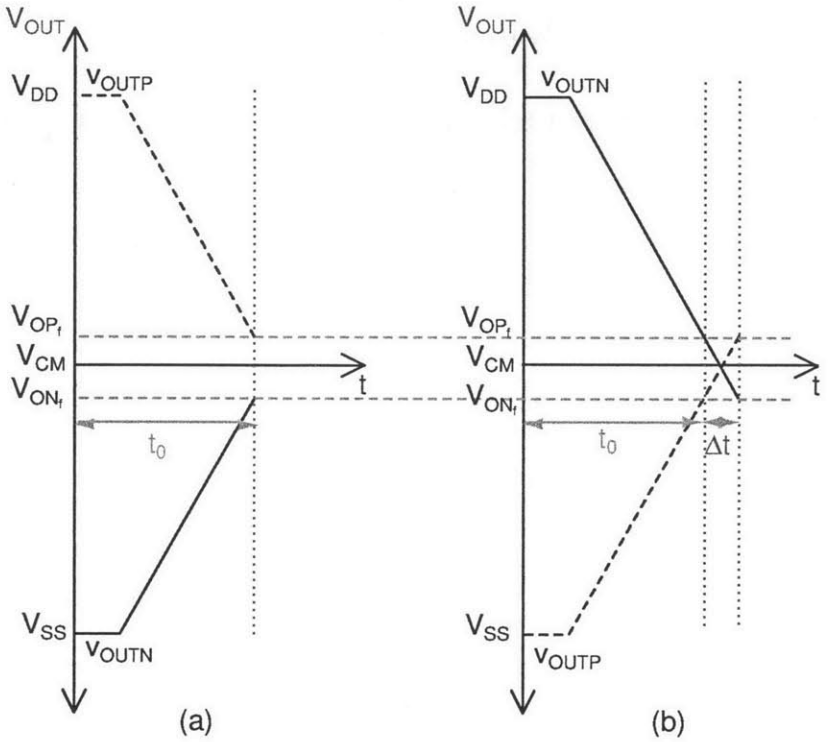


Figure 3-10: Fully-differential bidirectional output ramp operation in the case of (a) correct output sign bit decision and (b) incorrect output sign bit decision. If the output final values V_{OP_f} and V_{ON_f} are close to V_{CM}, the time it takes the output voltages to reach their respective final values under both conditions is t_0 and $t_0 + \Delta t$, where Δt is small.

3.2.4 Advantages and Disadvantages

The main advantage of the bidirectional ramp technique is that it increases the available output swing effectively to full rail.

Another advantage is reduced ramp current and consequently power dissipation in the current sources by a factor of 2 in comparison to a unidirectional ramp ZCB implementation, for fixed ramp rate and fixed output swing $V_{OUT_{FS}} = V_{0_{MAX}} - V_{0_{MIN}}$ (where $V_{0_{MAX}}$ is the maximum output voltage and $V_{0_{MIN}}$ is the minimum output voltage). Suppose that in a single-ended unidirectional ramp ZCB circuit, the ramp duration for $V_{OUT_{FS}}$ is $t_{ramp} = t_{max} - t_{min}$, where t_{min} is the ramp duration for $V_{0_{MIN}}$

and t_{max} is the ramp duration for $V_{0_{MAX}}$. Then the full swing output voltage $V_{OUT_{FS}}$ can be expressed as :

$$V_{OUT_{FS}} = \frac{I_{uni} t_{ramp}}{C} \tag{3.10}$$

where C is the current source load capacitor and I_{uni} is the unidirectional ramp current. In a bidirectional ramp ZCB circuit, for the same ramp rate as in the unidirectional case, the output voltage swing for either the PMOS or NMOS current source is $\frac{V_{FS}}{2}$ and can be expressed as:

$$\frac{V_{OUT_{FS}}}{2} = \frac{I_{bi} t_{ramp}}{C} \tag{3.11}$$

where I_{bi} is the bidirectional ramp current and t_{ramp} is the same if the ramp rate is assumed to be fixed in both cases for a fixed load C. From Eq. 3.10 and Eq. 3.11, it follows that

$$I_{bi} = \frac{I_{uni}}{2}. \tag{3.12}$$

Alternatively at the same ramp rate, the bidirectional approach yields faster operation. Figure 3-11 illustrates this point through a comparison of the outputs of fully-differential bidirectional and unidirectional ramp ZCBC. First the unidirectional output ramp implementation is considered. For output values $V_{OP_f} > VCM$ and $V_{ON_f} < VCM$ (in this particular example $V_{OP_f} = \frac{3}{4}V_{DD}$ and $V_{ON_f} = \frac{1}{4}V_{DD}$), the output voltages v_{OUTP} and v_{OUTN} ramp down or up respectively through the entire output voltage range until they reach their final values v_{OP_f} and v_{ON_f}. In the bidirectional case the output polarity is predicted by the output-sign bit and nodes v_{OUTP} and v_{OUTN} are preset to the rail voltages closest to their respective final output voltage values V_{OP_f} and V_{ON_f} (in this example V_{DD} for V_{OP_f} and V_{SS} for V_{ON_f}). Note that for $V_{OP_f} < VCM$ and $V_{ON_f} > VCM$, the unidirectional and bidirectional ramp ZCB implementations are equivalent. In addition to reducing ramp current and consequently power dissipation by a factor of 2 for a fixed ramp rate and fixed output swing

$V_{OUT_{FS}} = V_{0_{MAX}} - V_{0_{MIN}}$, the magnitude of the output-dependent overshoot error is reduced compared to unidirectional ramp ZCBC for a fixed output swing. However, as the polarity of the total output overshoot error is no longer output-independent, the linearity of the stage is not improved over a unidirectional implementation as will be discussed next.

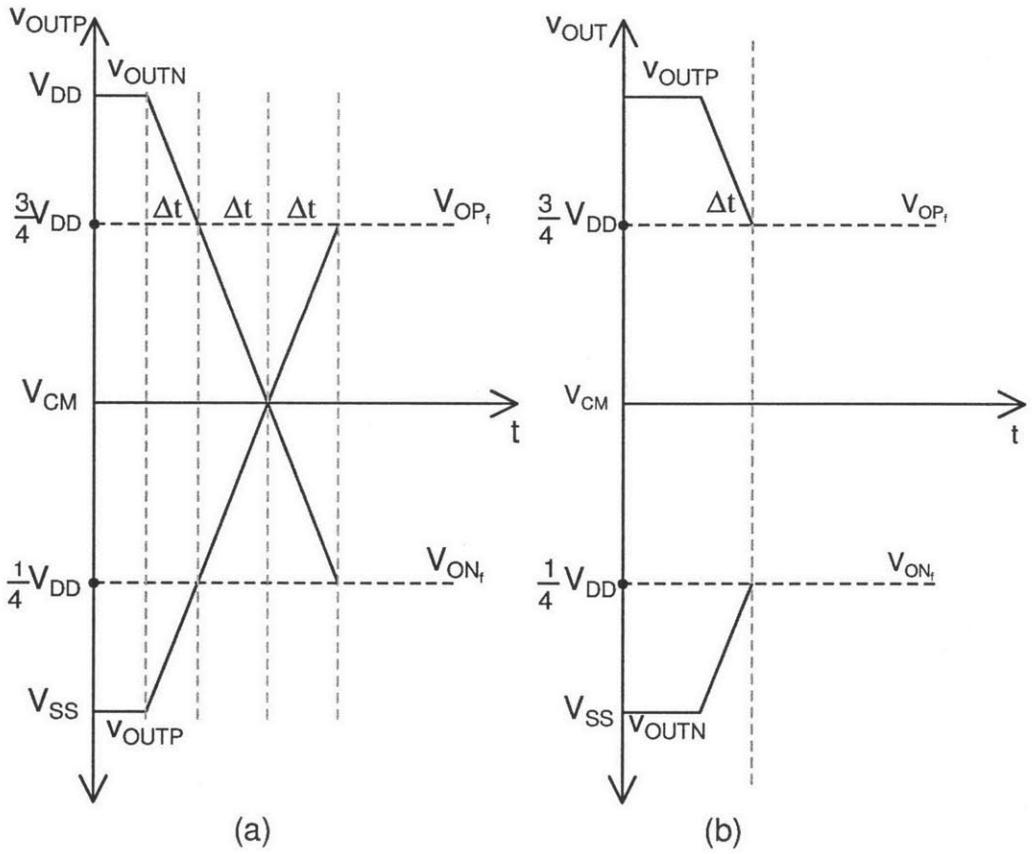


Figure 3-11: Fully-differential ZCB (a) unidirectional output ramp implementation vs (b) bidirectional output ramp implementation for the case of output voltage values, $V_{OP_f} = \frac{3}{4}V_{DD} > VCM$ and $V_{ON_f} = \frac{1}{4}V_{DD} < VCM$.

The main disadvantage of the bidirectional ramp ZCBC implementation is the output-sign bit dependent overshoot error, which will be considered next.

3.2.4.1 Bidirectional Ramp ZCBC Output Error

In unidirectional ZCBC the overshoot voltage error as a function of the ZCBC ideal output voltage v_O and the ZCD delay t_d can be expressed by the overshoot component of Eq. 2.14 in 2 repeated here for convenience:

$$v_{ov}(v_O(t), t_d) = \frac{I_0}{C} t_d - \frac{v_O(t) t_d}{R_O C} - \frac{I_0 t_d^2}{2 R_O C^2} \tag{3.13}$$

One important difference in a bidirectional ramp ZCBC is that the ramp rate changes sign with the output-sign bit. If $v_{OUT} > VCM$, the ramp rate is negative, if $v_{OUT} < VCM$, the ramp rate is positive. The output overshoot voltage error for a single ended design is then (the second order dependence on t_d is not included for simplicity):

$$v_{OV}(v_0(t), t_d) = \begin{cases} t_d \left(\frac{I_{0P}}{C_{TOT}} \right) - t_d \left(\frac{v_O(t)}{C R_P} \right), & v_{OUT} < VCM \\ - \left(t_d \left(\frac{I_{0N}}{C_{TOT}} \right) - t_d \left(\frac{v_O(t)}{C R_N} \right) \right), & v_{OUT} > VCM \end{cases} \tag{3.14}$$

where I_{0P} and R_P are the ideal current and current source output resistance of the PMOS current source and I_{0N} and R_N are the respective ones for the NMOS current source. The currents I_{0P} and I_{0N} represent differences from I_0 in the PMOS and NMOS current sources. It is clear from Eq. 3.14 that the output-independent components in Eq. 3.13 are no longer output independent but depend on the output polarity.

In a fully-differential, both unidirectional and bidirectional ZCBCs, the errors from both types of current sources at the positive and negative outputs are present and add up regardless of the output. The magnitude of the error is the same for both:

$$\mid v_{OV_{diff}}(v_O(t), t_d) \mid = \mid t_d \left(\frac{I_{0P}}{C} + \frac{I_{0N}}{C} \right) - t_d \left(\frac{v_O(t)}{C R_P} + \frac{v_O(t)}{C R_N} \right) \mid,$$

In terms of sign, however, with change in direction the output ramp sign changes and so does the error in the bidirectional case. The sign error change for a bidirectional case with fully-differential outputs v_{OUTP} and v_{OUTN} is expressed in Eq. 8 below:

$$v_{O_{diff}}(v_O(t), t_d) = \begin{cases} t_d\left(\frac{I_{0P}}{C} + \frac{I_{0N}}{C}\right) - t_d\left(\frac{v_O(t)}{CR_P} + \frac{v_O(t)}{CR_N}\right), & v_{OUTP} < VCM \\ -t_d\left(\frac{I_{0N}}{C} + \frac{I_{0P}}{C}\right) + t_d\left(\frac{v_O(t)}{CR_P} + \frac{v_O(t)}{CR_N}\right), & v_{OUTP} > VCM \end{cases} \quad (3.15)$$

Thus in addition to the INL and DNL errors present at the BDC transitions in an ADC pipeline stage, a bidirectional ZCB stage introduces DNL and INL errors at the transition of the output-sign bit in the middle of the output range between every BDC transition.

The error component in Eq. 8 $\pm t_d\left(\frac{I_{0P}}{C} + \frac{I_{0N}}{C}\right)$ changes polarity only but not its magnitude as the output changes for a constant ZCD delay t_d and can be removed through constant overshoot correction which is described in detail in the next section of this chapter. However, any variation in the delay with output voltage will result in an output nonlinearity error at the output-sign bit transition.

The output dependent error in Eq. 8 $\pm t_d\left(\frac{v_O(t)}{CR_P} + \frac{v_O(t)}{CR_N}\right)$ is attenuated by the second phase in a two phase pipeline ADC stage. In a hybrid CLS-OpAmp/ZCB implementation the error is attenuated by the loop gain of the opamp in feedback.

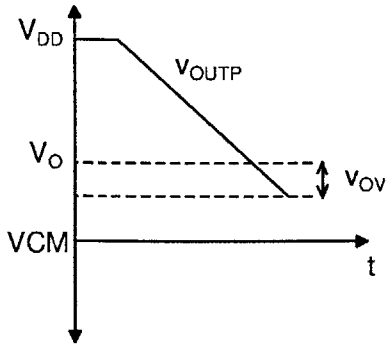
Recall from Chapter 2 that the output voltage of a hybrid CLS-OpAmp/ZCB based pipeline stage is:

$$v_{OUT}(t) = v_O + v_{ov}\left(\frac{1}{1 + A\beta\gamma} + \frac{A\beta\gamma}{1 + A\beta\gamma} e^{-\frac{t(1+A\beta\gamma)}{\tau}}\right), \quad (3.16)$$

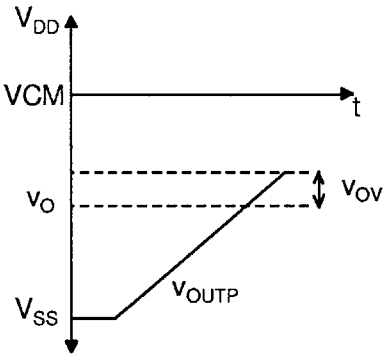
where v_O is the ideal output voltage, A is the DC gain of the opamp, τ is the open loop opamp time constant and γ is the attenuation factor from the opamp output voltage v_{amp} to the stage output v_{out} (refer to Figure 3-13 and Figure 3-14). The output error of the pipeline stage is the second term of equation 3.16. The bidirectional ramp ZCB coarse phase results in change in polarity with the output-sign bit:

$$v_{OUT}(t) = \begin{cases} v_O + v_{ov}(\frac{1}{1+A\beta\gamma} + \frac{A\beta\gamma}{1+A\beta\gamma}e^{-\frac{t(1+A\beta\gamma)}{\tau}}), & v_{OUT} < V_{CM} \\ v_O - v_{ov}(\frac{1}{1+A\beta\gamma} + \frac{A\beta\gamma}{1+A\beta\gamma}e^{-\frac{t(1+A\beta\gamma)}{\tau}}), & v_{OUT} > V_{CM} \end{cases}, \quad (3.17)$$

where V_{CM} is the mid-rail voltage. If the output voltage is less than V_{CM}, the output-sign bit by design is high. In this case during the coarse phase, the output is preset to V_{DD} and discharged by an NMOS current source, resulting in a negative overshoot error (refer to Figure 3-12a) at the ZCD transition. If the output voltage is larger than V_{CM}, the output-sign bit is low and during the coarse phase, the output is preset to V_{SS} and and charged by a PMOS current source, resulting in a positive overshoot error (refer to Figure 3-12b) at the ZCD transition. From Eq. 3.17, the overshoot error is attenuated both by the loop gain $H(s) = A\alpha\gamma$ and settled by the opamp in feedback for the duration of the fine phase. Figure 3-13 and Figure 3-14 show the waveforms at opamp input node v_X, the opamp output v_{AMP} and the output voltage v_{OUT} for an output-sign bit low and high respectively. If the output settles to the desired accuracy at the end of the fine phase and the loop gain is large enough the change in polarity of the output error does not limit the INL and DNL of the ADC. However, if the output does not settle to the desired accuracy or the loop gain is not large enough the output-sign change results in INL and DNL error in the mid-region between the stage bit decision transitions.



(a) Overshoot error when the output-sign bit is low, $v_{OUTP} > VCM$. The voltage v_O is the ideal output voltage. The overshoot error $v_{OV} < 0$.



(b) Overshoot error when the output-sign bit high, $v_{OUTP} < VCM$. The voltage v_O is the ideal output voltage. The overshoot error $v_{OV} > 0$

Figure 3-12: Overshoot error in single-ended bidirectional ZCBCs

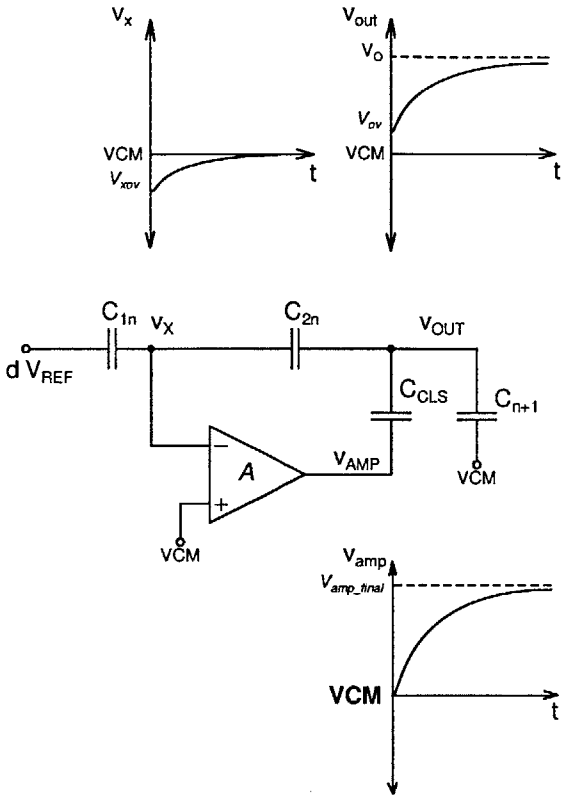


Figure 3-13: Fine phase correction of the error of a coarse phase bidirectional ZCB implementation when the output-sign bit is low in a single-ended hybrid CLS-OpAmp/ZCB pipeline stage. The output is settled to v_O which is the ideal final value of the output if the gain of the opamp A is infinite. The input to the opamp is settled to V_{CM}.

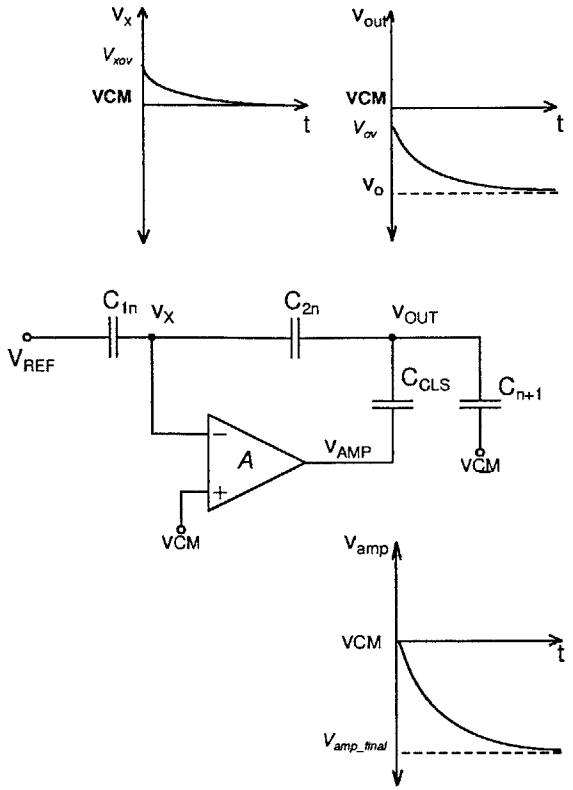


Figure 3-14: Fine phase correction of the error of a coarse phase bidirectional ZCB implementation when the output-sign bit is high in a single-ended hybrid CLS-OpAmp/ZCB pipeline stage. The output is settled to v_O which is the ideal final value of the output if the gain of the opamp A is infinite. The input to the opamp is settled to V_{CM}.

3.2.4.2 Number of BDCs in a bidirectional ZCB pipelined ADC

Another disadvantage of the bidirectional ramp generation is the added complexity of predicting the value of the output voltage with respect to V_{CM} every clock cycle. In the context of a pipelined ADC, the number of BDCs (n), compared to a conventional pipelined ADC stage, roughly doubles to $2n + 1$ in order to generate the output-sign bit.

In a pipelined ADC stage no redundancy is used when $log_2(n + 1) = k$, where n is the number of BDCs, and $G = 2^k$ is the gain of the stage. If $log_2(n + 1) > k$, redundancy is used. Conventionally one additional BDC is sufficient to introduce redundancy and the number of BDCs is $m = n + 1$. In the typical case the reference voltages are set as the minimum and maximum values of the nominal output range

of the stage and the the input to the stage is set by the references. Thus typically the output range limits the input range. In [6] increased number of BDCs and reference voltage scaling to full rail are used to extend the input range, for a limited output range. From [6] the input range can be increased by a factor of $x_{in} = \frac{n+1}{G}$ if the reference voltages are scaled by $x_{ref} = \frac{n}{G-1}$. In [6] $V_{DD} = 1.2V$, the single-ended output range is $V_{OUT_{FS}} = 0.4V$ and $G = 4$, then $x_{ref} = \frac{1.2V}{0.4V} = 3$ and it follows that $n = x_{ref}(G-1) = 9$. The single-ended input range is extended by $x_{in} = \frac{9+1}{4} = 2.5$ from $0.4V$ to $1V$. If the same technique is applied to this work, and the bidirectional ramp technique is not used for $V_{DD} = 1V$, for a single-ended output range of $V_{OUT_{FS}} = 0.2V$ (refer to Subsection 3.2.1) and $G = 4$, $x_{ref} = \frac{1V}{0.2V} = 5$. It follows that $n = x_{ref}(G-1) = 15$.

The stage output voltage is effectively full rail when using bidirectional ramp ZCB coarse phase. The references are set at $V_{REFP} = 1V$ and $V_{REFM} = 0V$ with $V_{CM} = 0.5V$. If no redundancy is used for $n = 3$, $k = 2$ and $G = 4$ the fully differential input range is $2V$, however there is no over-range protection for BDC offset errors. If one additional BDC is used for redundancy $n = 4$, and the references are kept the same, the output voltage is $0.75V$ which leaves $\pm 125mV$ from either rail for over-range protection. From $x_{in} = \frac{n+1}{G}$, it follows that the fully differential input is scaled down from $2V$ to $1.6V$. In this design $n = 6$ was chosen for slightly larger fully differential input range of $1.75V$, as the input range limits the attainable ADC SNR. For $n = 6$, the over-range protection from either rail is $\pm 250mV$. In both cases of $n = 4$ and $n = 6$, the total number of BDCs including the output-sign BDCs is $2n + 1 = 9$, and $2n + 1 = 13$ respectively and is smaller than 15.

3.3 Output Offset Error Correction in ZCBC

In an ZCB switched-capacitor circuit implementation, the current sources have infinite output impedance and the zero crossing detector (ZCD) has an infinitely fast response or zero delay. In Chapter 2 the output overshoot error for single ramp ZCB circuit is derived for a non-ideal current source of output impedance R_O and constant current

value I_0 and a finite ZCD delay t_d is derived as a function of the ideal output voltage v_O and t_d. The output overshoot error is stated here again for convenience:

$$v_{OV}(v_{OUT}(t), t_d) = \frac{I_0}{C} t_d - \frac{v_O(t) t_d}{R_O C} \tag{3.18}$$

where C is the load capacitor in the circuit. The focus of this section is on the output independent term $V_{OV} = \frac{I_0}{C} t_d$ of Eq. 3.18. For the purpose of this section, it is assumed that the variation of the finite ZCD delay is negligible. Thus the linear term Eq. 3.18 appears as a constant offset at the output, regardless of the input voltage to the ZCB circuit. Referred to the input, the error is indistinguishable from the offset of the ZCD and a correction mechanism is presented for canceling it.

3.3.1 Motivation

- The need for output offset correction in **single phase** ZCBC [5, 9, 26] is not as stringent as in their two-phase counterparts. The constant overshoot error can be viewed as an offset at the switched-capacitor circuit output and does not interfere with the operation and linearity of the circuit if the output range of operation is unlimited. At scaled supply voltages in modern technologies, however, the output swing is limited. In pipelined ADCs, the output offset error requires an increase in the stage over-range protection range and thus limits further the available ZCBC output range. ZCB pipeline stages inherently do not have a common mode feedback mechanism and the output error accrues with every subsequent stage and eventually can cause the later stages to go out of their linear range of operation, hence the need for error correction.

- In **a dual ramp** ZCBC, the attainable fine phase output linearity is proportional to the coarse phase error. Output offset error correction lessens the power consumption and design requirements of the fine phase implementation and is thus essential to a power-efficient design.

- If the **bidirectional ramp** technique, described in 3.2, is used with **either a single or dual phase** ZCBC, the change in polarity of the output ramp for $v_{OUT} > VCM$ and $v_{OUT} < VCM$ results in polarity change of the overshoot error. It follows that the overshoot error, which is output invariant in the conventional ZCB implementation is no longer independent of the output voltage. It no longer appears as a constant offset at the output but as a voltage, which changes polarity with the output-sign bit. The output-sign bit determines the switch in ramp direction based on the input.

3.3.2 Error Correction

Output offset error correction can be implemented both at the ZCB circuit input or output as demonstrated in [6, 26, 36, 20]. In [20], an externally controlled capacitor digital-to-analog converter (DAC) is implemented at the ZCB circuit output. Input error correction can be realized by introducing an offset of the same magnitude and opposite polarity as the input referred overshoot error [6, 26, 36]. The latter approach is chosen for this particular design.

An input correction offset voltage can be introduced directly at the input or internally to the ZCD circuit. The particular ZCD implementation in [9, 26, 5] lends itself to a programmable offset implementation through the load of the ZCD preamplifier - an approach, which does not incur additional complexity and is power-efficient. If the ZCD topology precludes internal offset generation, a more general method is to apply a correction voltage V_{corr} via a capacitor at node v_X of the ZCB circuit as shown in Figure 3-15.

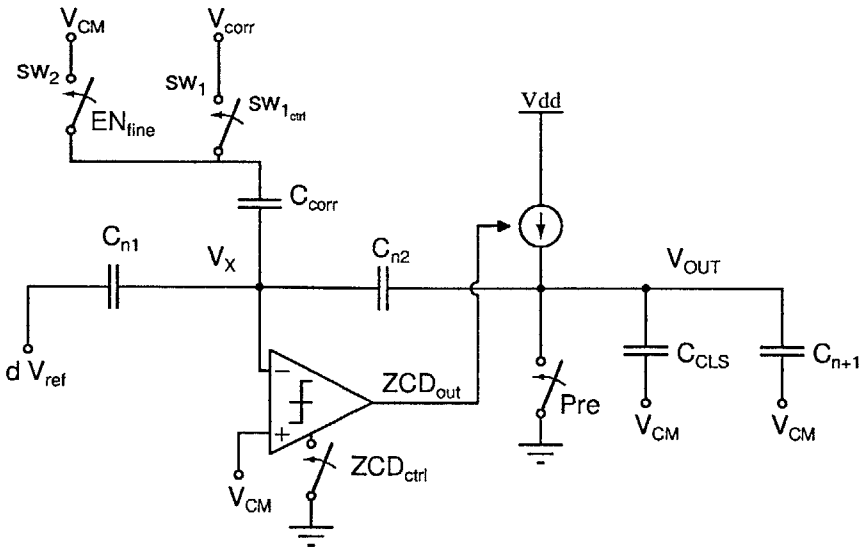


Figure 3-15: Overshoot correction implementation

A downside to adding an additional capacitor at the v_X node is increased thermal noise at the ZCB circuit output v_{OUT}. The size of the capacitor C_{corr} therefore has to be minimized, compared to the size of capacitors C_{1n} and C_{2n} and allow room for other parasitic capacitors due to the ZCD inputs for example at node v_X.

A comparison between the final voltages $v_{OUT_{corr}}$and v_{OUT}, when correction is enabled (black) and no correction is used (gray) is shown in Figure 3-16. A correction voltage V_{corr} is applied through sw_1 at the beginning of the charge transfer phase ϕ_2 (refer to Figure 3-15 and Figure 3-16). The voltage v_{Xcorr} at node v_X when error correction is applied, can be expressed as:

$$v_{Xcorr} = v_X + \kappa V_{corr}$$

where κ is the transfer function from the correction voltage node V_{corr} to node v_X. For this topology κ is:

$$\kappa = \frac{v_X}{V_{corr}} = \frac{C_{corr}}{C_{corr} + C_{n1} + (C_{n2} \parallel (C_{CLS} + C_{n+1}))}.$$

The change in the output voltage (Δv_{OUT}) when V_{corr} is applied through sw_1 is:

$$\Delta v_{OUT} = \kappa \left(\frac{C_{2n}}{C_{2n} + C_{CLS} + C_{n+1}} \right)$$

In Figure 3-16, the virtual ground condition is satisfied at time t_0. The ZCD output ZCD_{out} transitions at time t_1. Let $t_d = t_1 - t_0$. At time t_2 the voltage at node v_X is restored to its uncorrected value by turning off sw_1 and turning on sw_2 to connect the top plate of of the correction capacitor C_{corr} to V_{CM} as shown in Figure 3-15. The final ZCB circuit output voltage value sampled at t_1 is $v_{OUT_{corr}}$. In the case when no correction is applied, the virtual ground condition is satisfied at time t_3. If the ZCD can respond instantaneously, the output voltage $v_{OUT_{ideal}}$ it sampled at instant t_3. However, the ZCD has a finite delay and therefore the ZCD output does not transition until time t_4 when the output voltage $v_{OUT_{uncorr}}$ is sampled. In Figure 3-16, V_{OV} is only partially corrected and the voltage $v_{OUT_{corr}}$ is not equal to the desired output voltage $v_{OUT_{ideal}}$. The overshoot error, however, is reduced significantly compared to the uncorrected case $v_{OUT_{uncorr}}$.

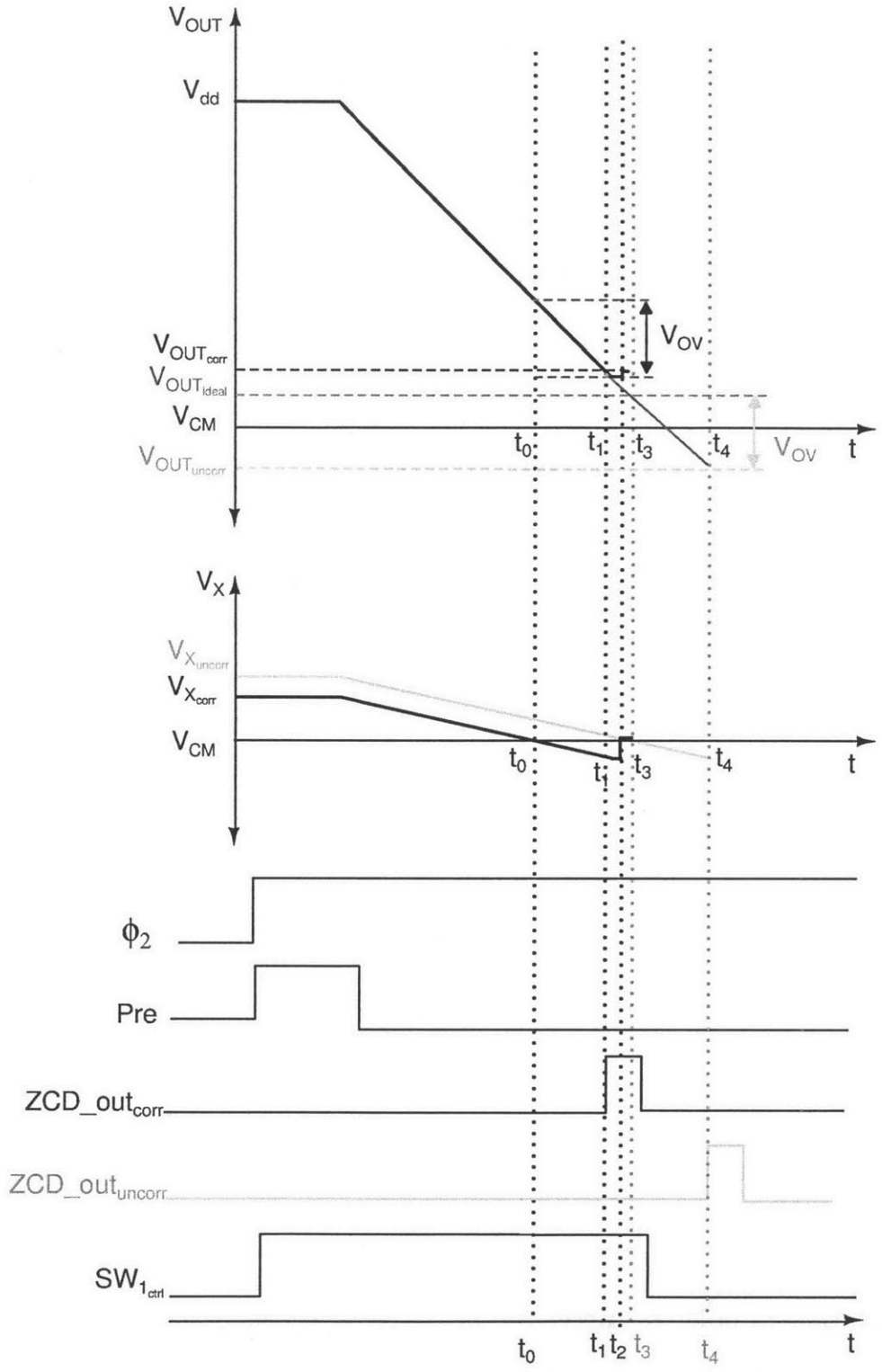


Figure 3-16: Voltage waveforms at the ZCBC output v_{OUT} and at v_X when partial constant overshot error correction is applied. Gray represents uncorrected waveforms. Black represents corrected waveforms. In the timing diagram, ϕ_2 enables the charge transfer phase, *Pre* is the preset signal and sw_1 and sw_2 enable the correction mechanism

The applied offset voltage at the input of the ZCD can be converted to time through the input voltage ramp. The time t_{corr} can be expressed as:

$$\frac{\kappa V_{corr}}{t_{corr}} = \beta"(\frac{dv_{OUT}}{dt})$$

where $\beta"(\frac{dv_{OUT}}{dt})$ is the ramp rate at v_X and

$$\beta" = \frac{C_{2n}}{C_{1n} + C_{2n} + C_{corr}}.$$

It follows that the correction time t_{corr} is therefore equal to:

$$t_{corr} = \frac{\kappa V_{corr}}{\beta"(\frac{dv_{OUT}}{dt})}.$$

The residual error in the output voltage offset correction can then be expressed as:

$$\begin{aligned} \Delta V_{OV} &= V_{OV} - V_{OV_{corr}} \\ &= (t_d - t_{corr})\frac{dv_{OUT}}{dt} \\ &= t_d\frac{dv_{OUT}}{dt} - \left(\frac{\kappa V_{corr}}{\beta"(\frac{dV_{OUT}}{dt})}\right)\frac{dv_{OUT}}{dt} \end{aligned} \tag{3.19}$$

Setting $\Delta V_{OV} = 0$ in Eq. 3.19 the corrected output voltage is expressed as:

$$V_{corr} = t_d\frac{1}{\kappa}\beta'\frac{dv_{OUT}}{dt} = \frac{1}{\kappa}\beta" V_{OV}.$$

It follows that in order to cancel the ZCD constant delay (which is equivalent to canceling the constant overshoot error, $V_{OV} = \frac{I_0}{C}t_d$), the voltage at v_X has to be offset by:

$$v_{Xcorr} = v_X - \frac{1}{\kappa}\beta" V_{OV}.$$

The output offset error must be corrected to the coarse phase output voltage accuracy requirement in a two-phase ZCB implementation. Suppose the coarse phase is accurate to K bits, the required correction voltage V_{corr} accuracy can then be derived from:

$$\mid \Delta V_{OV} \mid < \frac{V_{OUT_{FS}}}{2^{K+1}}$$

$$\mid V_{OV_{MAX}} - \frac{\kappa V_{corr}}{\beta"} \mid < \frac{V_{OUT_{FS}}}{2^{K+1}}$$

$$\mid \frac{\beta"}{\kappa} V_{OV_{MAX}} - V_{corr} \mid < \mid \frac{\beta"}{\kappa} \left(\frac{V_{OUT_{FS}}}{2^{K+1}} \right) \mid . \tag{3.20}$$

where $V_{OUT_{FS}}$ is the nominal ZCBC output range. Substituting real values in Eq. 3.20 for $K = 8$, $k = 0.05$, $\beta" \simeq \frac{1}{4}$ and $V_{OUT_{FS}} = 1V$ yields $\mid \frac{\beta"}{\kappa} V_{OV_{MAX}} - V_{corr} \mid < 10mV$. The correction voltage V_{corr} must therefore be accurate to $N + 1 - log_2(\frac{\beta"}{\kappa})$. For this particular example, the correction voltage V_{corr} must be accurate to 6.7 bits.

In a bidirectional ramp ZCB circuit is used, the applied correction voltage polarity has to change as the output current ramp direction changes. The output-sign bit $d_{outsign}$ can be used to control the correction voltage polarity as shown in Figure 3-17. The appropriate correction voltage polarity is selected through sw_{11} and sw_{12} in Figure 3-17.

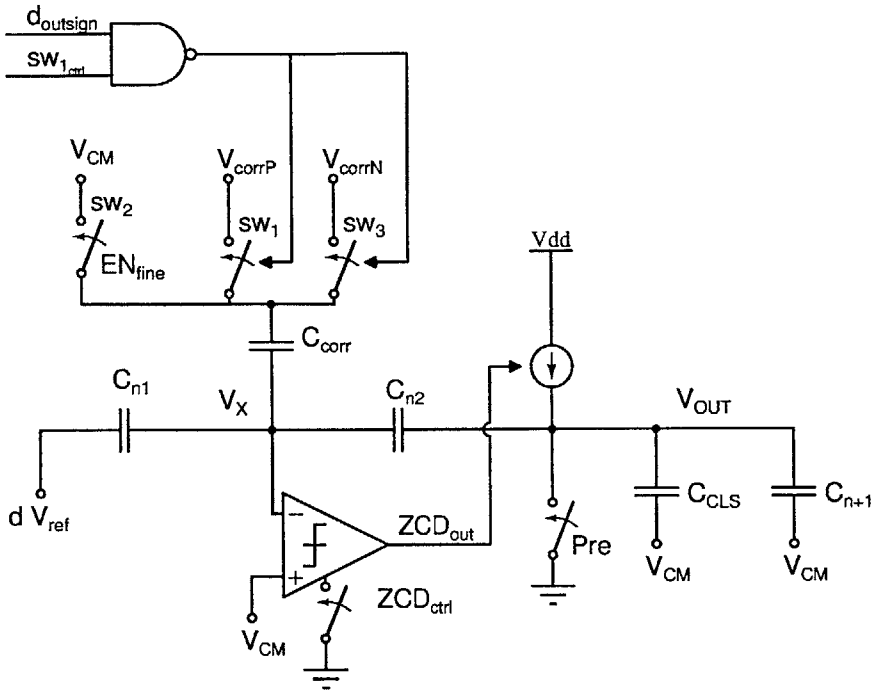


Figure 3-17: Constant overshoot correction for bi-directional ramp ZCBC

3.3.3 Self-correction in Hybrid CLS-OpAmp/ZCBC

One area for future improvement in the implementation of ZCBC overshoot constant correction is background self-correction. The overshoot error correction described in 3.3.2 can be automated through a feedback loop from the opamp output to the offset voltage applied at the input of the ZCD in a hybrid CLS-opampZCB switched-capacitor circuit (Figure 3-18 and Figure 3-19) .

The overshoot error can be sensed at the opamp output once the opamp has settled the coarse phase error voltage at the output v_{OUT} to the final output voltage $v_{OUT_{FINAL}}$ at the end of the fine charge-transfer phase. The opamp final voltage $v_{AMP_{FINAL}}$ is :

$$v_{AMP_{FINAL}} = \frac{C_{CLS} + C_{n+1}(C_{n1} \parallel C_{n2})}{C_{CLS}} v_{OUT_{FINAL}}.$$

Note that depending on the size of capacitor C_{CLS} the overshoot error is amplified by a factor of $\frac{C_{CLS}+C_{n+1}(C_{n1}\|C_{n2})}{C_{CLS}}$ at node v_{AMP}. For $C_{CLS} = C_{n+1}(C_{n1} \parallel C_{n2})$ the overshoot error increases by a factor of 2. The voltage V_{corr} is incremented though a

counter (U_2) and DAC (U_3) until the output final value $v_{AMP_{FINAL}}$ crosses V_{CM} and trips the comparator (U_1). Note that U_1 performs a zero-crossing function similar to the the ZCD. The trip point of U_1 determines when the virtual ground condition of the correction feedback loop is satisfied. The goal of the feedback loop is to cancel the constant overshoot error, but it does not need to be as accurate as the stage accuracy or the coarse phase accuracy, as demonstrated by Eq. 4.39. The comparator can only be activated once every number of cycles of the ADC sampling clock.

This automated correction method depends on a two-phase charge-transfer operation ZCBC combined with correlated level shifting (CLS). The second phase does not have to be opamp based.

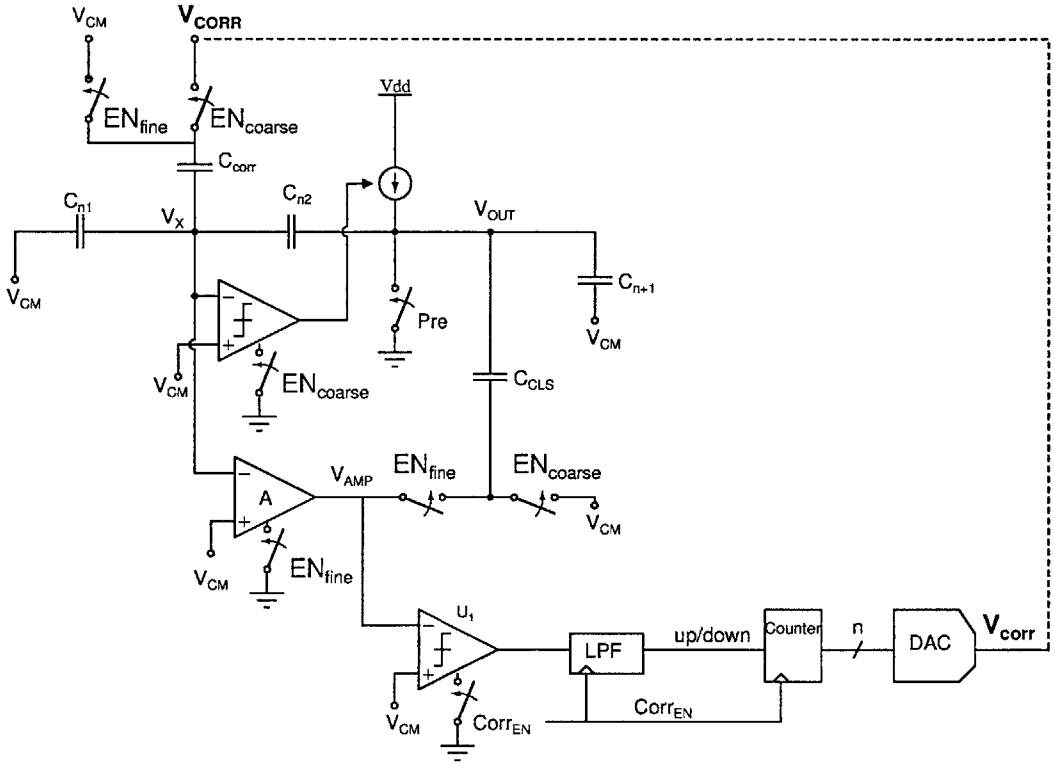


Figure 3-18: Background constant overshoot correction

3.3.4 Offset Error and Bidirectional Ramp ZCBC in 1-bit Pipelined ADC

The ideal transfer function for a single 1-bit pipelined ADC stage is:

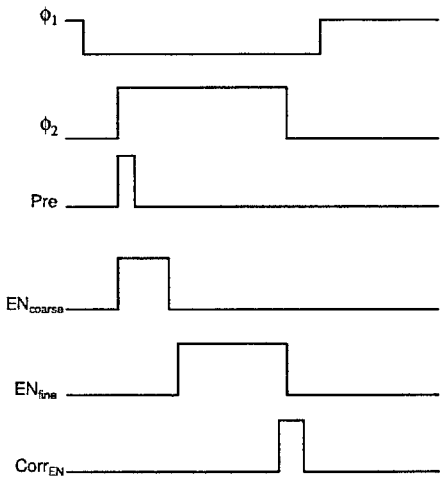


Figure 3-19: Timing diagram for background constant overshoot correction

$$v_O = 2v_{IN} - dV_{REF} \tag{3.21}$$

where v_O is the ideal stage output voltage, d is the sub-ADC output bit and V_{REF} is the ADC reference voltage. Suppose the pipeline stage is based on a ZCBC charge-transfer phase. Further suppose the ZCBC has an ideal current source and a ZCD constant delay t_d, producing a constant overshoot error V_{OV}. If unidirectional ramp ZCBC is implemented, the pipeline stage output voltage is:

$$v_{OUT} = 2v_{IN} - dV_{REF} + V_{OV}. \tag{3.22}$$

The constant overshoot error V_{OV} is indistinguishable from a constant stage offset error in an opamp based charge-transfer implementation and results in wide codes in the ADC transfer function if output over-range protection is not present.

If bidirectional ramp ZCB charge-transfer is implemented, the overshoot error changes polarity with the polarity of the output as discussed in 3 and the pipeline stage output can be expressed as:

$$v_{OUT} = \begin{cases} 2v_{IN} - dV_{REF} + V_{OV}, & v_{OUT} > 0 \\ 2v_{IN} - dV_{REF} - V_{OV}, & v_{OUT} < 0 \end{cases} . \tag{3.23}$$

and is illustrated in Figure 3-20 (for ADC reference voltages $V_{REFP} = 0.5V$, $V_{REFM} = -0.5V$ and constant overshoot error $V_{OV} = 0.1V$). The change in polarity of V_{OV} at the midpoint of the transfer function ($v_O = 0$ in Figure 3-20) results in wide codes at the bit-decision boundary.

If a positive stage offset is present $V_{off} > 0$, the pipeline stage transfer function can be expressed as:

$$v_{OUT} = \begin{cases} 2v_{IN} - dV_{REF} + V_{off} + V_{OV}, & v_{OUT} > 0 \\ 2v_{IN} - dV_{REF} + V_{off} - V_{OV}, & v_{OUT} < 0 \end{cases} .$$

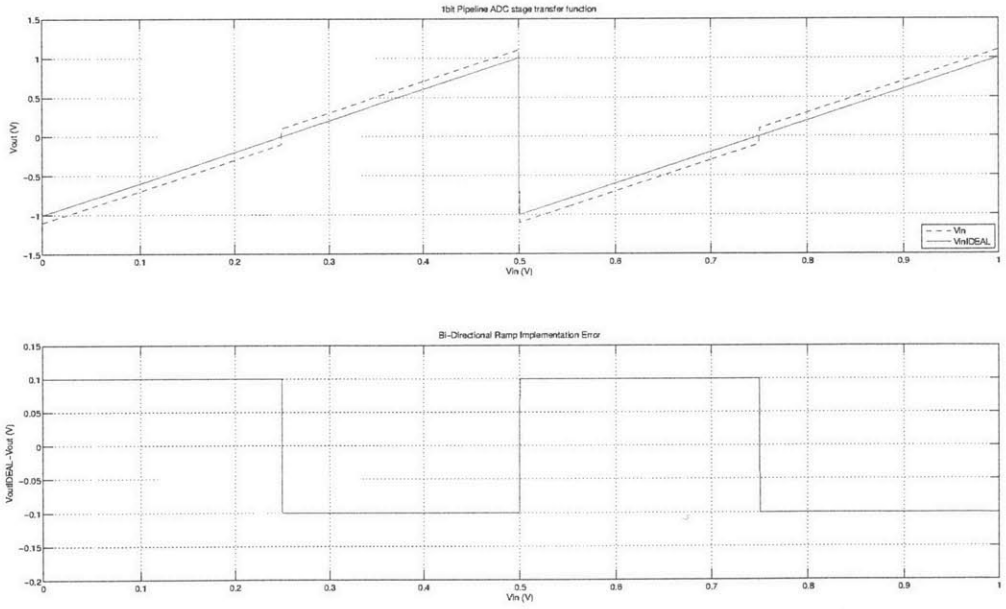


Figure 3-20: Transfer function (top) and overshoot error (bottom) for a bidirectional ramp ZCB implementation of 1-bit pipeline ADC stage with reference voltages $V_{REFP} = 0.5V$, $V_{REFM} = -0.5V$ and $V_{OV} = 0.1V$

If capacitor mismatch Δ is present between the input sampling capacitor C_1 and

feedback capacitor C_2 for the ideal 1-bit pipeline ADC and the overshoot error changes polarity with output polarity, the ADC pipeline stage transfer function as shown in Figure 3-21, is :

$$v_{OUT} = \begin{cases} (2+\Delta)v_{IN} - (1+\Delta)dV_{REF} + V_{OV}, & v_{OUT} > 0 \\ (2+\Delta)v_{IN} - (1+\Delta)dV_{REF} - V_{OV}, & v_{OUT} < 0 \end{cases}.$$

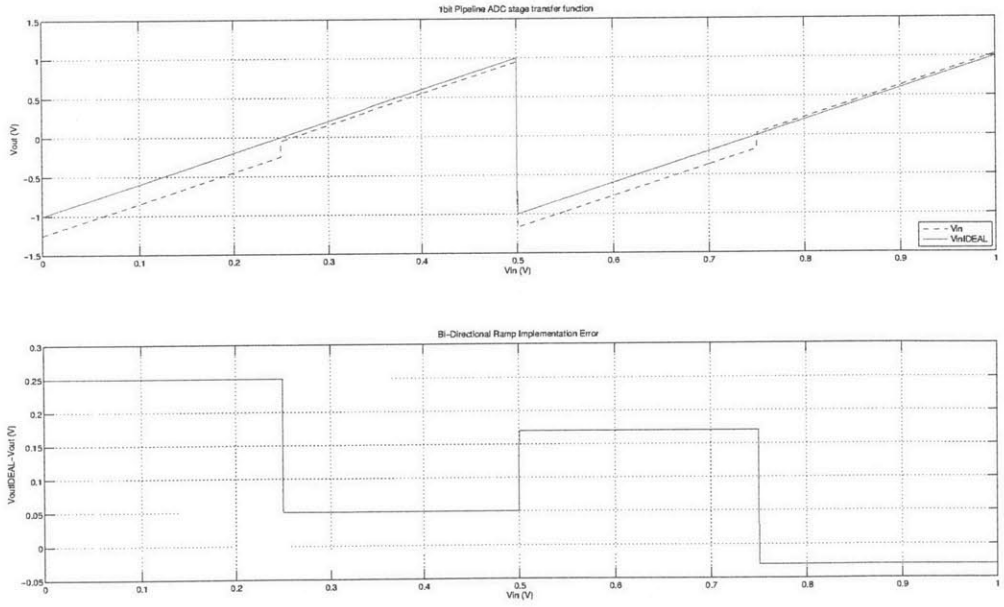


Figure 3-21: Transfer function (top) and overshoot error (bottom) for bidirectional ramp ZCB implementation of 1-bit pipeline ADC stage in the presence of capacitor mismatch, with reference voltages $V_{REFP} = 0.5V$ and $V_{REFM} = -0.5V$, and $V_{OV} = 0.1V$

The equivalent gain error in a ZCB charger-transfer implementation is similar to the error due to an opamp based charge-transfer implementation [6, 17, 36]. ZCBC gain error is due to finite current source resistance, R_O. If the ZCB circuit current source is assumed no longer ideal, the current ramp can be represented as:

$$I = I_0 - \frac{v_O I_0}{V_A}, \tag{3.24}$$

where I_0 represents the current source ideal current. Integrating equation Eq. 3.24 for the duration of the ZCD delay t_d, assuming a ZCB circuit load capacitor C and substituting the result into Eq. 3.22 yields to first order :

$$v_{OUT} = 2v_{IN} - dV_{REF} + \frac{I_0 t_d}{C} - \frac{t_d V_O I_0}{C V_A}.$$

Let $V_{OV} = \frac{I_0 t_d}{C}$. Then if finite current source output resistance is taken into account and the overshoot error changes polarity with output ramp direction, the ADC pipeline stage transfer function can be expressed as:

$$v_{OUT} = \begin{cases} \frac{2v_{IN} - dV_{REF} + V_{OV}}{1 + \frac{t_d I_0}{C V_A}}, & v_{OUT} > 0 \\ \frac{2v_{IN} - dV_{REF} + V_{OV}}{1 + \frac{t_d I_0}{V_A C}} & v_{OUT} < 0 \end{cases}$$

and is illustrated in Figure 3-22 (for ADC reference voltages $V_{REFP} = 0.5V$, $V_{REFM} = -0.5V$ and constant overshoot error $V_{OV} = 0.1V$).

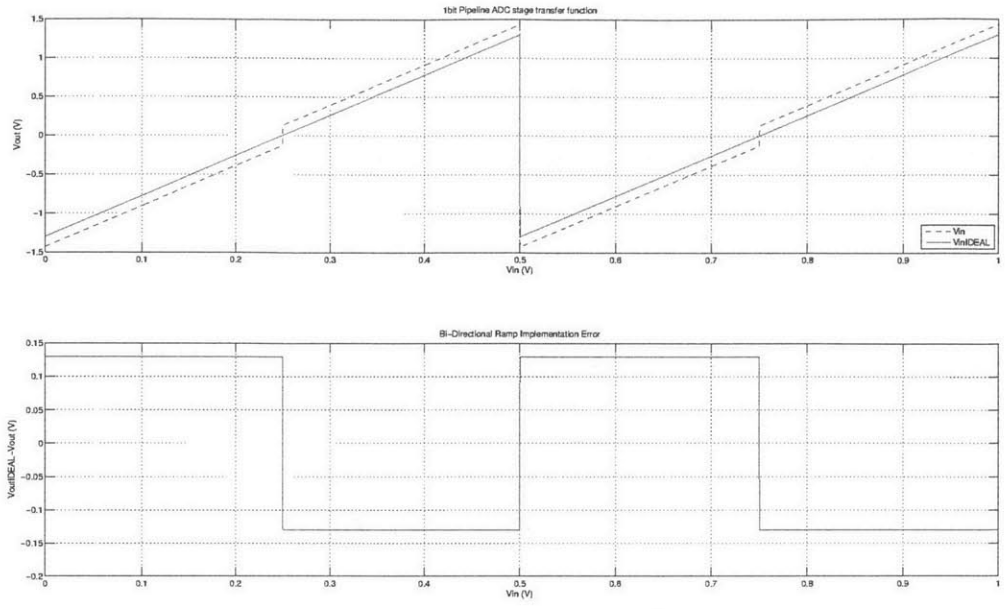


Figure 3-22: Transfer function (top) and overshoot error (bottom) for bidirectional ramp ZCBC implementation of 1-bit pipelined ADC stage in the presence of gain error, $V_{REFP} = 0.5V$, $V_{REFM} = -0.5V$ and $V_{OV} = 0.1V$.

Chapter 4

Test Chip Design

In this chapter the design and realization of 13-bit 100MS/s pipelined ADC is described. A hybrid CLS-opamp/ZCB switched-capacitor circuit is used to implement the multiplying digital-to-analog converter (MDAC) of an n^{th} pipeline stage. The ZCB phase is implemented using current steering and the bidirectional ramp approach described in 3.

4.1 Pipelined ADC Design

4.1.1 First Stage Top Level Design

To realize a 13-bit pipelined ADC, eight pipeline stages are implemented. An effective 2.8-bit sub-ADC with redundancy is used in the first pipeline stage with inter-stage gain $G = 4$. As discussed in Section 3.2 redundancy is used to mitigate the effect of stage errors, especially offset errors in the BDCs. The first stage transfer function is shown in Figure 4-1. As discussed in 3.2.4.2 the sub-ADC consists of six bit-decision comparators (BDCs) using redundancy for an effective fully differential input of $1.75V$.

The dotted lines in Figure 4-1 represent additional BDCs of the sub-ADC, needed to generate the output-sign bit for the coarse phase bidirectional ramp ZCB implementation. The total number of BDCs for bidirectional ramp ZCBC operation is

$(2n + 1) = 13$, if $n = 6$ is the number of main BDCs.

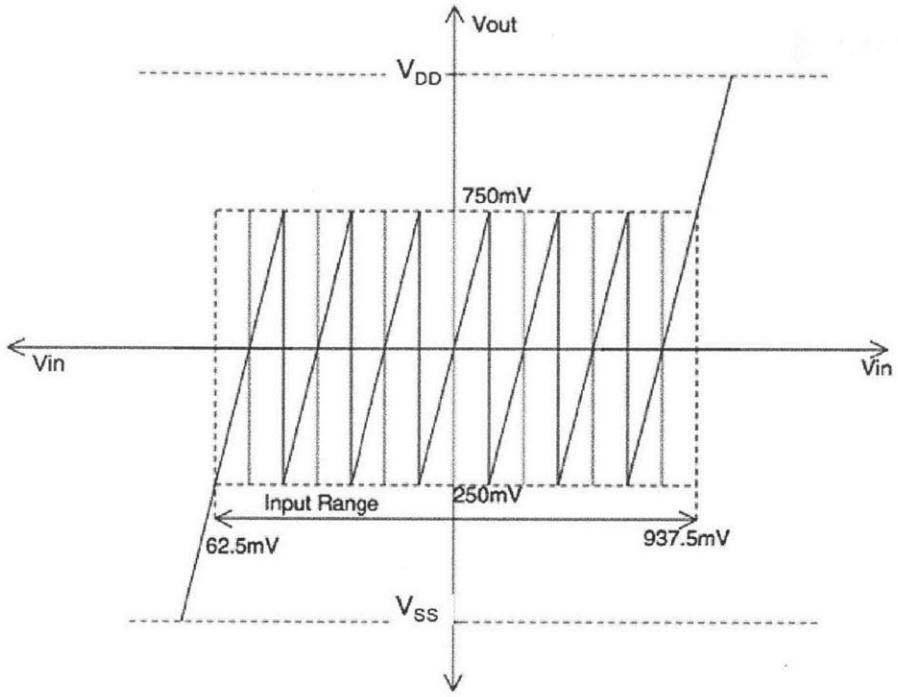


Figure 4-1: First stage transfer function. The dotted lines indicate the additional BDCs needed to generate the output-sign bit for bidirectional ramp implementation

4.1.1.1 Input Sampling Network

The quantization noise for an ideal N-bit ADC of an input amplitude $\frac{V_{FS}}{2}$ is uniformly distributed in the range $[-\frac{V_{FS}}{2^N}, \frac{V_{FS}}{2^N}]$. The mean-square value for a uniform distribution of the quantization error is [10]:

$$\bar{\varepsilon_q^2} = \frac{(\frac{V_{FS}}{2^N})^2}{12}. \tag{4.1}$$

The root mean-square quantization noise voltage $\sqrt{(\bar{\varepsilon_q^2})}$ for $N = 13$ and full scale input amplitude of 1.75V is $61.7\mu V$.

The signal power of an input $V_{in} = \frac{V_{FS}}{2} sin(2\pi \frac{1}{T} t)$ is:

$$\bar{V_{in}^2} = \frac{1}{T}\int_0^T \left(\frac{V_{FS}}{2} sin(2\pi \frac{1}{T}t)\right)^2 dt = \frac{V_{FS}^2}{8}. \tag{4.2}$$

The signal-to-noise ratio (SNR) of the ADC , taking only quantization noise into account, is defined as:

$$SNR = 10\log\left(\frac{\bar{V_{in}^2}}{\bar{\varepsilon_q^2}}\right). \tag{4.3}$$

Substituting Eq. 4.1 and Eq. 4.2 into Eq. 4.3 results in the best attainable signal-to-noise ratio SNR_0 for an N-bit ADC, only limited by quantization noise:

$$\begin{aligned} SNR_0 = 10\log & \left(\frac{\frac{V_{FS}^2}{8}}{\frac{(\frac{V_{FS}}{2^N})^2}{12}}\right) \\ =& 10\log\left(\frac{3}{2}2^{2N}\right) \\ =& 10\log\left(2^{2N}\right) + 10\log\left(\frac{3}{2}\right) \\ =& 6.02N + 1.76dB. \end{aligned}$$

Thermal noise contributed by the ADC circuit degrades the ideal SNR_0. If the input-referred ADC thermal noise power $\overline{v_n^2}$ is equal to the quantization noise power $\bar{\varepsilon_q^2}$ then the ADC SNR degrades by $3dB$:

$$\begin{aligned} SNR =& 10\log\left(\frac{\bar{V_{in}^2}}{2\bar{\varepsilon_q^2}}\right) \\ =& 10\log\left(\frac{\bar{V_{in}^2}}{\bar{\varepsilon_q^2}}\right) + 10\log\left(\frac{1}{2}\right) \\ =& SNR_0 - 3dB. \end{aligned}$$

The mean-square voltage of thermal noise, contributed by the resistors in the sam-

pling path, sampled on the input capacitor C is $\overline{v_n^2} = \frac{kT}{C}$ [10] where k is Boltzmann's constant and T is the temperature in Kelvin. The sampled thermal noise power has to be less than or equal to the quantization noise power to limit SNR degradation:

$$(\bar{\varepsilon_q^2}) \geq \frac{kT}{C}. \tag{4.4}$$

The minimum size of the total input capacitor for N-bit resolution ADC can then be determined by substituting Eq 4.1 into Eq. 4.4 and setting Eq. 4.4 as an equality:

$$C_{min} = \frac{2^{2N}(12)\,kT}{V_{FS}^2}.$$

Substituting $N = 13$ and $V_{FS} = 1.75V$, the minimum input capacitor C_{min} is $1.1pF$. For a conservative design the input capacitor C_{IN} was chosen to be $3.4pF$, which provides $\frac{kT}{C}$ noise equivalent to $N = 13.8$ bits. The input signal can be viewed as sampled differentially across two capacitors in series each of value $2C_{IN}$, which translates to $6.8pF$ at each differential input. Bottom-plate sampling is used and both the bottom and input sampling switches are bootstrapped [1]. Cadence simulations of the input sampling network, using an input bond-wire model for a bond-wire of length 1mm at each input, yielded 13.4 bits ENOB.

Capacitor splitting is used for reference voltage switching [6] of the DAC implementation in the first stage with a first stage unit capacitor C_{unit} of $860fF$. The input capacitor is split into 8 unit capacitors, six of which correspond to the BDCs of the stage and form C_{11} in Figure 4-2, while the remaining two unit capacitors form C_{21} for a total of $C_{IN} = 6.8pF$. The second stage input capacitor and third stage input capacitor are each scaled respectively by a factor equal to the inter-stage gain of 4.

4.1.1.2 First Stage Implementation

A top level diagram of the fully-differential CLS-opamp/ZCB implementation of the first pipeline stage is shown in Figure 4-2. The sub-ADC comprises 13 BDCs. Six of

the BDCs determine the transfer function of the first stage and the remaining seven resolve the output-sign bit for the bidirectional ramp ZCBC implementation. The BDC architecture and latch topology implemented in [6] is used in this work as it is shown to present lower input offset compared to other latch implementations.

The operation of the stage is based on two non-overlapping clock phases ϕ_1 and ϕ_2. During the sampling phase (ϕ_1) (refer to Figure 4-3), the input is sampled on the input sampling capacitors C_{11} and C_{21}. The main six BDCs digitize the input with effective 2.8-bits of accuracy. The output-sign BDCs are used to generate the output-sign bit, which in turn serves to choose the respective output preset voltage and ramp current direction. The output-sign bit is an input select signal for a mux $U1$ with UP or DOWN input control signals as shown in Figure 4-2. If the output-sign bit is high, the positive output voltage is preset low and a PMOS current source is enabled during the charge transfer phase ϕ_2, and vise verse for when the output-sign bit is low. The preset control signal Pre is generated from the output of the mux $U1$ and the clock phase ϕ_2. The current source control signal I_{CTRL} is a function of both the the output of the mux $U1$ and the ZCD output ZCD_{out}. At the start of ϕ_2 the the analog muxes U_2 and U_3 connect the corresponding reference voltages to the sub-ADC output word D to each of the six unit input capacitors of C_{11}. Once the ZCD detects the virtual ground condition the ZCD_{ctrl} signal turns off the ZCD and current and AMP_{ctrl} signal is generated to turn on the opamp and turn off the switches at the bottom plate of the level shifting capacitor C_{CLS} for the fine charge transfer phase. Current steering introduced in Chapter 3 and output offset correction, which will be discussed in further detail in this Chapter are implemented but not depicted in the diagram below for simplicity.

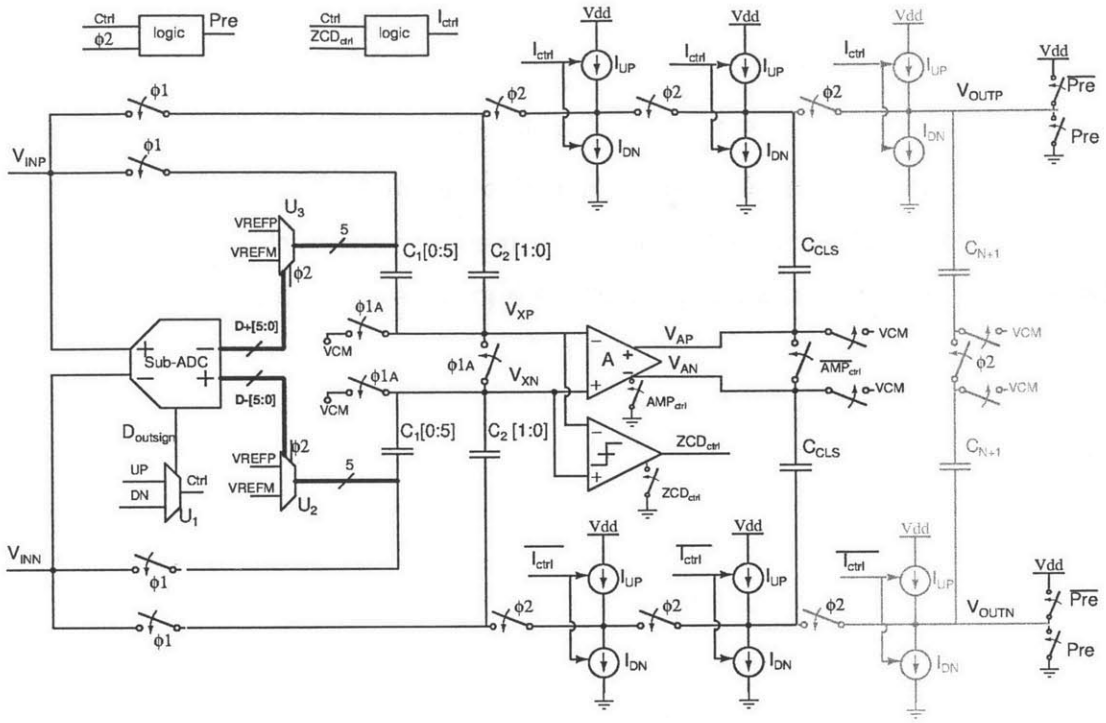


Figure 4-2: First stage fully-differential hybrid CLS-opamp/ZCB implementation. The areas in gray denote the second stage input capacitors and respective current sources

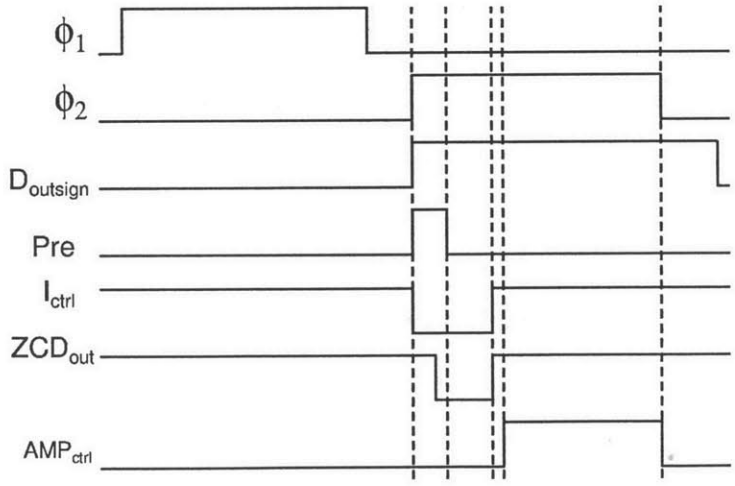


Figure 4-3: Timing diagram for first stage hybrid CLS-opamp/ZCB implementation. In this particular case the output-sign bit is resolved to be high.

4.1.1.3 Charge-Transfer Implementation

A simplified diagram of the coarse and fine phases of the charge transfer operation during ϕ_2 is shown in Figure 4-4 and the respective timing diagram is shown in Figure

4-5. The output-sign bit is assumed to be high. The charge transfer phase consists of a fast coarse ZCB phase and a fine opamp based phase. The capacitor C_{CLS} is charged during the coarse phase and level shifts the opamp output from the pipeline stage output during the fine phase to cancel the coarse phase estimate value in the feedback path. Thus the opamp settles exponentially only the coarse phase error to a more accurate final output voltage value.

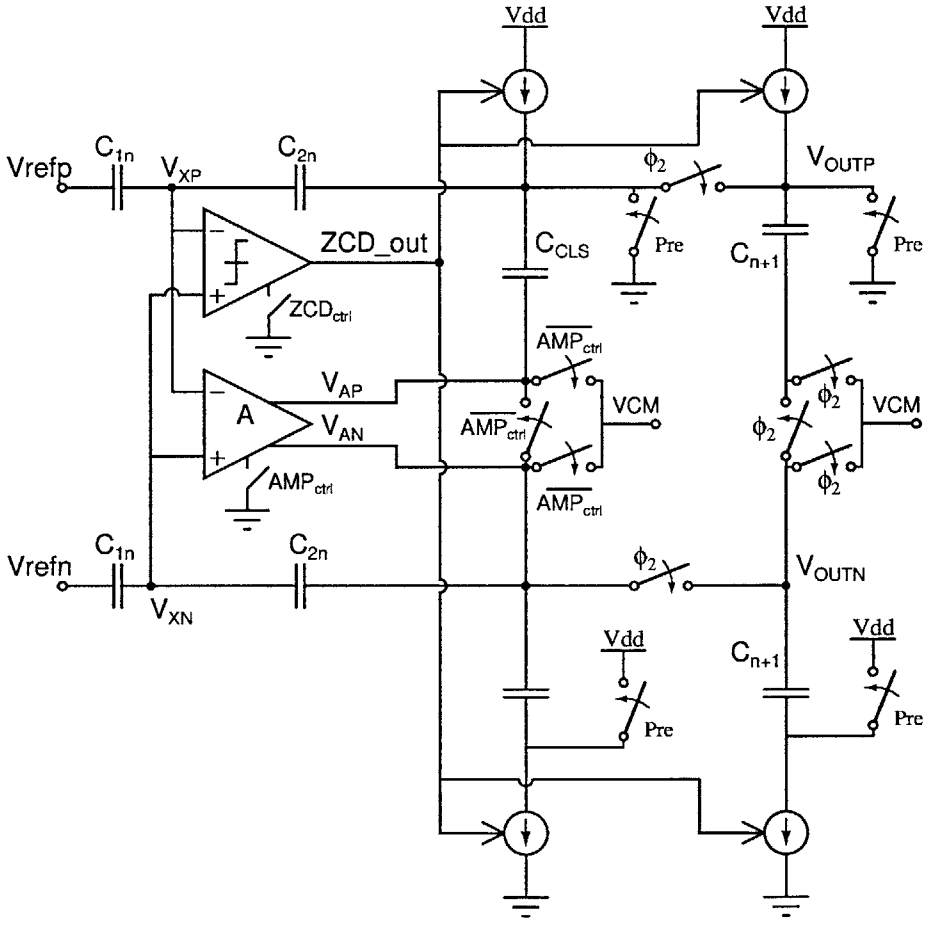


Figure 4-4: Charge-transfer implementation

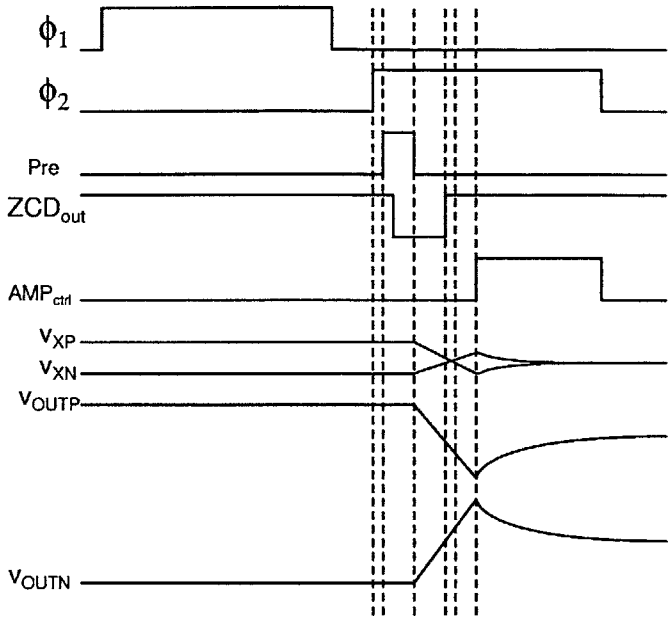


Figure 4-5: Timing diagram for charge-transfer implementation

4.2 Bidirectional Ramp Current Source Implementation

Complementary cascode current sources are implemented at each output for bidirectional ramp generation. Note that only one current source is active during a fixed charge-transfer operation. In [6] permanently disabled dummy complementary current sources are added in a unidirectional ramp ZCBC implementation for better output parasitic capacitance matching between the two differential outputs for high frequency power supply noise rejection. Thus in the bidirectional case the permanently disabled dummy current sources are not needed.

In [6] the transfer function from the power supply to the output of a PMOS current source $M1$ (refer to Figure 4-6) is derived as:

$$\frac{v_{out}(s)}{v_{dd}(s)} \simeq \frac{sr_{o_{M1}}C_{db_{M1}} + 1}{(sr_o(C + C_{db_{M1}}) + 1)(sr_{sw}C_{db_{M1}} + 1)}$$

where $C_{db_{M1}}$ is the current source bulk to drain junction capacitance, r_o is the current source output resistance, C is the total load capacitor charged by the current source and r_{sw} is the sampling switch resistance at the bottom plate of C. For simplicity of

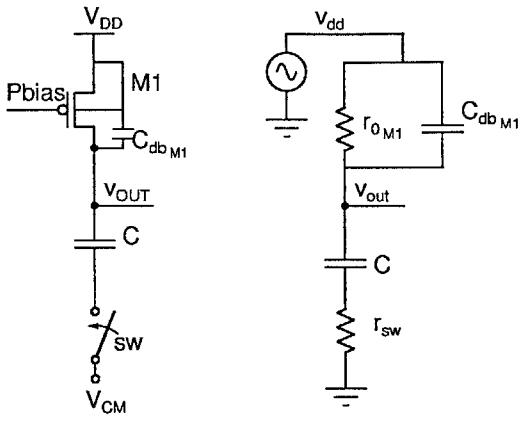


Figure 4-6: Power supply coupling to the current source output.

the analysis the current source is not cascoded but the analysis still holds if $r_{o_{M1}}$ is replaced by the cascode current source output resistance R_O and $C_{db_{M1}}$ is replaced by $C_{db_{M2}}$ is the drain junction capacitance of the cascode device $M2$ in Figure 4-7. The noise coupled through $C_{db_{M1}}$ in in Figure 4-7 of the cascode current source is attenuated by the gain of $M2$.

The switch resistance is assumed much smaller than the output resistance of the current source $r_{sw} \ll r_{o_{M1}}$ in Figure 4-6 and the parasitic junction capacitor at the drain of the current source $C_{db_{M1}}$ is assumed much smaller than the total load capacitor $C \ll C_{db_{M1}}$. At very low frequencies the supply noise is not attenuated and appears at the current source output. At higher frequencies the pole due to the current source output resistance $r_{o_{M1}}$ and load capacitor C causes supply noise to roll off with a first order system response. When the impedance of device bulk to drain junction capacitance $C_{db_{M1}}$ becomes much smaller than $r_{o_{M1}}$, the transfer function is approximated by capacitive divider $\frac{v_{out}(s)}{v_{dd}(s)} \simeq \frac{C_{db_{M1}}}{C+C_{db_{M1}}}$, formed by the junction capacitor C_{db} and the load capacitor C. The power supply noise for frequencies at which, the impedance of $C_{db_{M1}}$ is smaller than $r_{o_{M1}}$ and larger than r_{sw} is attenuated by $\frac{C_{db_{M1}}}{C+C_{db_{M1}}}$ and appears at the output. In a fully differential implementation if the device bulk to drain junction capacitance $C_{db_{M1}}$ is matched between the positive and negative outputs, the supply noise appears as common mode in this frequency range.

By design the load capacitor C, charged by the current source is much larger than capacitor $C_{db_{M1}}$. When correlated level shifting (CLS) is used the load capacitor doubles to $2C$ (for $C_{CLS} = C$ as is discussed in more detail in Subsection 4.3.2.2). However, to keep a fixed ramp rate the current must double accordingly. The drain to bulk capacitance $C_{db_{M1}}$ doubles with the width of the current source device for fixed device length as the current doubles and $\frac{v_{out}(s)}{v_{dd}(s)} \simeq \frac{C_{db_{M1}}}{C+C_{db_{M1}}}$ is unchanged. The use of correlated level shifting does not change the analysis presented above.

To reduce the power supply coupling at higher frequencies $C_{db_{M1}}$ should be minimized. One way to reduce $C_{db_{M1}}$ is to reduce the width of the current source devices and use a larger overdrive voltage V_{DSAT}. However, larger V_{DSAT} limits the available ZCB circuit output range, as it is limited to $2V_{DSAT}$ from either rail and increases flicker noise contribution from $M1$. In the prototype ADC the width of the devices was chosen for optimized output swing. The first stage output current source consists of 64 devices in parallel of width $W = 4.08\mu m$ and length $L = 0.12\mu m$, with an equivalent $C_{db} = 52fF$. The first stage total load capacitor is $6pF$. The high frequency power supply attenuation is then $\frac{v_{out}(s)}{v_{dd}(s)} \simeq \frac{C_{db}}{C+C_{db}} \simeq \frac{0.052pF}{6pf+0.052pF}$, which is $-41dB$ attenuation. As the drain to junction capacitance at both the positive and negative inputs are matched better through the presence of complementary current sources, the high frequency noise appears as common mode and is much better than $-41dB$.

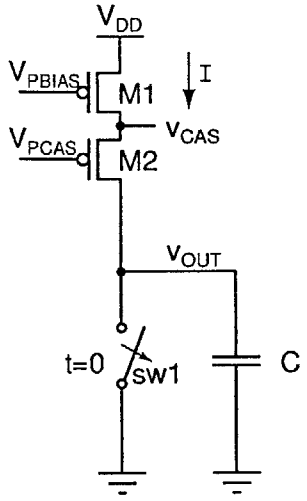


Figure 4-7: Simplified diagram of ramp generator

Assume the current source is cascoded and the current is I (refer to Figure 4-7). The maximum output-dependent overshoot error over the current source nominal output swing $V_{OUT_{FS}}$ can be derived as :

$$\mid v_{ov_{MAX}} \mid = t_d \frac{V_{OUT_{FS}}}{R_O C}, \tag{4.5}$$

where $R_O = r_{0_{M2}}(g_{m_{M2}} r_{0_{M1}} + 1)$ is the output resistance of a cascoded current source [10],where $g_{m_{M2}}$ and $r_{0_{M2}}$ are the transconductance and output resistance of $M2$ and $r_{0_{M1}}$ is the output resistance of $M1$ and t_d is the ZCD delay. The transconductance of $M2$, $g_{m_{M2}} = \frac{I}{2V_{DSAT_{M2}}}$ and $r_{0_{M1}} = r_{0_{M2}} = \frac{V_A}{I}$, where V_A is the Early voltage of $M2$, as both $M1$ and $M2$ carry the same current and are sized to have equal length and width. Substituting into Eq. 4.5 yields:

$$\mid v_{ov_{MAX}} \mid = t_d \frac{V_{OUT_{FS}}\,(2V_{DSAT})}{V_A^2} \frac{I}{C}$$

$$\mid v_{ov_{MAX}} \mid = t_d \frac{V_{OUT_{FS}}\,(2V_{DSAT})}{V_A^2} \frac{dv_{OUT}}{dt}.$$

For fixed output ramp rate $\frac{dv_{OUT}}{dt}$, full scale current source output voltage swing $V_{OUT_{FS}}$ and fixed ZCD delay t_d, the overshoot error is proportional to the overdrive

voltage of the current source devices. Therefore, minimizing the overdrive voltage minimizes the output dependent overshoot error. The current source devices were designed for an overdrive voltage of $V_{DSAT} = 160mV$ and two times the minimum device length was used for improved output resistance. Note that for a V_{DSAT} of $160mV$ in a bidirectional ramp implementation there is headroom for double cascoding for an upper rail of $1V$, which can improve linearity. The output swing for a NMOS current source is $V_{DD} - 3(160mV) = 1V - 480mV = 520mV$ The output range of either type of current source is $\frac{V_{DD}}{2} = 500mV$ in bidirectional mode. As the available margin is only $20mV$, it was not implemented in this design, however in future work the V_{DSAT} of the devices can be further reduced to allow for larger error margin.

Current splitting, introduced in [6] is used to eliminate the output switch in the current path of the multiply-by-two digital-to analog converter MDAC in the pipeline stage implementation. The series switch in the path of the current source at the output introduces output dependent voltage error because the switch on-resistance is output dependent and limits the linearity of the stage.

The current sources can be reconfigured for a range of unit bias currents from $33uA$ to $72uA$. The current can be stepped in five increments and three of the bias currents are shown in Table 4.1. The range of bias currents translates to first stage total ramp current $I_{BIAS_{1st}}$ charging the output load capacitor $C_{TOT} = C + C_{CLS}$ in the range of $2.1mA$ to $4.6mA$. The first stage differential ramp rate S_{diff} can be set from $6.6(10^8)\frac{V}{s}$ to $1.5(10^9)\frac{V}{s}$. In a bidirectional ZCB implementation, the ramp rate settings correspond to coarse phase durations of $\sim 1.5ns$ to $\sim 0.7ns$. In a hybrid CLS-OpAmp/ZCB implementation, the range of ramp rates can support sampling rates from $75MS/s$ to $100MS/s$, where it is assumed that the fine phase opamp settles to 4 time constants with a closed loop bandwidth of $150MHz$ and $200MHz$ respectively and the preset phase duration is $800ps$. The preset phase can be configured from $400ps$ to $800ps$ in the prototype ADC. From Cadence extracted simulations the ZCD delay (including buffer delay to the current steering switches) t_d is approximately

$\sim 100ps$. For a conservative estimate of the overshoot error a ZCD delay of twice the simulated delay is assumed $t_d = 200ps$. The differential overshoot error $V_{OV_{diff}}$ is estimated using $V_{OV_{diff}} = S_{diff}t_d$. Cadence simulations of the differential ramp rate change ΔS_{diff} over the valid current source output differential range of the first stage from $250mV$ to $750mV$ for each bias current are shown in Table 4.1. The differential ramp rate change ΔS_{diff} is used to estimate the maximum overshoot variation $v_{ov_{MAX}}$ over the valid current source output range form $250mV$ to $750mV$ for a ZCD delay $t_d = 200ps$. In the simulations both finite output resistance and nonlinear output capacitance contribute to the ramp rate variation over the output range of the pipeline stage. The corresponding accuracy referred to the input of the ADC is shown for each bias setting based on the estimate of $v_{ov_{max}}(200ps)$. Based on Table 4.1, the estimated accuracy of the coarse phase K is used for the design of the fine phase opamp presented in the subsequent sections (refer to Subsection 4.3.2.5).

	I_{min}	I_{mid}	I_{max}
$I_{BIAS_{unit}}$	$33uA$	$52uA$	$72uA$
$I_{BIAS_{1st}}$	$2.1mA$	$3.3mA$	$4.6mA$
S_{diff}	$6.6(10^8)\frac{V}{s}$	$1.1(10^9)\frac{V}{s}$	$1.5(10^9)\frac{V}{s}$
$V_{OV_{diff}}(200ps)$	$132mV$	$220mV$	$308mV$
ΔS_{diff}	$7.2(10^6)$	$1.1(10^7)$	$1.8(10^7)$
$v_{ov_{max}}(200ps)$	$1.4mV$	$2.2mV$	$3.6mV$
K bits	10	9	8

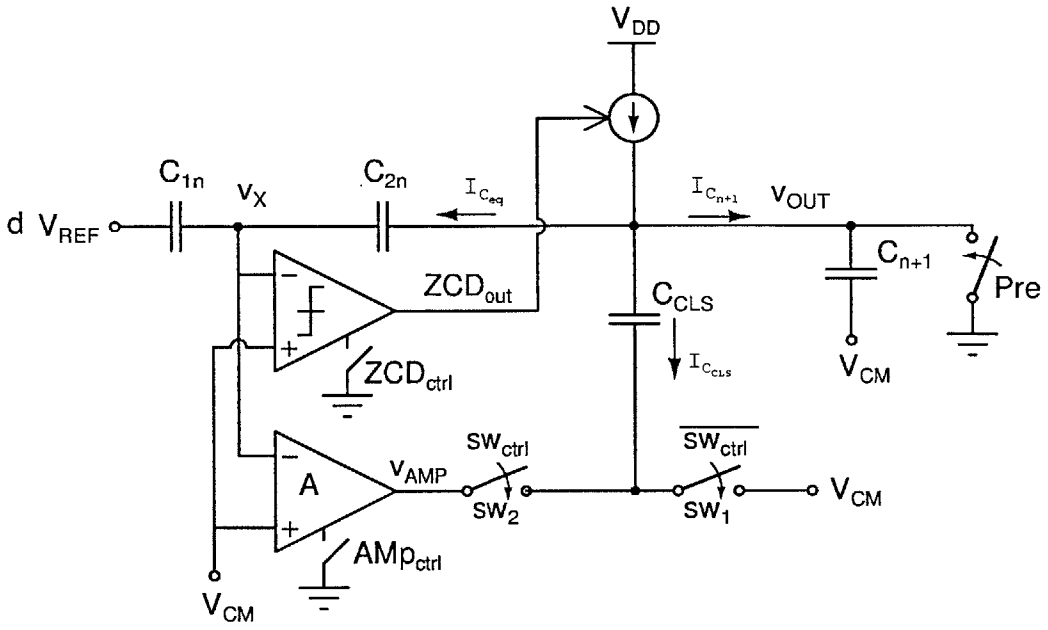
Table 4.1: Ramp rate variation ΔS_{diff} and overshoot error variation $v_{ov_{MAX}}$ over the valid differential output range of the current sources for the first pipeline stage design.

4.3 Opamp Design

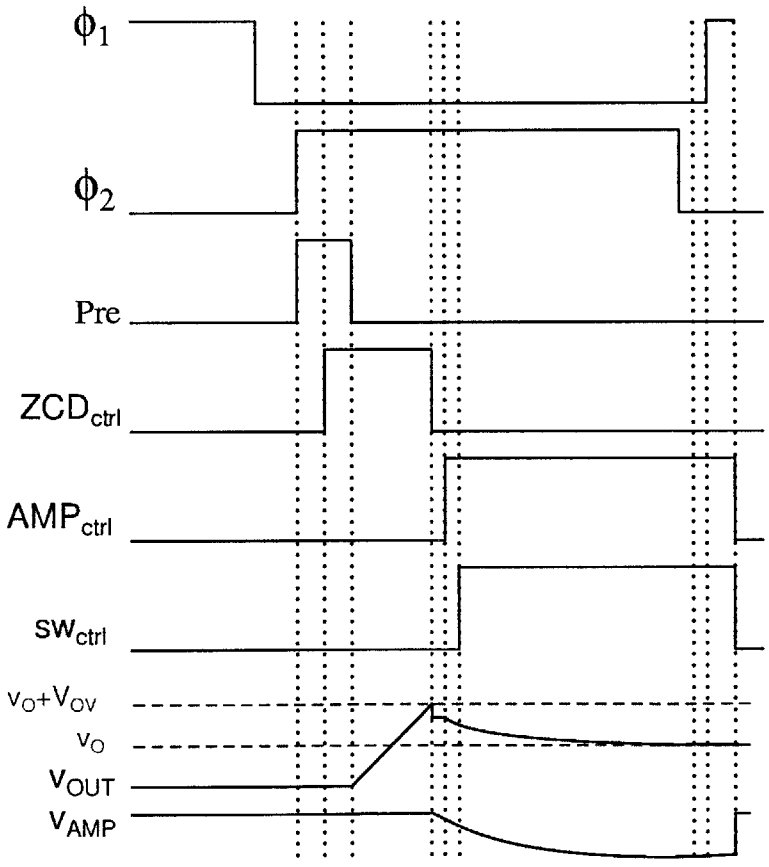
4.3.1 Top Level Description

In a hybrid CLS-OpAmp/ZCBC stage implementation of a pipelined ADC, the coarse ZCB phase serves as a fast approximation of the final output voltage and virtual

ground condition. During the fine phase, the opamp settles the output to its final value. At the end of the coarse phase of charge-transfer operation (refer to Figure 4-8a and Figure 4-8b), the ZCD detects the virtual ground condition (ZCD_{ctrl}). A delayed signal of the ZCD transition is generated to turn the ZCD off. In addition at the ZCD transition instant another signal is generated to turn the opamp on (AMP_{ctrl}) (Figure Figure 4-8b). As shown in Figure 4-8a, the level shifting capacitor C_{CLS} is charged during the coarse phase in parallel with the load capacitor $C = C_{1n} \parallel C_{2n} + C_{n+1}$ to a rough estimate of the final output voltage value. During the coarse ZCB phase the bottom plate of C_{CLS} is connected to V_{CM} through $sw1$ in Figure 4-8a. At the end of the coarse phase the bottom plate of C_{CLS} is disconnected from V_{CM} and connected to the output of the opamp through $sw2$. The voltage across the output sampling capacitor C_{CLS} is reset during the preset phase (Pre), in Figure 4-8b, every clock cycle to prevent the previous cycle level shifting voltage stored on C_{CLS} that introduces errors in the current value.



(a) Simplified diagram for the charge-transfer operation of a hybrid CLS-OpAmp/ZCBC circuit.



(b) Timing diagram and voltage waveforms at nodes v_{OUT} and v_{AMP} during the charge-transfer phase φ2.

Figure 4-8: Hybrid CLS-OpAmp/ZCB charge-transfer phase operation

4.3.2 Opamp Specifications

The attainable precision of the fine opamp phase is determined by the opamp gain, bandwidth and noise contribution. The error contribution of each will be considered in detail in this section.

4.3.2.1 DC Gain and Bandwidth

The stage output v_{OUT} is level shifted from opamp output v_{AMP} through capacitor C_{CLS} as shown in Figure 4-9. As discussed in Chapter 2, finite ZCD delay, finite output resistance and nonlinear output capacitance of the current sources results in an output voltage overshoot error at v_{OUT}, which can be expressed as a function of the ideal output voltage v_O and ZCD delay t_d by Eq. 2.14 in Chapter 2, the truncated version of which is repeated here for convenience:

$$v_{ov}(v_O, t_d) = \frac{I_0}{C} t_d - \frac{v_O(t) t_d}{R_O C}. \tag{4.6}$$

In Eq. 4.6, the effect of nonlinear parasitic capacitance is ignored for simplicity.

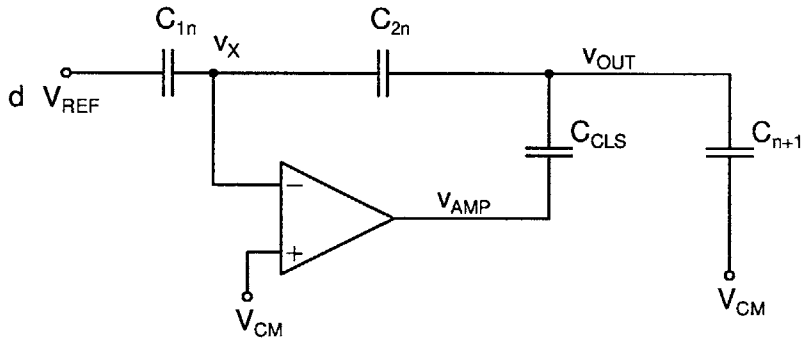


Figure 4-9: Fine opamp-based charger-transfer phase

The output voltage at the end of the coarse ZCB phase can thus be expressed as:

$$v_{OUT} = v_O + V_{OV} + v_{ov}$$

where v_O is the ideal output voltage at the end of the charge-transfer phase, V_{OV} is the constant component of the overshoot error (the first term in Eq. 4.6) and v_{ov} is the

output-dependent component of the overshoot error $v_{ov} = f(v_{OUT})$, corresponding to the the second term in Eq. 4.6. The constant overshoot error can be corrected using offset-cancellation circuit techniques and is assumed for the analysis here to be $V_{OV} = 0$. In the presence of constant overshoot error correction, the opamp must remove only the output-dependent error v_{ov} at v_{OUT} incurred at the end the coarse phase. Therefore an opamp output range, sufficient only to allow for the maximum output-dependent overshoot error is required.

At the beginning of the fine charge-transfer phase the initial voltage error to be corrected by the opamp is (assuming the start of the fine phase occurs at $t = t_0$):

$$v_{out}(t = t_0) = v_{ov}.$$

The voltage at the input of the opamp at the beginning of the fine charge-transfer phase is:

$$V_X = V_{CM} + \beta v_{ov}$$

where $\beta = \frac{C_{2n}}{C_{2n}+C_{1n}}$ is the feedback factor from the output to the input of the opamp. The output-dependent error at node v_X, at $t = t_0$ is:

$$v_x(t = t_0) = \beta v_{ov}.$$

At the instant, before the opamp is turned on, the opamp output is:

$$V_{AMP} = V_{CM}$$

and

$$v_{amp}(t = t_0) = 0.$$

During the fine phase, from Section 2.4.4, the waveform at the opamp input voltage

is:

$$v_X(t) = V_{CM} + \beta v_{ov}(\frac{1}{1+A\beta\gamma} + \frac{A\beta\gamma}{1+A\beta\gamma} e^{-\frac{t(1+A\beta\gamma)}{\tau}}), \tag{4.7}$$

the output voltage waveform is:

$$v_{OUT}(t) = V_O + v_{ov}(\frac{1}{1+A\beta\gamma} + \frac{A\beta\gamma}{1+A\beta\gamma} e^{-\frac{t(1+A\beta\gamma)}{\tau}}), \tag{4.8}$$

and the opamp output is:

$$v_{AMP}(t) = -v_{ov}(\frac{A\beta}{1+A\beta\gamma})(1 - e^{-\frac{t(1+AK)}{\tau}}), \tag{4.9}$$

where A is the DC gain of the opamp, $\tau = \frac{1}{\omega_{3dB}}$ is the opamp time constant, assuming the opamp is a first order linear system and ω_{3dB} is the open loop opamp bandwidth. The coefficient γ is the attenuation factor from the opamp output voltage v_{AMP} to the stage output v_{OUT} (refer to Figure 4-9).

The size of the output-dependent overshoot error v_{ov} determines the lower bound on the DC gain A and closed-loop bandwidth $w_{cl} = \frac{1}{\tau_{cl}}$ of the opamp. Assume the linearity of the output of a pipeline ADC stage must be M bits. In addition assume that the coarse phase provides output linearity of K bits. Then the opamp has to have sufficient gain and sufficient bandwidth to attenuate and settle the output voltage error v_{ov} and ensure the output voltage v_{OUT} is linear to M bits at the end of the charge-transfer phase. Let $L = M - K$. For a given ADC sampling rate f_s and fine phase L-bit linearity requirement, the opamp DC gain A and open loop bandwidth $\omega = \frac{1}{\tau}$ can be determined from the residual error at the output voltage node v_{OUT} at the end of the fine phase ($t = t_1$):

$$v_{out}(t_1) = v_{ov}(\frac{1}{1+A\beta\gamma} + \frac{A\beta\gamma}{1+A\beta\gamma} e^{-\frac{t_{fine}(1+A\beta\gamma)}{\tau}}) \tag{4.10}$$

where $t_{fine} = t_1 - t_0$ is the fine phase duration.

- **Opamp DC gain**

The first term of Eq. 4.10 represents the DC error remaining after the opamp has fully settled and is due to the finite opamp DC gain A. The minimum opamp gain for the required fine phase linearity of L bits can be derived from:

$$\frac{v_{ov}}{1+A\beta\gamma} \leq \frac{v_{ov}}{2^{L+1}}$$

$$1+A\beta\gamma \geq 2^{L+1}$$

$$A \geq \frac{2^{L+1}-1}{\beta\gamma}. \tag{4.11}$$

The fine phase opamp of the first stage of an N-bit pipelined ADC has the most stringent requirement as the maximum output nonlinearity error of first stage referred to the ADC input has to be $< \frac{V_{LSB}}{2}$ (where $V_{LSB} = \frac{V_{FS}}{N}$ is the ideal code width of the ADC with full scale input range V_{FS} and N-bit resolution) [10, ?]:

$$v_{out}(t_1) < \frac{V_{FS}}{2^{N+1}} G_1, \tag{4.12}$$

where $G_1 = 4$ is the gain of the first stage in this prototype, $V_{FS} = 1.75V$ is the ADC full scale input and the target accuracy is $N = 13$. From Eq. 4.12 it follows that the first stage output error at the end of the fine phase has to be $v_{out}(t_1) = \frac{V_{FS}}{2^{N+1-2}} = \frac{V_{FS}}{2^{N-1}} < 427uV$. In addition from Eq. 4.12, the first stage output linearity requirement from $(\frac{V_{FS}}{2^{N+1}})2^2 = \frac{V_{FS}}{2^{(N-2)+1}}$ is $M = N-2 = 11$ bits for $\frac{1}{2}V_{LSB}$ accuracy. As the gain of every subsequent stage G_n is also 4, it can be generalized that the output of stage n must satisfy $M_n = N - 2n$ for an N-bit pipelined ADC with $G_n = 4$.

For simplicity it is assumed that the ramp rate and ZCD delay are identical for all

stages of the pipelined ADC. It then follows that the coarse phase K-bit nonlinearity can be assumed for all stages to first order. Therefore, $L_n = M - K = N - 2n - K$ for $G_n = 4$. The minimum fine phase opamp DC gain requirement can then be found by substituting L_n into Eq. 4.11 for stage n is then:

$$A \geq \frac{2^{N-2n-K+1} - 1}{\beta\gamma}. \tag{4.13}$$

- **Opamp bandwidth**

The second term of Eq. 4.10 is due to the finite bandwidth of the opamp and can be used to find the minimum closed-loop bandwidth τ_{cl} of the fine phase opamp of the pipeline stage for a desired sampling frequency f_s and resolution N of the ADC. By design the fine phase duration is allocated $\frac{2}{3}$ of $\frac{T_s}{2}$, where T_s is the sampling period. It is assumed that the term $\frac{A\beta\gamma}{1+A\beta\gamma} \simeq 1$ for simplicity of the analysis (which holds if $A\beta\gamma \gg 1$). Then for a fine phase duration:

$$t_{fine} \simeq \frac{2}{3}\frac{T_s}{2} \simeq \frac{T_s}{3} \tag{4.14}$$

the output error will exponentially diminish to a value smaller than the required fine phase error corresponding to output linearity of L bits. The term $\frac{\tau}{(1+A\beta\gamma)}$ is the opamp closed-loop time constant τ_{cl}. For purposes of the following derivation, linearity of $L+1$ bits is assumed, in order to allow for enough error margin for the opamp gain error contribution to the output nonlinearity of the stage. Thus from the fine phase linearity requirement an expression for the closed-loop time constant τ_{cl} can be derived:

$$v_{ov} e^{-\frac{t_{fine}}{\tau cl}} \leq \frac{v_{ov}}{2^{L+1}} \tag{4.15}$$

$$e^{\frac{t_{fine}}{\tau cl}} \geq 2^{L+1} \tag{4.16}$$

$$\frac{t_{fine}}{\tau_{cl}} \geq (L+1)\ln 2 \tag{4.17}$$

$$\tau_{cl} \leq \frac{t_{fine}}{(L+1)\ln 2}. \tag{4.18}$$

Substituting Eq. 4.14 into Eq. 4.18 yields an expression for the minimum required closed-loop time constant τ_{cl} for an ADC sampling period T_s:

$$\tau_{cl} \leq \frac{\frac{1}{3}T_s}{(L+1)\ln 2}. \tag{4.19}$$

The closed-loop bandwidth for the n^{th} pipeline stage of an N-bit ADC, of gain $G_n = 4$ and fine phase linearity requirement $L_n = N - 2n - K$ is then:

$$\tau_{cl} \leq \frac{\frac{1}{3}T_s}{(N-2n-K+1)\ln 2}. \tag{4.20}$$

Note that in the case of a bidirectional ramp ZCB coarse phase implementation the overshoot error changes polarity and the output voltage at the end of the fine phase ($t = t_1$) from Eq. 4.10 is:

$$v_{out}(t_1) = \begin{cases} v_{ov}(\frac{1}{1+A\beta\gamma} + \frac{A\beta\gamma}{1+A\beta\gamma}e^{-\frac{t_{fine}(1+A\beta\gamma)}{\tau}}), & v_{OUT} < V_{CM} \\ -v_{ov}(\frac{1}{1+A\beta\gamma} + \frac{A\beta\gamma}{1+A\beta\gamma}e^{-\frac{t_{fine}(1+A\beta\gamma)}{\tau}}), & v_{OUT} > V_{CM} \end{cases}. \tag{4.21}$$

It is clear from Eq. 4.21 that the residual error at the output of the ADC pipeline stage changes polarity with output voltage. However, the absolute magnitude of the output error at the end of the fine phase is unchanged and the above analysis for the fine phase opamp design requirements still holds.

4.3.2.2 Output Voltage Range

The relationship between the stage output v_{out} and the opamp output v_{amp} (refer to Figure 4-9) is determined by the choice of level shifting capacitor C_{CLS},

$$\frac{v_{out}}{v_{amp}} = \frac{C_{CLS}}{C_{CLS}+C} = \gamma,$$

where

$$C = C_{n+1} + C_{2n} \parallel C_{1n}$$

Note that the opamp output parasitic capacitor is small compared to the load capacitor for this particular design and is ignored in this analysis. For large values of C_{CLS}, $v_{amp} \simeq v_{out}$ (refer to Eq. 4.22) and the opamp output swing has to accommodate the maximum output-dependent overshoot error $v_{ov_{MAX}}$. When $C_{CLS} = C$, then $\gamma = \frac{1}{2}$ and the opamp output swing has to accommodate two times the maximum output-dependent overshoot error $2v_{ov_{MAX}}$. As the size of the level shifting capacitor decreases further with respect to C, the attenuation factor γ increases and the opamp output swing requirement grows proportionately to $\frac{1}{\gamma}v_{ov_{MAX}}$, as shown in Eq. 4.22.

$$\frac{1}{\gamma} = \begin{cases} 1, & C_{CLS} \gg C \\ 2, & C_{CLS} = C \\ \simeq \frac{C}{C_{CLS}}, & C_{CLS} \ll C \end{cases} \tag{4.22}$$

The coarse phase current source power dissipation scales up with larger values of C_{CLS} (refer to Figure 4-8b). The total coarse phase current I_{coarse} is (refer to Figure 4-8a) :

$$I_{coarse} = I_C + I_{C_{CLS}} = S(C + C_{CLS}),$$

where S is the coarse phase output ramp rate. Therefore larger C_{CLS} alleviates the opamp output range specification but increases the coarse phase power consumption. The minimum of the function $f(C_{CLS}) = v_{amp}I_{coarse} = \left(v_{ov_{MAX}}\frac{C_{CLS}+C}{C_{CLS}}\right)(I(C + C_{CLS})$, occurs at $C = C_{CLS}$ as shown in Appendix D. Therefore $\gamma = 2$ is chosen for the prototype ADC.

The attenuation factor γ and the maximum output dependent overshoot error $v_{ov_{max}}$ set the range requirement for the opamp output

$$\mid v_{amp} \mid = \mid \frac{v_{ov_{MAX}}}{\gamma} \mid, \tag{4.23}$$

where the maximum output-dependent overshoot error $v_{ov_{max}}$ occurs at the maximum swing of the stage output voltage $V_{OUT_{FS}}$ and from Eq. 4.6

$$\mid v_{ov_{MAX}} \mid = \mid \frac{t_d V_{OUT_{FS}}}{R_O C} \mid . \tag{4.24}$$

where R_O is the current source output resistance and can be expressed as $R_O = \frac{I_{coarse}}{V_A}$, where V_A is the early voltage of the current source. Substituting for R_O in Eq. 4.24 results in:

$$\mid v_{ov_{MAX}} \mid = \mid \frac{t_d V_{OUT_{FS}} I_{coarse}}{V_A C} \mid$$

$$\mid v_{ov_{MAX}} \mid = \mid \frac{t_d V_{OUT_{FS}} S}{V_A} \mid \tag{4.25}$$

where S is the coarse phase ramp rate . Substituting Eq. 4.25 into Eq. 4.23 yields the minimum opamp output range requirement:

$$v_{amp} = \frac{t_d S V_{OUT_{FS}}}{\gamma V_A}. \tag{4.26}$$

The first stage opamp output range requirement given the parameter in Table 4.1 is discussed in Subsection 4.3.2.5.

- **Effect of level shifting capacitor C_{CLS} on closed loop DC gain and bandwidth**

In the fine phase analysis thus far, the opamp was assumed to have a first order system response with DC gain A, open loop bandwidth $\omega_{3dB} = \frac{1}{\tau}$, unity gain bandwidth

$\omega_u = A\omega_{3dB}$, and a single pole p located at:

$$p = -\frac{1}{R_{amp}C_{load}}$$

where R_{amp} is the opamp output resistance, assuming a single stage opamp for simplicity and $C_{load} = C_{p_{amp}} + (C_{CLS} \parallel (C_{n+1} + C_{eq})$,where $C_{p_{amp}}$ is the output parasitic capacitance of the opamp and $C_{eq} = C_{1n} \parallel C_{1n}$. In the prototype ADC, $C_{p_{amp}}$ is much smaller than $C_{CLS} \parallel (C_{n+1} + C_{eq})$ and is ignored here for simplicity and

$$C_{load} = C_{CLS} \parallel (C_{n+1} + C_{eq}). \tag{4.27}$$

The open loop opamp bandwidth $\omega_{3dB}$is then:

$$\omega_{3dB} = \frac{(C_{CLS} + C_{n+1} + C_{eq})}{R_{amp}C_{CLS}(C_{n+1} + C_{eq})}.$$

The closed loop gain G_{CL} of the fine phase opamp in feedback in Figure 4-9 can then be expressed as:

$$G_{CL} = \frac{1}{\gamma\beta} = \frac{(C_{CLS} + C_{n+1} + C_{eq})(C_{1n} + C_{2n})}{C_{CLS}C_{2n}}$$

and the opamp closed loop bandwidth ω_{CL} is:

$$\begin{aligned}
\omega_{CL} &= \frac{\omega_u}{G_{CL}} \\
&= \frac{A\omega_{3dB}}{\frac{1}{\gamma\beta}} \\
&= A\beta\gamma\omega_{3dB} \\
&= A\beta\left(\frac{C_{CLS}}{C_{CLS} + C_{n+1} + C_{eq}}\right)\left(\frac{C_{CLS} + C_{n+1} + C_{eq}}{R_{amp}C_{CLS}(C_{n+1} + C_{eq})}\right) \\
&= A\beta\left(\frac{1}{R_{amp}(C_{n+1} + C_{eq})}\right)
\end{aligned}$$

Note that the closed loop bandwidth ω_{CL} for a fixed R_{amp} is independent of the level shifting capacitor C_{CLS} and that independence holds only under the assumption that the parasitic output capacitance of the opamp $C_{P_{AMP}} \ll C_{CLS} \parallel (C_{n+1} + C_{eq})$.

4.3.2.3 Thermal Noise

For an opamp in a hybrid CLS-OpAmp/ZCBC pipeline stage implementation, with finite gain A and time constant τ, the thermal noise power spectral density at the output of the opamp during the fine charge-transfer phase (refer to Figure 4-10) is:

$$v_{no}^2 = v_{ni}^2 \left(\frac{1}{\beta'} \left(\frac{A\gamma\beta'}{1 + A\beta'\gamma} \right) \left(\frac{1}{1 + s\tau_{cl}} \right) \right)^2 \tag{4.28}$$

where v_{ni}^2 is the input-referred opamp thermal noise power spectral density, β' is the feedback factor:

$$\beta' = \frac{C_{2n}}{C_{P_{in}} + C_{1n} + C_{2n}}$$

and $\tau_{cl} = \frac{\tau}{1+A\gamma\beta'}$ is the closed-loop time constant. Note that the opamp input parasitic capacitor $C_{P_{in}}$ increases the output noise and for that reason is included in this analysis. The feedback factor β' decreases as $C_{P_{in}}$ increases. If $C_{P_{in}} = 0$, then $\beta' = \beta = \frac{C_{2n}}{C_{1n}+C_{2n}}$ and from Eq. 4.28, the noise power gain is minimum. Let :

$$\lambda = \frac{1}{\beta'} \left(\frac{A\gamma\beta'}{1 + A\gamma\beta'} \right),$$

Then the total integrated thermal noise power at the opamp output at the end of the fine charge transfer phase is:

$$\overline{v_{no}^2} = \lambda^2 \int_0^\infty \frac{v_{ni}^2 df}{\left(1 + \left(\frac{f}{f_{cl}}\right)^2\right)} \tag{4.29}$$

$$= \bar{v_{ni}^2} (\lambda^2 \frac{\pi}{2} f_{cl}) \tag{4.30}$$

where $f_{cl} = \frac{1}{2\pi\tau_{cl}}$ is the opamp closed-loop bandwidth.

To establish the maximum allowed total thermal noise contributed by the fine phase opamp at the output of an n^{th} stage of an N-bit pipelined ADC, the noise is referred to the input of the ADC. If the signal gain of an n^{th} pipeline stage is G_n, and all stages have the same gain, then the aggregate gain from the ADC input to the output of stage n is $G_{tot} = \Pi_{k=1}^{n} G_k$. The maximum ADC input-referred mean-square thermal noise power contributed by the fine phase opamp in stage n must be less than the ADC quantization noise power to maintain the ADC SNR as discussed in 4.1.1.1. When the thermal noise power is equal to the quantization noise power, the SNR of the ADC degraded by $3dB$. Recall that for an ADC, the root-mean-square quantization noise power is $\frac{\left(\frac{V_{FS}}{2^N}\right)^2}{12}$ [10]. Taking the square root of both the input-referred mean-square noise power and mean-square quantization noise power yields:

$$\frac{1}{G_{tot}}\sqrt{\overline{v_{no}^2}} < \left(\frac{V_{FS}}{2^N\sqrt{12}}\right)$$

and

$$\sqrt{\overline{v_{no}^2}} < \left(\frac{V_{FS}}{2^N\sqrt{12}}\right) G_{tot} \tag{4.31}$$

where V_{FS} is the full scale input range of the ADC. From Eq. 4.31 the maximum allowed output-referred opamp noise voltage for the fine phase of the first stage of the prototype ADC is $246uV$. Substituting Eq. 4.30 into Eq. 4.31 yields an expression for the input referred root-mean-square noise density:

$$\sqrt{\overline{v_{ni}^2} T^2 \frac{\pi}{2} f_{cl}} < \left(\frac{V_{FS}}{2^N\sqrt{12}}\right) G_{tot}$$

$$\sqrt{\overline{v_{ni}^2}} < \frac{1}{\sqrt{\lambda^2 \frac{\pi}{2} f_{cl}}} \left(\frac{V_{FS}}{2^N\sqrt{12}}\right) G_{tot}.$$

Table 4.2: Summary of opamp specifications

Specification	Value
Gain (A)	$> \frac{2^L-1}{\beta\gamma}$
Settling time (τ) [s]	$> \frac{\frac{1}{3}T_s}{(L+1)\ln 2}(1+A\beta\gamma)$
Input-referred thermal noise $\left(\sqrt{\bar{v}_{ni}^2}\right)$ $[\frac{V}{\sqrt{Hz}}]$	$< \frac{1}{\sqrt{\lambda^2 \frac{\pi}{2} f_{cl}}} \left(\frac{V_{FS}}{2^N\sqrt{12}}\right) G_{tot}$
Output voltage range (v_{amp}) [V]	$> \frac{t_d S V_{OUT_{FS}}}{\gamma V_A}$

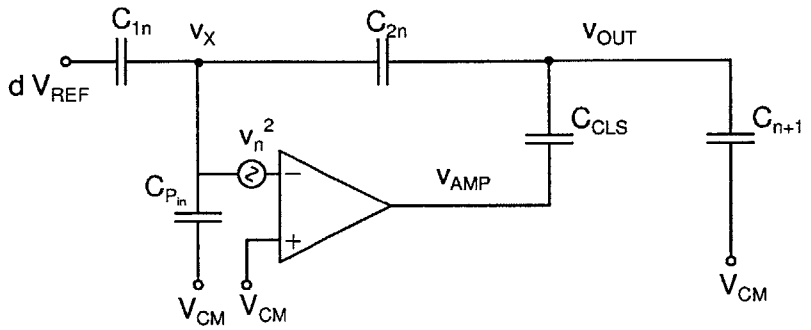


Figure 4-10: Fine phase opamp input parasitic capacitor C_P increases the total integrated thermal noise at v_{OUT}.

4.3.2.4 Summary

Table 4.2 summarizes the opamp specifications required for a fine charge-transfer phase with output linearity up to L bits, for a sampling period T_s and coarse phase ramp rate S. Note that the analysis was done for a single-ended case.

4.3.2.5 First Stage Design Considerations

The opamp specifications of the first pipeline stage are dictated by the desired ADC accuracy and more specifically the output linearity of the first stage. In addition the opamp specifications are constrained by the first stage coarse phase output linearity. For an N-bit ADC accuracy the input referred error must be $\varepsilon_{IN} \leq \frac{V_{FS}}{2^{N+1}}$, where V_{FS} is the ADC input range and N is the ADC resolution [40, 28]. To achieve $N = 13$ bits accuracy, assuming $V_{FS} = 1.75V$, first stage gain $G_1 = 4$ and 3-bit sub-ADC, the error at the output of the first stage ε_1 must be:

$$\varepsilon_1 < \frac{V_{FS}G_1}{2^{N+1}} \tag{4.32}$$
$$<427\mu V.$$

Cadence simulations of the error due to the finite current source resistance of the first stage current sources and nonlinear output capacitance showed better than 8 bits of linearity ($K > 8$) at the largest unit bias current of $72uA$ (refer to Table 4.1) at the end of the coarse charger-transfer phase using a bidirectional ZCB implementation. As a reference, previous single phase ZCB pipelined ADC implementations [6, 9] in $90nm$ CMOS with a first stage 3-bit sub-ADC and first stage gain of $G_1 = 4$, have attained 10-bit linearity up to 100MS/s with a unidirectional ZCB implementation. The differential ramp rate in [6, 9] is on the order of $S_{diff} \simeq 2(\frac{1V}{4ns}) = 5(10^8)\frac{V}{s}$ for a sampling period of $10ns$, which is comparable to the minimum bias current ramp rate of this design. Therefore it is conservative to assume a nominal 8-bit coarse phase linearity for this design.

Table 4.3 presents a summary of circuit design parameter requirements for the fine phase opamp of the first pipeline stage of a 13-bit pipelined ADC operating at 100MS/s. The fine phase linearity has been assumed up to $L = 2$, $L = 3$ and $L = 4$ bits for each case of coarse phase linearity of $K = 9$, $K = 8$ and $K = 7$ for a fixed first stage output linearity requirement of $M = 11$ (refer to Eq. 4.32). The sampling period T_s is assumed to be 10ns for 100MS/s sampling rate. From Eq. 4.14 the fine phase duration t_{fine} is assumed to be $\sim \frac{1}{3}T_s$. For a stage gain of $G_1 = 4$, the feedback factor β is $\frac{1}{4}$. The attenuation factor from the opamp output to the stage output is $\gamma = \frac{1}{2}$. Therefore the attenuation in this particular design from the opamp output to the opamp input is $\frac{1}{8}$. The parameter num_τ represents the number of closed-loop time constants for settling, and ω_u is the unity-gain bandwidth of the opamp and is computed from $\tau = \tau_{cl}(1 + A\beta\gamma)$, where τ the opamp bandwidth and $\omega_u = \frac{A}{\tau}$. The opamp gain requirement is calculated using Eq. 4.13. The closed-loop bandwidth τ_{cl}

is computed using Eq. 4.18. The parameter $v_{amp} = \frac{v_{ov_{MAX}}}{\gamma}$ is the fully differential opamp output voltage swing assuming the constant overshoot error V_{OV} is canceled as described in Chapter 3. The value of $v_{ov_{MAX}}$ was estimated as $v_{ov_{MAX}} = 2(\frac{V_{FS}}{2^K})$ to allow a margin of error.

L	2	3	4
K	9	8	7
A	$35dB$	$42dB$	$48dB$
num_τ	3	4	5
τ_{cl}	$1.1ns$	$0.85ns$	$0.65ns$
ω_u	$2\pi(1.15GHz)$	$2\pi(1.5GHz)$	$2\pi(1.87GHz)$
v_{amp}	$7mV$	$14mV$	$27mV$

Table 4.3: Fully-differential opamp specifications for 3-bit,4-bit and 5-bit fine phase accuracy.

From A and v_{amp} in Table 4.3 it is clear that the output range allows for a telescopic opamp implementation even with a limited positive supply voltage of $1V$. The parameter $v_{amp} = \frac{v_{ov_{MAX}}}{\gamma}$ is the fully differential opamp output voltage swing assuming the constant overshoot error V_{OV} is canceled as described in Chapter 3. In this particular design a very conservative approach was taken with $\sim 200mV$ output range. It is an oversight in the prototype of the ADC that the load of the telescopic opamp was not double cascoded. Double cascoding the load of a telescopic opamp constrains the output range to $V_{DD} - 3V_{DSAT} - V_{CM}$, where it is assumed that all load devices have the same V_{DSAT}, and the output common mode voltage is at mid-rail (V_{CM}). In the prototype ADC $V_{DSAT} = 160mV$, which results in $V_{DD} - 3V_{DSAT} - V_{CM} = 20mV$ for a supply of $1V$, which is smaller than the maximum value in Table 4.3. The overdrive voltage V_{DSAT} can be reduced while biasing the load devices closer to weak inversion, which would have allowed for sufficient swing and improved the DC gain of the opamp.

4.3.3 Choice of Opamp Topology

The opamp topology is dictated by the gain, speed and output swing necessary to bring the approximate coarse phase output of the pipeline stage to a more precise estimate of the ideal output. A single stage telescopic opamp meets the above specifications. It provides a boost in gain through cascoding at the cost of limited output swing and has better noise performance than a folded cascode opamp [34].

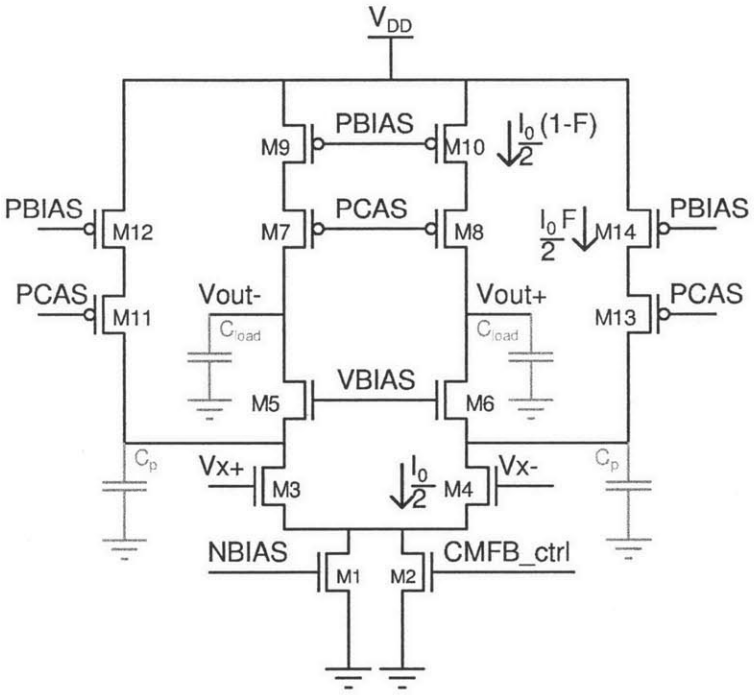


Figure 4-11: Modified telescopic opamp

A variation of the standard telescopic topology (refer to Figure 4-12) offers improvements in opamp noise and gain at no significant speed detriment and preserves the output range of the opamp for the same total current (refer to Figure 4-11). A fraction F of $\frac{I_0}{2}$, where I_0 is the opamp tail current is steered through the side branches ($M11$, $M12$, $M13$, $M14$). For the purpose of comparison, the standard topology and this topology are assumed to be designed to have the same bias current, same voltage output range of operation, input device and main branch device sizes. For simplicity the analysis below only considers the equivalent differential half circuit.

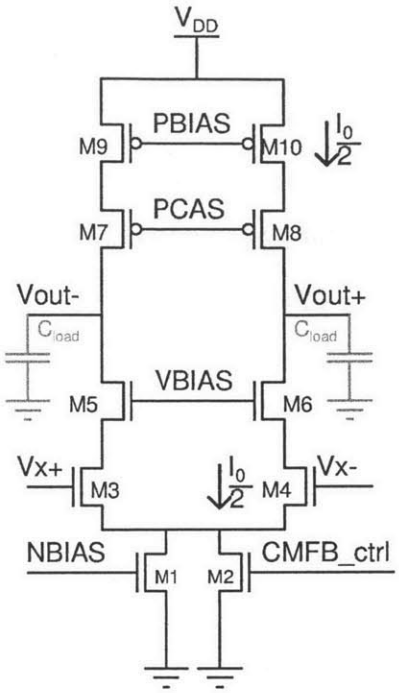


Figure 4-12: Telescopic opamp

- **Thermal Noise**

For simplicity it is assumed that in Figure 4-12 all load PMOS devices ($M7 - M10$) and NMOS cascode devices ($M5$ and $M6$) and the equivalent devices in Figure 4-11 have the same transconductance g_m. The input devices ($M3$ and $M4$) have a transconductance $g_{m_{M3}} = g_{m_{M4}} = g_{m_{in}}$ and output resistance $r_{0_{M3}} = r_{0_{M4}} = r_{0_{in}}$ in both figures. For the standard telescopic opamp, the cascode devices contribute negligible noise. The remaining contributing thermal noise sources are the input devices and the PMOS load devices $M9$ and $M10$, similar to the the case of a simple differential pair [10]:

$$v_{in}^2 = 2\left[\frac{8kT}{3g_{m_{M3}}}(1 + \frac{g_{m_9}}{g_{m_{M3}}})\right] \tag{4.33}$$

where v_{in}^2 is the equivalent input mean-square thermal noise power density. If the input devices are biased in weak inversion to reduce thermal noise then:

$$v_{in}^2 = 2\left[\frac{2kT}{g_{m_{M3}}}(1+\frac{4g_{m_9}}{3g_{m_{M3}}})\right]. \tag{4.34}$$

The main difference from a thermal noise standpoint between a differential pair and a standard telescopic opamp is the ratio of the transconductance of the PMOS load devices to the transconductance of the input devices. In the simple differential pair case the load devices can be scaled down in width and thus carry higher current density trading off range for reduced noise with $\frac{g_{m_{M9}}}{g_{m_{M3}}} \leq 1$. In the standard telescopic topology due to limited output range the load PMOS devices ($M7 - M10$) cannot be scaled as easily in width, which results in higher noise for the telescopic opamp as $\frac{g_{m_{M9}}}{g_{m_{M3}}} \approx 1$. Steering current away from the load devices ($M7 - M10$) in Figure 4-11 separates to a degree the noise and range trade-off in the standard telescopic opamp topology. Range is not limited for the side PMOS branches ($M11 - M14$) and that allows for scaling the width of devices ($M11 - M14$) down. In addition it allows more control over the ratio of the transconductance $g_{m_{M12}} = g_{m_{M14}}$ of the side branch devices $M12$ and $M14$ to the transconductance of the input devices $M3$ and $M4$, gm_{M3} to minimize the noise contribution of load devices $M12$ and $M14$.

For this analysis it is assumed that $M9$ and $M10$ have the same current density as that in an equivalent standard telescopic opamp, and their transconductance is proportional to the current $\frac{I_0}{2}(1-F)$. The cascode devices $M5$, $M6$, $M7$, $M8$, $M11$ and $M13$ are assumed to contribute negligible noise. The equivalent input thermal noise power density for the modified telescopic opamp topology is, assuming the input devices are biased in their square law region of operation:

$$v_{in}^2 = 2\left[\frac{8kT}{3g_{m_{M3}}}(1+\frac{(1-F)g_{m_{M9}}}{g_{m_{M3}}}+\frac{Fg_{m_{M12}}}{g_{m_{M3}}})\right].$$

If the input devices can be scaled up to be operating in weak inversion to further reduce the input referred thermal noise density:

$$v_{in}^2 = 2\left[\frac{2kT}{g_{m_{M3}}} + \frac{8kT}{3g_{m_{M3}}}\left(\frac{(1-F)g_{m_{M9}}}{g_{m_{M3}}} + \frac{Fg_{m_{M12}}}{g_{m_{M3}}}\right)\right]$$

In the implementation of the modified telescopic opamp $F = 0.4$ and $g_{m_{M12}} = \frac{g_{m_{m9}}}{2}$, then:

$$v_{in}^2 = 2\left[\frac{2kT}{g_{m_{M3}}}\left(1 + \frac{4}{3}\left(\frac{0.6g_{m_{M9}}}{g_{m_{M3}}} + \frac{0.4(\frac{g_{m_{M9}}}{2})}{g_{m_{M3}}}\right)\right)\right]$$

$$v_{in}^2 = 2\left[\frac{2kT}{g_{m_{M3}}}\left(1 + \frac{4}{3}\left(\frac{0.8g_{m_{M9}}}{g_{m_{M3}}}\right)\right)\right]. \tag{4.35}$$

It is clear from Eq. 4.34 and Eq. 4.35, that the input referred thermal noise power density is reduced in the proposed modified topology.

As already discussed optimizing the fine phase opamp output range is not as stringent a requirement as in a conventional telescopic opamp implementation and the ratio $\frac{g_{m_{M9}}}{g_{m_{M3}}} < 1$ can be minimized. By design $\frac{g_{m_{M9}}}{g_{m_{M3}}} \approx 0.65$ and the thermal noise spectral density is:

$$v_{in}^2 \approx 2\frac{3(4kT)}{g_{m_{M3}}}.$$

- **DC Gain**

The DC gain of the standard telescopic opamp is $G = -g_{m_{M3}}R_{out}$, where R_{out} is the output resistance of the opamp, $R_{out} = R_{outp} \| R_{outn}$ and $R_{outp} = R_{outn} = r_{0_{M9}}(g_{m_{M7}}r_{0_{M7}} + 1) = R$, therefore $R_{out} = \frac{R}{2}$ and $G = -g_{m_{M3}}\frac{R}{2}$. When a fraction F of the current is steered through the side PMOS branches bypassing the output of the opamp, the gain of the modified telescopic opamp G_F is:

$$G_F = -g_{m_{M3}} R_{outF}$$

where $R_{outF} = R_{outpF} \| R_{outnF}$ is the output resistance of the modified telescopic opamp and can be represented as a function of the standard telescopic opamp output resistance and F as follows:

$$R_{outpF} = \frac{R_{outp}}{(1-F)\sqrt{(1-F)}}$$

$$R_{outnF} = \frac{R_{outn}}{\sqrt{(1-F)}}$$

$$R_{outF} = \frac{R}{\sqrt{(1-F)}(2\text{-F})},\ R = R_{outp} = R_{outn}$$

$$G_F = -g_{m_{M3}} R_{outF} = \frac{2G}{\sqrt{(1-F)}(2-F)}$$

Note that when $F = 0$, no current steering branches are present and all the tail current flows though the load devices in the standard telescopic opamp topology and $G_F = G$. When $F = 0.4$, $G_F = 1.6G$, or an improvement in gain of 4dB. Larger fraction of the bias current, steered away from the load results in larger gain improvement.

- **Range**

In the general case, the output range is the same as the one of the standard telescopic opamp since the load devices ($M7 - M10$) at the output are not scaled as are the side branch devices ($M11 - M14$). In the specific implementation of this topology range is less stringent and allowed for further reduction in noise.

- **Bandwidth**

The standard telescopic opamp unity gain bandwidth w_u for a load capacitor C_{load} is:

$$\omega_u = \frac{g_{m_{M3}}}{C_{load}}.$$

Although opamp output parasitic capacitance $C_{p_{amp}}$ is much smaller than the load capacitor C_{load} and had been ignored in the opamp bandwidth analysis thus far it is included here to present a general expression for the modified telescopic topology. When a fraction F of the tail current is steered away from the load in the modified telescopic opamp, the width of the load devices $M7 - M10$ and cascode devices $M5 - M6$ is reduced by a factor of $(1-F)$. As a result the output parasitic capacitance is scaled down by the same factor, which results in a slight improvement in bandwidth. In this particular design, however the load capacitor $\sim 1.5pF$ is significantly larger than the output parasitic capacitance $C_{p_{out}}$, which is $< 50fF$ and this improvement is negligible.

$$w_u = \frac{g_{m_{M3}}}{C_{load} + (1 - F) \cdot C_{p_{amp}}}$$

One drawback of this topology is that the parasitic poles at the respective drain of the input devices $M3$ and $M4$ move in and slow down the opamp for larger side branch currents and sets an upper bound on how large F can be. The parasitic pole $p = -\frac{g_{m_{M5}}}{Cp}$ (refer to Figure 4-11), where $g_{m_{M5}}$ is the transconductance of $M5$ and scales by a factor of $(1 - F)^{\frac{1}{2}}$, if $M5$ is biased in square law regime.

In Figure 4-13 the gain bandwidth plots for $F = 0$ and $F = 0.3$ are shown for a telescopic opamp, which meets the fine phase opamp requirements of the first pipelined ADC stage of this work.

- **Slew rate**

Another drawback of this design variation of the telescopic opamp is reduced slew rate by a factor of (1-F). In this specific design the opamp is expected to operate over a very limited output range around the mid-rail voltage V_{CM} to only correct the output dependent overshoot error. The operation of the ZCB coarse phase is comparable

to slewing in a standard opamp implementation of a pipeline stage. Therefore the function of this opamp is primarily to settle the small residual output error from the ZCB phase, assuming the constant part of the overshoot has been corrected. Thus the slew rate degradation does not affect this particular design. If the common mode feedback circuit is applied through $M9$ and $M10$ instead of the bias device $M2$, the slew rate is not limited.

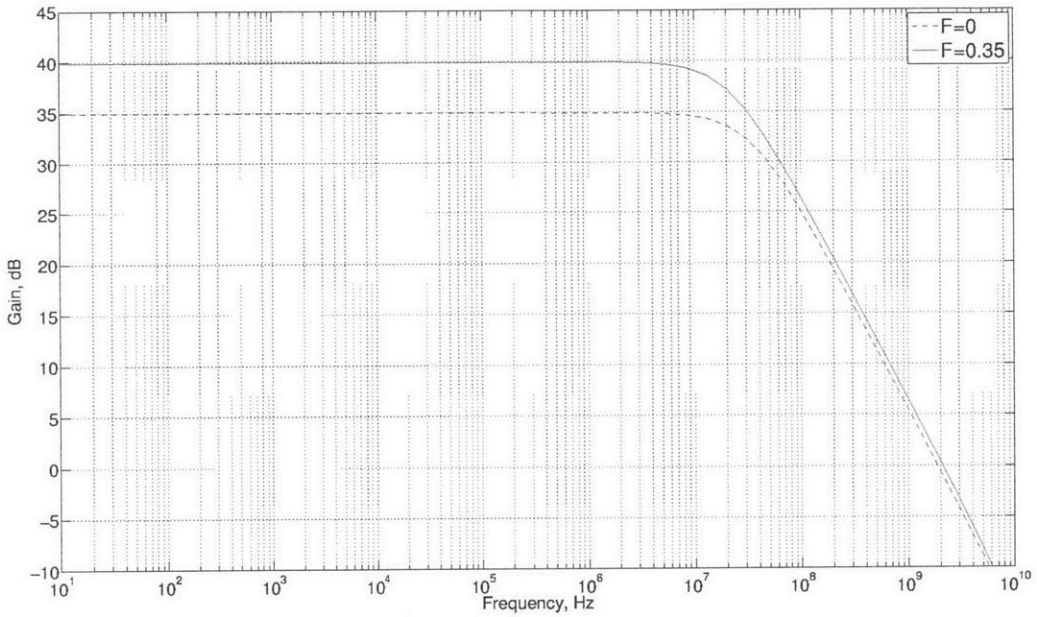


Figure 4-13: Gain bandwidth plot for a telescopic opamp for F=0 and F=0.35

4.3.4 Implementation

The opamp powers up only during the fine phase of the charge-transfer phase as shown in Figure 4-14. The opamp turn-on and turn-off is controlled through switches at the cascode nodes v_P and v_N in Figure 4-14 to V_{CAS} when the opamp is turned on and to the respective rail when the opamp is off. A standard switched capacitor common mode feedback (CMFB) circuit is used to regulate the common mode for the fully differential implementation of the opamp [10]. The opamp is turned on while

the outputs are still connected to V_{CM}, to prevent glitches due to clock feed-through at the output due the opamp starting up.

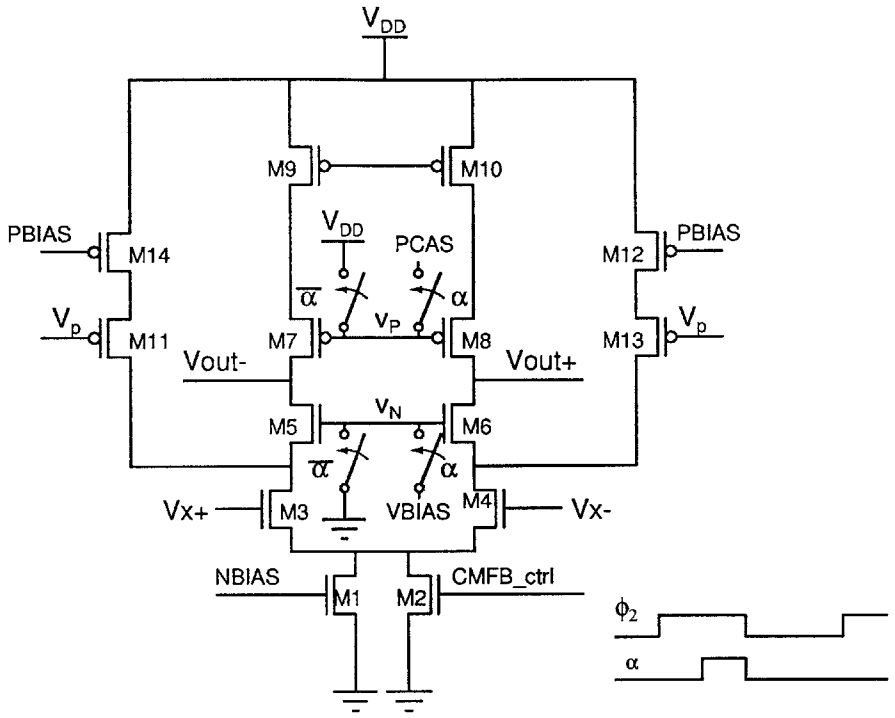


Figure 4-14: Opamp implementation. The control signal α turns on and off and on the opamp during the charge-transfer phase ϕ_2.

The first stage opamp was designed for flexibility to operate over a range of bias currents from $1.6mA$ to $3.6mA$. The nominal bias current of $2.6mA$ was chosen for a unity gain bandwidth of $\omega_u \simeq 2\pi(2GHz)$, for a load capacitance of $1.6pF$ and a gain of $\sim 40dB$ (refer to Figure 4-13). The length of all opamp devices just as the length of the ramp current source devices was chosen to be a factor of 2 that of a minimum length device of $65nm$ for improved output resistance and intrinsic gain. The width of the input devices was scaled up to reduce flicker noise, while keeping total parasitic capacitance introduced at the opamp inputs at a reasonable level. The total parasitic input capacitor is $< 5\%$ of the total sampling capacitor which is $6.8pF$ at each of the two inputs. The input parasitic capacitor increases the total output referred noise as shown in Section 4.3.2.3. From cadence simulations the total output-referred noise is $182uV$ which is less than the desired $246uV$ from Subsection 4.3.2.3.

The second stage and third stage input sampling capacitors, C_2 and C_3 respectively, are scaled by a factor of 4 with respect to their preceding stage $C_2 = \frac{1}{4}C_1$ and $C_3 = \frac{1}{4^2}C_1$. The second stage fine phase opamp drives an output load capacitance, which is $\frac{1}{4}$ that of the first stage input sampling capacitor C_1. Stages three through eight are identical and the fourth stage input sampling capacitor $C_4 = C_3$ is not scaled with respect to the third stage input sampling capacitor. The third stage fine phase opamp thus drives an output load capacitance C_{load_3} from Eq. 4.27:

$$C_{load_3} = C_{CLS_3} \parallel (C_4 + C_{13} \parallel C_{23}),$$

where $C_{CLS_3} = (C_4 + C_{13} \parallel C_{23})$, $C_4 = C_3 = \frac{1}{4}C_2$ and $C_{13} \parallel C_{23} \simeq \frac{1}{4}C_3 \simeq \frac{1}{4}(\frac{1}{4}C_2)$. Therefore $C_{load_3} \simeq \frac{1}{2}(C_4 + \frac{1}{4}C_3) \simeq \frac{1}{2}(\frac{5}{4})C_3 = \frac{5}{8}(\frac{1}{4}C_2) \sim \frac{1}{8}C_2$. The second and third stage opamp bias currents are scaled by the same amount as their respective load capacitors. The opamp unity gain bandwidth for a telescopic opamp is $\omega_u = \frac{g_{m_{M3}}}{C_{load}}$ (Figure 4-11), where $g_{m_{M3}}$ is the input device transconductance, which is proportional to the bias current I_0 when the input devices are biased in weak inversion and C_{load} is the opamp load. As both the load capacitor and bias current are scaled by the same factor, the unity gain bandwidth ω_u does not change.

4.4 ZCD Considerations

4.4.1 Background

The coarse phase performance of a hybrid CLS-OpAmp/ZCB ADC pipeline stage limits the overall output linearity of the stage. ZCBC output linearity is limited by the output dependent overshoot error, $v_{ov}(v_{OUT})$. The overshoot error is directly related to the ZCD delay t_d by:

$$v_{ov_{MAX}} = t_d \frac{V_{OUT_{FS}}}{t_{ramp}} \tag{4.36}$$

where $v_{ov_{MAX}}$ is the maximum magnitude of the output dependent overshoot error, t_{ramp} is the coarse phase ZCB ramp duration for a full swing output voltage $V_{OUT_{FS}}$

and $\frac{V_{OUT_{FS}}}{t_{ramp}} = \frac{dV_{OUT}}{dt}$ is the ZCB circuit ramp rate. From Eq. 4.36 it is clear that to achieve the minimum possible overshoot and best output nonlinearity for a fixed ramp rate, the goal of the ZCD design is to minimize the delay t_d.

In a hybrid CLS-OpAmp/ZCB 13-bit pipelined ADC with sampling period $T_s = 10ns$, the coarse phase by design is fast and for this design its duration is approximately $t_{ramp} \sim \frac{1}{3}\frac{T_s}{2} \sim 1.5n$ for the minimum bias current. A nominal coarse phase output linearity of 8 bits referred to the ADC input is assumed for a 13-bit ADC (refer to Subsection 4.3.2.5), which translates into $\frac{V_{FS}}{2^8} = 6.8mV$, where V_{FS} is the ADC input range and it $1.75V$ for this design. From Table 4.1, the maximum ramp rate variation at the maximum bias current is $1.8(10^7)\frac{V}{s}$ and for a delay of $t_d = 200ps$ the coarse phase differential error is $3.6mV$, which is approximately half of the required error. However, note that the maximum ramp rate variation occurs at a differential ramp rate$S_{diff} = 1.5(10^9)\frac{V}{s}$. For a delay $t_d = 200ps$ the total overshoot error is $v_{OV} = S_{diff}t_d = 300mV$ which is $> \frac{1}{2}$ of the nominal fully differential output range $V_{OUT_{FS}} = 0.5V$. Therefore, at the maximum output voltage of $750mV$ (refer to Figure 4-1) the coarse phase output is larger than the supply of $1V$. Ideally the constant overshoot error component of v_{OV} is canceled and the output is well within its linear range. However, for a conservative design, the minimum ZCD delay $t_{d_{min}}$ must be on the order of a factor of two smaller $\sim 100ps$. Note that there is additional delays from the zero-crossing instant to the output voltage estimate being stored on the output capacitor at the end of the coarse phase so the total delay will be effectively larger than $100ps$.

4.4.2 ZCD Delay Variation

The main sources of ZCD delay variation are: 1) change in the input ramp rate, 2) change in input common mode voltage and 3) power supply variation.

Input ramp variation is caused by deviation in the ramp current from its nominal value due to the finite resistance and nonlinear parasitic capacitance of the current

source. In [17, 36][17, 36], the delay dependence on the input ramp is considered for a ZCD, comprised of a preamplifier and a threshold detector. The latter is assumed to have a negligible delay compared to the preamplifier. The preamplifier has transconductance Gm, output resistance R_O, output capacitance C_O and time constant $\tau = R_O C_O$. The output of the preamplifier is clamped to an initial voltage V_{CLAMP}. The delay t_d in this case is defined as the time it takes the preamplifier output to reach the threshold voltage V_M and is considered for two different implementations of the preamplifier:

$$t_d = \begin{cases} \sqrt{\frac{2V_M C_O}{M_X Gm}}, & t_d \lll \tau \\ \frac{V_M}{M_X Gm R_O}, & t_d \ggg \tau \end{cases}. \tag{4.37}$$

where M_X is the slope of the ZCD input ramp. The first case in Eq. 8 represents a preamplifier which operates as an integrator (that is, it has high DC gain and low bandwidth). The second case represents a fast, low gain preamplifier which settles its output within the duration of the ZCD propagation delay t_d.

Next the effect of the input ramp dependent delay is considered for both cases above (Eq. 8) on the output overshoot error. Recall the ZCBC output voltage error as a function of the ideal output voltage v_O and ZCD delay t_d from Eq. 2.14 in Chapter 2 expressed in terms of the early voltage of the current sources V_A:

$$\varepsilon_{OUT}(v_O(t), t_d) = \frac{I_0}{C} t_d - \frac{v_O(t) I_0 t_d}{V_A C} - \frac{I_0^2 t_d^2}{2 V_A C}. \tag{4.38}$$

where I is the ramp current, C is the ZCB circuit load capacitor charged by the ramp current. Note that only the ZCD delay dependent components of Eq. 2.14 are considered. Substituting Eq. 3 into Eq. 8 yields an expression for ε_{OUT} as a function of the input ramp M_X:

$$\varepsilon_{OUT}(M_X) = \begin{cases} \left[\sqrt{\frac{2V_M C_O}{M_X Gm}} - \sqrt{\frac{2V_M C_O}{M_X Gm}}\left(\frac{v_O(t)}{V_A}\right) - \left(\sqrt{\frac{2V_M C_O}{M_X Gm}}\right)^2 \left(\frac{I_0}{2V_A}\right)\right]\left(\frac{I_0}{C}\right), & t_d \ll \tau \\ \left[\frac{V_M}{M_X GmR_O} - \frac{V_M}{M_X GmR_O}\left(\frac{v_O(t)}{V_A}\right) - \frac{V_M}{M_X GmR_O}\left(\frac{I_0}{2V_A}\right)\right]\left(\frac{I_0}{C}\right), & t_d \gg \tau \end{cases} . \tag{4.39}$$

The input ramp rate is: $M_X = \frac{dV_X}{dt}$, where V_X is the ZCD input. The relationship between the ZCBC output V_{OUT} and V_X is $V_X = \beta V_{OUT}$, where β is the voltage divider from the ZCBC output to the ZCD input. The output and input ramps are related by:

$$M_X = \frac{\beta dV_{OUT}}{dt} = \frac{\beta I_0}{C}. \tag{4.40}$$

Substituting Eq. 4.40 into Eq. 4.39 then results in:

$$\varepsilon_{OV}(M_X) = \begin{cases} \sqrt{\frac{2V_M C_O M_X}{Gm}}\frac{1}{\beta} - \sqrt{\frac{2V_M C_O M_X}{Gm}}\left(\frac{v_O(t)}{\beta V_A}\right) - \left(\frac{2V_M C_O}{G_m}\right)\left(\frac{I_0}{2V_A\beta}\right), & t_d \ll \tau \\ \frac{V_M}{\beta GmR_O} - \frac{V_M}{\beta GmR_O}\left(\frac{v_O(t)}{V_A}\right) - \frac{V_M}{\beta GmR_O}\left(\frac{I_0}{2V_A}\right), & t_d \gg \tau \end{cases} .$$

For a fast ZCD pre-amplifier, the input ramp delay variation has no effect on the output overshoot error to first order. On the other hand, if the pre-amplifier approximates an ideal integrator the output overshot error depends on the square root of the input ramp due to the ramp integration function. Note that in this case the constant the output-independent component of the overshoot error is no longer output-independent. From the above analysis it follows that to minimize output dependency of the ZCD delay it is desirable to design the ZCD pre-amplifier to have a time constant much smaller than t_d.

4.4.3 ZCD Implementation

The ZCD topology in this design is similar in structure to the general topology used in [6, 9, 26] which consists of a fast differential to single-ended pre-amplifier stage, followed by a dynamic threshold detector.

The differential pair preamplifier in [6] is replaced by a Bazes amplifier [3] shown in Figure 4-15. The advantages of the Bazes amplifier are twofold. First, in its small signal range of operation, for a fixed bias current and similar bandwidth, the Bazes offers twice the gain of a differential pair [3] if the transconductance of the input devices $M3$, $M4$, $M5$ and $M6$ are matched, at the expense of an increased input parasitic capacitance. Second, when outside of its linear range of operation the bias current of the Bazes amplifier increases with the input signal and speeds up the output transition as opposed to a differential pair which has a fixed bias current. Therefore for the same bias current as a differential pair the Bazes amplifier can be faster without wasting additional static power because unlike the differential pair, it is not slew-limited. It also has a full rail output, which allows it to be followed directly by an inverter, eliminating the need to bias the differential pair for a common mode output voltage with respect to the the trip voltage of the following threshold detector.

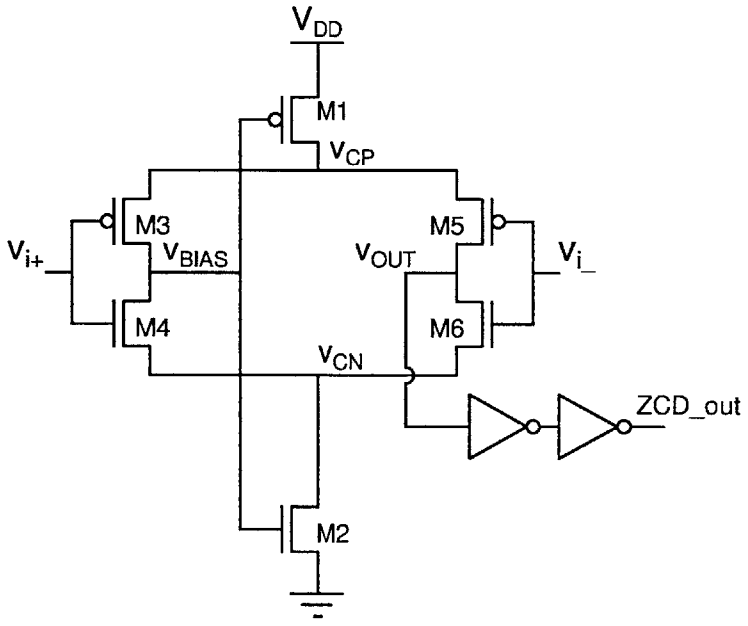


Figure 4-15: Bazes amplifier topology

In [3] devices $M2$ and $M1$ in Figure 4-15 are biased in the triode region (while

the input devices are biased in saturation) when the input voltages are at mid-rail, which gives the Bazes amplifier the capacity for output current larger than the bias current during the output transitions, making it a power efficient topology for high speed applications. The In addition with the current sources biased in their triode region, the outputs V_H and V_L are very close to the rails, ensuring an almost rail to rail output range, which provides a margin of variation of the logic threshold of the subsequent logic gates. In this mode of operation the Bazes amplifier, represents a differential version of an inverter or the dynamic threshold detector in [6] and its operation and analysis are explored further in [29].

If $M1$ and $M2$ are biased in saturation, the capacity for large current swings at the transition point diminishes and instead the current varies by a small amount around the bias point until the circuit leaves its linear range, that is $M1$ or $M2$ goes into cut off. At that instant, if $M1$ is cut off, then the current in M_2 increases proportionately to the input voltage until M_2 goes into its triode region and the output starts to slowly approach the respective rail. The reason for a small voltage variation, for small inputs, at node v_C when $M1$ and $M2$ are biased in saturation vs triode region, is that node v_{bias} is attenuated by the loop gain when the devices are in saturation as will be shown in subsection 4.4.3.1.

- Bazes amplifier turn on/off

In Figure 4-16 the NMOS switch (sw_1) in the current path of $M1$ is used to turn on and off the Bazes amplifier. The control signal for turning on the ZCD is generated from the preset control signal (Pre), while a delayed ZCD output signal ZCD_{out} is used to control the ZCD turn-off. As the current in $M1$ is cut off through sw_1, the bias node v_{BIAS} is pulled high turning off $M2$. An additional PMOS switch (sw_2) is added to pull the node v_{cp} to the upper rail and ensure that $M5$ and $M4$ are fully off.

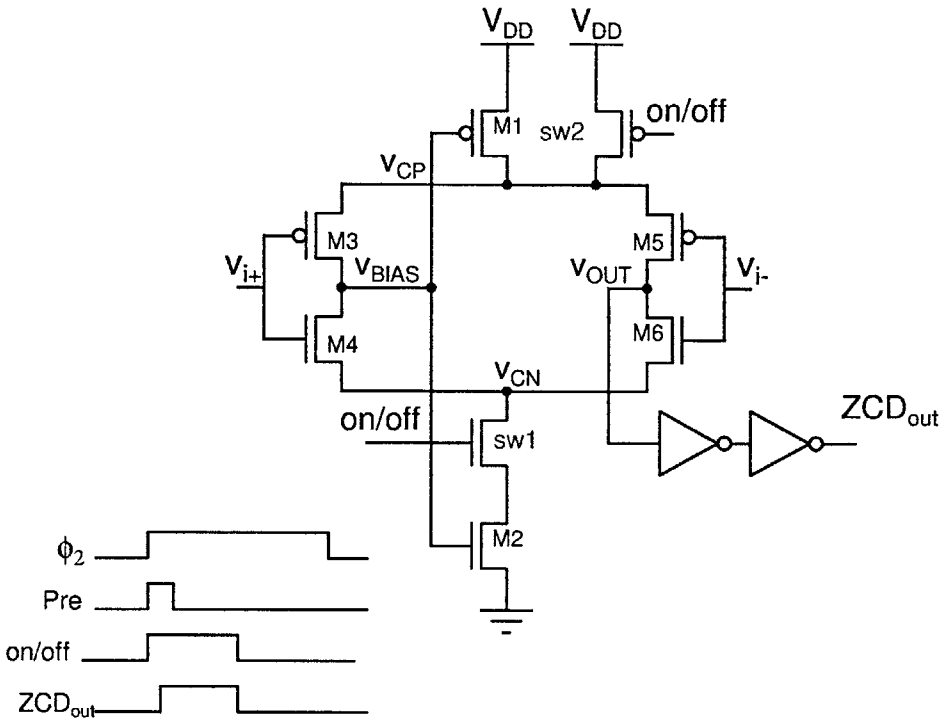


Figure 4-16: Turn-on and turn-off of the Bazes amplifier

4.4.3.1 Bazes Amplifier Small Signal Analysis

The small signal gain of the Bazes amplifier for all devices in saturation is derived by making several assumptions along the way to simplify the analysis. The goal is to gain an understanding of the operation of the circuit rather than derive an exact transfer function. Devices $M3$,$M4$, $M5$ and $M6$ are assumed to have the same transconductance g_{mi} and the same output impedance r_{oi}. Devices $M1$ and $M2$ are also assumed to to have the same transconductance g_{mbias} and the same output resistance r_{ob}. To simplify the analysis it is useful to first find the equivalent small signal resistance looking into the drains of the input transistors $M3, M4, M5$ and $M6$.

To do the small signal analysis of the Bazes amplifier, first the feedback loop is disconnected at the bias node v_{BIAS} (refer to Figure 4-17).

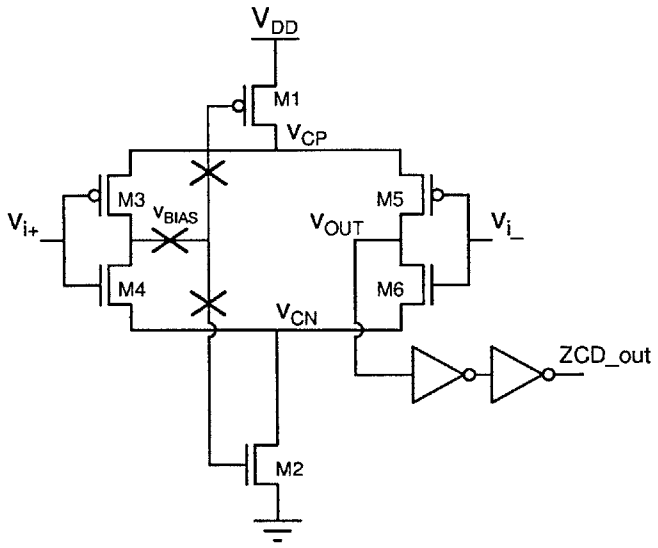


Figure 4-17: Bazes amplifier schematic. The feedback loop at node v_{BIAS} is disconnected.

The equivalent Thevenin resistance r'_{out}, looking into the drain of M_4 in Figure 4-17, can be found by setting the inputs to all devices to incremental ground and injecting a current i_{test} into v_B Figure 4-18:

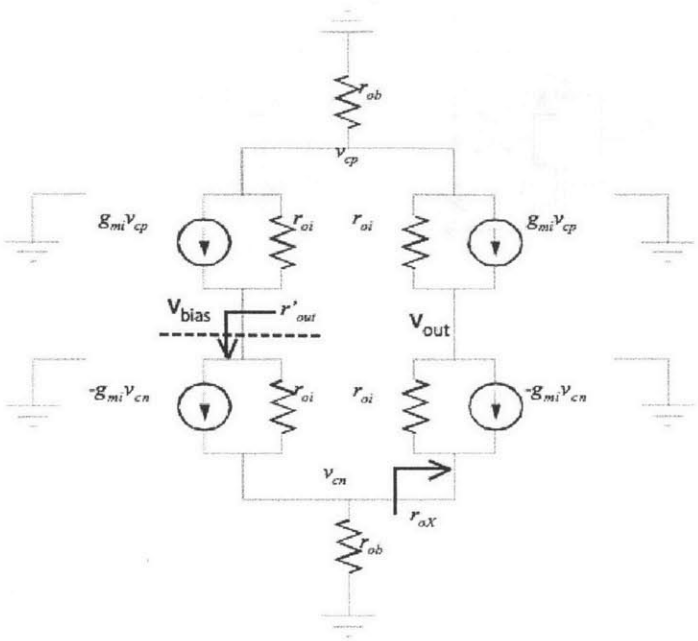


Figure 4-18: Small signal diagram for finding the equivalent Thevenin resistance looking into the drain of $M4$.

$$r'_{out} = \frac{v_{test}}{i_{test}} \tag{4.41}$$

$$i_{test} = \frac{v_{test} - i_{test}(r_{ob} \parallel r_{ox})}{r_{oi}} - i_{test}(r_{ob} \parallel r_{ox})g_{mi} \tag{4.42}$$

where r_{ox} is the equivalent resistance looking into the source of $M6$ in Figure 4-17, which will be derived next :

$$r_{oX} = \frac{v_{test}}{i_{test}}$$

$$v_{out} = r_{oi} i_{test} + r_{ob} i_{test} (g_{mi} r_{oi} + 1) \tag{4.43}$$

$$i_{test} = \frac{v_{test} - v_{out}}{r_{oi}} + g_{mi} v_{test}. \tag{4.44}$$

From Eq. 4.41, Eq. 4.43 and Eq. 4.44 it follows that:

$$r_{ox} = \frac{2 r_{oi}}{1 + g_{mi} r_{oi}} + r_{ob}. \tag{4.45}$$

If $g_{mi} r_{oi} \gg 1$

$$r_{ox} = \frac{2}{g_{mi}} + r_{ob} \tag{4.46}$$

and $r_{ob} \gg \frac{2}{g_{mi}}$ then Eq. 4.45 can be simplified to:

$$r_{ox} \approx r_{ob}. \tag{4.47}$$

From Eq. 4.42 and Eq. 4.47 it follows that the equivalent Thevenin resistance r'_{out} is :

$$r'_{out} = r_{oi} + \frac{r_{ob}}{2} (1 + g_{mi} r_{oi}). \tag{4.48}$$

By symmetry the Thevenin equivalent resistance, looking into the drains of the remaining input devices M_3, M_5 and $M6$ in Figure 4-17 is also r'_{out}.

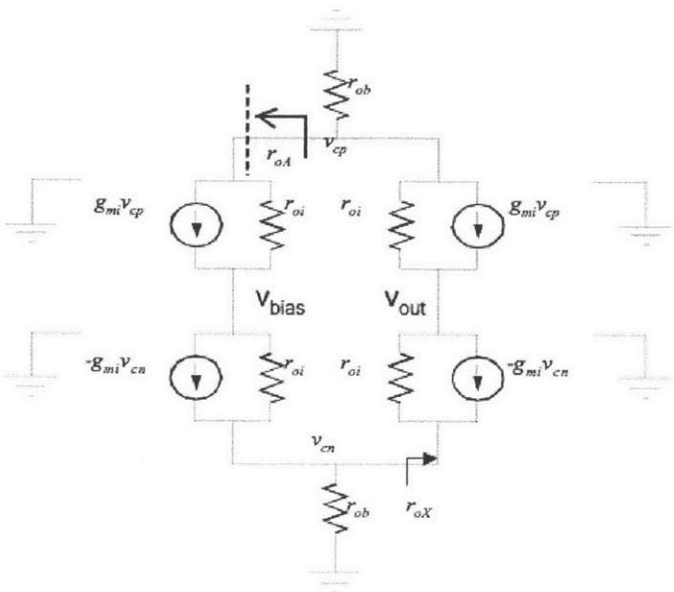


Figure 4-19: Small signal diagram for finding the equivalent Thevenin resistance looking into the source of $M3$.

Next the equivalent Thevenin resistance r_{oA}, looking into the source of M_3 will be derived (refer to Figure 4-19):

$$r_{oA} = \frac{v_{test}}{i_{test}}.$$

$$v_b = i_{test}\left[r_{oi} + (1 + g_{mi}r_{oi})(r_{ob} \parallel r_{oX})\right] \tag{4.49}$$

$$\frac{v_{test} - v_b}{r_{oi}} + g_{mi}v_{test} = i_{test}. \tag{4.50}$$

Substituting Eq. 4.47 into Eq. 4.49 and Eq. 4.50 and further into Eq. 4.48 the equivalent resistance r_{oA} can be expressed as:

$$r_{oA} = \frac{r_{oi} + r_{oi}(g_{mi}\frac{r_{ob}}{2} + 1) + \frac{r_{ob}}{2}}{(1 + g_{mi}r_{oi})}$$

$$r_{oA} = \frac{2r_{oi}}{(1 + g_{mi}r_{oi})} + \frac{r_{ob}}{2}.$$

If $g_{mi}r_{oi} \gg 1$ then:

$$r_{oA} \simeq \frac{2}{g_{mi}} + \frac{r_{ob}}{2}. \tag{4.51}$$

If $g_{mi}r_{ob} \gg 4$ then the approximation can be made:

$$r_{oA} \approx \frac{r_{ob}}{2}. \tag{4.52}$$

By symmetry then the equivalent small signal resistance looking into the sources of all four input devices $M3, M4, M5$ and $M6$ (in Figure 4-17) is $r_{oA} = r_{oC} = r_{oB} = r_{oB}$ and shown in Figure 4-20.

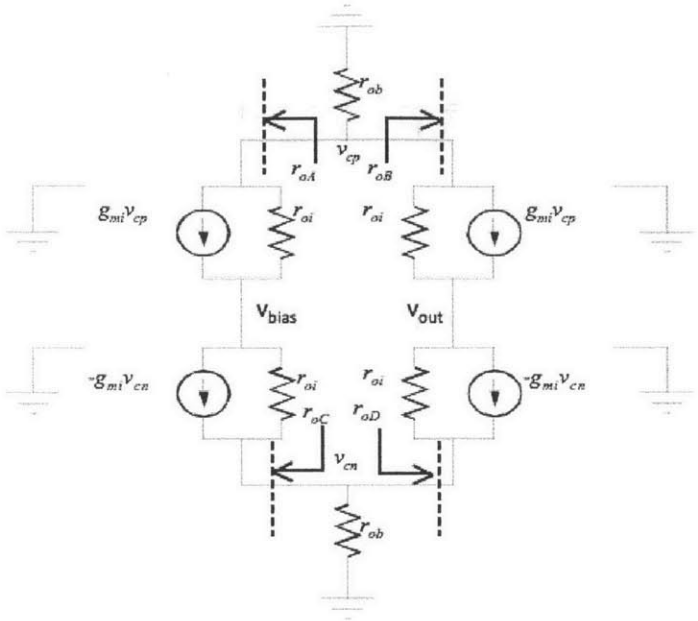


Figure 4-20: The equivalent Thevenin resistance looking into the sources of all four input devices is the same by symmetry

A block diagram is derived in Figure 4-22, using the equivalent resistances derived above, for the transfer function from v_{i+} to node v_{cp} with v_{i+} applied at the gate of $M3$. The negative input v_{i-} grounded by superposition (refer to Figure 4-21) and the input to $M4$ is also set to ground. To simplify the analysis only devices $M3$ and $M1$ in Figure 4-17 as well as the equivalent resistances $r_{oB} = r_{oA}$, and r'_{out} are considered in this part of the analysis.

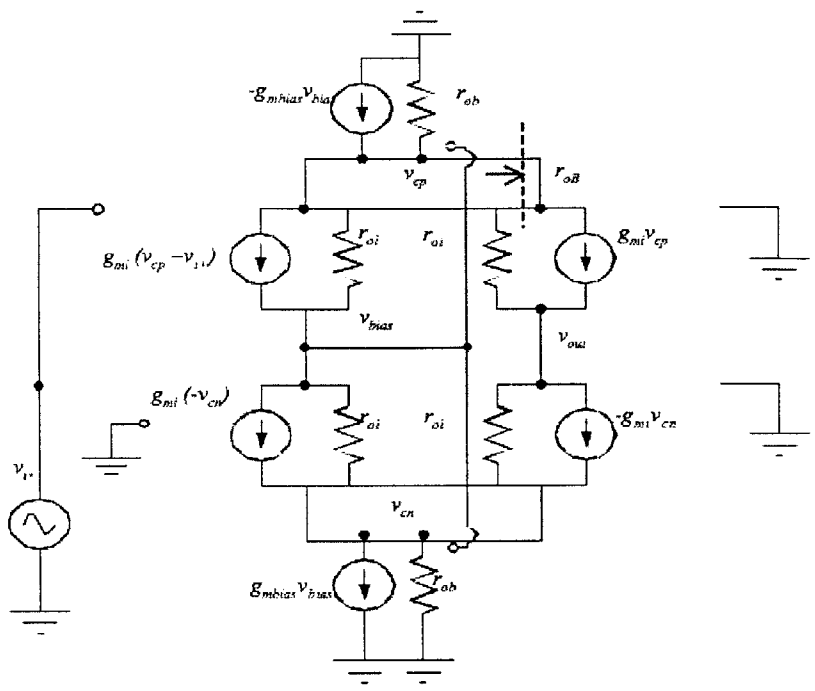


Figure 4-21: Small signal diagram to derive the transfer function from v_{i+} to v_{cp} and the transfer function from v_{i+} to v_{bias} with v_{i-} grounded.

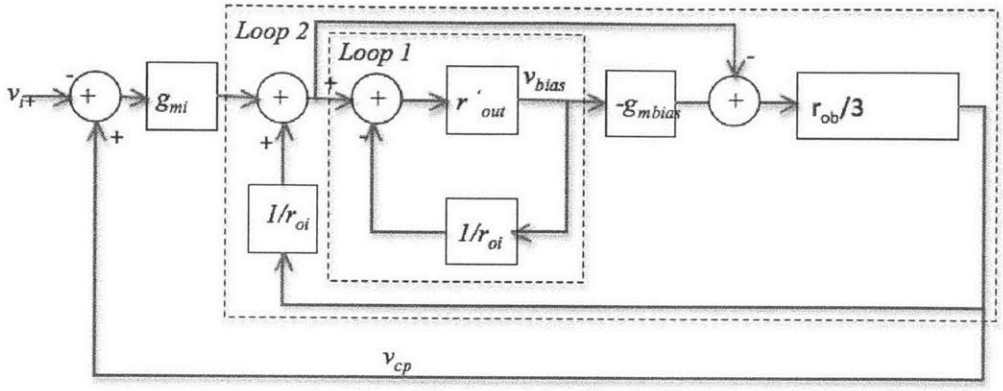


Figure 4-22: Block diagram for half circuit of the ZCD

The block diagram in Figure 4-22 can be reduced to the block diagram in Figure 4-23.

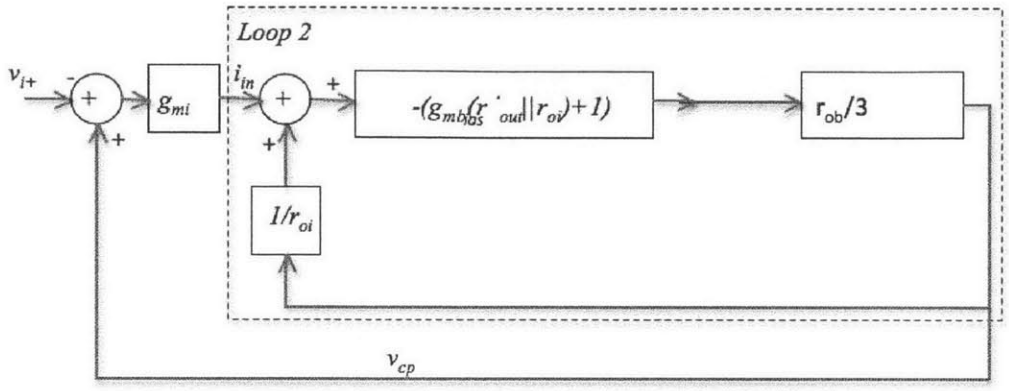


Figure 4-23: Reduced block diagram for half circuit small signal analysis of the Bazes amplifier.

From the reduced block diagram of Figure 4-23the transfer function from the current $i_{in} = g_{mi}(v_{i+} - v_{cp})$ to node v_{cp} can be found to be:

$$\frac{v_{cp}}{i_{in}} = \frac{-(g_{mi}(r'_{out}||r_{oi}) + 1)\frac{r_{ob}}{3}}{1 + g_{mi}(r'_{out}||r_{oi}) + 1)\frac{r_{ob}}{3}\left(\frac{1}{r_{oi}}\right)} = -H. \tag{4.53}$$

Then the transfer function from v_{i+} to v_{cp} is:

$$\frac{v_{cp}}{v_{i+}} = \frac{g_{mi}H}{1 + g_{mi}H}. \tag{4.54}$$

From Eq. 4.48 the approximation can be made that $r'_{out}||r_{oi} \approx r_{oi}$, and using this approximation the term $g_{mi}H$ is reduced to:

$$g_{mi}H = g_{mi}r_{oi}. \tag{4.55}$$

Then substituting Eq. 4.55 into Eq. 4.54 yields:

$$\frac{v_{cp}}{v_{i+}} = \frac{g_{mi}r_{oi}}{1 + g_{mi}r_{oi}} \approx 1 \tag{4.56}$$

if $g_{mi}r_{oi} > 1$. By symmetry between the top and bottom half of the circuit (having made the assumptions in the beginning of this section), the gain from v_{i+} to node v_{cn} $\frac{v_{cn}}{v_{i+}} \approx 1$ holds.

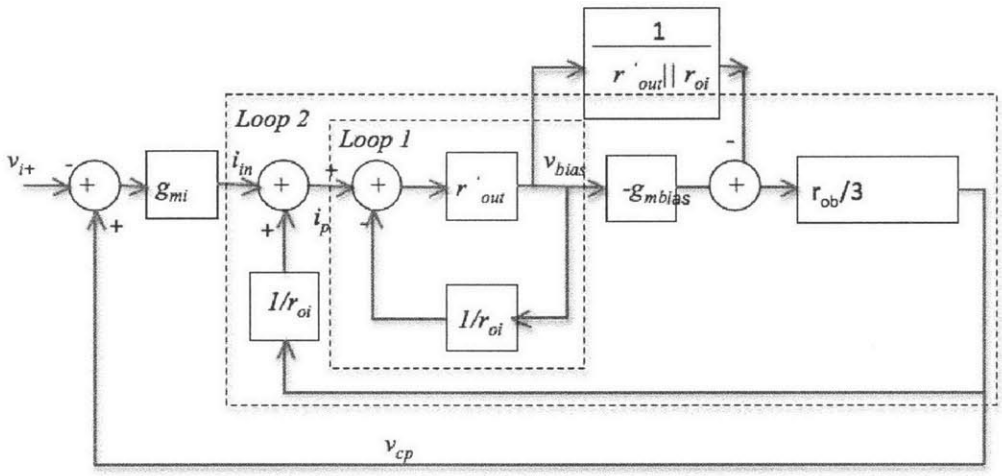


Figure 4-24: Block diagram for transfer function from the positive input node v_{i+} to the bias node v_{bias} of the Bazes amplifier.

From Loop 2 in Figure 4-24 the transfer function from the current i_{in} to node v_{bias} is:

$$\frac{v_{bias}}{i_{in}} = \frac{r_{oi}}{1 + r_{oi}(\frac{1}{r_{oi}})(\frac{r_{ob}}{3})(g_{mbias} + \frac{1}{r_{oi}})},$$

(where it is assumed that $r'_{out}||r_{oi} \approx r_{oi}$) which can be further simplified to :

$$\frac{i_{in}}{v_{bias}} = \frac{r_{oi}}{1 + \frac{r_{ob}}{3}(g_{mbias} + \frac{1}{r_{oi}})}. \tag{4.57}$$

The transfer function from node v_b to v_{cp} from the block diagram in Figure 4-24 is:

$$\frac{v_{cp}}{v_{bias}} = (-g_{mbias} - \frac{1}{r_{oi}})\frac{r_{ob}}{3}. \tag{4.58}$$

Then the transfer function from v_{i+} to v_{bias} from the block diagram above and Eq. 4.57 and 4.58 is:

$$\begin{aligned}
\frac{v_{bias}}{v_{i+}} &= -\frac{\frac{g_{mi}r_{oi}}{1+\frac{r_{ob}}{3}(g_{mbias}+\frac{1}{r_{oi}})}}{1 + \frac{g_{mi}r_{oi}}{1+\frac{r_{ob}}{3}(g_{mbias}+\frac{1}{r_{oi}})}(g_{mbias} + \frac{1}{r_{oi}})\frac{r_{ob}}{3}} \\
&= -\frac{g_{mi}r_{oi}}{1 + \frac{r_{ob}}{3}(g_{mbias} + \frac{1}{r_{oi}}) + g_{mi}r_{oi}(g_{mbias} + \frac{1}{r_{oi}})\frac{r_{ob}}{3}} \\
&= -\frac{g_{mi}r_{oi}}{1 + \frac{r_{ob}}{3}(g_{mbias} + \frac{1}{r_{oi}})(1 + g_{mi}r_{oi})} \\
&\simeq -\frac{1}{1 + \frac{r_{ob}}{3}(g_{mbias} + \frac{1}{r_{oi}})},
\end{aligned} \tag{4.59}$$

where the assumption is made that the gain of the input devices is larger than 1, $g_{mi}r_{oi} \gg 1$. It follows that nodes v_{cp} and v_{cn} follow the input voltage, while change in the positive input voltage is attenuated by the negative feedback loop to node v_{bias} and the current through $M3$ and $M4$ is fairly unchanged (refer to Figure 4-25). The general concept of this feedback mechanism is described in [33].

The gain from both inputs v_{i+} and v_{i-} to the output v_{out} can then be derived by superposition by setting the gates of $M4$ and $M6$ to ground and applying v_{i+} to the gate of $M3$ and v_{i-} applied to the gate of $M5$ (refer to Figure 4-17):

$$v_{out_1} \simeq g_{mi_{M5}}(v_{cp} - v_{i-})r_{oi}$$

where it is assumed that $r'_{out}||r_{oi} \approx r_{oi}$ and from Eq. 4.56 $v_{cp} \simeq v_{i+}$. By symmetry for grounded gates of $M3$ and $M5$ and with v_{i+} applied to the gate of M4 and v_{i-}

applied to the gate of $M6$:

$$v_{out_2} \simeq -g_{mi_{M6}}(v_{i-} - v_{+})r_{oi},$$

where it is assumed that $r'_{out}||r_{oi} \approx r_{oi}$ and from Eq. 4.56 $v_{cn} \simeq v_{i+}$. The output voltage v_{out} is the sum v_{out_1} and v_{out_2}.

$$v_{out} \simeq \left[g_{mi_{M5}}(v_{i+} - v_{i-}) + g_{mi_{M6}}(v_{i+} - v_{i-})\right] r_{oi}$$

or

$$\frac{v_{out}}{v_{in}} \simeq \left[g_{mi_{M5}} + g_{mi_{M6}}\right] r_{oi}.$$

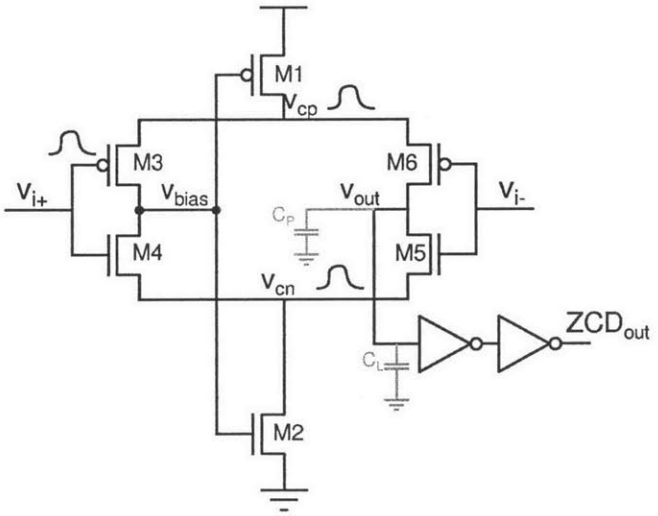


Figure 4-25: Small signal operation of the Bazes amplifier

The Bazes amplifier can be approximated as a first order system with transfer function with a single dominant pole at the output, as nodes v_{BIAS}, low resistance node, while v_{out} is a high impedance node:

$$H(s) = \frac{G}{1 + s\tau} \tag{4.60}$$

where

$$\tau = \frac{1}{(C_p + C_L)r_{out}}. \tag{4.61}$$

The load capacitor to the Bazes amplifier C_L in Figure 4-25 is the parasitic input capacitance of a small size inverter and is much smaller than the Bazes amplifier output parasitic capacitor C_P in Figure 4-25 and can be ignored. The Bazes amplifier output parasitic capacitor C_P is a sum of the drain parasitic capacitance of devices $M5$ and $M6$:

$$C_P = Cd_{M5} + Cd_{M6}.$$

The drain capacitance of $M5$ and $M6$ consists of the drain to gate overlap capacitance C_{gd} and the drain junction capacitance C_{dj}, both of which scale with the width of the device. To maximize the speed of the Bazes amplifier, the drain capacitors of $M5$ and $M6$ should be minimized by choosing smaller width devices. To bias the bottom and top current sources in saturation the input devices have to be biased in weak inversion, which ultimately sets the size of the input devices at a bias current. All input devices are sized for match transconductance. For a fixed bias current I_{bias}, biasing $M5$ and $M6$ in weak inversion results in larger transconductance to bias current ratio $\frac{gm}{I_{bias}}$ than if the devices were in square law regime and therefore improve gain and power efficiency. Minimum length input devices were used to optimize bandwidth at the cost of diminished device output resistance and therefore gain, since speed is the driving factor in this design. In comparison to a differential pair, the increase in the input parasitic capacitance by roughly a factor of two of the Bazes amplifier is the cost for the respective increase in gain by the same amount for matched input NMOS and PMOS device transconductance.

Devices $M1$ and $M2$ set the ZCD bias current and were sized to be in saturation for a given bias current. The bias current was determined by optimizing the bandwidth of the ZCD. The parasitic capacitance and the resistance at the bias node v_{BIAS} form

the second non-dominant pole in the circuit, which appears at:

$$p_2 = -\frac{1}{C_{v_{BIAS}}\left(\frac{1}{gm_{M3}+gm_{M4}}\right)}$$

where $C_{v_{BIAS}}$ is the capacitance at the bias node v_{BIAS} and is composed of the gate to source capacitance C_{gs} of $M1$ and $M2$ and the the drain capacitance of $M3$ and $M4$. The gain bandwidth plot for $I_{bias} = 550\mu A$ is shown in Figure 4-26 below.

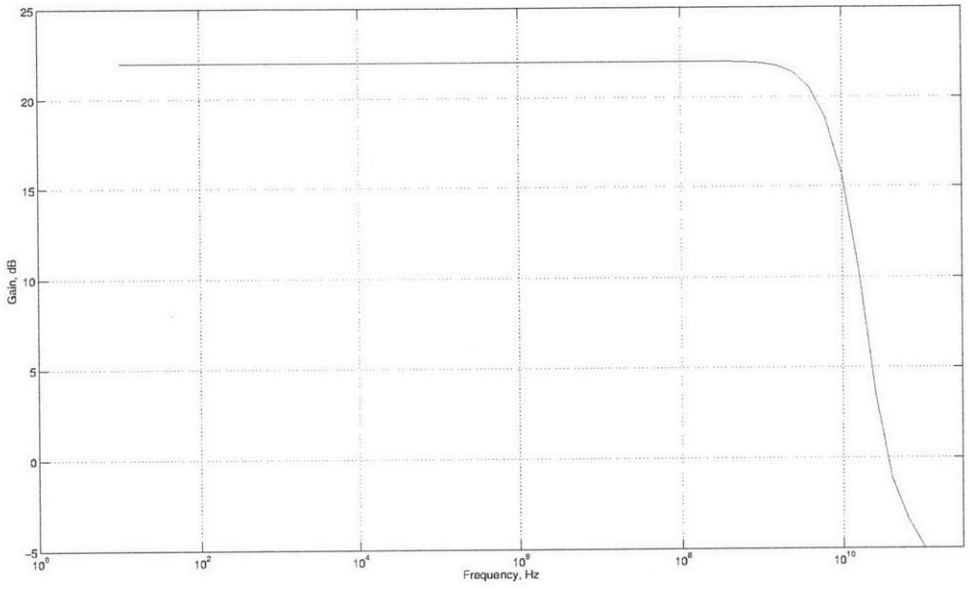


Figure 4-26: Gain bandwidth plot for the ZCD implementation with bias current $I_{bias} = 550\mu A$

The maximum differential input voltage to the ZCD is $250mV$ by design, half of which represents the runway range referred to the input. The output runway range is defined as the output voltage range covered by the output ramp, which does not constitute a valid output range. If the output voltage in single ended ZCBC is preset to the upper rail V_{DD} but the valid output range only starts at $\frac{3}{4}V_{DD}$, than the difference between the upper rail and the maximum ZCBC output voltage accounts for the output runaway voltage referred back to the ZCD input. The runaway voltage helps to ensure the output dynamics for all valid inputs is identical in the case that the ZCD does not fully settle. In a ZCB circuit the starting voltage at the input

to the ZCD is not fixed but is input dependent. To ensure that the output crosses the threshold voltage at the same point for the range of valid starting voltages, the output of the ZCD has to either settle or be at the same point even for the minimum starting input voltage. The runway voltage ensures that the input to the ZCD always starts below the minimum valid input voltage to the ZCD. In [6] an expression for the ZCD delay is derived, assuming the ZCD can be approximated by a first order system. The input is a ramp and the output is the ramp response of a first order system. The expression for the delay is :

$$t_d = \tau(1-e^{\alpha}).$$

where τ is the time constant of the ZCD and $\alpha = \frac{T_2}{\tau}$, where T_2 is the zero-crossing instant. If $\alpha \gg 1$, then $t_d = \tau$ and the ZCD output has been assumed to have mostly settled. Otherwise, for a constant switching threshold the runway voltage provides sufficient input voltage margin to the ZCD so that the output voltage follows the same dynamics regardless of the minimum valid ZCD input.

4.4.3.2 Simulated Delay Variation

The output linearity of the coarse ZCB phase of a hybrid CLS-OpAmp/ZCB pipeline ADC stage, limited by the finite resistance of the current sources is defined in Chapter 2 in Eq. 4.36 repeated here for convenience:

$$v_{OV}(v_O(t_0), t_d) = \frac{I_0}{C}t_d - \frac{v_O(t_0)t_d}{R_O C}$$

whereI_0 is the current of an ideal current source, t_0 is the zero-crossing instant, v_O is the ideal output voltage, R_O is the finite resistance of the current source and C is the load capacitor. In the output nonlinearity analysis thus far the ZCD delay t_d has been assumed constant. If t_d varies with output voltage by $\Delta t_d = f(v_O)$ the coarse phase output error is:

$$v_{OV}(v_O(t_0), t_d) = \frac{I_0}{C}t_d + \frac{I_0}{C}\Delta t_d - \frac{v_O(t_0)t_d}{R_O C} - \frac{v_O(t_0)\Delta t_d}{R_O C}, \tag{4.62}$$

where the first component $\frac{I_0}{C}t_d$ represents the constant overshoot error, while the remaining three components contribute to the coarse phase output voltage nonlinearity. The last error component of Eq. 4.62 is much smaller than the remaining errors $\Delta t_d \ll R_O C$. Thus the main output nonlinearity contribution is due to the ideal ramp rate $\frac{I_0}{C}$ multiplied by the variation in ZCD delay Δt_d.

- Input ramp vs delay variation

Cadence simulation results of delay variation versus input ramp variation are plotted in Figure 4-27. The delay is measured from the crossing point of the inputs to the midpoint of the output of two inverters following the ZCD and is measured to be $\sim$ 10%, which translates to a $\sim$ 10% variation of the constant overshoot error $V_{OV} = \frac{I_0}{C}\Delta t_d$. The input ramp is varied by equal increments up to $\sim$ 6.4%, which is larger than the expected variation of $< 2\%$ over the valid output range (refer to Table 4.1 in Section 4.2) . If the ramp rate variation is 2% at a differential ramp rate at the input to the ZCD of $(10^8)\frac{V}{s}$, this results in $\sim$ 3.2% delay change and an output voltage error for a stage gain of 4 of $\frac{I_0}{C}\Delta t_d = 4(10^8)(0.032)60ps = 800uV$, specified in Subsection 4.3.2.5) which is smaller than the nonlinearity output error in Table 4.1 of $1.4mV$ and is within the coarse phase output linearity for the first pipeline stage of 8 bits referred to the ADC input. (Note that the input ramp rate at the ZCD of $10^8\frac{V}{s}$ corresponds to the intended minimum output ramp rate of $4.3(10^8)\frac{V}{s}$ by design, while Cadence simulation of the implementation of the minimum output ramp rate yields $6.6(10^8)\frac{V}{s}$, hence the difference between the choice of input ramp rate variation and the ramp rate indicated in Table 4.1.)

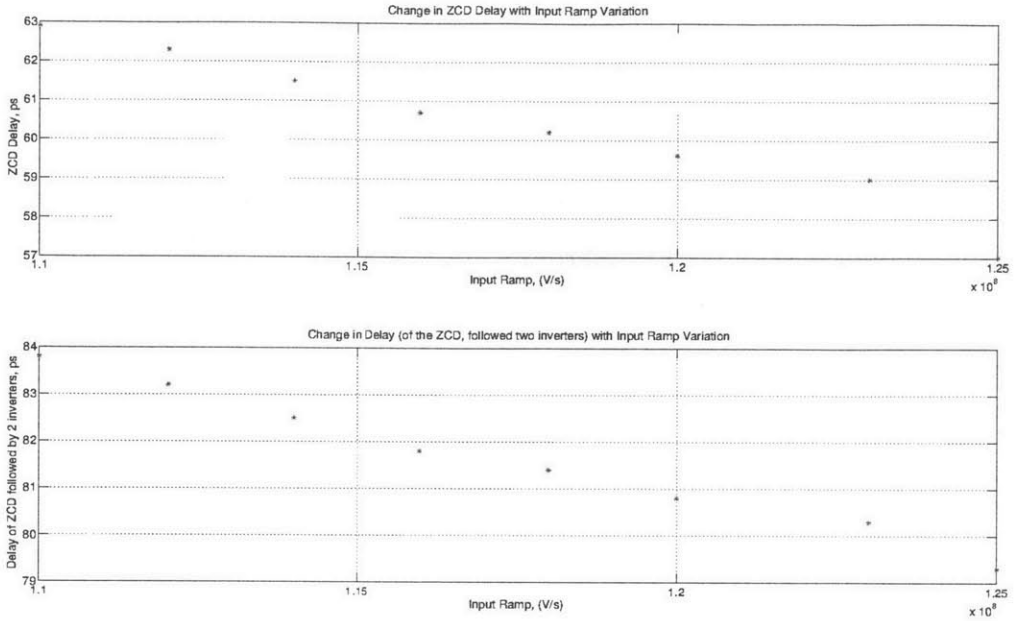


Figure 4-27: ZCD delay variation in [ps] with input ramp variation

- Power supply vs delay variation

The attenuation from the power supply variation v_{dd} to variation in the Bazes amplifier bias voltage v_{bias} is determined by a resistive divider formed by the diode connected devices $M1$ and $M2$ at node v_{bias}:

$$\frac{v_{bias}}{v_{dd}} = \frac{g_{mM2}}{g_{mM1} + g_{mM2}}$$

By symmetry the output v_{out} follows the change in bias voltage v_{bias} for common mode signals such as power supply variation. If the transconductance of $M1$ and $M2$ is the same, then the power supply attenuation factor is $\frac{1}{2}$. The size of $M1$ is increased to improve the power supply attenuation such that $g_{mM2} \simeq 0.6 g_{mM1}$ and $\frac{v_{bias}}{v_{dd}} \simeq 0.4$. The cost for increasing the size of $M1$ is increased total parasitic capacitance at the bias node, which can slow the ZCD as the non-dominant pole moves closer to the dominant pole.

Simulated results in Cadence of delay with change in power supply voltage are

plotted in Figure 4-28 for an input ramp rate of $(10^8)\frac{V}{s}$. A change in the power supply of $40mV$ results in $\sim$ 9% ZCD delay change. At a differential ramp rate at the input to the ZCD of $1(10^8)\frac{V}{s}$, the output voltage error for a stage gain of 4 is $\frac{I_0}{C}\Delta t_d = 4(10^8)(0.09)84ps = 3.02mV$ which is still within the ADC coarse phase requirements of 8-bit linearity referred to the ADC input.

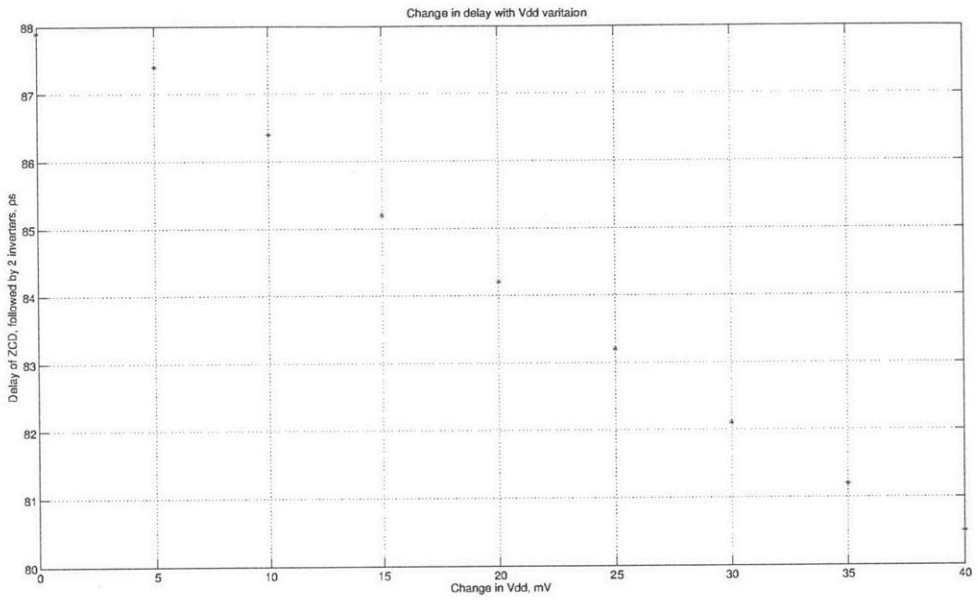


Figure 4-28: Delay of the Bazes amplifier, followed by 2 inverters in [ps]

- Common mode voltage vs delay variation

From Eq. 4.59, a change in the positive input voltage v_{i+} is attenuated by the loop gain of the negative feedback to v_{bias}. The Bazes amplifier uses negative feedback for any change (common mode or differential) at v_{bias} due to v_{i+}. Nodes v_{cp} and v_{cn} follow the input node v_{i+}. The v_{i-} changes by the same amount. The current through devices $M4$ and $M3$ (refer to Figure 4-25) is fixed as discussed in the analysis above. However, due to the finite resistance of $M1$ and $M2$, the bias current will change and the output voltage v_{out} will change to accommodate the change in current.

In Figure 4-29, the simulated results in Cadence show the change in ZCD delay, bias current and bias node v_{bias} for a $30mV$ common mode voltage change for an input

ramp rate of $10^8 \frac{V}{s}$. For comparison, the full scale differential input voltage is $250mV$, with $125mV$ allotted to the runaway input [6]. Simulated results in Cadence of delay with change in power supply voltage are plotted in Figure 4-28 for an input ramp rate of $10^8 \frac{V}{s}$. A change in the common mode voltage of $30mV$ results in $\sim 4\%$ ZCD delay change. At a differential ramp rate at the input to the ZCD of $10^8 \frac{V}{s}$, the output voltage error for a stage gain of 4 is $\Delta v_{OUT} = \frac{I_0}{C} \Delta t_d = 4(10^8)(0.04)92ps = 1.6mV$ which is still within the ADC coarse phase requirements of 8-bit linearity referred to the ADC input.

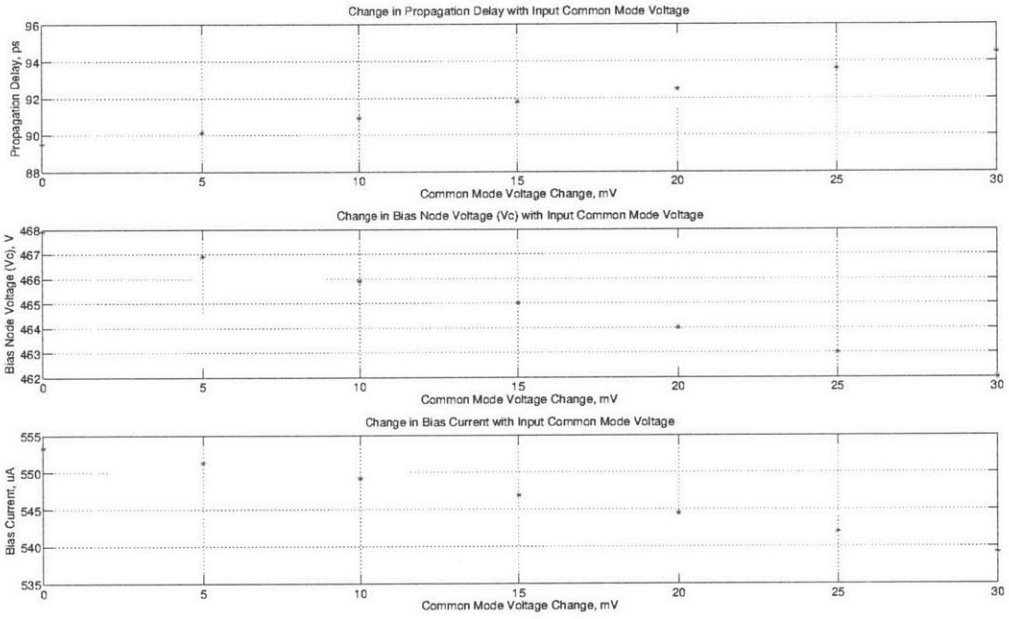


Figure 4-29: Delay variation vs common mode voltage change simulated for the Bazes amplifier, followed by two inverters. The top plot shows the delay variation in [ps] vs common mode voltage change. The middle plot shows the variation in the output voltage and the bias node v_{bias} in [mV] and the bottom plot shows the bias current change in $[\mu A]$ vs common mode voltage change.

4.4.3.3 Noise Analysis

The noise contribution from $M1$ and $M2$ can be derived by adding a voltage source in series with node v_{bias} in the block diagram derived in Subsection 4.4.3.1 and shown here again in Figure 4-30.

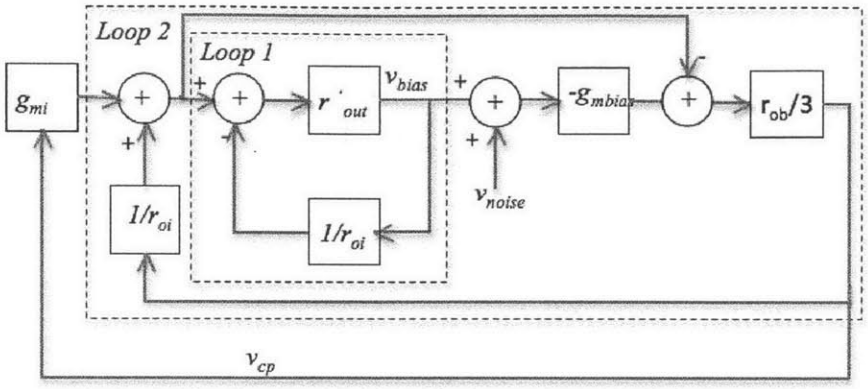


Figure 4-30: Block diagram for noise transfer function to the output of the Bazes amplifier from $M1$ or $M2$.

For clarity the diagram is redrawn as shown in Figure 4-31.

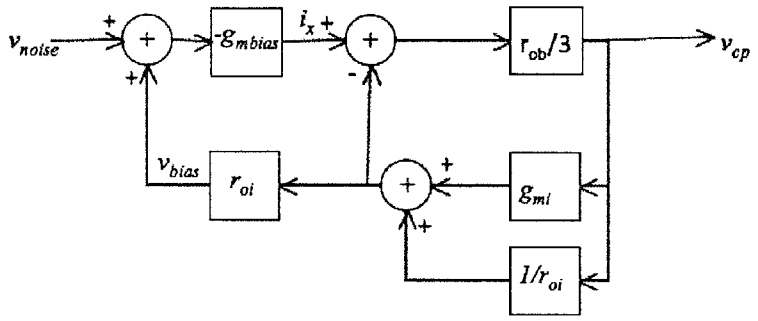


Figure 4-31: Redrawn Block diagram for noise transfer function to the output of the Bazes amplifier from $M1$ or $M2$.

From the reduced block diagram of Figure 4-31, the transfer function from i_x to v_{cp} is derived:

$$\frac{v_{cp}}{i_x} = \frac{\frac{r_{ob}}{3}}{1 + (g_{mi} + \frac{1}{r_{oi}})\frac{r_{ob}}{3}}. \tag{4.63}$$

Then the transfer function from v_{noise} to node v_{cp} is:

$$\frac{v_{cp}}{v_{noise}} = \frac{-gm_{bias}(\frac{v_{cp}}{i_x})}{1 + g_{mbias}(\frac{v_{cp}}{i_x})r_{oi}(g_{mi} + \frac{1}{r_{oi}})}. \tag{4.64}$$

Substituting Eq. 4.63 into Eq. 4.64 results in:

$$\frac{v_{cp}}{v_{noise}} = \frac{-gm_{bias}\left(\frac{\frac{r_{ob}}{3}}{1+(g_{mi}+\frac{1}{r_{oi}})\frac{r_{ob}}{3}}\right)}{1+g_{mbias}\left(\frac{\frac{r_{ob}}{3}}{1+(g_{mi}+\frac{1}{r_{oi}})\frac{r_{ob}}{3}}\right)r_{oi}(g_{mi}+\frac{1}{r_{oi}})}$$

$$= \frac{-gm_{bias}\frac{r_{ob}}{3}}{1+(g_{mi}+\frac{1}{r_{oi}})\frac{r_{ob}}{3}+g_{mbias}\frac{r_{ob}}{3}r_{oi}(g_{mi}+\frac{1}{r_{oi}})}$$

$$= \frac{-gm_{bias}\frac{r_{ob}}{3}r_{oi}}{r_{oi}+(g_{mi}r_{oi}+1)\frac{r_{ob}}{3}(1+g_{mbias}r_{oi})} \tag{4.65}$$

$$\simeq \frac{-1}{1+(g_{mi}r_{oi})} \simeq \frac{-1}{g_{mi}r_{oi}}, \tag{4.66}$$

where it is assumed that $g_{mi}r_{oi} \gg 1$.

Thus the noise contribution due to $M1$ or $M2$ to the output noise power density can be expressed as:

$$\frac{v_{no_1}^2}{v_{noise}^2} = \left(\frac{v_{cp}}{v_{noise}}\right)^2\left(\frac{v_{out}}{v_{cp}}\right)^2$$

where $\frac{v_{out}}{v_{cp}} = g_{mi}r_{oi}$ and $\frac{v_{cp}}{v_{noise}} \simeq \frac{-1}{g_{mi}r_{oi}}$. It follows that $\frac{v_{no}^2}{v_{noise}^2} \approx 1$. Device $M1$ is biased on the verge of weak inversion, while $M2$ is in weak inversion. The voltage noise power spectral density of $M1$ is $v_{noise_{M1}}^2 = \frac{\gamma 4kT}{gm_{M1}}$, while that of $M2$ is $v_{noise_{M1}}^2 = \frac{n4\gamma kT}{gm_{b_{M2}}}$, where n is the ideality factor for weak inversion and γ is the noise coefficient, which depends on the region of operation and varies from $\frac{2}{3}$ for devices biased in the square law regime to $\frac{1}{2}$ for devices biased in weak inversion, k is Boltzmann's constant $(1.38(10^{-23})JK^{-1})$ and T is the temperature in Kelvin. The output noise power spectral density contribution from all four input devices $M3$,$M4$, $M5$ and $M6$ is:

$$v_{no_2}^2 = 4(g_{mi}r_{oi})^2 v_{ni}^2,$$

where $v_{ni}^2 = \frac{n4\gamma kT}{g_{mi}}$ (all four devices are biased in weak inversion and sized for the same transconductance g_{mi}). The voltage noise power spectral density contributed

by all devices in the Bazes amplifier is then:

$$\begin{aligned} v_{no}^2 &= v_{no_1}^2 + v_{no_2}^2 \\ &= \frac{\gamma 4kT}{gm_{M1}} + \frac{n\gamma 4kT}{gm_{M2}} + 4(g_{mi}r_{oi})^2 \left(\frac{n\gamma 4kT}{g_{mi}}\right). \end{aligned}$$

To refer the output noise power spectral density to the input v_{i-}, we divide by the square of the gain from v_{out} to v_{i-} :

$$v_{ni}^2 = \frac{1}{(2g_{mi}r_{oi})^2}\left[\frac{\gamma 4kT}{gm_{M1}} + \frac{n\gamma 4kT}{gm_{M2}}\right] + 4\left(\frac{n\gamma 4kT}{g_{mi}}\right) \tag{4.67}$$

$$\simeq \left(\frac{n\gamma 4kT}{g_{mi}}\right) \tag{4.68}$$

It is clear from Eq. 4.67 that the power spectral density of the voltage noise contributed by devices $M1$ and $M2$ is attenuated by the gain from the Bazes amplifier output to the inputv_{i-}. By design $g_{m_{M4}} \simeq g_{mM3} \simeq g_{mM5} \simeq g_{mM6} \simeq 5mS$. The equivalent noise bandwidth for steady state operation for a first order linear system is NBW $= \frac{1}{4\tau}$, where τ is the time constant of the system [10]. The assumption is made that the Bazes amplifier is fast enough to have mostly settled by the time the output reaches the threshold of the subsequent stage. Under this assumption the input-referred integrated root-mean-square noise voltage, assuming $n = 1$, $\gamma = \frac{1}{2}$ and $\tau = 32ps$, is $\sim 137\mu V$.

The assumption is made here that the Bazes amplifier output settles by the time it reaches the threshold of the following stage. The equivalent noise bandwidth is defined from stationary noise analysis, assuming the noise is filtered with a single pole system. A general expression for the noise bandwidth of a first order system with time constant τ_o is derived in [36] sampling white noise for a time t_i as :

$$NBW = \frac{1}{4\tau_o} coth(\frac{t_i}{2\tau_0}) u(t_i)$$

which for $t_i \ggg \tau_o$ approximates the steady state case of $NBW = \frac{1}{4\tau_o}$. If $t_i \lll \tau_o$, the system is much slower than the integration time and the equivalent noise bandwidth is $NBW = \frac{1}{2t_i}$. The minimum integration time $t_{i_{MIN}}$ for the crossing detector is the time it takes the ZCBC output v_{OUT} to ramp to the maximum valid output voltage from the upper rail Figure 4-32 which represents the preset voltage in this example. At the minimum bias current of the ADC, the single-ended ramp rate is $S_{se} = 3.3(10^8)\frac{V}{ns}$, the nominal single-ended output swing of the ZCBC is $0.5V$ from a minimum output voltage of $0.25V$ to a maximum output voltage of $0.75V$. The supply is $1V$. The time $t_{i_{MIN}}$ can then be expressed as:

$$t_{i_{MIN}} = \frac{1V - 0.75V}{3.3(10^8)\frac{V}{s}} = 758ps.$$

Therefore the approximation for the noise bandwidth for the steady state case holds as $t_{i_{MIN}} > \tau$, where $\tau = 32ps$ is the Bazes time constant.

The input-referred total integrated noise voltage from Cadence simulation is $\sqrt{\bar{v}_{ni}^2} = 144\mu V$ for a bias current $I_{BIAS} = 550\mu A$.

Noise voltage at the input to the ZCD translates into an error at the output voltage of the ZCBC during the coarse phase, as the noise voltage is effectively an error in the virtual ground condition. From Subsection 4.4.1 the output nonlinearity error of the coarse phase is desired to be $\epsilon < 6.8mV$. To refer the output error ϵ to the virtual ground node we multiply by the transfer function from the output v_{out} to the virtual ground node v_x which is $\frac{C_{n2}}{C_{n2}+C_{n1}} = \frac{1}{4}$ (refer to Figure 4-32). It follows that the error at the virtual ground node ϵ_x is desired to be less than $1.72mV$.

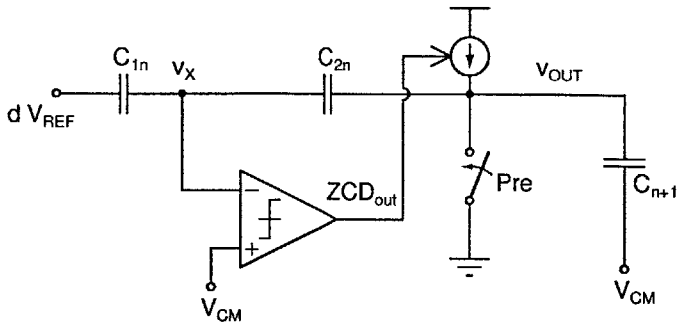


Figure 4-32: ZCB switched-capacitor circuit diagram

4.4.3.4 ZCD and Bidirectional Ramp ZCBC

The Bazes amplifier is bidirectional and can be used regardless of the switch in directions of the input ramps. For part of the output waveform from either rail to the other, the ZCD goes though nonlinear regions of operation where either $M1$ or $M2$ go out of their linear region of operation, which could change in the ZCD delay for transitions form V_H to V_L and vise verse. To avoid any differences in delay, due to the two devices pulling the output high or low in bidirectional ZCBC the ZCD topology is reconfigured with the output-sign bit (which dictates the output ramp direction) so that for any input regardless of ramp direction the output always transitions from V_L to V_H. To avoid errors due to charge injection, using switches at the input of the ZCD, the output of the ZCD was changed internally in the ZCD topology as shown in Figure 4-33. Two switches are introduced for the purpose of preserving the unidirectional output of the ZCD. Switch $sw1$ is on when the output sign bit is high and switch $sw2$ is on when the output sign bit is low. Due to device threshold mismatches, the ZCD offset in either configuration will slightly differ. However, the large input sizes of the input devices reduce this mismatch. In addition ZCD only contributes an error towards an approximate value of the output voltage at the end of the coarse phase.

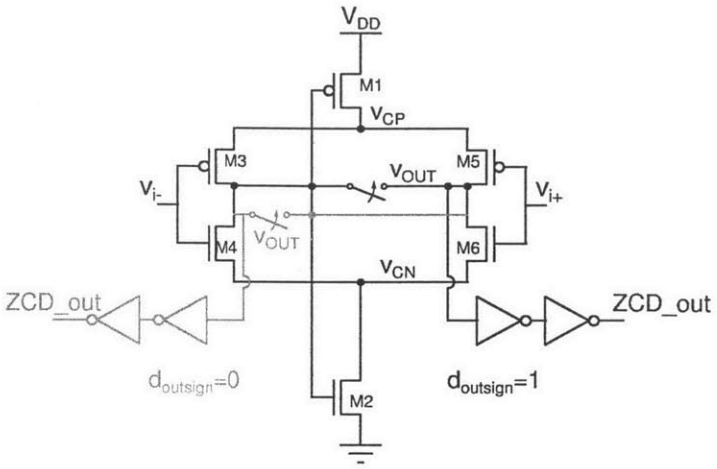


Figure 4-33: ZCD configuration for bidirectional ramp coarse phase implementation. Switches on the right and left of v_{OUT} are controlled by the output sign bit.

4.4.4 Future Work

One method to improve the power supply sensitivity of the Bazes amplifier is to bias $M1$ as a constant current source, while $M2$ remains diode connected at node v_{BIAS} (in Figure 4-15). The v_{BIAS} node is no longer a resistive divider between two diode connected devices, while the rail-to-rail output swing as well as bias current increase during the output transition are preserved.

Chapter 5

Experimental Results

A prototype pipelined ADC was fabricated in a TSMC 65nm 1V CMOS process. The die area is $3mm$ x $2mm$. A layout diagram is shown in Figure 5-1. The ADC area is approximately $2mm$ x $350\mu m$. The area of the first stage is $400\mu m$ x $350\mu m$. The remaining area of the die was used for decoupling capacitors for the supply voltages and the reference voltages to the ADC. A $1.3nF$ capacitor is implemented as on-chip decoupling capacitor between the reference voltages V_{REFP} and V_{REFM} of the ADC.

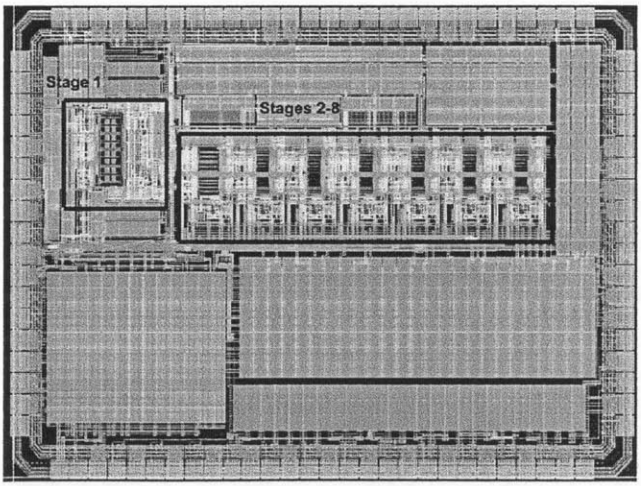


Figure 5-1: Layout of Hybrid CLS-OpAmp/ZCB pipelined ADC in $65nm$ CMOS

5.1 Test Setup

The setup for experimental testing of the pipelined ADC is shown in Figure 5-2. An Agilent 8644B synthesized signal generator was used to generate a single frequency sinusoidal input test signal, which is filtered by a bandpass filter and converted form a single-ended to a fully differential signal through two cascaded transformers ADT4-1T from Mini Circuits. The master clock Clk_{in} for the ADC was generated by a Standard Research Systems Model CG635 2.05GHz synthesized clock generator. A control signal synchronized with the master clock, also generated by the clock generator was used for the generation of the overshoot correction voltage applied to the ADC. Two Agilent 8644B signal generators were used to generate the bit streams D_0 and D_1 and clock signals clk_0 and clk_1 for two off-chip shift registers. The first shift register (bit stream D_0) provided flexibility in the control for the non-overlap duration for clock phases ϕ_1 and ϕ_2 as well as the duration of the preset phase. In addition it provided control bits for the five bias current configurations of the on-chip bias circuit of the ADC. The second shift register (bit stream D_1) was used to configure the pipeline stages in either unidirectional or bidirectional mode of operation for the coarse ZCD phase of charge-transfer operation using a single bit per stage to control a multiplexer incorporated in each stage, which can set the coarse ramp direction for the stage. The output bits of the pipelined ADC were captured by Tektronix TLA 715 Logic Analyzer. The ADC output clock clk_{out} used for readout of the data was used as an external clock by the logic analyzer. The output data was read on both edges of the output clock. The signal generator and clock generator are synchronized when collecting the data for the FFT plot.

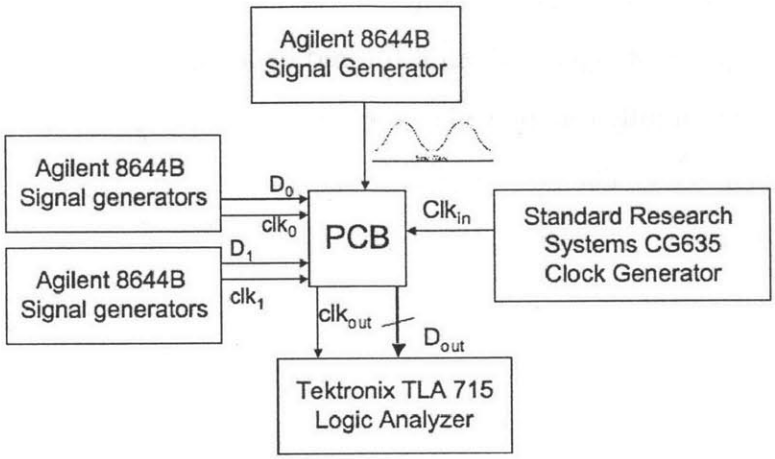


Figure 5-2: ADC test setup

5.2 Results

5.2.1 Static Linearity

Static linearity is used to characterize the DC transfer function of an ADC. Two metrics are typically used: differential nonlinearity (DNL) and integral nonlinearity (INL). Integral nonlinearity is defined as the distance of the code centers in the ADC transfer function from a straight line fit from one end to the other of the output code. Differential nonlinearity is defined as the deviation of the code transition widths from the ideal width of 1LSB. For an ideal ADC the transition codes are 1LSB and the DNL is 0. The DNL of an ADC can also be viewed as the change in input voltage it takes the ADC to transition between two output codes.

The static linearity of the ADC was measured using a histogram test [11]. The frequency of the input signal to the ADC was $5MHz$. The size of the output sample was 4.16 x 10^6 output codes. The number of samples, K, required for a high-confidence

measurement is [11] :

$$K = \frac{\pi 2^{N-1} Z_{\frac{\alpha}{2}}^2}{\beta^2},$$

where N is the number of bits, β is the static linearity measurement resolution, and $Z_{\frac{\alpha}{2}} = 2.576$ for $\alpha = 0.01$ or 99% confidence level. Thus for $K = 4.16(10^6)$ the static nonlinearity measurement is accurate to $\pm 0.14 LSB$ with 99% confidence level for $N = 13$.

Figure 5-3 and Figure 5-4 show the DNL and INL versus output code at an ADC sampling frequency $f_s = 21 MS/s$. The maximum INL and DNL were measured at ± 3 and ± 1.4 on a 13-bit scale.

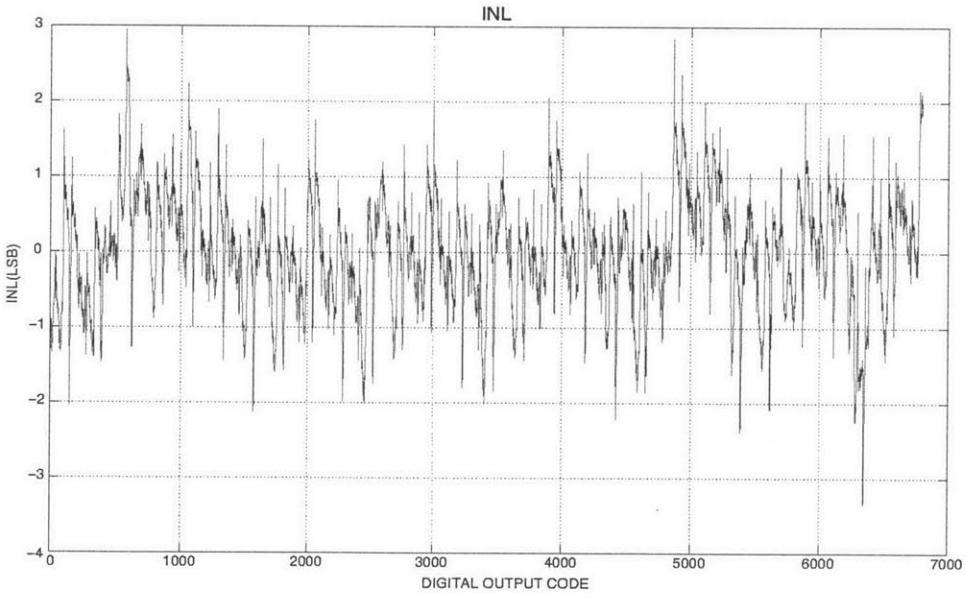


Figure 5-3: INL measurement at fs =21MS/s (13-bit)

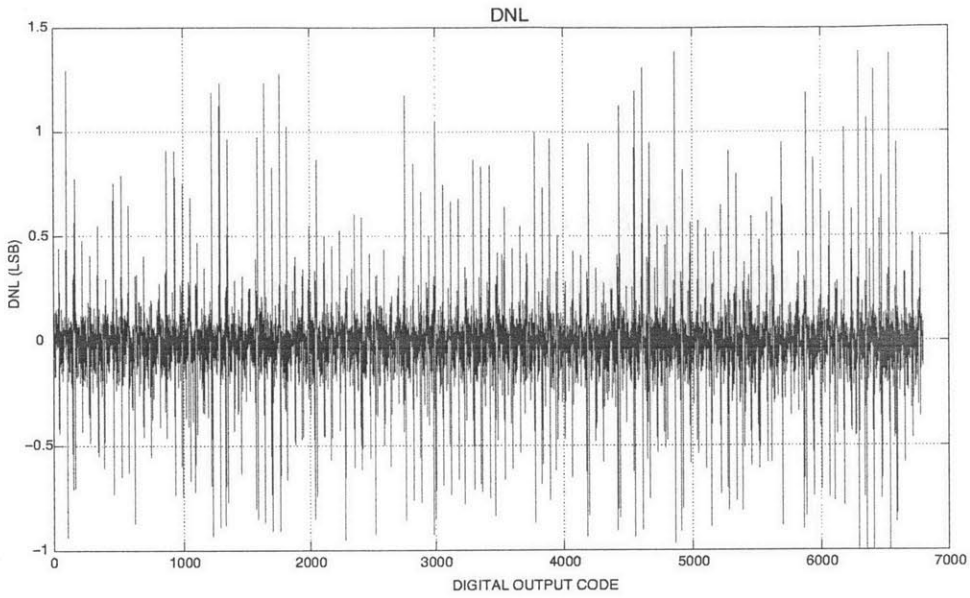


Figure 5-4: INL measurement at fs =21MS/s (13-bit)

5.2.2 Dynamic Linearity and Noise Performance

The dynamic performance of the ADC was measured by analyzing the Fast-Fourier Transform (FFT) of the output codes for an input tone at $5MHz$ and a sampling rate of $21MS/s$. The linearity and noise performance of the converter can be characterized by the signal-to-noise-plus-distortion measurement (SNDR), where SNDR is defined as the ratio of signal power to noise and harmonic power in the digital ADC output. The peak SNR, SNDR, SFDR are shown in Table 5.1. The effective number of bits (ENOB) is determined based on the ADC SNDR for a full scale input signal [28] as follows:

$$ENOB = \frac{SNDR_{dB} - 1.76_{dB}}{6.02dB/bit}. \tag{5.1}$$

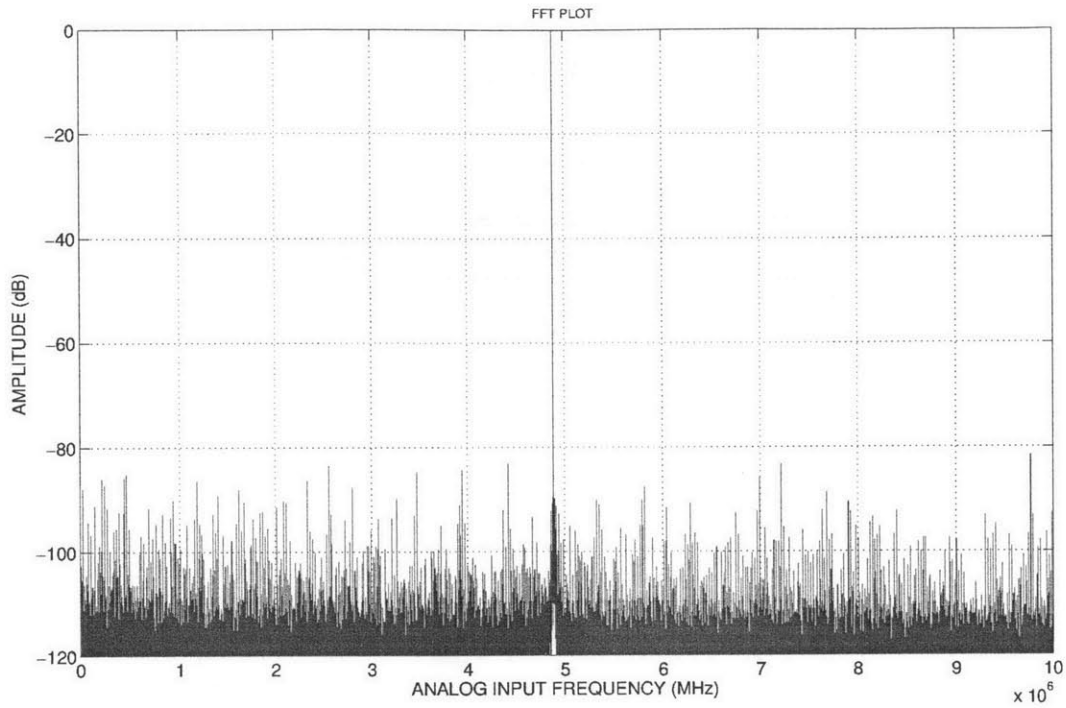


Figure 5-5: Measured FFT of the pipelined ADC for full scale input signal of 5MHz, sampling frequency $f_s = 21MHz$, N = 65K points.

5.2.3 Summary

Table 5.1 summarizes the performance of the implemented ADC. The total analog power is $2.7mW$ at the minimum bias current setting for the ADC, corresponding to a coarse phase differential ramp rate of $0.66\frac{V}{ns}$. Most of the analog power is consumed by the first stage current sources and opamp and the on-chip bias network. The total digital power was measured to be $1.2mW$. There are two reference voltage resistor ladders on chip each consuming $\sim 1.5mW$ for a total of $\sim 3mW$. The analog power includes an on-chip bias circuit. The ADC was tested at a supply of $1.08V$ supply. The sampling frequency was set to $21MS/s$ and the input signal frequency was $5MHz$ as displayed by the FFT plot in Figure 5-5.

The Figure of merit (FOM) for the ADC as a function of the power dissipation P, sampling frequency f_s and the effective number of bits as defined in [41] as:

$$FOM = \frac{P}{f_s 2^{ENOB}}.$$

Specification	Value	Units
Technology	65	nm
Supply voltage	1.08	V
ADC area	700	μm^2
Sampling frequency	21	MS/s
Input frequency	5	MHz
Fully differential input amplitude	1.75	V
Analog power	2.7	mW
Digital power	1.2	mW
ADC voltage references power	3	mW
SNDR	67.9	dB
SNR	68	dB
SFDR	81.5	dB
ENOB	11	bits
FOM	160	fJ

Table 5.1: ADC performance summary

5.3 Limitations on Performance

5.3.1 Stage-Independent Constant Overshoot Correction Error

Constant overshoot correction (as described in Chapter 3) is implemented in the first five stages of the pipelined ADC. Recall from Chapter 2 that the constant overshoot error V_{OV} is defined as the component of the overshoot error at the end of the coarse phase of charge-transfer for the case of a finite ZCD delay of constant value t_d and constant slope ramp $S = \frac{I_0}{C}$ (refer to Eq. 2.14, $V_{OV} = \frac{t_d I_o}{C}$) where I_0 is the current of an ideal current source and C is the load capacitor. The ZCD implementation

is identical in each of the five pipeline stages. However, there is variation in both the ramp rate and the ZCD offset from stage to stage due to layout variations and device mismatch. In addition the wiring parasitic capacitance in each stage is not identical at the ZCD output as the stages are scaled and there are variations in the layout from stage to stage. Both of those factors result in a different ZCD delay t_{d_n} for each stage n and therefore different constant overshoot error V_{OV_n}. Therefore a different correction voltage V_{CORR_n} is necessary for stage n, where n here corresponds to stages 1 to 5. An oversight in the design of the overshoot correction implementation resulted in connecting all five correction voltages corresponding to the first five stages of the pipelined ADC to a single node and therefore a single correction voltage. This precluded proper correction of the constant overshoot error for each stage independently.

Focused ion beam (FIB) technology was used to edit five die, of which three were functional. Through the FIB modification the overshoot correction control signal, *Enable* in Figure 5-6, for stages three through five was disabled permanently leaving only the first two stages with the capability for constant overshoot correction.

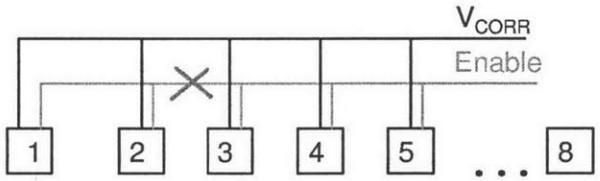


Figure 5-6: The overshoot correction control *Enable* signal is disabled for stages three through five of the pipelined ADC die though a FIB edit.

5.3.2 Constant Overshoot Correction Implementation for the First and Second Pipeline Stage

The first and second pipeline stage require two different correction voltages, while they share a single correction voltage node and the same overshoot correction *Enable* signal controls both as shown in Figure 5-7. In order to apply the respective correction voltage, during the coarse ZCD phase of the charge-transfer operation, to the first

and second stage, a square wave synchronized to the input clock is applied at the correction voltage node V_{CORR} as shown in Figure 5-7. Thus the first stage correction voltage V_1 is applied during ϕ_2 corresponding to the first stage charge-transfer phase. The second stage correction voltage V_2 is applied during ϕ_1 corresponding to the second stage charge-transfer phase. The ADV3219, an 800MHz, low noise 2:1 video analog MUX was used to drive the correction node. The clock signal to the ADV3219 was synchronized to the master clock of the ADC. The first and second pipeline stage therefore have constant overshoot error correction, independent of each other.

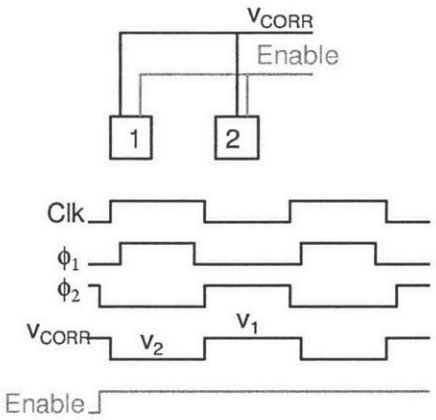


Figure 5-7: To decouple the overshoot correction voltage applied during the coarse phase of charge-transfer to the first and second stage, a square wave synchronized to the master clock *Clk* to the ADC, is applied to the correction voltage node V_{CORR}. The first stage correction voltage V_1 is applied during ϕ_2, while the second stage correction voltage V_2 is applied during ϕ_1, where ϕ_1 and ϕ_2 are the non-overlapping phase clocks of the pipelined ADC.

5.3.3 Output Nonlinearity Error Due to Overshoot Error in the Third Pipeline Stage

The constant overshoot correction is permanently disabled for stages three through five and in consequence the fine phase opamp of each of these stages has to correct the total overshoot error to the desired corresponding accuracy of the stage for a 13-bit piplined ADC. Of those the third stage is most critical because its output non-

linearity requirement is most stringent. Therefore the third stage fine phase opamp must have sufficient DC gain A_3 and sufficient bandwidth $\frac{1}{\tau_3}$ to reduce both the output-dependent component v_{ov} and uncorrected constant component V_{OV} of the ZCD coarse phase overshoot error $v_{OV} = V_{OV} + v_{ov}$. In contrast the fine phase of the first and second stage must correct only the output dependent overshoot error v_{ov} due to the constant overshoot correction.

Recall from Chapter 4 that the output voltage error at the end of the charge-transfer phase is:

$$v_{out_3}(t_{fine}) = \frac{v_{OV_3}}{1 + A_3\beta\gamma} + \frac{v_{OV_3}A_3\beta\gamma}{1 + A_3\beta\gamma}e^{-\frac{t_{fine}(1+A_3\beta\gamma)}{\tau_3}} \tag{5.2}$$

where v_{out_3} is the output of the third pipeline stage, t_{fine} is the fine phase duration, $\beta\gamma = \frac{1}{8}$ is the feedback factor from the output to the input of the opamp, and $\tau_{cl3} = \frac{\tau_3}{1+A_3\beta\gamma}$ is the closed loop bandwidth of the third stage opamp.

The output nonlinearity error of the third stage of an N-bit pipelined ADC referred to the ADC input must be $< \frac{V_{LSB}}{2}$ at 13-bit resolution(where V_{LSB} is the ideal code width of the ADC) [10, 28]. Therefore the third stage output error at the end of the fine phase can be expressed as :

$$v_{out_3}(t_{fine}) < \frac{V_{FS}}{2^{N+1}} \prod_{n=1}^{3} G_n \tag{5.3}$$

where $\prod_{n=1}^{3} G_n$ is the cumulative gain of the first three stages of the ADC, $G_n = 4$ is the gain of stage n, $V_{FS} = 1.75$ is the ADC full scale input and $N = 13$ is the ADC resolution.

The first term of Eq. 5.2 represents the third stage opamp DC gain error at the output while the second term represents the opamp settling error. First only the DC gain error at the output is considered. Substituting just the first term of Eq. 5.2 into Eq. 5.3 yields:

$$\frac{V_{OV_3} + v_{ov_3}}{1 + A_3\beta\gamma} < \frac{V_{FS}}{2^{N+1}} \prod_{n=1}^{3} G_n.$$

Substituting $G_n = 4$ as the gain of stage n, $V_{FS} = 1.75$ and $N = 13$ it follows that the error due to finite opamp gain at the output of the third stage must be:

$$\frac{V_{OV_3} + v_{ov_3}}{1 + A_3\beta\gamma} < 6.8mV. \tag{5.4}$$

At the lowest bias ramp current setting of the ADC, the differential ramp rate is $S_{diff} = 6.6(10^8)\frac{V}{s}$ (refer to Table 4.1). If a worst case ZCD delay $t_d = 200ps$ is assumed (which is a factor of two of the ZCD delay $t_d \simeq 100ps$ from Cadence simulations), the total differential overshoot error is $V_{OV_3} = S_{diff}t_d = 132mV$. From Eq. 5.4 it follows that A_3 has to be larger than 147 for $\beta\gamma = \frac{1}{8}$. Cadence simulation of the ZCD delay showed t_d to be less than $100ps$ and in this case $V_{OV_3} = S_{diff}t_d = 66mV$, the DC gain A_3 must be larger than 70. Therefore in the worst case of $t_d = 200ps$, the third stage opamp DC gain (which is on the order of $40dB$ from Cadence simulations using nominal device models) is not sufficient if bidirectional ramp implementation is used for the coarse phase of the third stage and will result in INL errors in the mid-range between bit decision transitions due to the change in ramp direction. When setting the coarse phase in bidirectional ramp ZCB mode of operation, the gain error changes sign with the output ramp direction change and limits the linearity of the stage. In unidirectional mode the gain error appears as an output voltage offset.

Therefore during testing the third stage was set in unidirectional mode. In unidirectional mode the error term $\frac{V_{OV_3}}{1+A_3\beta\gamma}$ of Eq 5.2 appears as an offset, which is indistinguishable from the remaining offsets in the stage and it does not affect the ADC output linearity as long as the contribution of all offsets does not exceed the over-range protection at the output. The over-range protection is $0.25V$ from either rail.

The dominant source of offset are the BDCs and their offsets, which in worst case can be assumed on the order of $\pm 25mV$ and can contribute $100mV$ of offset at the output for a stage gain of 4. One disadvantage of using unidirectional mode is that in the presence of offsets in the stage, the output can go out of the linear operating range of the cascode current sources, which contributes a larger output-dependent overshoot error at the end of the coarse phase.

Therefore when set in unidirectional mode only the output dependent overshoot component of the gain error must satisfy Eq. 5.4:

$$\frac{v_{ov_3}}{1 + A_3\beta\gamma} < 6.8mV,$$

which is consistent with the original design of the third stage opamp. From Table 4.1 the output dependent overshoot error for ZCD delay $t_d = 200ps$ is $v_{ov_3} = 1.4mV$ which even with no fine phase present is $< 6.8mV$. If the output swing is larger than the linear range of operation of the current sources from Cadence simulations the differential ramp change is on the order of $\Delta S_{diff} = 1.6(10^8)$, at the minimum bias current setting of the ADC, for an output range from $0V$ to $0.9V$ and upper rail of $1V$. The equivalent differential output dependent overshoot error for a ZCD delay $t_d = 200ps$ is $v_{ov_3} = 32mV$. Substituting $v_{ov_3} = 32mV$ into $\frac{v_{ov_3}}{1+A_3\beta\gamma} < 6.8mV$ yields an opamp DC gain requirement of $A_3 > 29$ which is within the design parameters of the third stage opamp (refer to Table 4.3).

Next the settling error of the third stage opamp is considered. Substituting the second term of Eq. 5.2 into Eq. 5.3 yields:

$$\frac{v_{OV_3} A_3\beta\gamma}{1 + A_3\beta\gamma} e^{-\frac{t_{fine}(1+A_3\beta\gamma)}{\tau_3}} < \frac{1}{2}\left(\frac{V_{FS}}{2^{N+1}}\right)\prod_{n=1}^{3} G_n, \tag{5.5}$$

where for a more conservative calculation the error has been assumed to be $\frac{1}{2}\left(\frac{V_{FS}}{2^{N+1}}\right)$. Further to simplify the analysis, it is a assumed that $\frac{A_3\beta\gamma}{1+A_3\beta\gamma} \approx 1$. From Eq. 5.5 it

follows that:

$$\tau_{cl_3} < \frac{\frac{1}{3}T_s}{ln\left(\frac{1}{2}\frac{V_{FS}}{2^{N+1}}\prod_{n=1}^{3}G_n\right)}$$

where $t_{fine} = \frac{1}{3}T_s$ by design and T_s is the ADC sampling period. Substituting $N = 13$, $G_n = 4$ and $v_{OV_3} = 132mV$ for a ZCD delay $t_d = 200ps$ results in the following expression of the closed loop time constant as a function of the ADC sampling frequency:

$$\begin{aligned}\tau_{cl_3} &< \frac{\frac{1}{3}T_s}{ln\left(\frac{v_{OV_3}}{\frac{1}{2}\frac{V_{FS}}{2^{N+1}}\prod_{n=1}^{3}G_n}\right)} \\ &< \frac{T_s}{11}.\end{aligned} \tag{5.6}$$

The closed loop time constant of the third stage opamp τ_{cl} is $1.1ns$ from Cadence simulations with nominal device models, and $\tau_{cl} = 1.9ns$ with slow device models for both PMOS and NMOS devices. From Eq 5.6 the worst case sampling period of the ADC for $\tau_{cl} = 1.9ns$ is $T_s = 21ns$, corresponding to a sampling frequency of $47MS/s$.

From INL measurements at a sampling rate of $21MS/s$ for an input signal of $5MHz$, when the third pipeline stage is configured in bidirectional ZCB coarse phase mode the constant error contributed by the third stage is slightly less than $\sim 1LSB$ on a 13-bit scale. It can be concluded that is sufficient to correct the output dependent overshoot error as explained above. However, due to the unidirectional operation, the larger overshoot may have caused the current sources to go out of their high-output resistance region and mayeb have contributed more output nonlinearity than simulated.

At the same time at $21MS/s$ the closed loop bandwidth of the opamp is sufficient to settle v_{OV_3} to the desired accuracy of the third stage output. Measurements at an ADC

sampling rate of $41MS/s$ showed an increase in the third stage error contribution to $\sim 2LSBs$ on a 13-bit scale, which indicates that the opamp closed loop settling time is larger than simulated. Note that if the total overshoot error in the third stage v_{OV_3} is corrected to less than $1LSB$ at on 13-bit scale, referred to the ADC input of $V_{FS} = 1.75V$, it can be concluded that the gain is sufficient to correct the output dependent component of the overshoot error, which is smaller than its constant counterpart as the original design intended.

The lack of constant overshoot correction is a limiting factor in the ADC output linearity especially at frequencies below $40MS/s$. From the analysis above at $20MS/s$ it is assumed that the fine phase opamp fully settles.

5.3.4 First and Second Stage Opamp Gain and Settling Error

The bidirectional ZCB coarse phase implementation produces an INL and DNL error in the mid-range between transitions of the sub-ADC in the first and second pipeline stages of the ADC as discussed in Section 3.2. The source of nonlinearity is the change in polarity of the overshoot error with the output-sign bit, which determines the change in ramp direction:

$$v_{OV} = \begin{cases} v_{OV}, & v_{OUT} < V_{CM} \\ -v_{OV}, & v_{OUT} > V_{CM} \end{cases}.$$

The overshoot correction cancels to first order the overshoot component $\pm V_{OV}$ of $v_{OV} = \pm V_{OV} - (\pm v_{ov})$ by switching the polarity of the correction voltage applied with the output-sign bit as described in Section 3.3. The remaining output-dependent component $\pm v_{ov}$ is settled by the opamp in feedback during the fine phase:

$$v_{OUT}(t) = \begin{cases} v_O + v_{ov}(\frac{1}{1+A\beta\gamma} + \frac{A\beta\gamma}{1+A\beta\gamma}e^{-\frac{t(1+A\beta\gamma)}{\tau}}), & v_{OUT} < V_{CM} \\ v_O - v_{ov}(\frac{1}{1+A\beta\gamma} + \frac{A\beta\gamma}{1+A\beta\gamma}e^{-\frac{t(1+A\beta\gamma)}{\tau}}), & v_{OUT} > V_{CM} \end{cases}, \quad (5.7)$$

where v_{OUT} is the stage output voltage during the fine phase and v_O is the ideal output voltage.

Mid-range errors in both the first and second stage limit the output linearity of the ADC to ± 3 LSBs on a 13-bit scale at $20MS/s$ as shown in Figure 5-3. From Eq. 5.7 the error in both stages is due to larger output dependent error v_{ov} than in simulations or insufficient gain $A_{1,2}$. The coarse phase nonlinearity and fine phase opamp gain cannot be decoupled from the measurements because the main bias network controls both the ramp current source and the opamp bias current for all stages. Therefore it is assumed that they both contribute to limiting the INL and DNL of the ADC. From Table 4.3 a minimum gain of $35dB$ and larger than 8-bit coarse phase nonlinearity referred to the ADC input limits the ADC linearity to < 12 bits. At the nominal corner the gain is $40dB$, which is too close to the nominal design requirements and does not allow sufficient margin of error for process variations. It follows that the coarse phase nonlinearity is larger than in simulation (refer to Table 4.1). From Cadence simulation over corners the worst case gain of the first stage is $35dB$.

From Subsection 4.3.2.5, the first stage output linearity requirement was established to be 11 bits for $\frac{1}{2}$ LSB accuracy at 13 bit resolution referred to the input for a first stage gain G_1 of 4. At the nominal design the fine phase accuracy requirement $K = 3$ (refer to Table 4.3) and the coarse phase linearity requirement is 8. For 8-bit linearity at the first stage output at the end of the coarse phase, the output error referred to the input must be:

$$\varepsilon_1 < \frac{V_{FS}G_1}{2^{N+1-K}}.$$

Substituting $G_1 = 4$, $V_{FS} = 1.75$, $K = 3$ and $N = 13$, the output error at the end of the coarse phase is $\varepsilon_1 < 3.4mV$.

One possible source of error limiting the coarse phase linearity is insufficient power supply rejection of the zero crossing detector (ZCD). The power supply of the ZCD was incrementally decreased by $40mV$. The observed change in an intentionally

uncorrected constant overshoot error as measured on a 13-bit scale INL plot varies at a rate of less than $2LSB/40mV$ on a 13-bit scale. Assuming the fine phase opamp has fully settled, the nominal opamp gain is $A_1 = 40dB$ and the closed loop feedback factor is $\beta\gamma = \frac{1}{8}$, the fine phase attenuates the coarse phase by a factor of 13. The deduced error from the INL plot on a 13-bit scale for $V_{FS} = 1.75V$ is then $\varepsilon_{estimated} \approx (1+A\beta\gamma)\left[\frac{V_{FS}}{2^{13}}(2LSBs)\right] \approx 5.6mV$. It is larger than the simulated error in Subsection 4.4.3.2, which is less than the 8-bit coarse phase requirement. Note that this is an estimation, however it illustrates the power supply sensitivity of the ZCD delay.

Insufficient settling of the DAC voltage references at each bit decision comparator transition also can contribute to coarse phase output nonlinearity especially at coarse phase maximum ramp duration of $\sim 1.6ns$ at the minimum bias setting of the ADC. The references have to settle to the desired accuracy of 13 bits referred to the input of the ADC ideally by the minimum output voltage of the nominal output swing of the stage. In the prototype ADC the minimum preset phase duration of $\sim 400ps$, while the maximum preset phase duration is $\sim 1ns$. The first stage unit capacitor is $850fF$, and the on-resistance of the switch to either V_{REFP} or V_{REFM} is $R_{sw} \sim 10\Omega$, which results in a time constant of $8.5ps$. As the ramp rate duration is fixed by the minimum bias current the preset phase duration could be stepped from $1ns$ in increments of $100ps$. The preset duration did not affect the mid-range INL error down to $600ps$. The reference switch resistance R_{sw} does not have a significant effect on the internal voltage reference voltage settling response, when bond-wire and board trace inductance is taken into account, therefore a damping resistor in series with the reference voltage regulator output on board is used. A model for settling of the reference voltages is considered in Appendix F taking into account bond-wire and test board trace inductance as well as a damping series resistor R for an on-chip reference decoupling capacitor of $1.3nF$. The system is critically damped for $R \simeq 2\Omega$, which was used during testing.

In order to establish the fine phase opamp settling error contribution, the constant

magnitude component of the overshoot error $\pm V_{OV}$ for both stages was intentionally not fully corrected through the correction applied as described in Subsection 5.3.2 to establish at what sampling rate the opamp settling error of each stage limits the output ADC linearity on a 13-bit scale. The first stage overshoot error did not change up to a sampling rate of $51MS/s$, while the second stage overshoot error increased by approximately $\sim 1LSB$ at an ADC sampling rate of $41MS/s$, which indicates that the second stage opamp closed loop time constant is not sufficient to settle the coarse phase overshoot error at $41MS/s$ and limits the INL and DNL of the ADC at higher sampling rates at the minimum bias current.

From Figure 5-3, the opamp gain of both stages is not sufficient to correct the nonlinearity of the coarse phase of each respective stage. From Table 4.3 a minimum gain of $35dB$ and larger than 8-bit coarse phase nonlinearity referred to the ADC input limits the ADC linearity to < 12 bits. From Cadence simulation over corners the worst case gain of the first stage is $35dB$. At the nominal corner the gain is $40dB$, which is too close to the nominal design requirements and did not allow margin of error for process variations.

5.3.5 Constant Magnitude Overshoot Error with First Stage DAC Transitions

The first stage total overshoot error v_{OV} is different by up to $\sim 2LSBs$ for different DAC configurations in the first stage as can be seen in the INL plot (refer to Figure 5-3). The total overshoot error is a function of the ramp rate S and the ZCD delay t_d. In measurements the error is present when no overshoot correction is applied as well. It is assumed that the reference voltages switched with each DAC configuration settle by the end of the preset phase, because varying the preset phase duration did not affect the overshoot voltage variation.

5.3.5.1 Output-Sign Bit Decision Comparator Offset

One possible source of error is random offset in the output sign bit decision comparator (BDC) which determines the switch in output current ramp direction for a fixed DAC capacitor configuration. A different BDC determines the output sign bit for each DAC capacitor transition of the first stage. If the worst case offset error of a BDC is on the order of $25mV$ for one DAC configuration and $-25mV$ for another DAC configuration, the output ramp switches direction at output voltages separated by a difference of $G_1(25mV - (-25mV) = G_150mV$, where $G_1 = 4$ is the gain of the first stage. The coarse phase output ramp rate varies with output voltage due to current source finite output resistance and nonlinear capacitance. At the minimum bias current the differential ramp rate is $S_{diff} = 6.6(10^8)\frac{V}{s}$ (from Table 4.1) and the ramp rate variationΔS from Cadence simulations over the valid output range of $\pm 250mV$ is $7.2(10^6)\frac{V}{s}$. Thus if half of the ramp rate variation $3.6(10^6)\frac{V}{s}$ is assumed over a $\sim 200mV$ range and a worst case ZCD delay of $t_d = 200ps$ is assumed the output voltage overshoot error difference between the two DAC configurations is $0.7mV$ at the end of the coarse phase. If a gain of $35dB$ (worst case first stage DC opamp gain from Cadence simulations over corners) is assumed, the output nonlinearity of $0.7mV$ is attenuated by $\frac{1}{1+A_1\beta\gamma}$, where A_1 is the fine phase first stage opamp gain, $\beta = \frac{1}{4}$ is the feedback factor from the first stage output to the opamp input and $\gamma = \frac{1}{2}$ is the attenuation factor form the opamp output to the stage output. The residual first stage output voltage error is then $88uV$ and contributes $\sim \frac{1}{2}LSB$ on a 13-bit scale for $1.75V$ ADC input range. If the ramp rate variation is larger than $3.6(10^6)\frac{V}{s}$ as indicated by the INL and DNL results in Figure 5-3 and Figure 5-4 than the error contribution is likely larger than $\sim \frac{1}{2}LSB$.

5.3.6 Comparison with Other ZCB References

Authors	Publication	Technology	Supply voltage	FOM ($\frac{fJ}{step}$)	Sampling rate (MS/s)	ENOB	SFDR (dB)
this work		$65nm$	$1V$	160	20	11	81.5
Hershberg[21]	$ISSCC'10$	$180nm$	$1.8V$	406	20	11.1	76.5
Lee*[26]	$JSSCC'12$	$65nm$	$1V$	41	50	11	85.8
Chu[8]	$VLSI'10$	$90nm$	$1.2V$	53	100	10.5	80
Brooks[5]	$ISSCC'09$	$90nm$	$1.2V$	88	50	10	68
				98	25	10.6	73
Shin[37]	$VLSI'08$	$65nm$	$1.2V$	161	26	8.73	70.4
Sepke [35]	$ISSCC'06$	$180m$	$1.8V$	300	8	10	

Table 5.2: Performance comparison to other ZCB pipelined ADCs

* The topology is intended as a voltage programmable ADC with capability for scaled supply down to $0.5V$ and the operation at $1V$ is chosen for comparison

Table 5.2 shows the comparison to previous ZCB pipelined ADC implementations. The hybrid CLS-OpAmp/ZCB architecture was first presented in [21]. This work, despite its performance limitations preserves the output linearity at the same sampling speed in 65nm CMOS technology at 1V supply. The coarse phase improvements despite the very fast differential coarse phase ramp rate of $0.66\frac{V}{ns}$ and diminished fine phase opamp gain compared to a $180nm$ implementation contribute to maintaining the ADC performance. A two phase topology is implemented in [35], [37] and [26] and single phase ZCB implementation is used in [8, 5]. It is clear from Table 5.2 that ZCBC based only implementations achieve much better power efficiency and single phase implementations can maintain the performance at high ADC sampling rates.

Chapter 6

Conclusion and Future Work

In this work, the use of a two phase hybrid architecture, combining the power efficiency of ZCBCs with the benefit of an opamp in negative feedback, were explored for improved precision through the design of a 13-bit pipelined ADC. In addition the use of correlated level shifting (CLS) allowed for a limited nominal opamp swing and lessened requirements on the opamp gain and bandwidth, which allowed for a single stage opamp topology and better power efficiency than an opamp based pipelined stage. Current steering is used to minimize the ZCD delay for improved coarse phase linearity. In addition the use of bidirectional ramp ZCB operation was explored for extended pipeline stage output swing and reduced current for a fixed sampling rate. This is especially relevant to a high precision design in deep sub-micron technologies, in which the supply limits the available output range. In addition high precision requires large input sampling capacitors and therefore large currents in a ZCB implementation and a ramp current reduction by a factor of two is significant. However, the bidirectional operation was one of the limiting factors of the prototype ADC performance below the desired accuracy and sampling speed as it introduced errors in the INL and DNL at the mid-range between bit decision transitions. The loop gain of the fine phase was not sufficient to reduce the nonlinearity errors due to the bidirectional operation to the desired linearity of 13 bits. An oversight of

the design is that both the bidirectional ramp operation and CLS allowed for double cascoding of the current sources and single stage telescopic opamp implementation even at 1V supply and was not implemented in this design. Using a double cascoded telescopic amplifier would improve the fine phase loop gain and not limit the opamp output as in the prototype the output range was designed to be significantly larger (by a factor of 6 than the required for the maximum expected coarse phase output nonlinearity). An oversight in the overshoot correction implementation limited the third stage performance to the minimum on-chip bias current setting and a sampling rate of $20MS/s$.

An area for future exploration is to use feedback within the pipeline stage in order to correct the constant magnitude overshoot error which, switches sign with output ramp direction. The error can be sensed at the opamp outputs at the end of the fine phase of charge-transfer and is amplified by the ratio of the total load capacitor to correlated level shifting capacitor. The technique can be used with unidirectional ramp implementation as well as with a ZCB fine phase implementation.

The lack of separate bias control for the current sources and the fine phase opamp of the on-chip bias network precluded testing at lower ramp rates and the results reflect the linearity limitations of a ZCB coarse phase, which is comparable to a single-phase bidirectional ZCB implementation operating at roughly $200MS/s$ attenuated by the loop gain of the fine phase, which is on the order of 10 for this design. Furthermore future designs should allow separate controls for flexibility in testing.

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Appendix A

Transfer Function of Opamp Based Multiply-by-two

Switched-capacitor Circuit

To derive the transfer function of the multiply-by-two switched-capacitor circuit in Figure 2-2(Chapter2), charge conservation is used. The total charge at the end of ϕ_1 should be equal to the total charge at the end of ϕ_2. Assuming an ideal opamp of infinite gain, the change in charge on capacitor C_{1n} is:

$$\Delta Q_1 = C_{1n}[(V_{CM} - dV_{ref}) - (V_{CM} - V_{IN})]. \tag{1}$$

The change in charge on the feedback capacitor C_{2n} is:

$$\Delta Q_2 = C_{2n}[(V_O - V_{CM}) - (V_{IN} - V_{CM})]. \tag{2}$$

Charge conservation holds that the change in charge on the input capacitor C_{1n} must equal the change in charge on the feedback capacitor C_{2n} at the end of ϕ_2:

$$\Delta Q_1 = \Delta Q_2. \tag{3}$$

Substituting Eq. 7 and Eq. 8 into Eq. 3 gives the following relationship between V_{OUT} and V_{IN}:

$$V_{OUT} = (\frac{C_{1n} + C_{2n}}{C_{2n}})V_{IN} - \frac{C_{1n}}{C_{2n}}dV_{ref}$$

for an ideal opamp of infinite gain.

The transfer function, for an opmap-based multiply-by-two circuit of a pipelined ADC stage for an opamp of finite gain A, can be derived using charge conservation, following the same steps as above. The change in charge on capacitor C_{1n} is:

$$\Delta Q_1 = C_{1n}\left[(V_X - d\,V_{ref}) - (V_{CM} - V_{IN})\right] \tag{4}$$

where $V_X = V_{CM} - \frac{V_{OUT}}{A}$. The change in charge on the feedback capacitor C_{2n} is:

$$\Delta Q_2 = C_{2n}\left[(V_{OUT} - V_X) - (V_{IN} - V_{CM})\right] \tag{5}$$

Charge conservation requires that:

$$\Delta Q_1 = \Delta Q_2 \tag{6}$$

Substituting Eq. 4 and Eq. 5 into Eq. 6 yields:

$$C_{1n}(V_{OUT} - d\,V_{ref} - \frac{V_{OUT}}{A} = C_{2n}(V_{OUT} + \frac{V_{OUT}}{A} - V_{IN})$$

$$V_{OUT} = \left(\frac{1}{1 + \frac{1}{A}(\frac{C_{1n}+C_{2n}}{C_{2n}})}\right)\left(\frac{C_{1n}+C_{2n}}{C_{2n}}V_{IN} - \frac{C_{1n}}{C_{2n}}d\,V_{ref}\right).$$

Appendix B

Dual Ramp ZCBC Fine Phase Overshoot Error

From 2.14, the coarse phase overshoot is to first order can be approximated by : $V_{ov_{coarse}}(V_0(t)) = \frac{I_{0_{coarse}}}{C} t_d - \frac{V_0(t) t_d}{R_{O_{coarse}} C}$, where $V_0(t) = \frac{I_{0_{coarse}} t}{C}$ is the ideal output voltage. Then the output voltage is :

$$V_{OUT_{coarse}}(t) = V_0(t) + V_{ov_{coarse}}(V_0(t)) \tag{7}$$

Assume t_d is the same for both phases of operation and $C = C_{eq} + C_{n+1}$ in both cases, where $C_{eq} = C_{1n} \parallel C_{2n}$.

$$V_{ov_{fine}} = \frac{1}{C}\left(\int_0^{t+t_d} (I_{fine} + \frac{V_{OUT_{coarse}}(t)}{R_{O_{fine}}}) dt. \right. \tag{8}$$

If the the fine phase current dependence on the variable coarse phase overshoot error then the the fine phase output voltage at the ZCD transition can be expressed by substituting Eq. 7 into Eq. 8 :

$$
\begin{aligned}
V_{OUT_{fine}}(t) &= -\frac{1}{C}\Big(\int_0^{t+t_d}(I_{fine}+\frac{V_{OUT_{coarse}}(t)}{R_{O_{fine}}})dt \\
&= -\frac{1}{C}\Big(\int_0^{t+t_d}(I_{fine}+\frac{\frac{I_{0_{coarse}}}{C}t+\frac{I_{0_{coarse}}}{C}t_d}{R_{O_{fine}}})dt - \frac{1}{C}\int_0^{t+t_d}(\frac{-I_{0_{coarse}}t_d}{R_{O_{fine}}R_{O_{coarse}}C^2}t)dt \\
&= -\frac{1}{C}\Big(\int_0^{t+t_d}(I_{fine}+\frac{\frac{I_{0_{coarse}}}{C}(t+t_d)}{R_{O_{fine}}})d(t+t_d) + \frac{1}{C}\frac{I_{0_{coarse}}t_d(t+t_d)^2}{R_{O_{fine}}C^2R_{O_{fine}}} \\
&= -\left[\frac{I_{fine}(t+t_d)}{C}+\frac{I_{0_{coarse}}(t+t_d)^2}{2C^2R_{O_{fine}}}-\frac{I_{0_{coarse}}t_d(t+t_d)^2}{R_{O_{fine}}C^3R_{O_{fine}}}\right] \\
&= -\frac{I_{fine}(t+t_d)}{C}-\left[\frac{I_{0_{coarse}}t^2}{2C^2R_{O_{fine}}}+\frac{I_{0_{coarse}}t_d^2}{2C^2R_{O_{fine}}}+\frac{I_{0_{coarse}}tt_d}{C^2R_{O_{fine}}}\right]\left(1-\frac{t_d}{R_{O_{coarse}}C}\right) \\
&= -\frac{I_{fine}(t+t_d)}{C}+\left[-\frac{V_0(t)^2}{2I_{0_{coarse}}R_{O_{fine}}}-\frac{I_{0_{coarse}}t_d^2}{2C^2R_{O_{fine}}}-\frac{V_0(t)t_d}{CR_{O_{fine}}}\right]\left(1-\frac{t_d}{R_{O_{coarse}}C}\right) \\
&= -\frac{I_{fine}t}{C}-\frac{I_{fine}t_d}{C}-\frac{V_0(t)t_d}{CR_{O_{fine}}}\left(1-\frac{t_d}{R_{O_{coarse}}C}\right)-\left(\frac{I_{0_{coarse}}t_d^2}{2C^2R_{O_{fine}}}+\frac{V_0(t)^2}{2I_{0_{coarse}}R_{O_{fine}}}\right)\left(1-\frac{t_d}{R_{O_{coarse}}C}\right)
\end{aligned}
$$

Subtracting the ideal voltage $V_{fine_{ideal}} = -\frac{I_{0_{fine}}t}{C}$ from $V_{fine}(V_0(t))$, and ignoring the square terms the output error at the end of ϕ_2 can be defined as as function of the ideal output voltage $V_0(t)$:

$$
V_{ov_{fine}}(t_d) = -\frac{I_{fine}t_d}{C}-\frac{V_0(t)t_d}{CR_{O_{fine}}}
$$

The fine phase output dependent overshoot is then:

$$
v_{ov_{fine}}(V_0(t)) = -V_0(t)\frac{t_d}{R_{O_{fine}}C}\left(1-\frac{t_d}{R_{O_{coarse}}C}\right)
$$

Appendix C

Dual Ramp ZCBC with CLS Fine Phase Overshoot Error

From Eq. 2.14, the coarse phase overshoot error is: $V_{ov_{coarse}}(V_0(t)) = \frac{I_{0_{coarse}}}{C_{coarse}} t_d - \frac{V_0(t)t_d}{R_{O_{coarse}} C_{coarse}} - \frac{(V_0(t))^2}{2I_0 R_O} - \frac{I_0 t_d^2}{2R_O C_{coarse}^2}$, where $V_0(t) = \frac{I_{0_{coarse}} t}{C_{coarse}}$. Only the output dependent component of the overshoot error is corrected during the fine phase and it is assumed that the ZCD delay t_d is the same for both phases. The voltage divider from the ZCBC output node V_{OUT} to the bottom plate voltage of C_{CLS} ($V_{fineCLS}$) is $\frac{1}{\gamma} V_{OUT}(t) = V_{fineCLS}(t)$, where $\gamma = \frac{C_{CLS}}{C_{eq}+C_{n+1}+C_{CLS}}$. The capacitor being discharged by the fine phase current source is $C_{fine} = C_{CLS} \parallel (C_{n+1} + (C_{1n} \parallel C_{2n}))$. Let

$$v_{ov_{coarse}} = -\frac{V_0(t)t_d}{R_{O_{coarse}} C} = -\frac{I_{0_{coarse}} t_d t}{R_{O_{coarse}} C} \tag{9}$$

be the coarse phase output dependent overshoot error, then the fine phase overshoot voltage at V_{fine} is:

$$V_{ov_{fineCLS}} = -\frac{1}{C_{fine}} \left(\int_0^{t_d} \left(I_{fine} + \frac{V_{CM} - \frac{1}{\gamma} v_{ov_{coarse}}}{R_{O_{fine}}} \right) dt \right) \tag{10}$$

where V_{CM} is the voltage at the bottom plate of C_{CLS} during the coarse phase and therefore the initial condition at the output of the fine phase current source, and $R_{O_{fine}}$ is the output impedance of the fine phase current source. Substituting Eq. 9 into Eq. 10 yields:

$$\begin{aligned} V_{ov_{fineCLS}} &= -\frac{1}{C_{fine}} \left(\int_0^{t_d} \left(I_{fine} + \frac{V_{CM} - \frac{1}{\gamma} v_{ov_{coarse}}}{R_{O_{fine}}} \right) dt \right) \\ &= -\frac{I_{fine} t_d}{C_{fine}} - \frac{V_{CM} t_d}{R_{O_{fine}} C_{fine}} + \frac{-\frac{1}{\gamma} I_{0_{coarse}} t_d^3}{2R_{O_{fine}} R_{O_{coarse}} C_{fine} C_{coarse}^2} \end{aligned}$$

Let $I_{0_{fine}} = I_{fine} + \frac{V_{CM}}{R_{O_{fine}}}$, then

$$V_{ov_{fineCLS}} = -\frac{I_{0_{fine}} t_d}{C_{fine}} + \frac{\frac{1}{\gamma} I_{0_{coarse}} t_d^3}{2R_{O_{fine}} R_{O_{coarse}} C_{fine} C_{coarse}^2}. \tag{11}$$

The fine phase overshoot voltage at the output node V_{OUT} is then $V_{ov_{fine}} = \gamma V_{ov_{fineCLS}}$.

To make a comparison to the fine phase overshoot error in a dual ramp ZCBC without use of CLS, the fine phase overshoot error is expressed as:

$$V_{ov_{fine}} = -\frac{1}{C_{fine}} \left(\int_0^{t_d} (I_{fine} + \frac{V_0(t) - v_{ov_{coarse}}}{R_{O_{fine}}}) dt. \right. \tag{12}$$

Substituting Eq. 9 into Eq. 12 yields:

$$\begin{aligned} V_{ov_{fine}} &= -\frac{1}{C_{fine}} \left(\int_0^{t_d} (I_{fine} + \frac{V_0(t) - v_{ov_{coarse}}}{R_{O_{fine}}}) dt \right. \\ &= -\frac{1}{C_{fine}} \left(\int_0^{t_d} (I_{fine} + \frac{\frac{I_{0_{coarse}} t}{C_{coarse}} - v_{ov_{coarse}}}{R_{O_{fine}}}) dt \right. \\ &= -\frac{I_{fine} t_d}{C_{fine}} - \frac{I_{0_{coarse}} t_d^2}{2R_{O_{fine}} C_{fine} C_{coarse}} + \frac{I_{0_{coarse}} t_d^3}{2R_{O_{fine}} R_{O_{coarse}} C_{fine} C_{coarse}^2}. \end{aligned} \tag{13}$$

Appendix D

Derivation for optimal value of level shifting capacitor in a hybrid CLS-OpAmp/ZCB switched capacitor circuit

The coarse phase ramp current in a hybrid CLS-OpAmp/ZCB circuit is $I = I_C + I_{C_{CLS}} = SC + SC_{CLS} = S(C + C_{CLS})$,where S is the coarse phase ramp rate.

The variable $f(C_{CLS}) = Iv_{amp}$, where $v_{amp} = v_{ov}\frac{C_{CLS}+C}{C_{CLS}}$ is the output swing of the opmap can be optimized with respect to C_{CLS} by first taking the derivative of $f(C_{CLS})$:

$$\begin{aligned}\frac{df}{dC_{CLS}} &= \frac{d}{dC_{CLS}}\left[S(C + C_{CLS})\left(v_{ov}\frac{C_{CLS}+C}{C_{CLS}}\right)\right] \\ &= Sv_{ov}\frac{C_{CLS}(2C + 2C_{CLS}) - (C + C_{CLS})^2}{C_{CLS}^2} \\ &= Sv_{ov}\frac{C_{CLS}^2 - C^2}{C_{CLS}^2}\end{aligned}$$

and then setting $\frac{df}{dC_{CLS}} = 0$ results in:

$$C_{CLS} = C.$$

The second derivative $\frac{d^2f}{dC_{CLS}} = -\frac{2C^2}{C_{CLS}^3} < 0$, which proves $f(C_{CLS}) = Iv_{amp}$ is a minimum at $C_{CLS} = C$.

Appendix F

Reference Voltage Model

A simplified model for the reference voltage switching is shown in Figure -1. The switch *sw* is turned on at the beginning of the charge-transfer phase ϕ_2 at every clock cycle of the ADC.

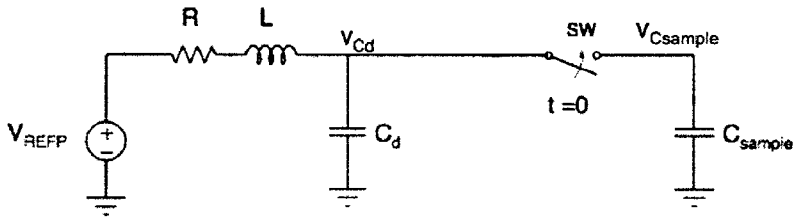


Figure -1: Model of reference voltage, including bond-wire and test board trace inductance L, damping series resistance R, on-chip decoupling capacitor C_d, sampling capacitor C_{sample} and reference switch resistance R_{sw}.

At the beginning of ϕ_2, capacitor C_{sample}, which is assumed to be fully discharged, is connected through switch *sw* in Figure -1 in parallel with the on-chip decoupling

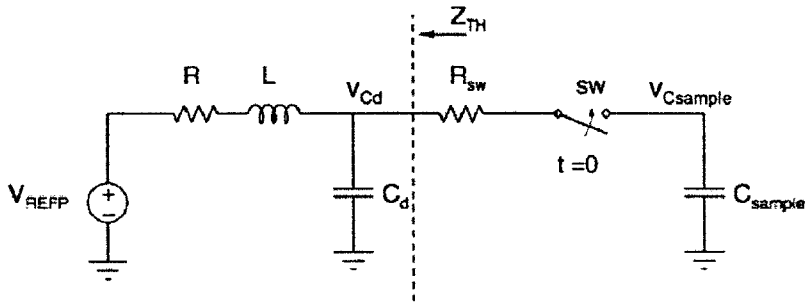
capacitor C_d. Capacitor C_d has been previously charged to V_{REFP}. As charge is shared between C_{sample} and C_d, at time $t = 0$, which corresponds to the beginning of ϕ_2 , the initial voltage $V_{C_{sample}}(0^+)$ can be found to be:

$$V_{C_{sample}}(0^+)(C_d + C_{sample}) = Q_{C_d}(0^-) + Q_{C_{sample}}(0^-), \tag{14}$$

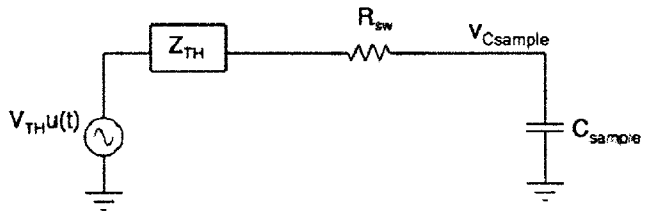
where $Q_{C_{sample}}(0^-) = 0$ and $Q_{C_d}(0^-) = V_{REFP}C_d$. It follows that:

$$V_{C_{sample}}(0^+) = \frac{V_{REFP}C_d}{(C_d + C_{sample})}. \tag{15}$$

To derive the transfer function for the above network, the Thevenin equivalent at node V_{C_d} is found as shown in Figure -2.



(a)



(b)

Figure -2: Simplified reference voltage model

The Thevenin equivalent impedance Z_{TH} is :

$$Z_{TH} = (Ls + R) \parallel \frac{1}{C_d s} \tag{16}$$
$$= \frac{Ls + R}{(Ls + R)C_d s + 1}.$$

The equivalent voltage V_{TH} (s) is :

$$V_{TH}(s) = \frac{V_{REFP}}{s}(\frac{1}{(Ls + R)C_d s + 1}. \tag{17}$$

Let $v_{IN}(s) = \frac{V_{REFP}}{s}$, then $H(s) = \frac{v_{C_{sample}}}{v_{IN}}$ is :

$$H(s) = \frac{1}{(Ls + R)C_d s + 1}(\frac{\frac{1}{C_{sample}s}}{\frac{Ls+R}{(Ls+R)C_d s+1} + R_{sw} + \frac{1}{C_{sample}s}}),$$

where the denominator of $H(s)$ is $den(s) = 1$ and the numerator of $H(s)$ is $num(s) = s3R_{sw}C_{sample}LC_d + s^2(L(C_d + C_{sample}) + R_{sw}RC_dC_{sample}) + s(R(C_d + C_{sample}) + R_{sw}C_{sample}) + 1$.

Next we substitute real design values in Eq. ?? for the on-chip decoupling capacitor $C_d = 1.3nF$, sampling capacitor $C_{sample} = 6.8pF$ and reference switch resistance $R_{sw} = 10\Omega$. The bond-wire inductance is approximated to be $2nH$, assuming a bond-wire model of $1nH/mm$. MATLAB plots for a damping resistor of $R = 0.5\Omega$, $R = 1\Omega$ and $R = 2\Omega$ are shown in Figure -3, Figure -4 and Figure -5 respectively. For a damping resistor $R = 2\Omega$ the system is approximately critically damped from Figure -5.

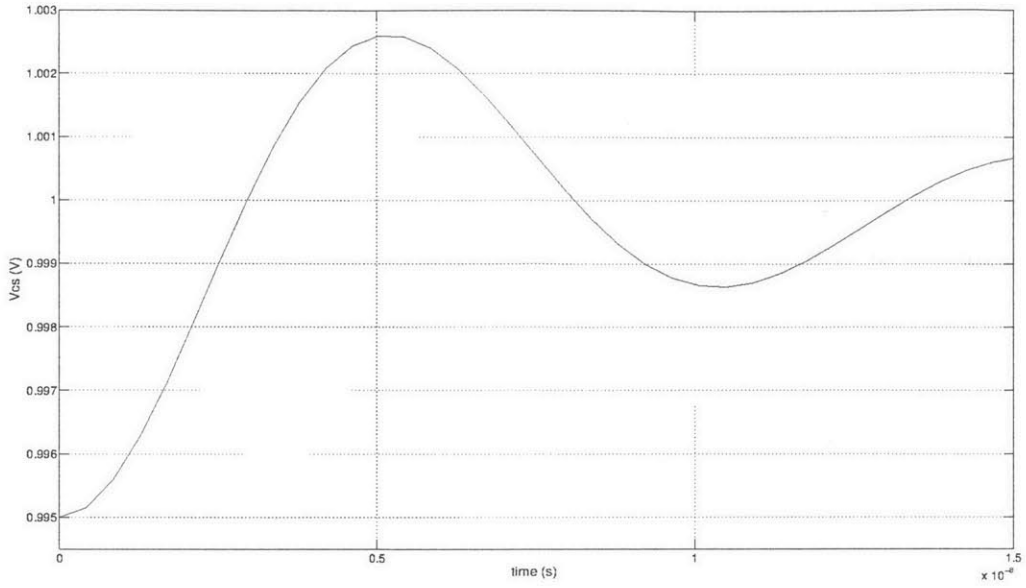


Figure -3: Voltage waveform at $v_{Csample}$ for damping resistor $R = 0.5\Omega$, after the reference switch closes at the beginning of ϕ_2.

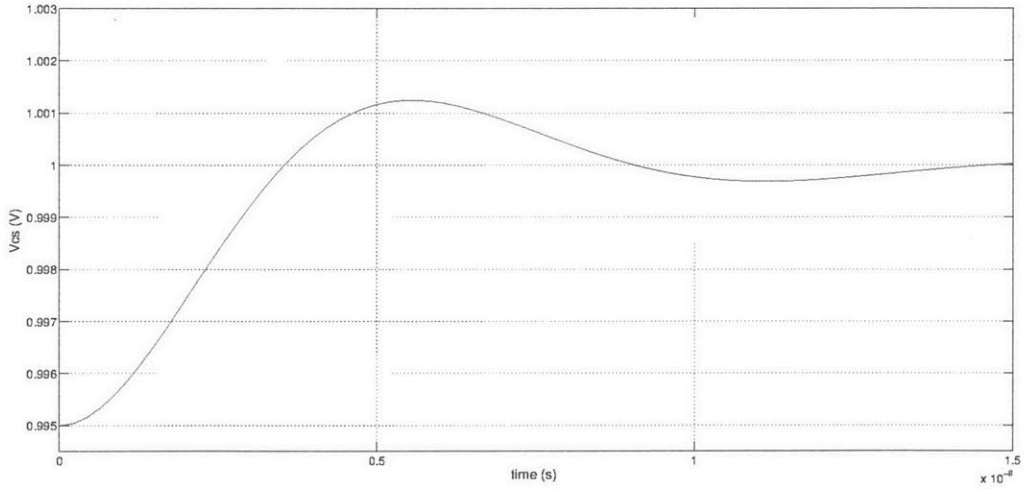


Figure -4: Voltage waveform at $v_{Csample}$ for damping resistor $R = 1\Omega$, after the reference switch closes at the beginning of ϕ_2.

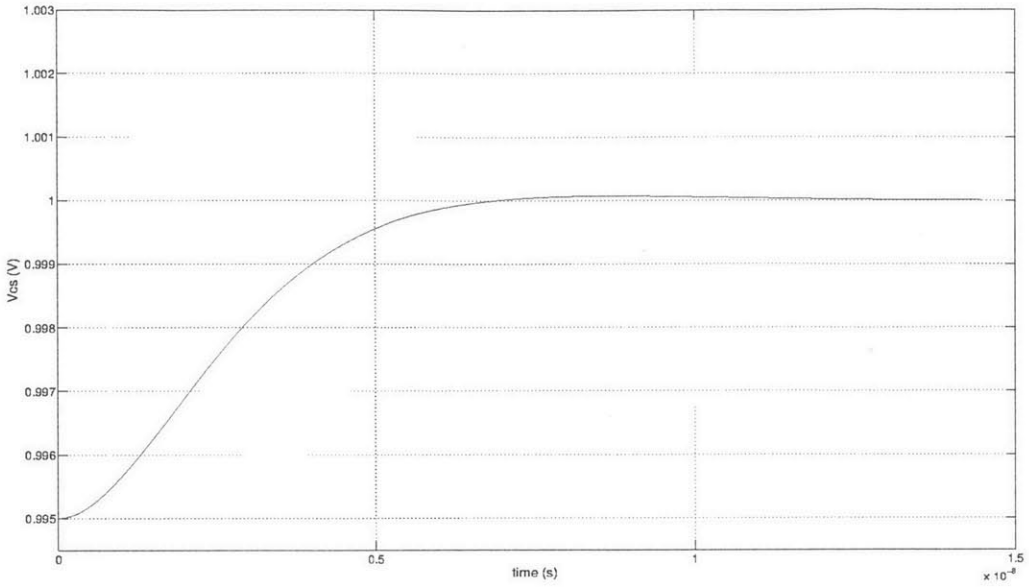


Figure -5: Voltage waveform at $v_{Csample}$ for damping resistor $R = 2\Omega$, after the reference switch closes at the beginning of ϕ_2.