

Vertical Silicon Nanowire Arrays for Gas Sensing

by

Hangbo Zhao

B.Eng., Tsinghua University (2011)

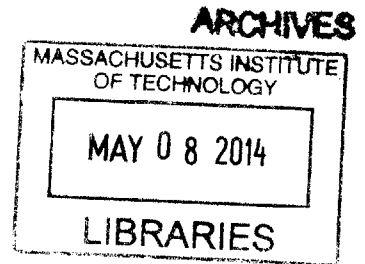
Submitted to the Department of Mechanical Engineering in partial fulfillment of the requirements for the degree of

Master of Science in Mechanical Engineering

at the

Massachusetts Institute of Technology

February 2014



© 2013 Massachusetts Institute of Technology. All rights reserved.

Signature of Author: 

Department of Mechanical Engineering

November 13, 2013

Certified by: 

Carl V. Thompson

Professor of Material Science and Engineering


Thesis Supervisor

Certified by: 

Evelyn Wang

Professor of Mechanical Engineering

Thesis Supervisor

Accepted by: 

David E. Hardt

Department of Mechanical Engineering

Chairman, Committee for Graduate Students

Vertical Silicon Nanowire Arrays for Gas Sensing

by

Hangbo Zhao

Submitted to the Department of Mechanical Engineering
on November 13, 2013, in partial fulfillment of the requirements for the degree of
Master of Science in Mechanical Engineering

Abstract

The goal of this research was to fabricate and characterize vertically aligned silicon nanowire gas sensors. Silicon nanowires are very attractive for gas sensing applications and vertically aligned silicon nanowires are preferred over horizontal nanowires for gas sensing due to the high density of nanowire arrays and the increased nanowire surface area per substrate area. However, the development of such devices has been limited by a number of challenges. Two of the key challenges in fabricating vertical silicon nanowire sensors are the difficulty of making electrical contact to the tops of the wires and the large serial resistance of the substrate.

In this thesis, highly ordered, dense arrays of vertically aligned silicon nanowires in patterned areas have been fabricated utilizing metal assisted chemical etching (MACE) in combination with interference lithography. In addition, we report a novel and simple approach for making reliable top electrical contacts by using tilted electron beam evaporation with a custom-built rotation plate. A suspended metal top contact layer was formed on vertically aligned silicon nanowires using this approach. We have also systematically investigated the contact behavior between silicon nanowires and metal electrodes with different nanowire doping and contact materials. Ohmic contact was formed between the suspended top metal layer and the tips of silicon nanowires. We have also solved the serial resistance problem by using lightly doped epitaxial silicon films (needed for the sensors) on heavily doped substrates. Based on these

techniques and design considerations, we have successfully fabricated vertically aligned silicon nanowire field effect gas sensors.

Finally, we have demonstrated highly sensitive detection of hydrogen, oxygen, 10 ppm (parts-per-million, 10^{-6}) ammonia and nitrogen dioxide gases using the fabricated sensor devices at room temperature. The sensors have exhibited the highest sensitivity per unit chip area for hydrogen, oxygen and 10 ppm NH_3 gases at room temperature, among other vertically aligned silicon nanowire based gas sensors reported. Further improvements of the current sensor devices can be made to accelerate response and recovery of gas sensing.

Thesis Supervisor: Carl V. Thompson

Title: Professor of Materials Science and Engineering

Thesis Supervisor: Evelyn Wang

Title: Professor of Mechanical Engineering

Acknowledgment

First and foremost, I would like to express my deepest gratitude to my research advisor, Prof. Carl V. Thompson in the Department of Material Science and Engineering, for his excellent guidance and tremendous support during the past two years. He has been extremely patient to help me overcome the difficulties starting the research here at MIT. His vision, immense knowledge and constant encouragement have inspired and helped me in all the time of research and writing this thesis.

I would also like to thank my academic advisor, Prof. Evenly Wang in the Department of Mechanical Engineering, for her kindness and valuable suggestions in my research and graduate study. She has always been patient and supportive whenever I have questions and difficulties. I am also thankful for my collaborator, Prof. Harry Tuller and Di Chen, for their great support on facilities and insightful discussions in the past months.

Most of this work was done using the facilities of the Microsystems Technology laboratories (MTL) and Nanostructures Laboratory (NSL) at MIT. I would like to thank the research staffs in MTL and NSL. In particular, I want to thank Kurt Broderick at MTL and James Delay at NSL who have been patiently helped me get experienced in micro and nano fabrication.

The research work in this thesis would not be possible without the help of my colleges. I would like to especially thank Dr. Swee Ching Tan, Wen Zheng and Ahemd Al-Obeidi for their patience, efforts and useful discussions inside the group. I also want to thank Dr. Hang Yu, Robert Mitchell, Alan Gyebyun Kim, Tomas Batcho, Duanhui Li, Daniele Perego and Rachel Zucker and past members of the Materials for Micro and Nano Systems Group. I am honored to work in this group with such wonderful researchers and friends.

Finally, I would like to express my special thanks to my family, especially my parents for their unconditional support over these years. My beloved Zhaozhao, I can find no words to express my gratitude for your love and support.

Table of Contents

Acknowledgment	2
List of Figures	4
List of Tables	8
Chapter 1 Introduction	12
1.1 Motivation and Background.....	12
1.2 Fabrication techniques for silicon nanowires.....	14
1.3 Introduction to silicon nanowire field effect gas sensor	17
1.3.1 Mechanism of silicon nanowire field effect gas sensor.....	17
1.3.2 Effects of device parameters on silicon nanowire field effect gas sensor performance.....	19
1.3.3 Configurations of silicon nanowire field effect sensors	21
Chapter 2 Silicon Nanowire Fabrication by Metal Assisted Chemical Etching (MACE).....	25
2.1 Introduction to MACE	25
2.2 Metal film patterning techniques for MACE	29
2.2.1 Nanosphere lithography	29
2.2.2 Interference lithography.....	34
2.3 Fabrication of wires-in-trench structures using MACE	38
Chapter 3 Silicon Nanowire FET Design and Fabrication	41
3.1 Design overview.....	41
3.2 Structure design.....	41
3.3 Ohmic contacts between silicon nanowire and electrodes	52
3.4 Top electrical contact fabrication.....	59
3.4.1 Overview.....	59
3.4.2 Tilted electron beam evaporation for top contact	62
3.5 Bottom contact and wire bonding	68
3.6 Device electrical characterization	70
Chapter 4 Silicon Nanowire FETs for Gas Sensing.....	71

4.1	Measurement setup.....	71
4.2	Gas sensing results	72
4.2.1	Hydrogen and oxygen detection	73
4.2.2	Ammonia and nitrogen dioxide detection	78
4.2.3	Periodic sensing results	79
4.3	Discussion and conclusion	82
Chapter 5 Summary and Outlook		88
5.1	Summary	88
5.2	Future work	89
List of Reference.....		92

List of Figures

Figure 1.1 Schematic of growth of a silicon nanowire using the vapor-liquid-solid (VLS) approach.	15
Figure 1.2 Schematic of the sensing mechanism of SiNW a p-type field effect gas sensor. The black dots represent the majority hole carriers inside the p-type silicon nanowire. The yellow squares represent metal electrodes connected to the two ends of nanowires. The red and green dots represent reducing and oxidizing gases, respectively.	17
Figure 1.3 (a) Schematic of planar silicon nanowire biosensor. (b) Schematic of three regions of the system: cylindrical silicon nanowire, insulating oxide layer and electrolyte. (c) Sensitivity of silicon nanowire (p-type) as a function of nanowire diameter, length and doping densities [58].	21
Figure 1.4 Planer silicon nanowire FET sensor: (a) schematic of planar silicon nanowire FET sensor fabrication; (b) SEM image of two silicon nanowire FETs [59].	22
Figure 2.1 Schematic of metal assisted chemical etching (MACE). The yellow part represents the noble metal film deposited on the silicon substrate.	26
Figure 2.2 Scheme of processes involved in metal-assisted chemical etching [51].	27
Figure 2.3 Scheme of nanosphere lithography in combination with MACE [70]	30
Figure 2.4 Dip coating process. The device used is a custom-built dip coater.	31
Figure 2.5 SEM image of polystyrene nanosphere monolayer by assembled using dip coating.	32
Figure 2.6 Polystyrene nanosphere diameter as a function of RIE time for the RIE condition: 10 mTorr and 40W.	33
Figure 2.7 SEM images of (a) polystyrene spheres after Au deposition; (b) Au mesh after lift-off.	33
Figure 2.8 SEM image showing silicon nanowires after 6 min wet etching. The silicon nanowire height is about 570 nm.	34
Figure 2.9 Process flow for interference lithography and MACE.	35
Figure 2.10 SEM image of an ARC pillar array after RIE. The period of the ARC pillar array is 400 nm and the diameter of the pillars is about 125 nm.	36

Figure 2.11 Si nanowire array fabricated using interference lithography; period=420 nm, diameter=200 nm and height=2.2 μm	37
Figure 2.12 Process flow for fabricating a wires-in-trench structure using interference lithography and MACE.....	39
Figure 2.13 Scanning electron microscopy (SEM) images showing (a) fabricated Si nanowires with period 410 nm, diameter 300 nm and height 5.25 μm ; (b) wires in patterned trench areas.	40
Figure 3.1 Two electrical contact schemes for vertically aligned Si nanowire FET sensors: (a) top-top contact; (b) top-bottom contact. The red lines represent the current flow paths.....	42
Figure 3.2 Simulation of a square top-top contact structure in COMSOL: (a) Two square top contact pads on the Si substrate; (b) Electrical potential distribution in a square top-top structure with a bias potential of 1 V.....	43
Figure 3.3 <i>I-V</i> curve of a square top-top contact structure shown in Figure 3.2 based on a COMSOL simulation.....	44
Figure 3.4 Simulation of a ring top-top contact structure in COMSOL: (a) one circular and one ring top contact pads on the Si substrate; (b) Electrical potential distribution in a ring top-top structure with a bias potential of 1V.....	45
Figure 3.5 <i>I-V</i> curve of a ring top-top contact structure of Figure 3.4 based on a COMSOL simulation.....	45
Figure 3.6 Simulation of top-bottom contact structure in COMSOL: (a) scheme of one top contact pad with a back contact to the Si wafer; (b) Electrical potential distribution in the top-bottom structure when the bias potential of the top contact is 1V.....	46
Figure 3.7 <i>I-V</i> curve of the top-bottom contact structure between top and bottom contacts in COMSOL simulation.....	47
Figure 3.8 <i>I-V</i> curve between square top and top contacts using epitaxial wafer in COMSOL simulation.....	50
Figure 3.9 <i>I-V</i> curve between ring top and top contacts using epitaxial wafer in COMSOL simulation.....	50
Figure 3.10 <i>I-V</i> curve of top-bottom contact structure using epitaxial wafer in COMSOL simulation.....	51
Figure 3.11 Scheme of the contact material test: (a) scheme of metal deposition through a shadow mask; (b) scheme of contact pads and measurement.....	53

Figure 3.12	<i>I-V</i> measurement results for contacts between two Au pads on (a) p-type (b) n-type lightly doped Si wafers.	54
Figure 3.13	<i>I-V</i> measurement for contact between two Ni pads on p-type lightly doped Si.	56
Figure 3.14	Formation of the different phases of nickel silicide on a (100) Si wafer [78].	57
Figure 3.15	<i>I-V</i> measurement for contact between two Ni pads on p-type lightly doped Si after rapid thermal annealing at 500°C in forming gas for 1 minute.	57
Figure 3.16	<i>I-V</i> measurement for contact between two Cr/Au pads on p-type heavily doped Si. The linear <i>I-V</i> relationship is consistent with the theory that heavily doped Si forms good Ohmic contact with metal.	59
Figure 3.17	Schematic and real images of the fabrication of ZnO NRA sensors [79].	60
Figure 3.18	Schematic of vertical Germanium nanowire fabrication process [80].	62
Figure 3.19	Schematic of tilted electron beam evaporation for making a top contact.	63
Figure 3.20	A custom-built rotating plate for tilted ebeam evaporation.	64
Figure 3.21	SEM micrographs of a 800 nm Au film deposited at an angle of 60° with respect to the sample normal: (a) cross-section of the SiNW array (b) top view of the large top contact area.	65
Figure 3.22	SEM micrographs of an Au film after a two- step ebeam evaporation process: (a) cross-section of SiNW array; (b) top view of the large top contact area.	66
Figure 3.23	SEM micrographs of a Ni film after a two-steps ebeam evaporation process: (a) cross-section of SiNW array; (b) top view of the large top contact area.	68
Figure 3.24	Schematic of the fabricated SiNW field effect sensor.	69
Figure 3.25	Picture of the fabricated sensor device with (a) an LCC chip carrier; (b) a TO Headers chip carrier.	69
Figure 3.26	<i>I-V</i> curve of a fabricated sensor device with Au contact top contact.	70
Figure 4.1	Schematic of gas sensing characterization setup.	71
Figure 4.2	Photos of the gas sensing equipment: (a) sensor device inserted in device holder; (b) plastic tube with sensor device inside; (c) Labview interface for MFC control.	72
Figure 4.3	Electrical response of the SiNW field effect gas sensors to H ₂ gas.	74
Figure 4.4	Normalized resistance change of SiNW field effect sensors for air test and multiple H ₂ gas sensing cycles.	75
Figure 4.5	Electrical response of the SiNW field effect gas sensors to O ₂ gas.	76

Figure 4.6 Normalized resistance change of SiNW field effect sensors for air test and multiple O ₂ gas sensing cycles.	77
Figure 4.7 Comparison of typical electrical response to H ₂ and O ₂ sensing.	78
Figure 4.8 Normalized resistance change to 100 ppm NH ₃ and NO ₂ gases.	79
Figure 4.9 Electrical response to periodic switches of H ₂ gas at room temperature; H ₂ exposure interval = 1 h.	80
Figure 4.10 Electrical response to periodic switches of O ₂ gas at room temperature; O ₂ exposure interval = 1 h.	80
Figure 4.11 Electrical response to periodic switches of NH ₃ gas at room temperature; NH ₃ exposure interval = 1 h.	81
Figure 4.12 Electrical response to periodic switches of NO ₂ gas at room temperature; NO ₂ exposure interval = 1 h.	82
Figure 4.13 Electrical responses of vertical SiNW array-based sensor to periodic switches of (a) oxygen and (b) hydrogen gases at room temperature [40].	83
Figure 4.14 Porous top electrode sensor (black) and solid electrode sensor (red) responses to 500 ppb of NH ₃ at ~30% RH [85].	85
Figure 4.15 Response to ammonia and nitrogen dioxide at various concentrations for an ordered, vertically aligned silicon nanowire-based sensor with a porous electrode [86].	86

List of Tables

Table 3.1 Summary of analytical and simulated substrate resistances for top-top and top-bottom contact structures (assuming the Si wafer resistivity $\rho=10 \text{ } \Omega\cdot\text{cm}$).	48
Table 3.2 Parameters of the epitaxial silicon wafer used for sensor fabrication.....	49
Table 3.3 Comparison of simulated substrate resistances of both top-top contact (square and ring shapes) and top-bottom using uniformly lightly doped Si and epitaxial Si wafers.....	52
Table 3.4 Table of measured values of the Schottky barrier height between different types of semiconductors and metals [76].....	55
Table 4.1 Comparison of sensitivity per unit chip area to H_2 and O_2 between the sensor presented in this thesis and that reported by Han <i>et al.</i>	83
Table 4.2 Comparison of parameters of sensor device presented in this thesis and by Han <i>et al.</i>	84
Table 4.3 Comparison of sensitivity to 10 ppm ammonia and chip size of our fabricated device with that reported by Pehrsson <i>et al.</i>	86
Table 4.4 Comparison of parameters of sensor device presented in this thesis and by Pehrsson <i>et al.</i>	87

Chapter 1 Introduction

1.1 Motivation and Background

Gas sensors are playing an increasingly important role in our lives for a wide range of applications in control of industrial and vehicle emission, detection of toxic or flammable gas leakage, and environmental monitoring [1-3]. There have been many studies of the detection of gases such as O₂, O₃, H₂, N₂, CO, CO₂, SO₂, NO, NO₂, H₂O, etc. [4, 5] Various materials have been explored as sensing elements for gas sensors, including metals, metal oxides, semiconductors, polymers, etc. [6-8] Basically, the electrical or optical properties of these materials will be changed when analyte gases physically absorb or form a chemical bond with the sensing materials. This effect is much more pronounced when the dimension of the materials shrinks to micro- or even nanometers. This is because a larger portion of the materials is on the surface instead of being in the bulk form. This effect has led to considerable investigation of different nanostructures for gas sensors in the past decades [9, 10].

Among all the nanostructures, such as nanoparticles [11-14], nanobelts [6, 15-17], nanorods [18-20] and nanotubes [21-26], nanowires have attracted the most attention for sensing applications [27-30]. A nanowire is basically a one-dimensional nanostructure with its diameter in the range of 1-100 nm. This type of architecture exhibits novel and interesting electrical, mechanical, optical properties that are not significant in the material's bulk form. Nanowire gas sensors can be classified into several categories based on the material used, including metal nanowire sensors [31-33], metal-oxide nanowire sensors [34, 35], conducting polymer nanowire sensors [36, 37], silicon nanowire (SiNW) gas sensors [38-40] and other semiconductor nanowire sensors [41].

Silicon nanowire gas sensors, which have attracted much attention from researchers in recent years, are believed to be promising next generation gas sensors with high sensitivity, selectivity, ultrafast sensing

speed and compatibility with integration with integrated circuits (IC) and manufacture using the tools and manufacturing infrastructure provided by the microelectronics industry. Silicon nanowire gas sensors, compared with other gas sensors of different materials and dimensions, have advantages for gas sensing applications that include:

(a) Large surface-to-volume ratio

Since the diameters of nanowires are in the nanometer range while their lengths are in the micrometer range, the surface-to-volume ratio of high aspect ratio nanowires can be very large compared to materials in the bulk form. This feature enables ultrahigh sensitivity. Due to their small size, a small amount of gas adsorption is sufficient to change the electrical or optical properties of nanowires significantly, such as the carrier distribution inside nanowires, or the refractive index. The nanoscale size of the wires allows gas detection of extremely low concentrations down to parts-per-billion (ppb).

(b) Large scale production and higher integration

Compared to nanowire sensors made from other materials, silicon nanowire sensors are much more attractive in terms of fabrication and integration. Existing complementary metal–oxide–semiconductor (CMOS) fabrication techniques widely used in the industry make mass production of silicon nanowires possible. In addition, nanowires can be integrated with many other functional parts such as devices for signal processing, power supplies and wireless communication devices in a single chip using standard CMOS technology.

(c) Label-free, real-time detection and room temperature operation

Typically nanowire gas sensors do not require labeling as nanowires are usually used as electrical signal transducers. This enables real-time signal readout without expensive and complicated labeling as in many other biosensors. Another great advantage of silicon nanowire sensors is that they can operate at a low

temperature. The temperature of operation is one of the most important parameters for gas sensors. Many thin film metal oxide gas sensors have an elevated operating temperature, even hundreds of degree Celsius [42-44]. Since small amounts of analyte gas can result in measurable electrical or optical signals inside silicon nanowires, silicon nanowire-based gas sensors can be operated at room temperature, which makes them more practical for use in different environments.

(d) Low power consumption and low weight

The dimensions of nanowire-based gas sensors make them extremely power saving. The power needed in an integrated nanowire gas sensor generally involves just electrical (or optical) measurements and signal processing. A single ZnO nanowire gas sensor can operate at extremely low power levels of $\sim 15\text{-}30\ \mu\text{W}$ [45].

With all the advantages given above, silicon nanowire based gas sensors have attracted much attention in the past decades. The semiconducting properties of silicon nanowires make it easy to modulate their electrical properties, which provides a direct sensing readout. In addition, nanowire gas sensors made from silicon can be integrated with CMOS technology, which makes them extremely attractive in terms of manufacturing and applications. Field effect transistors (FETs) are the most common category of nanowire gas sensors. Silicon nanowires are excellent building blocks for field effect transistors (FETs), which exhibit significant conductivity changes when exposed to analyte gases [46]. Silicon nanowire field effect gas sensors will be discussed in more details in section 1.3.

1.2 Fabrication techniques for silicon nanowires

There are numerous SiNW fabrication methods, which are commonly classified into two categories: bottom-up and top-down methods.

The bottom-up method assembles individual atom and molecule to build up a variety of nanostructures. There are a number of bottom-up methods for silicon nanowire fabrication, which include vapor-liquid-solid (VLS) growth, chemical vapor deposition (CVD), etc. Among these approaches, VLS is the most commonly used method for fabrication of silicon nanowires. The VLS approach was first explored by Wagner et al. for crystal growth of silicon whiskers [47]. A schematic of the VLS growth process is shown in **Figure 1.1**. As **Figure 1.1** shows, the metal catalyst absorbs the vapor and forms liquid alloy, which becomes supersaturated. This supersaturation drives the precipitation of the crystal. Because vapor (reaction gases), liquid (catalyst alloy) and solid (precipitated nanowires) phases are involved during this process, it is known as the VLS method. This VLS mechanism was firstly used to grow various types of micro-scale whiskers. Then it was employed to grow 1D nanowire structures from the 1900s by a number of groups and was then widely accepted as a key method for the growth of semiconductor nanowires.

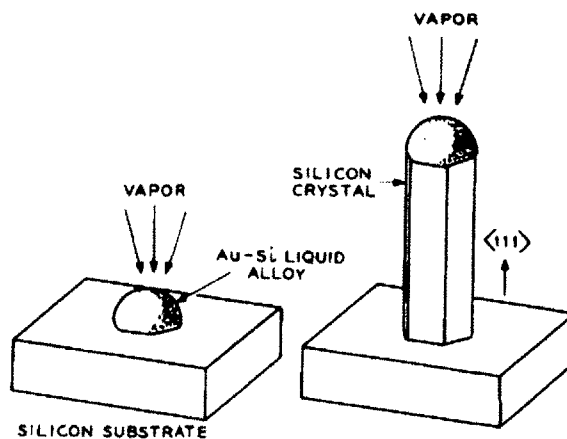


Figure 1.1 Schematic illustration of growth of a silicon crystal using the vapor-liquid-solid (VLS) approach [47].

In a typical VLS silicon nanowire growth process, Au is used as the metal catalyst while SiH₄ is used as the gaseous precursor. The SiH₄ is decomposed and incorporated at the Au surface, forming an Au-Si eutectic alloy. The silicon nanowire grows from this alloy due to the supersaturation and nucleation of crystal silicon. As the dominant fabrication technique for silicon nanowires, VLS method has several advantages. First, it can be used to generate nanowires on any type of surface, such as silicon or silicon-on-insulator (SOI) wafers, making it very attractive for various applications. Another advantage is that the VLS method can be used to grow nanowires with dimensions ranging from sub-nanometers to hundreds of nanometers [48, 49]. However, there are also distinct disadvantages of the VLS growth method. First, the VLS process takes place at a high temperature (typically a few hundred degrees Celsius). Second, the unintended metal contamination from the catalyst in silicon nanowires is often difficult to avoid. In addition, the growth direction of epitaxial silicon nanowires is diameter-dependent. For silicon nanowires grown epitaxially on (100) silicon by the VLS method, the growth direction is <111> for a diameter small than 20 nm and <110> for a larger diameter [50]. Therefore VLS method cannot be used to grow silicon nanowires normal to the (100) silicon substrate. Similarly, the epitaxial growth of silicon nanowires normal to (110) substrates has not been accomplished without the use of templates [51]. This growth direction limitation hinders the applications of VLS method in fabricating nanowires for functional devices.

Compared to bottom-up approaches, top-down approaches are more standard techniques for semiconductor manufacturing. Typical top-down approaches involve deposition, patterning and etching processes to reduce the lateral dimensions to the nanoscale. Common top-down approaches include the use of electron-beam lithography (EBL), nanoimprint lithography, scanning probe lithography, interference lithography and focused-ion-beam (FIB) lithography, etc. Nanoscale patterns are created by the use of photons, electrons or ions and then the bulk material is etched away with patterned masks by

either wet or dry etching. The key advantage of top-down approaches is that it is easy to fabricate large scale well-ordered arrays of nanowires with high uniformity. In addition, the top-down approach is lithography based so it is compatible with standard IC manufacturing technology. The shortcomings of top-down approaches include low throughput and difficulty in achieving small sizes.

1.3 Introduction to silicon nanowire field effect gas sensor

1.3.1 Mechanism of silicon nanowire field effect gas sensor

The sensing mechanism of silicon nanowire field effect gas sensors is shown in **Figure 1.2**.

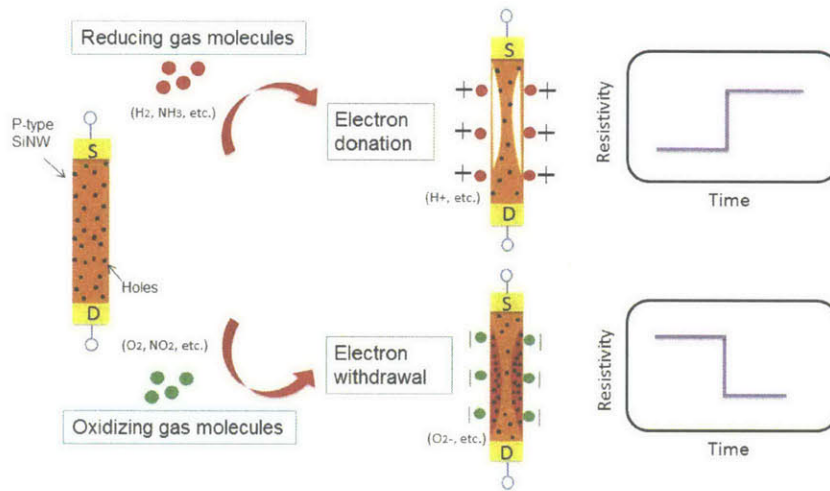


Figure 1.2 Schematic of the sensing mechanism of a SiNW p-type field effect gas sensor. The black dots represent the majority hole carriers inside the p-type silicon nanowire. The yellow squares represent metal electrodes connected to the two ends of nanowires. The red and green dots represent reducing and oxidizing gases, respectively.

The basic idea is that a silicon nanowire can be configured as a Field Effect Transistor (FET) so that its resistivity can be modulated by the surface charge associated with the gas adsorption and desorption processes. SiNWs serve as the conductive channel for carriers and the two ends of the SiNWs are

connected to source and drain contacts. Then the electrical field induced by the gas adsorption and desorption processes occurring at the SiNW surfaces act as the gate. The principle of gas sensing by SiNWs is believed to be the result of electron transfer between SiNWs and the target gas, with accumulation or depletion of carriers inside SiNWs [52, 53]. For a p-type doped SiNW as shown in **Figure 1.2**, when reducing gas molecules (H_2 , NH_3 , etc.) are absorbed on the SiNW surface, the electron donating properties of those gas molecules deplete the majority hole carriers (h^+) in the SiNW, leading to an increase of the SiNW resistivity. In contrast, when oxidizing gas molecules such as O_2 , NO_2 are absorbed on the SiNW surfaces, their electron withdrawing property causes accumulation of the hole carriers inside the SiNW, leading to a decrease of the SiNW resistivity. Although this general sensing principle is commonly accepted, details about how the gas molecules communicate with the SiNWs with the existence of the silicon dioxide (SiO_2) layer at room temperature remains to be investigated. Joshi and Kumar proposed that the sensing phenomenon of SiNWs may occur via the passivation of dangling bonds or incomplete covalent bonds, or the available fast surface states at the Si/ SiO_2 surface by the target gases [54]. In their proposed sensing mechanism, the target gas molecules can donate or withdraw electrons due to the very high reactivity of the incomplete bonds or surface states at the silicon dioxide surface.

The conductivity of a SiNW is

$$G = \frac{n e \mu \pi D^2}{4L} . \quad (1.1)$$

where n is the initial carrier concentration, μ is the mobility of the electrons, D and L are the diameter and length of the nanowire channel, respectively. When analyte gases are absorbed onto the SiNW surface, the induced change of conductivity is [35, 55]:

$$\Delta G = \frac{\Delta n e \mu \pi D^2}{4L} . \quad (1.2)$$

where Δn is the average carrier concentration inside the wire. This equation means the gas sensing process changes the carrier concentration. The modifications of the electrical transport by absorbed gases can be qualitatively explained by a nonequilibrium Green's function [56, 57]. In this way, by monitoring the resistance change of the SiNW arrays, the concentration of specific gas molecules can be detected.

1.3.2 Effects of device parameters on silicon nanowire field effect gas sensor performance

The performance of a sensor is characterized in terms of its sensitivity, speed, selectivity and stability, which are known as “4s”. Sensitivity corresponds to the relative property changes in sensors. In the case of field effect sensors specifically, sensitivity means the change of conductivity. Speed is the characterization of the time needed by the sensor to produce a reliable signal during the sensing process. Selectivity corresponds to the ability to distinguish particular target analytes among other molecules. Stability is the ability to produce a stable signal for a considerable period of working time.

For silicon nanowire gas sensors, sensitivity and sensing speed are the two most critical characteristics. While selectivity and stability are also important, they are more determined by the functionalization of sensor devices, such as the surface treatment. The sensing speed of a silicon nanowire field effect sensor depends on the configuration of the sensor device, the gas adsorption and desorption path, surface modifications and so on. As the most important characteristic, the sensitivity of the sensor is strongly affected by the device parameters apart from the surface modifications, including the nanowire diameter, length, density, doping level and sensor configurations.

The sensitivity of a silicon nanowire sensor is defined as the relative conductance change:

$$S = \frac{\Delta G}{G} . \quad (1.3)$$

A simple approximation can be made to evaluate the effects of device parameters on sensitivity [58]. As illustrated in **Figure 1.2**, exposure to analyte gas molecules leads to carrier accumulation or depletion in the silicon nanowires. Assume that the surface charge density σ induced by the carrier accumulation or depletion is constant, the amount of charge induced per unit length is given by

$$\Delta Q = \pi\sigma D. \quad (1.4)$$

The change in conductance is then given by

$$\Delta G = \frac{\pi D \mu \sigma}{L}. \quad (1.5)$$

So the sensitivity is

$$S = \frac{4\sigma}{eDn}. \quad (1.6)$$

Equation (1.6) suggests that silicon nanowires with small diameters and low doping levels will exhibit higher sensitivity. This conclusion drawn from the approximation is a useful guide for silicon nanowire field effect sensor design.

More explicit theoretical models can be built to quantitatively evaluate the sensitivity of silicon nanowire field effect sensors. Nair and Alam modeled planar silicon nanowire biosensors in fluid environments and evaluated the sensitivity as a function of nanowire diameter, length and doping level [58]. The simulation result is shown in **Figure 1.3**.

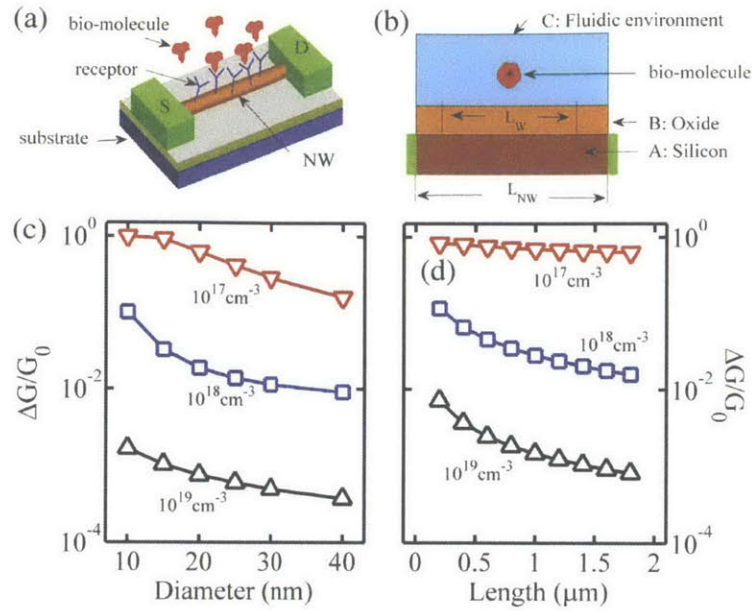


Figure 1.3 (a) Schematic of a planar silicon nanowire biosensor. (b) Schematic of three regions of the system: cylindrical silicon nanowire, insulating oxide layer and electrolyte. (c) Sensitivity of silicon nanowire (p-type) as a function of nanowire diameter, length and doping densities [58].

Note here that L_w represents the length affected by a single target biomolecule attachment, not the nanowire length. **Figure 1.3 (c)** shows that the sensitivity increases with smaller nanowire diameter and lower doping density, which is consistent with the approximation results in Equation (1.6).

1.3.3 Configurations of silicon nanowire field effect sensors

Based on the sensing mechanism described in section 1.2.1, several strategies have been developed for the fabrication of silicon nanowire FET gas sensors. The configurations can be classified into two major categories: planar and vertical.

(a) Planar silicon nanowire FET sensor

Most of the silicon nanowire FET sensors developed have planar configurations. A schematic of this configuration is shown in **Figure 1.4 (a)**.

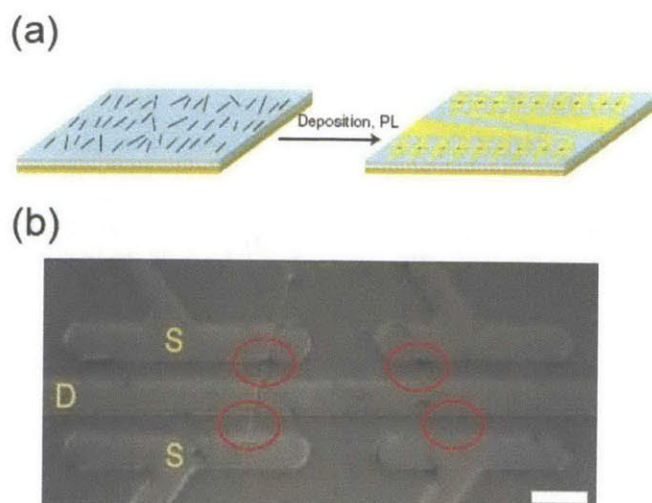


Figure 1.4 Planer silicon nanowire FET sensor: (a) schematic of planar silicon nanowire FET sensor fabrication; (b) SEM image of two silicon nanowire FETs [59].

In the planar configuration, silicon nanowires lie horizontally on a substrate with their two ends connected to metal electrodes. Typical fabrication processes for planar sensors involve lithographical patterning of contact pads on a silicon substrate, silicon nanowire growth and deposition on the substrate, photolithography writing of source and drain electrodes. A part of a fabricated sensor array is shown in **Figure 1.4 (b)** where an individual silicon nanowire crosses the source and drain electrodes. The major drawback of this planar configuration is the alignment of the silicon nanowires and electrodes. The silicon nanowires are usually removed from the substrate where they are generated by a sonication process. Subsequently, they are deposited onto another substrate with electrodes. A major challenge of this configuration is the alignment of silicon nanowires and electrodes. When the silicon nanowires are deposited onto the substrate, the random orientation of the silicon nanowires makes it difficult to connect nanowires to electrodes efficiently. Although various techniques have been used to align the nanowires,

such as assembly by electrostatic interaction [60] and dip-coating [61], it remains challenging to align the nanowires well so that each individual nanowire can be connected to the metal electrodes.

(b) Vertical silicon nanowire FET sensor

Compared to the planar configuration, vertically aligned silicon nanowire sensors are preferred for sensing applications for the following reasons:

- The surface area of the nanowires exposed to the analyte is increased

In this concept, instead of arranging the nanowires flat on the substrate the nanowires are oriented normal to the substrate surface, like tiny columns. In this way almost all the surface area of the nanowires is exposed to the environment for sensing.

- Much denser nanowire arrays can be made to maximize the sensing area per device

In the planar case, a typical nanowire density on the substrate is approximately 1-2 NWs/100 μm^2 [59] while the density of vertically aligned nanowires is $1 \text{ NW}/p^2 \mu\text{m}^2$, where p is the period of the nanowire array. For $p=300 \text{ nm}$, the density is $1 \text{ NW}/0.09 \mu\text{m}^2$, which is about three orders of magnitude higher than the planar case. Therefore the total sensing area per unit area of substrate is maximized in the vertical configuration. This can be further increased without adding additional footprint by fabricating longer nanowires.

For these reasons, a vertical array of highly ordered nanowires is suited for sensing applications. However, the main challenge in fabricating sensors based on large arrays of vertically aligned nanowires is the construction of the electrical contact at the top of nanowire arrays. Direct deposition of metal onto the nanowire array will connect the two ends of a nanowire and cause a short-circuit.

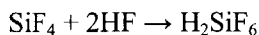
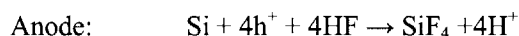
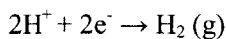
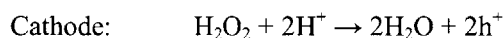
To address this problem, a number of approaches have been tried over the past decade. The most commonly used approach involves metal deposition on partially exposed nanowire tips embedded in a polymeric sacrificial layer [62, 63]. The sacrificial matrix prevents the metal from reaching the lower part of the nanowires and the substrate. However, this approach has limitations such as the nonuniformity of the polymer coating, nanowire surface contamination, etc. In this research, a novel tilted electron beam evaporation method was employed to make reliable top contacts, which overcomes this issue in the vertical nanowire sensor fabrication.

Chapter 2 Silicon Nanowire Fabrication by Metal Assisted Chemical Etching (MACE)

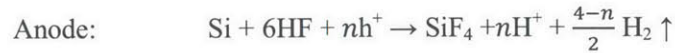
2.1 Introduction to MACE

Among all the fabrication approaches for silicon nanowires, including the top down and bottom up methods introduced in section 1.3, metal assisted chemical etching (MACE) stands out and it has attracted great attention in the last decade.

MACE was first reported in stain etching of porous Si covered with aluminum in an etching solution composed of HF, HNO₃ and H₂O in 1997 [64]. It was found that the incubation time was significantly reduced due to the presence of the aluminum metal film on top of the Si substrate. Dimova-Malinovska later demonstrated that the decreased incubation time was a consequence of the catalytic feature of the aluminum film that boosted the reduction of HNO₃ [65]. The mechanism of MACE was further investigated and explained by Li and Bohn *et al.* by etching a Si substrate with a thin layer of noble metal sputtered on it in an etching solution of HF, H₂O₂ and EtOH [66]. A reaction scheme was proposed that is described by the following reaction equations:



Since then, several models have been proposed to quantitatively explain the reactions involved in MACE. A more commonly accepted model was proposed by Chartier et al. that the amount of hydrogen generated is a function of the ratio of H_2O_2 to HF in the etching solution [67]. The proposed anode and overall reactions are:



In general, a schematic of the use of the MACE process to make nanowires is shown in **Figure 2.1**:

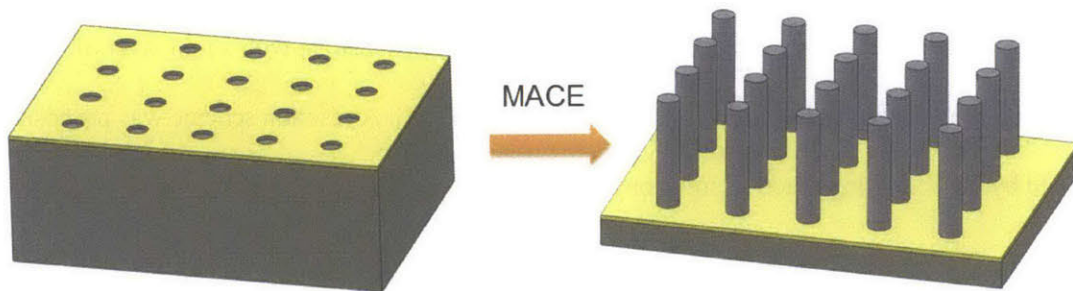


Figure 2.1 Schematic of metal assisted chemical etching (MACE). The yellow part represents the noble metal film deposited on the silicon substrate.

A silicon substrate is partially covered by a film of noble metal (e.g. Au, Pt, Ag) and it is put in an etchant solution composed of HF and an oxidant (e.g. H_2O_2 , HNO_3). The noble metal acts as a cathode to catalyze the reduction of the oxidant, producing a lot of holes. These holes are then injected into the valence band

of the silicon substrate due to a higher electrochemical potential of oxidants. These injected holes oxidize the silicon which is immediately etched away by HF in the solution. Therefore the silicon area with noble metal on top of it is etched much faster than the silicon without noble metal coverage. This different etch rate results in the sinking of the noble metal, leaving behind a highly ordered array of nanowire structures.

The processes involved in MACE are suggested by Huang and Gösele et al. shown in **Figure 2.2**:

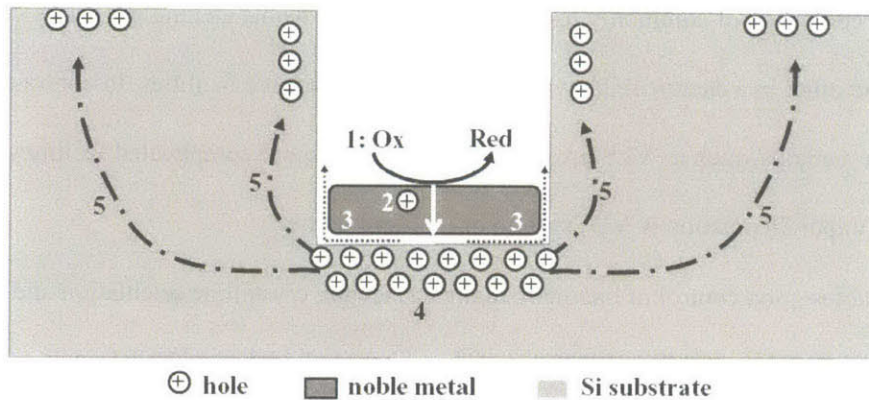


Figure 2.2 Scheme of processes involved in metal-assisted chemical etching [51].

Process 1: The oxidant in the solution is preferentially reduced with the existence of noble metal as catalysts, generating holes;

Process 2: The generated holes diffuse through the noble metal and reach the metal-silicon interface;

Process 3: The Si underneath the noble metal is oxidized by the injected holes and then immediately etched away by the HF, forming H_2SiF_6 ;

Process 4: There is high concentration of holes at the metal-silicon interface. As a result, the silicon in contact with the noble metal is etched much faster than the silicon without noble metal coverage;

Process 5: When the ratio of oxidant to HF is large, the generation rate of holes is greater than the rate of consumption of holes. Therefore there are net holes diffusing from the metal-silicon interface to the

silicon where there is no metal on it. The result of this net hole diffusion is that silicon left behind might be porous due to the hole injection.

Compared to other silicon nanowire fabrication methods, MACE is gaining increasing interest for many reasons, including the following:

- MACE is a simple and economical method for controllable fabrication of Si nanowires. The etching solution is composed of commonly used chemicals and the whole etching process is conducted at room temperature in a chemical lab without use of any expensive facilities. In contrast, many other fabrication methods, such as VLS growth or dry etching require complicated facilities such as a Chemical Vapor Deposition (CVD) system or a plasma etcher.
- MACE enables good control of nanowire diameter, length, crystalline orientation and doping. The geometry of the fabricated Si nanowires can be well controlled during the fabrication process. Since the cross-section of the resulting Si nanowires is determined by the noble film, it can be precisely controlled by various metal film patterning techniques, which will be discussed in detail later. The height of the Si nanowires can be controlled by the etching time.
- As for material characteristics of the Si nanowires, such as crystalline orientation and doping concentration, they are essentially the same as the Si substrate. However, in VLS growth method, the crystalline orientation of silicon nanowires is dependent on the nanowire diameter [50].
- MACE enables fabrication of silicon nanowires normal to the substrate. As previously discussed, the growth direction of silicon nanowires epitaxially grown on (100) substrate by VLS method is not normal to the substrate. In contrast, the etching direction of (100) silicon substrate is $\langle 100 \rangle$ using MACE. It has also been demonstrated that epitaxial [110] silicon nanowires can be fabricated on (110) substrate using MACE by suppressing the crystallographically preferred $\langle 100 \rangle$ etching direction [68].

- The quality of the lightly doped Si nanowires fabricated by MACE is very high. MACE can be used to produce anisotropic high-aspect-ratio lightly doped Si nanowires without incurring lattice damage. In comparison, dry etching methods such as Deep Reactive Ion Etching (DRIE) leads to scalloped and sloped surfaces and also induces defects to the etched Si nanowire surfaces [69].

2.2 Metal film patterning techniques for MACE

As described in section 2.1, the cross-section of the etched Si nanowires is a replica of the shape of the holes in noble metal films on the Si substrate. Therefore, in order to control the shape, diameter, periodicity or density of the fabricated Si nanowires, metal film patterning techniques are used in combination with MACE to fabricate high-aspect-ratio Si nanowires. Several approaches have been developed for this template-based MACE, including a nanosphere lithography method [70, 71], a block copolymer lithography method [72], an AAO mask method [73], an interference lithography method [74]. Among these metal film patterning techniques, nanosphere lithography and interference lithography methods were investigated and used for fabricating Si nanowires in this thesis research, as presented in the following sections.

2.2.1 Nanosphere lithography

Nanosphere lithography starts from self-assembly of a monolayer of nanospheres made from polystyrene or silica, followed by a reactive ion etching (RIE) process to reduce the size of the nanospheres. After the RIE process, the nanospheres shrink and become the mask for subsequent noble metal (gold or silver) film deposition and lift-off. The as-deposited metal film works as the catalytic mask for the MACE process. The scheme of this method is depicted in **Figure 2.3**.

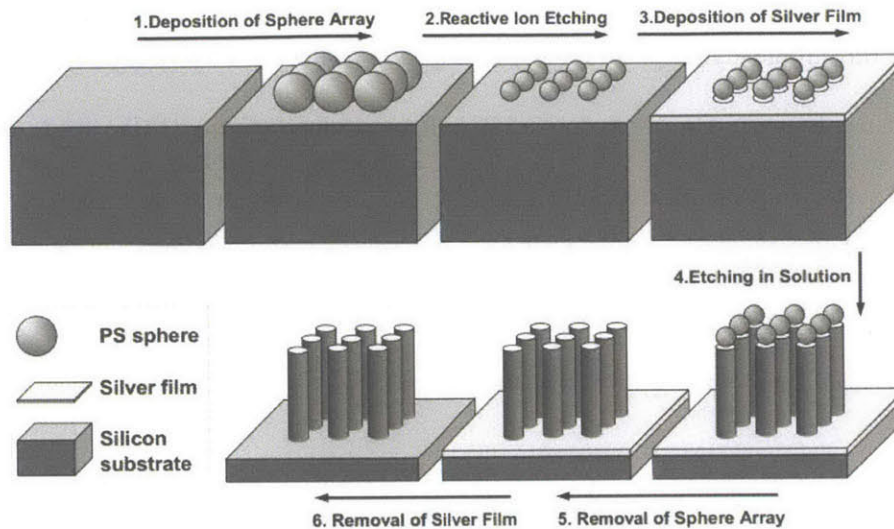


Figure 2.3 Scheme of nanosphere lithography in combination with MACE [70].

Therefore, the period and diameter are determined by the initial diameter of the nanospheres and the remaining size of the nanospheres after reactive ion etching.

The detailed procedure for the nanosphere lithography method used in this thesis research is outlined below:

- I. A Si substrate was cleaned in a piranha solution composed of $\text{H}_2\text{SO}_4 : \text{H}_2\text{O}_2 = 3:1$ for 15 minutes to grow a thin layer of silicon dioxide. The purpose of this step is to make the Si surface hydrophilic for subsequent nanosphere coating.
- II. A dip coating method was used to coat a monolayer of polystyrene spheres using a dip coater built by Shih-wei Chang for her PhD thesis research [75].



Figure 2.4 Dip coating process. The device used is a custom-built dip coater.

A polystyrene colloidal solution (Fisher Scientific, 10 wt%, sphere size 500 nm) was diluted in deionized (DI) water to 1.2 wt%. The piranha cleaned Si substrate was then clipped by a sample holder and inserted into the diluted polystyrene colloidal solution. The sample was pulled up with the stage actuated by a piezoelectric motor at a withdrawal rate of 1 $\mu\text{m/s}$, leaving a monolayer of polystyrene spheres on the Si substrate surface. A closely packed polystyrene nanosphere monolayer can be seen in the scanning electron microscope (SEM) micrographs in **Figure 2.5**.

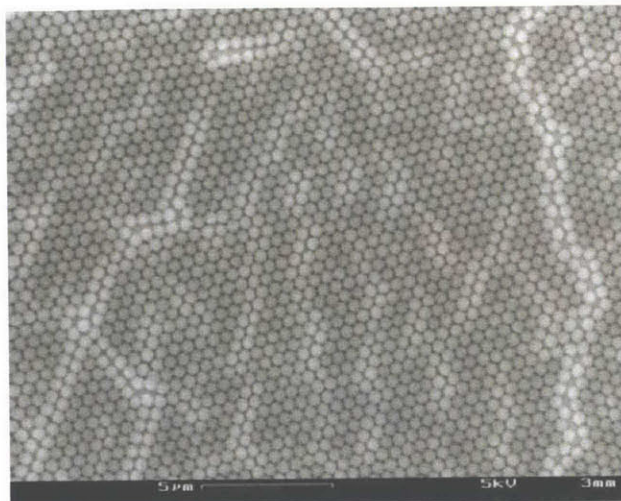


Figure 2.5 SEM image of polystyrene nanosphere monolayer assembled using dip coating.

- III. A dry etching process was needed to reduce the diameter of the nanospheres. For polystyrene, oxygen reactive ion etching (RIE) was used. The pressure and power of oxygen plasma used was 10 mTorr and 40W, respectively. The remaining diameter of the PS nanospheres with respect to time is plotted in **Figure 2.6**. The etch rate was approximately 40 nm/min.

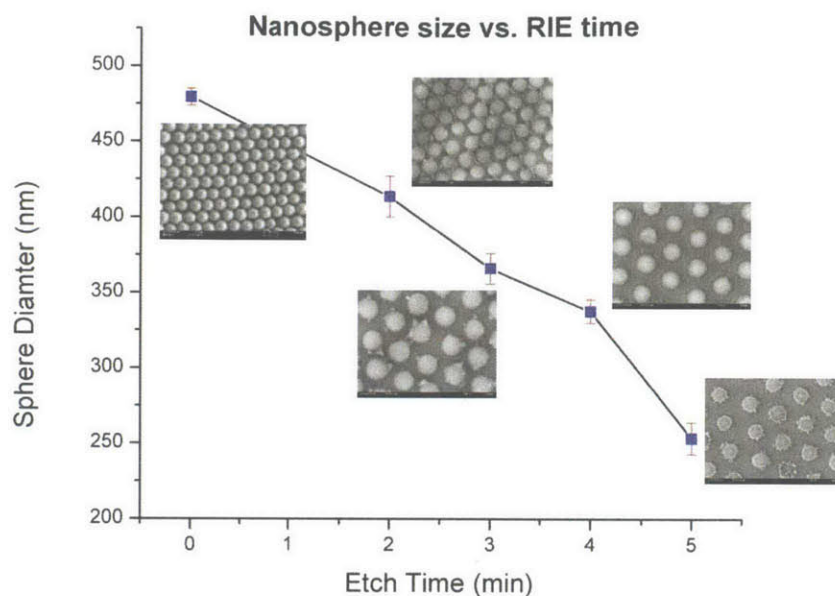


Figure 2.6 Polystyrene nanosphere diameter as a function of RIE time for the RIE condition: 10 mTorr and 40W.

IV. After dry etching of the nanospheres, a 15 nm thick Au film was deposited on the sample using an electron beam evaporator. A lift-off process was performed by sonicating the sample in toluene for 3 min, forming a porous Au mesh on the Si substrate. SEM images before and after the lift-off process are shown in **Figure 2.7**.

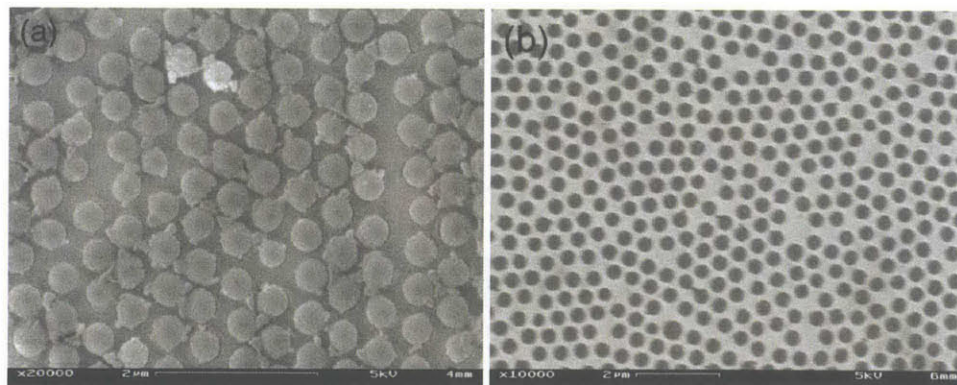


Figure 2.7 SEM images of (a) polystyrene spheres after Au deposition; (b) Au mesh after lift-off.

- V. The samples were then put in an etching solution composed of HF, H₂O₂ and H₂O (6:1:36) at room temperature. The height of the etched Si nanowires was a function of the etch time, which will be described in later sections. For an etch time of 6 minutes, the resulting height was approximately 570 nm.

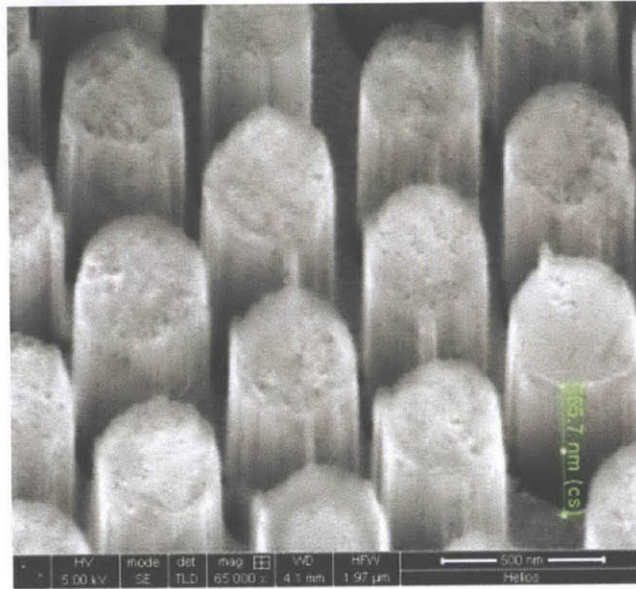


Figure 2.8 SEM image showing silicon nanowires after 6 min wet etching. The silicon nanowire height is about 570 nm.

2.2.2 Interference lithography

Compared with nanosphere lithography, interference lithography allows better control of the diameter, period, and ordering of Si nanowires. The basic process flow is shown in **Figure 2.9**.

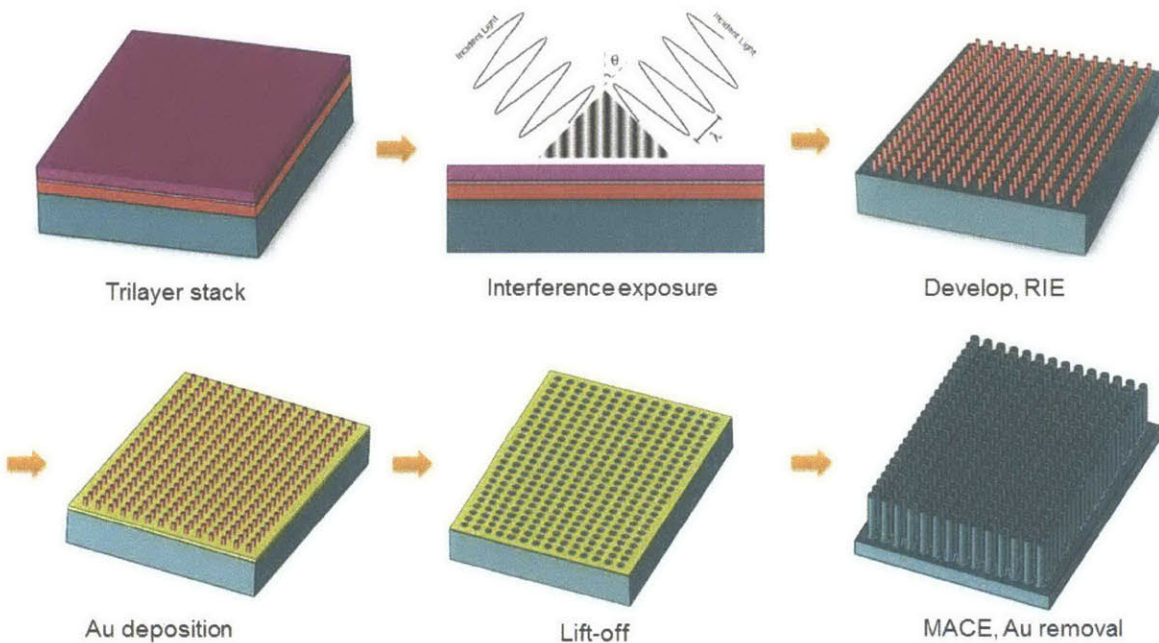


Figure 2.9 Process flow for interference lithography and MACE.

The detailed procedure for use of the interference lithography method is listed below:

- I. The interference lithography process starts from making a trilayer stack on <100> lightly doped p-type Si wafers. First, a 220 nm thick BarLi anti-reflection coating (ARC) is spin-coated on the Si substrate with a spin speed of 4600 RPM for 60s. The sample is then baked at 175°C for 90 seconds. Then a 20 nm thick SiO₂ interlayer is deposited by electron beam evaporation as the second layer. The purpose of this interlayer is to facilitate pattern transfer from photoresist to the ARC layer so that good sidewalls can be obtained in subsequent metal film deposition and lift-off processes. The top layer is coated by spin coating of 200 nm photoresist PFI-88 (Sumitomo Chemical Co.) with a spin speed of 3750 RPM for 60s, followed by a pre-exposure bake at 90°C for 90s.

II. The trilayer stack on the Si wafer is then exposed with a HeCd laser ($\lambda = 325$ nm) using a Lloyd's mirror. By performing two perpendicular laser exposures, periodic post patterns are recorded in the photoresist PFI-88 due to the standing wave properties in the Lloyd's mirror setup. The period and diameter of the post arrays are determined by the half angle between the mirror and substrate in the Lloyd's mirror setup and the exposure dose, respectively. The period is described by the following equation:

$$P = \frac{\lambda}{2\sin\theta} \quad (2.1)$$

Where $\lambda = 325$ nm in our case, θ is the half angle at which the incident light and the reflected light meet. For a post array with $P = 325$ nm and diameter 200 nm, $\theta = 23^\circ 58'$ and the exposure time is 3min 22s for a laser power of 0.17 μ W.

III. After exposure, the sample is immersed in CD-26 developer (Shipley Micropost [®]) for 60 s to remove the unexposed PFI-88 photoresist, so the post array pattern is formed in the top PFI-88 layer after development as shown in **Figure 2.10**.

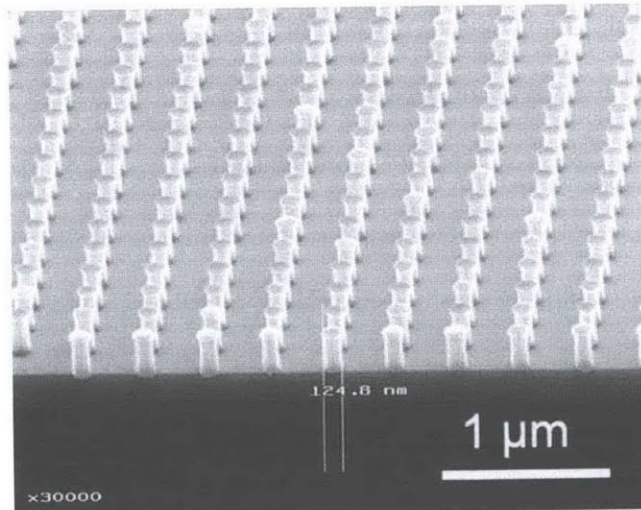


Figure 2.10 SEM image of an ARC pillar array after RIE. The period of the ARC pillar array is 400 nm and the diameter of the pillars is about 125 nm.

- IV. A reactive ion etching (RIE) process is performed to transfer the post array pattern to the underlying ARC layer. First, a CF₄ plasma (of power 150 W, pressure 10 mTorr) is used to etch the SiO₂ interlayer away for 2 minutes with the top photoresist functioning as an etch mask. Subsequently, a He and O₂ plasma (of power 300 W, pressure 10 mTorr) are used to etch the ARC layer for 1 minute. The remaining PFI-88 is also stripped by the oxygen plasma. After this RIE process, an ARC post array is obtained on the Si substrate.
- V. A gold layer of 15 nm thickness is deposited onto the sample using electron beam evaporation. The lift-off process is performed by soaking and sonicating the samples in N-Methyl-2-pyrrolidone (NMP) at 85°C for 5 min and 2 min, respectively. The samples are then etched in a solution of HF, H₂O₂ and H₂O (6:1:36) at room temperature. The fabricated Si nanowires in the SEM micrograph in **Figure 2.11** are the result of 20 minutes' etching. After etching, the Au film can be removed by immersing the sample in Au etchant for 10 s.

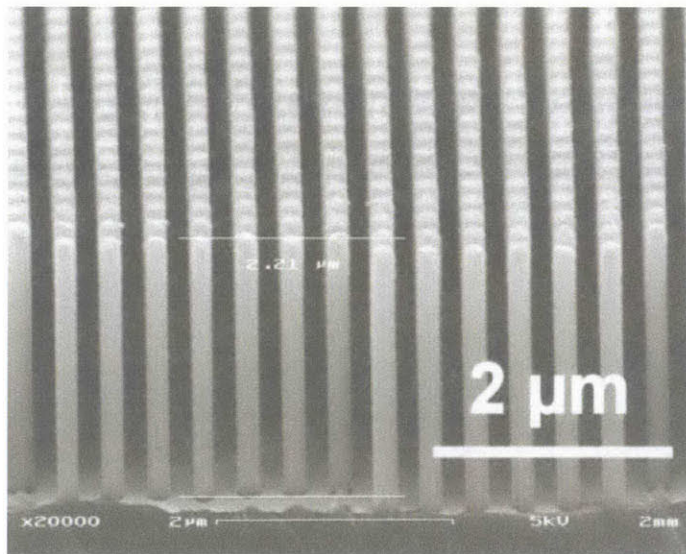


Figure 2.11 Si nanowire array fabricated using interference lithography; period=420 nm, diameter=200 nm and height=2.2 μm.

2.3 Fabrication of wires-in-trench structures using MACE

As shown in section 2.2, metal assisted chemical etching in combination with nanosphere lithography or interference lithography enables fabrication of an ordered array of Si nanowires. Comparing these two methods, nanosphere lithography provides much less control of the geometry of the Si nanowire arrays.

First, the period of the Si nanowire array is determined only by the initial diameter of the polystyrene spheres, which cannot be changed once the colloidal solution is purchased. Second, the diameter of the fabricated nanowires is determined by the RIE process, which serves the purpose of reducing the nanosphere diameters. As the diameter of the polystyrene spheres shrinks to less than 250 nm, the periphery of the spheres becomes rough (as shown in the inset of **Figure 2.6**), making the cross section of the resulting Si nanowires not circular.

Another important aspect is the ability to fabricate Si nanowire arrays in well patterned positions. This is critical since the structure of Si nanowires in patterned trenches must be controlled for array-type devices, such as chemical sensors.

A process for making a wires-in-trench structure has been developed in the research group using interference lithography with MACE. The process flow is shown in **Figure 2.12**.

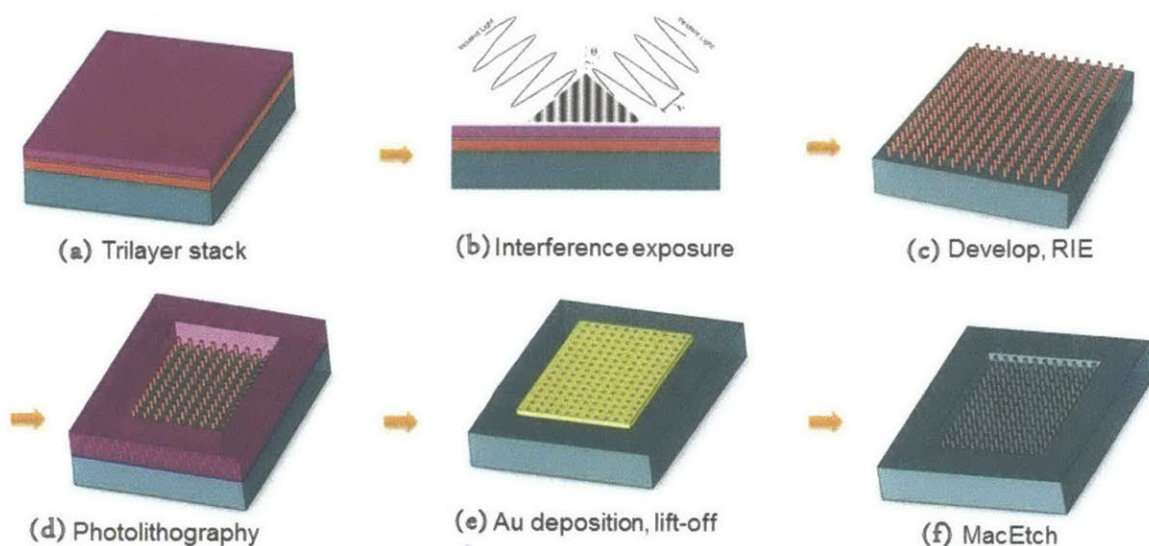


Figure 2.12 Process flow for fabricating a wires-in-trench structure using interference lithography and MACE.

The first several steps for making ARC post arrays is the same as described in section 2.2.2. After an ARC nanopillar array is obtained (**Figure 12 (c)**), photolithography is employed to pattern the trench area.

The detailed procedure is listed below.

- I. Bake the ARC pillar array sample at 150°C for 5 minutes for dehydration;
- II. Spin coat a negative photoresist NR9-3000 PY (Futurrex, Inc.) at a spin speed of 700 RPM for 5s and then raise to 3000 RPM for 55s. Perform a pre-exposure bake at 150°C for 1 minute.
- III. Expose the sample through a mask with square patterns (5 mm x 5 mm) in a mask aligner MA4. The exposure time was 15 s for a UV light power of 9-10 mW/cm².
- IV. Perform a post-exposure bake (hard bake) at 100°C for 1 minute.
- V. Immerse the sample in developer RD6 (Futurrex, Inc.) for 20 s and dry with a nitrogen gun.

After exposure and development, we obtained an ARC nanopillar array with patterned photoresist NR9-PY3000 on top of the ARC pillars (**Figure 12 (d)**). Subsequently, a 15 nm Au film was deposited on the sample using electron beam evaporation. The subsequent lift-off and etching processes were the same as described in section 2.2.2. Note that after lift-off, a patterned Au mesh was obtained in a position defined by the mask during the photolithography step (**Figure 12(e)**). After the wet etch step, a Si nanowire array was fabricated in the defined trench area. SEM images of fabricated wires-in-trench structures are shown in **Figure 2.13**.

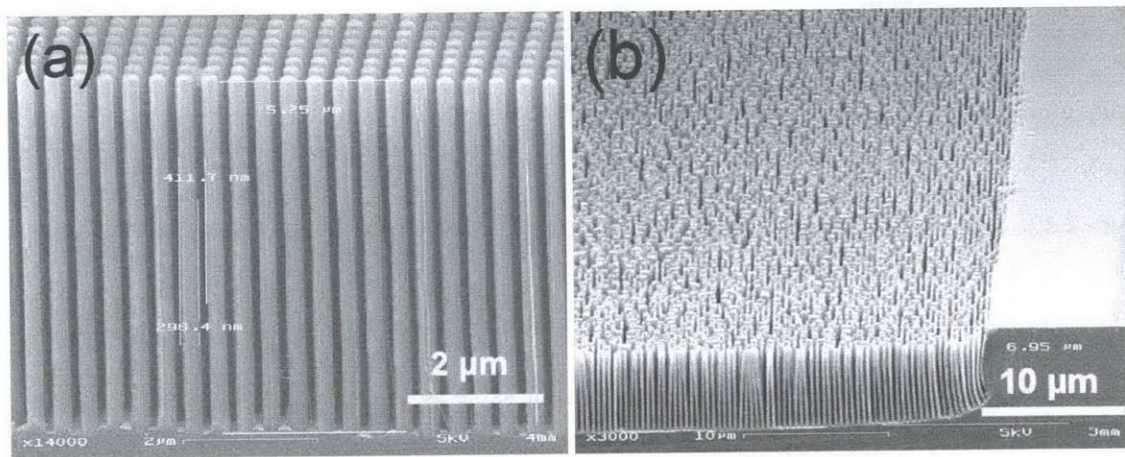


Figure 2.13 Scanning electron microscopy (SEM) images showing (a) fabricated Si nanowires with period 410 nm, diameter 300 nm and height 5.25 μm ; (b) wires in patterned trench.

As we can see from **Figure 2.13**, Si nanowires with aspect ratios of 18 were fabricated in a patterned trench area. With this capability, array-based devices can be made with a single silicon substrate, such as multiple trenches with Si nanowires inside.

Chapter 3 Silicon Nanowire FET Design and Fabrication

3.1 Design overview

The mechanism of silicon nanowire FET sensors is that Si nanowires can be configured as FETs so that the resistivity of the nanowires can be modulated by the charge induced by target analytes at the Si nanowire surfaces. In this way, the amount (or concentration) of the target analytes (gases, ions, biomolecules, etc.) can be detected by monitoring the resistivity change of the Si nanowires.

Based on Equation (1.6) in section 1.3.2, silicon nanowires need to be thin and lightly doped in order to obtain maximum sensitivity. In addition, to better extract signal (resistivity change) from a measurement and increase the signal-to-noise ratio, there are several design considerations:

- The silicon nanowire needs to be lightly doped;
- Serial resistance from the substrate has to be minimized;
- Contact resistance between the Si nanowires and metal electrodes has to be minimized. That is to say, the contacts between Si nanowires and metal electrodes should be Ohmic.

3.2 Structure design

For vertically aligned Si nanowire arrays, metal electrodes must be connected to the two ends of the Si nanowires so that the resistance of the Si nanowires can be measured electrically. A metal electrode must be in full contact with the Si nanowire tips while the two electrodes cannot be in contact, which would cause a short circuit. To meet these requirements, there are two designs proposed here: top-top and top-bottom contact structures, as shown in **Figure 3.1**.

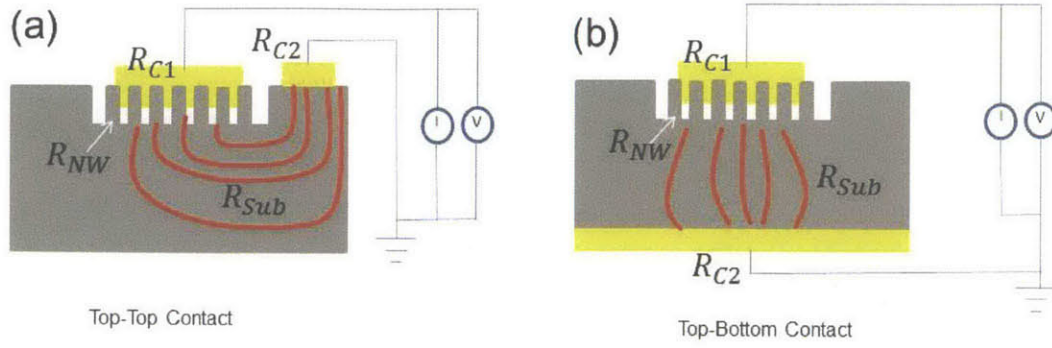


Figure 3.1 Two electrical contact schemes for vertically aligned Si nanowire FET sensors: (a) top-top contact; (b) top-bottom contact. The red lines represent the current flow paths.

The measured resistance in the closed circuit is the total resistance

$$R_{\text{total}} = R_{NW} + R_{Sub} + R_{c1} + R_{c2} , \quad (3.1)$$

where R_{NW} and R_{Sub} are the resistances of the Si nanowires and substrate, and R_{c1} and R_{c2} are the contact resistances between the Si nanowires and metal electrodes. To maximize the signal to noise ratio, R_{Sub} , R_{c1} and R_{c2} must be minimized. For the two structure designs, resistance simulations were conducted using COMSOL Multiphysics.

Assume a 3 cm x 2 cm Si substrate with resistivity $\rho_{NW} = 10 \Omega \cdot \text{cm}$ (lightly doped) is used, and the period, diameter and height of the SiNW array are 400 nm, 200 nm and 5 μm , respectively. Assume the area of the Si nanowire array in contact with the top metal electrode is 0.4 cm x 0.4 cm. The resistance of the Si nanowire array is

$$R_{NW} = \rho_{NW} \frac{L}{A} = 10 \Omega \cdot \text{cm} \frac{3 \mu\text{m}}{0.16 \text{ cm}^2 \times \frac{\pi(100 \text{ nm})^2}{(400 \text{ nm})^2}} = 0.01 \rho_{NW} . \quad (3.2)$$

where ρ_{NW} is the resistivity of the Si nanowires. For these conditions, R_{Sub} in the two structure designs was calculated below. For the top-top contact structure, two shapes of metal contact pads are considered

here: square pads and ring pads. Assume that Ni is used as the contact material in the following simulations with resistivity $\rho = 6.99 \times 10^{-8} \Omega \cdot m$.

For the square pads, it is assumed that the area of the two Ni pads is $0.4 \text{ cm} \times 0.4 \text{ cm}$, separated by a distance of $d = 0.2 \text{ cm}$ (**Figure 3.2 (a)**). Note here that the distance can be smaller but we can still estimate R_{Sub} for smaller distances since R_{Sub} changes approximately linearly with the pad distance. When one pad is grounded ($E=0 \text{ V}$), the electrical potential of another pad is swept from -1 V to 1 V . The electrical potential distribution for bias= 1 V is plotted in **Figure 3.2 (b)**. The corresponding simulated $I-V$ curve is shown in **Figure 3.3**.

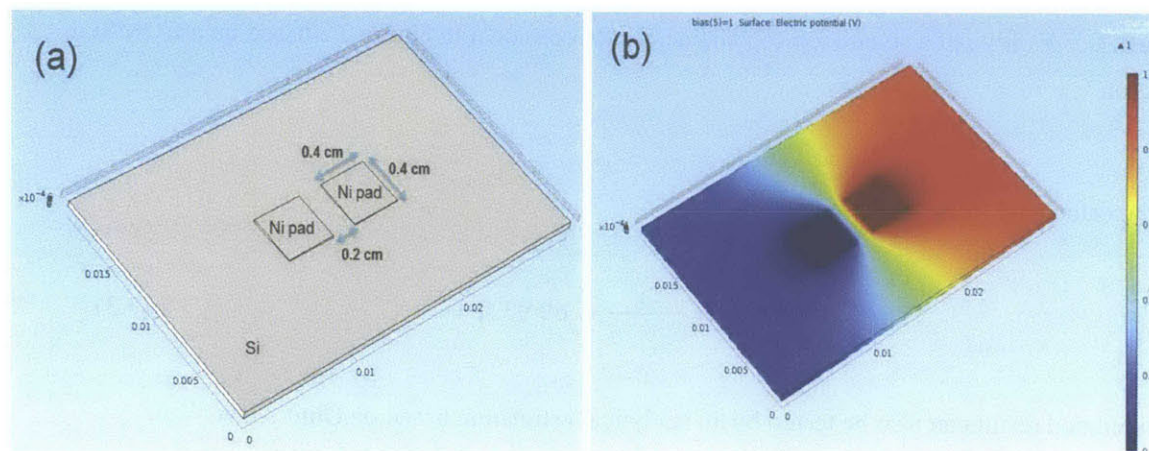


Figure 3.2 Simulation of a square top-top contact structure in COMSOL: (a) Two square top contact pads on the Si substrate; (b) Electrical potential distribution in a square top-top structure with a bias potential of 1 V .

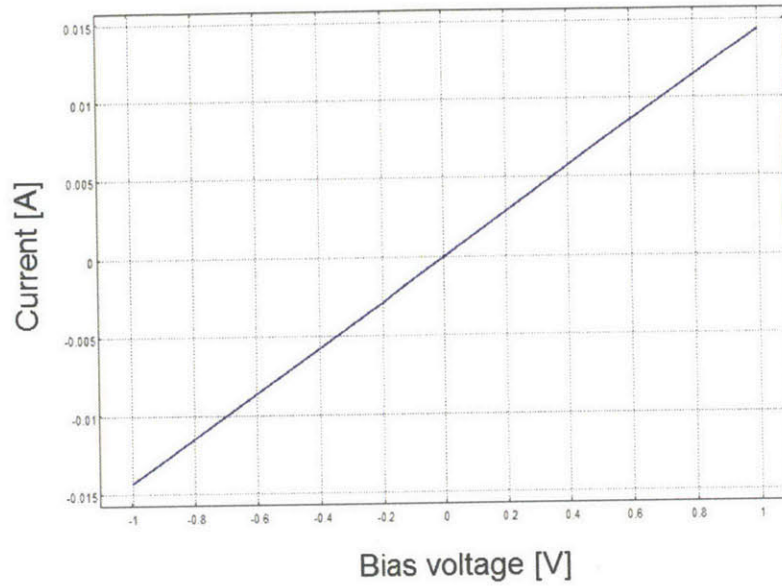


Figure 3.3 I - V curve of a square top-top contact structure shown in Figure 3.2 based on a COMSOL simulation.

It can be calculated from the I - V curve that

$$R_{Sub} = \frac{U}{I} = \frac{1V}{0.0143A} \approx 69.93 \Omega. \quad (3.3)$$

This simulated result can also be tested by an analytical estimation based on Ohm's law.

$$R_{Sub} = \rho \frac{L}{A} = 10 \Omega \cdot cm \frac{0.2 cm}{0.4 cm \times 500 \mu m} = 100 \Omega. \quad (3.4)$$

Here we assume that the current density inside the Si substrate is uniformly distributed inside the wafer thickness (500 μ m). The simulated and analytical results are close.

Another contact design for the top-top structure is a circle and a ring pads. Assume a circle and a ring pads are used as the two top contact pads, as shown in **Figure 3.4**.

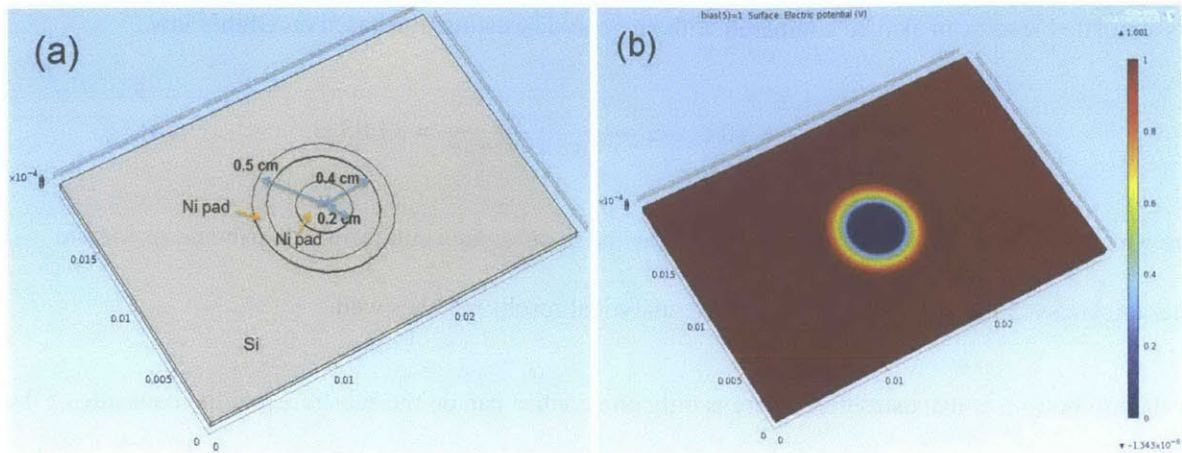


Figure 3.4 Simulation of a ring top-top contact structure in COMSOL: (a) one circular and one ring top contact pads on the Si substrate; (b) Electrical potential distribution in a ring top-top structure with a bias potential of 1V.

The corresponding simulated I - V curve of this ring contacts is shown in **Figure 3.5**.

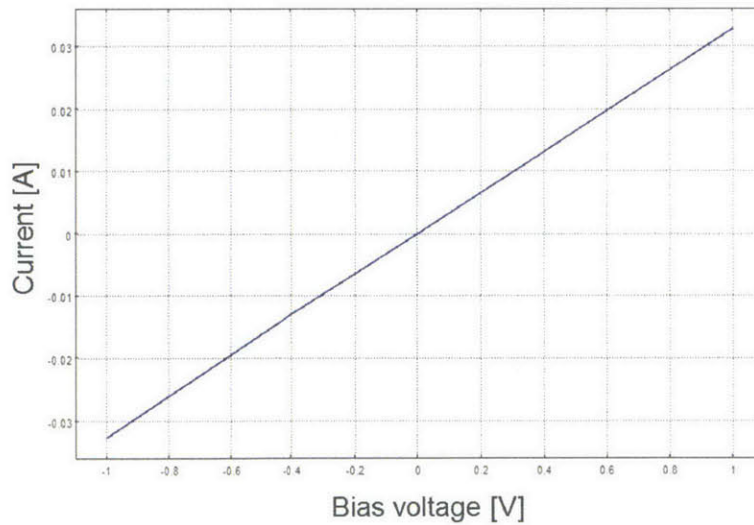


Figure 3.5 I - V curve of a ring top-top contact structure of Figure 3.4 based on a COMSOL simulation.

Similarly, it can be calculated from the I - V curve in **Figure 3.5** that

$$R_{Sub} = \frac{U}{I} = \frac{1V}{0.0327A} \approx 30.58 \Omega . \quad (3.5)$$

This simulated result can also be compared with an analytical estimation based on Ohm's law.

$$R_{Sub} = \rho \frac{L}{A} = 10 \Omega \cdot cm \frac{0.2 cm}{\pi \times 0.4 cm \times 500 \mu m} = 31.83 \Omega. \quad (3.6)$$

Here we also assume that the current density inside the Si substrate is uniformly distributed inside the wafer thickness (500 μm). The simulation and analytical results matches well.

For the top-bottom contact structure, there is only one contact pad on the substrate and the backside of the Si wafer is contacted with a deposited bottom metal electrode. In the COMSOL simulation, the bottom contact is grounded and the bias of the top contact is swept from -1V to 1V. The corresponding simulated I - V curve between the top and bottom electrodes is shown in **Figure 3.7**.

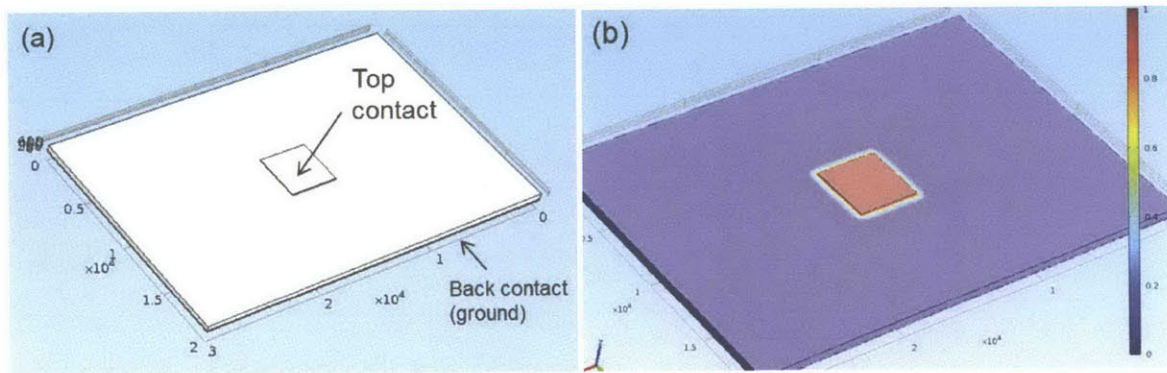


Figure 3.6 Simulation of top-bottom contact structure in COMSOL: (a) scheme of one top contact pad with a back contact to the Si wafer; (b) Electrical potential distribution in the top-bottom structure when the bias potential of the top contact is 1V.

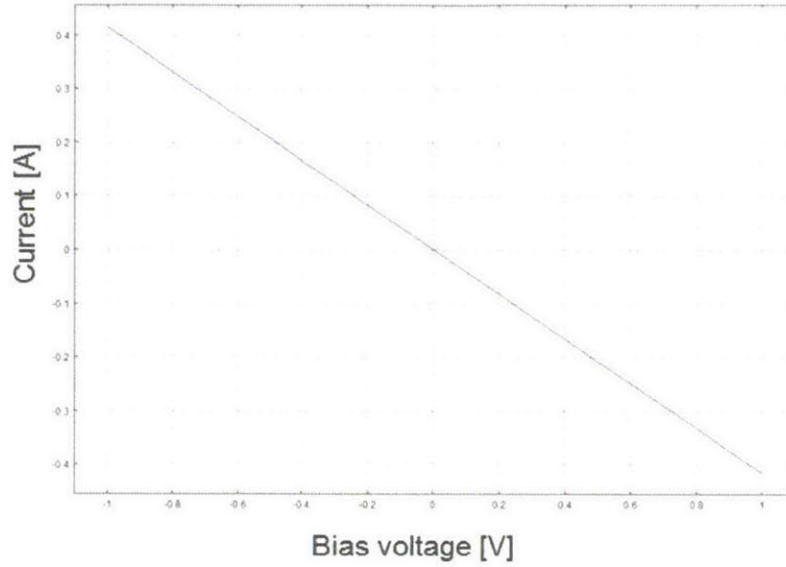


Figure 3.7 I - V curve of the top-bottom contact structure between top and bottom contacts in COMSOL simulation.

Note that the current is negative for a positive bias due to the definition of the sign of current in COMSOL. The simulated resistance of the Si substrate is

$$R_{Sub} = \frac{U}{I} = \frac{1V}{0.4146A} \approx 2.41 \Omega. \quad (3.7)$$

This result can also be compared with a simple analytical estimation. Assuming the current which flows from the top contact through the Si substrate is confined to a cross-section equal to the top contact pad (0.4 cm x 0.4 cm), the substrate resistance is

$$R_{Sub} = \rho \frac{L}{A} = 10 \Omega \cdot cm \frac{500 \mu m}{0.4 \text{ cm} \times 0.4 \text{ cm}} = 3.13 \Omega. \quad (3.8)$$

Comparing this analytical value to the simulated result, it can be found that the simulation result is reasonable.

The results of the simulations and analytical estimations are summarized in **Table 3.1**:

Contact Structure		Analytical Substrate Resistance [Ω]	Simulated Substrate Resistance [Ω]
Top-Top	Square	100	69.93
	Ring	31.83	30.58
Top-Bottom		3.13	2.41

Table 3.1 Summary of analytical and simulated substrate resistances for top-top and top-bottom contact structures (assuming the Si wafer resistivity $\rho=10 \Omega \cdot \text{cm}$).

As shown in **Table 3.1**, the substrate resistance in the top-bottom contact structure is much smaller than that in the top-top contact structure by about one order of magnitude. However, the current pad-to-pad distance in this analysis is 2 mm. Techniques such as photolithography can reduce this distance to the micro scale to achieve comparable or even smaller substrate resistance than the top-bottom contact structure. This is because the substrate resistance is approximately inversely proportional to the pad-to-pad distance according to Ohm's law. For example, if the gap in the ring contact structure is reduced from 2 mm to 1 μm , the corresponding substrate resistance will be about 0.015 Ω , which is much smaller than that in the top-bottom structure. This result is very meaningful as a top-top contact structure is desired for integration with other devices.

We have calculated that $R_{NW} = 0.01\rho_{NW}$, where ρ_{NW} is the resistivity of the Si nanowires. If ρ_{NW} is the same as the substrate resistivity $\rho_{NW} = 10\Omega \cdot \text{cm}$, then $R_{NW} = 0.1 \Omega \ll 2.412 \Omega$. Therefore, in order to maximize the ratio of Si nanowire resistance to substrate resistance, the resistivity of the SiNW should be much larger than that of the substrate. To solve this problem, an epitaxial Si wafer was used in the process. The parameters of the epitaxial Si wafer (Silicon Valley Microelectronics, Inc.) used are listed in **Table 3.2**:

Diameter	150 mm	Resistivity	0.01-0.02 ohm-cm
Type/dopant	P/Boron	Thickness	510-540 μm
Orientation	100		
Epitaxial Layer			
Type/Dopant	P/Boron	Thickness	6.75-8.25 μm
Resistivity	8.5-11.5 ohm-cm		

Table 3.2 Parameters of the epitaxial silicon wafer used for sensor fabrication.

This epitaxial Si wafer was used in the fabrication of SiNW arrays using interference lithography and MACE. Because the height of the etched SiNWs is about 5 μm which is less than the epitaxial layer thickness (6.75-8.25 μm), the fabricated SiNWs are in the layer. The remaining epitaxial layer underneath the silicon nanowire arrays is about 3 μm in thickness.

To evaluate the substrate resistance, electrical simulation is also conducted using COMSOL. The resistivity of the SiNWs and the epitaxial layer are $\rho_{\text{NW}} = 10 \text{ ohm} \cdot \text{cm}$ and the substrate resistance is $\rho_{\text{sub}} = 0.01 \text{ ohm} \cdot \text{cm}$, respectively.

For the top-top contact structure, both square and ring contacts (configuration shown in **Figure 3.3** and **Figure 3.4**) are simulated with the epitaxial wafer specified in **Table 3.2**. The corresponding I - V curve between the two pads for square and ring contacts are shown in **Figure 3.8** and **Figure 3.9**, respectively.

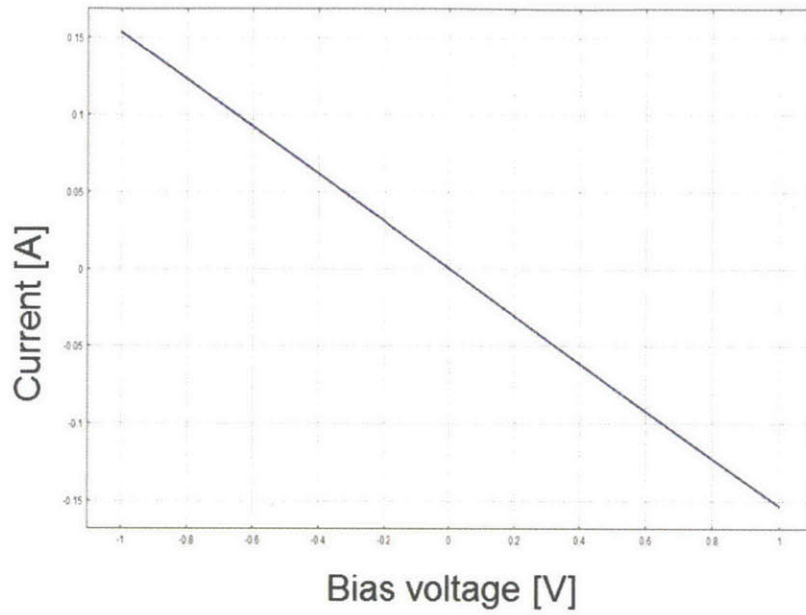


Figure 3.8 I - V curve between square top and top contacts using epitaxial wafer in COMSOL simulation.

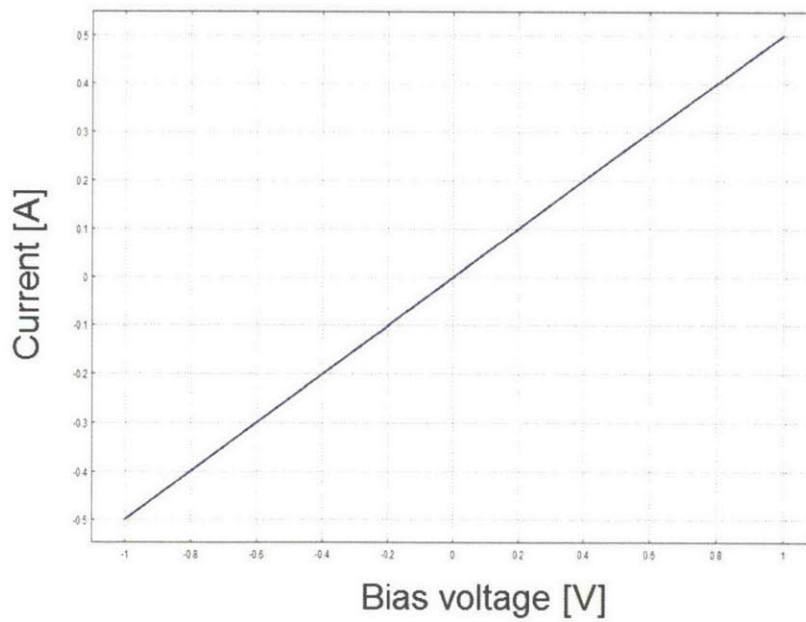


Figure 3.9 I - V curve between ring top and top contacts using epitaxial wafer in COMSOL simulation.

It can be calculated from the I - V curves that the substrate resistance of the square and ring top-top contact are

$$\text{Square:} \quad R_{Sub} = \frac{U}{I} = \frac{1V}{0.1532A} \approx 6.53 \Omega. \quad (3.9)$$

$$\text{Ring:} \quad R_{Sub} = \frac{U}{I} = \frac{1V}{0.4988A} \approx 2.00 \Omega. \quad (3.10)$$

For the top-bottom contact structure shown in **Figure 3.6**, the I - V curve of the device using epitaxial wafer is shown in **Figure 3.10**.

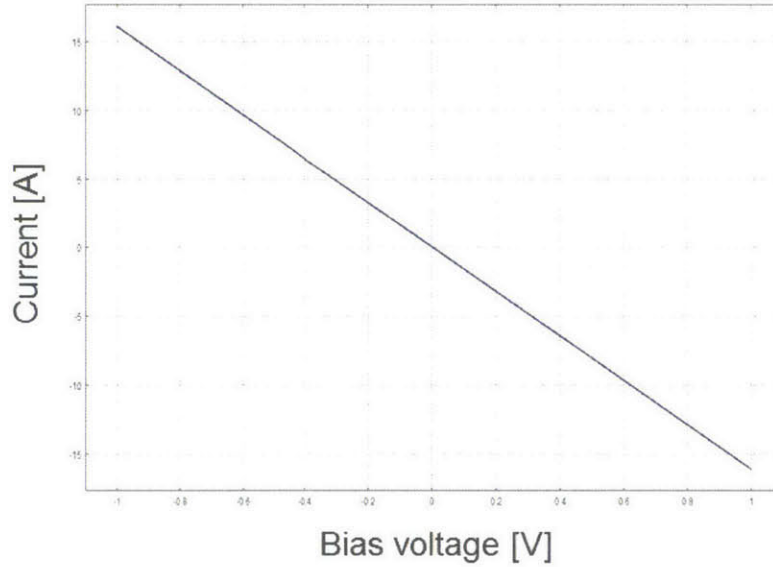


Figure 3.10 I - V curve of top-bottom contact structure using epitaxial wafer in COMSOL simulation.

Similarly, the substrate resistance between the top and bottom electrodes is

$$R_{Sub} = \frac{U}{I} = \frac{1V}{16.09A} \approx 0.062 \Omega. \quad (3.11)$$

To sum up, the substrate resistances of both top-top contact (square and ring shapes) and top-bottom using uniformly lightly doped Si and epitaxial Si are listed in **Table 3.3**.

Contact Structure		Substrate resistance [Ω]	
		Lightly doped Si wafer	Epitaxial Si wafer
Top-Top	Square	69.93	6.53
	Ring	30.58	2.00
Top-Bottom		2.41	0.062

Table 3.3 Comparison of simulated substrate resistances of both top-top contact (square and ring shapes) and top-bottom using uniformly lightly doped Si and epitaxial Si wafers.

Table 3.3 shows that by replacing the uniformly lightly doped Si wafer with a wafer which is heavily doped with a thin lightly doped epitaxial layer on top, the substrate resistances for both top-top and top-bottom contacts are significantly reduced by at least one order of magnitude. The reason for much smaller substrate resistance is that the major part of the substrate material is changed from lightly doped to heavily doped.

Another conclusion drawn from the simulations is that if the pad-to-pad distance is on the order of a few millimeters, the top-bottom contact design is preferred due to its much lower substrate resistance. That is why the top-bottom contact design is used in this study. However, the pad-to-pad distance can be reduced to the micro scale by lithographic or other patterning techniques. Then the top-top contact may have even smaller substrate resistance compared to the top-bottom design, which opens the possibility of on-chip sensing integrated with other electronic devices.

3.3 Ohmic contacts between silicon nanowire and electrodes

To measure the resistance of SiNW arrays, electrodes need to be in contact with the SiNWs. In order to minimize the contact resistances, Ohmic contacts are desired for the fabrication of SiNW field effect gas sensors.

➤ Top contact material

The top contact is made with the SiNWs, which are p-type and lightly doped. Gold and nickel were chosen and tested for making Ohmic contact to silicon wafers with different doping type and doping level.

I. Au

The contact tests were done by depositing two contact pads on the Si wafer by electron beam evaporation through a shadow mask, as shown in **Figure 3.11**.

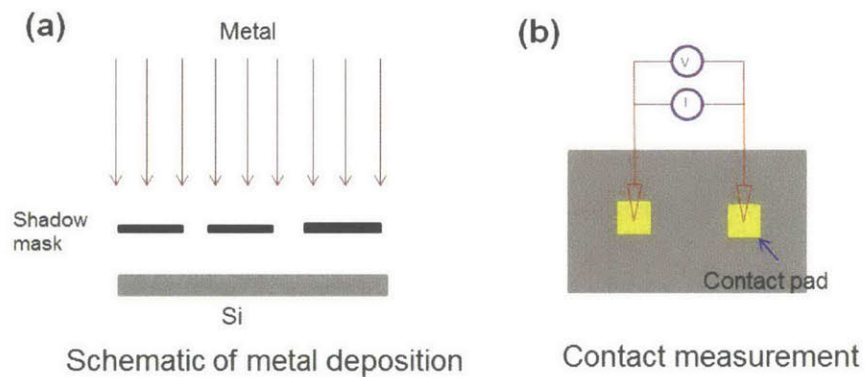


Figure 3.11 Scheme of the contact material test: (a) scheme of metal deposition through a shadow mask; (b) scheme of contact pads and measurement.

Two metal contact pads were deposited on the Si substrates with different doping level and dopant type. I - V measurements were performed to test if the I - V curves were linear. The measurement results for Au with p-type and n-type lightly doped Si are shown in **Figure 3.12**:

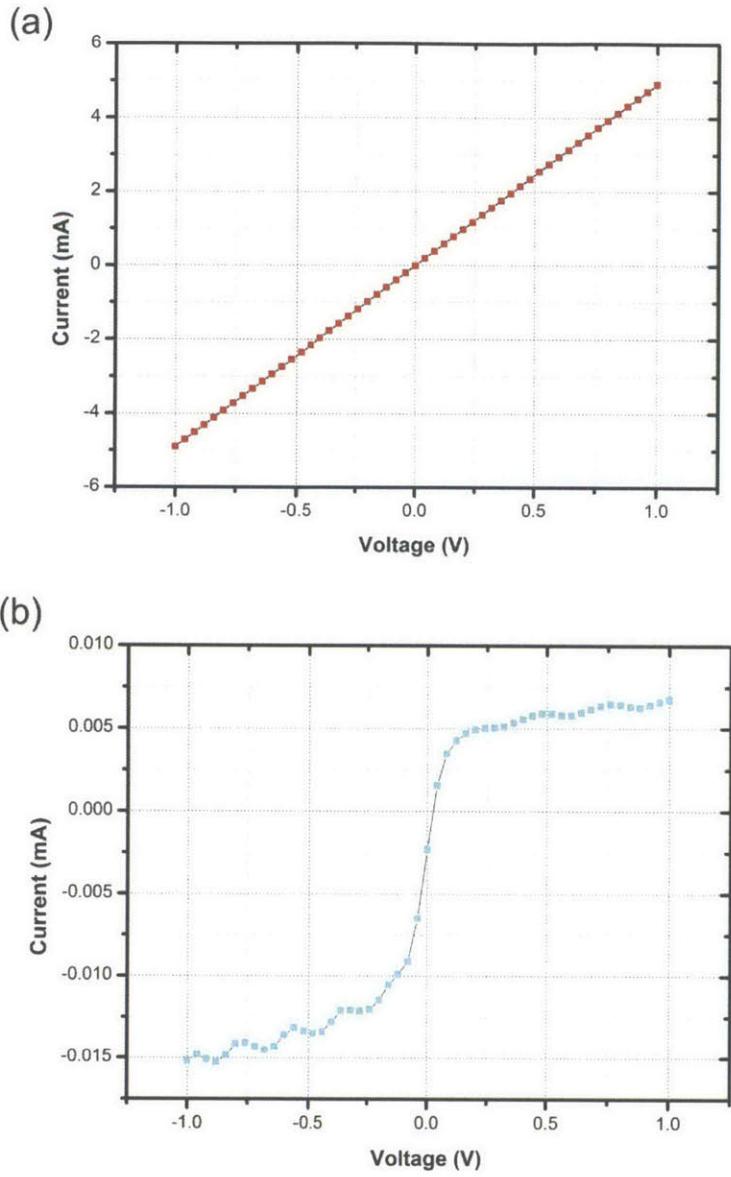


Figure 3.12 I - V measurement results for contacts between two Au pads on (a) p-type (b) n-type lightly doped Si wafers.

The linear curve in **Figure 3.12 (a)** indicates that Au forms very good Ohmic contact with p-type lightly doped Si. In comparison, the contact between Au and n-type lightly doped Si is a Schottky junction. The difference can be explained by the Schottky barrier height between the semiconductor and metal, as shown in **Table 3.4**.

Semiconductor	Metal	Barrier height, Φ_B^a (V)		
		I	II	III
n-CdS (vac-cleaved)	Au	0.78	0.80	-
	Cu	0.36	0.35	
n-CdS (chem-cleaved)	Au	0.68	0.66	0.68
	Cu	0.50	0.41	0.47
n-GaAs (vac-cleaved)	Au	0.90	0.95	-
	Cu	0.82	0.87	-
p-GaAs (vac-cleaved)	Au	0.42	0.48	-
	Pt	-	0.48	-
n-Ge (vac-cleaved)	Au	-	0.45	-
	Al	-	0.48	-
n-Si (chem-treated)	Au	0.78	0.80	0.79
	W	0.65	0.65	0.67
p-Si (chem-treated)	Au	-	-	0.25

^aI, photoelectric measurement; II, capacitance measurement; III, measurement of I - V characteristic.

Table 3.4 Table of measured values of the Schottky barrier height between different types of semiconductors and metals [76].

As shown in the table in **Table 3.4**, the barrier height between p-Si and Au is 0.25 eV, while the barrier height between n-Si and Au is about 0.65 eV. The lower the barrier height is, the more linear the I - V curve is. For a low barrier height like 0.25 eV, as in the p-Si/Au case, the I - V curve is almost linear and the contact can be called “Ohmic”. Therefore, Au can be used to form Ohmic contacts with p-type lightly doped Si.

II. Ni

In addition to Au, nickel was tested as alternative top contact material as Ni is a much cheaper material. The same contact test (**Figure 3.11**) was performed on Ni with p-type lightly doped Si. Note that for all the Ni contact tests, the sample was dipped in diluted HF solution (1:50 in deionized water) for 15 seconds before electrical measurement to remove the nickel oxides. The measurement is shown in **Figure 3.13**.

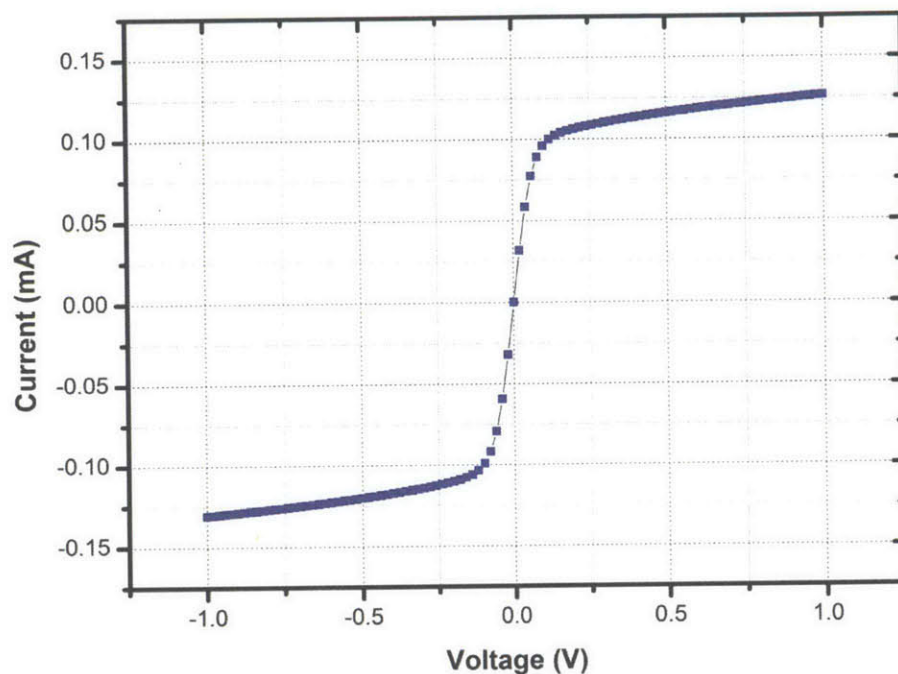


Figure 3.13 I - V measurement for contact between two Ni pads on p-type lightly doped Si.

The I - V curve in **Figure 3.13** shows a typical Schottky junction. According to an online metal-semiconductor barrier height calculator [77], the barrier height between Ni and p-type lightly doped Si is about 0.45 eV, so it is expected that the I - V curve is not linear.

In order to form an Ohmic contact between Ni and p-type lightly doped Si, nickel silicide can be formed by rapid thermal annealing (RTA), which will greatly lower the barrier height. Among the various phases of silicide, NiSi is the most commonly used. During the past decade, NiSi replaced TiSi₂- and CoSi₂-

based metallization in VLSI ICs, owing to its lower annealing temperature and lower resistivity. The different phases of nickel silicide during annealing are shown in **Figure 3.14** [78]:

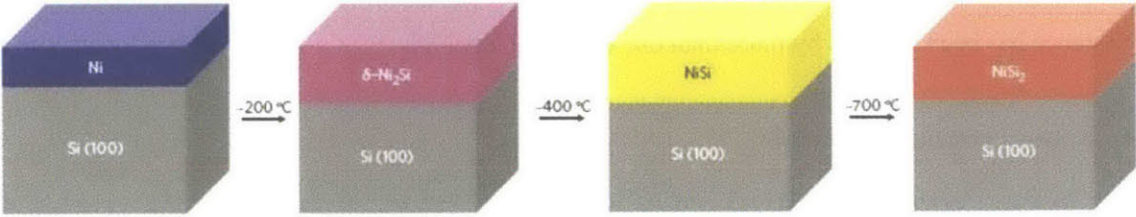


Figure 3.14 Formation of the different phases of nickel silicide on a (100) Si wafer [78].

The sample with Ni contact pads on the Si substrate was annealed at 500°C in forming gas (H₂+N₂) for 1 minute. The contact behavior was measured again and the *I-V* curve is shown in **Figure 3.15**.

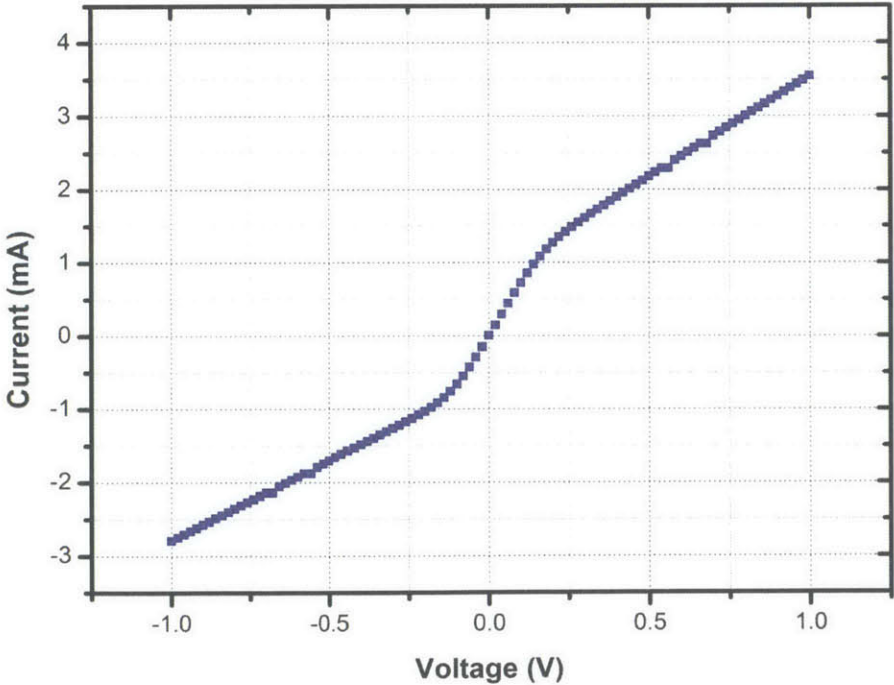


Figure 3.15 *I-V* measurement for contact between two Ni pads on p-type lightly doped Si after rapid thermal annealing at 500°C in forming gas for 1 minute.

Compared with the measurement in **Figure 3.13**, the I - V curve becomes much more linear after the RTA process. The formation of NiSi during the annealing reduces the energy barrier between Ni and Si, making the contact much more Ohmic. It can be found in **Figure 3.13** and **Figure 3.15** that the total resistance has been reduced by more than one order of magnitude.

➤ **Bottom contact material**

The bottom contact metal was deposited on the backside of the Si substrate. For the epitaxial Si wafer used in the sensor fabrication process, the backside of the Si substrate is p-type heavily doped (see Table 2). The resistivity is $\rho=0.01$ - 0.02 ohm-cm. It can be calculated from an online resistivity & mobility calculator [77] that the dopant concentration is approximately $N_A=5 \times 10^{18}$ cm⁻³. Such a high doping level makes it easy for carriers to tunnel through the energy barrier between the Si substrate and metals, resulting in Ohmic behavior.

A Cr/Au bilayer was used to make the bottom contact. Cr was deposited between the Si substrate and the Au layer to enhance adhesion. The thickness of the Cr/Au bilayer was 10 nm/100 nm. A contact test was also done with Cr/Au as two contact pads on p-type heavily doped Si. The I - V curve indicates good Ohmic contact (as shown in **Figure 3.16**):

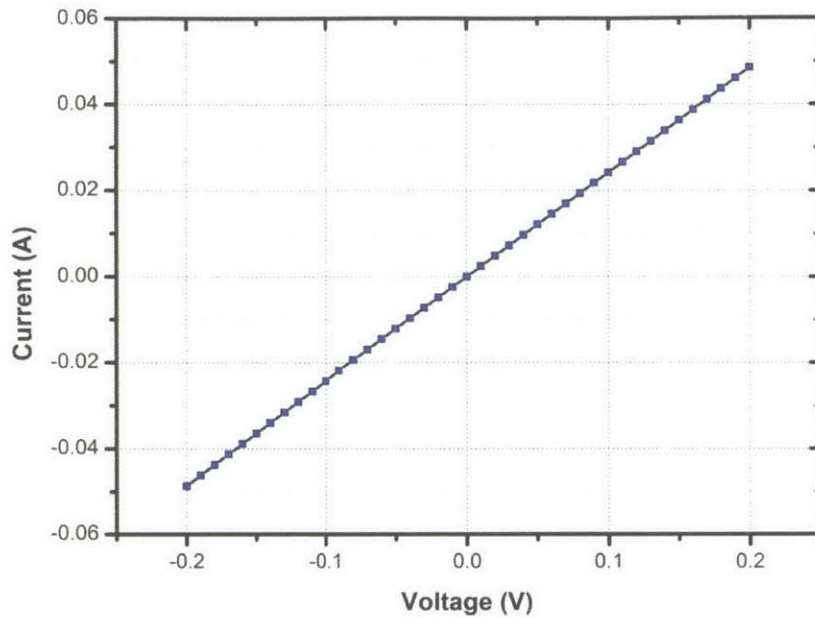


Figure 3.16 I - V measurement for contact between two Cr/Au pads on p-type heavily doped Si. The linear I - V relationship is consistent with the theory that heavily doped Si forms good Ohmic contact with metal.

In conclusion, by conducting the contact tests, it was found that Au or Ni can be used as top contact materials and a Cr/Au bilayer can be used as the bottom contact material to obtain Ohmic contacts between the Si wafer and the metal electrodes. For Ni, a rapid thermal annealing process is necessary to cause formation of NiSi.

3.4 Top electrical contact fabrication

3.4.1 Overview

The major challenge in making electrical contacts to vertically aligned SiNW sensors is in making the top electrical contact. The metal electrode needs to be in contact with the upper part of the SiNW array

without touching the other ends of the SiNWs or the substrate. A number of approaches have been explored to make reliable top electrical contacts. The most common approach involves using a polymer as a sacrificial layer for suspended metal electrode deposition [39, 41, 79]. A typically procedure is shown in **Figure 3.17** [79]:

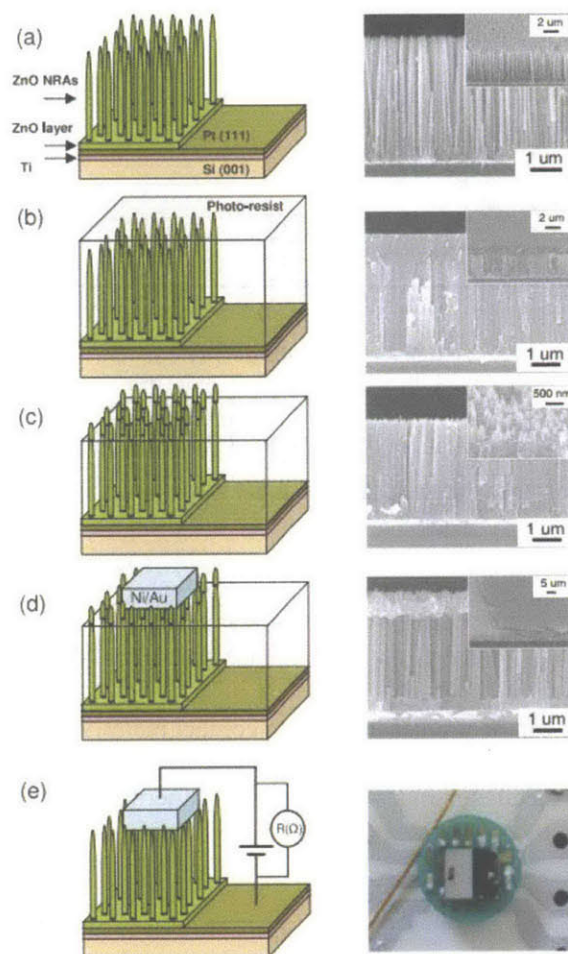


Figure 3.17 Schematic and real images of the fabrication of ZnO NRA sensors [79].

Typically, a polymer is filled into the nanowire gaps by spin coating to embed the nanowire array in the polymer. Plasma etching is then performed to etch back the polymer and reveal the nanowire tips. Subsequently, a metal layer is deposited on the exposed tips by sputtering or thermal evaporation to form

contacts with the nanowire array. Finally, the polymer is removed, forming an air-bridged top electrical contact.

However, this approach has many drawbacks. First, it is challenging to embed the nanowire arrays well inside polymers, especially when the wire spacing in the array is small. The small gaps in dense nanowire arrays make it difficult for the polymer to fill the gaps well. If the polymer layer is suspended in some of the nanowire areas and has a small thickness, it might be etched completely during the subsequent plasma etching process. The metal deposition step will then cause a short-circuit of the device. Second, if the nanowire heights are non-uniform, uniform coating with polymers is even more difficult. Finally, the polymer may not be removed completely and the residue will contaminate the nanowire surfaces, and affect their sensor functionality.

Due to the reasons mentioned above, a few researchers have explored alternative approaches to construct top electrical contacts. Han et al. developed a technique to directly form suspended layer of polystyrene on the upper part of vertical SiNWs by bringing an aluminum foil with spin-coated polystyrene into contact with the nanowire surface and heating to its glass transition temperature.[40] However, the variation of polystyrene thickness makes it very challenging to just cover the upper part of SiNWs. The nanowire height is usually less than 10 μm while the roughness of the polystyrene after heating is very likely to exceed the nanowire height. In this case, those nanowires which are entirely embedded in the polystyrene matrix will not be utilized. It is therefore expected that the uniformity of the top contact will not be very good. Koto et al. developed a process based on sacrificial layer deposition and chemical mechanical polishing (CMP) to make top contact [80], as shown in **Figure 3.18**.

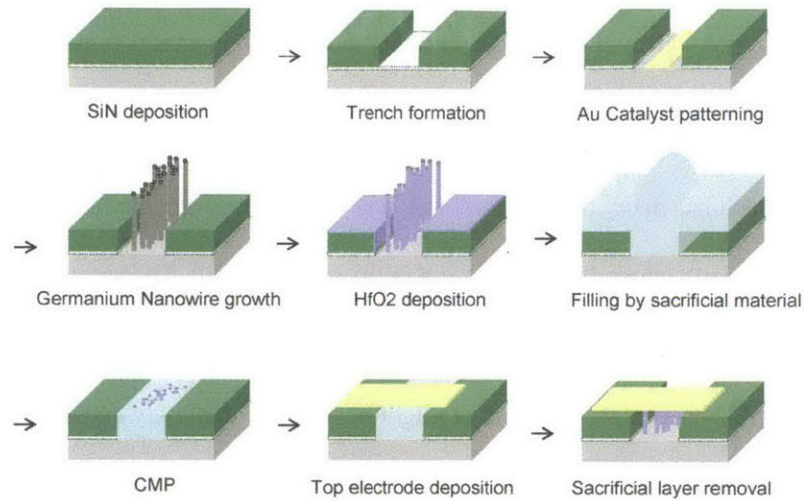


Figure 3.18 Schematic of vertical Germanium nanowire fabrication process [80].

However, this process involves complicated processes such as CMP for planarization, PECVD of SiO_2 as the sacrificial layer and sacrificial layer removal. Therefore new approaches for constructing mechanically reliable and electrically Ohmic top contacts are needed.

3.4.2 Tilted electron beam evaporation for top contact

To overcome the limitations of existing approaches for the fabrication of top electrical contact to vertically aligned nanowires, a new technique has been developed in this study. Tilted electron beam evaporation was used to deposit metal film on the uppermost part of SiNW tips to directly form a suspended top contact. A schematic is shown in **Figure 3.19**.

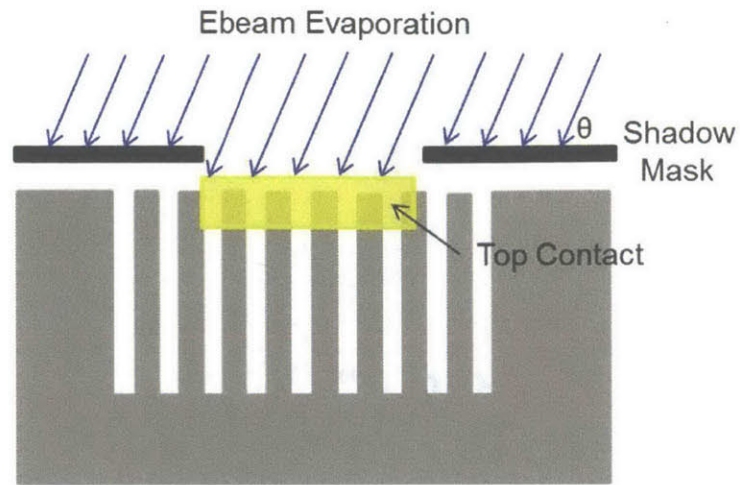


Figure 3.19 Schematic of tilted electron beam evaporation for making a top contact.

As shown in **Figure 3.19**, metal is deposited onto the SiNW sample at an angle θ in an electron beam evaporator. A shadow mask is placed just above the sample to pattern the top contact area. In this way, metals can be deposited and accumulated on the SiNW tips without going down to the substrate due to the shadowing effect. The tilted evaporation is realized using a custom-built rotating plate shown in **Figure 3.20**.

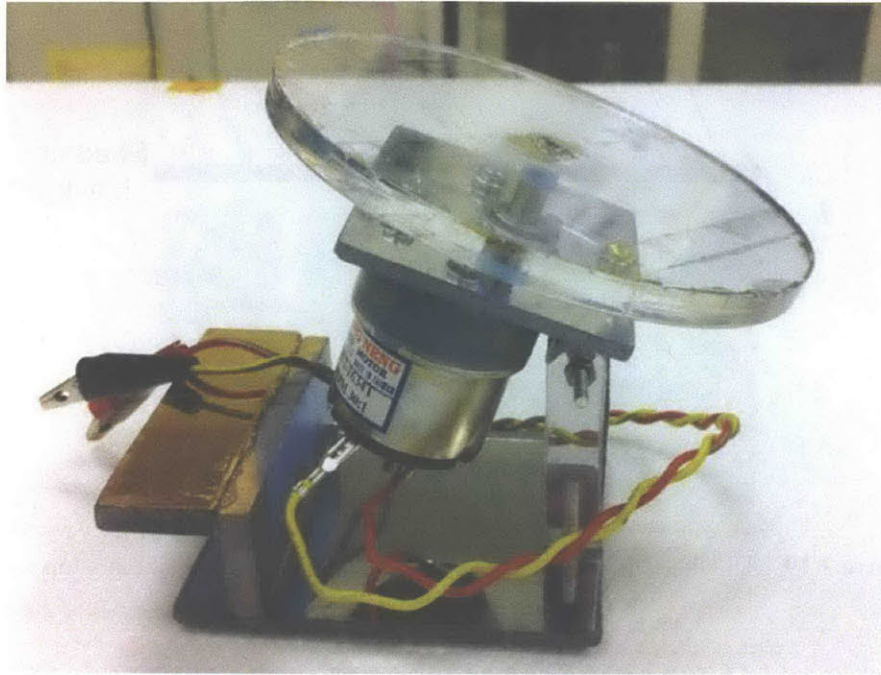


Figure 3.20 A custom-built rotating plate for tilted ebeam evaporation.

During evaporation, the sample is placed on the transparent circular plate, which can be tilted at an angle with respect to the evaporant source. The rotating plate can also rotate during the evaporation process driven by an electric motor to ensure conformal metal coverage over the top contact area. This device is run on a battery, which is also placed inside the chamber of the electron beam evaporator.

A two-step deposition process was developed for tilted electron beam evaporation. After fabrication of wires-in-trench structures using interference lithography, as shown in **Figure 2.13**, the sample was dipped in diluted HF solution (1:50 in deionized water) for 10 seconds to remove the native oxide on the surface of the SiNWs to ensure good Ohmic contact between the SiNWs and the metal film.

Au was first used as the top contact material. After attaching the SiNW sample onto the rotating plate using double-sided adhesive tape, the rotating plate was put inside the electron beam evaporator immediately after the HF dip. The rotating plate was tilted at an angle of 60° with respect to the metal

source. A shadow mask with a $4\text{ mm} \times 4\text{ mm}$ opening was put on the sample for contact patterning. 800 nm Au films were then deposited onto the sample at a rate of about 1 \AA/s . A scanning electron microscopy (SEM) micrograph of a cross-section of a sample are shown in **Figure 3.21**.

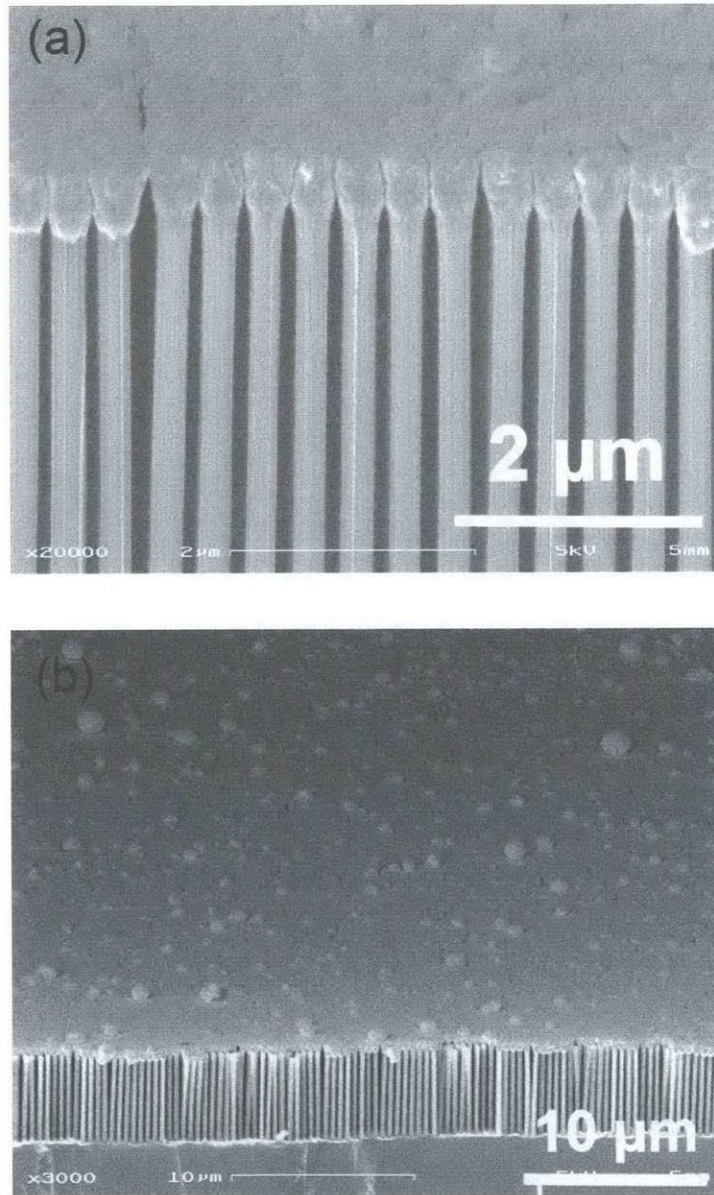


Figure 3.21 SEM micrographs of a 800 nm Au film deposited at an angle of 60° with respect to the sample normal: (a) cross-section of the SiNW array (b) top view of the large top contact area.

A second evaporation step was performed in order to completely seal the top Au film. 300 nm Au was deposited onto the sample at normal incidence with respect to the sample through the same shadow mask used in the first tilted evaporation step. After this second deposition, the suspended Au film became continuous, as shown in **Figure 3.21**.

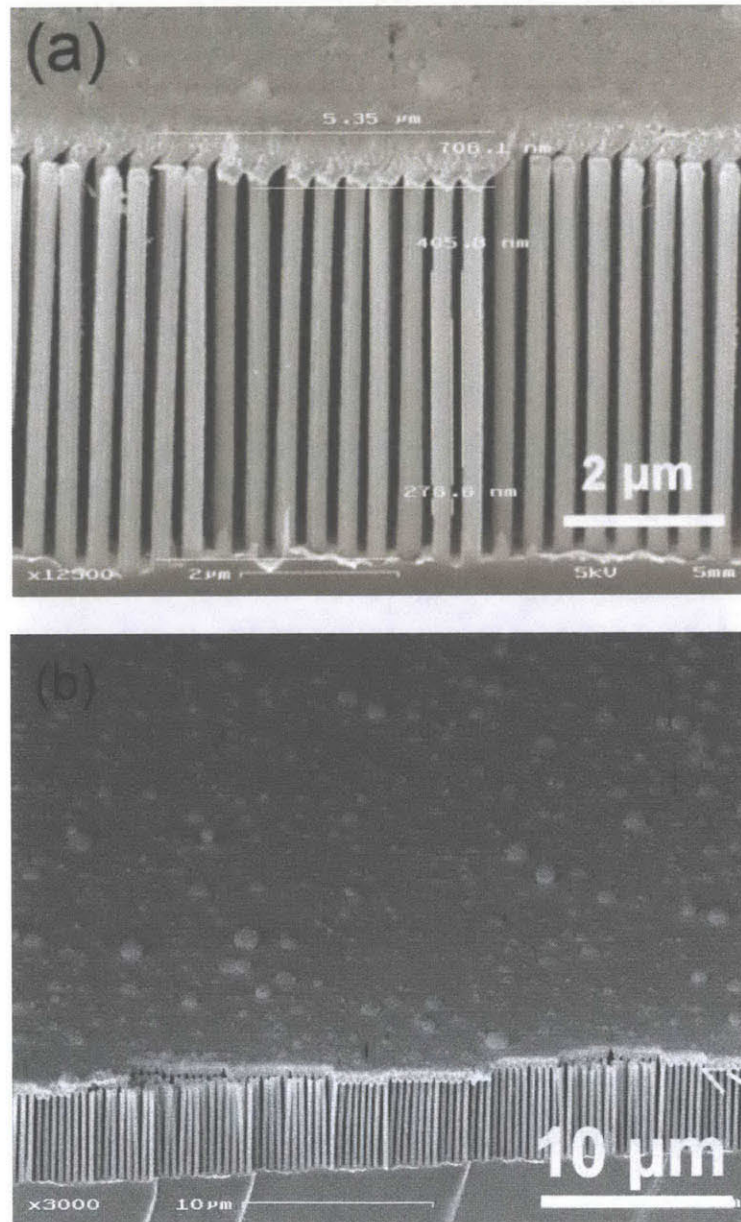


Figure 3.22 SEM micrographs of an Au film after a two-step ebeam evaporation process: (a) cross-section of SiNW array; (b) top view of the large top contact area.

As the SEM micrographs show, the Au film was fully sealed to form a continuous film suspended on the top of the SiNW arrays. The final Au film thickness was about 700~800 nm.

In addition to Au, Ni was also tested as the top contact material, following the same tilted evaporation process for Au described above. SEM micrographs of the Ni top contact after the two-step electron beam evaporation are shown in **Figure 3.23**.

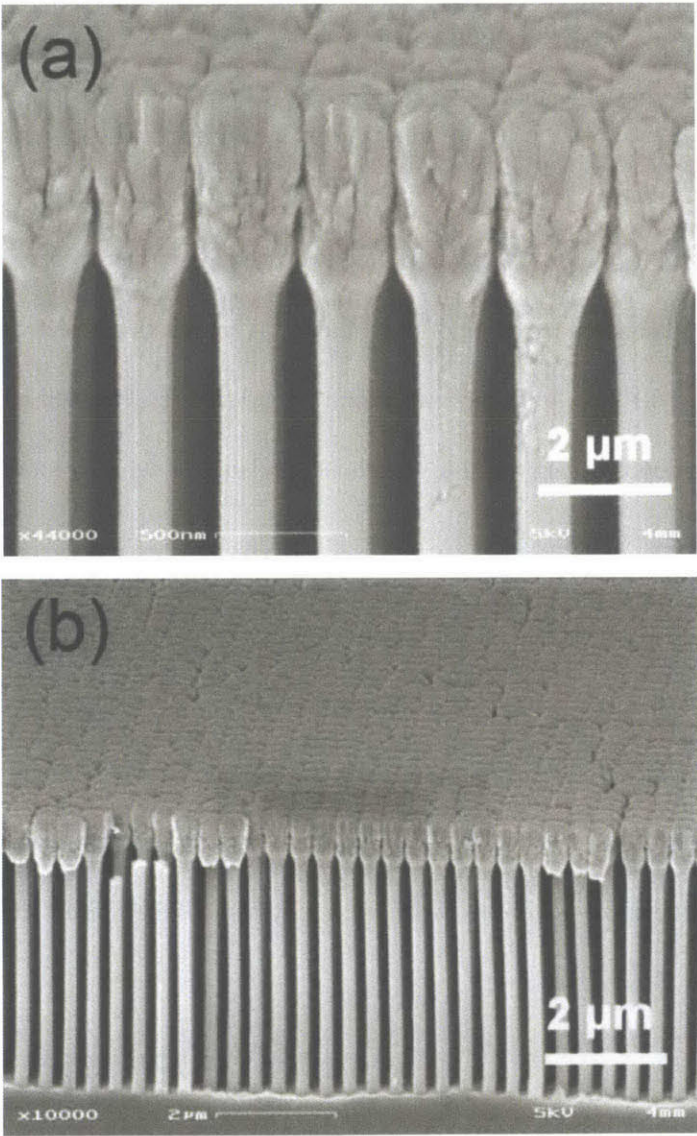


Figure 3.23 SEM micrographs of a Ni film after a two-step ebeam evaporation process: (a) cross-section of SiNW array; (b) top view of the large top contact area.

3.5 Bottom contact and wire bonding

After the construction of the top contact using the tilted electron beam evaporation approach, the bottom contact was made by depositing a bilayer of Cr and Au. The role of the Cr layers was to enhance the adhesion between the Si backside and the Au contact. The contact test results show that such as bilayer will form a good Ohmic contact with the heavily doped Si substrate.

The sample was dipped in a diluted HF solution for 10 seconds for surface oxide removal. A 10 nm Cr layer was then deposited onto the backside of the epitaxial Si sample using electron beam evaporation with a deposition rate of 0.1 Å/s. A 100 nm Au second layer was then deposited immediately after the Cr layer deposition with a deposition rate of 1 Å/s (without breaking vacuum) by rotating the deposition material inside the ebeam evaporator.

After fabrication of the top and bottom contacts, the sample was mounted on a Leadless Chip Carrier (LCC) or TO Headers (Spectrum Semiconductor materials, Inc.) with a double-sided conductive carbon tape. The top contact metal film was connected to the chip carrier using silver conductive epoxy (Ted Pella, Inc.). A small amount of silver epoxy was deposited onto the top contact film and a thin electrical wire was immersed in the epoxy before it hardened. A schematic of the sensor device is shown in **Figure 3.24**.

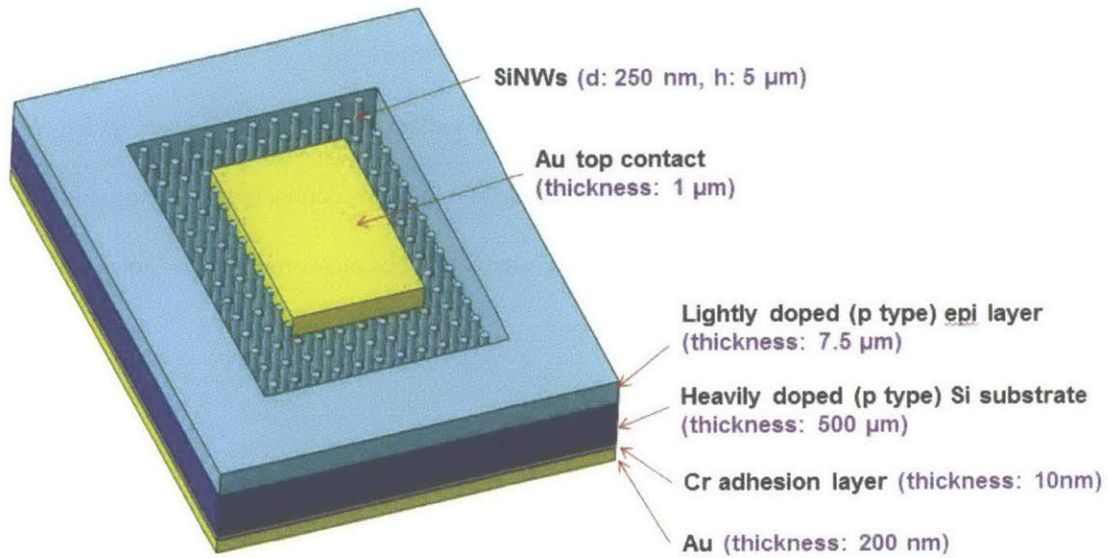


Figure 3.24 Schematic of the fabricated SiNW field effect sensor.

Sensor devices were made with different chip carriers as shown in **Figure 3.25**:

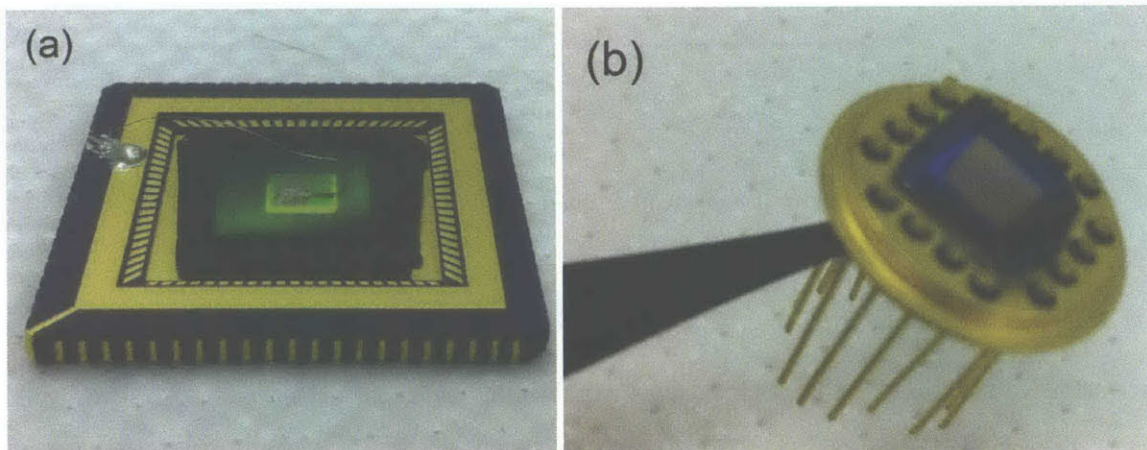


Figure 3.25 Picture of the fabricated sensor device with (a) an LCC chip carrier; (b) a TO Headers chip carrier.

3.6 Device electrical characterization

After the sensor device fabrication, the current (I) – voltage (V) characteristic of the sensor device was measured using a probe station. The two probes were landed on the pads connected to the top and bottom contact of the sensor device. **Figure 3.26** shows the I - V characteristics measured from a fabricated device with Au as the top contact material.

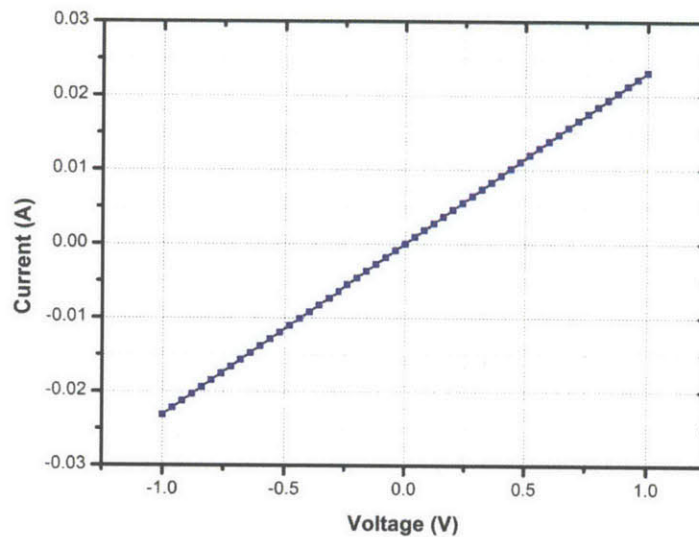


Figure 3.26 I - V curve of a fabricated sensor device with Au contact top contact.

The voltage was swept from -0.1V to 0.1V and the current was recorded. The linear I - V curve shown in **Figure 3.26** clearly shows the Ohmic characteristic of the electrical contact between the SiNW array and the top and bottom electrodes. This is consistent with the previous contact tests described in section 3.3.

Chapter 4 Silicon Nanowire FETs for Gas Sensing

4.1 Measurement setup

In order to demonstrate the sensing performance of the fabricated SiNW sensor devices, a sensing measurement setup was built for gas sensing. **Figure 4.1** represents a schematic of the sensing characterization system:

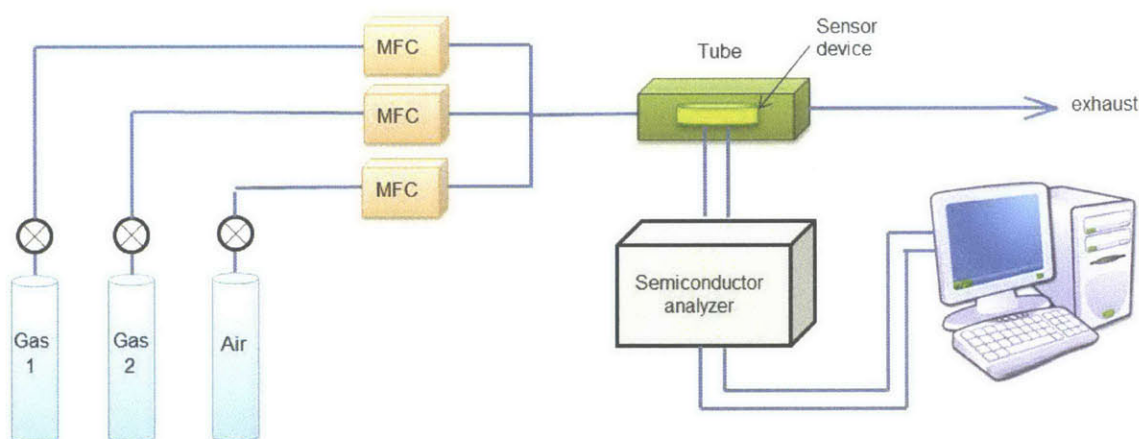


Figure 4.1 Schematic of gas sensing characterization setup.

Gas tanks with target analyte gases were connected to Mass Flow Controllers (MFC) which were used to control the flow rate of the gas. The sensor device with TO Headers chip carriers was inserted in a device holder (**Figure 4.2 (a)**) and placed into a transparent plastic tube (**Figure 4.2 (b)**). The two pins were connected to the top and bottom contacts of the sensor device. The size of the tube was about 10 cm x 3 cm x 2 cm. Analyte gases flowed through the tube where they were absorbed onto the SiNW surfaces. The sensor device was electrically connected to a Solartron impedance analyzer (Solartron analytical.,

Inc.). The MFCs were programmed using a Labview interface (**Figure 4.2 (c)**). The sensing setup was in a fume hood for safety considerations.

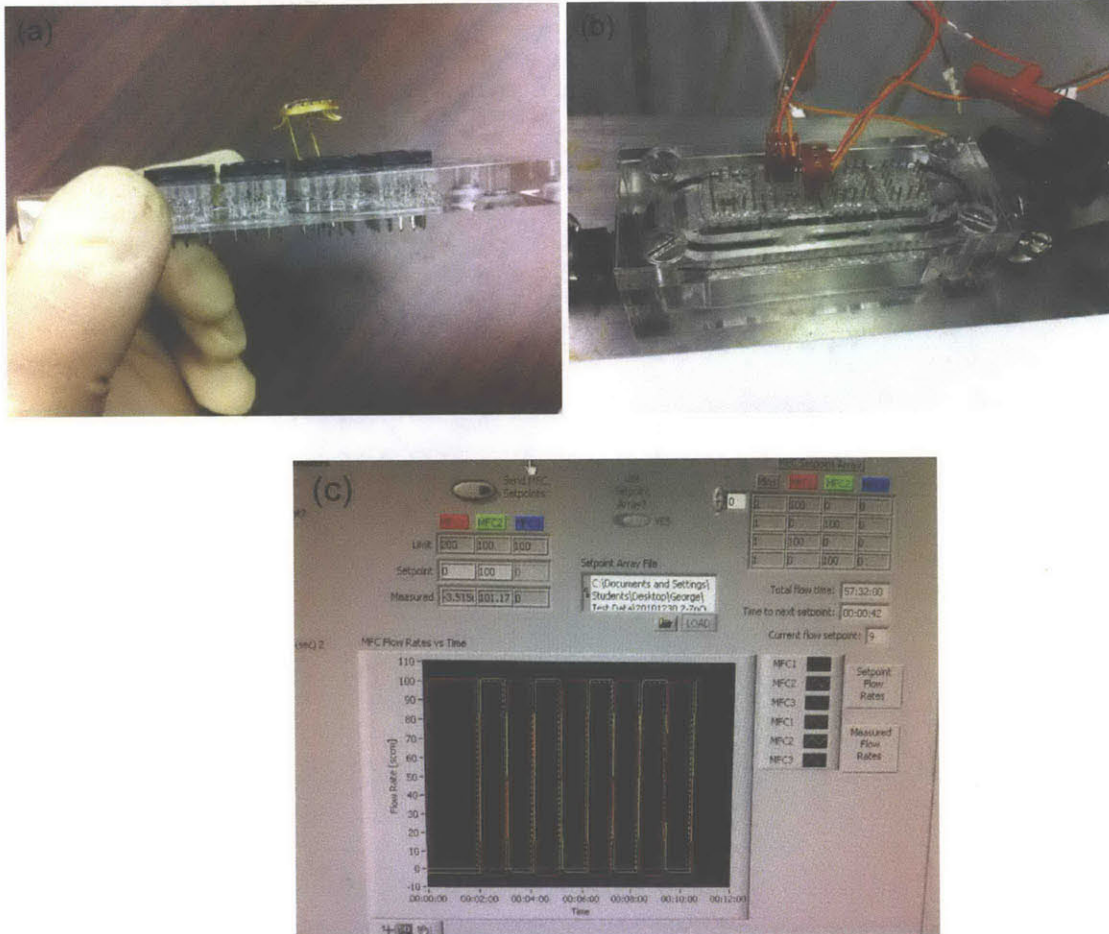


Figure 4.2 Photos of the gas sensing equipment: (a) sensor device inserted in device holder; (b) plastic tube with sensor device inside; (c) Labview interface for MFC control.

4.2 Gas sensing results

As explained in section 4.1, reducing gases such as hydrogen absorbed on the SiNW surface can lead to an increase of the SiNW resistivity while oxidizing gases like oxygen have the opposite effect. To test the

performance of our sensor devices, sensing measurements were performed with the setup shown in **Figure 4.1**, using different gases including hydrogen, oxygen, ammonia and nitrogen dioxide gases as target gases at room temperature. Gases were connected to the tube through three MFCs. A built-in program CorrView in a Solartron impedance analyzer was used to monitor the resistance of the sensor device. A constant voltage of $V=0.1V$ was applied between the two pins of the device, which were connected to the top and bottom electrodes of the sensor device. The current of the closed circuit was recorded using the impedance analyzer at a sample rate of 5 Hz. Therefore the resistance can be calculated and plotted directly from the measured current without any filtering or smoothing data processing steps. All the sensing measurements were carried out at room temperature.

4.2.1 Hydrogen and oxygen detection

Hydrogen and oxygen gases were first tested as target gases to demonstrate the sensing performance of the devices.

a. Hydrogen sensing

Initially the device was sitting in the plastic tube in an air ambient. At time $t = 120$ s, pure hydrogen gas flowed into the system with a flow rate of 100 sccm (standard cubic centimeters per minute). The total measuring time was 30 min. The resistance response to H_2 is plotted in **Figure 4.3**.

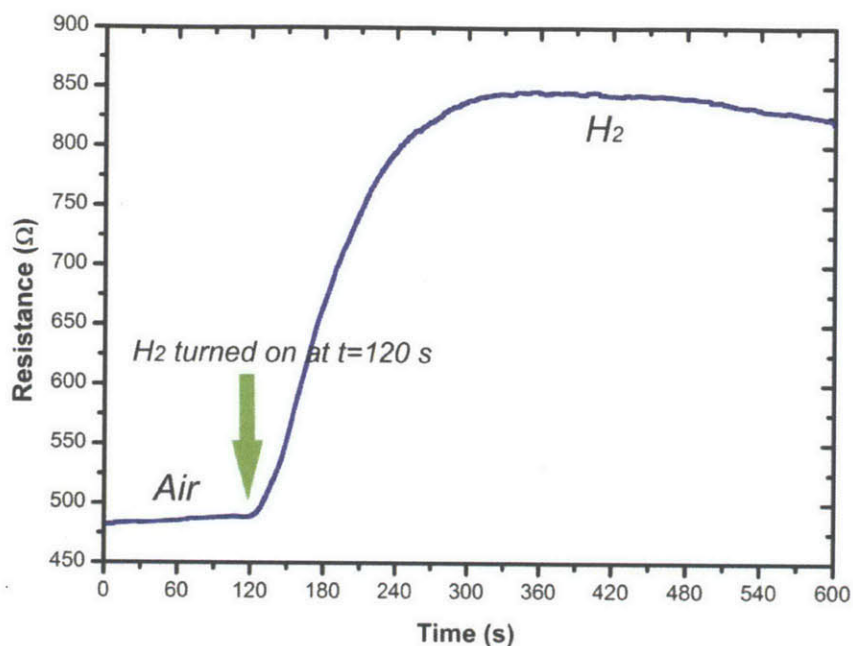


Figure 4.3 Electrical response of the SiNW field effect gas sensors to H₂ gas.

As shown in **Figure 4.3**, the device resistance increased immediately when exposed to H₂ after a few seconds. Then the resistance reached a saturation point after exposure to the hydrogen gas for 3 minutes.

To test the repeatability of the hydrogen sensing result, a number of sensing cycles were conducted including an air test as the control experiment. The sensor response is plotted as the normalized resistance change, which is defined as the change in resistance divided by the initial baseline resistance ($\Delta R/R_0$).

The normalized resistance change is plotted in **Figure 4.4**.

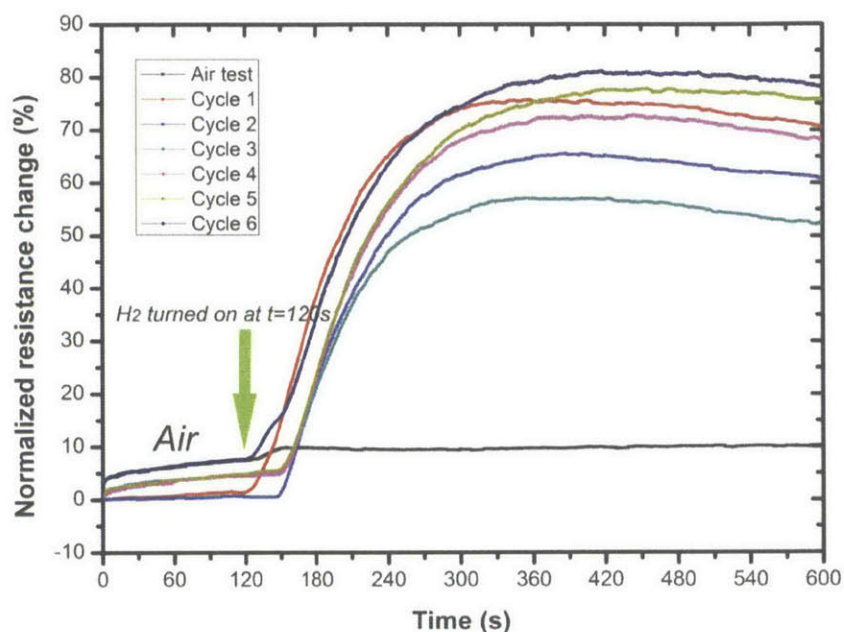


Figure 4.4 Normalized resistance change of SiNW field effect sensors for air test and multiple H₂ gas sensing cycles.

First, an air test was performed to eliminate possible resistance change induced by the air gas. For the air test, the sensor device was initially in an air ambient. At time $t = 120$ s, air was sent into the tube with a flow rate of 100 sccm. As the air test curve shows, the resistance of the device almost did not change. Subsequently, six H₂ gas sensing cycles were performed. For each cycle, pure H₂ gas flowed into the tube with the same flow rate (100 sccm) after time $t = 120$ s. Between each cycle, the device was heated on a hotplate at 200 °C for 10 minutes and then cooled down to room temperature for 15 minutes. This heating process was used to accelerate the gas desorption process so that the device could return to the initial baseline resistance quickly after a sensing cycle. The curves in **Figure 4.4** clearly show that the sensing response to H₂ gas was repeatable, indicating good stability of the sensor device. The resistance increased instantly after H₂ gas was turned on and it reached saturation after exposing to H₂ gas for about 3 minutes. The normalized resistance change at saturation level is about 60%~80%. The resistance dropped a little bit after reaching the maximum point. Similar overshooting behaviors are also reported in other gas sensing experiments reported by Pehrsson *et al* [81]. This overshooting phenomenon in resistance is considered to be the result of the competition between diffusion and reaction of the gas molecules at the nanowire surface under non-steady state conditions [82].

(b) Oxygen sensing

The same sensing experiments were done using oxygen as the target gas. Pure oxygen gas was turned on at $t = 120$ s with a flow rate of 100 sccm. As expected, oxygen exposure led to very quick decrease of the sensor's resistance and it reached saturation after about 6 minutes, which was just the opposite to hydrogen sensing. The normalized resistance change $\Delta R/R_0$ is about 15%. A typical electrical response of a sensing test to oxygen gas is shown in **Figure 4.5**.

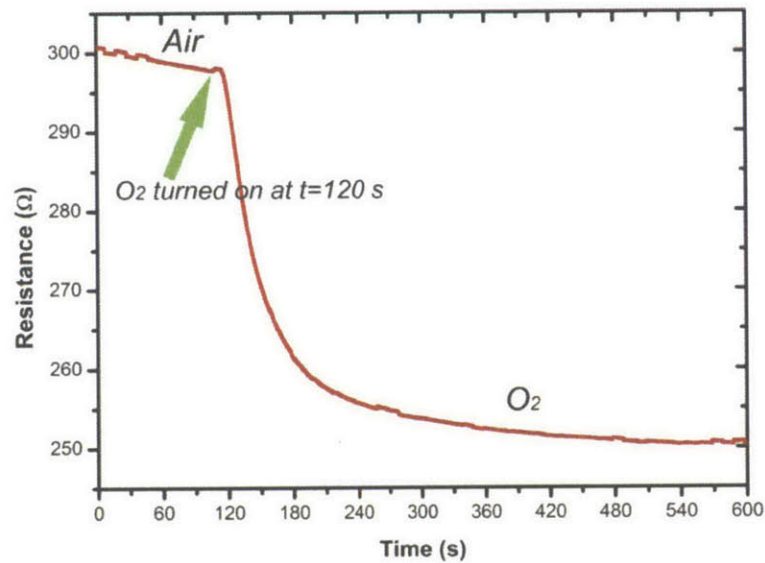


Figure 4.5 Electrical response of the SiNW field effect gas sensors to O_2 gas.

Similar to the cycle tests in the hydrogen case, multiple sensing cycles were conducted including an air test. The sensors also went through the same heating and cooling processes as described in H_2 gas sensing. **Figure 4.6** presents the electrical response of the sensor device to air and O_2 gas.

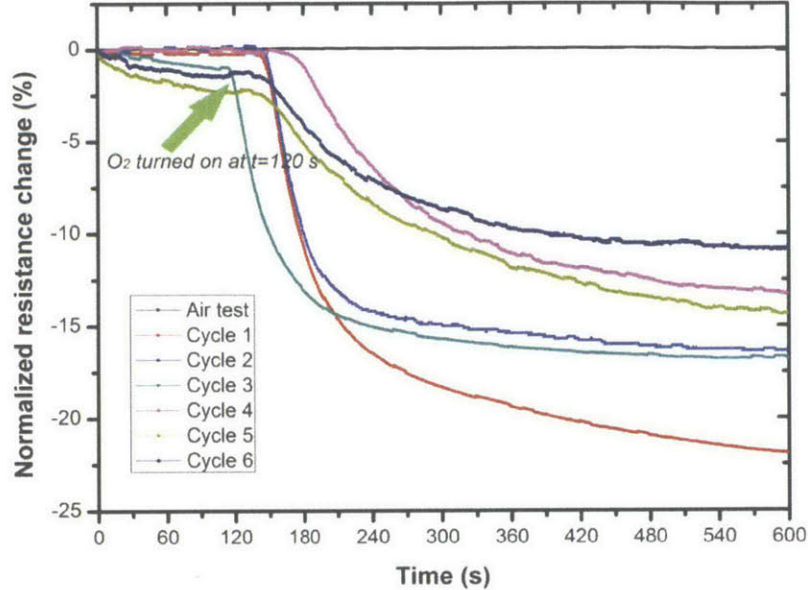


Figure 4.6 Normalized resistance change of SiNW field effect sensors for air test and multiple O₂ gas sensing cycles.

As shown in **Figure 4.6**, almost all the curves reached saturation after exposure to O₂ gas for 8 minutes. The largest normalized resistance change is about 22% at $t = 10$ min. For the total 6 cycles, the range of maximum normalized resistance change is about 11% to 22%. As we can see, the sensitivity has roughly a decreasing trend from cycle 1 to cycle 6. This degradation might be the result of the thickening of the oxide layer during the heating process. Further material characterization (such as transmission electron microscopy) can be done to evaluate the change in the nanowire structures.

To compare the different response to H₂ and O₂ gases, the normalized resistance change can be plotted using two typical sensing data shown in **Figure 4.3** and **Figure 4.5**. The comparison is shown in **Figure 4.7**. It clearly shows different trends of resistance change when the sensor device is exposed to hydrogen or oxygen gas. The electrical responses are consistent with the electron donating properties of H₂ and electron withdrawing properties of O₂. The normalized resistance changes for H₂ and O₂ at saturation levels are 70% and 16%, respectively.

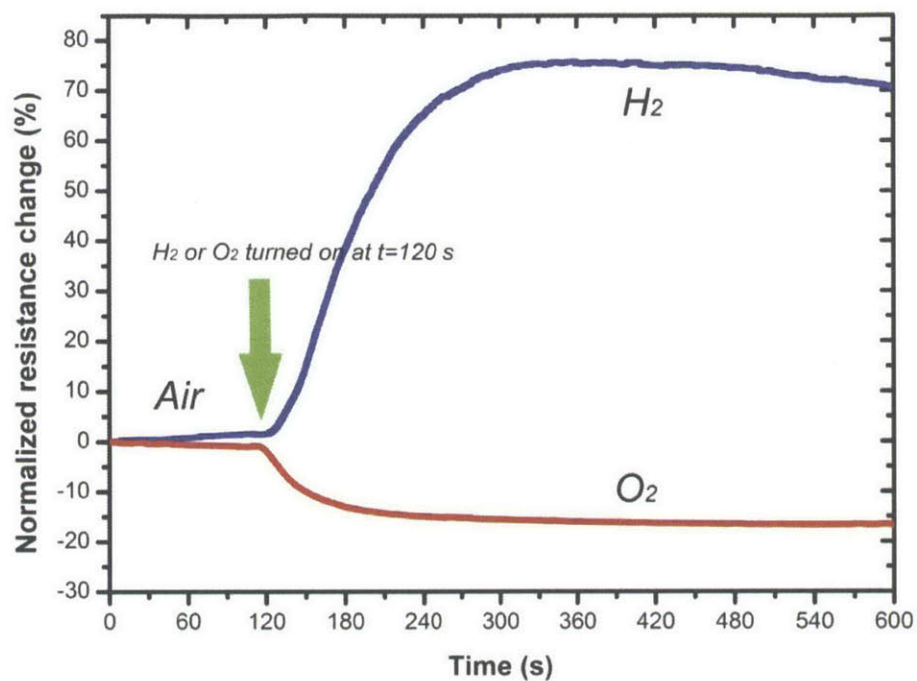


Figure 4.7 Comparison of typical electrical response to H₂ and O₂ sensing.

4.2.2 Ammonia and nitrogen dioxide detection

To evaluate the sensing capabilities of our silicon nanowire sensors, the devices were also tested when exposed to low concentrations of ammonia (NH₃) and nitrogen dioxide (NO₂). Ammonia and nitrogen dioxide are hazardous gases and common air pollutants. Ammonia contributes to several important environmental problems, including toxic effects on vegetation [83], atmospheric visibility [84] and transformation into components of PM 2.5 [85]. As for nitrogen dioxide, it is a well-known by-product from combustion or automobile exhaust emissions. It is also hazardous to the environment and human beings, especially for the formation of acid rain. Therefore the detection of these gases has important applications for pollution monitoring [86].

NH₃ and NO₂ gases at low concentrations were detected using the fabricated silicon nanowire field effect sensor devices. Initially the device was in a dry air ambient where the resistance almost did not change. At time $t=300$ s, 10 ppm (parts-per-million) NH₃ and NO₂ gases in air flowed into the tube with a flow rate of 100 sccm. The resistance of the sensor device increased (decreased) upon exposure to the NH₃

(NO₂) gas, which was similar to the H₂ (O₂) sensing, as shown in **Figure 4.8**. The different responses to 10 ppm NH₃ and NO₂ gases demonstrate the capability of the fabricated sensor to detect low concentrations of these gases in air. However, the sensing speed was much slower than the hydrogen and oxygen sensing. After 1 hour, both curves still did not reach saturation. The normalized resistance changes at $t = 1$ h for 10 ppm NH₃ and NO₂ are 33% and 15%, respectively.

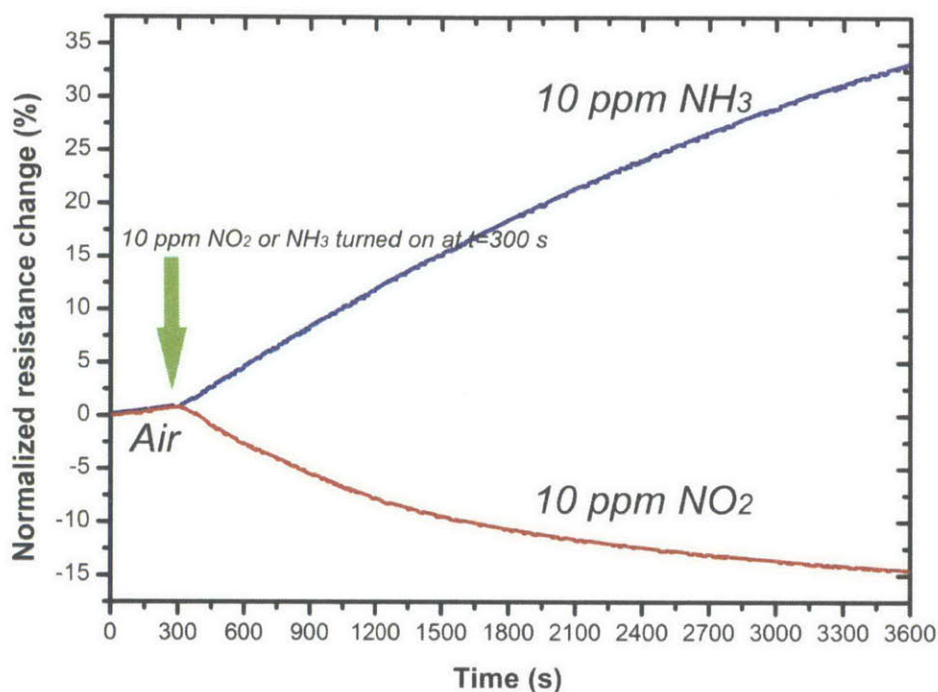


Figure 4.8 Normalized resistance change to 100 ppm NH₃ and NO₂ gases.

4.2.3 Periodic sensing results

To test the rate of recovery of the fabricated sensors, periodic gas sensing experiments were conducted for different gases.

H₂ and O₂ were first tested as target gases. **Figure 4.9** and **Figure 4.10** present typical electrical responses of the fabricated SiNW sensor to periodic exposures to pure H₂ and O₂ gases at room temperature, respectively. The sensor was in an air ambient in the first 20 minutes, then the analyte gas was turned on (with a flow rate of 100 sccm) and off periodically, with intervals of 1 hour for both the on and off status. It can be observed that both the resistance increased (decreased) instantly when the H₂ (O₂) gas was turned on for the first time and subsequently reached a saturation level. However, in the following gas-off

period, there was only a small fluctuation of resistance for H₂. For O₂, no obvious resistance changes were observed when O₂ was turned off. No signs of recovery were observed during later cyclic gas on and off periods.

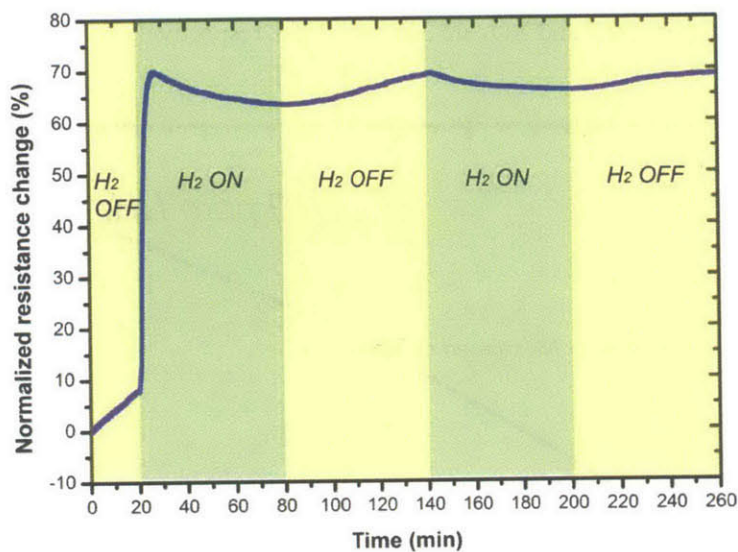


Figure 4.9 Electrical response to periodic switches of H₂ gas at room temperature; H₂ exposure interval = 1 h.

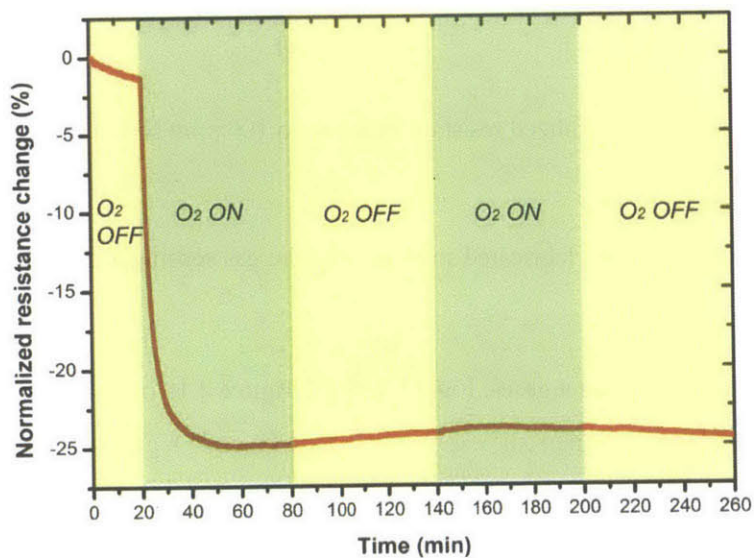


Figure 4.10 Electrical response to periodic switches of O₂ gas at room temperature; O₂ exposure interval = 1 h.

Figure 4.9 and **Figure 4.10** indicate poor recovery capabilities of the sensors. For further confirmation, similar periodic sensing tests were done for NH_3 and NO_2 gases by replacing the analyte gases to 10 ppm NH_3 and NO_2 . The electrical responses are shown in **Figure 4.11** and **Figure 4.12**. For 10 ppm NH_3 , the resistance increased slowly after exposure to NH_3 and reached saturation after about 4 hours. However, the periodic switches of analyte gas had little influence on the resistance of the device (**Figure 4.9**). Similar result was obtained for 10 ppm NO_2 . The resistance kept decreasing after exposure to the NO_2 gas for the first time.

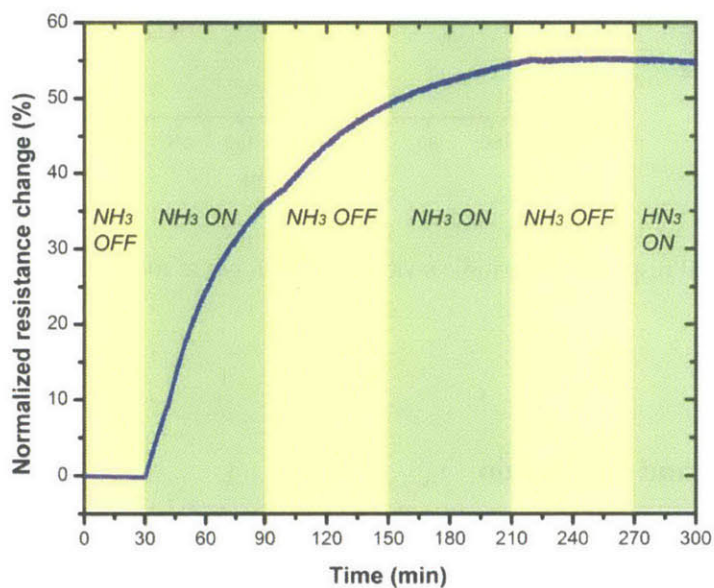


Figure 4.11 Electrical response to periodic switches of NH_3 gas at room temperature; NH_3 exposure interval = 1 h.

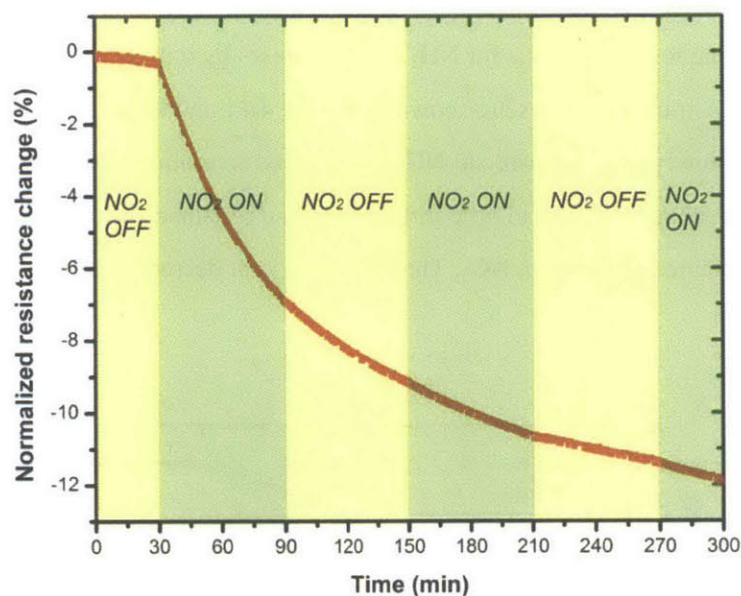


Figure 4.12 Electrical response to periodic switches of NO₂ gas at room temperature; NO₂ exposure interval = 1 h.

4.3 Discussion and conclusion

In this Chapter gas sensing results were presented using the fabricated silicon nanowire field effect gas sensors. Both reducing and oxidizing gases have been tested at room temperature.

First, the sensor successfully exhibited different resistance changes upon exposure to both oxidizing and reducing analyte gases, which have electron donating and withdrawing properties. For pure H₂ and O₂ gases, the maximum normalized resistance changes are 80% and 22%, respectively. The time for saturation is about 3-5 minutes. Good repeatability has also been demonstrated by multiple cycle sensing tests. 10 ppm NH₃ and NO₂ gases balanced in air were also tested. 33% and 15% normalized resistance changes were observed after exposure to 10 ppm NH₃ and NO₂ for 1 hour. However, the device did not reach saturation within 1 hour. Periodic sensing measurements were conducted to test the recovery capability of the sensor devices. Nevertheless, no recovery was observed when analyte gases were turned off for 1 hour.

Similar studies can be found in the literature. Han *et al.* fabricated gas sensors based on vertical silicon nanowire arrays by using an air-bridged top electrical contact [40]. **Figure 4.13** shows their sensing results for H₂ and O₂.

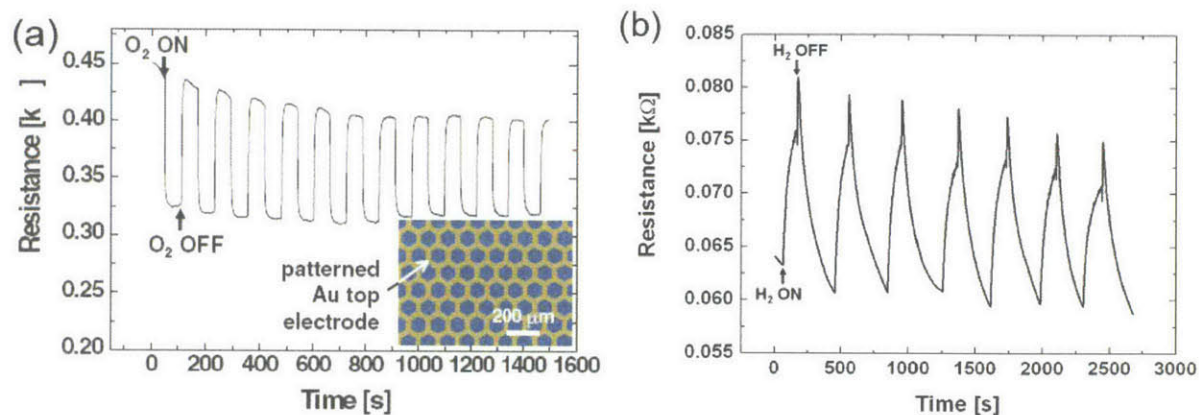


Figure 4.13 Electrical responses of vertical SiNW array-based sensor to periodic switches of (a) oxygen and (b) hydrogen gases at room temperature [40].

As shown in **Figure 4.13**, the calculated normalized resistance changes are 35% for oxygen and 20% for hydrogen. In comparison, our sensors exhibit similar sensitivity for oxygen sensing (22%) and much higher sensitivity for hydrogen sensing (80%). If the metric of sensitivity per unit chip area is used, our device shows better performance. The chip area of the sensor reported by Han *et al.* is about 10 mm × 10 mm while our device has an area of 7 mm × 7 mm. This comparison is listed below in **Table 4.1**.

Sensors	Ours	Han <i>et al.</i>
Sensitivity to H ₂	80%	20%
Sensitivity to H ₂ /chip size	163.3% /cm ²	~20% / cm ²
Sensitivity to O ₂	22%	~35%
Sensitivity to O ₂ /chip size	44.9% /cm ²	~35% /cm ²

Table 4.1 Comparison of sensitivity per unit chip area to H₂ and O₂ between the sensor presented in this thesis and that reported by Han *et al.*

It can be found that our device exhibits higher sensitivity per unit chip area for both H₂ and O₂. A careful comparison of our device and the reported work is listed in **Table 4.2**.

Sensors	Substrate doping	SiNW doping	SiNW diameter	SiNW length	SiNW density	Contacts
Presented in this thesis	p-type, heavily doped	p-type, lightly doped	250 nm	5 μm	6×10^8 NW/cm ²	Ni, top bottom, ohmic
Han, <i>et al.</i>	p-type, lightly doped	p-type, lightly doped	50 nm	8 μm	10^{10} NW/cm ²	Au, top bottom, ohmic

Table 4.2 Comparison of parameters of sensor device presented in this thesis and by Han *et al.*

As **Table 4.2** shows, the sensor device presented in this study differ from that by Han *et al.* mainly in the SiNW geometry, density and substrate doping. The smaller SiNW diameter and higher SiNW density of their sensors are supposed to contribute to higher sensitivity. Therefore, the higher sensitivity of our device for hydrogen sensing is mainly attributable to the low substrate resistance in our design. As discussed in section 3.2, the use of epitaxial Si wafer greatly decreases the substrate resistance.

A distinct difference in the behavior of our devices from the behavior reported by Han *et al.* is the response time and recovery time (defined as the time required to reach 90% of the final equilibrium value). The response time and recovery time of their device is claimed to be about 5 s. However, our device has a response time of about 3-5 min and no recovery has been observed within one hour.

The slow sensing speed and poor recovery of our device is believed to be the result of two possible reasons: the solid electrode and the nanowire temperature.

First, the solid top electrode hinders the gas adsorption and desorption processes. Because the top electrode is not porous, analyte gases can only diffuse from the periphery of the nanowire array into the closely arranged network of nanowires forest in order to interact with individual nanowires. As the diffusion distance from the top contact is ~ 700 nm (the top contact layer thickness) and ~ 2 mm from the side, this solid top electrode is supposed to significantly delays the gas adsorption and desorption process compared to a porous top electrode. This argument is supported by a study of vertical silicon nanowire gas sensor with a porous top electrode by Pehrsson *et al.* [39]. They fabricated the periodically porous top electrodes by using a nanosphere-enabled metal deposition method. Sensors with a porous top electrode and solid top electrode which were identical in all other aspects were tested and compared. The electrical responses to 500 ppb (parts-per-billion) NH_3 are shown in **Figure 4.14**.

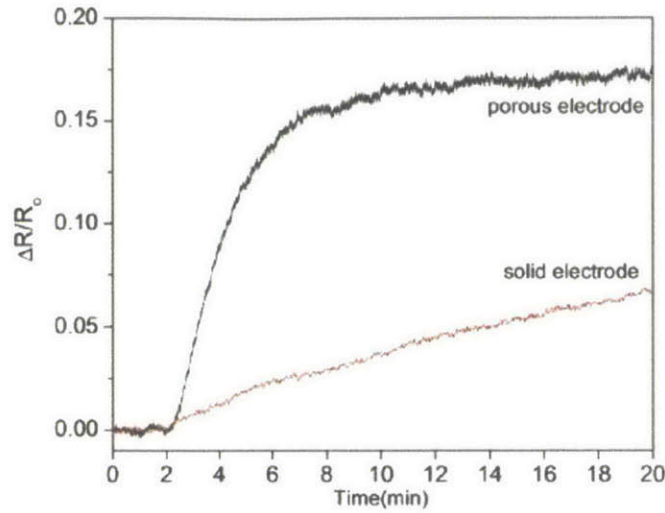


Figure 4.14 Porous top electrode sensor (black) and solid electrode sensor (red) responses to 500 ppb of NH_3 at $\sim 30\%$ RH [87].

As **Figure 4.14** shows, the sensors with a porous top electrode reached the saturation level in approximately 6 min. In comparison, the sensor with a solid electrode, which was similar to our device, required almost 1 h to reach saturation (data not shown). This difference indicates that the solid top electrode significantly delays detection response. Moreover, it is likely to be the reason that no recovery was observed after analyte gases were turned off after 1 h. Similar studies about gas desorption and recovery were also investigated by Pehrsson *et al.* [81]. It was found that even for sensors with a porous top electrode, the sensor needed 1h of clean air exposure to partially desorb the analyte from the nanowire surfaces at 40°C . This may explain why our device has poor recovery capabilities.

Another possible reason is the nanowire temperature during measurement. The Joule heating effect will heat the nanowire at a higher temperature than room temperature. In this study, the gas sensing measurement is done by applying a constant 0.1 V voltage. The power of the Joule heating is about

$$P = \frac{U^2}{R} = \frac{0.1^2}{400} = 2.5 \times 10^{-5} \text{W} = 25 \mu\text{W} \quad (4.1)$$

So the Joule heating power is very small in this study. However, if a larger voltage is applied, the heating power can be large enough to increase the temperature of the wires. The temperature has a significant influence on the response time and recovery time, which has also been demonstrated by the heating

process in the cycle tests shown in **Figure 4.4** and **Figure 4.6**. It might be possible that the gas sensing experiments reported by Han *et al.* was conducted with a higher Joule heating power therefore higher temperature of the nanowires.

The NH₃ and NO₂ sensing results can also be compared to similar studies by Pehrsson *et al.* [81]. The response to NH₃ and NO₂ at various concentrations for a vertically aligned silicon nanowire-based sensor with a porous electrode is shown in **Figure 4.15**.

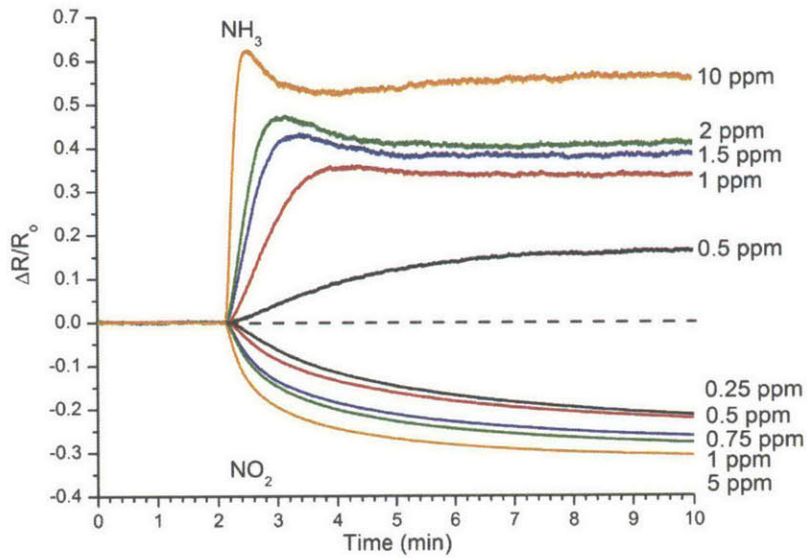


Figure 4.15 Response to ammonia and nitrogen dioxide at various concentrations for an ordered, vertically aligned silicon nanowire-based sensor with a porous electrode [81].

Their sensors reached saturation in 10 min for 10 ppm NH₃, with a normalized resistance change of 56%. Our sensing results in **Figure 4.11** shows that the normalized resistance change at saturation level is about 55%, despite the fact that it took hours for our sensor to reach saturation. If we take into account the chip size to calculate the sensitivity per unit chip area, the comparison is as shown below in **Table 4.3**.

Sensor	Sensitivity to 10 ppm NH ₃	Chip size	Sensitivity/chip size
Ours	55%	7mm×7mm	112.2% /cm ²
Pehrsson <i>et al.</i>	56%	25mm×25mm	8.95% /cm ²

Table 4.3 Comparison of sensitivity to 10 ppm ammonia and chip size of our fabricated device with that reported by Pehrsson *et al.*

By comparison, it can be found that our device exhibits much higher (about one order of magnitude higher) sensitivity per unit chip area. Although they did not test 10 ppm NO₂, it is promising that our sensor may also have larger sensitivity per unit chip area since our chip size is about 10 times smaller than theirs.

The detailed sensor parameters of our device and that reported by Pehrsson *et al.* are shown in **Table 4.4**.

Sensors	Substrate doping	SiNW doping	SiNW diameter	SiNW length	SiNW density	Contacts
Presented in this thesis	p-type, heavily doped	p-type, lightly doped	250 nm	5 μm	6×10^8 NW/cm ²	Ni, top bottom, ohmic
Pehrsson <i>et al.</i>	p-type, lightly doped	p-type, lightly doped	200 nm	4 μm	$\sim 6 \times 10^8$ NW/cm ²	Au, top bottom, ohmic

Table 4.4 Comparison of parameters of sensor device presented in this thesis and by Pehrsson *et al.*

From **Table 4.4** it can be found that a major difference is the low substrate resistance our sensor has. This is likely to be the reason for much higher sensitivity per unit chip area. High sensitivity per unit chip area is an important metric for sensors as their size is scaling down to centimeters or even millimeters. It is essential to achieve high sensitivity using minimum chip areas, especially for commercialization and miniaturization of such devices.

In summary, the various sensing experiments have demonstrated the highest sensitivity per unit chip area for H₂, O₂ and 10 ppm NH₃ gas, among other vertically aligned silicon nanowire based gas sensors in the literature. Problems of the current sensor devices lie in the slow response for detection and inability to recover without heating. These problems are likely to be caused by two possible reasons: the solid top electrode and the Joule heating effect. A porous top electrode might facilitate the gas adsorption and desorption processes. The Joule heating effect during resistance measurement can increase the temperature of the nanowires therefore accelerate the response and recovery processes.

Chapter 5 Summary and Outlook

5.1 Summary

Over the last decades, there has been a considerable amount of work on nanowire-based gas sensors to fabricate sensors with high sensitivity, selectivity, stability and sensing speed. Although planar silicon nanowire based sensors have been studied and developed extensively, there have been far less studies of sensors based on vertically aligned highly ordered nanowires. Vertically aligned silicon nanowire array based sensors are preferable for a number of reasons, including much higher utilization of sensing area, high integration density of nanowires to electrodes, etc.

In the present study, metal assisted chemical etching was used to controllably fabricate vertically aligned silicon nanowires in trenches and these wire arrays were used to fabricate field effect gas sensors. Highly ordered large-area arrays of silicon nanowires were fabricated using both nanosphere lithography and interference lithography. The fabrication of patterned silicon nanowire arrays in trenches was demonstrated using photolithography and interference lithography. The flexibility of this fabrication method makes it ideal for fabrication of nanowire structures for gas sensing applications.

The effects of various sensor parameters on sensing performance, especially sensitivity, have been analyzed. Based on this investigation, a number of design considerations have been taken into account during the design and fabrication of the sensors. A new tilted electron beam evaporation approach was employed to deposit patterned metal on the upper part of the nanowire array, to serve as the suspended top contact. Contact materials were tested and selected for ohmic contact formation, a heavily doped wafer with a lightly doped epitaxial layer was used for low serial resistance and silver epoxy was used for wire bonding. The electrical characterization results showed the sensor devices had good ohmic contacts with high repeatability.

The sensing behavior of the silicon nanowire sensor devices was tested with a gas flow system setup. Highly sensitive detection of hydrogen, oxygen and 10 ppm ammonia and nitrogen dioxide gases has been demonstrated. The sensors have exhibited the highest sensitivity per unit chip area for hydrogen, oxygen and 10 ppm NH_3 gases, among other vertically aligned silicon nanowire based gas sensors reported. However, slow response for detection and the inability of recovery remain problems for the current sensors. These problems are likely to be caused by the solid top electrode, which significantly delays the gas adsorption and desorption processes.

5.2 Future work

In this section, some future research efforts are described in order to further advance our understanding of the gas sensing process and improve the sensing performance of the gas sensors.

(a) Surface treatment of SiNWs

In this research, the sensor devices were fabricated without any further treatment or modification of the silicon nanowire surfaces. The sensing mechanism is merely based on the adsorption of electron donating or withdrawing properties of analyte gases. However, it would be very interesting to look into the surface treatment of SiNWs. Many materials are more suitable for gas sensors in terms of sensitivity and stability compared to silicon. For sensitivity, many semiconducting metal oxides (such as TiO_2 , ZnO) and other wide bandgap materials have the ability to detect extremely low concentrations of analytes [88] and can have much larger resistance changes (even orders of magnitude). In particular, TiO_2 is widely used for gas sensors, both in the form of thin films [89] or nanowires [90]. However, it is worth noting that TiO_2 coated nanowire sensors are typically operated at temperatures ranging between 200-350 °C [90].

Moreover, a very big problem for silicon is surface oxidation. In comparison, metal oxide materials do not have such problems. Therefore it is promising to deposit other materials such as TiO_2 on SiNW scaffolds using Atomic Layer Deposition (ALD). The high aspect ratio structure and high nanowire surface area per substrate area of the SiNW scaffold can be taken advantage of and the functional layer on the SiNW surfaces can offer more flexibility in choosing the sensing materials. Surface modification is also crucial for selective sensing.

(b) Improving the sensing speed and recovery capabilities

In order to improve the gas sensing speed, the top electrode can be made porous instead of a continuous suspended layer. In the existing device in this research, the top contact layer was continuous. A porous top electrode makes it easy for the analyte to directly reach the nanowires. A porous top electrode is also crucial to realize fast recovery since the gas desorption process is also significantly facilitated. The improvement can be made by using a perforated shadow mask during the tilted ebeam evaporation process. For example, a shadow mask can be designed with $100\ \mu\text{m}$ -sized holes. When this mask is used during the tilted ebeam evaporation process, a perforated metal film will be deposited onto the top of the nanowire arrays. It is very promising that this change is supposed to solve the recovery problem the current sensors have and it should also increase the sensing speed upon exposure to analyte gases.

Another approach to increase sensing speed is to pattern the silicon nanowire arrays with channels for gas flow. During the step (d) in **Figure 2.12**, the ARC nanopillars can be patterned in certain distributed areas separated by gas or liquid flow channels. This can help deliver the analyte gases much easily to the nanowire sensing areas. In this way, the response time and recovery time might be reduced significantly.

(c) Self-heating effect of silicon nanowires

In this study, the sensor was operated at room temperature with a constant DC voltage $V=0.1V$ applied for measurement. However, the adsorption and desorption of gases occur faster at an elevated temperature due to higher kinetic energy. The operational temperature can be changed by utilize the Joule heating effect of silicon nanowires. The applied voltage for measurement can be tuned to change the temperature of the silicon nanowire arrays. By increasing the sensing temperature, this self-heating effect of silicon nanowires can be used for improving the response speed and achieving fast recovery. This Joule heating effect has been utilized on a Palladium nanowire sensor to accelerate response and recovery to hydrogen gas sensing [91].

Self-heating effect can also be potentially used to selectively modify the nanowire surface by generating a localized heat to produce chemical reactions on nanowires [92]. This local surface modification can be very useful for selective sensing. For example, different nanowire areas (or channels) can be modified locally by different functional groups to achieve multiplexed detection on a single device.

List of Reference

1. Erickson, D., et al., *Nanobiosensors: optofluidic, electrical and mechanical approaches to biomolecular detection at the nanoscale*. *Microfluidics and Nanofluidics*, 2008. **4**(1-2): p. 33-52.
2. Gardner, J.W., et al., *CMOS Interfacing for Integrated Gas Sensors: A Review*. *Sensors Journal, IEEE*, 2010. **10**(12): p. 1833-1848.
3. Azad, A.M., et al., *SOLID-STATE GAS SENSORS - A REVIEW*. *Journal of the Electrochemical Society*, 1992. **139**(12): p. 3690-3704.
4. Grieshaber, D., et al., *Electrochemical Biosensors - Sensor Principles and Architectures*. *Sensors*, 2008. **8**(3): p. 1400-1458.
5. Hodgkinson, J. and R.P. Tatam, *Optical gas sensing: a review*. *Measurement Science & Technology*, 2013. **24**(1).
6. Comini, E., et al., *Stable and highly sensitive gas sensors based on semiconducting oxide nanobelts*. *Applied Physics Letters*, 2002. **81**(10): p. 1869-1871.
7. Sun, Y.-F., et al., *Metal Oxide Nanostructures and Their Gas Sensing Properties: A Review*. *Sensors*, 2012. **12**(3): p. 2610-2631.
8. Itagaki, Y., et al., *Toxic gas detection using porphyrin dispersed polymer composites*. *Sensors and Actuators B-Chemical*, 2005. **108**(1-2): p. 393-397.
9. Chen, X., et al., *Nanowire-based gas sensors*. *Sensors and Actuators B: Chemical*, 2013. **177**(0): p. 178-195.
10. Jimenez-Cadena, G., J. Riu, and F.X. Rius, *Gas sensors based on nanostructured materials*. *Analyst*, 2007. **132**(11): p. 1083-1099.
11. Anker, J.N., et al., *Biosensing with plasmonic nanosensors*. *Nature Materials*, 2008. **7**(6): p. 442-453.
12. Lee, K.-S. and M.A. El-Sayed, *Gold and silver nanoparticles in sensing and imaging: Sensitivity of plasmon response to size, shape, and metal composition*. *Journal of Physical Chemistry B*, 2006. **110**(39): p. 19220-19225.
13. You, C.-C., et al., *Detection and identification of proteins using nanoparticle-fluorescent polymer 'chemical nose' sensors*. *Nature Nanotechnology*, 2007. **2**(5): p. 318-323.
14. Benjaminsen, R.V., et al., *Evaluating Nanoparticle Sensor Design for Intracellular pH Measurements*. *ACS Nano*, 2011. **5**(7): p. 5864-5873.
15. Sadek, A.Z., et al., *Characterization of ZnO nanobelt-based gas sensor for H-2, NO2, and hydrocarbon sensing*. *IEEE Sensors Journal*, 2007. **7**(5-6): p. 919-924.

16. Fields, L.L., et al., *Room-temperature low-power hydrogen sensor based on a single tin dioxide nanobelt*. Applied Physics Letters, 2006. **88**(26).
17. Cheng, Y., et al., *Mechanism and Optimization of pH Sensing Using SnO₂ Nanobelt Field Effect Transistors*. Nano Letters, 2008. **8**(12): p. 4179-4184.
18. Wang, J.X., et al., *Hydrothermally grown oriented ZnO nanorod arrays for gas sensing applications*. Nanotechnology, 2006. **17**(19): p. 4995-4998.
19. Kabashin, A.V., et al., *Plasmonic nanorod metamaterials for biosensing*. Nature Materials, 2009. **8**(11): p. 867-871.
20. Wei, A., et al., *Enzymatic glucose biosensor based on ZnO nanorod array grown by hydrothermal decomposition*. Applied Physics Letters, 2006. **89**(12).
21. Wang, J., *Carbon-nanotube based electrochemical biosensors: A review*. Electroanalysis, 2005. **17**(1): p. 7-14.
22. Besteman, K., et al., *Enzyme-coated carbon nanotubes as single-molecule biosensors*. Nano Letters, 2003. **3**(6): p. 727-730.
23. Kong, J., M.G. Chapline, and H.J. Dai, *Functionalized carbon nanotubes for molecular hydrogen sensors*. Advanced Materials, 2001. **13**(18): p. 1384-1386.
24. Li, J., et al., *Carbon nanotube sensors for gas and organic vapor detection*. Nano Letters, 2003. **3**(7): p. 929-933.
25. Zhang, M.G., A. Smith, and W. Gorski, *Carbon nanotube-chitosan system for electrochemical sensing based on dehydrogenase enzymes*. Analytical chemistry, 2004. **76**(17): p. 5045-5050.
26. Modi, A., et al., *Miniaturized gas ionization sensors using carbon nanotubes*. Nature, 2003. **424**(6945): p. 171-174.
27. Cui, Y., et al., *Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species*. Science, 2001. **293**(5533): p. 1289.
28. Wan, Q., et al., *Fabrication and ethanol sensing characteristics of ZnO nanowire gas sensors*. Applied Physics Letters, 2004. **84**(18): p. 3654-3656.
29. Zhang, D.H., et al., *Detection of NO₂ down to ppb levels using individual and multiple In₂O₃ nanowire devices*. Nano Letters, 2004. **4**(10): p. 1919-1924.
30. Huang, Y., X.F. Duan, and C.M. Lieber, *Nanowires for integrated multicolor nanophotonics*. Small, 2005. **1**(1): p. 142-147.
31. Liu, Z. and P.C. Searson, *Single nanoporous gold nanowire sensors*. Journal of Physical Chemistry B, 2006. **110**(9): p. 4318-4322.
32. Im, Y., et al., *Investigation of a single Pd nanowire for use as a hydrogen sensor*. Small, 2006. **2**(3): p. 356-358.

33. Favier, F., et al., *Hydrogen sensors and switches from electrodeposited palladium mesowire arrays*. *Science*, 2001. **293**(5538): p. 2227-2231.
34. Comini, E. and G. Sberveglieri, *Metal oxide nanowires as chemical sensors*. *Materials Today*, 2010. **13**(7-8): p. 28-36.
35. Kolmakov, A. and M. Moskovits, *Chemical sensing and catalysis by one-dimensional metal-oxide nanostructures*. *Annual Review of Materials Research*, 2004. **34**: p. 151-180.
36. Dan, Y., et al., *Gas sensing properties of single conducting polymer nanowires and the effect of temperature*. *Nanotechnology*, 2009. **20**(43).
37. Dan, Y., et al., *Dielectrophoretically assembled polymer nanowires for gas sensing*. *Sensors and Actuators B: Chemical*, 2007. **125**(1): p. 55-59.
38. Cui, Y. and C.M. Lieber, *Functional nanoscale electronic devices assembled using silicon nanowire building blocks*. *Science*, 2001. **291**(5505): p. 851-853.
39. Hyun Jin, I., R.F. Christopher, and E.P. Pehr, *Periodically porous top electrodes on vertical nanowire arrays for highly sensitive gas detection*. *Nanotechnology*, 2011. **22**(35): p. 355501.
40. Han, H., et al., *Air-Bridged Ohmic Contact on Vertically Aligned Si Nanowire Arrays: Application to Molecule Sensors*. *Advanced Materials*, 2012. **24**(17): p. 2284-2288.
41. Offermans, P., M. Crego-Calama, and S.H. Brongersma, *Gas Detection with Vertical InAs Nanowire Arrays*. *Nano Letters*, 2010.
42. Getino, J., et al., *Environmental applications of gas sensor arrays: combustion atmospheres and contaminated soils*. *Sensors and Actuators B-Chemical*, 1999. **59**(2-3): p. 249-254.
43. Xu, Y.L., X.H. Zhou, and O.T. Sorensen, *Oxygen sensors based on semiconducting metal oxides: an overview*. *Sensors and Actuators B-Chemical*, 2000. **65**(1-3): p. 2-4.
44. Tomchenko, A.A., et al., *Semiconducting metal oxide sensor array for the selective detection of combustion gases*. *Sensors and Actuators B-Chemical*, 2003. **93**(1-3): p. 126-134.
45. Tien, L.C., et al., *Room-temperature hydrogen-selective sensing using single Pt-coated ZnO nanowires at microwatt power levels*. *Electrochemical and Solid State Letters*, 2005. **8**(9): p. G230-G232.
46. McAlpine, M.C., et al., *Highly ordered nanowire arrays on plastic substrates for ultrasensitive flexible chemical sensors*. *Nature Materials*, 2007. **6**(5): p. 379-384.
47. Wagner, R.S. and W.C. Ellis, *VAPOR-LIQUID-SOLID MECHANISM OF SINGLE CRYSTAL GROWTH (NEW METHOD GROWTH CATALYSIS FROM IMPURITY WHISKER EPITAXIAL + LARGE CRYSTALS SI E)*. *Applied Physics Letters*, 1964. **4**(5): p. 89-8.

48. Yang, P., R. Yan, and M. Fardy, *Semiconductor Nanowire: What's Next?* Nano Letters, 2010. **10**(5): p. 1529-1536.
49. Wolfsteller, A., et al., *Comparison of the top-down and bottom-up approach to fabricate nanowire-based Silicon/Germanium heterostructures.* Thin Solid Films, 2010. **518**(9): p. 2555-2561.
50. Schmidt, V., S. Senz, and U. Gosele, *Diameter-dependent growth direction of epitaxial silicon nanowires.* Nano Letters, 2005. **5**(5): p. 931-935.
51. Huang, Z., et al., *Metal - Assisted Chemical Etching of Silicon: A Review.* Advanced Materials, 2011. **23**(2): p. 285-308.
52. Wan, J., et al., *Silicon nanowire sensor for gas detection fabricated by nanoimprint on SU8/SiO₂/PMMA trilayer.* Microelectronic Engineering, 2009. **86**(4-6): p. 1238-1242.
53. Peng, K.-Q., X. Wang, and S.-T. Lee, *Gas sensing properties of single crystalline porous silicon nanowires.* Applied Physics Letters, 2009. **95**(24): p. 243112-3.
54. Joshi, R.K. and A. Kumar, *Room temperature gas detection using silicon nanowires.* Materials Today, 2011. **14**(1-2): p. 52-52.
55. Ramgir, N.S., Y. Yang, and M. Zacharias, *Nanowire-Based Sensors.* Small, 2010. **6**(16): p. 1705-1722.
56. Ng, M.-F., et al., *Theoretical investigation of silicon nanowires: Methodology, geometry, surface modification, and electrical conductivity using a multiscale approach.* Physical Review B, 2007. **76**(15): p. 155435.
57. Zanolli, Z., et al., *Gas Sensing with Au-Decorated Carbon Nanotubes.* ACS Nano, 2011. **5**(6): p. 4592-4599.
58. Nair, P.R. and M.A. Alam, *Design considerations of silicon nanowire biosensors.* Electron Devices, IEEE Transactions on, 2007. **54**(12): p. 3400-3408.
59. Patolsky, F., G. Zheng, and C.M. Lieber, *Fabrication of silicon nanowire devices for ultrasensitive, label-free, real-time detection of biological and chemical species.* Nature Protocols, 2006. **1**(4): p. 1711-1724.
60. Heo, K., et al., *Large-Scale Assembly of Silicon Nanowire Network-Based Devices Using Conventional Microfabrication Facilities.* Nano Letters, 2008. **8**(12): p. 4523-4527.
61. Tao, A., et al., *Langmuir-Blodgett silver nanowire monolayers for molecular sensing using surface-enhanced Raman spectroscopy.* Nano Letters, 2003. **3**(9): p. 1229-1233.
62. Lai, E., W. Kim, and P.D. Yang, *Vertical Nanowire Array-Based Light Emitting Diodes.* Nano Research, 2008. **1**(2): p. 123-128.
63. Xu, S., et al., *Self-powered nanowire devices.* Nat Nano, 2010. **5**(5): p. 366-373.
64. Sarathy, J., et al., *DEMONSTRATION OF PHOTOLUMINESCENCE IN NONANODIZED SILICON.* Applied Physics Letters, 1992. **60**(13): p. 1532-1534.

65. DimovaMalinovska, D., et al., *Preparation of thin porous silicon layers by stain etching*. Thin Solid Films, 1997. **297**(1-2): p. 9-12.
66. Li, X. and P.W. Bohn, *Metal-assisted chemical etching in HF/H₂O₂ produces porous silicon*. Applied Physics Letters, 2000. **77**(16): p. 2572-2574.
67. Chartier, C., S. Bastide, and C. Levy-Clement, *Metal-assisted chemical etching of silicon in HF-H₂O₂*. Electrochimica Acta, 2008. **53**(17): p. 5509-5516.
68. Huang, Z., et al., *Ordered Arrays of Vertically Aligned [110] Silicon Nanowires by Suppressing the Crystallographically Preferred <100> Etching Directions*. Nano Letters, 2009. **9**(7): p. 2519-2525.
69. Cloutier, S.G., et al., *Enhancement of radiative recombination in silicon via phonon localization and selection-rule breaking*. Advanced Materials, 2006. **18**(7): p. 841-+.
70. Huang, Z., H. Fang, and J. Zhu, *Fabrication of Silicon Nanowire Arrays with Controlled Diameter, Length, and Density*. Advanced Materials, 2007. **19**(5): p. 744-748.
71. Peng, K., et al., *Ordered silicon nanowire arrays via nanosphere lithography and metal-induced etching*. Applied Physics Letters, 2007. **90**: p. 163123.
72. Chang, S.W., et al., *Densely Packed Arrays of Ultra - High - Aspect - Ratio Silicon Nanowires Fabricated using Block - Copolymer Lithography and Metal - Assisted Etching*. Advanced Functional Materials, 2009. **19**(15): p. 2495-2500.
73. Huang, Z.P., et al., *Extended arrays of vertically aligned sub-10 nm diameter 100 Si nanowires by metal-assisted chemical etching*. Nano Letters, 2008. **8**(9): p. 3046-3051.
74. Choi, W.K., et al., *Synthesis of Silicon Nanowires and Nanofin Arrays Using Interference Lithography and Catalytic Etching*. Nano Letters, 2008. **8**(11): p. 3799-3802.
75. Chang, S.-w., *Fabrication of High Aspect Ratio Silicon Nanostructure Arrays by Metal-Assisted Etching*, in *Department of Materials Science and Engineering* 2010, Massachusetts Institute of Technology
76. Wang, S., *Fundamentals of Semiconductor Theory and Device Physics* 1989, New Jersey: Prentice Hall.
77. Brigham Young University, D.o.E.C.E. *Metal-Semiconductor Ohmic and Schottky Contacts*. Available from: <http://www.cleanroom.byu.edu/ohmic-schottky.phtml>.
78. François Léonard, A.A.T., *Electrical contacts to one- and two-dimensional nanomaterials*. Nature Nanotechnology, 2011. **6**: p. 773-783.
79. Park, J.Y., D.E. Song, and S.S. Kim, *An approach to fabricating chemical sensors based on ZnO nanorod arrays*. Nanotechnology, 2008. **19**: p. 105503.
80. Koto, M., P.W. Leu, and P.C. McIntyre, *Vertical germanium nanowire arrays in microfluidic channels for charged molecule detection*. Journal of the Electrochemical Society, 2009. **156**: p. K11.

81. Field, C.R., et al., *Vapor Detection Performance of Vertically Aligned, Ordered Arrays of Silicon Nanowires with a Porous Electrode*. Analytical chemistry, 2011.
82. Matsunaga, N., et al., *Diffusion equation-based study of thin film semiconductor gas sensor-response transient*. Sensors and Actuators B: Chemical, 2002. **83**(1–3): p. 216-221.
83. Zbieranowski, A.L. and J. Aherne, *Ambient concentrations of atmospheric ammonia, nitrogen dioxide and nitric acid in an intensive agricultural region*. Atmospheric Environment, 2013. **70**: p. 289-299.
84. Barthelmie, R.J. and S.C. Pryor, *Implications of ammonia emissions for fine aerosol formation and visibility impairment - A case study from the Lower Fraser Valley, British Columbia*. Atmospheric Environment, 1998. **32**(3): p. 345-352.
85. Behera, S.N. and M. Sharma, *Transformation of atmospheric ammonia and acid gases into components of PM2.5: an environmental chamber study*. Environmental Science and Pollution Research, 2012. **19**(4): p. 1187-1197.
86. Karmarkar, K.H. and G.G. Guilbault, *The detection of ammonia and nitrogen dioxide at the parts per billion level with coated piezoelectric crystal detectors*. Analytica Chimica Acta, 1975. **75**(1): p. 111-117.
87. In, H.J., C.R. Field, and P.E. Pehrsson, *Periodically porous top electrodes on vertical nanowire arrays for highly sensitive gas detection*. Nanotechnology, 2011. **22**: p. 355501.
88. Kim, I.-D., et al., *Ultrasensitive Chemiresistors Based on Electrospun TiO₂ Nanofibers*. Nano Letters, 2006. **6**(9): p. 2009-2013.
89. Stefan, B., G. Velichka, and R. Milka, *Characterization of reactive sputtered TiO₂ thin films for gas sensor applications*. Journal of Physics: Conference Series, 2010. **253**(1): p. 012040.
90. Tian, W.-C., et al., *Sensing Performance of Precisely Ordered TiO₂ Nanowire Gas Sensors Fabricated by Electron-Beam Lithography*. Sensors, 2013. **13**(1): p. 865-874.
91. Yang, F., D.K. Taggart, and R.M. Penner, *Joule Heating a Palladium Nanowire Sensor for Accelerated Response and Recovery to Hydrogen Gas*. Small, 2010. **6**(13): p. 1422-1429.
92. Yun, J., et al., *A self-heated silicon nanowire array: selective surface modification with catalytic nanoparticles by nanoscale Joule heating and its gas sensing applications*. Nanoscale, 2013. **5**(15): p. 6851-6856.