Low Voltage Field Emitter Arrays through Aperture Scaling

by

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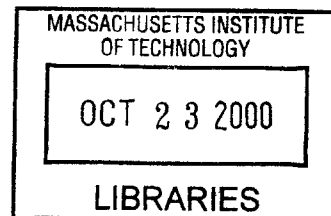Department of Electrical Engineering and Computer Science
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ABSTRACT

Field-emission arrays (FEAs) are under consideration for a variety of electronic device applications. The reduction of device turn-on and operating voltages has been a topic of intense FEA research. The purpose of this work was to explore the reduction of FEA operating voltage through scaling the gate aperture and the tip radius, with the ultimate objective of integrating FEAs with CMOS technology. This work will also examine the suitability of "classical" electron emission theories when dimensions are scaled.

We report the results of experimental and numerical simulation studies of the scaling of field emitter array (FEA) gate apertures to 100 nm and below. Electrostatic simulation indicates that by scaling the gate aperture, it is possible to fabricate devices that will support flat panel display applications at a gate voltage of 15 V.

We demonstrated 100-nm-gate aperture molybdenum FEAs that turned on at gate voltages as low as 12 V and achieved a current density of 10 $\mu A/cm^2$ at 17 V. It was possible to modulate the emission current density of the molybdenum devices by three orders of magnitude with a gate voltage swing of 5 V. The concept of device scaling was then applied to a silicon system where ultra small field emitters were fabricated, using oxidation sharpening, at a 200 nm period with gate apertures as small as 70 nm.

We demonstrated 70-nm-gate aperture silicon FEAs that turned on at gate voltages as low as 10 V and achieved emission currents of 1 μA at V_g of 13 V which represents an array current density of approximately 10,000 $\mu A/cm^2$. Currents as high as 30 μA were measured at V_g of 21 V. Transmission electron microscopy (TEM) of the tips verified that the tip radii have a lognormal distribution with a mean radius of 4.5 nm. The measured tip radii are consistent with the electrical characterization of the devices.

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1 INTRODUCTION

1.1 BACKGROUND

As technology in the areas of computers, communications and information systems advances there is an increased interest in flat panel displays for portable applications. In many cases, such as the laptop computer, it is the display requirements that are a major driver for the system. In present day laptops almost half of the power budget is allocated for display operation. The power consumed by the display, especially in portable systems, is attracting increasing attention and has created a need to develop a high efficiency, low cost and lightweight display technology.

At present, the Active-Matrix Liquid-Crystal Display (AMLCD) is the dominant technology used for almost all-portable system applications. Although AMLCDs are a lightweight technology, they lack high efficiency [1]. This is due to the fundamental nature of the transmissive LCD: It is a light valve that is only able to transmit at most 15% (5% for color) of the backlight through multiple layers, diffuser, polarizer, filters, and liquid crystal, each reducing the amount of light to pass [2]. An emissive display such as a Cathode Ray Tube (CRT) provides higher spot brightness and higher luminous efficiency; however, it is bulky and dissipates substantial power in deflector electrodes and filament making it unsuitable for low power applications. Furthermore, the screen brightness and efficiency is limited by the sequential addressing scheme. An ideal display would combine the physical characteristics of the LCD (thin, lightweight, matrix addressable) with the display properties of the CRT (high luminous efficiency, high spot brightness, large viewing angle).

Field Emitter Arrays (FEA) can provide a matrix-addressable flat electron source with the size and weight characteristics of a LCD display. A flat display made with this matrix addressable

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electron source would have the benefits of an emissive display, such as high brightness and higher efficiency, without the bulky package [3].

Significant reduction in field emitter operating voltages occurred in the last few years. Early field emitters made of etched Molybdenum wires operated at voltages from 1,000 – 30,000 V [4]. Spindt *et al.* of SRI reported field emission arrays with gate apertures of 1 μm that operated in the range of 100 - 300 V in 1976 [4]. The advances in the thin film technology that were being developed for the semiconductor industry enabled fabrication of an annular gate electrode that is in close proximity to the emitting tip. The reduction in the operating voltage was primarily due to the reduction in size of the devices. In 1993 arrays of field emitters fabricated at MIT Lincoln Laboratory with gate apertures of 160 nm operated in the range of 20 - 30 V [5]. Again, this improvement in performance was attributed to the reduction in size. Further advances in lithography, thin film deposition and surface micro-machining that have reduced the critical dimensions of semiconductor devices to about 0.1 μm, have enabled the fabrication of high current density electron sources operating at lower gate voltages.

The use of a field emitter array, (FEA), as a two dimensional matrix addressable electron source in a CRT like architecture will produce a display that takes advantage of the benefits of an emissive display such as a CRT in a package with a size and weight of an LCD (Figure 1). Further reduction in the operating voltage of the FEA to 10 – 15 volts will enable the control of the display's electron source by standard MOSFET drivers.

1.2 PROBLEM STATEMENT

The performance of a field emission device is determined by the ability of electrons to tunnel through the barrier at the emitter's surface. The important parameters are the height and width of

the barrier at the surface. The emission current density depends on these two parameters. The width of this barrier is determined by the surface electric field and the height is related to the materials workfunction. The current density is modulated by an applied voltage that changes the surface electric field. Simple electrostatics relate the surface field to the applied voltage and a device's geometry [6]. Theory and past work predict an improvement in device performance as the devices are scaled down in size [4,5] due to increased field enhancement and a reduction in the barrier width. Using standard materials with workfunctions of 4 – 5 volts, the size regime necessary to fabricate low voltage field emitter arrays (LV-FEAs) is below 160-nm gate aperture demonstrated by Lincoln Laboratory. FEAs with apertures at or below 100 nm at high packing densities (200-nm tip-to-tip spacing) need to be investigated through both simulation and experiments to determine if they can operate at low gate voltages.
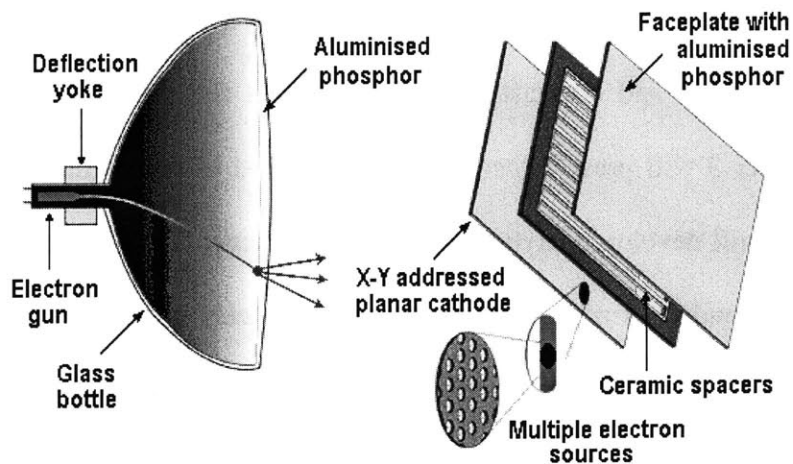
Figure 1: Comparison of CRT and a FED [7].
The principle of operation behind both the CRT and FED are similar. Electrons are emitted into a vacuum and accelerated to a phosphor screen to give off light. The FED uses a flat 2D array of electron sources instead of the single electron source of the CRT.

1.3 OBJECTIVES AND TECHNICAL APPROACH

The main objective of this work was to demonstrate low voltage FEAs that can operate at gate voltages of ~15V by taking advantage of nano-scale device geometries and high cone packing densities. Numerical modeling was used to explore the feasibility and to confirm the effects of device scaling. In order to achieve the necessary patterning, interferometric lithography was explored as a way to fabricate periodic arrays of 100 nm structures with 200-nm period. Two fabrication technologies incorporating interferometric lithography were developed for making the devices using; (a) a Spindt cone technique and (b) a silicon oxidation sharpening technique. Device physical structure was extensively analyzed followed by a correlation of device characteristics with structural parameters.

1.4 THESIS ORGANIZATION

Chapter 2 of this work will introduce the field emission display and other applications of FEAs. The chapter will compare and contrast the field emission flat panel display with competing technologies. Chapter 3 will present theoretical background of field emission from metals and semiconductors and will develop analytical models for devices. The analytical device models in Chapter 3 will be extended to more realistic device geometry through numerical modeling in Chapter 4. The results of numerical models of field emission devices will be presented. The device models and simulations presented provided guidance for developing processes to fabricate devices presented in both Chapter 5 and Chapter 6. It also provided the analytical framework for interpretation of device results. Chapter 5 presents the experimental results for a Mo cone field emission device with 100 nm gate aperture and 200-nm period. The devices were fabricated using interferometric lithography (IL) and the Spindt process. Chapter 6 presents the experimental results for a silicon cone field emission device with 100 nm gate apertures and 200-

nm period. The devices were fabricated using IL, isotropic silicon etch, oxidation sharpening, and chemical mechanical polishing (CMP).

Based on the results and analysis performed in Chapters 5 and 6, Chapter 7 will present the summary and conclusions of this work. Appendices contain more detailed processing information, background on some of the numerical work and software routines from the electrostatic simulation.

2 FIELD EMISSION DISPLAYS

There are many applications that rely on the extraction of electrons into a vacuum to perform some function. Although we have been able to do this for almost a century, the ability to control the emission, from a device at room temperature using a low power signal would enable additional applications. Because of their ability to provide a pre-bunched electron source, field emitter arrays have been considered as a cold cathode replacement in traveling wave tubes [8, 9]. When current-density-modulated at high frequencies, FEAs become the basis for new architectures of RF sources such as inductive output amplifiers [10]. FEAs are also under consideration for such applications as electric propulsion [11], pressure sensors [12], mass spectrometry [13, 14], and electronic cooling [15]. Presently, the most predominant application for FEAs is the field emission display, FED.

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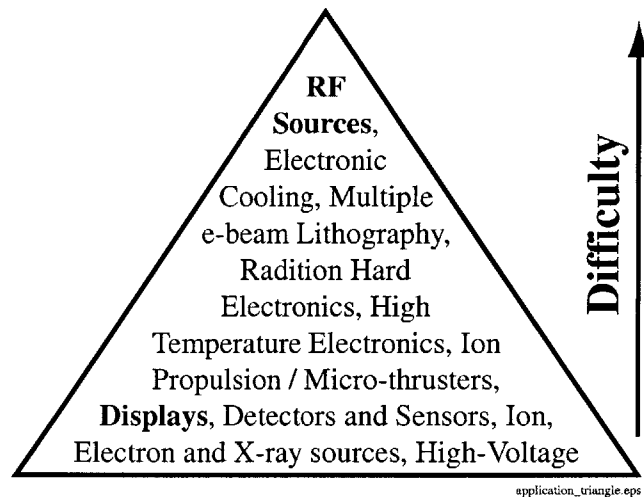
Figure 2: Applications for Gated Electron Field Emitters
The difficulty associated with using a field emitter as an electron source in an application could relate to such requirements as frequency and current density.

This chapter will introduce the FED by comparing and contrasting it to the CRT. The remainder of the chapter will focus on the use of FEAs in flat panel display applications and some of the

competing technologies. The final section to this chapter will investigate how the performance of an FED could be affected by the ability to operate FEAs at low gate voltages.

2.1 FIELD EMISSION DISPLAY AND THE CATHODE RAY TUBE

The cathode ray tube (CRT) is the major component in most present day televisions and computer monitors. The CRT is a large vacuum envelope with a single thermionic emission source. Electrons are 'boiled' off of the emitter and accelerated to the phosphor screen where they cause the phosphor to luminesce. A single electron beam is rastered over the entire screen by magnetic coils or electrostatic deflection plates and steering electronics. The high-energy electrons excite phosphors in a process referred to as Cathodeluminescense (CL). In CL, a high-energy electron excites the wide bandgap semiconductor host and generates electrons and holes. Eventually excitons are formed in the phosphor and transfer their energy to an activator ion, which is then excited to emit light [16]. CL has many advantages for display applications:

- High brightness
- High dynamic range in brightness (nonlinear voltage response)
- Full color
- Wide viewing angle
- High spatial resolution

The major drawback in CRTs is the sheer size and weight. As displays get larger a proportionally larger tube (in depth also), larger deflection components, and larger magnetic deflection coils are needed. The electron source is located far from the screen because there is only a finite amount of energy available to deflect the electron through a large angle. Another drawback is the sequential drive mechanism that does not translate the high spot brightness into high average screen brightness. Arrays of field emitters on the other hand could provide an

electron source in close proximity to the phosphor screen. Figure 3 is a schematic diagram of a typical field emission flat panel display (FED). It is essentially a 'flat' CRT.
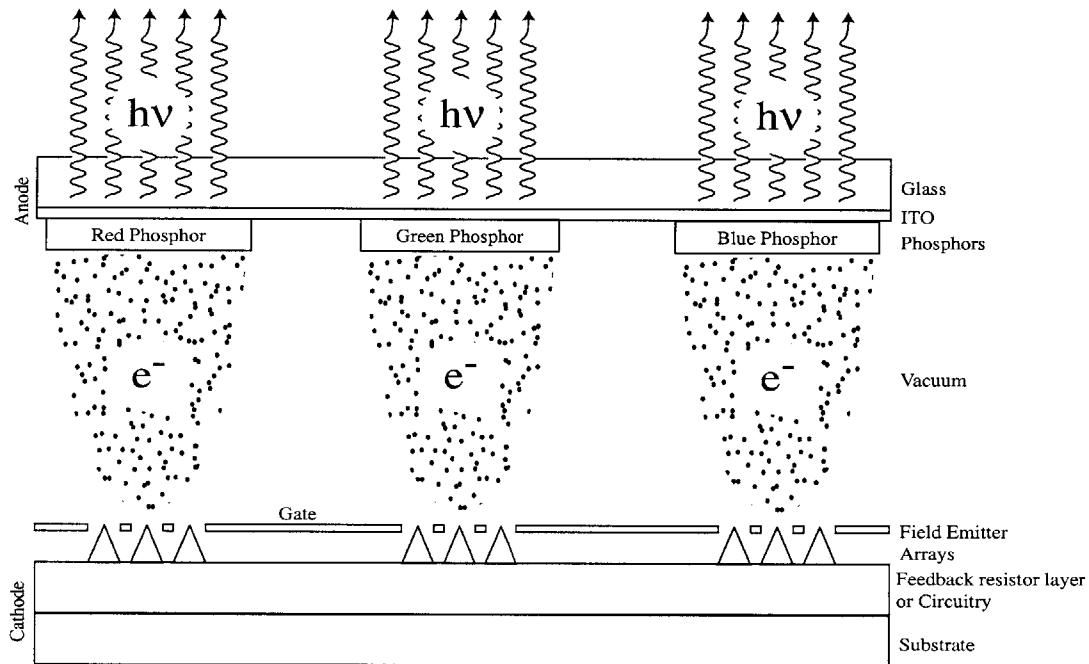
Figure 3: Concept for a Field Emission Display, (FED)
The FED is made up of a substrate (cathode) which holds a two dimensional matrix addressable array of field emitters and underlying control circuitry. A vacuum envelope over which electrons are accelerated by the anode potential separates the cathode from the anode. The anode is glass faceplate coated with indium tin oxide (ITO) and phosphors. The electrons strike the phosphors and give off light.

The FED is composed of a glass faceplate coated with a layer of indium tin oxide (transparent conductor) and phosphors. Similar to a television screen, the electrons are accelerated to the faceplate across the vacuum region. Unlike the CRT, the separation between the base-plate to the faceplate is only 1 – 2 mm. The base-plate is made up of the field emission arrays on a thin substrate. In contrast to the CRT, FEDs have arrays of electron emitters for each pixel of phosphors on the faceplate. The ability to matrix address and control the individual arrays eliminates the need for deflection coils found in CRTs. FEDs have been demonstrated by both

Candescent [17] and Pixtech [18]. Recently displays over 12" have been delivered by Pixtech for use by the U.S. Army as part of a DARPA development award.

Additionally by driving the display in a row-addressing scheme, an equivalent screen brightness can be achieved for a factor of ~ 1000 decrease in spot brightness (assuming a 1024 x 1280 pixel display). A 'smart' architecture, where each pixel has an embedded memory and is only addressed when necessary, would further reduce the spot brightness. These advances would allow phosphors to be operated more efficiently (avoiding saturation) and could lead to extended lifetimes. This control of the electron source could be accomplished through driver electronics located in the substrate underneath the array.

2.2 COMPETING DISPLAY TECHNOLOGIES

An emissive display with a field emission electron source would provide the excellent display attributes of a CRT with the size and weight benefit of other flat panel displays. A review of the current state of these other displays has served as motivation to pursue the field-emission display [19, 20] (FED).

2.2.1 Active Matrix Liquid Crystal Display (AMLCD)

AMLCDs are based on the 'light pipe' scheme and are presently the dominant flat panel display technology. Light from a uniform, well-controlled source is passed through multiple layers including polarizers, filters, and the liquid crystal layers [21]. The intensity of the light allowed through at any particular location (pixel) is based on the rotational angle of the liquid crystals. Active matrix addressing places a switch (transistor) at each pixel of the LCD to control the charging of a pixel capacitor to a voltage corresponding to the desired video signal for that pixel. This provides an improvement over the passive addressing by increasing the number lines that

can be addressed, and increasing the number of levels of gray scale [22]. Although LCDs are

driven at low voltages of 5 – 20 V [23], they still suffer from low efficiency due to the multiple

layers the light must pass through, poor viewing angle, sensitivity to temperature, and the

dependence on a very uniform flat light source. Some of these deficiencies are being addressed

in research. Presently, the screen size of AMLCDs is increasing and this technology that was

solely associated with the notebook computers is finding it's way onto the desktop.
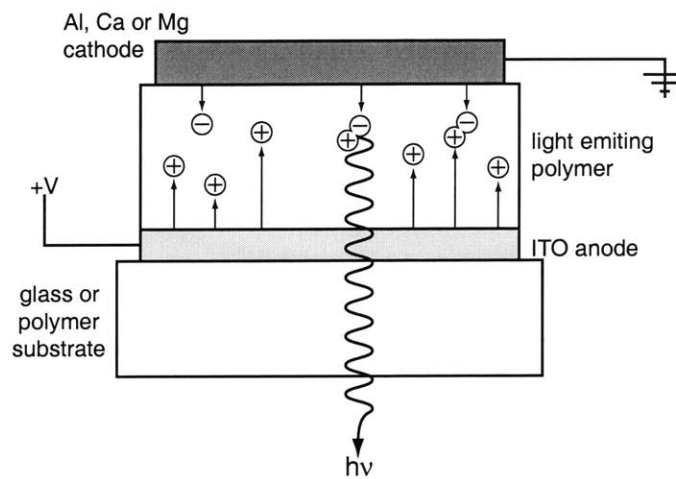
Figure 4: Schematic of a simple Organic Light Emitting Diode
A simple OLED is made up of an organic emissive layer sandwiched between two conducting contacts. A small potential (typically a few volts) across the organic layer results in charge being injected and recombining to give off light.

2.2.2 Active Matrix Organic Electroluminescence Displays (AMOLED)

An organic electroluminescent display consists of organic light emitting diodes which are made

up of an organic emitting layer sandwiched between two conducting layers [24, 25, 26]. Figure

4 shows a typical configuration where the first contact to the emissive layer is made using

indium tin oxide (ITO) as a conductor supported by a glass substrate. In addition to being a good

hole injector for a variety of emissive layers, the ITO is transparent and allows the light

generated in the emissive layers to escape. The second contact to the emissive layers needs to be

a good electron injector and is typically a low workfunction metal such as calcium or magnesium. Lifetime stability of OLEDs is under investigation due to the reactivity of these electron injection layers that can lead to degradation of the device.

In addition to having good emissive display qualities, OLEDs can be fabricated as transparent and flexible displays. This may enable new use of FPDs that is not achievable through other technologies.

Active Matrix Organic Electroluminescence Displays are being pursued as a way to achieve a high performance full color display [27] and to avoid operating the OLED at high currents necessary to achieve a screen brightness required in a passive matrix scheme. Even in an active matrix scheme, OLEDs still require high drive currents and hence high performance TFTs. The move toward polysilicon-TFTs [28] instead of amorphous-silicon TFTs was due to the higher mobility required to provide the high drive currents for the OLED [29].

2.2.3   Plasma Display Panels (PDP)

PDPs have a structure similar to an LCD. PDPs are based on a sandwich structure made up of two flat glass plates with a gas medium in between as shown in Figure 5. The two plates are patterned with conductors (one side transparent) for x-y addressability. In operation, PDPs use a high voltage to cause the breakdown of the gas to achieve photoluminescence from a phosphor [30]. This breakdown also provides a non-linear response to voltage. In addition to high voltage driver requirements (150 – 200 V), PDPs have difficulty obtaining adequate brightness and the omni-directional emission of light leading to cross-talk between pixels [23]. Additionally the energy consumed by, and the cost of the drive electronics are problems.
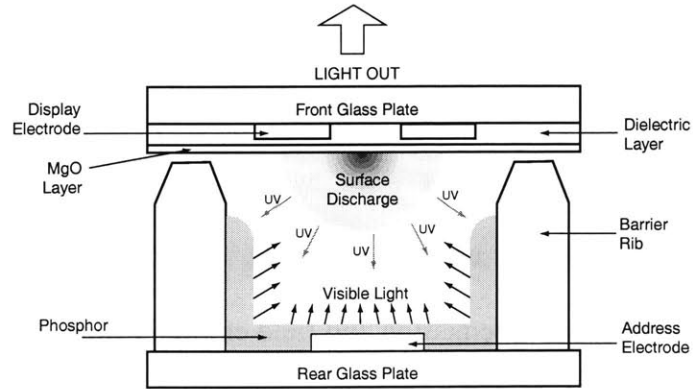
Figure 5: Pixel of a Plasma Display
Ultraviolet radiation from the plasma discharge activate the phosphor to emit light

2.3 ALTERNATIVE ELECTRON SOURCES FOR CATHODELUMINESCENCE

As alternatives to field emission from standard materials such a molybdenum and silicon, there has been a myriad of other electron sources being developed. Most of these approaches have focused on reducing the surface barrier to electron emission in order to improve cathode performance. These efforts have been motivated by the need to reduce cost by avoiding high-resolution lithography typically required by field emission. As opposed to reducing the width of the barrier at the surface, a reduction in the barrier height can be achieved by using a material with a low workfunction. The high surface electric field normally associated with a sharp cone or edge is not necessary to achieve emission from these materials. Research is being done on alternative materials to reduce the height of the barrier. However, most low workfunction materials oxidize easily and, thus, require very good vacuum packaging if stable device performance is required.

Thin films of diamond and diamond-like carbon [31] have been investigated as field emission sources. They have exhibited large emission currents at low electric fields; however the observed low-voltage field emission of these thin films is not clearly understood [32]. Literature

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has shown variations in the emission properties based on the structural nature of the films [33]. The key to emission from diamond may be related to the sharply faceted surface as opposed to a drastically lower work function. Recent work by Bandis, et al, suggest that diamond and diamond-like carbon do not have low workfunction [34]. They measured the energy distribution of electrons from simultaneous photoemission and field emission from a diamond surface. They showed that the workfunction is about 4.8 eV. They also showed that the photoemission is from the conduction band while the field emission is from the valence band. They concluded that field emission is from faceted surfaces or surface asperties. Gronig, et al, reported similar results for diamond-like carbon [35].

Similarly, wide-band-gap semiconductors [36, 37] are another candidate for an electron emission source by using band-gap engineering. Multiple layer devices can achieve negative electron affinity by injecting electrons from the conduction band of a wide bandgap material through a lower workfunction material into vacuum. Electron emission from planar cold cathodes has also been proposed through the use of an ultrathin wide-band-gap n-type semiconductor (UTSC) [38]. These devices exhibit electron emission in fields of ~ 50V/μm in a two-step mechanism: 1) injection of electrons from the metal to the UTSC through the Schottky junction, followed by, 2) electron emission from the UTSC under the control of the external electric field. The applied electric field and band bending in the UTSC lowers the emission barrier to allow electrons through or over it.

Even though there is a desire to achieve emission from planar films, there are cases where diamond films and wide-band-gap semiconductor films are either coated [39] onto or formed into cone shapes [40].

Because of their unique electrical and structural properties, nanotubes have also been considered as an electron source for cathodeluminescent applications [41]. Due to the difficulty in growing or placing a nanotube in a specific location, most nanotube devices are usually coated with a suspension of nanotubes. This makes it difficult to fabricate a three-terminal device. While emission is reported at low average fields, the device geometry results in high fields at the tip leading to significant electron emission [42].

Most of these technologies avoid the use of high-resolution lithography by taking advantage of the natural shape of the material (i.e. nanotube) or the low workfunction of the material. In many cases these devices are two terminal devices (i.e. diodes) which places significant limitation on the type of device applications. For example the use of a diode structure will not allow for independent control of luminous efficiency and brightness in a display.

2.4 CHALLENGES TO THE FIELD EMISSION DISPLAY

Although the conceptual design presented for the FED seems to address many display application issues such as brightness, efficiency etc, there are some challenges that need to be addressed before the successful integration of FEAs into an FED. A portable flat display needs to have high luminous efficiency (no wasted power in electronics), high brightness with good color qualities (use of high voltage phosphors), high resolution (small pixel size), and a long lifetime. These four areas are interrelated and discussed below:

2.4.1 High Gate Voltage

The high gate voltage of field emitters makes it difficult to create low cost CMOS driver electronics that are compatible with field emitters. Besides the difficulty in switching the high voltage, the power dissipated in these driver electronics is wasted when considering that it

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doesn't contribute to the light out of the display. This work will concentrate on reducing the operating gate voltage of the FEA. The implications of this reduction will be addressed in the following section.

2.4.2   Packaging and Spacer Technology

The second difficulty relates specifically to display package's ability to maintain vacuum [43] and for the manufacturing process to quickly achieve high vacuum from a very thin volume. In addition to the contamination of the emitter array and subsequent degradation in performance, the loss of vacuum can contribute to breakdown across the spacers that separate the faceplate from the base-plate. The vacuum spacers physically support the faceplate, but also provide electrical isolation to the large potential difference; (contamination and surface roughness on the spacers can lead to breakdown). The spacers are also affected by the drive to reduce the space between the cathode and anode to take advantage of proximity focusing and eliminate pixel crosstalk [44].

2.4.3   High Voltage Phosphor / Low Voltage Phosphor

The choice between resolution and luminous efficiency is a key trade-off in display design. In order to achieve a high-resolution display, proximity focusing is often used. This simple focusing scheme takes advantage of a small cathode anode spacing to minimize the amount of divergence of the electron beam before it reaches the anode. This small cathode to anode spacing will not allow the use of high voltage CRT phosphors that require anode potentials of 10,000 – 20,000 volts. Low voltage phosphors that operate at 500-1000 volts are used. Low voltage phosphors that are typically used for in a VFD show poor color properties and low luminous efficiency. Because of the low luminous efficiency, they must be operated at higher currents, which leads to shorter phosphor lifetimes. High voltage phosphors that are typically

used in CRTs have excellent color gamut, and require lower currents due to their high luminous efficiency. The high luminous efficiency is related to the high anode voltage required because high-energy electrons achieve a greater penetration depth, avoiding non-radiative recombination at the surface of the phosphor (typical of a low voltage phosphor). Table 1 compares the two phosphors and outlines the trade-off between luminous efficiency with HV phosphors, and display resolution associated with proximity focusing and low voltage phosphors.

Table 1: Comparison of High and Low Voltage Phosphors

Low Voltage Phosphors	High Voltage Phosphors
• High resolution (proximity focusing)	• Low resolution (due to anode spacing)
• Poor Color	• Excellent Color Gamut
• VFD Phosphors	• CRT Phosphors
• High current necessary to achieve brightness	• Low current
• Short lifetime due to coloumbic aging	• Long lifetime.
• Low Luminous Efficiency due to shallow electron penetration and non-radiative recombination at the surface.	• High Luminous Efficiency due to deep electron penetration

This trade off between luminous efficiency and resolution for the FED can also be addressed by including a focusing scheme that adds complexity to the display design.

2.5 SCALED / LOW VOLTAGE FIELD EMITTER ARRAY IMPLICATIONS

Although all the issues presented above need to be addressed to fully implement the FED, this work concentrates on the low gate voltage operation of a FEA. There are many respects in which a low voltage FEA would improve the overall performance of the FED. Areas from integration with MOSFETs to device reliability could all be effected.

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2.5.1 Standard Drivers

The previously described implementation of FEAs for a display application would allow for the possibility of control electronics to be implemented in standard CMOS logic which would reduce design costs. Present knowledge base for low power electronics and the availability of similar LCD driver electronics (operating at 5 – 20V) would reduce driver cost [23]. A standard CMOS process can be implemented easily in a fabrication process line.

2.5.2 Energy Storage in the Gate

The gate to cathode structure of the FEA resembles a capacitor. The energy stored in that gate is:

$$E = \frac{1}{2} C V_g^2$$

where C is the capacitance between the gate and cathode, and V_g is the gate voltage. The lower voltage will increase burnout resistance, since far less energy is stored in the gate. [5]

2.5.3 Addressing Electronics

Logic circuitry and driver electronics are being designed to operate at lower voltages. This will reduce the dynamic power dissipation in the display driver circuits. The power dissipated is:

$$E = C V_g^2 f$$

where f is the switching frequency. This will have greater implications as display pixel matrix increase. This power dissipation by the drivers (as opposed to the energy acquired by the electrons going to the phosphor screen) can not be converted to light and therefore is detrimental to the overall efficiency of the display.

2.5.4 High Frequency Operation

The frequency at which a field emission electron source can be operated is limited by the cutoff frequency defined by:

$$f_t = \frac{g_m}{2\pi C_g}$$

where g_m is the transconductance ($\Delta I_a/\Delta V_g$, rate of change of anode current with respect to the gate voltage) and C_g is the capacitance of the device which is attributed to the gate to cathode capacitance of a typical cone type field emitter array [45]. If the device is uniformly scaled the gate capacitance will increase due to a reduced gate to cathode spacing. The increase packing density will cause the transconductance to increase as the square of the scaling, resulting in an overall increase in the cutoff frequency [5].

2.5.5 MOSFET driven FEAs

The reduction in operating voltage would allow the integration of MOSFETs and FEAs on the same substrate. This would enable the co-fabrication of CMOS logic, memory and FEAs on a single crystal silicon substrate. An advantage of such a technology is the integration of small displays with other electronic circuits to form "systems-on-a-chip". Another advantage of this technology is the reduction of the massive wire bonding effort typically required for high definition matrix addressable displays.

3 ELECTRON EMISSION

This chapter will introduce some of the basic models that will be used to conceptualize the physics used to describe electron emission from a material. Both metals and semiconductors will be described by models, the former as a free gas of electrons confined by a potential barrier, the latter as a similar free electron gas, but with two levels that are lightly degenerate. To complete these models when considering electron emission, the concept of Schottky barrier lowering (image potential) will also be introduced in this chapter.
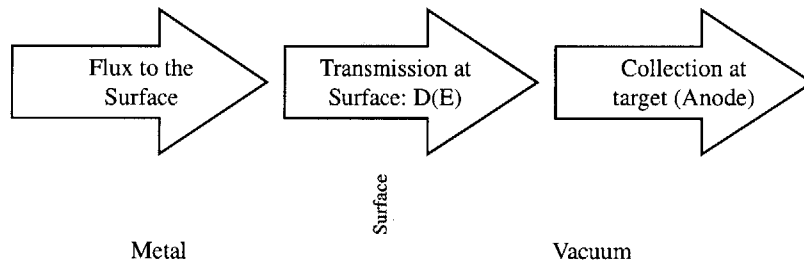
Figure 6: Electron Emission from a Metal
This general scenario shows that the emission of an electron from a metal can be broken down into electrons incident on the surface, transmission through or over the surface barrier and then movement of the electrons in vacuum.

A general description of electron emission from a conducting material, (metals and semiconductors), into vacuum is shown in Figure 6. In this picture of electron emission, there is a flux of electrons to the surface of the material followed by a transmission of these electrons through or over the surface barrier and finally the movement of the electrons from the surface once they are out in vacuum. In this work we are mainly concerned with the first two parts and will not consider in detail the action of the electrons once they are in vacuum.

The emission current density is the product of the incident flux, the transmission probability and the occupational probability of the state. For a 1D barrier, V=V(x), the emitted current density is found by integrating over all electron energies the product of the equilibrium flux of electrons incident on the surface and the probability that an electron penetrates the barrier as:

$$j = e \int_0^\infty D(E_x)N(E_x)dE_x \text{ amps/cm}^2$$

where $D(E_x)$ is the transmission probability at normal energy E_x, and $N(E_x)$ is the supply function comprised of the available electron states (giving energy dependence) and the occupation of those states as per the Fermi function (giving the temperature dependence).

$$N(E_x) = (2s+1)\frac{2\pi m k_B T}{h^3} \cdot \ln\left(1 + \exp\left[\frac{E_F - E_x}{k_B T}\right]\right)$$

where s is the electron spin, (see Appendix D).

The transmission function $D(E_x)$ must take into account the electron classically overcoming the barrier at the surface and the possibility of quantum mechanically tunneling through the barrier.

The actions of the electron in vacuum (labeled '*Collection at target (Anode)*' in Figure 6) will be based on the emitted electron energy and forces that act on the electron such as electric fields. Once the electrons are in vacuum, they can be accelerated, focused, bunched, or manipulated based on the application of interest.

3.1 THERMIONIC EMISSION

When considering thermionic emission, the focus is on the supply function. The material is heated and the electrons are thermally excited to higher energy states. The spread in the Fermi

function translates to there being a probability that electrons right below the Fermi level being moved up to occupy higher energy states. The barrier at the surface is assumed to be an infinitely wide step of height ϕ (workfunction) above the Fermi level as shown in the one-dimensional model of a metal Figure 7.
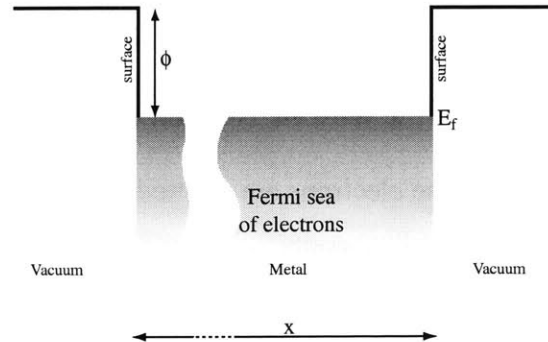
Figure 7: One-dimensional model of metal surface
A metal being modeled as a well of states, filled to the Fermi level E_f at $0\,^\circ K$. E_f is ϕ eV below the vacuum level, which is represented by the top of the well. Electrons at the surface in states above the vacuum level are free to escape the material into vacuum.

The barrier shown in Figure 7 is for no applied field on the surface. This is a good approximation for typical thermionic emission. Transmission from the material is completely classical because there is no quantum mechanical transmission through an infinitely thick barrier. Electrons at the surface with energies above the vacuum level are free to escape the material into vacuum. The transmission probability is:

$$D(E,F) = 1 \qquad\qquad E >= E_F + \phi$$
$$D(E,F) = 0 \qquad\qquad E < E_F + \phi.$$

where $F = 0$ when there is no applied field. Figure 8 shows the supply function of electrons incident on the surface for a variety of temperatures. Thermionic emission current density can be calculated by integrating $N(E,T)$ over energies above $E_F + \phi$. The current density can be shown to be: [46]

$$i = \frac{4\pi m e k_B^2}{h^3} T^2 e^{-\phi/kT} \text{ amp/cm}^2,$$

where the first parameters are grouped into Richardson's Constant [47]:

$$\frac{4\pi m e k_B^2}{h^3} \approx 120 \frac{Amps}{cm^2 K^2}.$$

As shown in Figure 8, high temperatures are required to achieve thermionic emission, (For a metal with a work function of 4.5 V, T must be between 1500 and 2000 K to get appreciable emission. For thermionic emission the electrons are emitted at energies above the vacuum level.
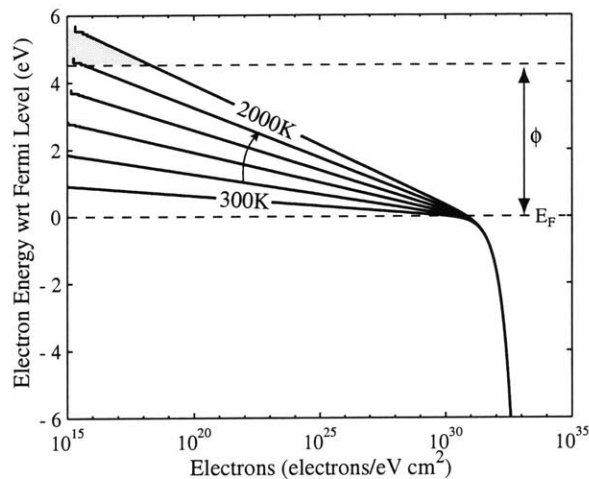
Figure 8: Electron supply function to the surface of a metal
At high temperatures the electrons will occupy states above the vacuum level (as shown in the shaded region. This example is based on a metal with a workfunction of 4.5 eV.

3.2 PHOTO-EMISSION

Photo-emission is similar to thermionic emission in that electrons acquire energy to overcome the barrier. In photo-emission a photon (with energy hv) interacts with an electron at the surface leading to the absorption of the energy of the photon by the electron. If the photon imparts enough energy to the electron, sufficient to overcome the barrier at the surface, the electron can

escape the material. Similar to thermionic emission, it is assumed that the transmission probability is 0 for electron with energy below $E_f + \phi$, and 1 for energies above $E_f + \phi$. The supply function in this case is directly proportional to the number of photons absorbed by the material, hence it is proportional to the intensity of the light source. Other factors effecting emission are the absorption coefficient and the escape depth of the electron.

3.3 FIELD EMISSION

Traditionally when examining field emission the focus in on the barrier at the surface of the material. Unlike thermionic emission and photoemission, an applied field at the surface bends the vacuum level to create a triangular barrier at the surface as shown in Figure 9. This changes the width of the surface barrier and hence its transmission probability.
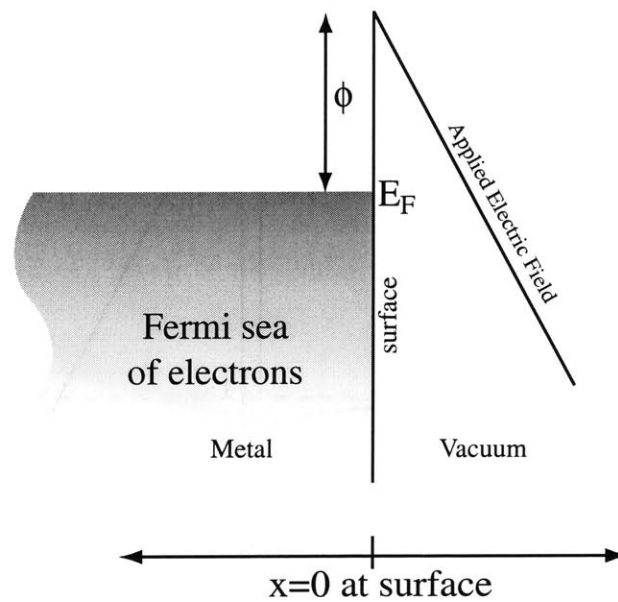
Figure 9: Model of a metal surface with an applied field
The applied field at the surface creates a triangular barrier that, if thin enough, can have appreciable electron tunneling, resulting in an emission current.

By modifying the surface transmission function, electrons are able to tunnel from the Fermi-sea to vacuum when the barrier width (at the energy) is less then 1 or 2 nm. For field emission the electrons are emitted from approximately the Fermi-level [46].

3.3.1   Basic Model of Potential at Surface of a Metal

The potential barrier at the surface of the metal is modeled after a planar structure where the electric field is uniform, creating a linear potential that starts at the surface a distance ϕ above the Fermi-level, see Figure 106. This translates to a potential:

$$V = -(\mu+\phi) \qquad\qquad \text{for x<0}$$
$$V = -eFx \qquad\qquad \text{for x=>0}$$

where F is the applied electric field in V/m, x is the distance from the surface in meters and the potential associated with the vacuum level at the surface of the metal is considered V=0.
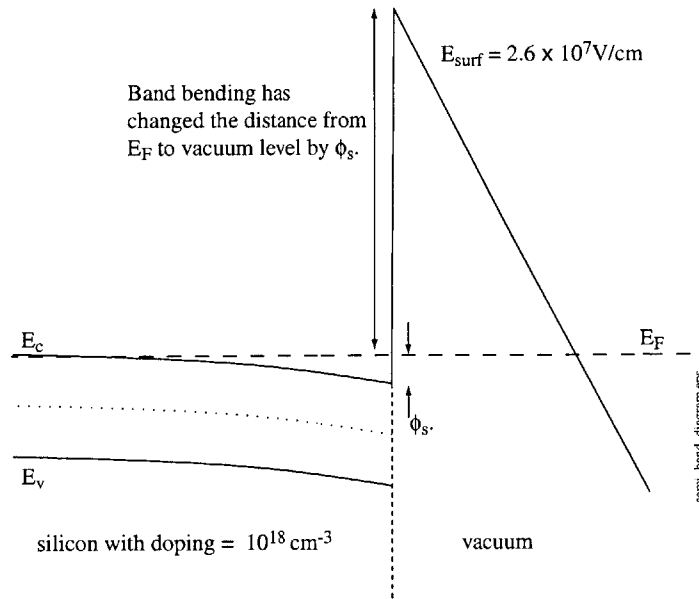
Figure 10: Band Diagram of Silicon with an external applied electric field.
The calculations for the band diagram were done using a modified version of SCHRED.
The solution is determined for the electrostatic, 'zero current' approximation.

3.3.2 Basic Model of Potential at Surface of a Semiconductor

Unlike a metal, the field penetration into even a highly doped semiconductor can be significant. The bending of the conduction band below the Fermi-level corresponds to the existence of a distributed, excess volume charge of electrons near the surface, more commonly referred to as an accumulation layer [46, 48, 49]. Once the conduction band has bent below the Fermi-level, Boltzman statistics no longer apply and Fermi- statistics must be used. The highest filled level should still correspond to the Fermi-level (within a few k_BT).
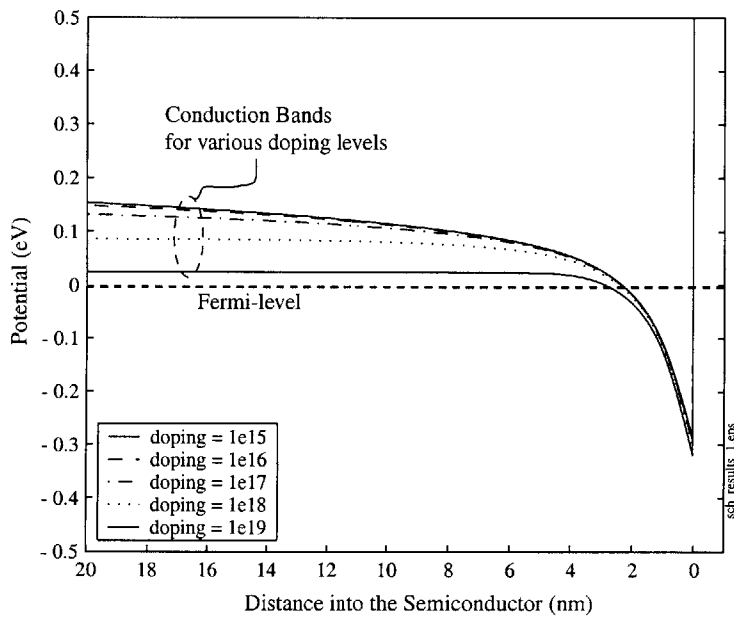
Figure 11: Conduction Bands at the surface for external electric field
The conduction bands for a variety of doping levels all have shifted a uniform amount independent of doping level in response to an externally applied electric field.

This bending of the bands causes the workfunction used in the Fowler-Nordheim equation to decrease. SCHRED developed at Purdue University [50] calculates the envelope wavefunctions and the corresponding bound state energies in typical MOS structures by solving self-consistently the 1D Poisson equation and the 1D Schroedinger equation. Simulations using a

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modified version of SCHRED [51] indicated that the position of the conduction band at the surface with respect to the Fermi-level will be independent of the doping level of the silicon.

This work uses Fowler-Nordheim theory to predict emission from silicon, using a workfunction of 4.04 eV. This has shown to be accurate in other simulation work [44]. Using Fowler Nordheim theory does not take into account the potential well nature, or quantization of energy levels in the 2D electron gas at the surface.
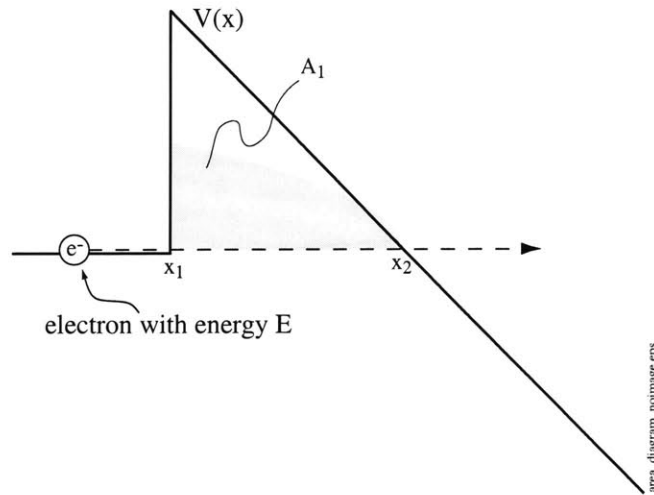
Figure 12: Tunneling through a triangular potential barrier
Based on WKB approximation, the transmission of an electron through a barrier is equal to the exponential of the integral of the square root of the area..

3.3.3   Fowler Nordheim tunneling without image potential

If we consider electrons at the Fermi-level, we can calculate a transmission coefficient for the barrier in Figure 9 using the Wentzel-Kramers-Brillouin (WKB) approximation (Appendix C). The probability that an electron traveling toward the surface will proceed through the barrier is:

$$D(E,V) \cong \exp\left[-2\sqrt{\frac{2m}{\hbar^2}}\int_{x1}^{x2} k(x)dx\right],$$

where

$$k(x) = \sqrt{V(x) - E} \, ,$$

and V(x) and E are the electrons potential and kinetic energies respectively [46] and x_1 and x_2 are the classical turning points. The integral in the above equation represents the area A_1 shown in Figure 12

The transmission through a barrier can be conceptualized as, $D \cong e^{-A_1}$ for a triangular barrier where:

$$A_1 = \int\limits_{x1}^{x2} k(x)dx$$

For the triangular barrier, A_1 can be easily solved analytically as:

$$A_1 = \frac{(\phi + E_F - E)^{3/2}}{2Fe}$$

which can be substituted into the equation for D(E,V) above. Additionally if we limit electrons to ones at the Fermi-level:

$$D = \exp\left[-\frac{4}{3e}\left(\frac{2m}{\hbar^2}\right)^{1/2} \frac{\phi^{3/2}}{F} \right],$$

where ϕ is in volts and F is in volts/cm. Multiplying D by the arrival rate of electrons approximates the emitted current. If this is done using the original D(E) and multiplying by the appropriate differential arrival rate as a function of electron energy the result is the Fowler-Nordheim Equation.

$$j = \frac{e^3}{8\pi h \phi} \cdot F^2 \exp\left[-\frac{4}{3e}\left(\frac{2m}{\hbar^2}\right)^{1/2} \frac{\phi^{3/2}}{F} \right] \text{ amps/cm}^2$$

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which relates the emitter current density to the applied surface electric field.

3.3.4   Variation in Tunneling probability with Image Potential

The largest deviation of the real barrier from the barrier shown in Figure 9 is the addition of the image potential [52, 53]. It represents the potential correction due to a force on an electron at position x outside a metal surface. This force is due to the charge induced in the metal by the electron at position x. This force is typically calculated by assuming that there is an image charge inside the conductor at an equal distance from the surface with an opposite charge.

The potential outside the conductor is due to the electron and an image charge. The force on the charge is the field at x due to all other charges except the charge itself, (the charge cannot act on itself) [54]. By integrating from ∞ to x we obtain the potential due to the image charge of:

$$V_{image} = \frac{e^2}{4\pi\varepsilon_o x} = \frac{0.3595}{x}$$

for V_{image} in eV and x in nm. Figure 13 shows the barrier including the image charge potential. The transmission through this barrier can be now related to the shaded area of the figure, A_2.
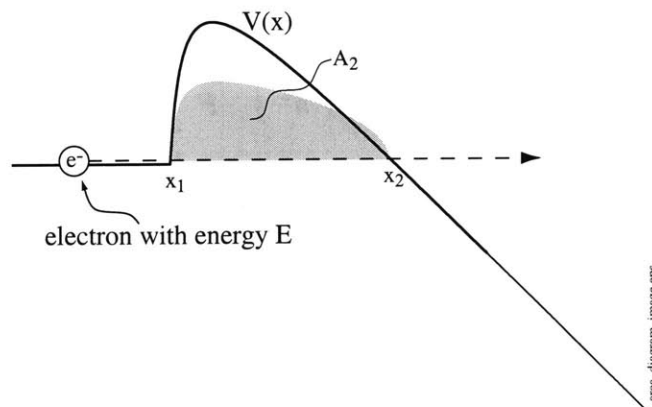
Figure 13: Tunneling through a potential barrier including the image charge potential
Based on WKB approximation, the transmission of an electron through a barrier is equal to the exponential of the integral of the square root of the area.

The new tunneling probability

$$D = e^{-A_2} = e^{-\alpha A_1}$$

where

$$\alpha = \frac{A_2}{A_1} = 0.95 - y^2$$

where

$$y = 3.8 \times 10^{-4} \frac{F^{\frac{1}{2}}}{\phi}$$

and α is always less then 1. More detail on the use do y in the above relationships, v(y) and t^2(y) presented below, see Appendix C.

3.3.5   Complete Fowler Nordheim Equation

The complete Fowler-Nordheim equation which describes the current density emitted, J [A/cm^2], as a function of the electric field at the metal surface, F [V/cm^2], and the material's workfunction, ϕ [eV] [55,[56].

$$J(F,\phi) = \frac{e^3 \cdot F^2}{8 \cdot \pi \cdot h \cdot \phi \cdot t^2(y)} \cdot \exp\left(-\frac{8 \cdot \pi \cdot (2 \cdot m)^{\frac{1}{2}} \cdot \phi^{\frac{3}{2}}}{3 \cdot h \cdot e \cdot F} \cdot v(y) \right)$$

where we see a similar parameter y which is:

$$y = \left(e^3 F \right)^{\frac{1}{2}} \bigg/ \phi$$

and e = electronic charge, h = Planck's constant and t^2(y) and v(y) are Nordheim elliptical functions which take into account the image charge effects. Their values are well approximated by t^2(y) = 1.1 and v(y) = 0.95 - y^2.[57] As compiled by Spindt (1976), the simplification and further manipulation of the above equation is as follows:

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$$J(\varepsilon,\phi) = \frac{A \cdot \varepsilon^2}{\phi \cdot t^2(y)} \cdot \exp\left(-B \cdot \frac{\cdot \phi^{3/2}}{\cdot \varepsilon} \cdot v(y)\right)$$

where $A = 1.54 \times 10^{-6}$ and $B = 6.87 \times 10^7$ and $y = 3.79 \times 10^{-4} E^{1/2}/\phi$.

3.3.6   Fowler Nordheim Coefficients

The Fowler Nordheim equation above relates current density to surface electric field. Conceptually, the total current from a tip should be computed by taking the integral of the current density over the entire emitter surface:

$$I = \int_S J(E(\vec{r}))dA$$

Although the tip surface can not be expressed in a closed form, the integral can be simplified assuming axial symmetry with $r(\theta) = R_{TIP}g(\theta)$ and the current written as:

$$I = 2\pi R_{TIP}^2 \int_\mu^1 J(E(x))g^2(x)xdx = \alpha' \pi R_{TIP}^2 J(E_A)$$

where the second equality expresses the mean value theorem. The effective emitting area $\alpha' \pi R_{TIP}^2$ indicates that there is a proportionality constant between the tip current density and the tip current. The proportionality constant is:

$$\alpha = \alpha' \pi R_{TIP}^2$$

Electrostatics can be used to show that there is also a similar proportionality constant β relating the field to the applied voltage. The derivation of β is shown in Section 3.4.

By substituting the following relationships into the Fowler-Nordheim equation,

$$J = \frac{I}{\alpha}, \text{ and } F = \beta V,$$

where α is the emitting area and β is the local field conversion factor at the emitter surface (see paragraph 3.4), the modified Fowler-Nordheim equation is given by:

$$I = a_{FN} V^2 \exp\left(\frac{-b_{FN}}{V}\right)$$

where:

$$a_{FN} = \frac{\alpha A \beta^2}{1.1\phi} \exp\left(\frac{B(1.44 \times 10^{-7})}{\phi^{1/2}}\right)$$

$$b_{FN} = \frac{0.95 B \phi^{3/2}}{\beta}$$
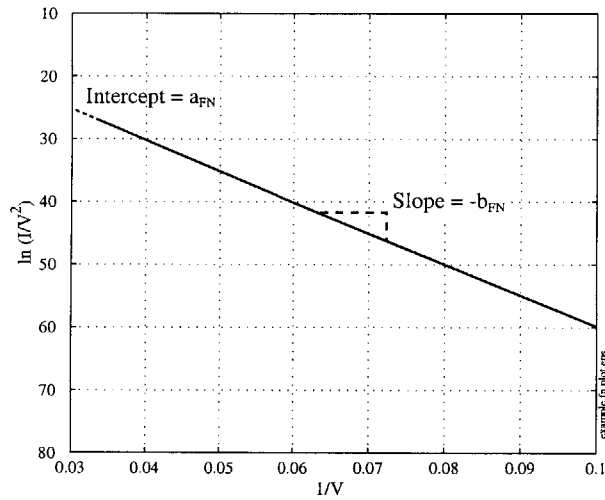
Figure 14: Example Fowler Nordheim Plot

Current associated with field emission that behaves as per the Fowler Nordheim equation will be linear on a Fowler Nordheim plot. The Fowler Nordheim coefficients a_{FN} and b_{FN} can be extracted from a linear fit of the data where a_{FN} is the y-intercept and $-b_{FN}$ is the slope.

The parameters a_{FN} and b_{FN} can be found from the slope and intercept of the Fowler Nordheim plot which is a plot of $\ln(I/V^2)$ vs. $1/V$. (Figure 14)

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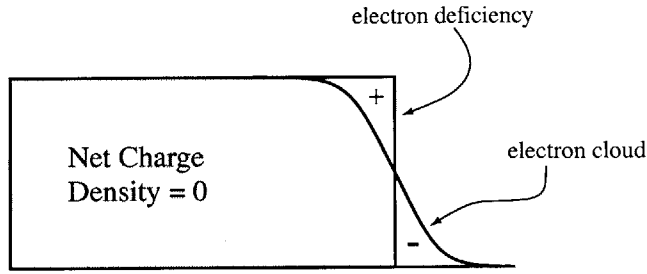
Figure 15: Global shift of the electron density

3.3.7 Shifted Image Potentials

The traditional image potential breaks down at the surface because of the singularity at the origin

[58]. Jensen proposed an analytical image charge potential that accounts for the change in origin

caused by a global shift of the electron density relative to the ionic core at the surface due to the

finite barrier [59] shown in Figure 15. Kiejna proposed a similar image charge potential to better

correlate numerical results with experimental measurements of energy distribution of field

emitted electrons [60]. By adding an additional term to shift the potential, both Kiejna and

Jensen were better able to represent the actual barrier:

$$V_{image} = \frac{0.3595}{(x + x_o)},$$

where Kiejna defines:

$$x_o = \frac{\alpha^2}{V_o}$$

where α is a constant < 1 and V_o is the $\mu + \phi$ (the distance from the bottom of the conduction band

to the vacuum level, μ = chemical potential, and ϕ = workfunction of the material). Kiejna uses

a value of $\alpha = 0.7$ for his approximation but provides no justification for the value.

Jensen's shifted image potential uses:

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$$x_o = \sqrt{\frac{\hbar^2}{2mV_o}}$$

where m is the electron mass and V_o is the distance from the bottom of the conduction band to the vacuum level. If the numerical values of the two shift terms are compared, there is good agreement, $x_{o(Jensen)} = 0.0553$ nm, and $x_{o(Kiejna)} = 0.0560$ nm. Based on such similar results from a theoretical analysis and experimental data, these shift terms are reasonable.

3.3.7.1 Uncertainty Region

Brodie proposed a model for calculating the workfunction of materials using the Heisenberg Uncertainty Principle [61, 62]. Using simple concepts such as atomic radius, it calculates workfunctions that are in fair agreement with experimental results. Brodie proposed that at the surface there is a region of "uncertainty" through which an electron traverses to escape from the surface, dx. In crossing this region, the electron converts it's kinetic energy to potential energy and hence no work is done in traversing this region. Furthermore Brodie postulates that the classical image force only begins to act at this distance (of uncertainty) from the surface.

The kinetic energy of an electron inside the metal as measured from the bottom of the conduction band is E_F. Once the electron transverses the 'uncertainty region' of width dx it has zero kinetic energy. The change in momentum over this distance is given by:

$$\Delta p = \sqrt{2mE_F}$$

where m is the effective mass of the electron inside the metal. By specifying the change in momentum above, the Heisenberg Uncertainty principle dictates that smallest uncertainty in position of the electron will be:

$$\Delta p dx = \frac{h}{2\pi}$$

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or:

$$dx = \frac{h}{2\pi\sqrt{2mE_F}} = \frac{0.1953}{\sqrt{E_F}}$$

where dx is in nm and the factor $(m^*/m)=1$ is assumed.

The 'Uncertainty' region of thickness dx over which the image potential does not act can be thought of as a shift of the image potential to a 'new' surface.
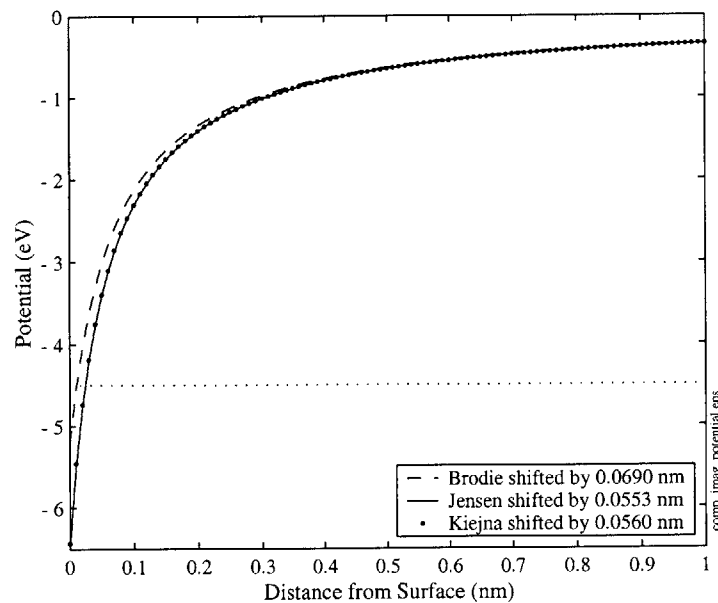
Figure 16: Shifted Image Potentials

Shifted Image Potentials as presented by Brodie, Jensen and Kiejna with shifts of 0.0690nm, 0.0553nm and 0.0560nm respectively.

3.3.7.2 Comparison of Different Image Potentials

In order to evaluate the different image potentials presented above, plots of the potentials for the first nm from the surface (for Brodie, the surface is assumed to be the edge of the uncertainty region) in Figure 16. Figure 17 shows the shifted image potentials superimposed on a triangular barrier formed by applying 3×10^9 V/m field to the surface, (a typical field at the onset of field

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emission), of a molybdenum tip. The values for molybdenum of μ = 8.01 eV and ϕ = 4.5 eV are used for these calculations [61].
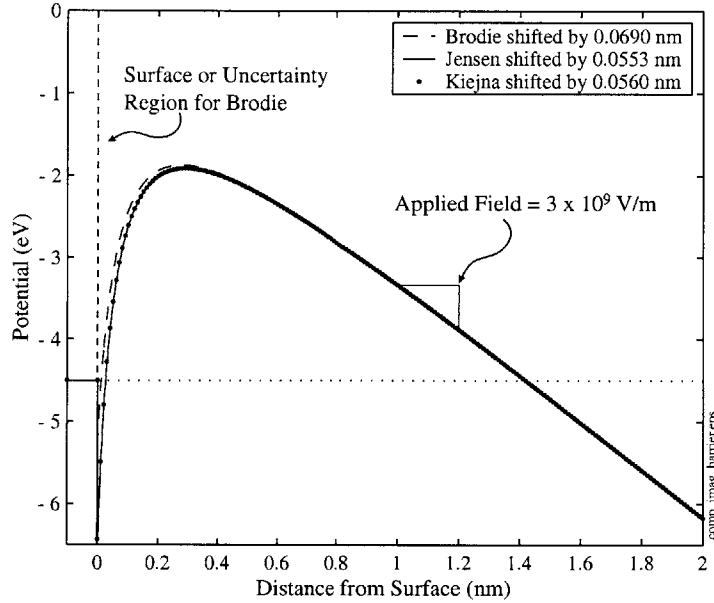
Figure 17: Effect of Shifted Image Potentials on triangular Barrier

The shifted image potentials from above are superimposed on a triangular barrier caused by a surface electric field of 3×10^9 V/m. The surface is considered to be the metal surface for the cases of Jensen and Kiejna where as it is the surface of the 'uncertainty' region spaced dx from the metal surface for the Brodie potential.

3.4 FIELD ENHANCEMENT

From a typical planar surface we can estimate the required field to get appreciable current flow from the device by assuming:

- that all the emission is from the Fermi level, and
- the tunneling probability becomes significant when the barrier width is 1 - 2 nm, (approximately the wavelength of the electron).

For a material with a work function of ϕ = 4.5 eV, the applied field is required to be 2×10^9 - 5×10^9 V/m. For a planar surface, a large voltage would be required to achieve these fields in a

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parallel plate model, even at sub-micron spacing. For a spacing of 50 nm, 250 volts would be required to achieve a surface electric field of 5×10^9 V/m.

$$5 \times 10^9 \frac{V}{m} \times 50 nm \times \frac{m}{10^9 nm} \Rightarrow 250V$$

This parallel plate example shows that in order to achieve a high field at low voltages we will need to use the physical structures such as sharp tips to enhance the surface electric field. The classical conical emitter structure has no analytical solution; however the "ball in a sphere" and "coaxial-cylinder" models can be solved analytically to provide insight into how the geometrical effects provide field enhancement.
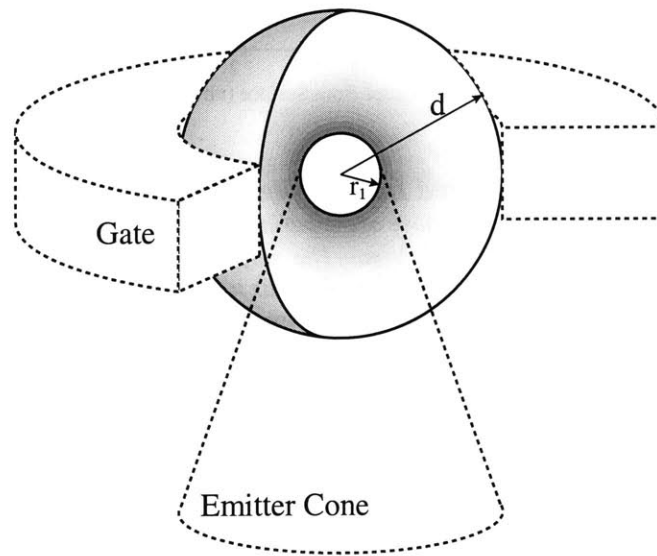
Figure 18: Ball in a Sphere Model
The outer shell is a thin conducting shell with radius = d and the inner conducting-ball has a radius = r_1. Free space is considered to be vacuum. When examining the field on the surface of the inner ball, this model provides a good first order approximation to surface electric field on the tip of a cone type emitter with a tip radius of r_1 and a gate aperture of 2d. The outer shell is held at a potential V_g and the inner ball is held at ground.

3.4.1   Ball in a Sphere

A good model for the geometry effects in a field emitter cone is the ball in a sphere model. The interior ball is analogous to the cone tip and the outer sphere is the gate structure. The ball in a sphere can be readily solved analytically in spherical coordinates

A solution to Laplace's equation can be determined for the region between the two surfaces by taking a linear combination of two known solutions in spherical coordinates:

$$V = \frac{A}{r} + B,$$

with boundary conditions given as:

$$V(r_1) = 0, V(d) = V_g$$

The electric field (F) can be found by taking the gradient of the potential, evaluating at r = r$_1$ gives the surface electric field to be:

$$F_{tip-surface} = -\beta V_G,$$

where,

$$\beta = \left[\frac{1}{r_1} + \frac{1}{d - r_1} \right],$$

In the case where d $\gg$ r$_1$, the electric field is independent of gate aperture (2·d) and inversely proportional to the radius of curvature of the tip. In order to achieve the previous required electric field (5 × 10^9 V/m) at low gate voltages (10 V) the radius of curvature (r$_1$) of the tip must be on the order of 2 nm.

3.4.2 Coaxial Cylinders

A good model for the geometry effects we see in ridge type field emitter is the coaxial cylinder model. The interior cylinder is analogous to the cone ridge and the outer cylinder is the gate structure. The coaxial cylinder model can also be solved analytically [63] in cylindrical coordinates.
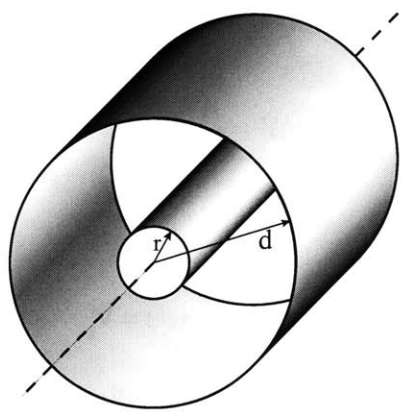
Figure 19: Coaxial Cylinders

The outer shell is a thin conducting cylinder with radius = d and the inner conducting-cylinder has a radius = r_1. Free space is considered to be vacuum. When examining the field on the surface of the inner cylinder, this model provides a good first order approximation to surface electric field on the edge of a ridge or thin film type emitter with a tip radius of r_1 and a gate to tip spacing of d. The outer cylinder is held at a potential V_g and the inner cylinder is held at ground.

A solution to Laplace's equation can be determined for the region between the two surfaces by taking a linear combination of two known solutions in cylindrical coordinates. The electric field (F), can be found by taking the gradient of the potential; evaluating at r = r_1 gives the surface electric field to be:

$$F_{ridge-surface} = -\beta V_G \text{, where } \beta = \frac{1}{r_1 \cdot \ln\left(\frac{r_1 + d}{r_1}\right)},$$

The field factor associated with the coaxial cylinders, (and ridge type emitters) is less than that for the ball in a sphere or cone type emitters. Hence, ridge like structures are less useful for low voltage FEDs.

3.5 SUMMARY

The models presented in this chapter provide a framework for understanding of the physics of field emission and field emission devices. The extension of these analytical models to numerical models will provide a better understanding of actual device geometries operation as described in the next chapter.

4 NUMERICAL MODELING

The analytical models presented in Chapter 3 provide a wealth of qualitatively information about how we expect the field emission devices to behave. The next step beyond the analytical model is to solve a numerical model. The numerical models provide solutions to a geometry that is not solvable by analytical means. Although the numerical models still contain assumptions or idealities, they provide a more accurate picture of device operation.

This chapter introduces some background on previous field emission numerical models and the different techniques that have been used. The specifics about the modeling done in this work will be presented followed by the results of the simulation as a tool for predicting the performance as the gate aperture is scaled below a 1 µm. Additionally, some analysis of the tunneling barrier shape will be presented.

4.1 SIMULATION LITERATURE REVIEW

Most electrostatic simulation work on field emission involves the use of an electrostatic solver, and the evaluation of device performance based on ε-field solutions. Previous simulation work has been concentrated in three areas; focusing [44, 64, 65, 66, 67, 68], electrical characterization [63, 44, 69, 70, 71], and thermal effects [63,71, 72, 73].

4.1.1 Focusing Modeling

Many applications of FEAs (both display and microwave) require a collimated electron beam. A well-collimated beam allows further separation of the faceplate and base-plate in a field emission display without the spread of the electron beam thus avoiding the trade off between resolution and luminous efficiency. Focusing methods have included proximity focusing or the use of an

additional focusing electrode. In addition to providing a well-collimated beam, the effects of the focusing must be considered on the performance of the device. In some focusing schemes there may be a reduction of the local ε-field at the tip due to the focusing electrode (typically seen when $V_{focus} < 0.0$), or current loss to the focusing electrode, (typically seen when $V_{focus} > 0.0$). This work does not include analysis involving a focusing electrode but the modular nature of the software will easily allow the addition of focusing electrodes for such analysis.

4.1.2 Electrical Performance Modeling

Simulation that concentrates on the electrical performance of the FEAs has been conducted to analyze the effects of varying device geometry. The work that has studied the large emitter regime where gate apertures range from 1100 nm [71] to 4000 nm [69] and uses tip radius of curvatures generally ranges from 10 - 50 nm. These models have difficulty predicting device performance based on the cone having a smooth spherical cap with radius much larger then 10 nm. Experimental results have indicated that the electric fields at the tip are too small by a factor of 4 to account for the observed field emission without requiring an unreasonably small work function [4]. While features below 10 nm will most likely dominate device performance, it is difficult to model tip radius of curvature below 10 nm with most electrostatic simulators. This is primarily due to the large difference in dimensional scales of the tip (nm), aperture (μm) and anode (mm), (modeling a 3-nm feature in a 100 μm problem space), and the inability of a solver to resolve them with a finite number of mesh points [63]. Although the study does not analyze rough surfaces and uses a spherical cap for the emitter tip, the size regime being investigated is small enough (1 nm < radius of curvature < 5 nm) to indicate the general feature size of the emitter. Ultra sharp uniform emitters have been shown and simulated in previous work by Hori [74] and Yang [44]. In addition the problem space is scaled to the emitter size in order to

provide fine resolution in the active region of the device. Boundary conditions are adjusted to account for the changes in problem space size.

4.1.3   Thermal and Mechanical Modeling

Thermal modeling has been conducted on a variety of emitter structures to evaluate the effects of the typical high local current densities. Based on the results of these studies device performance of the simulated devices was monitored in terms of operating voltage, but also based on local current densities. At representative current densities device failure is not likely to be due thermal effects [71, 72, 73], but instead due to Maxwell stresses at the tip. [73]

4.2   ELECTROSTATIC MODELING METHODS

There are two main non-analytical methods for conducting an electrostatic simulation, Finite Element Method (FEM) and Boundary Element Method.

4.2.1   Finite Element Methods (FEM)

Finite Element Methods break the problem space into discrete sections. The solution is determined for each 'finite element' where the overall solution meets the boundary conditions and satisfies the system of equations that are being solved. For a 2D-solution space the finite elements are triangles as shown in the mesh in Figure 20. The use of a 2D solution to simulate a 3D model limits the models to ones that are independent of one variable (e.g. axially symmetric in cylindrical coordinates). Full 3D finite element modeling is considered to be very computationally intensive.
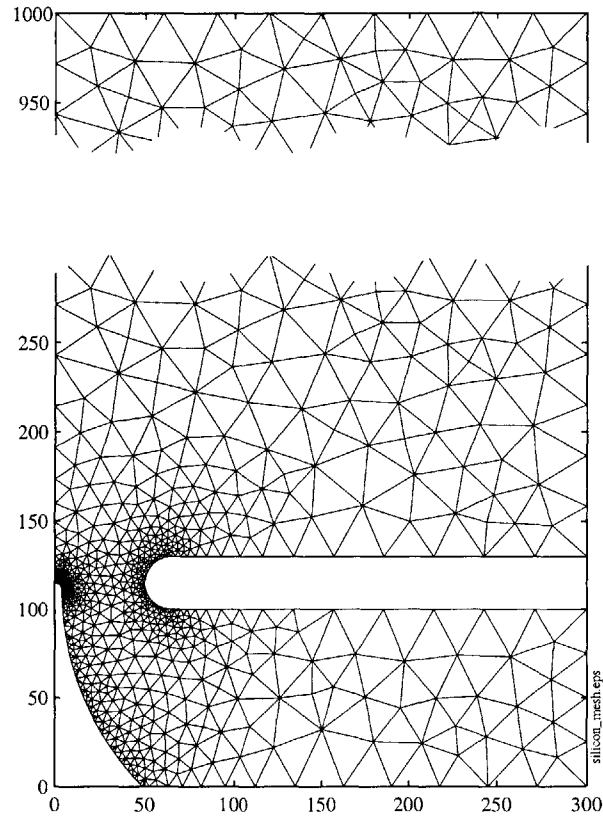
Figure 20: Example solution space for 2D FEM
This meshed solution space takes advantage of the axially symmetry of the problem to provide a 3D solution.

4.2.2   Boundary Element Methods (BEM)

BEM meshes the boundary elements that are lines for a 2D model and surfaces for a 3D problem. The solution is determined at the nodes of the boundary elements. At every interior point to the boundary, the governing partial differential equations are satisfied [75, 76]. Because the solution is determined only for the boundary, no internal mesh is required and there are no unknowns associated with the interior points. It has been shown to be more computationally advantageous to go to a Boundary Element Method [44] as shown in Figure 21 when modeling of 3D structures that can not be simplified to a 2D model based on some symmetry.
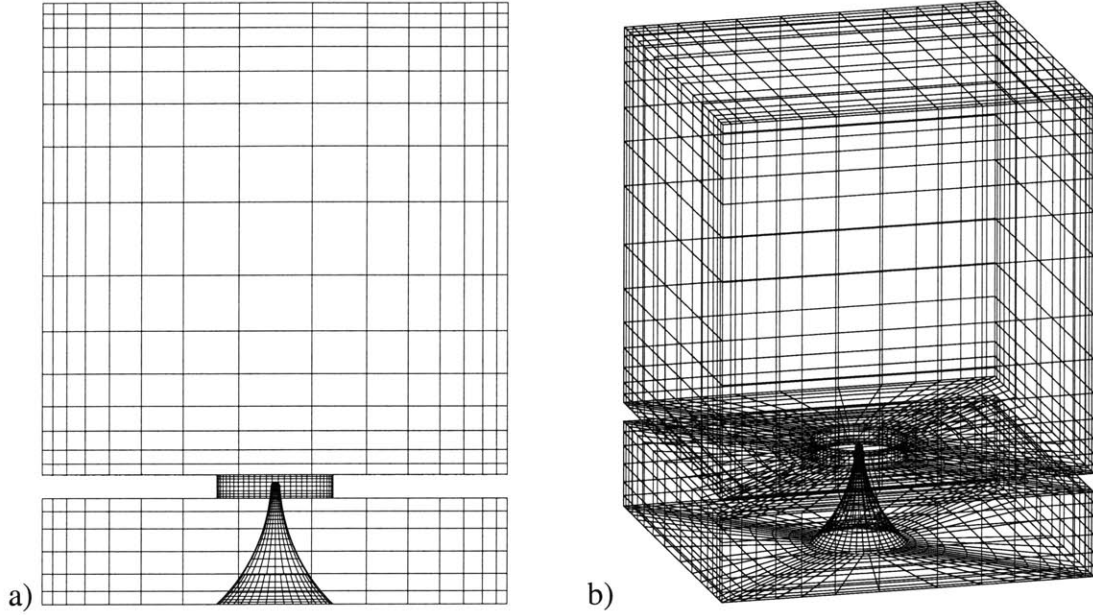
Figure 21: 3D BEM solution space where the surface is meshed
The 3D BEM does not require the structure to have any symmetry. These models were
created using a BEM solver, (developed by Y.J. Yang) for comparison to the solution of
the finite element modeling.

4.3   ELECTROSTATIC SIMULATION IN THIS WORK

Electrostatic simulations in this work were done in the MATLAB Partial Differential Equation

Toolbox (PDE Toolbox). The toolbox allows a 2 dimensional problem to be defined along with

associated boundary conditions and differential equation coefficients. The general equation that

is solved is:

$$-\nabla \cdot \left(c\nabla u\right) + au = f \text{ in the bounded domain } \Omega,$$

where c, a, f and the unknown, u, are scalar, complex valued functions defined on Ω. By setting

c = x [77] and a = f = 0 we have a differential equation in a form for solving Laplace's equation

in cylindrical coordinates with axial symmetry.

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The use of the MATLAB PDE solver allowed the use of scripts (m-files) for model construction and solving. The solutions are transferred to the traditional MATLAB workspace where they are manipulated and analyzed to determine device performance and characteristics.

Once the solution is brought to the MATLAB workspace, the surface fields are analyzed and tunneling current is determined by using the Fowler-Nordheim equation. Additional analysis of the potential barrier and tunneling through that barrier is also done and will be discussed in later sections.
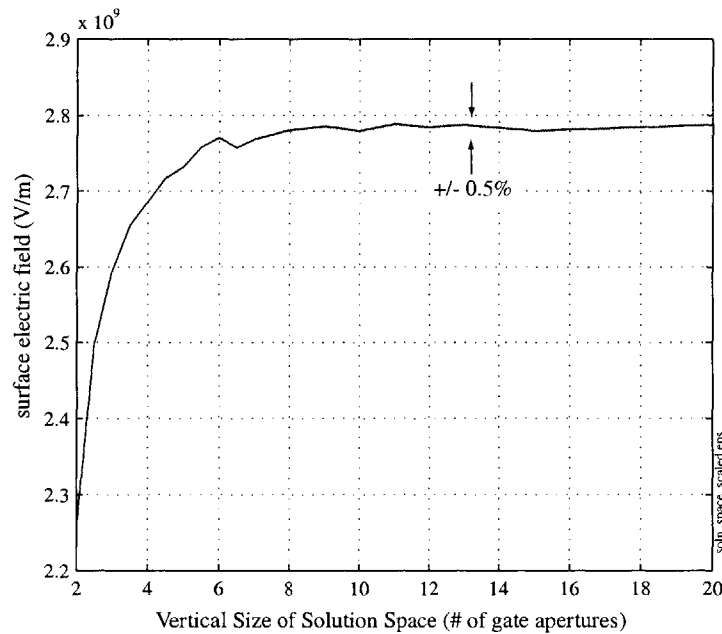
Figure 22: E-field solution on the surface of the tip vs. solution space size
The vertical size of the solution space was scaled and solved in increments of the gate aperture (100 nm). When the top Dirichlet boundary was at 800 nm, the solution converged to within ± 0.5% of a stable solution. The location of the top boundary was set to 1000 nm (10 'gate apertures').

4.3.1   Description and Set-up of the Model Space

Due to the axially symmetric nature of the problem, only half of the emitter needs to be defined in this case. The model is made up of a half cone, the gate structure. In order to avoid problems

with resolution of the solver, the problem space is limited to ten times the gate aperture in the r direction and three times the gate aperture in the z direction. This solution space size was chosen because the electric filed solution on the tip of the cone converges to a stable value, (comparison to a boundary element model presented later confirms the stable electric field solution. Figure 23 shows a layout from the solver package with labels added to indicate boundary conditions.
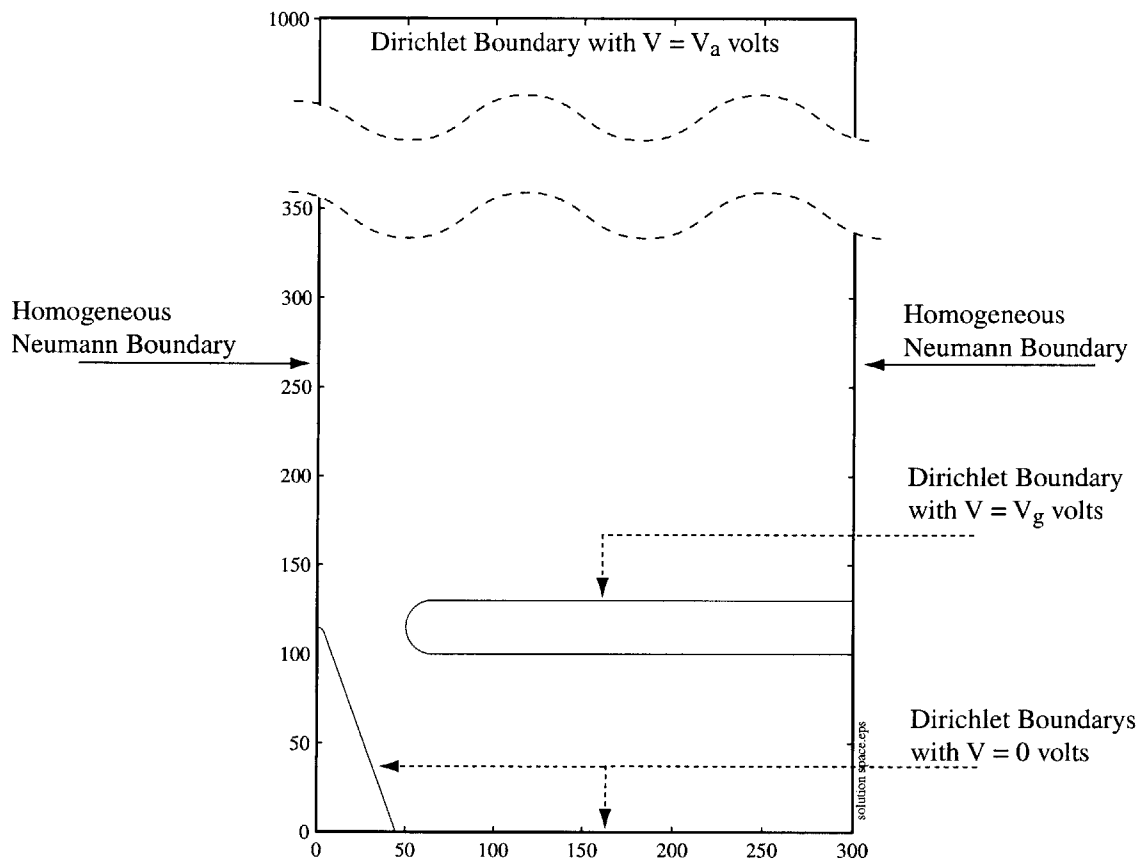
Figure 23: Problem Space with Boundary Conditions

The top edge in the problem space is selected as a boundary with a voltage. This boundary is set to a Dirichlet boundary condition, $V = V_a$. Because this is not actually the anode, V_a was chosen to apply a constant field of 1 V/μm, (setting an 'electric field' boundary condition by this

technique was due to difficulties and errors when using non-homogeneous Neumann boundary conditions in axially symmetric mode of MATLABs PDE toolbox). The left edge is set to a homogeneous Neumann boundary condition and represents the z-axis in the cylindrical coordinate system. The right edge is also defined to be a homogeneous Neumann boundary condition (meaning that there will be no normal components of the ε-field at this boundary). The bottom edge of the problem space and surface of the emitter tip is assigned a Dirichlet boundary condition, V = 0 volts. The surface of the gate is also assigned a Dirichlet boundary condition, V = V_g volts.

4.3.1.1 Superposition of Electric Field

Laplace's equation is linear in potential and allows a general solution to the Electric field to be found as a superposition of a basis set of solutions [66,78]. In order to minimize the run times for each model solutions were done in two steps:

1. Solve the electrostatic Problem with $V_a = 0$ V and $V_g = 1.0$ V.
2. Solve the electrostatic Problem with $V_a = 1.0$ V and $V_g = 0.0$V.

By creating two solutions, (U_a and U_g), the post processing routines can create solutions for a variety of boundary conditions by taking linear combinations of the two solutions as per

$$U_{total}(r,z) = V_a U_a(r,z) + V_g U_g(r,z).$$

This allows for the sweeping of either the gate voltage or the anode voltage without having to re-solve the electrostatic problem for the new boundary conditions.

4.3.1.2 Location of a Point (r, z) in the Mesh

One of the major challenges and computationally intensive part of a finite element mesh solution is to determine the location, (which triangle), of the point of interest in the triangular mesh. In

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order to save computational time, a two step approach was taken in order to determine which triangle the point of interest lies within.

a) General Triangle   b) Standard Triangle
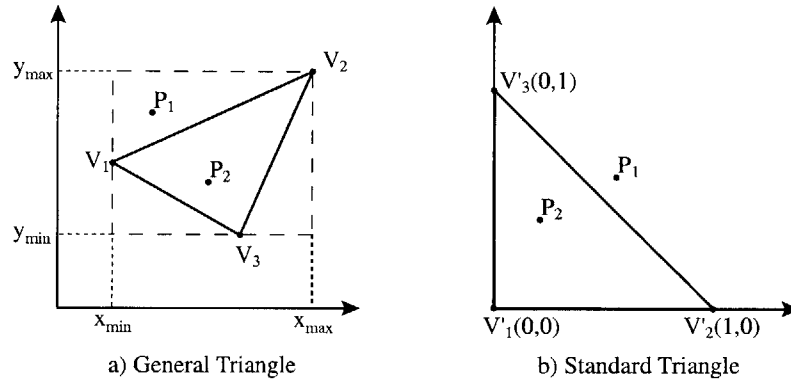
Figure 24: Triangle in a Rectangle

To determine if the point lies in a triangle in the array, the coordinates of the point are compared to the rectangle that encloses the triangle (See Figure 24a). This will eliminate all but a few triangles from further comparison. If a triangle passes the first criterion, then the coordinates of the point are transformed with the following matrix.

$$\begin{bmatrix} r' \\ z' \end{bmatrix} = \begin{bmatrix} (r_3 - r_2) & (r_1 - r_2) \\ (z_3 - z_2) & (z_1 - z_2) \end{bmatrix}^{-1} \begin{bmatrix} (r - r_2) \\ (z - z_2) \end{bmatrix}$$

This transforms the point (r, z) in r-z space to the point (r', z') in r'-z' space. As seen in Figure 24 a & b, the location of (r', z') can be compared in location to a standard right triangle with vertices at (0,0), (1,0), and (0,1). If the transformed point lies within this transformed triangle, then (r, z) lies within the original triangle. The point P_1 in Figure 24 would pass the first criterion because its r value falls within r_{min} and r_{max} and it's z value fall between z_{min} and z_{max}, but when transformed to r'-z' space, would lie outside the standard right triangle. Point P_1 does

not lie within the triangle in question. The point P_2 would also pass the first criterion and pass

the second criterion therefore is found to lie within the triangle in question.

In order the speed up these routines, the software takes advantage of matrix representation of the

data and routines that come with the MATLAB PDE toolbox for examining neighboring

triangles.

4.4 MODEL VALIDATION

Numerical models can introduce errors due to inadequate meshing or round-off error. In order to

understand the magnitude of the numerical errors that are introduced in the PDE toolbox simple

models were built and compared to the exact analytical solutions.

4.4.1 Comparison to Ball in a Sphere

The first model that was constructed was the simple ball in a sphere. The solution and

applicability of this model to typical field emission situations was described in paragraph 3.4.1

on page 15. The model was constructed with the following parameters:

Table 2: Parameters for Ball in a Sphere Model Validation

Geometric Feature	Size
Inner ball radius	10 nm
Outer Sphere radius	100 nm
Inner Ball Potential	0 V
Outer Sphere Potential	1 V

With the inner ball potential set at ground and the outer sphere set to 1 V the potential was

mapped radially out from the surface of the ball as shown in Figure 110.
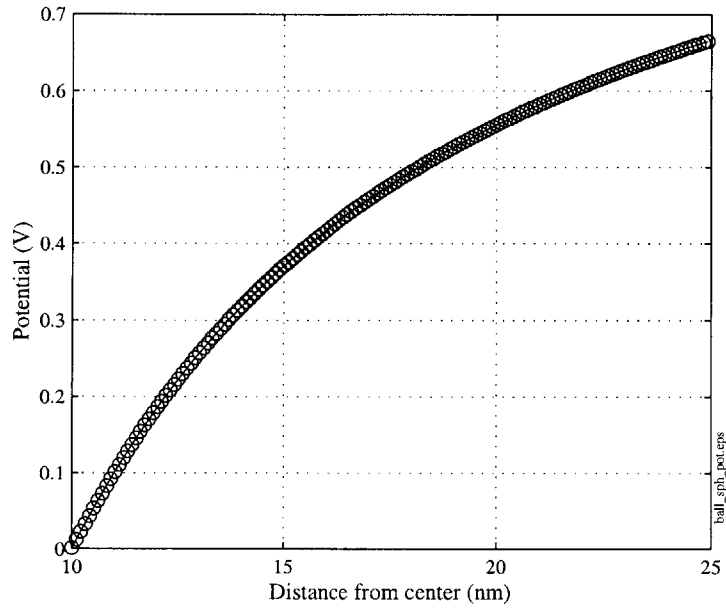
Figure 25: Ball-in-a-sphere Potential

The potential shown here is mapped from the outer surface of the ball (r = 10 nm) out to 25 nm. The inner surface of the sphere is much further out, but the main area of interest is right at the ball surface. The error drops as the solution is mapped further out.
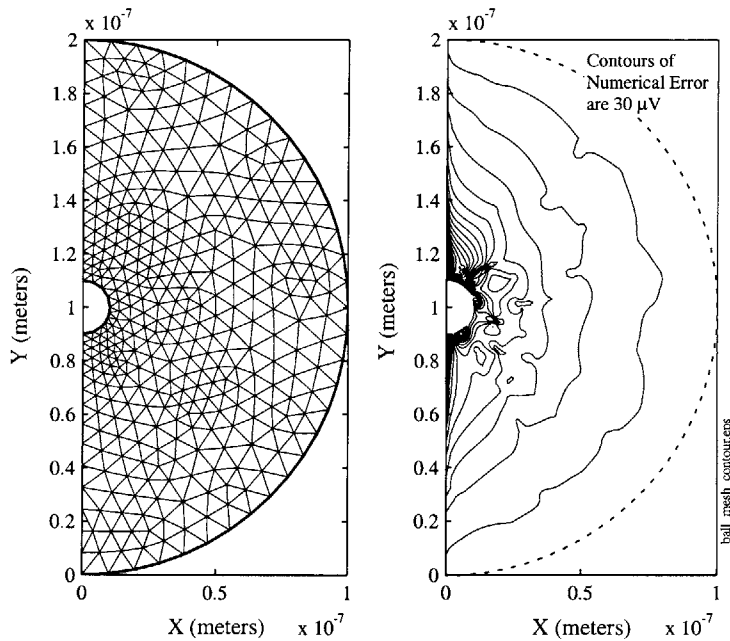
Figure 26: Ball in a sphere Solution Space and Contours of Error

The axially symmetric solution space is meshed and solved. The numerical solution at every triangle vertex is compared to the analytical solution and the error is plotted in the contour plot.

The meshed axially symmetric solution space and contours of the error in the potential solution are shown in Figure 26. Both the contours and a surface plot of the absolute value of the error in the potential is shown in Figure 27. The maximum absolute error of the potential was found to be 1.8×10^{-3} volts near the inner ball. The % error was an inaccurate measure of the solution because the largest errors came in a region where the solution was going toward zero. The surface electric field was also compared and the numerical error was 0.5 %. The accuracy of $\sim 10^{-3}$ volts is good enough when analyzing potential barriers that are over 1 volt in size.
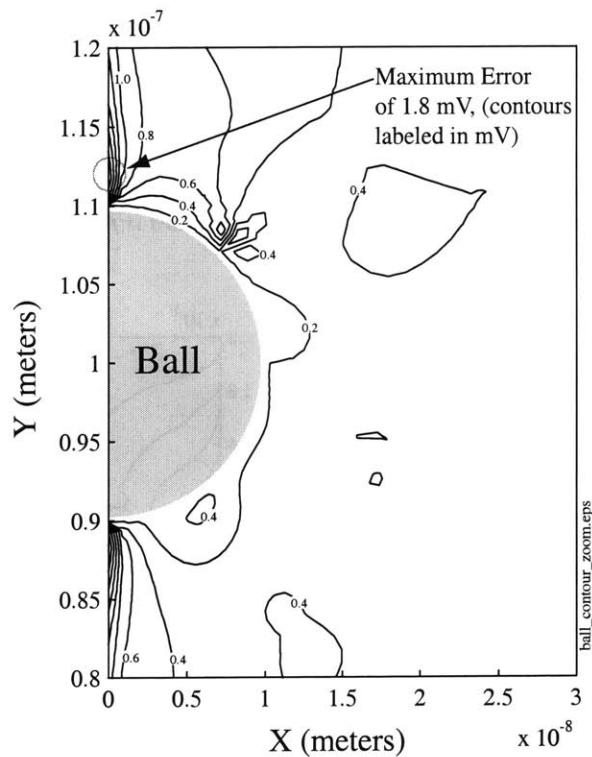
Figure 27: Contours of error near Ball
The contour plot shows the location of the absolute error in the ball in a sphere numerical solution of the potential when compared to the analytical solution. The largest the errors along the axis of symmetry of the problem. Magnitude of the error is at most 1.8×10^{-3} volts.

4.5 FIELD EMISSION DEVICE SIMULATION RESULTS

The device models used to generate IV characteristics are made up of a geometry, boundary

conditions, and an electrostatic solution. The emission current from a device is determined by:

- segmenting the tip into shells (based on the geometry), each with an associated area and surface electric field,
- determining a current density using Fowler-Nordheim Theory and subsequently a current associated with each shell,
- summing over all the shells to determine a current for that tip.

Repeating this process for boundary conditions associated with varying the gate voltage

generates IV characteristics. The IV characteristics were plotted on Fowler Nordheim Plot as

shown in Figure 28 for 100 nm gate aperture arrays with various tip radius of curvature.
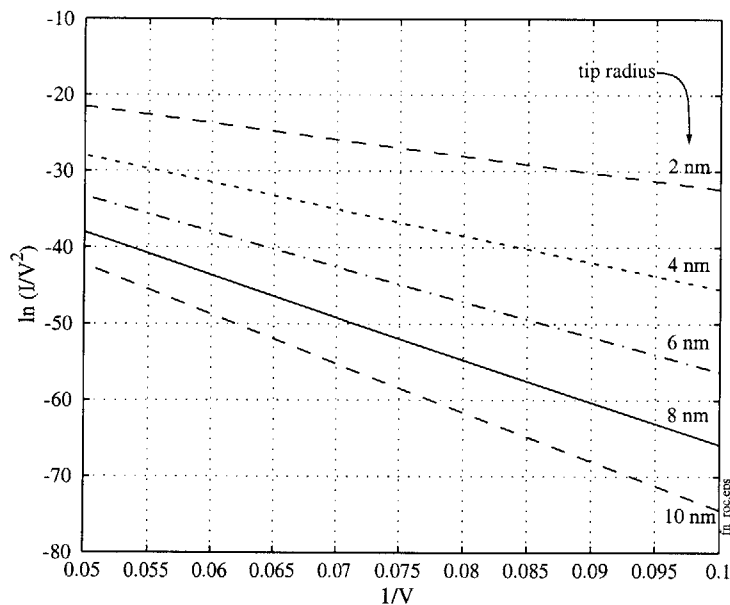
Figure 28: Fowler Nordheim Plot simulations with various ROC
Fowler Nordheim plot generated form the electrostatic simulation of Spindt type Molybdenum tips with a 100-nm gate aperture.

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From the Fowler Nordheim plot, the Fowler Nordheim coefficients as described in Chapter 3 were extracted and are shown as a function of tip radius in Figure 29. As expected, α is proportional to r^2 and β is proportional to $1/r$.

a_{FN} – intercept of the Fowler Nordheim plot
b_{FN} – slope of the Fowler Nordheim plot
α - effective emission area
β - field factor

Equations for a_{FN}, b_{FN}, α, and β are presented in Chapter 3.
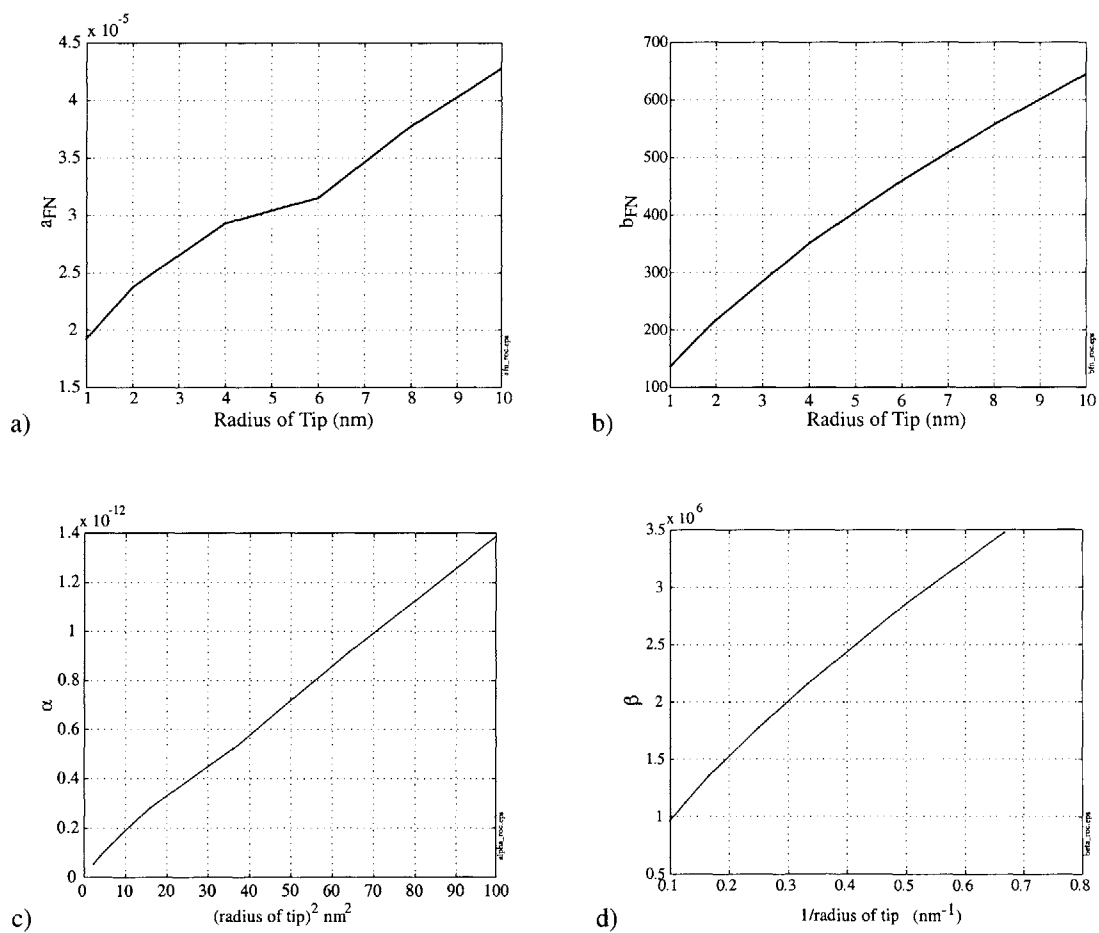
Figure 29: Fowler Nordheim Coefficients for Simulation

Plots of a_{FN}, b_{FN}, α, and β as a function of tip radius of curvature for the simulations shown in Figure 28.

4.5.1 Device Performance for Flat Panel Display Application

In order to determine the change in device performance as device geometry is scaled, a figure of merit called operating voltage, V_o, was established. V_o is the voltage required to provide an array current density, $(10 \ \mu A/cm^2)$, to support a typical flat panel display [79, 102].
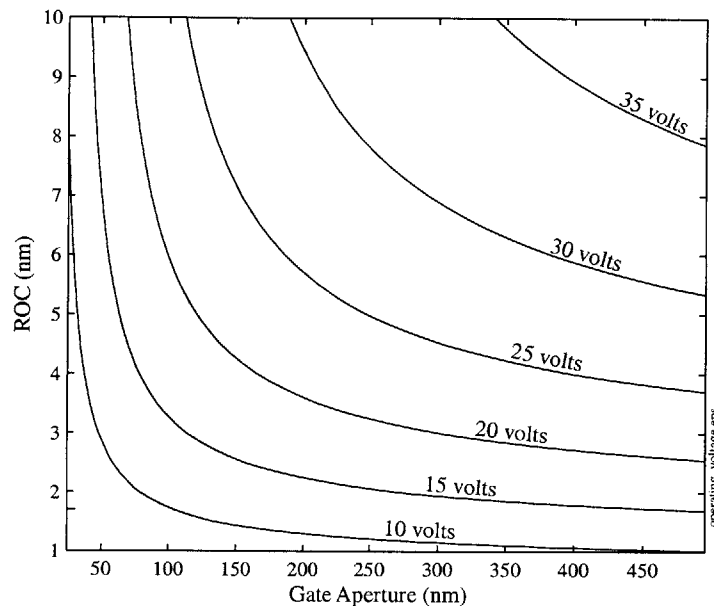
Figure 30: Contour Plot of V_o vs. Tip Radius and Gate Aperture
The contour lines show simulation results to predict the operating voltage to support a flat panel display application as a function of the tip radius and the gate aperture. The cone base angle is assumed to be 75°.

Figure 30 shows the dependence of the operating voltage on the gate aperture and the tip radius as the device is scaled well below the 1000 nm aperture regime. The simulations predict that it is feasible to fabricate 100 nm aperture arrays that will operate between 10 and 20 volts (indicated by the shaded region).

4.5.2 Comparison for FEM and BEM

The results from the FEM were compared to results from a BEM that was developed by Y.J. Yang [44]. Two models (FEM and BEM) were constructed with a tip shaped as if formed by

silicon isotropic etch and oxidation sharpening technique (see Figure 20 and Figure 21). Comparisons were done using a workfunction of 4.04 eV and a gate voltage of 20 volts. The surface electric fields from the two models are shown in Figure 31 where the field points for the BEM model are associated with the center of the panels shown and labeled in Figure 32. The field values for the FEM tip are associated with 30 equally spaced segments along the tip arc.
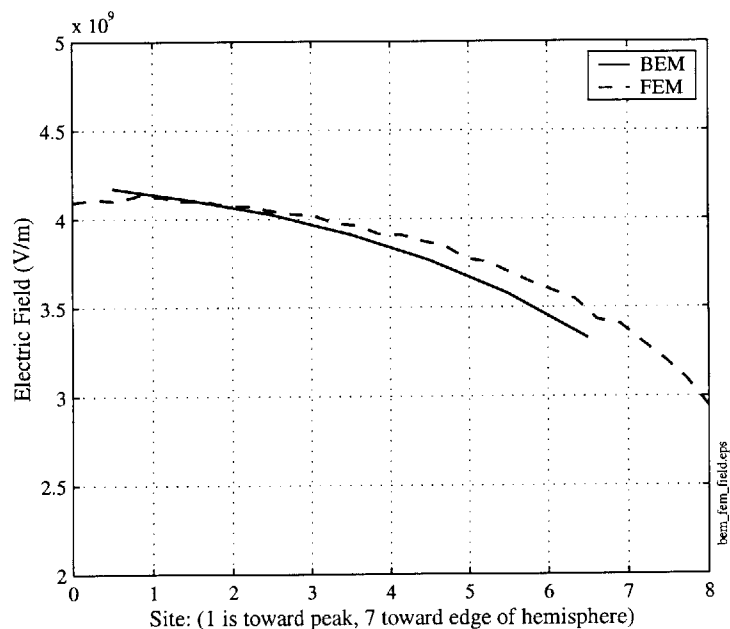
Figure 31: Comparison of the surface electric field for FEM and BEM
The two models are built with a 4-nm radius of curvature tip and a 100-nm gate aperture. The fields shown above are for a V_g = 20V. The BEM field points are associated with the center of a single panel (as shown in Figure 32). For the FEM solution, 30 points are analyzed along the 'arc' portion of the tip.
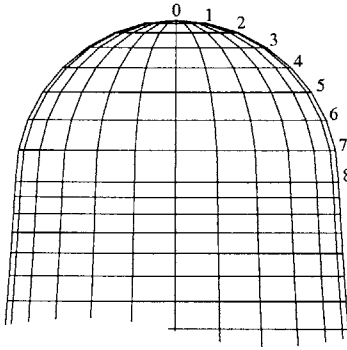
Figure 32: Diagram of the BEM tip
The numbers labeling the tip correspond to the x-axis in Figure 31, and Figure 33.

Using the field values shown in Figure 31, and assuming Fowler-Nordheim emission, the correspond emitted current densities were calculated and shown in Figure 33 as a function of position along the tip arc.
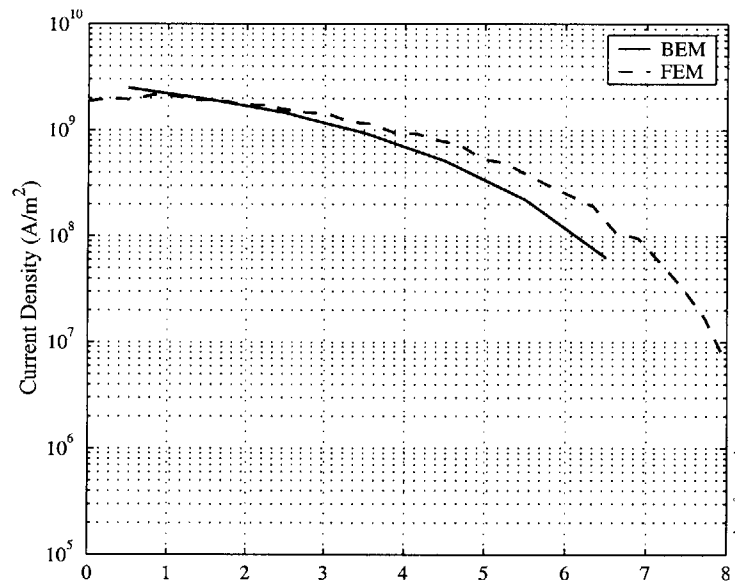
Figure 33: Comparison of BEM and FEM Current Density
The current density and current associated with the fields shown in Figure 31.

The FEM and BEM models were then evaluated with gate voltages from 10 to 40 volts and the results are shown in Figure 34. The numerical values of the Fowler Nordheim coefficients are

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shown in Table 3. There was a difference in the surface electric field that may have been due to the different boundary condition of the two models, (because the BEM model is a full 3D model, it uses 'tip in an array' boundary conditions). Even so, there is good agreement between the two models when predicting device performance. Fowler-Nordheim plots generated using the two models were compared and the voltages required to provide a specific emission current were determined. The difference in the voltages was less than 1 V.
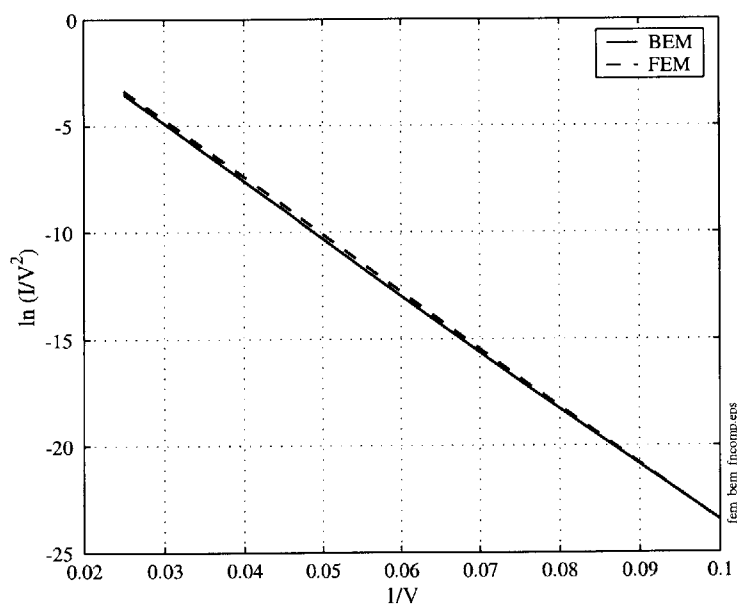
Figure 34: FN plots for BEM and FEM

The IV characteristics for the FEM and BEM show good agreement. There is only ~1 V difference for similar currents. The slopes and intercepts of the FN plots also show good agreement.

Table 3: FN parameters for FEM and BEM

	FEM	BEM
a_{FN}	21	23
b_{FN}	270	270
α	7.3×10^{-5}	7.9×10^{-5}
β	2.0×10^{6}	2.0×10^{6}

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4.5.3 Comparison of Spindt shaped tip to Silicon Shaped tip

Initial FEM models were of Spindt cone geometry, (Figure 35a), and the BEM model was built

for silicon cone geometry (Figure 21a). For the above comparison of BEM and FEM, new FEM

models were built to compare similar cone shapes to the BEM. Differences in comparisons of

Spindt FEM models and silicon BEM models lead to the analysis of the cone shape. Three FEM

simulations were done; a Spindt type cone (Figure 35a), silicon shaped cone (Figure 35b), and a

thin 'needle' shaped cone (Figure 35c),.
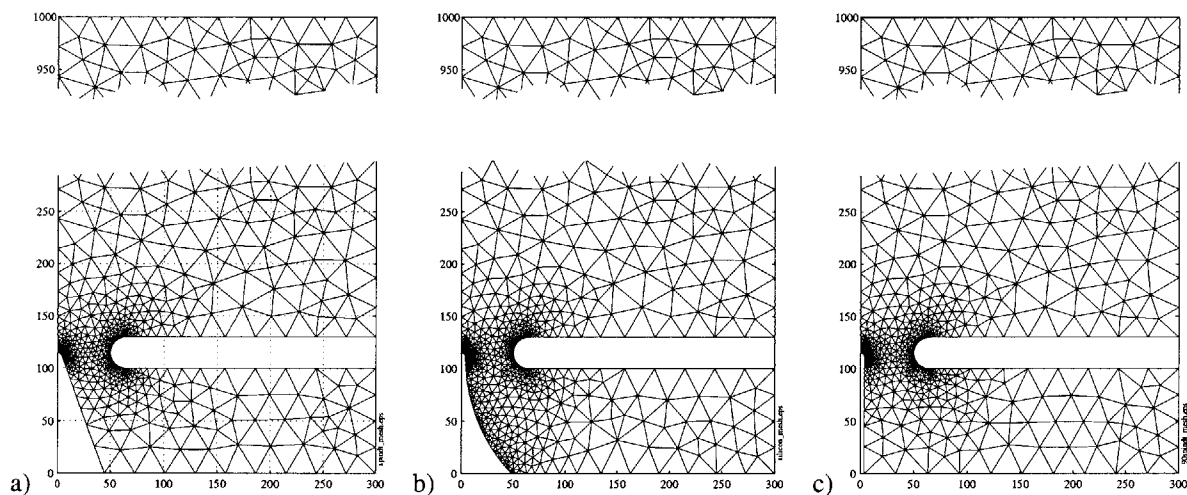
Figure 35: Three Cone Geometry

Three FEM models were built to analyze the cone shape on the surface electric field and device performance. From left to right are the Spindt shaped cone, the silicon shaped cone and the 'needle' shaped cone (which is analogous to the Spindt cone with a 90° base angle).

The results of the variation in cone shape are shown in Figure 36 where there is a 10% difference

in surface electric field between the Spindt cone and the needle shaped cone. The higher field

factor of the needle cone as compared to the Spindt cone is due to the fact that a larger portion of

the ball is exposed. This hemisphere on a post is closer than the rounded cone in structure to that

of the idealize ball in a sphere presented in Chapter 3 where all the field lines must terminate on

the small ball structure (resulting in the high surface field).

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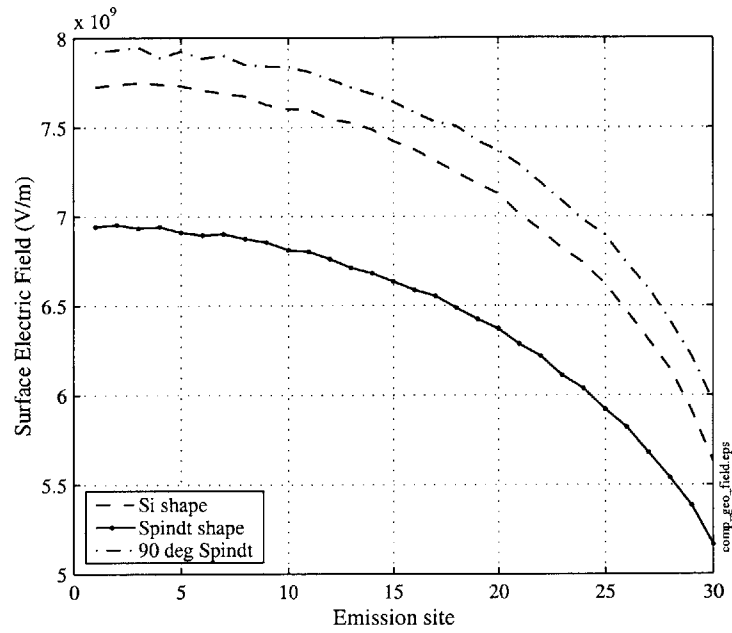
Figure 36: Comparison of Surface Electric Field for 3 Cone Geometry

The cones compared here are the typical 70° Spindt cone, the Silicon cone and the 90° Spindt cone. The radius of all cones is 4 nm and the gate aperture is 100 nm.
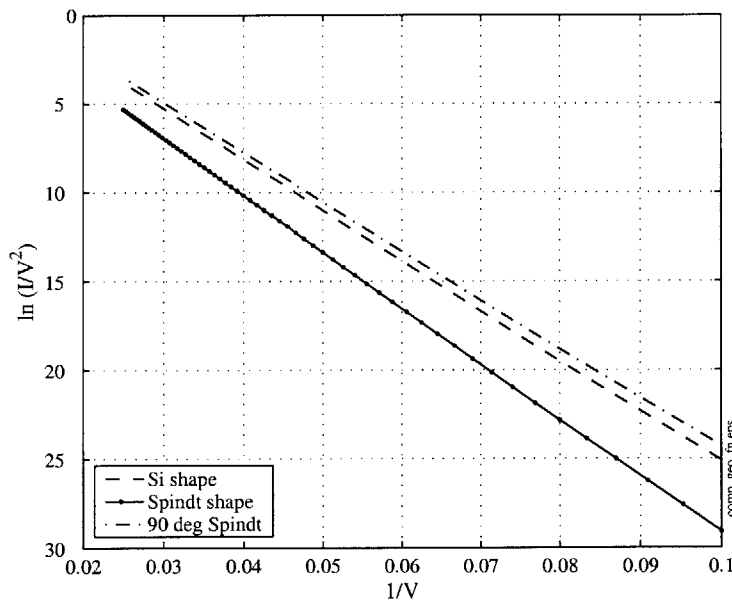
Figure 37: FN plot showing variation in device performance

The FN plot shows slight variation in slopes which relates to the field factor. The main variation is the intercept that relates to the effective emitting area. Based on the cone tip geometry, this is expected.

Although the different geometry imply different fabrication processes and different material, this comparison was done with a constant workfunction, ϕ = 4.5 eV which implies a molybdenum cone and shows the effects of the cone shape change. Assuming ϕ = 4.5 eV and Fowler-Nordheim theory, the device characteristics were compared using a FN plot.

In addition too variation in slope resulting from the different field factors, the simulations highlight the effect of cone shape on the effective emitting area, which can be seen by the shift downward in the FN plots shown in Figure 37. Variations in the effective emitting area predicted due to subtleties in the cone geometry could cause difficulties matching up simulation results with experimental results after determining the tip radius.

4.5.4 Tunneling Barriers for 100 nm aperture FEAs

The above analysis and most simulation work to predict the performance of FEAs are based on field emission device models, solving Poisson's equation subject to boundary conditions and using the Fowler Nordheim equation and surface electric field to determine the emitted current density. Because of the size regime of these models, there was a question to the validity of the Fowler Nordheim equation and the assumption of a triangular barrier. Earlier simulation work has investigated the effect of the shape of the barrier at the surface of the emission tip and the validity of the Fowler-Nordheim equation [80, 81, 82].

The solutions from the electrostatic simulations conducted in this work provided the electric field and potential over the entire solution space shown in Figure 20. Mapping the potential along a path normal to the surface forms a 1D-tunneling barrier. Although the electron may not travel in a perfectly straight path, this approximation was used based on the assumption that deviations

from this path would be due to the forces the electron experiences once it is outside the material

and beyond the barrier.
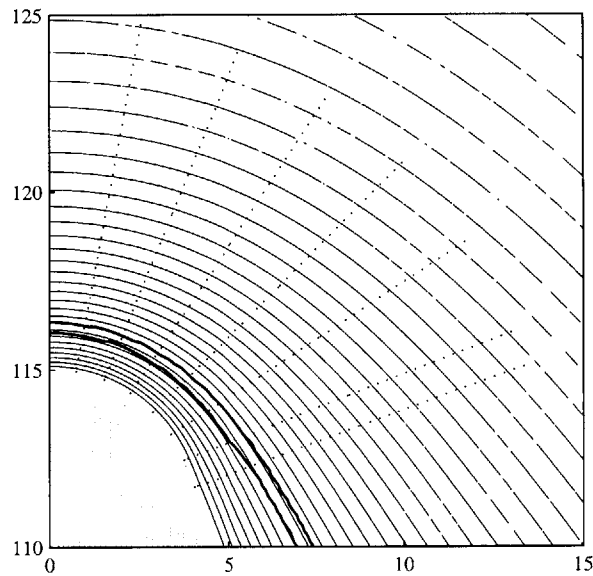
Figure 38: Contour plot of potential at tip surface.
The tip is shown as the gray shaded area. Contour lines show the potential around the
tip with the dotted lines showing the path the potential is measured along. The two dark
lines show the classical turning point furthest from the surface. The inner is for the
triangular barrier and the outer is for the real potential barrier.

Figure 38 shows a contour plot of the potential around the tip of a field emission cone. The

dotted lines are the paths where the potential is mapped out to construct a 'real' potential barrier

for comparison to the triangular barrier. The two thick lines indicate the location of the classical

turning points for the triangular barrier and the real potential barrier.

Figure 39 shows the profile of the potentials at three locations on the field emission tip. The

difference in the turning points can also be seen in the subplots as the point at which the potential

crosses the E = 0 dotted line.

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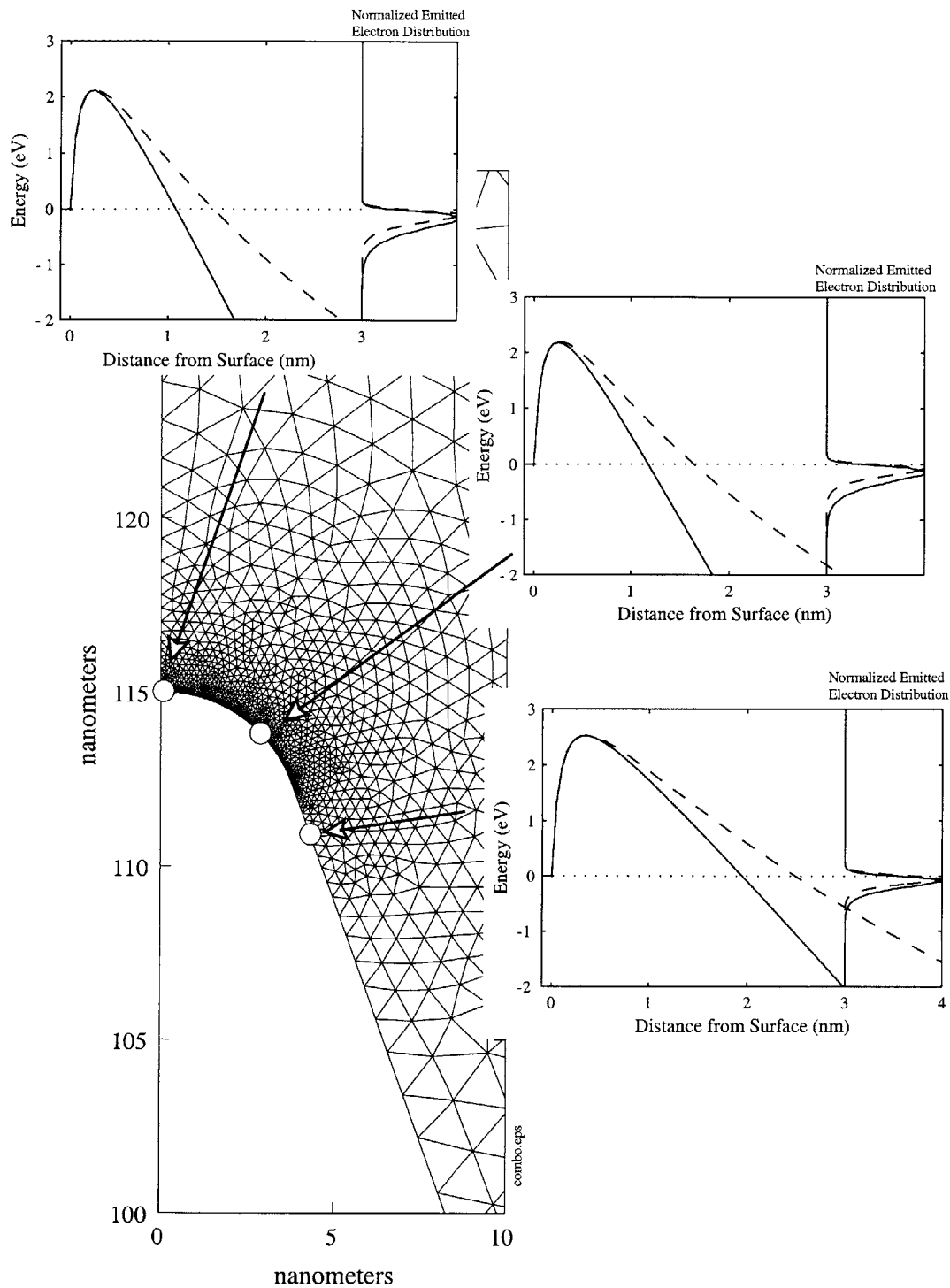
Figure 39: Barriers on different tip locations

Two barriers, traditional triangular (solid) and real potential (dashed) mapped in the simulation, are shown at different locations on the tip of a field emitter. Normalized emitted electron distributions are also shown.

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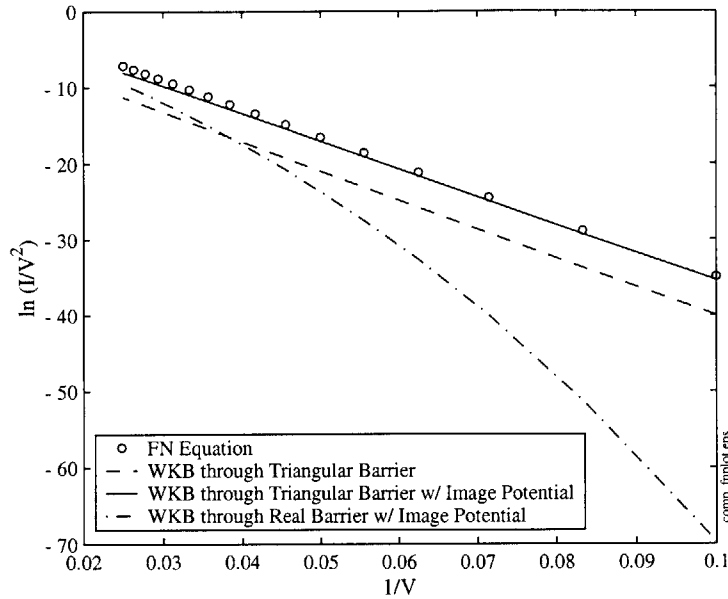
Figure 40: Fowler Nordheim Plot for different barriers

A comparison of using WKB to tunnel through the triangular barrier (no image potential), a triangular barrier with image potential, and a real barrier with image potential. These are overlaid with the standard Fowler Nordheim equation solution using the surface electric field.

4.5.4.1 IV Characteristics

The shape of the tunneling barriers discussed above determines the tunneling probability that in turn determines the emitted current density. It is the shape and width of the barrier above the Fermi level that we are most interested in. At low voltages, the width of the real barrier is much larger then the triangular barrier. As the voltage gets higher, the two barriers become similar. The result of this is shown in Figure 40 where the FN plot from the real barrier simulation is compared to the triangular barrier. At low voltages there is a large difference between the two, at higher voltages the two converge.

If real potential FN curve is analyzed using traditional FN analysis, the steeper slope at low voltages implies a lower field factor β that would indicate lower field factor.

4.5.4.2 Emitted Electron Energy Spread

The variation in the tunneling barrier width will not only lead to the difference in total emitted current, but will also change the electron energy distribution. The real potential gets wider more quickly as in energy is decreased. This will cause the transmission probability to decrease rapidly as a function of energy. The spread of the emitted electron energy would be narrower as shown in Figure 41.
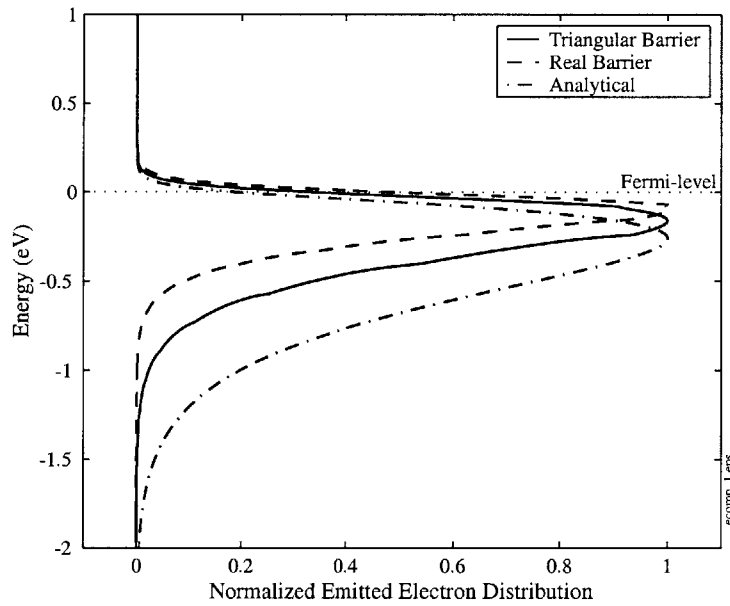
Figure 41: Spread in Emitted Electrons

The spread in emitted electrons is shown for the triangular barrier, real barrier (both calculated with numerical WKB), and analytical as described by P(E) in Appendix D.

Emitted electron distribution through the real potential barrier is shown in comparison to the normalized triangular barrier and the analytical solution as derived by Good and Mueller [123]. There is very good agreement in the shape above the Fermi-level where there is little difference in the barrier widths. There is significant variation below the Fermi-level.

4.5.5 Comparison with Experimental Results

One of the major concerns about the analysis of the barrier shape and the above FN plots is the comparison with experimental results. Experimental results that show the emission from tips traditionally form straight lines on the FN plot and agree with the standard FN theory. Figure 42 shows a comparison of some experimental results from a 100 nm aperture molybdenum tip. Over the range of the data, both the real potential and the data were linear. Unfortunately it was not possible to operate these ultra-small devices at higher gate voltages to examine the region to the left of the FN plot, because of oxide breakdown and device burn-out.
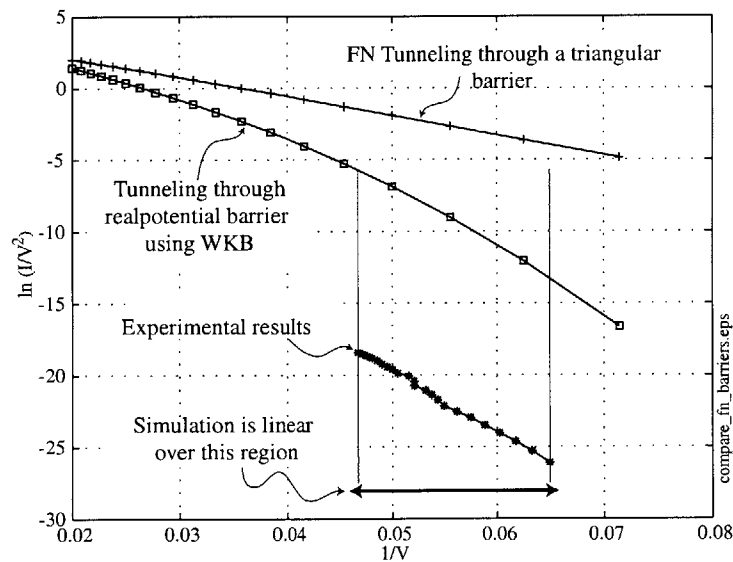
Figure 42: FN Plot comparing Experimental to Real Barrier Simulation
FN plot comparing the device characteristics from simulations using FN tunneling theory, WKB tunneling through a real potential barrier and experimental results from a 100 nm aperture Molybdenum FEA.
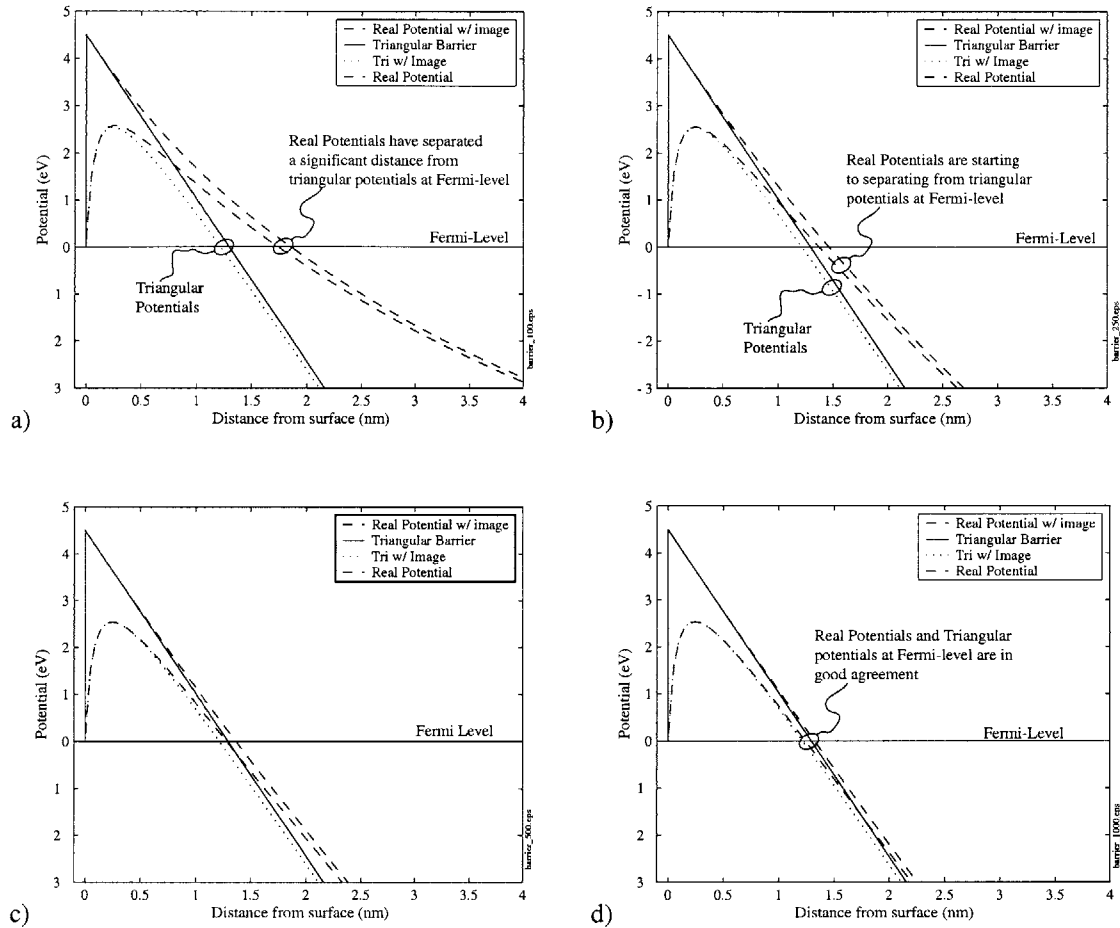
Figure 43: Variations in Tunneling Barrier with Scaling

The differences between the standard triangular barrier and the real potential barrier start to become pronounced in the 250 nm aperture device and become significant in the 100 nm aperture device. The above barriers show approximately the same surface electric field. All device geometry are scaled together as follows: a) 100 nm aperture, 4 nm radius tip, $V_g = 20V$; b) 250 nm aperture, 10 nm radius tip, $V_g = 50V$; c) 500 nm aperture, 20 nm radius tip, $V_g = 100V$; d) 1000 nm aperture, 40 nm radius tip, $V_g = 200V$.

4.5.6 <u>Changes in the Tunneling Barrier with Scaling</u>

Four models were built in order to determine the effects of device scaling on the tunneling barrier. The devices uniformly scaled from 100 nm aperture with a 4 nm tip radius up to a 1000 nm aperture with a 40 nm tip radius. Figure 43 shows that the agreement between the triangular barrier approximation and the real potential starts to break down only at the smallest device

geometries. To isolate the effects of the gate aperture and the tip radius, an additional 1000-nm aperture device was simulated with a 4-nm radius tip.

For comparison Figure 44 shows that the sharp tip in a large gate aperture device does have an effect on the barrier shape and there is a deviation from the assumed triangular barrier. For comparison of tunneling through the real barrier with the triangular barrier, it is most effective to examine the ratio of the two areas, (area of k(x) curve between the two classical turning points), under the barrier as presented in Chapter 3 and shown in Figure 13 where the area is calculated as

$$A_1 = \int_{x1}^{x2} k(x)dx,$$

and

$$k(x) = \sqrt{V(x) - E}.$$

For this calculation, the area, A_{real} or $A_{triangular}$, was measured as the area under the barrier and above the Fermi-level, which would relate to tunneling probability at Fermi-level ($E = E_F$). The ratio of the two areas was calculated as:

$$\gamma = \frac{A_{real}}{A_{triangular}}$$

Where a $\gamma > 1$ would indicate lower tunneling probability for electrons. The largest effect is due to the tip radius. Only models with the 4 nm radius show a large difference.
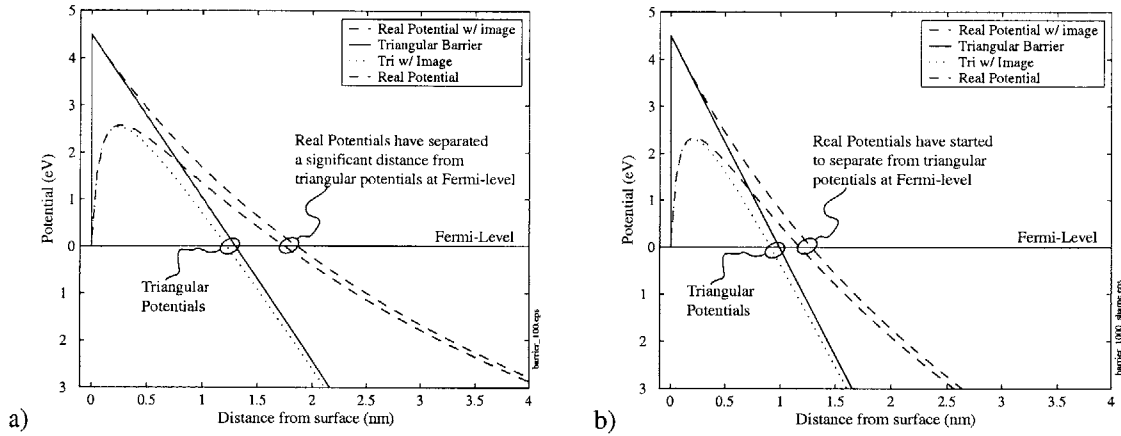
Figure 44: Tunneling Barrier for Sharp tip in Large Aperture

Tunneling barriers for a 1 μm aperture device with a 4 nm radius tip. The variation in the tunneling barriers starts to become evident with a sharp tip, but become significant when the aperture is scaled. a) 100 nm aperture, 4 nm radius tip, $V_g = 20V$; b) 1000 nm aperture, 4 nm radius tip, $V_g = 100V$

Table 4: Comparison of γ for various geometries

Aperture (nm)	Tip Radius (nm)	γ
100	4	1.33
250	10	1.08
500	20	1.02
1000	40	1.02
1000	4	1.24

4.6 SUMMARY

Numerical techniques used to predict field emitter device performance have been presented in this chapter. In particular, the numerical models have indicated that low gate voltage FEAs are feasible, and can operate at voltages near 10-15 volts. Modified tunneling barriers have also been studied to determine the ability to use traditional triangular barrier approximations for very small feature sizes. The comparison of these models to experimental data described in the next chapter indicates that the triangular barrier is acceptable over a range of operating voltages.

5 MOLYBDENUM SPINDT ARRAYS

Numerical modeling provided an excellent tool for the design of devices. Based on the scaling predictions that were presented above, a fabrication process was developed to construct 100-nm aperture FEA. The initial fabrication technique chosen was the Spindt process [4]. In this process, metal was evaporated through a small aperture that pinches off during the metal deposition, (causing the cone shape) to form the tip. Because of process compatibility concerns, almost all processing was done in the Technology Research Laboratory, which is not a standard CMOS fabrication laboratory.

Table 5: Laboratory Facilities

Technology Research Laboratory	TRL	Class 100 clean room for processing Silicon, III-V semiconductors, Au-contaminated substrates.	This lab was the main facility for work done on the Spindt arrays.
Integrated Circuits Laboratory	ICL	Class 10 clean room based on standard CMOS processing. All work is done on full 4 inch wafers, no pieces can be processed.	This lab was the main facility for the work done on the Silicon arrays.
Nanostructures Laboratory	NSL	Class 10 clean room (inner) and Class 10,000 clean room (outer) with unique equipment for working in the nano-size regime, x-ray lithography.	This lab was the main lab used to perform metrology on samples.
Space Nanotechnology Laboratory	SNL	Class 200 clean room with facilities that are dedicated to work on high-resolution x-ray gratings using interferometric lithography.	This was the facility where the Interferometric Lithography was done.
Research Group Laboratory		Individual Laboratories for the use by the research group. The lab used has test equipment for the analysis of device performance in a UHV probe-station.	Devices were characterized in the lab.

Table 5 shows a summary of the facilities that were used and supported this work (both Molybdenum and Silicon Arrays).

The beginning of this chapter presents the processing techniques and steps that are critical to the 100 nm aperture, (200 nm period) array process. These techniques include tri-level resist and interferometric lithography that are applicable to both the Spindt process and the silicon etch process that is presented in the next chapter. The remainder of this chapter will focus on the Spindt array fabrication process and the characterization of these devices.
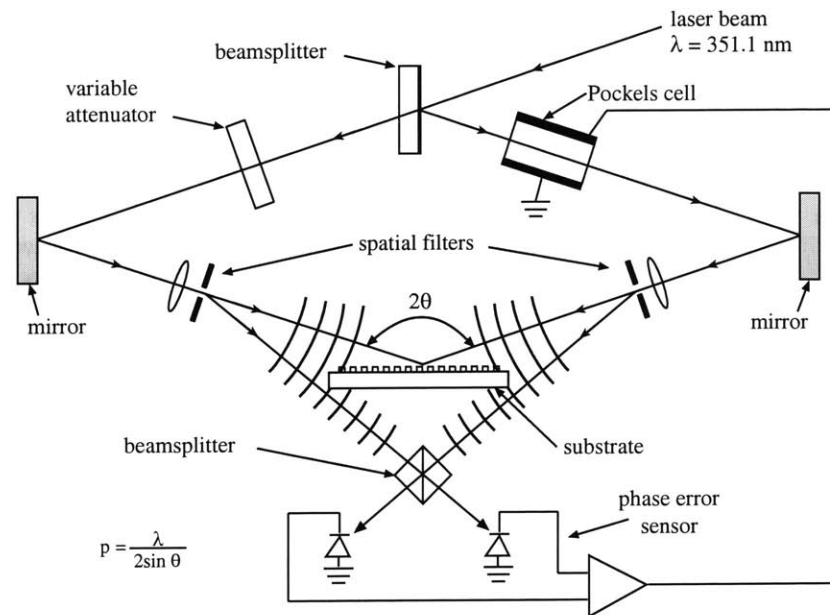
Figure 45: Schematic of MIT interference lithography (IL) system.
Fringes are stabilized in space by means of the feedback loop to the Pockels cell [85].

5.1 INTERFEROMETRIC LITHOGRAPHY

Device scaling required patterning features beyond the capability of traditional lithography in our facilities. The grid structure of the FEA lends itself to the use of interferometric lithography for patterning the array [5, 83, 84]. Interferometric lithography uses a laser beam that is split into

two and recombined to form a standing wave [85]. Two exposures orthogonal to each other form a post pattern in a positive resist.

A 351.1 nm wavelength Ar^+ laser was used to form a 200 nm period standing wave. The recombination angle for this period grating is $\theta = 61.37°$ as per:

$$p = \frac{\lambda}{2\sin\theta}.$$

IL with conventional thin single layer resist experienced difficulties in controlling resist line widths. This was primarily due to the standing wave that is formed from the highly reflective substrate. Because the size of the features from the IL will be used to define our gate aperture, a more sophisticated resist stack was necessary.

5.2 TRI-LEVEL RESIST PROCESS

In order to achieve the high contrast patterning with the interferometric lithography an anti-reflective coating (ARC, Brewers xHRi-16, [86]), was used. This layer was implemented to minimize the reflections from the substrate back into the photoresist, (PR, Sumitomo PFI-34A2, [87]). Good optical matching between PR and ARC could be obtained in a bi-level stack, however difficulties would occur during the transfer of the pattern from the PR to the ARC because both are organic and etched in O_2. To overcome the selectivity issue, a shadow evaporation would be done to form an oxide cap on the PR post. A tri-level structure was used to eliminate this shadow evaporation step [88]. The tri-level stack has a thin evaporated oxide layer in between the PR and ARC. The pattern was transferred to the oxide interlayer, and then to the ARC. Modeling of the tri-level stack on the substrate of interest was done to optimize the layer thickness.

Optical constants of the ARC were measured at J.A. Woollam Company using a Variable Angle of Incidence Spectroscopic Ellipsometer (VASE®) system. Each sample consisted of a single Brewer Science polymer antireflective (ARC) layer deposited onto a crystalline silicon substrate. Measurements were made over the spectral range 1.1 to 6.0 eV (207-1127 nm) in steps of 0.05 eV. Figure 46 show a plot of the optical constants as a function of wavelength. The n and k of interest were at $\lambda = 351.1$ nm where n = 1.677, k = 0.3649.
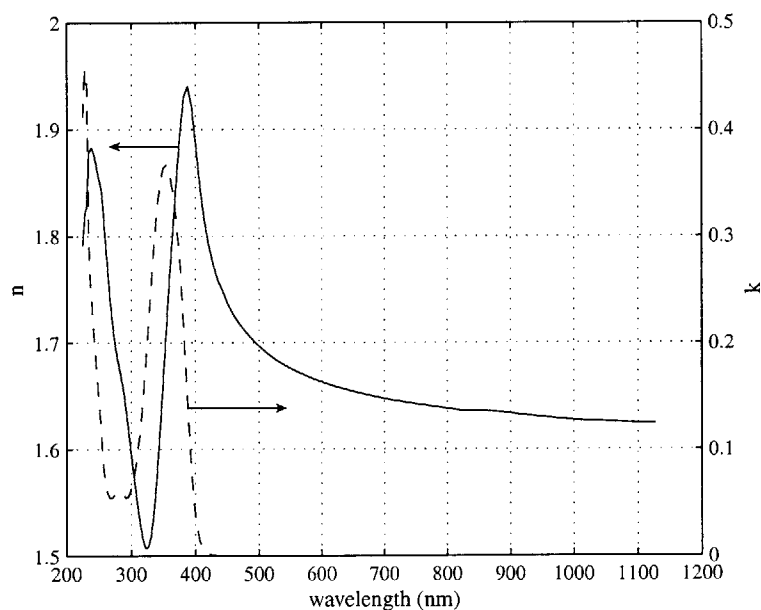
Figure 46: Optical constants n & k for Brewers xHRi-16

Optical constants n & k for Brewers xHRi-16 as a function of wavelength. The analyzed sample was a single layer of spun on dielectric on a single crystal silicon substrate. The sample was then baked on a hot plate at 180 °C for 1 minute.

The ARC layer thickness of the tri-level resist stack was optimized using optical modeling to minimize back reflection into the top photoresist layer as shown in Figure 47, [88]. The optimum ARC layer thickness for a silicon substrate with 100 nm of thermal oxide was 130 nm. The PR thickness was 200 nm and the oxide interlayer thickness was 15 nm.

90
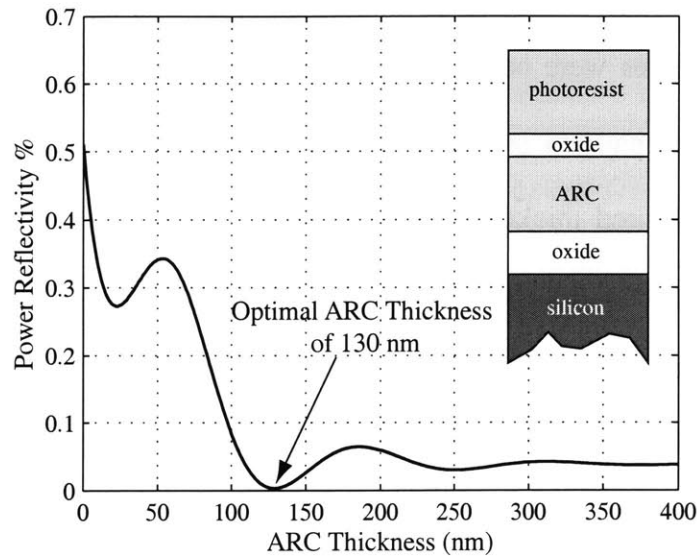
Figure 47: Optical Modeling of Tri-level stack

Using the optical properties above, the propagation of incident 351.1 nm wavelength light at an incidence of 61.37° is modeled in the layers as shown in the inset. A qualitative result shows the minimization of back-reflection into the photoresist at an ARC thickness of 130 nm.

5.3 MOLYBDENUM SPINDT ARRAYS

The initial sets of devices fabricated were classic Spindt cones made of Molybdenum. The gate metal was chromium and the gate dielectric was SiO_2. The devices were tested in a common cathode configuration; i.e. contact to all device cathodes is made by means of the test stage through the substrate.

5.3.1 Basic Cone Arrays

5.3.1.1 200 nm period Array Formation

The substrates are 100mm n-type Silicon Wafers. The gate oxide layer was formed by growing a 100 nm thick thermal oxide using a dry oxidation at 1000°C.

After a 5 minute UV ozone cleaning step, an Anti-Reflective Coating (ARC) was spun onto the substrate. The ARC was manually dispensed using a pipette [89] and pipette gun. The ARC was

dispensed onto a slowly rotating wafer, followed by a spread step and the final high-speed spin. The ARC coated substrates were baked in an oven at 180°C for 30 minutes. Because of the small feature sizes of the patterns etched, all pipettes have been pre-cleaned using a SC-1 [90]. Determination of the desired thickness of this coating is described earlier. For the 100 nm underlying oxide, the optimal thickness for the Brewers xHRi series ARC is 130 nm. An oxide interlayer was deposited onto the substrates in an e-beam evaporator. Because the substrates are still planar and featureless, planetary wafer holders were used to improve the film uniformity. An additional 5-minute UV ozone clean was performed prior to coating the wafers with HMDS in a vapor prime oven. The Sumitomo PFI-34A2 photoresist was also manually dispensed using the same technique as the ARC described above. The target thickness of the photoresist was 200 nm. The PR coated wafers were baked in an oven at 90°C for 30 minutes.
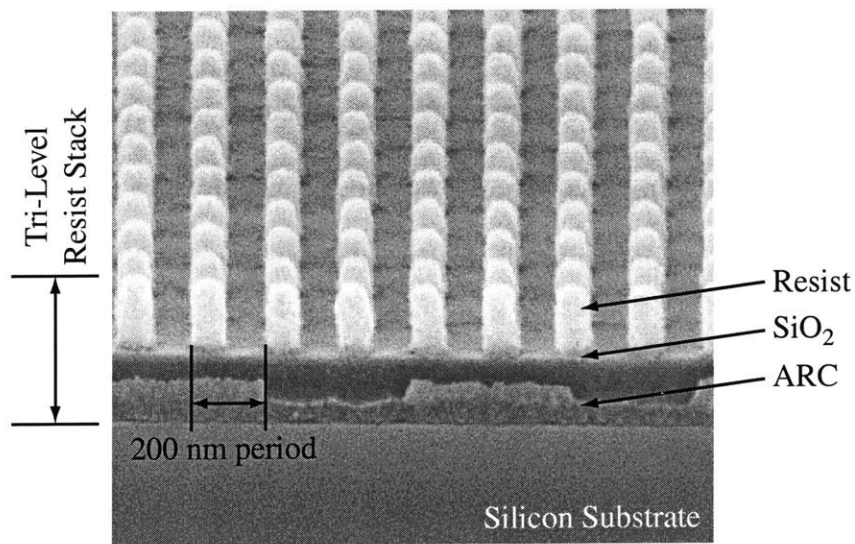
Figure 48: Posts of Photoresist after Interferometric Lithography
The 200 nm period posts show equal 1:1 line to post spacing. For the Spindt cone process, the diameter of the PR and subsequent ARC posts defines the gate aperture.

Wafers were subsequently brought to the Center for Space Research to be exposed using the Interferometric Lithography System (see Figure 45). Two exposures were performed; the second with the wafer rotated 90°. Each exposure dose was an 18.5 mJ/cm^2 exposure. The proper exposure and develop was verified using a scanning electron microscope. Figure 48 shows the photoresist posts after exposure and developing.

5.3.1.2 Tri-level etch and Gate Formation

The substrates were then etched in a reactive ion etcher to anisotropically transfer the pattern from the photoresist to the underlying ARC. This etch was done in a Plasmaquest ECR/RF reactive ion etcher. The etch consisted of a short descum followed by a CF$_4$ RIE to pattern the interlayer, and an O$_2$ RIE to pattern the ARC. Figure 49 shows the posts of ARC after the reactive ion etch.
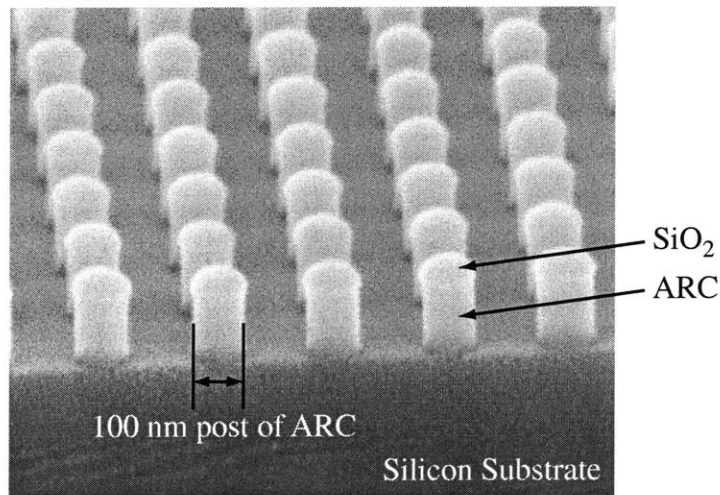
Figure 49: Posts of ARC after Pattern Transfer from photoresist
The thin caps on top of the ARC are the remains of the SiO$_2$ interlayer. The photoresist acts as mask for the interlayer etch, which then in turn acts as a mask for the ARC etch.

The posts of ARC acted as a lift-off mask for the deposition of the Chromium gate. 40 nm of chromium was evaporated using a special wafer chuck that holds the wafer directly above the source in the TRL e-beam evaporator [91] and rotates the wafer about its center axis. The ARC posts were then lifted off in Nanostrip [92], which is a derivative of the Piranha etch, (1:3 H_2O_2:H_2SO_4), that does not attack chromium.

5.3.1.3 Gate Oxide Etch

The resulting chromium hole pattern was then used as a mask to reactively ion etch through the gate oxide to expose the substrate for cone deposition. The oxide etch was a CF_4 RIE in an ECR plasma systems, [Plasmaquest], at a pressure of 50 mT. Figure 50 shows the gate oxide etched using the chromium gate as the mask.
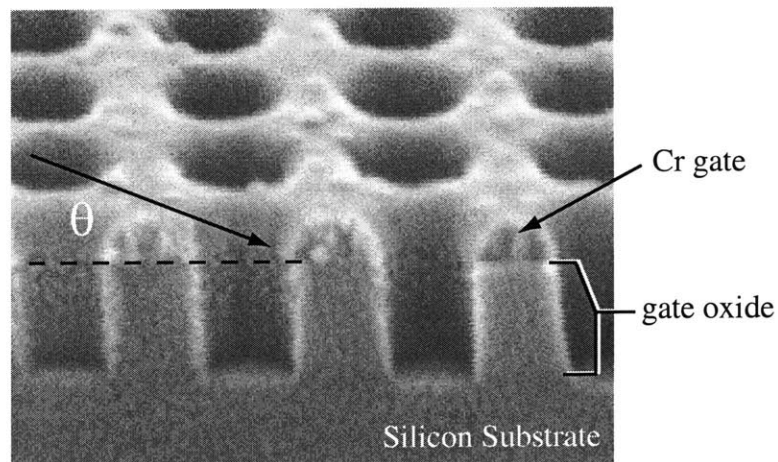
Figure 50: Gate oxide etched in a CF₄ RIE

5.3.1.4 Cone Formation

The resulting structure shown in Figure 50 was then ready for the Spindt cone deposition process. A 10-nm sacrificial parting layer of either Al or Al_2O_3 was evaporated at a glancing angle (θ shown in Figure 50) to cover the gate, but not to enter the 'silo' formed in the oxide. A

special wafer chuck was made to hold the substrate at an angle directly above the evaporator source while rotating the wafer on its center axis. After the parting layer was deposited the fixture was adjusted so the evaporation of the molybdenum was normal to the surface. The cone forms as molybdenum that was deposited on the gate slowly pinches off the aperture. Typically 150 - 200 nm of molybdenum was evaporated. Figure 51 shows the molybdenum cones.
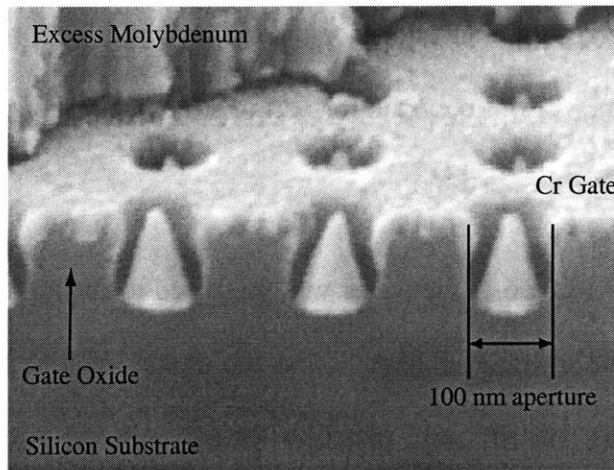
Figure 51: 100 nm Aperture Molybdenum Field Emitters
The Emitter array with Molybdenum cones shows the excess Molybdenum that is the result of the vertical cone deposition process.
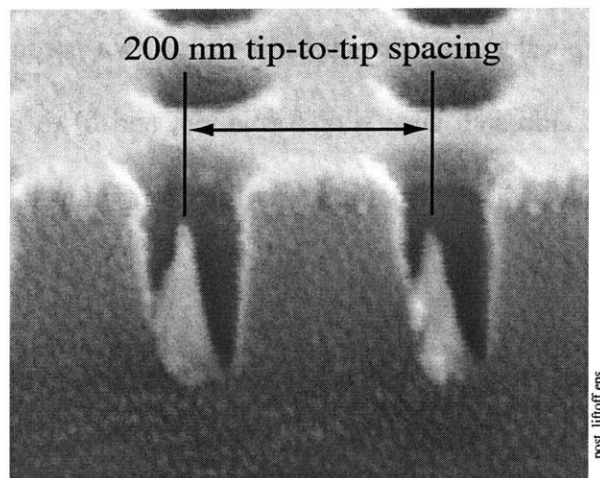
Figure 52: Emitter cones after the final lift-off step

After the cones were formed, the sacrificial layer was etched and the excess molybdenum was lifted-off. This was done in a NaOH bath with moderate ultrasonic agitation.

5.3.2 Device Fabrication

The above process was used as a proof of concept to show the cone formation process was feasible. Because the interferometric lithography is a maskless technique, cones are formed everywhere. This section describes the additional steps required for forming devices that can be electrically probed. The steps limit the cone formation to device regions, and pattern the gates to provide discrete devices on the substrate.

After the removal of the ARC posts the wafer was patterned to define the device regions. Mask #1 was used to pattern these features, (that define the device region) by protecting the device region during an additional lift-off step, (the first lift-off with the ARC left a layer with gate apertures everywhere, the second Cr lift-off fills the apertures except in the device region.). This mask was designed to be used with an image reversal process to leave large patterns of photoresist (10 × 10 µm, 100 × 100 µm, 500 × 500 µm squares) that protect the gate with 100 nm holes. Chromium was evaporated onto the substrate serves two purposes; a) fill in the 100 nm holes to prevent the gate oxide etch and 'silo' formation, and b) to provide a thicker layer of chromium for pads, and leads. The chromium was lifted-off in acetone. Figure 53 shows the patterns formed by Masks #1 and #2.

To pattern discrete devices, an additional lithography step was performed after the vertical Molybdenum evaporation. A standard positive photoresist was exposed using Mask #2 to form patterns that will become the pads, which allow electrical connection to the gates of the devices. The photoresist was the etch mask for the underlying layers of molybdenum, the parting layer

and the underlying chromium gate. The etch stopped on the gate oxide. In addition to isolating the individual devices, the etch facilitated the lift-off of the excess molybdenum. Compared to lifting off an entire 4" wafer, the small features shown above in Figure 53 were easier to undercut during lift-off.
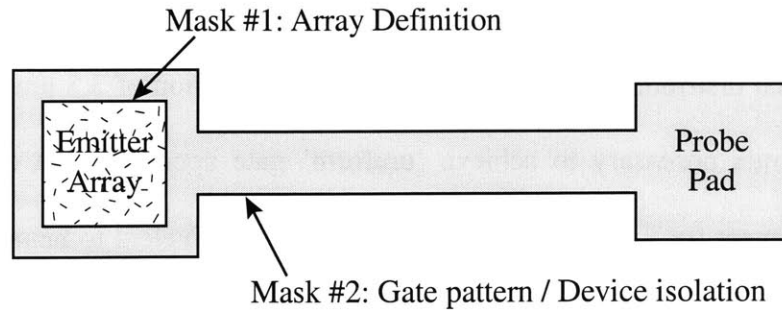
Figure 53: Masks for Spindt Cone Process

Mask #1 is a dark field mask because it will be used with an image reversal process. The negative side-wall slope from the image reversal will allow for an easier lift-off. Emitter arrays varied in size from 10μm to 500μm. Mask #2 is a light field mask and will be used to pattern standard photoresist to form an etch mask. Pad size as defined by mask #2 was 300 μm.
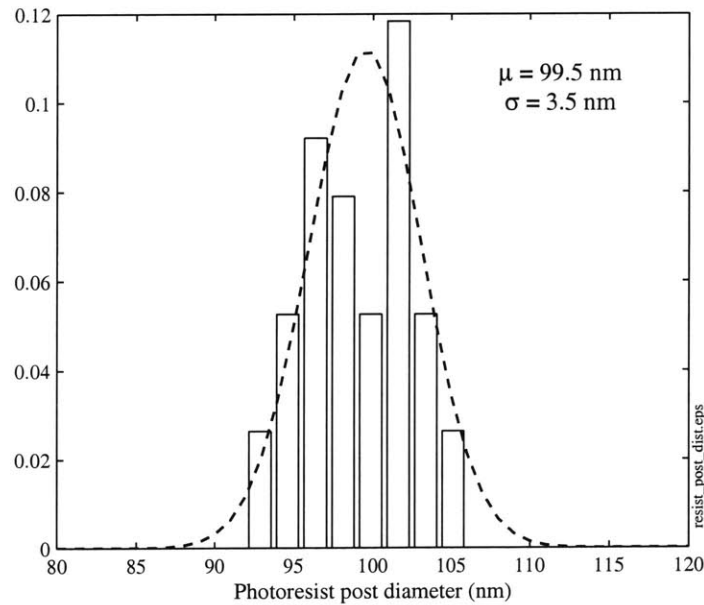
Figure 54: Distribution in photoresist post size from IL

5.4 ARRAY ANALYSIS

The post of PR is the feature whose pattern indirectly defines the gate aperture in the Cr lift-off. In order to understand sources of variation in the gate aperture, the diameter of the posts of PR were measured prior to the reactive ion etch which transfers the pattern to the interlayer and then into the ARC. The results of these measurements are shown in Figure 54.

When fit to a normal distribution, the data has a standard deviation of 3.5 nm. This variation is well within the limits necessary to achieve 'uniform' gate apertures. In comparison to the lithography requirement for FED production, this would be equivalent to being with 2σ of the $\pm$ 7% that is required for the gate aperture [93].

5.5 DEVICE CHARACTERIZATION

5.5.1 Test Configuration

Devices were tested in an UHV probestation. The system has two chambers, a main test chamber and a load-lock/conditioning chamber. The load-lock/conditioning chamber was pumped by a 160 l/s turbo pump and can quickly achieve pressures below 10^{-8} torr. This chamber has a heated stage in order to bake the wafer and desorb surface contaminants [94]. Substrates were baked at 200° for an hour prior to testing. The substrate was then transferred to the main chamber by means of a magnetically coupled transfer arm. The main chamber was pumped by a 220 l/s ion pump and can achieve pressures of 10^{-10} torr. This chamber has an electrically isolated XYZ stage (2" travel, 2" travel, and 8" travel respectively) and 4 independent XYZ probes/feedthroughs (1" travel in all directions). The chamber can be configured to have needle probes, an anode ball, a planar metal anode, and/or a phosphor coated screen.
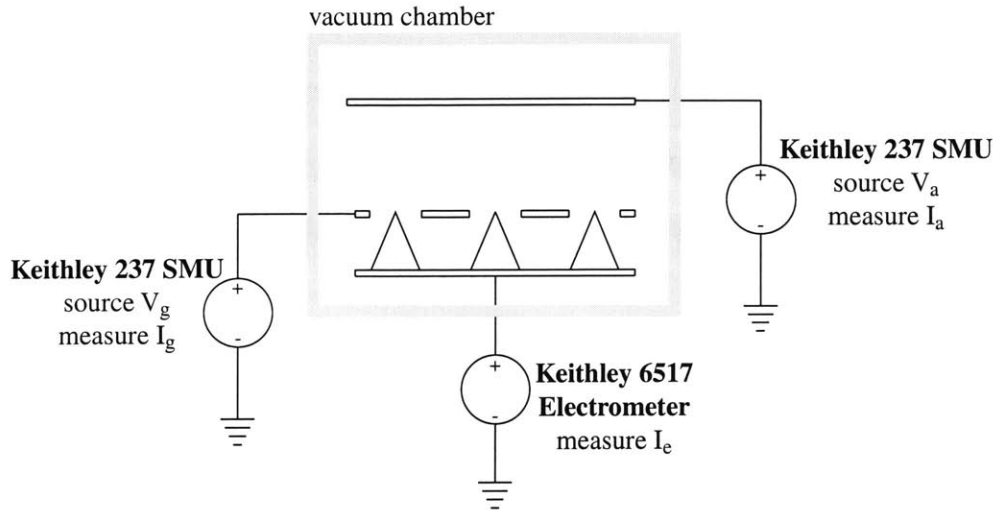
Figure 55: Configuration of Device in Test System
The device is held in the main chamber of the vacuum test system on an electrically isolated stage that is connected to ground through a Keithley 6517 Electrometer. The gate and anode are connected by probe arms to Keithley 237 high voltage source measurement units (SMU).

Electrical characterization for this work was done with a single probe for a gate contact, the cathode contact through the stage, and a nickel ball as the anode.

5.5.2 Molybdenum Spindt Arrays

Field emitter arrays with sizes of 100 μm^2, 500 μm^2 and 1000 μm^2 were characterized with the anode potential fixed at 600 V. The gate voltage was increased from ground until the onset of field emission, (a few nano-amps from the array). Devices turned on at voltages as low as 12 volts. After field emission was observed from a device, the gate voltage was ramped very slowly (often over many hours) up until the current is approximately 1 μA from the array. Once the anode current has stabilized, the gate was swept over a voltage range of interest, and the I_{anode}-V_{gate} information was collected.

5.5.2.1 Transfer IV Characteristics

A IV transfer characteristic and a Fowler Nordheim plot, are shown for a 100 μm × 100 μm array

of field emitters in Figure 56. With a cone density of 2.5 × 10^9 cones/cm^2, there are

approximately 250,000 cones in this array. This device operated in the range of 16 - 21 V.
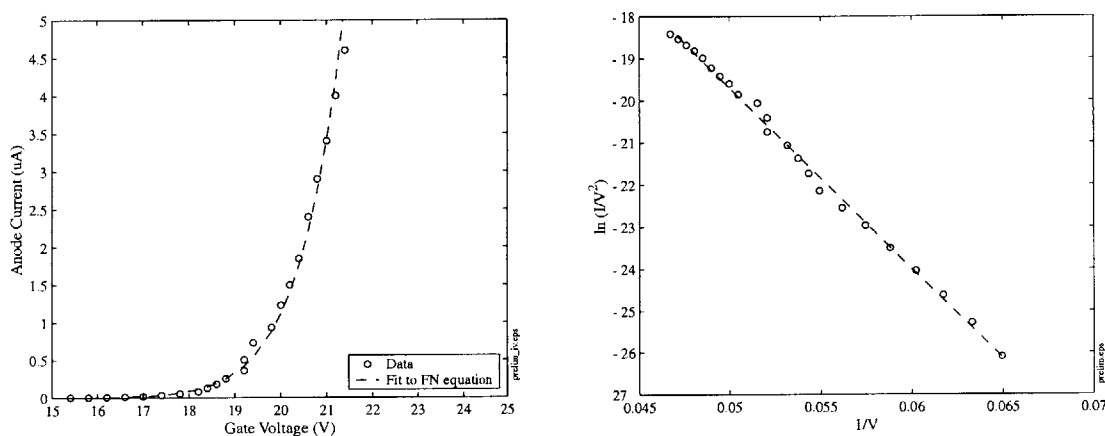
Figure 56: IV and FN for 100 nm aperture Molybdenum Array (4_25_1)
Anode current vs. Gate voltage and FN plot for array 4_25_1, 100 × 100 μm, tested at 5
× 10^{-10} torr. Fowler Nordheim coefficients: $a_{FN} = 3.3 \times 10^{-4}$, $b_{FN} = 370$, $\alpha = 1.6 \times 10^{-9}$,
$\beta = 1.8 \times 10^6$. The lines are the fit to the Fowler Nordheim equation, which is used to
extract the coefficients above.

The transfer IV characteristics of other devices are shown in Figure 57 through Figure 61. These

devices were also characterized under similar conditions.

100
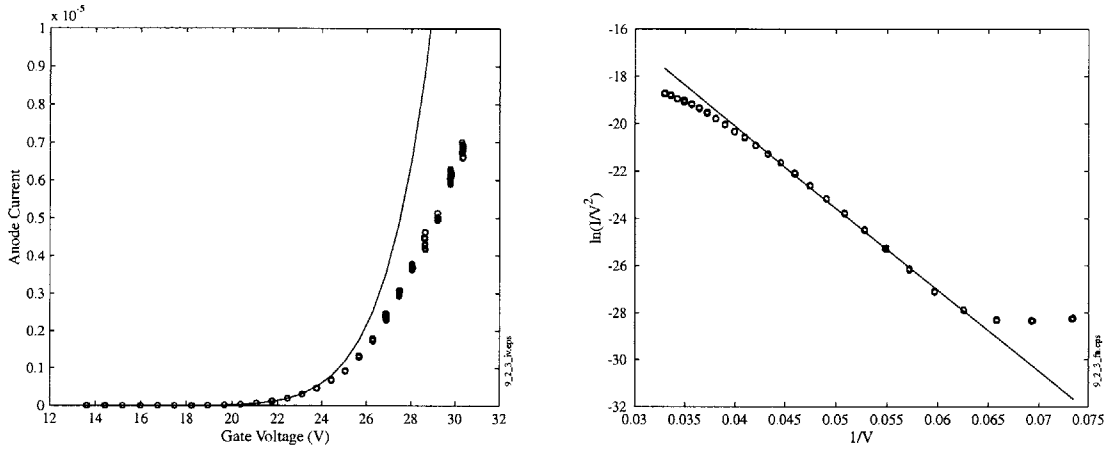
Figure 57: IV and FN for 100 nm aperture Molybdenum Array (9_2_3)

Anode current vs. Gate voltage and FN plot for array 9_2_3, 100 × 100 μm, tested at 5 ×
10^{-10} torr. Fowler Nordheim coefficients: $a_{FN} = 3.3 \times 10^{-4}$, $b_{FN} = 370$, $\alpha = 1.6 \times 10^{-9}$, β
$= 1.8 \times 10^{6}$. The lines are the fit to the Fowler Nordheim equation, which is used to
extract the coefficients above.

Figure 58: IV and FN for 100 nm aperture Molybdenum Array (9_2_5)

Anode current vs. Gate voltage and FN plot for array 9_2_5, 50 × 50 μm, tested at 5 ×
10^{-10} torr. Fowler Nordheim coefficients: $a_{FN} = 1.9 \times 10^{-2}$, $b_{FN} = 346$, $\alpha = 8.2 \times 10^{-9}$, $\beta =$
1.8×10^{6}. The lines are the fit to the Fowler Nordheim equation, which is used to extract
the coefficients above.

101
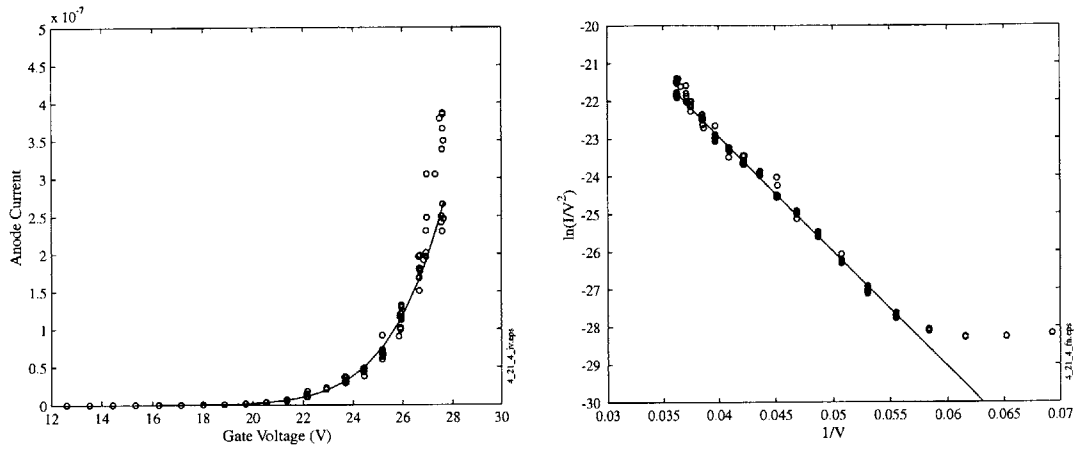
Figure 59: IV and FN for 100 nm aperture Molybdenum Array (4_21_4)

Anode current vs. Gate voltage and FN plot for array 4_21_4, 100 × 100 μm, tested at 5 × 10^{-10} torr. Fowler Nordheim coefficients: a_{FN} = 2.2 × 10^{-5}, b_{FN} = 305, α = 7.3 × 10^{-11}, β = 2.0 × 10^{6}. The lines are the fit to the Fowler Nordheim equation, which is used to extract the coefficients above.
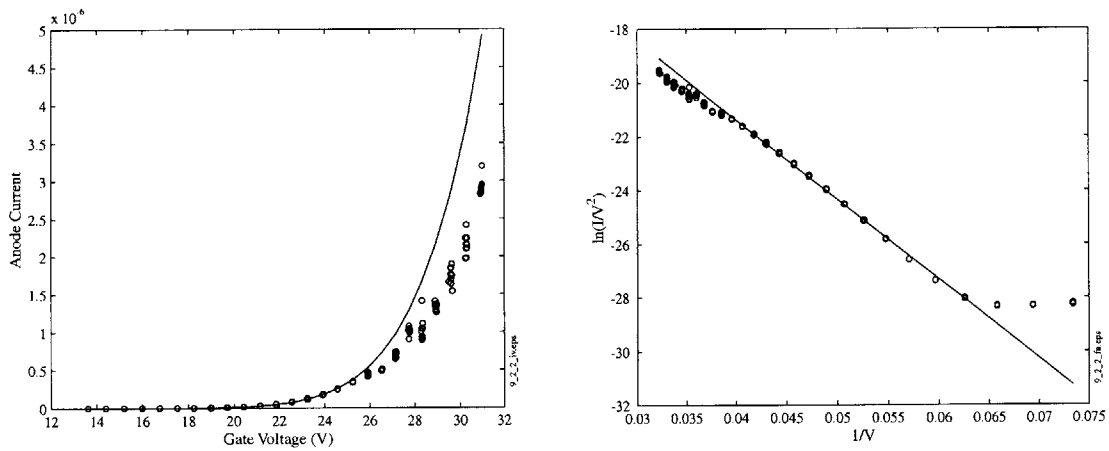
Figure 60: IV and FN for 100 nm aperture Molybdenum Array (9_2_2)

Anode current vs. Gate voltage and FN plot for array 9_2_2, 50 × 50 μm, tested at 5 × 10^{-10} torr. Fowler Nordheim coefficients: a_{FN} = 7.1 × 10^{-5}, b_{FN} = 295, α = 2.2 × 10^{-10}, β = 2.1 × 10^{6}. The lines are the fit to the Fowler Nordheim equation, which is used to extract the coefficients above.

102
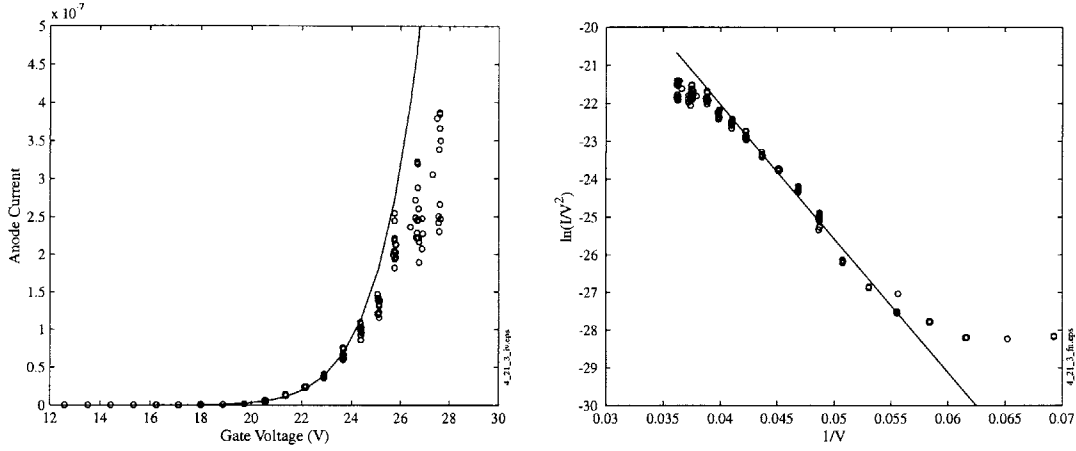
Figure 61: IV and FN for 100 nm aperture Molybdenum Array (4_21_3)

Anode current vs. Gate voltage and FN plot for array 4_21_3, 100 ×100 μm, tested at 5 ×10⁻¹⁰ torr. Fowler Nordheim coefficients: $a_{FN} = 3.8 \times 10^{-5}$, $b_{FN} = 354$, $\alpha = 1.7 \times 10^{-9}$, $\beta = 1.7 \times 10^{6}$. The lines are the fit to the Fowler Nordheim equation, which is used to extract the coefficients above.

Table 6: Summary of Device characteristics for Molybdenum arrays

	Type	Array Size	a_{FN}	b_{FN}	α	β
4_25_1	Molybdenum	100 × 100 μm	3.3×10^{-4}	370	1.6×10^{-9}	1.8×10^{6}
9_2_3	Molybdenum	100 × 100 μm	1.9×10^{-2}	346	8.2×10^{-9}	1.8×10^{6}
9_2_5	Molybdenum	50 × 50 μm	1.9×10^{-2}	348	8.1×10^{-9}	1.7×10^{6}
4_21_4	Molybdenum	100 × 100 μm	2.2×10^{-5}	305	7.3×10^{-11}	2.0×10^{6}
9_2_2	Molybdenum	50 × 50 μm	7.1×10^{-5}	295	2.2×10^{-10}	2.1×10^{6}
4_21_3	Molybdenum	100 × 100 μm	3.8×10^{-5}	354	1.7×10^{-9}	1.7×10^{6}

The electrical characterizations above indicate that initial predictions by the theory and simulation are qualitatively correct and device performance in terms of low voltage operation has improved. The variation in device performance as presented in Table 6 is small when comparing the field factors β and the radii, (calculated by different methods), shown in Table 7. The large variations in the effective emitting area are less pronounced when normalized against the values

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that compensate for the changes in tip radii. The variations in performance were therefore attributed to variations in the tip radius distribution that is addressed below.

The process presented here is similar to a Lincoln Laboratory, (LL), process that used 320 nm period IL to pattern the gate apertures [5]. The devices in this work did exhibit turn on voltages of approximately 5 volts less then the LL devices reported. The LL devices have lower field factors (indicating a larger tip radius, b_{FN} = 420 and β = 1.3×10^6) and higher effective emitting area for a smaller (900 tip) array. The effective emitting area was so large that it was actually larger then the reported array dimensions.

Another process that was based on the Molybdenum process that was an extension of this work was reported by Choi, et al [95]. The results of their characterization indicated higher field factor resulting in a lower turn on voltage than reported here by approximately 3 volts. One explanation for the higher field factor (b_{FN} = 125, and β = 4.4×10^6), may be the shape of the molybdenum cone. Choi shows a micrograph of a molybdenum cone that exhibits very vertical neck, as opposed the traditional triangular shape, but the tip radius measured is 9 nm which can not account for the high field factor. The effective emitting area presented in this work is at least 1 order of magnitude more than presented by Choi.

The three sets of data above show a trend of improved device performance as β increases even though there is a decrease in effective emitting area α. Even at the 100 nm size regime, the tip radius will play a dominant role in determining the device performance showing an increase in performance as β increases and α decreases.

Other work has explored the emission from nano-scale emitter structures. Driskill-Smith presents a process where 2.5 nm grains of AuPd are deposited onto a surface and used as a mask for a 10 nm deep etch into an underlying tungsten layer [96]. Although this work differs in process from the Spindt cone deposition work, it is exploring a smaller size regime of emission from metal, and achieves the nano-patterning without lithography. The results reported indicate higher field factor than any of the Spindt cone work above, $\beta = 5.8 \times 10^6$, but their emission area is 4 to 5 orders of magnitude less than reported by this work. No data was provided for voltages above 15 V, and the highest reported current was 10 nA. A low turn-on voltage of below 10 V is claimed, but the data indicates that this was demonstrated only when the anode was at 15 V, (the anode was <100 nm from the cathode and would increase the surface electric field). It was difficult to predict what the performance of these devices will be, or their limitations due to physical mechanisms as voltages and currents increase. The structure has a sharp tip, but supplying current to that tip, even in metal, may become an issue.

Additional work relating to the application of a LV-FEA to a flat display has been reported by Candescent Technologies. Although specific characterization data on the performance of the FEA was not presented, the work does report emission currents of 50 µA at a gate voltage of 30 V for a FEA with gate aperture below 150 nm [104].

Some devices tested showed saturation effects at high currents where they deviated from FN behavior. Two possible causes for this were considered to be additional resistance in the system and/or space charge effects. A deviation due to additional resistance would require an additional 200 kΩ in the system, (test apparatus, or internal to the device testing). This magnitude of resistance could not be attributed to either the resistance of the sharp tip, or the contact between

the tip and the substrate. Variations in the resistors built into the test systems would not account for more then a small percentage of the additional 200 kΩ required. Rathman, *et al*, attributes the saturation effect on beam overlap in high-packing-density vacuum-microtriode arrays, [97]. The simulation that Rathman presents does not take into account the variation in emission across the array due to variations in tip radii and predicts uniform emission from each of the tightly packed tips. Based on the tip radii analysis presented in Chapter 6, the effect of the tightly packed array will not play a role in the devices presented in this work. Bozler, et al, proposed the most reasonable explanation relating the space charge effect to the low anode field. [5]. The combination of the low gate voltage and the low anode field will result in space charge that will cause the deflection of electrons back to the gate.

The deviation from FN theory was also examined in light of the barrier analysis presented in Chapter 4. The experimental data presented has a transition from a linear region a saturated region on the FN plot to the curve. The analysis presented in Chapter 4 indicated a continuous gradual change in the slope and intercept on the FN plot. Base on this difference, the deviation of the experimental data from FN theory is not attributed to variations in tunneling barrier shape.

5.5.2.2 *Analysis of Molybdenum Arrays using Numerical Simulation*

An analysis of the experimental data was performed by comparing experimental results with the simulation. Figure 62 shows the process flow and assumptions that were made for this analysis. A sensitivity analysis of the material workfunction was done to determine how small errors in this value would affect the analysis results. A change in the assumed workfunction by ± 3% resulted in a change of the radius necessary to match the experimental slope by ± 3 %. The

subsequent comparison of $\alpha_{experimental}$ to $\alpha_{simulation}$ using the above radius introduced no <u>additional</u>

error as long as the same assumed workfunction was used in the calculation of α.

EXPERIMENTAL

Measure Device IV
Characteristics

↓

Construct FN plot and
measure slope (b_{FN}) and
intercept (a_{FN})

↓

Determine α_{exp} and β_{exp}
corresponding to the
measured a_{FN} and b_{FN}

Assume ϕ for the material
and the use Fowler Nordheim
Theory

COMPARISON

Determine which simulated
radius matches slope from
measured FN plot (measured
b_{FN} = simulated b_{FN})

↓

Compare measured a_{FN} to
simulated a_{FN}.

NUMERICAL SIMULATION

Measure gate aperture
and large geometric features

↓

Perform electrostatic
simulations with varied tip
radius.

↓

Calculate device IV
characteristics, calculate
slope (b_{FN}) and intercept
(a_{FN}) as a function of tip
radius

↓

Determine α_{sim} and β_{sim} as a
function of tip radius

Figure 62: Process for Array Analysis using Numerical Simulation
In addition to providing insight into the effects of device scaling, the numerical simulation can be used to perform array analysis based on measured IV data. The process of comparing the experimental data and simulation requires certain assumptions are properly included in both results.

In order to match the slope (b_{FN}) of the experimental data for the molybdenum arrays, a simulation model was developed based on a device with 100-nm gate aperture, 4-nm tip radius of curvature and 75 degree cone angle. The simulation indicates a higher value of the intercept, (a_{FN}), indicating an effective emitting area larger than the experimental results by the factors

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shown in Table 7. This difference in the effective emitting area is attributed to the distribution of cone tip radii in the array tested. We estimated the proportion of cones emitting to be 1.5×10^{-3} for the array in Figure 63 by comparing the data to the simulation results. The SEM in Figure 63 shows a tip with radius of 6 - 7 nm indicating that sharp tips do exist in the array. Further SEM work was conducted and 50 tips were sampled. The mean tip size was ~12.5 nm with a standard deviation of 2.6 nm (these measurements do not take into account the affect of grain size in the tip geometry). This distribution also confirms the possibility of a small percentage of the tips having a 4-nm radius. Based on the analysis of tip radius that is presented in Chapter 6, a small group of sharp tips can dominate array behavior. The electrical characterization of such an array would indicate a field factor and effective emitting area from only the sharpest tips.

Table 7: Tip radius analysis for Molybdenum arrays

	Tip radius used in numerical simulation to match experimental slope.	Ratio of $\alpha_{measured}$ to $\alpha_{simulation}$	Tip radius calculated using $\beta_{experimental}$ by ball in sphere model (assuming aperture of 100 nm)	Tip radius calculated using $r = 1/\beta_{experimental}$
4_25_1	4.5 nm	0.0015	5.2 nm	5.5 nm
9_2_3	4.5 nm	0.003	5.2 nm	5.5 nm
9_2_5	4.6 nm	0.003	5.5 nm	5.8 nm
4_21_4	4.0 nm	0.0005	4.7 nm	5.0 nm
9_2_2	3.9 nm	0.0003	4.5 nm	4.7 nm
4_21_3	4.6 nm	0.001	5.5 nm	5.8 nm

The lift-off cone deposition process as implemented in this work had a lower limit. If is only effective until the aperture is closed off to a size of approximately 10 nm (2x the radius). An analogy can be drawn between the final segment of the cone deposition and lift-off process for tip fabrication and the lift-off process used to nanofabricate single electron devices. Chen and Ahmed reported difficulty obtaining continuous sub-10-nm lines using lift-off after an e-beam

deposition, and moved to an ionized beam deposition technique, which gave smaller grain size [98]. Other literature confirms this 10 nm limit for lift-off and also attribute it to the metal deposition [99, 100]. The purpose of this comparison is not to predict that feature size could not be below 10 nm with a lift-off process. In fact the electrical data from Choi (presented above) [95], indicates a sub 5-nm feature, and Goodhue presented at TEM image of a single Mo tip that exhibited features, (grain size) below 5 nm [101], (no statistical data on tip radius distribution was presented). The purpose of this analogy is to show that feature definition by lift-off in the sub-10 nm regime is at the limit of the process capability and variation in the results can occur, possibly due to grain growth. This can lead to a tip radius distribution that would result in an experimental calculation of an effective emitting area that is smaller than the simulation that assumes a uniform array.
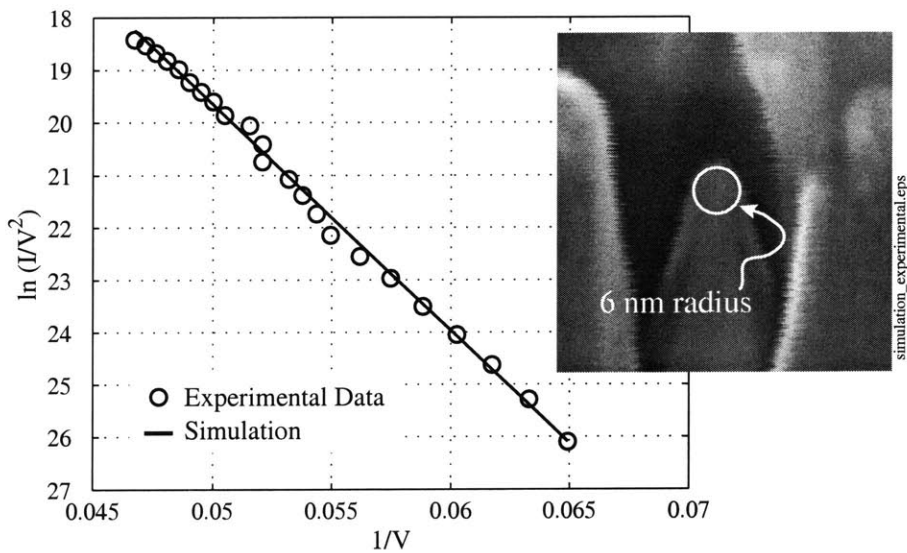
Figure 63: Comparison of Simulation to Experimental
Fowler Nordheim plot showing a comparison of simulation to experimental device data. Model is based on device with 100 nm gate aperture, 6 nm radius of curvature and a 75 degree cone base angle with 0. 1% or tips emitting.

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5.5.2.3 Device Longevity

Devices were tested for 48 hours to observe the effects of the initial device conditioning. During the first 24 hours of operation the anode current of a device would slowly increase while the gate voltage held constant. During the next 24 hours, the array stabilized in performance. Figure 65 shows the FN characteristics of an array after 0, 12, 24 and 48 hours. The result was consistent with experimental data provided by SRI on 1 μm gate aperture molybdenum tips [102] and by Shaw, et al, on 1 μm gate aperture silicon FEAs [103].
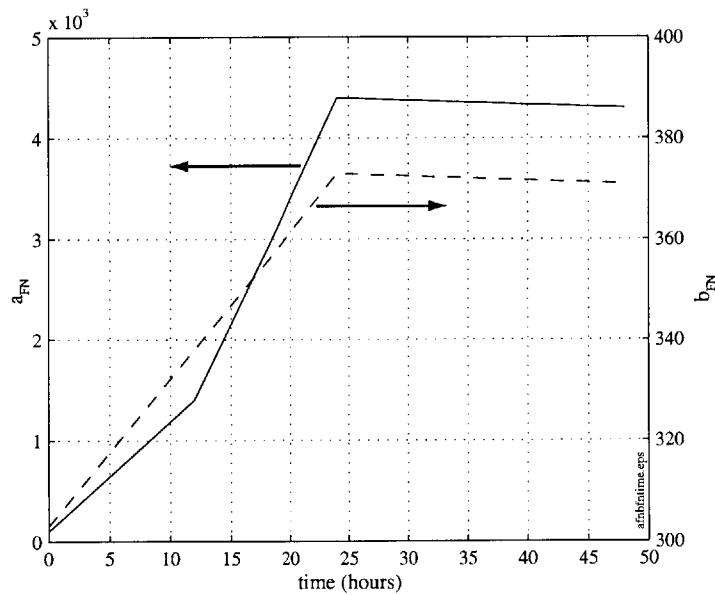
Figure 64: a_{FN} and b_{FN} over time
This is data for device performance over their first 48 hours. After 24 hours the array stabilized as seen in the leveling off of a_{FN} and b_{FN}.

The changes in device parameters (a_{FN} and b_{FN}) over the 48 hours of evaluation after the initial conditioning period could be explained by changes in the tip structure (tip radius), the proportion of tips emitting (effective emitting area) or the surface barrier (work function). Our data shown in Figure 64 indicates an increase in I_a, a_{FN} and b_{FN} with time suggesting a change in device characteristic. Even though there may be a change in the effective workfunction through a

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possible removal of surface adsorbates, the dominant change was due to the increase in effective emitting area. A possible mechanism that has been suggested by Schwoebel et $al.$ is smoothing of the tip. Schwoebel and Brodie of SRI attribute this change in tip radius to surface migration under the application of an electric field [94].

Numerical simulations were used to confirm that as the workfunction decreased b_{FN} would also decrease; however an increase in the tip radius was shown to provide this increase in both a_{FN} and b_{FN} (Figure 29). The results of 'seasoning' the array could also be seen in Figure 65 where the emission at high voltages is less noisy after 12 or more hours.
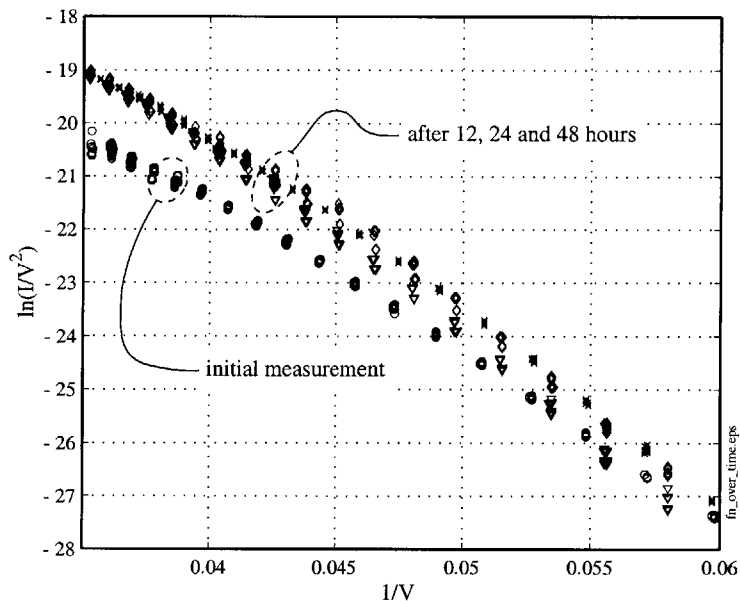
Figure 65: FN Plot of Array after 0, 12, 24 and 48 hours

This 100 μm × 100μm was run for 48 hours with the gate voltage held at 25 volts, periodically the array gate voltage was ramped and an IV characteristic was generated to determine the FN coefficients.

5.5.2.4 MOSFET switched FEAs

The MOSFET-FEA test configuration is shown in Figure 66 (inset). The MOSFET drain was connected to the emitter of the FEA while the MOSFET source was connected to ground. The

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gate of the FEA and the anode were held at constant voltages and the voltage on the gate of the MOSFET was ramped from 0 to 10 volts.
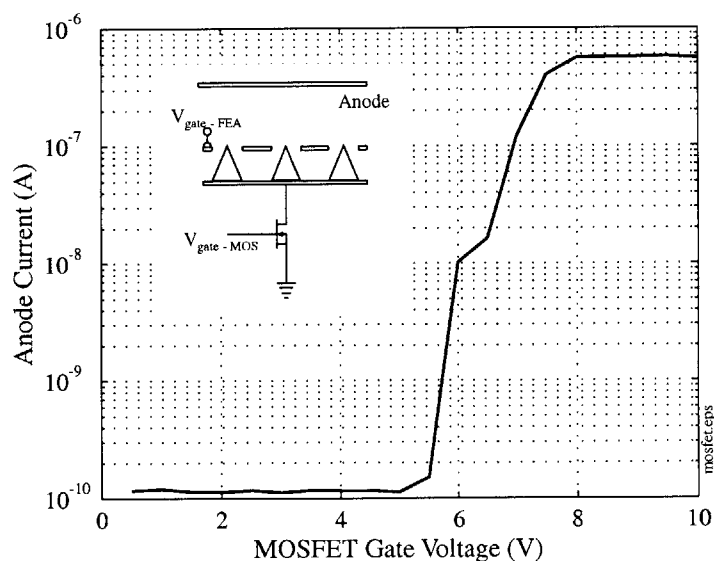
Figure 66: IV Characteristic of FEA - MOSFET
The inset shows the circuit set-up and the IV characteristics show a small control voltage on the gate of the MOSFET can control the FEA emission current by a factor of 4 orders of magnitude.

These tests explored a device operating regime in which the current is modulated by changing the 'electron supply' as opposed to the conventional situation in which current is modulated by changing the gate voltage and thereby changing the 'electron tunneling probability'. The structure shown is a cascode circuit with the MOSFET biased as a transconductance amplifier and the FEA biased as a current buffer. The results of the test shown in Figure 66 indicate that a voltage swing of 2.5 volts on the MOSFET gate can change the FEA anode current by four orders of magnitude. This result suggests that a low voltage can be used to switch the device. This configuration has implications for FED driver circuits and RF amplifier modulation.

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5.6 SUMMARY

The fabrication process outlined in this chapter successfully demonstrated 100-nm aperture devices at a 200-nm period. Device testing indicates that scaling the geometry reduces the operating voltage, which is in agreement with simulation results presented in Chapter 4. Quantitative comparison to simulation highlighted the effects of a distribution of tip radius on device performance.

The inaccurate prediction of the effective emitting area due to array non-uniformity prohibited the analysis of the shifted image potential presented in Chapter 3 and implemented in the numerical analysis of Chapter 4. Simulation indicated that the effect of the adjustment in the image potential causes a slight shift up of the FN curve, which could manifest itself as an increase in effective emitting area which made it difficult to quantitatively study.

Devices with turn-on voltages as low as 12 volts were demonstrated with anode currents of a few μA at voltages as low as 20 volts. The capability to modulate an emission current by 4 orders of magnitude with a 5 volt swing in the gate voltage was also demonstrated. The operation of an FEA with a discrete MOSFET showed the feasibility of operating these two devices together in a hybrid configuration to further lower the drive voltages to control emission current.

Choi, et al, extended the fabrication process presented to a matrix addressed FEA format on a glass substrate. The process is suitable for display fabrication and has been used to demonstrate FEAs with turn on voltage of 13 volts.

Some of the techniques used in this fabrication carried directly to the subsequent work on silicon cone fabrication described in the next chapter.

6 SILICON SHARPENED ARRAYS

The molybdenum field emission arrays with small gate apertures reported in the previous chapter suggest that low voltage operation of field emission arrays could be obtained by scaling the gate aperture using interferometric lithography. The results also indicate that there was significant variability in the resulting arrays because of variations in the tip radius due to the fabrication process. Previous works eliminate the variation in the device current by adding a ballast resistor to the emitter circuit to act as a feedback resistor and hence stabilize the emission current (Figure 3). This approach has attained a reasonable level of success because of the demonstration of displays based on this technology [104]. An analysis of this structure suggests the variability of the emission current is reduced if the resistor value is increased. In essence, the resistor may be viewed as approaching the behavior of a current source. It is therefore logical to consider replacing the high value resistor with a voltage controlled current source such as a n-channel MOSFET as shown in Figure 66 (inset). This configuration is essentially the MOSFET switched FEA reported in the previous chapter.

A logical extension of these MOSFET switched FEA is the fabrication of both the MOSFET and the FEA using silicon as depicted in Figure 67 [105, 106, 107, 108]. In this configuration the MOSFET drain sinks the emission current in the emitter of the FEA. The emission current could be controlled by the current through the MOSFET with the FEA acting essentially as an electron ejector for whatever current is in the drain of the MOSFET. Another view of this configuration is that of a cascode circuit with the FEA biased as a current buffer and the MOSFET biased as a transconductance amplifier. Hence any electron reaching the emitter of the FEA from the drain of the MOSFET is ejected. However a critical issue for this structure is the voltage on the drain

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of the MOSFET. A high voltage such as required for FEA may lead to breakdown on the MOSFET drain.

Ding, et al, recently reported high uniformity silicon field emission arrays with 1-μm gate aperture that were fabricated by isotropic etch of silicon, oxidation sharpening, LPCVD oxide and polysilicon, and chemical mechanical polishing [109]. They report tip radius of about 12 nm and arrays that were relatively uniform as demonstrated by the scaled emission currents from 10x10, 20x20, 30x30, and 60x60 silicon tip arrays. The devices turned on at about 30V.
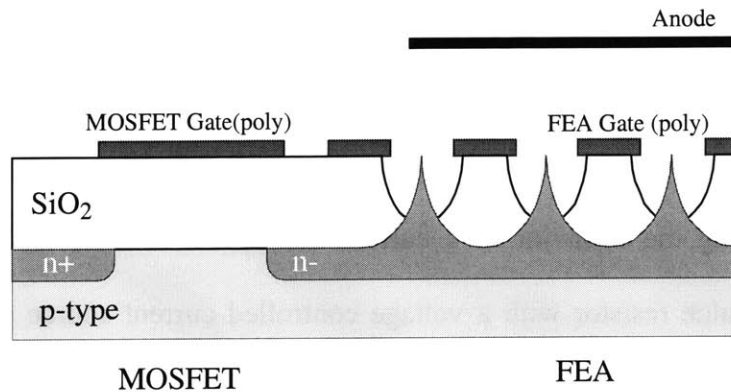
Figure 67: Concept of a MOSFET integrated with a FEA
One concept of the MOSFET – FEA integration would make the FEA part of the drain of the transistor. The gates of the two devices are shown above to be separate, but the thin dielectric layers of the scaled FEA and some device design may lend itself to a single gate design for certain applications.

A natural extension of the technology is the reduction of the gate aperture to 100 nm similar to what was reported in the last chapter. If the turn-on voltages and the gate operating voltage of the silicon FEAs are reduced, then it would be possible to integrate MOSFETs as current sinks for the FEA allowing the control of the emission current by the MOSFET gate. Other advantages to the configuration is the expected reduction in spatial and temporal (noise) variation of field emission current. Referring to the picture of electron emission given in Chapter

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3, the use of a MOSFET is tantamount to the control of emission current through the modulation of the electron supply function as opposed to the modulation of the transmission function (through changes to the barrier height or width). The control of the emission current through the modulation of the electron supply function should eliminate the temporal variations (noise) since the transmission function is not the limiting step in the serial process.

The above discussion provided the rationale for the exploration of low voltage silicon field emission arrays through aperture scaling, using interferometric lithography, silicon isotropic etch, oxidation sharpening, LPCVD of oxide and polysilicon and chemical mechanical polishing (CMP). The device fabrication process and characterization of the devices are reported in this chapter.

6.1 SILICON ARRAYS

Another fabrication process that is typically used to form field emitter cones is a silicon isotropic etch process that sharpens the tips with thermal oxidation. In this process the interferometric lithography was used to define a periodic oxide disc array which was used to mask an isotropic etch of silicon. Other processing steps include an oxidation for sharpening the tip and LPCVD of oxide and polysilicon to define the gate and gate aperture.

6.1.1   Basic Cone Arrays

6.1.1.1   200 nm Period Array formation

The initial steps to develop the silicon arrays were similar to the procedure outlined in Section 5.3. For the silicon arrays, all processing and substrate preparation were performed in the ICL (tri-level work for the Spindt arrays was done in TRL). The tri-level resist structure was built using the coater track and the e-beam. There is no capability for UV-ozone cleaning in ICL, so a

6 second O_2 plasma ash was substituted before ARC deposition and prior to surface treatment

with hexamethyldisilazane, (HMDS), which acted as an adhesion promoter for the photoresist.

The initial oxide for the silicon process was used as an etch mask for the rough cone formation.

6.1.1.2 Four Level Etch and Rough Cone formation

The pattern from the photoresist was transferred through the tri-level structure to the underlying

thermal oxide. This etch was performed in an AME 5000 reactive ion etcher and it comprises 4

steps; a de-scum using O_2, an oxide interlayer etch using CHF_3, an ARC etch using O_2 and

finally another oxide etch using CHF_3. The pressure was kept at 15 mT to provide an anisotropic

etch. The 100 nm diameter caps of SiO_2 was subsequently used as an etch mask in a plasma

etcher.
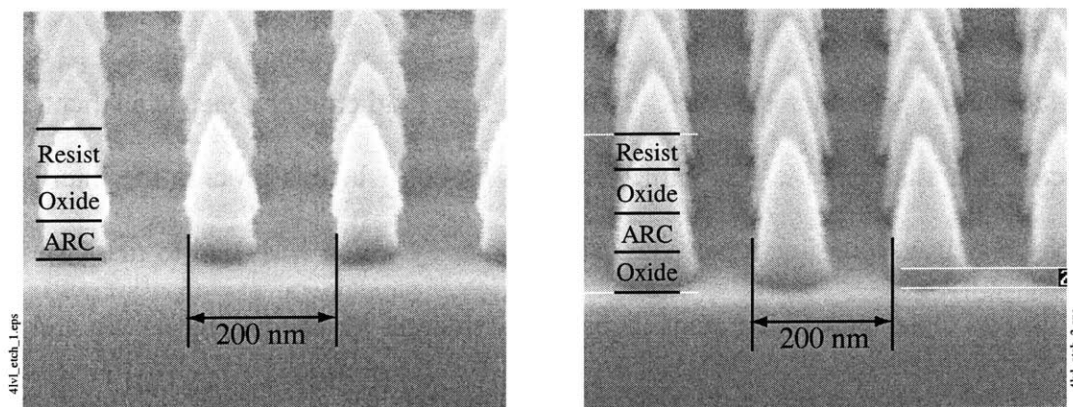
Figure 68: Progression of the Four-level etch
The four level etch uses each alternating layer as the etch mask for the underlying layer.
The etch goes all the way to the silicon substrate where the CHF_3 etch will stop. This
sample is shown with a 23 nm thermal oxide under the tri-level stack.

The cone shape was formed using a SF_6 plasma etch in a high pressure plasma etcher (LAM

Autoetch). The recipe included a short de-scum followed by a native oxide removal step. The

SF_6 etch was done at low power (50 W) at a pressure of 350 mT. The gas flow of SF_6 was 95

sccm with an equal amount of He flowing. A target thickness for the neck of the cone was 30-35

nm. This allows enough silicon to support the oxide cap while still defining the shape of the cone.
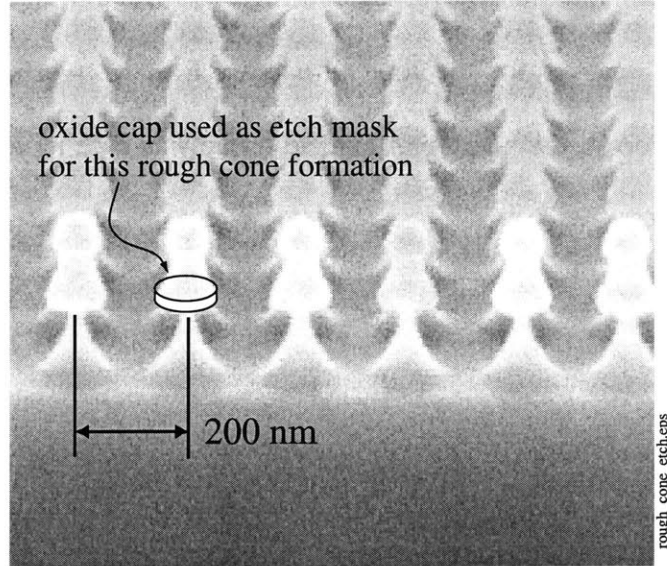
Figure 69: Rough Silicon cone shape from isotropic etching
The rough shape of the cone is a function of the lateral and vertical etch rate. The correct aspect ratio and undercut was achieved at 350 mT. The oxide cap that acts as the etch mask with the remainder of the tri-level material shown balanced on the cone.
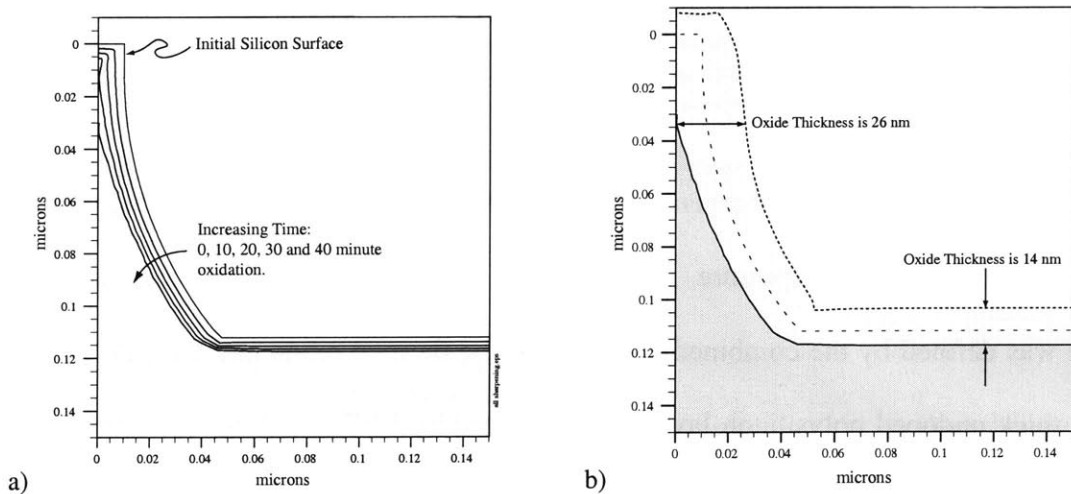
Figure 70: Oxidation of a Silicon Tip in SUPREM IV
An axially symmetric model of the Rough etched Si tip was formed in SUPREM IV and oxidized for 10, 20, 30 and 40 minutes at 900°C in dry O_2. a) The evolution of the silicon surface during the oxidation. The tip remains sharp even during the over-oxidation. b) The lateral oxidation rate is almost twice that of the vertical oxidation rate.

Residual ARC was removed in a Piranha solution and the oxide caps were removed in hydrofluoric acid. The tips were then sharpened using dry thermal oxidation at 900°C. Determination of the oxidation time was based on a 'lateral oxidation rate'. The vertical <100> oxidation rates are well known for the tube furnaces. Based on process simulations using SUPREM IV (Silvaco Tools), the horizontal oxidation rate was determined (as shown in Figure 70b).
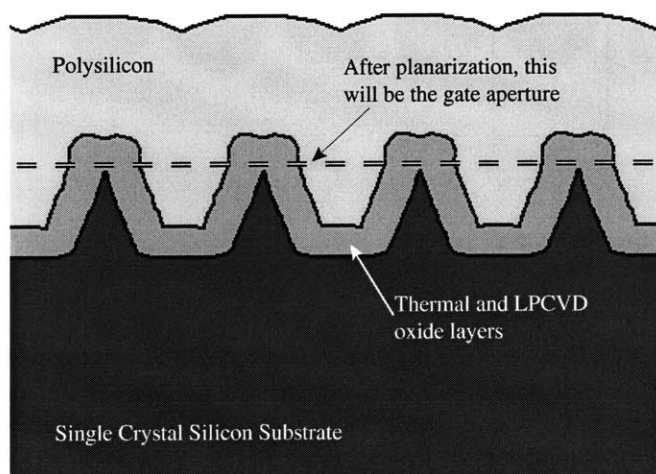
Figure 71: Silvaco simulation of array after sharpening and CVD
The combination of the oxidation sharpening and LPCVD oxide create the gate dielectric. When the structure is planarized to the level indicated by the dashed line, (--), the gate aperture will be approximately 2✕the thickness of the gate dielectric.

After the thermal oxidation to sharpen the tip, an LPCVD oxide that is conformal was deposited in order to define the gate aperture. From Figure 71 it can be seen that the size of the gate aperture was defined by the combined thickness of the thermal oxide and the LPCVD oxide. A 150-nm thick undoped polysilicon layer was deposited by LPCVD. This conformal layer must be thick enough to be above the emitter tips, even at its lowest point. The polysilicon layer when viewed before polishing shows a periodic structure following the array pattern, (Figure 72).

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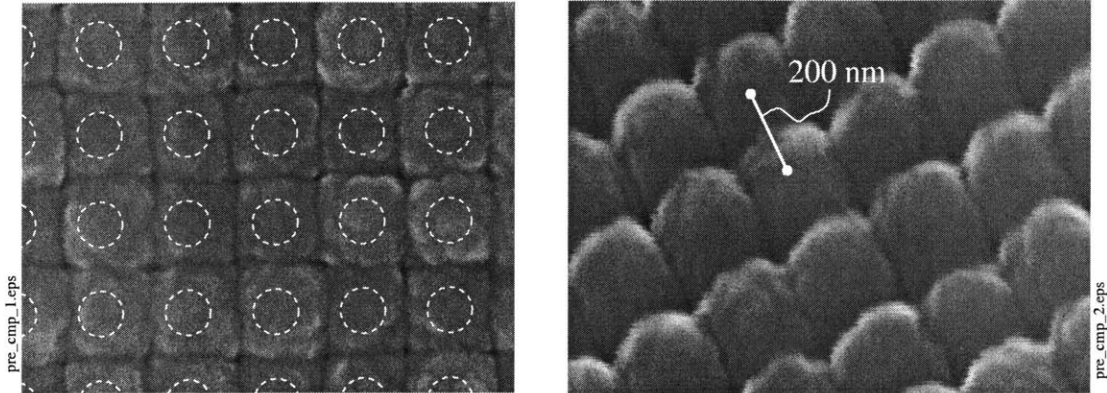
Figure 72: Top and 45° view of polysilicon deposition
The polysilicon conformal coverage allows the period of the underlying array to be seen after the polysilicon deposition. When comparing the to view with Figure 71 it is easy to identify the location of the gate apertures as shown by the white circles.

This surface of the wafer was then planarized using chemical mechanical polish (CMP) down to the level indicated by the dashed line in Figure 71 to expose the tips and create the gate apertures. Some of the gate oxide was removed with a short BOE dip to fully expose the tip. Enough dielectric must remain to structurally support the gate. Figure 73 a, b and c show the final device structure after the CMP of the gate.

6.1.2 Device Fabrication

The aforementioned process was used as a proof of concept to show that the cone formation process was feasible. Because the interferometric lithography is a maskless technique, cones are formed everywhere. This section describes the additional steps that were required to limit the cone formation to certain areas, and the patterning of the gates to provide discrete devices on the substrate. While forming discrete arrays, this process also formed a thicker oxide to support the thick polysilicon lines and pads that were be used to contact the array. Many of the figures in this section are of blank dummy wafers (no interferometric lithography).
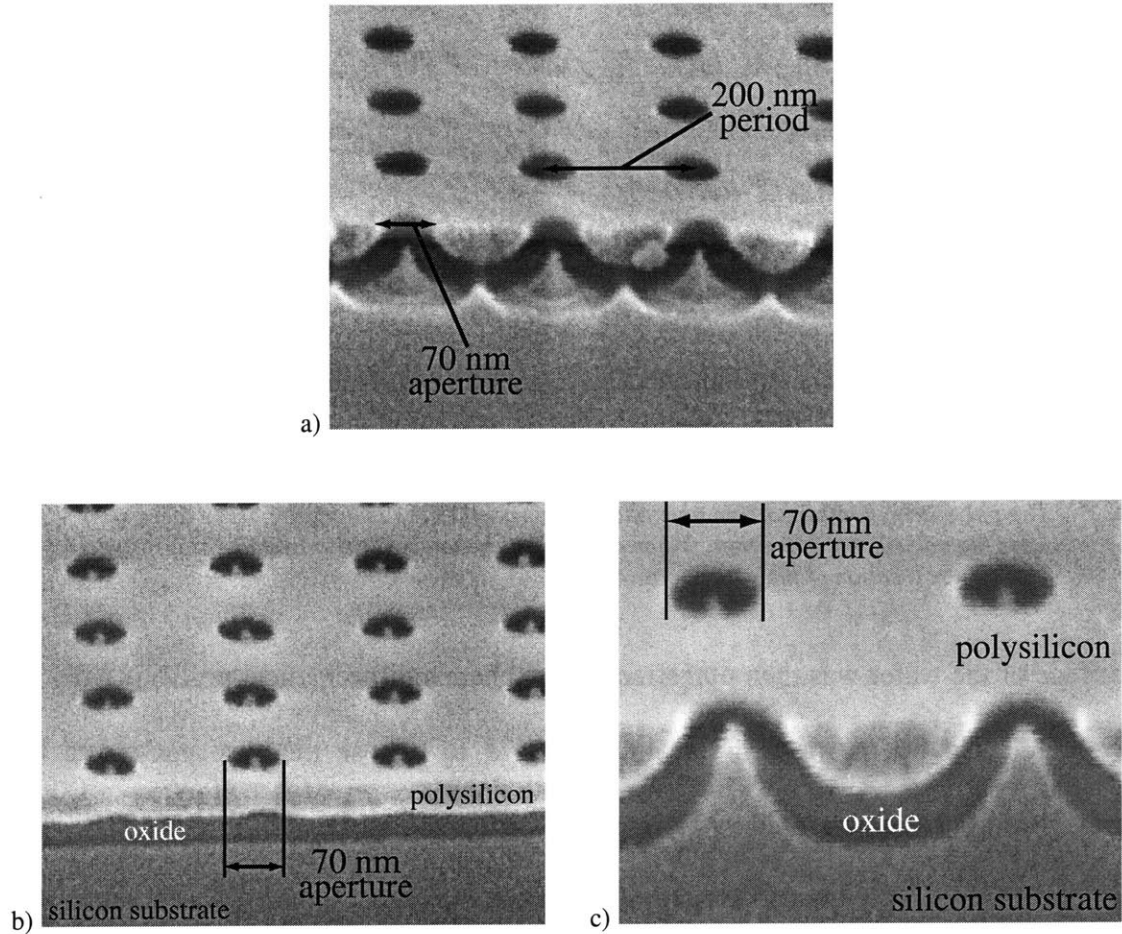
Figure 73: 200 nm period silicon arrays
The gate apertures on these arrays ranged from 70 – 90 nm. The figures show varying amount of gate oxide being removed.

After the rough cone formation (as shown in Figure 69) 200 nm of nitride (Si_3N_4) was deposited in a Concept One CVD machine at 400°C. The substrates were coated with positive photoresist and patterned with mask #1, which defined the device regions, using a g-line stepper. The pattern for mask #1 defined the regions where emitter tips were left intact. Additionally, there were sacrificial structures that surround the arrays that helped prevent 'rounding over' of the mesa edges in the later chemical mechanical polishing (CMP) steps. In this photo-step the exposure was set to be slightly higher than necessary to clear the resist, in fact the target

exposure was high enough to almost completely wash out the 1μm lines, (implying a 0.5 μm of edge erosion of the pattern).

Emitter Array

Probe Pad

Mask #2: Polysilicon gate pattern / Device isolation
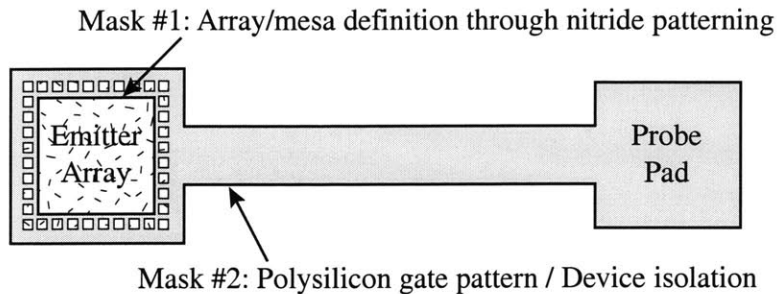
Figure 74: Masks for Silicon Cone Process

Both masks are dark field masks. Mask #1 is used to determine the region where cones will be formed to become the active region of the devices. Mask #2 will be used to pattern the polysilicon gate to provide device isolation.

Using the pattern formed by mask #1, the nitride and 200 nm of the underlying silicon were etched using an SF_6 plasma. The etch systems was a high pressure plasma etcher (LAM Autoetch) at a pressure of 500 mT. This high pressure provided undercutting of the silicon under the photoresist mask when forming the mesa. The high pressure also removed any traces of the cone structure in regions not protected.

The substrates were thermally oxidized to grow approximately 100nm of thermal oxide. Figure 75 shows the results of the first LOCOS oxidation on a dummy wafer. The nitride protected the region that has the rough cones from oxidation.

The nitride layer was stripped in a hot phosphoric acid bath, (later determined to be unnecessary) and another conformal coating of 200 nm nitride was deposited in the Concept-One. This new nitride layer was again patterned using mask #1. The exposure time for this run of mask #1 was chosen to underexpose the substrates. The alignment of the two exposures of mask #1 is critical.

Over-developing and under-etching the initial mesa formation, combined with the underexposure of this run gave approximately ± 0.5 µm of latitude in the alignment.
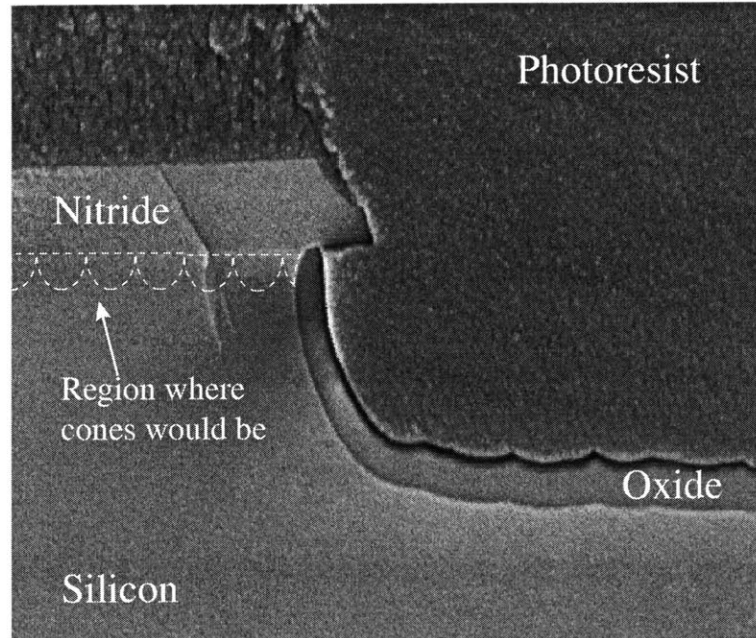
Figure 75: Results of LOCOS I step in Mesa Formation
The nitride cap protects the region where the cones would be (blank dummy wafer shown here). The wafer was coated with PR after the oxidation (prior to cleaving) so that the oxide could be highlighted with a BOE dip.

The second patterning of mask #1 was used to again pattern the nitride layer, stopping on the underlying oxide. The AME 5000 was used with an SF_6 RIE at 35 mT. The anisotropic nature of this etch minimized the undercut.

The patterned nitride again protected the mesa tops where the cones would be, but more importantly, protected the sidewalls of the mesa and prevented a bird's beak from forming at the plane of the original surface.

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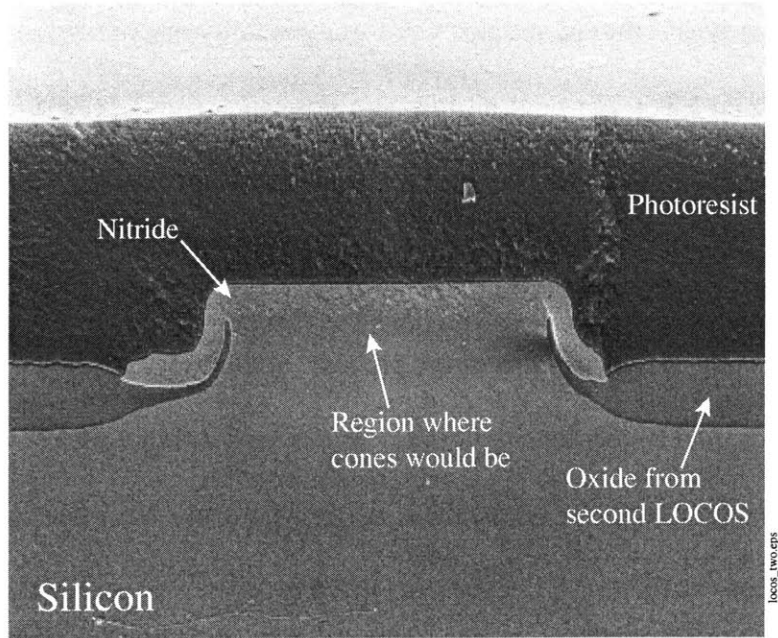
Figure 76: A small mesa after LOCOS II

The mesa top and sidewalls are protected from the second oxide growth. This prevented oxide from growing above the plane of the original silicon surface. The substrate (blank dummy wafer) was coated with photoresist after oxidation (before cleaving) so that the LOCOS oxide could be highlighted using a BOE dip.
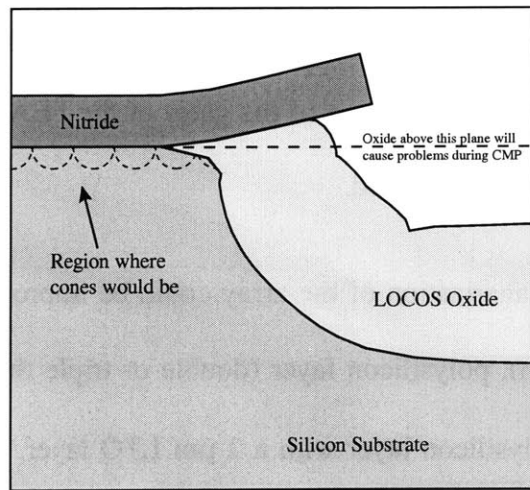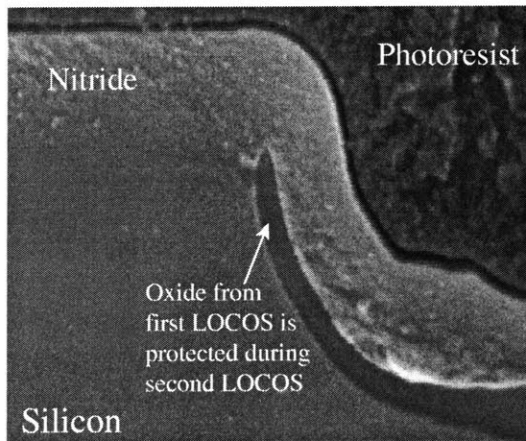
Figure 77: Comparison of Single LOCOS to Double LOCOS

The figure compares the results from the double LOCOS (of a blank dummy wafer) to a simulation of the single LOCOS using Silvaco. In order to achieve the thick oxide for additional isolation of the lines and pads, a single LOCOS would form a bird's beak above the top of the original silicon surface. This would cause difficulty in the later CMP step causing the array gates to be isolated from the lines and pad.

After the nitride layer was removed the tips were sharpened by dry oxidation at 900°C followed by the deposition of an LTO, optional nitride, and polysilicon by LPCVD. The substrate was then polished in the CMP to planarize the gate and expose the apertures.

In the original process (without patterning) the CMP step was difficult. The difficulty increased in the device process due to two artifacts of the process: a) the substrate was no longer planar due to the mesa structures, and b) the density of these structures was not uniform across the die. The polish therefore became a function of the mesa height, the array size, and the proximity of the array to other features on the wafer. Even if a specific array was polished successfully to the final point as shown in Figure 78a, the center of the array would not have the same gate thickness and gate aperture to the precision necessary to have a uniform FEA (Figure 78b). The overpolishing the edges of the array resulted in the reduction in gate polysilicon thickness and the increase in the gate aperture as shown in Figure 78b. This overpolish can initially impact device performance by removing the top of the tips. A more extreme situation would result in the electrical isolation of the gates of the FEA if the polysilicon around the edge of the array is completely removed.

The planarization of the array could be improved by one of two techniques; using a thicker, (~ 1.5 μm), polysilicon layer (double or triple the thickness of the original process), or following the polysilicon layer with a 2 μm LTO layer. Both these techniques improved the planarity of the array and eliminated the difficulties associated with completely polishing through the polysilicon at the edge of the mesa and isolating the array gate.

After the array was polished, the polysilicon gates were patterned with Mask #2 to form discrete devices and pads for electrical characterization of the devices. After the resist was stripped, the arrays were etched in BOE for 20 seconds to remove a portion of the gate oxide.
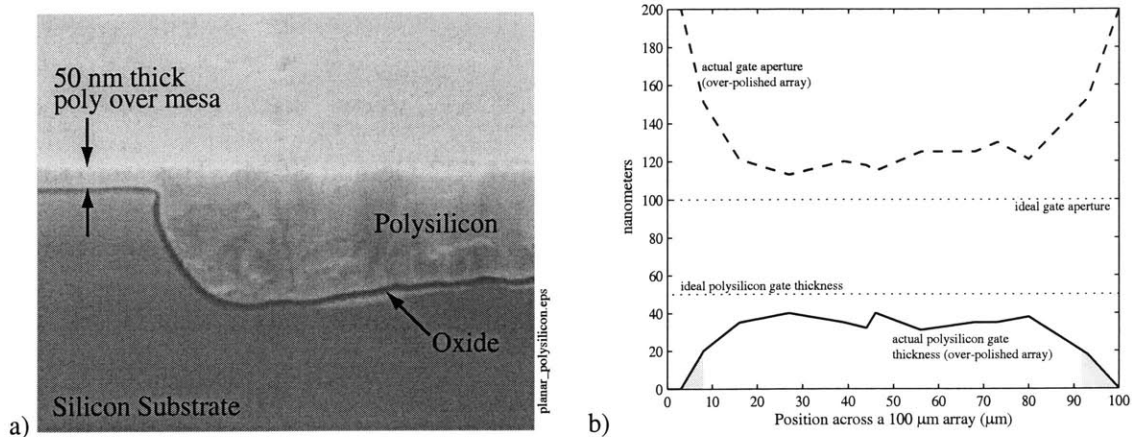
Figure 78: Planarization of the polysilicon gate layer
For the dummy wafer shown, the planarization of the polysilicon wafer would leave a thin polysilicon layer over the mesa (where the arrays would be) and a thick polysilicon layer for probing and connection to the device. The gray regions at the edges of the figure b) indicate that the over-polishing of the polysilicon indicates tips were damaged in these regions.

6.2   ARRAY ANALYSIS AND DEVICE CHARACTERIZATION

In addition to the measurements that were made above to study the planarity of the arrays after CMP, arrays fabricated using the above process underwent further study of their physical features. The tip radius measurements in conjunction with the electrical characterization provide a unified picture of the results of the above fabrication. The rest of this section will provide the results of the tip analysis, electrical performance and array analysis using numerical simulation.

6.2.1   Tip Radius Measurements

Even though these devices were scaled and the field factor β becomes increasingly dependent on gate aperture, the tip radius will still be the dominant parameter. The exponential relationship

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between the emission current and the surface electric field implies that, in an array of tips with a distribution in the tip radius, the sharpest tips will dominate the array performance. In order to investigate the distribution of tips, a sharpened array was examined in a SEM and TEM. The analysis and measurement in both the TEM and SEM has some error based on the magnification, quality of the image, and conditions of the sample.

Initial measurements were made using a ZEISS DSM 932 Gemini SEM. Tips were randomly sampled and measured over 1 cm^2. If the tip was too small to measure in the SEM it was classified as 'under 5 nm radius'. Of the 35 tips sampled, approximately 8 were in this 'under 5 nm radius' regime.
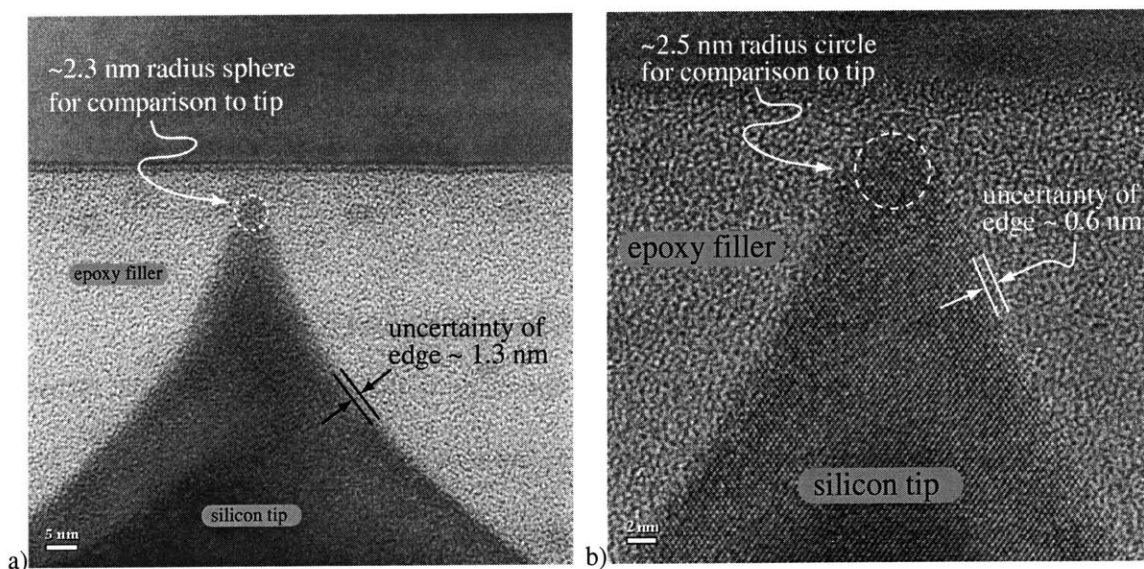
Figure 79: TEM of two sharp Silicon tips
In order to measure the sharpest tip TEM was used. The patterns due to the interference with atomic lattice of the silicon can be seen in the micrograph on the right.

Two sets of TEM images were taken. The first sample was prepared using a standard TEM sample preparation. Due to the nature of this TEM sample prep, all tips from these measurement are within a few microns of each other. Approximately 40 tips were imaged by this technique

using a JEOL 2010 TEM with high resolution capability. The second set of images was taken using a sample holder and preparation method developed more suited for imaging field emission tips. Similar to a concept presented by Goodhue, [101], the holder was designed that would allow the mounting of a FEA array sample as shown in Figure 80. The samples were mounted and approximately 30 tips were imaged over an edge 2 mm long. The second set of images was taken in a JEOL 200 microscope. Besides the short prep time, the second technique allowed for a larger area to be sampled, and the outline of the tip was more evident because the sample was not coated in epoxy for mounting. Unfortunately the JEOL 200 does not have a high-resolution pole piece and even at high magnification, the silicon lattice is not visible with this microscope.
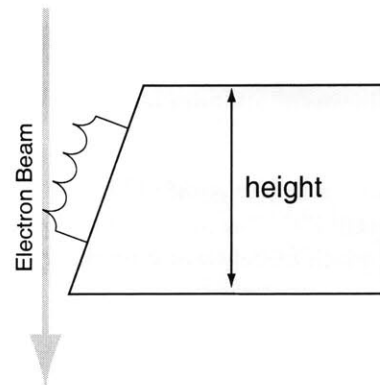
Figure 80: TEM holder for array tip analysis
A TEM holder was designed to integrate with a standard JEOL bulk holder and hold the emitter array sample in the electron beam. The last row of tips is easily imaged without the traditional TEM sample prep and thinning. The height of the holder is approximately 2.5mm. The sample dimensions were 2mm x 3mm and are mounted with a silver paint.

6.2.1.1 High Resolution TEM Analysis

At higher magnification as shown in Figure 79b, the silicon lattice is visible and can be used to determine the edge of the cone in the micrograph. By sampling the image and measuring the power spectrum for a given spatial frequency, the periodic structure of the cone is highlighted, (contours of the power spectrum are shown in Figure 82a) [110, 111, 112]. The average of the

power spectrum for a background area far from the cone was measured. The point where the power spectrum was double the background average determines the boundary of the cone as shown in Figure 82b. For some micrographs with low contrast, this technique did not provide much image enhancement. Utilizing more advanced filtering techniques and additional properties of the image could be used to do further enhancement.
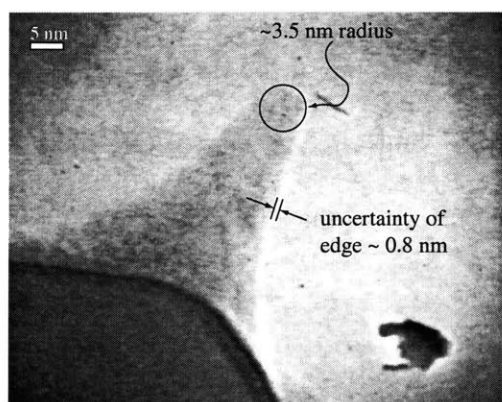
Figure 81: TEM image taken at MIT using TEM sample holder
The image was taken in a JEOL 200. The magnification of the microscope was 100,000 with an additional 12.5 x by the CCD and thermal image printer.

6.2.1.2 Tip Radius Distribution

The data that was collected from the three sources was compiled and is shown in Figure 83. Based on the uncertainties shown in the above TEM micrographs, the bins for the histogram were limited to dimensions above 1 nm. In order to investigate the tails of the distribution, the data was fit to three distributions that meet the following criteria: a) sample space admits only positive values, and b) distribution is skewed to the right (longer right tail). The *Log-Normal*, *Gamma*, and *Weibull* distributions were considered and fit to the data [113]. In addition to meeting the criteria above, these three distributions were chosen for their flexibility and adaptability by using a three-parameter model [114, 115]. The Weibull distribution has also been used in literature to describe particle size distributions [116].

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a)   b) ~ 1.6 nm radius circle
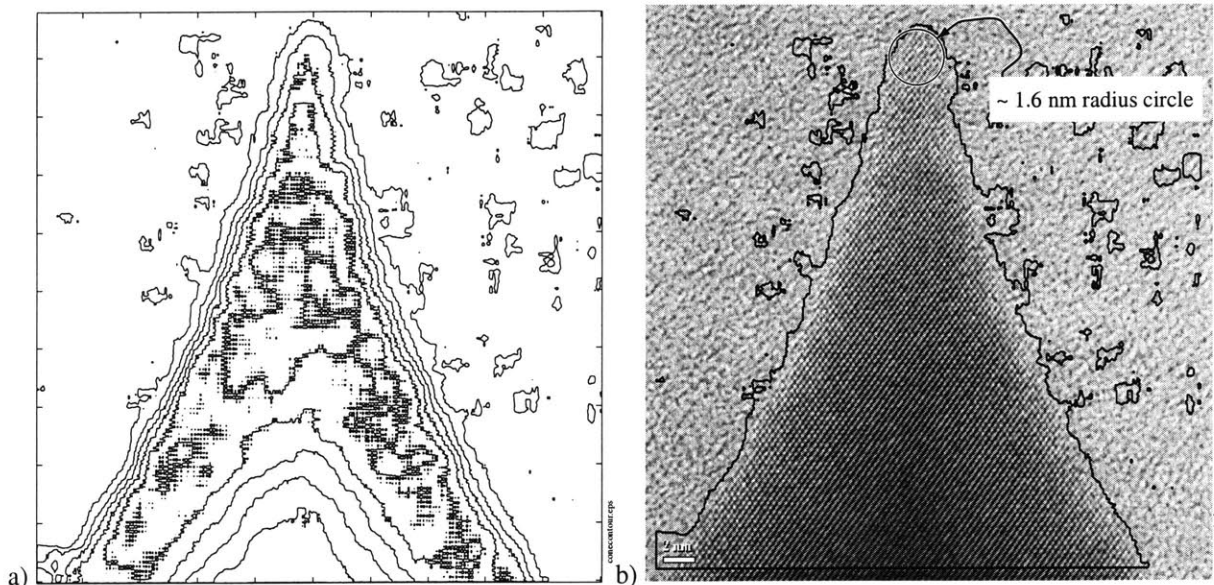
Figure 82: TEM Micrograph processing using Fourier Analysis

The micrograph can be enhanced using a simple spatial frequency analysis of the electronic image.

$\mu = 1.4973$, $\sigma = 0.49838$
peak at 3.5 nm
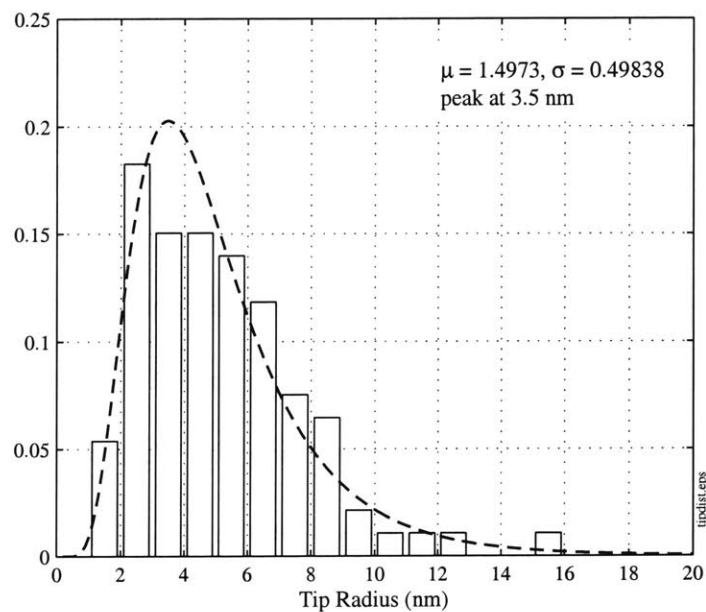
Tip Radius (nm)

Figure 83: Distribution of Silicon Tip radius

Tips from an oxidation sharpened Si array was measured in an SEM and a TEM. The data from over 90 tips is shown by the bars of the histogram and the dashed line is the fit to a log-normal PDF.

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All the distributions fit the data similarly, but the log-normal distribution was chosen after examining the linearity of the plot shown in Figure 84 generated in Matlab used to graphically compare data against a distribution.
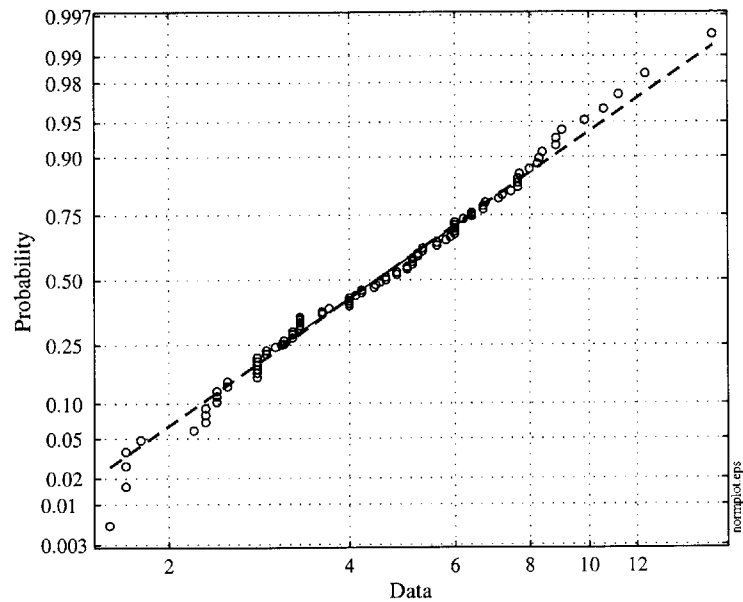
Figure 84: Log-Normal Probability plot for graphical testing
If the data plotted comes from a Log-Normal distribution, the plot will be linear.   Other probability density functions will introduce a curvature in the plot

The parameters above were used to generate a log-normal cumulative distribution function as shown in Figure 85. The results indicated that a few percent of the tips will have a radius of 2 nm or below. Similar results were also found when using the Weibull and Gamma distributions. Based on the measurements of the PR posts discussed in Chapter 5, the distribution was attributed to variations in the original lithography. Although the IL provides unprecedented accuracy in the array period, it was the choice of exposure dose and develop that determine the line to space ratio. Posts of PR that were exposed with IL were measured. The posts had a mean width of 99.5 nm, but a spread with a σ of 3.5 nm. To the first order, the tail of the PR post distribution was of the same size and shape as the right side of the tip distribution. In order to

eliminate variations in the tip radius, a self-limiting process needs to be developed. One possibility is the use of over-oxidation or a double oxidation technique as described by Liu [117].
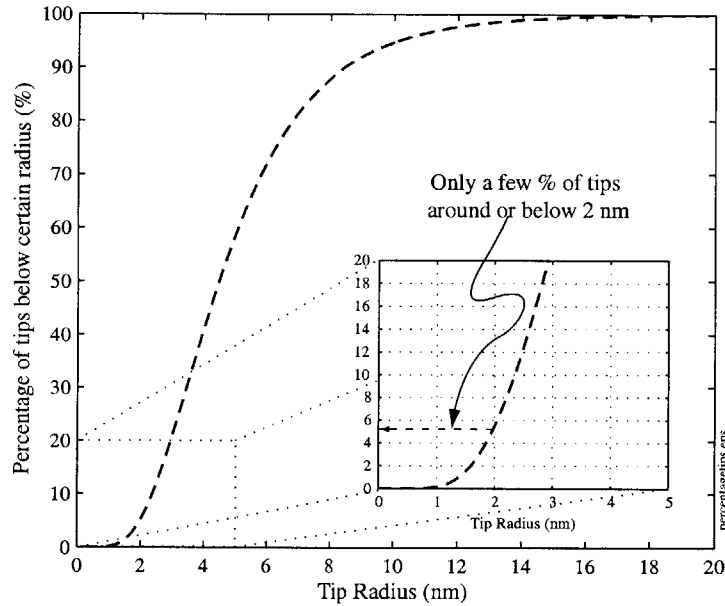
Figure 85: Percentage of tips below a certain radius
The inset shows that for the fit to the chosen distribution function above, that only a few percent of the tips have a radius of 2 nm or below.

6.2.2   Device Characterization Configuration

The test set-up for the characterizing the silicon arrays was similar to that of the molybdenum arrays described earlier. In order to remove any final surface oxide the silicon arrays were dipped in a 50:1 DI:HF solution and rinsed/dried immediately (within 30 seconds) before being loaded into the test system (followed by an immediate pump-down). Additionally the system now has a UHV leak valve attached to an ultra-pure hydrogen source. The bake out described earlier for the molybdenum arrays was modified to be done at a higher temperature (250° C) in a hydrogen ambient of 1×10^{-6} torr.

6.2.3 Silicon Arrays Device Characterization

6.2.3.1 Device IV Transfer Characteristics

Arrays of 100 µm were tested and characterized by measuring the anode and gate current while sweeping the gate voltage. Devices exhibited turn on at voltages as low as 9 – 10 V and typically emitted anode currents of 1-2 µA at voltages of 15 V, and anode currents as high as 30 µA at gate voltages of 22 V.
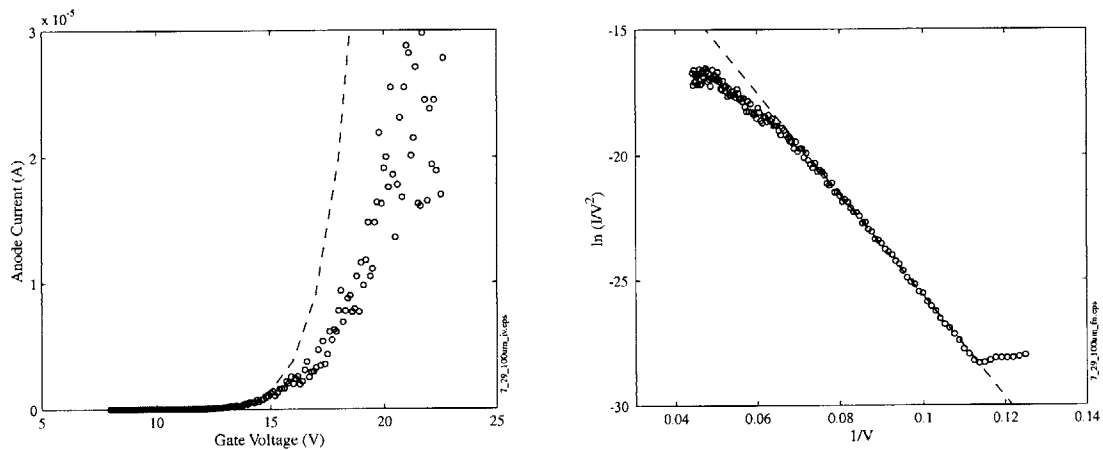
Figure 86: IV and FN for 200 nm period silicon array (729200)

Anode current vs. Gate voltage and FN plot for array 7_29_2_00, 100 × 100 µm, tested at 5 × 10⁻¹⁰ torr. Fowler Nordheim coefficients: $a_{FN} = 4.9 \times 10^{-3}$, $b_{FN} = 203$, $\alpha = 1.9 \times 10^{-11}$, $\beta = 2.6 \times 10^6$. The lines are the fit to the Fowler Nordheim equation, which is used to extract the coefficients.
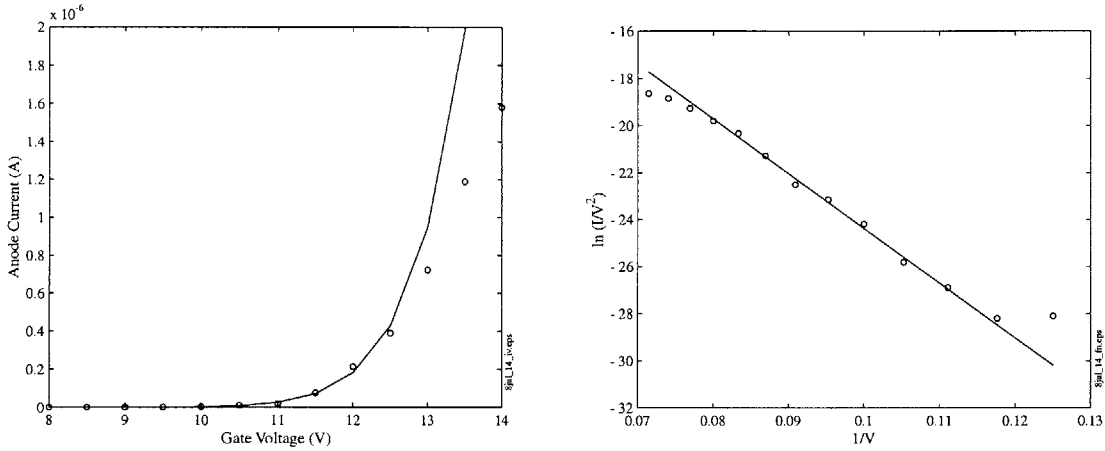
Figure 87: IV and FN for 200 nm period silicon array (708100)

Anode current vs. Gate voltage and FN plot for array 7_8_1_00, 100 × 100 μm, tested at 2 × 10⁻¹⁰ torr. Fowler Nordheim coefficients: $a_{FN} = 0.39$, $b_{FN} = 228$, $\alpha = 1.9 \times 10^{-9}$, $\beta = 2.3 \times 10^6$. The lines are the fit to the Fowler Nordheim equation, which is used to extract the coefficients.
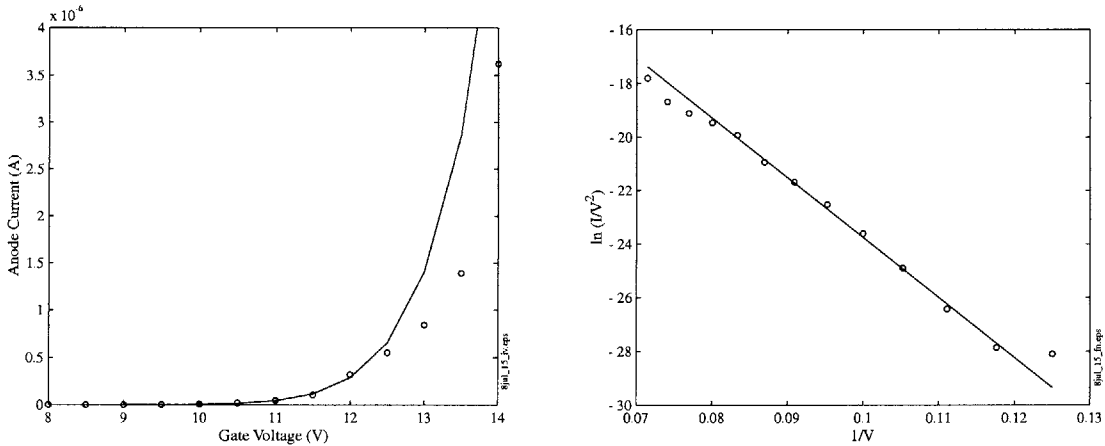
Figure 88: IV and FN for 200 nm period silicon array (708200)

Anode current vs. Gate voltage and FN plot for array 7_8_2_00, 100 × 100 μm, tested at 2 × 10⁻¹⁰ torr. Fowler Nordheim coefficients: $a_{FN} = 0.43$, $b_{FN} = 235$, $\alpha = 2.3 \times 10^{-9}$, $\beta = 2.3 \times 10^6$. The lines are the fit to the Fowler Nordheim equation, which is used to extract the coefficients.

The characteristics of the device shown in Figure 89 a-d are from the same device. Figure 89a and b show the performance of the device after initially turning on and ramping up to operating voltages. Figure 89 c and d shows the same device after operating with a gate voltage of 15 V

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and an anode current of 0.5 – 1.0 µA for over 5 hours. There is very little difference between the

two characteristics when comparing the FN coefficients.
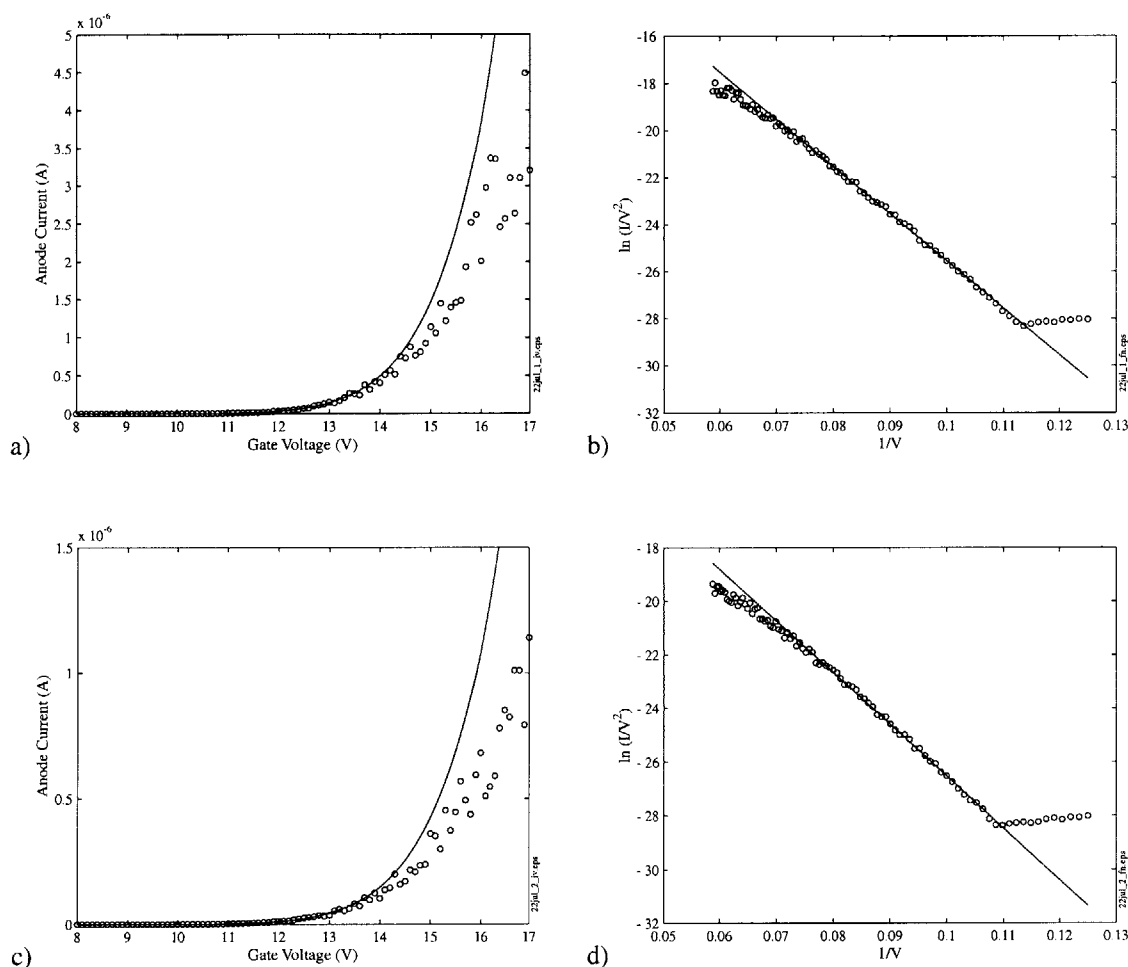
Figure 89: IV and FN for 200 nm period silicon array (722100)
Anode current vs. Gate voltage and FN plot for array 7_22_1_00, 100 × 100 µm, tested at 1 ×10⁻¹⁰ torr. Fowler Nordheim coefficients were initially: a_{FN} = 0.0052, b_{FN} = 203, α = 8.3 ×10⁻¹¹, β = 2.6 ×10⁶. The final value of the coefficients were: a_{FN} = 0.0074, b_{FN} = 190, α = 2.7 × 10⁻¹¹, β = 2.7 × 10⁶. The lines are the fit to the Fowler Nordheim equation, which is used to extract the coefficients.

Table 8: Summary of Device characteristics for Silicon arrays

	Type	Array Size	a_{FN}	b_{FN}	α	β
729100	Silicon	100 × 100 µm	4.9×10^{-3}	203	1.9×10^{-11}	2.6×10^{6}

729200	Silicon	$100 \times 100 \ \mu m$	1.5×10^{-2}	204	6.2×10^{-11}	2.6×10^{6}
708100	Silicon	$100 \times 100 \ \mu m$	3.9×10^{-1}	228	1.9×10^{-9}	2.3×10^{6}
708200	Silicon	$100 \times 100 \ \mu m$	4.3×10^{-1}	235	2.3×10^{-9}	2.3×10^{6}
722100	Silicon	$100 \times 100 \ \mu m$	7.4×10^{-4}	193	2.7×10^{-11}	2.7×10^{6}

Table 8 shows the summary of device characterization for silicon. In addition to the electrical measurements in Table 8, Table 9 shows the results of some array analysis similar to the analysis presented in Chapter 5. The dominant tips for the devices were between 2 and 3 nm. This result was consistent with the tip distribution study that was done earlier. The device characteristics showed consistency based on device location.

- 729100 and 729200   wafer #9, die 3
- 722100   wafer #9, die 1
- 708100 and 708200   wafer #1, die 7

Table 9: Tip radius analysis for Silicon arrays

	Tip radius used in numerical simulation to match experimental slope.	Ratio of $\alpha_{measured}$ to $\alpha_{simulation}$	Tip radius calculated using $\beta_{experimental}$ by ball in sphere model (assuming aperture of 100 nm)	Tip radius calculated using r = $1/\beta_{experimental}$
729100	2.2 nm	0.001	3.6 nm	3.8 nm
729200	2.1 nm	0.001	3.6 nm	3.8 nm
708100	2.7 nm	0.038	4.2 nm	4.3 nm
708200	2.7 nm	0.046	4.2 nm	4.3 nm
722100	2.0 nm	0.001	3.5 nm	3.7 nm

The effect of the external electric field on a silicon surface was described in Chapter 3. The amount of band bending could contribute to changes in the effective workfunction seen by electron at the Fermi-level in the silicon. Figure 90 shows graphically the effect of the band bending on the emission barrier. The inset shows that the effective workfunction can be

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decreased by 10% at an external field of 3×10^7 V/cm which is a typical value to achieve appreciable current from field emission.
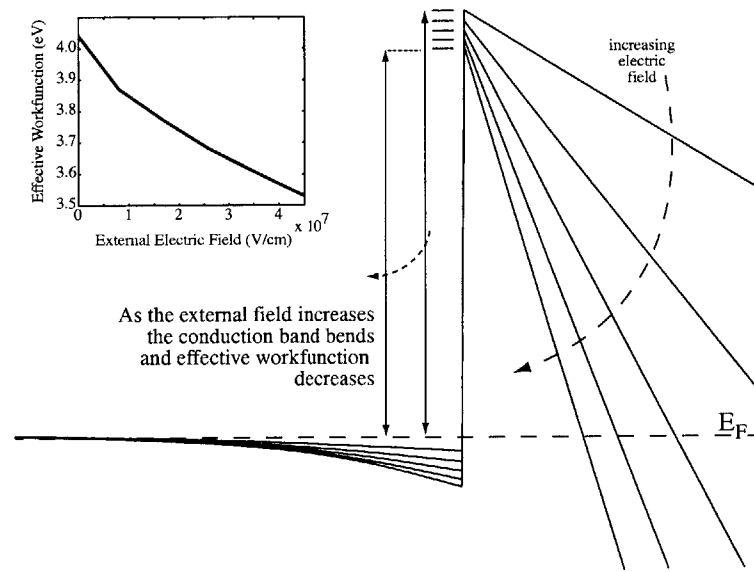
Figure 90: Band bending in Silicon for various E-fields

The external electric field will penetrate the silicon and bend the bands. This shift will pull the top of the barrier down an equal distance. Electrons at the Fermi-level see a different height barrier then with no applied field. For silicon, the increase external electric field not only reduces the barrier width, but reduces it's height.

The silicon devices also deviated from FN theory at currents level of 1 μA. One explanation relates back to the reduction in the effective workfunction presented above. Although the change in the slope of the data in the FN plot (b_{FN}) could be attributed to the shift in workfunction, there would also be a corresponding increase in a_{FN}. An increase in a_{FN} was not observed. The behavior although appearing to deviate from FN behavior, could be considered to be consistent with FN theory, but for a different barrier.

The deviation from FN behavior of the device has been attributed to current saturation due to electron supply limitation arguments [118]. The maximum current attainable from the conduction band would be:

$$I_{sat} = \alpha q n v_{sat}, \text{ where } \alpha = \pi r^2$$

where r is the tip radius and α represents the cross sectional area current must flow. For the devices tested above, with r = 2 nm, and n = 10^{18} cm^{-3} the saturation current per tip is calculate to be approximately 60nA. For an array with 0.1% of the tips (of a 250,000 tip array) operating, this translates to a saturation current for the array of 15 μA. This saturation effect would occur in different radius tips at different currents and therefore could be a gradual effect as the gate voltage was increased.

Only one device demonstrated currents as high as the 15 μA discussed above, yet all the devices exhibited some sort of electron supply limited saturation above 1 μA. These devices were in the size regime ~ 0.1 μm where electron transport could be ballistic in nature. Ballistic transport in these devices counters the velocity saturation argument above because electrons are not limited by v_{sat} in ballistic transport. Therefore, the current limit to the tip may be due to the structure of the cone. An electron will have to be moving directly toward the tip of the cone because no scattering events in the distance to traverse the entire device will occur unless caused by an interaction with the surface. This could limit the electron supply function to the area (the top of the tip) where transmission out into vacuum can occur.

90 nm gate apertures silicon FEA have been reported by Takemura of NEC [122]. These devices show similar field factors and effective emission area as the device reported here. The most significant difference between the two processes was the array period. Even though the aperture of the NEC device was 90 nm, the tip-to-tip spacing was approximately 1 μm. The additional space allowed the use of thicker dielectric layers and more cathode-gate isolation, subsequently the NEC devices could be operated at much higher voltages without breakdown. Based on

limited data that was reported, devices reported here provided higher emission currents than the NEC devices when operated at equivalent gate voltages, (NEC data indicates: $a_{FN} = 1.1 \times 10^{-3}$, $b_{FN} = 280$ $\alpha = 4.4 \times 10^{-9}$, and $\beta = 1.9 \times 10^{6}$, $1/\beta = 5.3$ nm).

The starting point in developing this silicon process presented above was a silicon process used to fabricate 1 μm aperture arrays [109]. These larger arrays have been reported to exhibit turn on voltages of approximately 30V. Although the apertures are a full order of magnitude larger than the devices reported in this work, Ding et al, reports an oxidation sharpened tip of 15 nm, only a factor of 4 larger then the reported tip radii from the previous section. By comparison to Ding's work, further scaling of the tip radius beyond the work reported here might be difficult. The large devices also are capable of operating at voltages over 100 V to achieve emission of almost 1 μA per tip.

6.2.3.2 Output IV Characteristics

The measurements to this point have shown the effect of the gate voltage on the emission current. For the devices tested, the emitted current was not a function of the anode voltage. In earlier discussion we considered the field on the surface of the tip as the product of the gate voltage and a field factor β, we could also consider an equally valid effect from the anode voltage. The field on the surface of the tip was considered to be the superposition of the two:

$$E_{surf} = \gamma V_a + \beta V_g$$

The fact that the emitted current was not a function of the anode voltage indicates that the product of γV_a is much smaller then βV_g. This agrees with the fact that the geometrical field factor, γ, was associated with an anode which was at a distance of over 100 μm and β was associated with the gate which was at a distance of under 50 nm.

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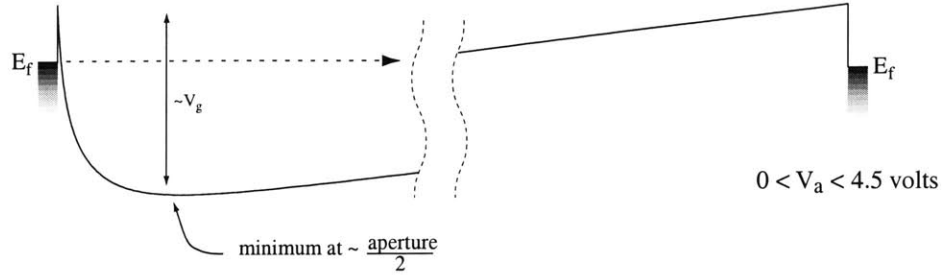
Figure 91: Potential profile from emitter tip to anode at 0 V

Although the emission current does not depend on the anode voltage, the current collected by the anode was a function of the anode voltage. Figure 91 through Figure 93 show one-dimensional potential profiles from the emission tip to the anode, (for various V_a from 0 V to the typical V_a $\gg V_g$ where FEAs are usually operated). The first profile in Figure 91 shows $0 < V_a < 4.5$ where 4.5 is assumed to be the workfunction of the anode material. Because electrons are emitted at the Fermi-level in field emission, they do not have the energy to overcome the barrier at the anode, and no anode current should be collected. In Figure 92, when $V_a = 4.5$, electrons are collected by the anode (this could be seen in Figure 94 and Figure 95 for various V_g and anode distances).
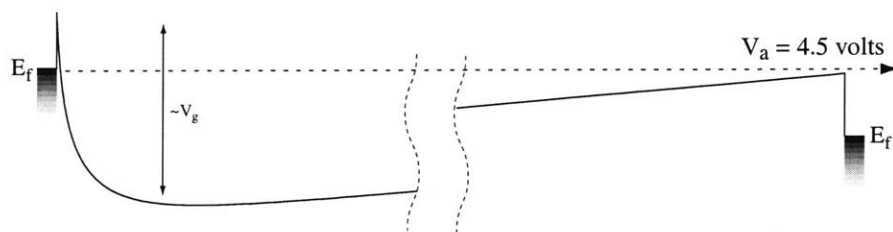
Figure 92: Potential profile from emitter tip to anode at 4.5 V

Although under the condition $V_a < V_g$, there will have a retarding field between the gate and the anode, the electron should always reach the anode because of the kinetic energy it gains from the

initial acceleration by the gate potential ($\sim qV_g$). In the two-dimensional and three-dimensional cases, the emitted angle of the electron will effect its ability to be collected. If the retarding field is strong enough to cause the <u>vertical</u> component of the electron velocity to go to zero before it reaches the anode, then the electron would be accelerated back to the gate.
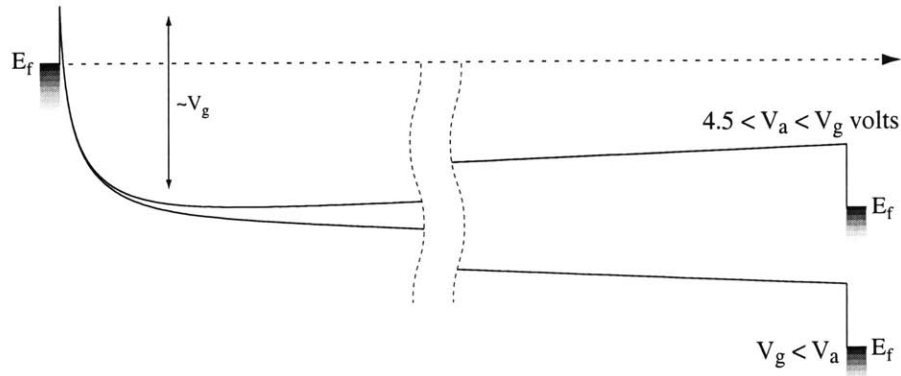
Figure 93: Potential profile from tip to anode for various $V_a > 4.5$

The variation in current collected in Figure 95 for the two anode positions can be attributed to the effect of the electron emission angle. For the anode voltages shown, the anode that has larger emitter/anode separation does not collect as much current as the anode that has smaller emitter-anode separation. The difference between them was that the electrons leaving the gate aperture region do not have large enough vertical velocity after leaving the gate region to overcome the retarding field mentioned above.
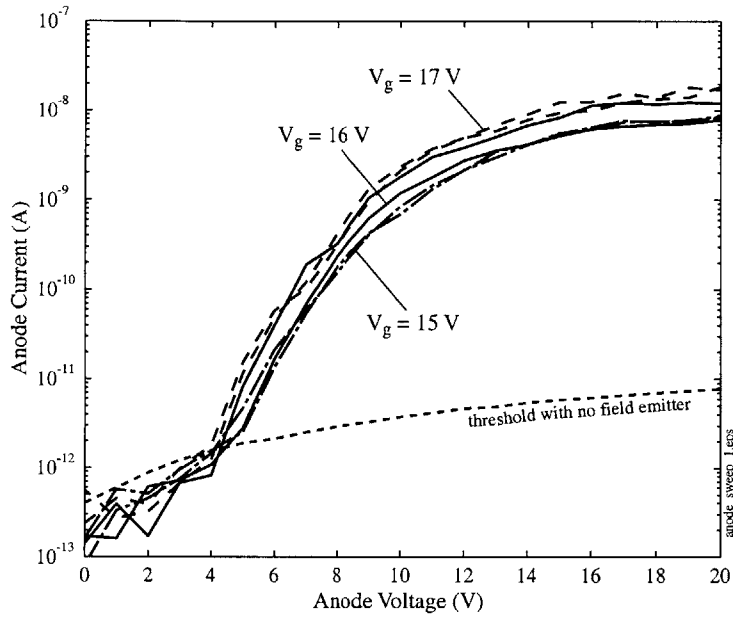
Figure 94: Anode Current as a Function of Anode Voltage

The emitted current is only collected at the anode when the it can overcome the barrier at the anode and when the field is strong enough to prevent the current from being attracted back down to the gate. The total emitted current for these measurements remained constant.
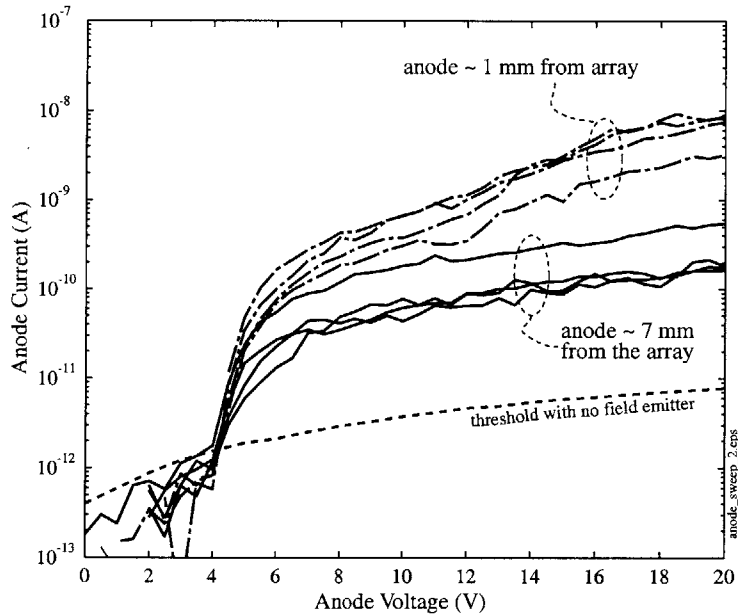
Figure 95: Collection of electrons for two anode distances

The closer anode was able to collect more current due to its position. For the higher anode, the retarding field was able to reduce the velocity of a portion of the electrons to zero before they were collected.

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6.2.3.3 Hydrogen Clean

The condition of the surface affects the emission of electrons from the material [119]. Contaminants, surface states or a thin oxide can effect the barrier height and reduce the emitted current density. We investigated the use of hydrogen treatments to change emission properties. An array was first tested under UHV conditions. While the device was operating the pressure in the chamber was increased by throttling the vacuum valve to the pump and leaking in hydrogen. Figure 96a shows the initial IV characteristic of the device. Figure 96b is a plot of the measured anode current as a function of the H_2 pressure. By running the device in the H_2 ambient, the high local fields around the tips can ionize the hydrogen. The contaminants or oxides on the surface would be removed by the excited species. The effect is similar to that reported for glow discharge plasma treatment in hydrogen [119].
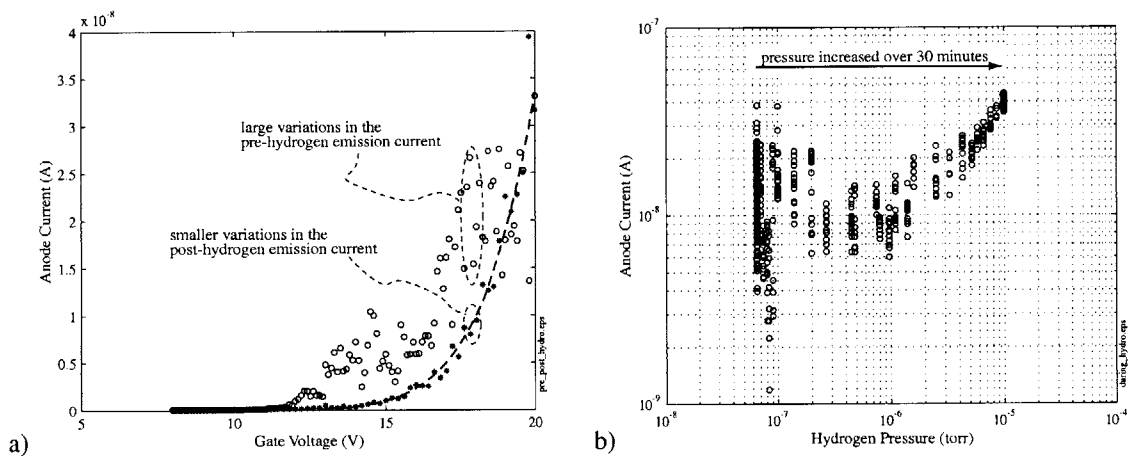
Figure 96: Effect of Device Operation in H₂ Ambient

a) Prior to the operation in a H2 ambient, the emission from the device was very noisy (o). b) As the H2 pressure was increased, b) shows the emission current increased and stabilized. After the chamber was pumped back down, the dashed line in a) shows good agreement with Fowler Nordheim theory and the measurement after running in the H₂ ambient (*).

We observed similar effects by operating the device in hydrogen ambient as previously reported [120, 121]. The result was an increase and stabilization of the emission current. This is

observed in the right tail of the data in Figure 96b and the stabilized IV characteristic in Figure 96a which was taken when the chamber was again restored to UHV conditions.

6.2.3.4 Charged Nitride Layer

Some devices were fabricated with a thin nitride layer between the gate oxide and the polysilicon gate. This additional layer was reported to reduce gate leakage [122] by increasing the creep distance (distance along the dielectric surface between the gate and cathode). This nitride layer would remain under the gate after the exposure of the tip by removing of some gate oxide.

100 μm x 100 μm arrays with the nitride layer initially turned on at voltages as low as 10 volts, emitted currents as high as 2 μA at a voltage of 14 volts, and exhibited extremely low gate currents of only a few nA. At a constant gate voltage, the emitted current would gradually decay and the device would, over a period of a few minutes, settle in to a lower anode current. In the downward ramp of the gate voltage the IV characteristics shifted to higher voltages indicating lower current for the same gate voltage. If the device was left off for a few minutes, the original I-V data could be reproduced.

This non-permanent change in the device was attributed to charging of the nitride layer. Figure 98 shows an emitter tip with the nitride layer. A build-up of emitted or leaked charge on the nitride would terminate electric field lines analogous to a capacitor structure that would effectively lower the electric field on the surface of the emitter tip. A portion of the applied voltage would now be dropped across the capacitive layer, and result in a reduced surface electric field.

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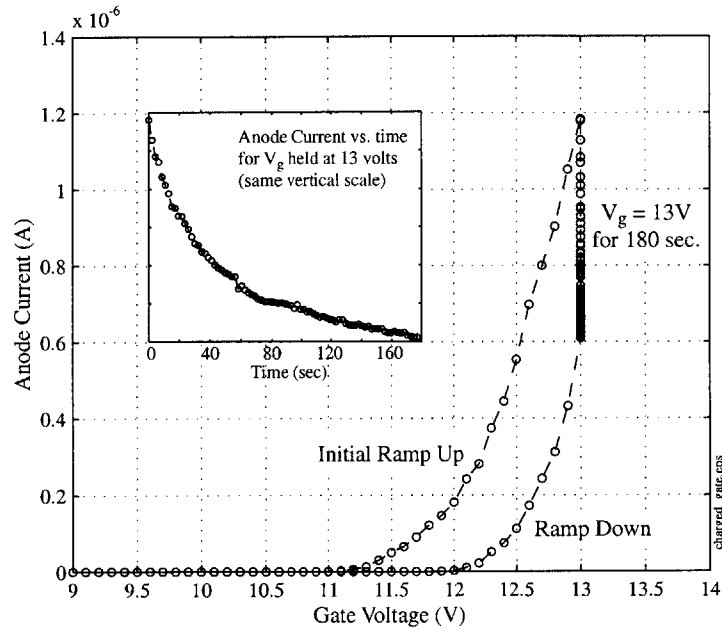
Figure 97: Reduction in emitted current over time

The devices IV characteristics will gradually and not-permanently change over time while the device is operating. If the device is left off, the original performance will be re-established.

silicon substrate
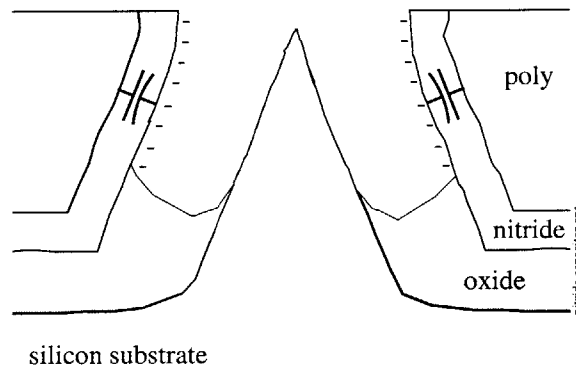
Figure 98: Emitter Tip with Nitride Layer

The nitride layer could hold charge on it's surface which could terminate electric field lines and act as a capacitor, effectively lowering the gate voltage from the tip's point of view.

Based on the voltage shift shown in Figure 97 and the structure in Figure 98 estimates were made to determine the charge that would be necessary to cause voltages of ~1 V on a capacitor similar in structure to the nitride layer. The 1 V shift in the two curves above does not take into

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account the fact that there could be charging of the capacitor as the voltages is quickly ramped up from $V_g = 0$ V. Assuming an area of 7500 nm^2 per tip and a 250,000 tip array, the capacitance of the 15 nm thick nitride would be ~7.7 pF. For a voltage of 1V on this capacitor, that would require ~7.7 pC of charge. Even at low voltages, only a small fraction of the gate current, which was in the range of 10^{-9} A, would have to remain to induce this effect.

Although these devices did have almost an order of magnitude less gate current than the devices without nitride, the nitride layer did have the effect of raising the gate voltage required to get a certain amount of emission. The effect of depositing charge on the nitride layer creates a charge storage medium in the device analogous to a 'memory' in the device. There may be applications where an FEA exhibiting a 'two state', may be useful if the charge does not leak readily. Additional device design could contribute to a 'self-limiting' device that has a feedback path where the current flows affect the charge storage on the nitride. This in turn effects the field on the tip, which could close the feedback loops and affect the current.

6.2.3.5 Analysis of Silicon Arrays using numerical simulation

Based on the electrical measurements, the silicon devices were analyzed using the numerical simulation in the manner as described in Chapter 5. In order to match the slope of the FN plot of the array whose data is shown in Figure 86, the numerical simulation required an aperture of 100 nm and a tip radius of 2.1 nm. The value of the simulated emission current and the simulated emitting area of the array is a factor of 100 more then the measured experimental data. Based on the tip distribution presented earlier, we attribute this to the fact that only a few percent of the tips have a radius as sharp as 2 nm and they will dominate the device performance. Additionally, the non-planar aspect of the array could result in the loss of tips in the outer edge of the array, through polishing. For the 100 µm array shown in Figure 78, 5 µm of tips along the outer edge

could have been polished, resulting in the reduction of tips by 20%. The amount of array that could have been damaged by polishing varied based on the device and it's location. Devices that were tested showed overpolishing of the array edge by up to 15 μm.

A more complex electrostatic simulation was used to verify that a small portion of tips can dominate the device performance and give the array the characteristics of a smaller array with only sharp tips. A model of a 100 μm x 100 μm array with a tip distribution as presented above was built. This model was made by varying the tip radius in individual simulations for each bin of the distribution, appropriately weighted by the number of tips as given by the distribution. The total current for the array is the sum of the individual models, where I_i is the current from a tip with radius$_i$ and n_i is the number of tips with that radius.

$$I_{array} = \sum_i I_i(radius_i) \cdot n_i \text{ , where } \sum_i n_i = 250,000$$

The total number of tips was 250,000 to correspond to the number of tips in a 100 μm x 100 μm array. Figure 99 shows the results of that simulation, and the comparison to a uniform tip radius array. In order to achieve a equivalent field factor, β, a 1.7 nm uniform array was modeled. If the variation in the effective emitting area is attributed to the number of tips emitting, approximately 5% of the tips would contribute to the emission current. This was verified by modeling a 12,500-tip array of 1.7 nm tips as shown in Figure 99.

The use of the numerical model in conjunction with tip distribution data verified that an array's performance is dominated by the sharpest tips even if they make up only a small percentage of the total. This could account for the deviation in $\alpha_{measured}$ from $\alpha_{experimental}$ for a simulation of uniform tips. This effect is more important as the tip radius is reduced. The difference in

performance between a 2 nm and a 3 nm tip, is much more significant then the difference between a 12 nm tip and a 13 nm tip. This can be demonstrated by considering that β increases 51% when changing from 3 nm to 2 while it only increases 7.8%. This may explain the apparent uniformity of the device reported by Ding [109].
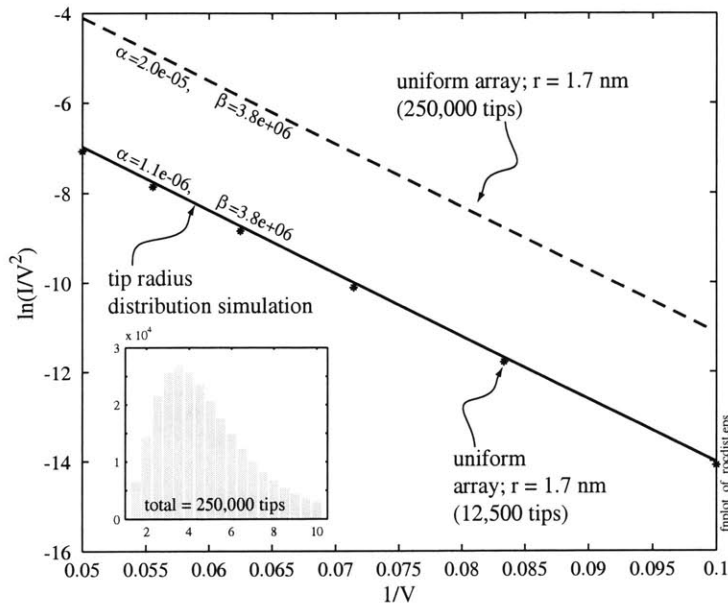
Figure 99: FN plot for an array with a Log-Normal tip distribution

The two lines shown are of electrostatic simulations of two 100μm x 100μm arrays (250,000 tips). The top line is an array of tips that are uniform 1.7 nm across the array. The bottom is an array of tips with a distribution as shown in the inset (this is the same distribution shape that was determined in Section 6.2.1 in Figure 83. For comparison, an array of 12,500 (5% of 250,000) was also simulated. The two plots indicate that an array with a distribution of tips will be dominated by the performance of the sharpest tips even if these are only a fraction of the total number of tips.

Numerical simulation of an array with a tip distribution was then compared to experimental data. Figure 100 shows the results when using a tip distribution as determined by the measurements that were made at MIT and assuming a full 250,000 tip array, (the AMER measured tips were excluded because the measurements were made outside of our control and may not have been random in nature). The difference in intercept between the simulation and experimental data is attributed to array damage during the polishing as discussed earlier. A 15 μm wide damaged

region along the edge of the array can result in a loss of over 50% of the tips causing the shift shown.
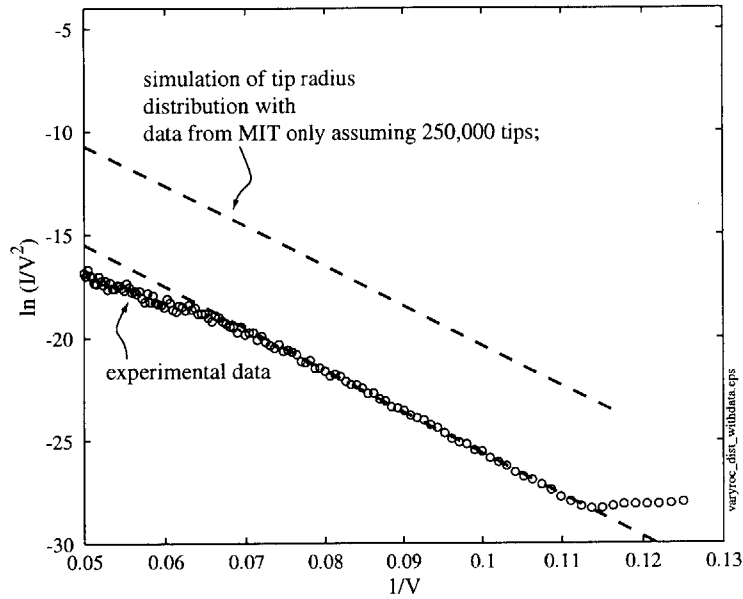
Figure 100: FN plot comparing experimental data to simulation of tip radius distribution

6.2.3.6 MOSFET driven FEAs

In order to investigate the performance of the silicon arrays operating with MOSFETs, the array was then connected to a standard n-channel MOSFET as the source of current. The system was configured as shown in the inset of Figure 101. The FEA was set up with a gate voltage of 15 volts and the FET was initially set with a gate voltage of –5 volts to keep it off. The gate voltage of the FET was swept from – 5 to –1 volt and was able to control the emission (and anode) current of the FEA.

The data from Figure 101 is re-shown in Figure 102 and in both figures includes a dashed line showing the transfer characteristics of the individual MOSFET (V_{ds} = 15V) and the individual FEA V_{gFEA} = 15 V also shown. The graphs show three distinct regions in the device

characteristics, (only two are visible in Figure 102 due to the linear scale). To the left of V_{gMOS} = -2V the current is limited by the FET. This region could be considered analogous to a FEA operating in the supply-limited region. The flux of the electrons to the surface is the dominant parameter. For V_{gMOS} above -2 V the current is limited by the FEA. This region is controlled by the probability of tunneling through the barrier. Increase in current flow would require changes to the barrier, which could come about by increasing V_{gFEA}. Increasing V_{gFEA} would shift the horizontal line in Figure 102 up to a higher steady state operating current. The third region is only evident in Figure 101 where the resolution of the test system limits the accuracy of the test system at V_{gMOS} below -2.4 V.
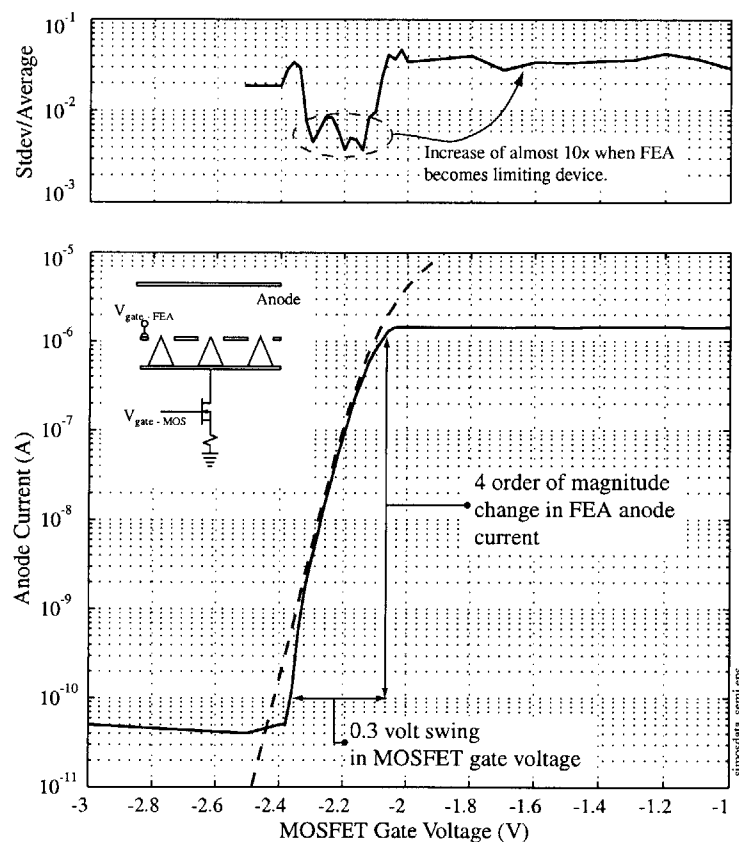
Figure 101: Performance of Si-FEA with MOSFET 'current supply'
The saturated MOSFET acted as a voltage controlled current supply for the FEA. The low gate voltage of the array (V_{gFEA} = 15 V) allowed the use of a standard discrete MOSFET.

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As the MOSFET gate voltage was varied, multiple data points (>10) were taken at each voltage. The data presented is an average at each of the MOS gate voltages. The spread in the data at each of the MOS gate voltages depended on the region of operation. When the FEA was the limiting device, the variations were almost an order of magnitude higher then when the MOSFET was the limiting device. The upper plot in Figure 101 shows these two regions by plotting the standard deviation of the data divided by the average for each MOS gate voltage. The leftmost bump in the 'Stdev/Average' plot shown in the top of Figure 101 is attributed to the operation in a regime that is limited by the test system. Current level are ~ 40 pA and cause larger normalized variations in the current.
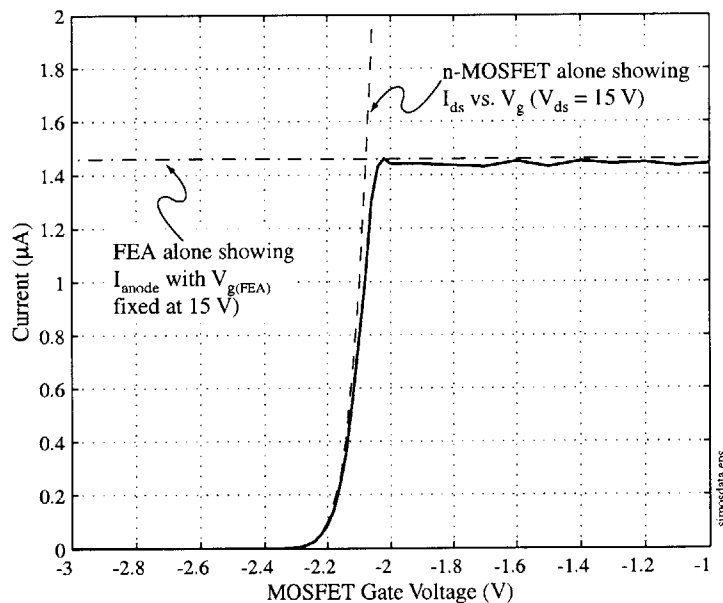
Figure 102: FEA-FET data

The FEA-MOSFET data is shown with the performance data of each individual device overlaid. The combination shows two distinct regions. To the left of $V_{gMOS} = -2$ V the current is limited by the FET (electron supply limited) while at V_{gMOS} above -2 V the current is limited by the FEA (electron tunneling limited).

The combination of the FEA and FET allows emission current to be controlled by a small voltage in addition to creating a more stable emission current when operating in the FET limiting regime.

6.3 SUMMARY

Silicon FEAs were fabricated using interferometric lithography, using an isotropic etch process. Thermal oxidation was used to further sharpen the tips. Both electrical characterization and observation in SEM and TEM confirm a tip distribution with a few percent of the tips at approximately 2 nm radius. Silicon FEAs turned on as low as 10 V and achieved currents as high as 30 μA at 21 V. The operation of a low voltage FEA / MOSFET hybrid (two discrete devices) demonstrated the ability control stable emission current with a signal as small as 0.4 V.

7 CONCLUSIONS

This thesis investigated low voltage operation of field emitters and has presented a study using small aperture and small period field emission arrays to attain low-voltage operation. The main objective was to demonstrate FEAs that can operate at gate voltages of ~ 15V by taking advantage of nano-scale geometries and high cone packing densities.

7.1 SUMMARY OF RESULTS

Numerical simulations using a 2D axially-symmetric finite element solver in MATLAB were used to determine the effect on performance of scaling of field emitter array (FEA) to gate apertures of 100 nm. These simulations indicated that by scaling the gate aperture, it is possible to fabricate devices that will support display applications at a gate voltage of 15 V.

Using interferometric lithography, we have fabricated FEAs with 100 nm apertures at a period of 200 nm, giving the highest cone densities reported (2.5 x 10^9 cones/cm^2). There was good agreement between device simulation and experimental results, both indicating that the operating voltage of the FEA will be reduced as the gate aperture is scaled down to 100 nm. We demonstrated 100 nm gate aperture Molybdenum FEAs that turned on at gate voltages as low as 12 V and achieved a current density of 10 μA/cm^2 at 17 V. The molybdenum devices were able to modulate emission current density by three orders of magnitude with a gate voltage swing of 5 V. The successful use of the molybdenum devices with a discrete MOSFET as a voltage controlled current supply was also demonstrated.

Using similar lithography, we demonstrated 70 nm gate aperture Silicon FEAs at a 200 nm period that turned on at gate voltages as low as 10 V and achieved emission currents of 1 μA at

V_g of 13 V, which represents an array current density of approximately 10,000 μA/cm^2. Currents as high as 30 μA were measured at V_g of 21 V. The use of numerical simulation to analyze experimental array performance indicated that the tested arrays exhibited characteristics of simulated devices with tip radius of 2 nm. An analysis using a TEM was done to determine a tip radius distribution (~100 tips were measured) and verified tips radii under 2 nm, which was in agreement with the electrical characterization and simulation. More detailed simulations using the calculated tip distribution confirmed the fact that only the sharpest tips, even if only a small percentage of the total, will dominate the array performance. Silicon arrays were also successfully operated with a discrete MOSFET used to modulate the cathode current supply. A 0.4 V signal to the gate of the transistor was able to modulate the emission current by 4 orders of magnitude.

This work has shown that the operating voltage of field emitter arrays can be significantly reduced by scaling the devices to the 100-nm size regime. These ultra sharp tips still exhibited Fowler-Nordheim type emission over the range of voltages we applied. Traditional theories that are used to describe FEAs could be extended to this size regime and were valid for low gate voltages but deviated at higher voltages. This size regime posed many fabrication challenges that can translate into variability in device performance. Low gate voltage operation allows the device to overcome this variability by the integration with solid state devices that can control the device performance, and produce a hybrid device that is better then either individual and may enable additional applications.

7.2 RECOMMENDATIONS FOR FUTURE WORK

This work has successfully achieved its goals of exploring the forefront of FEA technology in the nano regime, and demonstrating devices with excellent electrical characteristics. There are many items that were learned but not investigated. This section will mainly focus on the lessons learned relating to fabrication, weaknesses in the process and suggestions for improvement.

7.2.1 Device Fabrication - Silicon:

Chemical Mechanical Polishing: The most difficult part of the silicon process was the CMP to planarize the gate and expose the gate apertures. This effort was made more difficult by non-uniformity across the wafer. Future processing should focus on this problem as the main hurdle for increasing device yield.

Tip Formation and Sharpening: Even though the silicon devices proved to be an excellent low voltage electron emitter, device performance could be improved by 100 to 1000 times if an array of uniform tips, (in the 2 nm size range, uniform to under 1 nm), could be fabricated. Although there may be room for improvements in the present process, it is this author belief that uniformity at this size can not be achieved by control of a lithography or etch step. The process must be modified to allow the over-sharpening of the tips until they possibly reach some fundamental limit that has not been explored in this work. Liu and Gamble report that repeated thermal oxidation with oxide removal in between has been was used as a way to achieve uniform tips for AFM applications [117]. Although the tip radii reported are almost an order of magnitude larger then one reported in this work, there may be some way to incorporate the oxidation mechanism.

MOSFET FEA Integration: The integration of FEAs on the same substrate (and as fundamentally one device as shown in Figure 67) has been reported in literature. The use of LV-FEAs in such a process will allow the use of more standard FET designs that do not need to withstand extremely high V_{DS}. Further work should look at how the MOSFET-FEA combination can act as a voltage controlled, low noise electron source. Current uniformity should be investigated to confirm that the overall MOSFET-FEA device would be more uniform, not dependent on variations in parameters such as tip radius.

Electron Supply Study to examine Saturation and/or Ballistic Transport: One of the areas that would be valuable to investigate is the question of electron supply in the silicon devices that are on this size scale, and the effect of current density

Device Testing: Further device testing should be done to examine the possibility of valence band emission from LV-FEAs. This testing will relate to the electron supply work above and the tip formation work. If a current limit could be identified for each size tip, it may be possible to indirectly determine the shape of the tip radii distribution through electrical characterization. More complicated models would be needed to interpret the changing slope of the FN at extremely high fields. It would be expected that smaller tips would be current limited while larger tips are not.

APPENDIX A: MOLYBDENUM FEA FABRICATION

This process is **Au contaminated**. Both the ARC and the PR are approved for processing in TRL. This process includes steps to pattern and isolate active regions to electrically test devices.

STEP	FACILITY	EQUIPMENT	NOTES
PREPARE SUBSTRATE			
Step 1: RCA Clean	ICL	RCA Station	
Step 2: Gate Oxide Growth	ICL	Tube A2	100 nm dry thermal oxide growth using recipe 121 and a variable time of 65 minutes at 1000C.
TRI-LEVEL RESIST AND INTERFEROMETRIC LITHOGRAPHY			
Step 3: Anti-Reflective Coating	TRL	coater	5 minute Ozone Clean followed by spin on of 130 nm of Brewers XHRi-16 ARC. Bake at 180 C.
Step 4: Interlayer evaporation	TRL	e-beam	15-20 nm thick SiO_2 using Planetary Holders. Deposition rate = 2 A/sec Density = 2.2 Acoustic Impedance = 8.25 Set Thickness to 0.200 kA Tooling = 214% **Power and Time Settings**
			Time Power Rise 1.0 ~ Soak 1.0 10 Pre-deposition 0.15 9 Maximum ~ 15
Step 5: Photoresist	TRL	HMDS/coater	200 nm of Sumitomo Resist PFI-34A2 with a pre-bake at 90 C.
Step 6: Interferometric Lithography	CSR	Main Holography System.	Exposure of 200nm period array with a dose of approximately 18.5 mJ/exposure. Develop on the CSR wafer-track using recipe 1, which is a 1 minute bake at 120 C and a 30 second develop in OPD-262.
TRI-LEVEL ETCH AND GATE LIFT-OFF			

Step 7: Tri-level etch	TRL	Plasmaquest	Three level etch made up of a descum (O_2 RIE), oxide etch (CF4 RIE), ARC etch (O_2 RIE).
Step 8: Chromium Gate Evaporation	TRL	e-beam	50 nm Chromium evaporation using the angled evaporator fixture with $\theta = 0°$
Step 9: Chromium Gate Lift-off	TRL	Acid Hood	Using nanostrip, remove the ARC. Done at room temp for 1 minute in the ultrasonic bath to avoid the re-deposition of the Chromium or oxide caps on the substrate. Place the wafer into the beaker using a single wafer holder with the wafer facing at a downward angle. When the wafer is removed, immediately rinse with flowing DI before putting in a DI bath.

PATTERN ACTIVE REGION OF DEVICES

Step 10: Photoresist	TRL	Coater	Standard Resist for Image Reversal. Pre-bake at 90 C for 30 minutes.
Step 11: Mask #1 Exposure, active region definition	TRL	Karl Suss Aligner 2	Standard Image Reversal process. With develop and postbake at 130 C for 30 minutes
Step 12: Second Chromium gate evaporation to cover non-active regions	TRL	e-beam	50 nm Chromium evaporation. The standard lift-off plate can be used based on the size of the features that will be lifted-off.
Step 13: Lift-off of the Chromium	TRL	Photo-wet Right	Acetone to lift-off PR

GATE OXIDE ETCH AND CONE DEFINITION

Step 14: Gate Oxide Etch	TRL	Plasmaquest	Oxide etch (CF_4, O_2) if there is a possibility of a polymer build-up, a short O_2 RIE may be added to the end of the recipe to insure a contact with the substrate. H_2 is added to the etch to stop on the Silicon substrate.
Step 15: Parting Layer Evaporation	TRL	e-beam	Angled Evaporation of 15 nm of Al to form gate parting layer; angle determined from SEM (typically $\theta = 70°$).
Step 16: Vertical Cone Deposition	TRL	e-beam	Vertical evaporation of Molybdenum to form cone thickness = 150 nm

PATTERN DEVICES AND GATE CONTACT PADS

Step 17: Photoresist	TRL	HMDS/coater	Standard Positive resist process followed by a 90 C 30 minute bake.

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Step 18: Mask #2 Exposure, pad definition	TRL	Karl Suss Aligner 2	Standard Exposure and develop followed by a 30 minute post-bake at 120 C.
Step 19: Metal Etch	TRL	Plasmaquest	Using a three step recipe, etch though the Molybdenum, Aluminum and Chromium layers to isolate the devices. This patterning will also help in the lift-off process to remove the sacrificial Al and excess Molybdenum.
Step 20: Oxide Removal	TRL	Acid hood	Using a swab, remove the native oxide from the back of the wafer with BOE.

FINAL DEVICE PREPARATION

Step 21: Removal of parting layer	5th Floor Group Lab	Hood	Remove Aluminum parting layer using NaOH and ultrasonic. Follow this clean with a Detergent clean. There should also be a solvent clean once the wafer is returned to TRL.
Step 23: Back contact evaporation	TRL	e-beam	Evaporation of Al onto the back of the wafer for contacting the substrate.
Step 24: Surface cleaning of field emitter tips	TRL	Plasmaquest	Optional Step: there may be a desire to do a H_2 plasma clean of the field emitter tips prior to removing them from TRL.

APPENDIX B: SILICON FEA FABRICATION

This process is **not** Au contaminated. Almost all processing is done in ICL. For facilities outside ICL, (CSR, NSL) new wafer chucks and holders were fabricated and there are dedicated tweezers and processing tools for these non-gold wafers. Both the ARC and the PR used have been previously approved for processing in TRL and ICL.

STEP	FACILITY	EQUIPMENT	NOTES
PREPARE SUBSTRATE			
Step 1: RCA Clean	ICL	RCA Station	
Step 2: Gate Oxide Growth	ICL	Tube A2	100 nm dry thermal oxide growth using recipe 121 and a variable time of 65 minutes at 1000C
TRI-LEVEL RESIST AND INTERFEROMETRIC LITHOGRAPHY			
Step 3: Anti-Reflective Coating	ICL	coater	6 second ash followed by spin on of 130 nm of Brewers XHRi-16 ARC. Bake at 180 C.
Step 4: Interlayer evaporation	ICL	e-beam	15-20 nm thick SiO_2 using Planetary Holders. Deposition rate = 2 A/sec Density = 2.2 Acoustic Impedance = 8.25 Set Thickness to 0.200 kA Tooling = 214% Power and Time Settings Time / Power Rise 1.0 / ~ Soak 1.0 / 10 Pre-deposition 0.15 / 9 Maximum ~ / 15
Step 5: Photoresist	ICL	HMDS/coater	200 nm of Sumitomo Resist PFI-34A2 with a pre-bake at 90 C.
Step 6: Interferometric Lithography	CSR and ICL	Main Holography System and ICL coater track	Exposure of 200nm period array with a dose of approximately 18.5 mJ/exposure. After dose wafers are done and analyzed, developing is done in the ICL on the developer track which is a 1 minute bake at 120 C and a 30 second develop in OPD-262.

FOUR-LEVEL ETCH

Step 7: Four-level etch	ICL	AME-5000	Four level etch made up of a Descum (O_2 RIE), Oxide etch (CHF_3 RIE), ARC etch (O_2 RIE) and a final Oxide etch (CHF_3 RIE).
Step 8: Rough Cone Formation	ICL	Etcher-1	Using recipe 011 with a modification to the final step to reduce the pressure to 350 mT
Step 9: Removal of ARC and PR with Piranha Clean	TRL	Acid Hood	In-order to avoid any interlayer caps that may remain, the ARC removal is done in the TRL acid hood in Silicon compatible glassware.

MESA FORMATION

Step 10: Piranha Clean	ICL	Pre-metal Bench	Do this clean in order to return to processing in ICL.
Step 11: Nitride Deposition	ICL	Concept-One	Deposit 2000 A of Si_3N_4, Use recipe '2000a nitride'. The densification will reduce the thickness to 94% of the originally deposited thickness.
Step 12: Nitride Densification	ICL	Tube B5	Recipe 205 at Temp of 950 C for 30 minutes
Step 13: Mask #1 to define Mesas	ICL	HMDS, coater, stepper2, developer	Using standard PR coating, exposure and develop. Pattern the regions that will remain as the mesas on the wafer.
Step 14: Etch Nitride and Form Mesa	ICL	Etcher-1	Etch Nitride and underlying Silicon to a depth of 0.5 μm.
Step 15: Ash to Remove PR	ICL	Asher	Standard Ash to remove Photoresist
Step 16: Pre-metal Clean	ICL	Pre-metal	Standard green piranha and HF dip prior to tube run.
Step 17: LOCOS I	ICL	Tube B5	Oxidize to form approximately 1000A of oxide. Recipe 122 which is at a temp of 1000 C for 7 minutes, 12 seconds.
Step 18: Nitride Cap Removal	ICL	Nitride Bench and BOE Bench	Short HF dip prior to Nitride removal in hot Phosphoric.
Step 19: Piranha Clean	ICL	Pre-metal Bench	Do this clean in order to return to processing in ICL.
Step 20: Nitride Deposition	ICL	Concept-One	Deposit 2000 A of Si_3N_4, Use recipe '2000a nitride'. The densification will reduce the thickness to 94% of the originally deposited thickness.

Step 21: Nitride Densification	ICL	Tube B5	Recipe 205 at Temp of 950 C for 30 minutes
Step 22: Mask #2 to protect Mesas during LOCOS II	ICL	HMDS, coater, stepper2, developer	Using standard PR coating, exposure and develop. Pattern the regions that will remain as the mesas on the wafer. The alignment of this step to the previous exposure of Mask #1 is critical. This exposure should be 'underexposed' to make sure that the PR pattern is slightly larger then the previous use of this mask.
Step 23: Etch Nitride and Form Mesa	ICL	AME-5000	Etch through the nitride with a very anisotropic etch to form vertical side-walls. This is to maintain the nitride coverage on the mesa side-walls.
Step 24: Ash to Remove PR	ICL	Asher	Standard Ash to remove Photoresist
Step 25: Pre-metal Clean	ICL	Pre-metal	Standard green piranha and HF dip prior to tube run.
Step 26: LOCOS II	ICL	Tube B5	Oxidize to form approximately 4000A of oxide. Recipe 122, which is at a temp of 1000, C
Step 27: Nitride Cap Removal	ICL	Nitride Bench and BOE Bench	Short HF dip prior to Nitride removal in hot Phosphoric.

OXIDATION SHARPENING AND GATE FORMATION

Step 28: Pre-metal Clean	ICL	Pre-metal	Standard green piranha and HF dip prior to tube run.
Step 29: Oxidation Sharpening	ICL	Tube B4	Thermal oxidation using Dry O2. Recipe 206 at a temp of 900 C for a time of 3 hours. This step needs to be modified based on the rough cone formation above. The thickness of the thermal oxidation sharpening should be approximately equal to the neck. This is based on the consumption rate silicon during oxidation
Step 30: Additional Gate Oxide Deposition LPCVD Oxide	ICL	Tube A7	Conformal deposition of 20 nm of oxide to define the gate aperture to be approximately 100 nm in diameter. Recipe 454 (which is a slow version of the normal recipe) for 5 minutes assuming a rate of 42 A/min.
Step 31: LTO Densification	ICL	Tube B4	Recipe 201 was used with a time of 30 minutes
Step 32: RCA Clean	ICL	RCA Station	

Step 33: Polysilicon Deposition	ICL	Tube A6	Deposit conformal layer of doped polysilicon, 300 nm thick, Recipe 461 with a time of 45 minutes assuming a deposition rate of 65 A/min.
Step 34: Doping of the Gate	Ion Implant Services		Send out for Implant
Step 35: Dopant Activation	ICL	Tube B4	

PLANARIZE GATE

Step 36: Planarize Gate	ICL	CMP	Polish the gate flat
Step 37: Post CMP Clean	ICL	Pre-metal Bench	

PATTERN GATE AND FINAL DEVICE PREPARATION

Step 38: Mask #2 Patterning	ICL	HMDS, coater, stepper2, developer	
Step 39: Pattern the Polysilicon gate	ICL	AME-5000	
Step 40 Cut up Dies	ICL	Die Saw	
Step 41: Gate oxide removal	TRL	Acid hood	BOE Dip.

APPENDIX C: WKB APPROXIMATION

INTRODUCTION

The Wentzel-Kramers-Brillouin Approximation is useful when analyzing transmission through

barrier geometry described by a function V(x).
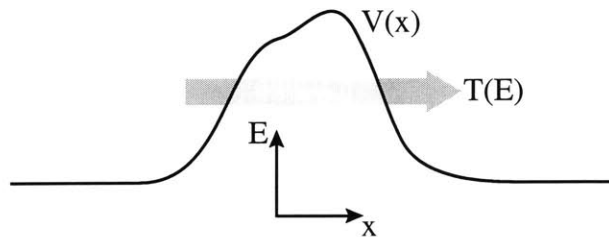
Figure 103: Example Barrier for use of WKB Approximation
1D Potential Barrier whose height is a function of x. The tunneling probability for an
electron at energy E is T(E).

RECTANGULAR BARRIER

For electrons with energy (E) below the top of a finite rectangular barrier ($E<V_o$), transmission

(T) through the barrier is described by (analytical solution):

$$\frac{1}{T} = 1 + \frac{V_o}{4(V_o - E)E} \sinh^2(2a\kappa),$$

where V_o is the height of the barrier, 2a is the width and:

$$\kappa = \sqrt{\frac{2m(V_o - E)}{\hbar^2}}.$$

This transmission function could be approximated by (analytical approximation):

$$T = \frac{4E}{V_o} e^{-4a\kappa}$$

when $E<<V_o$ and therefore $\kappa>>1$.

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ARBITRARY SHAPED BARRIER

It the barrier in Figure 103 is represented by a series of rectangles as shown in Figure 104 where

the tunneling probability through each rectangle is T_i, then the tunneling probability through the

entire barrier could be calculated as a product of the tunneling probabilities of each rectangle as:

$$T_{barrier} = \prod_{i=1}^{n} T_i \, .$$
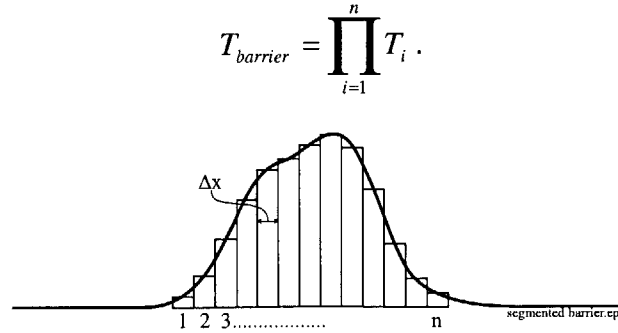
Figure 104: Segmented Potential Barrier
The barrier shown in Figure 103 represented by a series of rectangular barriers.

Using the approximation for the tunneling probability above, $T_{barrier}$ would be:

$$T_{barrier} = \left(\frac{4E}{V_1} e^{-2\kappa_1 \Delta x} \right) \left(\frac{4E}{V_2} e^{-2\kappa_2 \Delta x} \right) \cdots \cdots \left(\frac{4E}{V_n} e^{-2\kappa_n \Delta x} \right)$$

Which can be approximated as

$$T_{barrier} = e^{-\sum_{i} 2\kappa_i \Delta x}$$

Because with $\kappa \gg 1$ the exponential term will dominate. In the limit, the above summation can

be replaced by an integral where κ is a function of x because V is now a function of x.

$$T_{barrier} = e^{-\int_{0}^{d} 2\kappa(x) dx}$$

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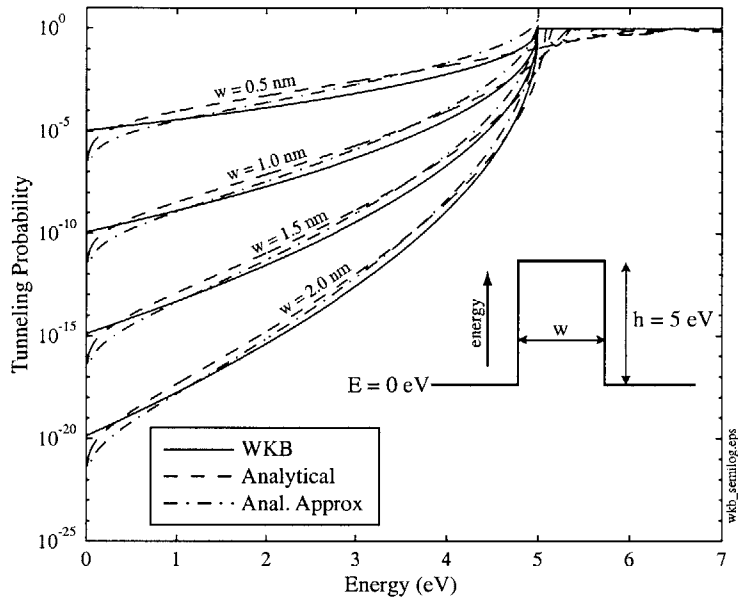
Figure 105: Comparison of WKB and Analytical Results

Comparison of the tunneling probabilities of an electron through a rectangular barrier as shown in the inset. The methods include the WKB integral, the complete analytical solution as solved using the Schroedinger equation and the approximation to the analytical solution.

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APPENDIX D: FOWLER NORDHEIM DERIVATION

Good and Mueller presented a derivation of the Fowler Nordheim equation in 1956 [123]. The tunneling current density is described by:

$$J(F) = e\int_{-\infty}^{\infty} P(E_x, F)dE_x = e\int_{-\infty}^{\infty} N(E_x)D(E_x, F)dE_x$$

where J is the emission current density per unit area which is a function of F, the surface electric field in V/m, $P(E_x,F) \cdot dE$ is the number of electrons within dE that emerge from the metal per second per unit area. P(E) could be broken down into a supply function $N(E_x)$ and a transmission function $D(E_x)$.

The supply function is described by:

$$N(E_x) = \frac{4\pi mk_b T}{h^3} \ln\left(1 + e^{\frac{E_F - E_x}{k_b T}}\right).$$

Where E_F is the Fermi-level (eV), k_b is Boltzman's constant (eV/K), m is the mass of an electron (eV/s·cm^2), T is temperature (K) and h is Plank's constant (eV·s).

The transmission function describes the probability that an electron at the surface with energy E_x will tunnel through the potential barrier described by V(x), x = 0 at the surface (Figure 106)

$$V(x) = -W_a \qquad\qquad \text{where x<0}$$

$$V(x) = -eFx - \frac{e^2}{4x} \qquad\qquad \text{where x>0}$$

0 V
vacuum level

$V(x) = -eFx$

$V(x) = -eFx - \dfrac{e^2}{4x}$

ϕ

$-W_a + E_F$

x_1 and x_2 are classical turning points for electrons at a given energy

μ

barrier eps

$-W_a$

x = 0 at surface
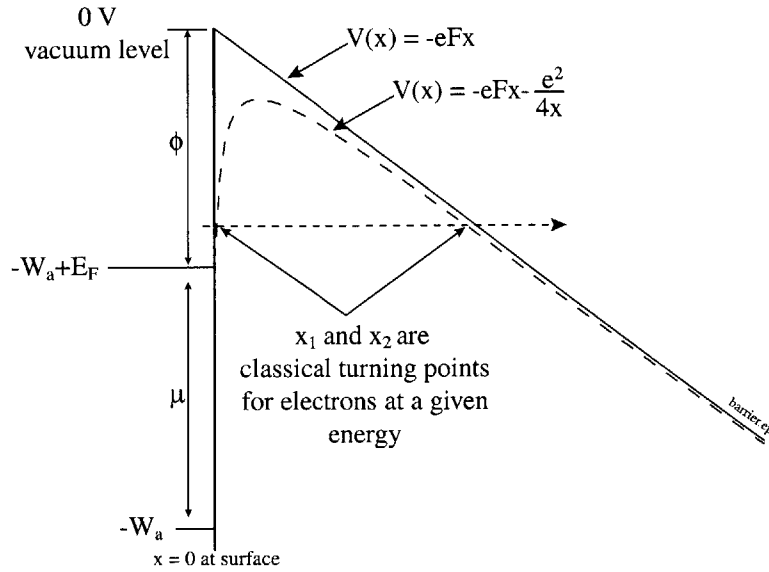
Figure 106: Potential Barrier at the surface of the metal

The barrier shown with and without the image potential. For the derivation done here, the vacuum level is assumed to be at 0V and the Fermi level is ϕ eV below that. The bottom of the band is at -Wa.

Using the WKB approximation, the transmission through this barrier can be approximated by:

$$D(E_x, F) = e^{\int_{x_1}^{x_2} \sqrt{\frac{8m}{\hbar^2}[V(x,F)-E_x]}\,dx}$$

This integral could be solved in terms of elliptical integrals of the first and second kind by introducing the parameter y where y is the following (initially y is presented as a function of the energy, the workfunction is substituted because of the typical emission energy of the electrons):

$$y = \frac{\sqrt{e^3 F}}{\phi}$$

To get:

$$D(E_x, F) = e^{-\frac{4\sqrt{2m|E|^3}}{3\hbar eF}v(y)},$$

where v(y) is:

$$v(y) = 2^{1/2}\sqrt{1+\sqrt{1-y^2}}\left[E(k) - \left(1-\sqrt{1-y^2}\right)K(k)\right],$$

E(k) and K(k) are the complete elliptic integrals of the first and second kind, and k^2 is:

$$k^2 = \frac{2\sqrt{1-y^2}}{1+\sqrt{1-y^2}}.$$

The above solutions for D and N can be combine to show that:

$$P(E_x, F) = \frac{4\pi mk_b T}{h^3} e^{-\frac{4\sqrt{2m|E|^3}}{3heF}v(y)} \ln\left(1 + e^{\frac{E_F - E_x}{k_b T}}\right).$$

Based on the assumption that most electrons are emitted with an energy approximately equal to the Fermi-level, the exponential factor from D can be replaced by a power series expansion and the introduction of t(y) as follows:

$$-\frac{4\sqrt{2m|E|^3}}{3heF}v(y) \approx -c + \frac{E - \phi}{d} \quad \text{where}$$

$$c = \frac{4\sqrt{2m\phi^3}}{3heF}v(y), \text{ and } d = \frac{heF}{2\sqrt{2m\phi}t(y)}, \text{ and } t(y) = v(y) - \frac{2}{3}y\frac{dv}{dy}.$$

Figure 107 shows the accuracy of the power series over the small range of interest at the Fermi-level.
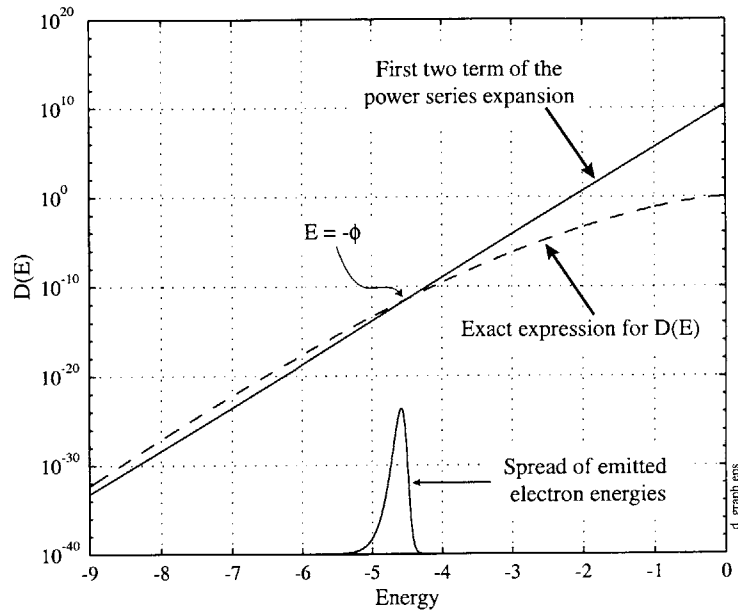
Figure 107: Exact and Approximate solution of D(E)

Comparison of the exact solution for D to the power series expansion around E=-φ. The lower part of the graph shows the spread of electron energies (arbitrary units) which was later calculated for an applied field of $F=2\times10^9$ V/m.
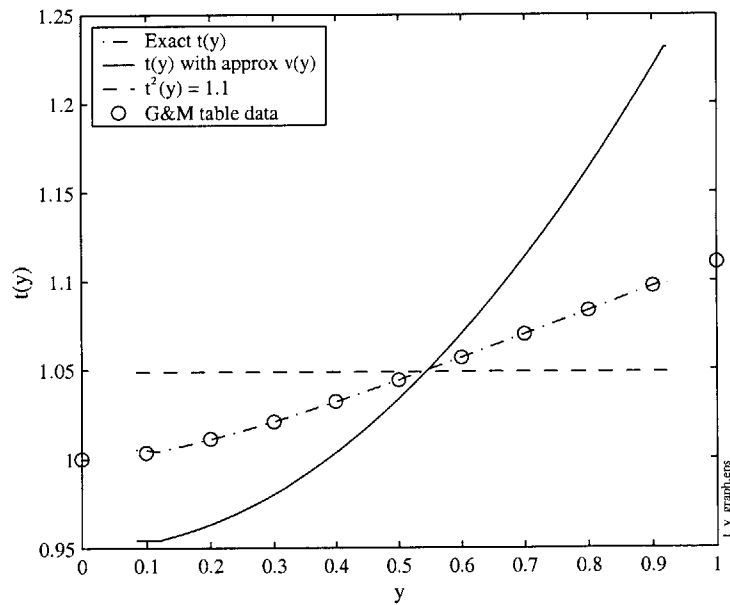
Figure 108: Comparison of Exact values of t(y) with various approximations.

Comparison of exact values of t(y) with the approximate found using an approximation for $v(y)=0.95-y^2$, and the approximation of $t^2(y)=1.1$. The exact results correspond well with the data from the table of Good and Mueller.

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Further approximations could be made with the assumption of a low temperature limit. At lower temperatures, N can be approximated by the following substitution:

$$k_b T \ln\left(1 + e^{\frac{E_F - E_x}{k_b T}}\right) = 0 \qquad \text{when } E_x > \phi$$

$$k_b T \ln\left(1 + e^{\frac{E_F - E_x}{k_b T}}\right) = \phi - E \qquad \text{when } E_x < \phi.$$

The results of this approximation are shown in Figure 109. The error is only evident in the region above the fermi-level.
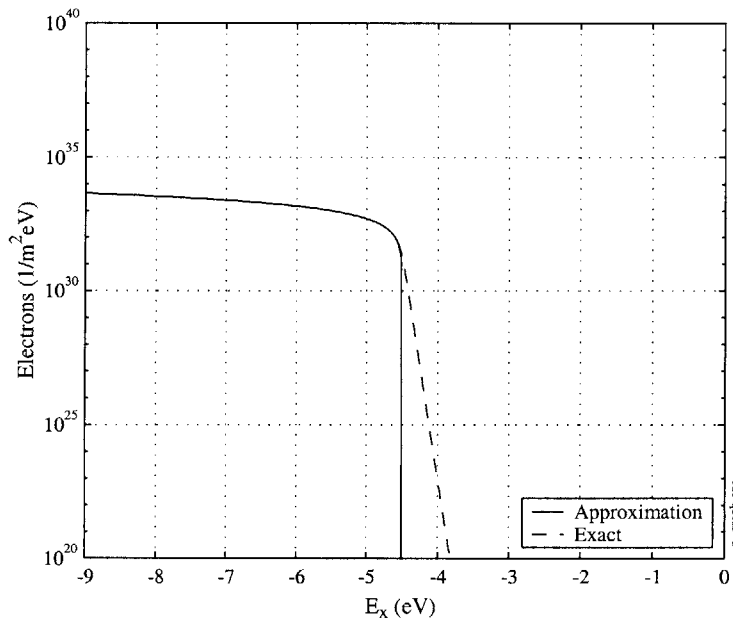
Figure 109: Exact and approximate values for N(E)
Comparison of the exact solution for $N(E_x)$ at $T=300K$ with the low temperature approximation.

A function P_{approx} could be found by combining all of the above approximations. Figure 110 compares the exact value of P to P_{approx}. By inserting values for constants into P_{approx} and integrating over all energies, the traditional Fowler Nordheim equation relating J (A/cm^2) to F(V/cm) and ϕ (eV) is found to be

$$J(F,\phi) = \frac{A \cdot F^2}{\phi \cdot t^2(y)} \cdot \exp\left(-B \cdot \frac{\cdot \phi^{3/2}}{F} \cdot v(y)\right)$$

where

$$v(y) = 0.95 - y^2, \quad t^2(y) = 1.1, \quad y = 3.79 \times 10^{-4} \frac{\sqrt{F}}{\phi},$$

and $A = 1.54 \times 10^{-6}$ and $B = 6.87 \times 10^7$.

The approximate solution (designated by J_{FN}) is compared to the exact solution (J_{exact}) with approximations is shown in Figure 111.
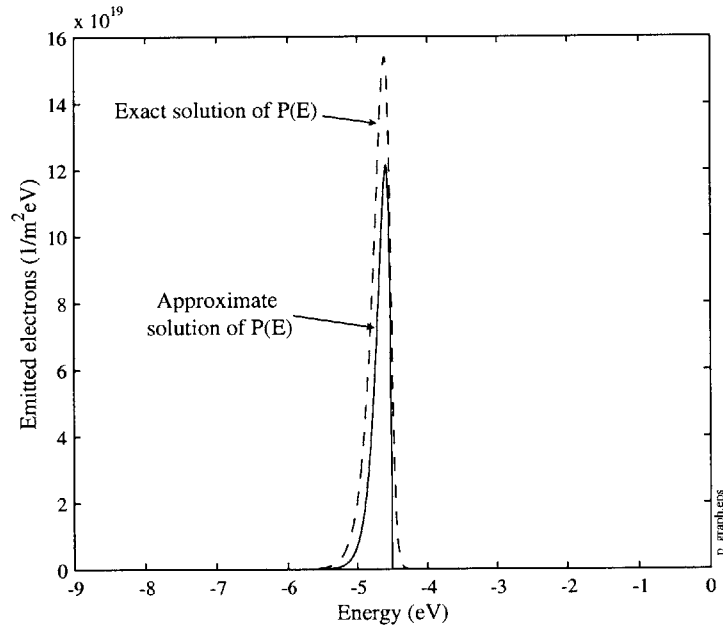
Figure 110: Comparison of exact and approximate values of P

Comparison of P as determined exactly from the elliptical integrals and complete function N to the P_{approx} which is calculated from the above approximations.

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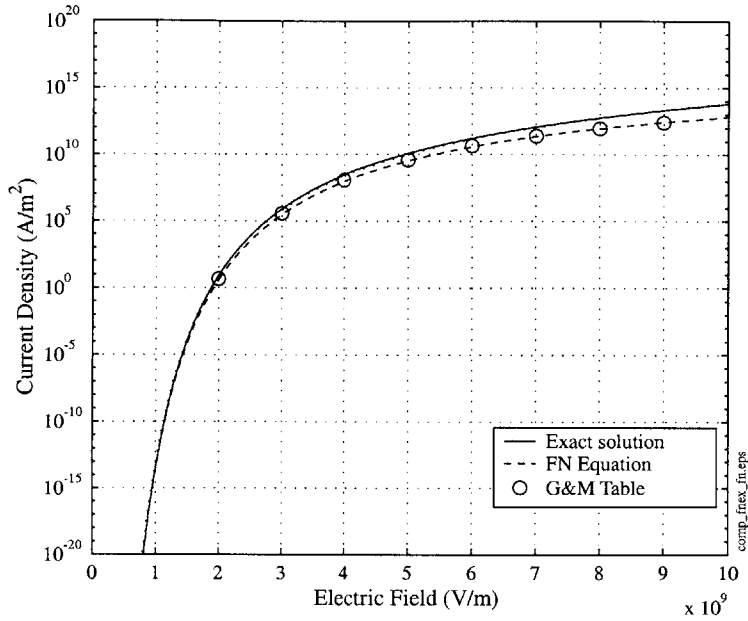
Figure 111: Various solutions for tunneling current J

Comparison of the exact solution of the tunneling current by integrating $P(E_x, F)$ over all energies while using the complete elliptical integrals (Exact), the approximation for $v(y)$, integration of P_{approx} and the J_{FN} as per the equation. Overlaid is also data from tables from Good and Mueller, which agree well with the traditional equation and the integration of the complete approximation of P_{approx}.

APPENDIX E: ELLIPTICAL INTEGRALS

The derivation of the FN equation is based on using the WKB approximation to determine the tunneling through a barrier. If this barrier contains components related to the image potential, the solution to the WKB integral has elliptical integrals.

K and E are complete elliptic integrals of the first and second kind:

$$K(k) = \int_0^{\pi/2} \frac{d\varphi}{\sqrt{1 - k^2 \sin^2 \varphi}}$$

$$E(k) = \int_0^{\pi/2} \sqrt{1 - k^2 \sin^2 \varphi} \, d\varphi$$

These functions were used in description of the Fowler Nordheim derivation. The numerical accuracy of their implementation needs to be verified. The MATLAB function:

$$[K,E] = ellipke(m, tol)$$

returns the values of K and E as a function of m, where $k^2 = m$. An exact implementation of the above equations was also written using numerical integration to evaluate K and E.

Table 10: Numerical Values of K(m) and E(m)

M	K(m)	E(m)
0.00	1.570796326794897	1.570796327
0.10	1.612441348720219	1.530757637
0.20	1.659623598610528	1.489035058
0.30	1.713889448178791	1.445363064
0.40	1.777519371491253	1.399392139
0.50	1.854074677301372	1.350643881
0.60	1.949567749806026	1.298428034
0.70	2.075363135292469	1.241670567
0.80	2.257205326820854	1.178489924
0.90	2.578092113348173	1.104774733
0.99	3.695637362989875	1.015993546
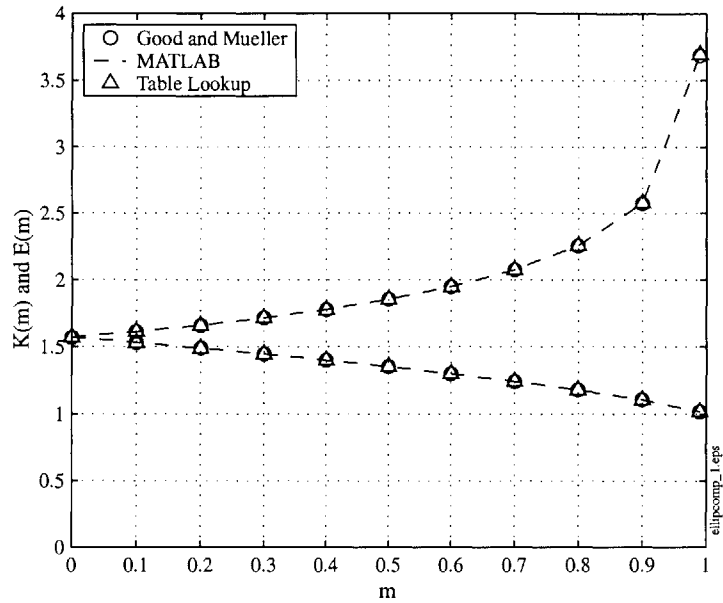
Figure 112: Comparison of Elliptical Integrals

The values of the complete integrals of the first and second kind as evaluated by the built-in MATLAB function, the numerical representation of the functions K(k) and E(k) above as presented in Good and Mueller [123], and the Table 10 above.
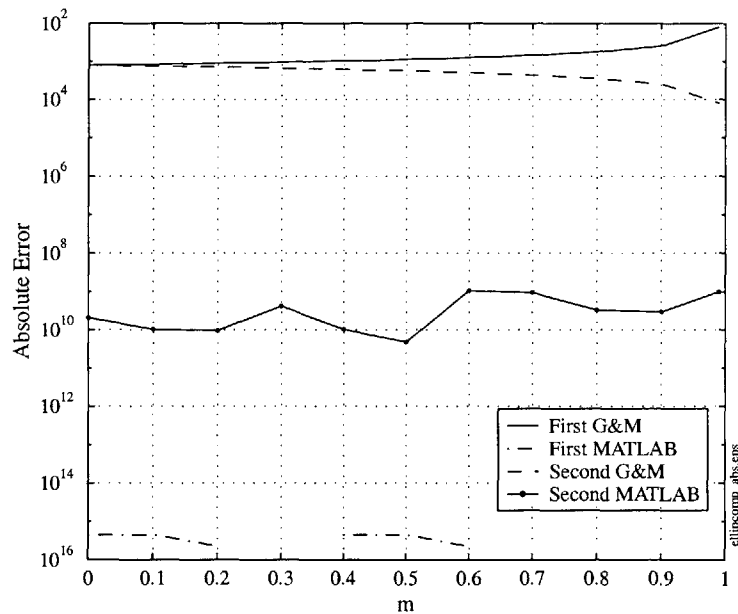
Figure 113: Absolute Error in Elliptical Integrals

The built-in MATLAB functions provide the most accurate results in comparison to the Table 10 above. The accuracy seems to be limited to the number of digits for the values of K(m) and E(m). The errors related to the numerical implementation of the equations above are assumed to be from the numerical methods.

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APPENDIX F: TEM IMAGES

In order to do analysis of the tip radius, the use of a transmission electron microscope (TEM) was necessary for measurement of the smallest tips. The following images were taken in a JEOL 2010 TEM at Advanced Materials Engineering Research Inc. The use of a standard TEM sample preparation with the very high cone packing density made it possible to examine multiple tips per TEM sample.

A standard TEM sample preparation includes:

- Coating the top of the sample with an epoxy and attaching it to another piece of material, in this case the other material was another piece of silicon to form a 'sandwich' with the tips protected on the inside.
- The 'sandwich' is mounted vertically so that the edge is polished until it is only 1 μm thick.
- The 'sandwich' is ion milled until a hole forms.
- The edges of that hole will be extremely thin and will allow inspection by a TEM.

The final result is shown 'edge-on' in
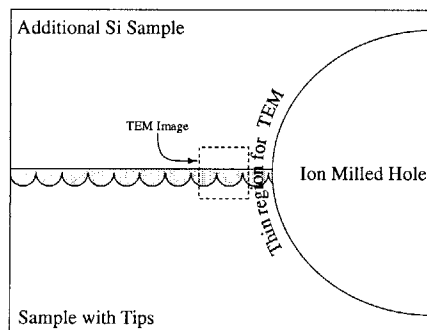
Figure 114: Standard TEM sample preparation

This edge on view of the sample is approximately 1 μm thick on the left side, and thinned down by ion milling until a hole is formed to the right. At the edge of the hole the sample is thin enough for TEM (approximately 200 nm thick).

Silicon

epoxy fill

50 nm

20 nm

2 nm
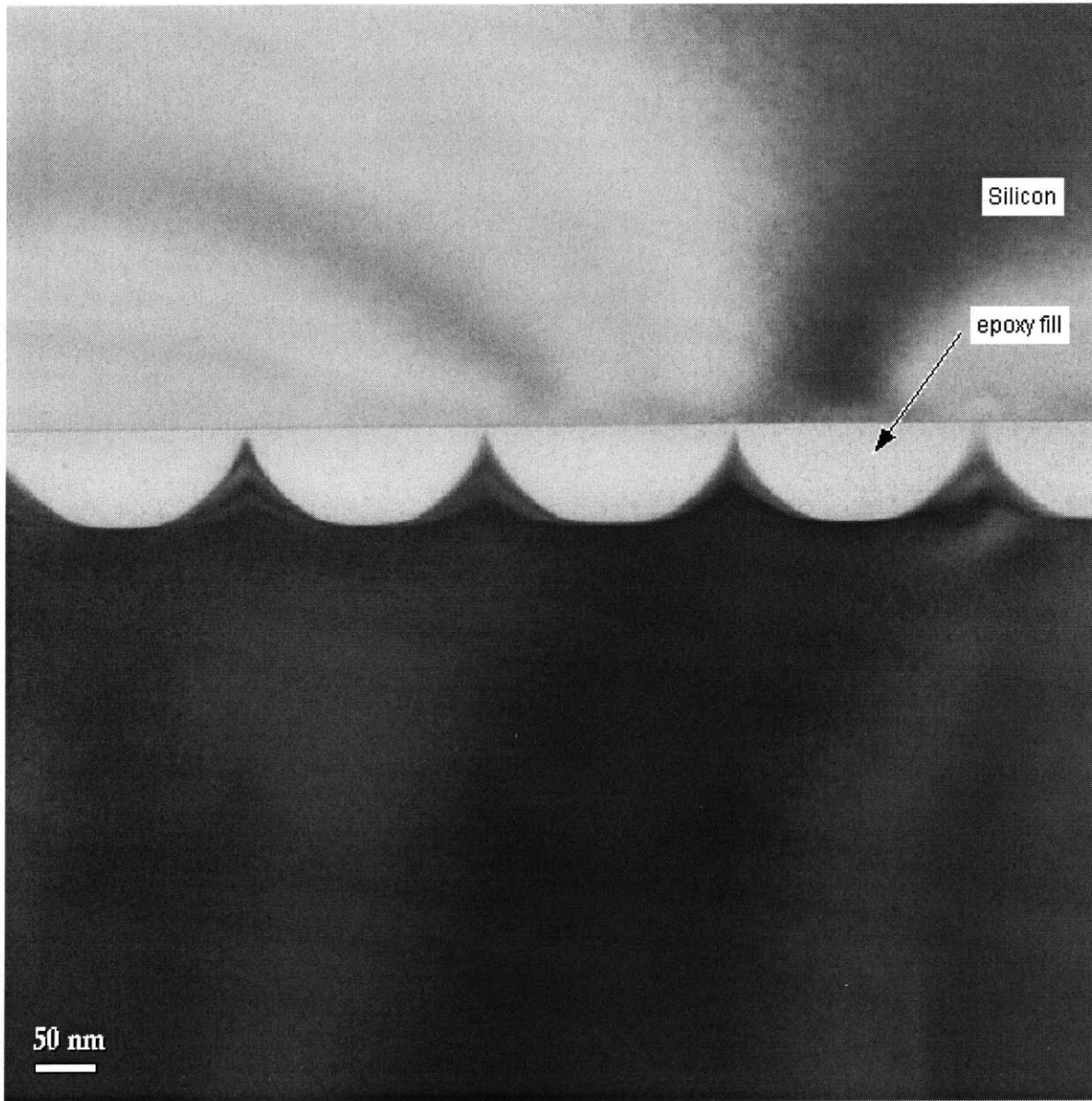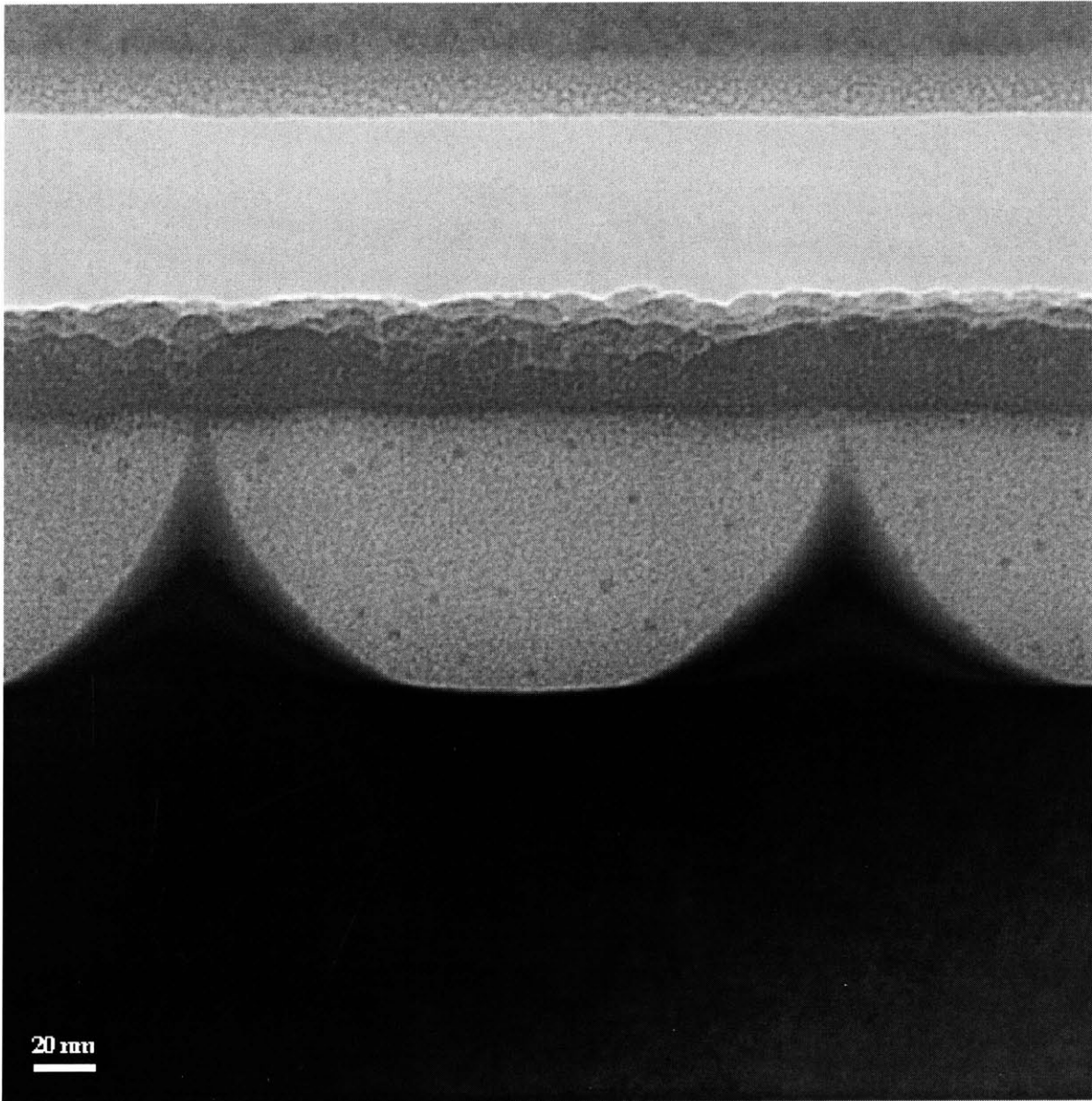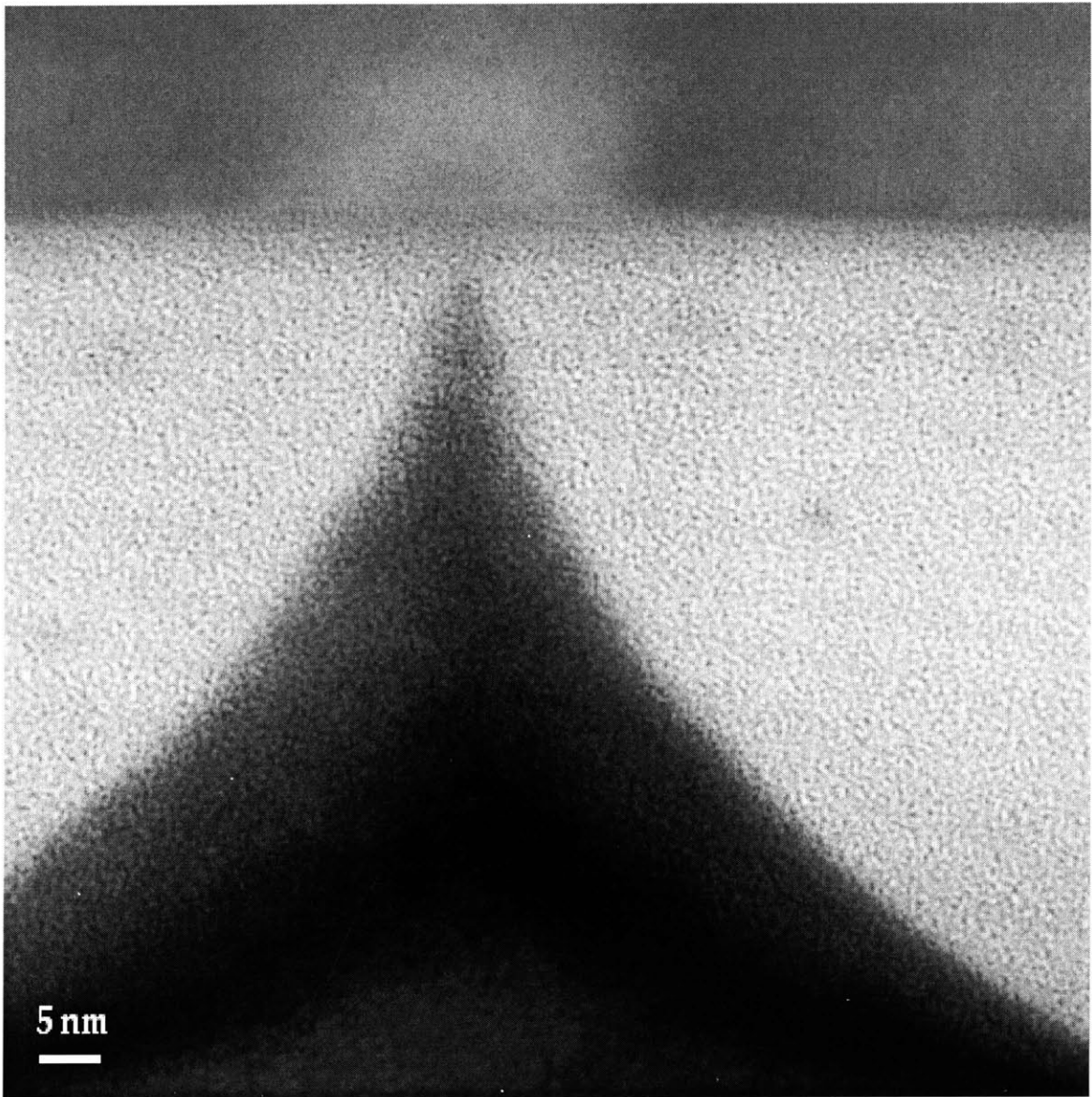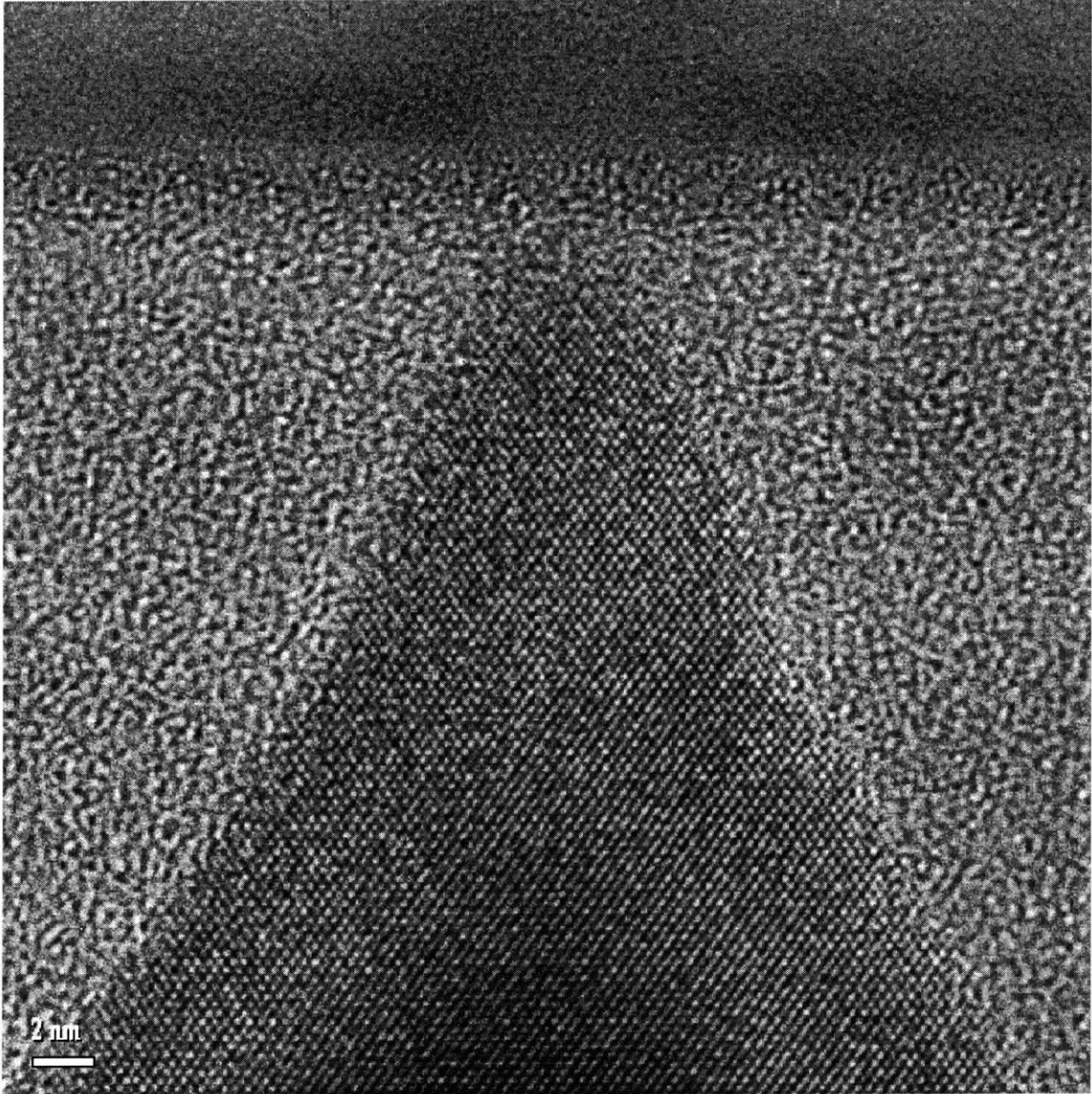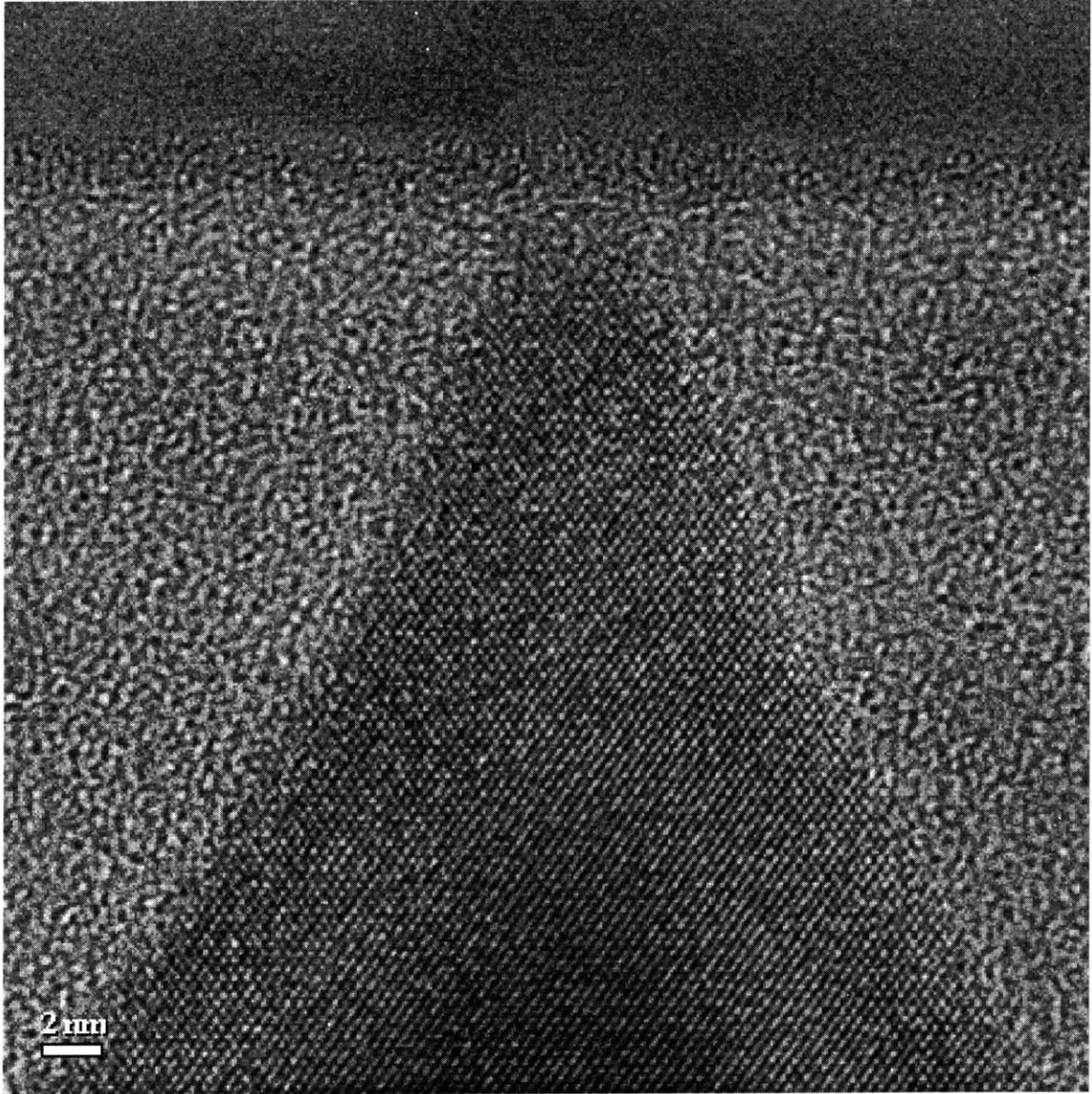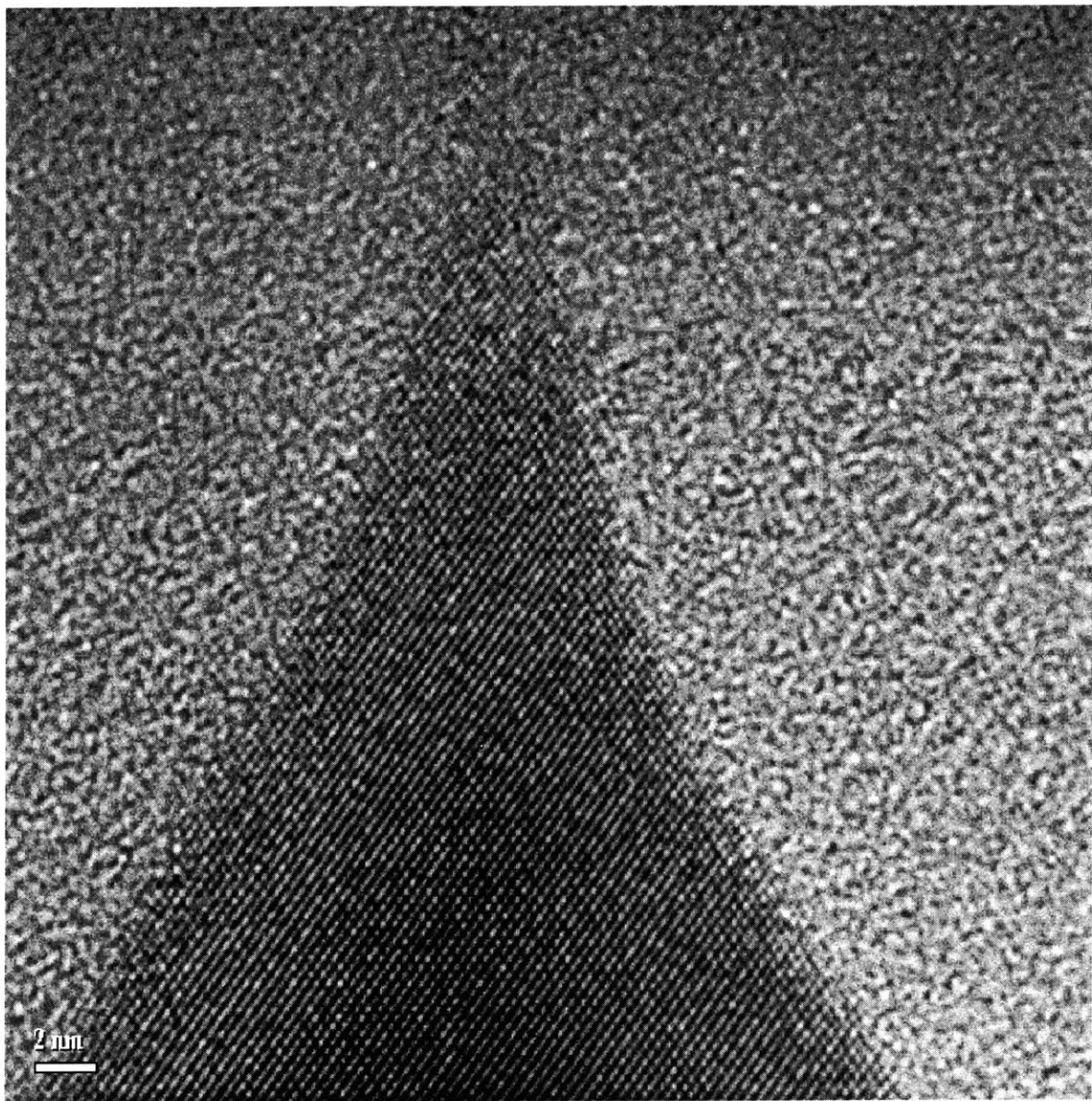
APPENDIX G: MATLAB CODE

All of the electrostatic simulation work was conducted in MATLAB version 5.x. The code was written in a modular form (creating the m-files as functions) in order to ease debugging and to allow the re-use of software. This section includes the functions and routines that were used to implement the simulations. The main routine for simulation of Spindt arrays was *maintest.m* and its silicon array counterpart *simaintest.m*. These routines did the following:

Geometry
(roc, aperture, etc.)

PDE Solver

- Create Model
- Solve

Solution
Detailed Geometry

Main Workspace

- Determine emission points
- Map Potential
- Calculate IV data

Boundary Conditions
$(V_g, V_a, \text{etc.})$
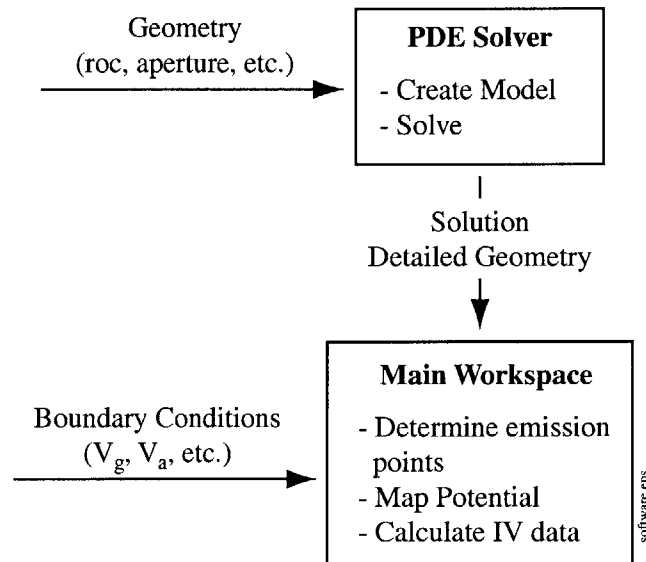
Figure 115: Schematic of MATLAB Software

All of the functionality of the software is controlled from a Main Workspace m-file that provided geometry information to the PDE solver. The model is built and solved and the information is passed back to the main workspace. The boundary conditions are incorporated, potentials are mapped and the emitted current is calculated, (this last step may be repeated for multiple boundary conditions such as sweeping the gate voltage).

A description of each routine including inputs and outputs of the function are located at the top of the routine after the function definition statement.

CONE

```
function [x,y] = cone(r,h,t,s);
%       CONE(roc, height, theta, segments) - gives the points for a cone
%       with a roc, height, base angle = theta, and s segments along the
%       tip arc.

x = zeros(s+3,1);
y = x;

%       Define the points along the y axis

x(1) = 0;               % base corner
y(1) = 0;

x(2) = 0;               % cone tip
y(2) = h;

%       Define the points along the curved tip

for i = 1:s
        ang = (90 - ((t*i)/s))*pi/180;
        x(2+i) = cos(ang)*r;
        y(2+i) = (sin(ang)*r)+(h-r);
end

%       Define the base point

l = r/cos(t*pi/180);
ht = h+l-r;             % total height if cone was a perfect triangle

x(s+3) = ht/tan(t*pi/180);
y(s+3) = 0;

return;
```

DCONEMODEL

```
function [pa,ea,ta,ua,pg,eg,tg,ug] = dconemodel(apr,roc,hei,thi,the,mr)
%        This version of the CONEMODEL routine finds and returns two soln
%        One for the potential on the gate and a grounded anode, the other
%        For the potential on the anode and a grounded gate.  A super-
%        position of these two soln will give the total soln.

xmax = apr.*3;                    %   nm
ymax = apr.*3;                    %   nm

%        Dummy geometry data
%apr = 100e-09;                              %  gate aperture
%roc = 10e-09;               % tip radius of curvature
%hei = 100e-09;                       %  gate height and oxide thickness
%thi = 30e-09;               %  gate thickness
%the = 67;                   %  cone base angle in degrees

uct = apr./3;               %  undercut of the gate

%        Start the pdetoolbox

[pde_fig,ax]=pdeinitdave;
save finum.mat ax;

%        Set to the Generic Scalar Mode

pdedave('appl_cb',1);
set(ax,'DataAspectRatio',[1 1 1]);
set(ax,'PlotBoxAspectRatio',[xmax ymax 1]);
set(ax,'XLim',[0 xmax]);
set(ax,'YLim',[0 ymax]);
set(ax,'XTickMode','auto');
set(ax,'YTickMode','auto');
set(ax,'ycolor',[1 1 1]);
set(ax,'xcolor',[1 1 1]);

%
%        Construct the model based on the geometry parameters
%        Geometry description:
%

        %  Cone
        [xc,yc] = cone(roc, hei+(thi/2), the, 30);
        pdepoly(xc',yc','cone');

        %  Gate
        [xg,yg] = gate(apr, hei, thi, xmax);
        pdepoly(xg',yg','gate');

        %  Oxide
%        [xo,yo] = oxide(apr, hei, uct, xmax);
%        pdepoly(xo, yo,'oxide');

        %  Solution Space
        pderect([0 xmax 0 ymax],'R1');

        %  Combine the above three
        set(findobj(get(pde_fig,'Children'),'Tag','PDEEval'),'String','R1-(cone+gate)');

%
% Set up the Boundary conditions:
%

        pdedave('changemode',0);

        % The entire cone will be set to ground (V=0);

        for b1 = 1:31
                pdesetbd(b1,'dir',1,'1','0');
```

```
          end
          pdesetbd(55,'dir',1,'1','0');

          % gate set to (Vg=1) for the first soln

          for b1 = 32:53
                  pdesetbd(b1,'dir',1,'1','1'); % The last '1' is the voltage
          end

          % anode set to (Va=0) for the first soln

          pdesetbd(54,'dir',1,'1','0'); % The last '0' is the voltage

          % vertical boundaries set as neuman

          for b1 = 56:58
                  pdesetbd(b1,'neu',1,'0','0');
          end

%         Mesh generation:

setuprop(pde_fig,'Hgrad',1.3);
setuprop(pde_fig,'refinemethod','regular');

          %         Initiate the Mesh and refine it 'mr' times

          pdetool('initmesh');
          for m1 = 1:mr
                  pdetool('refine');
          end;
          pdetool('jiggle');

%         Set up the Partial Differential Equation with the following
%         PDE coefficients:

pdeseteq(1,'x','0','0','1.0','0:10','0.0','0.0','[0 100]');

%
%         Solve the PDE for the gate potential model
%

pdetool('solve');

[pg,eg,tg,ug,cg] = getpetuc;

%
% Set up the Boundary conditions for the Anode model:
%

%         pdedave('changemode',0);

          % gate set to (Vg=0) for the second soln

          for b1 = 32:53
                  pdesetbd(b1,'dir',1,'1','0'); % The last '0' is the voltage
          end

          % anode set to (Va=1) for the second soln

          pdesetbd(54,'dir',1,'1','1'); % The last '1' is the voltage

%
%         Solve the PDE for the anode potential model
%

pdetool('solve');

[pa,ea,ta,ua,ca] = getpetuc;

return;
```

EMISSIONPTS

```
function [x,y,n,a] = emissionpts(r,h,t,s,d);
%       [X,Y,N,A] = EMISSIONPTS(ROC,HEIGHT,THETA,SEGMENTS,DIST) will give
%       the X and Y coordinates of the emission points from a cone emitter
%       There will be 2*S points, 1 in the center of each segment of the arc
%       (S segments in the arc) and S along the leg of the cone.  They will
%       all be a distance DIST from the surface.

[cx,cy] = cone(r,h,t,s);

% Do the points along the arc

for c1 = 1:s

        %  Determine the normal to the surface
        v = cx(c1+2)-cx(c1+1)+i*(cy(c1+2)-cy(c1+1));
        l = abs(v);
        n(c1) = angle(v).*180/pi + 90;

        %  Determine the point located 0.1 nm from the surface
        x(c1) = (cx(1+c1)+cx(2+c1))/2 + d*1e-9*cos(n(c1)*pi/180);
        y(c1) = (cy(1+c1)+cy(2+c1))/2 + d*1e-9*sin(n(c1)*pi/180);

        %  Determine the area associated with that point
        a(c1) = l*2*pi*((cx(1+c1)+cx(2+c1))/2);
end;

len = sqrt((x(1)-x(2)).^2 + (y(1)-y(2)).^2);

% Do the points along the leg

for c1 = s+1:2*s
        n(c1) = 90-t;
        x(c1) = x(c1-1)+(len.*cos(t*pi/180));
        y(c1) = y(c1-1)-(len.*sin(t*pi/180));
        a(c1) = l*2*pi*(x(c1-1)+(len.*cos(t*pi/180))/2);
end;
```

EATPT

```
function [x, y] = eatpt(pnt, p, t, Ex, Ey);

%       Determine which triangle the point lies in

        trn = tri(pnt, p, t);

%       Determine the verticies of that triangle and the values
%       the verticies;

        x = Ex(trn);
        y = Ey(trn);

return;
```

MAINTEST

```
%       Field Emitter Tip Simulation
%       David Pflug
%       5/04/99
%
%
%       Modification to the Main routine to look at the different ways of
%       explaining the differences in the tunneling current for the
%       real potential and the triangular barrier.
%
%       I will use the Fowler Nordheim Equation to calculate the current
%       through two alternative triangular barriers:
%
%       Fowler Nordheim #2 is where the barrier is a triangle going
%       through the points (0,wf) (top of the triangle) and (tp,0)
%       the classical turning point for the real potential.
%
%       Fowler Nordheim #3 is where the barrier is defined by the slope
%       of the potential at the classical turning point and extended
%       back to the surface of the material.  The workfunction is then
%       calculated from this line.

%       Calcuate the IV characteristics for a specific emitter geometry.
%       The resolution of the simulation can be scaled from fine to medium
%       to coarse.
%
%       The outputs include IV characteristics, FN plots, electron energy
%       distribution.

clear

%
%
%       For a given geometry, determine the potential profiles
%       extending out from the tip surface areas.


%---------------------------------------------------------------------
%       Parameters for the model
%---------------------------------------------------------------------

%       Geometry Parameters

apr = 100e-09;              % gate aperture (m)
roc = 4e-09;               % tip radius of curvature (m)
hei = 100e-09;             % gate height and oxide thickness (m)
thi = 30e-09;              % gate thickness (m)
the = 70;                  % cone base angle in degrees

num = 250000;              % number of emitters in the array.

%       Other Parameters

wf = 4.5;                  % Material Workfunction (eV)


%       Variable Parameters which effect soln time


ans = input('Do you want fine, medium, or coarse resolution [f,m,c]? ','s');

if strcmp(ans,'f')

        Vgstep = 2.0;      % step in the gate voltage (volts)
        dE = 0.05;         % increment in the energy
        pstep = 0.05e-9;   % step in the line from surface (meters)
        mr = 2;            % number of mesh refinements

elseif strcmp (ans,'m')
```

```
        Vgstep = 3.0;          % step in the gate voltage (volts)
        dE = 0.1;              % increment in the energy
        pstep = 0.1e-9;        % step in the line from surface (meters)
        mr = 1;                % number of mesh refinements

else

        Vgstep = 5.0;          % step in the gate voltage (volts)
        dE = 0.5;              % increment in the energy
        pstep = 0.25e-9;       % step in the line from surface (meters)
        mr = 0;                % number of mesh refinements


end;

%-----------------------------------------------------------------
%       Create the model and determine the soln.
%-----------------------------------------------------------------

ans = input('Do you want to used a saved soln? ','s');

if strcmp(ans,'n')
        [pa,ea,ta,ua,pg,eg,tg,ug] = dconemodel(apr,roc,hei,thi,the,mr);
        save soln.mat;
else
        load soln.mat;
        who
end;



%-----------------------------------------------------------------
%       Determine the emission points for the cone
%-----------------------------------------------------------------


dist = 0.001;  %       distance from the surface in nm

[x,y,normal,area] = emissionpts(roc,hei+thi/2,the,30,dist);



%-----------------------------------------------------------------
%       Determine the emission paths and potentials along those paths
%-----------------------------------------------------------------


%       Parameters

Vgmin = 10;
Vgmax = 40;
plen = 10e-9;  %       Total distance to map the potential
dx = pstep;
len = 0:dx:plen;

Vg = Vgmin:Vgstep:Vgmax;
Va = max(pg(2,:)).*1e6;        %  This will set the anode voltage
                       % to be approximately 1 V/um.

t = tg;        %       ta and tg should be the same
p = pg;        %       pa and pg should be the same

%       Determine the emission paths:

[pthx, pthy, trng, ugpth, uapth] = emisspaths2(x, y, normal, p, t, ug, ua, plen, pstep);



%-----------------------------------------------------------------
%       Create the Image Potential Ui
%-----------------------------------------------------------------
```

```
d = 0:pstep:plen;
%a = -0.2093;
%b = 0.0465;
%
%        Build the image potential 'Ui' of the form
%                a
%        Ui = -----
%              d + b
%        Where the potential will be -4.5 at 0 and reduce to -0.01 at
%        d = 2;

Ui = imagepot(d,wf);


%------------------------------------------------------------------
%        Build the Supply Function... this will be applicable for
%        all of the models...
%------------------------------------------------------------------

%        Parameters

kb = 8.62e-5;   %  eV/K
Temp = 300;     %  K
s = 2;          %  electron spin
e = 1;          %  eV
hbar = 6.6e-16;         %  eV*s
m = 5.69e-16;   %  eV*s^2/cm^2
h = hbar.*2.*pi;        %  eV*s

%        Energy Range of interest

E = -10:dE:5;
Ef = 0;

%        2D Density of States from P.H. Cutler et al, 'Tunneling theory
%        and vacuum microelectronics, IVMC 1989, Bath, England.

N1 = 1 + exp((Ef-E)./(kb.*Temp));
N2 = (2.*s+1).*2.*pi.*m.*kb.*Temp./(h^3);


N = N2.*log(N1);


%------------------------------------------------------------------
%        Other convienent parameters
%------------------------------------------------------------------


sites = size(x,2);
elevel = size(E,2);


%------------------------------------------------------------------
%        Step throught the gate voltages for IV relationship
%------------------------------------------------------------------

for c1 = 1:size(Vg,2);

        % Build the superposition of the potential
        % and the electric field

        upth = Vg(c1).*ugpth+Va.*uapth;
        u = Vg(c1).*ug+Va.*ua;

        [Ex, Ey] = pdegrad(p, t, u);


        %------------------------------------------------------------------
        %        Determine the Surface E-field using the previously found
        %        triangles for the initial point
        %------------------------------------------------------------------
```

```matlab
for c2 = 1:sites
        Esurfx(c2) = Ex(trng(c2,1));
        Esurfy(c2) = Ey(trng(c2,1));
        Emag(c2) = abs(Esurfx(c2)+i.*Esurfy(c2));
end;


%----------------------------------------------------------------------
%       Create the triangular barrier 'fowpot' which is a
%       linear extension of the surface e-field.
%----------------------------------------------------------------------


for c2 = 1:sites
        fowpot(c2,:) = wf - Emag(c2).*d;
end;


%----------------------------------------------------------------------
%       Superimpose the image potential on the upth and
%       create a barrier
%----------------------------------------------------------------------


for c2 = 1:sites
        uipth(c2,:) = wf-upth(c2,:)+Ui;
end


%----------------------------------------------------------------------
%       Determine the turning points for the Fowler Nordheim
%       and the real potentials
%----------------------------------------------------------------------


[tpr, tplr] = min(abs(uipth(:,[3:size(uipth,2)])'));
[tpf, tplf] = min(abs(fowpot(:,[3:size(fowpot,2)])'));


%----------------------------------------------------------------------
%       Determine the current associated with this gate voltage
%----------------------------------------------------------------------


for c2 = 1:sites

        tic;
        fprintf('Working on Voltage %i in site %i',Vg(c1), c2);

        %----------------------------------------------------------
        %       Fowler Nordheim tunneling from standard
        %       triangular barrier
        %----------------------------------------------------------

        Jf(c2) = fowler([Emag(c2) 0],wf);            % A/m^2
        If(c2) = Jf(c2).*area(c2);


        %----------------------------------------------------------
        %       Fowler Nordheim tunneling from triangular
        %       barrier #2 (connect turning point and surface)
        %----------------------------------------------------------

        %       Determine the Emag from the slope of the line from
        %       the real turning point to the surface

        Emag2(c2) = wf./d(tplr(c2));
        wf2 = wf;

        Jf2(c2) = fowler([Emag2(c2) 0],wf2);          % A/m^2
```

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```
If2(c2) = Jf2(c2).*area(c2);


%------------------------------------------------------------------
%       Fowler Nordheim tunneling from triangular
%       barrier #3 (connect turning point and surface)
%------------------------------------------------------------------

%       Determine the slope of the real potential at the
%       real turning point

slope = diff(uipth(c2,:));
Emag3(c2) = -slope(tplr(c2))./dx;
wf3 = d(tplr(c2)).*Emag3(c2);

Jf3(c2) = fowler([Emag3(c2) 0],wf3);          % A/m^2
If3(c2) = Jf3(c2).*area(c2);


%------------------------------------------------------------------
%       WKB with surface e-field and no image potential
%       For comparison to regular FN equation
%------------------------------------------------------------------

%  Tunneling Probability

Tfni(c2,:) = wkb(E, fowpot(c2,:), m, dx*100);

%  Normal Energy Distribution of EMITTED Electrons

Pfni(c2,:) = Tfni(c2,:).*N;   %  e-/(cm^2*s*eV)
PAfni(c2,:) = Pfni(c2,:).*area(c2).*10000;
               %  the 10000 is to change the P to m^2
               %  e-/(s*eV)

%  Integrate over all the energy levels to get the
%  total current for this boundary condition

Ifni(c2,:) = 1.6e-19.*trapz(PAfni(c2,:)).*dE;

%------------------------------------------------------------------
%       WKB with surface e-field with image potential
%------------------------------------------------------------------

%  Tunneling Probability

Tfi(c2,:) = wkb(E, fowpot(c2,:)+Ui, m, dx*100);

%  Normal Energy Distribution of EMITTED Electrons

Pfi(c2,:) = Tfi(c2,:).*N;      %  e-/(cm^2*s*eV)
PAfi(c2,:) = Pfi(c2,:).*area(c2).*10000;
               %  the 10000 is to change the P to m^2
               %  e-/(s*eV)

%  Integrate over all the energy levels to get the
%  total current for this boundary condition

Ifi(c2,:) = 1.6e-19.*trapz(PAfi(c2,:)).*dE;

%------------------------------------------------------------------
%       WKB with real potential soln and image potential
%------------------------------------------------------------------

%  Tunneling Probability

Twi(c2,:) = wkb(E, uipth(c2,:), m, dx*100);

%  Normal Energy Distribution of EMITTED Electrons

Pwi(c2,:) = Twi(c2,:).*N;      %  e-/(cm^2*s*eV)
```

```matlab
            PAwi(c2,:) = Pwi(c2,:).*area(c2).*10000;
                        %  the 10000 is to change the P to m^2
                        %  e-/(s*eV)

            %  Integrate over all the energy levels to get the
            %  total current for this boundary condition

            Iwi(c2,:) = 1.6e-19.*trapz(PAwi(c2,:)).*dE;


            %-------------------------------------------------------------
            %         Calculate time left in simulation
            %-------------------------------------------------------------

            ti = toc;
            time = ((size(Vg,2)-c1)*sites+(sites-c2))*ti/60;
            fprintf(', with %3.1f minutes left\n',time);


    end;


    %------------------------------------------------------------------------
    %         Determine the total currents for the specific boundary
    %         boundary contition (Vg);
    %------------------------------------------------------------------------

    IFN(c1) = num .* sum (If);
    IWKBtri(c1) = num .* sum (Ifni);
    IWKBimg(c1) = num .* sum (Ifi);
    IWKBreal(c1) = num .* sum (Iwi);

    IFN2(c1) = num .* sum (If2);
    IFN3(c1) = num .* sum (If3);


    %------------------------------------------------------------------------
    %         Determine the Energy Distribution of electrons emitted
    %         for each boundary condition (Vg);
    %------------------------------------------------------------------------

    EDWKBtri(c1,:) = sum (PAfni);
    EDWKBimg(c1,:) = sum (PAfi);
    EDWKBreal(c1,:) = sum (PAwi);

end;

%------------------------------------------------------------------------
%         Coefficient Analysis
%------------------------------------------------------------------------

[al1, be1, af1, bf1] = fncoeff(Vg, IFN, wf);
[al2, be2, af2, bf2] = fncoeff(Vg, IWKBtri, wf);
[al3, be3, af3, bf3] = fncoeff(Vg, IWKBimg, wf);
[al4, be4, af4, bf4] = fncoeff(Vg, IWKBreal, wf);

fprintf(1,'\talpha\t\tbeta\t\tafn\t\tbfn\n');
fprintf(1,'FN surf\t%6.2e\t%6.2e\t%6.2e\t%6.2e\n',al1,be1,af1,bf1);
fprintf(1,'WKB tri\t%6.2e\t%6.2e\t%6.2e\t%6.2e\n',al2,be2,af2,bf2);
fprintf(1,'WKB img\t%6.2e\t%6.2e\t%6.2e\t%6.2e\n',al3,be3,af3,bf3);
fprintf(1,'WKB rel\t%6.2e\t%6.2e\t%6.2e\t%6.2e\n',al4,be4,af4,bf4);
save solved.mat;


%------------------------------------------------------------------------
%         Plot Results
%------------------------------------------------------------------------

f1 = figure;

subplot(2,2,1);
plot(Vg,IFN);
title('IV relationship for FN Equation')
xlabel('Gate Voltage (V)');
ylabel('Anode Current (A)');
```

```
subplot(2,2,2);
plot(Vg,IWKBtri);
title('IV relationship for WKB Triangular Barrier')
xlabel('Gate Voltage (V)');
ylabel('Anode Current (A)');

subplot(2,2,3);
plot(Vg,IWKBimg);

title('IV relationship for WKB Triangular Barrier w/ Image Potential')
xlabel('Gate Voltage (V)');
ylabel('Anode Current (A)');

subplot(2,2,4);
plot(Vg,IWKBreal);
title('IV relationship for WKB with Real Potential and Image')
xlabel('Gate Voltage (V)');
ylabel('Anode Current (A)');cyclines;

forplot(f1,8);
fullpage(f1,0.75,'landscape');
footnote(f1,['apr = 'num2str(apr.*1e9) ' nm, roc = ' num2str(roc.*1e9) ' nm']);
print f1.ps

f2 = figure;

fnplot(Vg,IFN);
hold on;
fnplot(Vg,IWKBtri);
fnplot(Vg,IWKBimg);
fnplot(Vg,IWKBreal);
cyclines;

title('Fowler Nordheim for Different Tunneling Methods')
forplot(f1,12);

legend ('FN Equation', 'WKB tri barrier', 'WKB tri w/ image', 'WKB with real and image');
fullpage(f2,0.75,'landscape');
footnote(f2,['apr = 'num2str(apr.*1e9) ' nm, roc = ' num2str(roc.*1e9) ' nm']);
print f2.ps

f3 = figure;
hold on;

plot(Vg,IFN);
plot(Vg,IWKBtri);
plot(Vg,IWKBimg);
plot(Vg,IWKBreal);

title('IV relationship for Different Tunneling')
xlabel('Gate Voltage (V)');
ylabel('Anode Current (A)');

forplot(f3,12);
fullpage(f3,0.75,'landscape');
axis ([Vgmin Vgmax 0 5e-9]);
cyclines
legend ('FN Equation', 'WKB tri barrier', 'WKB tri w/ image', 'WKB with real and image',2);
footnote(f3,['apr = 'num2str(apr.*1e9) ' nm, roc = ' num2str(roc.*1e9) ' nm']);
print f3.ps


%-------------------------------------------------------------------
%       Plot Normalized Energy Distribution of Electrons
%       for a give Vg
%-------------------------------------------------------------------

V = 20;          % this is the gate voltage to use

[q,c1] = min(abs(Vg-V));
```

```
f4 = figure;
hold on;

plot(E,EDWKBtri(c1,:)./max(EDWKBtri(c1,:)));
plot(E,EDWKBimg(c1,:)./max(EDWKBimg(c1,:)));
plot(E,EDWKBreal(c1,:)./max(EDWKBreal(c1,:)));

title(['Energy Distribution of Emitter electrons for Vg = ' num2str(20)]);
xlabel('Energy Level (eV)');
ylabel('Normalized electrons');
axis ([-2 1 0 1]);

forplot(f4,12);
fullpage(f4,0.75,'landscape');
cyclines
legend ('WKB tri barrier', 'WKB tri w/ image', 'WKB with real and image',2);
footnote(f4,['apr = 'num2str(apr.*1e9) ' nm, roc = ' num2str(roc.*1e9) ' nm']);
print f4.ps


%-------------------------------------------------------------------
%       Plot Normalized Energy Distribution of Electrons
%       for all Vg
%-------------------------------------------------------------------

[meshE,meshV] = meshgrid(E,Vg);

%       For Standard Triangular Barrier

for c1 = 1:size(EDWKBtri,1)
        norm(c1,:) = EDWKBtri(c1,:)./max(EDWKBtri(c1,:));
end

f5 = figure;
contour(meshE,meshV,norm)
axis ([-2 2 5 30]);
title('Energy Distribution for Different Voltages for Triangular Barrier');
xlabel('Energy (eV)')
ylabel('Gate Voltage');
forplot(f5,12);
fullpage(f5,0.75,'landscape');
footnote(f5,['apr = 'num2str(apr.*1e9) ' nm, roc = ' num2str(roc.*1e9) ' nm']);
print f5.ps

%       For Triangular barrier with Image potential

for c1 = 1:size(EDWKBimg,1)
        norm(c1,:) = EDWKBimg(c1,:)./max(EDWKBimg(c1,:));
end

f6 = figure;
contour(meshE,meshV,norm)
axis ([-2 2 5 30]);
title('Energy Distribution for Different Voltages for Triangular with Image');
xlabel('Energy (eV)')
ylabel('Gate Voltage');
forplot(f6,12);
fullpage(f6,0.75,'landscape');
footnote(f6,['apr = 'num2str(apr.*1e9) ' nm, roc = ' num2str(roc.*1e9) ' nm']);
print f6.ps

%       For Real Potential with image potential

for c1 = 1:size(EDWKBreal,1)
        norm(c1,:) = EDWKBreal(c1,:)./max(EDWKBreal(c1,:));
end

f7 = figure;
contour(meshE,meshV,norm)
axis ([-2 2 5 30]);
title('Energy Distribution for Different Voltages for Real Potential');
```

```
xlabel('Energy (eV)')
ylabel('Gate Voltage');
forplot(f7,12);
fullpage(f7,0.75,'landscape');
footnote(f7,['apr = 'num2str(apr.*1e9) ' nm, roc = ' num2str(roc.*1e9) ' nm']);
print f7.ps
```

PDEINITDAVE

```
function [hfig,hax] = pdeinitdave
%PDEINIT Start PDETOOL from scripts.

%    Magnus Ringh 7-01-94, MR 11-07-94.
%    Copyright (c) 1994-97 by The MathWorks, Inc.
%    $Revision: 1.5 $  $Date: 1997/05/14 22:12:54 $

pde_fig=findobj(allchild(0),'flat','Tag','PDETool');
if ~isempty(pde_fig),
  pdedave('new');
else
  pdedave;
end
pde_fig=findobj(allchild(0),'flat','Tag','PDETool');
ax = findobj(allchild(pde_fig),'flat','Tag','PDEAxes');
set(pde_fig,'CurrentAxes',ax)
no = nargout;
if no>0
  hfig = pde_fig;
end
if no>1
  hax = ax;
end
```

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