Vertically Integrated Transistors for Field Emission Applications

by

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Abstract

Field emission devices have demonstrated several research and commercial applications in the areas of flat panel displays, microwave power devices, imaging sensors and electron sources. Recent work has shown the feasibility of using integrated MOSFETs to control and enhance field emission stability and operating characteristics. This research effort investigates the integration of vertical MOS transistors with field emitter arrays as a means to enhance field emission device capabilities and range of applications. Vertical MOSFET device modeling was performed using MEDICI, a commercially available electrostatic simulator. In addition, process modeling was conducted using SUPREM to optimize design and layout sequencing for device fabrication. Working devices were fabricated and tested in the Integrated Circuits Laboratory within the Microsystems and Technology Laboratory at MIT. Techniques to achieve high-density field emitter arrays necessary for integrated VMOS / FEA devices were also investigated. This study determined that it is feasible to integrate and control field emitter arrays with vertical MOSFET devices.

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Title: Associate Professor of Electrical Engineering and Computer Science

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"break a piece of wood and I am there, lift up a stone and you will find me"

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Chapter 1 - Introduction

1.1. Background

With recent advancements in device fabrication technology and portable electronic devices, there has been a growing demand for compact, energy-efficient information displays. For this reason there has been a large effort in the past several years to develop and improve upon cold cathode field emission sources for flat panel display applications. One of the most promising applications has been to use field emitter arrays to create thin, lightweight cathodoluminescent displays with high luminous efficiency and low power consumption. In a typical cathode ray tube (CRT) display an electron beam is electronically rastered across a large vacuum envelope to energetically excite phosphors on the display screen. Spatially modulating the electron beam density causes pixels on the phosphor screen to luminesce thereby creating the desired image [1]. CRT's have very high brightness and luminous efficiency [2] however the large vacuum tube required for the display precludes it from being implemented in portable electronic devices.

The liquid crystal display (LCD) is currently the dominant display technology for portable display applications [3]. Active matrix LCD's utilize a matrix-addressable set of cells filled with liquid crystal to create a display image. A liquid crystal material is sandwiched between two transparent conducting electrodes and light polarizing elements. By applying a voltage across an individual cell, the alignment of the liquid crystal molecules can be altered to increase or reduce the light transmission through the cell. In this manner an image can be formed by selectively addressing the desired cells [1,4]. It is essentially a spatial light modulator. While this addressing technique is very powerful and makes a very compact display possible, the lower brightness and decreased efficiency due to low transmission of the liquid crystal are the main drawbacks to liquid crystal displays.

The field emission display concept combines the benefits of both the CRT (cathodoluminescence, high luminous efficiency, and brightness) and LCD (lightweight, compact, and matrix-addressable) technologies. The display utilizes matrix-addressable arrays of field emitters to generate vertically traveling beams of electrons (Figure 1). A typical FED sub-pixel consists of a field emitter array which is proximity focused onto a red, green or blue phosphor

element. The FEAs are independently addressed and generate separate electron beams for each sub-pixel element. By using a two dimensional array of FEAs, images can be formed on a phosphor screen with the high brightness and luminous efficiency characteristics of a CRT. A very compact, lightweight and high brightness display can be realized by using a matrix-addressing scheme for the field emitter arrays [5,6]. The field emission display described above is essentially a very thin display based on the CRT concept. Matrix addressable field emission displays with low voltage operation have been fabricated and demonstrated for their feasibility as a display technology [1,3,5,6,7].

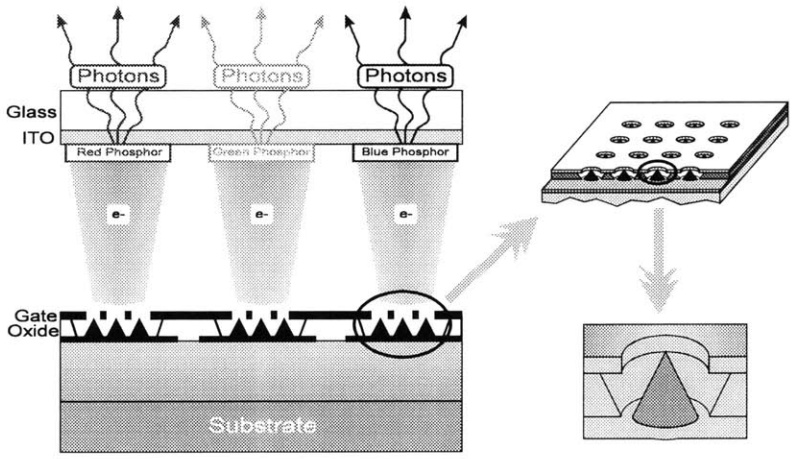


Figure 1. Field Emission Display concept

Individually arrays, each containing several hundred field emitter devices, are addressed to generate vertically traveling beams of electron. The electron beams are accelerated towards a phosphor coated electrode and generate red, green, or blue light upon striking the respective phosphor.

1.2. Motivation

One of the main difficulties in creating viable field emission displays is the need to use large switching voltages in order to generate electron beams from the field emitter tips. The first field emitter arrays of Spindt cones fabricated at SRI had diameters of 1 μm operated in the range of 100 - 150 V [8]. To turn the field emitter arrays on or off would require switching these large voltages across each arrays' respective gate electrode. In addition to concerns about oxide breakdown and device stability, the driver circuitry required to operate at these high voltages would be prohibitively complex and financially non-viable. With advances in fabrication technology and lithographic techniques field emission devices smaller than 200 nm with operating voltages as low as 15-20 V have been realized

[9,10]. However even at these low voltages, power consumption of driver circuits for a 1,000 x 1,000 pixel array would be rather large.

It is possible to decrease the operating voltage of FEAs by an order of magnitude, to only 2-3 volts. This can be done by tying a transistor structure in series with an array of field emitting devices. In this arrangement the field emitter gate electrode can be held at a constant (necessarily higher) voltage while the MOSFET device is used as a switch to open or close a conduction path for electrons. When the MOSFET is turned on, electrons can flow to the array and be subsequently emitted from the tips through the field emission process. By reducing the gate voltage of the MOSFET below the device threshold, the conduction channel is removed and the field emitter tips do not emit electrons. In this manner the field emission process can be controlled through the use of a low-voltage, CMOS-compatible MOSFET process.

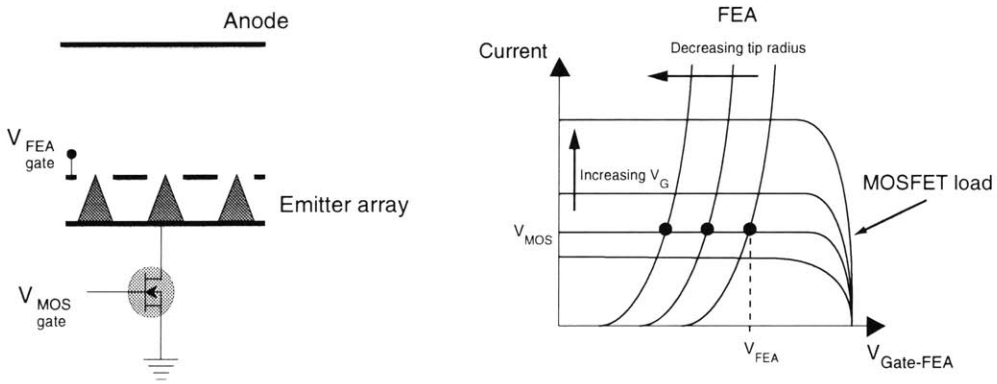


Figure 2. MOSFET / FEA concept

Integrated devices would allow low voltage, matrix-addressable switching capability for each field emitter array. The MOSFET device would act as a voltage controlled current source allowing stable device operation at a given load voltage (V_{MOS}) even with variations in emitter tip radius.

Another important issue in field emitter operation is that the emission current is a highly sensitive function of the surface potential barrier. The shape of the potential barrier is determined by several factors including the material work function, surface states, tip geometry and applied voltage on the gate electrode. Due to the small device geometries, small fluctuations in the FEA gate voltage can cause significant changes in the emitted current resulting

in non-stable operation. In addition, non-uniformity of field emitter tip geometry due to variability in the fabrication process can also result in large differences in output current characteristics and noisy device operation.

These issues can be alleviated also with the integration of a MOSFET / FEA device. Conceptually, the MOSFET acts as a voltage controlled current source (VCCS) in series with the field emitter devices. The VCCS in series with the FEA allows the emission current to be independent of small variations of barrier height or width (i.e. variance in work function, tip radius, or gate voltage).

The goal of integrating the two devices is to control the FEA output current characteristics through the use of a series VCCS provided by the MOSFET. It also has the added benefit of reducing the switching voltage and dynamic power consumed by the driver circuitry. Previous work has demonstrated the feasibility of implementing a MOSFET / FEA device structure [11]. It has been shown that integrated MOSFET / FEA devices not only provide more stable operation but also that low switching voltages and even MOSFET logic operations can be realized [12,13]. The goal of this work is to investigate using a vertical MOSFET structure for integration with a field emitter array.

1.3. Problem Statement

The output current of field emission devices is exponentially dependent on the electric field at the device tip. Slight variations (~1-5 nm) in device geometry or gate voltage can significantly alter emission current and device stability. In addition power consumption in electronic devices is quadratically dependent on the voltage swing used to switch the device on or off. For field emitter devices, large gate voltages (50-100V) are typically needed to initiate the field emission process and generate electron beams of sufficient current density for display applications. By implementing an integrated MOSFET / FEA structure to create a voltage controlled current source in series with the field emitter devices, increased stability in device performance and low voltage switching can be realized [11-13].

1.4. Objectives and Approach

It is the objective of this work to analyze an integrated MOSFET / FEA device structure and to create a vertical transistor to be integrated with a field emitter array. A vertical structure is desirable so that each addressable field

emitter array can be controlled independently without sacrificing device density or display resolution capability. Electron conduction in the field emission and transistor processes will also be examined to determine the requirements needed to implement the integrated device.

1.5. Thesis Outline

The second chapter in this thesis will present a background on electron emission from both metal and semiconductor materials, while electron transport and analytical models of MOSFET devices are derived in Chapter 3. In Chapter 4 the fabrication process used to create the vertical transistor structures is outlined and compared to process simulation results. Device simulation and experimental results are shown in Chapter 5. Integration of the vertical MOSFET structures and field emitter arrays are explored in Chapter 6, conclusions are presented Chapter 7.

Chapter 2 - Field Emission Theory

2.1. Electron Emission from a Surface

Field emission can be defined as the emission of electrons from one condensed phase to another phase through the action of an external electric field. Field emission is fundamentally a quantum mechanical phenomenon wherein an applied electric field allows electrons to tunnel through the potential barrier at a material interface. The field causes a deformation in the surface potential which, if large enough, allows electrons to have an appreciable tunneling probability (Figure 3). This phenomenon is fundamentally different from thermionic or photoemission in which sufficient energy to overcome a material's work function is directly transferred (through lattice vibrations or photons) to an electron.

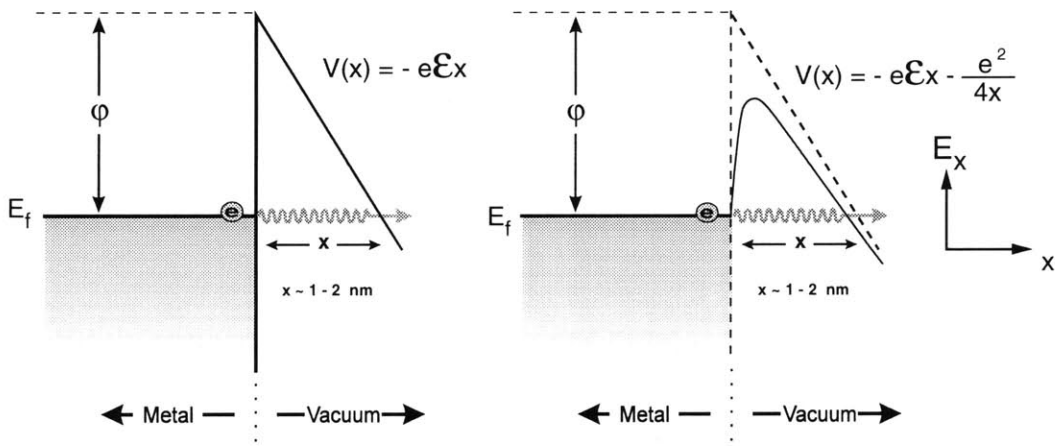


Figure 3. Field Emission through Electron Tunneling

Potential barrier without (a) and with (b) image charge effects

In the case of thermionic emission, the emitting material is heated such that there is an increase in the proportion of electrons that have sufficient energy to surmount the surface barrier (work funtion). In photoemission, energy is transferred to an electron by an incident photon and the electron is ejected from the material (Figure 4).

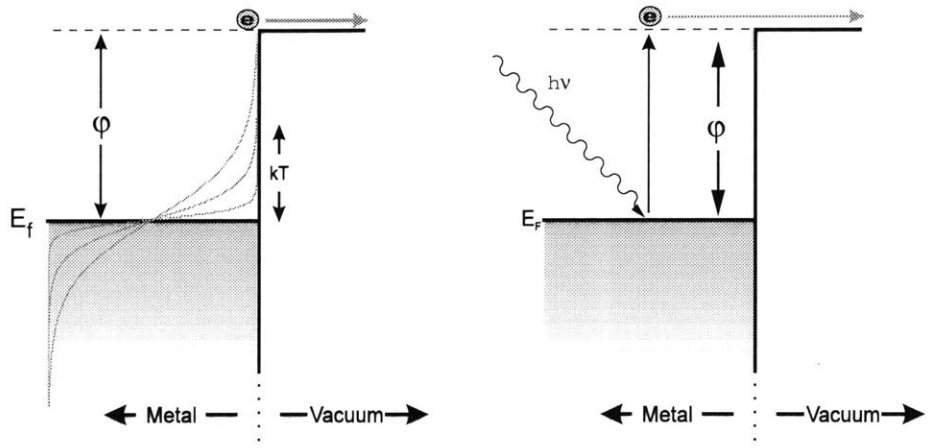


Figure 4. Thermionic and Photo Emission of Electrons

In the case of field emission, the electron is transmitted *through* the potential barrier while in the thermionic or photoemission, the electron is given enough energy to *go over* the potential barrier.

2.2. Fowler-Nordheim Tunneling

Much work has been done to describe the underlying physical phenomena of field emission. As early as the 1920's [14]. R.H. Fowler and L.W. Nordheim developed a theoretical model of field emission which consists of quantum mechanical tunneling through a potential barrier. In their derivation they directly solved Schrodinger equation for a one-dimensional potential barrier using Bessel and Hankel wavefunction solutions. A simplification of the Fowler-Nordheim result based on a WKB approximation was carried out by Good and Mueller [19] and is outlined below. The F-N tunneling current is based on emission from a metal surface where the electrons are assumed to form a free electron gas within the surface and obey Fermi-Dirac statistics. The emitted current density is given by

$$J(E_x, \mathcal{E}) = e\int_{-\infty}^{\infty} N(E_x)T(E_x, \mathcal{E})dE_x \tag{1}$$

where E_x is the electron energy normal to the surface, $N(E_x)$ is an electron supply function, $T(E_x, \mathcal{E})$ is the transmission probability through the potential barrier, and $\mathcal{E}$ is the surface electrostatic field [15]. If the material temperature is relatively low (corresponding to a sharply defined Fermi-Dirac distribution), most of the emitted

electrons originate from a small energy interval around the Fermi level of the metal [16]. The supply function is found by combining the electronic density of states and carrier distribution normal to the surface (x-direction) to yield

$$N(E_x) = \frac{4\pi m k_b T}{\hbar^3} \ln\left(1 + \exp\left(\frac{E_f - E_x}{k_b T}\right)\right) \tag{2}$$

By using the WKB approximation for the transmission through the potential barrier shown in Figure 3b the transmission coefficient is given by [17]

$$T_{WKB}(E_x, \mathcal{E}) = \exp\left(-\int_{x_1}^{x_2} \sqrt{\frac{8m(V(x) - E)}{\hbar^2}} dx\right) \tag{3}$$

where the potential due to the applied electric field $\mathcal{E}$, and x_1,x_2 are the classical turning points in the potential barrier. The image charge (caused by the emitted electrons above the metal surface) is given by

$$V(x) = -e\mathcal{E}x - \frac{e^2}{4x} \tag{4}$$

where the zero for energy is set equal to the vacuum level (Figure 3). Without the image charge correction term, the transmission probability through a triangular potential barrier is readily solved [15] to be

$$T_{WKB}(E_x) = \exp\left(-\frac{4}{3e\mathcal{E}}\sqrt{\frac{2m}{\hbar^2}}(\varphi - E_x - E_F)^{3/2}\right) \tag{5}$$

The exponential dependence that is characteristic of tunneling phenomena has been well verified in field emission experiments [18].

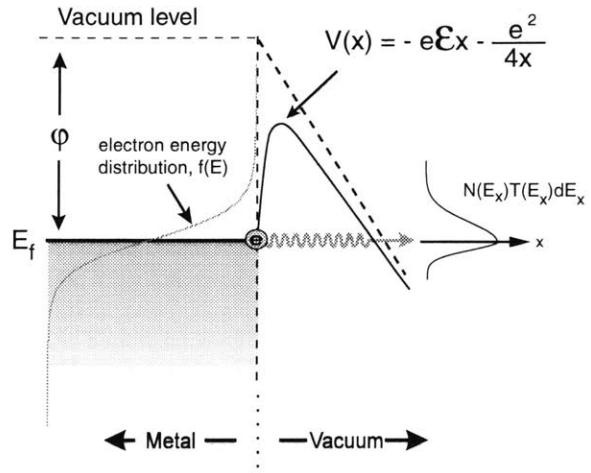


Figure 5. Energy diagram for Field Emission from a Metal Surface

Electron energy perpendicular to the metal surface, E_x, is dependent on the Fermi-Dirac distribution f(E). Emitted electron energy distribution is also shown as a function of energy by $N(E_x)T(E_x,\mathcal{E})dE_x$.

Through the use of elliptical integrals [19] it is possible to solve for the transmission coefficient with the image charge correction term by introducing a parameter *y*, to yield

$$T_{WKB}(E_x,\mathcal{E}) = \exp\left(-\frac{4\sqrt{2m|E_x|^3}}{3\hbar e\mathcal{E}}v(y)\right) \qquad \text{with} \qquad y = \frac{\sqrt{e^3\mathcal{E}}}{|E_x|} \tag{6}$$

where *v(y)* is essentially a correction term to the WKB approximation given by

$$v(y) = \frac{1}{\sqrt{2}}\sqrt{1+\sqrt{1-y^2}}\left[L(k)-\left(1-\sqrt{1-y^2}\right)K(k)\right] \qquad \text{with} \qquad k^2 = \frac{2\sqrt{1-y^2}}{1+\sqrt{1-y^2}}$$

L(k) and K(k) are complete elliptical integrals of the first and second kinds

$$L(k) = \int_0^{\pi/2}\sqrt{1-k^2\sin^2\theta}\,d\theta \qquad K(k) = \int_0^{\pi/2}\frac{d\theta}{\sqrt{1-k^2\sin^2\theta}}$$

The above solutions for $N(E_x)$ and $T_{WKB}(E_x, \mathcal{E})$ can then be combined to give the current density

$$J(E_x, \mathcal{E})dE_x = N(E_x)T(E_x, \mathcal{E}) = \frac{4\pi m k_b T}{\hbar^3} \ln\left(1 + \exp\left(\frac{E_f - E_x}{k_b T}\right)\right) e^{-\frac{4\sqrt{2m|E_x|^3}}{3\hbar e\mathcal{E}} v(y)} \tag{7}$$

By assuming that the electrons are emitted from an energy near E_f, the exponential factor in $T_{WKB}(E_x, \mathcal{E})$ can be approximated with a Taylor series expansion about $E_x = E_f$

$$-\frac{4\sqrt{2m|E_x|^3}}{3\hbar e\mathcal{E}} v(y) \approx -\frac{4\sqrt{2m|\varphi|^3}}{3\hbar e\mathcal{E}} v(y) + 2\sqrt{2m\varphi}\frac{E_x - E_f}{he\mathcal{E}} t(y)$$

with

$$t(y) = v(y) - \frac{2}{3} y \frac{dv(y)}{dy}$$

A further approximation in the low temperature limit can be made for the supply function $N(E_x)$ to estimate that

$$k_b T \ln\left(1 + \exp\left(\frac{E_f - E_x}{k_b T}\right)\right) \approx 0 \qquad \text{when} \qquad E_x > E_f \tag{8}$$

and

$$k_b T \ln\left(1 + \exp\left(\frac{E_f - E_x}{k_b T}\right)\right) \approx E_f - E_x \qquad \text{when} \qquad E_x < E_f \tag{9}$$

With the above assumptions, for $E_x < E_f$, the current density can then be expressed as

$$J(E_x, \mathcal{E})\, dE_x = \frac{4\pi m k_b T}{\hbar^3} \exp\left(-\frac{4\sqrt{2m|\varphi|^3}}{3\hbar e\varepsilon} v(y) + 2\sqrt{2m\varphi}\frac{E_x - E_f}{he\varepsilon} t(y)\right)(E_f - E_x)$$

Integrating the above expression over all possible energies from E_c to E_f it is possible to derive the Fowler-Nordheim expression for current density under cold field emission conditions as

$$J(\mathcal{E},\varphi) = \frac{e^3 \cdot \mathcal{E}^2}{8 \cdot \pi \cdot h \cdot \varphi \cdot t^2(y)} \cdot \exp\left(\frac{8 \cdot \pi \cdot (2 \cdot m)^{1/2} \cdot \varphi^{3/2}}{3 \cdot h \cdot e \cdot \mathcal{E}} \cdot v(y) \right) \tag{10}$$

where e is the electronic charge, h is Planck's constant and $t^2(y)$ and $v(y)$ are the functions of the aforementioned Nordheim elliptical integrals which take into account image charge effects. The integration does assume that the conduction band energy E_c is far below the Fermi energy and can therefore be approximated by -∞ in the lower limit of the integral.

Their values are well approximated by $t^2(y) = 1.1$ and $v(y) = 0.95 - y^2$ [20]. As compiled by Spindt, the simplification and further manipulation of above equation yields

$$J(\varepsilon,\phi) = \frac{A\mathcal{E}^2}{\varphi t^2(y)} \cdot \exp\left(-B\frac{\varphi^{3/2}}{\mathcal{E}} \cdot v(y) \right) \tag{11}$$

Numerical factors in the above equations are given by $A = 1.54 \times 10^{-6}$, $B = 6.87 \times 10^7$, $y = 3.79 \times 10^{-4} \mathcal{E}^{1/2}/\phi$.

Including the previous approximations for $t^2(y)$ and $v(y)$, the change from current density to current and $\mathcal{E}$-field to voltage can be expressed as

$$I = \int J(\varepsilon,\phi)dy = \alpha J \qquad \text{and} \qquad \mathcal{E} = \beta V \tag{12}$$

where α and β are fitting factors that are meant to roughly correspond to the emitting area is the local field conversion factor at the emitter surface. Actual computation of the emitting current involves determining the electric field everywhere on the tip surface which can be done numerically. However due to the complex geometry of the emitter tip region, the α and β coefficients are used to arrive at a somewhat simplified analytical equation for the emission current.

If these approximations are used the modified Fowler-Nordheim equation is given by

$$I = a_{FN} V^2 \exp\left(-b_{FN}/V\right) \tag{13}$$

where:

$$a_{FN} = \frac{\alpha A \beta^2}{1.1\varphi} \exp\left(\frac{B\left(1.44\times10^{-7}\right)}{\varphi^{1/2}}\right) \quad \text{and} \quad b_{FN} = \frac{0.95 B \varphi^{3/2}}{\beta}$$

The parameters a_{fn} and b_{fn} can be found from the slope and intercept of the Fowler Nordheim plot of I/V^2 vs. $1/V$ as shown in Figure 6. Fowler-Nordheim theory of electron field emission has been widely accepted due to its good correlation to experimental data.

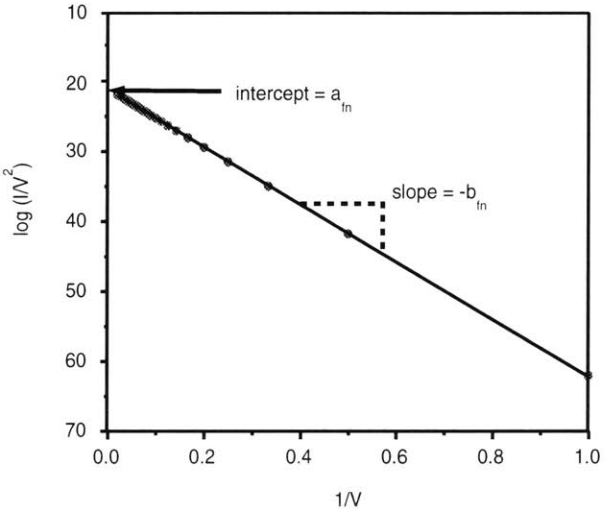


Figure 6. Fowler-Nordheim I-V Characteristic

Typical Fowler-Nordheim field emission characteristics plotted as log (I/V^2) versus $1/V$

2.3. Field Emission from Semiconductors

There has been a concerted effort to use semiconductor or insulator-based field emitters for display, sensor and microwave applications [21,22,23]. One motivation for this work is the ability to selectively control the material's electronic band structure through epitaxial growth, chemical vapor deposition or implant doping techniques. By

using these methods, the field emission characteristics can be modified or controlled to exhibit enhanced performance. While conceptually similar to tunneling from metals, electron emission from semiconductors must take into account a material's electronic band structure, field penetration within the material, and interface surface states to accurately describe the underlying physical processes. To this end, several assumptions made in the Fowler-Nordheim derivation must be reviewed with greater scrutiny.

For a band gap material, the Fermi energy level is no longer located above the conduction band minimum as in the case of a metal. It lies in most cases somewhere between the valence and conduction bands. In addition the large electric fields that are generated for field emission can significantly alter the electronic band structure near the surface thereby changing the conduction characteristics of the device (Figure 7).

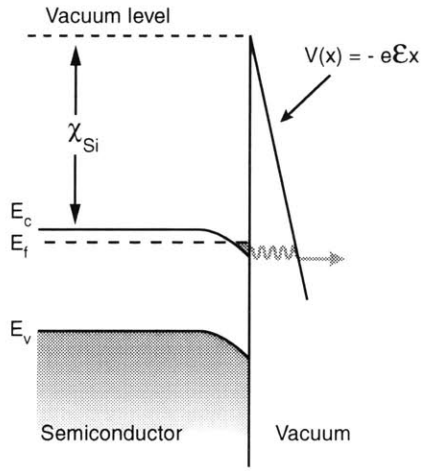


Figure 7. Field Emission from a Semiconductor Surface.

Band bending caused by the external electric field results in an accumulation layer to form near the surface of silicon. Image charge correction to the potential V(x) is not shown.

Comparing the energy diagrams for metal (Figure 3) and silicon field emission (Figure 7), it is apparent that the surface electron concentrations are quite different. In the case of a metal, the supply of electrons is assumed to be very large such that there is almost no electric field penetration into the material. The electric field is therefore terminated very close to the surface by a surface charge. In the case of a semiconductor however, the electron concentration inside the material can be altered by the electric field and at the surface there will be a corresponding shift of the conduction band with respect to the Fermi energy.

Conceptually under high electric fields the silicon surface can appear metallic-like from an electronic point of view. This is because under high field conditions, a two-dimensional Fermi sea of electrons or holes is created to form a surface inversion or accumulation layer. Thus while the Fermi level is below the conduction band minimum in the bulk, at the surface it is above the conduction band and the very high concentration of carriers makes it behave somewhat like a metal surface.

In the derivation of field emission in Section 0, the most general expression for the emitted current density can be expressed as

$$J(E_x,\mathcal{E}) = e\int_{-\infty}^{\infty} N(E_x)T(E_x,\mathcal{E})dE_x$$

where again E_x is the electron energy normal to the surface, $N(E_x)$ is an electron supply function, $T(E_x)$ is the transmission probability through the potential barrier, and $\mathcal{E}$ is the electric field at the surface. It was also seen that for low temperatures the emitted electrons originate from a small energy interval around the Fermi level. The supply function is found by combining the electronic density of states and carrier distribution normal to the surface (x-direction) to yield

$$N(E_x) = \frac{4\pi m k_b T}{\hbar^3}\ln\left(1+\exp\left(\frac{E_f - E_x}{k_b T}\right)\right)$$

Investigations have been done in which modified Fowler-Nordheim equations are derived for field emission from silicon [16,24,], however these derivations focus mainly upon the fact that the electron distribution may not be sharply peaked about E_f consequently resulting in a broader energy distribution of emitted electrons. In addition, more rigorous analyses of the electron energy distribution and its impact on the transmission probability have been carried out [25] but often they become mathematically cumbersome and obscure the underling physics to some degree. The focus in the subsequent sections will be to examine the electron supply function, $N(E_x)$, and transmission probability, $T(E_x,\mathcal{E})$, to ascertain how they are affected in silicon-based field emission.

2.3.1. ELECTRON SUPPLY FUNCTION IN SILICON EMISSION

In the case of a metallic surface the Fermi energy, E_f, lies at the top of the conduction band and was taken to be equal to the material work function, φ, with respect to the vacuum level. For a semiconductor a similar procedure for deriving the field emission current density may be followed however the material work function must now be modified to

$$\varphi_{Si} = \chi_{Si} + (E_c - E_f) \tag{14}$$

where χ_{si} is the silicon electron affinity (Figure 7). In general it is difficult to determine the location of the Fermi level in a silicon field emission device. A simple model is proposed however, in which the silicon field emitter is represented analogous to a metal-oxide-semiconductor system. The motivation for this approach draws from the similarity between field emission into vacuum and electron tunneling through a thin film (oxide in this case) [16]. The goal of this formalism is to determine of the Fermi level within the semiconductor and subsequently find the modified potential φ_s.

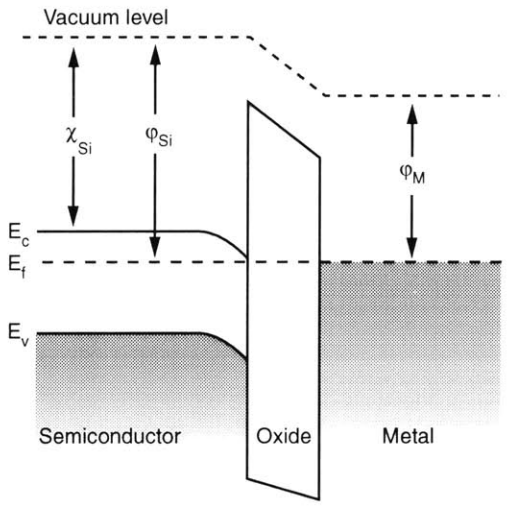


Figure 8. Energy diagram for a MOS Structure

A high electric field on the field emitter tip results in significant band bending at the silicon surface.

The proposed approach uses fundamental charge and field relations for a planar MOS system and correlates the resulting solution to the field emitter structure. The goal is to determine the electrostatic potential and location of the

Fermi level at the silicon surface. This can then be used to correct for the silicon work function variation described in the above equation for φ_{Si}. Several considerations must be taken into account when relating these two systems. First is the assumption that the Fermi level of the silicon tip does not vary significantly over the tip radius of curvature from which most electron emission occurs. This will be shown through simulation results conducted for a metal field emitter [26]. Secondly, the metal work function must be set equal to the silicon work function in the model so that the built in potential $\phi_{bi} = (\varphi_{Si}-\varphi_m)$ is identically zero. This is obvious since in the case of a field emitter system, there is no potential difference between the silicon emitter tip and the metal gate electrode in equilibrium. The electrostatic equations governing the MOS system can be solved to arrive at expressions for the surface charge density, potential and electric field. To then match the MOS system to the field emitter, a sufficiently large voltage can be applied to the metal to achieve a surface electric field solution that is comparable to field intensities found on field emitter structures. In addition, the oxide dielectric constant can be set equal to one to simulate the vacuum region of the emitter system. Because charge and potential equations are being solved analytically, physical considerations such as oxide breakdown do not need to be taken into account.

There are several basic relations that can be used to describe the MOS structure that will be correlated the field emitter system. These relationships describe the charge distribution and electric fields within the structure and when modified appropriately, can be used for non-equilibrium conditions as well. A very succinct analysis has been done [27] and will be used to present an analytical solution to the MOS system. Figure 9 shows a schematic of a MOS structure and the associated charge distribution, electric field, and electrical potential within the semiconductor material.

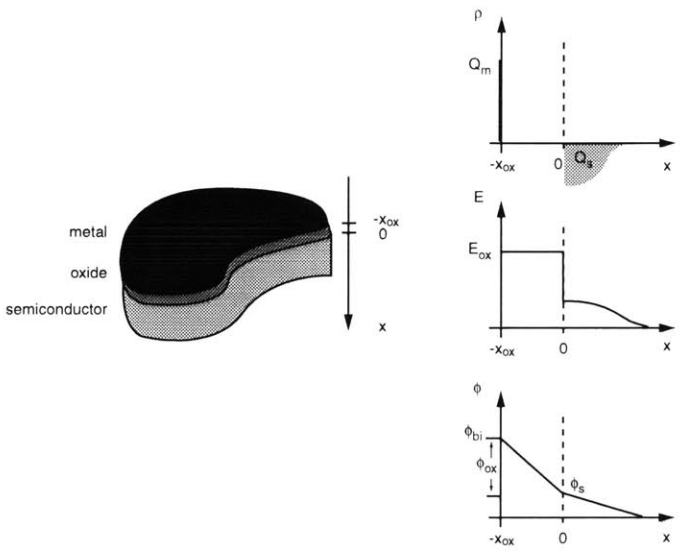


Figure 9. MOS Structure

Charge density, electric field, and electric potential as a function of distance are shown. If the silicon and metal work functions are equal, the built-in potential, ϕ_{bi} will be zero.

Applying Gauss' law to a region that encloses the entire semiconductor charge Q_s it is seen that the electric field within the oxide region is

$$\mathcal{E}_{ox} = -\frac{Q_s}{\varepsilon_{ox}} \tag{15}$$

In addition, since the dielectric constants of the oxide and silicon are different we have that

$$\varepsilon_{ox}\mathcal{E}_{ox} = \varepsilon_{si}\mathcal{E}_s \tag{16}$$

giving

$$\mathcal{E}_s = -\frac{Q_s}{\varepsilon_{si}} \tag{17}$$

for the electric field at the semiconductor surface.

The potential drop across the surface ϕ_{bi} (the difference in work function between the metal and semiconductor materials) is equal to

$$\begin{aligned}\phi_{bi} &= \phi_s + \phi_{ox} \\ &= \phi_s + x_{ox}\mathcal{E}_{ox} \\ &= \phi_s - \frac{Q_s x_{ox}}{\varepsilon_{ox}} = \phi_s - \frac{Q_s}{C_{ox}}\end{aligned}$$

If a voltage V is applied to the metal surface the equation is modified to

$$\phi_{bi} + V = \phi_s - \frac{Q_s}{C_{ox}} \tag{18}$$

To solve more rigorously for an electrostatic bias condition, a Poisson-Boltzmann formulation was followed to determine the electric charge, potentials and fields within the silicon device. For a uniformly doped n-type semiconductor the charge density can be expressed as

$$\rho = q(n - p - N_d) \tag{19}$$

Where p and n are the carrier densities, N_d is the dopant concentration, and q is the electronic charge. With this charge density Poisson's equation for electrostatic potential is then

$$\frac{d^2\phi}{dx^2} = -\frac{q}{\varepsilon_{Si}}(n - p - N_d) \tag{20}$$

Since the oxide layer between the silicon and metal surfaces prevents current flow, the semiconductor is in equilibrium and the relation $np = n_i^2$ holds. For this situation Boltzmann statistics may be applied and the carrier concentrations can be expressed as

$$\begin{aligned} n &= n_o \exp(\frac{q\phi}{kT}) \approx N_d \exp\left(\frac{q\phi}{kT}\right) \\ p &= p_o \exp(\frac{-q\phi}{kT}) \approx \frac{n_i^2}{N_d}\exp\left(-\frac{q\phi}{kT}\right)\end{aligned} \tag{21}$$

where n_o and p_o are the electron and hole concentrations in the bulk and the potential deep within the bulk is taken to be zero. This assumes that most donor sites are fully ionized such that $n_o \sim N_d$, which is valid at room temperature or above. In the bulk, charge neutrality demands that

$$n_o - p_o - N_d = 0 \tag{22}$$

Combing the above four results yields the Poisson-Boltzmann equation for the electrostatic potential,

$$\begin{aligned} \frac{d^2\phi}{dx^2} &= -\frac{qN_d}{\varepsilon_{Si}}\left[\left(\exp\left(\frac{q\phi}{kT}\right)-1\right)-\frac{n_i^2}{{N_d}^2}\left(\exp\left(-\frac{q\phi}{kT}\right)-1\right)\right] \\ &= -\frac{qN_d}{\varepsilon_{Si}}F(\phi) \end{aligned} \tag{23}$$

Going through the mathematical analysis (Appendix A), boundary conditions for the surface electric potential can be solved for and a self-consistent expression for the electric potential can be reached. Once the electric potential as a function of distance is known the electric field and semiconductor charge can be solved for from the equations

$$\mathcal{E} = -\frac{d\phi}{dx} = \sqrt{\frac{2kTN_d}{\varepsilon_{Si}}}\,F(\phi) \tag{24}$$

and

$$\begin{aligned} Q_e &= -qN_d\int_0^\infty \exp\left(-\frac{q\phi}{kT}\right)-1\;dx \\ Q_h &= q\frac{n_i^2}{N_d}\int_0^\infty \exp\left(\frac{q\phi}{kT}\right)-1\;dx \end{aligned} \tag{25}$$

Once a solution is found for the electrostatic potential, it is possible to observe the electrical response and determine several parameters of interest. Energy band and electric field calculations are shown in Figure 10. In order to simulate field emitter conditions, the electrostatic solution for the surface electric field was matched to field calculations conducted for finite element analysis solutions (section 0). Electric field intensities on the order of $\mathcal{E}$~3.5x10^9 V/m were calculated.

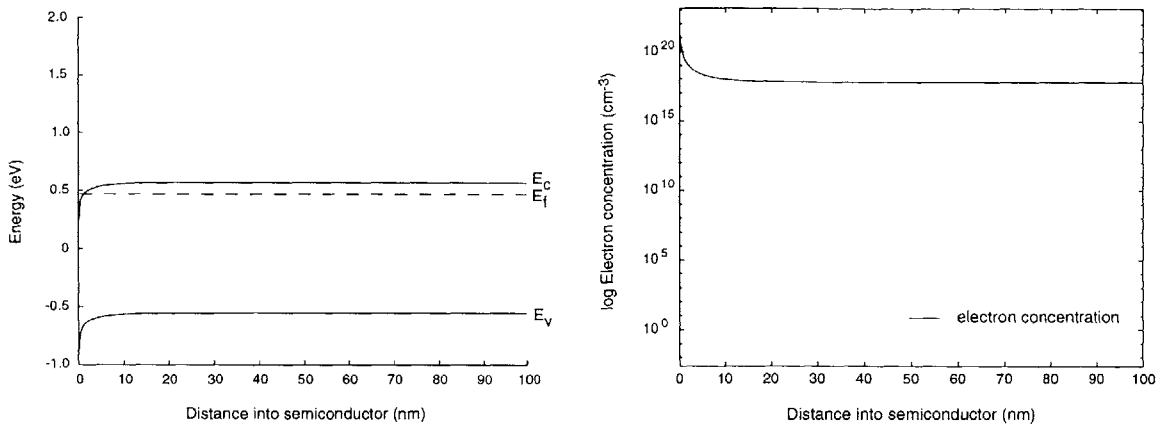


Figure 10. N-type Silicon Emitter: Energy Band Diagram and Electron Concentration

Accumulation condition for n-type silicon emitter tip under an electric field matching condition of $\mathcal{E}$~3.5x10^9 V/m. Silicon concentration of N_d = 1e17 cm^{-3}.

As can be seen in the above figure, the accumulation layer that forms causes the conduction band to drop below the Fermi level near the surface. The very high electron concentration near the surface causes the material to behave very similar to a metal. It should be noted that the calculated electron concentration is on the order of 10^{23} cm^{-3}. In actuality a quantum mechanical 2-D electron gas exists at the interface due to the confinement of the electron gas very close to the surface (within ~100Å). The resulting concentration of the 2-D electron gas in on the order of 10^{12}-10^{13} cm^{-2}.

2.3.2. TRANSMISSION PROBABILITY IN SILICON

As in the case of a metal, there exists a potential barrier between the silicon surface and vacuum. When high fields are applied to the field emitter tip, deformation of the potential barrier occurs and appreciable electron tunneling through the barrier can occur. A fairly rigorous analysis of the electron energy distribution and its impact on the transmission probability has been carried out [25] but is somewhat mathematically cumbersome. The analysis looks at the effects of a non-sharp Fermi-Dirac distribution on the transmission probability,

$$T_{WKB}(E_x) = \exp\left(-\int_{x_1}^{x_2} \sqrt{\frac{8m(V(x)-E)}{\hbar^2}}\,dx \right)$$

and derives modified expressions for the WKB transmission probability. The equations are solved analytical through Taylor expansion and match well to experimental data. However through modeling simulations done by [26], it has

been seen that the high electric fields in field emitter devices are fairly uniform over the emitter tip region. Figure 11 shows a boundary element mesh that was developed by Dr. J.Y. Yang [28] to determine electric field potential and emission current densities of small (~4-10nm) emitter tip radii.

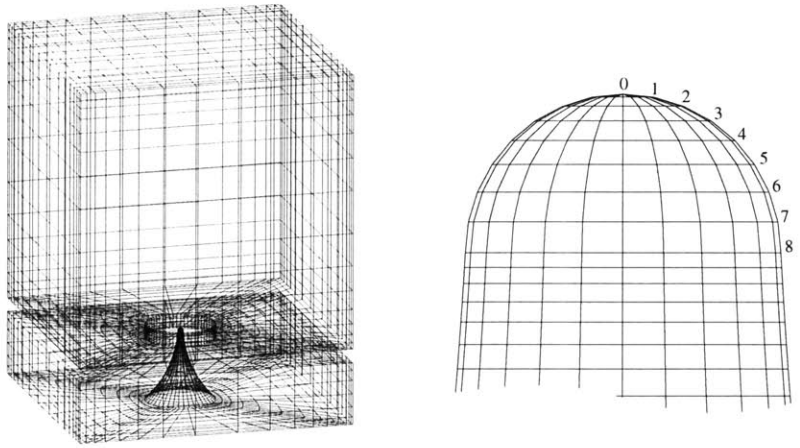


Figure 11. Boundary Element Mesh for Field Emitter Tip

(a) Mesh used to simulate field emitter electrostatic conditions and (b) expanded view of the field emitter tip with associated numbering for Figure 12.

As can be seen in Figure 12, the electric field over the simulated emitter tip region drops from approximately 30% from panel #0 to panel #8. The emitted current density however decrease by several orders of magnitude over this region and indicates as expected that the emission current is very strongly affected by the surface electric field.

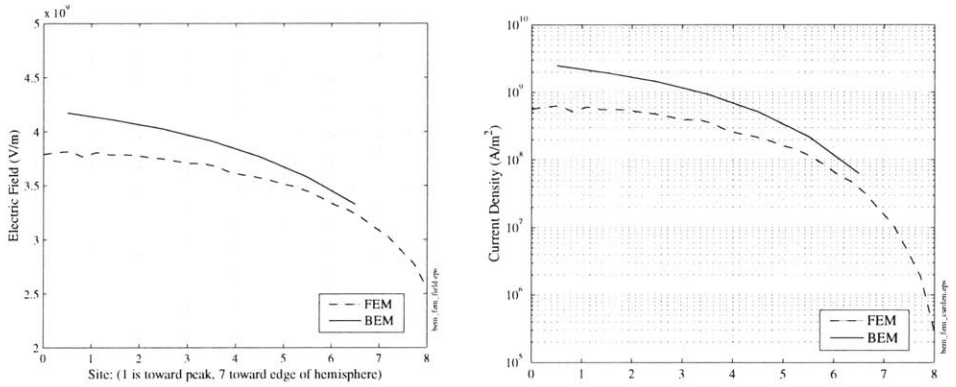


Figure 12. Electric Field and Current Density for BEM and FEM Models

The electric fields and associated current density of the BEM mesh shown in Figure 11. Also shown are comparisons to Finite Element Mesh results [26].

Thus while the transmission probability and subsequent emission current density will be strongly influenced by this field variation at the tip (due to the tunneling probability having an exponential dependence on the electric field), the effect of a spread-out electron distribution within the silicon tip surface is expected to not play as significant a role in altering the emission current density.

Chapter 3 –MOSFET Theory

3.1. Vertical MOSFETs

The vertical MOSFET (VMOS) behaves similarly to the lateral MOSFET (LMOS) in regards to device operation. The predominant difference between the two devices is that in contrast to the LMOS, the current flow between source and drain regions occurs perpendicular to the wafer surface in the VMOS structure. Figure 13 shows a schematic of vertical and lateral MOSFET devices. Several key differences are apparent between the two structures. For the LMOS, the channel width can be increased along the z-direction while the VMOS channel width is equal to the pillar circumference, $2\pi r$. The width and length parameters are consequential since the drive current of the device is directly proportional to the W/L ratio. One important parameter to be aware of in analyzing a MOSFET device is the extent of the depletion region under the inverted channel region. For the LMOS device, the depletion region can extend into the silicon substrate without restriction. The depletion region of the VMOS however is limited to the pillar volume contained between the source and drain regions. If the depletion volume is too small, it may not be possible to reach an inversion condition for the VMOS device. As the extent of the depletion region is dependent on the substrate doping level and applied gate voltage, calculations can be done to determine if the VMOS is operating in this depletion-limited regime.

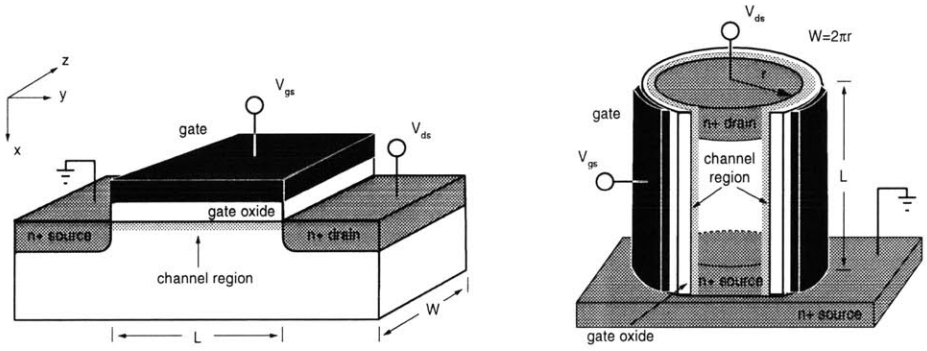


Figure 13. Lateral & Vertical MOSFET schematic

For the vertical MOSFET structure, the cylindrical shell around the pillar circumference defines the channel region. The length and width of the device are determined respectively by the height of the silicon pillar and the pillar circumference ($2\pi r$).

Several works exist that provide analysis of short-channel or fully-depleted vertical MOSFET structures [29,30,31,32,33,34], however the equations derived are mainly applicable to devices where the extent of the depletion region in the device is nearly equal to or greater than the volume in the vertical silicon pillar device (Figure 13). For the case of the devices fabricated in this work, short-channel effects and total body depletion do not play as significant a role due to the specified device dimensions. Both the extent of the inversion layer and depletion region are such that the cylindrical devices are only partially depleted and can be modeled with good accuracy using planar MOSFET analysis. The applicability and accuracy of the planar model was confirmed through the analytical calculations and verified with both simulation and experimental data. Hence a model for the vertical MOSFET structure will be developed using theory for a planar device structure.

3.2. Lateral MOSFETs

In order to understand the electronic behavior of MOSFET devices, an examination of the governing electrostatic equations was performed. Much excellent analysis has been done in this area [35,36,37] and it is instructive to present a succinct theory from this body of work. This not only provides a fundamental framework from which to start from but also allows an analytical examination of the device behavior to be completed.

A typical n-channel MOSFET under inversion is shown schematically in Figure 14. The MOSFET operates by using an electric field perpendicular to the channel region to modulate the electron current density between the source and drain junction regions. When a sufficiently large bias voltage is applied to the gate electrode, the charge density under the oxide layer can be altered to form a conducting channel between the doped source and drain regions. This channel is referred to as the inversion layer since the electrical characteristics of the silicon are "inverted" from p-type to n-type (electron concentration becomes greater than the p-type dopant concentration).

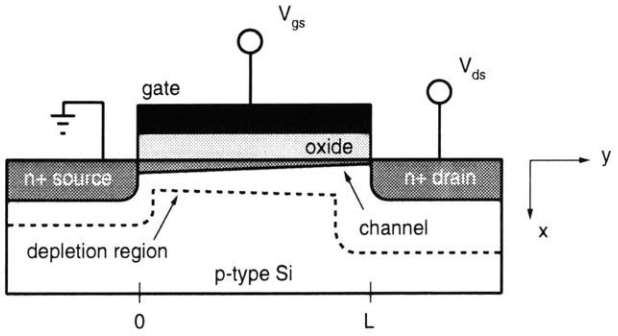


Figure 14. Lateral MOSFET schematic

An n-channel MOSFET under applied bias conditions $V_{gs}>V_T$, $0<V_{ds}<V_{dsat}$

If there is a potential difference between the source and drain (e.g. the source is grounded and a drain voltage is applied), electrons will flow from the source to the drain through the conducting inversion layer. At small drain voltages the inverted channel region behaves like a resistance and the drain current I_D depends linearly upon the drain voltage (linear regime). As the drain voltage, V_d, is increased it eventually reaches a point at which the width of the inversion layer $x_{inv}=0$ at the location $y=L$. This is called the pinch-off point and the voltage at which it occurs is defined as the saturation voltage, V_{dsat}. For any further increase in drain voltage, the drain current will saturate (saturation regime) and does not increase as the contact between the drain and the channel no longer exists ($x_{inv}=0$).

Basic MOSFET characteristics will now be derived under the following assumptions: 1) the device forms an ideal MOS structure so that there are no interface traps or fixed charge with the gate oxide, 2) drift current dominates over diffusion current, 3) carrier mobility in the inversion layer is constant, and 4) doping in the channel region is uniform. In addition the vertical electric field in the channel region is assumed to be much larger than the lateral electric field between the source and drain regions (gradual channel approximation). Figure 15 shows a MOSFET in the linear regime of operation. Under the conditions stated above, the charge induced in the semiconductor at a distance y from the source is given by

$$Q_s(y) = -C_{ox}\left(V_{gs} - \phi_s(y)\right) \tag{26}$$

where as before, $\phi_s(y)$ is the surface potential at y and C_{ox} is the gate capacitance per unit area. The total charge in the semiconductor is also the sum of the charge in the inversion layer (Q_{inv}) and the charge in the space charge region (Q_{sc})

$$Q_s(y) = Q_{inv}(y) + Q_{sc}(y) \tag{27}$$

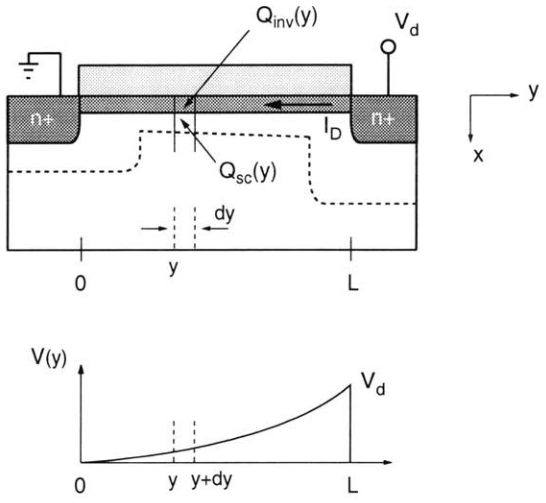


Figure 15. Enlarged View of MOSFET Channel region

MOSFET operating in the linear regime. Drain voltage drop along the channel is shown.

An equation for the charge in the inversion layer as a function of y can then be reached as

$$\begin{aligned} Q_{inv}(y) &= Q_s(y) - Q_{sc}(y) \\ &= -C_{ox}\left(V_{gs} - \phi_s(y)\right) - Q_{sc}(y) \end{aligned} \tag{28}$$

The charge in the depletion region, $Q_{sc}(y)$, in the inversion regime of operation is given by

$$Q_{sc}(y) = -qN_a x_d = -\sqrt{2\varepsilon_{si} qN_a \left(V(y) - 2\phi_f\right)} \tag{29}$$

where x_d is the width of the depletion region and , ϕ_f is defined as the potential necessary to bend the energy bands down so that $E_F = E_i$. Thus for a strong inversion condition the surface potential can be said to be $2\phi_f$.

$$\phi_s(inv) \approx 2\phi_f = \frac{2kT}{q} \ln\left(\frac{N_a}{n_i}\right)$$

Substituting the above equations into the expression for Q_{inv} yields

$$Q_{inv}(y) = -C_{ox}\left(\left(V_{gs} - V(y) - 2\phi_f\right) + \sqrt{2\varepsilon_{si} q N_a \left(V(y) - 2\phi_f\right)}\right) \tag{30}$$

The conductivity of the channel can be approximated by [38]

$$\sigma(x) = qn(x)\mu_n(x)$$

where n is the electron concentration and μ_n is the electron mobility in the channel region. For constant mobility, the channel conductance is then

$$G = \frac{W}{L}\int_0^{x_{inv}} \sigma(x)dx = \frac{W}{L}\mu_n \int_0^{x_{inv}} qn(x)dx \tag{31}$$

The integral in equation above just corresponds to the total charge per unit area in the inversion layer and is therefore just equal to Q_{inv}

$$\frac{1}{R} = \frac{W}{L}\mu_n Q_{inv}(y)$$

The channel resistance along an incremental section dy is given by

$$dR = \frac{dy}{W\mu_n Q_{inv}(y)}$$

and the voltage drop across dy is then

$$dV = I_D dR = \frac{I_D dy}{W\mu_n Q_{inv}(y)} \tag{32}$$

Integrating the left side of equation (32) from [0 V_d] and the right side from [0 L] yields an expression for the drain current

$$I_D = \frac{W}{L}\mu_n C_{ox}\left[\left(V_{gs} - 2\phi_f - \frac{V_d}{2}\right)V_d - \frac{2}{3}\frac{\sqrt{2\varepsilon_{si} q N_a}}{C_{ox}}\left(\left(V_d + 2\phi_f\right)^{\frac{3}{2}} - \left(2\phi_f\right)^{\frac{3}{2}}\right)\right] \tag{33}$$

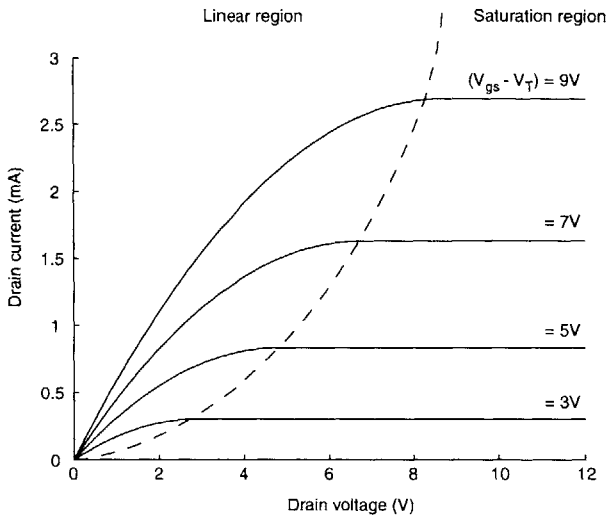


Figure 16. MOSFET Drain Current Characteristic

I_D versus V_d plot for a uniformly doped MOSFET device.

For the case for small drain voltages equation (33) reduces to

$$I_D = \frac{W}{L}\mu_n C_{ox}\left[(V_{gs} - V_T)V_d\right] \tag{34}$$

where V_T is the threshold voltage

$$V_T = \frac{\sqrt{2\varepsilon_{si} q N_a (2\phi_f)}}{C_{ox}} + 2\phi_f \tag{35}$$

We can see that this corresponds to the linear regime of operation in Figure 16. The channel conductance and transconductance are given by

$$\begin{aligned} g_D &= \left.\frac{dI_D}{dV_d}\right|_{V_{gs}=\text{constant}} = \frac{W}{L}\mu_n C_{ox}\left(V_{gs} - V_T\right) \\ g_m &= \left.\frac{dI_D}{dV_{gs}}\right|_{V_d=\text{constant}} = \frac{W}{L}\mu_n C_{ox} V_D \end{aligned} \tag{36}$$

In the saturation region of operation, V_{dsat} can be obtained from

$$Q_{inv}(y) = -C_{ox}\left(\left(V_{gs} - V(y) - 2\phi_f\right) + \sqrt{2\varepsilon_{si} q N_a \left(V(y) - 2\phi_f\right)}\right)$$

with $y=L$ and $Q_{inv}(y)=0$ since the inversion channel thickness, $x_{inv}=0$, at pinch-off. This gives a saturation voltage

$$V_{dsat} = V_{gs} - 2\phi_f + \frac{\varepsilon_{si} q N_a}{C_{ox}^{\ 2}}\left(1 - \sqrt{1 + \frac{2V_{gs} C_{ox}^{\ 2}}{\varepsilon_{si} q N_a}}\right)$$

The saturation current is easily obtained by substitution and is given by

$$I_{Dsat} \approx \frac{1}{2}\frac{W}{L}\mu_n C_{ox}\left(V_{gs} - V_T\right)^2 \tag{37}$$

which is independent of the drain voltage (Figure 16). For the idealized MOSFET in the saturation regime, the channel conductance is zero and the transconductance is

$$g_m = \left.\frac{dI_D}{dV_{gs}}\right|_{V_d = \text{constant}} = \frac{W}{L}\mu_n C_{ox}\left(V_{gs} - V_T\right) \tag{38}$$

Chapter 4 - Device Fabrication and Simulation

4.1. Device Structure

Device fabrication was carried out with the objective to create vertical structures that exhibited similar electrical characteristics of MOSFET devices. Previous work [39,40,41] has demonstrated the feasibility of creating similar vertical-based MOSFET structures. Two main fabrication techniques exist for creating vertical MOS devices. The first method involves the use of epitaxy on a silicon substrate to create the source, channel and drain regions of the MOSFET. The doping level of the various regions is modified by changing the gas phase concentration during the epitaxial deposition process and can yield very good control of the pillar dopant profile [42,43]. An alternative approach to creating a vertical MOS structure involves etching a vertical pillar into the silicon substrate, growing a gate oxide along the pillar sidewall and then using a vertical implant step to create source and drain regions [34,44,45]. Both device structures are shown schematically in Figure 17.

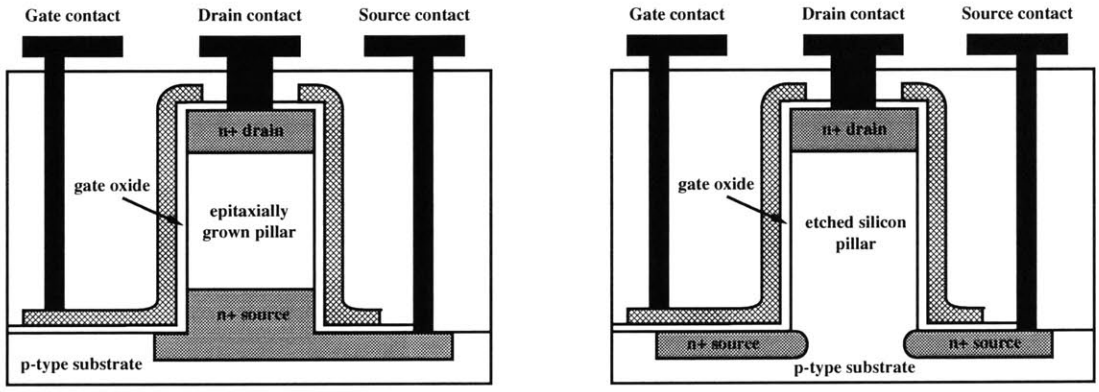


Figure 17. Vertical MOSFET design

(a) VMOS formed by epitaxial deposition of silicon, (b) similar structure fabricated by etching a silicon pillar followed by a vertical ion implant step.

It was determined that an etched pillar approach to create the vertical MOS would be preferred for several reasons. Two benefits to the pillar approach are uniformity of the gate oxide on the vertical sidewall and the ability to contact the MOSFET body region to adjust the device threshold voltage if desired. It is apparent that in the epitaxial approach, the body region is sandwiched between the two doped source and drain regions, effectively isolating it

from the bulk substrate. If the device body volume is not large enough, the region could become completely depleted before an inversion channel is formed thus limiting device operation. Additionally with epitaxial growth processing, often film non-uniformity, crystalline defects, and bunching of film layers [46] in small geometries (i.e. corners or edges) can lead to undesirable film qualities.

4.2. Process Outline and Layout

A fabrication process implementing only four photolithography mask steps was used to create the vertical MOSFET structures. Process simulations were carried out using SILVACO to verify design flow and feasibility of each process step. Simulation results and fabrication process flow for VMOS structures are summarized in Figure 18. In general the process simulation results agreed very well with fabrication processes and provided a good guideline to investigate alternative fabrication methodologies without running silicon in the laboratory. Some factors that were not anticipated through simulation will be detailed in the next section.

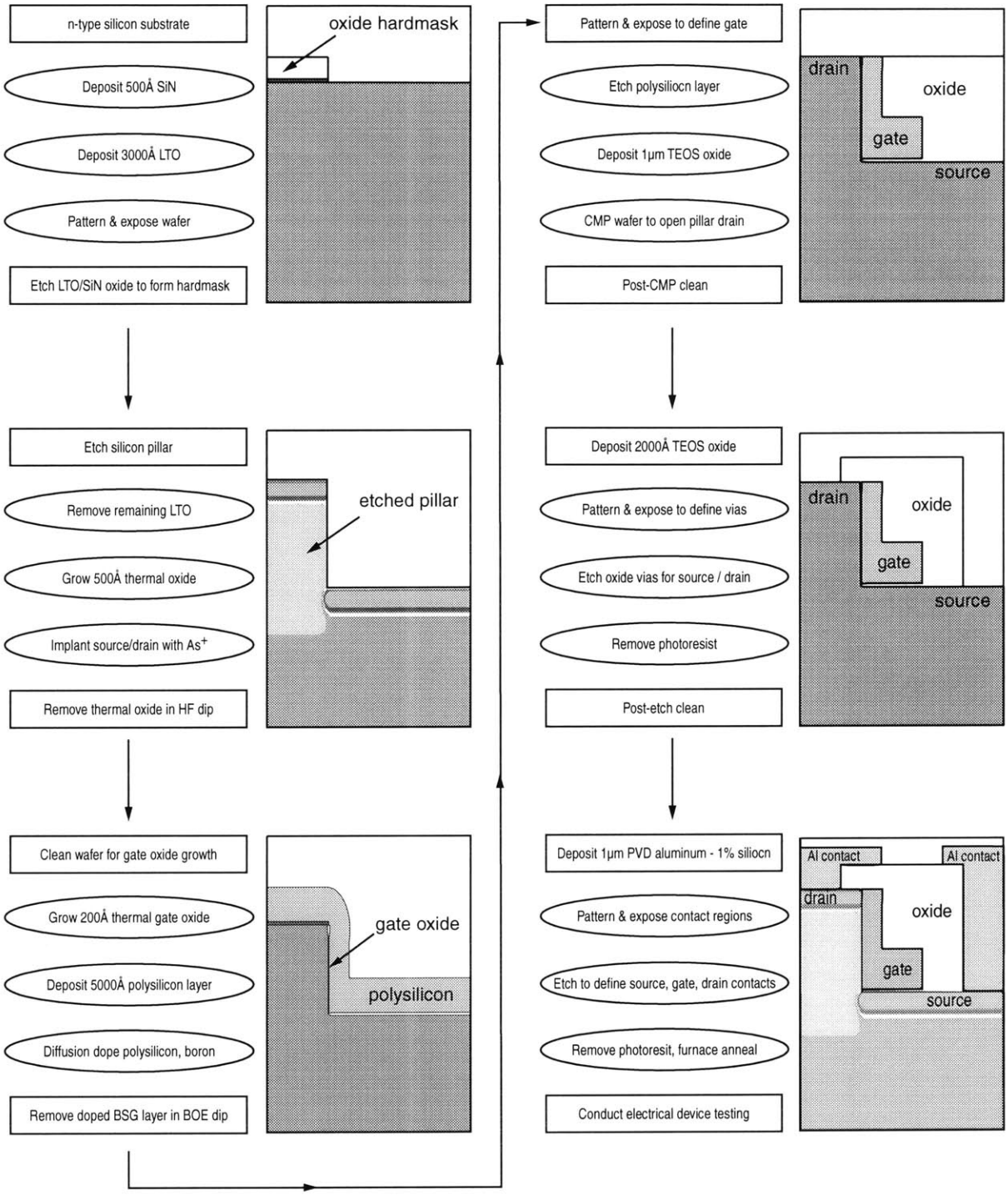


Figure 18. VMOS Process Design & Simulation

4.3. Device Fabrication

Devices were fabricated on 4" n-type substrates with a nominal resistivity of $\rho \sim 4\ \Omega$-cm. It was desired that n-channel VMOS devices be created. However an n-type substrate was chosen so that individual VMOS pillar arrays could be electrically isolated from each other through use of a p-type tub implant.

For the initial VMOS processing, a 500Å silicon nitride (SiN) layer, 3000Å low temperature oxide (LTO) and 5000Å polysilicon layer were deposited onto the silicon substrate. Because the LTO film was to be used as an oxide hardmask for etching VMOS pillars in silicon, a densification was carried out at 950°C to give a high oxide/silicon selectivity during the etch step. The top polysilicon layer was patterned with photoresist and anisotropically etched in a Cl_2/HBr plasma chemistry to form an implant mask layer for the p-tub formation. Process simulations indicated that a high energy boron implant could penetrate the 3000Å LTO and 500Å SiN layers to a depth that would produce uniform tub doping. A boron (B_{11}^+) implant was done with a beam energy and implant dose of 195 keV and 2e14 cm^{-2}. After implantation, an extended anneal step was performed to ensure sufficient diffusion of the implanted species and to provide a uniformly doped p-type layer in the top ~2μm of the n-type substrate. The doping level at this stage is important because it determines the channel doping and subsequently V_T of the VMOS devices. Figure 19 shows good agreement between simulated and actual implant profiles along the vertical direction of the pillar structure (Figure 17). Implant profiling was performed using quadrapole secondary ion mass spectroscopy (SIMS) measurements through an external vendor.

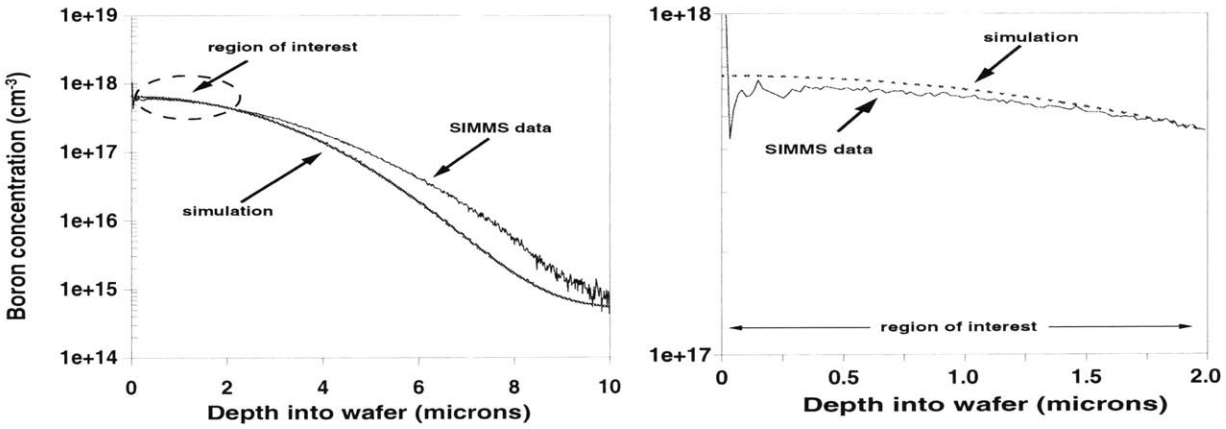


Figure 19. Simulated and measured boron implant profiles

Dopant profiles shown good matching in the region of interest (VMOS pillar). Doping profile is along the vertical direction into the substrate.

The LTO and SiN layers were then patterned with photoresist and etched in a low pressure CHF_3 plasma to form an oxide hardmask for the VMOS pillar arrays. After definition of the oxide hardmask posts (3000Å in height), the silicon pillars that would form the VMOS device were etched in using a CHF_3/HBr chemistry. A low pressure etch was used to give a vertical device profile such that the device channel region (the pillar sidewalls) would not become unintentionally doped during the source / drain implant step. Once the silicon pillar were formed, the oxide hardmask was removed with hydrofluoric acid and a 500Å thermal oxide was grown. The thermal oxide was used as additional protection for the VMOS sidewall channel against possible implant doping. There was some concern that the thermal oxide grown at the top regions of the pillars would introduce stress and possible film delamination of the SiN layer at the pillar tops however process simulations indicated that the SiN layer would adhere sufficiently to the silicon surface. The SiN film is used to provide process latitude in a subsequent chemical mechanical polishing step where it will serve as an etch stop. Post-etch scanning electron micrographs of the pillar etch and subsequent sidewall oxidation are shown in Figure 20.

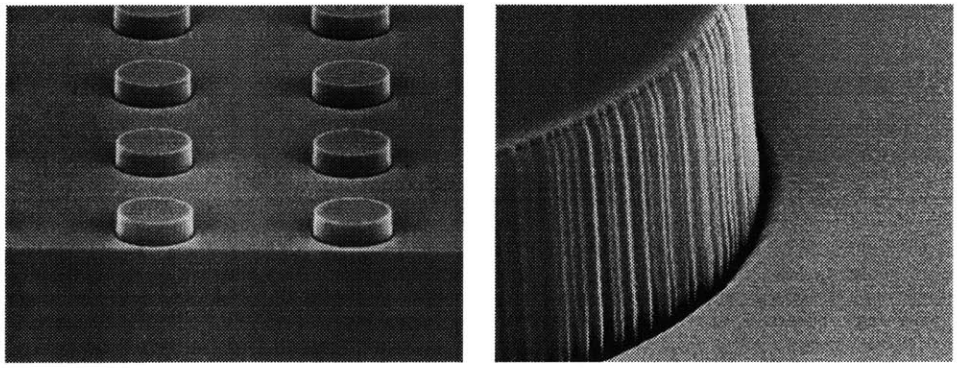


Figure 20. Silicon pillars for Vertical MOS structure

Vertically etched pillar arrays and magnified view of an oxidized pillar sidewall.

As can be seen from Figure 21 there exists surface texturing on the sidewall regions of the silicon pillars. This texturing is due to the pattern transfer of the oxide hardmask into the silicon substrate during the etch process. From SEM inspection the groove depth and period appear to be on the order of 50Å and 200Å respectively. This raises some interesting possibilities regarding the electron transport in the conducting inversion channel of the VMOS under applied bias conditions. While surface roughness in the vertical direction appears to be somewhat constant (on the order of 5-15Å), the grooved sidewall might results in many vertical conduction channels along the sidewall. Each channel could be isolated from neighboring channels due to the lateral periodicity of the texturing. However, this phenomena is likely only to occur when the device is in weak inversion. Under strong inversion where the gate voltage is sufficiently larger than the device threshold voltage, all of the channel regions would become inverted. However the degree of inversion would differ slightly causing an adjustment in the amount of total current density flowing upwards through the vertical MOSFET device. In addition, it is expected that the interface integrity between the silicon and gate oxide layer will not be as smooth as a traditionally grown thermal oxide in planar MOSFET fabrication due to the somewhat stochastic chemical processes involved in reactive ion etching.

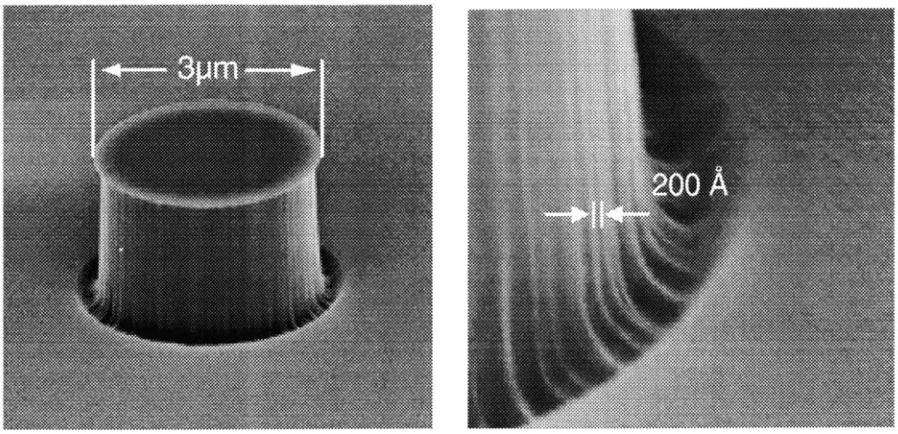


Figure 21. Sidewall texturing of VMOS channel

Grooves with 200Å-300Å periodicity and depth of ~50Å can be clearly seen.

Highly doped source and drain regions of the VMOS device were then simultaneously created by an arsenic (As^+) implant of 150 keV with a 5e15 cm^{-2} dose. Arsenic was chosen as the implant species over phosphorous because of its lower diffusion coefficient. Because phosphorous would diffuse to a much larger extent in subsequent thermal processing steps, undesired body isolation of the VMOS pillar could result. Due to the low pressure plasma etch, a small amount of micro-trenching (~150 nm) at the base of each silicon pillar was observed. This was initially a concern as it could create a high resistance region between the sidewall MOS inversion channel and the source contact. However it was seen that subsequent processing steps allowed sufficient diffusion of the arsenic implant under the pillar edge to create a well defined channel path for electron conduction.

Following the source / drain implant the protective sidewall oxide was removed with hydrofluoric acid and the device gate oxide was thermally grown in a N_2O ambient at 1000 °C. From planar monitor wafers, a gate oxide thickness of 250Å was measured. However it was apparent that due to the dependence of thermal oxidation rate on crystal orientation, the vertical sidewall thickness could vary substantially from the measured planar value. To verify this critical parameter, selective oxide etching was done to delineate the actual gate oxide. Figure 22 shows a vertical gate oxide thickness of 185Å which is approximately one third the measured and observed planar oxide thickness of 450Å. The difference in planar versus vertical gate oxide thickness is mainly due to the different levels of doping within the structure. As can be seen in Figure 25, the source region of the device has a high arsenic concentration (formed by the aforementioned implant step) that will increase the silicon oxidation rate at that

surface. The pillar sidewall region on the other hand is doped with a boron concentration that is approximately three orders of magnitude lower (Figure 19) than the heavy arsenic implant. Simulation of thermal oxidation showed similar quantitative results.

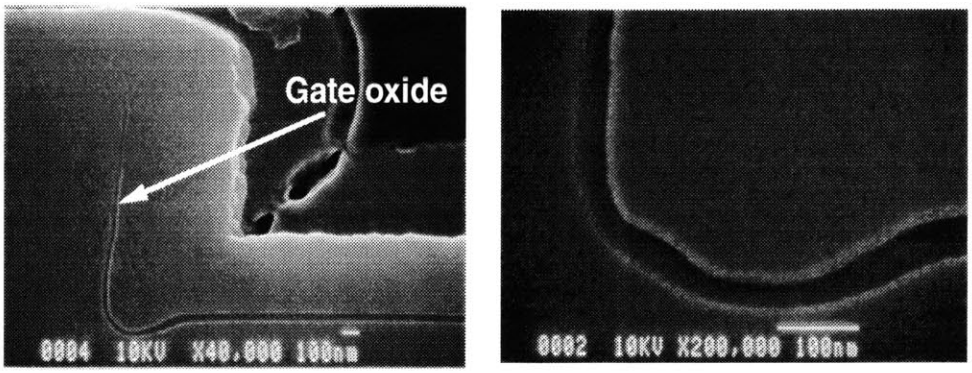


Figure 22. Vertical sidewall gate oxide

(a) Etched micrograph used to delineate the VMOS gate oxide, (b) Gate oxide at a corner region of the VMOS pillar

Immediately following gate oxidation, 5000Å of undoped polysilicon was conformally deposited. The film was then doped using a solid source diffusion of phosphorous at 925 °C to provide a low resistance path for the VMOS gate. The polysilicon layer was patterned with photoresist and etched in a high pressure Cl_2/HBr plasma to form the gate electrode structure. Figure 23 shows at the polysilicon gate pattern for a VMOS pillar array at progressive levels of magnification. The polysilicon grain structure can be clearly seen.

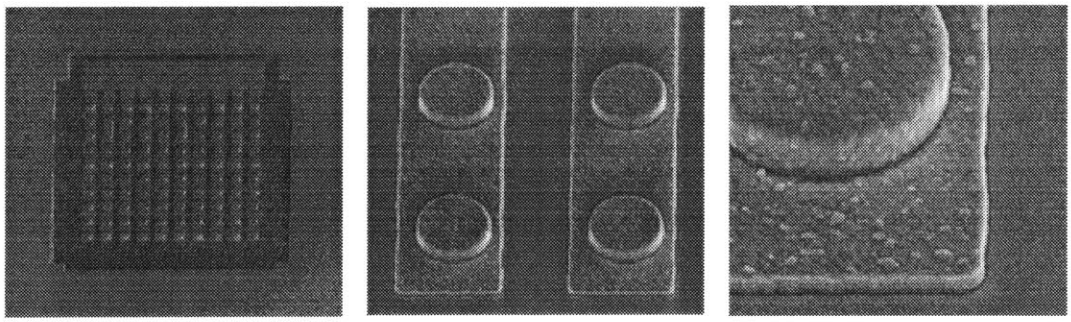


Figure 23. Polysilicon gate electrode

(a) 10x10 VMOS array, (b) two columns of VMOS devices with polysilicon gate, (c) magnified view of patterned polysilicon gate covering one VMOS pillar.

In order to contact the drain region at the top of the VMOS device without shorting to the vertical gate electrode, it was necessary to CMP the polysilicon layer. By using this polishing technique, it was possible to open a drain contact region at the top of the VMOS pillars (Figure 24). It was very important however to avoid over-polishing the pillars, which would result in removal of the doped drain junctions at the upper region of the pillars. It is for this that the aforementioned silicon nitride layer was initially deposited onto the substrate. The CMP polishing selectivity of polysilicon to silicon nitride is approximately 5:1, allowing significant process latitude in the case of a non-uniform CMP process.

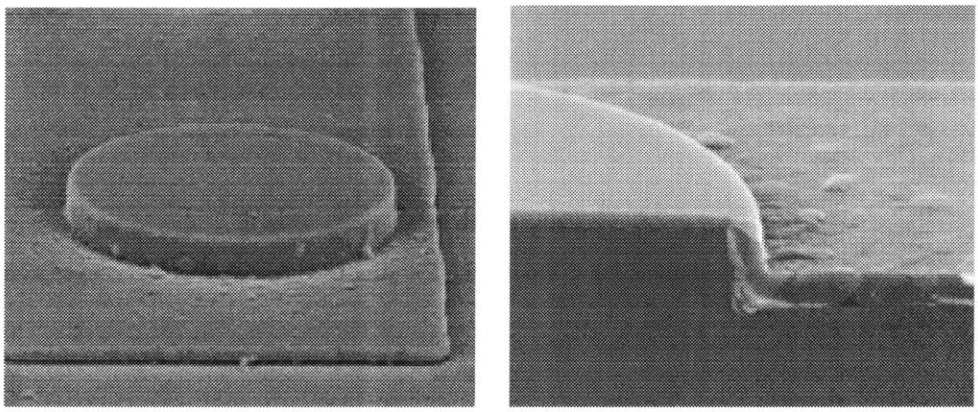


Figure 24. Gated VMOS pillars after CMP polishing

(a) Top and (b) cross-sectional views of VMOS pillars after CMP polishing.

Dopant stained SEMs were taken to verify that the drain junctions were still intact after chemical mechanical polishing (Figure 25). It can be seen that subsequent thermal processing steps allowed for sufficient diffusion of the source dopant under the pillar edge thereby providing a continuous path for conduction electrons. In addition good agreement was observed between actual devices and simulated process results.

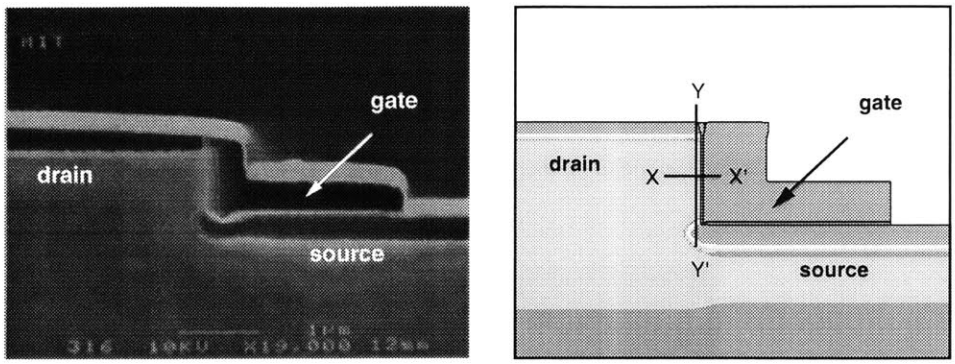


Figure 25. VMOS Device with Source, Drain and Gate regions

Actual and (b) simulated device fabrication results. Dark regions correspond to high ($>10^{19}$ cm^{-3}) n-type dopant concentration.

Dopant profiled from process simulations are plotted in Figure 26. Doping variations were seen both within the channel region (X-X') and along the VMOS body region (Y-Y'). The body doping variation is caused by the redistribution of implanted boron species during the annealing step (Figure 19). Variation in the channel doping is likely a consequence of boron out-diffusion during the formation of the gate oxide.

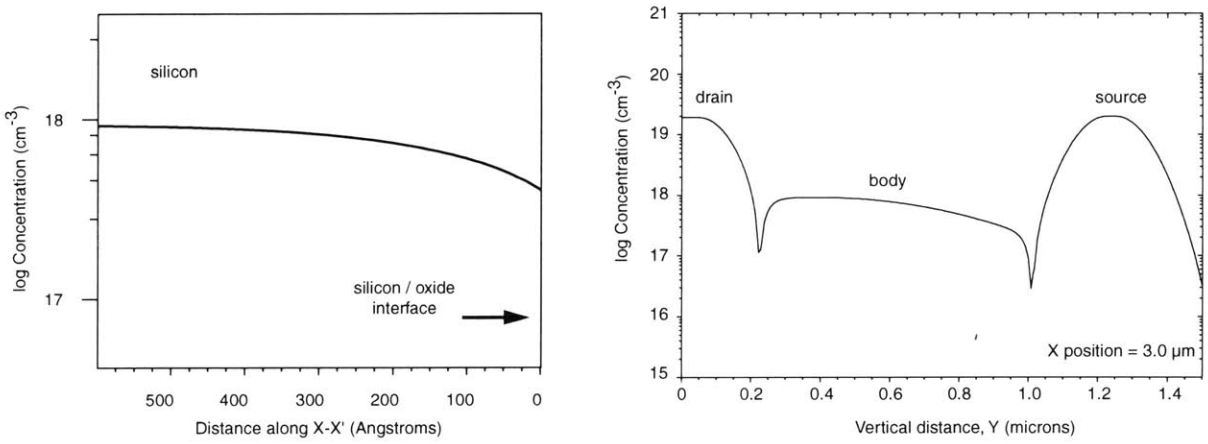


Figure 26. VMOS Doping Distributions

Dopant concentrations are shown along the X-X' and Y-Y' axis of Figure 25b. (a) The decrease in channel concentration at the silicon/oxide interface occurs due to dopant out-diffusion during the gate oxidation step. (b) Body doping variation from drain to source results from the boron implant step (Figure 19).

For the final processing steps, a 3000Å TEOS oxide layer was deposited to isolate the source, drain, and gate regions and contact vias were etched through this oxide. Low pressure physical vapor deposition was used to deposit

1μm of aluminum-silicon film onto the wafer. A one percent silicon concentration was used in the deposition to prevent aluminum from spiking into the silicon and possibly shorting the device. The wafer was patterned and etched in a Cl_2/BCl_3 plasma to define the metal contact regions for the VMOS device arrays.

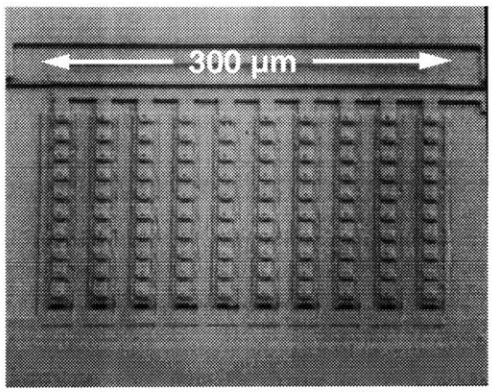


Figure 27. Completed VMOS device arrays

10x10 device arrays of vertical MOSFET devices.

Chapter 5 - Device Characterization

5.1. Device Simulation

The motivation for device simulation is two-fold: firstly to assess the validity and applicability of MOSFET analytical expressions derived in Chapter 3 and secondly to correlate numerical simulation results to actual device performance. Device modeling was carried out using MEDICI and SUPREM simulation environments. Both are commercial products available from Avanti and Silvaco. SUPREM implements several semiconductor process models (ion implantation, diffusion, etc) and was used simulate the device fabrication process. Using measured process data and process simulation results as a template, a device mesh was generated in MEDICI and used to characterize electrical device behavior in response to applied voltage conditions.

5.1.1. PHYSICAL MODELING

In order to extrapolate accurate device electrical characteristics, care was taken to verify that MEDICI simulation parameters closely matched data measured on fabricated devices and SUPREM process simulation results (Table 1). These data values were used as input variables for the MEDICI device mesh. Device profiles were not imported directly from SUPREM to MEDICI due to file incompatibility. In the case of dopant distribution from implant and diffusion processes, agreement of simulated and experimental profiles (Figure 19) lends support to the validity of this approach. Figure 28 shows a cross-sectional view of the simulated VMOS doping profile (SUPREM) and the corresponding profile used for electrostatic simulations (MEDICI). The profile corresponds to distance along the X-X' line drawn in Figure 25b. The drop in doping concentration at the silicon-oxide interface occurs during the gate oxidation process (Figure 20b). Because the silicon pillar sidewall does not have a capping layer, dopant out-diffusion [47] results in a decreased surface concentration of the implanted boron species. This will naturally have an impact on the MOSFET threshold voltage and must be taken into account for the electrostatic device simulation.

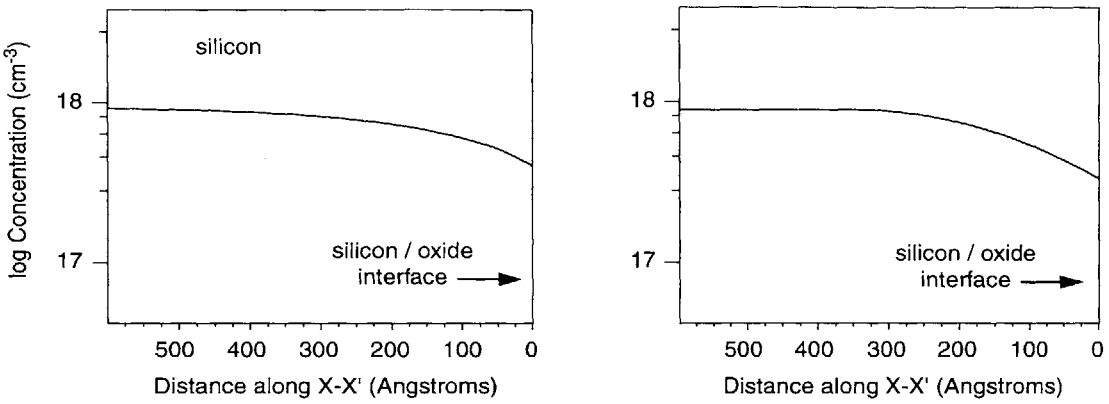


Figure 28. Lateral Doping Profile of Vertical MOS Channel

(a) SUPREM doping simulation output and (b) MEDICI input doping profile.

Another important doping variation that was taken into consideration was the vertical non-uniformity of the post-annealed boron implant. While a high temperature anneal step considerably flattened out the implanted dopant distribution (Figure 19), the dopant concentration along the channel (Y-Y' in Figure 25) drops approximately 60% over the first 1.5μm of the pillar structure. This graded doping distribution (lower doping at the source) alters the threshold voltage along the device channel and could exacerbate drain induced barrier lowering (DIBL) and device pinch-off in the saturation regime. The severity of these effects in the fabricated VMOS device will be discussed further in the following section. While it is not feasible to experimentally extract a full 2-dimensional doping profile, vertical and lateral dopant distributions that matched simulation and experimental data (Figure 19, Figure 28) were implemented in the MEDICI device mesh. The good correlation between dopant simulation and experimental data allows us to extract and use a 2-dimensional doping profile mesh with a reasonable level of confidence. Figure 29 shows the dopant distribution and device mesh used for electrostatic simulations in MEDICI.

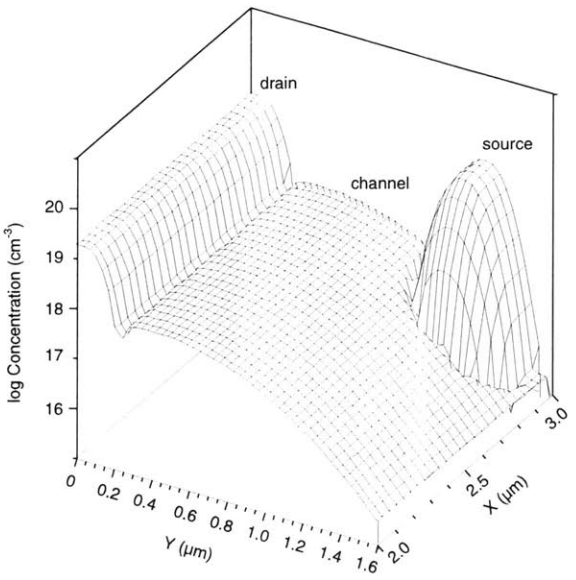


Figure 29. MEDICI Device Mesh and Dopant Distribution

Dopant variations in source, drain and channel regions of the VMOS device mesh are shown.

5.1.2. ELECTRICAL MODELING

In order to model MOSFET characteristics, a detailed electrostatic analysis of the device was conducted. The analytical framework for a MOS structure, outlined in section 2.3.1, is obviously applicable to the MOSFET device. The fundamental relations remain the same however appropriate corrections are necessary since the semiconductor is now p-type for the MOSFET rather than n-type as in the case of the field emitter. In particular, the charge density is given by

$$\rho = q(p - n - N_a)$$

where N_a is the p-type doping concentration in the bulk. The electron and hole concentrations are then

$$n = n_o \exp(\frac{q\phi}{kT}) \approx \frac{n_i^2}{N_a} \exp\left(-\frac{q\phi}{kT}\right)$$

$$p = p_o \exp(\frac{-q\phi}{kT}) \approx N_a \exp\left(\frac{q\phi}{kT}\right)$$

As before the point of zero potential is taken to be far inside the bulk. Solving the Poisson-Boltzmann equation

$$\frac{d^2\phi}{dx^2} = -\frac{qN_a}{\varepsilon_{Si}}\left[\left(\exp\left(-\frac{q\phi}{kT}\right)-1\right)-\frac{n_i^2}{N_a{}^2}\left(\exp\left(\frac{q\phi}{kT}\right)-1\right)\right]$$

for the electrostatic potential, it is possible to observe the electrical response and determine several device parameters of interest. Energy band and electric field calculations are shown in Figure 30. Significant band bending is apparent near the semiconductor surface under inversion conditions. In addition, a sharp increase in the electric field occurs where the inversion layer is formed as expected.

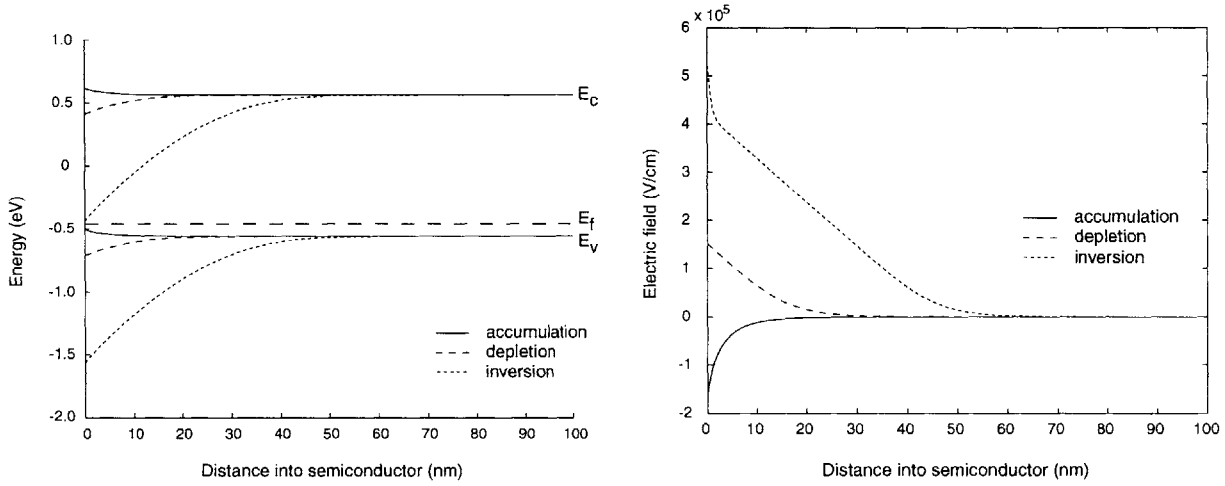


Figure 30. MOSFET Energy Band Diagram and Electric Field Calculation

As can be seen, under strong inversion a sharp triangular potential exists at the silicon surface. This leads to quantization of carriers and the formation of a 2-D electron gas. Doping concentration of N_a = 6e17 cm^{-3}, gate oxide thickness x_{ox} = 190 nm.

Figure 31 show doping concentration and surface charge (at the silicon-oxide interface) as a function of applied gate voltage. The onset of inversion occurs when the electron concentration at the surface begins to exceed the background dopant level. From the electrostatic calculations this transition occurs at a gate voltage of approximately Vg = 2.3 volts. Very good agreement was seen between this analytical solution and actual device measurements.

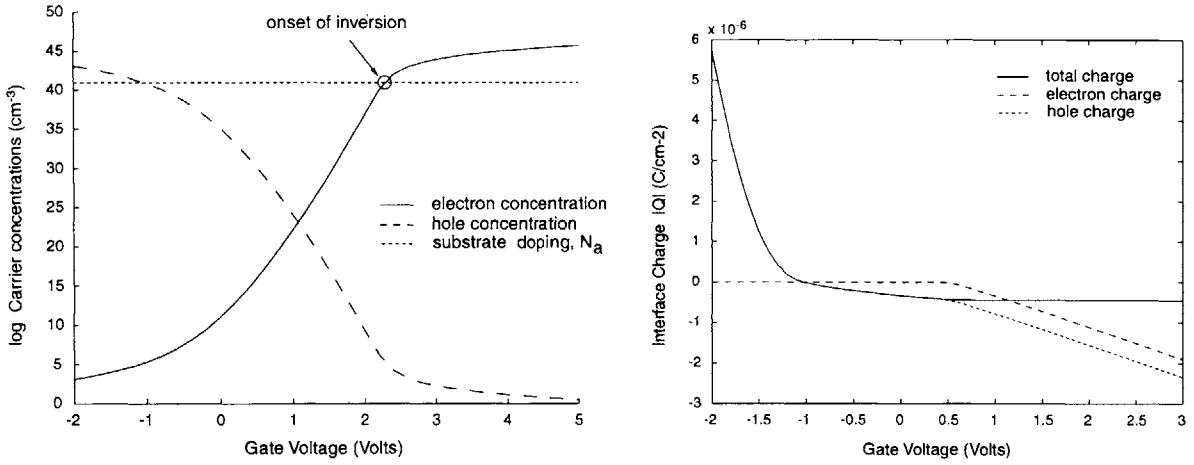


Figure 31. Carrier Concentration and Charge at the Silicon Surface

Doping concentration of N_a = 6e17 cm^{-3}, gate oxide thickness x_{ox} = 190 nm.

5.2. Electrical Testing

Electrical testing of completed vertical MOSFET devices were done using an HP4145b probe station. Several key figures of merit were measured and compared to simulated and analytical predicted values. In general, actual device data matched very well with predicted metrics.

Good correlation was observed between process simulations and fabricated VMOS devices. Simulated fabrication parameters such as gate oxide thickness, junction depths, and doping profile distributions were all within 10% of actual measured values. Electrical device characteristics also showed good agreement with actual devices. Device parameters from both simulation and experimental measurements are summarized in Table 1. Tested VMOS pillars were 8μm in diameter corresponding to a device width of 25.1μm (2πr). The device length and junction depth were determined by inspection of dopant stained scanning electron micrographs (Figure 25).

Process Parameters	Process Simulation	Experiment
VMOS device width	25.1μm	25.1μm
VMOS device length	0.78 μm	0.78 μm
Gate oxide thickness	190 Å	180-200 Å
VMOS body doping	6.6e17 cm^{-3}	6.0e17 cm^{-3}
Drain junction depth	0.26 μm	0.28 μm
Source junction depth	0.31 μm	0.32 μm
Lateral source diffusion	0.13 μm	0.16 μm

Table 1. Comparison of Simulated and Measured Process Parameters

Device Parameters	Device Simulation	Experiment
Threshold Voltage	2.2 V	2.05 V
Drain Current (V_{gs}=3V)	99.2 μA	97.4 μA
Subthreshold Leakage	0.027 μA/μm	0.032 μA/μm
Subthreshold Slope	146 mV/decade	110 mV/decade

Table 2. Comparison of Simulated and Measured Device Parameters

Some discrepancy is apparent between simulated and experimental values for the subthreshold leakage and subthreshold slope. This is believed to be a result of extrapolation error from experimentally measured data (Figure 35). Due to only partial current measurements in the subthreshold regime (V_{gs}<2.1 V), a sharply defined subthreshold slope was not available.

Good agreement was seen for simulated and experimental drain characteristics. Figure 32 shows drain voltage as a function of drain voltage for various gate voltage levels. The values shown are normalized currents for one VMOS pillar from an 10x10 array of VMOS devices (Figure 27).

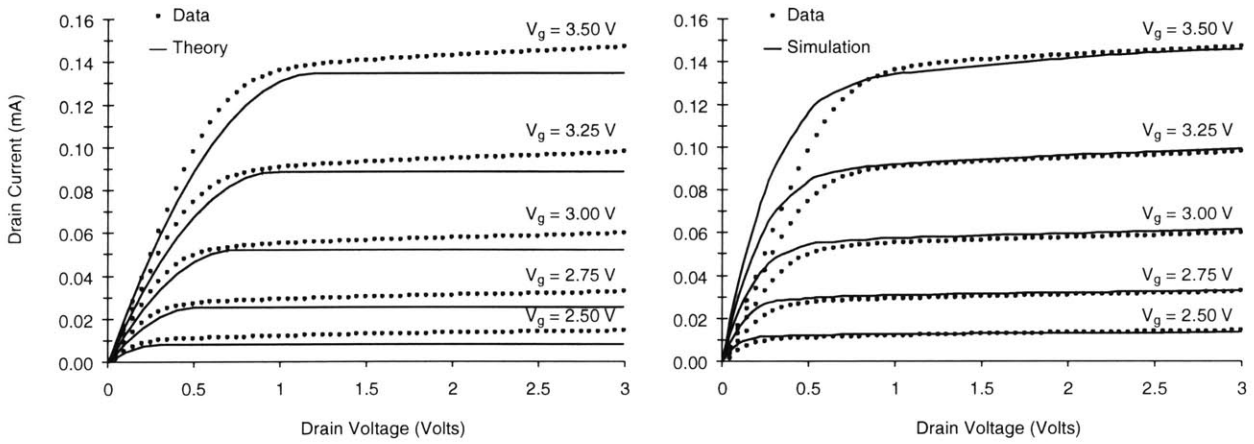


Figure 32. VMOS Drain Current Characteristics

Normalized drain current for one VMOS device as a function of drain voltage for several applied gate voltages. Graphs show good correlation of actual device data to (a) analytically predicted and (b) simulated I-V characteristics.

Comparing simulation and theoretical results with the device data, it is clear that the device drain current exhibits some deviation from the predictive models. In particular from Figure 32a, the drain current continues to increase as drain voltage is ramped beyond the saturation point (V_{dsat}). This is most likely due to some drain-induced barrier lowering (DIBL) at higher values of the drain voltage, V_{ds}. As V_{ds} is increased beyond V_{dsat}, the pinch-off effect becomes more pronounced and the effective channel length is reduced. The drain current, which is proportional to (W/L_{eff}) therefore necessarily increases with increasing drain voltage. By modifying the analytical equations to decrease L_{eff} as a function of V_d, it was possible to see the same effect (Figure 33a).

In addition to this effect, a 'tilting' of the drain characteristics is observed. This tilting is often observed in MOSFET devices and can be explained by a series or contact resistance at the device source and drain junctions. In effect a voltage drop exists across this resistance which decreases the effective drain to source voltage seen by the device. As a result, the drain current decreases from what it would be if there were no resistive effects.

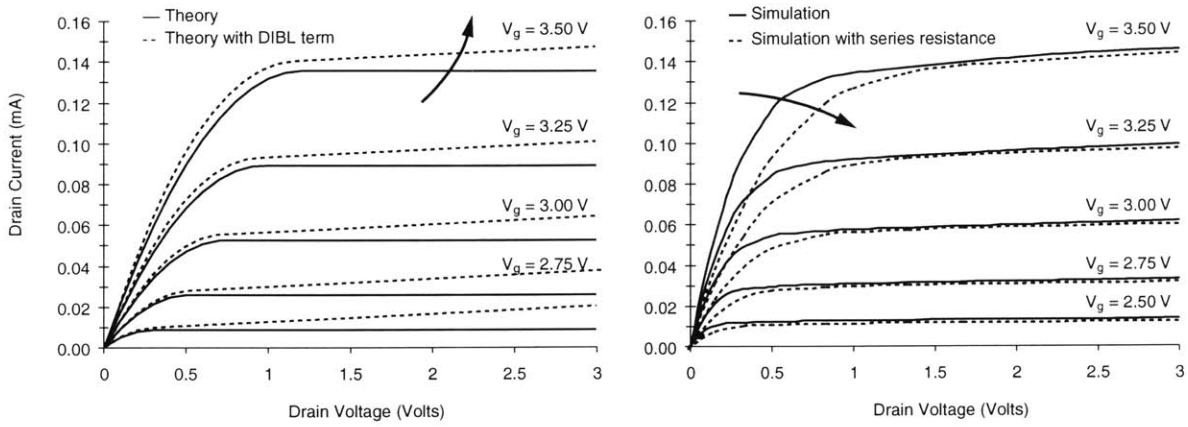


Figure 33. Correction Effects for Drain Current Characteristics

Adding DIBL to the analytical model causes drain current to increase as a function of drain voltage for $V_d > V_{dsat}$ (b) Incorporation of source resistance into the simulation model causes a shift in output current as seen on actual devices (Figure 32b).

A series resistance of R_s=700μΩ/μm was put into the simulation model as this is a reasonable value for the given device doping levels [48,49]. As can be seen from , with the inclusion of series resistance, the simulation results matched very well to device data

Another factor that may account for the difference between simulated and measured drain characteristics could be reduced mobility in the actual device that was not fully accounted for in the simulation. For the device simulation in MEDICI, a concentration dependent mobility model and a surface mobility model were used concurrently. The first model uses tabulated values for bulk mobility calculations and is used to determine current flow away from the surface. The second model takes into account surface scattering at the silicon / oxide interface and is more dependent upon the channel concentration, surface electric field, and scattering.

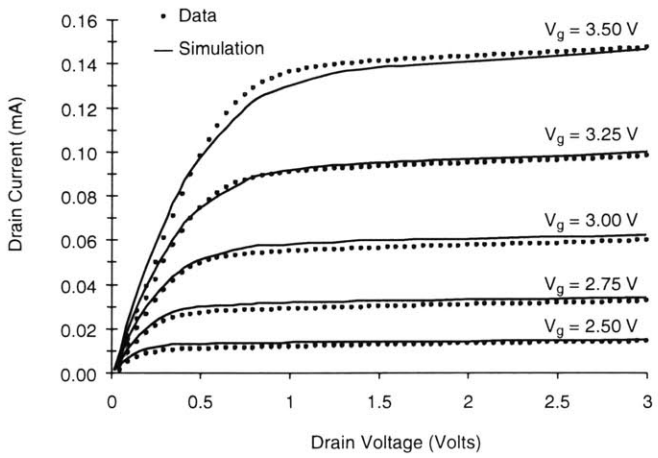


Figure 34. VMOS Drain Current Characteristics with Correction Effects

Good matching between device data and simulation was seen after series resistance corrections were added to the device model.

Some deviation was observed between simulated gate current characteristics and measured device values. This is though to be mainly due to series resistance in the device that was not present in the simulation model for the data shown in Figure 35. Another factor that may account for the lower simulated values could be a shorter effective channel length on the actual device caused by a gradual drop in doping concentration for the source and drain junctions. This would decrease the effective channel length in the device and result in higher output current.

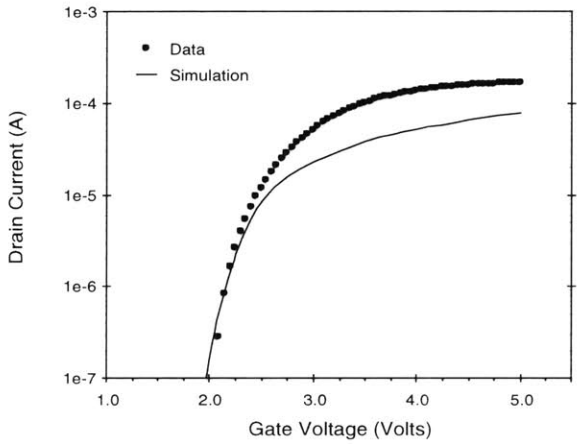


Figure 35. VMOS Gate Current Characteristics

As stated earlier, a graded doping distribution (lower doping at the source) will increase V_T along the device channel thereby increasing device pinch-off in the saturation regime. The resulting effect would be current saturation at a lower drain voltage (decreased V_{dsat}) causing a lower drain current characteristic. It was seen however, that the graded dopant distribution shown in (Figure 19) does not strongly impact the drain current characteristic. Figure 36 shows simulation results for a graded doping distribution versus a reverse-graded distribution. Typically an increase in current would be expected for the reverse-graded doping profile, as a more pronounced diffusion current would increase the total device current. In addition, the reverse-graded distribution would lower the threshold voltage at the drain (lower doping) thereby reducing the body effect and pinch-off condition. It was realized however, that while the ion-implanted doping distribution varies significantly in the VMOS body, the channel doping just below the gate oxide (Figure 28) is fairly uniform within the region of interest (i.e. the inversion layer thickness, ~100nm). This channel uniformity can likely be attributed to the non-uniform out-diffusion of the implanted boron dopant during formation of the thermally grown gate oxide. Since the diffusion rate is proportional to the gradient of the dopant concentration, there will be an increasing degree of dopant out-diffusion as one moves towards the top region of the pillar (Figure 19). This effect will result in a channel doping that is more uniform than the larger variation seen in the body doping. As can be seen, the drain characteristics are quite similar for both the graded and reverse-graded distributions (Figure 36).

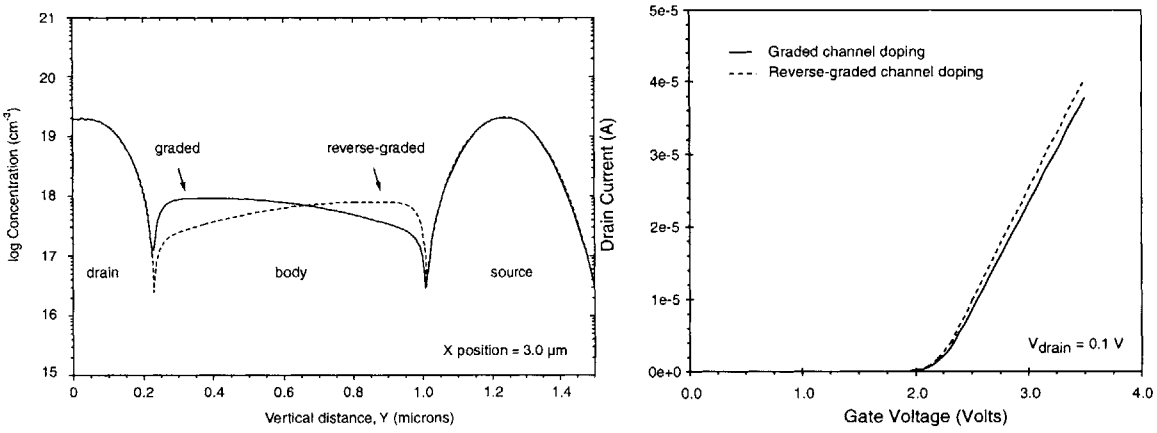


Figure 36. Impact of Graded Channel Doping on Drain Characteristic

VMOS drain characteristics for graded and reverse-graded doping simulations were seen to be highly similar. This indicates that the variation in doping distribution along the channel region does not vary significantly enough so that device performance is affected.

Chapter 6 - MOSFET / FEA Integration

6.1. Motivation and Applications

There are several reasons why we are seeking to integrate MOSFET and FEA structures. As outlined in this section, in order to obtain appreciable current density from a field emitter array (10-100μA), gate voltages of approximately 50-100 Volts are necessary. In device operation, the energy dissipated in switching is given by

$$E_{diss} \approx \frac{1}{2} C(\Delta V)^2$$

It is clear that lowering the switching threshold voltage will result in much reduced power consumption of the driver circuits. This voltage scaling is particularly effective in the case where several thousand devices that may be addressed in a matrix array (such as in a display application). Reducing the on-off switching voltage for a field emitter array can be accomplished by two distinct methods. The first possibility is to aggressively scale the field emitter tip dimensions such that field emission be induced at a much lower gate voltage (10-20 volts). Scaling the gate aperture surrounding the emitter tip will strongly increase the electric field at the tip surface. This will results in higher tunneling probability and consequently a higher emission current density (see Chapter 0).

The other option to reduce the FEA operating voltage is to tie a MOSFET device in series with the area. In this scenario the MOSFET acts as a switch to open or close a current loop between the field emitter array and ground potential. By holding the FEA gate electrode at a high potential, the MOSFET device acts a switching device. In addition, if the emission current is greater than the MOSFET drain current in the saturation regime, the MOSFET will act as a load and can function as a current limiting device for the FEA. This not only allows more stable device operation but may possibly extend FEA device lifetime as well. Figure 37 illustrates the integrated MOSFET / FEA current characteristics and operating principle.

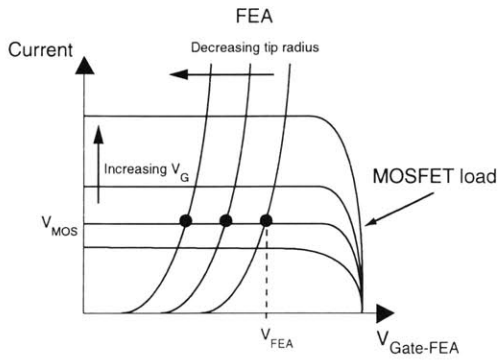


Figure 37. MOSFET and FEA current characteristics

The intersections of both curves represent points of stable device operation.

6.2. Requirements for VMOS / FEA Integration

Two approaches may be taken for creating integrated VMOS / FEA devices. A one-to-one method attempts to construct one field emitter device (FED) above each vertical MOSFET. The other approach utilizes one VMOS structure to address a field emitter array (FEA), essentially a one-to-many method. Both approaches are shown schematically in Figure 38. While the single FED approach is more conducive in studying the effects of the integrated system on a single field emitter, thereby reducing statistical variations that exist between emitter tips, two difficulties arise in this approach. The first and main obstacle is the requirement of current matching between the transistor switch and the emitting device.

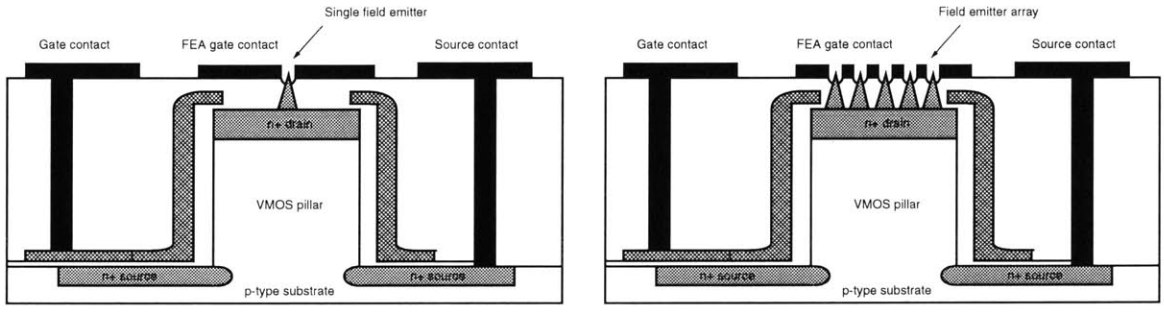


Figure 38. Approaches to VMOS / FEA Integration

Schematic representations of integrated devices using a (a) one-to-one or (b) one-to-many fabrication method.

As shown in Figure 37, in order to achieve a stable performance, both transistor and FEA current characteristics must intersect at a given operating voltage. In Chapter 0 it was seen that typical VMOS drain currents were on the order of 0.1 - 1.0μA for a 8μm diameter VMOS transistor. This corresponds to a VMOS W/L ratio of ~32 and a drain area of 50 μm^2. For the VMOS structures, the transistor channel length is determined by the pillar etch step (Figure 20) and diffusion of the drain implant (Figure 26). It is seen that the circumference of the silicon pillar determines the device width. Figure 39 shows total and normalized current characteristics of field emitter arrays tested in the laboratory [50]. While only a small percentage of devices are expected to be contributing to most of the emission current, it is clear that the current produced by a single emitter is on the order of 100nA.

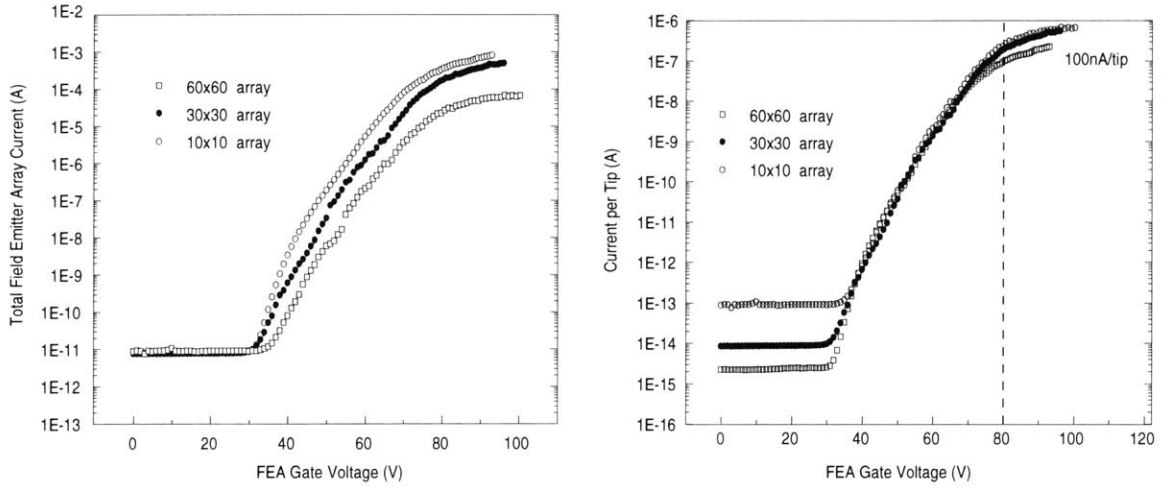


Figure 39. Typical FEA Current Characteristics

(a) Total and (b) normalized current for several field emitter array sizes [50].

To achieve current matching between the two devices, it is necessary to integrate many tips per transistor device. Assuming a fixed nominal emission current, the number of tips required to achieve a matching condition can be readily determined and is illustrated in Figure 40.

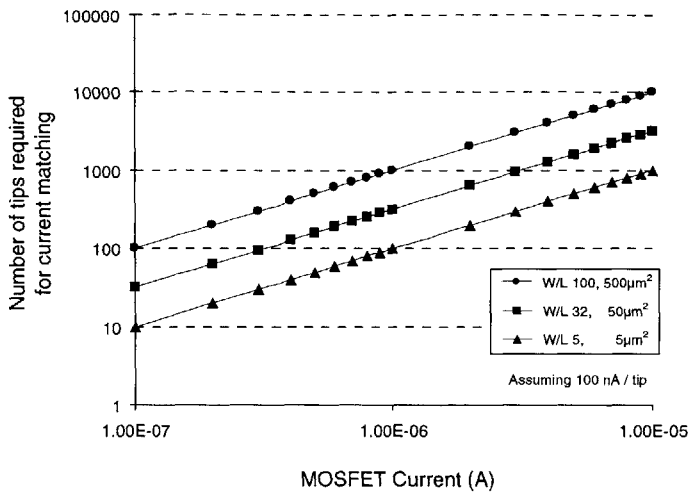


Figure 40. Required Number of Tips for Current Matching

Larger MOSFET W/L ratios will increase VMOS current thereby requiring a larger number of emitter tips to achieve a current matching condition. Since FEA area is dependent on pillar radius, drain area is shown as a function of the corresponding W/L ratio.

6.3. Fabrication Methods for VMOS / FEA Devices

In order to determine the feasibility of integrated VMOS / FEA devices, simulations were conducted for a process design flow. The device fabrication follows a similar sequence to the VMOS design outlined in Section 0 (Figure 18). Instead of depositing a metal contact layer as in the last VMOS process step, a deposition of n+ doped amorphous silicon or polycrystalline silicon is done followed by a CMP step. After the base silicon layer is completed, an oxide layer used to form a hardmask for the silicon FEA etch step (Figure 41b). For the tip density required for current matching, it will be necessary to use special techniques to form 100nm or 200nm period oxide caps. These techniques will be discussed in further detail below. The field emitter tips are then formed by an isotropic silicon etch in a plasma reactive ion etcher (Figure 46). A thermal oxidation sharpening step and oxide deposition are followed by an oxide etch to open contact vias to the VMOS gate and source regions (Figure 41c). A highly doped polysilicon layer is then deposited. The deposited film simultaneously forms the FEA gate VMOS source, and VMOS gate regions. The polysilicon undergoes CMP to open the FEA gate regions followed by a short HF dip to expose the FEA tips (Figure 42b). A final mask layer then is used to define and etch the FEA gate, VMOS gate, and VMOS source contacts (Figure 42c).

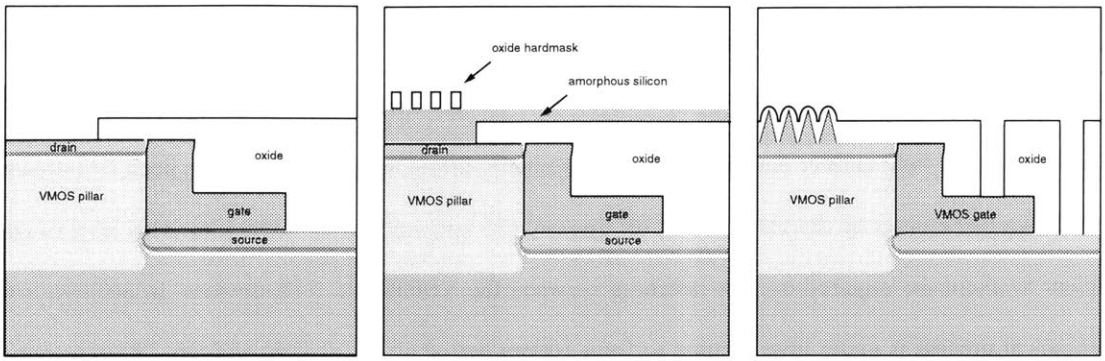


Figure 41. Integrated Process of FEA and VMOS Device

(a) VMOS pillar structure before metal deposition step, (b) deposition of amorphous silicon layer, CMP silicon layer, pattern and etch to form oxide hardmask, (c) etch field emitter tips, thermal oxidation sharpening and oxide etch to create VMOS gate and source via openings. Simulation plots are axially symmetric about the left vertical axis.

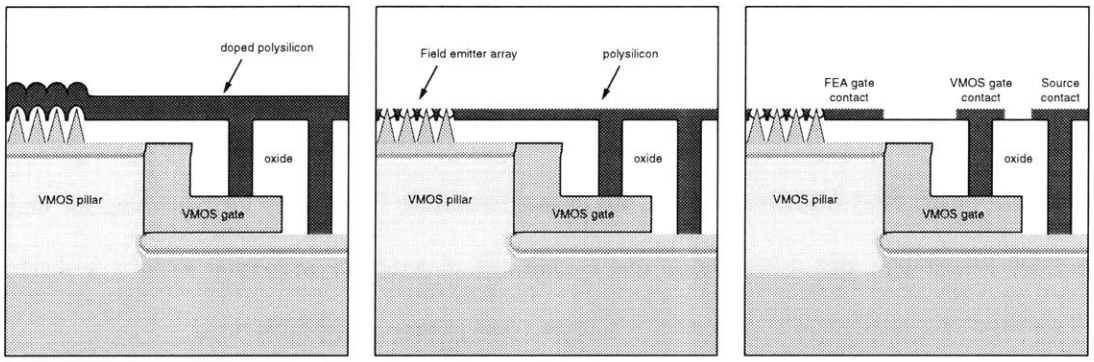


Figure 42. Integrated Process of FEA and VMOS Device

(a) Deposition of polysilicon for contact material, (b) CMP to create FEA gate openings, wet oxide etch to expose FEA tips (c) pattern and etch of polysilicon to form device contacts. Simulation plots are axially symmetric about the left vertical axis.

6.4. Fabrication Methods to Form Very High Density FEAs

In order to fabricate several hundred tips in conjunction with a single transistor device, three techniques are possible. The first and most simple approach is to create a lateral transistor whose W/L ratio is independent of the field emitter array area. This method is currently under investigation within the research group. In the case of a vertical transistor structure, the FEA area is constrained by the available region on the top drain of the VMOS structure (Figure 38b). For a VMOS device of radius r, the transistor width, given by $2\pi r$, and the top drain area, πr^2, are not

independent. We see from Figure 40, that for a nominal device with W/L of 32, a drain area of $50\mu m^2$ must accommodate approximately 500 emitter tips are required to realize current matching for a 50μA MOSFET device. Aggressive scaling of field emitter devices using interferometric lithography techniques has been investigated and it has been shown that emitter tip densities of $2.5x10^9$ tips/cm^2 (25 tips/μm^2) are possible [26]. This level of tip density is sufficient to attain the required current matching between the VMOS and FEA devices. In addition a maskless electrochemical process is under investigation to form 100nm period arrays of field emitters. Both techniques will be outlined below.

6.4.1. INTERFEROMETRIC LITHOGRAPHY

To reach tip densities of $2.5x10^9$ tips/cm^2, field emitter devices of a 200nm period must be fabricated. These small dimensions are typically beyond the capabilities of standard lithography exposure tools. By using an interferometric lithography process, it is possible to fabricate field emitter arrays with a 200nm period between individual field emitter tips.

The grid pattern of the FEA lends itself to the use of interferometric lithography for patterning the emitter tips. Interferometric lithography uses a laser beam that is split and re-combines with itself to form a standing wave pattern. Two exposures orthogonal to each other will form a post pattern in a positive resist.

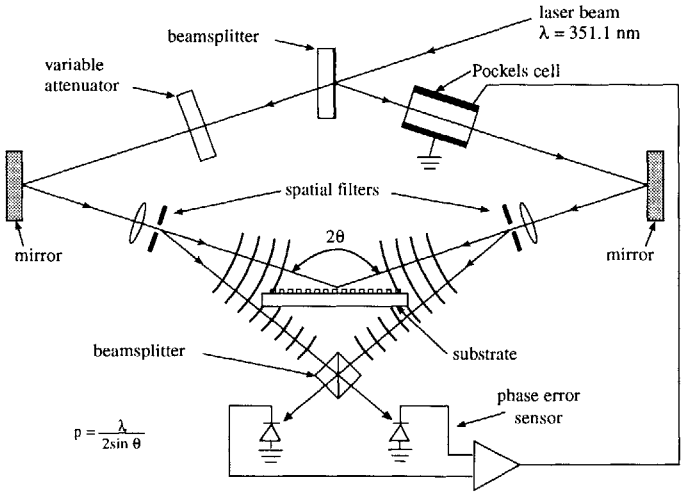


Figure 43. Schematic of Interferometric Lithography System

Fringes are spatially stabilized by means of a feedback loop on the Pockels cell.

A 351.1 nm wavelength argon laser is used to form a 200 nm period standing wave. The recombination angle for this period grating is $\theta = 61.37°$ as per:

$$p = \frac{\lambda}{2\sin\theta}$$

In order to achieve the high contrast patterning with the interferometric lithography an anti-reflective coating (ARC) was used when the wafer was exposed. This layer serves to minimize reflections from the substrate back into the photoresist, thereby ensuring good pattern transfer.

To prepare VMOS samples for interferometric lithography (IL) exposure, an oxide layer was deposited before the CMP processing step described earlier (see Figure 24). The subsequent chemical polish resulted in an exposed silicon surface (VMOS drain region) surrounded by the deposited oxide. At this stage a thin oxide was thermally grown on the top surface of the exposed silicon and the tri-level layer was spun on. The purpose of the oxide layer is to act as an etch hardmask for the silicon field emitter devices. After preparation, the wafers were exposed using the interferometric lithography system (Figure 43). Each wafer was exposed twice, with the wafer rotated 90° between each exposure to form the post array pattern. Each exposure was done at approximately 18.5 mJ/exposure. Figure 44 shows the photoresist posts after exposure and developing.

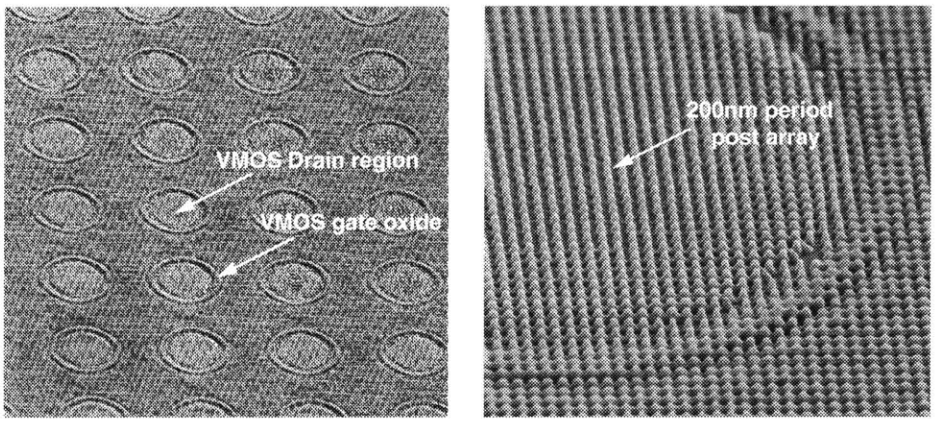


Figure 44. Developed Posts on Top of VMOS Pillar Arrays

Photoresist exposure of interferometric lithography pattern.

As can be seen, the post patterns resolved much more clearly on the circular silicon regions than on the surrounding oxide layer. This was expected as the thickness of the tri-level resist layer was designed to minimize surface reflections off of a silicon substrate and not an oxide layer. While interferometric lithography has been utilized in previous works [26], this may be the first time its use has been demonstrated on highly non-planar surfaces. To transfer the photoresist pattern into the underlying oxide layer, the tri-level structure was etched in a reactive ion etcher using a CHF_3 and O_2 plasma chemistry. Figure 45 shows the sub-100 nm diameter caps of SiO_2 that will be subsequently used as an etch mask for the field emitter tips.

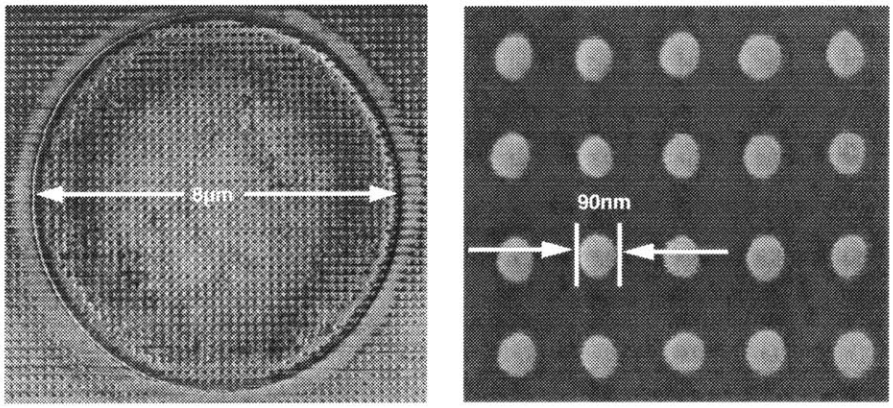


Figure 45. Pattern Transfer to Form 100nm Oxide Posts

Post-etch processing show good pattern transfer of 200nm period post arrays formed by interferometric lithography.

While these structures have not been fully processed with the integrated VMOS transistor as of this writing, 200nm period field emitter arrays have been fabricated on silicon substrates by Dr. David G. Pflug [26]. The processing steps are similar to those outlined above. After the oxide post formation, an isotropic silicon etch is used to form tip arrays (Figure 46a).

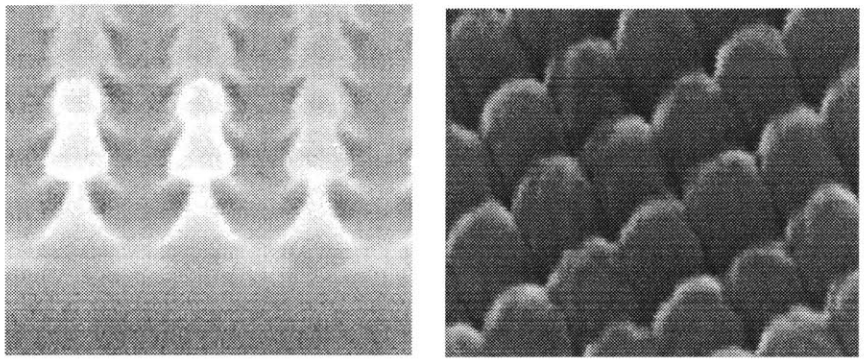


Figure 46. Formation of Si Emitter Tips and Polysilicon Deposition

(a) Rough shape of the silicon cone is a function of the lateral and vertical etch rate, tip sharpening is accomplished by a thermal oxidation step. (b) The conformal polysilicon surface will be planarized to expose the tips and create gate apertures [26].

The oxide caps are then removed in a hydrofluoric solution and a thin thermal oxide is grown to sharpen the emitter tips. Conformal oxide and polysilicon layers are the deposited (Figure 46b). Finally the polysilicon layer is polished in a CMP step to form the field emitter gate aperture. A second hydrofluoric dip is used to remove a small amount of the deposited oxide thereby exposing the silicon emitter tips. Figure 47 shows completed arrays of 200nm period silicon field emitter tips.

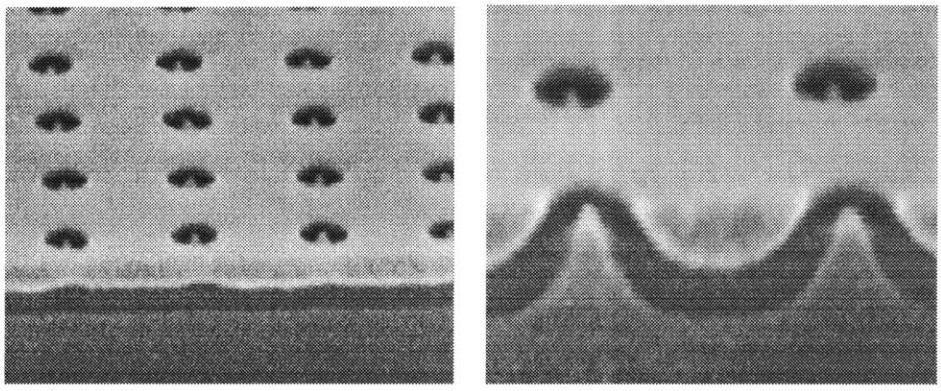


Figure 47. Fabricated 200nm Period Silicon Field Emitter Arrays

Final fabricated arrays of silicon field emitters with 200nm pitch and 80nm gate aperture [26].

6.4.2. SELF-ORDERED PERIODIC ARRAYS THROUGH ELECTROCHEMICAL PROCESSING

A second approach to fabricating high-density field emitter arrays was also investigated. Due to the complexity of the interferometric lithography system and it high sensitivity to exposure and substrate film conditions a non-lithographic electrochemical process was explored. In this method, chemical anodization of a thermally deposited aluminum film creates a self-ordered periodic array of hexagonal cells. The goal of this technique is to use the periodic array as a pattern transfer layer to form oxide caps for field emitter array formation (Figure 48, Figure 49).

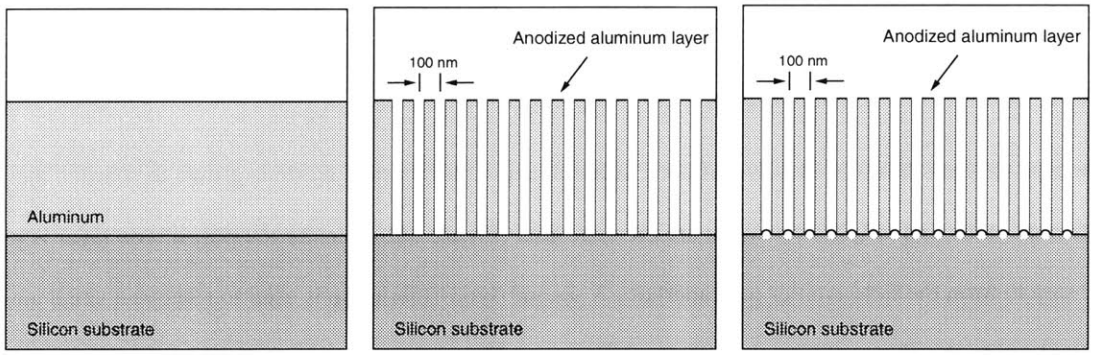


Figure 48. Process Sequence to Create 100nm Period Field Emitter Tip Arrays

(a) Thermal deposition of aluminum of silicon substrate, (b) electrochemical anodization of aluminum to form 100nm periodic arrays, (c) thermal oxidation of silicon to form oxide caps.

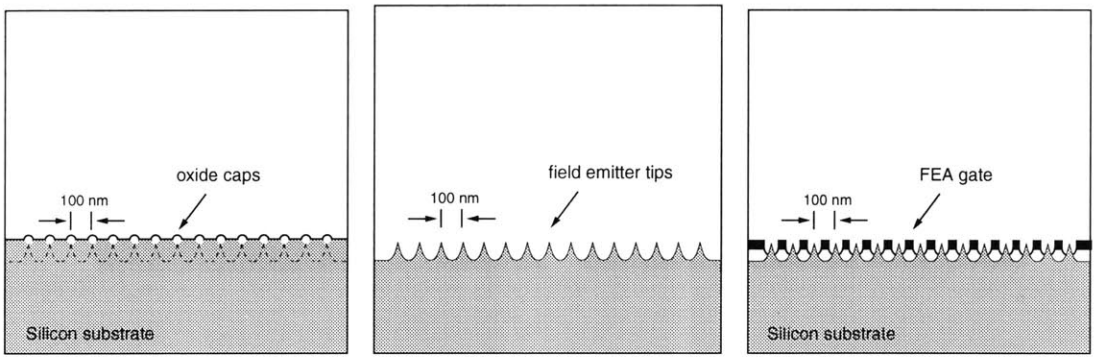


Figure 49. Process Sequence to Create 100nm Period Field Emitter Tip Arrays

(a) Wet etch of aluminum oxide layer, (b) isotropic plasma etch to form silicon field emitter tips, (c) deposition of polysilicon FEA gate, CMP, and wet oxide etch to expose emitter tips.

Self-ordered pore formation from aluminum anodization has been studied and has several possible applications ranging from nano-fabrication [51,52] to photonic crystals [53]. While theoretical frameworks have been proposed to explain the exact chemical reaction and formation mechanisms [54], the physical process is not completely understood as of this writing. In addition, most work has used blank aluminum sheets to form the periodic array structures. In this work however, formation of self-ordering periodic structures have been demonstrated on silicon substrates. This advancement is highly beneficial to several possible further applications that may be integrated with existing CMOS processes. Electron micrographs of the self-formed arrays are shown in Figure 50. While further processing is required to form oxide caps and field emitter tips the current progress to date is highly encouraging.

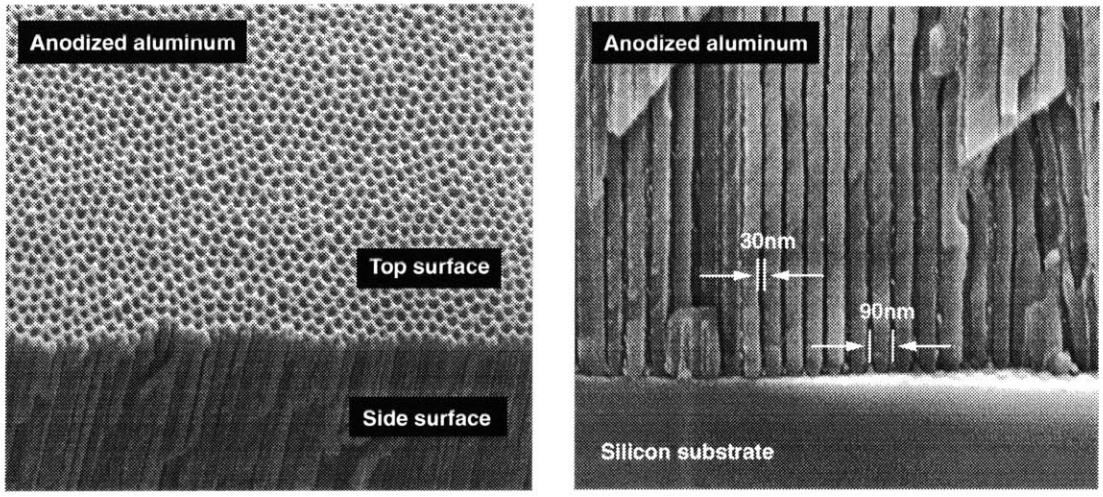


Figure 50. Self-ordered 100nm Periodic Pores Arrays on Silicon

Fabricated arrays show hexagonal packing with 30nm pore diameter and 90nm pore spacing.

Chapter 7 – Conclusions

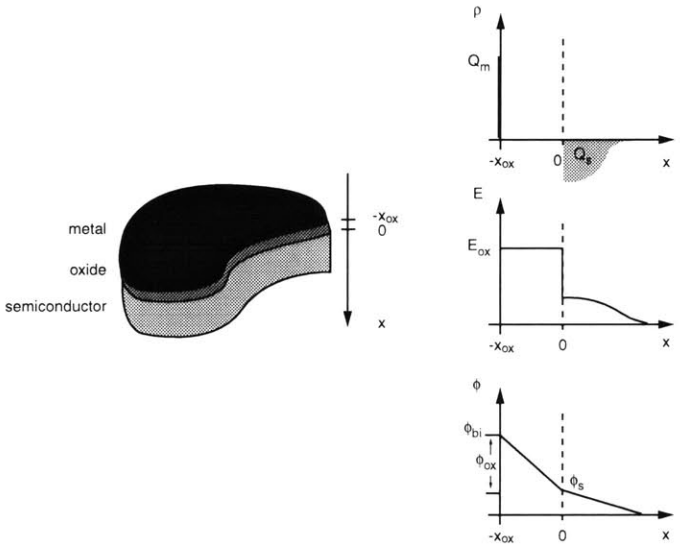
Integration of FEA and MOSFET device structures has been explored as a means to provide greater device stability as well as low voltage switching control. A process to create a vertical MOSFET device was simulated and verified. Vertical MOSFET devices were fabricated and tested in the Integrated Circuits Laboratory at MIT. Models to describe the physical and electrical device characteristics were developed and showed very good agreement with both analytical and numerical simulation results. Through process simulation, integration of vertical MOSFET devices and high density field emitter arrays was shown to be feasible.

To create integrated MOSFET / FEA devices it was determined that a high field emitter array density was required to reach a current matching condition for the desired device operation. In order to achieve emitter densities greater than $1x10^9$ tips/cm^2, two possible methods were explored. The first method involved using an interferometric lithography system to form period arrays of field emitter tips. Fabrication capability of FEAs with packing density of greater than of $2.5x10^9$ tips/cm^2 was demonstrated through the use of interferometric lithography techniques. A second approach to create very high density emitter arrays was also investigated. Using maskless, electrochemical processing, periodic array formation with spacings of <100nm was demonstrated. The self-forming arrays showed the possibility of reaching even higher FEA device packing densities on the order of $1x10^{10}$ tips/cm^2. The electrochemical process, in addition to being maskless, provided much larger across-wafer uniformity and the ability to selectively pattern specified substrate areas.

Several possible applications of the integrated VMOS / FEA devices are possible and may be investigated further. Some of these include low-voltage, matrix-addressable field emission displays, photosensitive detectors, and microwave amplifiers. Further work into optimizing VMOS / FEA design and theoretical analysis is also anticipated.

Appendix A: Electrostatic Analysis of MOS Structure

There are several basic relations that can be used to describe the MOS structure that will be correlated the field emitter system. These relationships describe the charge distribution and electric fields within the structure and when modified appropriately, can be used for non-equilibrium conditions as well. A very succinct analysis has been done [27] and will be used to present an analytical solution to the MOS system. The figure below shows a schematic of a MOS structure and the associated charge distribution, electric field, and electrical potential within the semiconductor material.



MOS Structure

Charge density, electric field, and electric potential as a function of distance are shown. If the silicon and metal work functions are equal, the built-in potential, ϕ_{bi} will be zero.

Applying Gauss' law to a region that encloses the entire semiconductor charge Q_s it is seen that the electric field within the oxide region is

$$\mathcal{E}_{ox} = -\frac{Q_s}{\varepsilon_{ox}}$$

In addition, since the dielectric constants of the oxide and silicon are different we have that

$$\varepsilon_{ox}\mathcal{E}_{ox} = \varepsilon_{si}\mathcal{E}_{s}$$

giving

$$\mathcal{E}_{s} = -\frac{Q_s}{\varepsilon_{si}}$$

for the electric field at the semiconductor surface. The potential drop across the surface ϕ_{bi} (the difference in work function between the metal and semiconductor materials) is equal to

$$\begin{aligned}\phi_{bi} &= \phi_s + \phi_{ox} \\ &= \phi_s + x_{ox}\mathcal{E}_{ox} \\ &= \phi_s - \frac{Q_s x_{ox}}{\varepsilon_{ox}} = \phi_s - \frac{Q_s}{C_{ox}}\end{aligned}$$

If a voltage V is applied to the metal surface the equation is modified to

$$\phi_{bi} + V = \phi_s - \frac{Q_s}{C_{ox}}$$

To solve more rigorously for an electrostatic bias condition, a Poisson-Boltzmann formulation was followed to determine the electric charge, potentials and fields within the silicon device. For a uniformly doped n-type semiconductor the charge density can be expressed as

$$\rho = q(n - p - N_d)$$

Where p and n are the carrier densities, N_d is the dopant concentration, and q is the electronic charge. With this charge density Poisson's equation for electrostatic potential is then

$$\frac{d^2\phi}{dx^2} = -\frac{q}{\varepsilon_{Si}}(n - p - N_d)$$

Since the oxide layer between the silicon and metal surfaces prevents current flow, the semiconductor is in equilibrium and the relation $np = n_i^2$ holds. For this situation Boltzmann statistics may be applied and the carrier concentrations can be expressed as

$$n = n_o \exp(\frac{q\phi}{kT}) \approx N_d \exp\left(\frac{q\phi}{kT}\right)$$
$$p = p_o \exp(\frac{-q\phi}{kT}) \approx \frac{n_i^2}{N_d} \exp\left(-\frac{q\phi}{kT}\right)$$

where n_o and p_o are the electron and hole concentrations in the bulk and the potential deep within the bulk is taken to be zero. This assumes that most donor sites are fully ionized such that $n_o \sim N_d$, which is valid at room temperature or above. In the bulk, charge neutrality demands that

$$n_o - p_o - N_d = 0$$

Combing the above four results yields the Poisson-Boltzmann equation for the electrostatic potential,

$$\frac{d^2\phi}{dx^2} = -\frac{qN_d}{\varepsilon_{Si}}\left[\left(\exp\left(\frac{q\phi}{kT}\right)-1\right)-\frac{n_i^2}{N_d{}^2}\left(\exp\left(-\frac{q\phi}{kT}\right)-1\right)\right]$$

Going through the mathematical analysis (Appendix A), boundary conditions for the surface electric potential can be solved for and a self-consistent expression for the electric potential can be reached. Once the electric potential as a function of distance is known the electric field and semiconductor charge can be solved for from the equations

$$\mathcal{E} = -\frac{d\phi}{dx} = \sqrt{\frac{2kTN_d}{\varepsilon_{Si}}}\ F(\phi)$$

and

$$Q_e = -qN_d \int_0^\infty \exp\left(-\frac{q\phi}{kT}\right)-1\ dx$$
$$Q_h = q\frac{n_i^2}{N_d}\int_0^\infty \exp\left(\frac{q\phi}{kT}\right)-1\ dx$$

Using the mathematical identity that

$$\frac{d^2\phi}{dx^2}\left(2\frac{d\phi}{dx}\right)=\frac{d}{dx}\left(\frac{d\phi}{dx}\right)^2$$

the Poisson-Boltzmann equation can be re-written as

$$\frac{d}{dx}\left(\frac{d\phi}{dx}\right)^2=-\frac{2qN_d}{\varepsilon_{Si}}\left[\left(\exp\left(\frac{q\phi}{kT}\right)-1\right)-\frac{n_i^2}{N_d{}^2}\left(\exp\left(-\frac{q\phi}{kT}\right)-1\right)\right]\frac{d\phi}{dx}$$

The equation can then be integrated from within the bulk region at $x=\infty$ to some point x in the surface (where $x=0$ is the oxide-silicon interface) such that

$$\int_\infty^x \frac{d}{dx}\left(\frac{d\phi}{dx}\right)^2 dx=-\frac{2qN_d}{\varepsilon_{Si}}\int_\infty^x\left[\left(\exp\left(\frac{q\phi}{kT}\right)-1\right)-\frac{n_i^2}{N_d{}^2}\left(\exp\left(-\frac{q\phi}{kT}\right)-1\right)\right]\frac{d\phi}{dx}dx$$

$$\left(\frac{d\phi}{dx}\right)^2\Bigg|_x-\left(\frac{d\phi}{dx}\right)^2\Bigg|_\infty=-\frac{2qN_d}{\varepsilon_{Si}}\int_0^\phi\left[\left(\exp\left(\frac{q\phi}{kT}\right)-1\right)-\frac{n_i^2}{N_d{}^2}\left(\exp\left(-\frac{q\phi}{kT}\right)-1\right)\right]d\phi$$

$$\left(\frac{d\phi}{dx}\right)^2=\frac{2kTN_d}{\varepsilon_{Si}}\left[\left(\exp\left(\frac{q\phi}{kT}\right)-\frac{q\phi}{kT}-1\right)+\frac{n_i^2}{N_a{}^2}\left(\exp\left(-\frac{q\phi}{kT}\right)+\frac{q\phi}{kT}-1\right)\right]$$

A first-order differential equation for the electrostatic potential can now be expressed as

$$\frac{d\phi}{dx}=-\sqrt{\frac{2kTN_d}{\varepsilon_{Si}}}\left[\left(\exp\left(\frac{q\phi}{kT}\right)-\frac{q\phi}{kT}-1\right)+\frac{n_i^2}{N_d{}^2}\left(\exp\left(-\frac{q\phi}{kT}\right)+\frac{q\phi}{kT}-1\right)\right]^{\frac{1}{2}}$$
$$=-\sqrt{\frac{2kTN_d}{\varepsilon_{Si}}}\,F(\phi)$$

To obtain the electrical potential as a function of distance, one further integration must be carried out. Namely

$$\int_{\phi_x}^{\phi}\frac{d\phi}{F(\phi)}=-\sqrt{\frac{2kTN_d}{\varepsilon_{Si}}}\,x$$

While this integration is rather difficult to perform analytically it is possible to solve numerically to obtain $\phi(x)$. From this result, it can be seen that the electric field is then

$$\mathcal{E} = -\frac{d\phi}{dx} = \sqrt{\frac{2kTN_d}{\varepsilon_{Si}}}\, F(\phi)$$

In addition the semiconductor charge due to electron and hole concentrations can be expressed as

$$Q_e = -qN_d \int_0^\infty \exp\left(-\frac{q\phi}{kT}\right) - 1 \; dx$$

$$Q_h = q\frac{n_i^2}{N_d} \int_0^\infty \exp\left(\frac{q\phi}{kT}\right) - 1 \; dx$$

Changing variables from x to ϕ gives

$$Q_e = q\sqrt{\frac{q^2\varepsilon_{Si}N_d}{2kT}} \int_{\phi_s}^0 \frac{e^{\frac{q\phi}{kT}} - 1}{F(\phi)} d\phi$$

$$Q_h = -q\frac{n_i^2}{N_d{}^2}\sqrt{\frac{\varepsilon_{Si}}{2kTN_d}} \int_{\phi_s}^0 \frac{e^{\frac{q\phi}{kT}} - 1}{F(\phi)} d\phi$$

A relationship between the surface potential ϕ_s and the applied voltage V can be obtained by combining the above equations to yield

$$V = -\phi_{bi} + \phi_s - \frac{\sqrt{2\varepsilon_{si}kTN_d}}{C_{ox}} F(\phi_s)$$

This equation is instrumental in that for a given voltage, this equation can be solved numerically to yield the boundary condition value of ϕ_s. After this value is found, all other semiconductor parameters such as charge distribution, electric field and carrier concentrations can be determined. From these results, the modification to the semiconductor work function, namely $(E_c\text{-}E_f)$ can be accounted for in the calculation of the electron supply function $N(E_x)$.

Appendix B: Matlab Electrostatic Simulation Code

nmosfet.m

```
% solve MOSFET Poisson-Boltzman equation
% [x,y] = ODE45('F',xspan,ic)
% integrate y' = F(x,y) from time x0 to xFINAL with initial conditions ic.

clear
figure(1); clf; figure(2); clf; figure(3); clf; figure(4); clf; figure(5);
clf
global q k eox esi T Na NC xox ni Wm
global V phi_s

%%%%%%%%%%%          constants          %%%%%%%%%%%%%

t=0;j=0;i=0;
k=8.61834e-5;      % eV/K
q=1.602e-19;       % C
esi=11.9*8.854188e-12;  % F/m
eox=3.9*8.854188e-12;   % F/m
T=300;             % K
Na=6e23;    % m-3
xox=190e-10;       % m
ni=1.07e16;        % must be changed if T changes
NC=3.1e25;  % m-3
NV=1e25;
Wm=4.04;    % eV, aluminum = 4.04eV

styles = {'b-' 'k-' 'r-' 'b-' 'b-' 'k-' 'r-' 'b-' 'b-' 'k-' 'r-' 'b-' 'k-'
'b-' 'k-' 'r-' 'b-' 'b-' 'k-' 'r-' 'b-' 'b-' 'k-' 'r-' 'b-' 'k-' 'b-' 'k-'
'r-' 'b-' 'b-' 'k-' 'r-' 'b-' 'b-' 'k-' 'r-' 'b-' 'k-' 'b-' 'k-' 'r-' 'b-'
'b-' 'k-' 'r-' 'b-' 'b-' 'k-' 'r-' 'b-' 'k-' 'b-' 'k-' 'r-' 'b-' 'b-' 'k-'
'r-' 'b-' 'b-' 'k-' 'r-' 'b-' 'k-' 'b-' 'k-' 'r-' 'b-' 'b-' 'k-' 'r-' 'b-'
'b-' 'k-' 'r-' 'b-' 'k-'};
styles2 = {'b--' 'k--' 'r--' 'b--' 'b--' 'k--' 'r--' 'b--' 'b--' 'k--' 'r--'
'b--' 'b--' 'b--' 'k--' 'r--' 'b--' 'b--' 'k--' 'r--' 'b--' 'b--' 'k--' 'r--'
'b--' 'b--' 'b--' 'k--' 'r--' 'b--' 'b--' 'k--' 'r--' 'b--' 'b--' 'k--' 'r--'
'b--' 'b--' 'b--' 'k--' 'r--' 'b--' 'b--' 'k--' 'r--' 'b--' 'b--' 'k--' 'r--'
'b--' 'b--' 'b--' 'k--' 'r--' 'b--' 'b--' 'k--' 'r--' 'b--' 'b--' 'k--' 'r--'
'b--' 'b--' 'b--' 'k--' 'r--' 'b--' 'b--' 'k--' 'r--' 'b--' 'b--' 'k--' 'r--'
'b--' 'b--'};

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

x0 = 0;
xfinal = 1e-7;
ic = 1;                 % initial guess
```

```
%Vval0 = -2: 0.2 : 5;
%Vvals = [0, Vval0];
Vvals = [0, -2, 3];           % V = 50 V, xox=190A gives n = 1e20 cm-3
                        %     E = 1e7 V/cm (field emission)
for V = Vvals
      t=t+1;
      ic = fzero('icF',ic);   % Solve for initial condition Phi_s
      phi_s = ic;
      xspan = [x0 xfinal];

      [x,phi] = ode45('F',xspan,ic);            % phi(i) = phi(x)

      figure(1)
      plot(x,phi,char(styles(t)))
      xlabel ('Distance into semiconductor (m)')
      ylabel ('Potential (Phi(V))')
      hold on
      zoom on

%%%%%%%%%%%%%%%% Fill in F_phi solutions  %%%%%%%%%%%%%%%

      for j=1 : size(x,1)
            F_phi(j)=(phi(j)/abs(phi(j)))*sqrt((exp(-1*phi(j)/(k*T))+phi
            (j)/(k*T)-1)+(ni^2/Na^2)*(exp(phi(j)/(k*T))-phi(j)/(k*T)-1));
      end

%%%%%%%%%%%%%%%% Plot E field       %%%%%%%%%%%%%%%%%%
      E = sqrt(2*k*T*q*Na/esi) * F_phi;
      figure(2)
      plot(x,E/100,char(styles(t)))
      xlabel ('Distance into semiconductor (m)')
      ylabel ('Electric Field (V/cm)')
      hold on
      zoom on

%%%%%%%%%% Plot electron concentration      %%%%%%%%%
      n = (ni^2/Na)*exp(phi/(k*T));
      figure(3)
      semilogy(x,n/1e6,char(styles(t)))
      xlabel ('Distance into semiconductor (m)')
      ylabel ('Electron concentration (cm-3)')
      hold on
      zoom on
      nconc(t)=n(1)/1e6;
      nconc2(t)=log(n(1)/1e6);
%%%%%%%%%% Plot hole concentration      %%%%%%%%%
      p = Na*exp(-phi/(k*T));
      figure(4)
      semilogy(x,p/1e6,char(styles2(t)))
      xlabel ('Distance into semiconductor (m)')
      ylabel ('Hole concentration (cm-3)')
      hold on
      zoom on
      pconc(t)=p(1)/1e6;
      pconc2(t)=log(p(1)/1e6);
%%%%%%%%%% Plot energy bands      %%%%%%%%%
```

```
      offset = 1.124/2;
      Ec = 1.124 - phi-offset;
      Ev = Ec-1.124;
      figure(5)
      hold on
      if V==0                          % plot equilibrium Ef in bulk
            Ei = (Ec+Ev)/2;
            phi_p = k*T*log(Na/ni);
            Efp = Ei - phi_p; %  Fermi level in bulk
            Efp2 = zeros(size(Efp,1),1); Efp2(:,1) = max(Efp);
            plot (x,Efp2,'k--')
      end
      if t==size(Vvals,2)                % plot inversion Ei
            Ei = (Ec+Ev)/2;
%           plot (x,Ei, 'r--')

      end
      plot(x,Ec,char(styles(t)))
      plot(x,Ev,char(styles(t)))
      xlabel ('Distance into semiconductor (nm)')
      ylabel ('Energy (eV)')
      zoom on

      clear F_phi % must clear since x range will differ on new solution
      Naval(t)= log(Na/1e6);
end


figure(7)
clf
hold on
plot (Vvals(1,2:size(Vvals,2)),nconc2(1,2:size(Vvals,2)),'r-')
plot (Vvals(1,2:size(Vvals,2)),pconc2(1,2:size(Vvals,2)),'b-')
plot (Vvals(1,2:size(Vvals,2)),Naval(1,2:size(Vvals,2)),'k-')
xlabel('Gate Voltage (Volts)')
ylabel ('log Carrier concentration (cm-3)')
zoom on
```

F.m

```
% Solve for electric potential phi
%TO BE USED [t,Y]=ode45('function',tspan,ic)

function F_phi=function1(x,phi)

global q k eox esi T Na NC xox ni Wm
global V

F_phi=-1*(sqrt(2*k*T*q*Na/esi))*(phi/abs(phi))*sqrt((exp(-
1*phi/(k*T))+phi/(k*T)-1)+(ni^2/Na^2)*(exp(phi/(k*T))-phi/(k*T)-1));
```

icF.m

```
% Solves initial condition for F(phi) as a function of applied voltage (V)
% finds zero of function b
% to be used from ic=fzero('icF',y0)    y0 = intitial guess

function b=function0(phi)

global q k eox esi T Na NC xox ni Wm
global V


b=-1*(sqrt(2*k*T*q*Na*esi))*(phi/abs(phi))*sqrt((exp(-1*phi/(k*T))+phi/(k*T)-
1)+(ni^2/Na^2)*(exp(phi/(k*T))-phi/(k*T)-1)) * xox/eox-k*T*log(ni^2/(Na*NC))-
phi+V;
```

Qex.m

% solves foe charge distribution as a function of x within the semiconductor material

```
clear

global q k eox esi T Na NC xox ni Wm
global V
%%%%%%%%%%%          constants          %%%%%%%%%%%%%

t=0;
k=8.61834e-5;
q=1.602e-19;
esi=11.9*8.854188e-12;
eox=3.9*8.854188e-12;
T=300;              % K
Na=6e23;     % m-3
xox=45e-10;         % m
ni=1.07e16;         % must be changed if T changes
NC=3.1e25;   % m-3
Wm=4.04;     % eV, aluminum = 4.04eV

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

ic=1; % ic = phi_s  boundary condition

Vsteps = -2 : 0.1: 2;

for V= Vsteps
      t=t+1;
      ic=fzero('icF',ic);
      icval(t)=ic;
      Vval(t)=V;
      phi_s=ic;

      integral=0;              %  do Qh integral peicewise
      if ic>0
            for phi=0:ic/200:ic;
                  val = intQe(phi);
                  integral=integral-ic*val/201;
            end
      else
            for phi=0:ic/200:ic;
                  val = intQe(ic+phi);
                  integral=integral+ic*val/201;
            end
      end

      Qe(t)=integral;
      Vt(t)=V;
end
Qeo=Qe/1e4;
```

```
figure(3)
clf
plot(Vt,Qeo,'k--')

t=0
for V= Vsteps
      t=t+1;
      ic=fzero('icF',ic);
      icval(t)=ic;
      Vval(t)=V;
      phi_s=ic;

      integral=0;             %  do Qh integral peicewise
      if ic>0
            for phi=0:ic/200:ic;
                  val = intQh(phi);
                  integral=integral-ic*val/201;
            end
      else
            for phi=0:ic/200:ic;
                  val = intQh(ic+phi);
                  integral=integral-ic*val/201;
            end
      end

      Qh(t)=integral;
      Vt(t)=V;
end
Qho=Qh/1e4;
figure(3)
hold on
plot(Vt,Qho,'r--')
xlabel ('V [V]')
ylabel ('|Qh| [C/cm^2]')

Qso = Qeo+Qho;
plot(Vt,Qso,'b-')
```

intQe.m

```
% electron charge integration function for Qex.m

function a = functionQe(phi)

global q k eox esi T Na NC xox ni Wm
global V

if sign(phi) == 0
      a=0;
else
      if sign(phi)>0


a=(q*ni^2/Na)*sqrt(esi/(2*k*T*q*Na))*(exp(phi/(k*T))-1)/sqrt((exp(-
1*phi/(k*T))+phi/(k*T)-1)+(ni^2/Na^2)*(exp(phi/(k*T))-phi/(k*T)-1));

      end

      if sign(phi)<0

a=-1*(q*ni^2/Na)*sqrt(esi/(2*k*T*q*Na))*(exp(phi/(k*T))-1)/sqrt((exp(-
1*phi/(k*T))+phi/(k*T)-1)+(ni^2/Na^2)*(exp(phi/(k*T))-phi/(k*T)-1));

      end
end
```

intQh.m

```
% hole charge integration function for Qex.m

function a = functionQh(phi)

global q k eox esi T Na NC xox ni Wm
global V

if sign(phi) == 0
      a=0;
else
      if sign(phi)>0


a=-1*sqrt(esi*q^2*Na/(2*q*k*T))*(exp(-1*phi/(k*T))-1)/sqrt((exp(-
1*phi/(k*T))+phi/(k*T)-1)+(ni^2/Na^2)*(exp(phi/(k*T))-phi/(k*T)-1));

      end

      if sign(phi)<0

a=sqrt(esi*q^2*Na/(2*q*k*T))*(exp(-1*phi/(k*T))-1)/sqrt((exp(-
1*phi/(k*T))+phi/(k*T)-1)+(ni^2/Na^2)*(exp(phi/(k*T))-phi/(k*T)-1));

      end
end
```

mosiv.m

```
% calculates and plots ideal MOSFET IV characteristics
clear

%%%%%%%%%%          constants          %%%%%%%%%%%%

k=8.61834e-5;
q=1.602e-19;
esi=11.9*8.854188e-12;
eox=3.9*8.854188e-12;
T=300;              % K
Na=2.3e23;          % m-3
xox=40e-10;         % m
ni=1.07e16;         % must be changed if T changes
Wm = 4.1;    % eV  aluminum
X = 4.04;    % eV  Si electron affinity
Eg = 1.124; % eV
Ws = X + Eg + (k*T)*log(Na/ni);

styles = {'b-' 'k-' 'r-'};
styles2 = {'b--' 'k--' 'r--'};
styles3 = {'b-' 'k.-' 'r--'};
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

mu=500e-4;
W = 25.1; % um
L = 0.78;  % um

phi_f = (2*k*T)*log(Na/ni);
Cox = eox/xox;
Vfb = Ws-Wm  % eV

t=0;k=0;
Vrange = [2.5 2.75 3 3.25 3.5];
for Vg = Vrange
k=k+1;
      for Vd = 0 : .1: 3
      t=t+1;
      Id(t,k) = (W/L)*mu*Cox*((Vg-2*phi_f-Vd/2)*Vd-
(2/3)*(sqrt(2*esi*q*Na)/Cox)*((Vd+2*phi_f)^1.5-(2*phi_f)^1.5));
      Vdval(t) = Vd;
      VT = Vfb + (1/Cox)*sqrt(2*esi*q*Na*2*phi_f)+2*phi_f;
      end
t=0;
end
VT

for j= 1: size(Vrange,2)
      maxId(j) = max(Id(:,j));
      for t=1 : size(Id,1)
            if Id(t,j) == maxId(j)
```

```
                for k= t : size(Id,1)
                      Id(k,j) = maxId(j);
                end
            end
      end
end

Id = 100*Id;        % convert to mA

figure(1)
clf
hold on
for t = 1 : size(Vrange,2)
plot (Vdval,Id(:,t),'k-')
end
xlabel ('Drain voltage (V)')
ylabel ('Drain current (mA)')
zoom on
grid on

max(max(Id))
```

xdep.m

```
% calculates depletion width of p-type Si
%     under inversion as a function of doping

clear

%%%%%%%%%%     constants    %%%%%%%%%%%
kT= 25.86e-3;      % eV
q=1.602e-19; % C
esi=11.9*8.854188e-12; % F/m
eox=3.9*8.854188e-12; % F/m
ni=1.07e16;        % cm-3

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

k=0;
for Na = 1e23 : 0.01e23 : 5e23            % m-3
      k=k+1;
      xinv(k) = sqrt((2*esi*kT)/(q*Na));

      phi_sth(k) = (2*kT)*log(Na/ni);

      xdepl(k) = sqrt((2*esi*phi_sth(k))/(q*Na));

      Naval(k) = Na;
end

xinv = xinv*1e9;
xdepl = xdepl*1e9;
Naval = Naval/1e6;

figure(1)
clf
hold on
plot (Naval, xinv, 'r-')
plot (Naval, xdepl, 'b-')
xlabel ('Doping concentration (cm-3)')
ylabel ('Depletion width (nm)')
axis([1e17 5e17 0 120])
title ('Depletion width under inverison')
```

emitter.m

```
% solve MOSFET Poisson-Boltzman equation for n-type Si field emitter (planar)
% [x,y] = ODE45('F',xspan,ic)
% integrate y' = F(x,y) from time x0 to xFINdL with initial conditions ic.

clear
figure(1); clf; figure(2); clf; figure(3); clf; figure(4); clf; figure(5);
clf
global q k eox esi T Nd NV xox ni Wm
global V phi_s
%%%%%%%%%%          constants          %%%%%%%%%%%%
t=0;j=0;
k=8.61834e-5;
q=1.602e-19;
esi=11.9*8.854188e-12;
eox=3.9*8.854188e-12;
T=300;              % K
Nd=6e23;     % m-3
xox=200e-10;       % m
ni=1.07e16;        % must be changed if T changes
NV=1e25;     % m-3
Wm=4.04;     % eV, aluminum = 4.04eV

styles = {'b-' 'k-' 'r-'};
styles2 = {'b--' 'k--' 'r--'};
styles3 = {'b-' 'k.-' 'r--'};
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
x0 = 0;
xfinal = 1e-7;
ic = 1;                  % initial guess

Vvals = [0 , 5, -5];           % V = 15 V, xox=50A gives n = 1e20 cm-3
                        %      E = 1e7 V/cm (field emission)
for V = Vvals
      t=t+1;
      ic = fzero('icF2',ic);  % Solve for initial condition Phi_s
      phi_s = ic;
      xspan = [x0 xfinal];

      [x,phi] = ode45('F2',xspan,ic);           % phi(i) = phi(x)

      figure(1)
      plot(x,phi,char(styles(t)))
      xlabel ('Distance into semiconductor (m)')
      ylabel ('Potential (Phi(V))')
      hold on
      zoom on

%%%%%%%%%%%%%%%%%% Fill in F_phi solutions  %%%%%%%%%%%%%%%%
      for j=1 : size(x,1)
            F_phi(j)=(phi(j)/abs(phi(j)))*sqrt((exp(phi(j)/(k*T))-phi
      (j)/(k*T)-1)+(ni^2/Nd^2)*(exp(-phi(j)/(k*T))+phi(j)/(k*T)-1));
      end
%%%%%%%%%%%%%%%%%% Plot E field       %%%%%%%%%%%%%%%%%%
```

```
      E = sqrt(2*k*T*q*Nd/esi) * F_phi;
      figure(2)
      plot(x,E/100,char(styles(t)))
      xlabel ('Distance into semiconductor (m)')
      ylabel ('Electric Field (V/cm)')
      hold on
      zoom on

%%%%%%%%%% Plot electron concentration      %%%%%%%%%
      n = Nd*exp(phi/(k*T));
      figure(3)
      semilogy(x,n/1e6,char(styles(t)))
      xlabel ('Distance into semiconductor (m)')
      ylabel ('Electron concentration (cm-3)')
      hold on
      zoom on

%%%%%%%%%% Plot hole concentration      %%%%%%%%%
      p = (ni^2/Nd)*exp(-phi/(k*T));
      figure(4)
      semilogy(x,p/1e6,char(styles2(t)))
      xlabel ('Distance into semiconductor (m)')
      ylabel ('Hole concentration (cm-3)')
      hold on
      zoom on

%%%%%%%%%% Plot energy bands      %%%%%%%%%
      offset = 1.124/2;
      Ec = 1.124 - phi-offset;
      Ev = Ec-1.124;
      figure(5)
      hold on
      if V==0                          % plot equilibrium Ef in bulk
            Ei = (Ec+Ev)/2;
            phi_p = k*T*log(Nd/ni)
            Efn = Ei + phi_p; %  Fermi level in bulk
            Efn2 = zeros(size(Efn,1),1); Efn2(:,1) = min(Efn);
            plot (x,Efn2,'k--')
%maxd = max(Efn)
      end
      if t==size(Vvals,2)                  % plot inversion Ei
            Ei = (Ec+Ev)/2;
            plot (x,Ei, 'r--')

      end
      plot(x,Ec,char(styles(t)))
      plot(x,Ev,char(styles(t)))
      xlabel ('Distance into semiconductor (m)')
      ylabel ('Energy (eV)')
      zoom on

      clear F_phi % must clear since x range will differ on new solution
end
```

emitter_icf.m

```
% solves initial condition for F(phi) as a function of applied voltage (V)
% finds zero of function b
% to be used from ic=fzero('icF',y0)    y0 = intitial guess

function b=function0(phi)

global q k eox esi T Nd NV xox ni Wm
global V


b=1*(sqrt(2*k*T*q*Nd*esi))*(phi/abs(phi))*sqrt((exp(phi/(k*T))-phi/(k*T)-
1)+(ni^2/Nd^2)*(exp(-phi/(k*T))+phi/(k*T)-1)) * xox/eox-
k*T*log(ni^2/(Nd*NV))+phi-V;
```

emitter_F2.m

```
%function for electrostatic potential phi for n-type Si field emitter
%TO BE USED [t,Y]=ode45('function',tspan,ic)

function F_phi=function1(x,phi)

global q k eox esi T Nd NV xox ni Wm
global V

F_phi=-1*(sqrt(2*k*T*q*Nd/esi))*(phi/abs(phi))*sqrt((exp(phi/(k*T))-
phi/(k*T)-1)+(ni^2/Nd^2)*(exp(-phi/(k*T))+phi/(k*T)-1));
```

emitter_Qex.m

```
clear

global q k eox esi T Na NC xox ni Wm
global V
%%%%%%%%%%          constants          %%%%%%%%%%%%%

t=0;
k=8.61834e-5;
q=1.602e-19;
esi=11.9*8.854188e-12;
eox=3.9*8.854188e-12;
T=300;              % K
Na=6e23;     % m-3
xox=45e-10;         % m
ni=1.07e16;         % must be changed if T changes
NC=3.1e25;  % m-3
Wm=4.04;     % eV, aluminum = 4.04eV

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

ic=1; % ic = phi_s  boundary condition

Vsteps = -2 : 0.1: 2;

for V= Vsteps
      t=t+1;
      ic=fzero('icF',ic);
      icval(t)=ic;
      Vval(t)=V;
      phi_s=ic;

      integral=0;              %  do Qh integral peicewise
      if ic>0
            for phi=0:ic/200:ic;
                  val = intQe(phi);
                  integral=integral-ic*val/201;
            end
      else
            for phi=0:ic/200:ic;
                  val = intQe(ic+phi);
                  integral=integral+ic*val/201;
            end
      end

      Qe(t)=integral;
      Vt(t)=V;
end
Qeo=Qe/1e4;
figure(3)
clf
plot(Vt,Qeo,'k--')

t=0
```

```
for V= Vsteps
      t=t+1;
      ic=fzero('icF',ic);
      icval(t)=ic;
      Vval(t)=V;
      phi_s=ic;

      integral=0;             %  do Qh integral peicewise
      if ic>0
            for phi=0:ic/200:ic;
                  val = intQh(phi);
                  integral=integral-ic*val/201;
            end
      else
            for phi=0:ic/200:ic;
                  val = intQh(ic+phi);
                  integral=integral-ic*val/201;
            end
      end

      Qh(t)=integral;
      Vt(t)=V;
end
Qho=Qh/1e4;
figure(3)
hold on
plot(Vt,Qho,'r--')
xlabel ('V [V]')
ylabel ('|Qh| [C/cm^2]')

Qso = Qeo+Qho;
plot(Vt,Qso,'b-')
```

emitter_Qe.m

```
function a = functionQe(phi)

global q k eox esi T Na NC xox ni Wm
global V

if sign(phi) == 0
      a=0;
else
      if sign(phi)>0


a=(q*ni^2/Na)*sqrt(esi/(2*k*T*q*Na))*(exp(phi/(k*T))-1)/sqrt((exp(-
1*phi/(k*T))+phi/(k*T)-1)+(ni^2/Na^2)*(exp(phi/(k*T))-phi/(k*T)-1));

      end

      if sign(phi)<0

a=-1*(q*ni^2/Na)*sqrt(esi/(2*k*T*q*Na))*(exp(phi/(k*T))-1)/sqrt((exp(-
1*phi/(k*T))+phi/(k*T)-1)+(ni^2/Na^2)*(exp(phi/(k*T))-phi/(k*T)-1));

      end
end
```

emitter_Qh.m

```
function a = functionQh(phi)

global q k eox esi T Na NC xox ni Wm
global V

if sign(phi) == 0
      a=0;
else
      if sign(phi)>0


a=-1*sqrt(esi*q^2*Na/(2*q*k*T))*(exp(-1*phi/(k*T))-1)/sqrt((exp(-
1*phi/(k*T))+phi/(k*T)-1)+(ni^2/Na^2)*(exp(phi/(k*T))-phi/(k*T)-1));

      end

      if sign(phi)<0

a=sqrt(esi*q^2*Na/(2*q*k*T))*(exp(-1*phi/(k*T))-1)/sqrt((exp(-
1*phi/(k*T))+phi/(k*T)-1)+(ni^2/Na^2)*(exp(phi/(k*T))-phi/(k*T)-1));

      end
end
```

Appendix C: MEDICI Device Simulation Code

```
% MEDICI device simulation from Vertical MOS transistors
```

vmos.med

```
loop  steps=1

$*****************************  Inputs  *****************************
$
$Input Description:
$                 xmesh:            number of x meshpoints
$                 ymesh:            number of y meshpoints
$                 pillarw:    pillar radius
$                 pillarh:    pillar height
$
$                 srcxj:            junction depth under pillar (source
region)
$                 drainxj:    junction depth of drain (top of pillar)
$                 drainsp:    space between drain & delta doped region
$                 deltaxj:    junction depth of delta doping
$
$                 gateox:           gate oxide thickness
$                 bulkdop:    doping of bulk of wafer
$                 draindop:   drain region doping
$                 deltadop:   drain2 delta doping
$                 srcdop:           source region doping
$                 R:          contact resistance (ohms)


assign      name=xmesh  n.value=120
assign      name=ymesh  n.value=50

assign      name=pillarw      n.value=3
assign      name=channel      n.value=@pillarw-0.02
assign      name=pillarh      n.value=1.2

assign  name=gateox     n.val=0.0190
assign      name=srcxj  n.val=0.185
assign      name=srcxj2 n.val=0.05
assign      name=drainxj      n.val=0.05
assign      name=drainsp      n.val=0.0
assign      name=deltaxj      n.val=0.0

assign      name=draindop     c.val=2e19
assign      name=deltadop     c.val=2e18
assign      name=bulkdop      c.val=9.43e17
$good assign      name=bulkdop      c.val=9.5e17
$     name=bulkdop      c.val=5e17
assign      name=srcdop c.val=2e19
assign  name=R          n.val=0
```

```
assign      name=xmax   n.value=@pillarw+@gateox+1
assign      name=ymax   n.value=@pillarh+0.5

$ Note: All distances are in um
$************************   MESH GENERATION   ****************************
$Initiate mesh
mesh cylindrical
$mesh

$ Tags for Mesh generation
x.mesh      n=1          l=0
x.mesh      n=2          l=@xmax/@xmesh
x.mesh      n=0.1*@xmesh      l=@pillarw-2*@srcxj
x.mesh      n=0.5*@xmesh      l=@pillarw-3*@gateox
x.mesh      n=0.9*@xmesh      l=@pillarw+3*@gateox
x.mesh      n=@xmesh    l=@xmax

y.mesh      n=1          l=0
y.mesh      n=@ymesh l=@ymax


$*********************************  Device regions  ********************

region name=pillar x.min=0 x.max=@pillarw y.min=0 y.max=@pillarh  silicon
region name=base   x.min=0 x.max=@xmax y.min=@pillarh y.max=@ymax silicon
region name=oxgate x.min=@pillarw x.max=@xmax y.min=0 y.max=@pillarh    oxide

$*********************************  Electrodes  ******************

electr name=drain  x.min=0 x.max=0.1 y.min=0 y.max=@drainxj
electr  name=substrate x.min=0 x.max=0.1 y.min=@ymax-0.1 y.max=@ymax
electr  name=gate x.min=@pillarw+@gateox x.max=@xmax y.min=0
+     y.max=@pillarh-2*@gateox void
electr      name=source x.min=@xmax-0.1 x.max=@xmax y.min=@pillarh
y.max=@pillarh+0.1

$*********************************  Dopings  ***************

$profile p-type n.peak=@bulkdop unif
$-----------------        Doping 1-D          ------------------------------
$profile p-type n.peak=5e17 y.min=0 y.max=@pillarh/3  y.char=0.5
$-----------------        Doping 2-D          ------------------------------

$ - - - - - -    original graded doping profile    - - - - - -
profile p-type n.peak=@bulkdop x.min=0 x.max=@pillarw-0.035 y.min=0
+     y.max=@pillarh/3   x.char=0.031   y.char=0.5 outf=bodydop.txt
$ - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

$ - - - - - -    reverse graded doping profile    - - - - - - - -
$profile p-type n.peak=@bulkdop x.min=0 x.max=@pillarw-0.035 y.min=0.9
$+    y.max=1.4   x.char=0.031   y.char=0.5 outf=bodydop.txt
$ - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

$ - - - - - -    const doping profile    - - - - - - - -
$profile p-type n.peak=@bulkdop x.min=0 x.max=@pillarw-0.035 y.min=0
$+    y.max=@pillarh/3   x.char=0.031   y.char=15 outf=bodydop.txt
$ - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
```

```
profile n-type n.peak=@draindop y.min=0 y.max=@drainxj y.char=0.1
$profile n-type n.peak=@deltadop y.min=@drainxj+@drainsp
$+    y.max=@drainxj+@drainsp+@deltaxj y.char=0.01
profile n-type n.peak=@srcdop x.min=@pillarw-@srcxj/2 x.max=@xmax
+     y.min=@pillarh+@srcxj2/2 y.max=@pillarh+@srcxj2 y.char=0.1 xy.rat=0.8

$*********************************   Plots  *****************

contact name=gate n.poly resistan=@R
models conmob fldmob srfmob2
symb newton carriers=1 electrons

plot.2d boundary fill title=VMOS
$contour doping fill
plot.2d grid boundary fill title=Mesh

plot.1d doping x.start=2.5 x.end=@xmax y.start=1.25 y.end=1.25
+     y.log points bot=1e15 top=1e21 color=2 title="Source doping"

      $theta is tilt, phi is spin
assign      name=phi    n.val=60
assign      name=theta  n.val=30

plot.3d doping log x.min=2 x.max=@pillarw y.min=0 y.max=@ymax-0.1
+ z.min=1e15 z.max=1e21 phi=@phi theta=@theta  ^fill.view ^equidist
$3d.surf c.auto

$regrid doping log ratio=3 smooth=1
$regrid doping log ratio=3 smooth=1
$plot.2d grid boundary fill title=Mesh2
log out.file=mdexg1

$ plot Channel doping across structure
plot.1d doping x.start=@pillarw-0.06 x.end=@pillarw y.start=@pillarh/2
+     y.end=@pillarh/2 y.log line=1 bot=8.5e16 top=5e18 color=1
title="Channel doping"

$$ plot Channel doping across structure - expanded view
$plot.1d doping x.start=@pillarw-0.3 x.end=@pillarw y.start=@pillarh/2
$+    y.end=@pillarh/2 y.log points bot=8.5e16 top=5e18 color=3
title="Channel doping 2"

$ plot Channel doping 0.05um (500 A) from pillar edge
plot.1d doping x.start=@channel x.end=@channel y.start=0 y.end=1.5
+     y.log bot=1e15 top=1e21 color=2 title="Vertical doping"

$ ------------------------  Ramp Vds to 0.1 V ------------------------------
solve V(gate)=0 V(drain)=0.01
solve V(gate)=0 V(drain)=0.05
solve V(gate)=0 V(drain)=0.1

$ ------------------------  Ramp Vgs to 3 V ------------------------------

log  ivfile="LOGS/jdrain.log"
assign name=VDS n.val=0.1
loop steps=10
```

```
     assign name=VGS n.val=(0.05 0.2 0.6 1.0 1.2 1.4 1.6 1.8 2.0 2.1)
     solve V(gate)=@VGS V(drain)=@VDS
l.end
loop steps=11
     assign name=VGS n.val=(2.2 2.3 2.5 2.75 3.0 3.25 3.5 3.75 4.0 4.5 5.0)
     solve V(gate)=@VGS V(drain)=@VDS
l.end
solve elec=gate save.bia outfile=Vgate.soln
log close

$*****************************************************************************

plot.1d title="Subthreshold - log Id vs. Vg" in.file="LOGS/jdrain.log" y.log
+     y.axis=I(drain) x.axis=V(gate) points color=1 symbol=1 line=1
+     outfile="PLOTS/subth_Navd943.txt"
label label="Vds = "@VDS" V

plot.1d title="Vgs vs Id" in.file="LOGS/jdrain.log"
+     y.axis=I(drain) x.axis=V(gate) points color=1 symbol=1 line=1
+     outfile="PLOTS/subth_Navd943.txt"
label label="Vds =  "@VDS" V

$ ------------------------  Ramp Vds to 3 V ------------------------------

log  ivfile="LOGS/jdrain2.log"
loop steps=11
    assign name=VDS n.val=(0 0.1 0.2 0.3 0.5 0.6 0.8 1 2 2.5 3)
    solve V(gate)=@VGS V(drain)=@VDS
l.end
log close

plot.1d y.axis=I(drain) x.axis=V(drain) points color=1 symbol=1 line=1
+     title="Vds vs Id" in.file="LOGS/jdrain2.log"
+     outfile="PLOTS/ID_Vg30.txt"
label label="Vgs = "@VGS" V, R = "@R

$ ---------------------------------------------------------------------

plot.2d bound junc depl fill scale title="1D potential contours"
contour poten ncont=5 color=2
label label="Vgs = "@VGS" V"

plot.2d bound junc depl fill scale title="Current flowlines"
contour flowlines ncont=21 color=4
label label="Vgs = "@VGS" V"

save mesh out.file="../MESH/"@profile".mesh"


l.end
```

Appendix D: SUPREM Process Simulation Code

vmos.in

```
go athena

#                          VMOS process

#SILVACO Process simulation for Vertical MOS transistor
go athena

line x loc=5.0 spac=0.5
line x loc=6.0 spac=0.1
line x loc=6.4 spac=0.002
line x loc=6.5 spac=0.002
line x loc=6.6 spac=0.01
line x loc=6.8 spac=0.1
line x loc=10.0 spac=0.5

#
line y loc=0.0 spac=0.02
line y loc=0.3 spac=0.02
line y loc=0.4 spac=0.1
line y loc=1.1 spac=0.02
line y loc=1.35 spac=0.02
line y loc=3.0 spac=0.25
                        #n-type Si, P 1e15 cm-3, rho=4 ohm-cm

init silicon c.phosphor=1.0e15 orientation=100

deposit nitride thick=0.05
deposit oxide thick=0.3


                                            struct outfile=a1.str
implant boron dose=2e14 energy=195 crystal
                                            struct outfile=a2.str

method compress init.time=0.10 fermi
diffus time=900 temp=1100 nitro press=1.00
                                            struct outfile=a3.str
deposit photo thick=1
                                            struct outfile=a3b.str
etch photores start x=0 y=-2.0
etch cont x=3.5 y=-2.0
etch cont x=3.5 y=1.0
etch done x=0 y=1.0
etch photores start x=6.5 y=-2.0
etch cont x=13.5 y=-2.0
etch cont x=13.5 y=1.0
etch done x=6.5 y=1.0
etch photores start x=16.5 y=-2.0
```

```
etch cont x=23.5 y=-2.0
etch cont x=23.5 y=1.0
etch done x=16.5 y=1.0
etch photores start x=26.5 y=-2.0
etch cont x=30 y=-2.0
etch cont x=30 y=1.0
etch done x=26.5 y=1.0
                                        struct outfile=a3c.str

                        # Oxide hardmask

etch oxide dry thick=1.00
etch photores dry thick=0.5
etch nitride dry thick=0.3

                                        struct outfile=a4.str
etch photores all

#etch nitride all
                                        struct outfile=a4b.str

                        # Silicon pillar
etch silicon dry thick=1.3
                                        struct outfile=a5.str
                        # HF dip so can implant As
etch oxide all
                # Thin oxide to protect sidewalls during implant
                                        struct outfile=a5b.str

                        # n+ implant

implant arsenic dose=1.0e16 energy=180 tilt=1 crystal
                                        struct outfile=a5d.str
                        # RCA clean

etch oxide all

# Form gate oxide + protective oxide cap on Si top layer
method compress init.time=0.10 fermi
diffus time=30 temp=925 dryo2 press=1.00 hcl.pc=0
# - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
extract name="gateox" thickness material="SiO~2" mat.occno=1 y.val=0.5
                                        struct outfile=a6b.str
# poly gate
#
deposit poly thick=0.50 divi=10 c.phosphor=1.0e20
                                        struct outfile=a7.str
deposit photo thick=1.0
etch photores start x=0 y=-5.0
etch cont x=2 y=-5.0
etch cont x=2 y=1.0
etch done x=0 y=1.0
etch photores start x=8 y=-5.0
etch cont x=12 y=-5.0
etch cont x=12 y=1.0
etch done x=8 y=1.0
etch photores start x=18 y=-5.0
```

```
etch cont x=22 y=-5.0
etch cont x=22 y=1.0
etch done x=18 y=1.0
etch photores start x=28 y=-5.0
etch cont x=30 y=-5.0
etch cont x=30 y=1.0
etch done x=28 y=1.0
                                        struct outfile=a8.str
etch poly dry thick=0.50

                                        struct outfile=a9.str
etch photores all
deposit oxide thick=1.5 dy=0.2
                                        struct outfile=a10.str
#                       CMP to SiN layer
etch above p1.y=0.045
                                        struct outfile=a11.str
#                       WET ETCH SIN
etch nitride all
                                        struct outfile=a11b.str
deposit oxide thick=0.3 dy=0.2
                                        struct outfile=a12.str
deposit photo thick=1.0
etch photores start x=4 y=-4.0
etch cont x=6 y=-4.0
etch cont x=6 y=1.0
etch done x=4 y=1.0
etch photores start x=9 y=-4.0
etch cont x=11 y=-4.0
etch cont x=11 y=1.0
etch done x=9 y=1.0
etch photores start x=14 y=-4.0
etch cont x=16 y=-4.0
etch cont x=16 y=1.0
etch done x=14 y=1.0
etch photores start x=19 y=-4.0
etch cont x=21 y=-4.0
etch cont x=21 y=1.0
etch done x=19 y=1.0
etch photores start x=24 y=-4.0
etch cont x=26 y=-4.0
etch cont x=26 y=1.0
etch done x=24 y=1.0
                                        struct outfile=a13.str
etch oxide dry thick=2.0
etch photores dry thick=0.7
                                        struct outfile=a14.str
etch photores all
                                        struct outfile=a14b.str

deposit titanium thick=0.05
deposit alumin thick=1
                                        struct outfile=a15.str
etch above p1.y=-0.7
                                        struct outfile=a15b.str
deposit photo thick=1.0
                                        struct outfile=a16.str
```

```
etch photores start x=0 y=-5.0
etch cont x=3 y=-5.0
etch cont x=3 y=1.0
etch done x=0 y=1.0
etch photores start x=7 y=-5.0
etch cont x=8.5 y=-5.0
etch cont x=8.5 y=1.0
etch done x=7 y=1.0
etch photores start x=11.5 y=-5.0
etch cont x=13 y=-5.0
etch cont x=13 y=1.0
etch done x=11.5 y=1.0
etch photores start x=17 y=-5.0
etch cont x=18.5 y=-5.0
etch cont x=18.5 y=1.0
etch done x=17 y=1.0
etch photores start x=21.5 y=-5.0
etch cont x=23 y=-5.0
etch cont x=23 y=1.0
etch done x=21.5 y=1.0
etch photores start x=27 y=-5.0
etch cont x=30 y=-5.0
etch cont x=30 y=1.0
etch done x=27 y=1.0

                                        struct outfile=a17.str
#
etch aluminum dry thick=0.5

etch photores dry thick=0.5
                                        struct outfile=a18.str
etch photores all
etch titanium dry thick=0.5

struct outfile=vmos.str

etch aluminum all
etch titanium all
etch oxide above p1.y=0.05
#
etch oxide start x=6.8 y=0.00
etch cont x=9 y=0.00
etch cont x=9 y=1.4
etch cont x=8 y=1.4
etch cont x=8 y=1.0
etch cont x=6.8 y=1.0
etch done x=6.88 y=0.0

struct outfile=vmos.str
```

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