Degradation of GaN High Electron Mobility Transistors under High-power and High-temperature Stress

by

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B.S. Electrical Engineering, The Pennsylvania State University, 2012

Submitted to the Department of Electrical Engineering and Computer Science in Partial Fulfillment of the Requirements for the Degree of

Master of Science in Electrical Engineering

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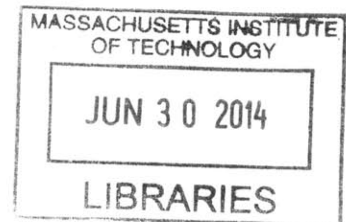

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ABSTRACT

GaN HEMTs (High Electron Mobility Transistors) are promising candidates for high power and high frequency applications but their reliability needs to be established before their wide deployment can be realized. In this thesis, degradation mechanisms of GaN HEMTs under high-power and high-temperature stress have been studied. A novel technique to extract activation energy of degradation rate from measurements on a single device has been proposed. High-power and high-temperature stress has revealed two sequential degradation mechanisms where the gate current degrades first and saturates only after which the drain current shows significant degradation. A study of the semiconductor surface of delaminated degraded devices shows formation of grooves and pits at the gate edge on the drain side. Electrical degradation is shown to directly correlate with structural degradation. Also, higher junction temperature is shown to results in more severe structural degradation.

Thesis supervisor: Jesus A. del Alamo
Title: Professor of Electrical Engineering

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Chapter 1. Introduction

The idea of the HEMT (high electron mobility transistor) structure was first brought out by Takashi Mimura in 1979 [1]. During the following year, both depletion-mode [2]and enhancement-mode [3]HEMTs on an AlGaAs/GaAs heterostructure were demonstrated. Conventional MOSFET structures rely on high electron or hole densities introduced by n- or p- type dopants to conduct current. The introduction of dopants in semiconductor material, while guaranteeing high carrier densities, also limits the mobility of these free carriers due to scattering with impurities. HEMTs avoid this by utilizing heterojunction of a highly-doped wide-bandgap n-type donor-supply layer and a non-doped channel layer without introducing impurities in the channel itself. This results in the extremely high electron mobility and makes the HEMT structure promising for electronic applications.

1.1 Introduction to GaN HEMTs

Ever since the first demonstration of high electron mobility transistor based on a GaN/AlxGa1-xN heterojunction in 1993 by Khan et. al [5], its development has skyrocketed. Due to its high electron mobility, high breakdown field, and high power density, GaN is a promising candidate for high power and high frequency applications. Compared with GaAs which has a basic power density of about 1.5 W/mm, GaN is able to reach a power density as high as 12 W/mm. This gives GaN based power amplifiers a huge advantage in that for the same power level, multiple GaAs based devices will be necessary while a single GaN based device is enough.

As illustrated in Fig. 1-1, the key characteristics of GaN, i. e. high dielectric strength, high operating temperature, high current density, high speed switching and low on-resistance make it an extremely promising material for power electronics applications. Table 1-1 summarizes some of the main material properties of GaN compared with other semiconductors used for power devices applications. The simultaneously achievable high breakdown field, high operation temperature, and large bandgap make GaN superior to other semiconductors.

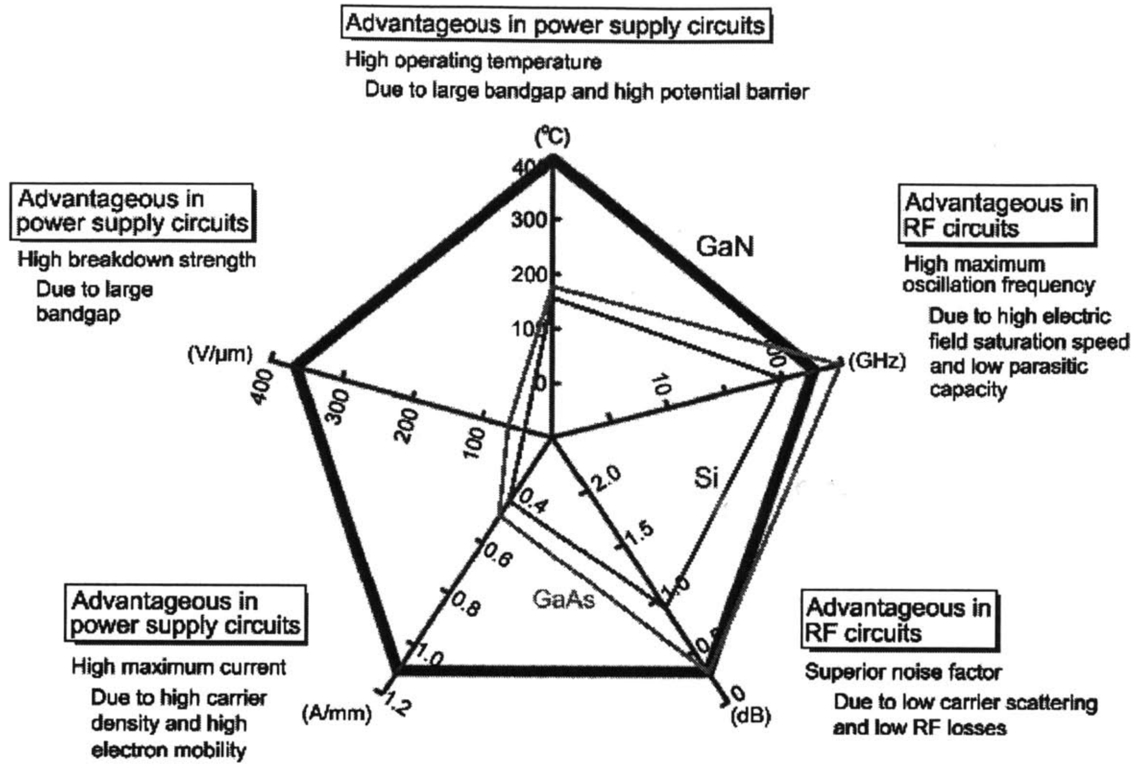

Figure 1-1. Key advantages of GaN compared with that of GaAs and Si. [4]

Material	Mobility μ, $cm^2/V{\cdot}S$	Dielectric Constant ε	Bandgap, E_g, eV	Breakdown field E_b, 10^6 V/cm	T_{max}, °C
Si	1300	11.9	1.12	0.3	300
GaAs	5000	12.5	1.42	0.4	300
4H-SiC	260	10	3.2	3.5	600
GaN	1500	9.5	3.4	2	700

Table 1-1. Material Properties of Microwave Semiconductors [6].

1.2 Previous Studies on Reliability

Despite the excellent performance and rapid development of AlGaN/GaN HEMTs, reliability is a serious issue without solving which the wide deployment of GaN based transistors will be impossible. Considerable research has been conducted in trying to figure out the underlying physics of various device degradation mechanisms. Up to now, the demonstrated degradation mechanisms include but are not limited to:

1) Inverse piezoelectric effect
2) Time-dependent trap formation
3) Percolative conductive paths formation
4) Electrochemical AlGaN and GaN degradation

Ever since the first observation by Joh and del Alamo [7], the degradation mode of GaN HEMTs under reverse gate bias consisting in an increase of gate leakage current and an enhancement of current collapse has been repeatedly observed by many other authors [8]–[19][20]. The mechanism involves defects existing at the gate edges which can promote the injection of electrons from the gate contact into the AlGaN barrier layer through a trap-assisted tunneling mechanism [10]. Those defects can be introduced during growth of the AlGaN/GaN heterostructure or during stress with gate being reverse biased which imposes a very high electric field at the gate edges. An electrical signature of such degradation mode is the presence of a critical voltage V_{crit} of $|V_G|$ above which a sudden gate leakage current increase of several orders of magnitude is observed. The physical explanation of such degradation mechanism takes into consideration the piezoelectric nature of GaN and AlGaN materials as well as the extremely high vertical electric field within the AlGaN barrier layer in a HEMT. When reverse bias is applied, the vertical component of the electric field at the gate-drain edge increases sharply. This in turn enhances the tensile strain and the stored elastic energy brought about by the inverse piezoelectric effect. The enhancement is most severe at the gate edge where the electric field reaches its maximum value. Once a certain critical level of stored energy or strain is reached, crystallographic defects can be produced in the AlGaN layer. These defects will then degrade the electrical characteristics of the transistor by affecting transport properties or by inducing trapping effect.

Biasing GaN HEMTs below V_{crit} itself, however, cannot guarantee the avoidance of device failure. As demonstrated by Marcon et al. [21] and Meneghini [22], if devices are stressed at constant reverse gate voltage for a sufficiently long time, catastrophic gate leakage increase may occur even below the critical voltage. Fig. 1-2 demonstrates such a situation where device is stressed under V_G = -30 V (V_{crit} = -35 V). Sudden increase of gate leakage happens after a sufficiently long stress time. To explain this, Meneghini *et al.* has proposed a percolative model where for long stress times, defects may be randomly generated within the AlGaN layer, due to the inverse piezoelectric effect or to the high electric field, which can lead to atom displacement. With increasing trap concentration, defects may overlap, and this may result in an increased gate current noise. Then after a sufficiently long stress time, a conductive path between gate and buffer can be generated and the gate diode is permanently damaged.

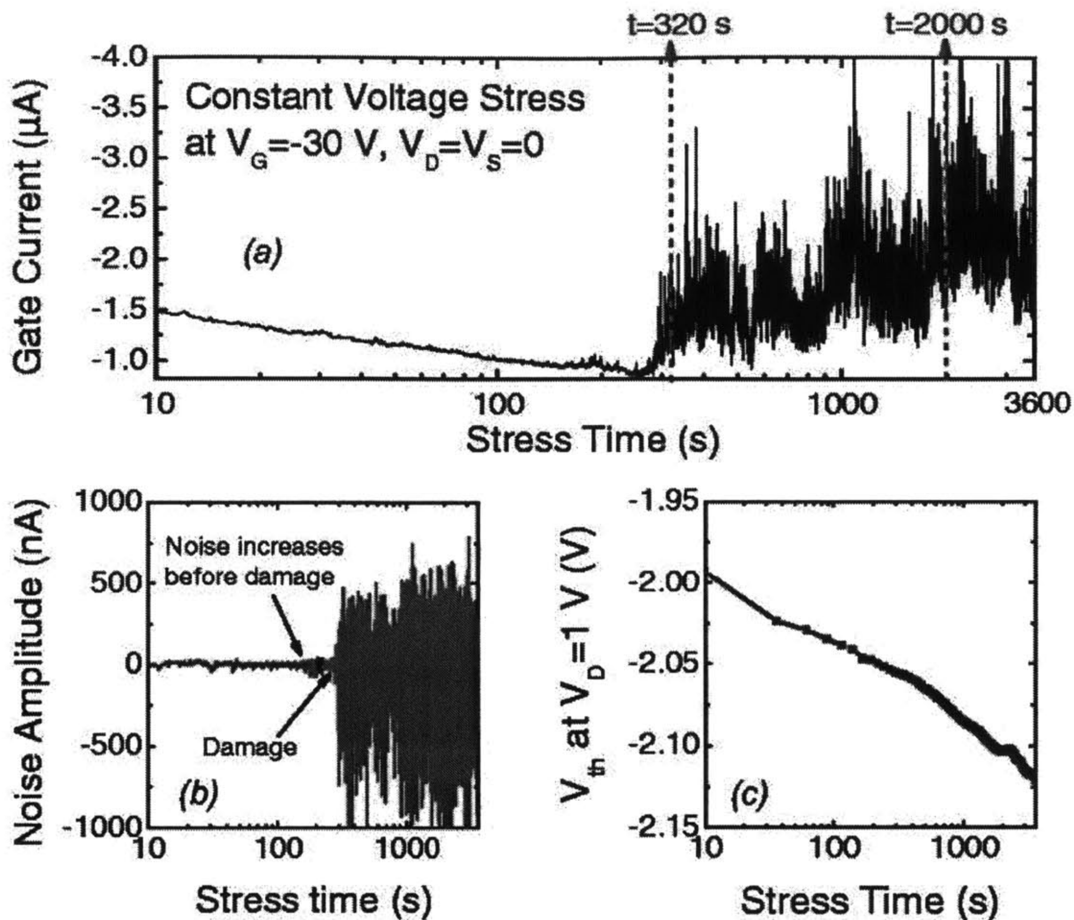

Figure 1-2. Results of a constant-voltage reverse-bias stress test. The three graphs report the variation of (a) gate current, (b) amplitude of the noise on gate current, and (c) threshold voltage during stress time. V_{crit} for the specific device is around -35 V [22].

Besides degradation of the Schottky gate, another reliability concern in GaN HEMTs is related to the degradation of drain saturation current and the overall output power. In [23], a direct correlation between the saturation drain current and structural degradation at the gate edge of GaN HEMTs stressed under OFF-state regime is established as illustrated in Fig. 1-3. Gao *et al.* [24] proposed an explanation for the structural degradation in AlGaN/GaN HEMTs under OFF-state stress where they postulate that water from the passivation layer surface and the external atmosphere, as well as holes caused by trap-assisted interband tunneling in the AlGaN barrier are likely to play an essential role in forming the surface pits. Moreover, they proposed that permanent drain current degradation is due to the reduction of the AlGaN barrier caused by surface pitting. However, a more detailed and comprehensive investigation of the reason for drain current degradation is still needed.

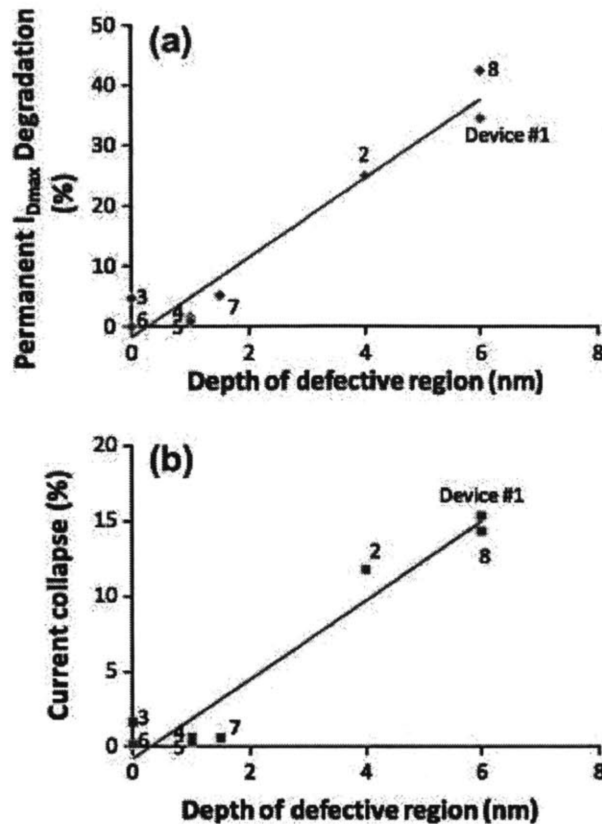

Figure 1-3. Correlation between electrical and structural degradation for AlGaN/GaN HEMTs degraded under OFF-state conditions: (a) permanent I_{Dmax} degradation vs. pit depth and (b) current collapse after stress vs. pit depth [23].

1.3 Motivation

The reliability of GaN HEMTs has greatly improved in recent years. The improvements include but are not limited to: suppression of current collapse to a large extent by passivating surface states using deposited or in-situ grown SiN , increase of DC breakdown voltage by utilizing field plates [25], and reduction of problems related with gate leakage current and its stability by engineering of the gate electrode, contact and recess area. Another important issue in a device technology is the value of mean time to failure (MTTF). The usually extremely long values are commonly derived by extrapolating the results of three-temperatures DC or RF accelerated tests according to the Arrhenius law and by using a certain level of degradation of a device parameter as failure criteria (for example, a 10% degradation in I_D). A wide set of data is available in the literature concerning Arrhenius-type testing of GaN HEMTs. Table 1-2 shows the main parameters of the accelerated tests adopted, and identifies the research

groups involved [26]. From the table, we can see that there is a large range of MTTF extracted by different laboratories on different technologies. It is not very meaningful for us to compare these values. To achieve more meaningful comparisons, there are still some problems left to be solved. First of all, the extrapolation of an MTTF requires knowing the activation energy with absolute certainty which is not always declared by the laboratories. Secondly, the activation energy is usually derived using high temperature testing. It is possible that high E_a mechanisms dominate at high temperatures while low E_a mechanisms dominate at lower temperatures which are relevant in actual device operation. By carrying out high temperature tests only, the low activation energy mechanisms might be overlooked. Thirdly, the interaction of the different accelerating factors (in particular current, temperature and voltage or electric field) is not known.

Affiliation	Year	L_g (μm)	E_a (eV)	MTTF (hours)	T_{ch}	V_{DS} (V)	F (GHz)	Ref.
Fujitsu	2004	0.8			~100°C	50	2.1	[99]
Nitronex	2005							[100]
Eudyna	2006	0.8		1×10^6 @200°C	200°C	50	DC	[109]
HRL	2007	0.15	1.8	3.5×10^9 @125°C	285°C, 315°C, 345°C	25		[39]
HRL	2007	0.15			285°C	25	10	[38]
Nitronex	2007	0.5	2.0	$>1 \times 10^7$ @150°C	150°C	28	DC	[101]
Fujitsu	2007		1.81	$>1 \times 10^6$ @200°C	300°C-350°C	50	DC	[12]
Toshiba	2007				250°C	30	DC	[102]
Toshiba	2007		1.4		200°C-300°C	30-40	DC	[102]
TriQuint	2007		1.05	$>1 \times 10^5$ @150°C		28	10	[21]
NG	2007	0.2	-0.15		75°C-175°C Tamb	15-30	10	[20]
Fujitsu	2008	0.5			200°C	50	2.5	[103]
Cree	2008	0.45			150°C	28	2.6	[111]
RFMD	2008	0.5			170°C	48		[14]
IAF	2008	0.5			225°C	50	2	[110]
Cree	2008	0.45		1×10^6 @175°C	175°C	28	DC	[111]
RFMD	2008	0.5	2.47	$>1 \times 10^6$ @200°C	200°C	48	DC	[14]
TriQuint	2008	0.25		1×10^7 @150°C	150°C	40	DC	[11]
TriQuint	2008	0.25		1×10^7 @150°C	260°C, 290°C, 320°C	40		[11]
Gal-EL	2009	0.5		1.5×10^7 @300°C, 50 V	150°C-300°C	40-65		[104]
Raytheon	2009		1.7	$>10^7$ at 200°C	150°C	28		[105]
Mitsubishi	2010	0.4	1.62	1×10^7 @150°C	250°C, 260°C	47	DC	[106]
RFMD	2011	0.5	2.4	1×10^7 @200°C		65		[107]
Fraunhofer	2011	0.25	1.7	5×10^5 @200°C		42		[98]
Sumitomo	2011	0.6	1.6	1×10^7 @200°C		55		[108]
UMS	2012		1.8	$>1.8 \times 10^6$ @200°C				[112]

Table 1-2. Summary of long-term accelerated tests on GaN HEMTs carried out by industrial laboratories. [26].

Considering all the above described improvements and problems still left to be solved, one goal of this project is to develop a stress methodology which can reveal the activation energy of device degradation rate from measurements on a single device. The underlying idea is to utilize step temperature stress where degradation rates at a wide range of stress temperatures are measured so that the ultimate E_a value obtained reflects both low temperature degradation mechanisms and high temperature degradation mechanisms. Besides this, we will also study the various degradation mechanisms of GaN

HEMTs stressed under high-power regime, which, despite its importance in RF applications, has received little attention compared with OFF-state stress regime. Thirdly, we will establish a quantitative correlation between electrical degradation and structural degradation.

1.4 Thesis Outline

The thesis is organized in the following way:

In Chapter 2, we will first introduce the devices studied in this thesis as well as the experimental techniques that have been utilized. Following that, we will describe our designed characterization suite. Both electrical stress methodology and surface examination procedures will also be introduced.

In Chapter 3, the results of electrical degradation of selected experiments will be shown where we have identified two sequential degradation mechanisms with different electrical signatures. Activation energies of degradation rates are extracted and compared with values obtained from conventional method on a similar device technology.

In Chapter 4, the results of structure degradation of the same selected experiments as in Chapter 3 will be shown where we have formed a hypothesis of two stages in structural degradation corresponding to the two mechanisms revealed in Chapter 3.

In Chapter 5, quantitative analysis of the correlations between electrical and structural degradation will be investigated.

Chapter 2. Experimental

2.1 Introduction

This chapter describes the devices, instrumentation setup, as well as the stress methodology adopted in this thesis. It begins with a description of the GaN HEMTs that are used for this study. Then the experimental setup and characterization suite developed for evaluating the various figures of merit will be discussed. Finally the tools and characterization approach used in device surface examination will be explained.

2.2 Devices

Figure 2-1 shows a schematic cross section of the GaN HEMT used in this study. These devices are fabricated by TriQuint Seminconductor. The device has Fe-doped GaN buffer deposited on a SiC substrate. Then a 16 nm AlGaN barrier layer with 28% Al mole fraction is used. 2DEG (2-D Electron Gas) is formed at the intersection of the AlGaN barrier layer and the GaN buffer due to spontaneous polarization of the AlGaN barrier as well as the strain introduced by lattice mismatch between the two materials. On top of the barrier layer is a 5-nm GaN cap layer.

All the devices investigated in this study have a 0.25 μm gate length and a 2 x 260 μm gate width. The geometry of the gate is a standard S-Band design with 2 μm gate-source spacing and 4 μm gate-drain spacing.

The actual samples available for testing are individual GaN power amplifiers in MMIC (Monolithic Microwave Integrated Circuit) form. A device thermal model has been provided by TriQuint Semiconductor for estimation of transistor junction temperatures.

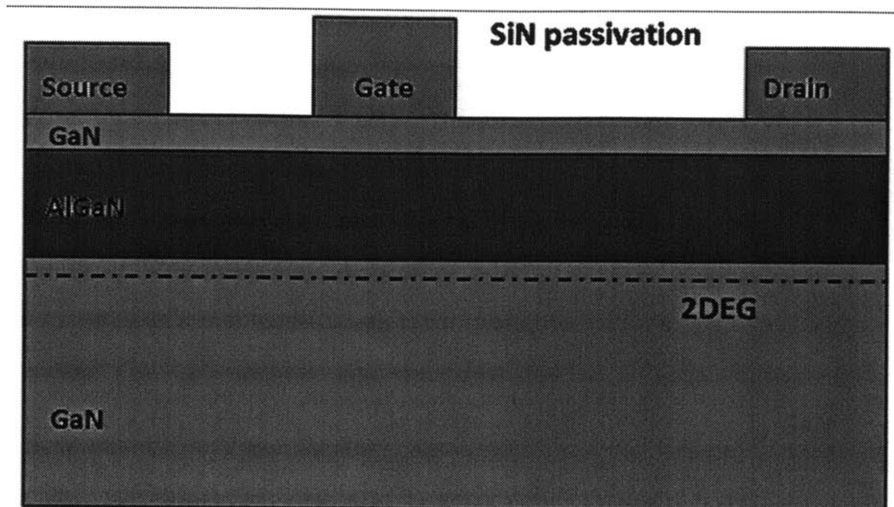

Figure 2-1. Schematic two-dimensional cross section of GaN HEMT (graph is not drawn to scale).

2.3 Electrical Experiments

The stress condition that is the focus of this study is the DC high-power and high-temperature stress regime. Devices are stressed under various V_{DS} and I_{DQ} high power conditions with base plate temperature raised from some starting temperature (higher than room temperature) in steps until the device finally blows up. Since the devices are in MMIC forms, a probe station is not suitable for device stressing and characterization. Instead, all our experiments are carried out on a four-channel Accel-RF life test system. Due to the unique properties of GaN HEMTs, electron trapping needs to be taken into consideration in order to distinguish it from permanent device degradation. We have developed a detrapping technique based on a thermal treatment of the devices. A benign characterization suite is adopted from [27] to characterize the device figures of merit before, during, and after stress experiments.

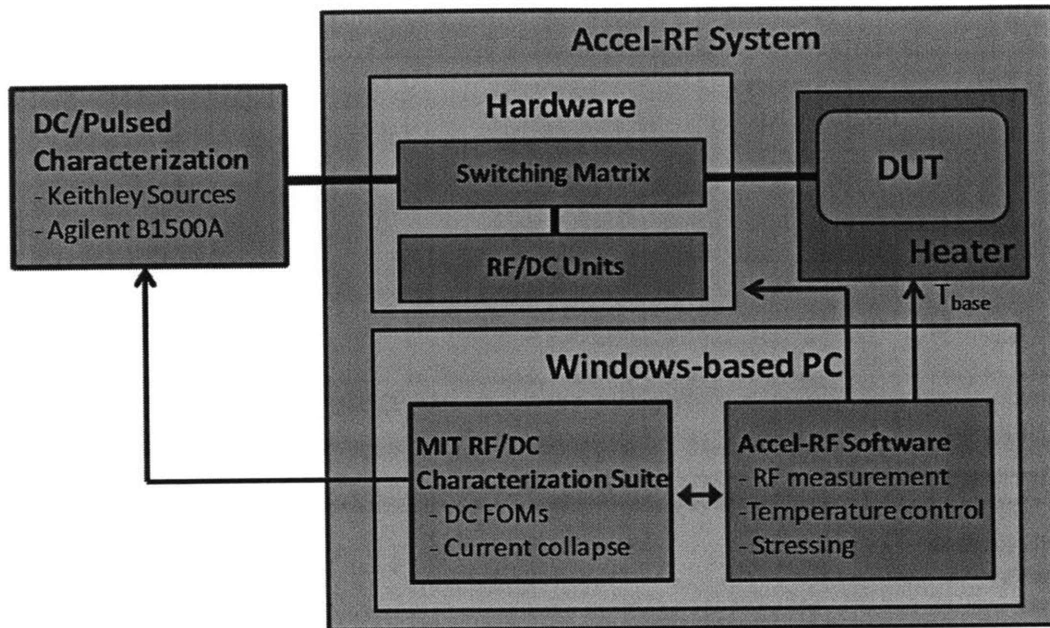

Figure 2-2. System configuration of stress test and characterization setup. Adopted from [28].

2.3.1 Experimental Setup

The experimental instruments used for this project are shown in Fig. 2-2. An Accel-RF AARTS RF10000-4/S system and a Keithley 2400 DC Source are used for device stress and characterization. The Accel-RF system has four channels, capable of stressing four devices simultaneously. The main components of the Accel-RF are Power Control Unit, Heater Control Unit, and RF Control Unit. In this project, the Power Control Unit is utilized to apply DC high power stress to the device under test (DUT) and the Heater Control Unit is utilized to apply step temperature stress to the DUT. The system is controlled by a windows-based PC. An internal switching matrix controls to which channel the stress is applied. For our study, an external Keithley 2400 DC source is connected to the Accel-RF system to carry out device characterization. Execution of the Accel-RF system and the external Keithley source are alternated with token files passed between the two. A C++ interface has been developed by J. Joh [27] and is utilized for this project to enable passing of token files to be incorporated into long routines which can run automatically. As shown in Fig. 2-3, this C++ interface enables users to design new experiments easily without changing the structure of the whole program.

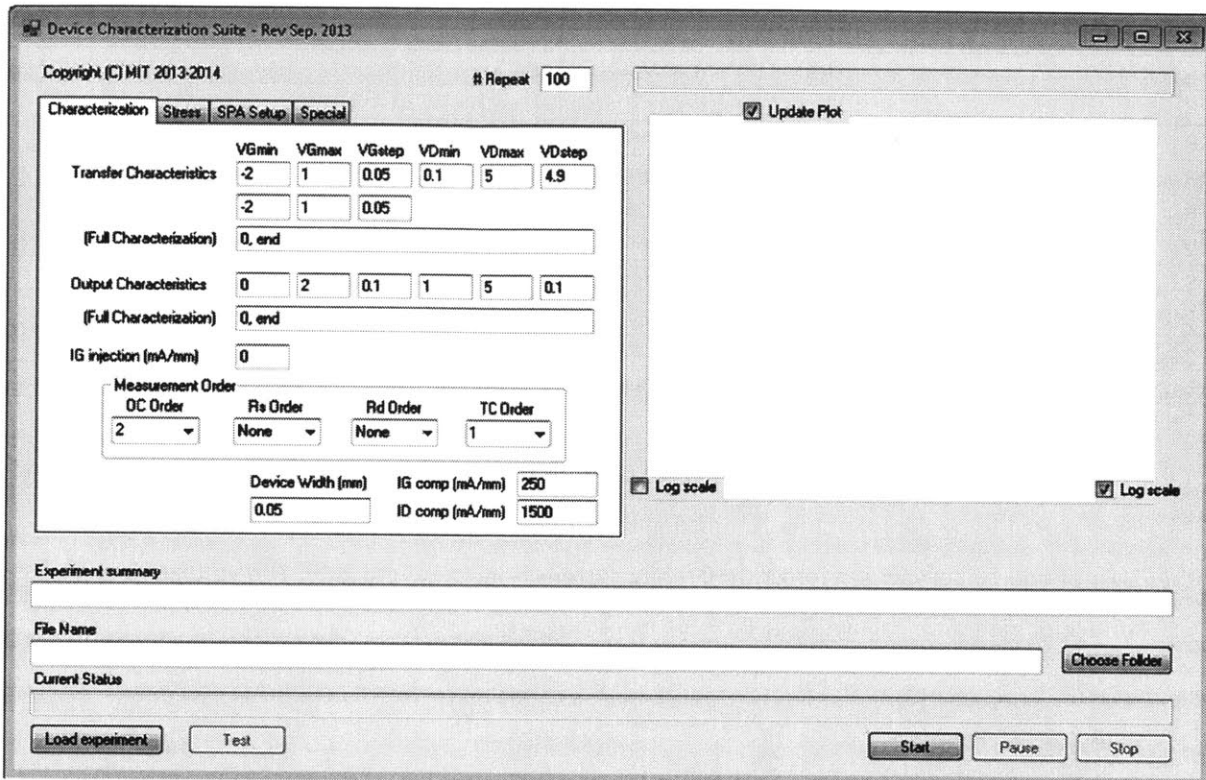

Figure 2-3. Characterization Interface written in C++ which enables alternative controls between the Accel-RF life test system and the external Keithley souce.

2.3.2 Characterization Suite

Since we anticipate the characterization of devices to be repeated many times for our study of device degradation under various stresses, it is important to develop a characterization suite that can accurately reflect device electrical performances even with certain level of degradation. At the same time, the characterization suite must be benign enough such that repeated characterization itself will not significantly degrade the devices. Under this philosophy and after testing, we have adopted a characterization suite that is similar to that in [27].

Parameter	Definition
I_{Dmax}	Drain current at V_{DS} = 5 V and V_{GS} = 2 V
R_S	Source resistance measured with I_G = 20 mA/mm
R_D	Drain resistance measured with I_G = 20 mA/mm
R_{TOT}	Total resistance between drain and source with gate floating
R_{CH}	Channel resistance. $R_{TOT} - R_S - R_D$
V_T	$V_{GS} - 0.5V_{DS}$ when I_D = 1mA/mm at V_{DS} = 0.1 V
SS	Sub-threshold slope at V_{DS} = 0.1 V and I_D = 1 mA/mm
DIBL	$V_{T\|VDS=0.1\,V} - V_{T\|VDS=5\,V}$
g_{mpk}	Peak transconductance dI_D/dV_{GS} at V_{DS} = 5 V
I_{Goff}	Gate current at V_{GS} = 5 V and V_{DS} = 0.1 V

Table 2-1. Definition of device parameters measured.

Table 2-1 shows the definition of various figures of merit to be monitored for our devices. Here, R_S and R_D are measured using the gate current injection technique as described in [29]. In these measurements, the drain or source current are forced to 0 while current is injected into gate. The voltage drop across gate-source or gate-drain, allows R_S or R_D to be extracted respectively.

2.3.3 Device Detrapping

Due to imperfect epilayer growth and some of the unique properties of the AlGaN/GaN heterostructure such as spontaneous polarization and lattice mismatch, both reversible and permanent device degradation take place in GaN HEMTs under stress, as have been demonstrated by several authors [30]–[32]. The reversible device degradation is believed to be caused by surface or bulk defects which can trap electrons and thus alter conduction band discontinuity as well as Schottky barrier height. Some of the typical manifestations of electron trapping in device electrical performance are a decrease in drain current and gate leakage current, an increase in resistance, as well as a negative shift of the threshold voltage. However, these changes are not permanent and do not reflect any structural degradation of the devices. We have sought to develop a technique to detrap those electrons and thus be able to isolate permanent device degradation. Usually, exposure to UV light (of an energy that might depend on device types due to the different energy levels of traps) turns out to be an effective and fast way to detrap electrons. However, since our DUTs are packaged, we have instead adopted a thermal treatment method. Based on repeated tests, we have found that baking at 250 °C for 7.5 hours can completely eliminate electron trapping in our devices.

2.4 Stress Test Methodology

Our stress tests are designed to study device degradation under high-power and high-temperature stress. The DC bias is fixed at a certain level with base plate temperature stepped up to study the dependence of degradation on temperature. To be able to monitor the evolution of various device figures of merit under stress, we would need to pause stress periodically and carry out characterization. Taking into account the fact that prolonged stress would introduce significant electron trapping, we would also need to detrap the devices occasionally in order to distinguish reversible trapping effect from permanent device degradation. Incorporating all these, the flow chart of our original design is shown in Fig. 2-4.

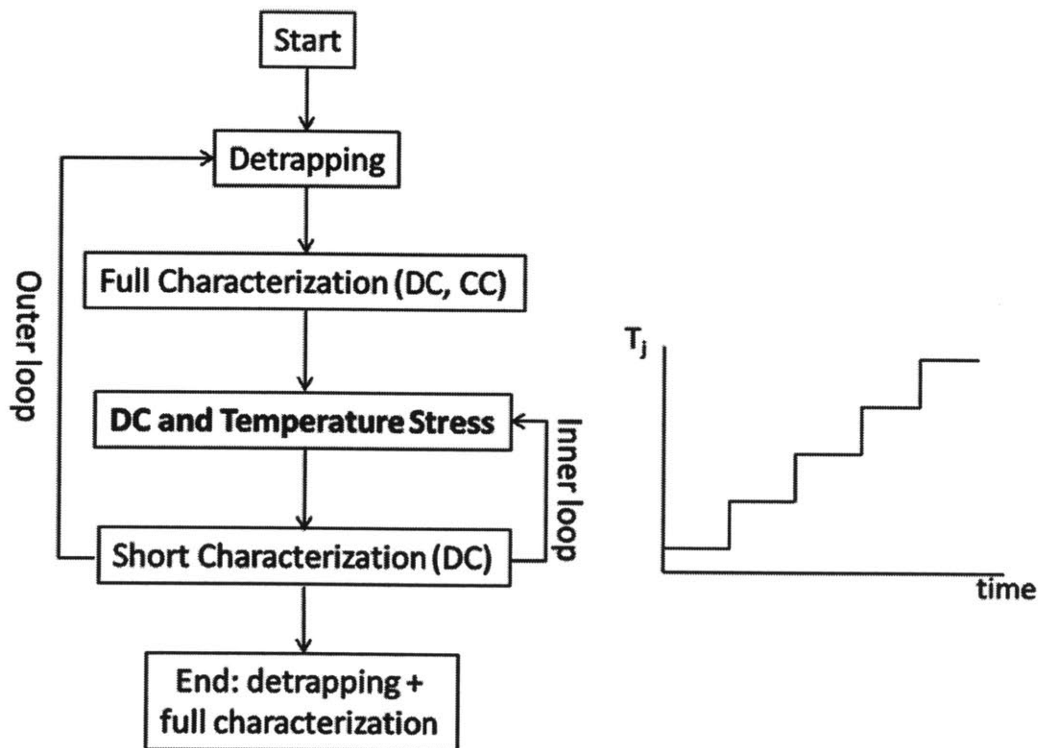

Figure 2-4. Experimental flow chart of the original high-power and high-temperature stress design.

Due to the fact that even a virgin GaN HEMT contains a significant amount of defects capable of trapping electrons, the very first step in our experiments is to bake the device at 250 °C for 7.5 hours in order to fully detrap all electrons. After the device is initialized in this way to a "clean" state, i. e., without any trapped electrons, a full characterization is conducted at T_{base} = 50 °C where various figures of merit are extracted such as I_{Dmax}, V_T, g_{mpk}, I_{Goff}, R_D, R_S, etc. Following this, we start to apply stress with a fixed V_{DS}

and I_{DQ} bias at a certain starting base plate temperature which is chosen to be 50 °C. The stress would last for 20 minutes after which we pause the stress, conduct a short characterization of selected figures of merit at base plate temperature of 50 °C. This stress and short characterization together compose the "inner loop" of the experiment. The entire inner loop repeats 20 times before we stop the stress again, conduct a detrapping step followed by complete I-V sweep characterization. The device is then stressed under the "inner loop" regime again at a higher base plate temperature. The detrapping, full characterization, and "inner loop" together compose the "outer loop". The entire experiment continues with base plate temperature raised up in steps until the device finally blows up.

An improved experimental approach was also developed. After several experiments carried out under the original approach, we found that gate leakage current turns out to degrade rather fast and the degradation saturates above some base plate temperature. The drain current, on the other hand, degrades rather slowly and only after the gate leakage degradation has saturated. This leads us to develop a procedure in which we first degrade the gate current without significant drain current degradation. After gate current degradation has saturated, we then focus on the degradation of drain current. Thus, a two-phase experimental approach is proposed as shown in Fig. 2-5.

In phase I, the big idea is to apply very short high-power step-temperature stress to achieve fast gate leakage current degradation without prominent degradation in drain current. As shown in Fig. 2-5 (a), in this approach, the experiment starts with an initial detrapping step followed by full device characterization. Then we move onto applying stress at fixed V_{DS} and I_{DQ} at a starting base plate temperature of 50 °C. The stress lasts for 3 minutes after which we pause the stress, characterize the device at 50 °C and stress the device under the same condition for another 3 minutes. Following this, the base plate temperature is raised by 20 °C and the process is repeated. We follow the same procedure at each base plate temperature from 50 °C to 220 °C in 20 °C step. After the 220 °C stress, the entire procedure is repeated a second time to make sure that gate leakage current degradation is well saturated. The reason we stop at 220 °C is based on our previous experience such that base plate temperature exceeding 220 °C might lead to ultimate failure of the device.

After phase I, we check to see if gate leakage current has indeed saturated before we move on to phase II. Then different from phase I, the stress period during phase II at each base plate temperature is much longer. As shown in Fig. 2-5 (b), we again start the experiment by a complete detrapping at 250 °C for 7.5 hours followed by DC characterization. Then DC high-power stress at a fixed VDS and IDQ level is applied with a base plate temperature starting from 120 °C. The stress lasts 1 hour after which we

conduct a device characterization at 50 °C. This is repeated 8 times. After the eight one-hour stress periods, we carry out a short detrapping step at 250 °C for 1.5 hours. Instead of the 7.5-hour long detrapping, here for the sake of conserving time, we only bake the device for 1.5 hours. This turns out to partially but not completely detrap the device as we will show in Chapter 3. Then the sequence of eight one-hour stress followed by a short detrapping step is repeated 3 times at the same stress level. That is to say, the device is stressed for a total time of 24 hours at each base plate temperature level. This process continues with the base plate temperature increased in steps until finally the device blows up.

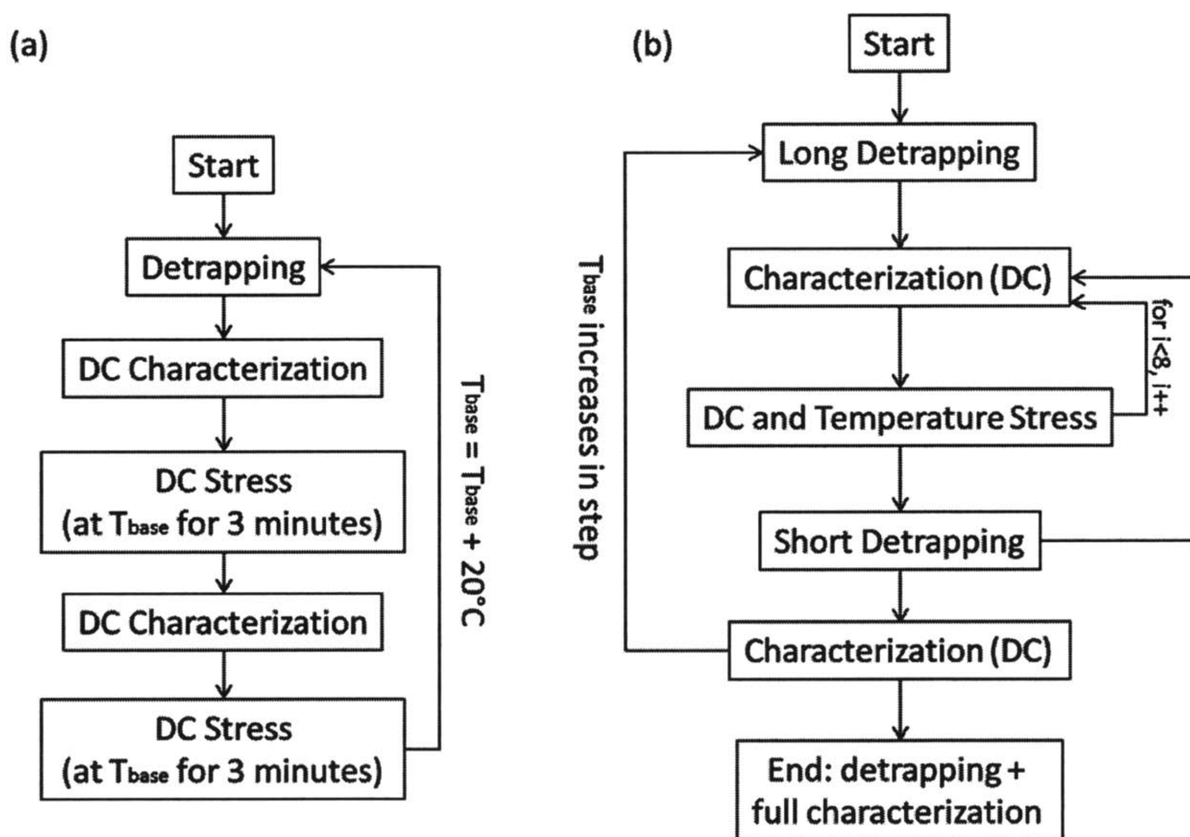

Figure 2-5. (a) Phase I, (b) Phase II, flow chart of the improved experimental design.

2.5 Device Delamination and Surface Examination

An important component of this study involves the examination of the surface of stressed devices in an attempt to correlate electrical degradation with structural degradation. A Zeiss Supra 40 SEM and an AFM-Nanoscope IV Scanned Probe Microscope have been used in device surface analysis. To be able to

observe the actual semiconductor surface, before SEM or AFM scanning, we have conducted a three-step process to remove the metal contacts for source, gate, and drain, as well as the SiN passivation layer [33].

2.5.1 Process and Machines

Similar to [33], SiN is first etched away in HF : H_2O (1:10) solution for 10 minutes following which metal contacts are removed in aqua regia, i. e., HCl : HNO_3 (3:1) under 80 °C for 40 minutes. The last step is the cleaning in H_2SO_4 : H_2O_2 (3:1) for 10 minutes. After this three-step wet etching process is completed, the device is ready for surface examination. The high resolution down to several nanometers of the Zeiss Supra-40 SEM makes it possible for us to scrutinize the device surface efficiently even if the features we would like to observe are on the nanometer scale. The AFM-Nanoscope IV Scanned Probe Microscope, on the other hand, enables quantitative analysis of the features of interest. Both the Zeiss Supra-40 SEM and the AFM-Nanoscope IV Scanned Probe Microscope have Windows-based control software which enables easy operation and data analysis.

2.5.2 Characterization Approach

In our surface characterization approach, we first obtain scans of the entire GaN HEMT on the chip using SEM. We follow this with a detailed SEM examination at the device gate edge on both the source side and drain side across the entire gate finger width. Since our devices have two gate fingers, this process needs to be repeated twice. For our devices stressed under high-power and high-temperature, it has been found that between the two gate fingers, there is always one finger that has more severe structural damage than the other finger. Also, it has been noticed that the center of each gate finger is more vulnerable to physical damage than the two ends of the gate finger.

AFM has higher spatial resolution but is very limited in scope. Because of this, we have focused our AFM analysis on the central region of the gate finger with more physical damage. We conduct multiple 1 x 1 µm scans around the center of gate fingers as representatives of the physical degradation of the device. Data carried by those scans are analyzed and averaged for each device.

2.6 Summary

In this chapter, we have introduced the devices studied in this thesis as well as the experimental techniques that have been utilized. A benign characterization suite is adopted based on the study in [27]. We have gone through the techniques and methodology employed, which are SEM and AFM scans, in analyzing surfaces of stressed devices. We have come out with two experimental designs for step-temperature stress experiments with the device biased in the high-power state. In the next chapter, results of electrical degradation will be shown and the degradation phenomena will be discussed.

Chapter 3. Electrical Degradation

In the previous chapter, we have discussed basic experimental approaches to study the electrical and structural degradation of GaN HEMTs. Now, in this chapter, we will be diving into the detailed results of device electrical degradation experiments and the mechanisms lying behind the observed phenomena.

3.1 Overall Degradation Phenomena

As described in chapter 2, shown in Fig. 3-1 is a typical experiment profile for a high-power and high-temperature stress experiment in our original experimental approach. V_{DS} is maintained at a certain level (40 V or 50 V depending on specific experiment). In or der to maintain I_{DQ} at a relatively constant value around 100 mA/mm, frequently measured values of the actually I_D under the stress voltage is used as a feedback to the Power control unit. If there is any I_D deviation from the target value due to device degradation, this feedback will enable the Power control unit to adjust the applied gate bias V_{GS} accordingly in order to bring I_D back to 100 mA/mm. The base plate temperature, T_{base}, is raised in step from 50 ° C to above 200 °C until the device blows up.

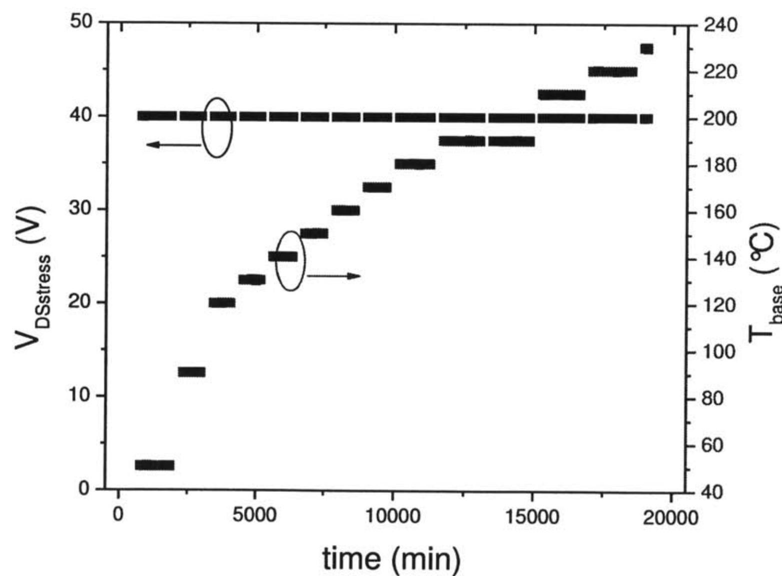

Figure 3-1. High-power and high-temperature stress conditions for the original experimental approach (discussed in section 2.4) to study GaN HEMTs degradation. In this particular case, V_{DS} is kept at 40V with T_{base} stepped up from 50 °C to 210 °C.

Fig. 3-2 (a) shows the typical stress conditions for phase I of the improved approach (discussed in section 2.4). In this case, V_{DS} and I_{DQ} are maintained at 40 V and 100 mA/mm with T_{base} raised from 50 °C to 220 °C in 20 °C steps. The ramping from 50 to 220 °C is repeated several times to make sure that gate leakage current degradation has been driven into saturation. The total stress time at each temperature is kept short at 6 minutes to ensure that no significant drain current degradation happens. Fig. 3-2 (b) shows the stress condition for phase II of the improved approach. Again, V_{DS} and I_{DQ} are maintained at 40 V and 100 mA/mm. T_{base}, however, is raised from 120 °C to 215 °C and the total stress time at each temperature, that is 24 hours or 36 hours depending on specific experiment, is much longer than that in phase I, in order to sufficiently degrade drain current.

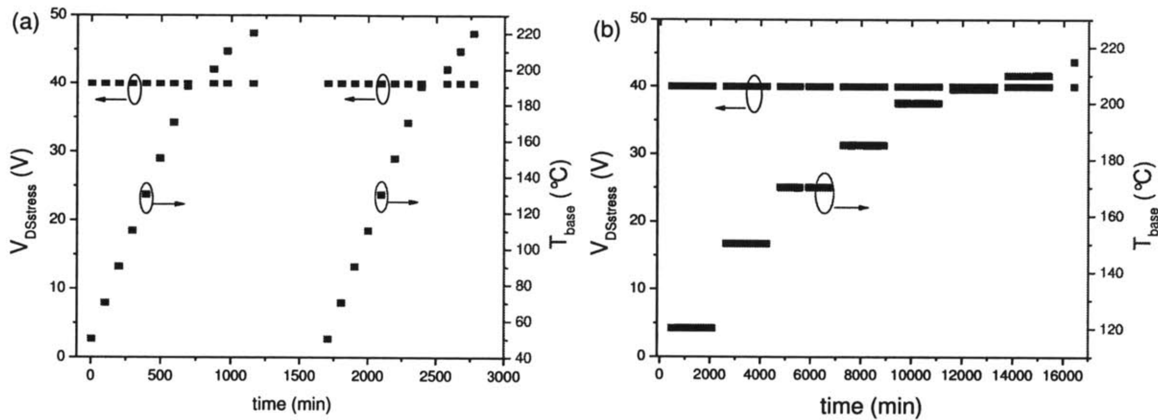

Figure 3-2. Stress conditions for (a) phase I of the improved experimental approach. In this particular case, V_{DS} is kept at 40V with T_{base} stepped up from 50 °C to 220 °C. The entire 50 to 220 °C temperature ramp is repeated twice (b) phase II of the improved experimental approach. In this particular case, V_{DS} is kept at 40V with T_{base} stepped up from 120 °C to 215 °C.

Fig. 3-3 (a) and (b) show the changes in drain current I_D and gate current I_G before and after the application of high-power high-temperature stress for a typical device. This is the result of the combined effects of Phase I and Phase II such that both gate leakage current and the maximum drain current are degraded. From the graph, we see that I_D has decreased by 67% at V_{DS} = 5 V from around 750 mA/mm down to 250 mA/mm. Since the two measurements are carried out after complete detrapping, the change in I_D is due to permanent degradation. From Fig. 3-3 (b), we can notice that the overall gate leakage current has increased by about 2 orders of magnitude. Threshold voltage has shifted in the negative direction (not shown) and the ideality factor has also degraded indicating damage of the Schottky contact.

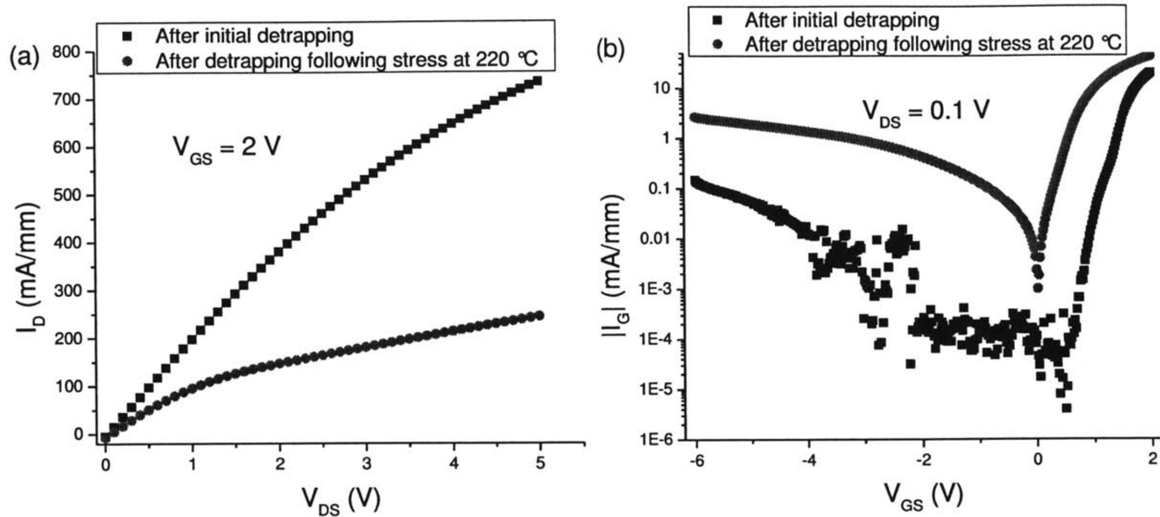

Figure 3-3. (a) Comparison of drain current at the beginning of stress experiment and after higher-power DC stress at 220 °C. Both measurements are carried out after device is completely detrapped by baking at 250 °C for 7.5 hours. The degradation is permanent, absence of electron trapping. (b) Comparison of gate leakage current at the beginning of stress experiment and after high-power DC stress at 220 °C. Both measurements are carried out after device is completely detrapped. Threshold voltage has shifted in the negative direction and the ideality factor has degraded.

3.2 Original Approach

In Chapter 2, we have introduced the stress methodology of our original approach where a device is stressed at a fixed DC level with the base plate temperature stepping up. Under such stress, device degradation happens as manifested through various figures of merit such as I_{Dmax}, I_{Goff}, V_T, R_D, etc. Shown in Fig. 3-4 are the changes in normalized I_{Dmax} and I_{Goff} as the base plate temperature is ramped up for a device labeled MMIC 25 Type B. We can notice from the right graph that below 170 °C, I_{Goff} stays at a relatively constant level. However, starting from 170 °C, I_{Goff} increases dramatically by about three orders of magnitude until T_{base} reaches 190 °C, after which the change in I_{Goff} saturates. Correspondingly, from the left graph, we notice that below 180 °C, I_{Dmax} shows very small degradation which is mainly due to electron trapping. However, starting from 190 °C, significant drain current degradation emerges and by the end of 220 °C stress, the permanent degradation of I_{Dmax} is as high as 67%. Also, by qualitatively comparing the decrease of I_{Dmax} at each base plate temperature level, we can observe that at higher temperatures, I_{Dmax} decreases more. This indicates a thermally activated behavior of I_{Dmax} degradation. Fig. 3-5 illustrates the changes in R_D and R_S of the device under stress. Consistent with I_{Dmax}, R_D shows negligible degradation when T_{base} is below 190 °C and starts to increase dramatically after 190 °C. The

outer loop data, which are represented by points sticking out, show thermally activated degradation trend. R_S, on the other hand, has a much smaller increase compared with R_D. This is different from what have been reported under V_{DS} = 0 V stress where R_D and R_S change in similar ways [10], [11], [23]. However, the result is similar to ON-state experiment reported in [34]. This indicates that the high electric field on the gate edge at drain side might be a significant driving factor for R_D degradation.

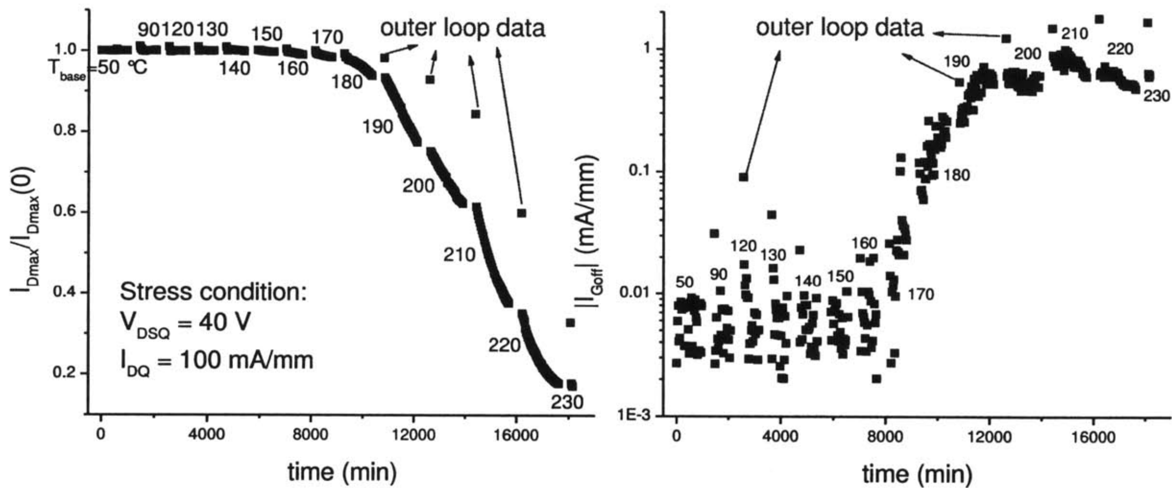

Figure 3-4. Degradation of I_{Dmax} and $|I_{Goff}|$ of MMIC 25 Type B. The points sticking out in the graph are measurements done following device detrapping (denoted as "outer loop data") and reflect permanent device degradation. The more clustered points are "inner loop data" which incorporate both electron trapping and permanent device degradation. Temperatures shown in the graph represent the stress temperature T_{base} which increases in steps.

Besides this experiment, we have carried out same type of high-power high-temperature experiments on more devices. Shown in Fig. 3-6 is the degradation of MMIC 29 Type B. Base plate temperature is raise from 50 °C directly to 190 °C to conserve time since we believe that higher temperature may be able to accelerate the device degradation so that a higher degree of degradation may be induced. From the right graph, we can see that the initial gate leakage current is rather large and the overall I_{Goff} degradation is small compared with MMIC 25 Type B. By the end of the experiment, $|I_{Goff}|$ is still increasing and has not saturated yet. At the same time, as shown in the left graph, the drain current experiences very small degradation and most of it is due to electron trapping. Fig. 3-7 shows the drain and source resistance degradation of the same device. Consistent with I_{Dmax} degradation, both R_D and R_S show negligible degradation.

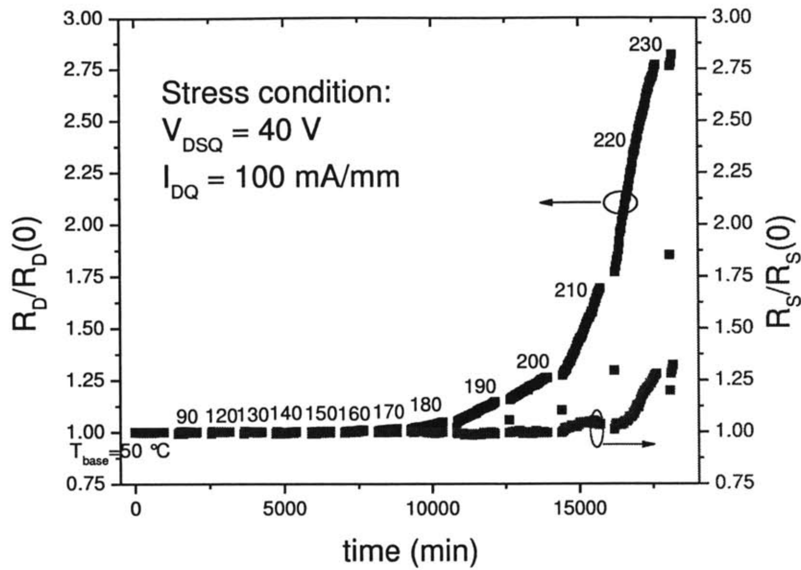

Figure 3-5. Degradation of R_D and R_S of MMIC 25 Type B under high-power and high-temperature stress. After isolating electron trapping effects (as reflected by outer loop data), R_D still increases by about two times. R_S, on the other hand, shows a much smaller increase.

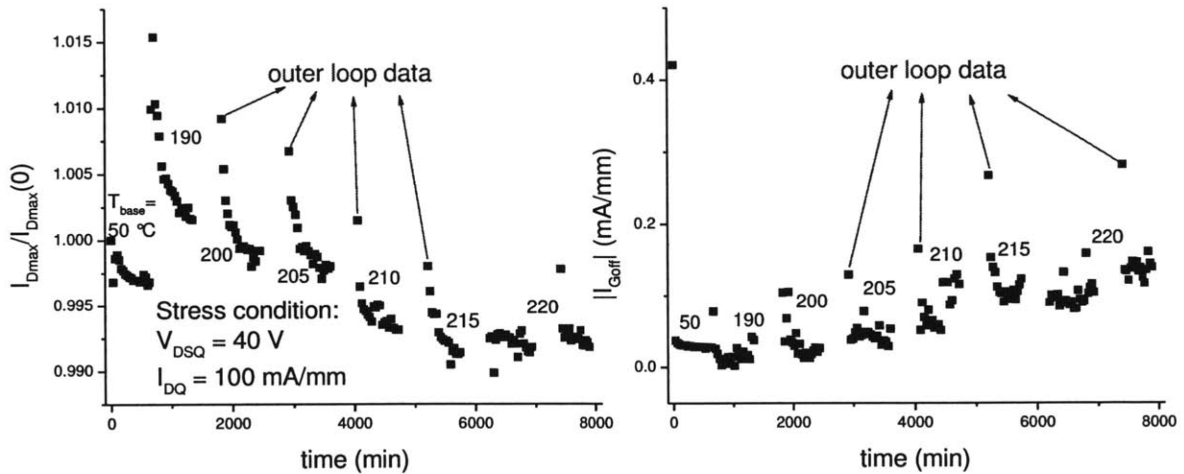

Figure 3-6. Degradation of I_{Dmax} and $|I_{Goff}|$ of MMIC 29 Type B. The points sticking out in the graph are measurements done following device detrapping and represent permanent device degradation. Both I_{Dmax} and I_{Goff} show little degradation.

Another similar stress experiment is carried out on MMIC 15 Type B as shown in Fig. 3-8. Below T_{base} = 120 °C, the drain current shows little increase during each temperature stress cycle. Similarly, the gate leakage current $|I_{Goff}|$ decreases during each temperature stress cycle. These are signs of incomplete detrapping of the device at the start of each temperature stress cycle. This might be due to some variations in the location in energy band and density of trapping sites existing in virgin devices such that

our detrapping technique does not work as well on this device as on others. At higher stress temperatures, permanent degradation of device emerges as the maximum drain current starts to decrease and the gate leakage current starts to increase. However, the overall degradation is small with $|I_{Goff}|$ still increasing at the end of experiment when the device blows up.

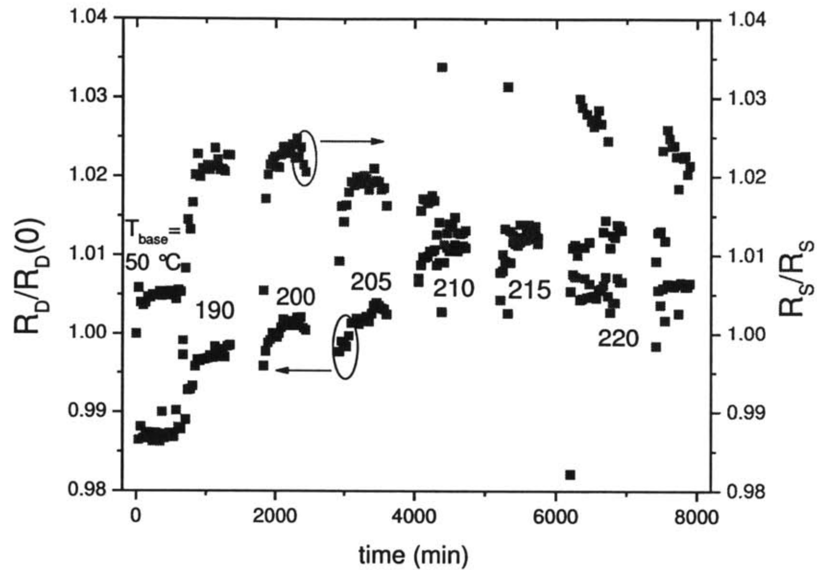

Figure 3-7. Degradation of R_D and R_S for MMIC 29 Type B under high-power and high-temperature stress. The overall degradation for both is negligible.

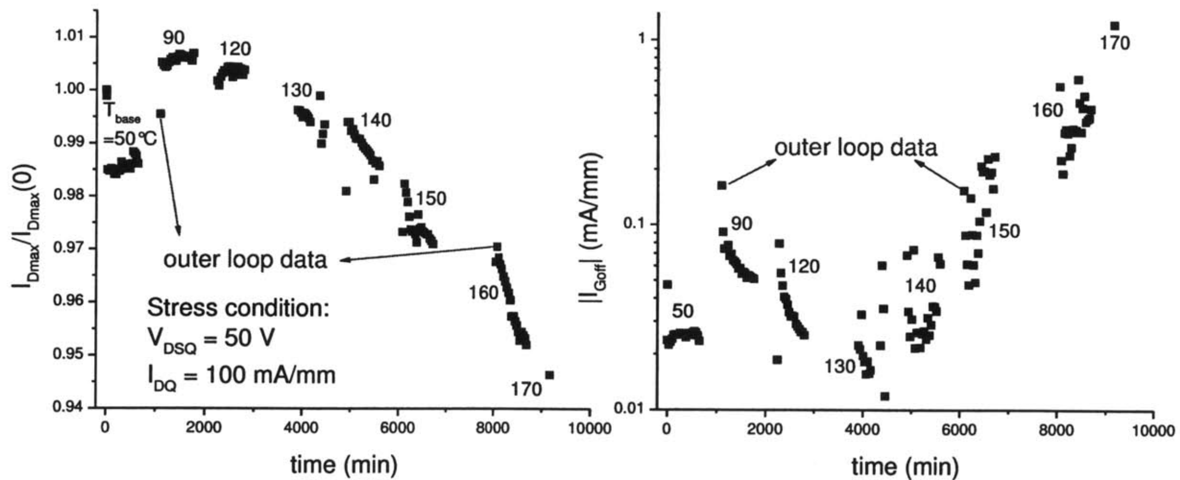

Figure 3-8. Degradation of I_{Dmax} and $|I_{Goff}|$ of MMIC 15 Type B. The points sticking out in the graph are measurements done following device detrapping and represent permanent device degradation. Both I_{Dmax} and I_{Goff} show little degradation.

Shown in Fig. 3-9 is the degradation of the drain and source resistance of the same device. Consistent with I_{Dmax}, R_D exhibits degradation starting from T_{base} = 130 °C and the overall amount of degradation is small. R_S, which is different from R_D, changes in the opposite direction such that by the end of the experiment, it is smaller compared with its initial value. This again indicates that our detrapping technique is not as effective on this device. The overall amount of change is very small for both R_D and R_S.

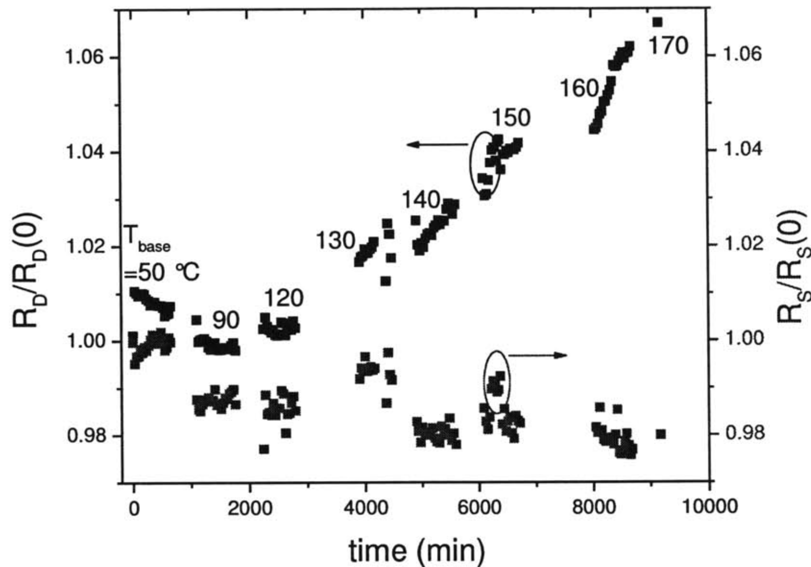

Figure 3-9. Degradation of R_D and R_S for MMIC 15 Type B under high-power and high-temperature stress. The overall degradation for both is negligible and R_S changes in the opposite direction as R_D does.

Yet another stress experiment is shown below in Fig. 3-10. Similar to the experiment conducted on MMIC 29 Type B, the base plate temperature is raised directly to 190 °C after the initial stress period at T_{base} = 50 °C. Looking at the right graph, we notice that gate leakage current has a sudden increase of about 2 orders of magnitude when T_{base} is raised to 190 °C and stays more or less at that level during the following higher temperature stress cycles. The points sticking out correspond to outer loop measurements. The difference between outer loop and inner loop data indicates that traps exist in the device. Correspondingly on the left graph, we can see that during T_{base} = 50 °C stress, the drain current only shows a small decrease. However, starting from T_{base} = 190 °C, significant drain current degradation takes place and the degradation trend continues until the device blows up. One thing that is different from our expectation is that the degradation shown by the outer loop data changes almost linearly with time and this seems to contradict with our previously observed thermally activated degradation.

However, if we think about the temperature steps used here, we will realized that the steps (5 °C) adopted here are very small such that the thermally activated trend may not be measurable.

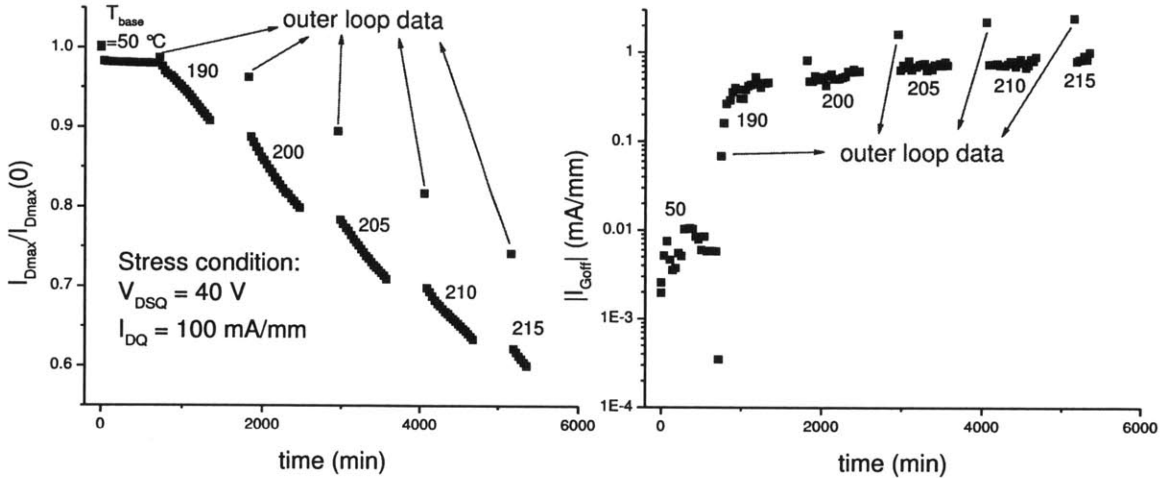

Figure 3-10. Degradation of I_{Dmax} and $|I_{Goff}|$ of MMIC 05 Type D. The points sticking out in the graph are measurements done following device detrapping and represent permanent device degradation. Both I_{Dmax} and I_{Goff} show little degradation at T_{base} = 50 °C. Significant drain current and gate leakage current degradation emerges above T_{base} = 190 °C

Fig. 3-11 shows the changes of R_D and R_S during stress. Consistent with the changes of I_{Dmax}, R_D starts to increase to a significant extend from T_{base} = 190 °C. R_S, as before, shows very limited degradation.

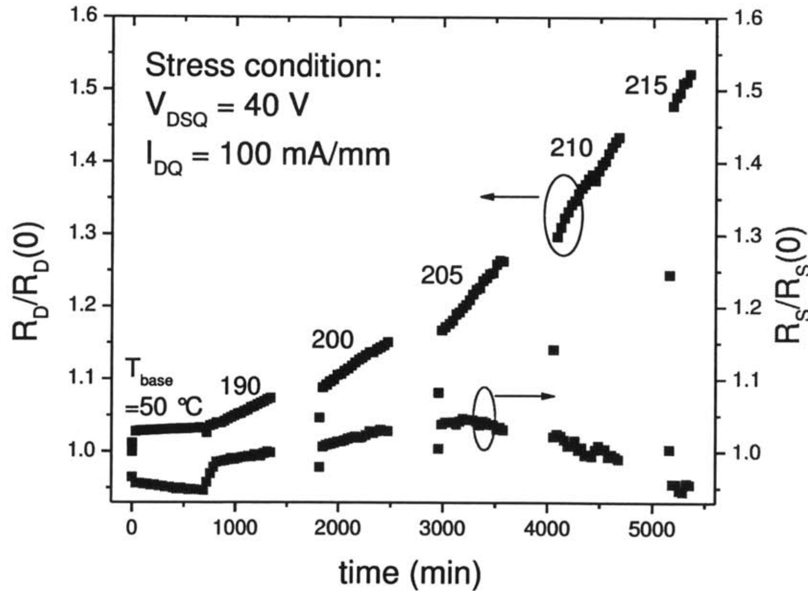

Figure 3-11. Degradation of R_D and R_S of MMIC 05 Type D under high-power and high-temperature stress. R_D starts to increase significantly from T_{base} = 190 °C and R_S shows no degradation.

Up till now, we have shown several experiments under similar stress conditions following the original experimental approach. In some devices, for example, MMIC 25 Type B and MMIC 05 Type D, we see very large drain current degradation together with gate leakage current increasing by several orders of magnitude. In these two experiments, R_D changes in a consistent way with I_{Dmax} and shows a significant increase. R_S, on the other hand, usually stays unchanged. However, this is not always the case. For other experiments, for example, MMIC 29 Type B and MMIC 15 Type B, insignificant degradation is seen in almost all measurable figures of merit. With limited I_{Dmax} degradation, it would be impossible for us to extract activation energy of the device degradation rate.

From the above four experiments, a first look seems to suggest that there is no clear sign at the early stage of an experiment indicating whether or not the device will exhibit significant amount of drain current degradation in the end before it finally blows up under step temperature stress. However, after more closely analyzing the experimental data, we notice that for devices showing larger I_{Dmax} degradation, gate leakage current always endures a large increase at some stage during the experiment and then gate current degradation tends to saturate. To be more precise, a significant amount of I_{Dmax} degradation happens only after the gate leakage current degradation has saturated. This is demonstrated in Fig. 3-12 below. The evolution of I_{Dmax} and I_{Goff} in the four experiments described above is shown where the x-axis represents the absolute value of gate leakage current and the y-axis represents the normalized drain current. Starting from the top left point which is where all the experiments start, initially, the drain current shows little change while the gate leakage current increases. This is reflected in the graph as the relatively flat shape of the curves at the beginning. Up to some point, the degradation of gate leakage is well saturated and it stops increasing further. It is at this point that the drain current starts to decrease. This is reflected in the graph as the curves take on a new branch pointing nearly straight down on the right side of the graph. As can be seen in Fig. 3-12, all four devices obey this trend very well.

To further investigate the permanent degradation of I_{Dmax} and I_{Goff}, the outer loop data is drawn in the same way as shown in Fig. 3-13. We now see that both permanent degradation and trapping related degradation obey this trend. Based on this, we propose that there are two different degradation mechanisms for gate and drain currents which happen in sequence. Similar findings have been demonstrated for device under OFF-state stress in [35].

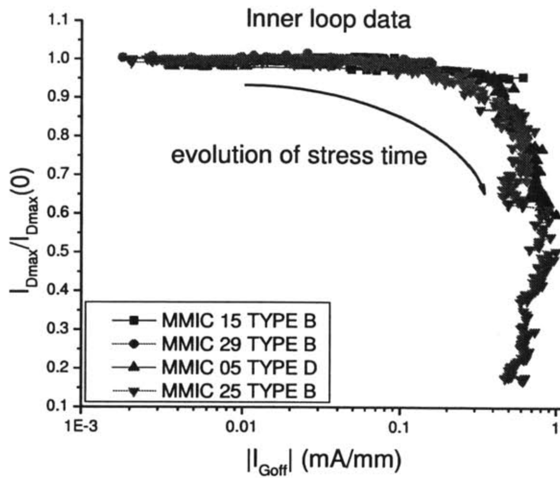

Figure 3-12. I_G vs. I_D degradation drawn with inner loop data. Both trapping related and permanent device degradation are included in the graph.

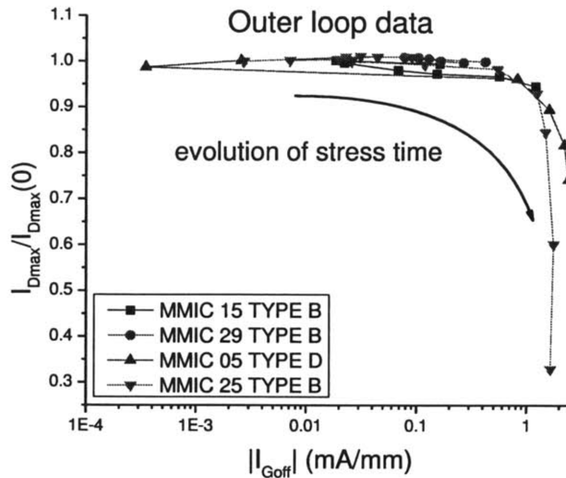

Figure 3-13. I_G vs. I_D degradation drawn with outer loop data. Only permanent device degradation is reflected in the graph.

With this in mind, we need to develop a new stress methodology where, ideally, we will be able to separate the degradation of I_{Goff} and I_{Dmax} and focus on only one degradation mechanism at a time. To achieve this goal, we take advantage of the fact that I_G degradation happens rather fast while I_D degradation takes some time to appear. Hence, we could design a two-phase experiment in which in Phase I, we stress the device for a short time to achieve I_G degradation without introducing any significant I_D degradation. After this during Phase II, we then focus on the degradation of I_D which happens at a lower rate and extract the activation energy of its degradation rate.

3.3 Improved Approach

The detailed stress conditions of the improved approach have been introduced in Chapter 2. Shown in Fig. 3-14 are the changes of I_{Dmax} and I_{Goff} during Phase I of an experiment conducted on MMIC 08 Type D. The device is stressed at V_{DS} = 40 V and I_{DQ} = 100 mA/mm with T_{base} raised from 50 °C to 220 °C in 20 °C steps. The stress time at each T_{base} level is 6 minutes and device is completely detrapped by baking at 250 °C for 7.5 hours before T_{base} is brought to a new level. The 50 °C to 220 °C ramp is repeated twice and is denoted in the graph as 1st cycle and 2nd cycle. This is to make sure that I_{Goff} is fully degraded by the end of Phase I. From the right graph, we can see that a sudden increase of I_{Goff} happens at the end of 1st cycle and during the 2nd cycle, I_{Goff} remains at a relatively constant level. This shows that our goal of

degrading I_{Goff} to saturation is indeed achieved under our improved experimental approach. Now if we look at the left graph which shows the degradation of the drain current, we can notice that the overall degradation by the end of 2nd cycle is very small, i.e., less than 4%. We now can claim that Phase I has successfully achieved our goals.

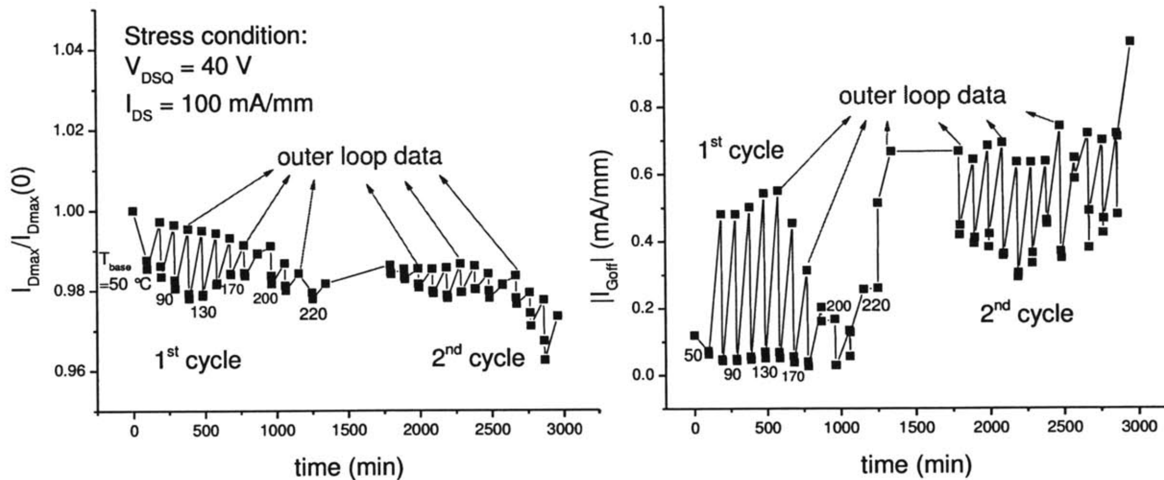

Figure 3-13. Degradation of I_{Dmax} and $|I_{Goff}|$ of MMIC 08 Type D during Phase I of the improved experimental approach.

The next step is Phase II of the experiment which is to study in detail the degradation of I_{Dmax} as well as to extract the activation energy of device degradation rate. The stress conditions are designed such that the electrical stress is the same as that in Phase I, i.e., V_{DS} = 40 V and I_{DQ} = 100 mA/mm. Stress temperature T_{base}, different from that in Phase I, starts at 120 °C and is raised in steps as T_{base} = 150 °C, 170 °C, 185 °C, 200 °C, 205 °C, 210 °C, and 215 °C (temperature at which the device blows up) consecutively. The stress time at each T_{base} is 24 hours and before raising the stress temperature to a higher level, the device is detrapped by baking it at 250 °C for 7.5 hours following which device characterization is performed.

Considering the fact that trapping phenomena is very prominent in AlGaN/GaN HEMTs, a 24-hour consecutive stress may generate traps such that the interpretation of our characterization would be difficult. Under this thought, we have divided the 24-hour stress period into three 8-hour blocks between which a short detrapping is done at 250 °C for 1.5 hours. Compared with the long 7.5-hour baking, this 1.5-hour baking may not be able to completely detrap the device. However, we would expect it to be able to free the majority of electrons trapped.

Shown below in Fig. 3-15 are the evolution of I_{Dmax} and I_{Goff} during Phase II stress. From the right graph showing $|I_{Goff}|$ changing with time, we can once again confirm that the gate leakage current degradation has already saturated and does not change much throughout Phase II stress period. The alternation between the higher points sticking out and the lower more clustered points is a reflection of electron trapping and detrapping. The drain current, which is shown in the left graph, shows a significant amount of degradation. The lowest sets of data points represent characterization done during stress which reflects both electron trapping and permanent device degradation. The high points at the beginning of each temperature level represent characterization done following the long detrapping and thus represent permanent device degradation only. The middle sets of data points represent characterization following the short detrapping. The difference between these data points and the completely trap free measurement proves that a 1.5-hour baking indeed cannot completely detrap devices although the majority of trapped electrons have been freed.

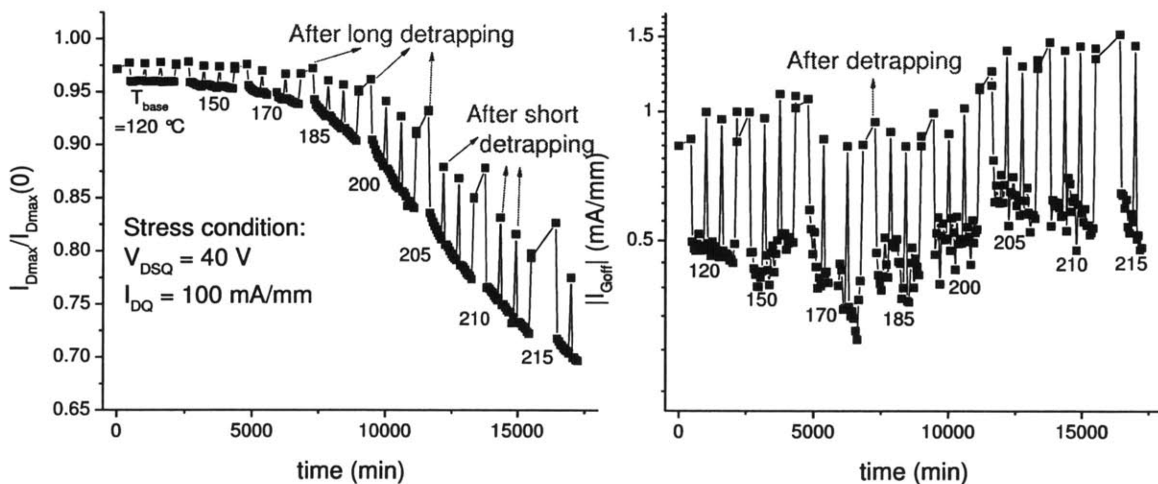

Figure 3-14. Degradation of I_{Dmax} and $|I_{Goff}|$ of MMIC 08 Type D during Phase II of the improved experimental approach.

Now that we have a device degraded in a very clear way, we will be able to study the thermal activation of the degradation. By using the outer loop data (both after long detrapping and short detrapping) or the inner loop data, we will be able to extract the activation energy for the rate of permanent degradation as well as the trapping related degradation. The details will be presented later in section 3.4.

A similar experiment is carried out under the improved approach on a different device MMIC 09 Type D. The electrical stress is the same as in the previous example. During phase I, T_{base} is raised from 50 °C to 210 °C in 20 °C step. The entire 50 °C to 210 °C ramp is repeated twice to fully degrade I_{Goff}. From Fig. 3-

16, we can see that the gate leakage current experiences a sudden increase at the end of the 1st cycle at 210 °C and stays at that high level during the 2nd cycle. I_{Dmax}, as we would expect, shows an overall very small decrease. From these, we know that through Phase I, our goals are achieved.

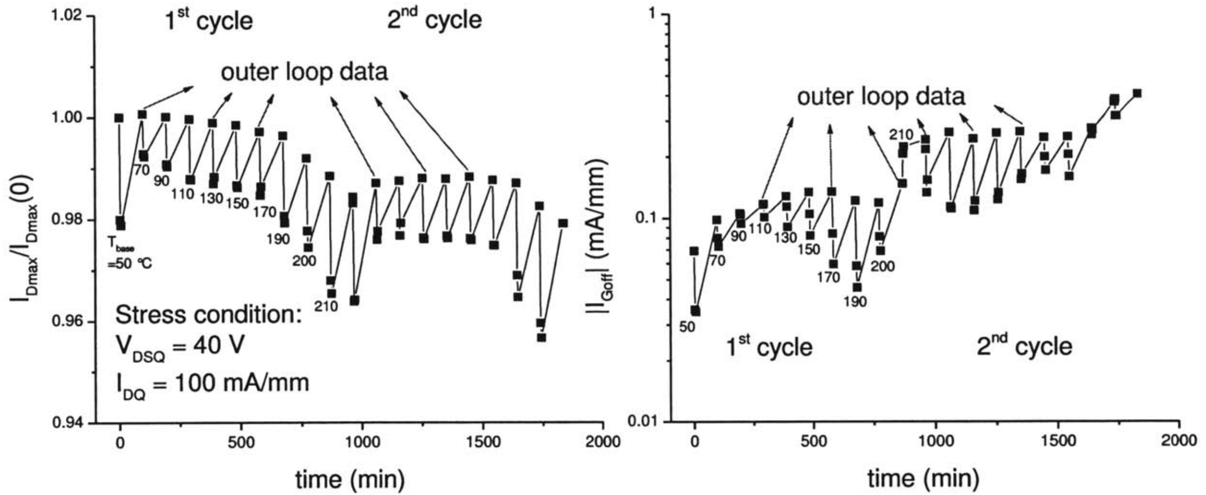

Figure 3-15. Degradation of I_{Dmax} and $|I_{Goff}|$ of MMIC 09 Type D during Phase I of the improved experimental approach.

One difference of this experiment from the previously described one is the detrapping technique we choose to adopt. In order to avoid the confusion introduced by using different baking time for device detrapping, here, we adopt a consistent detrapping technique which is to bake the device at 250 °C for 3 hours throughout Phase II. Also, the stress time at each T_{base} is now 36 hours instead of the 24 hours in the previous example. As shown in Fig. 3-17, which is the degradation of device during Phase I, we can see from the normalized drain current that there are only two sets of data points (instead of three sets of data points in the previous experiment), the higher ones sticking out occasionally and the lower more clustered ones. The two types correspond to outer loop data (device detrapped) and inner loop data respectively. I_{Dmax} shows gradually increased degradation as we increase the base plate temperature. From this, we will be able to extract the activation energy of the degradation rate. I_{Goff}, as shown on the right, stays at a relatively constant level even through there is still some increase. This small increase might actually be the reason that this device has a smaller overall I_{Dmax} degradation compared with the one shown previously.

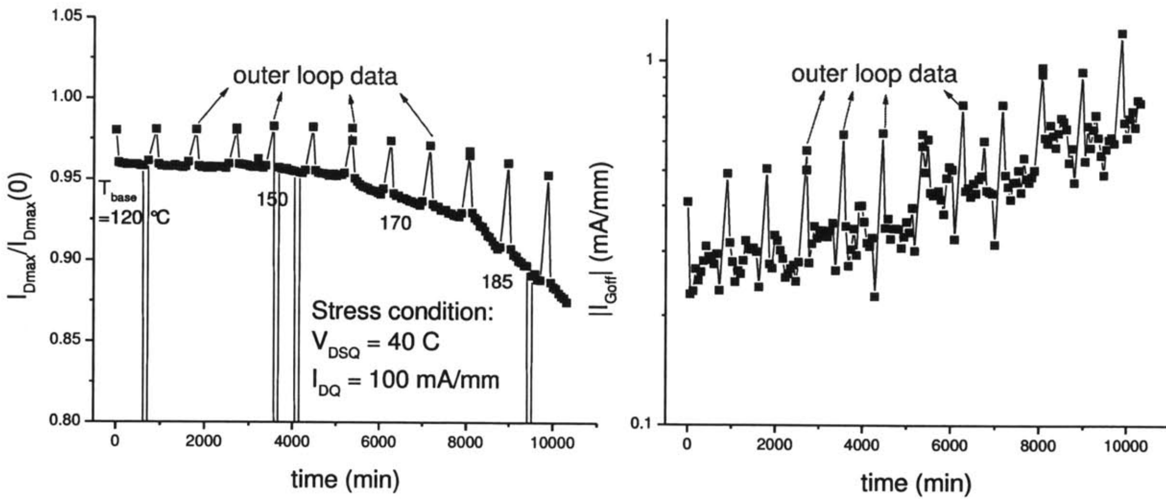

Figure 3-16. Degradation of I_{Dmax} and $|I_{Goff}|$ of MMIC 09 Type D during Phase II of the improved experimental approach.

Yet another experiment under similar stress methodology is carried out on MMIC 11 Type D. This time, a modified Phase I stress methodology is adopted where instead of starting from T_{base} = 50 °C and conducting temperature ramp, initial value of T_{base} = 190 °C is used. Temperature is then increased in 10 °C steps up to 220 °C. The entire 4-step ramp is repeated four times to make sure that I_{Goff} degradation is well saturated. This modification of Phase I is based on our previous observation that I_{Goff} tends to start degrading at a sufficiently high base plate temperature and 190 °C is high enough to degrade I_{Goff} but not too high such that the device might blow up.

The experimental result of Phase I stress is shown in Fig. 3-18. I_{Goff} does not show a very clear increasing trend. The overall change after the four temperature ramps is around an order of magnitude increase. However, since the value does not change much during the fourth ramp, we conclude that the degradation has saturated and we then move onto Phase II. As a supplement, shown in the left, I_{Dmax} has a very small change due to this Phase I stress (about 1% according to the detrapped measurements) and our goal of not degrading drain current to any significant extent is achieved.

We then proceed with Phase II stress. Similar to the experiment conducted on MMIC 09 Type D, base temperature is stepped up from 120 °C, followed by 150 °C, 170 °C, 185 °C, 200 °C, 210 °C, and stops at 220 °C where the device blows up. At each temperature, a total length of 36 hours of DC stress is applied. The 36-hour stress is divided into three periods between which a 3-hour baking at 250 °C is conducted to detrap the device. As shown in Fig. 3-19 in the left, I_{Dmax} starts to degrade from 150 °C and as T_{base} increases, the degradation is accelerated. This is similar to what we have been observing so far

under the improved stress methodology. If we look at the evolution of I_{Goff}, however, we notice something that is different from the previous experiments. Here, we find that gate leakage current, after remaining relatively constant with T_{base} below 185 °C, starts to increase again once T_{base} exceeds the value. This indicates that our stress in Phase I is not complete and the degradation of I_{Goff} has not entered the real saturation regime. This can be due to variations in the initial conditions of GaN HEMTs. From this, we see that the initial conditions can significantly affect how the device performs under stress test.

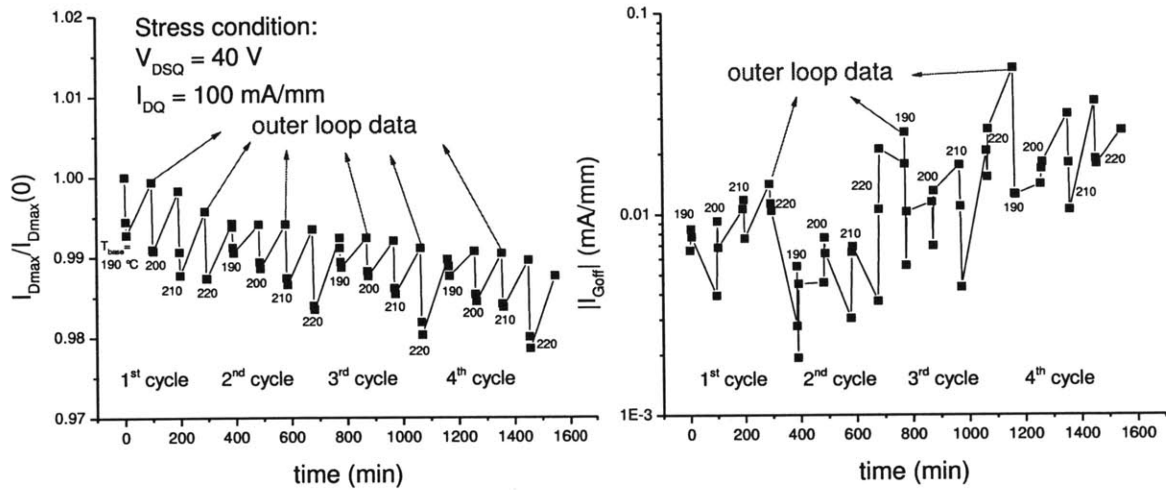

Figure 3-17. Degradation of I_{Dmax} and $|I_{Goff}|$ of MMIC 11 Type D during Phase I of the improved experimental approach.

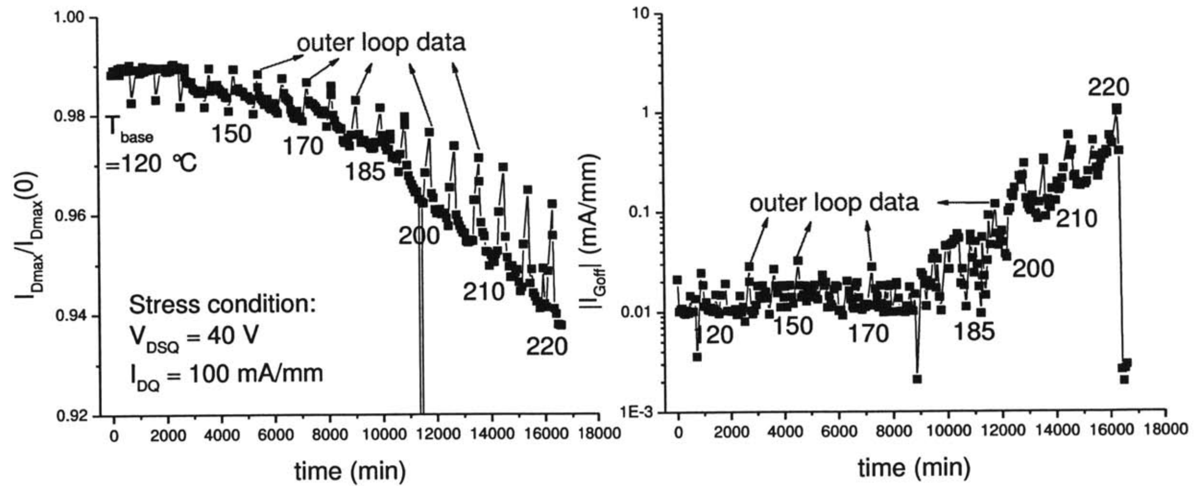

Figure 3-18. Degradation of I_{Dmax} and $|I_{Goff}|$ of MMIC 11 Type D during Phase II of the improved experimental approach.

Up to this point, we have seen three experiments conducted under the improved experimental approach. They all follows pretty well with our previous observations where significant I_{Dmax} degradation happens only after I_{Goff} degradation is saturated. If we plot Phase I and Phase II of the three new experiments together with the previous four experiments under the original approach in a similar way as shown in Fig. 3-12 and Fig. 3-13, we get the results shown in Fig. 3-20.

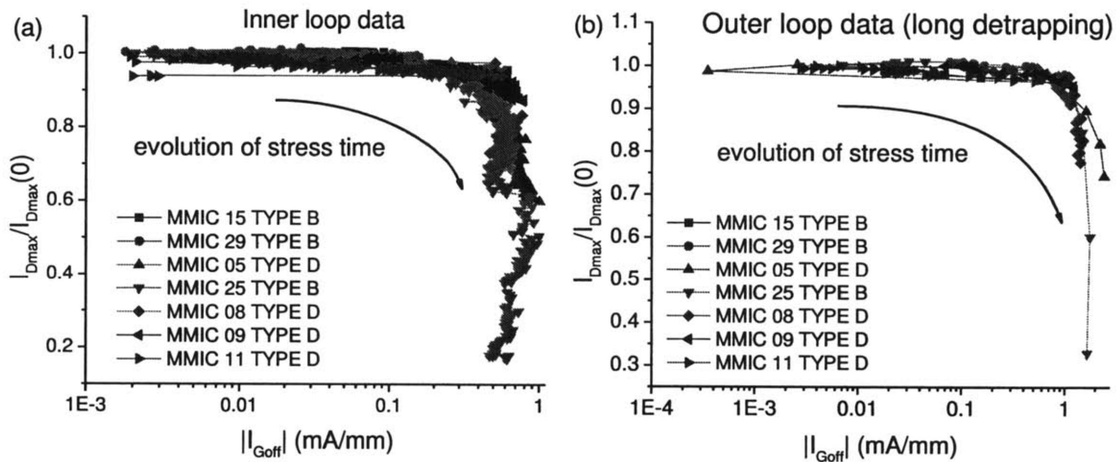

Figure 3-20. I_G vs. I_D degradation drawn with (a) inner loop data where both trapping related and permanent device degradation is included (b) outer loop data where only permanent device degradation is reflected. Results of the four experiments under the original experimental approach as well as the three experiments under the improved approach are shown.

In Fig. 3-20 (a), similar to Fig. 3-12 in section 3.2, the evolution of I_{Dmax} and I_{Goff} degradation is graphed on the same plot. Starting from the top left point (where stress experiments start), significant $|I_{Goff}|$ increase happens first with I_{Dmax} decreasing by only a small amount. Then at some later time when I_{Goff} degradation is saturate, I_{Dmax} degradation takes off. The almost abrupt turning in the graph clearly demonstrates these two consecutive degradation events. If we now look at Fig. 3-20 (b) which is the evolution of I_{Dmax} and I_{Goff} permanent degradation measured after device is detrapped, we observe again the clear chronological sequence of $|I_{Goff}|$ increase followed by the decrease in I_{Dmax}. This happens in all our seven experiments. As we show in Chapter 4, the two different degradation mechanisms correspond to different physical degradations of the device channel region which also happen in a sequential manner.

3.4 Activation Energy Extraction

One of the main goals of our stress experiments is to study the role of junction temperature in accelerating the overall device degradation and to enable the extraction of activation energies of degradation rate from measurements on a single device. The well-developed conventional way of extracting activation energy involves long-term accelerated life tests on a large amount of devices. The problem with this approach is such that at each stress temperature, a different device is needed and the initial performance variations among the virgin devices cannot be corrected for. This means that we have no way to check whether the device degradation at each temperature is unique to the specific device being tested or is a general phenomenon to all devices and is related to the specific stress temperature adopted. Another problem is that as we increase T_{base} in these life test experiments, there might be different degradation mechanisms dominant at different temperature. By constructing Arrhenius plot from high temperature stress experiments on a range of devices, each of which represents degradation rate at a certain stress temperature, all the ambiguities pointed out above may lead to a range of possible activation energies instead of a definite value [36]. Under the consideration of conserving devices and making sure the extracted activation energy indeed represent all the device degradation mechanisms in a properly weighted manner, our developed technique is of great value.

Recall that in section 3.2 and 3.3, DC high-power stress together with high temperature stress in a stepped temperature manner enables evaluation of degradation rate at various temperature levels from a single device. With the improved approach discussed in section 3.3, we are able to separate I_{Goff} and I_{Dmax} degradation so that prominent I_{Dmax} degradation can be produced under our stress methodology and the activation energy of I_{Dmax} degradation rate can then be extracted. In the following paragraphs of this section, details about the extraction of activation energy as well as the physical meaning of our extractions will be discussed.

An Arrhenius plot displays the logarithm of a kinetic constant ($\ln k$) plotted against inverse temperature. The Arrhenius equation can be written as,

$$k = Ae^{-E_a/k_B T} \tag{3.1}$$

where k is the kinetic constant, A is a pre-exponential factor, k_B is the Boltzmann constant, and E_a and T are the activation energy and temperature respectively. The traditional methodology to extract the

activation energy of device degradation rate involves measurements at different temperatures on different devices. Each device corresponds to a distinct stress temperature. The kinetic constant is often choose to be the time needed to achieve a certain degree of device degradation, say, time needed to achieve 10% degradation of I_{Dmax}. By reformatting the Arrhenius equation, we obtain,

$$\ln(k) = \ln(\mathrm{A}) - \frac{1}{k_B T} E_a \tag{3.2}$$

By conducting long-term experiments and obtaining (k, T) pairs, we can then construct the Arrhenius plot.

Recall that our designed experimental approach is to stress the device at different temperature T_{base} and measure the degradation rates of various FOMs at those temperatures. In this way, our new definition of Arrhenius plot can be defined as,

$$\ln(\frac{1}{|slope|}) = E_a(\frac{1}{k_B T_j}) + C \tag{3.3}$$

where $slope$ is the rate of change of the physical variable of interest. For example, in extracting the activation energy of I_{Dmax} degradation, $slope = \frac{\partial I_{D\max}}{\partial t}$. The other variables are: E_a represents the activation energy, k_B represents the Boltzmann constant, and T_j is the device junction temperature. Another issue worth pointing out here is the value of T_j used in the formula. Recall that in section 3.2 and 3.3, base plate temperatures were clearly specified in all the experiments. However, due to the fact that under high-power, device self-heating can be significant so that the actual junction temperature is likely to be not equal to the base plate temperature T_{base}. To correct for this, we have adopted a thermal model which incorporates both the base plate temperature and device self-heating and returns a more realistic junction temperature T_j as the output.

Starting with MMIC 25 Type B, we have shown before that the experiment is carried out under the original approach and for that particular experiment, significant I_{Dmax} degradation is observed. This large I_{Dmax} degradation turns out to enable very good fitting to the exponential relation inherent in the Arrhenius plot. As shown in 3-21 (a), E_a's for both the I_{Dmax} and R_D are extracted. Degradation rates of both are calculated from inner loop data which indicates that both electron trapping related

degradation and permanent degradation are included in the E_a's that we have obtained. This particular experiment gives an activation of 0.58 eV for the drain current and 1.00 eV for the drain resistance. The relatively large discrepancy of the two E_a's is mainly due to the complications introduced by trapping related degradation. Since traps exist in different energy levels as well as different positions inside the heterostructure, it is hard to interpret the activation energies. What is more, trapping and detrapping of electrons happen at different rates under different stress temperatures making it hard to interpret E_a for trapping related degradation in a consistent way. All these motivate us to study the outer loop data which reflects permanent device degradation only. In Fig. 3-21 (b) is the Arrhenius plot of I_{Dmax} and R_D with outer loop data. A much larger value of E_a for I_{Dmax} is obtained this time where we have 0.94 eV. This value turns out to be close to the reported value on similar device technologies [37] obtained from conventional long term life test experiments. The activation of R_D is close to that of I_{Damx} suggesting a similar degradation mechanism.

Under the original approach, the other three experiments introduced in section 3.2 have either too small a drain current degradation or too small a temperature step utilized which leads to insignificant thermally activated degradation. This means that trying to extract activation energies from these three experiments will lead to results with limited validity. So we proceed to the experiments under the improved approach. Actually one might recall that this failure of the original approach to guarantee E_a extraction is one of the important motivations for us to develop the improved approach at all.

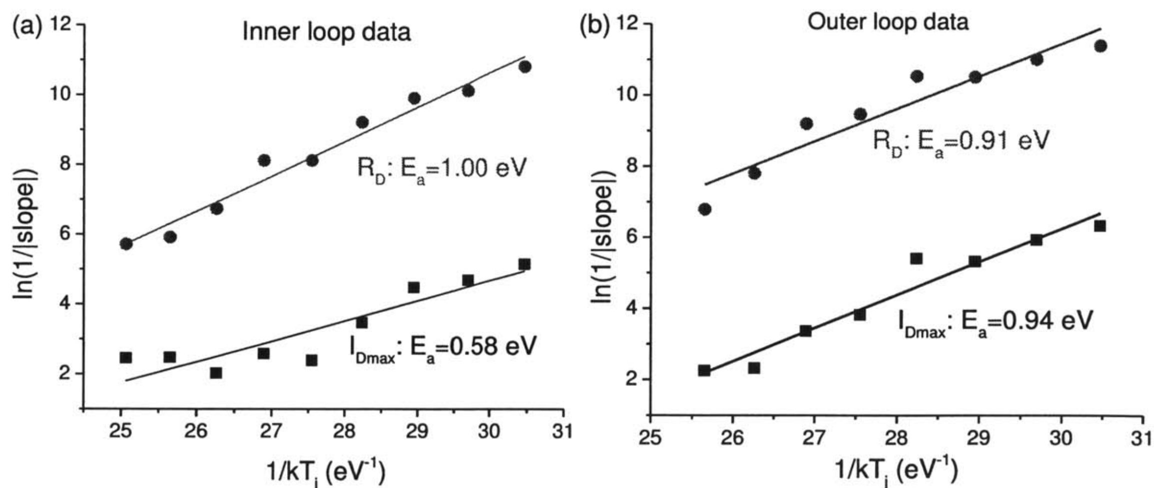

Figure 3-19. Arrhenius plot of I_{Dmax} and R_D for MMIC 25 Type B, where the points at each temperature T_j is defined as the rate of change of variables during that specific temperature. (a) E_a extracted from the inner loop data reflecting both trap related and permanent degradation mechanisms (b) E_a extracted from the outer loop data reflecting only permanent device degradation.

Shown below in Fig. 3-22 (a) is the Arrhenius plot for MMIC 08 Type D constructed from inner loop data of Phase II of the experiment. Similar to what has been explained previously, the E_a's here reflect both trapping related and permanent degradation. Again, E_a for I_{Dmax}, which is 0.43 eV here, is small. E_a for R_D, different from what we have seen before in MMIC 25 Type D, is close to the E_a for I_{Dmax}. As has been brought out before, trapping and detrapping of electrons during stress experiment makes the interpretation of the extracted E_a's very difficult. Evidence supporting this argument is the observation of enhanced detrapping at higher stress temperatures. At high junction temperature T_j, instead of keep increasing, the degradation rates for both I_{Dmax} and R_D decrease. This is reflected by the bending up at high T_j shown in Fig. 3-22 (a). This variation in electron detrapping rate supports our claim that E_a extracted from inner loop data does not accurate reflect the real device degradation rate.

To obtain more understanding of the temperature dependence of permanent device degradation, we have constructed the Arrhenius plot using the outer loop data (after the 7.5-hour long detrappings). As shown in Fig. 3-22 (b), this time, an activation energy of 1.04 eV for I_{Dmax} is obtained which even better approaches the reported E_a for a similar technology [37]. E_a for R_D, which is a little smaller than the one for I_{Dmax} but does not significantly deviate from it, suggests again that I_{Dmax} and R_D probably have the same physical degradation mechanism.

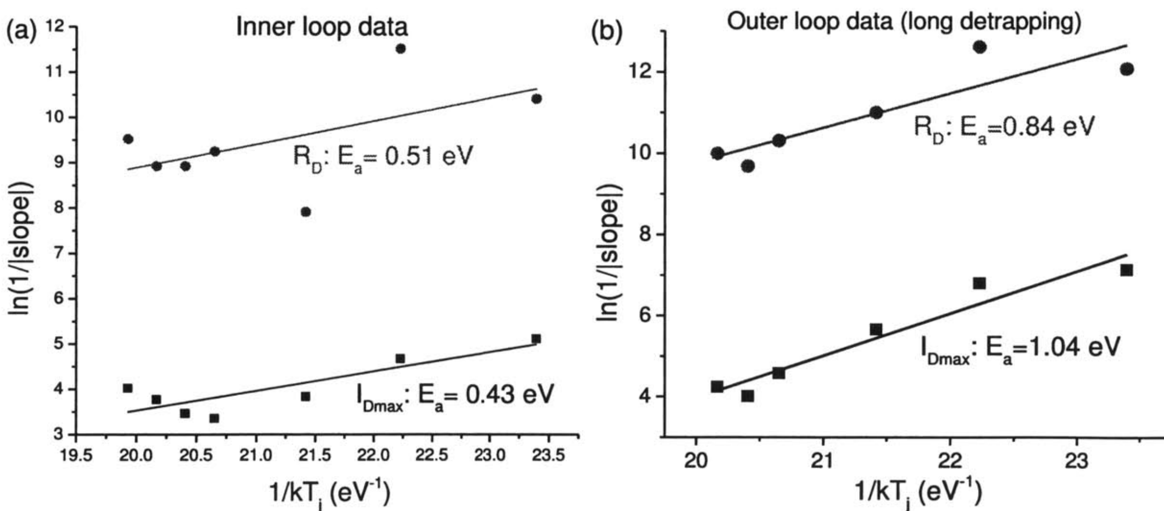

Figure 3-20. Arrhenius plot of I_{Dmax} and R_D for MMIC 08 Type D (experiment conducted under the improved stress approach), where the points at each temperature T_j is defined as the rate of change of variables during that specific temperature. (a) E_a extracted from the inner loop data reflecting both trap related and permanent degradation mechanisms (b) E_a extracted from the outer loop data reflecting only permanent device degradation.

Another experiment under the improved approach which is MMIC 09 Type D is also analyzed and E_a's for I_{Dmax} and R_D are extracted. Fig. 3-23 (a) shows the activation energy extracted from inner loop data which means electron trapping related degradation is included besides what matters more, i.e., the permanent degradation. The much larger E_a for both I_{Dmax} and R_D compared with previous experiments suggests that for this specific experiment, permanent degradation has a more weighted value in contributing to the activation energy. A more direct understanding of permanent device degradation is illustrated by Fig. 3-23 (b). Here, each data point corresponds to the rate of change of physical variables after device is detrapped. The E_a's reflect how permanent degradation is accelerated as temperature increase. I_{Dmax} seems to indicate that the degradation process is much strongly thermally activated than what have been revealed in our previous experiments. There are several possible reasons for this abnormality. First of all, if we recall the evolution of I_{Goff} during Phase II discussed in section 3.3, instead of staying flat as what we would expect, $|I_{Goff}|$ actually increases throughout the stress period although to a relatively small extent. This means that the gate leakage current degradation is not completely saturated. A result of this is that our extraction of activation energy for I_{Dmax} degradation mechanism may include some effect of I_{Goff} degradation mechanism. Secondly, the device in this experiment blows up at a relatively low junction temperature such that we only have three data points in extracting E_a's. This small number of sampling points can lead to inaccuracies.

Another experiment which is introduced in section 3.3 is shown below in Fig. 3-24. Again, E_a extracted from inner loop data is shown first followed by that extracted from the outer loop data. As expected, E_a's from inner loop data are small which indicates that trapping plays an important role in degrading device performance and this process is only weakly dependent on temperature. The outer loop data gives us activation energy of 1.04 eV for I_{Dmax} and 0.53 eV for R_D. This is extremely consistent with what we have been observing so far and also fit the reported E_a extracted from the conventional method [37] very well.

So far, we have shown activation energies of device degradation rate for four different experiments. Three of them show relatively consistent values of E_a for I_{Dmax} which are all somewhere around 1 eV. This turns out to be very close to the value reported in the literature for a similar technology under the conventional accelerated life test experiments. The other experiment, however, produces an E_a for I_{Dmax} of 1.87 eV, which is almost twice as large. As we have mentioned, one possible reason for this abnormally high value is that device under this specific experiment blows up at a low stress temperature and leaves us with only three data points to extract the activation energy. This lack of enough data can

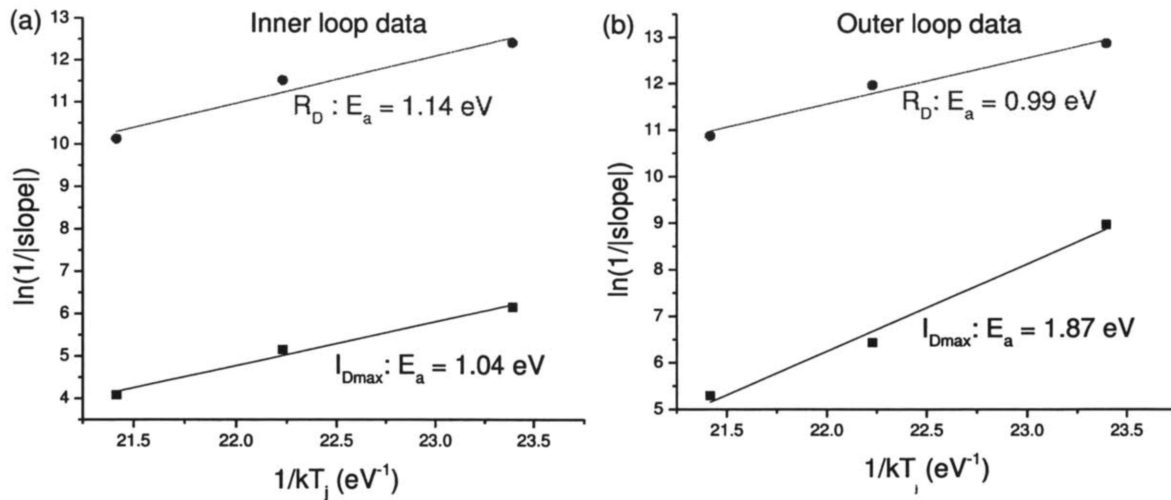

Figure 3-21. Arrhenius plot of I_{Dmax} and R_D for MMIC 09 Type D (experiment conducted under the improved stress approach), where the points at each temperature T_j is defined as the rate of change of variables during that specific temperature. (a) E_a extracted from the inner loop data reflecting both trap related and permanent degradation mechanisms (b) E_a extracted from the outer loop data reflecting only permanent device degradation.

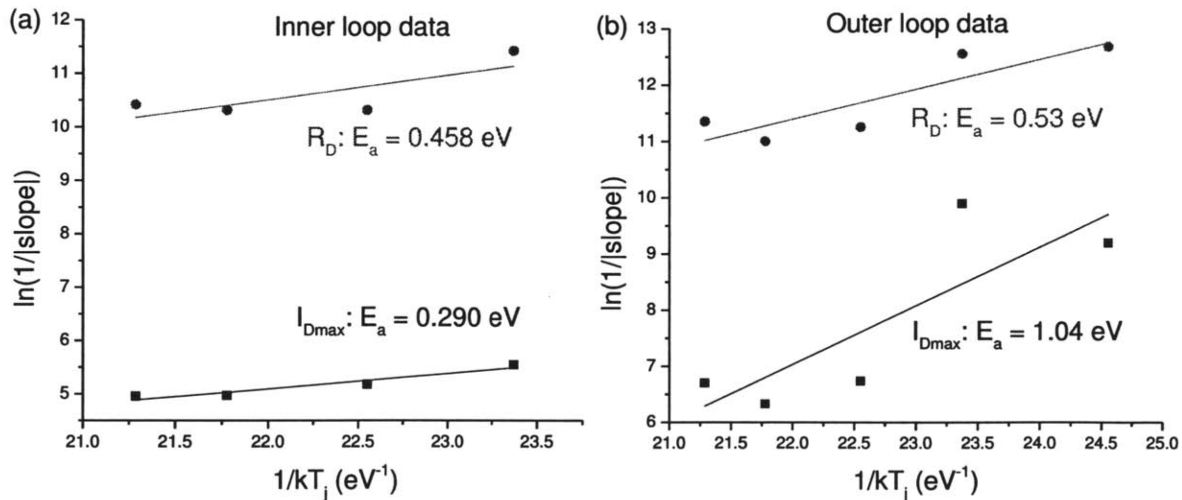

Figure 3-22. Arrhenius plot of I_{Dmax} and R_D for MMIC 11 Type D (experiment conducted under the improved stress approach), where the points at each temperature T_j is defined as the rate of change of variables during that specific temperature. (a) E_a extracted from the inner loop data reflecting both trap related and permanent degradation mechanisms (b) E_a extracted from the outer loop data reflecting only permanent device degradation.

result in inaccuracy. In general, the inner loop data, which reflect both trapping related and permanent degradation, returns a rather broad range of activation energies and as we have analyzed, is not a reliable way to reveal activation energy of a certain technology. The outer loop data is capable of reflecting activation energy rather accurately.

To further verify the effectiveness and accuracy of our designed stress methodology in extracting activation energy, we suggest that more experiments to be conducted. Also, experiments using devices from various processing techniques with different activation energies as needed to verify the versatility of our methodology.

3.5 Summary of Key Findings

In this chapter, we have shown the electrical degradation of GaN HEMTs under DC high-power and high-temperature stress conditions. Experiments under the original approach present some inconsistencies where some devices demonstrate significant drain current degradation while others shows very small overall changes in drain current. After careful analysis, we have found that larger drain current degradation is possible only if gate leakage current degradation is saturated. With this thought, we have devised an improved approach where the stress experiment is separated into two phases. During phase I, we degrade I_{Goff} to saturation so that during Phase II, only I_{Dmax} degradation takes place. Under this approach, we are able to extract activation energies of degradation rate of I_{Dmax} and R_D. We have also shown that trap related degradation is less dependent on temperature which is reflected as the relatively small E_a values obtained with inner loop data. Permanent degradation, on the other hand, is strongly thermally activated. The range of E_a's we have obtained from experiments, i.e., 0.94 eV to 1.04 eV, reveals E_a's very close to the values obtained using conventional method on a similar device technologies.

Chapter 4. Structural Degradation

In the previous chapter, we have discussed degradation of various device electrical figures of merit under high-power and high-temperature stress. The activation energy we are able to extract from a single device turns out to agree well with values obtained from conventional methods on a similar technology. In section 3.3, we briefly mentioned that the two sequential degradation mechanisms correspond to physical degradation which also happens sequentially. In the following sections of the chapter, we will explore structural damage in detail.

4.1 Overall Degradation Phenomena

All the devices studied in this project are packaged GaN amplifiers in MMIC form. Device structures have been introduced in section 2.2. In order to examine the device semiconductor surface under SEM and AFM, metal contacts for source, drain, and gate as well as the passivation layer on the top need to be removed. We have introduced in section 2.5.1 a three-step wet etching process to achieve this goal.

In general, we have found a consistent structural degradation pattern which is related to the electrical degradation across various tested devices. For devices with small overall I_{Dmax} degradation, we observe shallow grooves forming at the gate edge on the drain side. Fig. 4-1 is an SEM picture of the semiconductor surface of degraded device MMIC 29 Type B in which we see a permanent I_{Dmax} degradation of less than 1%. In this device, we find that a continuous shallow groove forms alone the gate edge.

On the other hand, for devices which exhibit significant permanent I_{Dmax} degradation, deep pits form at the gate edge on the drain side extending throughout the entire gate width. At some locations alone the gate width, the deep pits even merge into trenches. Illustrated in Fig. 4-2 is a SEM picture of the surface of device MMIC 05 Type D. We know from section 3.2 that the overall permanent I_{Dmax} degradation for the device is around 25%. In the figure, we can see that pits form at the gate edge and the dark color indicates that these pits are pretty deep. At some specific locations along the gate width, trenches that result from pits merging with each other are observed. Fig. 4-3 demonstrates such a case.

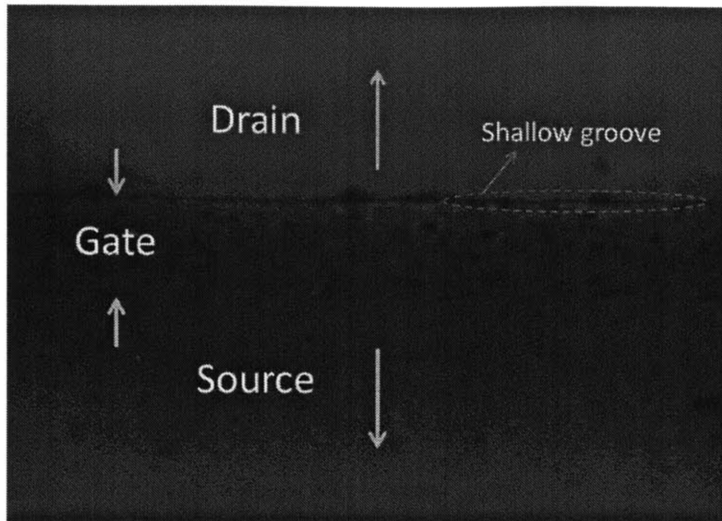

Figure 4-1. SEM picture of the surface of MMIC 29 Type B. The overall permanent I_{Dmax} degradation is less than 1%. A shallow groove forms alone the gate edge on the drain side.

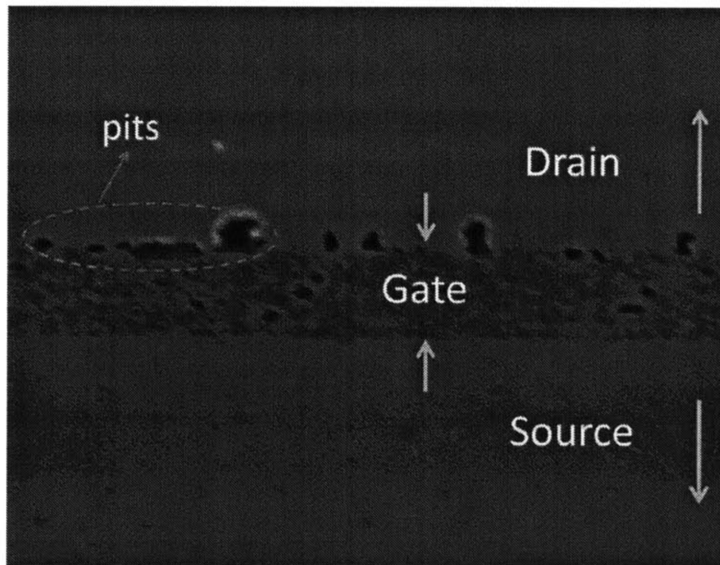

Figure 4-2. SEM picture of the surface of device MMIC 05 Type D. The overall permanent I_{Dmax} degradation is around 25%. Pits form at the gate edge on the drain side.

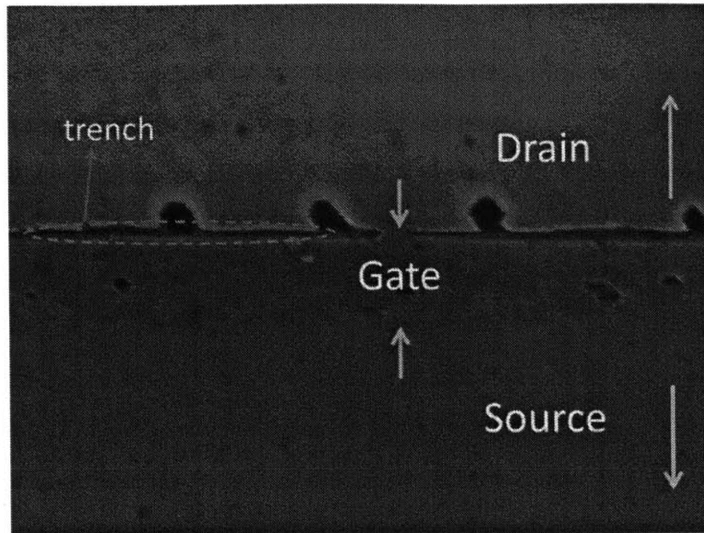

Figure 4-3. SEM picture of the surface of device MMIC 05 Type D. Deep trenches form at the gate edge on the drain side at some locations along the gate width.

The formation of deep trenches at the gate edge can be more clearly observed under AFM. As shown in Fig. 4-4, a 3-D cross-sectional view generated from AFM scans of the same device (MMIC 05 Type D) reveals a very deep trench at the gate edge. According to the scale of z-axis shown in the figure, it is impressive to notice that the trench is more than 20 nm deep indicating that the defect can extend all the way down to the GaN buffer layer.

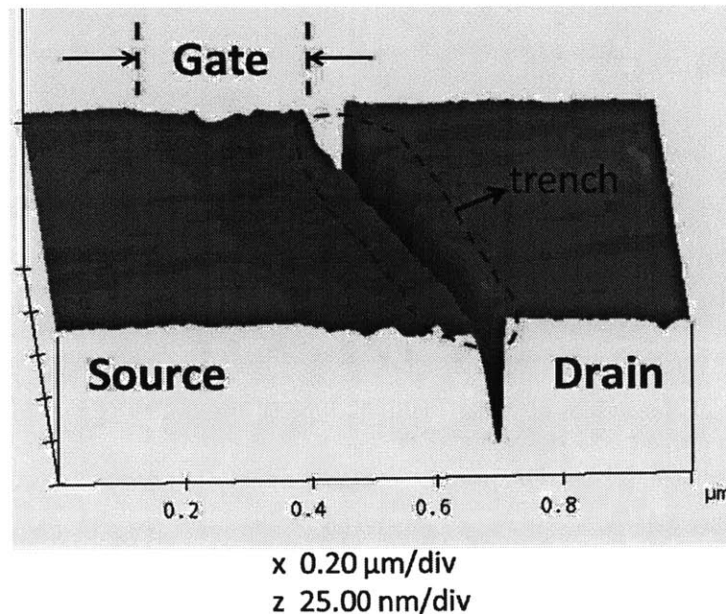

Figure 4-4. AFM picture of the surface of device MMIC 05 Type D. I_{Dmax} degradation for the device is around 25%. A Trench which is more than 20 nm in depth is clearly illustrated in the picture at the gate edge on the drain side.

4.2 SEM Analysis

A Zeiss Supra 40 SEM is utilized for this study as we have mentioned in section 2.5. Also discussed in section 2.5 is the methodology adopted to conduct SEM scans at various locations. Taking advantage of the fact that under SEM it is relatively easy to locate a specific position, we start with a wide scan across the entire surface of the semiconductor device. After locating the source, gate, and drain of the transistor, we then zoom into the gate region and further confine our scans to various locations along the gate width. Based on our observations, for all the two-finger GaN HEMTs, we have chosen the two ends as well as the center region of each of the gate fingers to be the focus of SEM studies. Shown below in Fig. 4-5 (a) is the same as Fig. 4-1 in section 4.1 which represent a SEM scan at the center of a gate finger for device MMIC 29 Type B (I_{Dmax} degrades by less than 1%). As mentioned before, in the picture we can observe a shallow groove formed at the gate edge on the drain side. Besides the center along the gate width, we also conducted SEM scans at the two ends of the same gate finger and the semiconductor surface condition is shown in Fig. 4-5(b). Similar to the central part of the gate finger along the gate width direction, the end also exhibits a shallow groove formation.

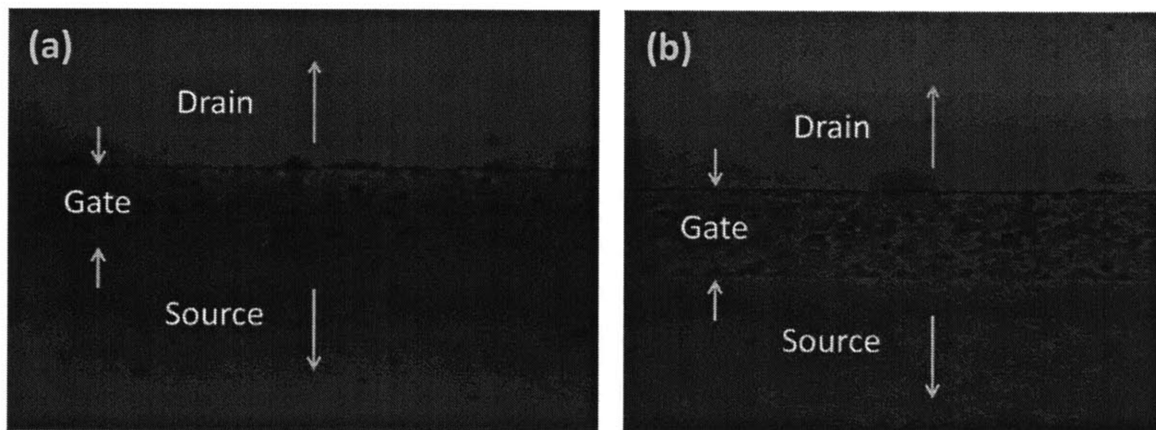

Figure 4-5. (a) SEM picture at the center of gate finger of MMIC 29 Type B. I_{Dmax} degrades less than 1% for this device. A shallow groove forms alone the gate edge on the drain side. (b) SEM picture at one end of gate finger of MMIC 29 Type B. Similar to Fig. 4-5 (a), a shallow groove forms along the gate edge on the drain side.

Similarly, we have conducted SEM analysis on MMIC 15 Type B, which, if we recall discussions in section 3.2, is a device that endures an overall permanent I_{Dmax} degradation of about 5%. In this device, we have observed pit formation. At some locations along the gate width, these pits merge into trenches of relatively short length. As shown in Fig. 4-6 (a), different from what we see in MMIC 29 Type B, here, scattered dark regions representing deep trenches exist at the gate edge. This suggests that more severe

physical degradation happens for this device. If we now move onto examining the semiconductor surface condition for the same gate finger but at one end along the gate width, as shown in Fig. 4-6 (b), we see similar trenches as the ones in Fig. 4-6 (a). However, we can notice that the density and length of the trenches at the center of the gate finger is larger than those at one end of the same finger.

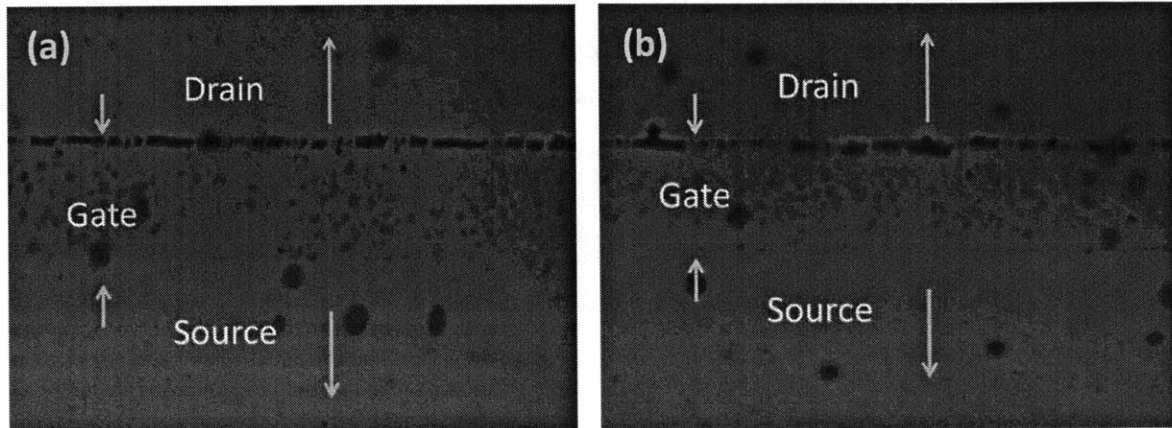

Figure 4-6 . SEM picture at (a) center of one of the two gate fingers (b) one end of one of the two gate fingers of device MMIC 15 Type B. I_{Dmax} degradation is about 5% for this device. Pits form at the gate edge and merge into trenches of some finite length at some locations.

Another device that is examined by SEM is MMIC 08 Type D. Recall that in section 3.3, we have shown that the overall permanent drain current degradation of the device is around 20%. From Fig. 4-7 (a), which is a SEM picture at the center of one of the gate fingers of the device, we notice a continuous trench at the gate edge on the drain side in the gate width direction. The continuity of the trench suggests that the density of the pits formed is so large such that they merge into a continuous trench. This indicates that the device experiences more significant structural damage than the previous two devices we have seen. Studying also the structural damage at one end of the same gate finger, as in Fig. 4-7 (b), we can see that high density pits form at the gate edge as well and they form almost continuous trenches.

Similarly, examination of semiconductor surface under SEM of MMIC 09 Type D is also conducted. The overall permanent I_{Dmax} degradation, as introduced in section 3.3, is around 5%. Shown in Fig. 4-8 (a) and (b) respectively are the SEM scans located at the center and one end of one of the two gate fingers of the device. At the center, we again see pit formation at the gate edge and due to the high densities of these pits, an almost continuous trench forms. At one end, one the other hand, the pit density is much lower and we observe scattered trenches with limited length at the gate edge.

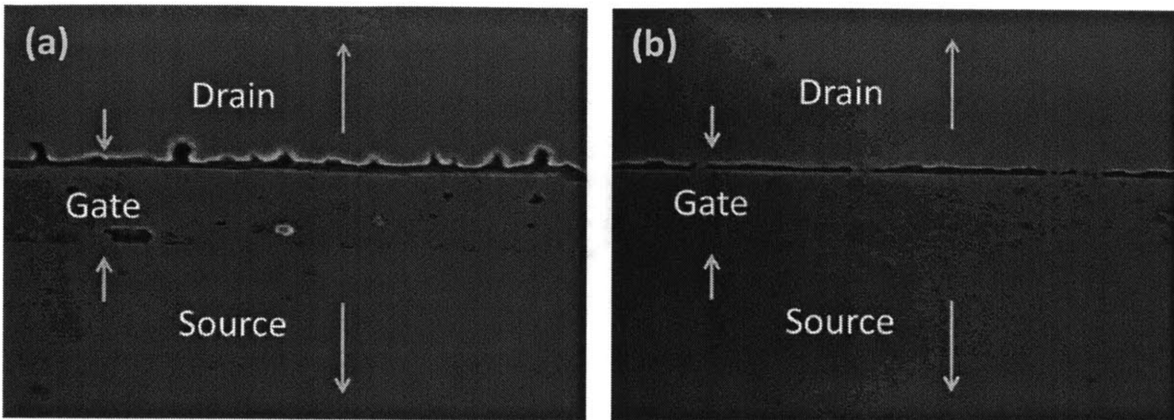

Figure 4-7. (a) SEM picture at the center of one of the two gate fingers of device MMIC 08 Type D. I_{Dmax} degradation is about 20% for this device. Pits form at the gate edge and merge into a continuous trench. (b) SEM picture at one end of one of the two gate fingers of device MMIC 08 Type D. Pits form at the gate edge and merge into almost continuous trenches.

Yet another device, MMIC 05 Type D, stressed under the high-power and high-temperature regime is examined under SEM. As discussed in section 3.2, the overall permanent I_{Dmax} degradation is around 25% for the device. Similar to MMIC 08 Type D, this device undergoes severe structural damage where pits with very high density form at the gate edge and merge into a continuous trench.

Up to this point, we have shown SEM scans of the semiconductor surfaces of five different devices stressed under high power and high temperature regime. In general, different devices exhibit different levels of structural degradation and it has been noticed that the more electrical degradation the device has undergone, the more structural degradation it will have.

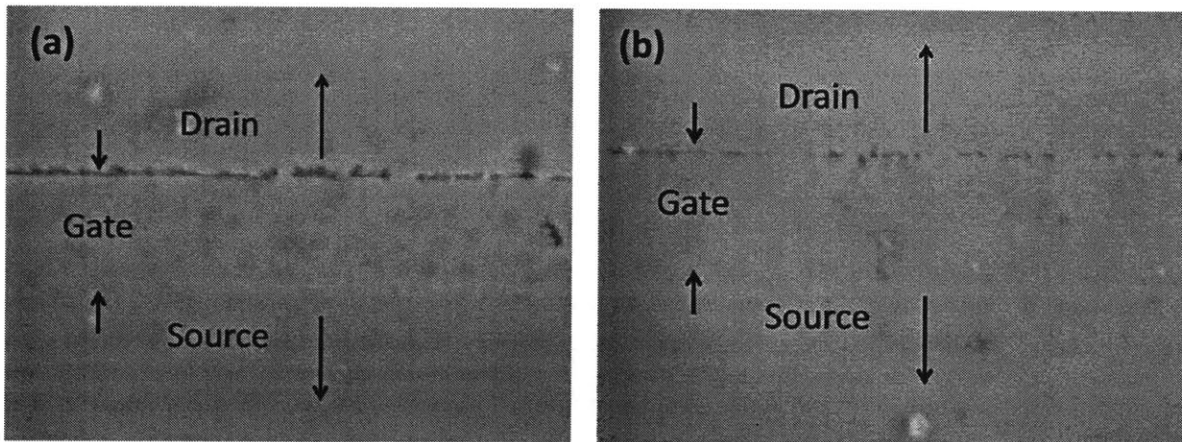

Figure 4-8. (a) SEM picture at the center of one of the two gate fingers of device MMIC 09 Type D. I_{Dmax} degradation is about 5% for this device. Pits form at the gate edge and merge into almost continuous trenches. (b) SEM picture at one end of one of the two gate fingers of device MMIC 09 Type D. High density pits form at the gate edge and merge into trenches at some locations.

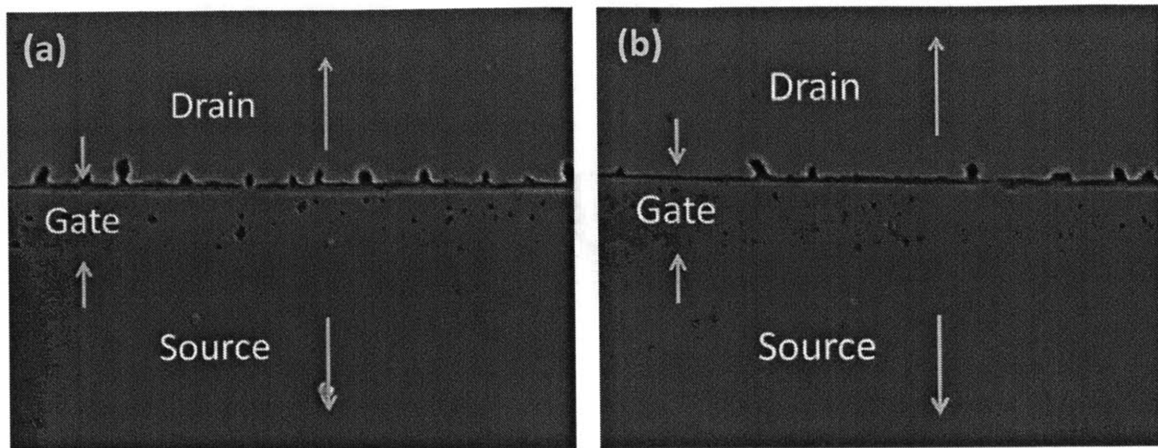

Figure 4-9. (a) SEM picture at the center of one of the two gate fingers of device MMIC 05 Type D. I_{Dmax} degradation is about 25% for this device.Pits form at the gate edge and merge into a continuous trench. (b) SEM picture at the center of one of the two gate fingers of device MMIC 05 Type D. Pits form at the gate edge and merge into almost continuous trenches.

4.3 AFM Analysis

In the previous section, we have seen qualitative analysis of structural degradation of several devices utilizing SEM. In general, grooves or pits (and trenches in extreme cases) are formed at the gate edge on the drain side. For devices enduring different levels of permanent I_{Dmax} degradation, the degree of structural degradation is also different. This qualitative analysis, however, is not sufficient to establish a more in-depth correspondence between device electrical degradation and structural degradation. In this sense, it is more insightful to conduct AFM scans on the stressed devices and carry out a quantitative analysis. In the rest of this section, we discuss in detail a study of device structural degradation under AFM.

Shown below in Fig. 4-10 is a three dimensional reconstruction of the semiconductor surface based on AFM scans of device MMIC 29 Type B which has an overall permanent I_{Dmax} degradation of less than 1%. From the figure, there is a shallow groove along the gate width at the edge on the drain side. However, the depth of the groove is very small and is not significantly different from the physical damage in the entire gate region. This insignificant defect formation at the gate edge agrees with what we have observed under SEM as discussed in the previous section.

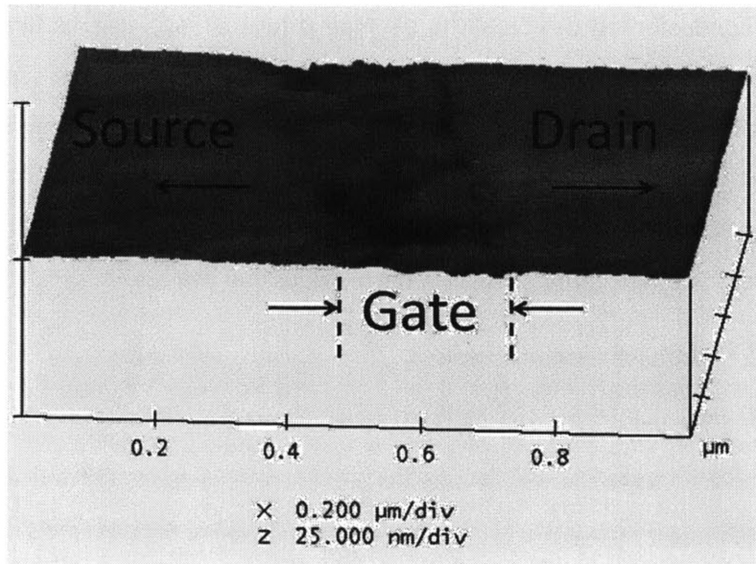

Figure 4-10. A 1 x 1 µm AFM scan of device MMIC 29 Type B at the center of one of the two gate fingers. I_{Dmax} degradation is less than 1% for this device. The x-axis represents the direction along the gate length and the y-axis represents the direction along the gate width. A shallow groove forms along the gate edge on the drain side.

Similarly, AFM scans are conducted on MMIC 15 Type B which has an overall I_{Dmax} degradation of around 5%. As shown below in Fig. 4-11, this time, we observe discontinuous pit formation along the gate width direction at the gate edge. Also, another interesting phenomenon we have noticed is that same as in device MMIC 29 Type B, there is erosion in the entire gate region to some extent. This is not observable under SEM where only planar information is available.

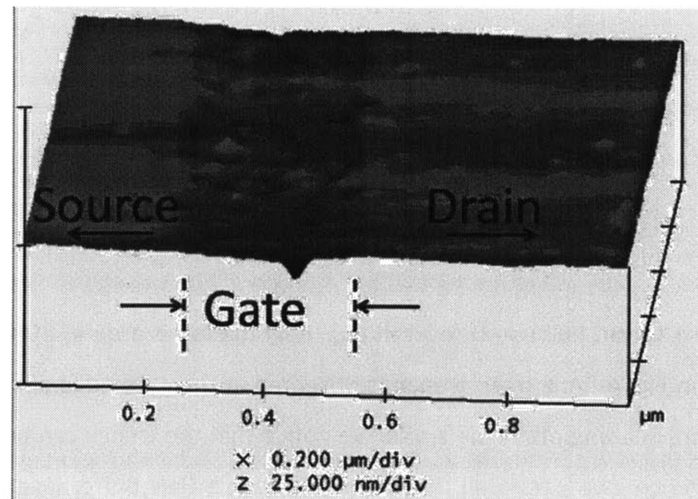

Figure 4-11. A 1 x 1 µm AFM scan of device MMIC 15 Type B at the center of one of the two gate fingers. I_{Dmax} degradation is about 5% for this device. Pits form at the gate edge on the drain side.

AFM scans are also conducted on device MMIC 08 Type D (overall I_{Dmax} degradation is around 20%). Recall from previous section, for this particular device, under SEM we observe significant structural degradation where pits form at the gate edge and those pits merge into almost continuous trenches in the gate width direction. In Fig. 4-12, a 1x1 μm AFM scan is shown where we can see directly the features revealed by SEM scans. Relatively deep and dense pits form along the gate edge. We also observe erosion under the entire gate region as in the previous two devices.

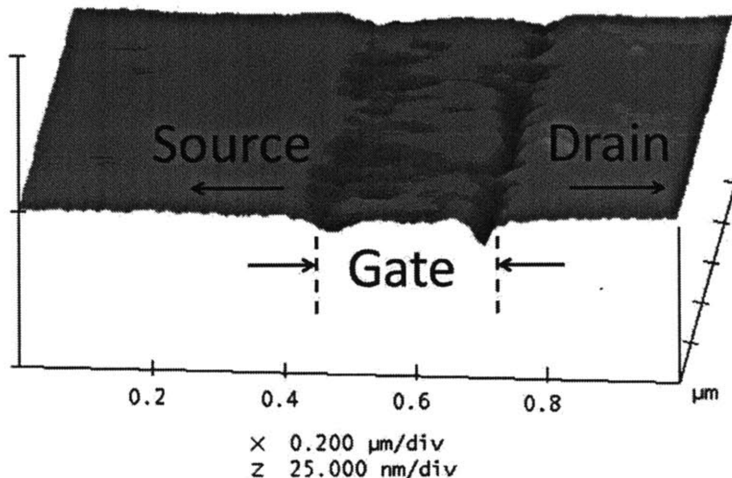

Figure 4-12. A 1 x 1 μm AFM scan of device MMIC 08 Type D at the center of one of the two gate fingers. I_{Dmax} degradation is about 20% for this device. Pits with high density form at the gate edge on the drain side and merge into an almost continuous trench along the gate width.

The semiconductor surface condition of device MMIC 09 Type D (overall I_{Dmax} degradation is around 5%) is also studied under AFM. From Fig. 4-13, similar to MMIC 08 Type D, MMIC 09 also exhibits relatively deep pit formation along the gate edge. However, since the scales for z-axis are the same for Fig. 4-12 and Fig. 4-13, we can conclude that the depth of the pits is not as large as those observed in MMIC 08. The density of the pits, however, is high enough such that almost continuous trenches form. Under gate erosion, again, exists for this device.

Another device, which is MMIC 05 Type D (overall I_{Dmax} degradation is around 25%), is also investigated using AFM. As shown in Fig. 4-14, a deep trench is observed at the gate edge along the entire 1 μm in the gate width direction. Reading off of the z-axis, we notice that the trench can be deeper than 25 nm. This means that the trench can extend all the way down to the GaN buffer layer. Besides this severe physical damage at the gate edge, we again see erosion in the entire gate region.

In order to quantitatively study the groove, pits and trenches, and erosion under the gate region, we have taken advantage of the extremely fine resolution of AFM and extracted width and depth of various features from the above shown scans. Illustrated in Fig. 4-15 is a cross-sectional view of a typical device where we have defined "Pit depth", "Trench width", and "Erosion depth". The scan shown here is conducted on device MMIC 05 Type D which has an overall I_{Dmax} degradation of around 25%. From the y-axis values, we notice that the Pit Depth is more than 20 nm which indicates that the structural degradation has penetrated the GaN cap layer and AlGaN barrier layer and has even reached the channel. The depth of eroded region under the gate is about 2-4 nm.

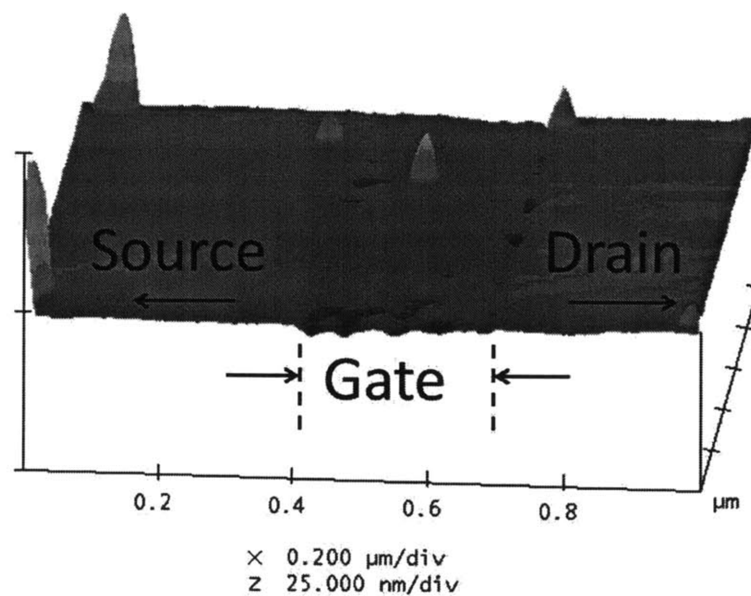

Figure 4-13. A 1 x 1 µm AFM scan of device MMIC 09 Type D at the center of one of the two gate fingers. I_{Dmax} degradation is about 5% for this device. Pits with high density form at the gate edge on the drain side and merge into an almost continuous trench along the gate width. The depths of the pits are not as large as those in Fig. 4-12.

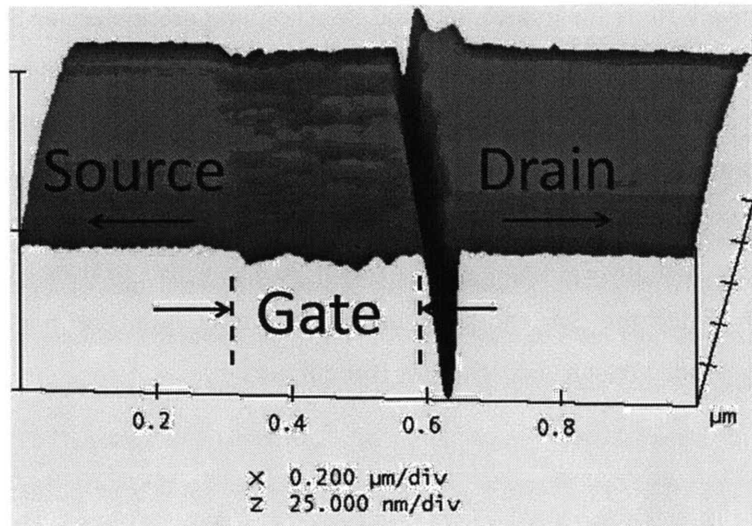

Figure 4-14. A 1 x 1 µm AFM scan of device MMIC 05 Type D at the center of one of the two gate fingers. X-axis represents the direction along gate length and y-axis represents the direction along gate width. A continuous trench forms at the gate edge throughout the 1 µm scan in y-axis direction.

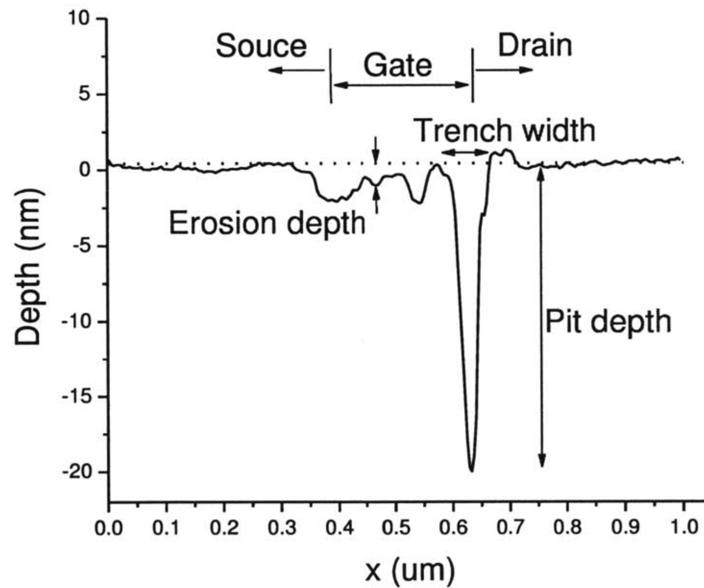

Figure 4-15. Cross-sectional view of a delaminated device showing the trench formed at the gate edge on the drain side as well as the gate undercut. "Trench width", "Pit depth", and "Erosion depth" are defined as shown in the figure. All quantities are averaged across a 1 µm scan in the gate width direction.

4. 4 Electrical Field and Temperature Dependence of Structural Damage

In section 4.2 and 4.3, we have shown planar views of semiconductor surfaces of the devices which have been stressed under high-power and high-temperature conditions. Prominent pits/trenches are found at the gate edge on the drain side. Besides, erosion under the entire gate region is also observed for all our stressed devices.

Electric field driven failure mode with a critical drain voltage for devices stressed under OFF-state has been repeatedly observed after the first observation by Joh and del Alamo [7]. Under that mode, degradation is proposed to be related to defect formation in the AlGaN barrier layer as a result of the high electric field. A hypothesis was made that lattice defects are introduced by excessive stress associated with the inverse piezoelectric effect. In [23], Joh demonstrated significant crystallographic damage for devices stressed under high-voltage in the OFF-state under TEM (Transmission electron microscopy) and established a correlation between the starting point of structural defect with the critical voltage. Comparing with the results of this project, we noticed that the structural damage of our devices which have been stressed under high-power and high-temperature regime is similar to those under OFF-state high drain voltage stress in [23]. In both cases, a groove in the GaN cap layer starts to be generated, after which pits develop and penetrate into the AlGaN barrier. This suggested to us that high electric field is also an important factor in our high-power and high temperature stress.

To study this in more detail, we have examined the relative degradation of the two fingers of each transistor. For all our tested devices, we find that one finger always has more severe structural damage than the other finger. We suspect this to be due to misalignment during the fabrication process which leads to asymmetric effective electric field at the edge of the two fingers. In fact, we find that the gate finger that is closest to the drain contact, as measured by SEM, suffers the greatest damage. This is illustrated in Table 4-1 where column 2 indicates the index of gate finger with more severe physical damage and column 3 and 4 give the distance between the gate and drain for each of the two fingers. Comparing the values, we can see that for the finger with smaller gate-drain distance which can result in higher effective electrical field during stress, the damage is more prominent.

Device Index	Gate finger with More Damage	Gate-Drain Distance of finger 1 (μm)	Gate-Drain Distance of finger 2 (μm)
MMIC 29 Type B	1	3.82	3.84
MMIC 15 Type B	1	3.7	3.91
MMIC 08 Type D	2	3.82	3.71
MMIC 09 Type D	2	3.81	3.79
MMIC 05 Type D	1	3.57	4

Table 4-1. For each of the five devices, gate fingers have been indexed with number 1 and 2. In both fingers of all five devices, the distance from the gate edge to the edge of the drain contact is measured under SEM. In every case, the gate finger that is closer to the drain contact has more severe structural damage.

However, there is also the possibility that the voltage applied at the drain side is so high (V_{DS} = 40 V or 50 V in our cases) that the 2DEG (two-dimensional electron gas) at AlGaN/GaN interface close to the gate edge on the drain side is well depleted such that almost all voltage in the extrinsic region drops there. Under such case, a smaller L_{DG} will not result in any significant increase in the effective electric field at the gate edge. In order to further confirm whether this different degree of damage for the two fingers of the same device results from different effective electric field, further experiments would be necessary where devices with different field plate designs, thus different electric field profiles at the gate edge, are to be tested. Also, simulations of the electric field profile would be valuable.

Another possible source for a discrepancy in the degree of structural damage between the two fingers of the same device is device self-heating. According to [38], the hot-spot can shift towards the drain in the gate-drain direction as V_{DS} increases. Also, an increase in V_{DS} can lead to the broadening of the temperature profile which will result in an increase in the overall gate-drain region temperature. For our devices stressed under high V_{DS} conditions, this can be a significant factor in changing the actual junction temperature. Misalignment during the fabrication processes alters the symmetry of the two fingers and can lead to different heat distribution around the two fingers under the same stress condition. This difference in heat distribution can results in non-uniform junction temperature across the gate fingers and leads to the difference in structural damage of the two fingers. To confirm this hypothesis, again, more experiments on devices with different gate finger designs are needed.

In [39], Li et al. has demonstrated that for AlGaN/GaN HEMTs stressed under high-power regime, pits form on the surface of the GaN cap layer at the edges of the gate fingers. The average pit area and density increase gradually from the edge to the center of the fingers and are more common along inner fingers than outer fingers. They have attributed this to a thermally activated nature of the formation of

the pits. Following their approach, we have evaluated the stress temperature dependence of the observed degradation phenomena by studying the evolution of the geometry of these features across the width of the device. Towards this end, multiple 5 µm x 5 µm AFM scans have been taken across the entire half of one gate finger. The pit and under gate erosion depth were averaged for each scan. Fig. 4-18 shows the average pit depth and under gate erosion depth as a function of gate finger location starting from the center of the gate. Pit depth is the largest at the center of the gate finger and it decreases away from the center towards the end of the gate finger. This is consistent with a thermally accelerated degradation process [39]. The erosion under the gate, on the other hand, does not show an obvious position dependence indicating that this degradation mechanism is relatively temperature independent.

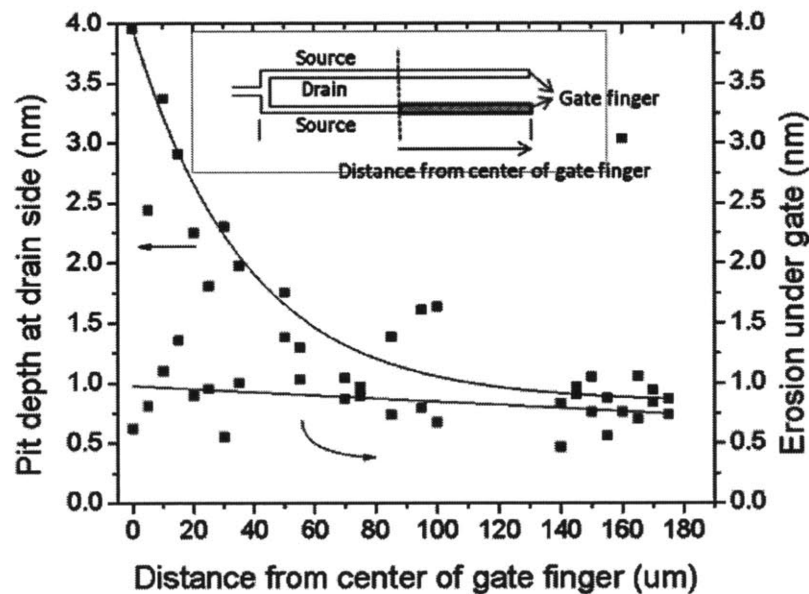

Figure 4-16. Distribution of pit depth along half of the gate width for the device with an overall I_{Dmax} degradation of 21.6%. Each point in the graph represents an averaged value across a 5 µm scan.

4.5 Summary

In this chapter, we have shown the structural degradation of the tested devices under high-power and high-temperature conditions under both SEM and AFM. We start with a three-step wet etching process to remove the metal contacts and SiN passivation layers. Following this, detailed SEM scans are

conducted at various locations near the device gate region and significant physical damage is found at the gate edge on the drain side. With this notion established, focused AFM scans at the gate edge are then conducted. It has been found that grooves, pits and trenches exist at the gate edge on the drain side for all the tested devices. The degree of the structural damage, though, varies across devices. Previous studies of devices under OFF-state high voltage stress have proposed that electric field is a causal factor for such pits/trenches formation along the gate edge. Under our designed high-power and high-temperature stress, however, due to the extra complexity brought about by device self-heating, it is not clear whether the underlying cause of physical defect formation is driven by high electric field or by high junction temperature or both. Further experiments are needed to shed light on this issue. Besides the pits formed at the gate edge, we have also observed erosion in the device gate region for all the tested devices. Unlike pit formation at the gate edge which we have demonstrated to be thermally activated, this gate undercut is only weakly dependent on temperature.

Chapter 5. Correlation between Electrical and Structural Degradation and the Physical Mechanisms Behind

In the previous chapter, we have shown mainly two types of structural degradation observed in our tested devices under high-power and high-temperature stress, i. e., pit/trench formation at the gate edge on the drain side and erosion under the entire gate region. In this chapter, we will establish correlation between device electrical degradation and structural degradation. In addition, we will also discuss the underlying physics of device degradation under our designed stress test.

5.1 Defect Formation at Gate Edge

Recall that in section 4.3, we have shown quantitatively the dimensions of the structural defects formed at the gate edge on the drain side for five samples. These five samples are stressed under various conditions (different V_{DS} and I_{DQ}) and end up with different levels of I_{Dmax} degradation by the time they blow up. For devices with relatively small I_{Dmax} degradation, shallow grooves appear along the gate fingers on the drain side of the device. For devices with prominent overall I_{Dmax} degradation, deep pits form that tend to merge into continuous trenches. Below in Table 5-1, the percentage degradation of I_{Dmax} for each of the five devices are shown (both inner loop data and outer loop data are included). We can see that the level of drain current degradation for these devices span a wide range.

	I_{Dmax} degradation (%) (outer loop data)	I_{Dmax} degradation (%) (inner loop data)
MMIC 29 Type B	0.22	0.82
MMIC 15 Type B	5.36	4.80
MMIC 09 Type D	4.70	12.56
MMIC 08 Type D	20.63	30.34
MMIC 05 Type D	25.80	40.00

Table 5-1. Overall drain current degradation of the five devices discussed in Chapter 4. Outer loop data are measurements after complete device detrapping which means that only permanent degradation is reflected in the data. Inner loop data, on the other hand, are measurements conducted without detrapping the devices so that both permanent degradation and electron trappings are incorporated.

In [23], [40], for devices stressed under OFF-state high voltage regime, it is shown that the more severe the electrical degradation a device endures, the more physical degradation the device will have.

Thinking back of both the wide range of electrical degradation and structural degradation our experiments reveal, we try to study the correlation between this two for our devices stressed under high-power and high-temperature regime. Fig. 5-1 shows comparisons between physical degradation and electrical degradation (both inner loop data and outer loop data). A positive correlation is clearly demonstrated for both the inner loop data and the outer loop data. From the figures, it appears that the inner loop data falls more closely on a linear correlation with the structural degradation while the outer loop data shows more deviations. However, recall in section 2.4 where we introduced the stress methodology, detrapping of device is conducted after several hours' of stressing of device. For our experiments, at the last stress temperature level (also the highest temperature for that experiment), it is usually the case that device blows up after a long time of stress but before we have a chance to detrap and characterize it. This indicates that the I_{Dmax} degradations reflected in Fig. 5-1 (b) are underestimated values. Due to the randomness of device blow-up time in the last stress period window, this underestimation is different for each of the five devices. This is the reason why the outer loop data seems to have more deviation from a linear correlation. This figure, together with the thermally activated behavior shown in section 4.4, confirm that pit formation at the gate edge on the drain side is responsible for the drain current degradation for devices stressed under high-power and high-temperature regime.

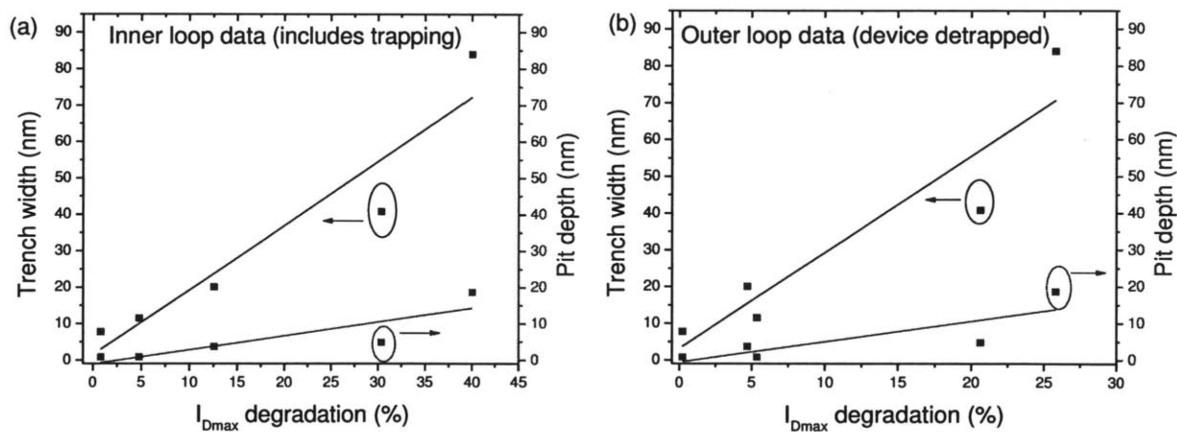

Figure 5-1. Correlation between electrical and structural degradation of the five devices biased under high-power stress regime. Both I_{Dmax} degradation vs. Trench width and I_{Dmax} degradation vs. Pit depth are shown. (a) I_{Dmax} degradation i calculated from inner loop data (b) I_{Dmax} degradation is calculated from outer loop data.

5.2 Erosion under Gate

Besides the damage formed at the gate edge, there is one unusual finding in all our stressed devices that to our knowledge has not been reported in the literature. Both the SEM and AFM analysis reveals visible erosion under the entire gate of the device. This is more clearly seen in the cross section of Fig. 4-20. Of all the figures of merit that we track in these devices, the average depth of this eroded region only correlates with the channel resistance. The channel resistance is derived from measurements of the ON resistance R_{on} (total resistance between drain and source with gate floating) and source and drain resistances obtained through the drain-current injection technique [29]. The correlation between under gate erosion depth and R_{CH} is shown in Figure 5-2 for the same five devices. The leftmost point in this graph comes from a virgin device. The finite value of erosion depth that we observe in the virgin device indicates that this damage originates in the process and is then enhanced as a result of electrical stress.

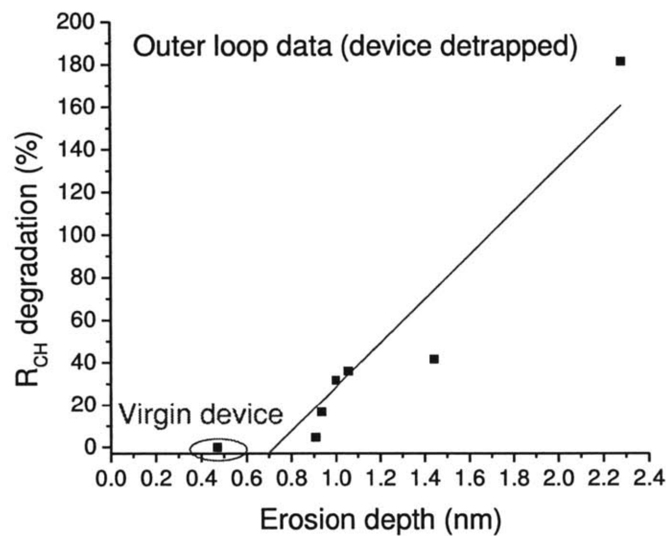

Figure 5-2. Correlation between the overall channel resistance R_{CH} degradation and the erosion in the gate region.

5.3 Hypothesis for Device Degradation

In chapter 3, we have analyzed high-power and high-temperature stress experiments conducted under the original approach where we see inconsistencies in device degradation behavior. Some devices show both large I_{Goff} and I_{Dmax} degradation while other devices, on the other hand, do not show I_{Goff} or I_{Dmax} degradation to any significant extent. After studying in detail the evolution of various figures of merit of

those devices and comparing the differences among them, we notice a universal behavior where larger I_{Dmax} degradation happens only if I_{Goff} has been severely degraded and the degradation is also saturated.

This motivates us to improve the original stress methodology and design a new two-phase experimental approach. Under the new approach, it is more clear that significant gate leakage current increase of several orders of magnitude happens relatively fast at some high stress temperature and then after some time, this increase tends to saturate. Only after this sequence of processes does I_{Dmax} shows significant degradation which is also thermally activated. To summarize, I_{Goff} degradation is a fast process which happens first while the I_{Dmax} degradation is a much slower process that follows I_{Goff} degradation and is highly thermally activated.

From all these observations, we propose that there are two different degradation mechanisms emerging sequentially under high-power and high temperature. This is also the case for OFF-state stress as described in [41]. If we now relate the described phenomena to observed structural degradation of the above examined devices stressed and showing different levels of electrical degradation, a pattern emerges where a groove along the gate edge on the drain side starts to form first. Our hypothesis is that this groove formation is related to the gate leakage current increase. The defects at the gate edge probably due to thermal effect act as leakage path for I_G. As these defects continue to form, the groove grows in depth and extends through the entire GaN cap layer.

After this first stage in both electrical and structural degradation, the high-power and high-temperature stress continues to degrade the device through pit formation at the gate edge where both the electric field and the junction temperature are the highest. These structural defects extend into the AlGaN barrier layer and affect the device transport characteristics by possibly depleting the 2DEG in the channel. In OFF-state stress experiments, inverse piezoelectric effect due to high electric field at the gate edge on the drain side is believed to be the cause of crack and pit formation [11], [23]. In our high-power and high-temperature experiments, V_{DS} is high enough such that inverse piezoelectric effect might as well play an important role.

5.4 Conclusions

In this chapter, we have shown the correlation between device electrical degradation and structural degradation under high-power and high-temperature stress. It has been shown that prominent device performance degradation start with the increase of gate leakage current I_{Goff} by several orders of magnitude. This electrical degradation turns out to be the signature of groove formation at the gate edge in the GaN cap layer. After I_{Goff} is well saturated, other figures of merit such as maximum drain current I_{Dmax} and drain side extrinsic resistance R_D start to degrade. Correspondingly, pits/trenches form following the continuous growth of the original shallow groove which will penetrate into the AlGaN barrier layer at some point. It is demonstrated that I_{Dmax} degradation is positively correlated with the width and depth of the pits. Interestingly, another significant material damage observed in all our stressed devices, i.e., finite erosion in the entire gate region, is found to be directly correlated with the overall channel resistance (R_{CH}) degradation.

All these experimental results motivate us to propose a process where two sequential degradation mechanisms happen. Groove formation in the GaN cap layer is probably due to thermal effect and results in defects that can act as leakage path for gate current. As the groove continues to grow, the GaN cap layer is breached and pits start to form into the AlGaN barrier layer. Considering the inverse piezoelectric effect, the pit formation will relax the elastic energy in the barrier layer and thus deplete the 2DEG in the channel, resulting in degradation in the transport characteristic of the device.

Chapter 6. Conclusions and Future Work

6.1 Conclusions

In this thesis, we have developed a stress methodology which can reveal the activation energy of the degradation rate with measurements from a single device. Using this methodology, GaN HEMTs are stressed under high-power and high-temperature conditions. A consistent pattern of electrical degradation emerges among all studied devices. Following this, structural degradation is examined using both SEM and AFM. Lastly, a close correlation between electrical and structural degradation is established for the device technology studied in this thesis.

In Chapter 3, we have shown that there are two degradation mechanisms existing for devices stressed under high-power and high-temperature conditions. Initially, gate leakage current degrades rather quickly and the degradation tends to saturate after a short stress time. Then in what seems to be a different degradation mechanism, the saturation drain current I_{Dmax}, exhibits much slower degradation. As we raise the stress temperature T_{base}, the degradation rate of I_{Dmax} accelerates. Based on this, we are able to extract the activation energy E_a of I_{Dmax} degradation rate. It turns out that our obtained E_a values follow closely with the reported values for a similar technology obtained using the traditional accelerated life test method. However, this is only the case if appropriate attention is given to mitigating carrier trapping which is pervasive in these devices. We have noticed from all our experiments that sizable I_{Dmax} degradation happens only if I_{Goff} degradation is well saturated in the first stage of the experiment.

In Chapter 4, following the electrical experiments, we have conducted a three-step wet etching process to prepare our degraded devices for surface examination under SEM and AFM. We have found that for devices with negligible I_{Dmax} degradation, grooves along the gate edge on the drain side exist while for devices with significant permanent I_{Dmax} degradation, pits and trenches are observable at the gate edge on the drain side. This structural damage is shown to be enhanced under high temperature by studying the evolution of the width and depth of the trenches along half of the gate finger width which has decreased temperature from the center to the two ends.

In Chapter 5, utilizing the fine scans under AFM, a quantitative correlation between the degree of electrical degradation and structural degradation is established. We have observed a similar positive correlation as what has been shown before for devices stressed in the OFF-state regime.

6.2 Future Work

In this work, several high-temperature step-temperature stress experiments have been carried out and based on which the activation energy of each of the devices is extracted using our modified Arrhenius law. We are able to obtain close values as suggested by conventional E_a extraction method on a similar device technology. However, in order to further verify the accuracy of our methodology, more experiments on the same type of device are needed to confirm the probability of correct prediction under our stress regime. Moreover, devices of different activation energies need to be tested in order to verify the versatility of our methodology. In addition, it would be great to study the early phase of the degradation of I_G using the same technique and extract E_a for I_G degradation as well. This will enable us to understand more about I_G degradation.

Besides this, in our semiconductor surface examinations, we have noticed that there is always more damage in one of the two gate fingers which has a shorter gate to drain distance between the two. We have discussed in Chapter 4 that such phenomenon can be a result of asymmetric distribution of effective electric field at the edges of the two gate fingers. However, due to the high junction temperature for all our experiments, this difference in structural damage for the two fingers can also be a result of difference in junction temperature for the two fingers of each device. In order to confirm which one is the correct reason, simulation of electric field distribution would be necessary. Also, devices with different gate to drain distances are needed to compare how the thermal distribution can affect structural degradation of the devices.

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