A High Voltage, High Current, Low Error Operational Amplifier with Novel Features

by

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Abstract

This project details the design and evaluation of an operational amplifier designed in XF40, a 40 Volt bipolar process.

Initially the signal path circuitry of the amplifier is outlined. Design decisions are chiefly formed around high voltage and high current drive functionality. A novel topology is introduced which compensates base current errors introduced by the individual stages, resulting in a very low (first-order canceled) overall input-referred voltage offset.

Novel features are introduced which expand the functionality of the amplifier. Input stage g_m is configurable, allowing for the tuning of amplifier bandwidth for a given gain configuration. A robust current-limiting architecture is implemented which allows for a user-configurable output current limit. When this current limit is reached, the amplifier latches into an alternate mode of operation, protecting the amplifier and the load. We utilize disjoint voltage supply rails at the input and output of the amplifier, substantially minimizing overall power dissipation. The chosen topology permits this feature without the introduction of additional errors. We introduce a "boosting" circuit which extends the large signal bandwidth and slew rate of the amplifier.

Amplifier performance is evaluated through simulation in Cadence and ADICE (SPICE). The amplifier is capable of driving ± 1 Ampere through capacitive and resistive loads. The result is a low distortion amplifier with microvolt-order input-referred offset (V_{OS}), 65 MHz large signal bandwidth, and 3000 V/μs slew rate, powered at 20 mA quiescent current.

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A few individuals have had a marked impact on me and have contributed to this project directly, and they must be noted.

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I would like to thank my industry supervisor Stefano D'Aquino for his close technical mentorship. Every single concept and design presented in this thesis is a product of countless discussions we had, exploring different circuits ideas and designs, most of which did not make this final thesis. The amplifier evolved significantly throughout the course of this project, heavily guided by Stefano's feedback and advice. Stefano helped me make the transition from the pen and paper problem solving mindset of my classes toward being able to apply circuit design techniques in a creative way.

Next I would like to thank the Linear Product Group at Analog Devices, Inc. for hosting my research project during the summer and fall of 2013, which permitted me to dedicate 100% of my efforts toward the development of this thesis project. I am very thankful to Stefano D'Aquino and David Whitney for giving me the opportunity to work on this project and offering me sound advice and motivation throughout. I was very fortunate to have supervisors who I could consult with daily, and this no doubt kept me focused and driven on the task at hand.

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for the past five years. A lot of my interest in the principles of analog circuit design is in no doubt inspired by the opportunities available to me as an undergraduate student, which I am grateful for. I am additionally indebted to the department's VI-A program which offered me this fantastic opportunity to pursue an advanced degree while experiencing research in industry.

This thesis project is, in some fashion, a culmination of my academic and personal achievements thus far, and therefore I am thankful to everyone who has played a role in my life.

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Chapter 1

Introduction

In this preliminary section we discuss some of the context behind the project. High output current amplifiers are a small subset of linear circuits, and we present the necessity for and applications of such a part. We describe the perks and challenges associated with developing a circuit intended for operation under high voltage and high current conditions. We address existing solutions which serve a similar function to the one detailed in this project. Finally, we establish the fundamental design objectives of the project.

1.1 Motivation

Improvements in semiconductor manufacturing over the past several decades have led to an industry-wide scuffle toward the development of smaller transistor devices. With the International Technology Roadmap for Semiconductors (ITRS) projecting a 14 nm standard for CMOS technology in 2014[1], advances in fabrication methods as well as developments in process technologies have allowed for the design of circuits using devices running at lower currents, at lower voltages, and at higher unity gain frequencies. This has done the signal processing world a great deal of good, permitting the creation of high speed amplifiers and converters, operating under these low voltage conditions. But developments in process technology for higher power, micron-scale process technology have lagged in compari-

son. Many commonly used high voltage bipolar and CMOS processes have not evolved with the same process technology innovations as their nanometer-scale counterparts.

Nonetheless the necessity for high voltage integrated circuits, capable of driving high currents, remains greater than ever before, with countless applications related to extant and emerging technologies. Integrated circuits capable of high voltage signals and power rails are necessary building blocks in systems ranging from simple power device drivers to more sophisticated frameworks involving class D audio amplifiers, motor controllers, power supplies, battery chargers, lighting ballasts, plasma display panels, ultrasound machines, and the list goes on. These circuits must be able to drive loads which require several Amperes of current, dissipating large amounts of power.

High voltage, high current circuit design occupies a unique niche in the integrated circuit design landscape, combining classical circuit architecture challenges with design decisions influenced by the necessity for high power operation. This project represents a foray into this realm, taking a very conventional circuit construct (an amplifier), and utilizing design decisions to make the amplifier capable of driving loads in excess of an Ampere at 40 Volts peak to peak. The high power nature of the project lends opportunity for novel, unique design decisions which bolster its performance, given the challenges involved.

1.1.1 Applications

There are numerous applications of high voltage, high current amplifiers, which can be used in any signal processing context involving arbitrary high voltage waveforms, driving loads which require significant current.

The most common application is in the driving of power FETs. Power MOSFETs are among the most commonly used switches and are widely used in power supplies, DC to DC converters, and motor controllers. In switching applications, the ability to slew very rapidly with low settling time is paramount. Power FETs

typically appear as high impedance loads, so the amplifier must be capable of functionality under high impedance load conditions. In a very similar context, a prime application of this part is as a pin driver for mixed signal and digital integrated circuits.

Another common application of this part is as a line driver, especially in the context of very-high bit digital subscriber line (VDSL), asymmetric digital subscriber line (ADSL), and cable drivers. Here, the accuracy of the signal is extremely important, so these applications emphasize transient performance of the part within a given set of frequencies (26 kHz to 1104 kHz for ADSL[2], 12 kHz to 12 MHz for VDSL[3]). Here transient distortion and power draw matter the most.

There are a handful of emerging technologies whose signal back-ends stand to benefit from the functionality of this part. Ultrasound machines are one of the few newer technologies designed exclusively for high power functionality. Consisting of high power inductive coils which pulse, these devices can draw very large amounts of current, often several amperes. This high current is necessary in order to deliver the power involved with the creation of these high intensity waves, often at above 10 Watts per square centimeter.

The wireless infrastructure market is another high voltage, high frequency context which uses high current output amplifiers, especially in the context of Base Transceiver Station (BTS) envelope tracking, a radiofrequency application which continuously modulates the power delivered to a given amplifier in order to increase power efficiency. In this context, bandwidth is very important because it is an application which would actually push the bandwidth of the part. Here, the power efficiency of the amplifier (tied to quiescent current draw and headroom), is likewise important. Envelope tracking is one RF-oriented technology which may use this amplifier to deliver a variable supply voltage to a circuit, seeking to minimize power dissipation. This is pictorally represented in Figure 1-1[4].

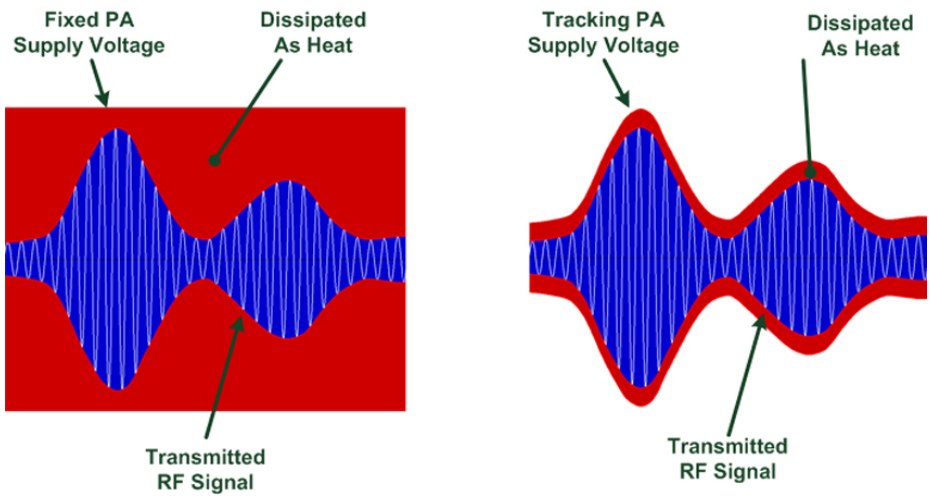

Figure 1-1: Depiction of envelope tracking technology

1.2 Design Considerations

The following section details the design considerations involved with high output current amplifier design. Initially we discuss the output stage, the portion of the amplifier which permits the amplifier to drive a high output current. Then we outline the problematic design considerations associated with high current drive functionality, as well as the necessity for protection circuitry.

1.2.1 Output Stage

A signature element of a high output current amplifier is its monolithic output stage. The output stage of the amplifier is the portion of the circuit which sees the load and thus must carry the full output current. Consider a typical Class AB output stage topology as depicted in Figure 1-2. Hereon this circuit will be referred to as the "output diamond." The bipolar transistor diamond buffer is a set of transistors which act as a voltage buffer, driving an output voltage (here V_{out}) which tracks an input voltage (the voltage at $High - Z$).

$$I_{out} = \frac{V_{out}}{Z_{load}} \tag{1.1}$$

For a given I_{out} sunk from the amplifier, the NPN device (Q1) must be able to

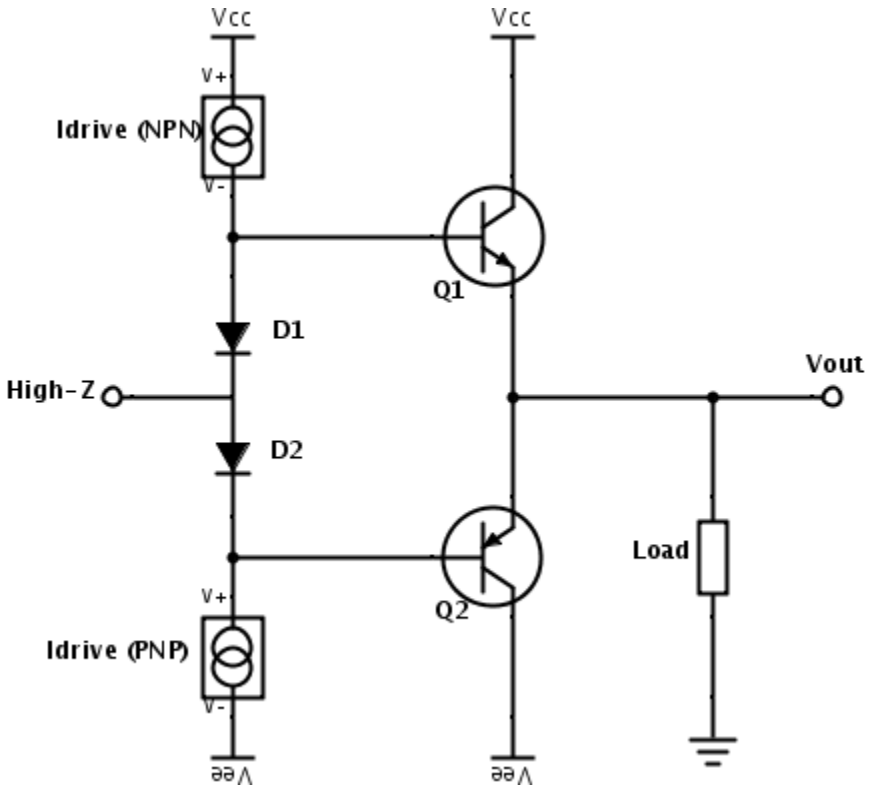

Figure 1-2: Two stages of output diamond buffer including predriver stage and class AB output

source a collector current at I_{out} without breaking down. In a corresponding fashion, when I_{out} is sourced into the amplifier, the PNP output device (Q2) must be able to sink I_{out}. The collector current of a bipolar junction transistor is proportional to the emitter area of the device[5, p. 11], thus very large output devices must be used.

But the current dependence on the output current drive extends beyond the output stage. One stage removed from the output stage sees:

$$I_{drive} = \frac{I_{out}}{\beta} \tag{1.2}$$

n^{th} order V_{BE} diamond buffers at the output stage would result in:

$$I_{drive} = \frac{I_{out}}{\beta^i} \quad \text{for} \quad i \leq n \tag{1.3}$$

In a high output current amplifier, each of these stages must be sized accord-

ingly, otherwise devices within the output buffer will suffer from breakdown at high current density.

1.2.2 Design Quandaries

As suggested earlier, there are numerous complications associated with the design of a high voltage, high current amplifier. The prior section introduced the staple of a high output current amplifier: the monolithic output stage. Many of these design dilemmas are tied to consequences of using large micron-scale devices in a large geometry process. Other design issues are reflective of the design decisions applied to circuit topologies used in a high current amplifier design.

The sheer size of high voltage transistors with micron-length gates results in large parasitics: internal resistances and junction capacitances, both of which scale with the size of the device. These parasitics heavily cut into the unity gain frequency of devices designed in a high voltage process, limiting the bandwidth of integrated circuits using the process. This puts a significant burden (or poses a challenge, however you choose to look at it) on the circuit designer rather than the process engineer to cleverly use the process to build a part with noteworthy specifications.

High quiescent current draw is a typical flaw of high current output amplifiers. Each transistor device has a range of collector current values where it operates near peak f_T. Devices in a high current drive amplifier deal with the unique scenario where they must have sufficient f_T both at quiescent (low) operating current and at their maximum current drive, corresponding to the maximum current of the part. This attribute is heavily dependent on quality of the process, and thus process engineers work to design transistor devices with "wide" f_T curves (as a function of I_C), offering maximum range of operating conditions.

Power efficiency is yet another relevant topic in high current integrated circuit design. This is tied to headroom at the input and output stages: the fraction of the supply voltage range which is unavailable to the signal swing. Larger head-

room therefore results in lower power efficiency, as this is supply power which is dissipated in the amplifier before ever making it to the load. Unfortunately, high current drive amplifier topologies make judicious use of circuit topologies which have poor headroom, namely the diamond buffer. At the input stage, the diamond buffer permits higher slew rates (useful in high voltage operation) and has worse headroom than its slower, rail-to-rail differential pair counterpart. At the output stage, a multiple stage diamond buffer must be used to step down the current from the exposed output stage to the High-Z node, protecting devices from high current exposure. As seen in Equation 1.3, each order of output diamond buffer (costing an additional V_{BE} from each rail) results in a current drive lessened by a factor of β. Power efficiency is hugely important for practical reasons, as the magnitude of the current and voltage signals in these applications will be quite high, so marginal improvements can result in nontrivial power gains.

Finally, errors abound in high current, high voltage circuit topologies. These errors manifest themselves in many different forms, from DC errors such as input-referred offset (V_{OS}) to transient errors such as frequency dependent noise and distortion. Input-referred offset occurs in large part because of differences in base current errors between PNP and NPN devices and their circuit constructs, especially in the form of current mirrors.

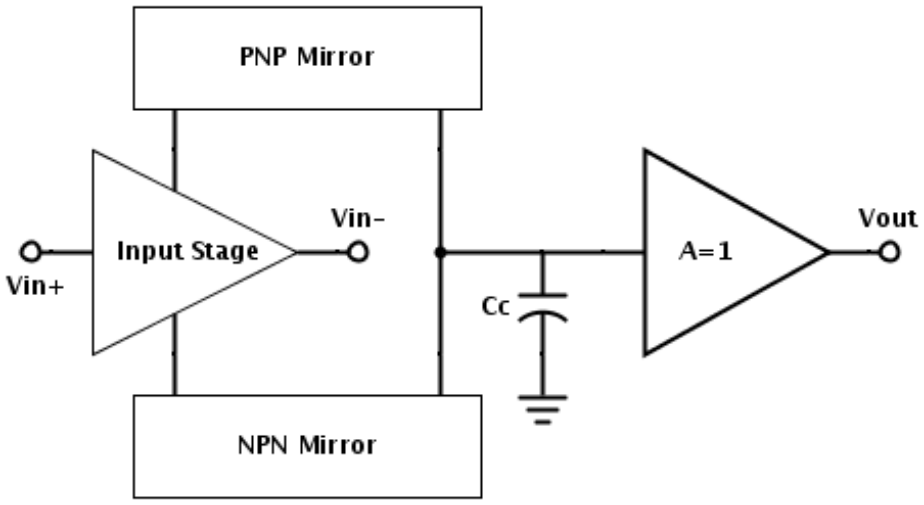

Figure 1-3: Classical current feedback architecture with current mirrors

Since V_{OS} minimization is an integral part of this thesis project, let us analyze one source of input-referred offset. Consider the amplifier architecture depicted in Figure 1-3. At steady state, the current coming out of the PNP and NPN current mirrors into the High-Z node must be equal, thus there is no current into the compensation capacitor, the High-Z node is not moving, and the output is not moving. If the NPN and PNP current mirrors are ideal, the current being sourced and sunk from the input stage will be equal. This will minimize the input-referred offset voltage at the non-inverting input (V_{in-}).

However, current mirrors suffer from base current errors, a loss of current between the input and output terminals due to current flowing into the bases of the devices in the signal path.

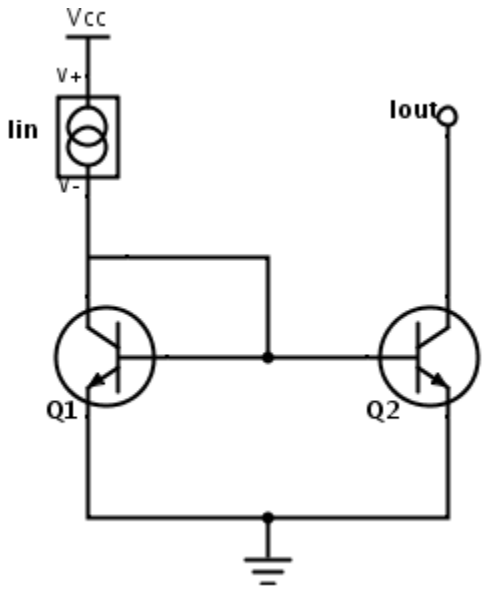

Figure 1-4: Simple current mirror with NPN devices

For a simple NPN current mirror such as the one in Figure 1-4, the output current is offset by two base currents, the currents flowing into the bases of Q1 and Q2.

$$I_{in} = I_{out}\left(1 + \frac{2}{\beta_{NPN}}\right) \tag{1.4}$$

More importantly, this error will be different in a NPN current mirror versus

a PNP current mirror because $\beta_{NPN} \neq \beta_{PNP}$ and could even be as significant as a factor of 2 to 1, depending on the process. Referring back to the current mirror amplifier topology, this means a disparity between the currents flowing into the NPN and PNP current mirrors. Depending on the input stage architecture, this difference in currents will result in an offset voltage at the inverting input, V_{OS}. More justification regarding the significance of V_{OS} and its calculation will be given in Chapter 2, in the context of the discussion of the amplifier input stage. Note that these base current errors scale with the magnitude of the collector currents of the devices. For a high current amplifier, devices have higher collector currents at DC because of the large devices involved, thus the base currents will be larger, and the magnitude of the difference between NPN and PNP base currents will be larger, hence a larger V_{OS}.

With regard to transient errors, total noise tends to be higher in large devices running at higher currents. Shot noise exhibits a proportionality to the current through a conductor[5, p. 737]. High-frequency distortion is tied to the bandwidth of the amplifier, as fringe effects occur when a signal through a part is driven at or near its bandwidth. With low bandwidth available, it is important that the part minimize high frequency distortion losses.

1.2.3 Protection

One of the risks of operating at high voltage and high current is potential breakdown of all components involved if they are not protected or rated for high current and voltage operation. This includes the amplifier driver, the load, the power supply, and the amplifier itself. Current spikes through active devices in the amplifier can burn out devices. If the load is not rated for a certain current or voltage, the load could be damaged. Similarly, current spikes could discharge or break fuses from the power supply. Amplifier system level protection consists of two areas: current limiting and ESD protection.

Current limiting is an internal control in the amplifier which prevents the out-

put from reaching a certain current level. This could be a configurable or a fixed current limit. In the case of a fixed current limit which is at or near the peak current drive of the part, this is often referred to as short circuit protection. This is characteristic of the output terminal being shorted to either rail, appearing as a zero impedance load. For any output signal voltage across an infinitely low impedance, the load will see an enormous current across it (at the absolute maximum current output of the amplifier) in the absence of short circuit protection, breaking down any unprotected electrical components in the load.

ESD Protection, or electrostatic discharge protection, protects terminals of the amplifier from electrostatic potential build up from physical contact with other electronics or with the human body. This build up results in high voltages across pins of the chip. Internal ESD protection consists of ESD diodes from the input and output terminals to the supply rails, discharging voltage build up and preventing the electrostatic potential from driving currents internally through the amplifier. There may also be ESD diodes between different supply rails of the amplifier and between other terminals of the amplifier ("clamping") to avoid excess voltage build up. ESD protection may also be externally applied to the part.

1.3 Existing Solutions

Although a nascent realm in the topic of amplifiers, there are a handful of solutions for amplifying a signal with a high current output. This topic describe an alternative system level solution as well as extant commercial parts which are competitive with the amplifier detailed in this thesis project.

1.3.1 Parallel Amplifiers

The task of delivering a given output current can be achieved by using a parallel combination of amplifiers, each with a current drive that is lower than the current demanded out the output. This implementation is less than desirable, however,

because of the inefficiencies involved with using multiple amplifiers.

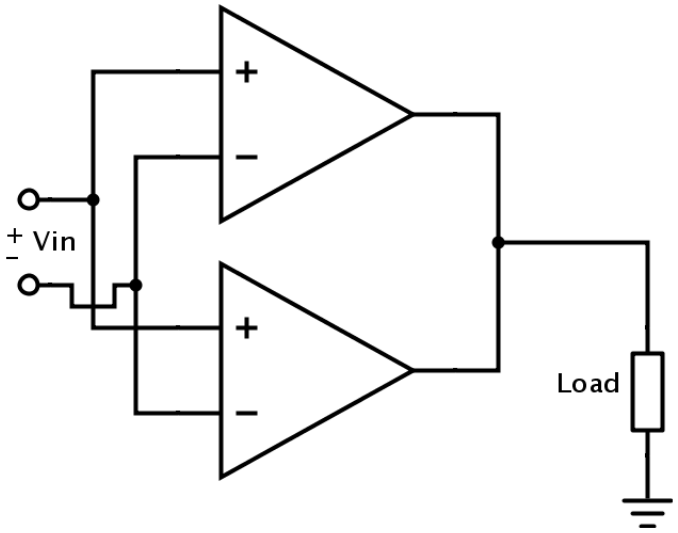

Figure 1-5: Parallel configuration of amplifiers

Given a load requiring a drive current I_{load}, multiple amplifiers can be combined in parallel, each with current drive I_n such that:

$$\sum I_n = I_{load} \tag{1.5}$$

Each amplifier will burn power by drawing current. This current usage is partially dependent on the sizing of the transistors in the signal path but is also determined by non-signal path stages such as bias circuitry. Using multiple amplifiers means duplication of these stages, and in the case of the non signal path circuitry, it is a power waste from having multiple biases which one would not see in a solution involving a single amplifier. Thus the use of parallel amplifier configurations is an alternative to the design of a singular high output current amplifier but is fundamentally less power efficient than using a single amplifier. The reuse of circuitry due to multiple amplifiers also has practical implications, requiring more on-chip board area and multiple heat sinks.

1.3.2 ADA4870

ADA4870 is the spiritual predecessor of the part detailed in this thesis project. It is *Analog Devices Inc*'s first foray into the development of a high output current amplifier capable of driving an output current up to 1 Ampere. ADA4870 is a current feedback amplifier with 34 mA supply current at a supply range of up to 40 V, and it has a large signal bandwidth of 40 MHz[6]. This amplifier has a peak slew rate of 2500 V/μs and features a shutdown pin, a thermal flag pin, and an internal short circuit protection mechanism with a fixed current limit of 1.1 A (beyond which the amplifier shuts off entirely). ADA4870 is still in development, scheduled for release in 2014.

This amplifier was designed in XF40, the same proprietary process that was used to design this part, and all schematics from the part were made available and consulted throughout the course of this project. This is crucial because it allows us to perform a one-to-one comparison of designs, abstracting out deficiencies posed by layout and package, which are not included in this project. This thesis project improves upon ADA4870 in process current efficiency based on sizing, resulting in radically lower supply current (roughly 20 mA), while maintaining the same transient and small signal capabilities which are at the limit of the process. The amplifier we will discuss uses a radically different topology which makes substantial improvements over ADA4870 in input-referred offset (V_{OS}), input headroom, CMRR, and PSRR. Additionally we take features that already exist in the ADA4870 and refine them, producing a much more robust solution for current limiting involving a configurable current limit and an alternative lower slew mode of operation which is activated when the current limit is reached, allowing the amplifier to limit the output at the current limit while still tracking the input.

1.3.3 LT1210

LT1210 is the industry leader high output current amplifier. As a current feedback amplifier capable of driving 1.1 A with a bandwidth of 35 MHz and a peak slew

rate of 900 V/μs[7], the amplifier has one of the highest current drives of any commercially available amplifiers. LT1210 has 15 mA quiescent supply current and voltage rails which go up to $\pm$15 V. The sole feature of the amplifier outside of the signal path is a shutdown pin.

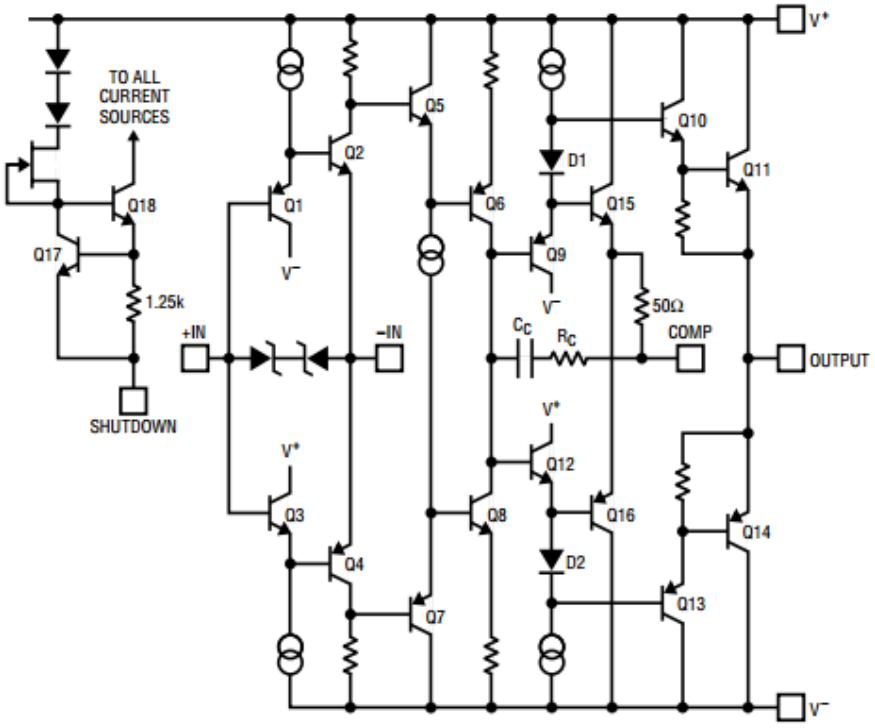

Figure 1-6: LT1210 simplified schematic from datasheet

LT1210's schematic is presented in Figure 1-6. Going over the topology, it uses a simple diamond input stage feeding current into two low input headroom current mirrors to drive the high-Z node. The output of the amplifier is a large $2V_{BE}$ diamond buffer with Darlington transistors (β^2) at its output for the high current drive. There is also a secondary diamond driving a compensation pin which is bypassed with a capacitor to the high-Z node. One could attach additional capacitance to this node, presumably to extend the compensation capacitance in order to stabilize the amplifier.

1.3.4 THS3091

THS3091 is a much lower current drive amplifier at 250 mA but is included here because it has excellent transient performance. It is a current feedback amplifier powered by 9.5 mA of supply current at DC with a supply range of 30 Volts[8]. It has a bandwidth of 210 MHz and a very high slew rate of 7300 V/μs while maintaining low distortion and low noise. THS3095, a variant of the part, has a power down feature.

The topology employed in this amplifier is not publicly available but can be guessed based on the published numbers on the datasheet. There is 1.4 Volts of headroom at the input, indicating that the input stage must be a simple single V_{BE} diamond buffer at the input, with a net input headroom of $V_{BE} + V_{CE_{sat}}$. There is a net 1.8 Volts of headroom at the output, which can only correspond to a single V_{BE} diamond buffer at the output, with extensive emitter degeneration. The large emitter degeneration could be attributed to the low noise justifies the low noise performance of the part, but this is the only single V_{BE} output stage we have looked at, possible because of the lower current drive of the part. Other attributes such as lower current supply and higher bandwidth are tied to the process utilized in the amplifier. The obscenely high slew rate of the part is somewhat of a mystery and would be tied to a higher transconductance input stage and lower parasitic and compensation capacitances.

This part represents a great reason why a system level designer might use amplifier parallelization to achieve a task. The higher bandwidth from using a lower voltage and lower current drive part can be combined with the use of multiple amplifiers to retain the bandwidth properties while achieving higher current drive. Again, the efficiency loss is in power and board area.

1.4 Design Objectives

Amplifier design is a thoroughly studied area of electrical engineering, both in industry and academia. Amplifiers as we know them have been commercially produced for the past fifty years, so what remains to be pursued? To avoid the pitfall of over-relying on classical architectures and principles, the spiritual objectives of this project are to design a part which:

1. occupies a specialized subset of the amplifier domain
2. pushes the boundaries of amplifier specifications
3. uses a novel system level architecture
4. implements features which add unique functionality

Practically, these objectives are interrelated. The amplifier must accomplish these objectives in the high output current domain. Accomplishment of novel specifications must be achieved without compromising the overall robustness and practicality of the amplifier. The new architecture of the amplifier must be practical as well and may integrate and may reuse existing stages and circuits to achieve a substantive result. Finally, the implementation of features must be tied to the application of the part and must be implemented without requiring inordinate configuration by the circuit's user. An assessment of these guiding principles and how well this project met them will be discussed in the conclusion.

Chapter 2

Design Decisions

This section of the thesis details the fundamental design decisions relating to the signal path architecture of the amplifier. This consists of a discussion of the process employed and characterization of devices used within the process. We introduce the input stage and output stage with explicit design justifications. We discuss the overall design strategy and present the current mirrors used which enable the objectives of the amplifier. Finally the chapter concludes with a block diagram of the overall amplifier.

2.1 Process

The process used in the implementation of this amplifier is XF40, a dielectrically-insulated complementary bipolar process. The minimum device geometry is 2 μm, and the devices are designed to withstand breakdown at up to 40 Volt potential difference from collector to emitter.

2.1.1 Background

Many of XF40's process attributes enable optimal device functionality in the high voltage and current domain, and this translates to improved performance of the circuits using this process. Consult Figure 2-1 for a cross-section of a NPN de-

vice in this process. The devices are isolated using trenches filled with oxide and polysilicon which wrap around the entirety of the device to achieve dielectric isolation of all components within the process, eliminating latchup and improving slew rate and packing density. Polysilicon emitter material allows for high frequency f_T with high beta early voltage products and high voltage breakdowns. The devices are created on bonded wafers, a form of silicon on insulator which brings two oxidized layers in contact with one another, one acting as material for the active devices and the other used for mechanical support for the device. The device process utilizes buried layers in the device layer to achieve low collector resistance. Additionally, the use of bonded wafers in conjunction with dielectric isolation reduces collector to substrate (C_{JS}) and base to collector (C_{JC}) junction capacitances.

XF40 belongs to *Analog Devices Inc*'s proprietary family of XFCB processes. Dating back to the early 1990s, there are numerous variants of the process, each designed for a different device voltage, but all retaining the fundamental characteristics of the process family: bonded wafers with trenches and polysilicon emitters. XF40 is a spiritual successor of CB, a 36 Volt process from 1992 which does not include the features of the XFCB class of families and thus suffers from high collector resistances and other tertiary effects.

2.1.2 Style

The particular geometry we use for this project is Style F, a geometry which uses emitter stripes surrounded by base stripes, with a strip of collector off to the side. This geometry is chosen because we want devices conducive to driving a large current from base to collector before saturating. This geometry allows for small distances from emitter to collector, and this distance does not change as we scale the size of the device up with multiple stripes. Additionally, it avoids some of the complexities and parasitics associated with using more complex geometries, such as one with a collector which wraps around the entirety of the device.

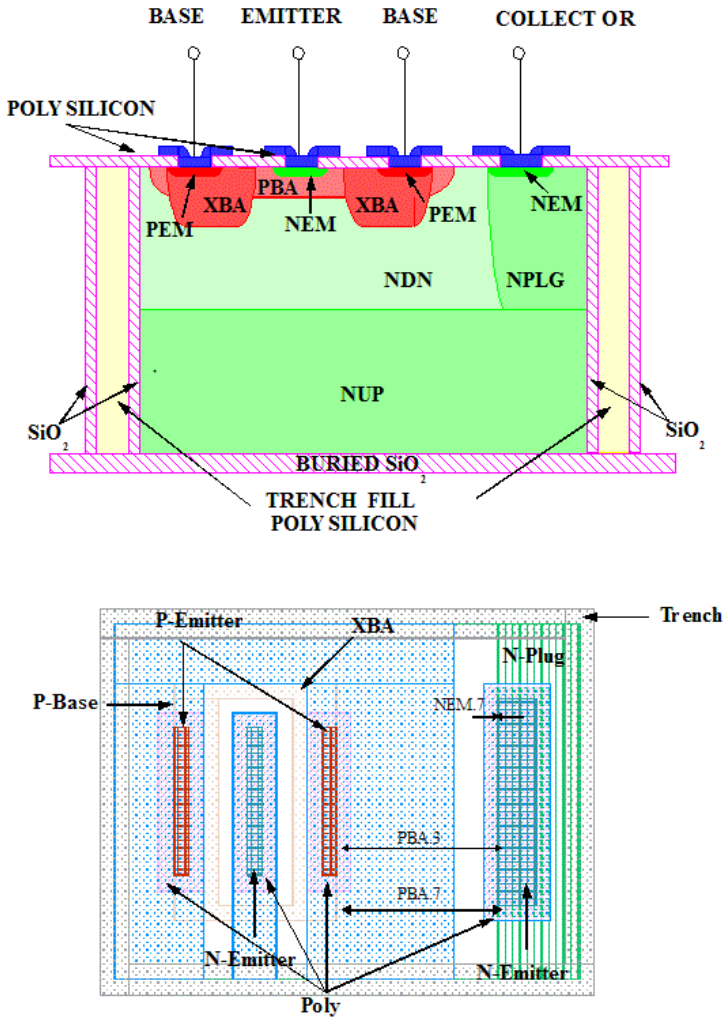

Figure 2-1: Cross-section of NPN transistor in XF40 process, side & top views

2.1.3 Area Scaling

Because we know already that the amplifier will use very large devices at the output stage, initially we look at the area scaling of devices in this process. The saturation current of devices exhibits a linear correlation with the area of the junction[5, p. 11], here corresponding to emitter area. f_T is proportional to g_m[5, p. 56] which is proportional to I_C[5, p. 27]. Transitively, f_T correlates to the I_C of the device, and we must be sure to pick an optimally sized device in order to squeeze the most bandwidth possible out of this process. We will be using very large, monolithic

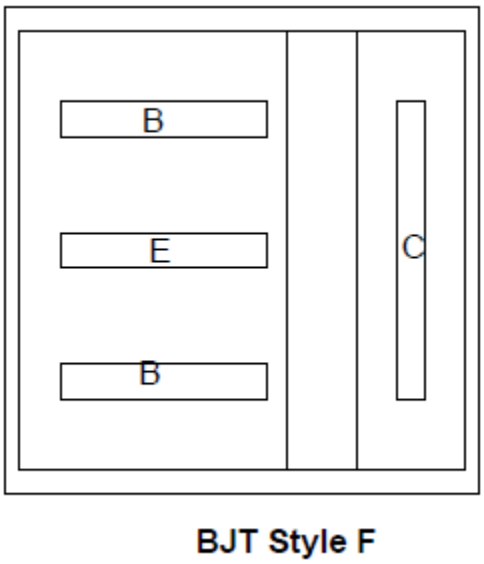

Figure 2-2: Style F Geometry

devices with large emitter areas, and there are multiple ways of achieving this:

1. Using more emitter stripes
2. Using larger emitter areas per stripe
3. Using more devices

There is a maximum number of stripes per device (10), so options 2 and 3 must be compared.

Figure 2-3 demonstrates a comparison of these two methods of scaling up device area. For a given emitter area of 200 μm^2, we initially take a singular NPN device with dimensions of 2 μm by 10 μm, 10 stripes, depicted as the green curve. This device exhibits a peak f_T at I_C = 4.4 mA. Taking the same emitter area, we then take four unit-sized NPN devices with dimensions of 2 μm by 2.5 μm, 10 stripes, seen as the brown curve. Again, the total emitter area is the same. This set of devices reaches a peak f_T at I_C = 11 mA, almost a threefold improvement in current-drive capacity at this fixed device area. This allows us to use smaller devices for a given peak current, saving power and area on the chip.

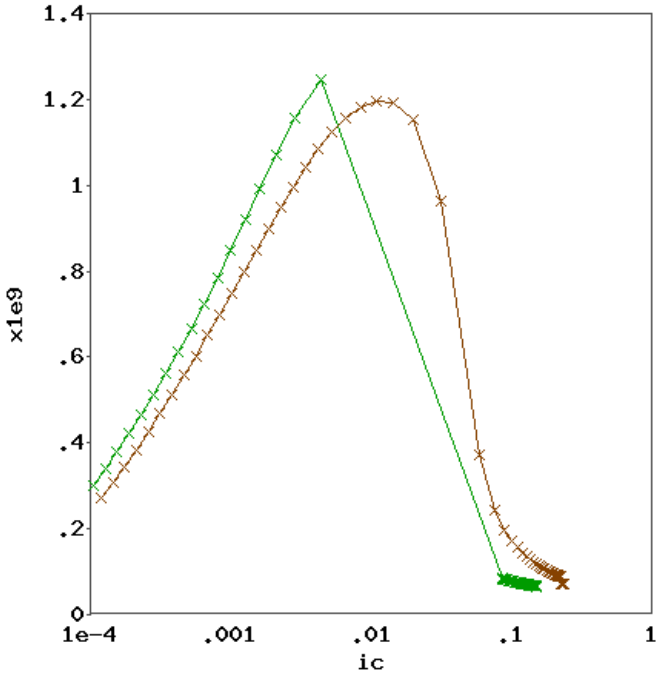

Figure 2-3: f_T versus I_C at A_E = 200 μm^2; Green - 1 2·10 10s, Brown - 4 2·2.5 10s

This advantage in number of devices over area scaling using large devices is likely due to the emphasis on device isolation using trenches, allowing for architectures using large quantities of densely packed transistors. Throughout the design of the signal path of this circuit we elect to use minimum size devices in large quantities.

2.1.4 Sizing

For reference purposes, Figure 2-4 shows f_T curves for the range of devices used in the signal path of the amplifier, ranging from a single device to 80 devices. At 80 devices (emitter area of 4000 μm^2, the aggregate transistor retains a reasonable f_T at a collector current of 1 Ampere, thus making this a reasonable sizing for the devices at our output stage.

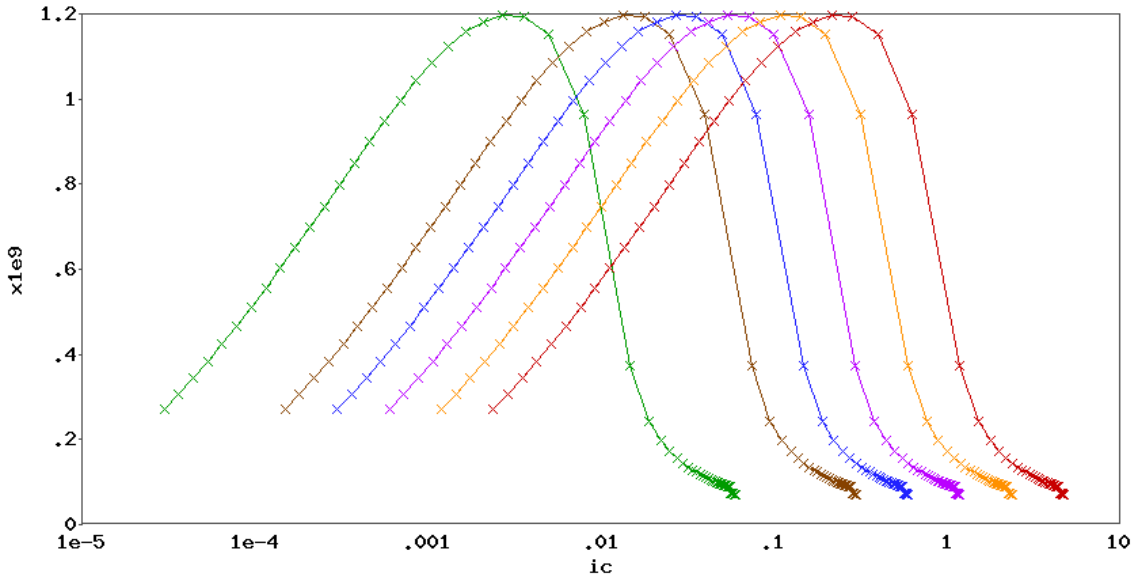

Figure 2-4: Sweep of f_T versus I_C; 1,5,10,20,40, and 80 devices (left to right)

2.1.5 NPN versus PNP

In the introduction, we characterized input-referred offset error as due in part to differences between NPN and PNP devices. In an attempt to bolster this claim, we quickly analyze the two types of devices in this process, evaluating differences in device f_T and β. This difference is due to the properties of the primary charge carrier: electrons in N type silicon and holes in P type silicon. In particular, electron mobility supercedes that of the hole[9], allowing for better device performance in NPN devices. Amplifier circuits use both NPN and PNP devices in symmetric fashion, so the inferior performance of the PNP device sets the limit for overall amplifier performance.

Figure 2-5 demonstrates this in the f_T curves of two single unit transistor devices, one NPN and one PNP. The NPN device both drives higher I_C and achieves higher f_T, a difference of almost 30%.

Figure 2-6 depicts the range of β of the same two devices across I_C. This difference is pronounced and reinforces the suggestion in Section 1.3.4 that the input-referred offset due to differences in base current error differences between NPN and PNP cannot be neglected. At low current drive we see that the difference in β

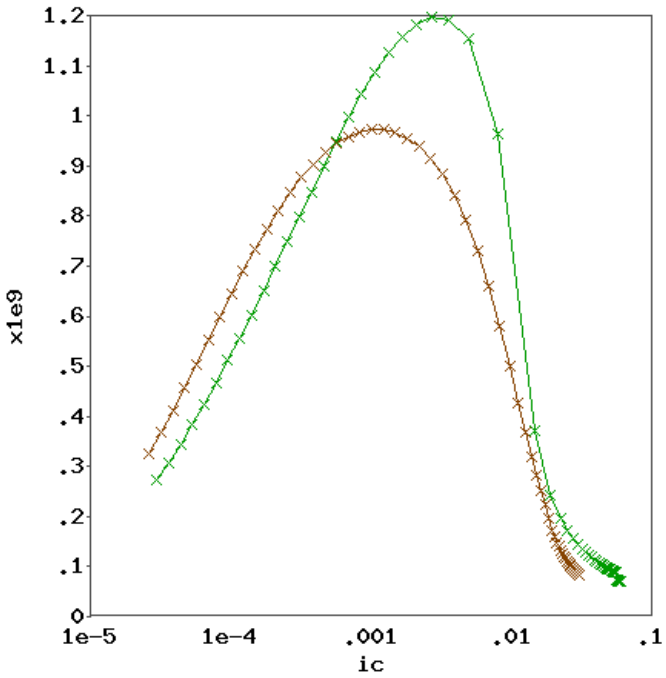

Figure 2-5: Sweep of f_T versus I_C; Green - NPN, Brown - PNP

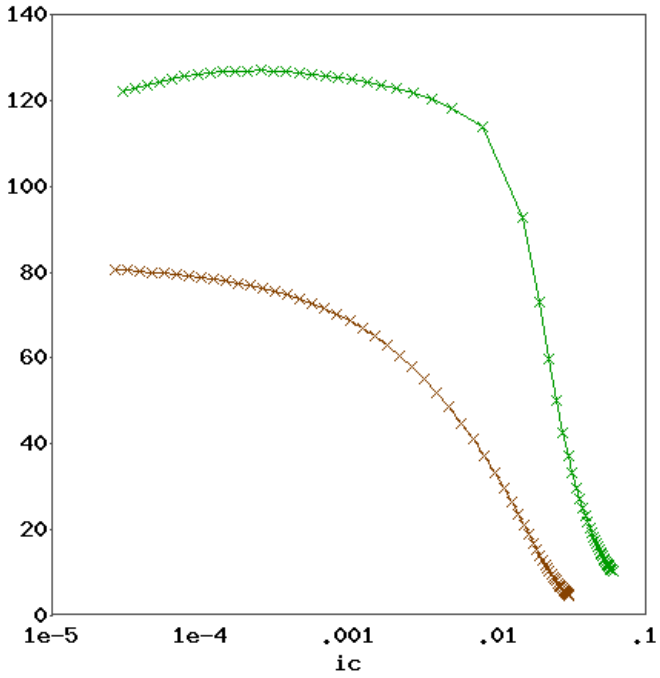

Figure 2-6: Sweep of β versus I_C; Green - NPN, Brown - PNP

is as much as 33%. At high currents the β rolls off much quicker in PNP devices than it does for NPN devices, limiting the current gain capacity of circuit topolo-

gies used in the process.

2.2 Input Stage

The input stage is the initial circuit in the amplifier which interfaces the input driver with the amplifier. In many topologies, the input stage acts as a g_m cell, taking the voltage difference between the two input terminals and producing a current which then passes into the body of the amplifier. We broadly introduce the amplifier's input stage and then expand on modifications of this input stage topology.

2.2.1 H-Bridge

For this amplifier we desire an input stage which can somehow combine the DC precision characteristics of the voltage feedback differential pair input stage with the high slew rate capabilities of the current-feedback diamond input stage. With a large buffer at the input, the diamond allows us the capacity to deliver a large current with a gain factor of β when slewing.

Implementing an input stage g_m cell using bipolar transistor diamond buffers one obtains a voltage feedback amplifier input stage with hybrid properties, and it is termed a H-Bridge. Depicted in Figure 2-7, each side of the H-Bridge behaves as a voltage buffer.

As V_{in+} swings high, device *Q1* turns off, dumping I_{bias1} into the base of *Q3*, upping the collector current and driving *Isnk_upslew*. At the same time, *Q2* turns on, stealing I_{bias2} from the base current of *Q4*, turning it off. The current that is coming out of the emitter of *Q3* takes the low impedance path, which is now the central impedance $\frac{1}{g_m}$. This current continues along the low impedance path and into the emitter of PNP device *Q6*, turning the device on harder and upping the second output current path *Isrc_upslew*.

As V_{in+} drops, device *Q2* turns off, passing the current from I_{bias2} into the base

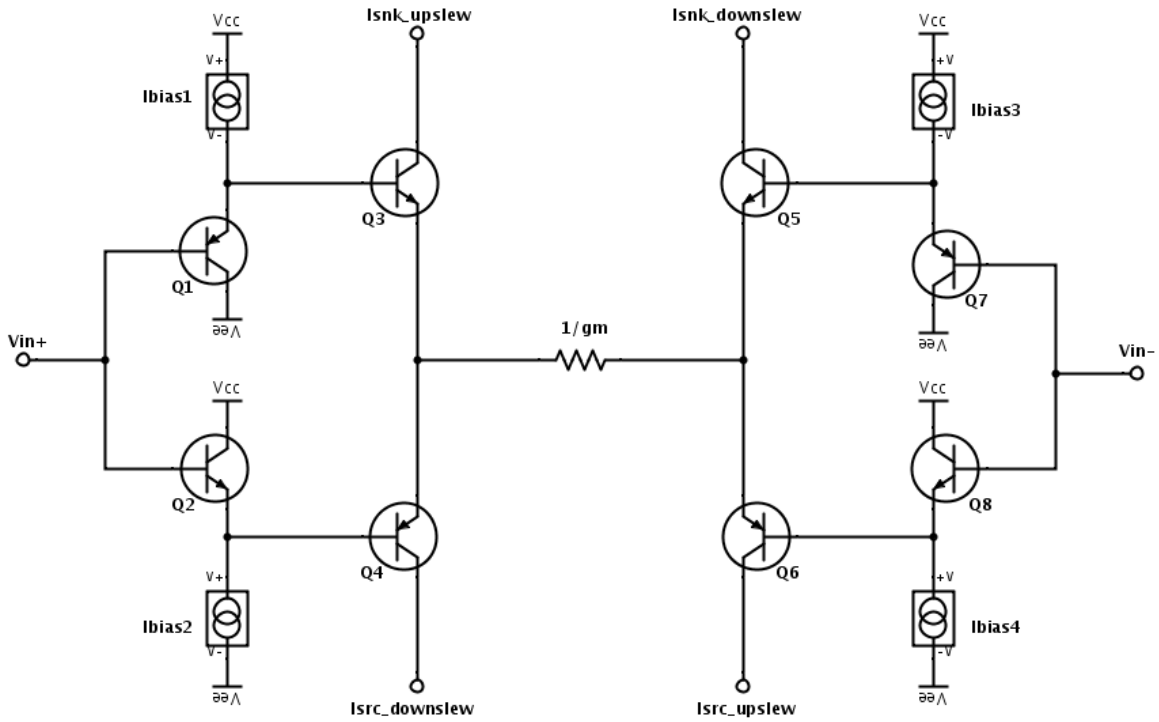

Figure 2-7: H-Bridge input stage

of *Q4* and sourcing current into *Isrc_downslew*. At the same time, *Q1* turns on harder, stealing current from I_{bias1} which would otherwise be base current for *Q3*, turning it off. The emitter current from *Q4* is sunk from the $\frac{1}{g_m}$ resistor and from the emitter of *Q5*, sinking current from *Isnk_downslew*.

Note that the inverse of events occurs when the input is in an inverting configuration, with an input signal at V_{in-}.

This circuit retains the high slew capacity of the current-feedback input architecture:

$$Isnk\_upslew_{max} = \beta_{NPN3} \cdot I_{bias1} \tag{2.1}$$

$$Isrc\_upslew_{max} = \beta_{PNP6} \cdot I_{bias4} \tag{2.2}$$

$$Isrc\_downslew_{max} = \beta_{PNP4} \cdot I_{bias2} \tag{2.3}$$

$$Isnk\_downslew_{max} = \beta_{NPN5} \cdot I_{bias3} \tag{2.4}$$

The input headroom of this input stage topology is V_{BE} + $V_{CE_{sat}}$, due to the predriver device and the current source transistor, respectively, in the diamond. The designer must be careful to discern what sort of circuit loads the current outputs from this input stage, as anything with more than a single V_{BE} of headroom will cut into the input headroom. This limits to two options: a simple mirror or a resistor.

Two major downsides of this kind of input stage are power consumption and noise. With this input stage we have doubled the quiescent current draw compared to that of a simple diamond; it is now $6 \cdot I_{bias}$. Since we now have more devices with higher potential for current gain, overall shot noise will be higher. The input stage is now eight active devices, twice that of a compound differential pair, and the sheer number of active transistors in the signal path ups the flicker noise[5, p. 741]. Additionally, the g_m cell resistor is a new source of thermal noise.

The most notable benefits from using this sort of input stage arise in analysis of the DC errors. An input stage circuit can have input-referred offset voltage contributions arising from three sources:

- A difference in V_{in+} and V_{in-} input impedances.
- An internal potential difference across the input stage $\Delta V_{BE} = V_{in-} - V_{in+}$.
- Difference in source and sink currents due to base current errors.

In the case of the H-Bridge, the first two of these attributes are handled. Both input terminals are now high impedance nodes, with:

$$Z_{in}[V_{in+}] = r_{b1} \parallel r_{b2} = r_{b_{PNP}} \parallel r_{b_{NPN}} \tag{2.5}$$

$$Z_{in}[V_{in-}] = r_{b7} \parallel r_{b8} = r_{b_{PNP}} \parallel r_{b_{NPN}} \tag{2.6}$$

Both are a combination of one NPN device and one PNP device, so provided that the devices are matched and the current bias is designed properly: $I_{bias1} =$

I_{bias3} and $I_{bias2} = I_{bias4}$ such that the quiescent currents of the NPN and PNP devices match, the input impedance at the two nodes will be identical. This will result in equivalent input bias currents:

$$I[V_{in+}] = \frac{I_{bias1}}{\beta_{PNP1}} + \frac{I_{bias2}}{\beta_{NPN2}} \tag{2.7}$$

$$I[V_{in-}] = \frac{I_{bias3}}{\beta_{PNP7}} + \frac{I_{bias4}}{\beta_{NPN8}} \tag{2.8}$$

The voltage at the inverting input tracks the inverting input, and we can reference V_{in-} to V_{in+} by following the base-emitter voltage drops. There are four paths one may take to get from the non-inverting input to the inverting input:

$$V_{in-} - V_{in+} = V_{EB1} - V_{BE3} + V_{BE5} - V_{EB7} \tag{2.9}$$

$$V_{in-} - V_{in+} = V_{EB1} - V_{BE3} - V_{EB6} + V_{BE8} \tag{2.10}$$

$$V_{in-} - V_{in+} = -V_{BE2} + V_{EB4} + V_{BE5} - V_{EB7} \tag{2.11}$$

$$V_{in-} - V_{in+} = -V_{BE2} + V_{EB4} - V_{EB6} + V_{BE8} \tag{2.12}$$

At DC there is no current flowing through the g_m resistor (otherwise the amplifier would be slewing), thus the voltage drop across it is neglected. The point of note here, however, is that the net voltage across the input stage (V_{OS}) due to input stage device base-emitter junction voltages sums up to zero:

$$V_{OS} = V_{in-} - V_{in+} = \sum \left(V_{BE_{NPN}}, V_{EB_{PNP}}, -V_{BE_{NPN}}, -V_{EB_{PNP}}\right) \approx 0 \tag{2.13}$$

Thus the input-referred offset due to mismatch in V_{BE} is minimized, provided that devices within their NPN and PNP subgroups are matched and devices of corresponding type are biased identically. On the upper path PNP devices *Q1* and *Q7* must have the same current bias, and NPN devices *Q3* and *Q5* must observe the same current bias. In the lower section NPN devices *Q2* and *Q8* must have the

same current bias, and NPN devices *Q4* and *Q6* must observe the same current bias. Minimally the constraints are set by a single path, with the collector currents established by translinearity[10].

In order to achieve $I_{C3} = I_{C5}$, we are constrained by the diamond's translinearity:

$$I_{C3} = \sqrt{I_{bias1} \cdot I_{bias2}} \tag{2.14}$$

$$I_{C5} = \sqrt{I_{bias3} \cdot I_{bias4}} \tag{2.15}$$

$$I_{bias1} = I_{bias3}; I_{bias2} = I_{bias4} \tag{2.16}$$

This design constraint in the relationship of bias currents promotes V_{OS} minimization between the input terminals of the amplifier.

The third contributor to input-referred offset is the mismatch in upslew and downslew currents due to base current errors in the input stage. This remains true; at DC $I_{E3} = I_{E4}$ and $I_{E5} = I_{E6}$. As a result, *Isnk_upslew* and *Isnk_downslew* are each down a NPN base current, while *Isrc_downslew* and *Isrc_upslew* are down a PNP base current. Within the stage itself, these base current errors are not cancelled; the burden now lies upon the implementation of this input stage into the greater architecture of the amplifier to deal with these errors before they reach the high-Z node. Minimally, one would want a contribution of a pair of NPN and PNP base current errors on each side of the amplifier in order to equalize the error contribution at the high-Z node.

2.2.2 Final Input Stage

For this thesis project I elect to use a variant of the H-bridge style input stage, sacrificing power and noise specifications in exchange for low input-referred offset and high slew rate. In principle, this makes the amplifier voltage feedback.

High slew rate is a crucial specification, allowing the amplifier to achieve the waveforms necessary for its intended applications. A very high slew rate will al-

low the amplifier to drive pulses with rapid, nanosecond-scale transitions typical of drivers for power FETs and pins. A high slew rate also prevents the amplifier from being bandwidth limited for high amplitude (voltage swing V_{pp}) input signals, where:

$$\left.\frac{\partial V}{\partial t}\right|_{max} = V_{pp} \cdot f_{bw}|_{max} \tag{2.17}$$

Finally, the use of an H-Bridge at the input stage paves the way for additional features which extend the configurability of the amplifier, allowing for improved specifications. The input stage explicit $\frac{1}{g_m}$ resistor allows for configuration of the transconductance of the input stage, breaking the mold of voltage feedback amplifier gain-bandwidth constancy to allow for bandwidth/phase margin tuning. This feature will be discussed as a stable feature of the amplifier. The multiple current output paths allow for splitting the input and output supply rails, offering the potential for enormous power conservation for the amplifier, especially in high gain configurations.

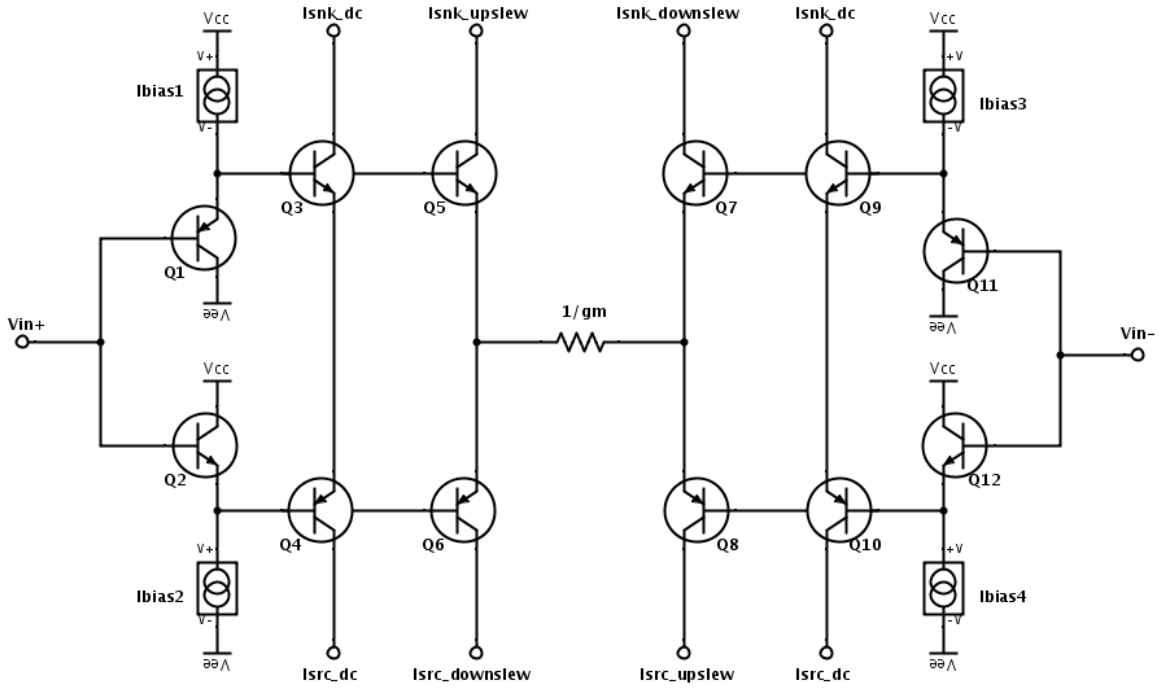

Figure 2-8: Amplifier input stage, H-Bridge configuration with modifications

Figure 2-8 depicts the final input stage with modifications. It is nearly identical to the H-Bridge pictured in Figure 2-7, with the addition of two stages, the stages containing transistors *Q3* with *Q4* and *Q9* with *Q10*. These two stages act as DC current paths which do not change with the voltage drive at the input. As one moves V_{in+}, the difference in V_{EB1} is offset by the difference in V_{BE2}, and thus $V_{EB3} + V_{BE4}$ remains relatively constant. As per the translinearity principle, the product of their currents must remain constant, thus the branch is a DC path. Note that this is different than in the case of *Q5* and *Q6* because there is an alternate path for current to take: through the g_m resistor. Thus at the extrema of slewing either transistor can turn off, breaking the exponential voltage-current relationship and thus translinearity does not apply.

Importantly, the current through these new paths are equal in magnitude to their corresponding signal current paths at DC. In order for this to be true, *Q3* must match *Q5*, *Q4* must match *Q6*, *Q9* must match *Q7*, and *Q10* must match *Q8*. With this true, the translinearity of each diamond sets the current coming out of the devices.

$$V_{EB1} + V_{BE2} = V_{BE3} + V_{EB4} = V_{BE5} + V_{EB6} \tag{2.18}$$

$$I_{bias1} \cdot I_{bias2} = Isnk\_dc \cdot Isrc\_dc = Isnk\_upslew \cdot Isrc\_downslew \tag{2.19}$$

$$V_{BE7} + V_{EB8} = V_{BE9} + V_{EB10} = V_{EB11} + V_{BE12} \tag{2.20}$$

$$Isnk\_downslew \cdot Isrc\_upslew = Isnk\_dc \cdot Isrc\_dc = I_{bias3} \cdot I_{bias4} \tag{2.21}$$

This relationship establishes the biasing methodology for the input stage and provides additional benefits at DC. Assuming matching devices, matching source and sink bias currents on each side of the H-Bridge, and $V_{in+} \approx V_{in-}$ (minimal V_{OS}):

Just as with the diamond buffer, the currents coming out of the diamond at the collector terminals will be offset by a base current, and one side of the amplifier sees a difference in NPN base currents while the other side of the amplifier sees a difference in PNP base currents. Figure 2-9 demonstrates this augmented H-Bridge

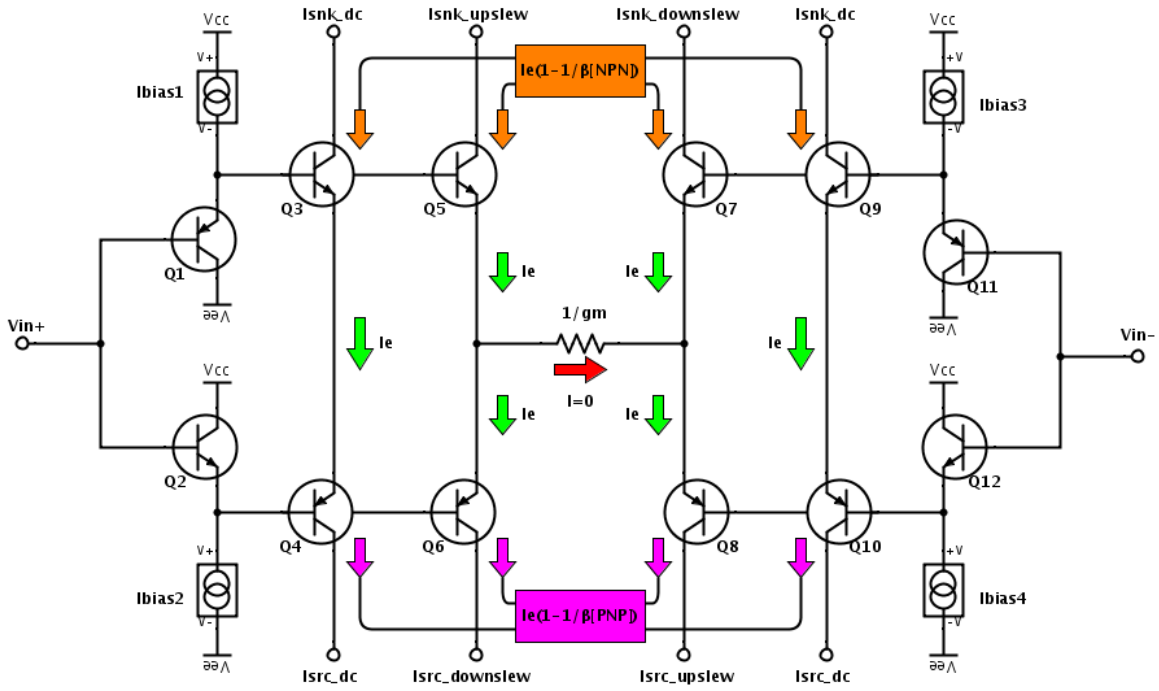

Figure 2-9: Amplifier input stage with superimposed base current errors

input stage architecture with superimposed base current errors. Here, now that we have DC stages, we replicate these base errors which at DC precisely match their signal-based counterparts.

This affords the designer enormous flexibility as far as dealing with these base current errors further on in the design of the amplifier. Now that we have duplicate DC currents with the same errors, there are more options for schemes that ensure both sides of the amplifier produce identical currents at DC at the high-Z node. Additionally, because these currents are DC and will not change in magnitude as the amplifier slews, they can be sent to either side of the amplifier, regardless of correlation to upslew or downslew, and the amplifier's transient performance will not be negatively impacted. There are numerous implementations that will harness this flexibility to achieve low V_{OS}, and the one used in this amplifier will be detailed later on in this chapter in the amplifier's overarching design strategy.

The other benefit of this modification over the original H-Bridge input stage is that it prevents either side of the amplifier from fully turning off when the amplifier is slewing. For example, when the input stage is slewing hard in the up-

wards direction, the turn-off of *Q1* leads *Q5* to drive a very large quantity of current $I_{bias1} \cdot \beta_5$. Meanwhile the turn-on of *Q2* turns off *Q6*. The end result is that *Isnk_upslew* is very high while *Isrc_downslew* is nominally zero. The same mechanism is reflected on the other side of the H-Bridge where *Isrc_upslew* is very high while *Isnk_downslew* is off. This means that the side of the amplifier designed to take the downslew current will be entirely off; the devices will be completely deprived of current. Adding DC components to both sides of the amplifier ensures that there is a minimum current threshold, the sum current through the two DC stages, that will keep the devices minimally on. This serves to help high frequency (at or near bandwidth) transient performance in the form of distortion, preventing delays and residual signal effects from turning on devices and charging parasitic capacitances.

This input stage will allow us the flexibility to design a robust, fast amplifier with great DC precision while permitting us the flexibility of design decisions and implementations that would otherwise not be possible in a simpler input stage. In exchange, it costs us additional quiescent current, input headroom ($V_{BE} + V_{CE_{sat}}$), and noise (minimally eight transistors in the signal path).

2.3 Output Stage

The output stage establishes the mechanism by which the amplifier interacts with the load. It presents the output impedance, which ideally should be as low as possible to minimize power dissipation I^2R in the amplifier before ever reaching the load, it limits the output headroom, and most importantly it sets the current drive of the amplifier. There are a variety of different output stages available in mixed signal circuits, many relying on switching to achieve greater power efficiency and lower distortion. But the range of options available to the purely analog designer are few and far between, and this project focuses on the implementation of a classical Class AB output stage, delving into the analog elements that drive it.

2.3.1 Output Devices

The Class AB output stage is a well-defined circuit topology, consisting of a set of NPN and PNP transistors which drive the output voltage and current. Refer back to Figure 1-2 on Page 21 for a simple class AB output stage topology. The output impedance is simply $r_{e1} \parallel r_{e2}$, which is relatively low.

The design and selection of output devices is crucially dependent on process, which determines the sizing of the transistors required to achieve a certain high current threshold. In simulation we determine that 80 units of 2 μm by 2.5 μm transistors with 10 stripes each are required to achieve a satisfactory high frequency f_T when driven with a collector current of 1 Ampere. This corresponds to an overall emitter area of 4000 μm^2.

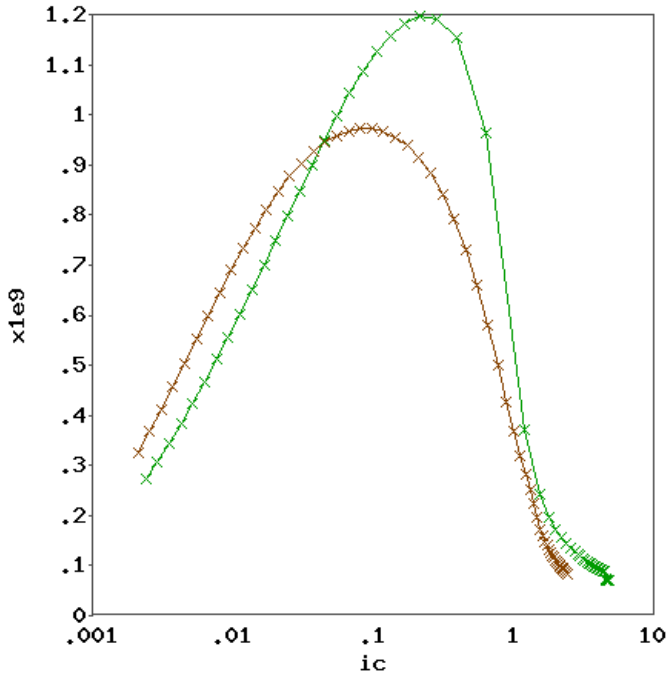

Figure 2-10: Sweep of f_T versus I_C for output devices; Green - NPN, Brown - PNP

Figure 2-10 demonstrates the f_T curve of these devices as a function of collector current. We can see that at above 1 Ampere both the NPN and PNP devices have unity gain frequencies of roughly 370 MHz, probably on the low end of what is sufficient to be able to drive waveforms at high current without significantly cutting

into the amplifier bandwidth. Similarly we find an appropriate quiescent bias current for the output stage, which for the PNP device must be above 3 mA for >400 MHz f_T and for the PNP device must be above 5 mA. Because these devices will be biased at the same current once the entire diamond architecture is presented, we establish a minimum baseline of 5 mA quiescent current for the output stage transistors.

2.3.2 Output Diamond

The output diamond buffer determines two prominent characteristics of the amplifier: the output headroom and the degree to which the amplifier's high-Z node is protected from the output current. Choosing which diamond buffer to use is prominently a trade-off between these two qualities.

The single V_{BE} diamond buffer was demonstrated in Figure 1-2 on Page 21 and represents a simple version of the output diamond buffer. This circuit has a headroom of $V_{BE}+V_{CE_{sat}}$ from the output device and the transistor which is acting as the current source to drive the output stage. As demonstrated in Equation 1.2, the current that must be driven is $\frac{I_{out}}{\beta}$.

Given the sizing we have chosen for the output devices, 80 units each, we analyze the characteristic beta of these devices at the amplifier's specified maximum drive of 1 Ampere. This is shown in Figure 2-11. At I_C = 1 A, $\beta_{NPN} \approx 100$ and $\beta_{PNP} \approx 25$. With how low β_{PNP} is, this is particularly concerning, because therefore in a single V_{BE} diamond we would require an I_{drive} of $\frac{1}{25}$ A = 40 mA. This would be either an unreasonably large bias current or a severalfold scaling up of the current out of the H-Bridge, also tied to a large quiescent current draw. Another option would be to further scale up the area of the output devices to reach a higher β for the given peak current, but this would raise the minimum quiescent current attached to the stage, established as 5 mA in the prior section.

Because of the unreasonable power costs associated with stepping down the peak current of an Ampere that we are hoping to achieve, we must therefore ex-

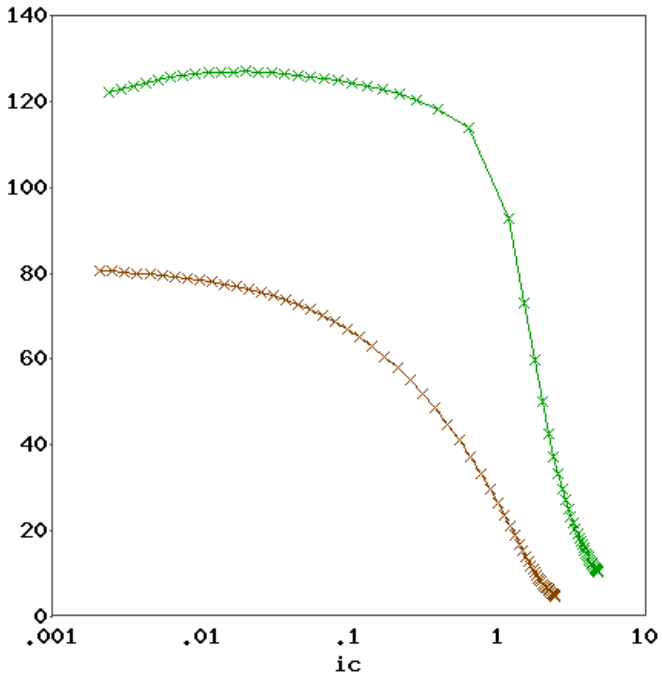

Figure 2-11: Sweep of β versus I_C for output devices; Green - NPN, Brown - PNP

plore the option of a higher order diamond buffer, sacrificing an additional V_{BE} of headroom but stepping down the current drive by another factor of β.

Figure 2-12 shows an implementation of such a 2 V_{BE} diamond buffer. This output stage has $2V_{BE} + V_{CE_{sat}}$ of headroom from the output node to rail. This is related to the emitter follower transistors in the final and penultimate stages as well as the transistor device acting as the current source. Now the current drive at the output is stepped up by β^2 to the output. More formally, when the amplifier is sourcing current, the amplifier can source $Idrive\_src \cdot \beta_3 \cdot \beta_5$ Amperes. On the other side of the amplifier, the output stage can sink up to $Idrive\_snk \cdot \beta_4 \cdot \beta_6$ Amperes of current. This is much more achievable with the low values of β witnessed in Figure 2-11.

2.3.3 Bootstrapping

For the final output stage of the amplifier used in this thesis project, we take the 2 V_{BE} diamond buffer and bootstrap the output.

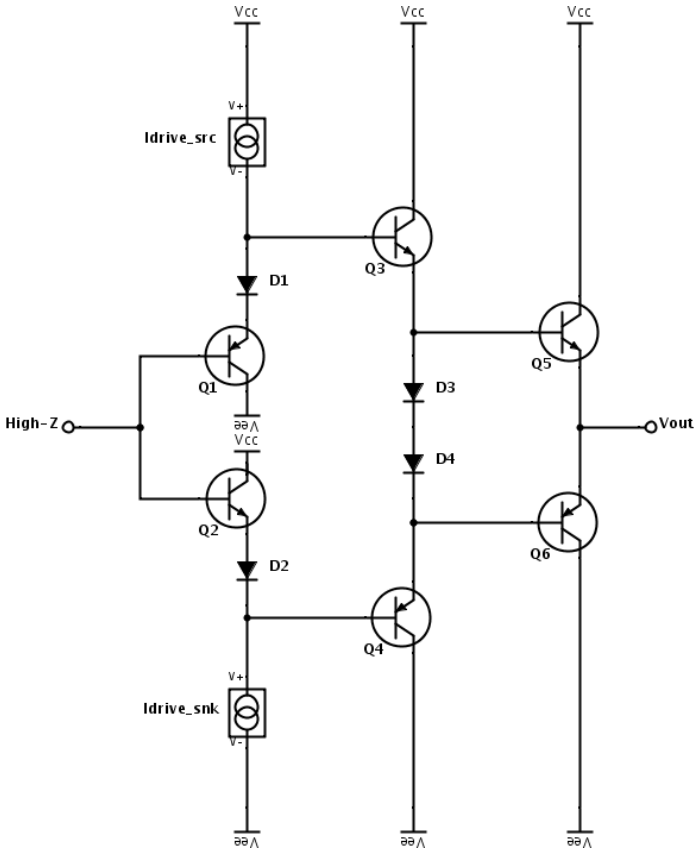

Figure 2-12: Classical 2 V_{BE} diamond buffer

In the design of circuits, bootstrapping involves the use of feedback from the output to the input of a circuit (typically unity gain) in such a way that a node in the circuit is ”pulled up as if by its own bootstraps”[11]. In this amplifier the output node is bootstrapped to the collector terminals of the predriver transistors in the diamond buffer.

The most significant impact of this design decision relates to parasitics of the devices *Q1* and *Q2*, in particular the base-collector capacitance (C_μ) of the devices. In the prior implementation from Figure 2-12, these devices had collector nodes which were railed. Thus the (C_μ) of these devices is added to the net capacitance seen at the high-impedance node. This had adverse effects, from lowering the amplifier's slew rate and effective bandwidth by lowering the pole frequency ($\frac{1}{RC_c}$) associated with the high-Z node. On the other hand, it provides additional stability by increasing the small signal phase margin, again because of lowering the

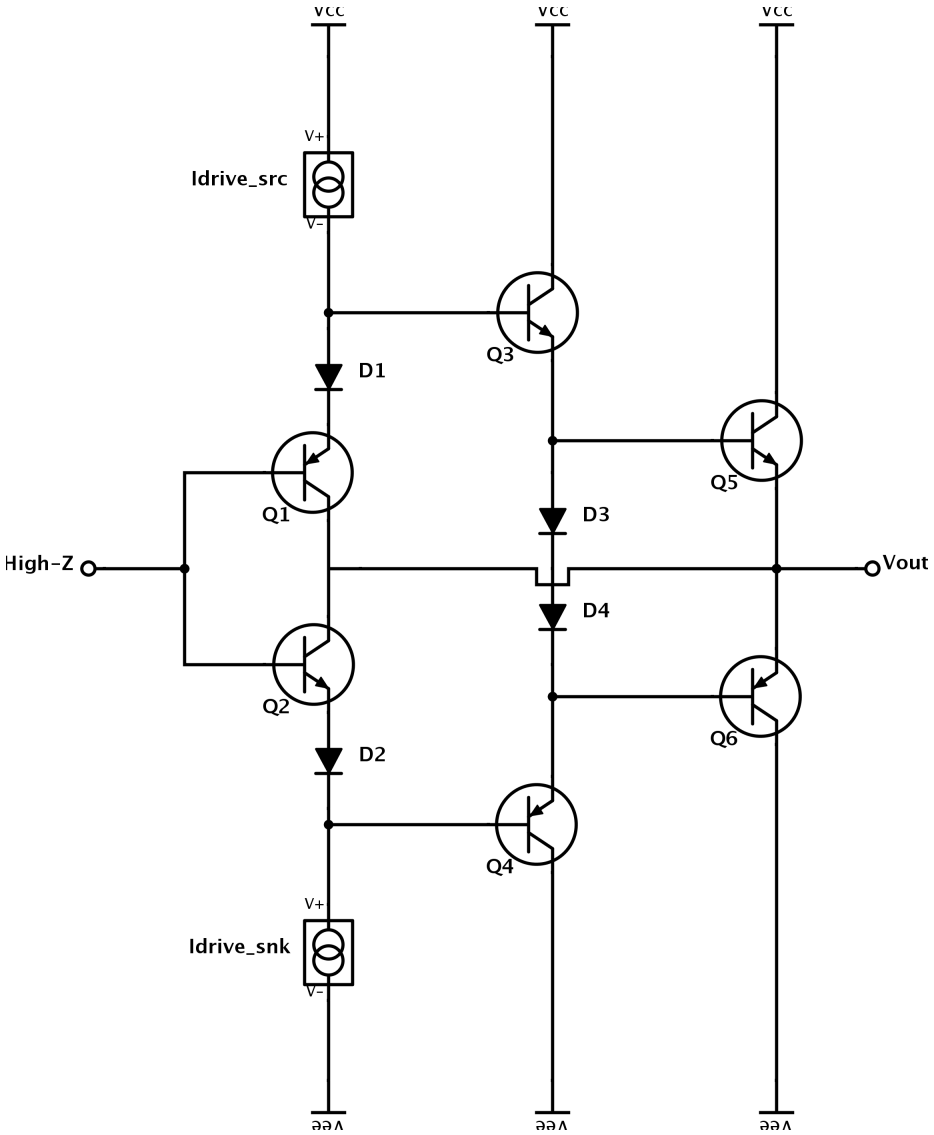

Figure 2-13: Amplifier output stage, Bootstrapped 2 V_{BE} diamond buffer

pole frequency. These are all direct consequences of an increased compensation capacitance (C_c) at the high-Z node.

Another point of note is that this bootstrap connection does not significantly increase the effective overall output impedance of the amplifier.

$$Z_{out} = r_{e5} \parallel r_{e6} \parallel r_{o5} \parallel r_{o6} \parallel r_{o1} \parallel r_{o2} \approx r_{e5} \parallel r_{e6} \tag{2.22}$$

Lastly, this connection saves a single stage worth of quiescent bias current by forcing two stages to share collectors. The devices *D1*, *Q1*, *Q2*, *D2*, and the devices

acting as *Idrive_src* and *Idrive_snk* now share a single stage's worth of current.

2.3.4 Output stage driver

The driver circuit consists of a set of stages which will take a current from the input stage (directly or indirectly) and perform two functions: create a high-Z voltage node to drive the input of the diamond buffer, create current paths to drive the current through the diamond buffer.

In doing so, one can abstract the inputs into such a circuit as *I_upslew* and *I_downslew*. When the input to the amplifier is slewing upward, the input stage and whatever circuits follow it will culminate in a burst of current in one direction: *I_upslew*. When the voltage at the input is dropping, *I_downslew* will rise.

In the former depictions of the output diamond buffer, the drive currents have been symbolically represented as ideal current sources *Idrive_src* and *Idrive_snk*. They could be implemented as such, but this would heavily limit the current drive of the output as well as the capacity of the diamond buffer to operate. When the input to the diamond buffer is slewing rapidly, a large current at the output will allow the voltage to change in order to track the input more effectively. To allow the drive currents into the diamond to scale with changes in the input, we relate these currents to the currents coming out of the input stage.

I_upslew corresponds to *Idrive_src* because when the output is sourcing increasing current for a fixed load impedance at the output, the output voltage will rise. Likewise, *I_downslew* correlates to *Idrive_snk* because sinking current at a constant load impedance will drop the output voltage. These relationships are necessary to understand in order to grasp the two-sided nature of the amplifier.

Figure 2-14 demonstrates the role of this circuit in conjunction with the output diamond buffer. From this figure we can identify much more easily that these two drivers can be implemented as three-stage current mirrors. The input stage of the current mirror takes the slew current. The second stage replicates the slew current and passes it into a high impedance node, performing a current to voltage

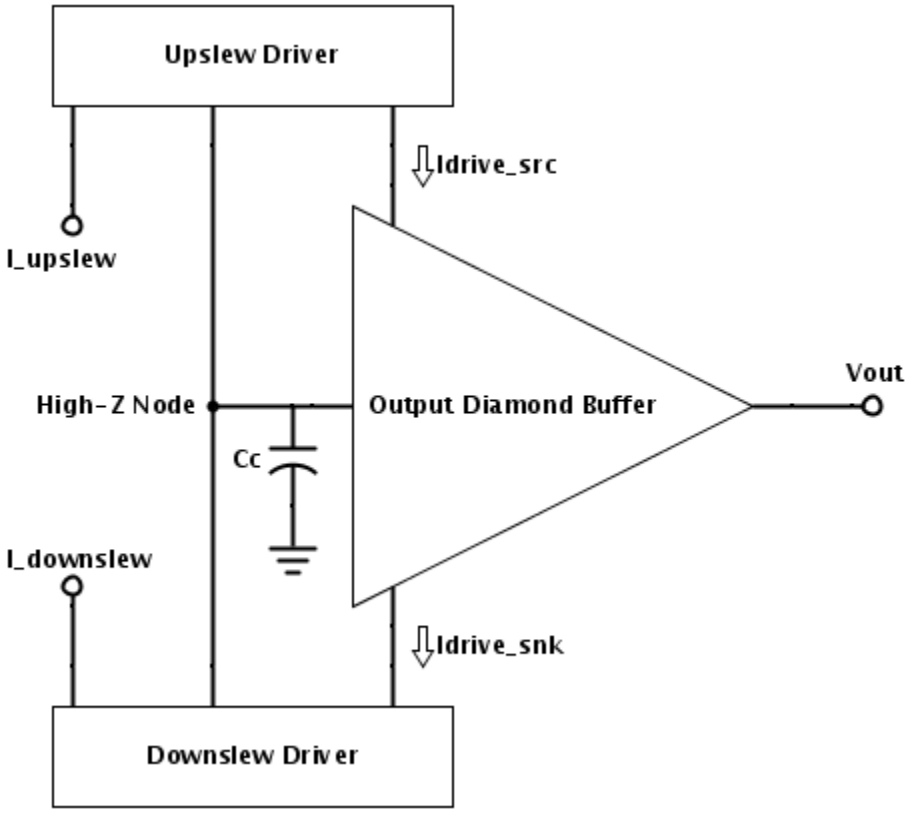

Figure 2-14: Abstracted output driver circuit with diamond buffer

conversion. Finally the third stage takes some scalar multiple of the drive current and passes it directly into the diamond buffer in order to give it current drive.

The implementation of this driver is largely inspired by the beta cancellation circuit from *Early voltage and beta compensation circuit for a current mirror* by Stefano D'Aquino[12]. In designing this stage, we initially elect to use a cascode current mirror for the driver topology. In analyzing the circuits used to achieve this driver, we will initially analyze one half of the amplifier. The downslew current driver consists of NPN devices while the upslew current driver uses PNP devices. Otherwise the two drivers are topologically identical.

We choose the cascode current mirror because it has a high output impedance of $\frac{\beta r_{o3}}{2}$, and this is shown in Figure 2-15.

The order of beta increase in output impedance is due to the cascode device at the output. Figure 2-15 depicts an example cascode current mirror constructed

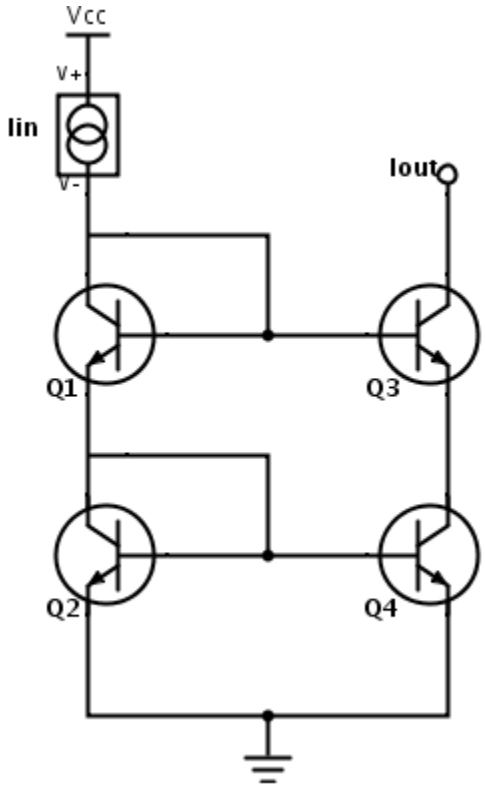

Figure 2-15: Cascode current mirror with NPN devices

from NPN bipolar transistor devices. Note that this high impedance output is necessary for the aforementioned current to voltage conversion at the high-Z node.

$$\Delta V_{highZ} = \frac{\Delta I}{Z_{highZ}} = \frac{\Delta I}{\frac{\beta r_o}{2}} \tag{2.23}$$

Having a high impedance stabilizes the high-Z node by damping changes in voltage with respect to fluctuations in current. The $\frac{r_b}{2}$ impedance contribution is from the predriver devices in the output diamond, while the $\frac{\beta r_o}{2}$ impedance is from the two cascode mirror outputs in parallel.

Finally, we analyze the base current errors attributed with the cascode current mirror. Refer once again to Figure 2-15. With respect to the input current I_{in}, I_{C1} sees an incremental loss of two base currents through the diode connected current path, one from the current into the base of *Q1*, and the second from the current through the base of device *Q3*. I_{E1} sees a gain of a base current from *Q1* from going

from the collector of the device to the emitter. Thus I_{E1} has a net base current loss of 1 base current, from device *Q3*, with respect to I_{in}. I_{C2} sees yet another loss of two base currents through the diode connected path, one from the current into the base of *Q2*, and another from the current into the base of *Q4*. Thus I_{C2} sees a net loss of three base currents, from the three devices *Q3*, *Q2*, and *Q4*.

The basis of the current mirror's functionality is that $V_{BE2} = V_{BE4}$, therefore $I_{C2} = I_{C4}$ assuming devices are sized identically and are matched. Thus the current at I_{C4}, like I_{C2}, is down three base currents with respect to the input current I_{in}. Finally, the current at the output I_{out} sees the loss of an additional base current from device *Q3*, going from the emitter current to the collector current, coming to a total of four base currents lost from the input to the output of the mirror. To sum things up:

$$I_{out} = I_{in} - I_{B3} - I_{B2} - I_{B4} - I_{B3} = I_{in} - 2I_{B3} - I_{B2} - I_{B4} \tag{2.24}$$

Note quite interestingly that the base current from device *Q1* does not show up in this aggregation of base current errors. This is an opportune result, meaning that in the cascode current mirror *Q1* can be sized and biased differently from the other three transistors without affecting the offset in current from input to output. Current can be injected into the collector of *Q2*, providing an alternate lower headroom input, without affecting the base current cancellation scheme. We will capitalize on this fact in our final design.

Also as a point of note, the cascode current mirror fixes the collector voltage of *Q4* to a single V_{BE} above the rail, the same voltage as the collector of *Q2*. The consequence of this is to prevent base-width modulation (due to the Early effect[5, p. 16]) from affecting the base current errors associated with these two devices.

In the Early effect model, the beta of a transistor device changes with device V_{CE}. The significance of this in this context is that when the collector voltage of a device is able to freely move, the base currents associated with the device can change accordingly. Now for *Q2* and *Q4* the collectors are fixed to the same volt-

age:

$$V_{C2} + V_{BE1} - V_{BE3} = V_{C4} \text{ therefore: } V_{C2} \approx V_{C4} \tag{2.25}$$

assuming devices *Q1* and *Q3* are matched.

In the model for the Early effect, the devices thus have the same betas and therefore $I_{B2} = I_{B4}$. The device at the output, *Q3*, however, is not compensated for and cannot be corrected in this fashion because the collector voltage must be able to move freely in order to serve its purpose as the high-Z node driving the output.

We add a third leg to the cascode mirror in order to implement the current drive stage, following the methods introduced in D'Aquino's patent to achieve base current cancellation as well as early effect compensation.

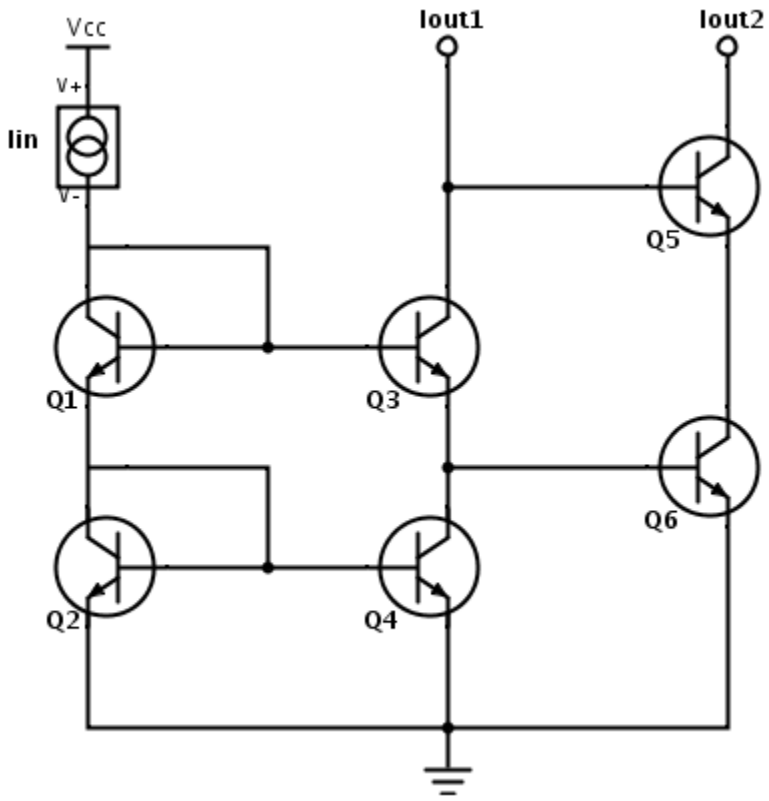

Figure 2-16: Cascode current mirror with NPN devices and third stage

Following the same analysis as in the case of the original cascode current mirror, we track the change in base current errors from I_{in} to I_{out1}. Note that I_{out2} does

not have to be base current cancelled because it is simply providing current drive to the output diamond. The voltage at the high-Z node is solely affected by the difference in currents between I_{out1} and its PNP counterpart.

I_{C1} is down two base currents from I_{in} due to the base currents of *Q1* and *Q3*. I_{E1} recovers the base current from *Q1*, and I_{C2} loses two additional base currents to *Q2* and *Q4*. Thus I_{C1} sees a net loss of three base currents due to *Q3*, *Q2*, and *Q4*. This is mirrored to I_{C4} with the same net loss of three base currents.

Now we encounter the first connection to the third stage. Now $I_{C4} \neq I_{E3}$. Instead, I_{E3} gains a base current from device *Q6* because $I_{E3} = I_{B6} + I_{C4}$. Thus I_{E3} sees a net loss of three base currents from *Q3*, *Q2*, and *Q4* and a gain of a base current from *Q6*. I_{C3} sees a loss of another base current from *Q3* going from emitter to collector of the device, and analogous to the case of the connection with *Q6*, here the connection with the base of *Q5* leads I_{out1} to step up a base current.

To recap:

$$I_{out} = I_{in} - 2I_{B3} - I_{B2} - I_{B4} + I_{B6} + I_{B5} \tag{2.26}$$

We discussed earlier (in the context of Early effect) that the voltage at the collector of *Q4* is fixed to the voltage at the collector of *Q2*, which is a single V_{BE} from the rail. The third stage transistor *Q6* whose base is connected to this node therefore satisfies:

$$V_{BE2} = V_{BE4} = V_{BE6} \tag{2.27}$$

Similar to the case of the two stage mirror, the ratio of currents in the third stage relative to the first stage is set by the ratio of areas of the transistors used. Using an emitter area sizing ratio of **1:1:2**, we can therefore approximately cancel the base current errors arising from the mirror. I_{out1} loses four base currents from the first and second stages and two base currents from the third stage, so driving the third stage at twice the base current (therefore twice the magnitude of base currents) will optimize base current cancellation to achieve $I_{out1} \approx I_{in}$. Note that the addition of

emitter degeneration to *Q2*, *Q4*, and *Q6* must adhere to a **2:2:1** ratio in order to be consistent with the area scaling of the devices, for resistance varies inversely with current through a component given constant voltage.

We now have an effective driver mirror which is internally base current cancelled and provides two output stages to suitably drive the voltage input and current drive of our output diamond buffer.

2.3.5 Output stage with driver mirrors

Designing the output diamond as well as the driver circuits has address the intended functionality of each subcircuit. The output diamond buffer has very high current gain capacity for high current drive functionality, and the driver circuits are designed to be low error.

A few intricacies arise when analyzing the connection between the driver circuit with the output diamond. Again solely analyzing one side of the amplifier:

To place the subset of the diamond pictured in context, *Q5* is one of the predriver transistors at the input of the diamond, *Q6* is acting as the drive current, and *Q7* and *Q8* are both current gain stages of the diamond with *Q8* being the monolithic 80 unit PNP device at the output of the amplifier.

Here, the aforementioned bootstrapping of the output stage serves an additional purpose: Early effect cancellation of device *Q5*. We can see this in the calculation of V_{C5}.

$$V_{C5} = V_{B5} - V_{BE5} - V_{D1} + V_{EB7} + V_{EB8} \tag{2.28}$$

$$V_{CB5} = -2V_{BE_{NPN}} + 2V_{EB_{PNP}} \tag{2.29}$$

This approximation is made because diode *D1* is implemented using a NPN bipolar junction transistor whose base and collector are shorted, thus the diode's voltage drop is characteristic of a V_{BE}. Obviously $V_{BE_{NPN}} \neq V_{EB_{PNP}}$ and these subsequent stages containing *Q7* and *Q8* will be biased at collector currents which

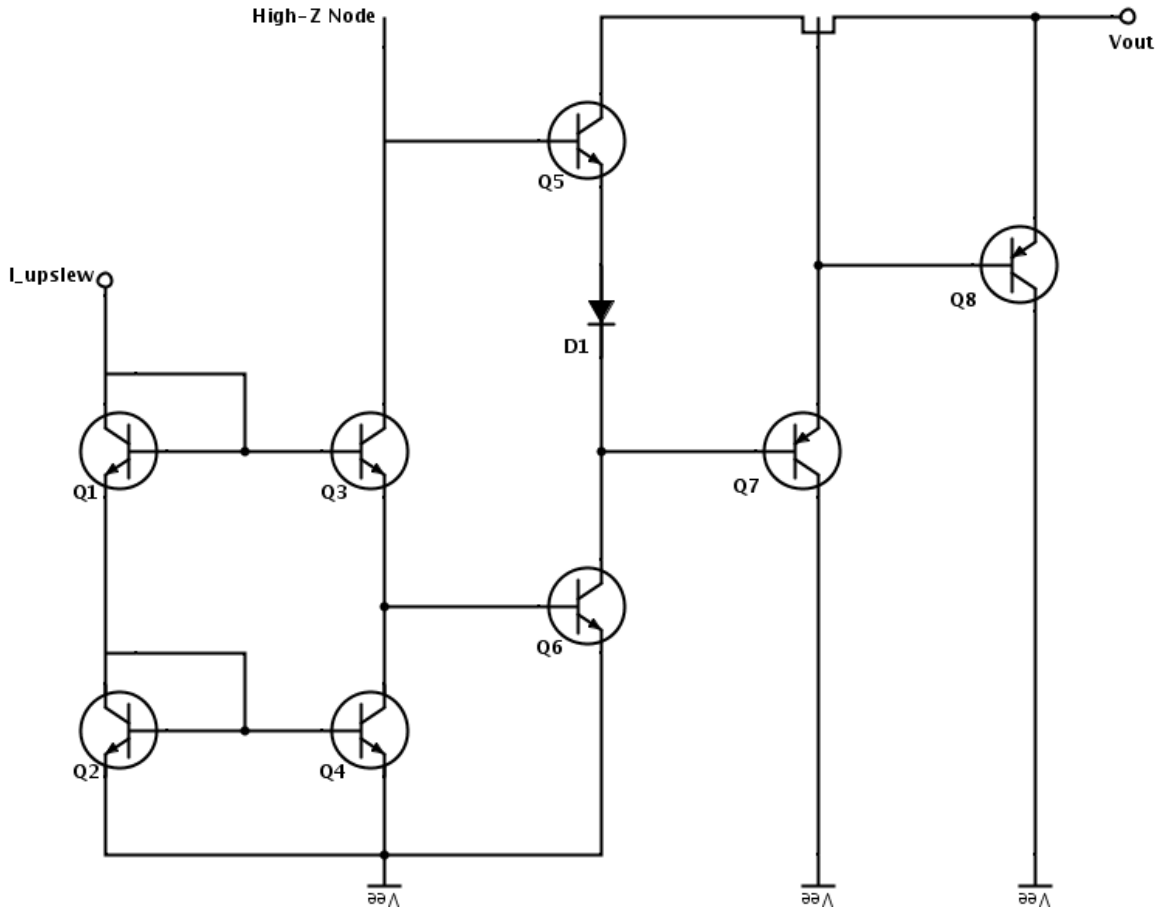

Figure 2-17: Cascode current mirror with NPN devices and third stage connected to amplifier output diamond

will be biased much higher than that of the current drive stage containing *Q5* and *D1*, thus the base-emitter voltage drops could be significantly different among the components involved in this voltage loop. But the key point of note is:

$$\Delta V_{CB5} \approx \Delta V_{CE5} \approx 0 \tag{2.30}$$

The beta of *Q5* will not change as a result of base-width modulation, thus three devices contributing base current errors in this circuit now have compensated early effect: *Q2*, *Q4*, and *Q5*. The remaining two devices, *Q3* and *Q6*, have collector voltages which are referenced to the output voltage, thus they have variable betas. However, *Q3* steals two base currents from the output whereas *Q6* adds two base currents to the output. These two devices will negate each other both at DC and

variable output voltage; thus the output current from the mirror is total base current compensated.

Finally we put the entire diamond output and driver circuitry together to demonstrate the cumulative result:

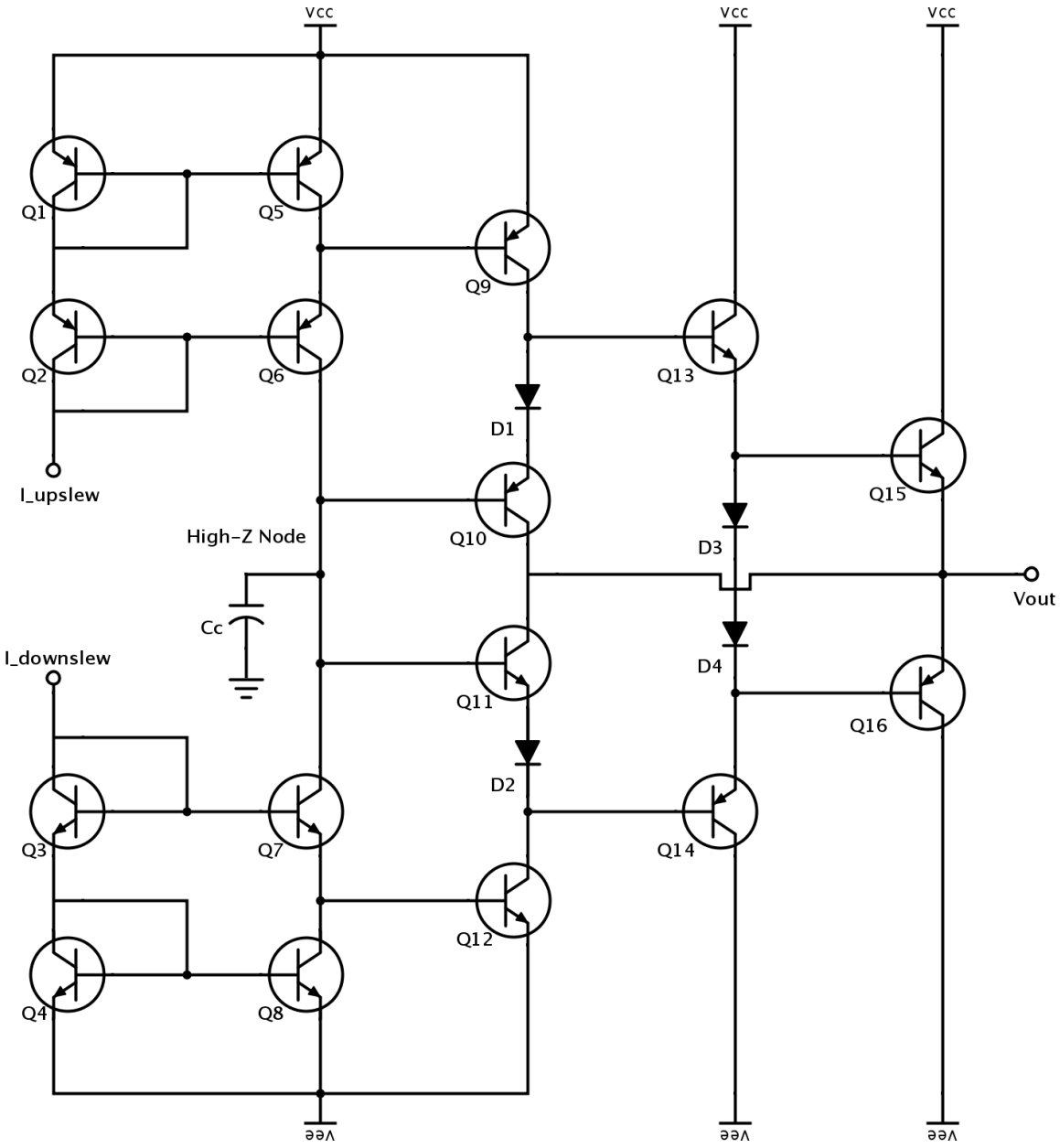

Figure 2-18: Complete transistor level representation of output stage

2.4 Current Mirrors

The function of the remaining current mirrors in this amplifier is to take current paths from the input stage of the amplifier, manipulate them, and produce the upslew and downslew currents into the driver mirrors which control the output stage of the amplifier. This part of the amplifier generally wants to be as simple as possible; fewer mirrors means smaller time lapse in the signal's transient path from input to output, and a simpler design means fewer stages and therefore lower quiescent current draw. The approach taken in this thesis assignment focuses less on simplicity, however, and emphasizes an approach which provides as ideal of a base current cancellation scheme as possible in order to minimize DC error of the amplifier.

2.4.1 Design Strategy

To represent the design logic of the current mirrors, we initially symbolically represent the H-Bridge, our input stage, and the input to our current mirrors. Formerly depicted in Figure 2-8, the H-Bridge can be modelled as two diamonds with a g_m resistor. Recall that in our version we have eight output current paths due to DC components.

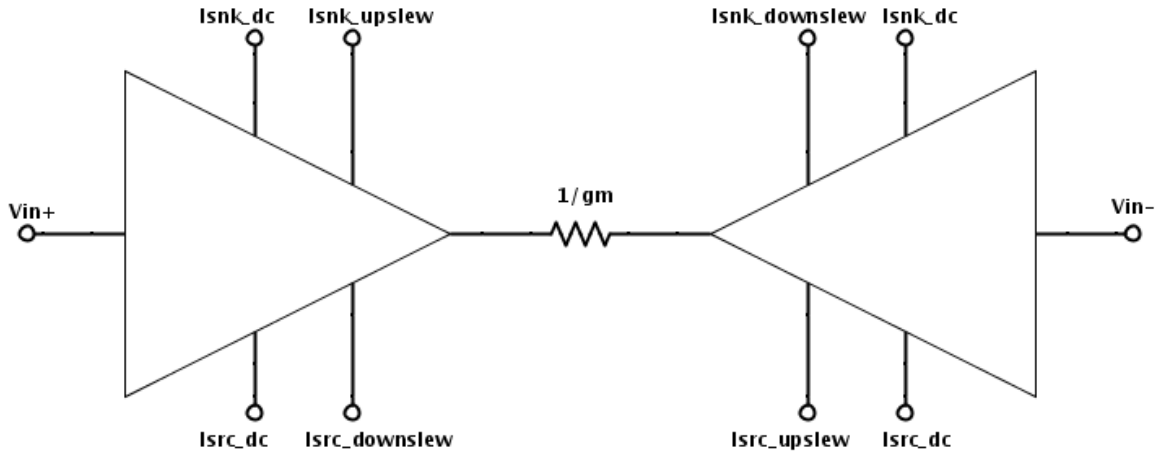

Figure 2-19: Model of H-Bridge variant input stage

The current mirrors will operate on all eight current outputs selectively to achieve

two goals in their interface with the output current drivers:

1. Upslew currents must be converted to sink currents and connected to *I_upslew*.

2. Downslew currents must be converted to source currents and conected to *I_downslew*.

DC currents can connect to either *I_upslew* or *I_downslew* because they do not vary as the input changes, but again only source currents may connect to *I_upslew* whereas only sink currents may drive *I_downslew*. There are a number of ways this can be implemented, even more if one chooses to selectively use only some of the signal current paths from the output stage.

We wish to use every path from the input stage, however, to get the maximum utilization out of the input signal current paths. The simplest way this can be implemented using mirrors is as follows:

Note that the signal path currents out of the left side of the H-Bridge are already in the correct direction to connect directly to the upslew and downslew current drivers. Therefore they do not need to be acted upon by the current mirrors. However, *Isnk_downslew* from the right side of the H-Bridge is a sink current and therefore must be mirrored to source into the downslew current driver *I_downslew*. Similarly, *Isrc_upslew* from the inverting side of the H-Bridge is a source current and must pass through a current mirror in order to drive the upslew current driver through *I_upslew*. For the sake of simplicity, we connect the DC current paths to their signal dependent counterparts. The real reason to split them is to deal with base current errors.

We will now superimpose the base current errors upon this scheme which were introduced in the discussion of our H-Bridge variant in Figure 2-9. Recall that the sink currents are down a NPN base current, which is equivalent to an incremental NPN base current upward. The source currents at the bottom of the input stage are down a PNP base current, which can be viewed as an incremental PNP base current upward.

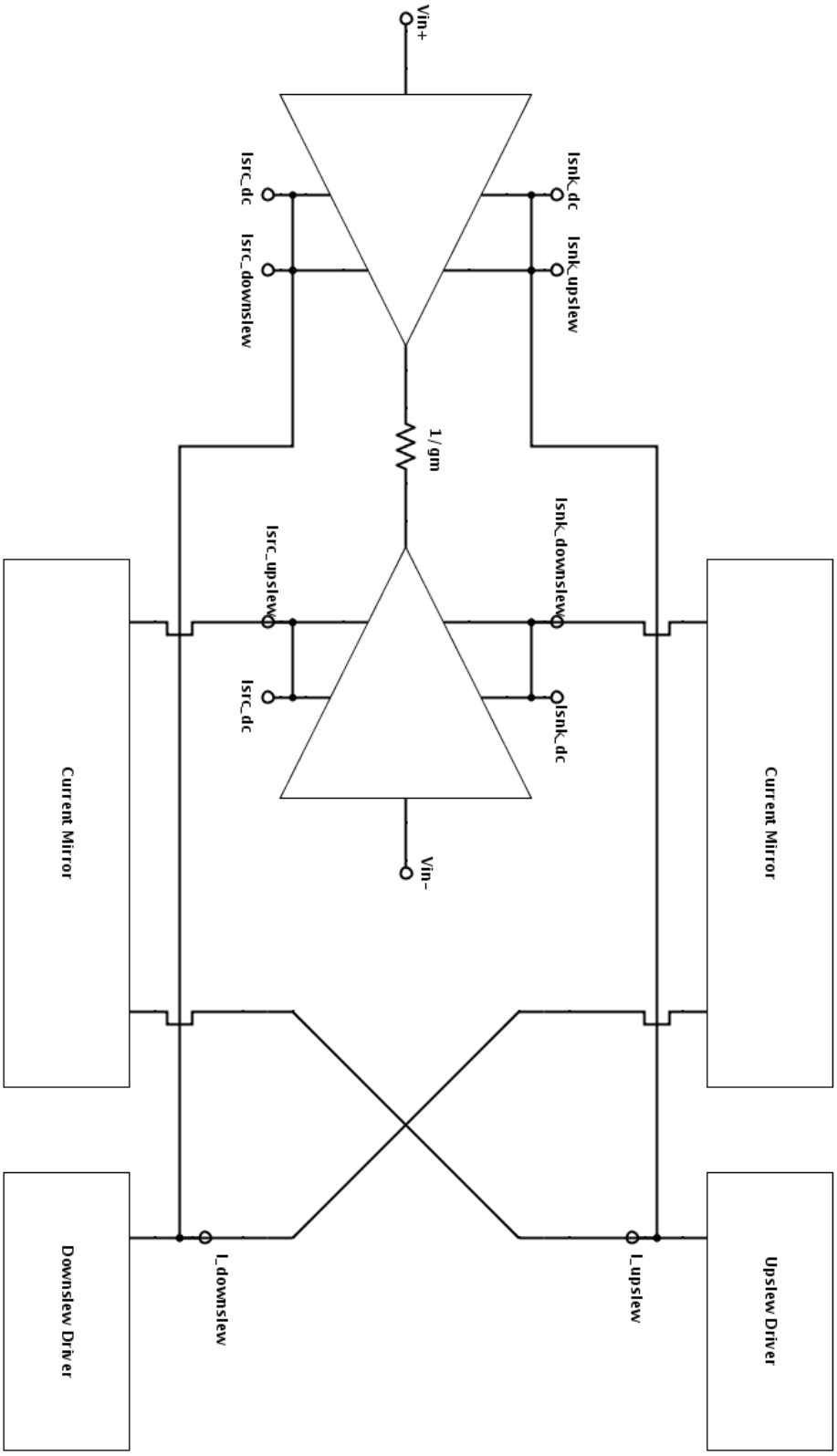

Figure 2-20: Current mirror implementation

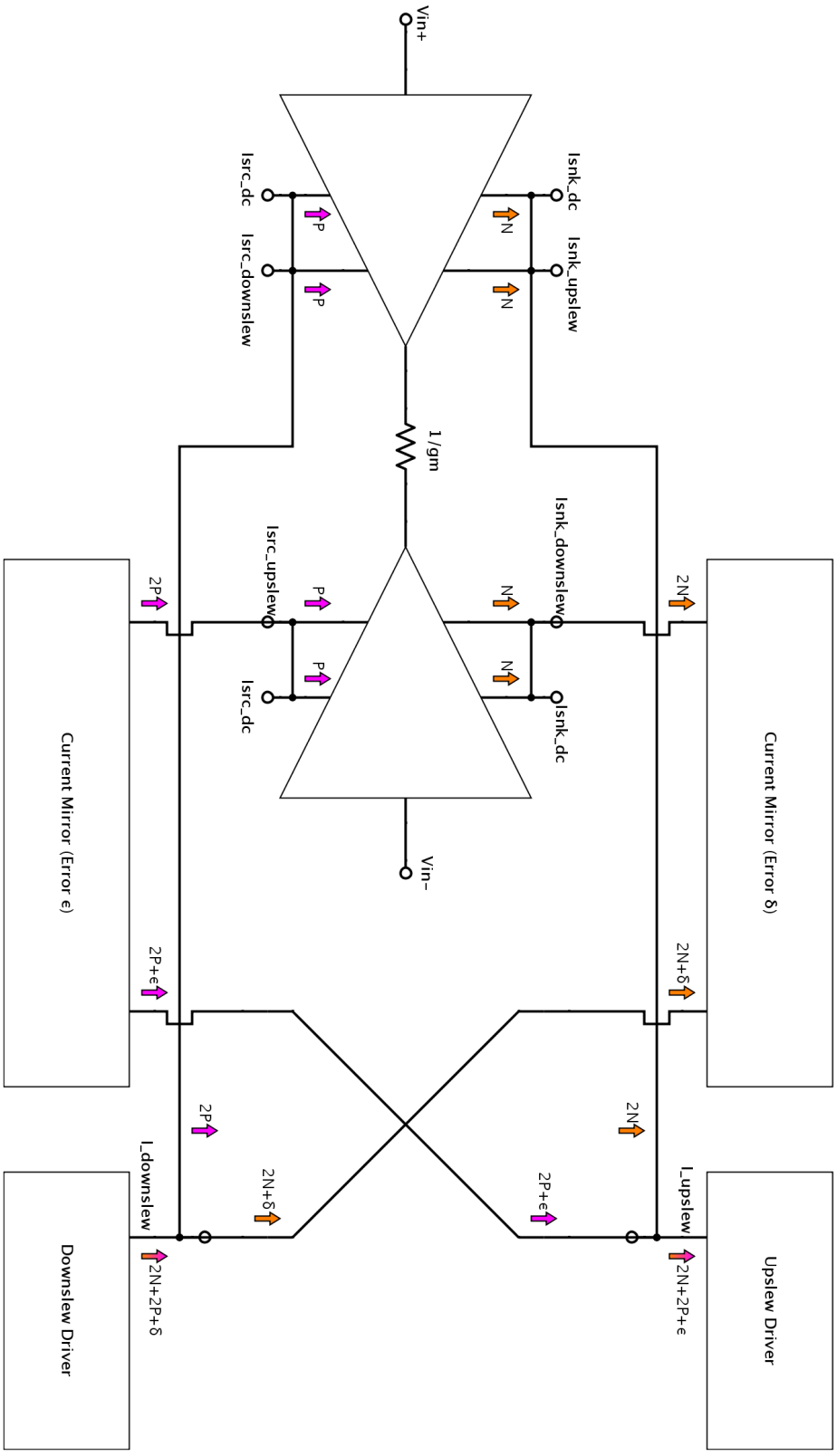

Figure 2-21: Current mirror implementation with base current errors superimposed

We now look at these base current errors and propagate them through the current mirrors in Figure. Assume that the current mirror at the high supply has a current translational offset of δ and the current mirror at the low supply has a current error of ϵ. *I_upslew* sees a net base current error of $2N+2P+\delta$ while *I_downslew* sees a net base current error of $2N + 2P + \epsilon$. The current mirrors that have been introduced thus far are the simple mirror, which has an offset of 2 base currents (Equation 1.22), and the cascode mirror which has an offset of 4 base currents (Equation 2.56). Additionally, the current mirror at the high supply rail would be implemented using PNP transistor devices while the low supply current mirror is designed using NPN transistor devices; the base current errors would be off by the number of base current errors multiplied by the difference in base currents between NPN and PNP devices.

We now analyze the Wilson current mirror, a four transistor current mirror like the cascode current mirror, whose current error between input and output currents is significantly lower than a single base current error (first-order base current compensated). It is shown in Figure 2-22. We use this current mirror because we need a mirror which does not introduce base current errors, and we do not care about input headroom of the mirror because it is not directly referenced to the input stage.

Initially I_{in} loses two base currents to *Q1* and *Q3* through the diode-connected connection across the base-collector of *Q1*. I_{C1} to I_{E2} recovers the base current lost from *Q1*. Thus I_{C2} is down a single base current, the base current from *Q3*. $V_{BE2} = V_{BE4}$, therefore I_{C4} like I_{C2} is down a single base current (from *Q3*) relative to I_{in}.

Now the analysis changes from the case of the cascode mirror. Going from I_{C4} to I_{E3} gains two base currents, the base currents going into the devices *Q2* and *Q4*.

$$I_{C3} = I_{E3} - I_{B2} - I_{B4}; I_{E3} = I_{C3} + I_{B2} + I_{B4} \tag{2.31}$$

In total I_{E3} is down a single base current from *Q3* and up two base currents from *Q2* and *Q4*. Finally I_{out} loses an additional base current to *Q3* by going from

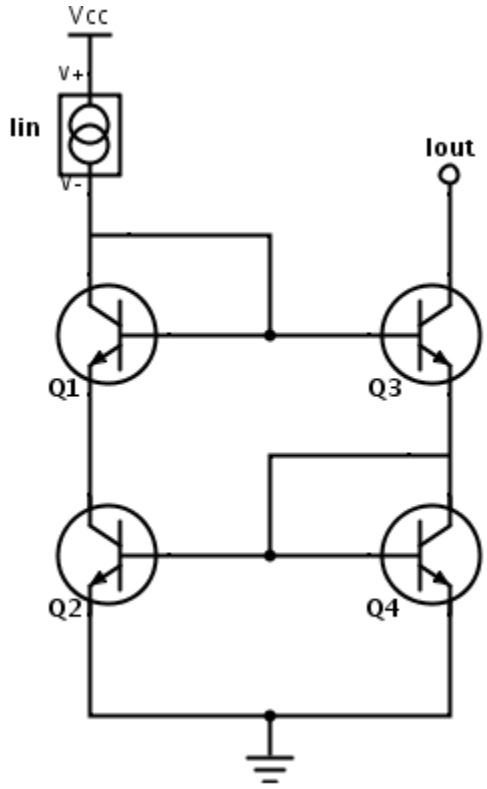

Figure 2-22: Wilson current mirror with NPN devices

emitter to collector, bringing the sum total of a loss of two base currents both from *Q3* and a gain of two base currents from *Q2* and *Q4*. To recap:

$$I_{out} = I_{in} - 2I_{B3} + I_{B2} + I_{B4} \approx 0 \tag{2.32}$$

This cancellation is true provided that the devices are matched, sized identically, and biased at the same currents. All of the devices are the same type whether NPN or PNP, so the base currents should cancel ideally. Note that just as in the case of the cascode current mirror *Q1* does not show up in the net base current errors, thus it may be biased differently and sized differently without affecting the performance of the current mirror.

Thus if we were to use a Wilson mirror to accomplish the current mirror scheme presented, we have a net cancellation of base current errors, the topology is simple, and the amplifier is complete.

2.4.2 Headroom

But the Wilson current mirror is not an option, for it breaks the input headroom of the amplifier. In the discussion of the H-Bridge input stage the headroom was cited as $V_{BE} + V_{CE_{sat}}$. Feeding the current output of the input stage into a Wilson current mirror extends the headroom even further to $2V_{BE} + V_{CE_{sat}}$, $2V_{BE}$ due to the Wilson current mirror's input headroom and $V_{CE_{sat}}$ due to the overall headroom of the diamond from input to collector output. This is also an issue for the connections which feed directly from the input stage into the cascode current mirrors driving the diamond output buffer, for the cascode current mirror also has an input headroom of $2V_{BE}$.

One possibility that was explored was to simply feed the current input into the lower stage of the Wilson mirror, recovering the single V_{BE} of headroom while biasing the higher stage transistor with a constant current source. (The voltage at the collector of *Q2* is:

$$V_{C2} = V_{BE4} + V_{B3} - V_{BE1} \approx V_{BE} \tag{2.33}$$

This low input headroom use of the Wilson current mirror is demonstrated in Figure 2-23.

Q1 is biased at I_{bias} while the other three transistors are biased at $I_{bias} + I_{in}$, but this does not affect the net base current errors of the Wilson current mirror because the base current of *Q1* does not have a contribution. The problem with this approach arises from a transient analysis of the functionality of this mirror. I_{bias} is constant while I_{in} fluctuates with the signal current. When the amplifier is slewing hard, I_{in} will be significantly higher than I_{bias}. The voltage at the emitter of *Q1* will rise up logarithmically with I_{in} while the voltage at the base of *Q1* will initially stay constant because it is solely biased with I_{bias}. This will cause the voltage drop V_{BE1} to crush below the transistor's turn-on voltage of $\sim 0.7V$, and the voltage could even go negative. In either case, device *Q1* will turn off, compromising the performance of the current mirror. For this approach to work one would need

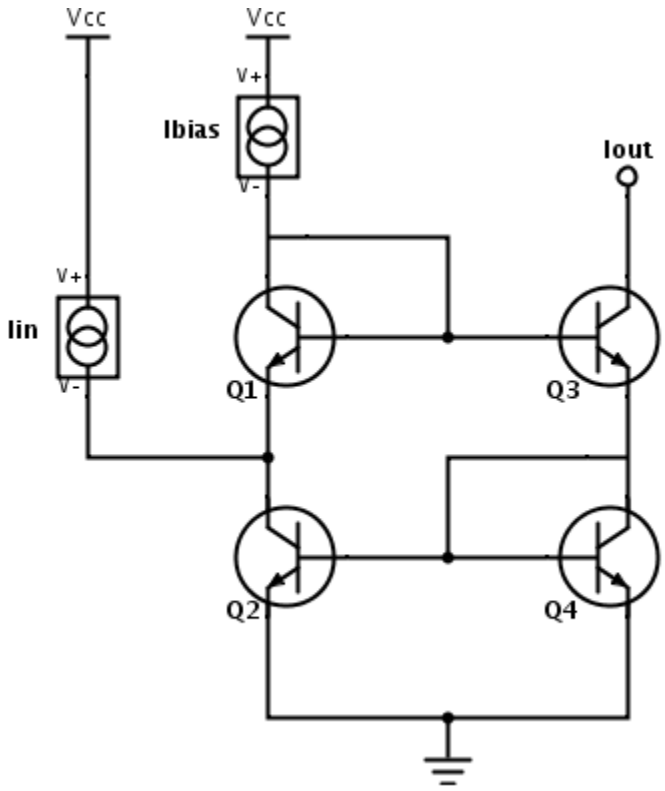

Figure 2-23: Wilson current mirror with low headroom input

to have an I_{bias} which varies with the I_{in}, but we already know that we cannot draw directly from the input stage because of the headroom of this input. We can however use this approach with the cascode current mirror drivers because we are feeding bias current from the other side of the amplifier through mirrors and into the higher headroom input, thus I_{bias} will vary as I_{in}.

In order for the input headroom to not be extended, the input stage must feed into a simple current mirror or a resistor. Note that headroom is indeed a very valuable resource for this amplifier and for its intended purposes because headroom corresponds to power efficiency, the headroom of the amplifier at the input and output are portions of the supply rail which are not accessible by the driver or the load. Input headroom is especially important because in high voltage applications the amplifier will often be used in high gain configurations, multiplying up the inaccessible voltage swing range. Our implementation must stick to the minimum headroom of the H-Bridge.

2.4.3 Implementation

Figure 2-24 symbolically shows the current mirror implementation that we use in this thesis project, and the claim is made that this configuration allows for both an input headroom of $V_{BE} + V_{CE_{sat}}$ and is approximately base current cancelled.

Initially, we check the input headroom by looking at all the collector node outputs of the input stage. These inputs must all connect to simple mirrors or the low input headroom connections of a cascode or Wilson current mirror. Starting with the left side of the H-Brige: *Isnk_dc* connects to a PNP simple mirror, *Isnk_upslew* connects to the low headroom input of the upslew driver cascode current mirror, *Isrc_dc* connects to a NPN simple current mirror, and *Isrc_downslew* connects to the low headroom input of the downslew driver cascode current mirror. On the right side of the H-Bridge, *Isnk_downslew* feeds into a PNP simple mirror while *Isnk_dc* connects to the low input headroom of a Wilson current mirror. *Isrc_upslew* connects to a NPN simple current mirror and *Isrc_dc* connects to the low headroom input of a NPN Wilson mirror. Thus, input headroom is not violated.

Next we evaluate the connections of the signal paths ensure that upslew and downslew currents make it to their corresponding driver. The trajectory of the signal dependent paths is relatively simple; one side feeds directly into the driver devices while the other side passes through a single simple mirror. The complex paths where the current must pass through two current mirrors only applies to the DC paths which will not change with the input, thus slew rate and the transient responsivity of the amplifier is not adversely affected by the intricacy of this current mirror scheme. The signal path still takes the same paths: one directly into the driver mirror and the other through a single simple mirror, thus one can expect the transient performance of this amplifier to be on par with that of the simplest implementation formerly discussed.

This approach uses low headroom inputs to the Wilson and cascode mirrors, but the problem outlined before is no longer an issue because in each case the second stage input tracks the lower stage input. For the case of the Wilson mirrors,

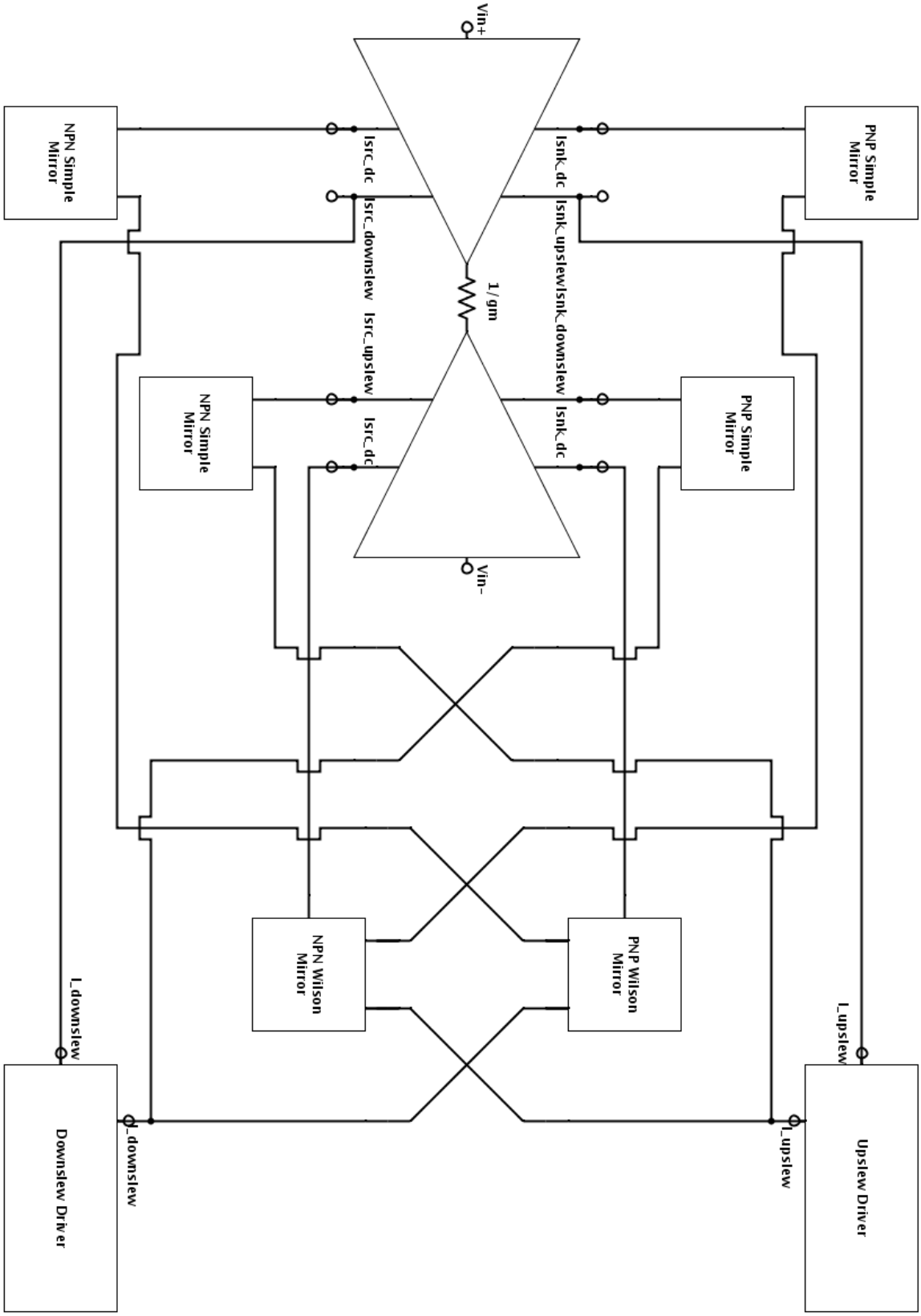

Figure 2-24: Low headroom current mirror implementation

only DC components pass through the mirror. Therefore there is absolutely no issue involved when the amplifier is slewing; the current through this path does not change. The cascode mirror sees equal signal-dependent paths at both of its inputs. To be fair, the low input headroom sees the current coming directly out of the H-Bridge while the higher input headroom sees the current coming out of the H-Bridge and a simple current mirror, so the timing difference between the inputs is effectively the time it takes for the signal path to travel through a single simple mirror. In simulation we later find this to be on the order of nanoseconds and the upper stage transistor does not turn off or even have noticeable drop in V_{BE} as a result of this; problem solved.

Next, we verify the claim that this current mirror scheme achieves base current cancellation to achieve matching currents at the driver inputs. This analysis builds on the understanding that simple mirrors contribute two base current errors of their respective NPN or PNP type, Wilson mirrors are base current error negligible, and the slew driver modified cascode current mirrors are base current error cancelled.

Figure 2-25 effectively demonstrates how the base current errors from the input stage and current mirrors propagate throughout the current mirror network in this amplifier. The elegance of this design arises from symmetry and the matching of base current errors from matching sources. That is to say that the base current errors from the H-Bridge are matched against base current errors also from the H-Bridge while each NPN and PNP simple current mirror has a counterpart to produce the same identical base current error and send it to the other side of the amplifier. This design effectively fights DC current paths against signal dependent paths in order to achieve this. In Figure 2-25, NPN and PNP base current errors arising from the diamond are denoted as N and P respectively, just as before. The base current errors from the simple current mirrors are shown as n and p: NPN and PNP device base current errors, respectively.

As a brief digression, this is not necessarily ideal notation because the base current error contribution from each device in the simple mirror is not equal (one sees

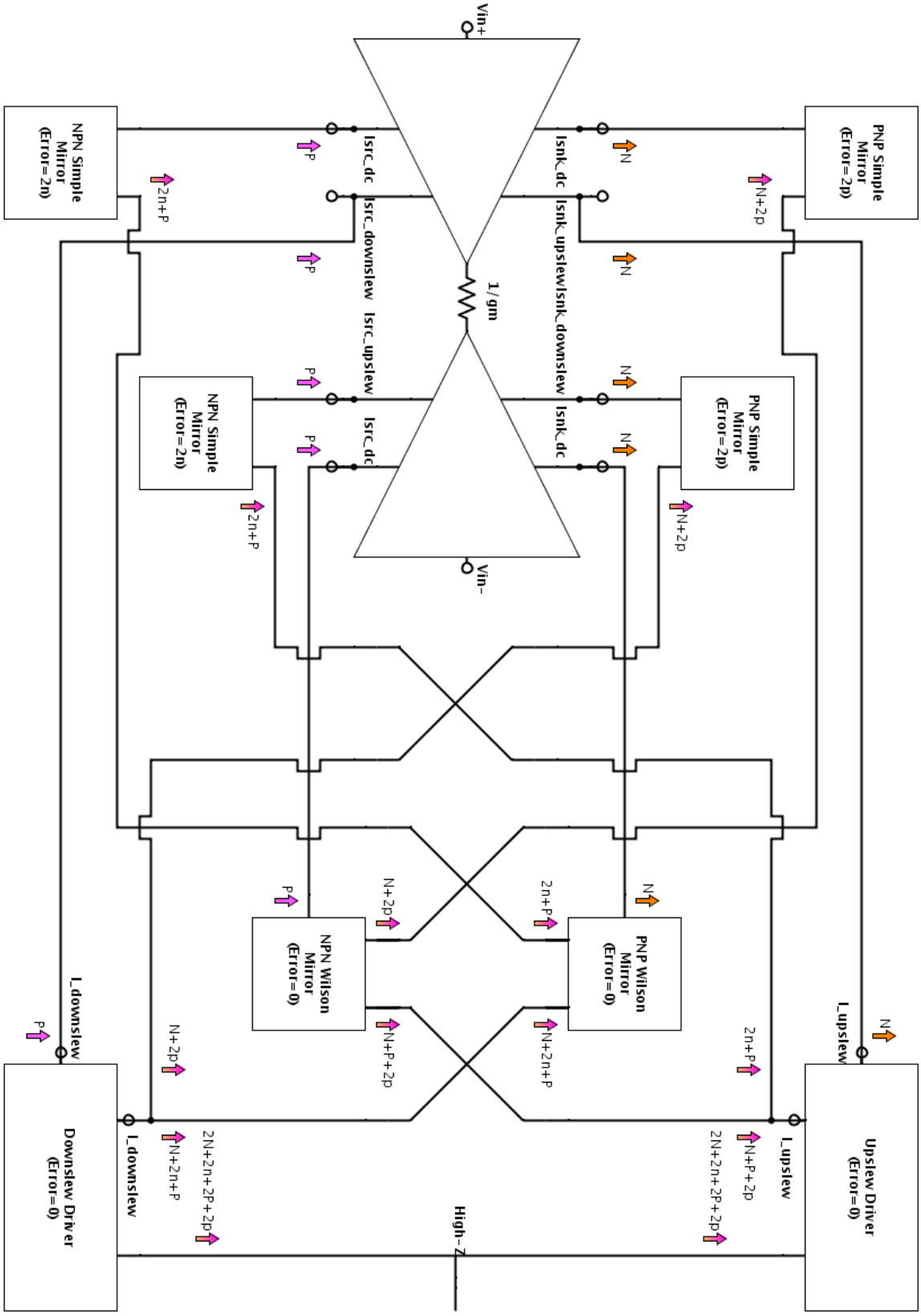

Figure 2-25: Low headroom current mirror implementation with superimposed base current errors

$V_{CE} = V_{BE}$ while the other sees $V_{CE} = V_{CC} - 2V_{BE} - V_{EE} \gg V_{BE}$), thus the devices have radically different betas and thus currents. More adequately one should substitute $2n$ with δ and $2p$ with ϵ. Regardless, the analysis produces the same result, just in a less semantically rigorous fashion. Also note that this influenced the key design decision of using a Wilson current mirror rather than some other lower input headroom internally base current compensated mirror. In the simple current mirror feeding into the slew driver current mirror, its output device sees a collector voltage of $2V_{BE}$ from the opposing supply rail because of the cascode current mirror at the input of the driver mirror. In order to get the base currents from each type of simple mirror to match, the other simple mirror must also have its output feeding into $2V_{BE}$ from the opposing rail. Quite conveniently, the Wilson current mirror has $2V_{BE}$ of input headroom at its input and is base current compensated, allowing us to ideally work each simple current mirror against each other.

The reason why we separate the distinction between these two types of base current errors (from the H-Bridge and from the simple mirrors) is due once again to base-width modulation, the Early effect, wherein the beta of the devices varies as the device collector-base voltage. In the H-Bridge, the devices at the output all see the same collector voltage: NPN devices at the top of the diamonds see $V_{CC} - V_{BE}$ while PNP devices see $V_{EE} + V_{BE}$. In the case of the simple mirrors, however, the situation is much different. For a NPN simple mirror the input device will see a collector voltage of $V_{EE} + V_{BE}$ while the collector voltage of the output device is $V_{CC} - 2V_{BE}$, for the output of the current mirror drives either a Wilson current mirror or a cascode current mirror. Analogously the PNP simple mirror will see a collector voltage at the input of $V_{CC} - V_{BE}$ and a collector voltage at the output of $V_{EE} + 2V_{BE}$. This in principle is why it is very hard to cancel the base current error of a singular simple mirror; the base current error contribution from each of the two devices is very different because of the Early effect. In this scheme we overcome this by replicating the currents and therefore the errors, thus achieving indistinguishability.

The total base current error from each side of the amplifier sums up to $2N+2n+$

$2P+2p$ on both sides of the amplifier, so the High-Z node at DC sees approximately identical currents from either side of the amplifier. This internally trivializes the overall V_{OS}, which we measure in simulation to be on the order of microvolts, a nontrivial achievement given supply range of 40 Volts.

2.5 Block Diagram

Putting all the pieces together we now have a block diagram of the signal path architecture of the amplifier, shown in Figure 2-26. This encapsulates the result of the theoretical design of the amplifier, omitting process, sizing, and current bias considerations. The amplifier has $V_{BE} + V_{CE_{sat}}$ headroom at the input due to the H-Bridge and $V_{BE} + 2V_{CE_{sat}}$ headroom at the output due to the $2V_{BE}$ diamond buffer driving the output. This design has eighteen total rail to rail transistor stages: eight from the H-Bridge, six from the current mirrors, and four from the output diamond buffer and its current drivers. The input-referred offset (V_{OS}) of this amplifier is minimized because the two input terminals have identical input impedance, the internal voltage drop across the input is effectively null, and the internal base current errors arising from differences in NPN and PNP devices are cancelled.

This concludes the design of the amplifier signal path.

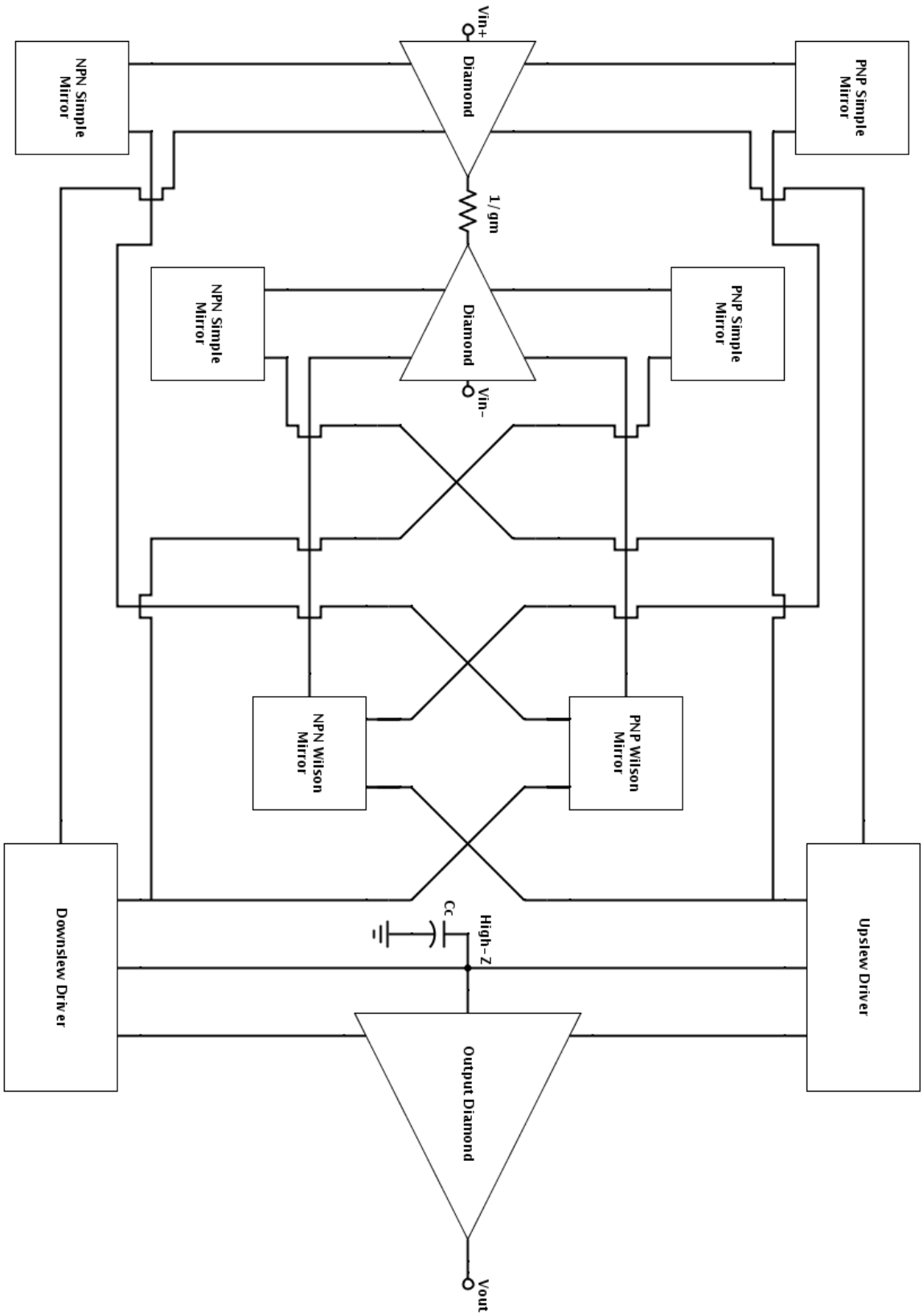

Figure 2-26: Block diagram of amplifier signal path

Chapter 3

Features

We now transition to a new stage of the design project: *features*. Whereas the functionality of an amplifier is well defined and there is a simple metric for judging its efficacy (datasheet specifications), the topic of features is much more open ended, subject to the resourcefulness of the designer. Features may manifest themselves in multiple different ways and are either external or internal. External features appear as in the integrated circuit as additional pins, requiring some sort of input from the circuit's user in order to unlock additional modes of operation or configurability. Internal features aid in the amplifier's ability to function without being explicitly required. This topic will discuss features that belong to both subsets.

3.1 Configurable g_m

Early on, we presented the rationale behind the use of an H-Bridge input stage, citing the signal path benefits of the topology including the potential for high slew rate and low input-referred offset. The input stage was also chosen with the intent to allow for additional configurability of the amplifier, in the form of the g_m resistor. This resistor across the two diamonds in the input stage will be externally chosen by the chip user (requiring two additional pins on the package) and can be used to tune the frequency response of the amplifier. By doing this, we wish to allow for maximum configurability, discretizing bandwidth and gain. To elaborate on this,

we delve into the small signal models governing the amplifier.

3.1.1 Small signal derivation

Initially we look at the simplest model of a voltage feedback amplifier, with open-loop gain $A(s)$, driven in a non-inverting feedback configuration, and we derive the transfer function $\frac{V_{out}}{V_{in}}$.

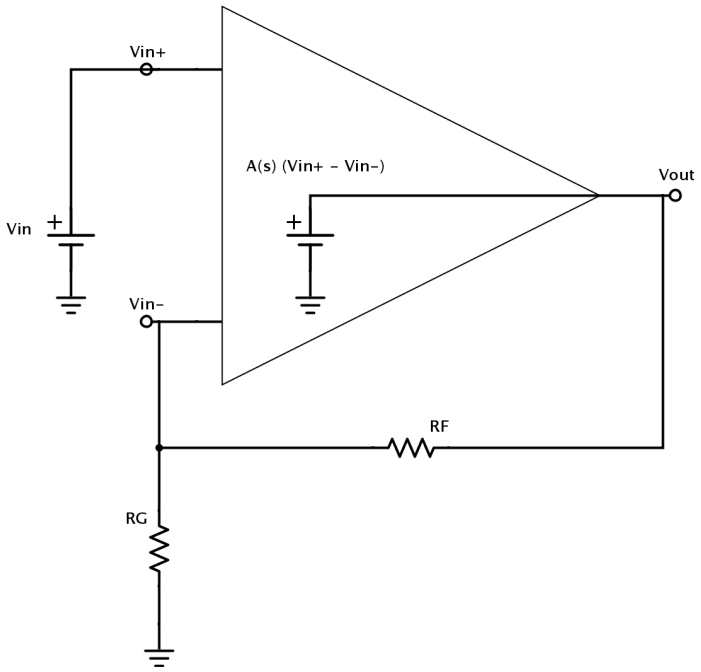

Figure 3-1: Simple non-inverting voltage feedback amplifier

$$V_{out} = A(s)(V_{in+} - V_{in-}) \tag{3.1}$$

$$V_{in-} = \left(\frac{R_G}{R_F + R_G}\right) V_{out} \tag{3.2}$$

$$\frac{V_{out}}{V_{in}} = \frac{A(s)}{1 + A(s)\left(\frac{R_G}{R_F+R_G}\right)} \tag{3.3}$$

Equivalently:

$$\frac{V_{out}}{V_{in}} = \left(1 + \frac{R_F}{R_G}\right) \frac{1}{1 + \frac{1}{A(s)}\left(1 + \frac{R_F}{R_G}\right)} \tag{3.4}$$

This is the transfer function of the amplifier, which is solely dependent upon the

amplifier's internal open loop gain and its feedback resistors. Note that $1 + \frac{R_F}{R_G}$ is our closed loop gain. As one would expect, at low frequencies the gain is in fact the closed loop gain. More information about the system (number of poles and their locations) depends on the nature of $A(s)$. Fortunately, because we have already established the internal structure of our amplifier, it is possible to derive a simple expression for $A(s)$. Figure 3-2 demonstrates our amplifier with the configurable g_m resistor.

Figure 3-2: Non-inverting voltage feedback amplifier with internals

$$I = g_m \cdot (V_{in+} - V_{in-}) \tag{3.5}$$

$$V_{out} = \frac{I}{sC_c} = \frac{g_m \cdot (V_{in+} - V_{in-})}{sC_c} \tag{3.6}$$

$$A(s) = \frac{V_{out}}{V_{in+} - V_{in-}} = \frac{g_m}{sC_c} \tag{3.7}$$

We can now plug this expression for $A(s)$ to derive a more complete expression for the transfer function of the amplifier.

$$\frac{V_{out}}{V_{in}} = \left(1 + \frac{R_F}{R_G}\right) \frac{1}{1 + \left(1 + \frac{R_F}{R_G}\right) \frac{sC_c}{g_m}} \tag{3.8}$$

It becomes immediately apparent that this model represents a single pole system whose pole frequency is at:

$$f_{pole} = \frac{g_m}{2\pi C_c} \left(\frac{1}{1 + \frac{R_F}{R_G}}\right) \tag{3.9}$$

Another key point of note here is the following:

$$\left(1 + \frac{R_F}{R_G}\right) \cdot f_{pole} = \frac{g_m}{2\pi C_c} \tag{3.10}$$

The closed loop gain multiplied by the pole frequency (which correlates to the

bandwidth frequency) evaluates to a quantity which depends on C_c and g_m. In typical voltage feedback architectures, the amplifier is packaged with a fixed input stage and a fixed compensation capacitance. These values are assumed to be constant, and this is the premise behind the notion that the gain bandwidth product of voltage feedback amplifiers is constant. Note that this assessment only applies to the theoretical single pole systems, and for amplifiers which have more poles because of additional gain stages or simply because of the load and parasitics, gain bandwidth constancy only applies in the single pole regime of the amplifier, between f_{pole1} and f_{pole2}.

By permitting the chip's user to set R_F, R_G, and g_m (in the form of a $\frac{1}{g_m}$ resistor), the user now has additional control over gain and bandwidth of the part. It is probably not practical to allow configurability of C_c, as this is partially governed by parasitic capacitances in the amplifier. As the user chooses to extend the gain of the amplifier, so too can he or she increase the transconductance of the input stage in order to achieve the same bandwidth as that of a lower gain configuration. This configurability has limitations; for a given g_m resistor $R_I = \frac{1}{g_m}$, the minimum value of R_I is limited by emitter degeneration and r_E of the exposed devices in the H-Bridge. Additionally, one could put a small capacitance across the terminals of the g_m resistor (in parallel) to artificially extend the bandwidth of the amplifier. At higher frequencies the capacitance will appear as a progressively lower impedance, perhaps negating g_m roll-off as a function of frequency and therefore possibly extending the bandwidth tied to f_{pole}.

3.1.2 Bandwidth-Phase Margin tradeoff

Most importantly, configuring the g_m resistor allows an inherent trade-off between bandwidth and stability, in the form of phase margin. As the pole is pushed outward, the bandwidth of the amplifier is extended. This is accomplished by raising g_m of the input stage by lowering R_I. Loop gain is equal to product of the forward and feedback gains[13] ($A\beta$ in the simple feedback model). The frequency at which

loop gain is unity is also known as crossover frequency.

$$\text{Loop Gain } = A(s)\left(\frac{R_G}{R_F+R_G}\right) = \frac{g_m}{sC_c}\left(\frac{R_G}{R_F+R_G}\right) = \frac{g_m}{2\pi f_c C_c}\left(\frac{R_G}{R_F+R_G}\right) \tag{3.11}$$

An increase in g_m to raise the bandwidth of the amplifier will thus increase the loop gain for a given frequency. Thus a loop gain of one will occur at a higher crossover frequency f_c. The phase margin is the difference between the phase of the function and negative 180 degrees at crossover frequency. At a higher crossover frequency, the overall phase of the function will be lower (as is the nature of phase with poles), and thus the phase margin will be lower. This illustrates that an increase in bandwidth will be met by a decrease in phase margin, a sacrificing stability for higher frequency performance. This is especially useful for pushing the limitations of the part.

3.2 Disjointed Supplies

The amplifier's current mirror implementation first presented in Figure 2-24 on Page 72 was chosen with the motive of enabling a topology which would allow the amplifier's user to utilize different voltage supply rails at the input and the output of the amplifier without detracting from the performance of the amplifier. This sort of feature offers the potential for a significant amount of quiescent power conservation, demonstrating an inefficiency in current amplifier architectures. When you are using an amplifier in a high gain where the input voltage will only have a certain range of values and the output voltage will have a much wider range of values (input range $\cdot$ gain), it does not make sense to use the same voltage rail at both the input and output because the inaccessible voltage range corresponds to a power loss.

3.2.1 Power considerations

Classically, the power efficiency of an amplifier is defined as the ratio of power delivered to the load divided by the total power from the supply rails.

$$\eta = \frac{P_{out}}{P_{supply}} \tag{3.12}$$

The power delivered from the power supply consists of two components, the power delivered to the load and power burned in the amplifier.

$$P_{supply} = P_{out} + P_{amp} \tag{3.13}$$

Power burned in the amplifier is necessary for signal amplification and for biasing the circuit. However, we seek to minimize P_{amp} and therefore P_{supply} in order to maximize the efficiency η of the power amplifier. P_{out} is dependent on the signal and on the impedance of the load, which correspond to the configuration of the amplifier.

3.2.2 Unified Supplies

Let us commence by analyzing a model of an amplifier configuration with fixed gain A and a single set of supply rails V_{cc} and V_{ee}, positive and negative voltages, respectively. This single set of rails is seen at both the input and output voltages, and the quiescent currents I_{qi} and I_{qo} are the DC currents seen by the input and output halves of the amplifier. This is shown in Figure 3-3.

In the case of the same supply rails at the input and output halves of the amplifier, the power delivered from the supply is simply the net current multiplied by the single set of voltage rails:

$$P_{supply} = (I_{qi} + I_{qo})(V_{cc} - V_{ee}) = (I_{qi} + I_{qo})V_{sr} \tag{3.14}$$

The minimum power required from the supply in order to transmit a particular signal with input voltage swing V_{isw} and gain A, however, is much less:

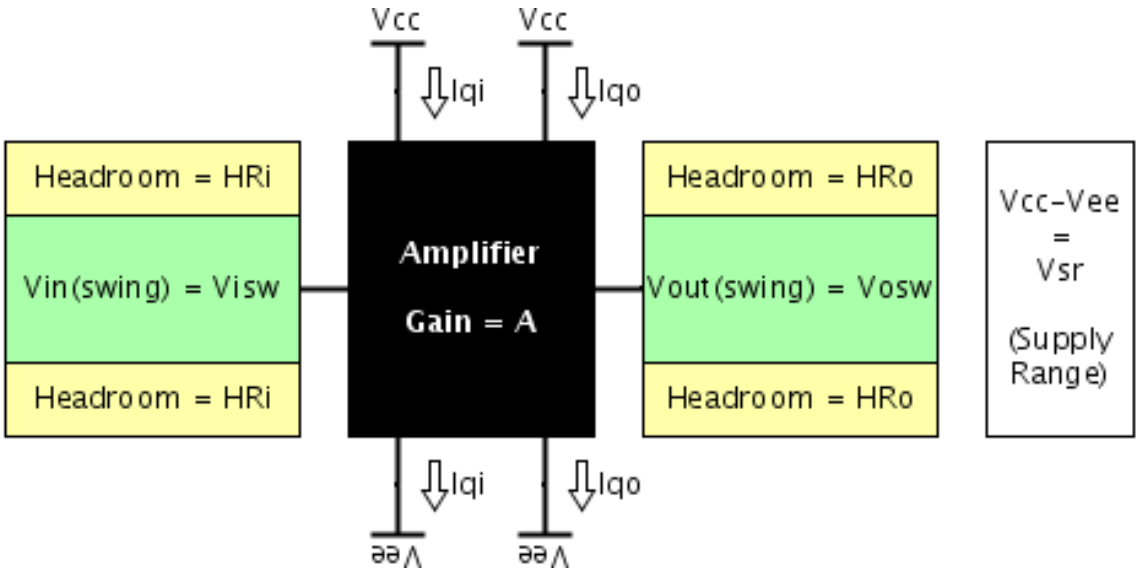

Figure 3-3: Power evaluation of amplifier with single set of voltage supplies

$$P_{supply_{min}} = I_{qi} \cdot (V_{isw} + 2HR_i) + I_{qo} \cdot (V_{osw} + 2HR_o) \tag{3.15}$$

For a given V_{isw} and V_{osw}, the relationship is simple, defined by the gain A.

$$V_{osw} = A \cdot V_{isw} \tag{3.16}$$

$$P_{supply_{min}} = I_{qi} \cdot (V_{isw} + 2HR_i) + I_{qo} \cdot (A \cdot V_{isw} + 2HR_o) \tag{3.17}$$

For a given set of input and output headrooms and quiescent currents (subject to internal amplifier design as opposed to external applied input signal and voltage rails):

$$P_{excess} = P_{supply} - P_{supply_{min}} \tag{3.18}$$

$$P_{excess} = (I_{qi} + I_{qo})V_{sr} - (I_{qi} \cdot (V_{isw} + 2HR_i) + I_{qo} \cdot (A \cdot V_{isw} + 2HR_o)) \tag{3.19}$$

$$P_{excess} = I_{qi}(V_{sr} - (V_{isw} + 2HR_i)) + I_{qo}(V_{sr} - (A \cdot V_{isw} + 2HR_o)) \tag{3.20}$$

$$P_{excess} = P_{excess_{input}} + P_{excess_{output}} \tag{3.21}$$

Obviously, we wish to minimize P_{excess}.

Given:

$$P_{supply} \geq P_{supply_{min}}, \text{ therefore } P_{excess} \geq 0 \tag{3.22}$$

$$V_{sr}, V_{isw}, I_{qi}, I_{qo}, HR_i, HR_o \geq 0 \tag{3.23}$$

In order to minimize P_{excess} we choose V_{isw} such that the excess power in either the input side or the output side evaluates to zero.

$$\min(P_{excess}) = \min\left(P_{excess_{input}} + 0, 0 + P_{excess_{output}}\right) \tag{3.24}$$

$$\min(P_{excess}) = \min\left(P_{excess_{input}}, P_{excess_{output}}\right) \tag{3.25}$$

$$\min(P_{excess}) = \min\left(I_{qi}(V_{sr} - (V_{isw} + 2HR_i)), I_{qo}(V_{sr} - (A \cdot V_{isw} + 2HR_o))\right) \tag{3.26}$$

Assuming $HR_i \approx HR_o$ and $V_{isw} \leq A \cdot V_{isw}$ (requires $A \geq 1$):

$$\min(P_{excess}) = I_{qi}(V_{sr} - (V_{isw}|_{\min(P_{excess})} + 2HR_i)) \tag{3.27}$$

$$I_{qo}(V_{sr} - (A \cdot V_{isw}|_{\min(P_{excess})} + 2HR_o)) = 0 \tag{3.28}$$

$$V_{sr} = A \cdot V_{isw}|_{\min(P_{excess})} + 2HR_o \tag{3.29}$$

$$V_{isw}|_{\min(P_{excess})} = \frac{V_{sr} - 2HR_o}{A} \tag{3.30}$$

$$V_{osw}|_{\min(P_{excess})} = V_{sr} - 2HR_o \tag{3.31}$$

This makes sense; the minimum power excess due to the difference between the supply rails and voltage swing occurs when the voltage swing is at the output headroom limit. This occurs when $A \cdot V_{isw} = V_{osw}$ is at the maximum it possibly can be, which is $V_{sr} - 2HR_o$. At this point the excess power burned due to the voltage swing not being at the rail headroom limit is coming from the input portion of the circuit, which is driving a current across a voltage supply range greater than the input voltage swing plus the input voltage headroom. This remaining voltage is inaccessible by the input signal but still corresponds to dissipated power, a gross

inefficiency.

Pictorally, this is demonstrated in Figure 3-4.

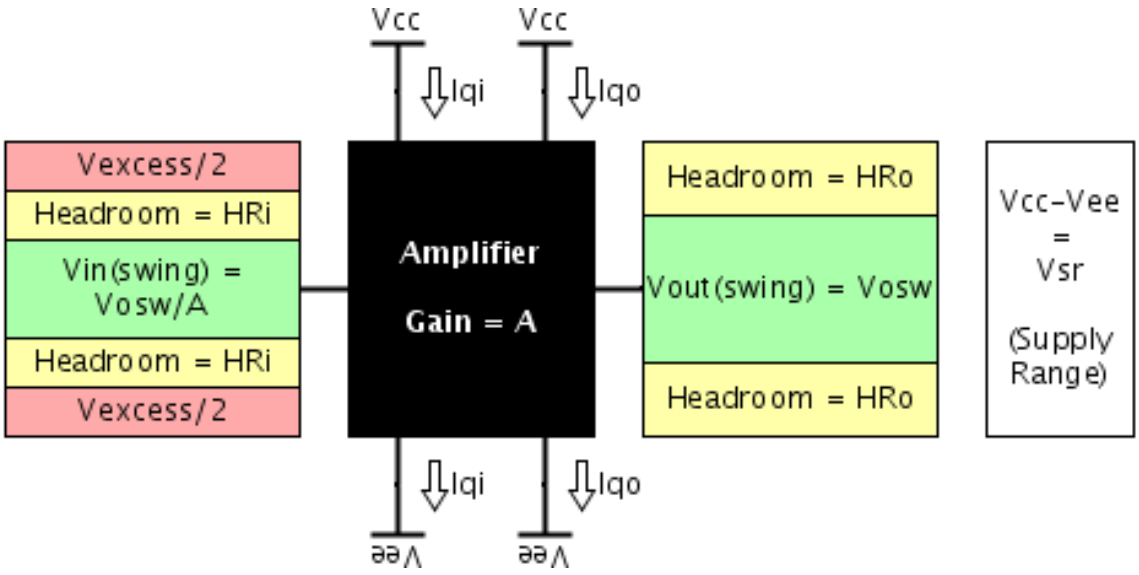

Figure 3-4: Power evaluation of amplifier with single set of voltage supplies and constrained signal relationship

Plugging in, we obtain a result for the minimum excess power:

$$\min(P_{excess}) = I_{qi}\left(V_{sr} - \left(\frac{V_{sr} - 2HR_o}{A} + 2HR_i\right)\right) \tag{3.32}$$

$$\min(P_{excess}) = I_{qi} \cdot V_{excess}|_{\min(P_{excess})} \tag{3.33}$$

$$V_{excess}|_{\min(P_{excess})} = V_{sr} - \left(\frac{V_{sr} - 2HR_o}{A} + 2HR_i\right) \tag{3.34}$$

This corresponds to the V_{excess} shown in Figure 3-4. To place this in the context of the application of the amplifier, let us assume that the supply range V_{sr} is 40 Volts, the headroom voltages at the input and output are negligible, and the quiescent current draw of the amplifier is evenly divided between the input and output halves ($I_{qi} = I_{qo} = 10$ mA). This excess voltage, and therefore the excess power, scales with the gain A of the amplifier as:

$$V_{excess}, P_{excess} \propto 1 - \frac{1}{A} \text{ for } A \geq 1 \tag{3.35}$$

At a gain A of 1, the excess voltage is null, and having matching supplies at the input and output allows the amplifier to potentially utilize a voltage swing which goes to the headroom limit voltage range of the amplifier. At higher gains, however, the drawback becomes immediately apparent. At a gain A of 2, the output voltage range is the full 40 V whereas in the input voltage range is solely 20 V, meaning $V_{excess} = 40V - 20V = 20V$. P_{excess} is 20 V $\cdot$ 10 mA $=$ 0.2 W. At $P_{supply} =$ 40 V $\cdot$ 20 mA = 0.8 W, this translates to a waste of 25% of the supply power. At a gain of 3, the excess voltage range is 26 V, with a power excess of 0.26 W (wasting 32.5% of the total power). And thus the power dissipated due to the excess voltage at the input increases with the amplifier gain, which is troublesome considering that these amplifiers are designed to be operating in gain configurations much greater than unity.

3.2.3 Disjoint Supplies

From the presentation of the power inefficiency resulting from using the same voltage rails to supply both the input and output components of the amplifier it becomes immediately apparent what the solution should be: split the voltage rails. Utilizing lower voltage supplies at the input allows the circuit user to lessen (or hopefully completely eliminate!) V_{excess} and P_{excess}, saving a large fraction of the total power burned from the power supply at DC.

With different supply ranges V_{sr1} And V_{sr2} at the input and output, respectively, the total power dissipated from the supply is less, while the criterion for minimum total power from the supply remains the same:

$$P_{supply} = I_{qi}V_{sr1} + I_{qo}V_{sr2} \tag{3.36}$$

$$P_{supply_{min}} = I_{qi} \cdot (V_{isw} + 2HR_i) + I_{qo} \cdot (V_{osw} + 2HR_o) \tag{3.37}$$

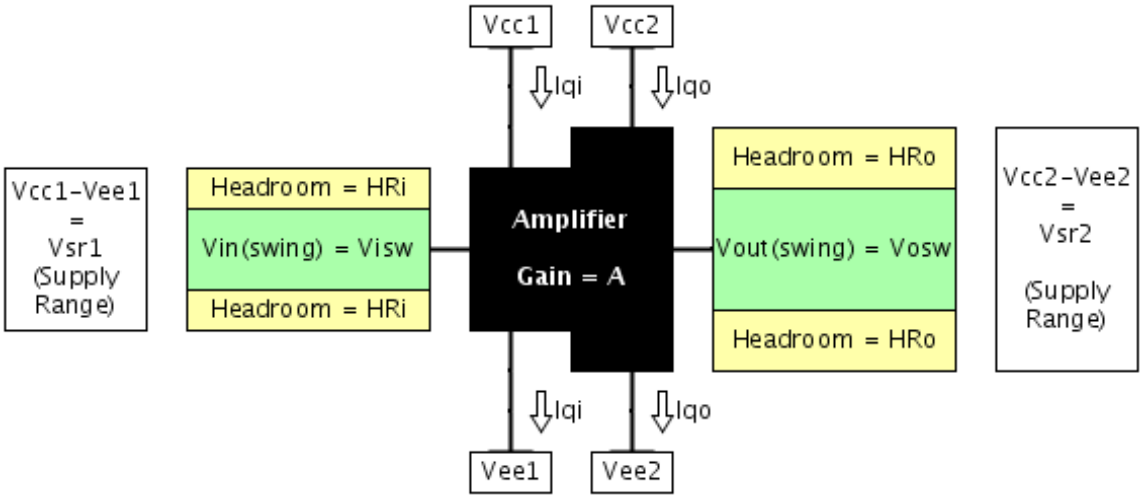

Figure 3-5: Power evaluation of amplifier with split voltage supplies

$$P_{supply_{min}} = I_{qi} \cdot (V_{isw} + 2HR_i) + I_{qo} \cdot (A \cdot V_{isw} + 2HR_o) \tag{3.38}$$

$$P_{excess} = P_{supply} - P_{supply_{min}} \tag{3.39}$$

$$P_{excess} = I_{qi}V_{sr1} + I_{qo}V_{sr2} - (I_{qi} \cdot (V_{isw} + 2HR_i) + I_{qo} \cdot (A \cdot V_{isw} + 2HR_o)) \tag{3.40}$$

$$P_{excess} = I_{qi}(V_{sr1} - (V_{isw} + 2HR_i)) + I_{qo}(V_{sr2} - (A \cdot V_{isw} + 2HR_o)) \tag{3.41}$$

Now the input and output voltage rails can be independently chosen to fully eliminate P_{excess}:

$$\min(P_{excess}) = 0 \text{ for } V_{sr1} = V_{isw} + 2HR_i, V_{sr2} = A \cdot V_{isw} + 2HR_o \tag{3.42}$$

$$P_{excess} = P_{supply} - P_{supply_{min}} = 0 \tag{3.43}$$

$$P_{supply} = P_{supply_{min}} \tag{3.44}$$

3.2.4 Issues

If utilizing different supply rails at the input and output of the amplifier does indeed support the notion that a major fraction of the total current draw can be conserved, why do no existing amplifiers have this option? An exhaustive search of

presently available commercial amplifiers turned up no results involving amplifiers which offer disjoint supply rails. Although still somewhat of a mystery, there are a few reasons at hand which address the inconvenience of this feature which probably explain its lack of existence.

Initially, most amplifier topologies are adversely affected by changing the voltage supply rails at the input and output. Depending on the internal topology, this is normally manifest in a input-referred offset which changes with the overall supply voltage difference $V_{sr2} - V_{sr1} = \Delta V_{sr}$. The reason for this is that if the input-referred offset is cancelled for a set of base currents (presumably under conditions of unified voltage supplies), changing the voltage supply of part of the amplifier will change these base currents according to the Early effect. Consider a device whose emitter is biased referenced to the input supply and whose collector is referenced to the output voltage rail (the output device of a current mirror or diamond, for example). Changing ΔV_{sr} corresponds to modulation of V_{CE} of the device, effectively changing the device's base current. This disrupts the base current cancellation scheme of the overall amplifier and thus for just about any scheme used, the input-referred offset V_{OS} will change when a difference between the supply rails is created. One of the attractive traits of the amplifier detailed in this thesis is that the signal path allows for modification of the supply rails at the input and output without affecting V_{OS}.

Next, many amplifiers do not benefit much from this change. For the numerical analysis performed in Section 4.3.2 stating the major power losses due to V_{excess}, the assumption was made that quiescent current is split evenly between the input and output halves. At DC, this is a strong likelihood given that the bias circuitry and all other supporting circuits are included in the input half of the amplifier (using the input rails). Of course the individual stages at the output will generally have higher quiescent current individually, so it is possible (and even likely) to have amplifier topologies where the quiescent current is more heavily weighted toward the output stage. Additionally, when the amplifier is slewing or driving a very low impedance load, resulting in a high current drive at the output, the portion

of the total current which is in the output scales up disproportionately because of the internal beta current gain stages. In cases where the output sees significantly more current than the input, the fraction of the total power which is lost due to the input voltage swing constriction will have a smaller fraction of power lost due to the input voltage range inefficiency but will still scale similarly.

$$\frac{\min(P_{excess})}{P_{supply}} = \frac{I_{qi}}{V_{sr}(I_{qi}+I_{qo})}\left(V_{sr} - \left(\frac{V_{sr}-2HR_o}{A} + 2HR_i\right)\right) \propto \frac{I_{qi}}{I_{qi}+I_{qo}} \quad (3.45)$$

Thus the ratio of power wasted corresponds to the fraction of the total current in the input portion of the amplifier. If this fraction is low, implementing disjoint supply rails is probably not worth it. In this amplifier the quiescent current split is in fact roughly half and half, so the power conservation achieved from splitting the rails is heavily justified.

In this evaluation we neglect power losses due to converters driving the DC voltages at the two supplies. Utilizing disjoint supplies suggests two sets of voltage rails instead of one, and thus an additional DC to DC power converter may be necessary on the board utilizing the amplifier in order to provide the second rail. Power losses due to inefficiencies from driving this second regulated voltage supply may lessen the total power saved.

Finally, there is the inconvenience of using multiple pins to require the circuit user to specify the second set of rails, including the inconvenience of utilizing two different power supplies. Obviously there is the option of attaching the same power supply to both sets of rails if the chip user wishes to, but the inconvenience of more pins could require a larger package, larger chip size, and more area on the integrated circuit dedicated to ESD Protection of the individual supply rails.

3.2.5 Making the split

Where does the circuit designer split the voltage rails to optimally implement disjoint supply rails? We demonstrated that the fraction of power that can be con-

served through splitting the power supplies corresponds to the fraction of current in the input versus the total current. Thus it is preferable to split the amplifier as close to the output as possible. Refer back to Figure 2-26 on Page 77 for the amplifier structure.

However, the high-Z node drives the output voltage and must have the same voltage supply range in order to do its job, thus the initial point where one can split the voltage supply rails must be before the high-Z node. Note that it would be pointless to make the split anywhere in the output diamond buffer because each stage of the diamond has nodes which are referenced to the output by a certain number of V_{BE}; one stage removed from the output is a single V_{BE} up or down from the output, and so forth. Such is the functionality of a diamond.

Next there is the current mirror driver circuit which creates the high-Z node voltage and the current bias for the output diamond. In the current mirror the output collector voltage is free to move to the opposite supply rail, however it is not possible to split the voltage supplies in the middle of a current mirror because this detrimentally affects the current mirror's biasing and destroys its constant current gain. This can be demonstrated in a straightforward derivation. For this example we will use a simple current mirror rather than a cascode current mirror; the V_{BE} relationship which is necessary to mirror current is the same, and the shortcoming is the same.

$$V_{ee1} + V_{BE1} = V_{ee2} + V_{BE2} \tag{3.46}$$

$$\frac{I_{out}}{I_{in}} = \frac{I_{S2}}{I_{S1}} e^{\frac{V_{ee1} - V_{ee2}}{V_T}} = \frac{I_{S2}}{I_{S1}} e^{\frac{\Delta V_{ee}}{V_T}} \tag{3.47}$$

We verify this formula by comparing it to standard operating conditions where $\Delta V_{ee} = 0$ therefore the ratio of currents is simply the ratio of I_S or device areas. However, now that the difference in emitter voltages of the two devices is nonzero, the dynamics of the current mirror change entirely. Now there is an exponential relationship between the output and input currents of the mirror, destroying biasing schemes and exponentially increasing the current (and thus power dissipated)

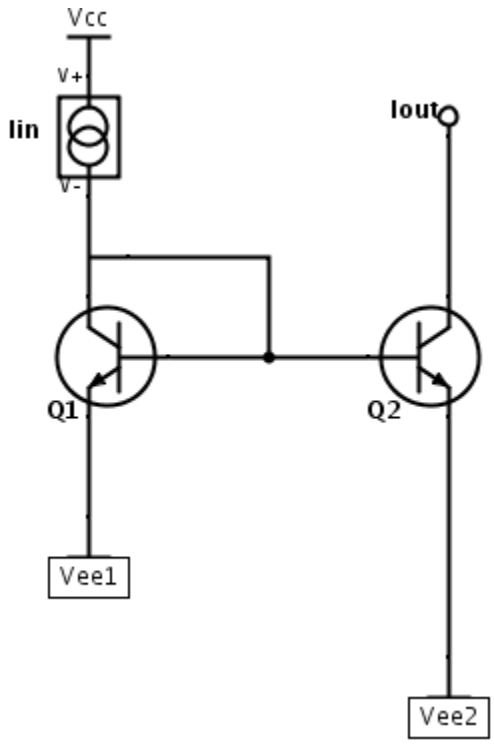

Figure 3-6: Simple current mirror with disjoint supplies

in subsequent stages of the amplifier.

Any location in the amplifier between current mirrors (at floating collector nodes) could possibly be a viable option for splitting the supply rails of the amplifier. Just as before, one needs to be careful of base width modulation on the output device of the mirror whose collector crosses over from one supply rail to another. This device will have a base current which is smaller than the base current formerly observed because of its increased collector-emitter voltage and therefore beta.

To demonstrate an input-referred offset which is created due to splitting the voltage supply rails, consider the following simple amplifier topology, initially with a consistent set of voltage rails throughout the part and with net base current cancellation, shown in Figure 3-7.

The buffers in the H-Bridge are simple diamond buffers with two signal path outputs apiece. For the sake of simplicity we utilize ideal current mirrors which do not contribute an offset in currents due to base current errors between their

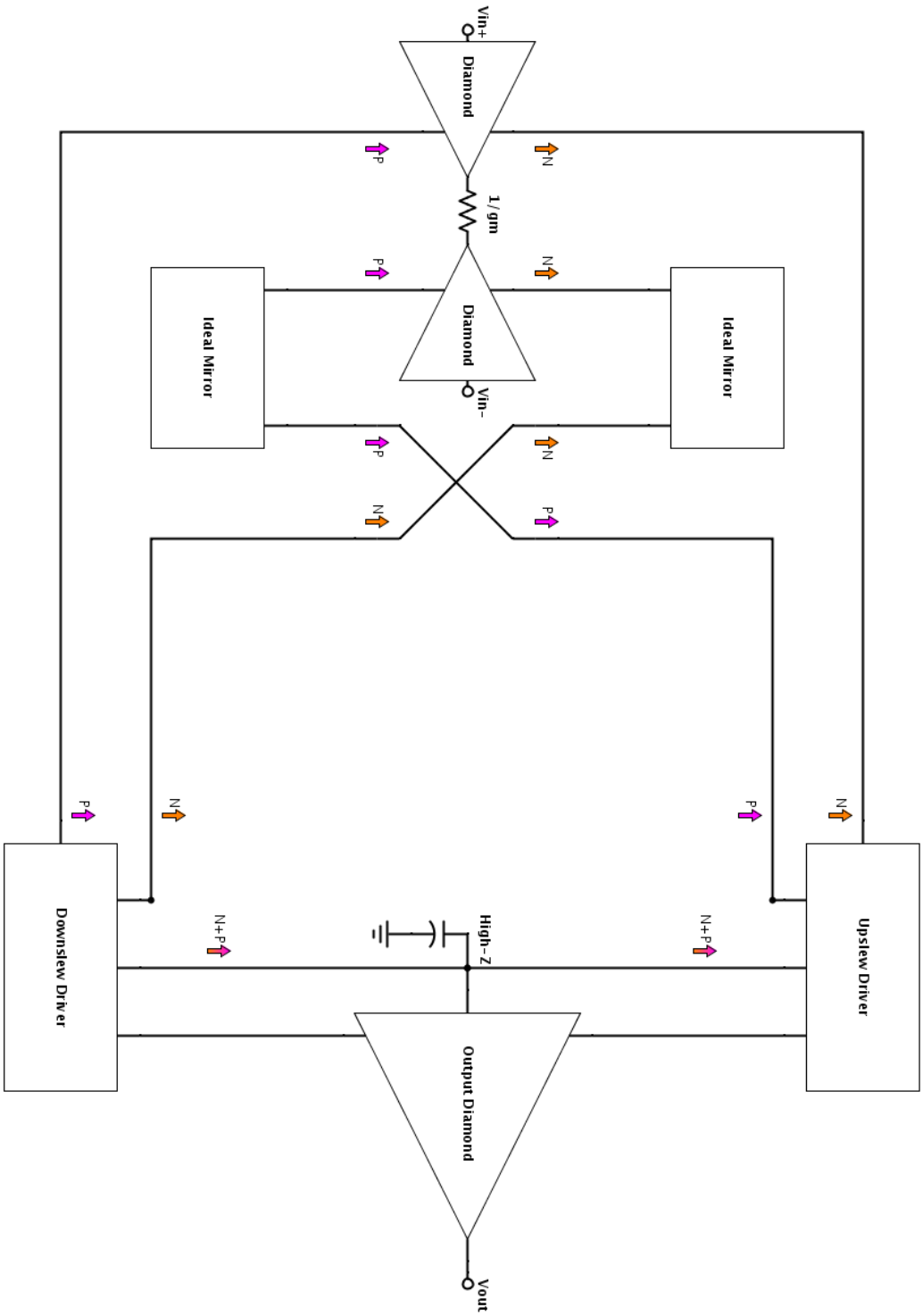

Figure 3-7: Simple topology with base current errors cancelled at consistent supply rails

input and output current paths, such as a Wilson current mirror or some other internally compensated current mirror. This topology takes the incremental base current error from one side of the H-Bridge and the base current error from the other side of the H-Bridge, pairing them together to achieve a net $N+P$ set of base current errors at the high-Z node. Likewise, an identical mechanic occurs on the other side of the amplifier resulting in the same $N+P$ set of base current errors on the other side of the amplifier. At least, this is true when there is no difference between the supply rails at the input and output ($V_{ee1} = V_{ee2}$).

When the input and output portions of the amplifier see different supply rails, the situation changes. The left side of the H-Bridge sees a current mirror input to the output set of voltage rails, thus the collectors at these nodes are $V_{cc2} - V_{BE}$ and $V_{ee2} + V_{BE}$ at the top and bottom of the diamond, respectively. However, the right side of the H-Bridge looks into a current mirror referenced to the input set of voltage rails, thus it has collector nodes which are a certain number of V_{BE} from V_{cc1} and V_{ee1}. For the sake of simplicity let us assume that the ideal current mirrors have a single V_{BE} of headroom. Thus when the voltage supply rails are split, the right side of the H-Bridge sees collector voltages of $V_{cc1} - V_{BE}$ and $V_{ee1} + V_{BE}$ at the top and bottom, respectively. Just as cited many times before, base width modulation of transistors (Equation 2.56) will modify their according βs and thus their effective base currents. We thus assign differing base current names to each of the four outputs of the H-Bridge and depict this in Figure 3-8, featuring disjoint supply rail-introduced base current errors of N_1, N_2, P_1, and P_2.

Consider the ideal situation under which the base current analysis is performed. Let the input branches each have a bias current of I_{bias}, be sized identically, and let the input be DC grounded.:

$$N_1 = \frac{I_{bias}}{\beta_{NPN}} = \frac{I_{bias}}{\beta_{0_{NPN}}\left(1 + \frac{Vcc1 - V_{BE}}{V_{A_{NPN}}}\right)} \tag{3.48}$$

$$N_2 = \frac{I_{bias}}{\beta_{NPN}} = \frac{I_{bias}}{\beta_{0_{NPN}}\left(1 + \frac{Vcc2 - V_{BE}}{V_{A_{NPN}}}\right)} \tag{3.49}$$

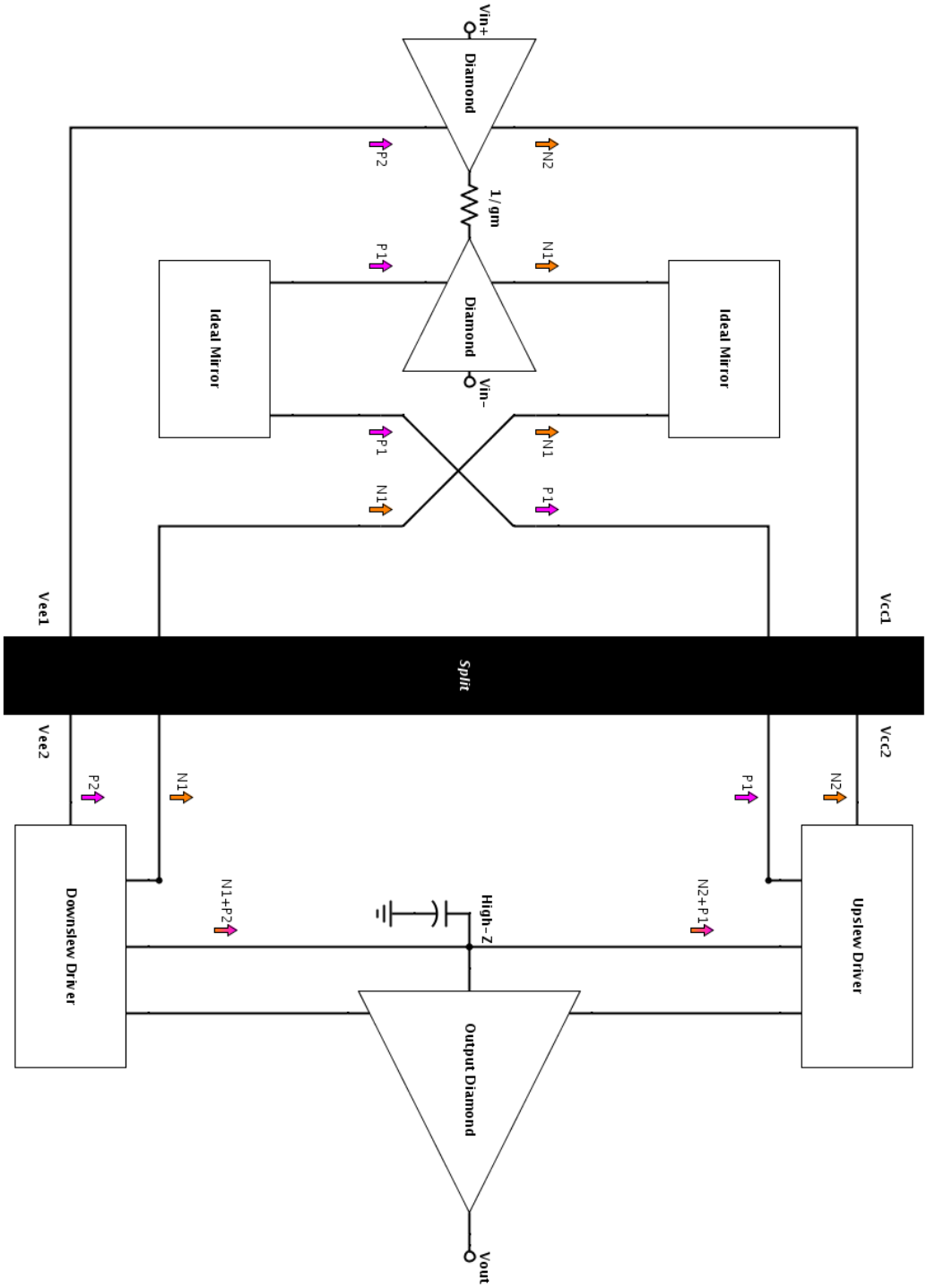

Figure 3-8: Simple topology with base current errors cancellation disrupted by disjoint supply rails

$$V_{cc1} \neq V_{cc2} \rightarrow N_1 \neq N_2 \tag{3.50}$$

Similarly at the bottom set of rails:

$$P_1 = \frac{I_{bias}}{\beta_{PNP}} = \frac{I_{bias}}{\beta_{0_{PNP}}\left(1 + \frac{Vee1+V_{BE}}{V_{A_{PNP}}}\right)} \tag{3.51}$$

$$P_2 = \frac{I_{bias}}{\beta_{PNP}} = \frac{I_{bias}}{\beta_{0_{PNP}}\left(1 + \frac{Vee2+V_{BE}}{V_{A_{PNP}}}\right)} \tag{3.52}$$

$$V_{ee1} \neq V_{ee2} \rightarrow P_1 \neq P_2 \tag{3.53}$$

When the base currents at opposing sides of the input stage no longer match each other they cannot be worked against each other to achieve idealized base current cancellation. As one increases the difference in supply voltages, the difference in base currents goes up, increasing V_{OS} accordingly. This is a complication that applies to most amplifier topologies.

3.2.6 Disjoint Supplies in this Topology

I claim that our topology effectively deals with this design quandary, permitting one to split the input and output power supplies without impacting the DC error of the amplifier. To perform a direct comparison just as in the case of the aforementioned topology which breaks under the conditions of split supply rails, we take the initial base current analysis of the signal path from Figure 2-25 and apply a split in the supply rails. Just is in the prior case, there is now a difference in the base current errors coming out of the input H-Bridge. However, the way in which these different errors propagate throughout the signal path of the amplifier differs from before:

N_1, N_2, P_1, P_2 are all defined the same as before. As demonstrated in Figure 3-9, this amplifier is our final design. It has the input stage with matched DC and signal dependent output paths for each diamond in the H-Bridge. Interestingly, just as in the unified supply rail case where the DC and signal paths (within each internal diamond) work against each other to cancel DC errors, in this disjoint rails

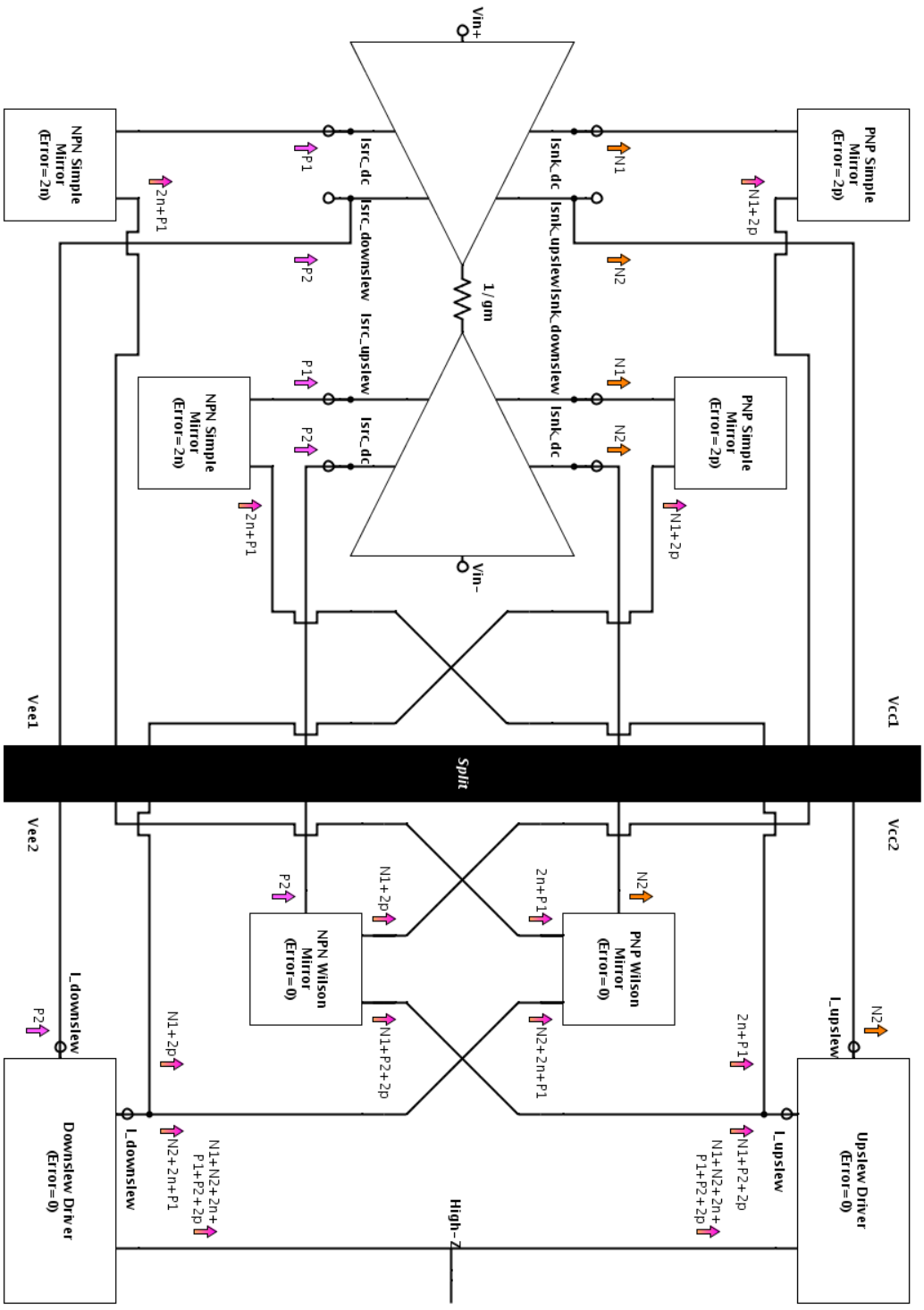

Figure 3-9: Amplifier topology which is resilient to disjointed power supplies

scheme the DC and signal paths in the overall H-Bridge work together to produce equal total base current error with an error contribution from each set of rails. In the left diamond the DC path connects to the input set of rails while the signal path feeds into the output portion of the amplifier. Conversely, in the right side of the H-Bridge the signal path connects to the input half of the amplifier while the DC path connects to the output.

For each diamond, whether it be the NPN side or the PNP side:

$$I_{dc} + I_{signal} = 2I_{bias} - \epsilon_1 - \epsilon_2 = 2I_{bias} - \epsilon \tag{3.54}$$

Just as in the case of the simple H-Bridge with solely one output for each diamond in the H-Bridge, if we take this aggregate error ϵ (formerly $N + P$, now $N_1 + N_2 + P_1 + P_2$) and send the contribution from each side of the H-Bridge (each diamond) to opposite sides of the amplifier and therefore opposite sides of the High-Z node, effectively achieving base current cancellation.

The astute reader may have noticed that this analysis completely omitted the impact of separating the input and output supply rails on the internal errors of the current mirrors. Errors arising from base width modulation applies to current mirrors whose output devices are exposed to the "split." Here the four simple current mirrors are the current mirrors whose output devices are looking into the split (along with the H-Bridge), and thus the effective error of each simple current mirror has changed. The V_{CB} of the output device for each simple mirror is $V_{cc} - V_{ee} - 3V_{BE}$ because the collector is $2V_{BE}$ from the high supply rail while the base is a single V_{BE} from the low supply rail.

Before:

$$2n = \frac{I_{bias}}{\beta_{0_{NPN}}} + \frac{I_{bias}}{\beta_{0_{NPN}}\left(1 + \frac{V_{cc} - V_{ee} - 3V_{BE}}{V_{A_{NPN}}}\right)} \tag{3.55}$$

$$2p = \frac{I_{bias}}{\beta_{0_{PNP}}} + \frac{I_{bias}}{\beta_{0_{PNP}}\left(1 + \frac{V_{cc} - V_{ee} - 3V_{BE}}{V_{A_{PNP}}}\right)} \tag{3.56}$$

Now:

$$2n = \frac{I_{bias}}{\beta_{0_{NPN}}} + \frac{I_{bias}}{\beta_{0_{NPN}}\left(1 + \frac{V_{cc2} - V_{ee1} - 3V_{BE}}{V_{A_{NPN}}}\right)} \tag{3.57}$$

$$2p = \frac{I_{bias}}{\beta_{0_{PNP}}} + \frac{I_{bias}}{\beta_{0_{PNP}}\left(1 + \frac{V_{cc1} - V_{ee2} - 3V_{BE}}{V_{A_{PNP}}}\right)} \tag{3.58}$$

But this change is actually not important. Regardless of the value of $2n$ and $2p$, each simple current mirror has a counterpart of the same type whose errors end up on the other side of the High-Z node. As long as both of the NPN and PNP current mirrors are modified identically, the base current error contributions from each are trivialized.

3.2.7 Addendum

One cannot emphasize enough the power significance of being able to split the supply rails. High voltage, high current amplifiers are very often meant to be utilized in a high gain configuration, where the quiescent power dissipated across the inaccessible voltage range at the input is a major fraction of the amplifier's total power draw. The downside of this amplifier implementation which permits for supply rail splitting without an impact on DC errors is that this topological structure does indeed have more current mirror stages than a conventional amplifier topology. However, the additional current draw from the additional stages is a marginally important contributor to total power dissipation compared to the power saved from idealized supply rail splitting, and this will be quantifiably evaluated in the conclusion. Note that in applications where the amplifier DC input offset is not an important specification it may be worth it to apply disjoint supply rails to a much simpler topology, neglecting the effect of DC errors in favor of power conservation. Nonetheless, I was unable to find any commercially available amplifiers which utilize this technique.

3.3 Current Limiting

As a fundamental effort in this project we attempt to design a robust current limiting solution. As a mechanism, this is the ability of an amplifier to set a maximum current drive for itself. When the input, load, and feedback conditions require an output signal that would exceed this current limit, some other mode of operation kicks in. When this current limit is configured to a fixed value at or near the maximum current drive of the part, this feature is often referred to as short circuit protection. Short circuit protection refers to the case where the output is driving the maximum current possible. When the amplifier output is shorted to rail, it is equivalent to seeing an infinitely low impedance. The amplifier under normal operation will be attempting to drive the output voltage to a certain value, supplying whatever current is necessary to accomplish this. Through Ohm's law we know that current through and impedance of a load are inversely proportional for a given output voltage. Thus as the impedance of the load becomes infinitesimally small, the current required to create a given voltage value blows up. The amplifier will drive current at its peak drive capacity, here set by whatever internal limiting mechanism the amplifier utilizes.

The design of an effective current limiting solution can be as complex as the design of the signal path itself, and the designer must take care to not interfere with the normal performance of the amplifier. The current limiting circuit must perform a series of functions in order to be effective. Initially, it must be able to sense the ouput current. There are several methods of implementing this, which will be discussed later. Next, the current limiting circuit must switch; it must perform a comparison which determines whether or not the feedback loop must kick in. Finally, the current limiting circuit must apply feedback in such a way that either thresholds the current output of the amplifier or turns it off, based on implementation.

The nature of a current limiting system is that of a feedback loop, and thus one encounters all the issues and design complications associated with a system

utilizing feedback. Stability becomes an issue in order to achieve a loop which does not produce a ringing or ripple while in operation. The system must be robust enough to function properly for a wide range of modes of operation where the variables involved are input signal and load. The load can be a combination of resistive and capacitive elements, resulting in real and complex impedances.

Another objective of this feature is to come up with a fully analog implementation of a current limiting system. This involves dealing with the limitations imposed by an analog system; we do not have digital switches at our disposal to arbitrarily turn portions of the amplifier on and off; any switching or implementation of multiple modes of performance must be implemented strictly using analog structures. This section commences with a brief discussion and analysis of existing implementations and outlines the unique architecture used in this thesis project.

3.3.1 Existing Parts

There are numerous commercially available amplifiers which possess a rudimentary implementation of short-circuit protection through V_{BE} turn-on[14], a simple implementation which turns on a transistor in order to deprive the output class AB transistors of base current, shutting them off. This can be seen in amplifiers such as the ubiquitous *LM741* monolithic amplifier[15]. However, this approach is overly simple and suffers from temperature dependence limitations (in both the turn-on condition as well as the effectiveness of the current limiting). As such, we will attempt to explore a more robust approach.

Linear Technology, Inc. commercially produces one product, the LT1970, whose amplifier functionality is geared toward a robust, highly configurable current limiting mechanism[16]. Figure 3-10 demonstrates this amplifier, showing the pins which permit configurability and limitations of the current limit.

Here, the sense resistor R_{CS} is external to the amplifier and must have a specified value of 1 Ω, placed between pins $SENSE^+$ and $SENSE^-$ The voltage across this resistor is compared against a manual input voltage to pins VC_{SRC} and VC_{SNK}, for

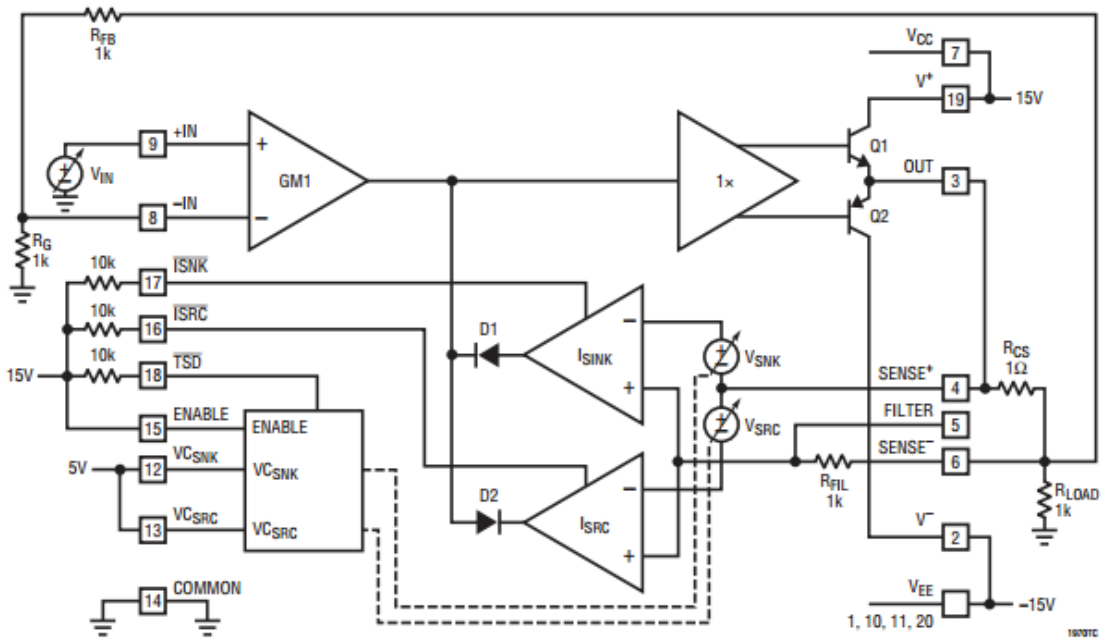

Figure 3-10: LT1970 block diagram featuring current limiting mechanism

the cases of source and sink output current, respectively. This difference is amplified in a set of feedback differential amplifiers which then act on the High-Z node of the amplifier, effectively achieving negative feedback. Finally there is a set of two pins I_{SRC} and I_{SNK}, digital flags which indicate whether or not current limiting is active in each direction.

One facet of the LT1970 amplifier which permits it to perform highly accurate, robust current limiting is that it has a very low slew rate. Specified as 1.6 V/μs on the datasheet, this amplifier must have a differential pair input stage, whose fixed tail current limit sets the low slew rate due to low current through the High-Z node. Thus the feedback path has less forward drive current to fight when current limiting is in effect, compared to the high slew rate case of a diamond or H-Bridge input stage. LT1970 boasts a 2% current limit accuracy at a current drive capacity of half an ampere, and this is strictly possible because the amplifier is so slow to begin with.

The ADA4870, *Analog Devices Inc.*'s high current drive part which has been mentioned numerous times in this thesis report, has current limiting functionality.

The current at the output is sensed, compared against a fixed current limit, and if the output current exceeds this predefined current limit the amplifier is simply shut off by turning off the bias, in a mechanism analogous to enabling the shutdown pin. This current limiting implementation is not configurable, and the behavior which entirely turns off the amplifier is less desirable than a feature which keeps the amplifier on but constrains the output within the current drive limitations of the part. A large inspiration of this part of the design project is to build on the achievements of the ADA4870's current limiting mechanism, adopting a similar methods for sensing the output current and utilizing a similar overall system structure for the current limit negative feedback loop.

3.3.2 Sensing

Sensing of the output current can only be accomplished in a few different ways. The simplest and most common approach is to utilize a sense resistor. We already mentioned that using the emitter degeneration resistors of devices at the output of the amplifier was not an option beause it would limit the headroom of the device, as well as increase the effective output impedance. The next option is to use an external sense resistor which would require two additional pins on the part. This was not practical either because we did not wish to add unnecessary pins; even more pins will be needed to configure the current limit of the amplifier.

The third place where the sense resistor can be placed is at the collector of the output devices. This takes advantage of our large headroom at the output ($2V_{BE} + V_{CE_{sat}}$) to ensure that we have enough headroom for this resistor to accrue a significant enough potential drop. While there is potential in this approach, it is actually quite complicated. Instead of turning on a device using V_{BE} turn-on we would need to buffer the voltage across the device to determine the current across it then act on this current. The buffer requires additional current biases and has transient limitations, both detrimental to our sensing mechanism.

We decide to take a different approach entirely. The output class AB stage uti-

lizes a set of 80 unit NPN and PNP transistors. Given the base-emitter voltage drops across these devices, we place additional single unit devices in parallel with the output stage devices, effectively sampling $1/80$ of the current across the output stage. One could think of the output stage as being eighty stages in parallel (eighty one with the sense stage). We take one of these stages as the current sampling stage, thus taking a fixed fraction of the total output current.

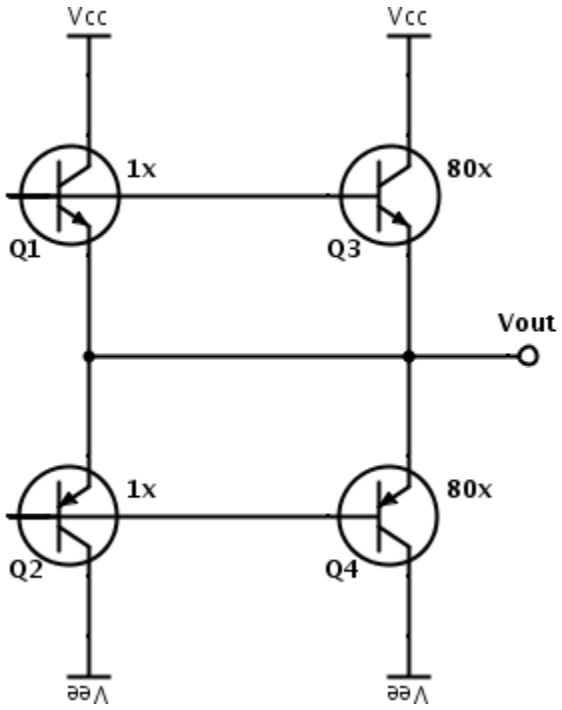

Figure 3-11: Current sense stage and output stage

Figure 3-11 demonstrates this implementation. For the NPN devices sourcing current, *Q1* and *Q3*:

$$V_{BE1} = V_{BE3} \tag{3.59}$$

$$V_T \ln\left(\frac{I_{C1}}{I_{S1}}\right) = V_T \ln\left(\frac{I_{C3}}{I_{S3}}\right) \tag{3.60}$$

$$\frac{I_{sense}}{I_{out}} = \frac{I_{C1}}{I_{C3}} = \frac{I_{S1}}{I_{S3}} = \frac{I_{S0_{NPN}} A_{E1}}{I_{S0_{NPN}} A_{E3}} = \frac{1}{80} \tag{3.61}$$

The same applies to devices sinking current, *Q2* and *Q4*:

In this implementation our sense stage, the class AB stage with single unit devices *Q1* and *Q2* thus senses the output current and scales it down by a factor of

80, a fact which will come in useful later. We now have a reliable and consistent method of performing current sensing on the output stage. Note that there is no temperature dependence involved in this current ratio; it is solely dependent on the ratio of device areas.

3.3.3 Current Limit Threshold Switching

Practically there are only a few means of achieving "switching" in the analog domain. Here what we are switching is a current path–the feedback loop–which we intend to dynamically turn on and off. To switch a current path one could implement the current as the tail current input into a differential pair, modulating the voltage applied to each side of the differential pair to split the input current between the two paths. This works, but in our case we need to be able to compare the sensed current from the output against a fixed reference current corresponding to a particular current limit.

Our switch implementation capitalizes on the monodirectionality of the output devices in a class AB stage to split a current going into this structure. Figure 3-12 demonstrates this implementation in the direction of sourced current drive:

Once again we have a current sense stage (devices *Q3* and *Q4*) acting upon the class AB output stage (devices *Q5* and *Q6*). I_{sense} from the former section is now fed into a current mirror. We use this current mirror because there is not enough headroom between the collector of *Q3* and the supply rail to fit our class AB current switch. Additionally, the voltage at the collector of *Q3* should not be able to change very much, otherwise it will affect the ratio of currents between the sense stage and the output stage in accordance with base width modulation:

$$\frac{I_{sense}}{I_{out}} = \frac{I_{C3}}{I_{C5}} = \frac{I_{S3}}{I_{S5}} = \frac{I_{S0_{NPN}} A_{E3} \left(1 + \frac{V_{CE(Q3)}}{V_{A_{NPN}}}\right)}{I_{S0_{NPN}} A_{E5} \left(1 + \frac{V_{CE(Q5)}}{V_{A_{PNP}}}\right)} \tag{3.62}$$

$$\frac{I_{sense}}{I_{out}} = \frac{1}{80} \left(\frac{1 + \frac{V_{C3} - V_{out}}{V_{A_{NPN}}}}{1 + \frac{V_{cc} - V_{out}}{V_{A_{NPN}}}} \right) \tag{3.63}$$

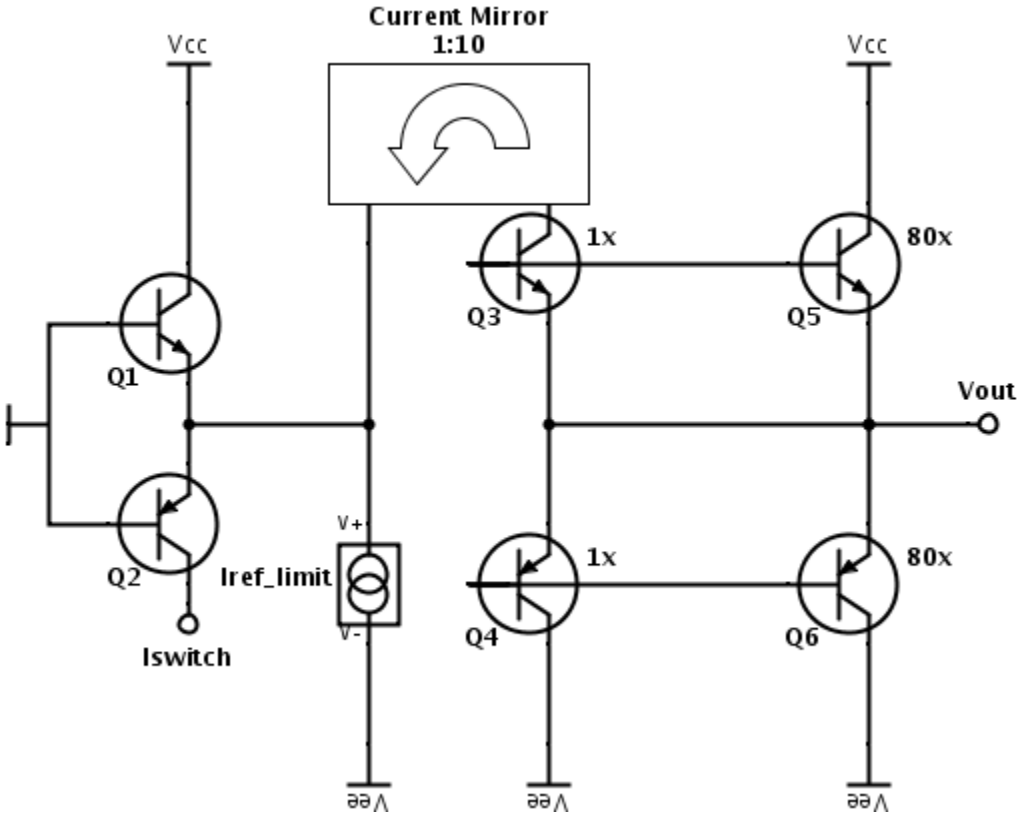

Figure 3-12: Depiction of current limiting sensing and switching

Seeing this expression, as long as we can keep V_{C3} as static as possible the ratio of currents between the output and sense stages will at least be constant.

Another opportunity which emerges from using a current mirror acting on the sensing current is the ability to scale down the current once again. Utilizing a 1:10 simple current mirror, the current coming out of this mirror is now $1/80 \cdot 1/10 = 1/800$ of the output current. And now we answer why we wish to scale down the sensed current so much. This current is compared against a reference current I_{ref_limit} corresponding to the current limit switch condition, and this is a quiescent current which will cost DC current draw and therefore quiescent power–all the time, even when current limiting is not active. We want this current to be as small as possible solely for power considerations. Dividing the output current down by a factor of eight hundred, an output current of one Ampere therefore has a reference current of 1.25 milliamperes. This is still a fairly large fraction of the overall current

of the amplifier, but it is at least reasonable.

We can make this current limit configurable by simply allowing the circuit user to set the emitter degeneration resistor of a device in whatever circuits are being used to create this fixed reference current. This could be a resistor in the diamond based current distribution or a resistor in the current mirror whose output device is the device acting as the current source. There are numerous possibilities which permit configurability of this current limit value, which is a great asset. Additionally it will only require one pin: the user will place the resistor between the single exposed pin and the rail to set the value.

Thus the current coming out of the current mirror feeds into the output of the class AB current switch consisting of devices *Q1* and *Q2*. These devices have their base tied to some reference voltage elsewhere in the output stage of the amplifier not pictured here. When the current coming out of the current mirror that corresponds to $1/800$ of the output current is less than the reference current, all of the current in the switch is coming out of the collector of device *Q1* and not from device *Q2*: $I_{switch} = 0$. When the current out of the mirror exceeds I_{ref_limit}, the amount of current from the mirror greater than the reference current trickles out of the collector of device *Q2*, turning on the switch current I_{switch}. As a piecewise function:

$$I_{1\_switch} = \begin{cases} 0 & \text{when } \frac{I_{out}}{800} \leq I_{ref\_limit} \\ \frac{I_{out}}{800} - I_{ref\_limit} & \text{when } \frac{I_{out}}{800} > I_{ref\_limit} \end{cases} \tag{3.64}$$

This is an idealized model of the behavior of our switching mechanism in our current limiting feedback loop.

3.3.4 Feedback

Now that we have a switch current, we analyze how to adequately use this current to achieve negative feedback completing the current limiting loop. We place our sensing and switching circuits in the context of our $2V_{BE}$ diamond buffer output

stage, shown in Figure 3-13.

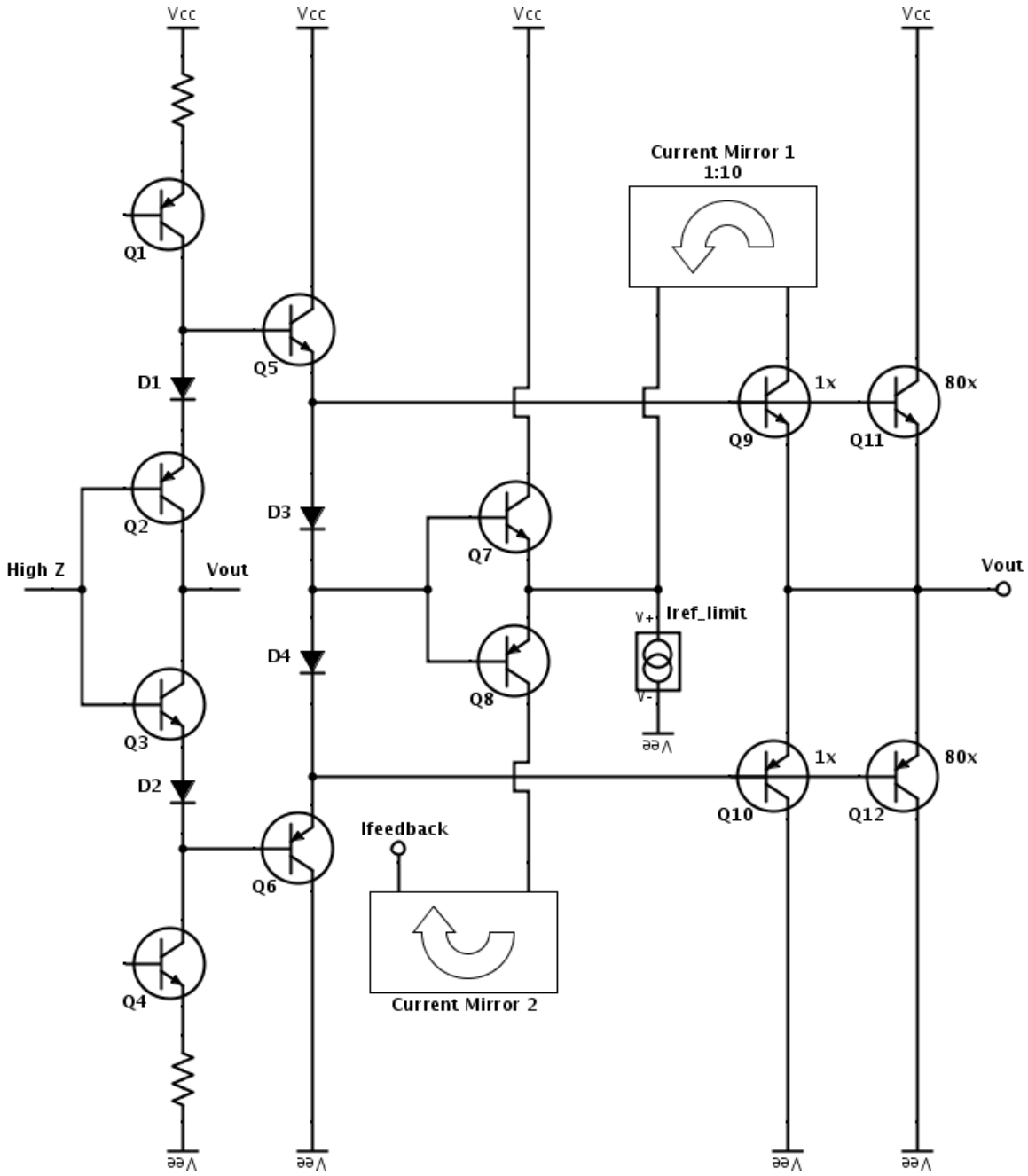

Figure 3-13: Current limiting feedback in our output diamond buffer

The current coming out the switch is now fed into a second current mirror to produce the feedback current $I_{feedback}$. This current mirror is necessary for two purposes: the feedback current must be a sink current because of the limited nodes available at which to apply feedback, and the additional gain stage could prove

useful, permitting us to tune our feedback loop. Now that we can see the entire output stage with part of the predriver mirrors, we can analyze the potential nodes where feedback can be applied.

- **Base of output device *Q11*** - applying a sink current to the base of the output device will steal base current from the output device, applying negative feedback in a fashion identical to the method utilized in the demonstrated V_{BE} turn-on implementation. This feedback is applied at a point which sees a current of $\frac{I_{out}}{\beta}$ or alternatively $I_{drive} \cdot \beta$ where I_{drive} is the collector current out of *Q1*. This is a comparatively high current, and thus in order to fight this large current when the amplifier is slewing, *Current Mirror 2* must have a reasonably high current gain.

- **Output of current driver** - applying a sink current to the output of the current driver steals current from the current drive of the diamond buffer as it enters the buffer, preventing current from reaching the output stage, slowing down the diamond buffer's ability to function. This point in the diamond sees I_{drive} or $\frac{I_{out}}{\beta^2}$. Thus this current is much lower than the current at the output, and one will achieve a much stronger feedback response for a given feedback current $I_{feedback}$.

- **Emitter degeneration resistor of current driver** - applying a sink current directly at the emitter degeneration resistor of *Q1* is similar to stealing the current coming out of the current source driver; the difference here is that we are now treating the resistor as the drive current source. The currents at this point are identical to the former case where the quiescent current is I_{drive} or $\frac{I_{out}}{\beta^2}$ referenced from the output. The substantial difference here is that this node is a low impedance point–the emitter of *Q1* as opposed to its high impedance collector–thus for a given applied current $I_{feedback}$ the voltage at the node will swing less as per $\Delta V = \Delta I_{feedback} \cdot Z_{in}$, resulting in a more stable feedback response.

- **High-Z node** - applying a sink current to the high impedance node will pull down the voltage at this point of the circuit, driving the output diamond buffer in the opposite direction. This achieves negative feedback, and recall that this is the approach utilized by the *LT1970*. One problem associated with this approach is the introduction of additional parasitics (especially capacitances) to the high-Z node by connecting additional devices to the high-Z node.

The second and third approaches were the most promising because of the lower current required for an effective response; however, there are numerous problems associated with this approach, which will be addressed.

3.3.5 Initial Implementation Problems

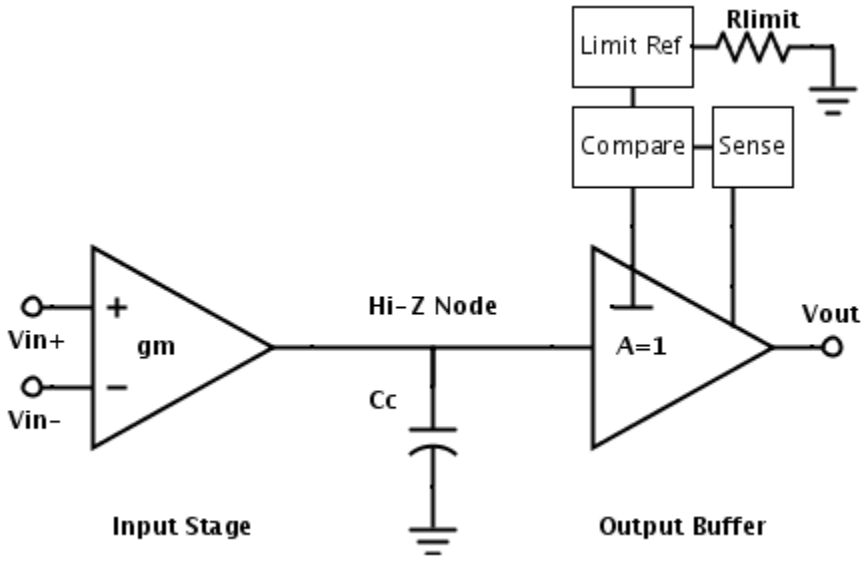

Figure 3-14: Initial current limiting implementation

The initial proposed solution utilizes a feedback loop which acts on the output stage of the amplifier, providing transient negative feedback to inhibit the current drive of the amplifier while it is slewing. The fundamental problems associated with this approach stem from the interaction between this proposed solution and

the inherent structure of our amplifier. The feedback current being applied scales with the current at the output, whereas the forward current drive scales with the voltage applied at the input of the amplifier. When current limiting kicks in, the current at the output will peter off, but changes to the input are simply not regulated. One could continue to drive the input, and the current coming out of the input stage H-Bridge which becomes current drive current I_{drive} at the output diamond will be very large, whereas the current limiting feedback current $I_{feedback}$ will not be able to keep up. Fighting I_{drive} with $I_{feedback}$ requires a very high current gain feedback loop which is very awkward to tune because an overshoot in gain will result in instability of the amplifier, and setting the gain for a single current limit and load will not necessary work for other configurable scenarios. It is thus very hard to design a one size fits all robust solution in this context.

The drive current is very high when the amplifier is slewing because it is referred to the current coming out of the input stage. This current is high because of the diamond-based input stage, our H-Bridge. We made this design decision consciously, acknowledging that the high current would allow us to have a very high slew rate. If we had used a differential pair input stage the current drive at the diamond buffer would be referenced to some scalar multiple of the tail current, which would be much easier to perform current limiting on because of the lower forward current drive, but we would have a much lower slew rate and consequentially a lower bandwidth. This is the approach that the LT1970 takes, emphasizing current limiting over slew and bandwidth. We could also use fixed current drive sources to drive the output diamond buffer, but this would limit our slew rate as well because it would retain the quiescent current properties of the existing architecture but be unable to provide more current when the amplifier is slewing. To match the slew current drive of the part would large DC current drivers and is not practical because it would overwhelm the quiescent power consumption of our part.

We initially explored utilizing current feedback applied solely to the output stage of the amplifier because this would offer the best transient effects given that the forward loop and feedback loops would have few stages, resulting in lower

time delays for signal to pass through the loop. This would ideally give us a quick and responsive feedback response to perform current limiting. Unfortunately, utilizing a feedback loop which fights the current drive of the output diamond buffer does not work in this topology for the reasons outlined above relating to stability, configurability, and overall robustness of the feedback loop.

3.3.6 Final Implementation

The final current limiting implementation is one of the most unique achievements of this design project because it takes very digital concepts such as turning off individual portions of the amplifier and turning on alternate stages but implements them in an analog fashion. Rather than simply fight the current drive of the amplifier alone, we elect to take a much more robust approach. When the current limit is reached, we turn off the input stage by debiasing the current bias inputs to the input stage and we reverse bias the entire input stage. We then turn on an alternate input stage, a compound differential pair. This input stage is now current limited by the tail current of the stage, allowing us to easily fight this fixed output current drive, keeping the output signal of the amplifier within its current limit.

Thus the amplifier has two modes of operation: the dominant, default mode in which the H-Bridge is driving the amplifier at high slew rate and bandwidth, and a degenerate mode in which the differential pair is active, driving the amplifier but at lower slew rate. When the amplifier turns on it defaults to the H-Bridge input stage and remains in this state until the output current triggers a latch. The latch suppresses the H-Bridge and activates the compound differential pair, keeping it in this mode until the latch is reset. The two-faced nature of this amplifier thus makes it a truly bipolar bipolar amplifier.

This approach retains the essence of the aforementioned implementation in that sensing occurs the same as before with a stage that samples a fraction of the output current of the amplifier. This current is mirrored and fed into a class AB current switch. When the switch overcomes a certain threshold, the current out of it makes

two paths. It both acts as a feedback current just as before but now also is sent to an analog switch circuit. When this switch circuit sees a current it turns on a latch in another discrete analog block. This latch turns on the differential pair input stage and suppresses the H-Bridge input stage. Turning the input stage on and off is made incredibly convenient because of the switchboard mechanism in our bias and the overall modular design of our bias and supporting circuits.

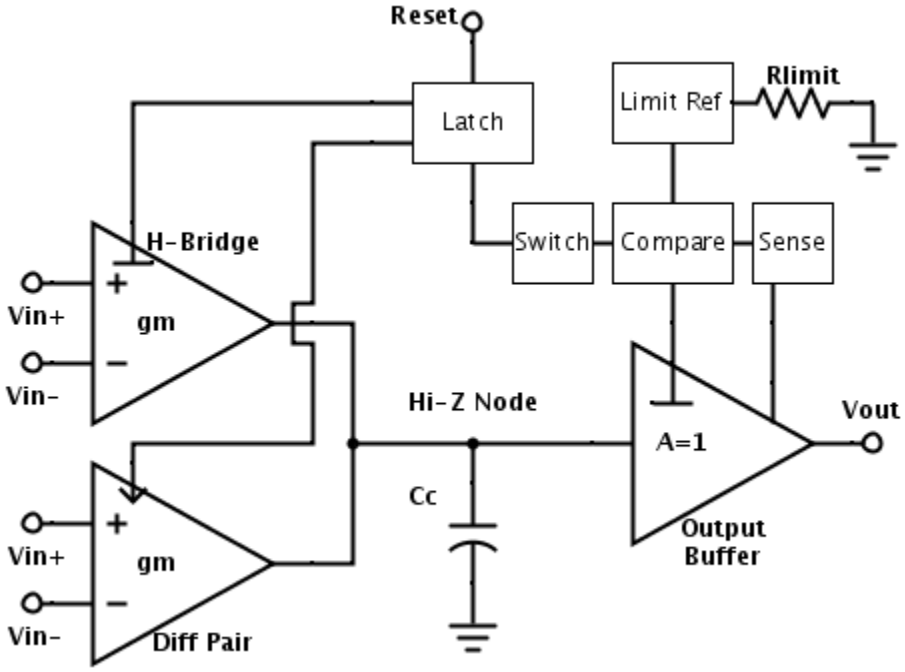

Figure 3-15: Final current limiting implementation

Figure 3-15 demonstrates a block diagram of our current limiting implementation.

3.3.7 Switching

The role of the switching circuit in this system is to take the variable feedback current coming out of the class AB current switch and activate a fixed switch current. This deals with the issue where initially the feedback current is very low, and it also allows us to use the current to perform other logic because we now will know the precise value of the current coming out of the switch block. We can now inject

this current into our control circuit because we know the magnitude of the current in its two states. This is preferable to simply relying on a variable current referred to the output sense current.

This switch is implemented as a differential pair circuit, shown in Figure 3-16.

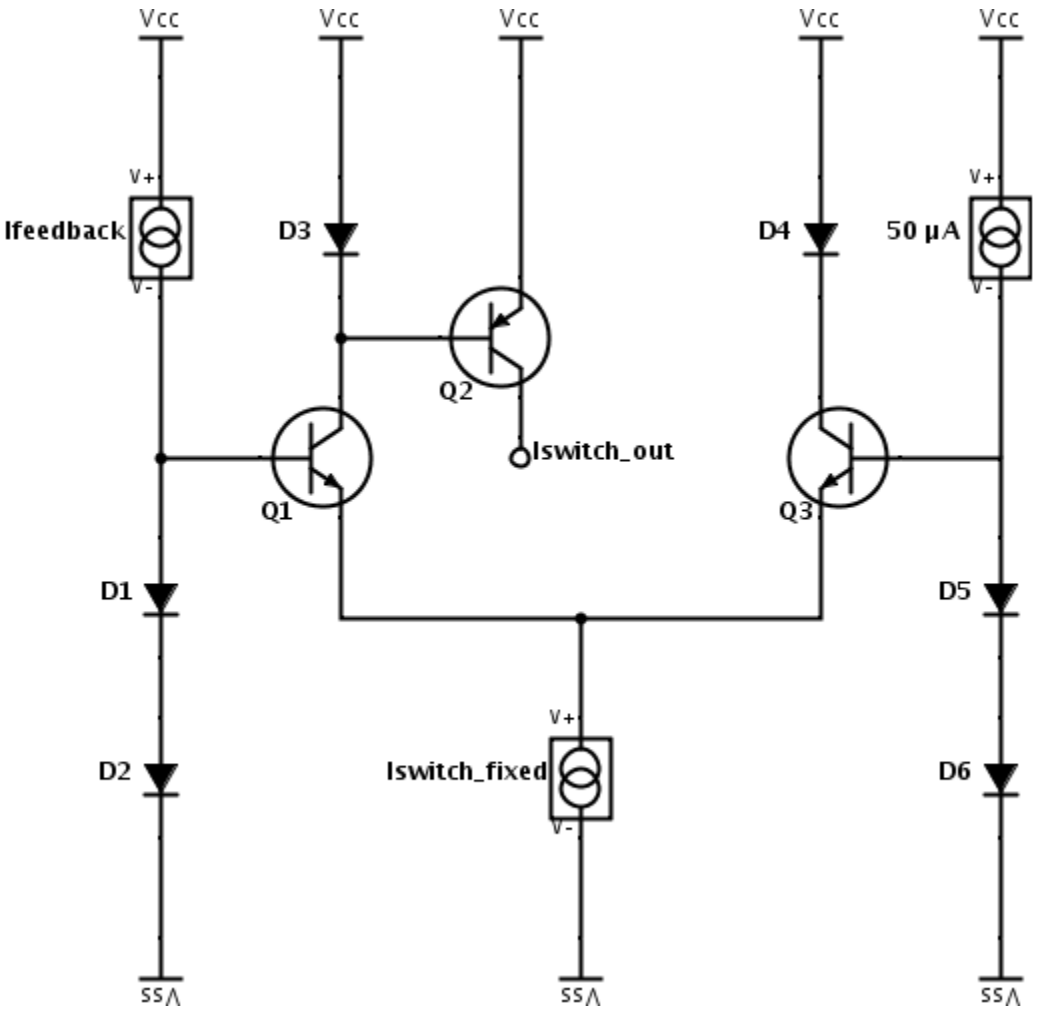

Figure 3-16: Switch in current limiting circuit

Consistent with the rest of the current limiting circuit, $I_{feedback}$ is the current coming out of the class AB current switch in the feedback loop. When current limiting is not in effect, $I_{feedback}$ is zero. The differential pair sees two inputs: the voltage produced by the current input from $I_{feedback}$ and a lightly biased current on the other side. This lightly biased 50 μA current exists to keep the default current out of the collector of *Q1* as zero, since *Q3* is biased on in the default case and thus

carries a majority of the tail current I_{switch_fixed}. This tail current is established as a predefined set current which matches a desired output current I_{switch_out} that will be needed for the latch, for the control circuit, and so forth. When a current greater than 50 μA comes into this circuit through $I_{feedback}$, the dynamics of the system change. *Q1* will turn on, driving a current from its collector. Device *Q2* will turn on and act like a simple current mirror with diode *D3*. As such, the switch has been activated and will output current through I_{switch_out}. This remains that case as long as the current coming in through $I_{feedback}$ is high enough.

This transistion happens very rapidly and is characterized by the following set of expressions where V_E is the common emitter voltage between the two devices *Q1* and *Q3* constituting the differential pair circuit.

$$I_{C1} = I_S e^{\frac{V_{B1}-V_E}{V_T}}; I_{C3} = I_S e^{\frac{V_{B3}-V_E}{V_T}} \tag{3.65}$$

$$\frac{I_{C1}}{I_{C3}} = e^{\frac{V_{B1}-V_{B3}}{V_T}} = e^{\frac{\Delta V}{V_T}} \tag{3.66}$$

$$\frac{I_{C1}}{I_{C1}+I_{C3}} = \frac{1}{1+e^{\frac{-\Delta V}{V_T}}}; \frac{I_{C3}}{I_{C1}+I_{C3}} = \frac{1}{1+e^{\frac{\Delta V}{V_T}}} \tag{3.67}$$

Given I_{switch_fixed} = $I_{C1} + I_{C3}$:

$$I_{C1} \approx \frac{I_{switch\_fixed}}{1+e^{\frac{-\Delta V}{V_T}}}; I_{C3} \approx \frac{I_{switch\_fixed}}{1+e^{\frac{\Delta V}{V_T}}} \tag{3.68}$$

Our two input currents to control the differential pair are $I_{feedback}$ and the trace 50 μA. They each feed into a stack of two diodes, the minimum number of V_{BE} to keep proper headroom at the base inputs of the pair of transistors (considering the V_{BE} of the device and $V_{CE_{sat}}$ of the current source). This gives us an expression for ΔV based on the voltages across the two diode stacks:

$$V_{B1} = 2V_T \ln\left(\frac{I_{feedback}}{I_S}\right) \tag{3.69}$$

$$V_{B3} = 2V_T \ln\left(\frac{50\mu A}{I_S}\right) \tag{3.70}$$

$$\Delta V = V_{B1} - V_{B3} = 2V_T \ln\left(\frac{I_{feedback}}{50\mu A}\right) \tag{3.71}$$

Plugging in yields the following:

$$\frac{I_{C1}}{I_{C1}+I_{C3}} = \frac{1}{1+\left(\frac{50\mu A}{I_{feedback}}\right)e^2}; \frac{I_{C3}}{I_{C1}+I_{C3}} = \frac{1}{1+\left(\frac{I_{feedback}}{50\mu A}\right)e^2} \tag{3.72}$$

$$I_{C1} \approx \frac{I_{switch\_fixed}}{1+\left(\frac{50\mu A}{I_{feedback}}\right)e^2}; I_{C3} \approx \frac{I_{switch\_fixed}}{1+\left(\frac{I_{feedback}}{50\mu A}\right)e^2} \tag{3.73}$$

The responsivity of the switch from one mode to the next is dependent on the ratio of currents between $I_{feedback}$ and the trace current of 50 μA. This was found to be ideal to achieve a stable switch which responds rapidly but not is not overly responsive such that it unintendedly turns itself on due to any unrelated stimuli (trace feedback current from when the amplifier is slewing, variations in supplies, temperature, and so forth). Note that if we had chosen to use large resistors instead of diodes to build the voltage drops at the inputs of the differential pair, there would be no ΔV logarithmic dependence on $I_{feedback}$; it would be linear. As such, the final expression for the current in each branch would exhibit an exponential relationship with $I_{feedback}$, which is even more responsive than the switch shown here. This design works sufficiently for our purposes, however.

The switch establishes a definitive logic state that establishes a condition for when current limiting must take effect.

3.3.8 Latch

Stability is a commanding property of any feedback loop, and it is no different in this case. If the switch block were to directly feed into current distributions, modulating which input stage is on and which input stage is off, we would run the risk of oscillations. This is especially relevant since the transient delay between our input stage and our output stage is so large; it is no secret that this design contains many stages. We choose to completely circumvent the risk of instability by controlling the state transition of the amplifier with the use of a latch.

The job of the latch is to look at the switch output current, and when the switch block indicates that current limiting is active the latch forwards the signal but retains the state. When the switch block which is transiently looking at the output current finds that current limiting is no longer necessary, the latch will continue forcing the amplifier to operate in a current limiting mode, using the alternate input stage. The amplifier will continue operating in this mode until the latch is reset, after which the amplifier returns to its default state, using the H-Bridge input stage. When the necessity for current limiting is detected, the latch will trigger again.

Like its counterpart the switch, the latch is a very digital concept which we must implement using analog components. Luckily for us, we can build upon the concepts we developed in the design of our switch; we just now have to add some sort of permanence or self-driving which forces the switch to remain in a state once flipped.

Once again, we have a differential pair in which the current input is by default zero. The other side of the differential pair has a light bias current of 50 μA which establishes it as the default state. In this default state I_{switch_out} is zero, I_{C4} sees all of the tail current I_{latch_fixed}, and thus I_{latch_out} is zero. When the switch current enters the circuit, device *Q1* turns on, and I_{latch_out} turns on, outputting a current mirrored from I_{latch_fixed}'s drive out the collector of *Q1*. Luckily for us, the equations which describe the operation of the majority of this circuit remain the same as before; no derivation is needed.

However, we now had an additional transistor and a unique connection. Transistor *Q2* is by default off. When the switch flips, a current comes out of the collector of *Q1*. Device *Q2* acts like a simple current mirror with diode *D3*, mirroring this fixed current. However, instead of sending this current to an output node like in the former case of the switch and like its brother device *Q3*, the source current from this device is sent into the base of device *Q1*. This is positive feedback; when the switch is flipped, device *Q2* turns on and keeps the switch on. Thus even when I_{switch_out} falls off and dwindles to zero the switch will remain latched in the on po-

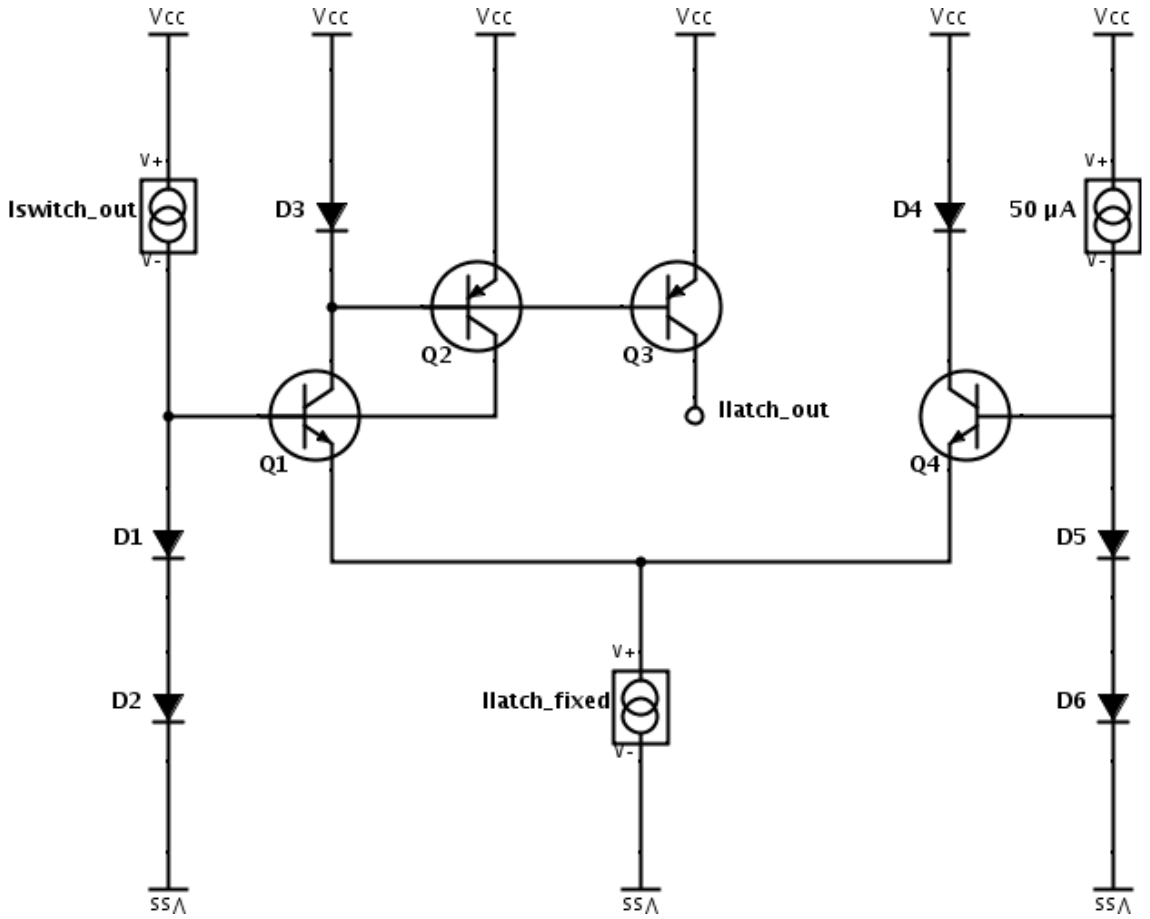

Figure 3-17: Latch in current limiting circuit

sition. There could be a high gain component to this current mirror which achieves this if necessary. In our schematic implementation we actually use a second differential pair switch which device *Q2* would then flip on, biasing the original switch on. Using more switches simply increases the robustness of this implementation: a third switch could be added which turns the trace 50 μA current on the other side of the switch off.

We do not demonstrate the reset pin in Figure 3-17 because there are several options for the placement of this pin. In essence, the reset pin must simply be an exposed node whose value can be driven to a high or low voltage to reset the switch. This could occur by utilizing the node at the emitter of devices *Q1* and *Q4*; pulling this pin down to the negative supply voltage will turn off the tail current and thus all currents in the latch, forcing the latch to reset. This is not optimal, how-

ever, because now neither output of the latch can be used while the reset is active. It is preferable to either use the node at the base of *Q1* or the node at the collector of *Q1*, pulling this voltage low and high, respectively. In the case of pulling V_{B2} low, devices *Q1*, *Q2*, and *Q3* are turned off, killing the positive feedback as well as its own output. This gives the circuit the opportunity to revert back to the default state. When V_{C1} is pulled high, diode *D3* is turned off, turning off devices *Q2* and *Q3*, killing only the positive feedback loop and allowing the circuit to immediately respond to whatever state it needs to be in once the reset pin is lifted. In our implementation we choose the third option.

The notion of using a latch offers a lot of external configurability to the circuit's user. Should he or she want to emphasize current limiting over amplifier performance, the latch never needs to be reset. Alternatively, the latch voltage can be permanently applied to disable current limiting capability of the part, permitting the amplifier to drive output current up to its inherent maximum current drive. External stimuli could be applied to this pin which applies a reset periodically or could respond to some flag which indicates when current limiting is active.

As a final point of note regarding the latch, the latch output current which goes into the control circuit to turn on the alternate input stage could be controlled downstream to produce the rudimentary current limiting mechanism of the ADA4870: current limiting triggered amplifier shut-off. A node either in the control circuit or in the current distribution biasing up the differential pair could be exposed which could then be pulled to a high or low voltage to interrupt the signal flow resulting from this chain of events. The alternate input stage will never turn on, the H-Bridge will still turn off, and thus the amplifier shuts off.

3.3.9 Alternative Input Stage

The output current from the latch suppresses the H-Bridge and activates an alternate input stage: a compound differential pair. In the default case the H-Bridge is biased up and the differential pair input stage is suppressed through reverse bias-

ing. This input stage is rather simple as one would expect from a differential pair input stage.

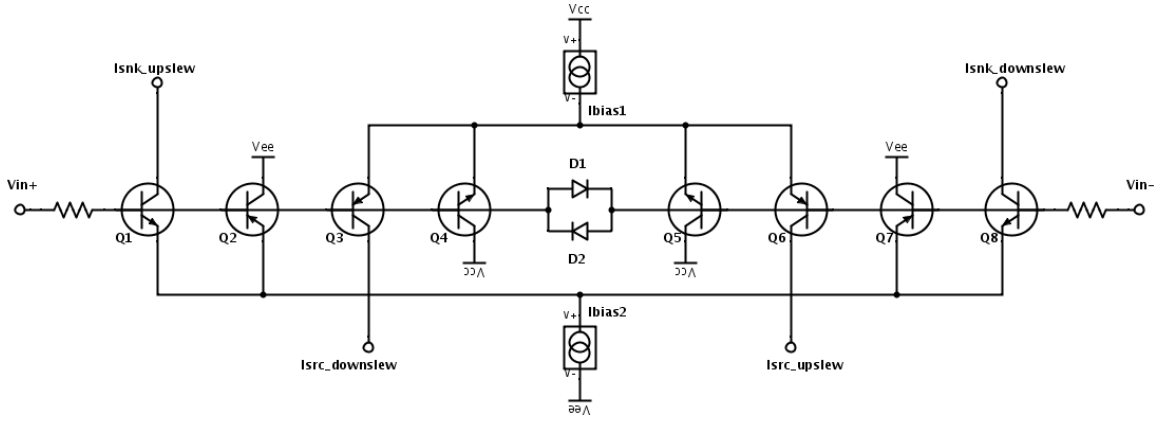

Figure 3-18: Alternate compound differential pair input stage

Devices *Q1*, *Q3*, *Q6*, and *Q8* are the fundamental four transistors which make up the essential structure of the differential pair. The bias currents I_{bias1} and I_{bias2} are very low to heavily slew limit the amplifier in this degenerate mode. Even when the stage is not biased it is still attached to the input stage, so we cannot permit this secondary input stage to compromise the functionality of the primary amplifier. Devices *Q4* and *Q5* clamp the voltage at the output of I_{bias1}, preventing it from exceeding a single V_{BE} below the input node. This is particularly important when I_{bias1} is negative and the input stage is reverse biased–in which case these devices are on. Likewise, devices *Q2* and *Q7* clamp the voltage at the output of current bias driver I_{bias2} within a single V_{BE} above the input stage. Again these devices are activated when the input stage is reverse biased and I_{bias2} reverses orientation.

Diodes *D1* and *D2* act as ESD protection on this input stage. We only have a single V_{BE} at our disposal here because a diode drop of two base-emitter junctions between the bases of the input devices will activate alternate current paths and turn the input stage on in response to a stimulus at the input when it should explicitly be off. This is the unfortunate interaction between the clamp devices and the primary driver transistors which we also observed was a possibility in the diamond based input stage. Example pairs which would otherwise turn the input

stage on when it is reverse biased:

- *Q1* and *Q7*
- *Q2* and *Q8*
- *Q3* and *Q5*
- *Q5* and *Q6*

Note that we depict two resistors at the input stage. If these were not here the ESD protection of a single V_{BE} across the diff pair would otherwise limit the ESD protection of the H-Bridge, which sees in total $2V_{BE}$ (one from each diamond's ESD diode in the H-Bridge) as well as the voltage across the g_m resistor between the two inputs. These resistances in the compound differential pair are very large such that a large voltage drop must be accrued across the input stage in order to activate the ESD diode path. These are large resistors (on the order of 1 $k\Omega$) but only trivially affect the headroom at the input stage because we have high impedance inputs; the current through these resistors is low and thus their voltage drops outside of ESD operation are inconsequential.

Thus concludes the discussion of the design of our current limiting system internal to the amplifier.

3.3.10 Timing Constraints

One important note needs to be made regarding the limitations of this system, a note that will apply to any current limiting mechanism but is especially relevant here because we have an amplifier with an otherwise inherently high slew rate and are attempting to perform current limiting on it. Understandably, there is a transient time delay corresponding to the activation and effect of the current limiting feedback loop. This time delay τ_{delay} corresponds to the total amount of time that elapses between when the output current hits the current limit and when the compound differential pair input stage becomes the dominant input stage driving the

output of the amplifier. Because of the numerous blocks involved in our system, τ_{delay} has numerous contributors:

$$\tau_{delay} = \tau_{sense} + \tau_{compare} + \tau_{switch} + \tau_{latch} + \tau_{\Delta input} + \tau_{in \rightarrow out} \tag{3.74}$$

The first few contributions are pretty straightforward and correspond to signal propagation delay arising from the stages of our current limiting system. $\tau_{\Delta input}$ corresponds to the amount of time it takes to concurrently reverse bias the H-Bridge and bias the differential pair. This corresponds to transient delays from the control and current distribution circuits. $\tau_{in \rightarrow out}$ refers to the propagation time for the signal from the newly activated input stage to propagate to the output.

During τ_{delay}, the output current could overshoot its current limit producing an error of $\Delta I_{overshoot}$ because the system does not kick in quickly enough.

The rate at which the current at the output changes is determined by the voltage slew rate of the part as well as the impedance of the load.

$$\frac{\partial I_{out}}{\partial t} = \frac{\partial V_{load}}{\partial t} \frac{1}{Z_{load}} \tag{3.75}$$

$$\Delta I_{overshoot} = \frac{\tau_{delay}}{Z_{load}} \left(\frac{\partial V_{out}}{\partial t} \right)_{slewrate} \tag{3.76}$$

As this demonstrates, the amount the output current of the amplifier will overshoot the ideal current limit is exacerbated by a large time delay attributed to the current limiting feedback loop, a high slew rate of the amplifier, or a small load impedance. There is no limit to this overshoot no matter how rapid of a current limiting feedback mechanism one implements, regardless of how slow one chooses to make their amplifier. This is beause Z_{load} is an external configuration, contingent upon the signal and and upon the nature of the load (resistive or capacitive). Z_{load} could be infinitely small (a short), guaranteeing that the output current can exceed the current limit. These are extreme examples that are unlikely under ordinary operating conditions of the circuit; however, they must be noted and addressed as an intrinsic limitation of this feature.

If the output current overshoot occurs there will be another timing consideration that will occur in which the amplifier recovers from the high current regime and dwindles back to its current limit: $\tau_{recovery}$. Depending on how extreme the overshoot is, the output may briefly turn off entirely or simply slew back down to its limit; whatever behavior is necessary to return to operation between the configurable current limit of the part imposed by the current limiting system. Thus the total time that elapses between when current limiting is required and when it is guaranteed to perform in a healthy fashion, tracking the input, is encapsulated by:

$$\tau_{ilimit} = \tau_{delay} + \tau_{recovery} \tag{3.77}$$

3.4 ”Boosting”

”Boosting” is a term which best describes the functionality of this next feature. This is a crude term; it has no formal existence in circuit literature, and there may be better means of capturing the essence of this subcircuit. Essentially, this is an additional circuit which when superimposed on the existing architecture of this amplifier gives improved large signal performance, improving the specifications of the part. However, this circuit must **not** have any quiescent power cost associated with it. This is a circuit which is entirely off at DC but enables when the amplifier is slewing, giving it an additional ”kick” to drive it harder, like overclocking a processor. The sole cost associated with this circuit is area on the chip but in return gives non-trivial gains in amplifier slew rate and bandwidth.

This circuit is explicitly designed for the topology presented here but could be applied to just about any amplifier with little adjustment or necessary interaction with the rest of the part.

3.4.1 Motivation

The motivation behind this circuit is twofold. Initially, one of the driving goals of this project was to produce a high current drive amplifier which could beat the specifications of its predecessor the ADA4870, but at a significantly lower quiescent current draw (20 mA instead of 33 mA). Many of the specifications attributed to bandwidth and slew rate, given that there are limited circuit architectures one can use, are heavily influenced and limited by process. Given that these two parts are in the same process (XF40), there was some progress made as far as sizing devices and implementation circuit topologies with less complexity and more refined functionality, but it was not enough. I needed to look for alternate methods of improving my amplifier while running at lower power–essentially trying to create something from nothing.

Next, I noticed a recurring theme in the design of the current limiting portion of the amplifier as well as the ESD protection circuits, especially the clamps across the input stage. Diodes and transistor devices which rely on V_{BE} turn-on to achieve operation have no quiescent current cost at DC but can transiently turn on and supply monolithic amounts of current when needed, as needed. As discussed in the context of current limiting, this current is obviously temperature dependent (and linearly so), but this is not problematic if we are simply speeding up the functionality of the amplifier by giving it more current drive rather than adjusting the voltage that the amplifier is attempting to track to.

I put these two concepts together to design a circuit which turns on while the amplifier is slewing heavily, introducing additional current into the signal path to better push the part to the limit of the process.

3.4.2 Implementation

When slewing, the transistor-based diamond buffer exhibits an inability to perform as an ideal buffer. We analyze the transient limitations of this circuit. Note that although the amplifier uses an H-Bridge input stage rather than a simple di-

amond buffer, the same logic applies twofold for the H-Bridge as it does to the diamond buffer. All implementations demonstrated here would be implemented to each side of the H-Bridge independently.

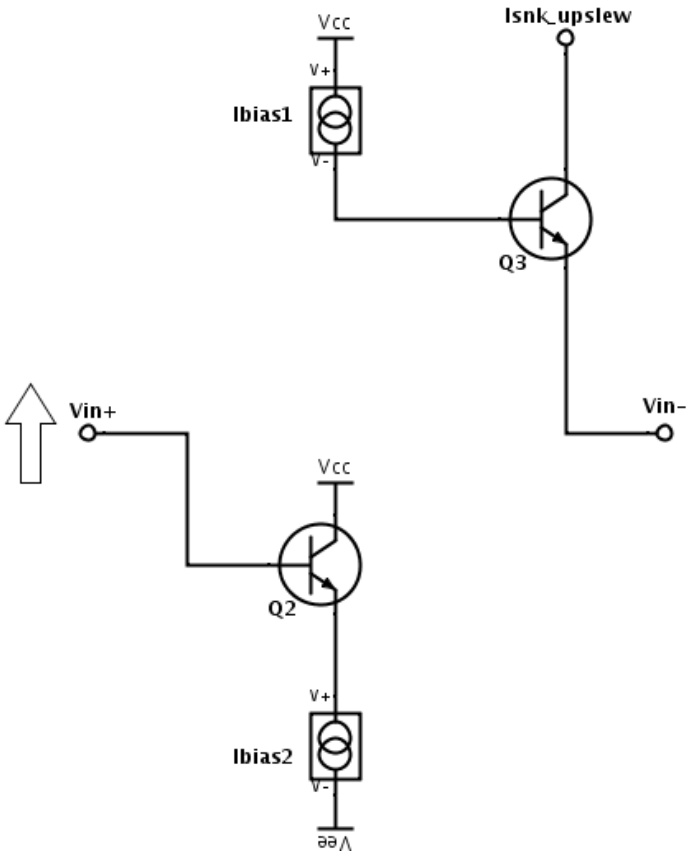

Figure 3-19: Upslew behavior of diamond buffer

Consider the case where the input is slewing upward very quickly. Figure 3-19 demonstrates the two devices which are active when the amplifier is slewing: *Q2* and *Q3*. Devices *Q1* and *Q4* are entirely off. There is no active connection between both sides of the diamond, therefore there is nothing to preserve the input-output relationship of the diamond buffer, which attempts to drive the output voltage V_{in-} to that of the input voltage V_{in+}. The output voltage is free to swing, solely subject to the limitation of clamps and ESD diodes.

One solution is to place clamp diodes across the diamond so that when the output of the diamond stops tracking the input it can only vary so much before it is clamped by the turn-on voltage of the diode. In simulation I noticed that

there was a significant amount of current passing through the clamp when the amplifier was slewing near bandwidth and at its peak slew rate, on the order of ten milliamperes. This current was going directly from the input source through the clamps, across the g_m resistor, out of the feedback resistor, and to the negative rail. This was wasted signal current.

Either fully replacing or in parallel with the ESD protection diodes across the diamond, I capitalize on this transient shortcoming of the bipolar junction transistor diamond buffer by utilizing transistors which turn on with the voltage difference across the diamond, and this is shown in Figure 3-20. Devices *Q5* and *Q6* are the two clamp transistors, and their sizing determines the amount of current that is generated for a given V_{BE} turn-on voltage across the diamond, due to the proportionality of collector current with device emitter area.

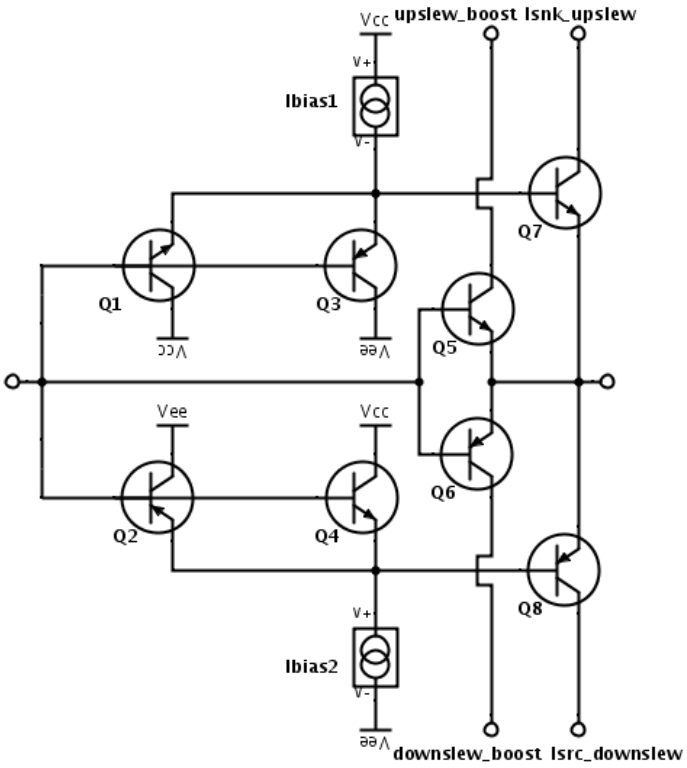

Figure 3-20: Capturing of clamp currents

When the voltage at the input of the diamond significantly leads the voltage at the output of the diamond (as in the case of a rapidly increasing upward voltage),

NPN device *Q5* will see a significant base-emitter voltage, turning on the device and thus driving its collector current *upslew_boost*, a sink current. In similar fashion, rapid downslew will produce an increase in the emitter-base voltage of PNP device *Q6*, sourcing current out of the collector of *Q6*: *downslew_boost*. As is the case with clamps, these two devices are off at DC and thus have no quiescent current cost associated with them nor any impact on DC input-referred offset error.

In this project I initially explored the possibility of injecting more current into the bias corresponding to each slew. When the amplifier is slewing upward, *Q7* is driving the upslew current which is βI_{bias1}, and when the amplifier is slewing downward, *Q8* is driving the downslew current which is βI_{bias2}. So I figured I could have the largest impact by taking these boost currents and using them to amp up the bias currents, shown in Figure 3-21.

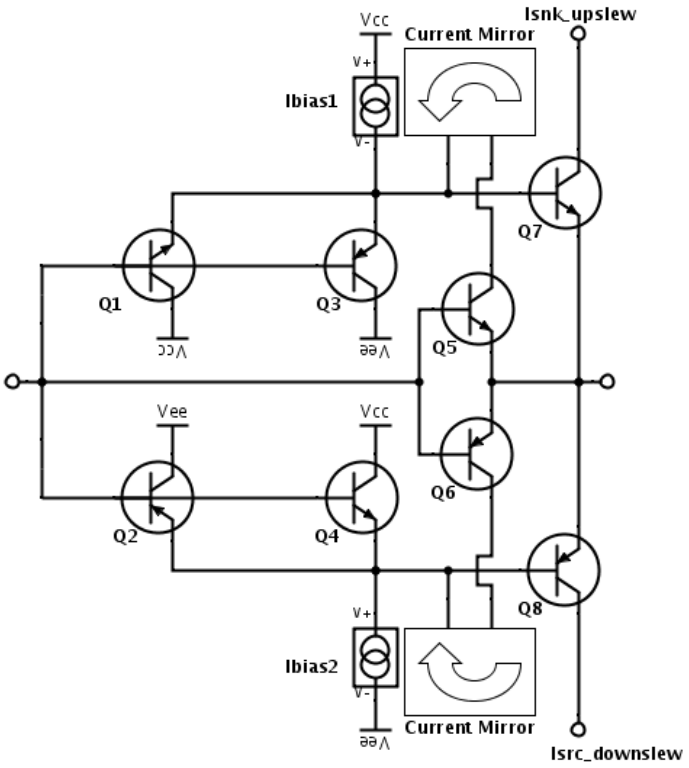

Figure 3-21: Clamp current driving input stage bias

This implementation is somewhat effective in that the output transistors have additional current available with which to drive their output currents. However,

I found that most of the additional current which was being provided as a bias current was not optimally contributing to signal from the input stage. Most of the upslew current mirrored from the collector of *Q5* would simply pass into the emitter of *Q3*, and likewise the downslew boost current from *Q6* was simply being sunk from the emitter of *Q4*, not contributing to output current from the input stage and thus not having a major impact on specifications of the amplifier. The reason for this is that devices *Q7* and *Q8*, the output devices of the diamond, were still requiring the same amount of current for a given slew of the input; their sizing was the same as before, and the quiescent current bias formerly provided was already greater than the peak base current of the devices for the given sizing. Not wishing to play a game of cat and mouse with sizing up the individual transistors and concurrently scaling the bias current, I turned to another approach, shown in Figure 3-22.

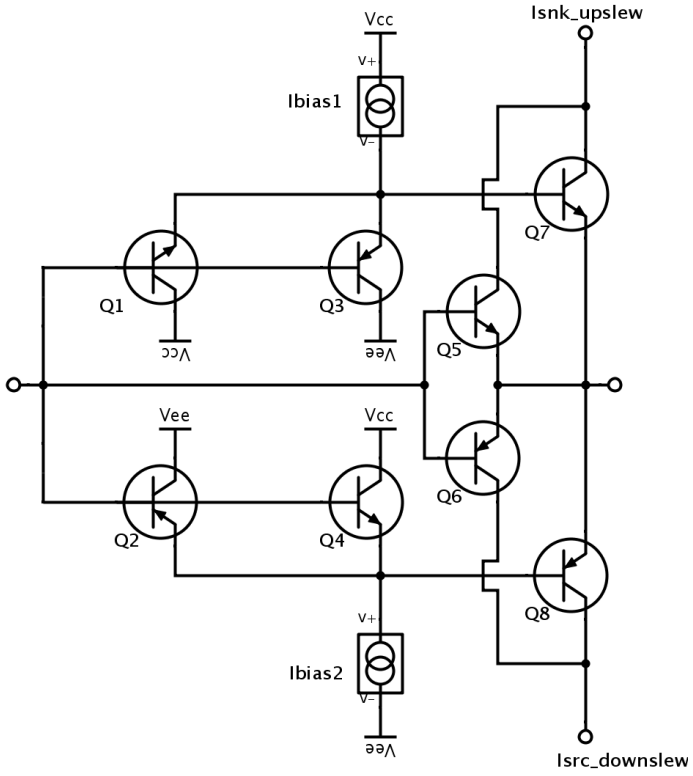

Figure 3-22: Clamp current driving signal path

Here the boost current is driven directly into the signal path of the amplifier,

and this is where I noted the most significant results. When slewing, the current from the clamp is several milliamperes, nearly as large as the current out of the diamond at its maximum slew rate, and thus with this current forced directly into the signal path it has a significant impact on the slew rate characteristics of the part. Having additional current helps the amplifier achieve large signal bandwidth and produced marginally better results in this respect as well.

Note that these two slew currents *upslew_boost* and *downslew_boost* can be injected in numerous locations throughout the amplifier. I mostly only focused on utilizing these currents in the input stage, but they could be passed anywhere in the signal path or current drive in subsequent stages of the amplifier. If injected early on in the signal path of the amplifier, subsequent current gain stages will apply to this current, potentially making better use of it. If utilized closer to the output stage of the amplifier, the transient power consumption of the amplifier will be less. With regards to abusing this feature, I found that too heavily sizing up the turn-on devices to produce very large currents could lead to noticeable total harmonic distortion due to the discontinuities in operation between when the ”boosting” devices are active and when they are off.

In this section we have made numerous broad claims regarding the benefits and consequences of this ”boosting” scheme, and they will be corroborated with empirical simulation data in the following chapter.

3.4.3 Problem and Fix

The one adverse consequence of this boosting circuit was an unfortunate interaction with my current limiting implementation. The feedback loop of the current limiting system turns the H-Bridge entirely off by turning off the bias current into the H-Bridge and then reverse biasing the H-Bridge. However, these turn-on ”boosting” transistors *Q5* and *Q6* prove problematic in this respect because changes in the voltage at the input, if significant enough, will turn on these devices and create currents that will come out of the H-Bridge, turning the input

stage back on if at the very least temporarily. Whether the boost currents from these devices feed into the bias current or directly into the signal path, the ”boosting” mechanism will turn the H-Bridge back on in a state where it should be off.

Ideally, this boosting circuit should be used in a context where there is no current limiting functionality, where very high slew rate, and where amplifier protection is de-emphasized since we are using transistors rather than rated ESD protection diodes. Thus, I needed to come up with a fix for my design.

The makeshift solution which was implemented to allow this ”boosting” circuit to coexist with the current limiting functionality of the amplifier involves a manual shut-off feature of the ”boosting circuit”. The simplest way to shut off a current manually is to feed it into a mirror and utilize the output of the mirror as the current output, taking note of the new directionality of the current. Then, when the voltage at the input of the current mirror is railed, the current mirror can be manually turned off. Current mirrors rely on matching of base-emitter junctions to replicate current, and when the input device is turned off, the output current of the mirror will be zero. This system-level implementation is shown in Figure 3-23.

Showing only the input stage and the current outputs, the boost currents are now each fed into a current mirror. There is a nontrivial transient delay associated with the additional current mirror, which makes it less preferable than simply taking the current and injecting it into the signal path directly. We compensate for this by taking the currents *upslew_boost* and *downslew_boost* and injecting them into the signal path down in the amplifier. When *upslew_boost_shutoff* is brought to the high supply rail V_{cc}, the output of the current boost path *upslew_boost* will be shut off, thus not interfering with current limiting. Analogously, when *downslew_boost_shutoff* is lowered to the negative supply rail V_{ee}, the output of the downslew current boost path *downslew_boost* will be turned off, killing *downslew_boost*. Thus the circuit user now has the option to shut off the current boosting functionality of the amplifier when current limiting functionality is emphasized.

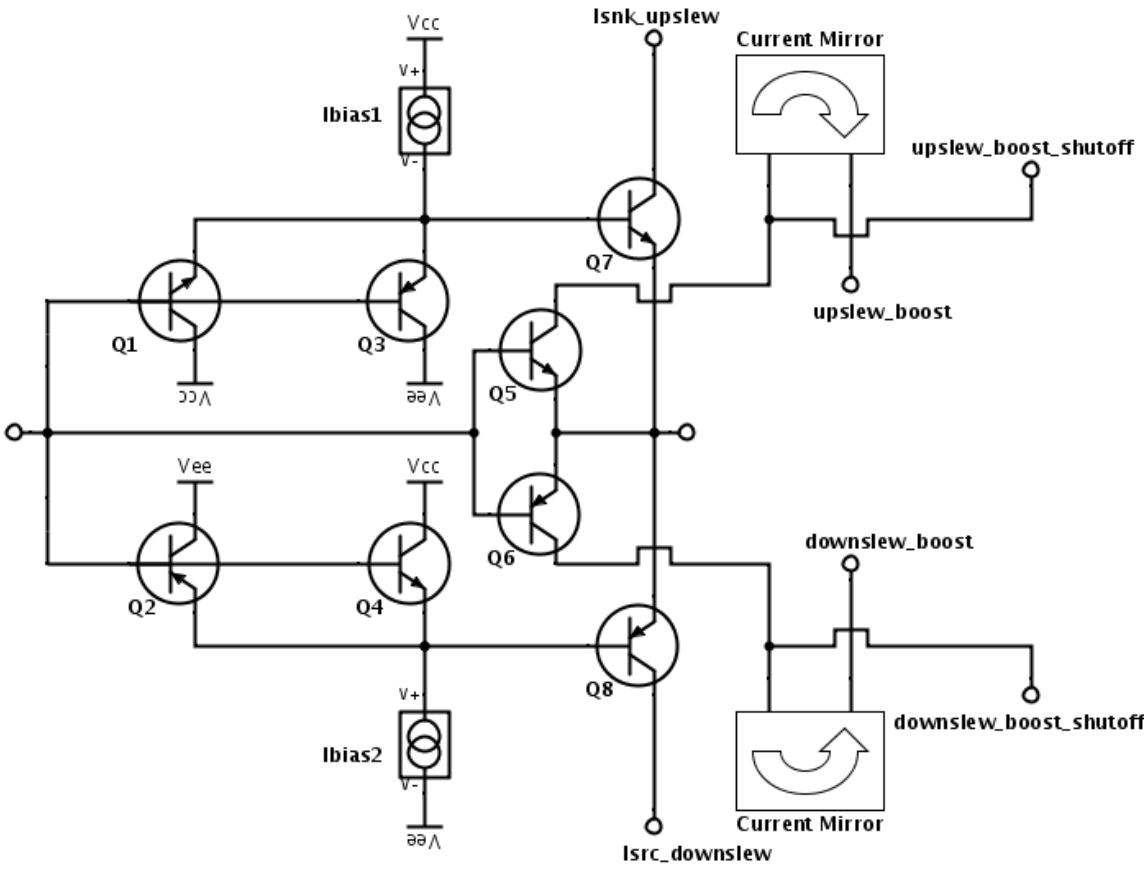

Figure 3-23: Boost circuit with shut off

3.4.4 Existing Implementations

I performed extensive research attempting to find other amplifiers and circuits which utilize this approach but was able to find few existing architectures. One commercially available part which incorporates a version of this kind of boosting is TI's OPA633, a high-speed buffer amplifier[17].

The implementation here is nearly identical to our proposed implementation in Figure 3-21 on Page 128. For the mirror from the boost current output to bias TI uses a low input-headroom mirror which is essentially the voltage across a resistor turning on a device by building up a base-emitter voltage drop. This mirror adds another current gain contribution to the boosting current: the boost current produces a voltage with a constant ratio that corresponds to the resistance of the turn-on resistor. This is a very high gain implementation of the ″boosting″

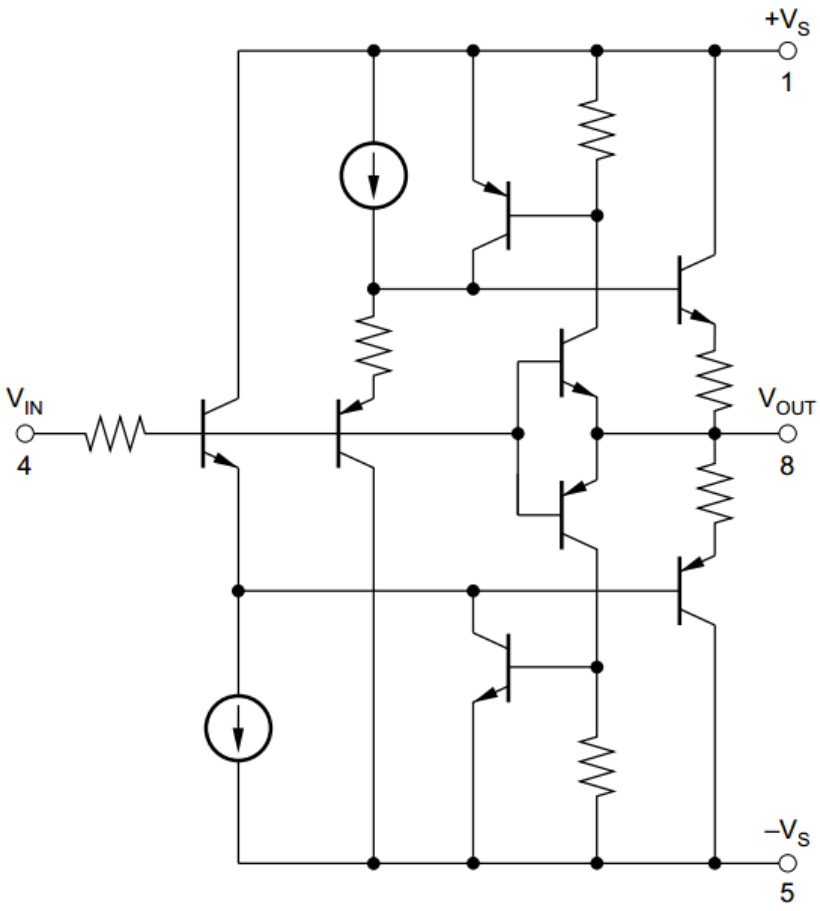

Figure 3-24: OPA633 buffer schematic

methodology that is presented here and demonstrates the potential for increasing the performance of a part by utilizing subcircuits which turn on transiently.

When the "boosting" circuit is active, OPA633's the additional bias current introduced by the turn-on devices exhibits a greater than exponential current gain dependence on the voltage across the diamond, ΔV.

$$I_{boost} = I_S e^{\frac{\Delta V}{V_T}} \tag{3.78}$$

$$\Delta I_{bias} = I_S e^{\frac{I_{boost} R}{V_T}} \tag{3.79}$$

$$\Delta I_{bias} \propto e^{e^{\Delta V}} \tag{3.80}$$

This is very high current gain stemming from the voltage disparity across the

input, indeed. For a buffer this certainly makes sense, since the quality of the buffer is determined by how accurately one can get the output of the buffer to track its input, and this ultra high current gain helps the output of the diamond move rapidly, letting buffer perform its job.

There are numerous other applications of this ”boosting” circuit structure which could additionally expand the performance of different parts of the amplifier. The same principles could be applied to the output stage, which is also a diamond buffer. When the output is lagging the high-Z node, devices would turn on which supply the output stage with additional current drive, boosting it and forcing the output to track the high-Z node more rapidly. This could potentially unlock even more bandwidth and slew rate. For now though, this establishes the concepts underlying the boosting circuit as implemented in this amplifier.

Chapter 4

Results

Outlining the methodology and design of the amplifier while making broad claims regarding its functionality and performance characteristics makes for great storytelling, but the proof of the pudding is in the eating. The purpose of this section is to present simulation results which demonstrate the capabilities of the amplifier while corroborating claims made throughout this thesis design proposal. This chapter opens by presenting a context behind the setup configuration of the amplifier in these simulation results, defining configurable variables primarily in the feedback network and load. Subsequently we present simulation results of the amplifier's performance capabilities at DC, at AC, and in the time domain. We follow by presenting the performance of supporting circuits and features of the amplifier, in the order they were introduced in the text. Finally the thesis concludes with a performance overview and a few closing words.

All simulations are performed in Adice5 (*Analog Devices Inc.*'s proprietary version of SPICE, using circuits constructed in Cadence using proprietary models for transistor devices in XF40.

4.1 Testbench

The testbench is the standard configuration of the amplifier which is used in evaluating the performance of the amplifier and is presented in Figure 4-1.

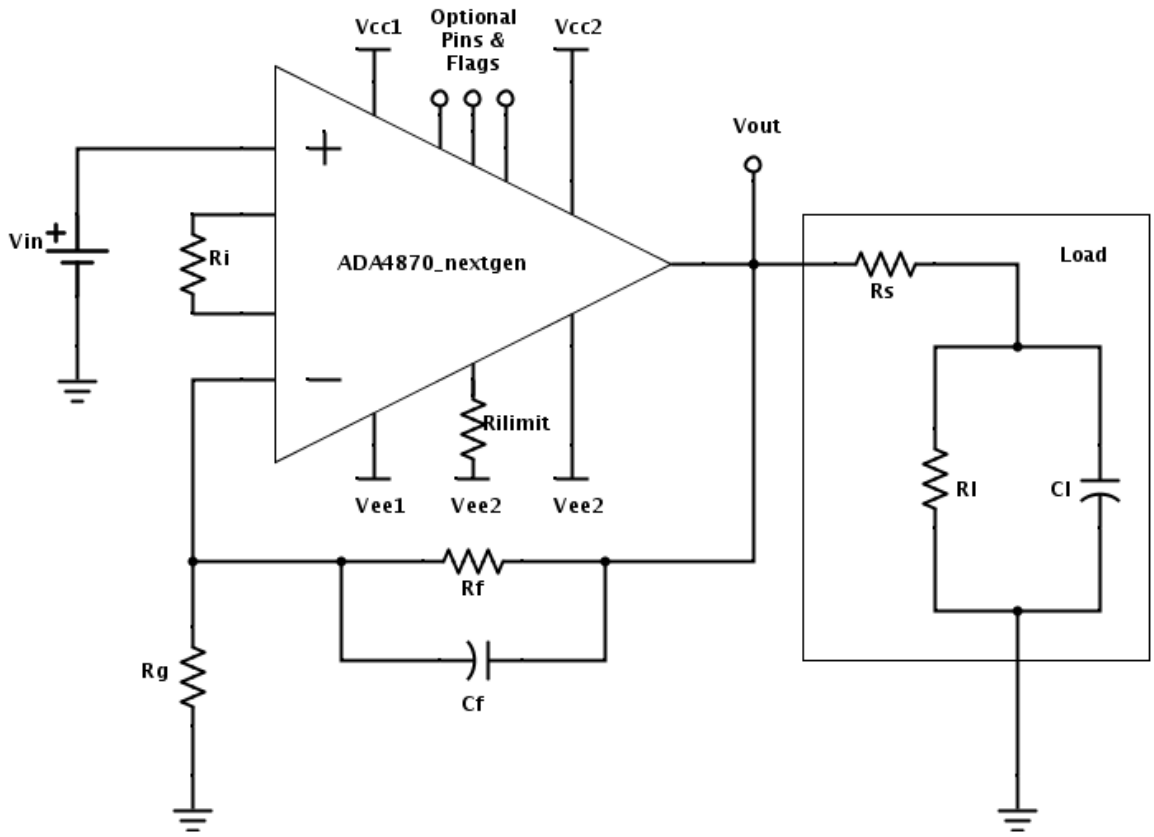

Figure 4-1: Amplifier testbench in non-inverting configuration

The configuration here shows the amplifier in a non-inverting input configuration, and this is the configuration that will be used for a majority of the simulation results. The symmetric nature of the amplifier's input stage and internals should mitigate the difference in amplifier performance between inverting and non-inverting configurations.

There are numerous variables in this setup that must be clearly defined:

- V_{in} - Input voltage signal
- R_f - Feedback resistor
- C_f - Feedback capacitor
- R_g - Current limit configuration resistor
- V_{cc1} - Input high supply rail

- V_{cc2} - Output high supply rail
- V_{ee1} - Input low supply rail
- V_{ee2} - Output low supply rail
- R_i - Effective g_m resistor across the H-Bridge.
- R_{ilimit} - Current limit configuration resistor
- R_s - Series output resistance
- R_l - Load resistance
- C_l - Load capacitance

Each configurable component has a default value that is kept equal across all simulation results. For example, we run most simulations in a gain of 2 configuration using $R_f = R_g = 500\Omega$. For all simulations except for the ones explicitly evaluating disjoin supply rails $V_{cc1} = V_{cc2}$ and $V_{ee1} = V_{ee2}$. These supply rails are $\pm 20V$ outside of the scenarios where we are testing supply rail variance. R_i is selected to be whatever value will give us a phase margin of $45°C$ for a given configuration and load. R_{ilimit} is 1000 Ω by default, corresponding to a current limit of 1 Ampere. Finally our load defaults to a mostly capacitive load: $R_s = 5\Omega$, R_l is very high (an open connection), and C_l is 100 pF. We vary this load considerably when evaluating AC and time domain results.

In addition to these variables, we have a large set of optional pins and flags that enable additional interactions with the amplifier that will be referenced to on an "as needed" basis. These are:

- Shutdown
- Latch reset
- Boosting disable
- Current limiting disable

- Differential pair turn-on disable
- Shutdown flag
- Current limiting switch flag
- Current limiting latch flag

4.1.1 C_f bandwidth extension

Capacitor C_f appears in our test bench as a capacitance in parallel with the feedback resistor R_f.

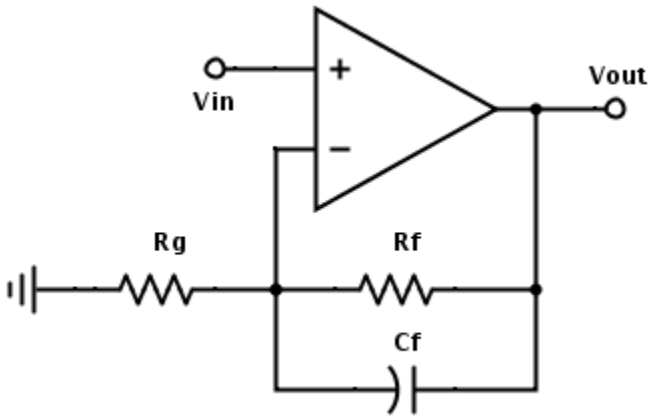

Figure 4-2: Non-inverting feedback with C_f

This has an interesting effect on the transfer function of the amplifier, since the feedback impedance is now complex due to the addition of a capacitance. Re-deriving our small signal transfer function from our discussion of configurable g_m:

$$\frac{V_{out}}{V_{in}} = \frac{A(s)}{1 + A(s)\left(\frac{R_g}{Z_f + R_g}\right)} = \left(\frac{Z_f + R_g}{R_g}\right) \frac{1}{1 + \frac{1}{A(s)} \frac{Z_f + R_g}{R_g}} \tag{4.1}$$

$$Z_f = R_f \parallel sC_f = \frac{R_f}{1 + sR_fC_f} \tag{4.2}$$

$$\frac{Z_f + R_g}{R_g} = \left(1 + \frac{R_f}{R_g}\right) \frac{1 + s\frac{R_fR_gC_f}{R_f + R_g}}{1 + sR_fC_f} \tag{4.3}$$

$$\frac{V_{out}}{V_{in}} = \left(1 + \frac{R_f}{R_g}\right) \frac{1 + s\frac{R_f R_g C_f}{R_f + R_g}}{1 + sR_f C_f} \frac{1}{1 + \frac{1}{A(s)}\left(1 + \frac{R_f}{R_g}\right)\frac{1 + s\frac{R_f R_g C_f}{R_f + R_g}}{1 + sR_f C_f}} \tag{4.4}$$

Without going through the hairy process of simplifying further we already see a pole-zero contribution to the transfer function (one which did not formerly exist without a complex Z_f) pop out of the expression:

$$\tau_{pole} = R_f C_f \rightarrow f_{pole} = \frac{1}{2\pi}\frac{1}{R_f C_f} \tag{4.5}$$

$$\tau_{zero} = \frac{R_f R_g C_f}{R_f + R_g} \rightarrow f_{zero} = \frac{1}{2\pi}\frac{R_f + R_g}{R_f R_g C_f} \tag{4.6}$$

We can produce a pole-zero combination in the vicinity of the bandwidth of our part in order to extend the bandwidth a smidgeon. Assuming that our bandwidth is on the order of 60 MHz we require the pole and zero to be above 60 MHz but not too far away; we want to extend the bandwidth before the gain of the transfer function ramps down too far. We also don't want to place these corner points too close to the bandwidth of the part otherwise the peaking from the pole zero pair could contribute to resonance/peaking near the bandwidth of the part. The default configuration utilizes $R_f = R_g = 500\Omega$ and a feedback capacitor of C_f = 3 pF.

$$f_{pole} = \frac{1}{2\pi}\frac{1}{(500\Omega)(3pF)} = 106 \text{ MHz} \tag{4.7}$$

$$f_{zero} = \frac{1}{2\pi}\frac{500\Omega + 500\Omega}{(500\Omega)(500\Omega)(3pF)} = 212 \text{ MHz} \tag{4.8}$$

One gross inconvenience of this implementation is that C_f will have to be changed when the gain of the overall amplifier feedback network is adjusted. Adjusting the gain of the circuit involves changing R_f, R_g, or the ratio between the two values. In order to keep the pole frequency constant R_f and C_f must remain the same. But changing R_g to adjust the gain of the amplifier will move the zero of this feedback network, changing the bandwidth extension properties. Thus we will have to change C_f as well to fix this. This is problematic because the implication is that C_f is another level of complexity tied to the feedback configurability of

the amplifier.

The solution to this is achieved by splitting R_f into two components, R_{f1} and R_{f2}, demonstrated in Figure 4-3.

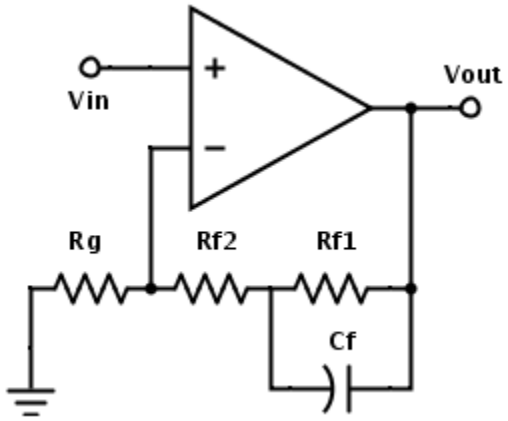

Figure 4-3: Non-inverting feedback with C_f and split R_f

Now the complex feedback impedance Z_f is:

$$Z_f = \frac{R_{f1}\left(\frac{1}{sC_f}\right)}{R_{f1}+\frac{1}{sC_f}} + R_{f2} = \frac{R_{f1}+R_{f2}+sR_{f1}R_{f2}C_f}{1+sR_{f1}C_{f1}} \tag{4.9}$$

$$\frac{V_{out}}{V_{in}} \propto 1 + \frac{Z_f}{R_g} = \left(\frac{R_{f1}+R_{f2}+R_g}{R_g}\right)\frac{1+s\left(\frac{R_{f1}C_f(R_{f2}+R_g)}{R_{f1}+(R_{f2}+R_g)}\right)}{1+s(R_{f1}C_{f1})} \tag{4.10}$$

$$f_{pole} = \frac{1}{2\pi}\frac{1}{R_{f1}C_f} \tag{4.11}$$

$$f_{zero} = \frac{1}{2\pi}\frac{R_{f1}+(R_{f2}+R_g)}{R_{f1}C_f(R_{f2}+R_g)} \tag{4.12}$$

With a split feedback resistor consider the case where R_{f1} and C_f are kept constant in order to fix the pole frequency of the feedback network. Changing R_f2 and R_g independently will in fact change the frequency of the zero introduced by this setup. However, as long as the sum $R_f + R_g$ is kept constant, the zero frequency will remain at the same value. Thus we now possess the capacity to adjust the DC gain of the feedback network while keeping the frequency contributions of the pole and zero introduced through bandwidth extension.

This does not kick in for a majority of the simulations presented in this chapter because most of the simulations utilize the amplifier in a gain of 2 configuration, so we are content with simply using the fixed feedback capacitance of 3 pF. The potential for bandwidth extension is here, however, and because of the ability to utilize constant R_{f1} and C_f regardless of amplifier closed loop gain, these components could even be internal to the IC, with a feedback pin exposed where the user configures R_{f2} and R_g, keeping the sum impedance of the two components constant.

4.2 Amplifier DC performance

DC performance of the amplifier is based solely on architecture. In these measurements the amplifier is not slewing; the input is at a DC value, and the quiescent properties of the amplifier are observed.

4.2.1 Input-referred offset

We commence with a demonstration of the input-referred offset of the amplifier, one of the cornerstone achievements of this amplifier. A sweep of the input-referred offset over temperature can be seen in Figure 4-4.

At room temperature (27°C) the input-referred offset is **-49.39** μV, and this is without any sort of trim whatsoever. Compare this to the input-referred offset of 3 mV of the ADA4870.

V_{OS} ranges from -143.6 μV at 0°C to 199.7 μV at 125°C, resulting in a total temperature drift of **2.75** $\mu V/^{\circ}C$. This is one tenth the ADA4870's temperature drift in simulation of 22.89 $\mu V/^{\circ}C$.

Figure 4-5 demonstrates a Monte Carlo simulation of the amplifier's input-referred offset to gauge its resilience to process variations. Over a sample size of a thousand iterations, the Monte Carlo simulation turned up a mean V_{OS} of 43.42 μV with a standard deviation of 547.8 μV.

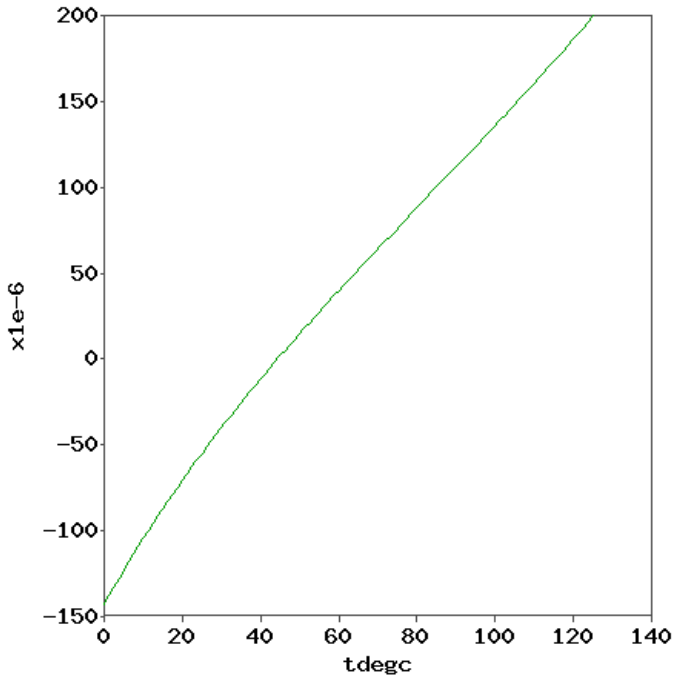

Figure 4-4: DC sweep of input-referred offset V_{OS} over temperature

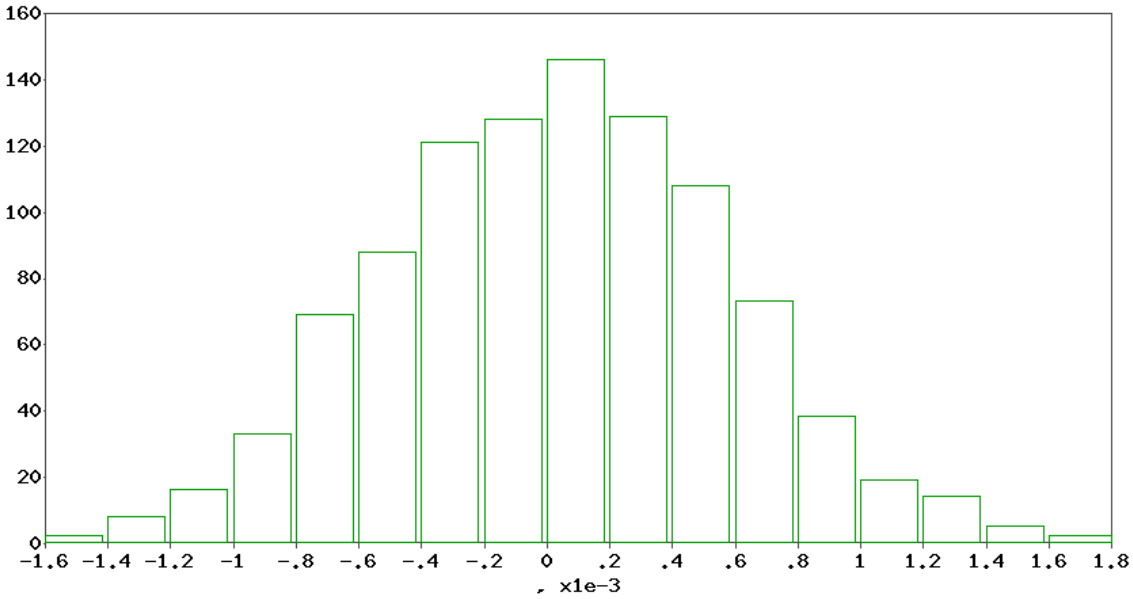

Figure 4-5: Histogram of V_{OS} from Monte Carlo model statistical simulation

4.2.2 Input impedance

The input impedance of the amplifier is determined by placing a voltage with a series resistor at the input terminal. Taking the voltage drop across the resistor one

can then derive Z_{in}:

$$\frac{V_{pin}}{V_{in}} = \frac{Z_{in}}{Z_{in} + R_{series}} \tag{4.13}$$

$$Z_{in} = \frac{V_{pin} R_{sense}}{V_{in} - V_{pin}} \tag{4.14}$$

Using this approach we calculate the input impedance of the non-inverting terminal to be **1.12** $M\Omega$ and find the impedance at the inverting terminal to be **1.15** $M\Omega$.

4.2.3 Input bias current

The input bias current is very low, as one would expect from a high-impedance input voltage feedback amplifier.

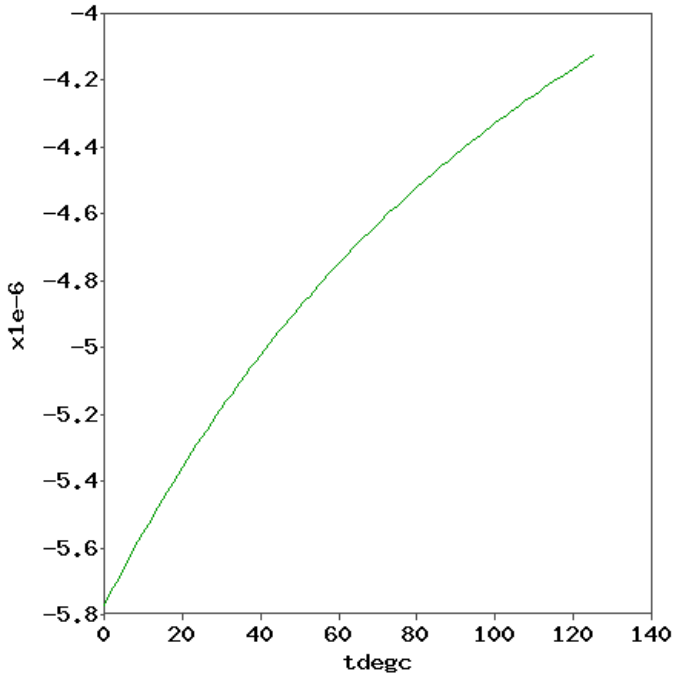

Figure 4-6: Sweep of non-inverting input bias current over temperature

The non-inverting input bias current is **5.236** μA at room temperature, and a sweep of the non-inverting input bias current over temperature can be see in Figure 4-6.

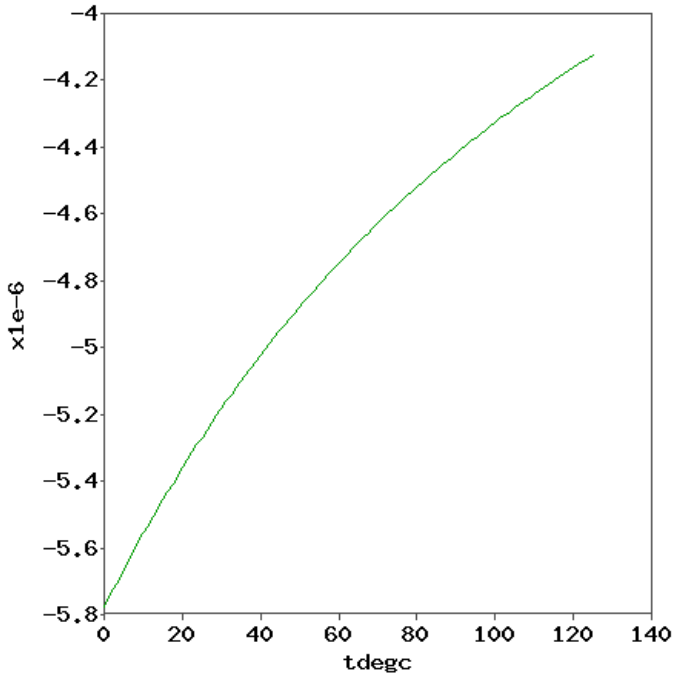

Figure 4-7: Sweep of inverting input bias current over temperature

The inverting input bias current is **5.237** μA at room temperature, and a sweep of the inverting input bias current over temperature can be see in Figure 4-7.

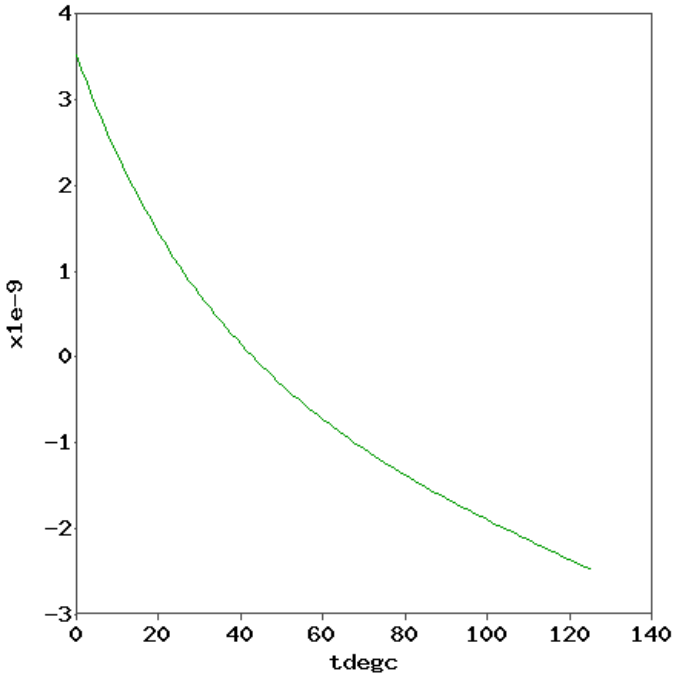

Figure 4-8: Difference in input bias currents over temperature

As a final point of note, because of the sheer symmetry of the amplifier input stage, the difference between input bias currents is miniscule: 918.3 pA at room temperature. A sweep of the difference in input bias currents can be seen in Figure 4-8. This means minimal contribution to input-referred offset.

4.2.4 Input headroom

We measure the input headroom by sweeping the input voltage from -20 Volts to 20 Volts and looking at the input predriver devices. When they are on, they conduct the 1 mA from the bias, but they turn off near the supply rails, indicating that the input voltage has exceeded the headroom of the part. The results of this simulation are shown in Figure 4-9.

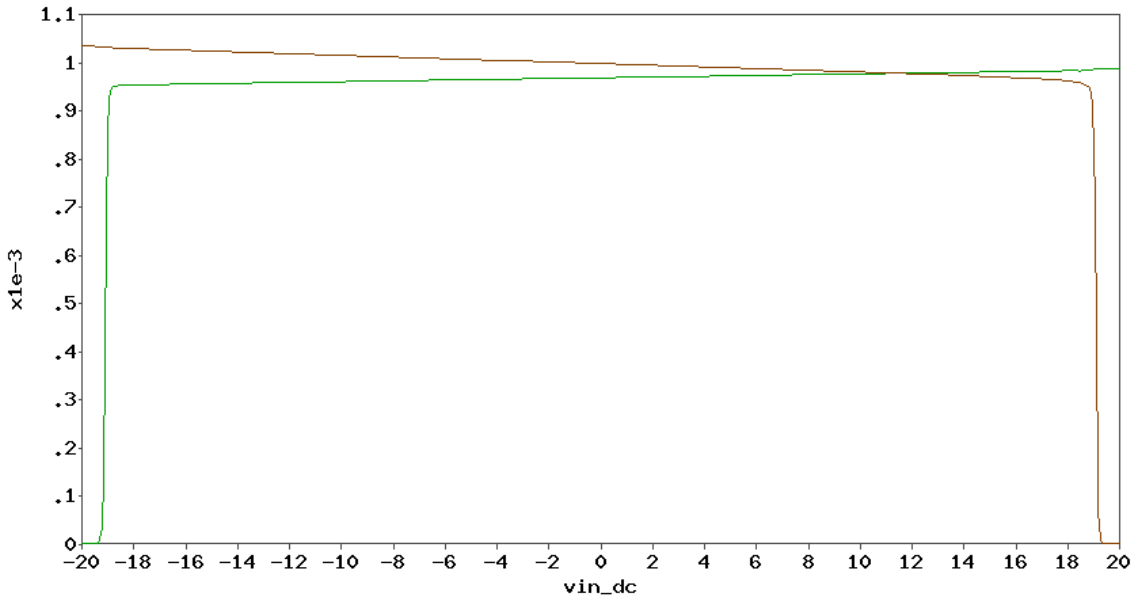

Figure 4-9: Sweep of input device I_C over input voltage; Green - low headroom, Brown - high headroom

The device referred to the lower supply rail turns on at -18.85 V, indicating a low supply headroom of **1.15 V**. The input headroom proves to be symmetric at the high supply range of the amplifier, with the other input driver device turning off at 18.85 V, setting an identical high supply headroom of **1.15 V**. Putting this together we come up with an input common mode voltage swing of **37.7 V**. These

values seem correct given the theoretical headroom value of $V_{BE} + V_{CE_{sat}}$ (along with emitter degeneration).

4.2.5 Output headroom

To test the output headroom limits of the amplifier we sweep the input voltage from -10 Volts to 10 Volts, in our default gain of 2 configuration. When the output is unable to track its expected output voltage, the amplifier is operating within the output headroom of the part. This sweep is shown in Figure 4-10.

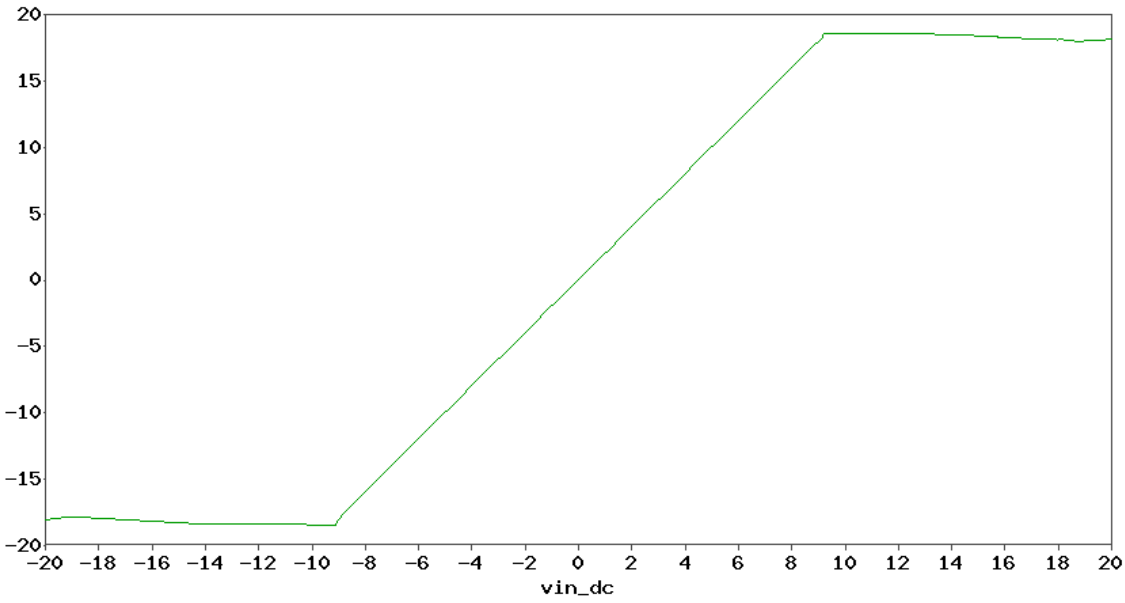

Figure 4-10: Rail to rail output voltage swing capabilities

The low supply headroom of the part breaks at -18.00 V, indicating a low supply headroom of **2.00 V**. The high supply headroom of the amplifier's output stage diverts at 18.39 V, thus the high range headroom is **1.61 V**. This is therefore a cumulative output voltage swing of **36.39 V**. These values seem relatively correct given the theoretical headroom of $2V_{BE} + V_{CE_{sat}}$ (again plus emitter degeneration).

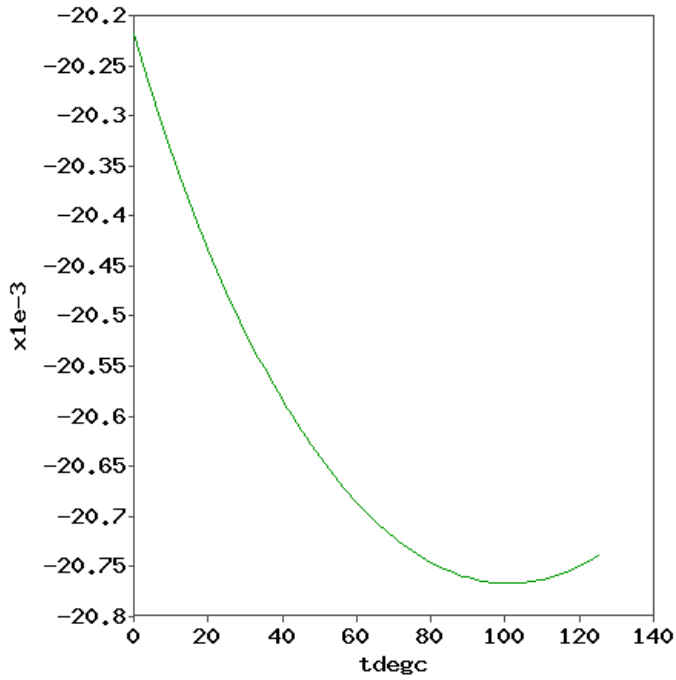

Figure 4-11: Sweep of amplifier supply current over temperature

4.2.6 Power consumption

The quiescent current draw of the amplifier is **20.49 mA** at room temperature, totalling **0.82 Watts** with 40 Volts supply range. This is a much lower power version of the ADA4870, which uses 33 mA quiescent current. A sweep of DC supply current as a function of temperature is shown in Figure 4-11. The total temperature drift of the supply current is **4.175** $\mu A/^{\circ}C$, which tells us that the temperature independence of our bias is stellar.

The supply current of the amplifier changes trivially as the voltage supply rails range from $\pm$10 V to $\pm$20 V and has a total supply drift of 135 μA/V, which indicates that our bias exhibits a decent degree of voltage supply independence. A sweep of DC supply current as a function of supply voltage is shown in Figure 4-11.

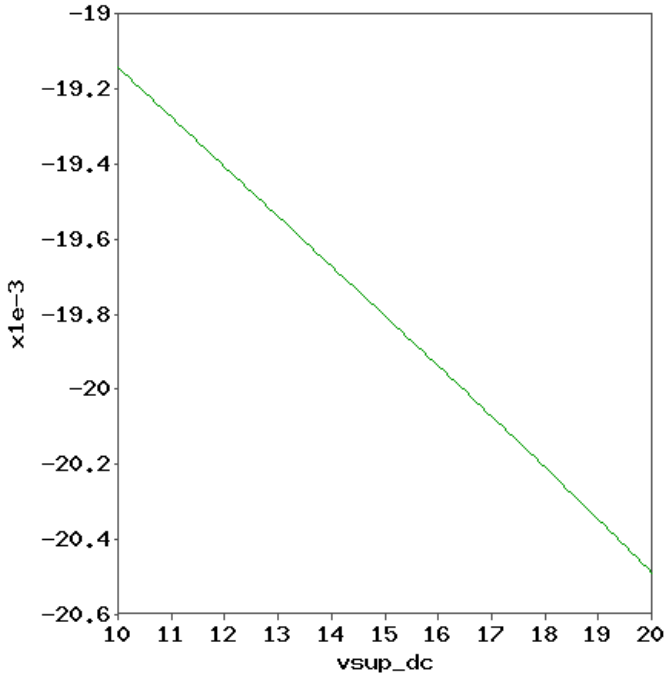

Figure 4-12: Sweep of amplifier supply current over supply voltage

4.3 Amplifier AC performance

Amplifier AC performance is simulated in the frequency domain, presenting the small signal characteristics of the amplifier. In this section we focus primarily on bandwidth and phase margin, and how they vary as certain parameters are swept. Finally we address other frequency domain attributes of the amplifier, such as noise, CMRR, and PSRR.

4.3.1 Bode plot

From Figure 4-13 we determine the small signal -3 dB bandwidth of the amplifier in this configuration to be **66.29 MHz**. The amplifier overshoots the low frequency gain by **2.407 dB**, which is a function of the moderately low phase margin (45°).

The phase of the amplifier configuration at a crossover frequency of 35.2 MHz is -135.1°, thus the phase margin of the overall amplifier is **44.9**°. The amplifier's phase as a function of frequency is shown in Figure 4-14.

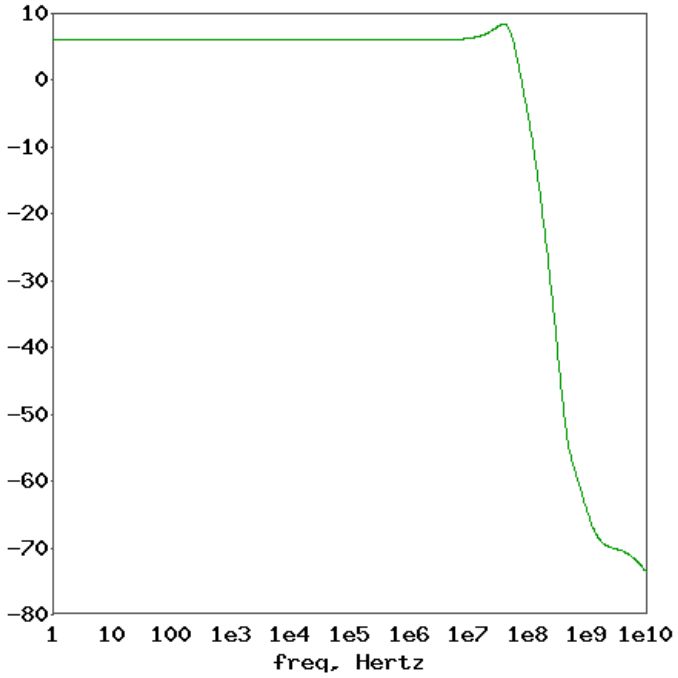

Figure 4-13: Gain Bode plot of amplifier in standard gain of 2 configuration

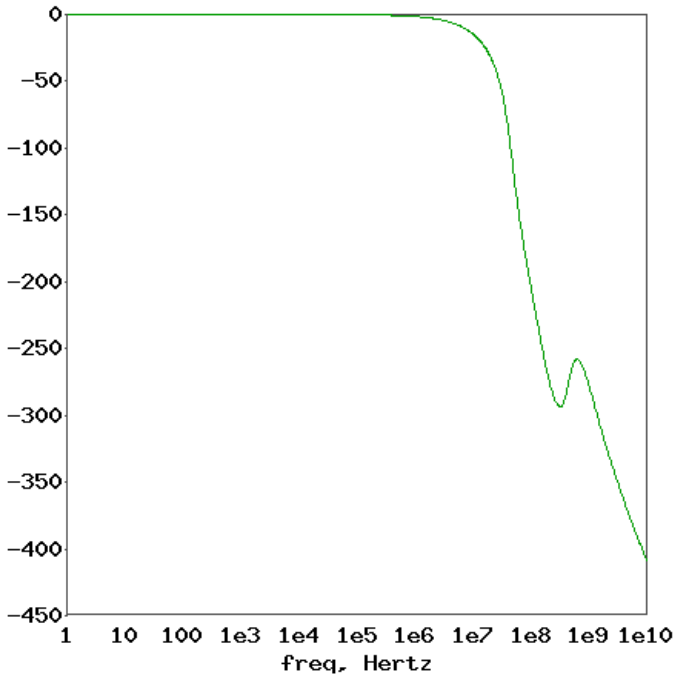

Figure 4-14: Phase Bode plot of amplifier in standard gain of 2 configuration

4.3.2 Loop gain

The loop gain amplifier is shown on Figure 4-15 on Page 4-15 and is established by a built-in Adice function which evaluates loop dynamics using the *Middlebrook*

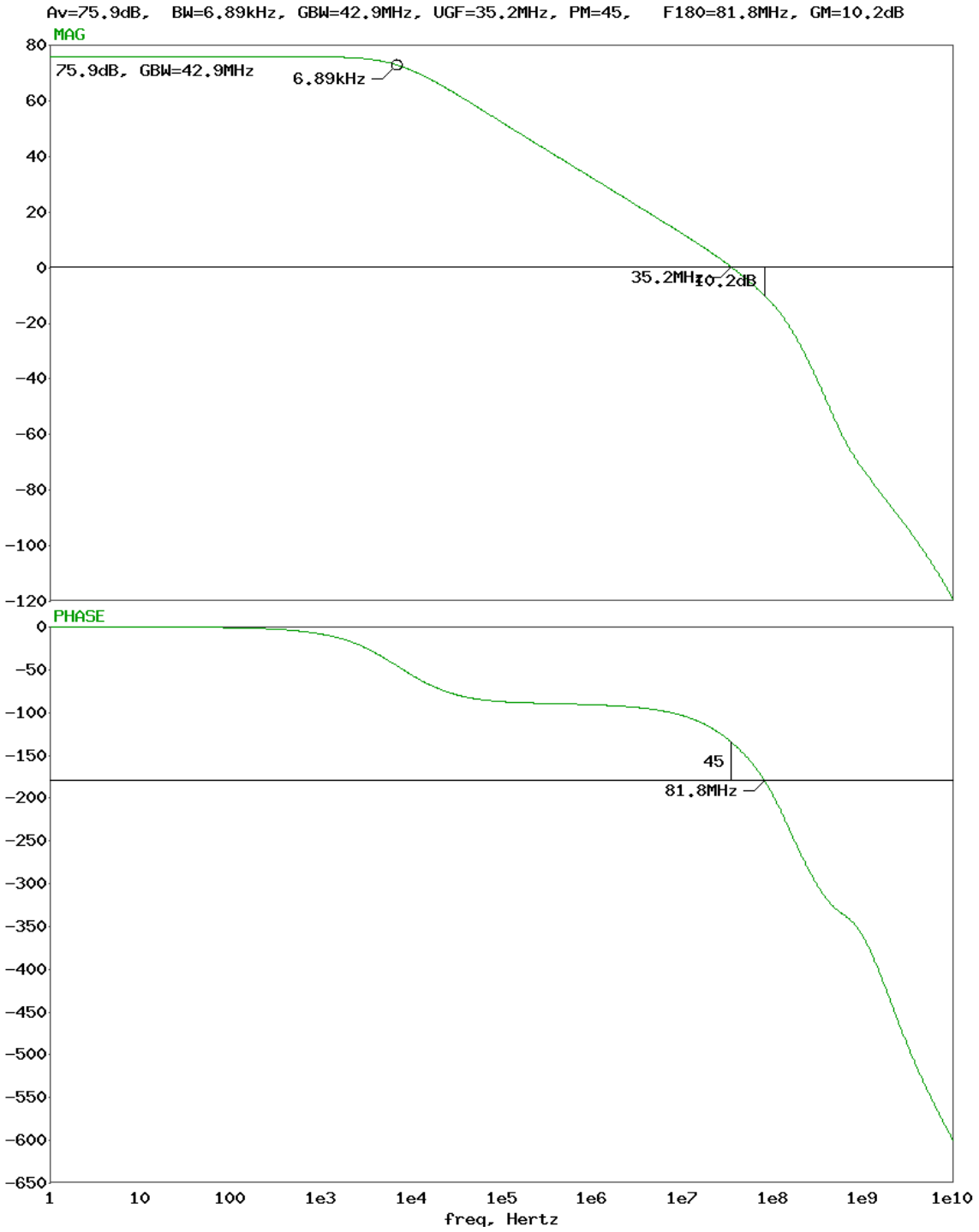

Figure 4-15: Loop gain characteristics of default configuration

method[18]. This methods gives us a crossover frequency of **35.2 MHz** and confirms our phase margin of **44.9**°.

4.3.3 AC characteristics over different gains

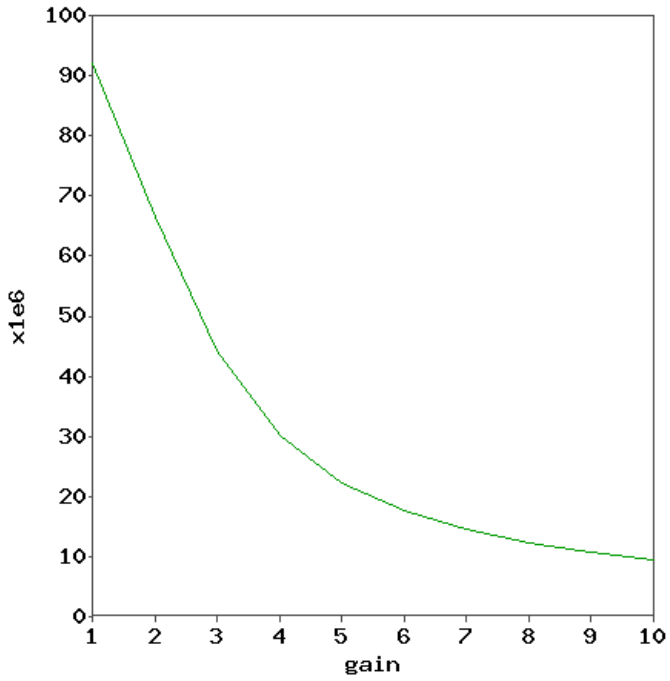

Figure 4-16: Sweep of amplifier small signal bandwidth over gain

As one elects to apply the amplifier in higher DC gain configurations, overall bandwidth of the amplifier reels in.

However, this loss in bandwidth as the gain of the amplifier increases is offset by an increase in the phase margin (stability of the amplifier). By adjusting g_m we will be able to recover bandwidth at higher gain configurations, as we will demonstrate later.

4.3.4 AC characteristics over purely capacitive loads

At higher capacitive loads we see that the additional capacitance cuts into the bandwidth of the part, again pulling in the small signal frequency response and trading bandwidth for stability.

This demonstrates that our amplifier is stable and has reasonable bandwidth at 10,000 pF, making it suitable for the driving of loads with high capacitive input impedances, such as a FET or pin.

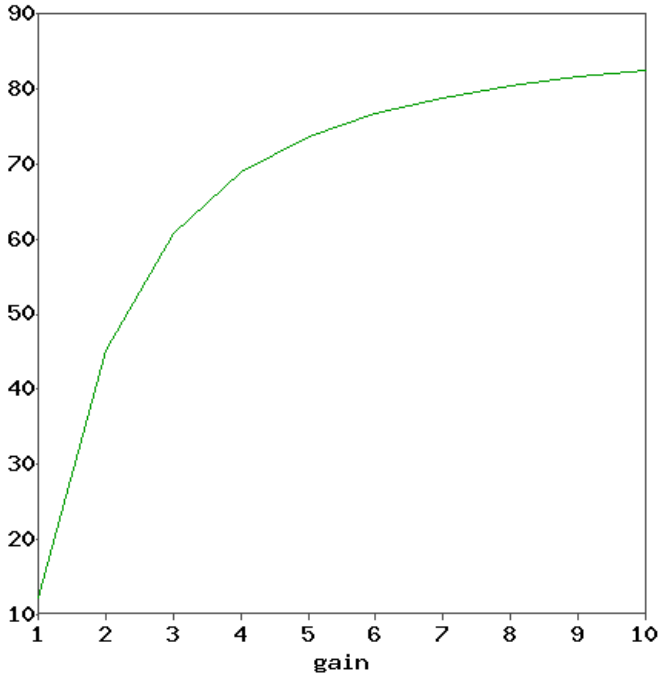

Figure 4-17: Sweep of amplifier small signal phase margin over gain

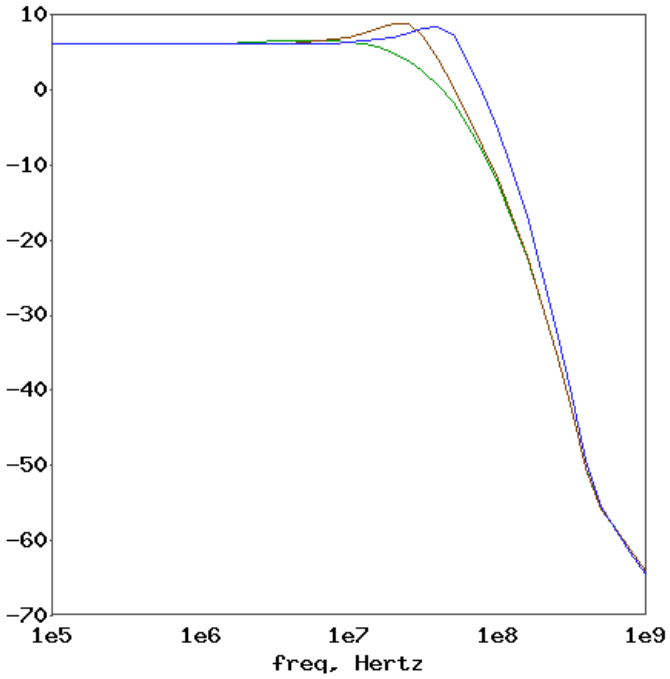

Figure 4-18: Magnitude Bode plot with varied C_L; Green - C_L = 100 pF, Brown - C_L = 1000 pF, Blue - C_L = 10000 pF

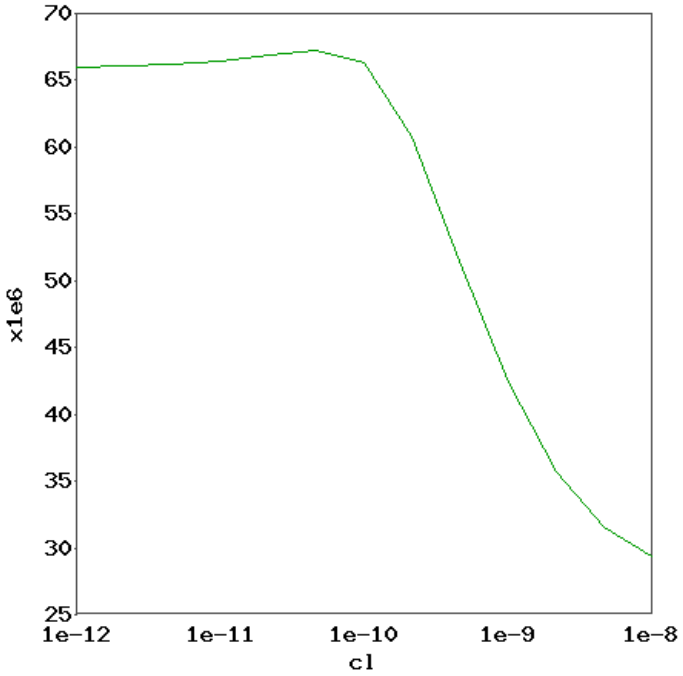

Figure 4-19: Sweep of amplifier small signal bandwidth over strictly capacitive load

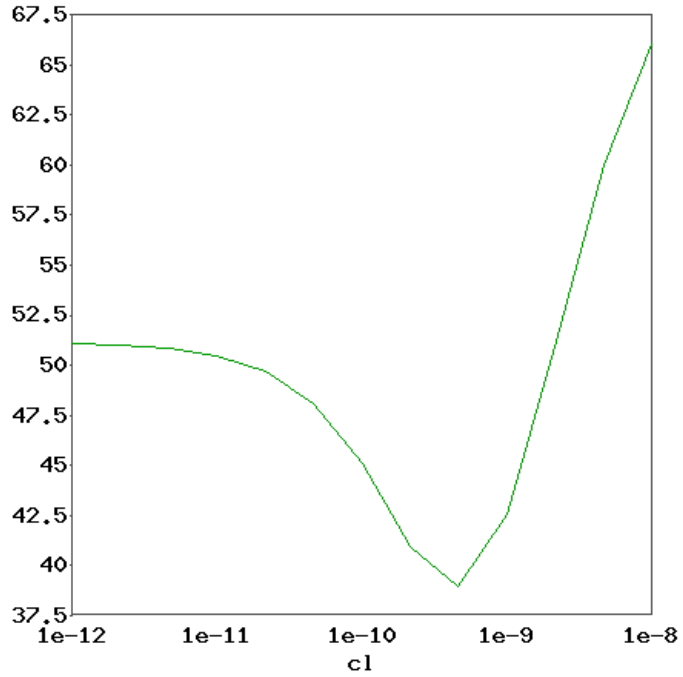

Figure 4-20: Sweep of amplifier small signal phase margin over strictly capacitive load

4.3.5 Noise analysis

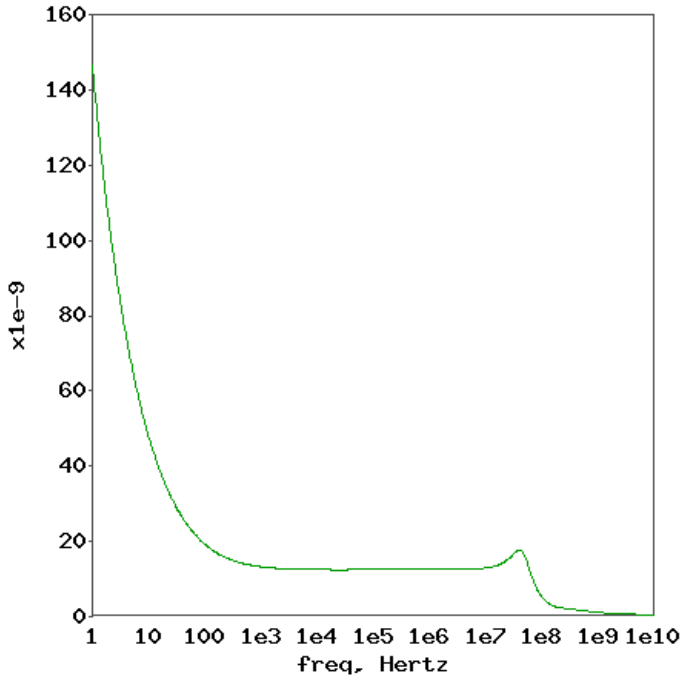

Figure 4-21: Sweep of total output voltage noise over frequency

At 100 kHz the total output voltage noise is **24.71** $nV/\sqrt{Hz}$. A component-based noise analysis tells us that the majority of the noise is contributed by emitter degeneration resistors in the current mirrors driving the output stage. Sadly we cannot make these resistors larger to mitigate the noise contribution because this would unnecessarily cut into our output voltage headroom. The input-referred voltage noise is **12.13** $nV/\sqrt{Hz}$ at 100 kHz, and the input current noise is **2.7** $pA/\sqrt{Hz}$ at 100 kHz.

4.3.6 CMRR

At low frequency (DC) the common mode rejection ratio is **88.05 dB**. The results of this simulation are shown in Figure 4-22.

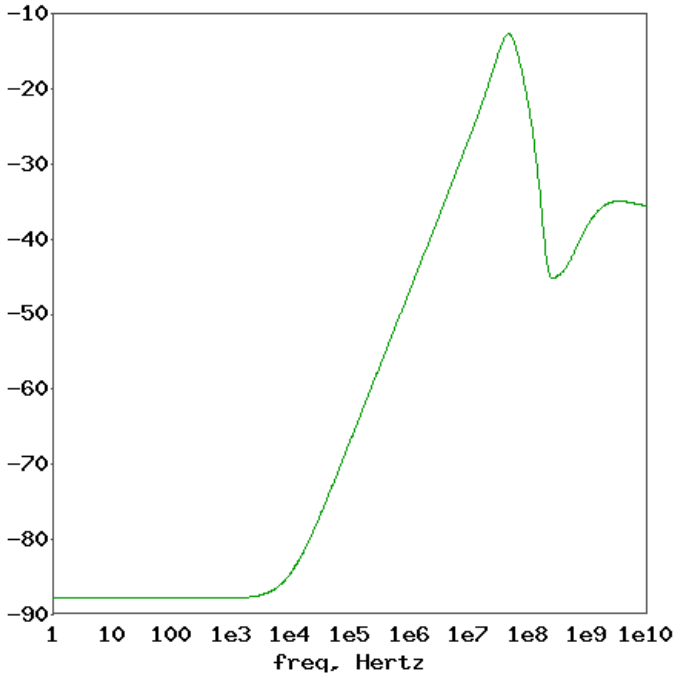

Figure 4-22: Sweep of CMRR over frequency

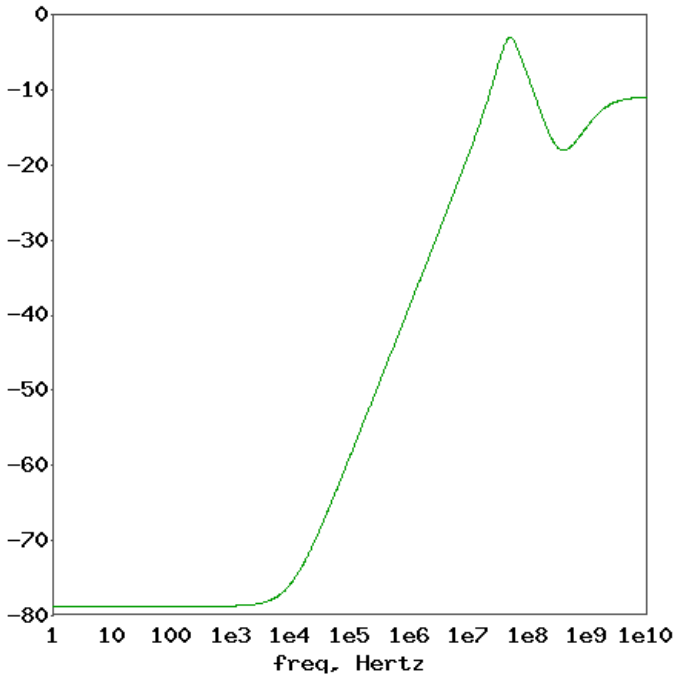

Figure 4-23: Sweep of PSRR over frequency

4.3.7 PSRR

At low frequency (DC) the power supply rejection ratio is **78.93 dB**. The results of this simulation are shown in Figure 4-23.

4.4 Amplifier transient performance

4.4.1 Pulse signal characteristics

In the standard gain of 2 configuration we drive an input voltage pulse with a voltage swing of 10 Volts and a slew rate of 2000 V/μs.

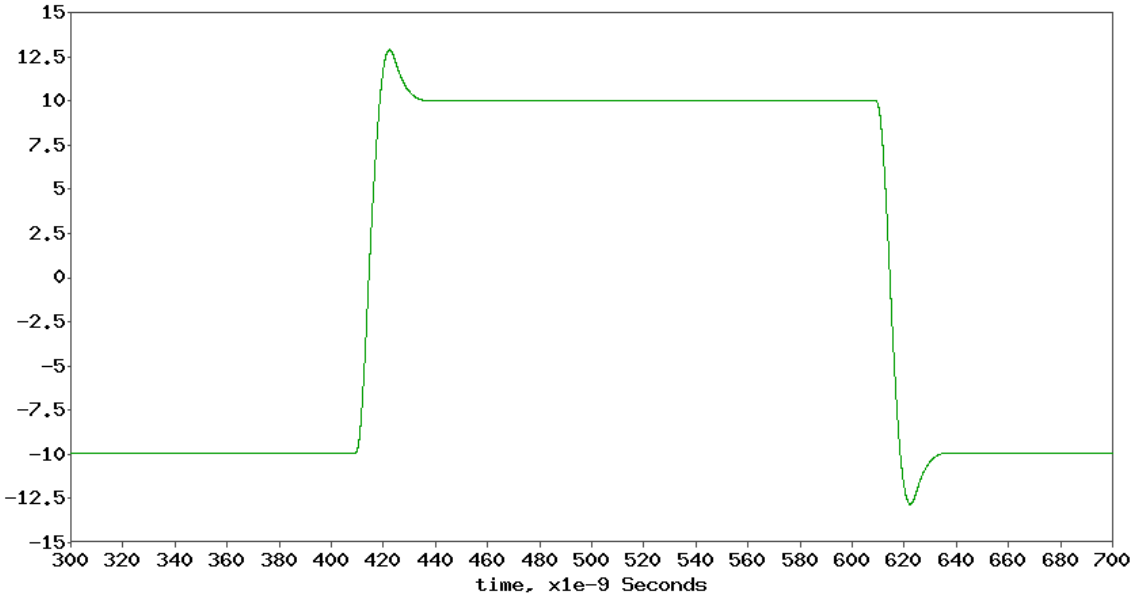

Figure 4-24: Time domain output pulse

Our output signal is a voltage pulse with amplitude of 10 Volts. The total time it takes to slew and settle is 37 ns for the rising edge, and the 10% to 90% mean slew rate is 2609 V/μs. For the falling edge the transistor time is 38 ns, and the 90% to 10% mean slew rate is 2683 V/μs.

This derivative waveform tells us that our peak slew rate is **3070** $V/\mu s$.

For kicks I speed the input signal up and drive the output voltage close to the headroom limitations of the part.

The peak slew rate of the part when the signal is stepping up is 4696 V/μs. When the signal is ramping down the slew rate caps at 5237 V/μs.

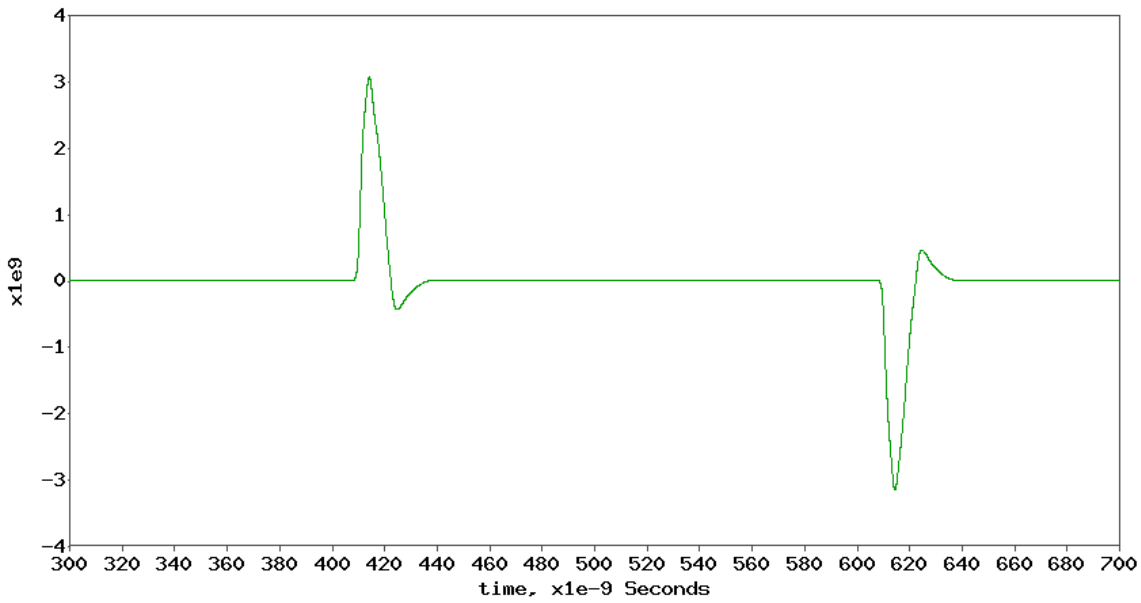

Figure 4-25: Time domain output voltage slew rate

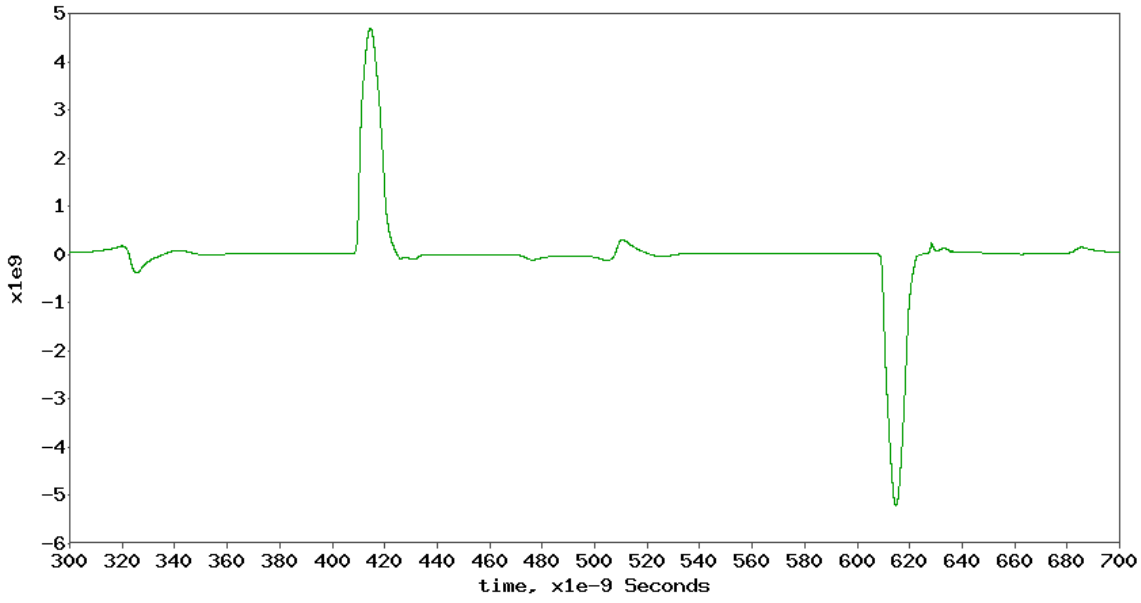

Figure 4-26: Maximum slew capacity of amplifier

4.4.2 Sinusoid signal characteristics

Driving a large signal voltage sinusoid with ideal output amplitude of 20 V_{PP}, at the bandwidth of the part the output will swing at roughly 70% of this: 14 V_{PP}.

Experimentally we find the large signal bandwidth frequency to be **68 MHz**.

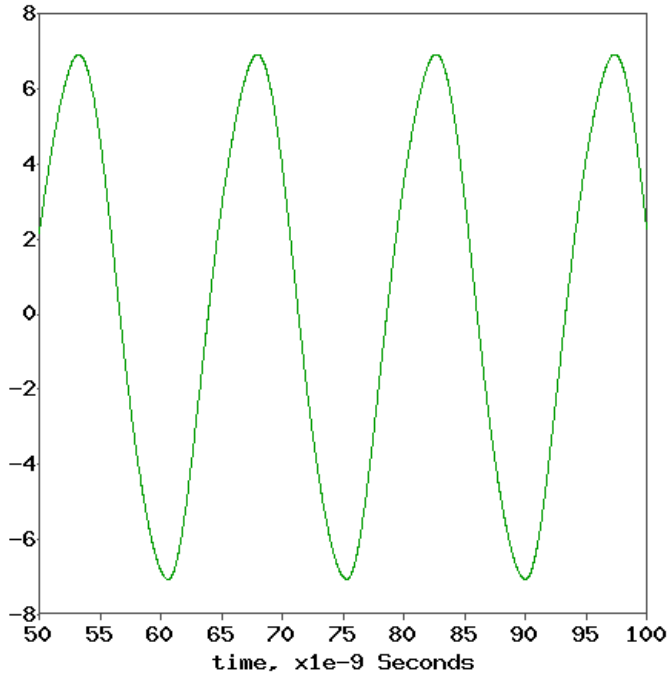

Figure 4-27: Output sinusoid at large signal (20 V_{PP}) bandwidth

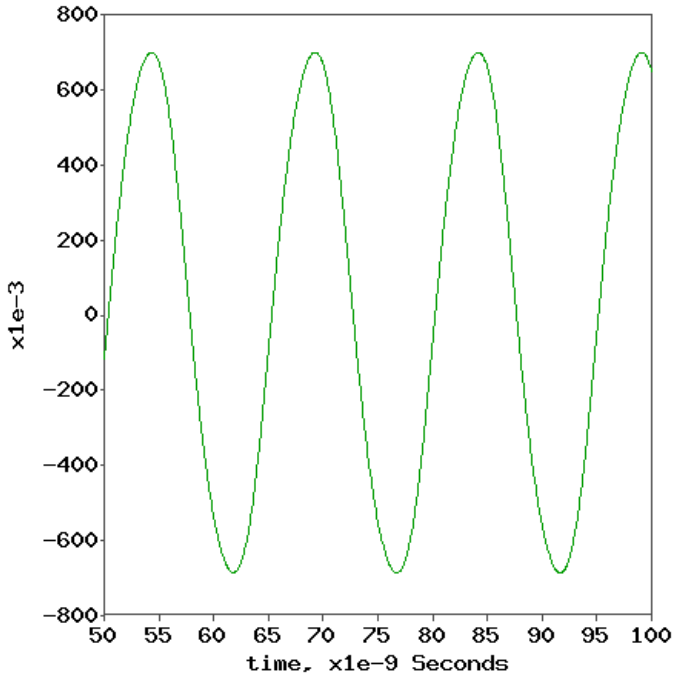

Figure 4-28: Output sinusoid at small signal (1 V_{PP}) bandwidth

Our small amplitude (target 1 V_{PP}) bandwidth is roughly the same as the large signal bandwidth with a frequency of **67 MHz**. In normal amplifiers this would

be higher than the large signal bandwidth but we have our ”boosting” circuit extending the swing potential of the output signal at the large amplitude sinusoid bandwidth whereas it is not kicking in in the case of the small amplitude signal.

4.4.3 Distortion

We measure the frequency-component total harmonic distortion present in large signal sinusoid voltage signals.

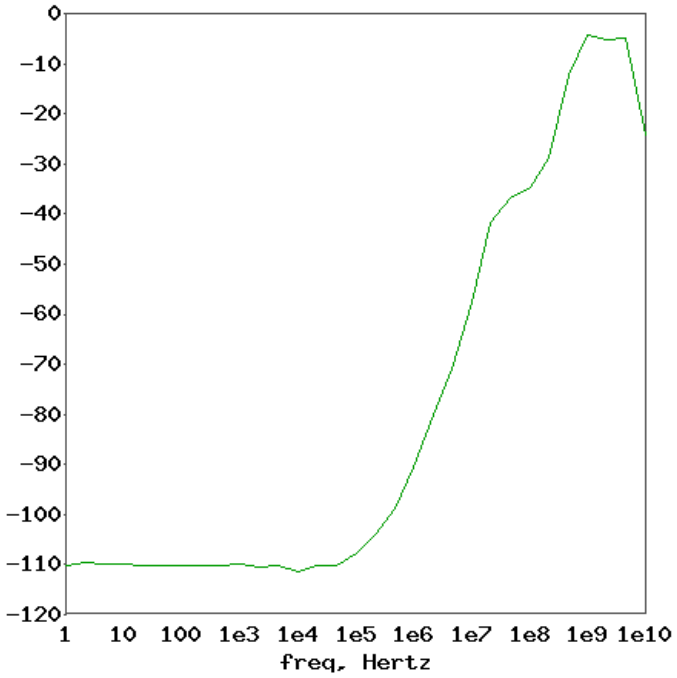

Figure 4-29: Second order total harmonic distortion as a function of frequency

THD2 represents the even mode distortion present in the amplifier. A sweep of THD2 as a function of frequency can be seen in Figure 4-29.

THD3 represents the distortion present acting on odd functions. A sweep of THD3 as a function of frequency can be seen in Figure 4-30.

Pertinent total hardmonic distortion values is shown in Table 4.1.

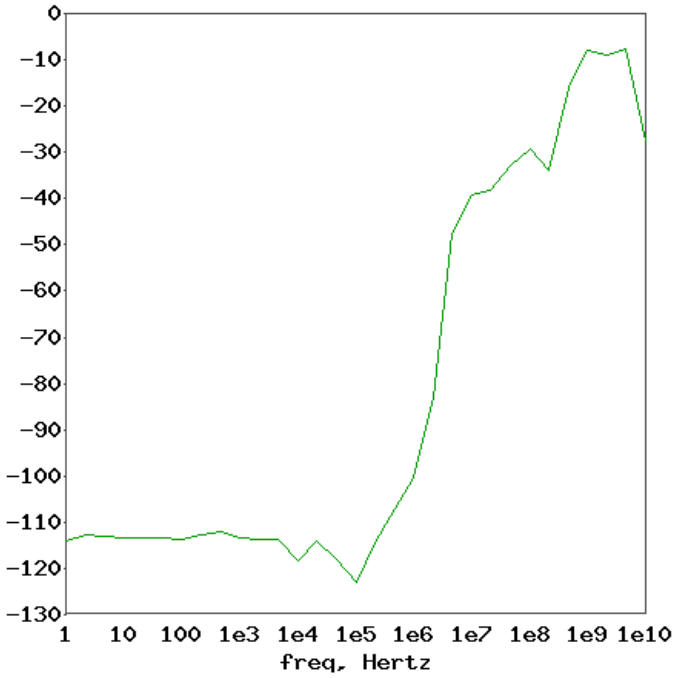

Figure 4-30: Third order total harmonic distortion as a function of frequency

Table 4.1: Total harmonic distortion at key frequencies

	THD2	THD3
100 kHz	-107.8 dB	-123.3 dB
1 MHz	-90.66 dB	-100.8 dB
10 MHz	-57.83 dB	-39.27 dB
100 MHz	-41.06 dB	-43.56 dB

4.5 Features

The features implemented in this amplifier allow for capabilities which require different means of evaluation than the simple evaluation of the amplifier's response to generic DC, AC, or small signal inputs. In order to establish the efficacy of these features, we subject each individually to an analysis of its individual merits.

4.5.1 Configurable g_m

Recall that our input stage transconductance is configurable through a resistor between the two diamonds in the H-Bridge: R_I. This value can be tweaked to adjust the bandwidth-stability tradeoff of the amplifier for a given configuration. As we saw in the AC analysis, changing the gain of a particular amplifier feedback network or changing the nature of the load will cause the bandwidth the change, and the phase margin accordingly. In a scenario where the g_m is fixed, the circuit user is helpless, but this is not the case here.

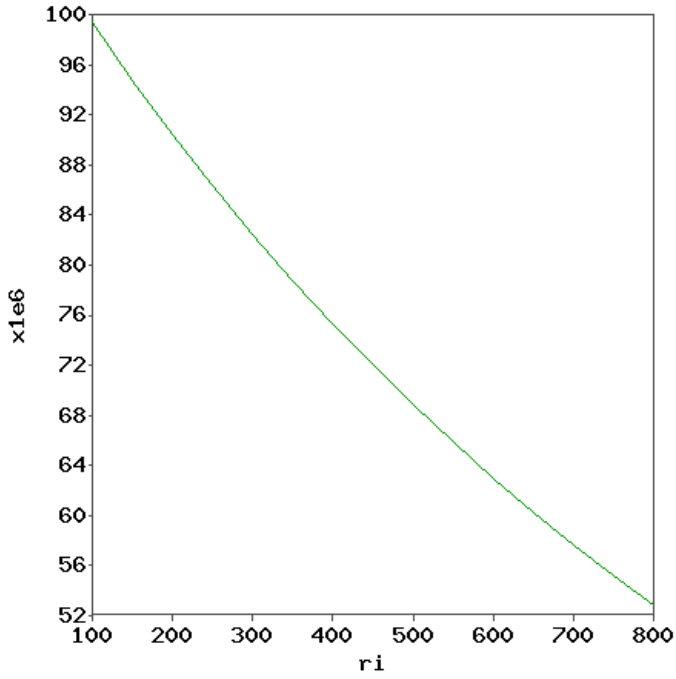

Figure 4-31: Sweep of small signal bandwidth as a function of R_I

Increasing R_I decreases the transconductance of the amplifier and its input stage, reducing the overall bandwidth.

Phase margin, however, increases with R_I because the stability of the overall amplifier configuration goes up as the transconductance decreases.

Figure 4-16 and Figure 4-17 demonstrated to us the detrimental small signal consequences of running the amplifier in higher gain configurations with fixed g_m. The bandwidth went down and the phase margin went up with gain.

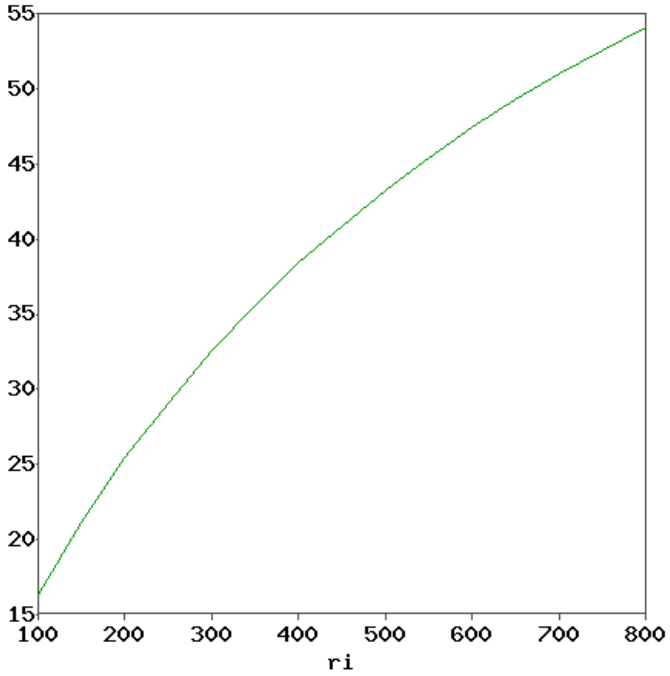

Figure 4-32: Sweep of phase margin as a function of R_I

With the ability to adjust g_m, however, we can normalize other gain configurations to 45 degrees of phase margin by adjusting R_I:

Table 4.2: Small signal characteristics versus gain, normalized by R_I

Gain	R_F	R_G	R_I	Phase Margin	Bandwidth
2	500 Ω	500 Ω	541 Ω	45.01°	66.29 MHz
3	500 Ω	250 Ω	202 Ω	45.03°	72.2 MHz
4	500 Ω	166.67 Ω	46 Ω	45.04°	76.41 MHz

A gain of 4 is the highest gain configuration we can use if we wish to keep the phase margin at 45°. The effects of decreasing R_I are limited by output R_E of devices in the diamond buffers in the input stage as well as by emitter degeneration resistors.

The same logic can be applied to normalize changes in bandwidth and phase margin due to the load.

4.5.2 Disjoint supplies

As mentioned under DC results, the total quiescent current draw of the part is 20.49 mA. In a gain of 2 configuration using default parameters the input set of supply rails (containing the input stage and mirrors along with all supporting circuits) draws 9.47 mA, 46.2% of the total current, , while the output set of supply rails draws 11.02 mA, 53.8% of the total current draw.

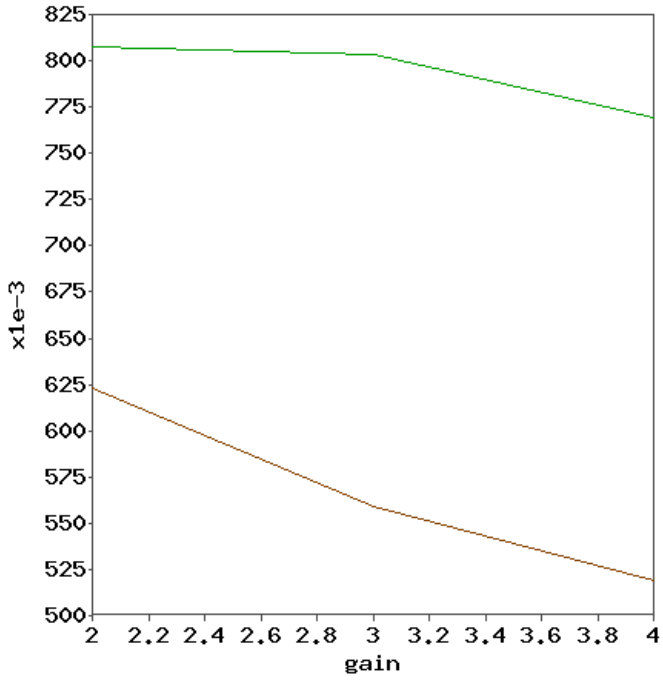

Figure 4-33: Quiescent power draw as a function of gain; Green - Unified supplies, Brown - Disjoint supplies

In this implementation we apply disjoint supply rails which scale proportionally with the gain of the amplifier. The supply rails are not tightly constricted to the headroom limit but rather are normalized to an output supply range of 40 V and a signal swing of 20 V. This is an inefficient but realistic implementation.

At a gain of 2, we save 185 mW of power by utilizing disjoint supply rails, at a gain of 3 we save 244.7 mW of power, and at a gain of 4 we save 250.6 mW of power. This validates the assertion made earlier that this implementation helps more at higher gain configurations.

At a gain of 2 we save 22.9% of the power burned in the amplifier at DC, at a

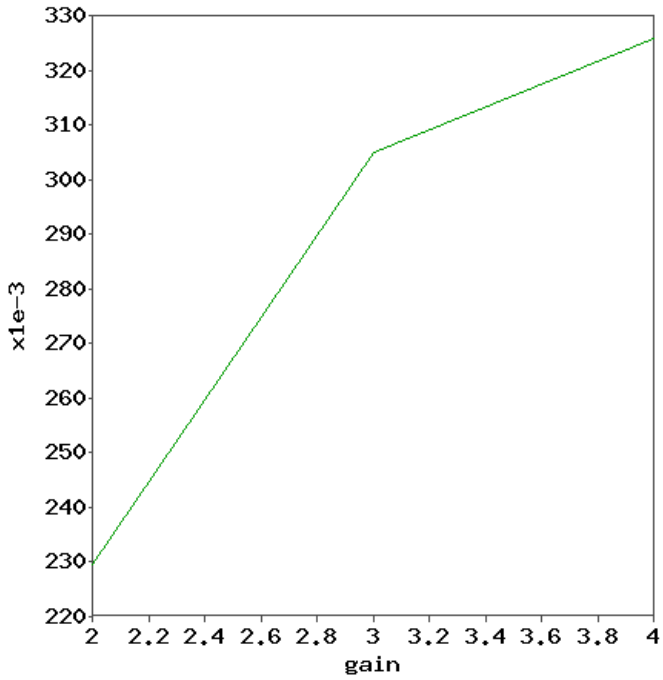

Figure 4-34: Fraction of total power saved by disjoint rails

gain of 3 we save 30.5% of the total power, and at a gain of 4 we save 32.6% of the total power.

4.5.3 Current limiting

The current limiting functionality of the amplifier is shown as a proof of concept. The necessity for high output current drive is created by using a very low impedance load. There are a vast number of ways this circuit could be tuned for better precision (to compensate for differences between NPN and PNP devices, sensing errors, differences in current gain, output impedances and so forth), but this is not prioritized in this demonstration. Here we show the effects of the current limiting in action, emphasizing configurability and limitations of the feedback loop.

Initially we establish a 1 Ampere current limit by using R_{ilimit} = 1 kΩ. We input a slow 10 V/μs ramp simply to test the low frequency characteristics of the circuit. We use a very small output impedance of 10 Ω.

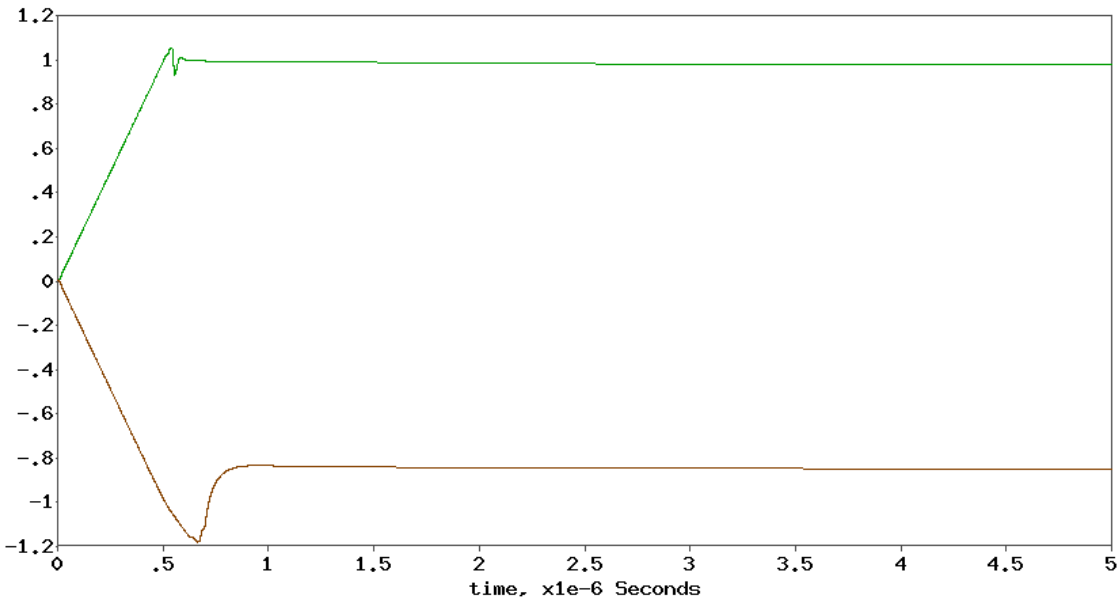

Figure 4-35: 1 Ampere current limit; Green - Output source current, Brown - Output sink current

The source current peaks to 1.05 Amperes before the H-Bridge turns off and we achieve the differential pair input stage. We explicitly see this transition in the major trough between when the output current begins coming down to zero and subsequently recovers before flattening out. The output source current settles to 977 mA. The sink current overshoots much harder, reaching -1.182 Amperes and finally settling at -855 mA.

By setting R_{ilimit} to 2kΩ, the current limit is now set to half an Ampere. The source current overshoots to 567 mA and settles at 512.9 mA. The sink current once again incurs a worse overshoot, up to -659.8 mA, and settles at 570.4 mA.

Finally for good measure we look at a lower current limit, 200 mA. This corresponds to R_{ilimit} = 5kΩ.

Understandably this implementation becomes must less precise at lower currents. The source current peaks at 298 mA before settling at 255 mA. The sink current peaks down to -353.2 mA and subsequently settles at -288 mA.

As a disclaimer we mentioned that there are many ways of circumventing the current limit imposed by this circuit, and this is certainly true. Increasing the slew

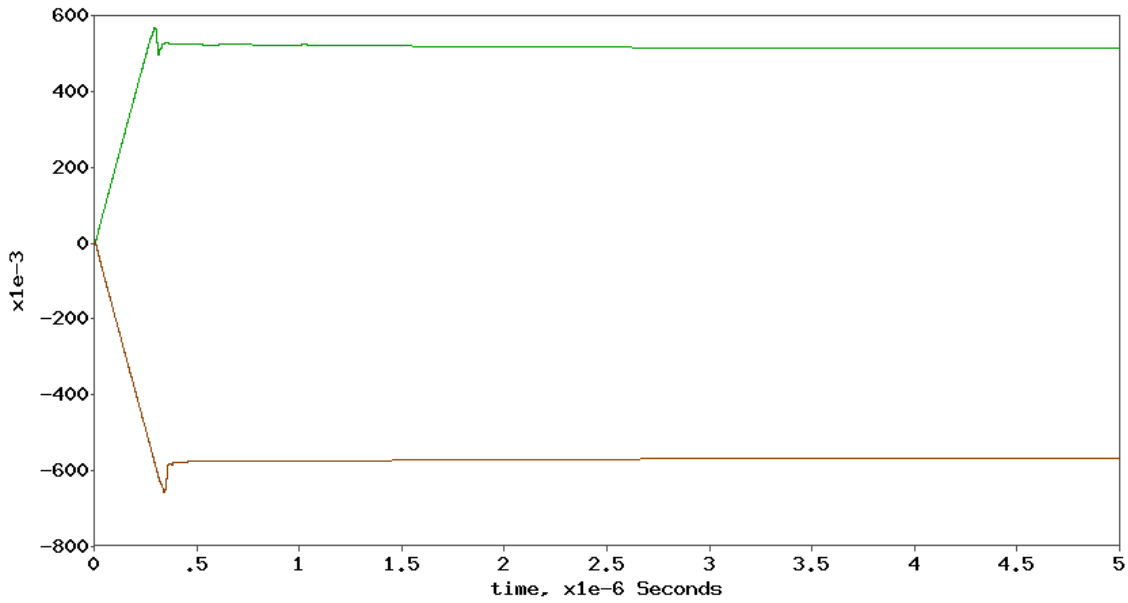

Figure 4-36: 500 mA current limit; Green - Output source current, Brown - Output sink current

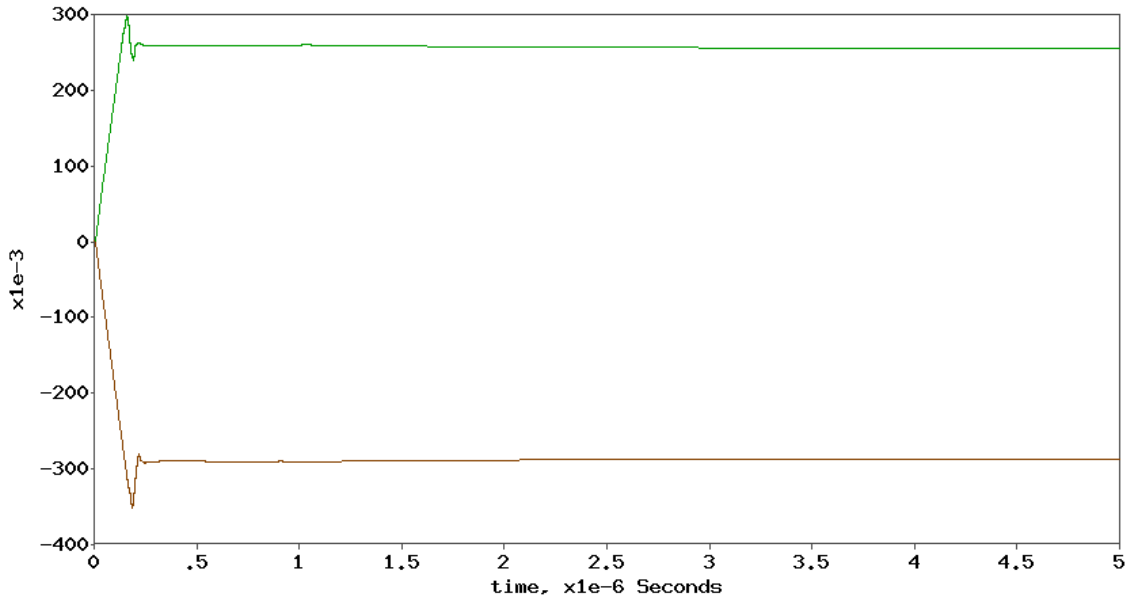

Figure 4-37: 200 mA current limit; Green - Output source current, Brown - Output sink current

rate at the output (by increasing the slew rate of the input signal) is a major contributor, as is decreasing the load impedance.

In the former simulations we used a slow input drive with an output slew rate of 20 V/μs. Here we can already see what happens when thee slew rate is increased

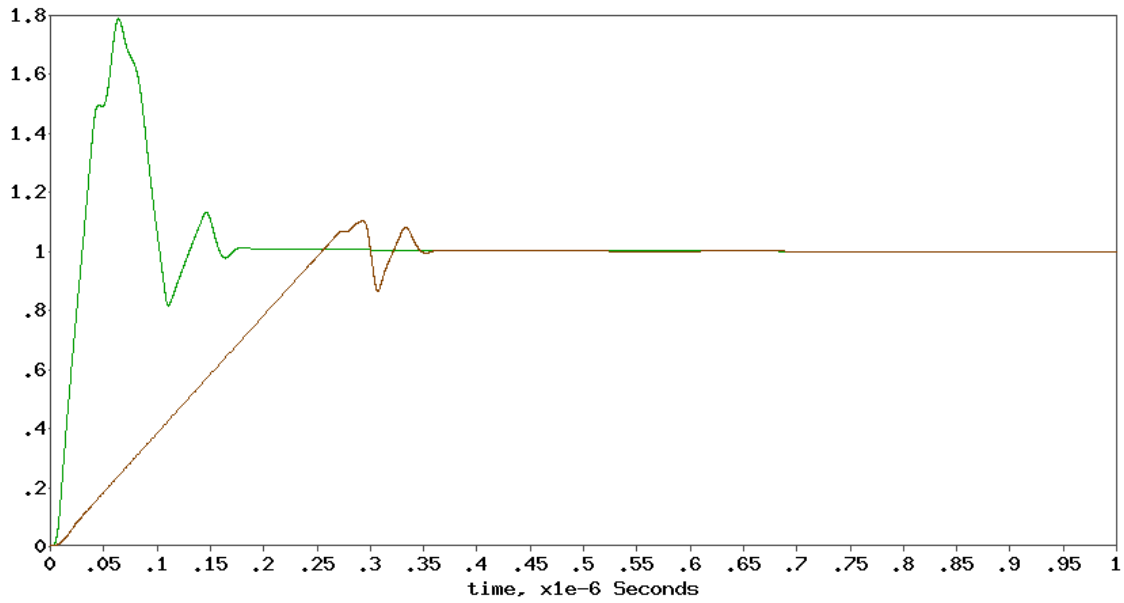

Figure 4-38: Variable slew rate 1 Ampere current limit; Green - 200 V/μs, Brown - 20 V/μs

by a factor of ten: the abhorred $\Delta I_{overshoot}$ appears. This is a significant (80%) current overshoot of the limit which could easily damage or destroy the part, and this slew rate is still far far below the bandwidth and slew limitations of the part. Fortunately, the values settle to the same current which is the intended functionality of the part.

Finally, we mentioned that the turn-on of the alternate input stage could be inhibited entirely to force the amplifier to shut off entirely. This behavior is shown in Figure 4-39.

Through the use of a single pin one can inhibit the turn-on of the compound differential pair alternate input stuff. Thus when the state of current limiting is entered, the amplifier will shut-off the H-Bridge and no other input stage will turn on; the amplifier will turn off and will remain off until the latch is reset.

4.5.4 "Boosting" validation

To demonstrate the efficacy of "boosting" as implemented in this circuit, we demonstrate the transient response of the amplifier both with and without boosting.

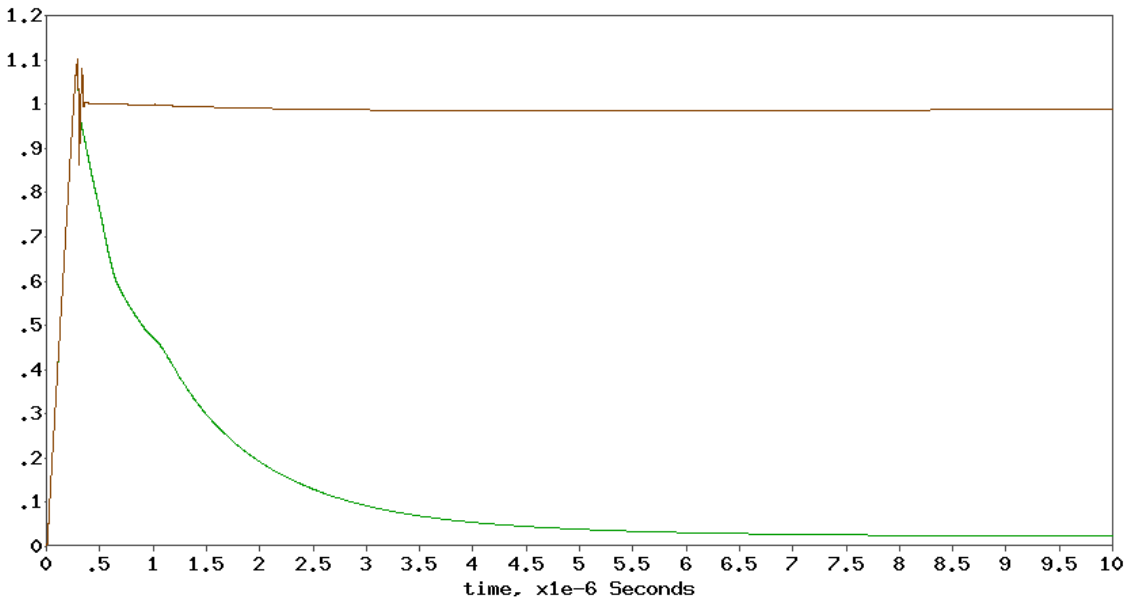

Figure 4-39: Current limiting modes of operation; Green - Shut-off mode, Brown - Default operation

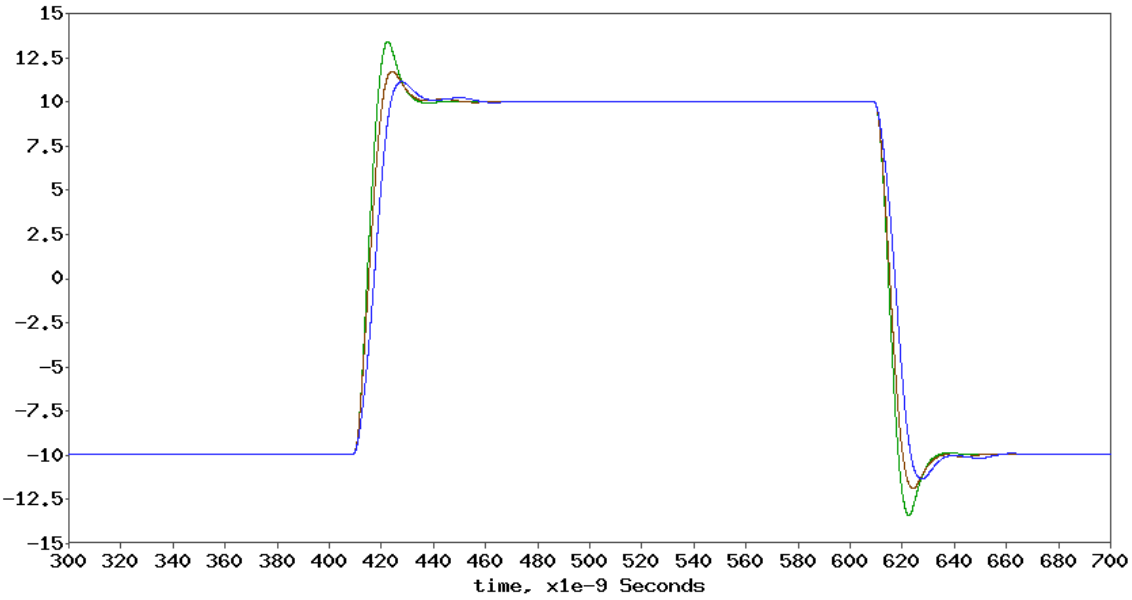

Figure 4-40: Time domain pulse response; Green - Final boosting implementation with current inject into signal path, Brown - Boosting implementation with additional current used to supplement bias, Blue - No boosting

The time domain pulse response in Figure 4-40 shows the effectiveness of current boosting because it can be clearly seen that the rising and falling edges are much more rapid and responsive in cases where boosting is applied. One down-

side to this speeding up of the amplifier is that the pulses appear as if they were in a system with lower phase margin; the pulse transistions are peakier and the value overshoots more. However, although it is not clear perhaps in the resolution presented in this paper, the boosted pulses settle more quickly than the unboosted system.

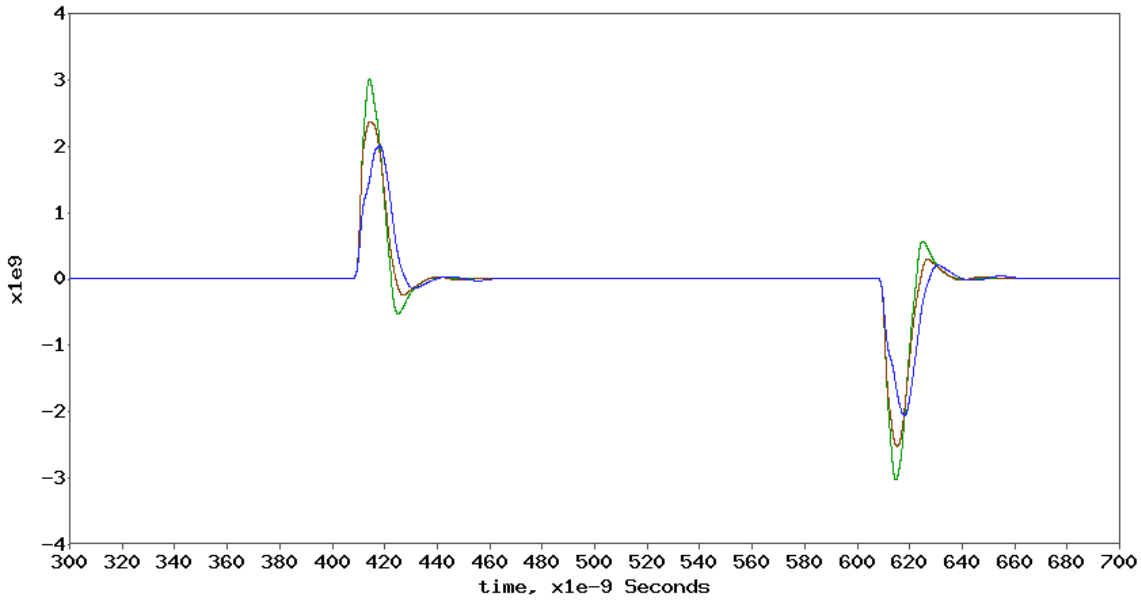

Figure 4-41: Slew rate during pulse response; Green - Final boosting implementation with current injected into signal path, Brown - Boosting implementation with additional current used to supplement bias, Blue - No boosting

A mapping of the slew rate of the amplifier in boosting versus non boosting cases in Figure 4-41 demonstrates the sheer amount of slew rate unlocked by the simple adjustment. For the rising edge the peak slew rate goes from 2000 V/μs unboosted to 3010 V/μs boosted through the signal path. Likewise the falling edge's peak slew rate jumps from 2074 V/μs to 3044 V/μs. In both of these cases it's a 50% increase in peak slew rate; not bad for a circuit that utilizes only a couple transistors!

Also the width of the boosted slew rates is thinner, further showing that the boosted transient response is smoother and more responsive.

The final key point of note here is that the slew rate gained between "boosting" by injecting current into the signal path versus simply driving more current to the

input bias is equally as significant as boosting versus not boosting at all.

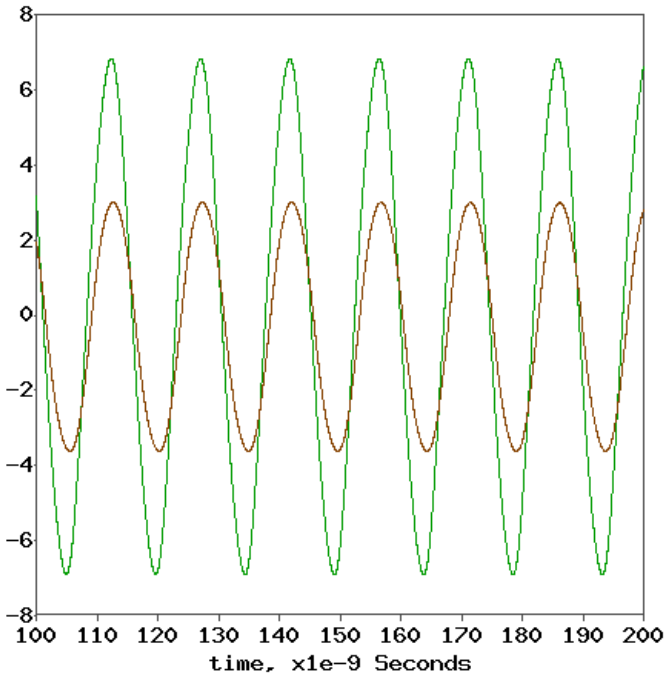

Figure 4-42: 68 MHz 20 V_{PP} sinusoid; Green - Final boosting implementation with current inject into signal path, Brown - No boosting

I made a claim earlier that boosting is giving us more large signal bandwidth as well, and this is evaluated in simulation in Figure 4-42. Taking our amplifier which has a large signal bandwidth of 68 MHz, I subsequently disabled boosting. The difference in large signal response is nontrivial; the additional current in the signal path is heavily facilitating the slew of the amplifier which is especially relevant when driving large amplitude sinusoids. The unboosted circuit has a large signal bandwidth of roughly 48 MHz; "boosting" pushed the large signal bandwidth out by an additional 20 MHz.

We owe a lot of the performance specifications of this amplifier to the improvements brought about by this boosting circuit, which allows us to run at a lower quiescent current while still retaining decent performance specifications at or near the limit of the process.

4.6 Conclusion

In this thesis project we successfully delved into multiple aspects of amplifier design, producing a part which is both functional and highly unique. Recall the spiritual design objectives of the project:

1. occupies a specialized subset of the amplifier domain
2. pushes the boundaries of amplifier specifications
3. uses a novel system level architecture
4. implements features which add unique functionality

Based on the specifications presented, this amplifier is a cutting edge amplifier which occupies a unique niche in the high output current domain. It achieves high current drive and high voltage operation but despite the high power applications of the part manages to retain very low DC errors. There are very few commercially available amplifiers capable of driving a full Ampere of current, and those that do exist, such as the LT1210, have glaring shortcomings (low slew rate/bandwidth) which are adequately accounted for in this amplifier's robust set of specifications.

As a successor to the upcoming part ADA4870 from *Analog Devices Inc.*, this amplifier makes tremendous strides in numerous areas, managing to meet or beat the performance specifications of the ADA4870 at a substantially lower quiescent current. The advances in performance can be attributed to improvements in sizing methods for the part as well as our "boosting" circuit. This part achieves lower input-referred offset, lower CMRR, lower PSRR, lower cumulative voltage noise, lower input headroom, and lower distortion numbers than the ADA4870, which are a function of the amplifier architecture and design techniques.

The unique topology implemented in this amplifier, based on symmetry and base current cancellation, allows the amplifier presented herein to have extremely low DC error. Perhaps this is not the most important attribute for a high power amplifier, but many of the methods introduced and exposed here may perhaps

find a more suitable home in a high precision amplifier. The concepts are there and could be equivalently applied in any process, for an amplifier geared toward any application. The system level architecture, both in the signal path and in the supporting circuits, is simple and straightforward which made it incredibly feasible to implement and execute all the features that I found necessary to embellish and supplement the performance of this part.

Every feature presented in this amplifier is strictly unique and achieves functionality which augments the capacity of the part in a unique way. g_m configurability allows the circuit user to break free from the chains of gain-bandwidth constancy to allow for tuning the frequency-dependent attributes of the amplifier, permitting use in a greater variety of applications and configurations. Splitting of the supply rails offers a great deal of potential for power conservation and is a refreshing divergence from a setup common to virtually all existing amplifiers. The current limiting mechanism, albeit rife with limitations and shortcomings, proved to be an excellent exercise in the application of analog principles toward the design of a more complex circuit solution. Finally, the "boosting" circuit, which has been demonstrated to heavily augment the functionality of the part at little cost, is effective but needs to be thoroughly evaluated to understand its limitations and consequences.

Future work on this part will involve layout and production of a part based on one of the revisions looked at during the design process, a lower power variant of the ADA4870. Subsequently it will be fabricated at *Analog Devices, Inc.* in Wilmington, MA.

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