Silicon CMOS Ohmic Contact Technology for Contacting III-V Compound Materials

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Silicon (Si)-encapsulated III-V compound (III-V) device layers enable Si-complementary metal-oxide semiconductor (CMOS) friendly ohmic contact formation to III-V compound devices, allowing for the ultimate seamless planar integration of III-V and Si CMOS devices in a common fabrication infrastructure. A method of making ohmic contacts to buried III-V films using silicide metallurgies has been established. NiSi/Si/III-V dual heterojunction contact structures are found to be optimal for integration. These structures allow contact resistivities to be controlled by Si/III-V interfaces and eliminate interactions between the buried III-V device and metal layers. Using a modified transmission line method (TLM) test structure fabricated using standard CMOS processing techniques, the specific contact resistivities of Si/GaAs and Si/In$_x$Ga$_{1-x}$As interfaces are extracted. The relationship between specific contact resistivity and heterojunction barrier width is considered. Among the structures tested in this work, p-type Si/GaAs and n-type Si/In$_x$Ga$_{1-x}$As yielded the lowest contact resistivities. Using the p-type Si/GaAs interface, a GaAs/Al$_x$Ga$_{1-x}$As laser with NiSi top contact is demonstrated, confirming the feasibility of NiSi/Si/III-V contact structures for III-V devices.

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Integration of III-V compound (III-V) semiconductors with Si complementary metal-oxide semiconductor (CMOS) friendly ohmic semiconductor (CMOS) friendly ohmic contact formation to III-V compound devices, allowing for the ultimate seamless planar integration of III-V and Si CMOS devices in a common fabrication infrastructure. A method of making ohmic contacts to buried III-V films using silicide metallurgies has been established. NiSi/Si/III-V dual heterojunction contact structures are found to be optimal for integration. These structures allow contact resistivities to be controlled by Si/III-V interfaces and eliminate interactions between the buried III-V device and metal layers. Using a modified transmission line method (TLM) test structure fabricated using standard CMOS processing techniques, the specific contact resistivities of Si/GaAs and Si/In$_x$Ga$_{1-x}$As interfaces are extracted. The relationship between specific contact resistivity and heterojunction barrier width is considered. Among the structures tested in this work, p-type Si/GaAs and n-type Si/In$_x$Ga$_{1-x}$As yielded the lowest contact resistivities. Using the p-type Si/GaAs interface, a GaAs/Al$_x$Ga$_{1-x}$As laser with NiSi top contact is demonstrated, confirming the feasibility of NiSi/Si/III-V contact structures for III-V devices.

In order to isolate the effects of contact metallization, nickel silicide contacts were made to Si-encapsulation layers grown epitaxially on bulk III-V substrates. Metallocrystal chemical vapor deposition (MOCVD) was used for epitaxial growth in this work because of its scalability and high throughput. A Thomas Swan/Aixtron close-coupled showerhead reactor with the unique capability of growing compound semiconductors and group IV materials in the same chamber was used. Silane (SiH$_4$) and germane (GeH$_4$) were the precursors for group IV growth and are doped with mixtures of phosphine (PH$_3$) or diborane (B$_2$H$_6$) diluted in hydrogen. The precursors for compound semiconductor growth relevant to this work are trimethylgallium (TMGa), trimethylindium (TMIn), trimethylaluminum (TMAI), and arsine (AsH$_3$), with dimethylzinc (DMZn) and disilane (Si$_2$H$_6$) as the p- and n-type dopants, respectively.

The contact structures were grown on epi-ready semi-insulating (100) GaAs and (100) InP wafers. Hall Effect measurements of single layer films grown on undoped substrates (for example doped GaAs/semi-insulating GaAs wafer or doped Si/undoped homoepitaxial GaAs/semi-insulating GaAs wafer) were conducted to confirm active carrier concentrations in each of the layers of interest.

Contacts to GaAs were fabricated with degenerately doped Si on degenerately doped GaAs homoepitaxial layers whereas contacts to In$_x$Ga$_{1-x}$As were fabricated with the following structure: degenerately doped Si/In$_x$Ga$_{1-x}$As/homoeptaxial In$_x$Ga$_{1-x}$As substrate. In$_{0.53}$Ga$_{0.47}$As was the composition chosen in this work because of its importance in electronic devices due to its lattice match with InP. The degenerate doping enables tunneling between the silicide and III-V films. All carrier concentrations are determined by Hall Effect measurements of single layer films grown on undoped substrates.

In the Si/GaAs structures, Si is grown on Ga-terminated GaAs surfaces, achieved by baking the GaAs substrate in N$_2$ without an AsH$_3$ overpressure for 2 minutes at 650 °C before introducing SiH$_4$, following the work of Bai, et al. for direct deposition of Ge on GaAs. The same procedure could not be applied to growth of Si on In$_{0.53}$Ga$_{0.47}$As due to In$_{0.53}$Ga$_{0.47}$As decomposition and In droplet formation. Instead, another technique employed by Bai, et al. was used. The In$_{0.53}$Ga$_{0.47}$As film was cooled to 400 °C under AsH$_3$ overpressure, and baked without the AsH$_3$ overpressure prior to SiH$_4$ introduction. Because SiH$_4$ decomposition at 400 °C is extremely low, the temperature was gradually raised to 650 °C at 1.7 °C/minute in the presence of

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The specific contact resistivity, $\rho_{c}$, is extracted for silicide ohmic contacts to n- and p-type GaAs and In$_{x}$Ga$_{1-x}$As films using the aforementioned optimal metallurgical structure. Determination of $\rho_{c}$ was based on the transmission line model (TLM). The traditional TLM structure was modified in such a way as to allow determination of NiSi to III-V film contact resistivity while maximizing CMOS processing compatibility. Si encapsulation layers and GaAs or In$_{x}$Ga$_{1-x}$As films were grown epitaxially on semi-insulating GaAs substrates in order to confine current flow to a degenerately doped channel layer. The fabrication process for these TLM test structures is detailed in Figure 1. Figure 1a shows the fabrication sequence on Si control structures and (b) NiSi/Si/III-V dual junction structures. (1,2) Mesas and contact areas are defined through etching. (3) Front-sides of the wafers are encapsulated in blanket PECVD SiO$_2$ and holes are etched in the SiO$_2$ to define silicide contact pads. (4) Blanket Ni is E-beam evaporated onto the samples and the samples are annealed to form nickel silicid in the SiO$_2$ holes. Unreacted Ni is removed in a wet etch. (5) Finally, E-beam evaporated Al is deposited and patterned.

SiH$_4$ gas flow. This method avoids decomposition of the In$_{0.53}$Ga$_{0.47}$As film and produces a continuous Si thin film encapsulated surface. Silicide metallurgies are a function of metal thickness and anneal temperature. In the first part of this work, optimal contact metallurgies for III-V/Si integration were evaluated by considering structural and electrical properties of different silicide structures constructed on degenerately doped n-type Si films/n-type GaAs substrates. These films were grown on n-type GaAs substrates to enable conduction through the wafer and isolate the characteristics of a single NiSi to GaAs contact. Blanket back-side contact to these structures was made with a NiGeAu alloy, a traditional III-V metallization material. Nickel was E-beam evaporated on the front-side of the wafers and patterned in a lift-off process. Various thicknesses of Ni were deposited, which, after rapid thermal anneal (RTA), resulted in varying silicide reaction depths. For contact isolation, the unreacted Si and degenerately doped GaAs were etched, with the silicide serving as a self-aligned mask. For this part of the work, the Si thickness was 900 Å and target Ni thicknesses were 200 Å, 600 Å and 900 Å.

I-V characteristics were measured through the wafers in order to gain a qualitative understanding of whether the junctions between each silicide metallurgy and GaAs produced ohmic or rectifying behavior. The silicide was probed directly without the aid of an Al current-spread layer for fabrication simplicity. Metallurgical properties of these silicides were determined with cross-sectional transmission electron microscopy (TEM), X-ray diffraction (XRD) and secondary ion mass spectroscopy (SIMS) analysis of unpatterned silicide samples. 20-40 XRD scans were taken between 20 of 30° and 60°; diffraction peaks were compared against tabulated powder diffraction files for phase identification. Through this analysis, the optimal metallurgical structure for integration was identified.

Using the optimal p-type contact with the lowest $\rho_{c}$, a quantum well (QW) graded-index separate confinement heterostructure (GRIN-SCH) GaAs/AlGaAs oxide-stripe laser with CMOS-compatible silicide front-side contact was demonstrated. The laser structure is illustrated in Figure 2 and has 1.5 μm cladding layers (Al$_{0.5}$Ga$_{0.5}$As), 125 nm undoped GRIN-SCH layers (Al$_{0.5}$Ga$_{0.5}$As to Al$_{0.3}$Ga$_{0.7}$As), followed by a 25 nm undoped SCH (Al$_{0.5}$Ga$_{0.5}$As), and a 10 nm undoped quantum well (GaAs). It is then capped with degenerately doped GaAs and Si to enable silicide contact formation. The target doping for the cladding layers was 1e18 cm$^{-3}$ and the laser structure was grown on n-type GaAs substrates in order to simplify device fabrication and to allow for a front-to-back contacted device. (For fabrication simplicity, back side contact was made using NiGeAu, a traditional III-V metallurgy)

Figure 1. Schematic of TLM fabrication sequence for (a) NiSi/Si control structures and (b) NiSi/Si/III-V dual junction structures. (1,2) Mesas and contact areas are defined through etching. (3) Front-sides of the wafers are encapsulated in blanket PECVD SiO$_2$ and holes are etched in the SiO$_2$ to define silicide contact pads. (4) Blanket Ni is E-beam evaporated onto the samples and the samples are annealed to form nickel silicid in the SiO$_2$ holes. Unreacted Ni is removed in a wet etch. (5) Finally, E-beam evaporated Al is deposited and patterned.

Figure 2. Schematic illustrating Si-encapsulated 851 nm GaAs/AlGaAs quantum well (QW) graded-index separate confinement heterostructure (GRIN-SCH) laser structure.

<table>
<thead>
<tr>
<th>Layer/Structure</th>
<th>Thickness/Composition</th>
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<tbody>
<tr>
<td>60nm p++ Si contact</td>
<td>280nm p++ GaAs contact</td>
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<tr>
<td>1500nm p Al$<em>{0.5}$Ga$</em>{0.5}$As cladding</td>
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<tr>
<td>125nm u.d. Al$<em>{0.5}$Ga$</em>{0.5}$As to Al$<em>{0.3}$Ga$</em>{0.7}$As GRIN-SCH</td>
<td>25nm u.d. Al$<em>{0.5}$Ga$</em>{0.5}$As SCH</td>
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<tr>
<td>10 nm u.d. GaAs QW</td>
<td>25nm u.d. Al$<em>{0.5}$Ga$</em>{0.5}$As SCH</td>
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<td>1500nm n Al$<em>{0.5}$Ga$</em>{0.5}$As cladding</td>
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n+ GaAs substrate
anti-reflective coatings on the facets. The front-side was probed directly with a tungsten probe tip whereas the back side was contacted through the solder.

Lasers were tested at room temperature without additional temperature control. A Melles Griot Model 06DL203A Diode Laser Driver provided the input current and Agilent 33250A Function Generator enabled pulsed operation. Optical output signals were collected with a multimode fiber coupled to one of the laser facets. Laser spectra were determined using an Ocean-Optics HR4000 CG-UV-NIR High Resolution Spectrometer. Laser power was measured with a Thor Labs PDA36A Si Amplified Photodetector. Because continuous mode laser operation saturated the photodetector power was measured in pulsed mode using a 2 μs pulse width and 0.2% duty cycle. The peak intensity of the power was recorded for each input current.

**Results**

A cross-sectional TEM image of Si-encapsulated GaAs is shown in Figure 3. N-type and p-type Si-encapsulated GaAs and In$_{0.53}$Ga$_{0.47}$As films look comparable, although with different degrees of surface roughness. The growth of Si on III-V is epitaxial, monocrystalline and continuous, despite high lattice mismatch between the two films. Carrier concentrations for the films used in this work, as determined by Hall Effect measurements, are shown in Figure 4. Degenerate doping levels were achieved in each of the films.

Cross-sectional TEM images of various silicide on n-type Si/GaAs films are shown in Figure 5, adapted from Pacella et al. With increasing thickness ratios of Ni:Si, the reaction depth of silicide into the Si/GaAs structure increases. At an initial Ni:Si thickness ratio of 2:9, only part of the Si reacts and the GaAs underneath appears unperturbed, as seen in Figure 5a for a film annealed at 450°C for 5 minutes. Two internal heterojunctions are formed (silicide/Si and Si/GaAs) and through-wafer I-V curves indicate that both junctions are ohmic. When Ni:Si thickness ratio is increased to 2:3 and annealed at 450°C for 5 minutes, all of the Si is consumed, as seen in Figure 5b. Ni:Si thickness ratio after rapid thermal anneal (RTA) at 450°C for 5 minutes and 1:1 Ni:Si after RTA at 600°C for 5 minutes, adapted from Pacella et al.

**Discussion**

Sil/III-V epitaxial structure.— The successful continuous epitaxial growth of Si on III-V films indicates that III-V films can be wholly encapsulated with Si. As noted previously, n-type Si caps have higher surface roughness than p-type Si caps. This roughness is consistent with previous observations and has been attributed to surface segregation of P atoms during growth. Micro-scale roughness should not, however, affect the ability to fabricate ohmic contacts. Carrier concentrations in the Si and III-V films are critically important to ohmic contact formation. It is especially important to determine if there is any cross-doping between the various epitaxial layers because Si is an n-type dopant for III-V films and group III and group V elements are p- and n-type dopants in Si respectively. Ga and As concentrations within Si films of two different growth rates are shown in Figure 6. These SIMS profiles are taken by topside sputtering through the Si layer. In Figure 6a, the growth rate of Si is 2.8 nm/s (this corresponds to the growth rate in undoped p- Si films) whereas in Figure 6b, the growth rate has been suppressed by a factor of 40 (this is for n+ Si). Ga concentrations in both samples are around 1e18 cm$^{-3}$ and may be the result of an exchange mechanism, as has been theorized for Ge on GaAs. It is interesting, however, to note that arsenic concentrations are much higher in films with faster Si growth rate. This data supports Bai, et al.’s theory that As incorporation is due to desorption of volatile As-containing compounds from the MOCVD reactor ambient. In this case, arsenic species remain from growth of the GaAs homoepitaxial layer and incorporates into Si growth. A reduced Si growth rate for the n+ Si film enables the As-containing species to be purged out of the system and suppresses arsenic incorporation into the silicon film. In order to lower arsenic incorporation in p-type Si films with faster growth rate, a reactor chamber purge might be implemented. Note that high arsenic concentrations have not affected the overall ability to degenerately dope Si films p-type, (the measured carrier concentrations in p-type Si were 1.90 ± 0.05e20 cm$^{-3}$). III-V structures that have been encapsulated with these Si films can then be migrated into CMOS fabs.

A SIMS scan showing Si concentration in GaAs is presented in Figure 6c. This data was taken from a p-Si/p-GaAs sample where the Si encapsulation layer was removed via a dry etch. The apparent Si spike at the top of the GaAs can be due to 1) Si diffusion or 2) incomplete removal of the Si cap layer, combined with surface roughening from dry etching prior to SIMS. The repercussion of possible Si diffusion on ohmic contact formation rests on whether the diffusing Si is neutral or negatively charged. For p-type contacts, in-diffusion of charged Si species may not be desirable because it can potentially counter-dope the III-V film. At worst, it can render the top surface of the III-V film n-type, creating a barrier at the p-type Si/III-V interface. As will be shown later, if this interfacial layer exists, it does not affect the ohmic behavior of the contact although it may affect contact resistance.
Ni/Si/GaAs metallurgical reactions.—Ni:Si thickness ratio of 2.9.—When “thin” Ni is deposited on a Si/GaAs structure, Ni reacts with Si without affecting the underlying GaAs as shown in Figure 5a. This Si/GaAs interface stability is consistent with previous observations.17,18 The restriction of the silicide reaction to occurring between Ni and Si (i.e., no reaction with underlying GaAs) allows for standard CMOS processing techniques to be applied with NiSi phase formation determined by anneal temperature: At low temperatures (below 250–300 °C), Ni diffuses into Si to form Ni-rich phases such as Ni2Si. At moderate temperatures (between 300 °C and 700 °C), NiSi forms through a reaction of 1 nm Ni + 1.86 nm Si resulting in 2.22 nm NiSi. Finally, NiSi2 nucleates at higher temperatures.19,20 XRD 20-ω results for our films with initial Ni:Si thickness ratio of 2:9 and RTA temperature of 450 °C is shown in black in Figure 7. The only X-ray peaks detected in XRD correspond to the expected X-ray signature of NiSi, confirming that NiSi is the only phase. Additionally, SIMS revealed that there is no additional out-diffusion of Ga or As after NiSi formation.

Ni:Si thickness ratio of 2:3.—When the Ni:Si thickness ratio is increased to approximately 2.3, all of the Si is consumed with NiSi formation, as shown in Figure 5b. In this case, the atomic ratio of Ni:Si is approximately 5:4 and XRD 20-ω scans of these samples after RTA, Figure 7, reveal that a combination of Ni5Si (gray X-ray peaks) and NiSi (black X-ray peaks) have formed. The relative strength of the Ni5Si signal versus the NiSi signal suggests that there are more Ni5Si grains than NiSi.

Ni:Si thickness ratio of 1:1.—With a further increased Ni:Si thickness ratio of 1:1, there is an interaction with the underlying GaAs. The calculated Ni:Si atomic ratio is 1.84 to 1. For this metallurgy, XRD 20-ω scans reveal that Ni5Si is the predominant phase formed at temperatures between 450 °C and 600 °C; no NiSi peaks are detected at all, as seen in the gray curve in Figure 7. The peak at 20 = 33.9° is neither Ni5Si nor NiSi but may be attributed to the [101] plane of NiAs. Additional TEM and XRD data for the phase evolution of this sample as a function of RTA temperature is presented in Figure 8. At 450 °C, a thick Ni5Si layer and thinner secondary layer are seen in Figure 8b. The interface between these two layers is relatively flat and demarked by a white line in the figure. When the anneal temperature is increased to 600 °C, the thickness of the Ni5Si remains approximately constant but the flat boundary between Ni5Si and the secondary layer breaks down (Figure 8c). This secondary layer also breaks into distinct grains, accompanied by an increase in the intensity of the NiAs XRD peak at 20 = 33.9°. When the anneal temperature is further increased to...
700 °C, the XRD peak at 33.9° disappears, as does the secondary layer beneath the Ni3Si. Coarsening occurs in the Ni3Si grain structure, leaving a bamboo structure which can be seen in the TEM image in Figure 8d. A very strong peak at 2θ = 31.5° also appears. This peak is most likely due to a surface oxide and can be attributed to either the [220] plane of Ni2SiO4 or the [102] plane of SiO2. Cross-sectional TEM images confirm the presence of a thin film on top of the Ni3Si, (Figure 8d).

A schematic of possible interactions which may give rise to these film structures is shown in Figure 9. At 450 °C the Si and GaAs layers stay relatively stable with Ni diffusion dominating silicide formation, similar to nickel silicide formation in CMOS.19–21 Excess Ni diffuses beyond the Si layer and reacts with the underlying GaAs. In thin film reactions between Ni and GaAs, both NiAs and NiGa are known to form.22,23 However, the lack of NiGa peaks in the X-ray data may be due to 1) NiGa grains being too small or too few to detect or 2) their non-existence. We suspect that there is far less NiGa than NiAs in the sample because the Ga easily diffuses into the Ni2Si, leaving regions of excess As. After a 5 minute anneal at 450 °C, gallium incorporation in the silicide is already higher than the arsenic, not shown. At 600 °C, this disparity might be even more pronounced.24 The result would be an excess of arsenic atoms at the GaAs/Si interface which can react with Ni to form NiAs. At 700 °C, in contrast, arsenic diffusivity in NiSi increases substantially and diffusion into the NiSi grains occurs.25 Additional grain growth in the Ni3Si can be seen and the NiAs grains are absorbed into the silicide.

NiSi/GaAs electrical characteristics.— Two metallurgical structures result in ohmic contacts, one with partial Si consumption (2:9 Ni:Si thickness ratio) and one with reaction into the GaAs (1:1 Ni:Si thickness ratio). The former must consist of two ohmic tunnel junctions, a NiSi/Si and a Si/III-V junction. The NiSi/Si junction is a CMOS standard and akin to a metal-semiconductor junction, with its ohmic behavior determined by doping in the semiconductor (Si). The Si/III-V interface, on the other hand, is established epitaxially and carrier conduction occurs because the semiconductors on either side are degenerately doped.

For the structure where all the Si is consumed in the silicide reaction but GaAs remains stable (2:3 Ni:Si thickness ratio), a rectifying junction is formed. Rectification at this interface suggests that an additional barrier to carrier conduction exists at the silicide/GaAs junction, possibly because additional trap states are induced by direct contact between silicide and GaAs.

This behavior may be expected because ohmic contacts have been formed using Ni thin films on GaAs in the past.25 For these samples, interaction between Ni and GaAs may eliminate trap states at the silicide-GaAs interface.

The dual junction NiSi/Si/III-V contact structure, however, is far more complex because the Si and III-V now have comparable sheet resistivities that convolute with further improvements via a more established industrial fabrication process. The dual junction NiSi/Si/III-V contact structure, however, is far more complex because the Si and III-V now have comparable sheet resistivities that convolute with further improvements via a more established industrial fabrication process.

**Figure 9.** Schematic of the interactions which may occur in NiSi/GaAs films with 1:1 Ni:Si ratio with annealing.
the Si edge that extends beyond NiSi, labeled $d_{\text{Si/edge}}$, in the schematic. These additional current paths must be represented in the equivalent circuit. In order to accurately extricate $\rho_c$ of Si/III-V from that of NiSi/Si, two methods are employed.

First, a 1D 700 resistor equivalent circuit of the NiSi/Si/III-V contact was built using the Quite Universal Circuit Simulator (QUCS). This model mimics the equivalent circuit shown in Figure 10b and discretizes the contact structure into small sections of length $\delta x$. In this model, the contact resistance between Si and III-V films is the only unknown parameter. The total contact resistance, $R_c$, is extracted from the modified TLM structure. Discretized sheet resistances of the Si and III-V layers, $\rho_{\text{Si}}$ and $\rho_{\text{III-V}}$, are extracted from Hall Effect measurements and discretized contact resistances of the NiSi/Si junction, $\rho_c(\text{NiSi/Si})$, are determined from NiSi/Si single junction samples. With these input parameters, $\rho_c$ is determined for a variety of ohmic Si/GaAs and Si/In$_{0.53}$Ga$_{0.47}$As interfaces. Results are shown in Figure 11b.

For some of the samples, an additional method of extracting $\rho_c$ was developed for comparison. A mask with TLM structures containing similar contact areas but different lengths for the Si edge, $d_{\text{Si/edge}}$, was used. By comparing total $R_c$ with $d_{\text{Si/edge}}$, the value of $R_c$ when $d_{\text{Si/edge}}$ shrinks to zero was determined. Standard TLM formulas were used to determine total $\rho_c$ of the NiSi/Si/III-V dual junction stack, from which $\rho_c$ of the NiSi/Si junction could be subtracted to enable determination of the Si/III-V single junction $\rho_c$. The data obtained from this experimental method is overlaid on the data from modeling in Figure 11b and shows good agreement.

The experimental extraction of $\rho_c$ (by altering $d_{\text{Si/edge}}$) has some advantages over extracting $\rho_c$ using the QUCS model. It is less reliant on accurate determination of the Si and III-V sheet resistances and NiSi/Si contact resistance, which must be inputted into the equivalent circuit model. However, because multiple TLM structures must be measured in order to extract each $\rho_c$, it does require more resistance measurements and a larger footprint on the wafer.

**Figure 11.** $\rho_c$ of (a) NiSi/Si junction and (b) Si/III-V junction, as determined by fitting data to an equivalent circuit model (●) and/or extrapolating contact resistances of samples without a Si edge (■).

**Figure 12.** Possible band diagrams for (a) n-Si/n-GaAs, (b) n-Si/n-InGaAs and (c) p-Si/p-GaAs, using the electron affinity rule for band alignments. The gray curves are ideal band diagrams without interface states whereas the black curves show band bending with the introduction of interface states. $E_F$ crosses the Fermi level at 0 eV and is depicted as a dashed line (--).
The $\rho_c$, across a metal-semiconductor barrier depends on barrier height, $\Phi_B$, carrier density in the semiconductor, $N$, dielectric constant of the semiconductor, $\varepsilon_m$, and tunneling effective mass, $m^*_{\text{tun}}$. For field emission,  
$$\rho_c \propto \exp\left( \frac{4\pi\Phi_B}{h} \sqrt{\frac{\varepsilon_m m^*_{\text{tun}}}{N}} \right), \quad [1]$$

where $h$ is Planck’s constant. $\rho_c$ is often quantified as a function of $N$ because the barrier to current conduction results from band bending in the semiconductor layer. For a semiconductor-semiconductor junction, band bending in both semiconductor layers contribute to the interface barrier. To better understand $\rho_c$ and draw comparisons between metal-semiconductor data in literature and semiconductor heterojunction data found in this work, we consider $\rho_c$ as a function of depletion width, $x_d$. $\rho_c$ can be rewritten as  
$$\rho_c \propto e^{\exp\left( \frac{\pi x_d \sqrt{8m^*_{\text{tun}}\Phi_B}}{h} \right)}, \quad [2]$$

In Figure 13, $\rho_c$ and $x_d$ for the semiconductor heterojunctions measured in this work are overlaid on NiSi/Si and PtSi/Si data from Stavitski et al.\textsuperscript{40} The $x_d$ at NiSi/Si and PtSi/Si interfaces are calculated using literature values for barrier heights (0.67 eV for NiSi/n-Si,\textsuperscript{42,43} 0.95 eV for PtSi/n-Si,\textsuperscript{44} 0.45 eV for NiSi/p-Si\textsuperscript{45} and 0.24 eV for PtSi/p-Si\textsuperscript{45}). The general trend shows thinner $x_d$ resulting in lower $\rho_c$. Therefore, we deem $x_d$ a good predictor of $\rho_c$ at Si/III-V heterojunction interfaces.

Laser with CMOS-metal front-side contact.— In order to demonstrate the feasibility of these NiSi/Si/III-V contacts on a functional device, a laser with silicide front-side contact was fabricated. Though a laser is not the most rigorous test of contact metallurgies, it provided a simple way to provide a proof of concept. The Si/GaAs heterojunction forms the p-type contact with lowest series resistance, $R_s$, of both types of devices 4.4 $\pm$ 0.2Ω and the threshold current densities, $J_{th}$, is 3.9 $\pm$ 0.3 kA/cm² for devices 4.5 $\mu$m to 7.6 $\mu$m wide and 510 to 530 $\mu$m long. These lasers demonstrate the feasibility of NiSi/Si/III-V contacts for current injection into laser devices.

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References
