Operation of Buck Regulator with Ultra-low Input Voltage

by

Cory Angelo Harris

Submitted to the Department of Electrical Engineering and Computer Science
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Abstract

Based on the LTC3621 and LTC3624, the designed buck regulator proposed in this thesis aims to lower the allowed input voltage and increase efficiency compared to the original part without making significant changes to quiescent current and part performance. This thesis will discuss additions and modifications made to the original afformentioned parts in order to achieve said goal. This thesis will provide an in depth analysis through simulations of the results of the changes made and a comparison of performance between the original and the redisigned part.

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Acknowledgments

I would like to thank Tom Sheehan, my mentor at Linear in Boston, for introducing me to the world of integrated circuits and providing me with the information needed to apply for the VI-A program. I would also like to thank my mentor at Linear in Milpitas, Steve Zhou. His wisdom and mentorship throughout my time in Milpitas were essential to my learning of IC design concepts, my increased interest in transistor level work, and my completion of this thesis project. I truly appreciate the time and effort he has put in over the months. I would also like to thank my MIT thesis supervisor David Perreault for taking the time to read and provide feedback on my thesis.

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Chapter 1

Introduction

Buck regulators are a very important and essential part of today's electronics. Buck regulators provide an efficient way to step down input voltages to match voltage requirements for certain components within a device. This technology quickly replaced the use of linear regulator because those devices lowered voltages through a resistive element thus making them rather inefficient. The power losses associated with Buck regulator are a combination of conduction and switching losses. Despite these losses, many of today's buck regulators can reach max efficiencies of 90+%.

The use of portable electronics has increased greatly over the past few years. Advancements in energy conversion and energy saving techniques have allowed devices to maximize portability without compromising functionality.

1.1 Motivation & Prior Work

As technology continues to advance the demand for lower voltage devices and the need for regulators that can operate and perform efficiently at these lower voltages is desired. Currently there are very few buck regulators in the market that can operate efficiently at low voltages. Linear Technology is an integrated circuits company that focuses on power products (Buck regulators, Boost regulators, etc...). As part of my thesis work through the MIT VI-A program, I will be working with design engineers at Linear Technology to develop a product to improve Linear's portfolio of buck

Manufacture r	Part	V_{IN} min	V_{IN} max	monolithic	I out
Linear	LTC3713 [4]	1.5	36	no	20
Linear	LTC3409 [5]	1.6	5.5	Yes	.6
Linear	LTC1622 [6]	2	9.8	no	5
Linear	LTC3621 [7]	2.7	17	yes	1
Linear	LTC3624 [1]	2.7	17	yes	2
Texas Instruments	TPS62243 [8]	2.5	6	yes	.3
Texas Instruments	TPS53319 [9]	1.2	22	no	14
Maxim Integrated	MAX1920 [10]	2	5.5	yes	.4
Maxim Integrated	MAX1515 [11]	1.3	3.6	yes	3
Linear	Proposed	2	17	yes	2

Table 1.1: Specifications for switching converters from IC companiesand proposed converter

regulators. Linear currently only has one buck regulator (LTC3713) on the market that has both low and high input voltage operation. However, this regulator is not a monolithic part and combines two separate die parts, a boost converter and a buck regulator in order to achieve operation at low voltages. The boost converter is not provided as part of the power stage, but rather to generate necessary voltages (e.g., for control logic) to run the power stage when the input voltage is low. Linear has a few other buck regulators that operate at low voltages but they are limited by smaller overall voltage range, low output current or require a seperate power supply. Other IC companies like Texas Instruments and Maxim Integrated also have buck regulator chips but similar to Linear, they are limited to small voltage ranges and low output current. A product comparison can be seen in table 1.1. My goal is to design a single die device that covers all common ranges of operation. This new device should be able to operate efficiently at both low and normal voltages while still providing the 2 amp current loads. table 1.1 below shows comparison of parts on the market and the proposed part.

1.2 Proposed Work

As seen in the table 1.1, the proposed buck regulator will closely resemble the LTC3624, a step-down regulator IC. The project will be based on this part. Modifications and additions will be made to this device in order to achieve the proposed specifications. With these changes we will increase the versatility of the part and increase the number of applications. This proposed part will have high efficiency, high load current and a wide input voltage range.

1.3 LTC3624 overview

The LTC3624 is a fixed frequency peak current buck regulator that uses the current at the inductor to determine when the top gate turns off after each clock cycle. A block diagram of the LTC3624 is shown in Figure 1-1. There are a few blocks that are particularly important for operation and will require modification to achieve proper operation under the new desired specifications. The bandgap block provides a reference voltage for the Error Amplifier and the various comparators. The LDO block creates the internal supply voltage for the chip. The Gate Drive Block controls the operation of the part and the states of the top and bottom side transistors. To ensure proper chip operation, each of these blocks will be examined and modified.

1.4 Application

Portable electronics have become the forefront of technological advancements over the past decades. With this increase in portability comes a strong desire for power efficiency devices. A desire to operate at lower voltages has become equally desired as well to increase power efficiency. This proposed part could find its way into dual cell NiMh devices. At 1.2 volts per cell and a safe discharge voltage of 1 volt, the proposed device with a 2 volt input minimum could be used. It also can be used in lithium cell powered devices that in many cases can operate down to 2.5 volts. The increased efficiency due to the implementation of an NMOS top-side Power FET makes the

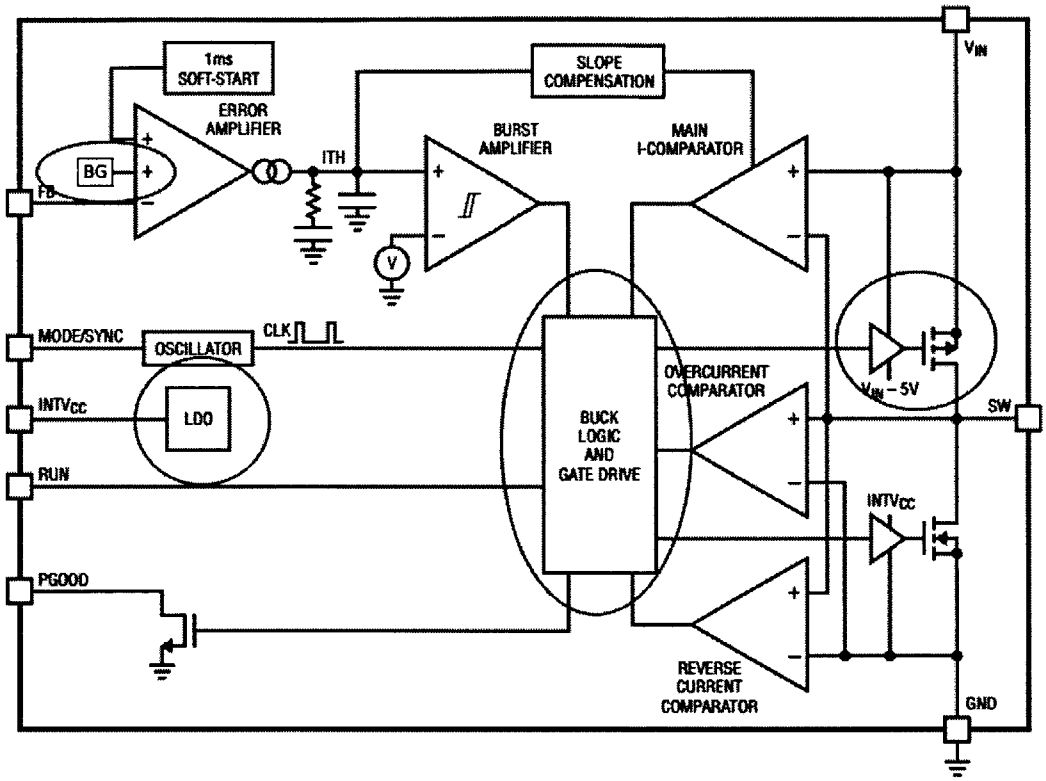


Figure 1-1: Block diagram of LTC3624. Circled are blocks to be modified[1]

device versatile and applicable over all the voltage ranges. This modification will increase efficiency over all of the voltages which means that in addition to being used for low voltage applications, it can be used for higher voltage applications as well including cell phones and laptops.

1.5 Chapter Overview

The following chapters will go through some of the changes and modifications made to the existing circuit in order to reach the proposed goal. Chapter 2 will focus on the bandgap block, specifically what prevents the original bandgap design from operating at less than 2.7 volts. It will address what changes were made to the initial schematic in order to achieve said goals. Chapter 3 will talk about the usage of a charge pump in the LDO block. it will go through all the components and design choices made when

designing the pump. Chapter 4 will look at the integration of the charge pump in to the LDO block. It will again highlight the additions made to the previous design. Chapter 5 will talk about the benefits of an NMOS top-side MOSFET vs. a PMOS device. It will explain in detail the new gate drive circuity created to operate the NMOS device. Chapter 6 will discuss all other modifications made to the original circuit block that was not covered in chapters 2-4. Chapter 7 will cover testing results of various blocks within the chip. These results will be tested and compared to the original design. Lastly a summary of changes and conclusions will be in chapter 8.

Chapter 2

Bandgap

The Bandgap is a crucial part of this converter's power regulation. The bandgap block provides a relatively temperature independent voltage source. This reference voltage is used throughout the part, particularly in the comparator stages including the main current comparator used to to determine the gate drive for the switching transistors. It is also used in the on die oscillator which determines the point in which the top-side device turns on. In figure 2-1 is a block diagram with the the components that are effected by the bandgap reference voltage.

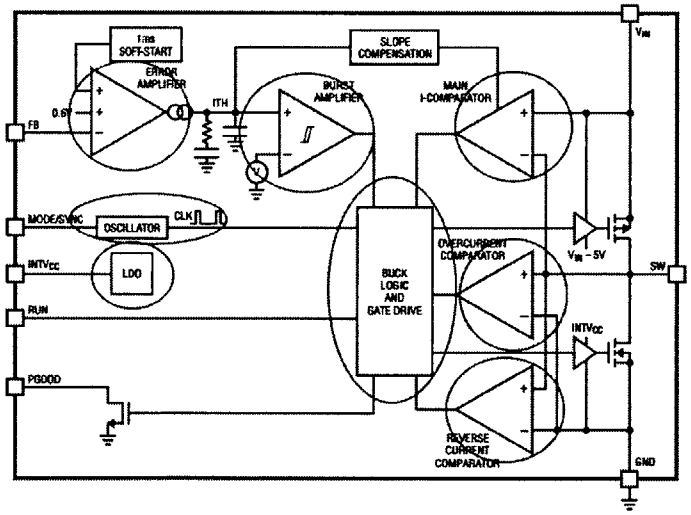


Figure 2-1: Blocks affected by the Bandgap reference voltage[1]

As the bandgap is an essential part of chip operation, the bandgap needs to be

able to operate under all operating conditions to ensure proper chip function. To test the bandgap circuit blocks, the edge cases will involve looking at the behavior under certain temperatures as well as different transistor modes. The LTC3624 has a stated minimum operating input voltage of at least 2.7 volts. The existing bandgap should therefore be able to create a reference voltage at 2.7 volts under all edge case conditions. Using a DC sweep on the input voltage of the bandgap block, we can determine at what input voltage the bandgap circuit is no longer able to create a reference voltage. The BGold marker from Figure 2-4 is the result of a DC sweep from 1 to 3 volts of the input supply with the original bandgap. The transistor mode was Slow Slow (SS) and the temperature was -45°C. The Y axis is the steady state reference voltage (v1p2) created by the bandgap block.

Under these worst case conditions, the bandgap block creates the desired reference voltage at a 2.7 input voltage as the datasheet states. However, the bandgap block fails to create a reference voltage when the input is less than 2.5 volts making the current bandgap design not suitable for the proposed part. As the goal of this project is to have operation as low as 2 volts, changes must be made to this bandgap block to achieve proper operation at sub 2.5 voltages.

2.1 Bandgap Block Anaylsis

Prior to redesigning the circuit block it is important to understand the reasoning behind the block's shortcomings in hopes that in understanding its flaws, changes can be made to alleviate the faults.

It is important to mention that the bandgap reference circuit is not directly supplied by the input voltage but rather by a created bandgap supply voltage. The reason for this is due to the fact that the part has a wide input voltage range (2.7-17 volts). Connecting the input directly to the bandgap circuitry would require all its transistors to be able to handle a 17 volt voltage difference across the terminals. Handling this voltage difference would requite the use of transistors that are often larger and slower than transistors that can only handle a 5 volt difference across terminals.

A bandgap supply voltage can be made using a PMOS device that can create a sub 5 volt bandgap supply voltage. This would significantly reduce the number of transistors that need to handle the higher voltage inputs. However, at a 2 volt input under certain edge cases the bandgap supply voltage is not 2 volts and is actually below the desired 1.2 reference voltage. It is for this reason the bandgap circuit does not work. The culprit behind this input voltage restraint has to do with how bias voltages are created for certain transistor gates in order to control the PMOS device that creates the bandgap supply.

2.1.1 Bandgap Supply Anaylsis

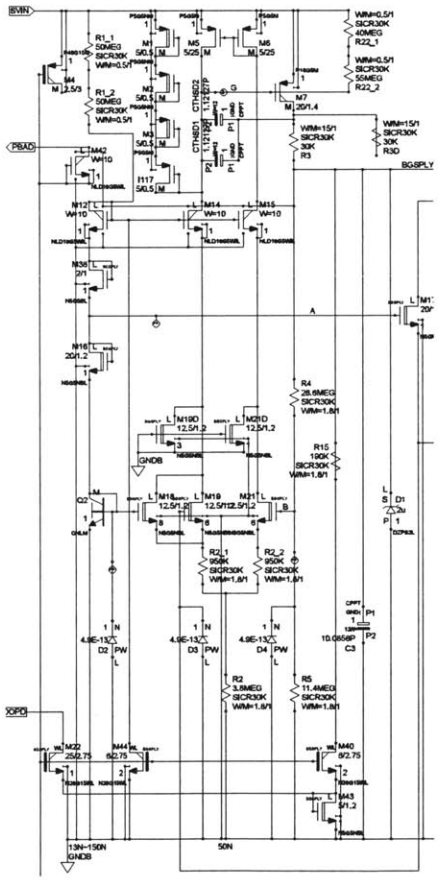


Figure 2-2: Cutout of bandgap schematic

A portion of the bandgap block that creates the bandgap supply has been added (Figure 2-2) to aid in explanation and referencing of transistors.

The role of transistor M18 is to provide current to the current branch until the reference voltage, which is used as the gate voltage for M19, is high enough for M19 to sink its own current. This current branch is of great importance as it aids in setting the gate voltage of the PMOS device (M7) used to create the bandgap supply voltage. If the reference voltage gets high enough, it should sink enough current and increase the source voltage to the point where M18 is turned off because of its lower gate voltage. The gate voltage is determined by the voltage drop across the resistors$R22_1$ and$R22_2$. If the bias voltage is not high enough, the amount of current going through M18 and the lower half of the current branch is minuscule. The current from the R22 resistors will charge the capacitors thus increasing the G voltage and turning off the M7 PMOS transistor. If the bias voltage is high enough, the NMOS will sink more current. To meet the NMOS current demands, more current will flow through the R22 resistors thus lowering the gate voltage. The increase in the M7 current will cause an increase in the B voltage. This in return through a current mirror, increases the amount of current sourced by the M5 and lowers the current needed by the resistor branch. This feedback loop continues until a steady state is reached. The M7 current also supply current and creates the bandgap supply voltage needed by the actual bandgap block used to create the reference voltage.

2.1.2 Temperature and Transistor mode effects

Analysis of the spice results suggests that the bias voltage created by the BJT is most affected by the low input voltage. All transistor types (MOSFET, BJT) are affected by temperature as well as the transistor operating mode.

Figure 2-2 contains a single current branch (Q2, M16, M38, M12) used to set gate voltages for 3 transistors (M18, M17, M14) within the bandgap block. This branch of diode connected transistors work by settling at the Drain-source voltage or Collector-Emitter voltage required to meet the amount of current in the branch. The value of the V_{BE} orV_{th} of each transistors is an important factor in determining the operating point of theses transistors. Assuming the MOS devices are in saturation, Equation 2.1can be used to determine the bias voltage of the transistor.

Transistor	Parameter	Typical n Typical p (TT) $T_{oxn} = 1.4e^{-8}$ $T_{oxnt} = 5.0e^{-8}$	Slow n Slow p (SS) $T_{oxn} = 1.6e^{-8}$ $T_{oxnt} = 5.5e^{-8}$
N5G5	V_{TO}	.71	.87
	μ_0	1.0	.895
	V_{SAT}	1.0	.875
	$C_{J/J_{SW}}$	.71	.87
N5G5N	V_{TO}	.38	.52
	μ_0	1.0	.88
	V_{SAT}	1.0	.88
	$C_{J/J_{SW}}$	1.0	1.15
NLD18G5B	V_{TO}	.63	.72
	μ_0	1.0	.895
	$C_{J/J_{SW}}$	1.0	1.15

Table 2.1: MOSFET transistor characteristcs comparison

$$V_{BIAS} = V_T + \sqrt{\frac{I_D}{\frac{W}{2L}\mu_n C_{ox}}} - V_s \tag{2.1}$$

This bias voltage equation is temperature dependent. Equations 2.2 and 2.3 provides a more in depth look at the threshold voltage and the temperature dependence of the surface potential Φ_F.

$$V_T = V_{TO} + \gamma\left(\sqrt{|V_{SB} + 2\phi_F|} - \sqrt{2\phi_F}\right) \tag{2.2}$$

$$\Phi_F = \left(\frac{kT}{q}\right)\ln\left(\frac{N_A}{N_i}\right) \tag{2.3}$$

The thermal voltage decreases with increase in temperature. There are other parameters that affect the threshold voltages. These parameters change based on the different transistor models used to turn simulations. Table 1 below highlights some of the different parameter values between the Typical and slow transistor models for MOSFETs in spice. The threshold voltage with zero V_{SB} (V_{TO}) is one parameter that directly affects the threshold voltage. Furthermore, the varying gate oxide thickness (T_{ox}) effects the oxide capacitance (C_{ox}) and the varying channel mobility (μ_o) effects μ_n both of which effect the bias voltage.

Transistor	Parameter	Typical	Slow
qnl	β_F	1.0	.75
	R_B	1.0	1.2
	R_C	1.0	1.2
	R_E	1.0	1.2

Table 2.2: BJT characteristics comarison

Similar observations can be made about BJTs. The bias equation and model comparison are below.

$$V_{BIAS} = \frac{kT}{q}\ln\left(\frac{I_C}{I_S}\right) - V_E \tag{2.4}$$

$$I_S = \frac{qA_E D_n n_i^2}{N_B W_B} \tag{2.5}$$

$$D_n = \frac{kT}{q}\mu_n \tag{2.6}$$

$$n_i^2 = DT^3 e^{\left(-\frac{qV_{G0}}{kT}\right)} \tag{2.7}$$

The reverse saturation currentI_s is highly temperature dependent resulting in the BJT bias voltage to decrease with increasing temperature [12]. Because of these characteristics, low temperatures and SS model testing will result in the highest V_{be} and threshold voltages. The increase of threshold and bias voltages lead to issues as the input voltage is lowered. As the input voltage decreases, the transistors are forced out of their desired saturation and forward active regions. The MOSFETs are forced into the sub threshold region where drain current is the result of diffusion rather than drift as in the saturation region. In this region the drain current is an exponential function of the gate voltage. This change in operating regions as well as the input voltage limitation can result in lower bias voltages. As the bias voltages are controlling NMOS devices, these lower voltages can prevent these transistors from being turned on.

2.2 Bandgap Supply Modification

Inserting a second current branch and separating the M18 gate voltage from the original branch will allow the gate voltage to be higher at lower inputs. By lowering the number of diode connected transistors in that branch, the V_{BE} voltage of the BJT will not be forced lower. Figure 2-3 below shows a comparison between the original single current line bias branch and the new redesigned dual current bias branch. A comparison of the reference voltage versus input voltages of the old and new design can be seen in Figure 2-4

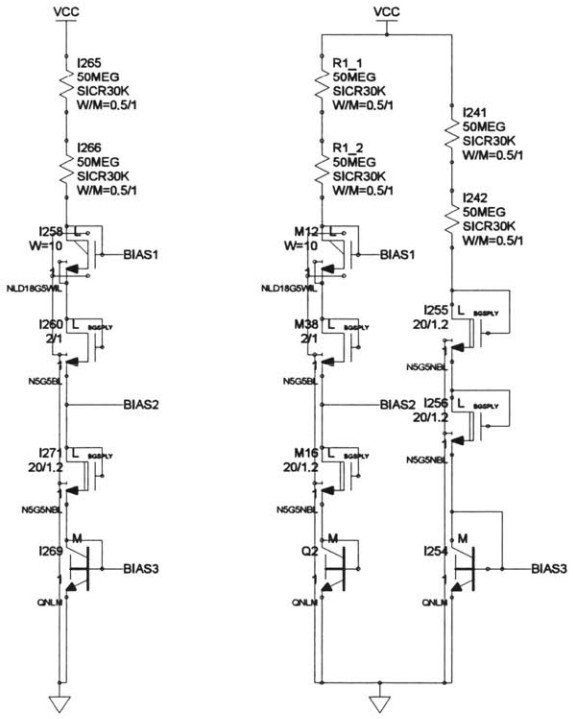


Figure 2-3: Comparison of old(left) and new(right) bandgap bias design

2.2.1 Drawbacks

Adding an extra current branch does not come without sacrifices. The lower input operating voltage comes at the expense of an increase in operating current. Figure 2-5 is a plot of the total current used in creating bias voltages for the old and new bandgap design.

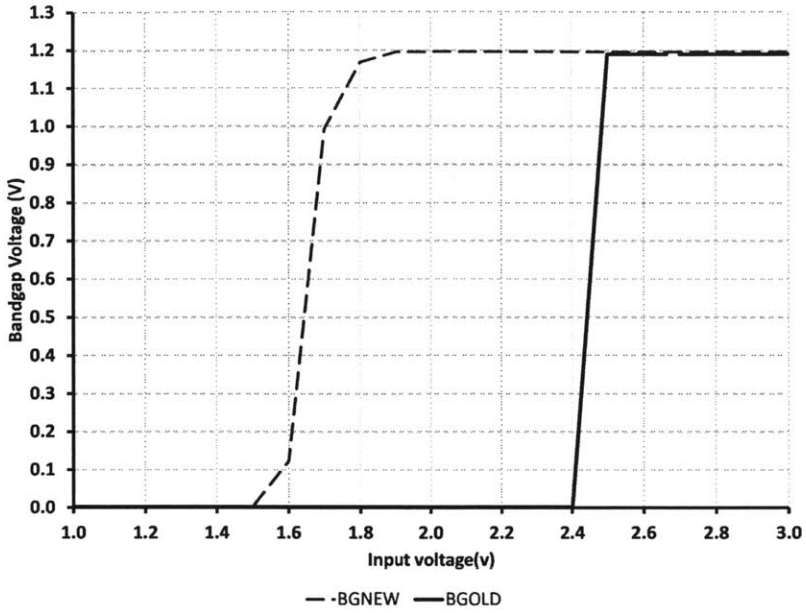


Figure 2-4: Comparison of bandgap voltage at differerent input voltages

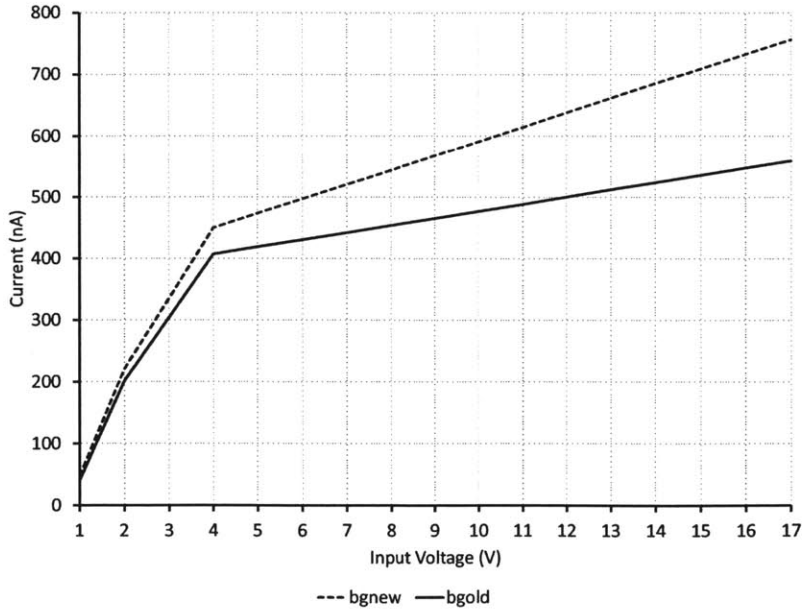


Figure 2-5: Comparision of bandgap Q current at different input voltages

Chapter 3

Charge Pump

The LDO is the circuit block that creates the internal supply voltage that is used to power the circuitry involved in operating the controller and converter. Similar to the bandgap , the is a crucial component of the chip's operation and affects all the blocks within this IC apart from the bandgap block which is expected to operate off of the Vin voltage. The affected blocks can be seen in Figure 3-1.

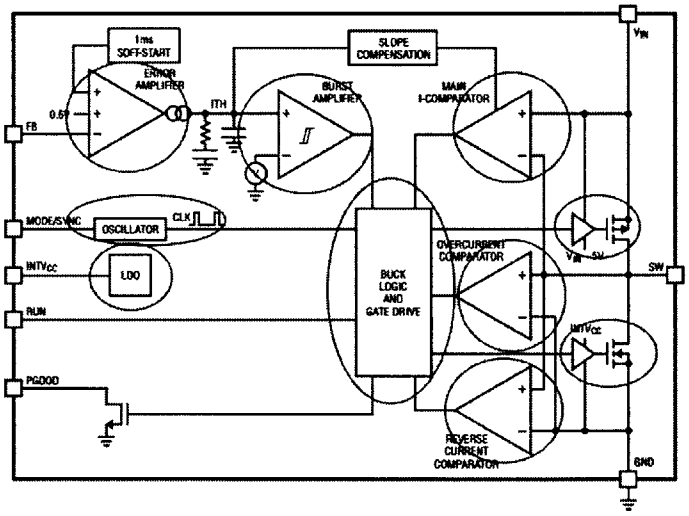


Figure 3-1: Circuit blocks affected by the LDO block[1]

The original LDO block uses a PMOS device to create an internal supply voltage around 3.6 volts. This block, however is limited by the input voltage, so the internal supply will drop below 3.6 volts when the input voltage is below 3.6 volts. an LDO

ready signal is used to set the point at which the internal supply can be used to power the remaining circuit blocks and is set at roughly a 2.7 volt threshold. At the proposed 2 volt input the internal supply voltage will not be above 2 volts using the original LDO block. This is problematic as the internal supply will not be high enough to trigger the LDOReady signal or provide enough voultage to bias up many of the other circuit blocks. Furthermore an internal supply voltage of only 2 volts will result in power issues due to lack of overhead in inverters and other logic circuitry.

The proposed solution to increase the internal supply voltage during low V_{IN} operation is to integrate a charge pump. A brief overview of the new LDO design can be seen in Figure 3-2. The original LDO will serve as the input into the charge pump. However, the charge pump may not always be needed. To determine when the charge pump is need, the output of the original LDO will also serve as a signal to determine whether or not the charge pump is needed. Chapter 3 will talk about the charge pump design while chapter 4 will talk about the integration of the charge pump into the existing LDO to create the new LDO.

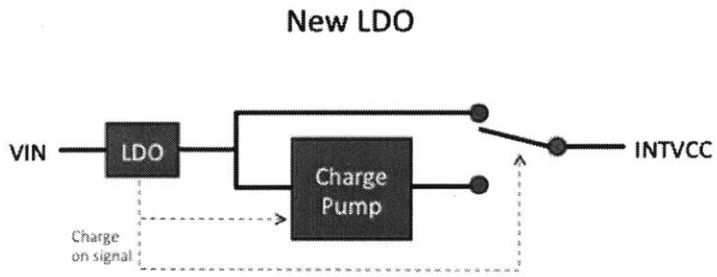


Figure 3-2: New LDO Design with Integrated Charge Pump

3.1 Charge pump overview

A charge pump is a device that uses capacitors and switching controls in order to create an output voltage that is higher than its input voltage. Depending on the circuit design, number of capacitors and stages, or switching configuration, output voltages can double, triple or even quadruple the input voltage [13]. As stated previously, one

of the issues raised with lowering the input voltage is that the internal supply voltage will not be high enough to effectively and efficiently power circuit blocks within the device. To resolve this issue, a charge pump will be used to create a voltage higher than the input voltage to aid in creating the internal supply voltage. To keep things relatively simple, a two stage doubling charge pump will be used. With a goal of operation as low as 2 volts, a doubling charge pump should be able to create a voltage close to 4 volts, which is more than enough voltage to effectively operate the circuit blocks.

A basic two stage doubling charge pump can be seen in Figure 3-3. The charge pump works in two stages. In the first stage, switches 1 and 2 are closed and 3 and 4 are open. This creates a connection between V_{IN} and ground across a capacitor known as the flying capacitor. This stage allows the capacitor to charge to up to V_{IN}. In stage 2, switches 3 are 4 are closed while 1 and 2 are open. This creates a connection between V_{IN} and V_{OUT} across the flying capacitor. Since the flying capacitor is to be charged to V_{IN}, and V_{IN} is connected to the negative terminal of the capacitor, the voltage at V_{OUT} is V_{IN} + V_{IN} (2 x V_{IN}). this voltage is then used to charge another capacitor called the reservoir capacitor. As the reservoir capacitor gets charged by the 2 x V_{IN} voltage, the flying capacitor becomes discharged. However, by switching back and forward between these 2 stages, we allow the flying capacitor to become recharged each time it returns to stage 1. The reservoir capacitor also becomes discharged due to the load but similarly the reservoir capacitor becomes recharged during stage 2. Providing that the load does not exceed the charging rate, the end result should be a reservoir capacitor at $2xV_{IN}$ voltage with some amount of voltage ripple.

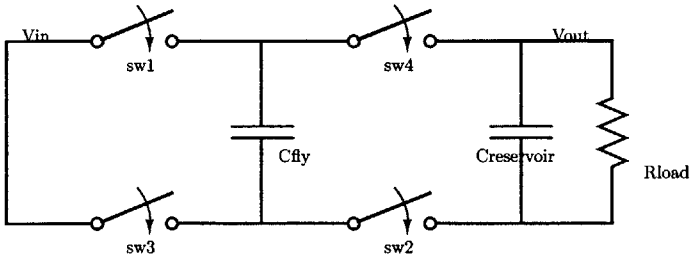


Figure 3-3: Basic charge pump

3.2 Burst vs. Constant frequency charge pumps

There are two different types of charge pump designs to be considered in designing a charge pump, burst mode and constant frequency. The differences between the two techniques lie in how the capacitors are charged and the feedback controlled. In the burst mode configuration, a constant current is used to charge the capacitors and feedback controls the switches that determine which state the charge pump is in. In this method, the switch rate is variable. In the constant frequency configuration the device switches between the two states at a constant rate. However, instead of a constant current source to charge the capacitor, a variable current source is used. Feedback is used to determine how much current goes into to charging and discharging the capacitors. Although the burst mode design is simpler and more common there are a few benefits in using the constant frequency design over the burst mode. One of the main faults with burst mode is the amount of input and output noise in part due to the variable frequency. The constant frequency charge pump has much less input and output noise which will be beneficial when it comes to making sure the added circuitry doesn't effect the chip as a whole because the noise frequency can be set to be the same as the chip's switching frequency. The output ripple of the constant frequency design is also much less than that of the burst mode [14]. The burst mode design tends to have slightly less quiescent current, but the noise and ripple benefits outweigh the lower quiescent current. The following sections will discuss the design of the constant frequency charge pump components.

3.3 Constant frequency charge pump design overview

There are a few things to consider prior to designing. First, the Charge pump will be powered by a Maxer circuit that compares the input and output voltage. The maxer circuit always selects the higher of the two voltages. This is beneficial to provide logic with as much voltage swing as pssible. The ideal switches from the basic design will be replaced with gm amplifiers. These amplifiers will supply current based on the

voltage at the output, applying more current when output voltage is high and less current when current is close to the desired amount. There will be two clocks that will work asynchronously to create the constant frequency component of the charge pump. When the output voltage is low, it implies that the LDO voltage is not high enough yet to power the other circuit blocks. The die oscillator therefore will not function. During this area of operation a secondary oscillator based on a Schmitt trigger design will be used. When the LDO voltage becomes high enough to pwoer the remaining parts, the Schmitt trigger is no longer needed and the charge pump can run off the die oscillator. This method also places the charge pump and other circuit blocks in synch which can reduce noise. A block diagram can be seen in figure 3-4.

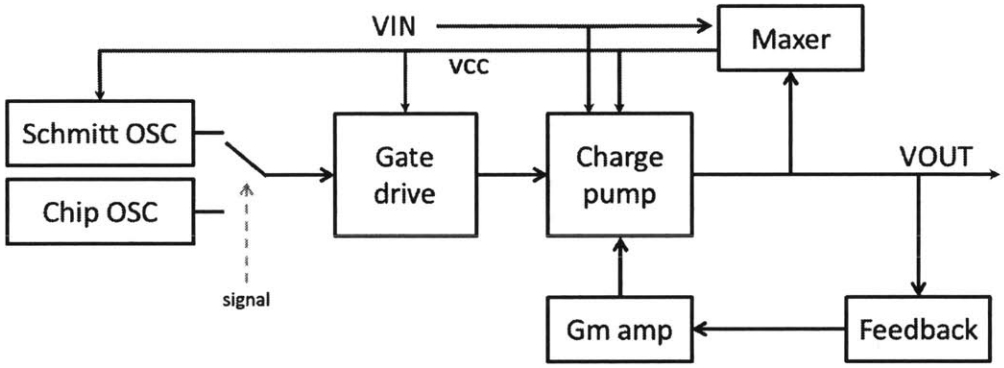


Figure 3-4: Charge pump block diagram

3.4 GM Amplifier for Constant frequency charge pump

The ideal switches shown in the basic charge pump design (Figure 3-3) are implemented using GM amplifiers. When the switch is open, the GM amplifier will not sink ay current. When the switch is closed the GM amplifier will sink current inversely proportional to the voltage on the reservoir capacitor.

When the feedback voltage is low relative to the reference voltage, the amount of current in the feedback branch relative to the reference branch is small. This lesser

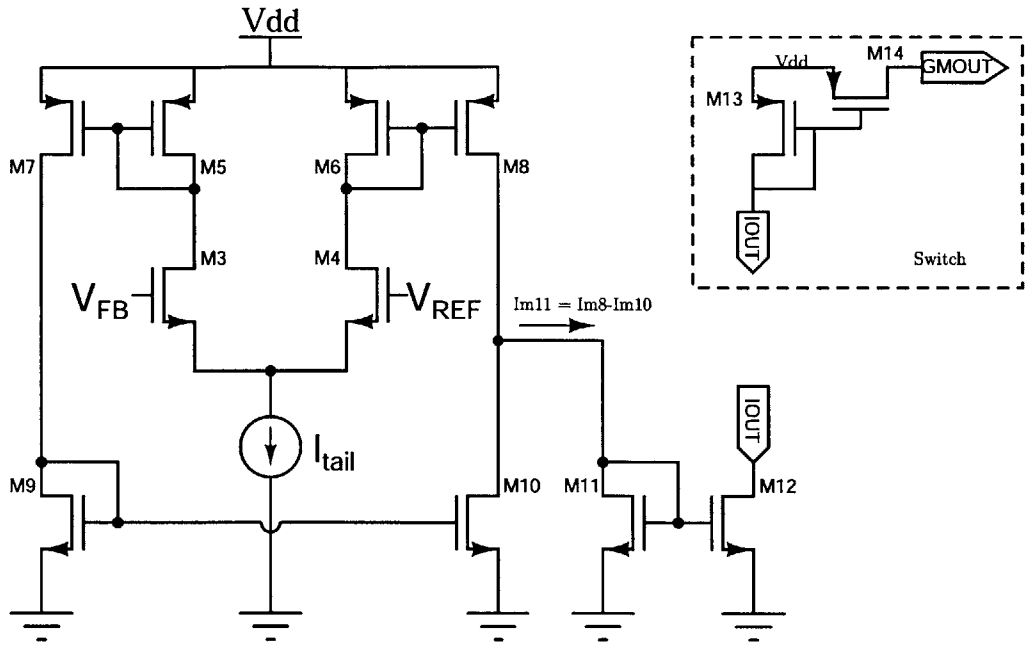


Figure 3-5: Gm amplifier

feedback branch current will be mirrored and multiplied and the resulting current is mirrored. The reference current is also mirrored and multiplied. To satisfy KCL rules, the current into the last current mirror is equal to the difference between the two currents. When the feedback voltage is higher than the reference voltage then the NMOS (M10) current is larger than the PMOS (M8) current. In this case however, the NMOS (M11) of the last stage current mirror can only sink current, not source it, so it cannot supply the current needed to satisfy the KCL rules. The NMOS device is forced into deep triode region. This lowers the node voltage to ground minimizing the current at M11 and I_{OUT}.

3.4.1 Transistor Sizing

The sizing of the transistors in this amplifiers is dependent on the amount of load we expect from the internal supply. As a conservative measurement we expected at most 20mA load on the internal supply. With roughly a 50% duty cycle, the current source would need to be able to supply over 40mA of current in the worst case otherwise

the reservoir capacitor would never increase in charge stored. By adjusting transistor sizes of the current mirroring stages, we can increase the current to reach the desired 40mA. There are four sets of current mirrors. By design choice, we chose to have a 3μA tail current. This current is provided by sourcing a 1.5μA current from the LDO block and using a 2x NMOS current mirror. The current sourced from both branches of the differential amplifier are mirrored with an 8x current mirror. The NMOS current mirror is not multiplied so that there is an even comparison between the feedback and reference branch. The current that results from the difference between the PMOS and NMOS current gets mirrored with a 100x current mirror. The final stage which is built into the charge pump gate circuitry involves a 37x PMOS current mirror. If all the tail current were to go to the reference branch, then 88.8ma would be used to charge the flying capacitor.

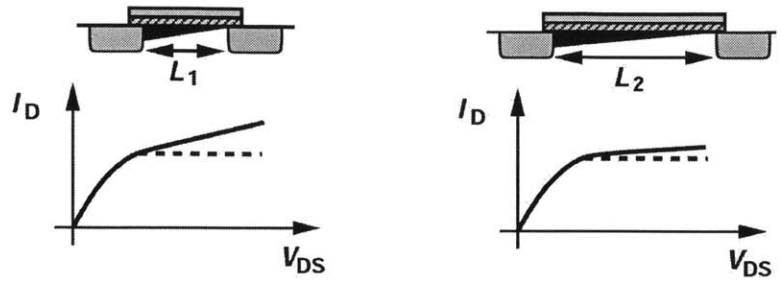
To have relatively accurate current mirrors, the transistors will be sized with large channel lengths.The reason for this is because the output mirrored current is not exactly equal to the transistor scaled input current.

$$I_{out} = I_{in}\frac{(W/L)_2}{(W/L)_1}\left(\frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}}\right) \tag{3.1}$$

$$\lambda \propto \frac{1}{L} \tag{3.2}$$

Increasing the transistor length will decrease the variation of saturation current over different values of V_{DS} due to channel length modulation[15]. Figure 3-6 shows the saturation current over V_{DS} of a short length device (3-6a) versus a long one (3-6b) . A longer device will result in an output current more closely equal to the width scaled input current. However with a larger transistor length, a larger transistor width will be needed to ensure that the device is operating in saturation. It becomes a trade off between overall transistor area and current mirror accuracy.

The transistors, whose gates serve as the input to the differential pair, are sized such that the transistors are operating in weak inversion. Weak inversion is the optimal operating condition due to its behavior as a result of various input voltages [16]. Transistors in weak inversion have a lower voltage mismatch contribution and



(a) Short length (b) Long length

Figure 3-6: The effects channel length modulation has on saturation current for larger length transistors versus smaller[15]

achieve a greater transconductance efficiency [17]. Furthermore weak inversion is considered to be more power efficient than operation in the saturation region as the current required in saturation to reach the same settling performance as a device in weak inversion is higher.

3.4.2 Gain Calculation

$$\begin{aligned} A_v &= G_m R_{OUT} \\ R_{OUT} &= R_{on} || R_{op} \\ G_m &= B g_{m1} \\ B &= \frac{W_6}{W_4} \\ A_v &= B\sqrt{2\frac{W}{L}\mu_n C_{ox} I_{tail}}\frac{R_{on}R_{op}}{R_{on}+R_{op}} \end{aligned}$$

3.4.3 Transconductance

3.4.4 Feedback Voltage

The feedback voltage into the differential amplifier is created using a resistor divider from the output. The sizes of these resistors depend on the reference voltage as well as the desired charge pump voltage.

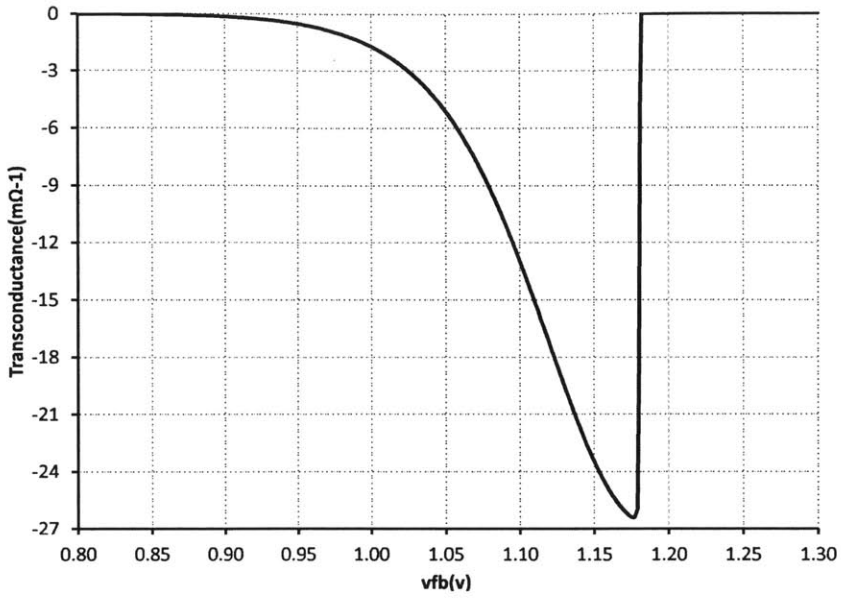


Figure 3-7: Plot of transconductance vs. feedback voltage

$$\frac{R_1}{R_1 + R_2} V_{CHG} = V_{ref} \tag{3.3}$$

The reference voltage used in the differential amplifier is the voltage from the bandgap block which is approximately 1.18 volts. The desired charge pump voltage is 3.6 volts. Sizing R_1 and R_2 as .41MΩ and .2MΩ respectively allows us to achieve the desired charge pump voltage.

To achieve a faster charge time and compensate for relatively low gain, the feedback voltage is set to 0 volts until a certain voltage is reached. After this voltage is reached the feedback voltage becomes the voltage at the resistor divider. This allows for maximum current while the reservoir capacitor is being charged. A transistor parallel to the R_2 resistor allows us to achieve this. A low trip voltage will result in a high signal for the gate of the transistor. Turning on the transistor will bypass R_2 resistor bringing the feedback voltage close to ground. A low signal turns off transistor equal to voltage over R_2.

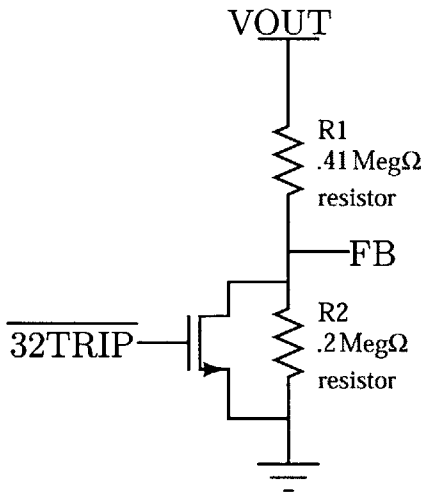


Figure 3-8: Feedback branch with resistor override

3.4.5 Shut Off

The charge pump is not always operating especially when the input voltage is above 3.2 volts. In these states, the GM amplifier does not need to operate either. In order to minimize quiescent and operating current, a few additions are added to the amplifier. The first step is to turn off the GM amplifier is to by shutting off the current going into the amplifier. The LDO supplies a 1.5μA current using a PMOS current mirror. An added PMOS device allows us to use a signal to shut off current going into the amplifier. However, this is not sufficient to completely turn off the amplifier. Leakage current into the amplifier gets amplified causing current to still be sinked.To further reduce current loss, transistors are added to the gates of the current mirror transistors (M1 and M14). When the GM amplifier needs to be turned off, these transistors pull the gates to ground preventing the transistors from being turned on and mirroring current. These additions can be seen in Figure 3-10.

To achieve the feedback voltage, a resistor divider is used. This results in power loss and added operating current. Adding an NMOS transistor to the resistor divider branch allows us to control when current is allowed to flow through this branch. Run signal used to control the NMOS will be explained later in the chapter.

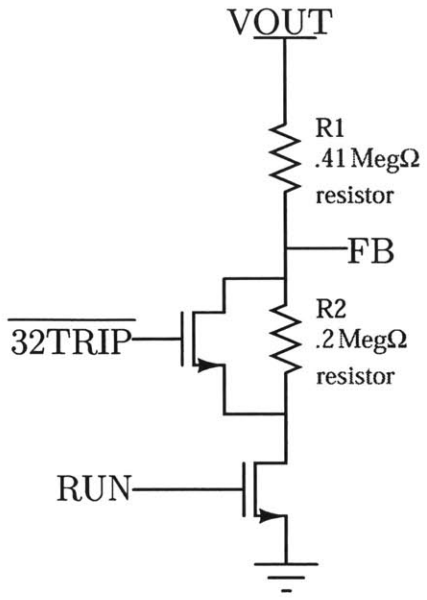


Figure 3-9: Feedback branch with resistor overide and current shutoff

3.4.6 Final Design Schematic

The transconductance amplifier with transistor sizing and shutoff circuitry can ne seen in figure 3-10.

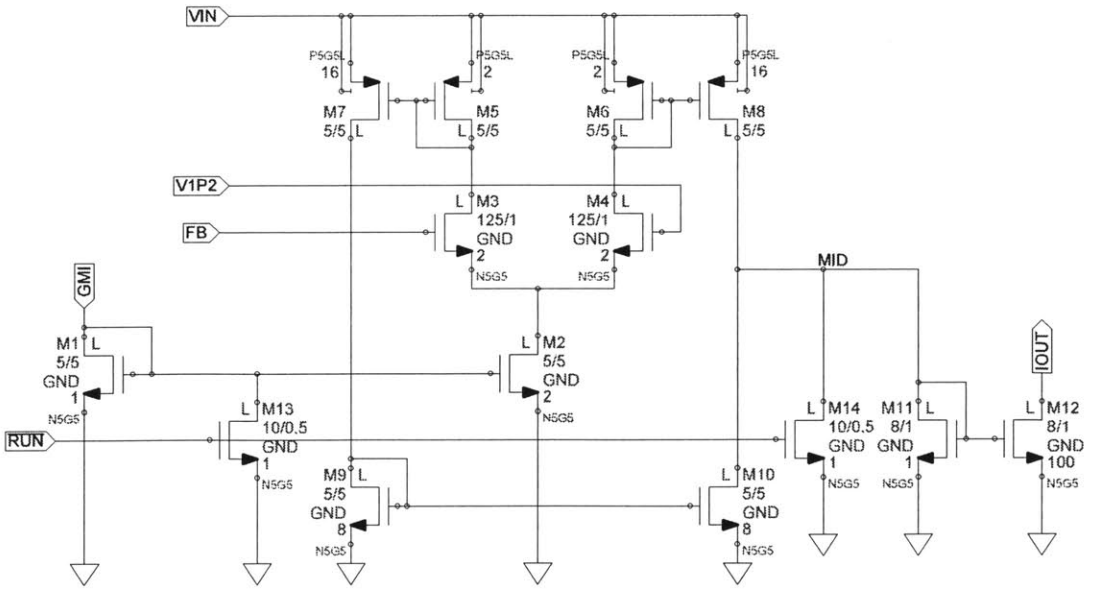


Figure 3-10: Complete design of gm amplifier

3.5 Charge Pump Region of Operation

As the charge pump is not always needed, this section will cover what determines whether or not the charge pump is operating.

There are three factors involved in determining whether or not the charge pump is on, the charge on signal described in the overview, the sleep signal, as well as the 3.2trip signal. When the Charge on signal is low, the LDO supply voltage is high enough such that a charge pump is not needed to create the internal supply voltage. Therefore, a low charge on signal will always result in a low run signal regardless of the state of the other two factors. When the charge on signal is high, the charge pump's state is determined by the other two factors, the sleep signal and the 3.2 trip signal. The 3.2 trip signal is a comparator that is high when the internal supply voltage is above 3.2 volts. If the device is not in sleep and the charge on signal is high, the run signal will be high and the charge pump will operate. If the device is in sleep but the internal supply has not reached the 3.2 trip point, the charge pump will continue to operate until the 3.2 trip point is reached. For internal supply voltages above 3.2 volts, if the part is in sleep, the run signal will be low and the charge pump will not operate. The device will remain in this state until the part wakes from sleep or until the low load lowers the voltage on the reservoir capacitor enough to trip the lower threshold of the 3.2 trip comparator. The charge pump will then turn on and charge the internal supply capacitor until 3.2 volts is reached again. A summary of the operating conditions can be seen in the truth table (Table 3.1).

Table 3.1: Desired Operating Conditions

Chargon	Sleep	3.2trip	RUN	$\overline{RUN}$
1	1	1	0	1
1	1	0	1	0
1	0	1	1	0
1	0	0	1	0
0	1	1	0	1
0	1	0	0	1
0	0	1	0	1
0	0	0	0	1

The truth table above can be created using a pair of NAND gates and an inverter and is shown in Figure 3-11.

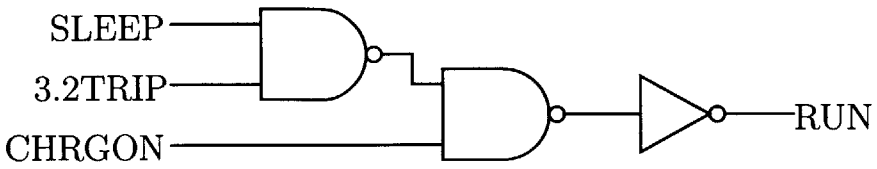


Figure 3-11: Logic used to make RUN Signal

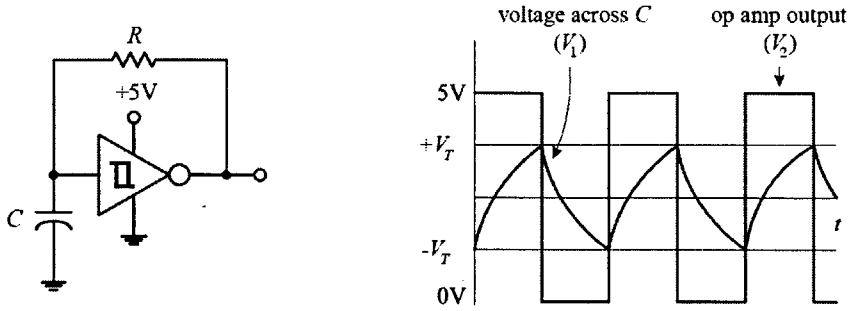
3.6 Charge Pump Oscillators

The design of the charge pump to be used in the LDO block is a constant frequency charge pump. An oscillator is required to set the rate at which the charge pump circuitry switches from charging the flying capacitor to charging the reservoir capacitor. The LTC3624 has an oscillator built into the die. However, this oscillator can only operate when the LDO Ready signal is high and the part is not in sleep. A secondary oscillator is required when the charge pump is needed to bring the internal supply voltage high enough to trigger a high LDO Ready signal. The secondary oscillator is built using a Schmitt Trigger Resistor-Capacitor oscillator design.

3.6.1 Schmitt Trigger Oscillator Design

A Schmitt trigger oscillator is used to control the charge pump when the output voltage is low. Figure 3-12a is the basic design for the Schmitt trigger oscillator. When the capacitor voltage (Vc) is less than the V+ threshold, the output voltage is VCC. This creates a positive voltage drop across the resistor thus charging the capacitor. Once the threshold is met, the output will be changed to ground. A negative voltage drop across the resistor will result in the discharging of the capacitor lowering the input voltage of the Schmitt trigger. Once the low threshold is met the

output will return to VCC and the cycle repeats.A plot of the input and output nodes can be seen in the figure 3-12b.



(a) Schematic (b) Waveform

Figure 3-12: Schmitt-trigger oscillator and voltage waveforms[2]

Add-ons to a basic Schmitt trigger have been made to fit the operation of the oscillator. The oscillator must be able to be turned on and off. A NAND gate provides this functionality. A low signal will lock the output low and the input eventually low as well. A high run signal will cause the NAND gate to act as an inverter with the output of the Schmitt inverter as the inverter. A third inverter is added so that the output is opposite the input when the device is operating. The design can be seen in Figure 3-14.

3.6.2 Oscillator Frequency

The LTC3624's oscillator operates at roughly 2MHz. Although the design will be made such that neither this oscillator or the Schmitt trigger oscillator will be running at the same time, the goal is still to make the Schmitt trigger oscillation frequency roughly 2MHz. Doing this will result in similar overall operation of the charge pump regardless of the state that it is in and regardless of which oscillator is controlling its gate. Furthermore there will be a much smoother transition when the charge pump changes from being controlled by the Schmitt to being controlled by the LTC3624. The frequency of the Schmitt trigger oscillator can be made by considering the amount of hysteresis in the Schmitt trigger, and the sizing of the resistor and capacitor. The resistor and the capacitor creates the time constant. The equations below show the

relationship between component values and frequency.

$$V_t = (V_{final} - V_{initial})\left(1 - e^{\frac{-t}{RC}}\right) + V_{initial} \tag{3.4}$$

$$V_{th+} = (V_{CC} - V_{th-})\left(1 - e^{\frac{-t}{RC}}\right) + V_{th-} \tag{3.5}$$

$$t = -RC\ln\left(1 - \frac{V_{th+} - V_{th-}}{V_{CC} - V_{th-}}\right) \tag{3.6}$$

$$frequency = \frac{1}{period} = \frac{1}{2t} \tag{3.7}$$

Iit is not easy to determine by hand the values of V_{th+} and V_{th-}. The thresholds values are highly dependent on VCC voltage as well as the rate of change on the input voltage into the Schmitt. Simulating the Schmitt-NAND-Schmitt design will allow us to determine the threshold voltages needed to determine the resistor and capacitor values. To get the threshold values, we will ramp up and down an input voltage and measure the trip points on the output. As the goal is to operate at a 2MHz frequency, we will change the voltage over a 500ns period. A plot of the input and output can be seen in figure 3-13

Using the plot, the threshold voltages are 1.4 and .4 volts. Using equation 3.8 and setting the capacitor to 5pf, one can solve for the value of R.

$$R = \frac{1}{2fC\ln\left(\frac{V_{CC}-V_{th-}}{V_{CC}-V_{th+}}\right)} \tag{3.8}$$

Since the Vcc voltage of the digital devices are connected to the maxer, as the charge pump operates, the maxer voltage will eventually increase once the output voltage of the charge pump surpasses the input voltage. Because of these changes in VCC voltages and threshold values, we expect the frequency to increase as the voltages increase. A higher frequency should result in lower amount of voltage ripple on the output. Since only one oscillator is operating at a time, the variation in frequency should not be in an issue in overall operation of the device. The LTC3624 oscillator will run the charge pump once the ldordy signal is high so that only one oscillator is

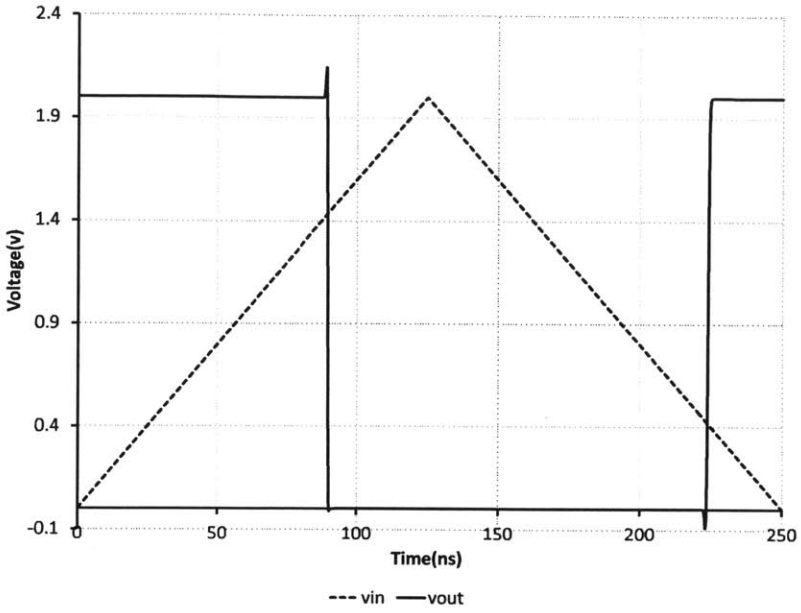


Figure 3-13: Plot of Schmitt-NAND-Schmitt output

being used. The final design with component calues can be seen in Figure 3-14.

3.6.3 Final Design Schematic

The final design of the Schmitt trigger with NAND gate shutoff can be seen in Figure 3-14.

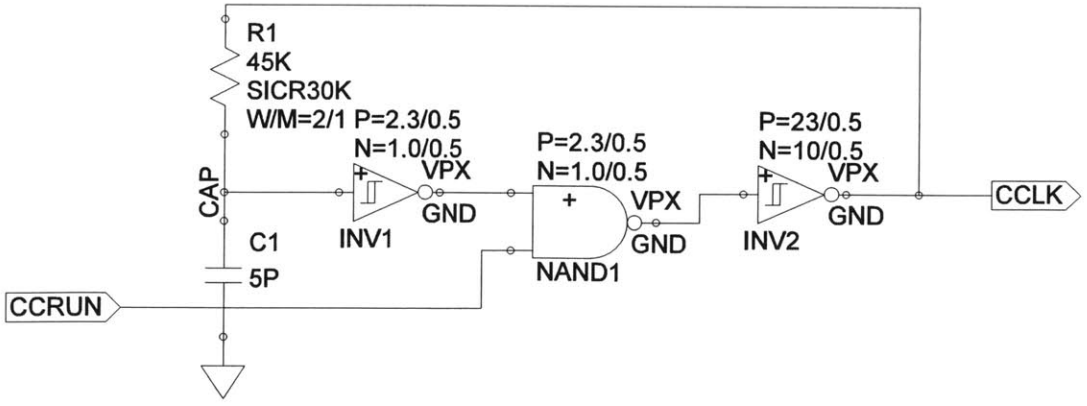


Figure 3-14: Complete design of Schmitt Trigger Oscillator

3.6.4 LTC3624 Oscillator

As shown in the charge pump block diagram (figure 3-4), when the output voltage is high enough, the original chip oscillator will be used. However, the clock used to replace the Schmitt trigger oscillator is not exactly the clock used to control the switching for the part as a whole. In this chip, the clock signal is only high for a very small portion of the clocks period, as its purpose is just to signal that the top-side device should be turned on. The short duration of the clock signal being high is insufficient for this application. A High clock represents the time in which the fly capacitor is being charged. With a short duration, the flying capacitor wont be charged and the overall $V_{IN}+$ flying capacitor voltage wont be very high which leads to issues when it comes to charging the internal supply reservoir capacitor. A desired clock signal would be one with a 50% duty cycle. This will provide time for both stages of the charge pump to operate.

This oscillator clock can still be used to operate the charge pump with a few additions. The CLKDIV2 signal is a clk that is generated using the clock signal and a latch. With the latch, the CLKDIV2 signal will become high at the first occurrence of a high clock, and will only return low on the next high clock signal. The end result is a clock with a 50% duty cycle. This signal could be used to operate the charge pump, however, the period of this signal is twice that of the original clock.

To create a 50% duty cycle clock that has the same operating frequency as the die oscillator, a pair of one shots are used. A one shot is a technique used to create a delayed rising or falling edge.

The delay associated with the one shot is associated with the sizing of the resistor and the capacitor. However, The LTC3624 is expected to operate at either 1MHz or 2.25MHz. Additional capacitors are added in parallel to the original capacitors to increase capacitance when operating on the 1 MHz frequency. Transistors and a 1MHz signal is used to determine when the additional capacitance is added to change the RC time constant. It is important to note however that since the 1MHz and 2.25 MHz 3624s are actually two separate parts, this functionality will not be used and in

actual design would be removed and the RC sizing would be made based on the part (1Mhz or 2.25MHz).

The NOR gate is added to ensure that the one shot is only operating under certain conditions. If we recall from section 3.5, the clock selection is dependent on the run and sleep signals. A low run signal resulted in a high clock selection suggesting that this 50 clock signal was needed. Without the nor gate this one shot would run whenever the original oscillator was running which in some cases would be a waste of energy is the oscillator was not needed. The 50% clock schematic can be seen in Figure 3-15.

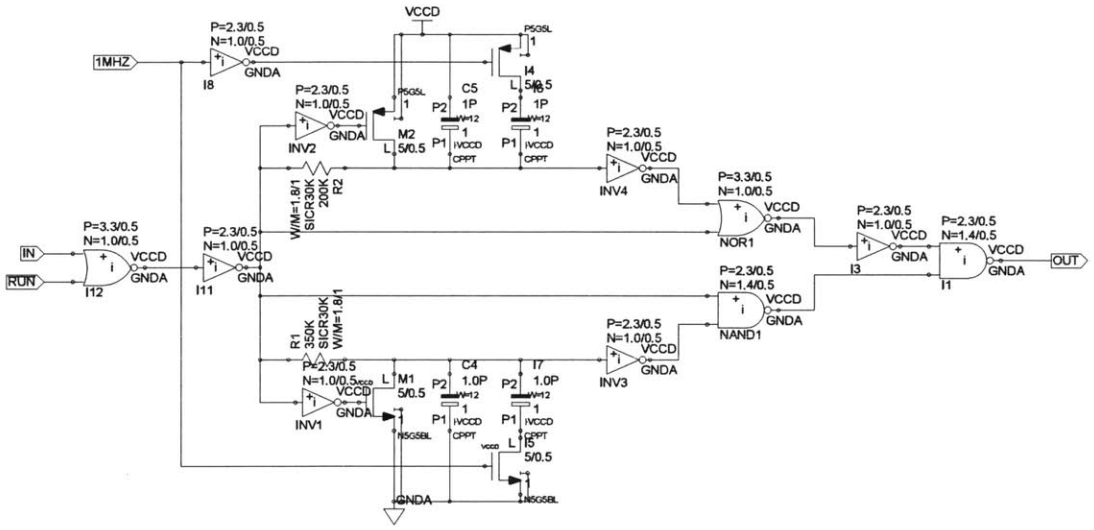


Figure 3-15: 50% clock

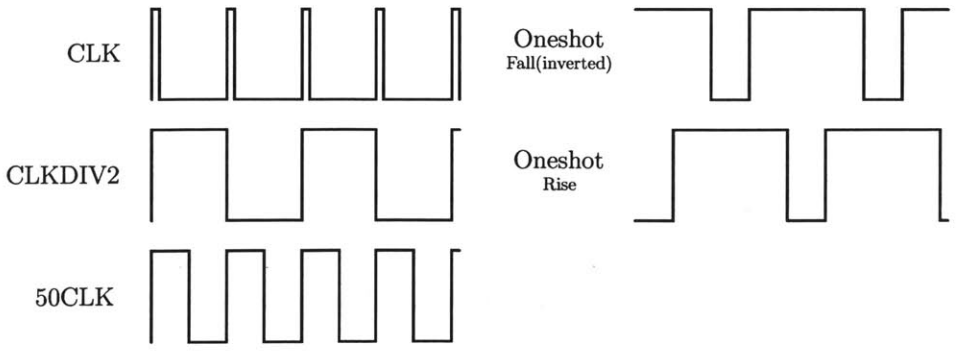


Figure 3-16: 3 input NAND gates that creates clk signal

3.6.5 Oscillator Selection

Now that both oscillators have been designed, a decision must be made as to which oscillator should be used for controlling the charge pump switches. The charge pump can be run by either the LTC3624 oscillator or the Schmitt trigger oscillator. To reduce noise between the charge pump circuitry and the rest of the parts circuitry, whenever the LTC3624's oscillator is running, the charge pump will also operate with that oscillator. From Table 3.1, there are 3 states that will result in a high run signal. Since there is no case where run is high and chargon is low, that factor will be ignored. LDOReady signal will be introduced to the calculations creating 6 possible states. However, two of these states are not possible. The sleep circuit block incorporates the LDO Ready signal. If the LDO Ready signal is low, the part is put in sleep mode, so the sleep signal is high. Therefore all states where LDO Ready signal is low and sleep signal is low can be ignored. The LTC3624 oscillator block does not operate when the part is in sleep. Looking at the remaining four states, if the part is in sleep, the charge pump will need to be operated using the Schmitt trigger oscillator. When the sleep signal is low, the LDO ready signal is high which means that the ltc3624 oscillator is operating and can be used for the charge pump. Because of how the LDO Ready signal is factored into the sleep state, looking at the LDO ready signal is not necessary. Furthermore, the 3.2trip signal is factored into the run signal and so is not needed in determining the clock. In the end, the selection of the clock is determined by a comparison between the run signal and the sleep signal. The reduced truth table above can be created with a NAND gate.

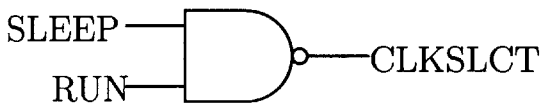


Figure 3-17: NAND to make CLKSLCT signal

If the clock select node is high, the output of the NAND gate paired with the LTC3624 oscillator is the inversion of the oscillator. A low clock select signal will make the output of the NAND gate high regardless of the behavior of the LTC3624

Table 3.2: Desired clock selection based on various inputs

RUN	LDORdy	Sleep	3.2trip	Clk Select
1	1	1	0	0
1	0	1	0	0
~~1~~	~~1~~	~~0~~	~~1~~	~~1~~
~~1~~	~~0~~	~~0~~	~~1~~	~~0~~
1	1	0	0	1
1	1	0	0	1
~~1~~	~~0~~	~~0~~	~~0~~	~~0~~
0	-	-	-	1

oscillator. A NAND gate is also added to the output of the Schmitt trigger oscillator. The input into this NAND gate will be an invert clock select signal. The $\overline{clkslct}$ signal will also serve as the run signal for the Schmitt trigger oscillator. A high *clkslct* signal results in a low $\overline{clkslct}$ signal. A low signal into the Schmitt oscillator's NAND gate will lock the output low. The output of the following NAND gate will therefore be locked high due low Schmitt oscillator output. If *clkslct* is low, The Schmitt trigger will run normally and the output of the exterior NAND gate will be the inverted output of the Schmitt trigger oscillator.

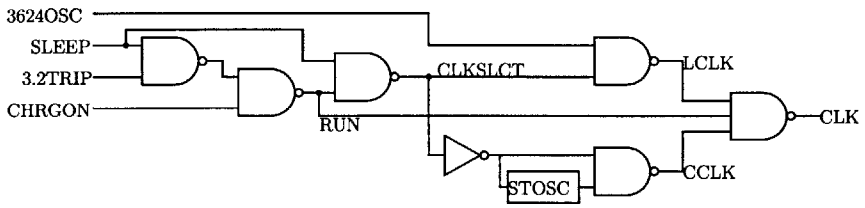


Figure 3-18: Complete Clock selection with inputs

The last step in creating the clock is to combine the output of the NAND gates. A three input NAND gate is used to create the clock input. The three inputs are the two outputs of the previously described NAND gates as well as the run pin. A low run signal will lock the clock output high regardless of the NAND gates' behavior. If the run signal is high, then the clock is the invert of the output of the NAND gate that is not locked high by the clock select node. When the LTC3624 oscillator is used, the two inversions make it such that the charge pump clock is in sync with the

oscillator which reduces noise.

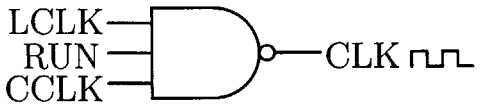


Figure 3-19: 3 input NAND gates that creates clk signal

Table 3.3: Truth Table of 3 input nand

LCLK	RUN	CCLK	CLK
1	0	1	1
1	0	ON	CCLK
ON	1	1	LCLK
ON	0	1	1

Furthermore, the run pin serves as an override. In the case where run is low, it was chosen that the clock select be high. In the cases where run is low but the LTC3624 oscillator is operating, there will be a clock signal going to the input of the three input NAND gate. However, the low run signal will still result in a locked high output. This situation has almost no additional power loss because the LTC3624 oscillator is already running to operate other circuit blocks.

3.7 Gate Control

The design of this charge pump was based off an existing charge pump, the LTC3200. The gate drive was one of the components that remained largely unchanged from the LTC3200.

The gate drive was designed to prevent shorting while switching. It was made sure that switch 2 and 3 were never on at the same take time, as well as switch 1 and 4. The gate of switch 2 is controlled by G2N. A High G2N signal guarantees a high output signal at NAND devices 2, 6 and 8 and result in a low signal at EN3 which controls the gate of switch 3. Similar behavior occurs with switches 1 and 4. The G4P signal controls the gate of switch 4. A low G4P signal turns on switch 4. This

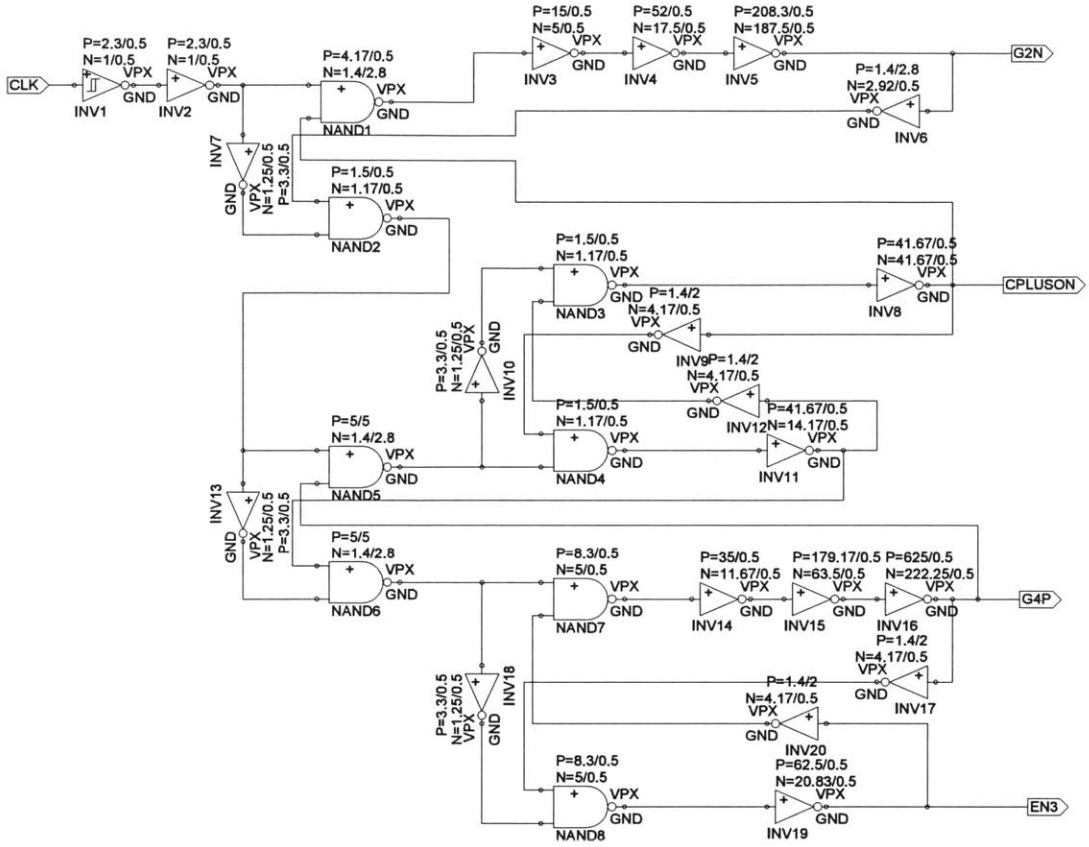


Figure 3-20: Gate drive for chargepump switches

guarantees high signals for NAND devices 5 and 3 which results in a low CPLUSON signal which turns off the current mirror switch 2. The CPLUSON signal cannot change until G4P signal is high.

3.7.1 Operation

The gate drive is designed such that only 1 switch changes its state at a time. On the falling edge of the clock signal, the low top input to NAND1 results in the G2N signal to be the first of the 4 switches to change states. NAND2 is in a lock state due to an inverted G2N signal. As G2N was previously high, the NAND2 was locked high. Once G2N becomes low the high top input is joined with an inverted clk signal creating a low NAND2 output. This low value makes the output of NAND5 high and the output of NAND3 high as well. Note that NAND4 and NAND6 are not

immediately affected by these changes due to a previously high CPLUSON signal. The high NAND 3 signal results in a low CPLUSON signal and switch 2 becomes the second switch to change states. The CPLUSON signal links back to the NAND1 device, locking its state. The low CPLUSON signal causes there to now be two high inputs into NAND4 changing its output to low. The low output cause there to now be two high inputs at NAND6 changing its output to low. Furthermore this low output causes the bottom input of NAND3 to be low, locking its state. The low output of NAND6 leads to a high output at NAND7 and a low G4P signal, making switch 4 the 3rd switch to change states. NAND8 is not immediately affected by the change in the NAND6 output because G4P was previously high. G4P signal links back to NAND5, and once G4P becomes low it locks the state of NAND5. Furthermore, Once G4P becomes low, NAND8 now has 2 high inputs, making the output high and EN3 becomes high making switch 3 the last switch to change states. A high EN3 output makes the bottom input to NAND7 low locking its state. In conclusion, on a falling edge, the switches change states in the following order; Switch2, which changes from being closed to open, Switch 1, which also changes from being closed to open, Switch 4, which changes from being open to closed, and lastly switch 3, which changes from being open to closed.

When the rising edge of the clk signal comes around, NAND1, 3, 5 and 7 are in lock states. The high clock signal makes the output of NAND2 high, followed by the output of NAND6 followed by the output of NAND8 making EN3 low and switch 3 is the first switch to change states. The low EN3, unlocks NAND7 which now has 2 high inputs and causes G4P to high, making switch 4 the second switch to change states. The high G4P locks NAND8 and unlocks NAND5 which now has 2 high inputs making its output low. This low output changes the output of NAND4 high which locks the state of NAND6 and changes the bottom input of NAND3 to high. NAND3 now has two high inputs making its output low and changing CPLUSON high making switch 1 the third switch to change. A high CPLUSON locks NAND4 and unlocks NAND1 which now has 2 high inputs changing G2N high making switch 2 the final switch to change states. NAND2 becomes locked in the process. In conclusion, on

a rising edge, the switches changes states in the following order; Switch 3, which changes from closed to open, Switch 4, which changes from closed to open, Switch 1, which changes from open to closed and lastly Switch 2 which changes from open to closed.

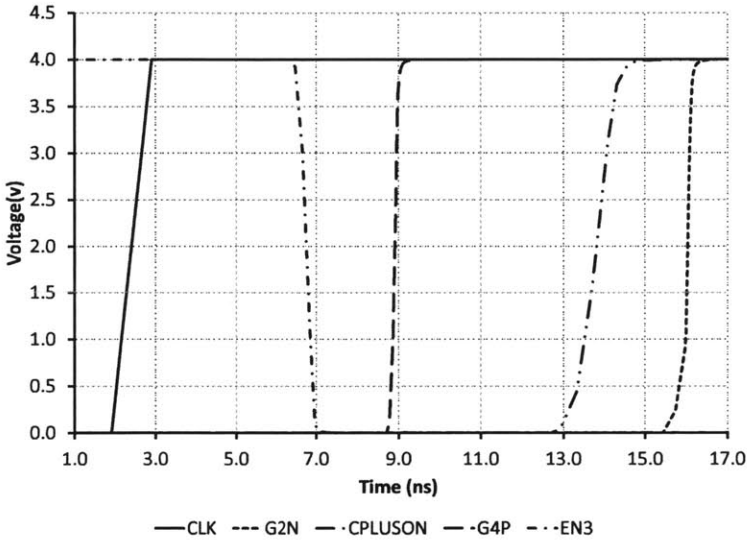


Figure 3-21: Plot of switch responses to rising clk edge

3.7.2 Switches

The 4 switch signals operate the charge pump as follows. A PMOS transistor is used to create switch 4 and is controlled by the G4P signal. An NMOS transistor is used to create switch 3 and is controlled by the EN3 signal. Switch 1 and switch 2 are created using current mirrors. The current mirrors are controlled by controlling the gates of the current mirror.

3.8 Maxer

One thing to consider when building this charge pump is how to power it. As shown in the charge pump block diagram (figure 3-4), the maxer takes the input and output

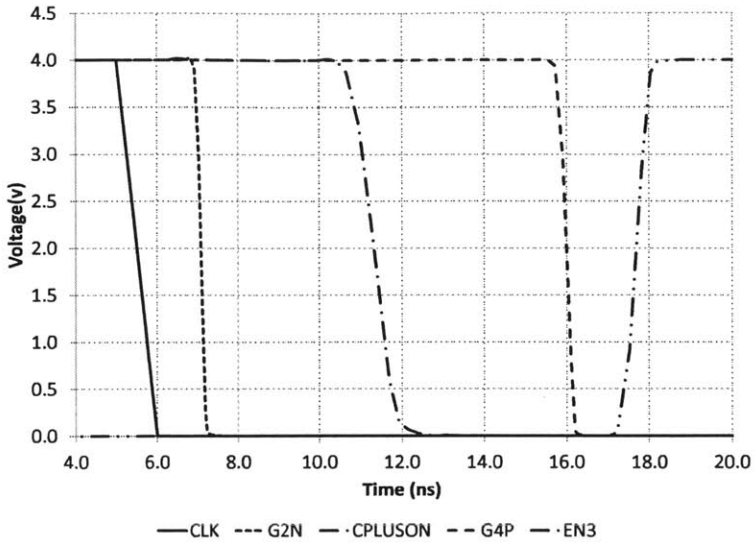


Figure 3-22: Plot of switch responses to falling clk edge

voltage of the charge pump and outputs to the charge pump and its relevant circuitry the higher of the two voltages. This circuit is particularly useful when the chip is first turned on. Since the internal supply voltage may not be high enough at early stages of creating the internal supply another voltage must be used at the early stages. In our situation, The maxer will compare the voltage in to the charge pump (LDOVCC) as well as voltage at the output of the charge pump (V_{OUT}). At the early stages the LDOVCC voltage is expected to be higher, but as the reservoir capacitor charges V_{OUT} will eventually surpass LDOVCC and V_{OUT} will then be used to power the charge pump and its control circuitry.

The maxer circuit works in part due to the use of current mirrors. However, instead of the normal configuration in which the transistors share the same source, the transistors involved in the PMOS current mirror have different sources. The amount of current in these transistors is highly dependent on the source to gate voltage. The transistors will share the same gate voltage meaning that the output current is entirely dependent on the sources.

The maxer circuit can be seen in Figure 3-23. A current source gets mirrored to 2 NMOS transistors. The two NMOS transistors are connected to a PMOS device

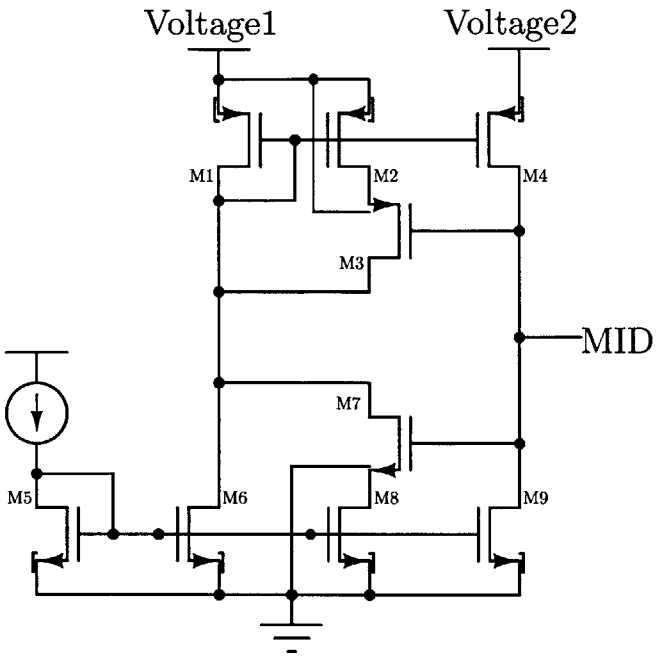


Figure 3-23: Currrent mirror based maxer circuit

whose source voltage is connected to one of the 2 voltages we are trying to compare. The PMOS devices are connected in a current mirror configuration. If voltage 1 is greater than voltage 2, then the right most PMOS will not be able to supply enough current to match the NMOS transistor. This will force the NMOS transistor into deep triode and the mid voltage will be pulled to ground. Alternatively if voltage 2 is higher the PMOS current will exceed that of the NMOS transistor. The PMOS will be forced into deep triode and the mid voltage will be pulled to the source voltage. The M2 and M3 pair as well as the m7 and M8 pair adds hysteresis to the current mirror to help the mid voltage reach either its low or high state. If the mid voltage lowers towards ground, the M3 transistor will turn on sourcing some of the NMOS current and reducing the amount of current for the M1 transistor. This will lower the current in the M4 transistor due to a higher gate voltage. This will increase the difference in current between the NMOS and PMOS transistor. Similarly, when the mid voltage increases, the M8 transistor turns on increasing the amount of sink current to the branch. This will increase the PMOS current and the NMOS-PMOS

current difference.

The output of the mid voltage represents the higher voltage, where ground voltage means voltage1 is higher and a high voltage means voltage 2 is higher. To create this into a voltage source that equals the higher voltage, the circuit shown in figure 3-24 is used. The output of the mid node goes through an inverter connected to voltage 1 and ground. The inverter has these sources because if the mid voltage is voltage 2, then it must be higher than voltage 1 and the output of the inverter with certainly is ground. The output of the inverter goes to another inverter powered by voltage 2 and connected to ground. If voltage 1 was the output of the first inverter then voltage 1 is larger than voltage 2 so the output of the second inverter will certainly be ground. If the output was ground, the output would be V_{OUT}. This powering configuration prevents shoot through in the inverters. The outputs of the inverters serve as gate voltages for 2 PMOS transistors that connect the 2 voltages. VPX will be the node voltage in between the two PMOS transistors. Since the gate voltages are complementary only 1 PMOS device will be on at a time. The on transistor will be forced into deep triode due to the other PMOS being off. VPX will be pulled to the source of the transistor in deep triode. It is important to notice that the gate of the transistor that is supposed to be shutoff is always connected to the higher voltage. This insures complete shutoff of the transistor and reduced leakage current.

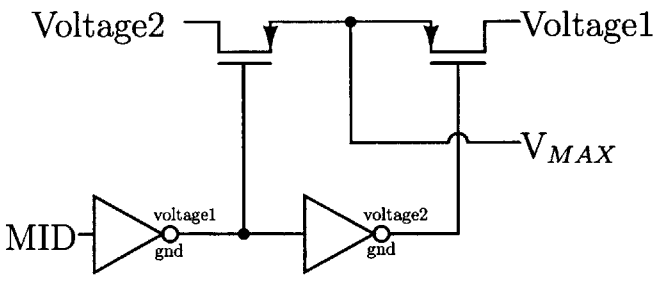


Figure 3-24: PMOS voltage selection for maxer

3.8.1 Maxer Shutoff

Similar to the gm amplifier, the Maxer circuit block does not always need to be operating. Just like the transconductance amplifier, the LDO will supply current (240nA) to the maxer using a PMOS current mirror. An added PMOS device allows a signal to shut off current going into the maxer circuit. To further prevent current within the maxer, an NMOS device is added to the gates of the NMOS current mirror. A high signal will pull the gate voltage to ground preventing mirrored current.

Although the maxer may not always need to be functioning, since the output of the maxer (VPX) is used as the supply voltage for the charge pump control circuitry, VPX cannot be left floating when the maxer is not operating. The maxer needs to be either tied to V_{OUT} or V_{IN}. When the charge pump is off, V_{OUT} is floating and the internal supply voltage is roughly equal to the LDO supply voltage which serves as the input to the charge pump. In this case, the maxers output (VPX) should be V_{IN} regardless of whether or not the run signal is high.When the charge on signal is high, If the run signal is low then based on the how the run is designed, the V_{OUT} of the charge pump must be above 3.2 volts. Since the charge on signal is high, the LDO supply voltage (V_{IN}) must be less than or around 3.2 volts. V_{OUT} is therefore larger than V_{IN} and the output of VPX should be V_{OUT}. When the Run signal is high, the maxer will function normally.

To control the maxer output, a PMOS and an NMOS device are added to the mid node of the maxer circuit. When the PMOS is on and the NMOS is off, the mid node voltage will be V_{OUT} and VPX will equal V_{OUT}. When the NMOS is on and the PMOS is off, the mid node voltage will be pulled to ground and VPX will be equal to V_{IN}. When both devices are off, the maxer operates normally. A summary of desired maxer outputs and required PMOS and NMOS signals can be seen in Table 3.4 below.

The desired signals can be made using a few digital devices as seen in Figure 3-25. It is important to know that because both the PMOS and NMOS logic use the charge on signal, it is not possible for both the PMOS and NMOS transistors to be on at

Table 3.4: Table of Maxer outputs based on varied inputs

RUN	$\overline{RUN}$	chargon	Maxer	PMOS	NMOS
0	1	1	V_{OUT}	0	0
0	1	0	V_{IN}	1	1
1	0	1	ACT	1	0
1	0	0	V_{IN}	1	1

the same time.

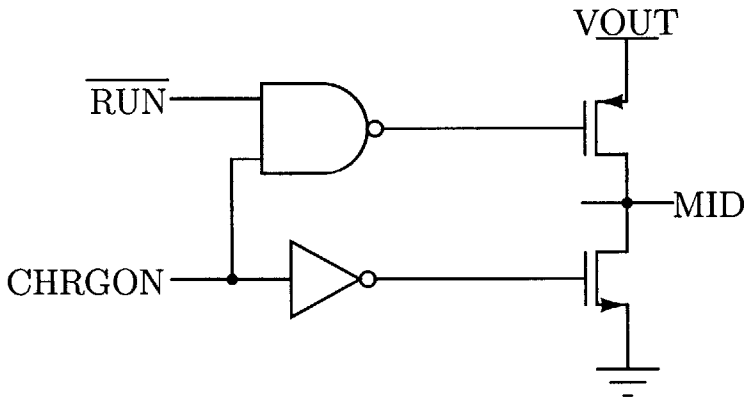


Figure 3-25: Maxer position overide circuitry

3.8.2 Final Maxer Design Schematics

The final maxer design with transistor sizing and shutoff circuitry can be seen in Figure 3-26.

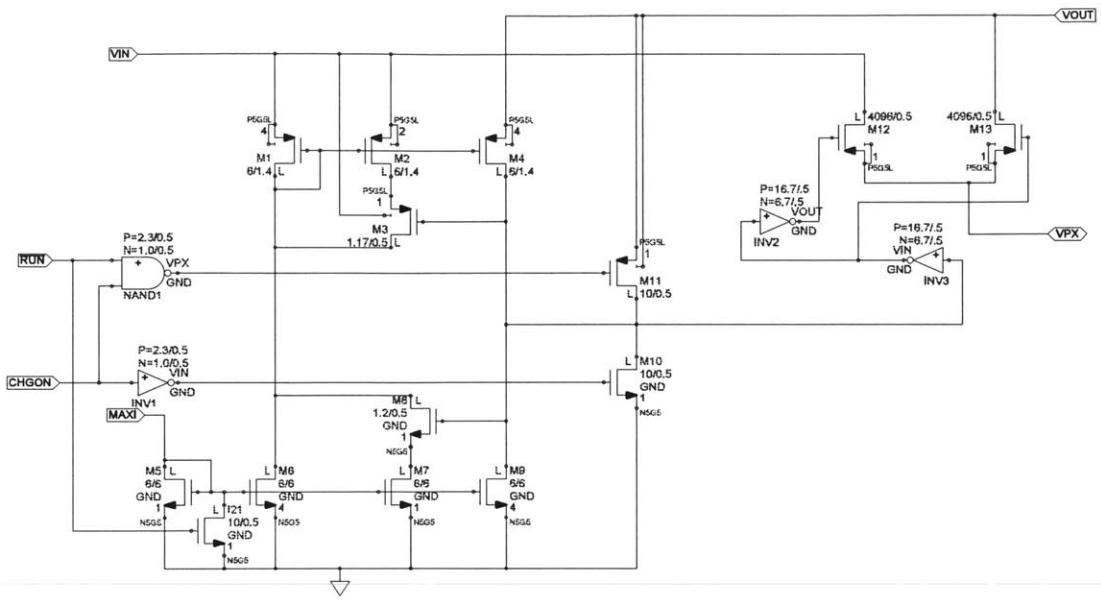


Figure 3-26: Complete design of maxer circuit

3.9 Final Design Charge Pump

The final design schematic for the charge pump that incorporates the maxer, run control circuitry, Schmitt trigger oscillator and clock selection can be seen in Figure 3-27.

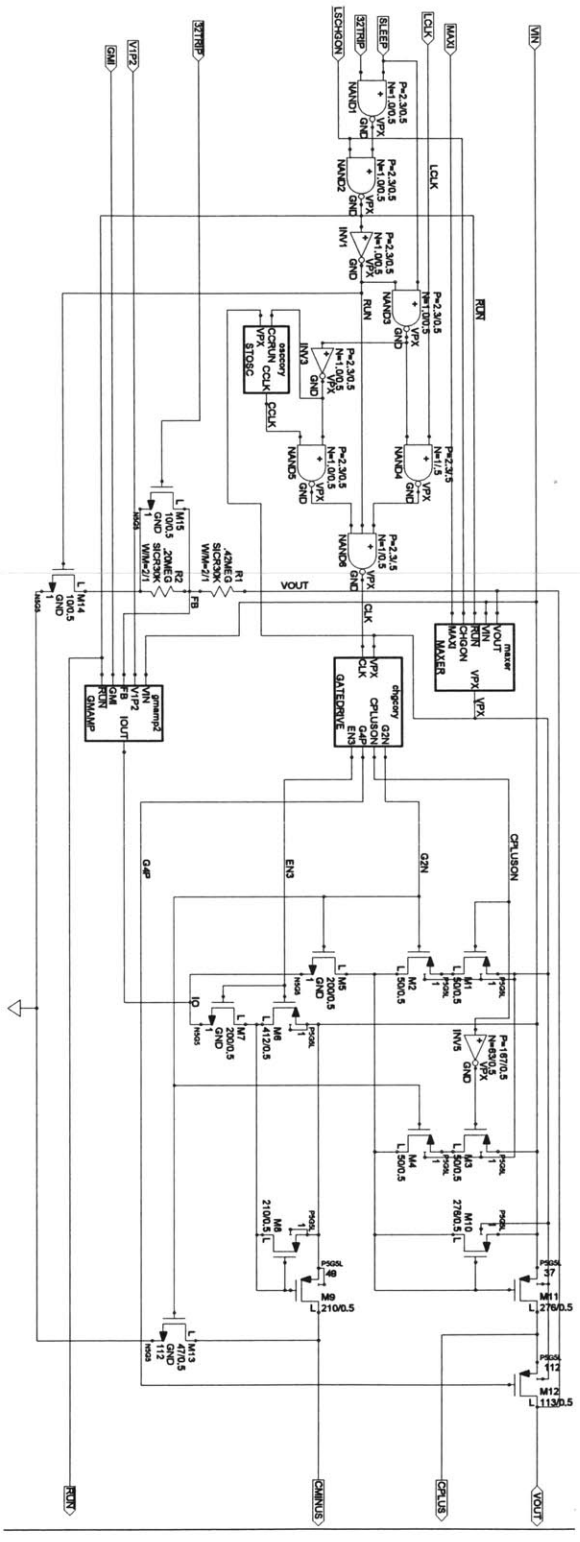


Figure 3-27: Complete design of charge pump block

Chapter 4

LDO Charge Pump Integration

With the addition of a Charge pump, changes must be made to the LDO to integrate the charge pump. Figure 4-1 shows a block diagram of the new ldo design.This chapter will discuss the signals added to operate the charge pump, the switch implemented to control the LDO output and the current supply for the charge pump.

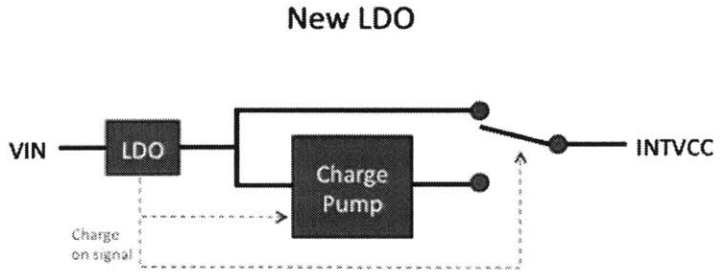


Figure 4-1: New LDO Design with Integrated Charge Pump

4.1 SPDT Switch

As shown in Figure 4-1), the new LDO will be able to switch between what is attached to the internal supply output (LDOVCC or the charge pump output). To implement this functionality, a Single Pole Double Through (SPDT) switch will be created.This switch is implemented using two PMOS devices. Figure 4-2 are the SPDT PMOS switches controlled by the level shifted charge on signal, which will be explained

in the later section, and its inverse. It is important to notice that in both of these PMOS devices, the substrate is tied to the internal supply voltage (drain of the PMOS device). The reason for this is that at steady state, the internal supply voltage is equal to or higher than the voltage at the labeled source of the PMOS. If the LDOVCC $\rightarrow$ INTVCC switch had the substrate tied to the LDO supply voltage and the input voltage was not high enough and the charge pump was needed, then the internal voltage would be brought up to a voltage higher than the LDO supply. At this point, back-biasing current would flow from the internal supply back to the LDO supply essentially acting like an additional load for the charge pump. This setup would prevent the internal supply voltage from reaching the desired voltage. Similar statements can be made for if the charge pump switch had the substrate tied to the charge pump output though the penalties would not be as severe as the charge pump, in its off state, has the switch that connects to the flying capacitor open. There are a few cases where the LDOVCC voltage or the charge pump output voltage is higher than the internal supply output. In fact, since there is a voltage drop over the transistor when its on, this is often the case. However, the transistors are sized to minimize the voltage drop. Furthermore slight leakage into the internal supply may be beneficial in bringing the internal supply cap to the desired voltage.

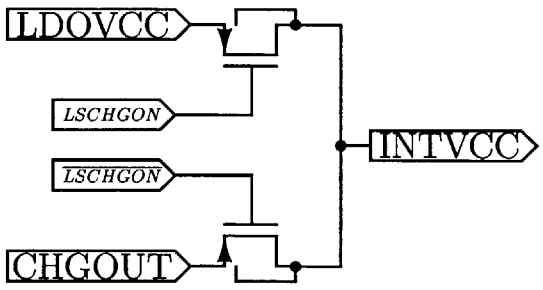


Figure 4-2: SPDT switch with charge on control

4.2 Level Shifted Charge on signal

The signal that controls the SPDT is the Level Shifted Charge On Signal (LSCHGON). As the name suggest this signal is the level shifter version of the charge on signal used to determine whether or not the charge pump needs to used. The Chargeon signal comparator is powered by the LDOVCC. The use of the level shifter is extremely important for both PMOS devices. When the internal supply is voltage is created by the charge pump output, the transistor connecting the LDO supply to the internal supply should be off. Although the labeling suggests that the LDO supply node is the source and the internal supply node is the drain, once the internal supply voltage surpasses the LDO supply voltage, these labels switch and the internal supply voltage becomes the source and the LDO supply voltage becomes the drain. The source-gate voltage is now the difference between the internal supply voltage and the gate voltage. Since the gate voltage is no larger than the LDO supply voltage, if the magnitude of the gate voltage is over vtp smaller than the magnitude of the internal supply voltage, then the PMOS will turn on and current will flow from source to drain (internal supply→LDO supply). This makes using the LDOVCC voltage to turn the PMOS unsuitable. However, this issue can be resolved by using a higher voltage to control the gate.Assuming minimal voltage drop across the PMOS transistors, the internal supply voltage should always at steady state be equal or greater than the LDO supply voltage. Implementing the level shifter will insure that the higher voltage is used to turn off the PMOS transistor reducing leakage current. There are a few cases where the LDO supply voltage is larger than the internal supply voltage. For example, when the device has just been turned on and the charge pump is still in the process of bringing the internal supply up to the correct voltage. In this case, slight leakage current from the LDO supply to the internal supply is favorable as it will help to bring the internal supply voltage up quicker.

The basis behind a level shifter is rather simple as it takes advantage of transistor behavior and can be seen in Figure 4-3.The level shifter is built using 4 transistors, 2 PMOS and 2 NMOS. When the CHGON signal is high transistors M1 & M4 are

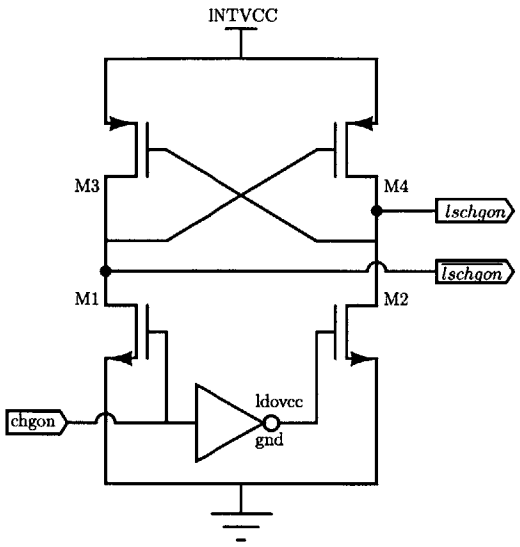


Figure 4-3: Charge on signal level shifter

on while transistors M2 & M3 are off. This makes the $\overline{LSCHGON}$ (drain of M1) signal low(ground) and the $LSCHGON$ (drain of M4) signal high(intvcc). Similarly, when CHGON is low M2 & M3 are on while M1 & M4 are off making $\overline{LSCHGON}$ high and $LSCHGON$ low. Each of these signals will connect to each of the 2 PMOS devices used to make the PMOS SPDT switch. As these signals are opposite one another. Only 1 PMOS device will be on at a time while the other is off.

4.3 Current Supply

The maxer and the gm amplifier are both devices within the charge pump that need external current to operate. The gm amplifier was design to use 1.5μA of current, while the maser circuit needs around 240nA. The LDO block will supplies these currents. The existing LDO block had an 80nA sink current supply. Using scaled current mirrors, we can source the required current needed for these devices to operate. Scaling the PMOS devices by 19 across the current mirror creates a current source of 1.52μA. Using another current mirror and scaling the PMOS devices by 3 across the current mirror creates a current source of 240nA. As stated in section X, there are

points in operation where the gmamp and maxer are not used. One of the techniques to prevent these devices from using any current in these states is to shut off current to the circuit blocks. A PMOS is added to each of the current mirrors allowing the shutoff of current to the blocks. A review of section X shows that these devices are not needed when the RUN signal is low. Therefore, the PMOS devices are controlled using $\overline{RUN}$ signal. Figure 4-4 shows the added circuitry.

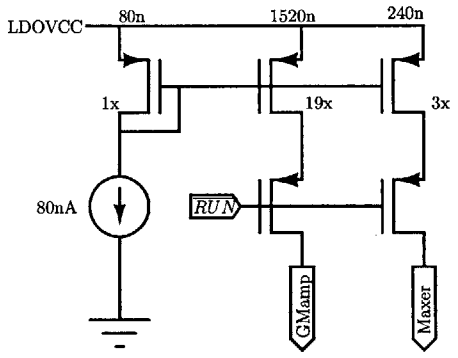


Figure 4-4: Controlled current sources for GMamp and Maxer

4.4 Comparator

In the original LDO block, a single comparator was used to determine whether or not LDO block provided an internal supply voltage high enough to operate the other blocks. This signal was the LDOReady signal. Two comparators have been added to the LDO block to create two signals described over the past 2 chapters, 3.2trip and Chargeon signals. The design of the comparator can be seen in figure 4-5. The mid node voltage is the input voltage to a Schmitt inverter. As the the two currents are compared, the mid voltage changes based on which transistor is being forced into deep triode. The output will therefore be either ground or the internal supply voltage based on what the input voltage is.

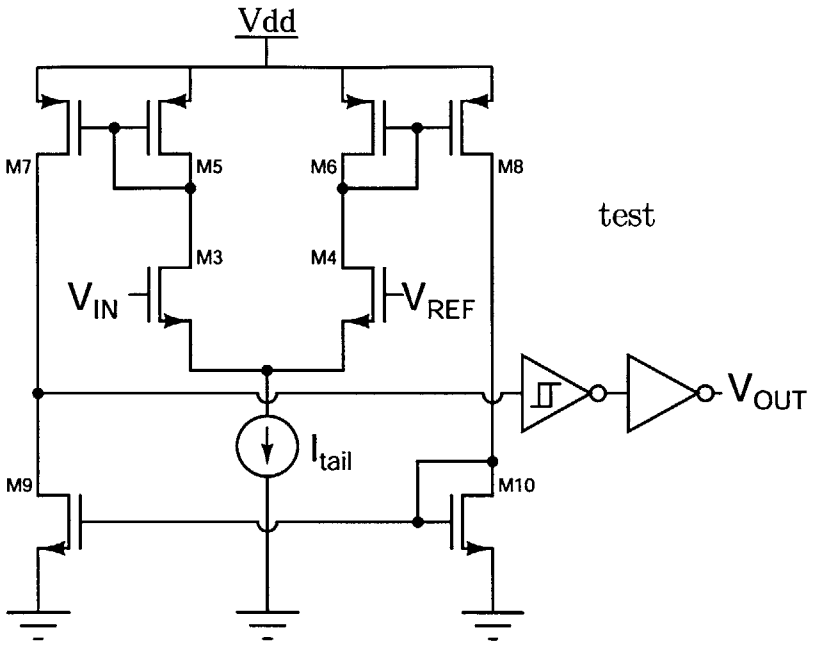


Figure 4-5: Comparator

4.4.1 Input Voltage & Hysteresis

DC hysteresis is added to the comparators in order to prevent false tripping or chatter at the output of the comparator. This hysteresis is implemented through the resistor branch used to set the input voltage into the differential amplifier. Mosfets placed in parallel with resistors in the resistor branch are added. On both rising and falling transitions, the changing state of the transistor is used to reinforce the transition in the desired direction by changing the voltage into the differential amplifier input. When the transistor is turned on, the resistor the transistor is in parallel will no longer be included in the voltage division equation. When this transitions occurs there will be a sudden change in the input voltage. Smoother transitioning is achieved with a Schmitt trigger prior to the output. This addition will allow resistor branch changes prior to changing the output.These jumps in voltage will will prevent the input from hanging around the trip points, which will reduce the chance of chatter and false trips. The gates of these transistors are controlled by the comparator output so that the first sign of a change in state will result in a change of the resistor divider.

The 3.2trip signal and the new LDO ready signal use the internal supply voltage to determine the signals state. As a current saving measure, the input voltage into each of the comparators will come from a shared current branch. We can do this because we expect the trigger points of the 3.2 trip signal to be higher in voltage than the trigger points for the new LDO ready signal in both the transition from high to low and low to high. As the name suggest, we would like the 3.2trip signal to trip at 3.2 volts. A branch with 5 resistors can be used to make comparator voltages with hysteresis for both signals. The equations below are for the rise and fall stages for each comparator. Resistors R4 and R5 are used to add hysteresis to the branch. R4 is used to add hysteresis to the LDOready comparator, while R5 is used to provide hysteresis to the 3.2 trip comparator. The resistor branch with hysteresis for both comparators can be seen in figure 4-6.

$$1.18 = V_R \frac{R2 + R3}{R1 + R2 + R3} \tag{4.1}$$

$$1.18 = V_F \frac{R2 + R3 + R4}{R1 + R2 + R3 + R4} \tag{4.2}$$

$$1.18 = V_R \frac{R3 + R4}{R1 + R2 + R3 + R4} \tag{4.3}$$

$$1.18 = V_F \frac{R3 + R4 + R5}{R1 + R2 + R3 + R4 + R5} \tag{4.4}$$

The desired trip voltages are as followed. For the LDO Ready signal, the desired rising and falling trip voltages are 2.8v and 2.5v respectively. For the 3.2 trip signal, the rise and fall are 3.2 and 2.9 volts respectively. With the above equations and desired values, there are 4 equations and 5 unknowns. To solve this predicament, one of the resistor values can be arbitrarily chosen or an equation representing the total sum of resistances in the branch can be added. The end resistor values are as followed: $24M\Omega$, $4.69M\Omega$, $13.94M\Omega$, $2.82M\Omega$ and $2.92M\Omega$ for resistors 1 through 5 respectively.

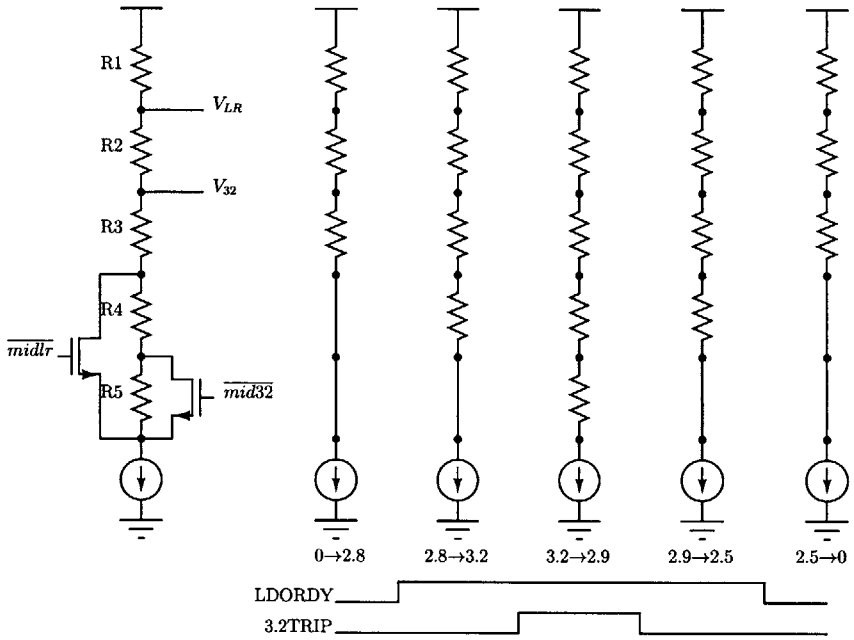


Figure 4-6: Resistor branch with hystersis stages

4.5 Final Design Schmatic

The newly designed LDO with Charge pump can be seen in Figure 4-7

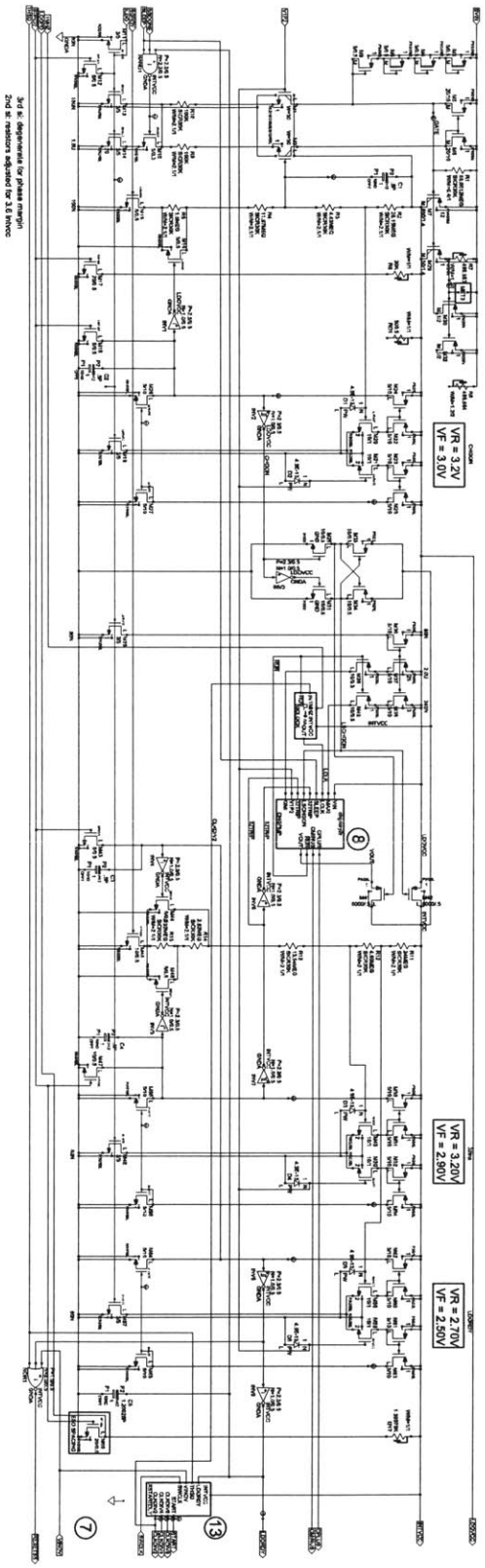


Figure 4-7: Complete design of new LDO block

Chapter 5

Top-side MOSFET

The current design of the LTC3624 has a PMOS device used for its top-side MOSFET and a NMOS devices for its bottom-side MOSFET. This PMOS device was most likely used for simplicity. Controlling the PMOS device would only require the use of 2 voltages; A V_{IN} voltage to turn the device off and a ground voltage to turn the device on. If the top-side were to be an NMOS, the control system would be more complicated. To turn on the NMOS device, a voltage above the switch node and the V_{IN} voltage would be needed. Although a PMOS requires simpler control circuitry, there are a few reasons why an NMOS device is a better choice for the top-side MOSFET. Electron mobility in an NMOS device is greater than hole mobility in a PMOS device. This results in lower on resistance for a given transistor size of an NMOS versus a PMOS. On resistance plays an important role in achieving the goal of higher efficiency at lower voltages. Higher on resistances lead to larger amounts of energy loss. In addition to having an inherently larger on resistance, the resistance of a PMOS device in the current configuration will increase even more as the input voltage decreases while the NMOS resistances tend to stay constant. This is in part due to the PMOS configuration. On resistance is effected by the gate to source voltage. In a PMOS device the input voltage serves as the source voltage. So the V_{GS} voltage is different for various input voltages. The resistance only becomes constant when device is fully in the saturation region. The NMOS used for the bottom side transistor has a constant V_{GS} voltage because the gate powered by the internal supply

voltage which remains relatively constant.The use of an NMOS device will lead to a constant and lower on resistance of the FET resulting in less conduction loss. On a less important note, NMOS devices tend to be faster than PMOS devices, which will lead to faster switching times. It is for these reasons that changing the top-side device to an NMOS is pertinent to achieving the proposed goal. Similar to state 2 of the charge pump, we will be using a charged capacitor to increase the voltage at the gate to be above V_{IN}. This chapter will go through the different circuit blocks built to make the gate drive circuity for the NMOS top-side MOSFET.

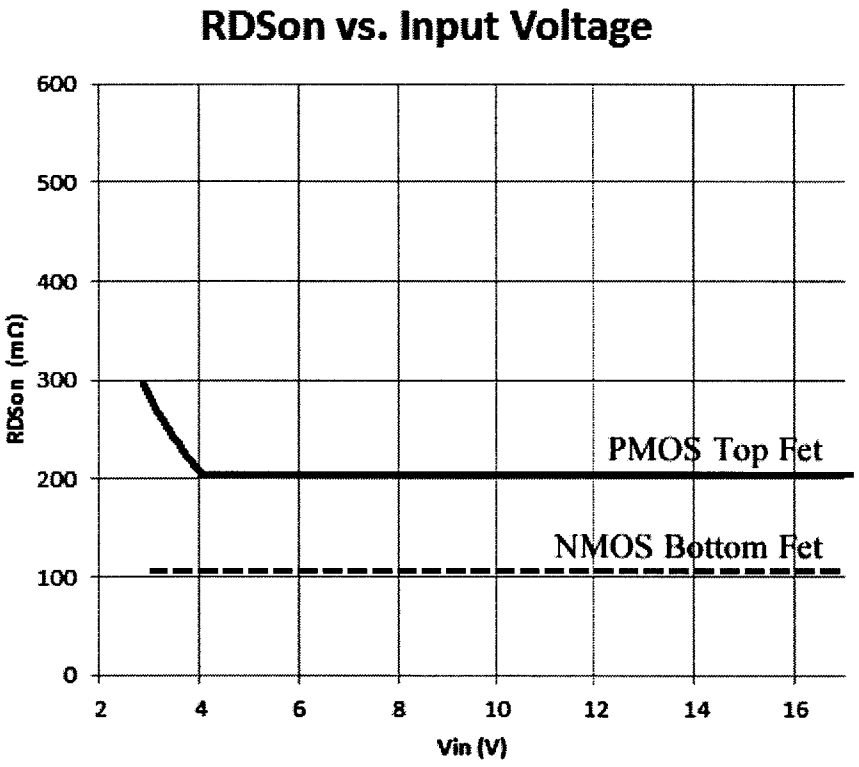


Figure 5-1: RDS_{on} of PMOS high side FET vs NMOS low side FET[1]

5.1 Design and Signal overview

The main mechanism behind turning on the top-side NMOS device is the use of a boost capacitor which will be explained more detail in the next section. To make sure

that this mechanism operates correctly, a few signals are used. A few of these signals will be defined here briefly to make it easier to understand the following sections that describe circuit blocks in more detail. The TON signal is a signal that is high when the Bottom side FET is off and the Gate drive signal is high. When high, it symbolizes that the Top gate can be turned on. This signal however ranges from ground to the internal supply voltage. An additional signal, TON_HS, is created based off of the state of the TON signal but ranges from the switch node to the Boost capactor node voltage. The Boostlow signal (BL) is high once the voltage of the gate on the top-side node is no longer significantly above the switch node voltage. This signal voltage ranges from SW to Boost. An additional signal, Top Gate Low (TGL), is created based off of the state of the BL signal but ranges from ground to the internal supply voltage.

5.2 Charging Boost Capacitor

Somewhat similar to a charge pump, a capacitor will be used to boost the gate voltage of the NMOS device. The boost capacitor is added to the switch node voltage. By charging this capacitor we create a voltage above the switch node. With appropriate charging, the Gate voltage will surpass the gate to source voltage of the NMOS device, turning on the transistor. At a high enough voltage the gate voltage will exceed the input voltage putting the device in saturation. Under normal operation, the internal supply voltage will be around 3.6 volts, and thanks to the charge pump circuitry added, we expect this 3.6 voltage even at low VINs. The internal supply voltage will be used to charge the boost cap. Since the boost cap is connected to the switch node, there are only certain instances in which the internal supply can charge the cap. When the top-side is on, the switch nodes is roughly equal to the input voltage. This would be problematic given the range of input voltages the devices is expected to operate at. However when the top-side device is off and the bottom side device is on, the switch node voltage is roughly equal to ground. It is for this reason that the boost capacitor can and will only be charged while the bottom-side device is on. The

circuitry involved in charging the boost cap can be seen in figure 5-2.

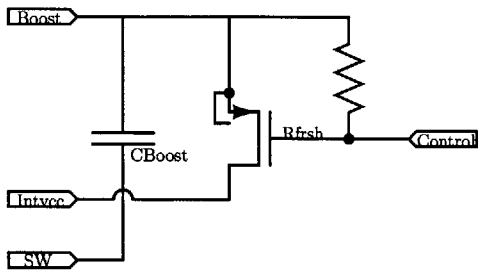


Figure 5-2: Boost Refresh

The control signal works in coordination with the bottom-side turn on signal. When the top-side is on and the bottom side is off, the $\overline{RFRSH}$ is pulled to Boost. Since the Boost signal will most likely be greater than the internal supply (V_{in} + $V_{C_{Boost}}$), the PMOS device is off and no current will flow back into the internal supply. This is also the reason why the substrate of the PMOS device is tied to the Boost node. When $\overline{RFRSH}$ is low, the bottom-side is on making the switch node voltage roughly ground. At this point the boost cap voltage will be less than or equal to the internal supply. Therefore the DRVCC (Internal Supply) will be the source for the PMOS device and the boost node the drain, and current will flow from source to drain charging the capacitor.

5.3 Changing Signal Voltages

5.3.1 Boost Low LTH

The boost low signal is generated by comparing the Top Gate voltage to the switch voltage. The gate of a diode connected NMOS with the source tied to the switch voltage is used to control a PMOS with its source tied to boost. If the boost voltage is more than a threshold voltage above the swtch, current will flow through the transistor creating a voltage drop accross across a resistor. This node voltage will increase as the boost voltage increases beyond the switch voltage as current flowing throught the resistor will increase. When this node voltage becomes high enough, it

will reach the trip voltage of the schmitt inverter and the $\overline{BoostLow}(\overline{BL})$ signal will become high, which means that the topgate voltage is high enough.

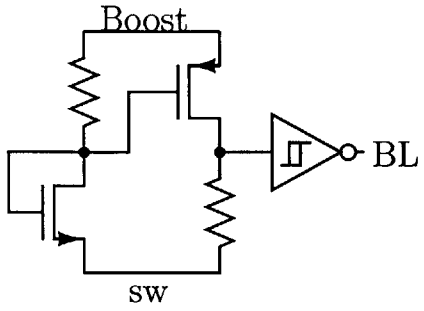


Figure 5-3: Boost low signal

The boost low signal is used to create a top gate low signal. One shots are used on both the rising and falling edge of the $\overline{BL}$ signal. on a rising edge, a high to low to high pulse is createds to charge a capactitor at the control node. A reinforcement circuit shown in figure 5-4 is used to maintain the node voltage and bring the capacitor voltage to the internal supply voltage (VCCD). The Top Gate low signal will be low. On the falling edge, a pulse is used to discharge the capacitor at the control node bringing it to ground. The reinforcement circuit will keep the node at ground. The Top gate low Signal will be high.

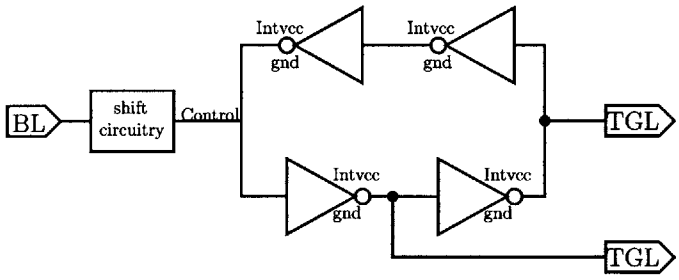


Figure 5-4: Signal transition high to low with reinforcement

5.3.2 TON LTH

The $\overline{TON\_HS}$ signal used to control the top gate driver and is generated from the TON signal. The signal is created using a method similar to the method used to generate the Top gate low signal. One shot falls and rises are used to generate pulses to change the state of an output node which is later reinforced with inverters. In this case a rising input signal results in a low $\overline{TON\_HS}$ signal while a falling input signal will result in a a high $\overline{TON\_HS}$. The design can be seen in figure 5-5. Since the output is going to a lower voltage. The charging caps and circuitry are based off of PMOS transistors as opposed to NMOS transistors used in the Boostlow block when generating the TGL signal.

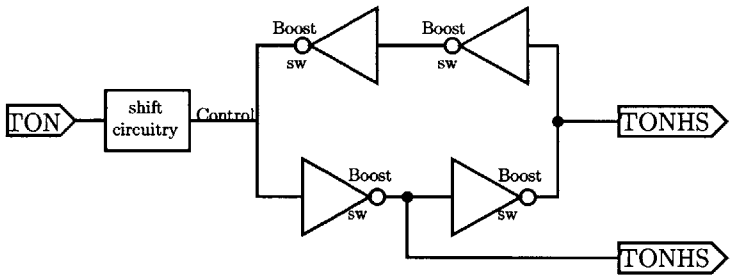


Figure 5-5: Signal transition low to high with reinforcement

5.4 Sleep

The Ton LTH block and the BL HTL block essentially serve as the control center for the operation of the top gate controller as these signals determine what state the driver is in. It is for this reason that the sleep functionality is integrated into these blocks. During sleep, it is desired that the top gate be low. This is integrated in the BLHTL block by pulling the control node to ground creating a high TGL signal. In addition, in the TonLTH block, the control block is pulled up to boost creating a low TONHS signal.

5.5 Top gate driver

When the top gate driver is in charge of turning on and off the top-side device. A common occurrence in buck converter switching is excessive ringing on the switch node when the top-side device is turned on. This non desirable ringing is primarily due to parasitics associated with the switching transistors.When the bottom-side device is on, energy is stored in the corresponding drain and source parasitic inductances. When the top gate is turned on quickly, it creates an RLC resonant circuit between the parasitics of the top-side and bottom-side devices. This creates the voltage overshoot and node ringing [18]. In addition to adding noise to the system, the ringing can result in breakdown of the top-side transistor if the gate-source voltage exceeds the maximum transistor voltage rating and the bottom-side transistor if the drain-source voltage is exceeded.

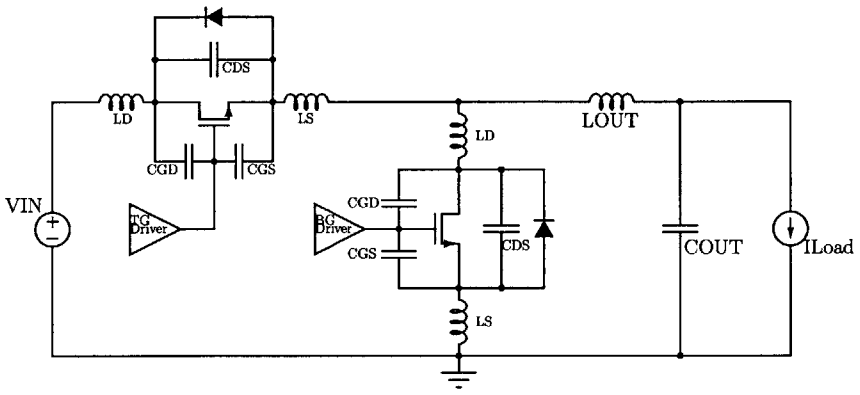


Figure 5-6: Buck converter with transistor parasitics

It is important to design a driver that will reduce the parasitic effects and reduce switch node ringing. A few techniques have been used in the past including; increased precision in layout to reduce parasitic inductance, adding gate resistance to slow down device turn on or adding a RC snubber circuit to attenuate switch node ringing [3]. The proposed solution involves the used of controlled current mirrors.

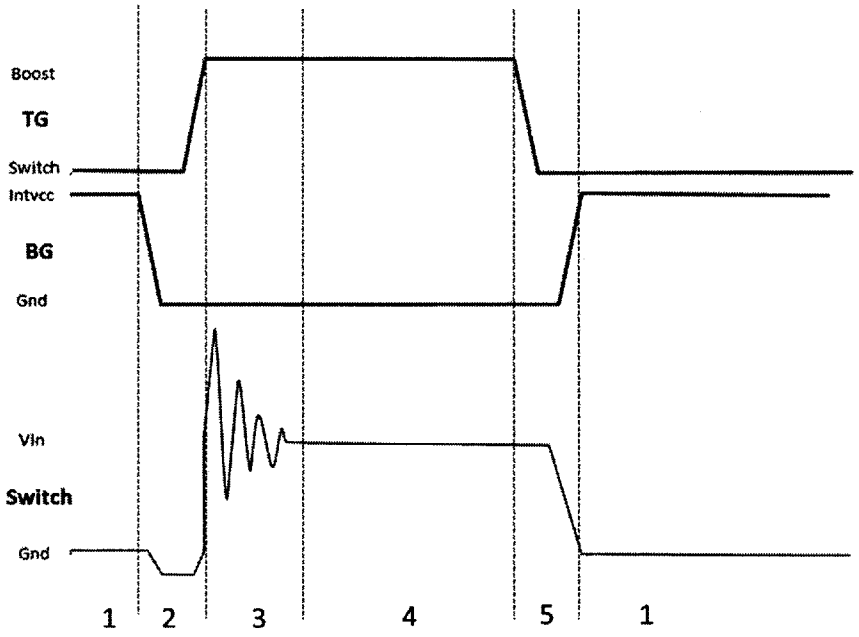


Figure 5-7: Buck converter tranistion stages and switch node ringing [3]

5.6 Gate drive

The gate drive signal (GDRIVE) is essential in determining, whether the top or bottom gate is on. Some logic is used to determine the state of the gate drive signal. For the bottom gate to turn on, the gate drive signal needs to be low, and for the top gate to be turned on, the signal needs to be high. The logic used has not changed significantly from the original design and therefore will not be explained in detail. The Gate drive signal was determinant on various other signals including, the sleep signal, clock signal and various trip signals. An addition made to the schematic was the Top Gate Low Delay signal (TGLOWDLY). The reason for this signal will be explained in a later section. This signal is now paired with the I_{TRP} signal in a NOR gate. This addition now requires that both the Top Gate Low Delay signal and the I trip signal have to be low in order for the Gate Drive signal be high and turn on the top gate. Likewise a high signal form either of the two signals will result in the Gate drive signal becoming low.

5.7 TGLOW

The TGLOW signal is added to ensure that the Top gate has time to discharge. This node only becomes necessary in certain cases where the I_{TRP} signal may not be tripped due to the operating state.

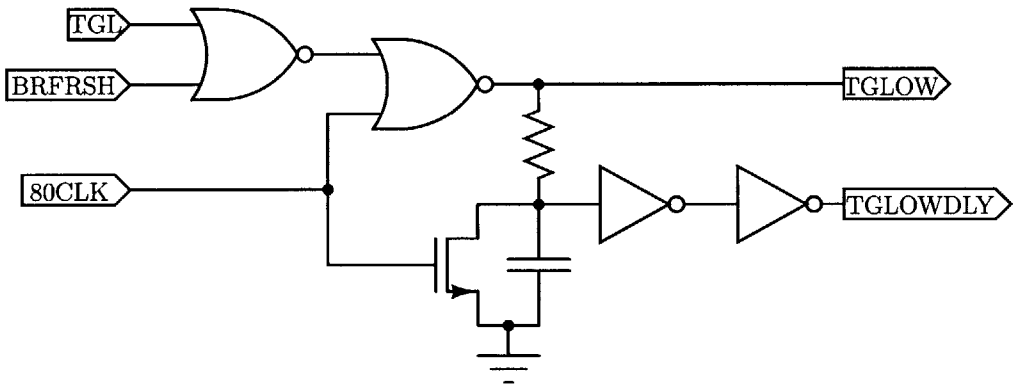


Figure 5-8: TGLow Block

5.7.1 Dropout Refresh

As explained earlier in this chapter, the boost capacitor is charged when the top-side FET is off and bottom-side FET is on. However, a few issues can occur under specific operating conditions. The gates are controlled using a peak current mode method in which the bottom side turns on when the current peak limit is reached. However, in cases where the load is high, and the bottom side does not have time to turn on before the next clock cycle, the boost cap can go for a period of time uncharged. As the duty cycle approaches 100%, the part is designed to enter a dropout state where the top-side device is turned on continuously. Under this operation, the boost capacitor will never be charged and component leakage may lead to charge reduction on the capacitor. The purpose of the dropout refresh is to every so often force the

bottom side on and give the boost cap the opportunity to be charged. Without this addition, the boost cap can decrease to a point in which it is incapable of turning on the top-side device. Using a series of D flip flops, there is a forced refresh ever 512 cycles. The dropout refresh is incorporated into the TGLow block shown in figure 5-8 This signal, BRFRSH, when high, creates a low signal at one of the inputs of the nor gate that determines the TGLOW signal. When the 80CLK signal becomes low the TGLOW signal will be high.

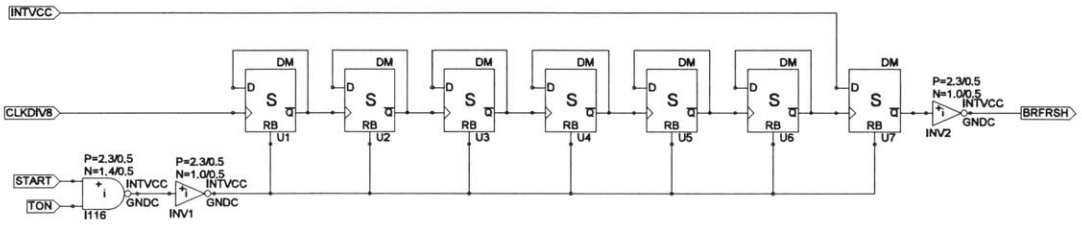


Figure 5-9: Dropout Refresh

5.8 TBlank

The TBlank signal serves the same purposes as original chip, to provide low side blanking for the ipeak comparator. The Tblank signal is generated using a one-shot rise with the TON signal as the input. The Top gate low signal is integrated into the one shot makinlg the Blank signal high whenever TGL is high

Chapter 6

Chip Modifications

To ensure that the device operates at low voltages, we must make sure that all circuits can operate with the changes made. Most of the circuit blocks are powered by the internal supply voltage. These circuit blocks won't experience much changes since the charge pump brings the internal supply voltage up to a respectable voltage when the V_{IN} voltage is low. It is important, however, to review circuit blocks that work directly with the V_{IN} voltage. This chapter will review blocks affected by the changes made and if necessary explain the changes made to the circuit block. A review of the circuit block diagram with the circuit blocks to be discussed circleed can be seen in figure 6-1.

6.1 bandgap block

Changes made to the bandgap block to accommodate the lower input voltage were explained in chapter 2. However some of the the block's output nodes are effected by this change. There are blocks with in the the chip schematic that make use of the bandgap supply (BGSPLY) voltage and the bandgap ready signal (BGRDY & $\overline{BGRDY}$). Lower input voltages means that these signals and the blocks that make use of these nodes must be able to operate with the lower node voltages. Due to transistor voltage drop these signals have a voltage slightly less than the input voltage.

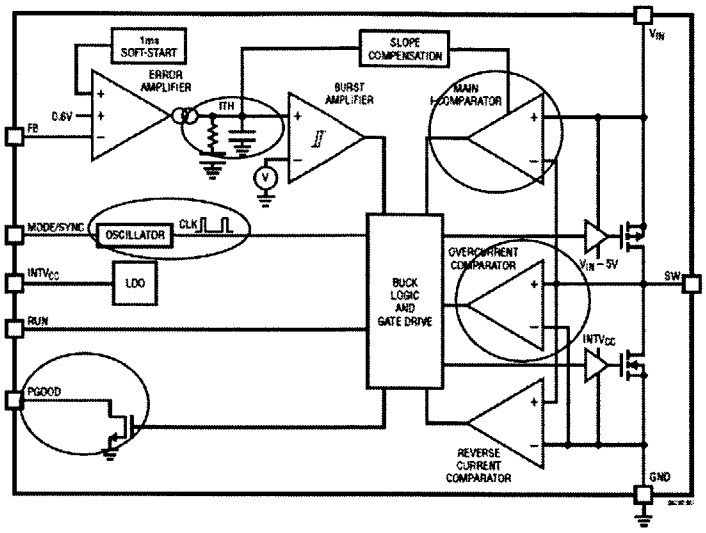


Figure 6-1: Circuit block diagraram with blocks to be slightly modified circled[1]

6.2 LDO block

Changes made to the LDO block to accommodate the lower input voltage were explained in chapters 3 & 4. These changes have to do with creating the internal supply voltage, the LDO's main function. The LDO block uses the BGRDY & $\overline{BGRDY}$ signals. BGRDY signal is used to control the resistor branches used to set voltages for the comparator. The $\overline{BGRDY}$ signal is used to shut off the current mirror powered by the LDO current. In both cases however, the lower BGRDY & $\overline{BGRDY}$ do not effect their functions. The voltages will still be well above the NMOS threshold voltage. Therefore no additional changes are needed.

6.3 Thermal Shutdown

The thermal shutdown block uses the bandgap supply voltage as the source for its inverters. The lower bandgap supply voltage will not effect the operation of this block because the TH1 and TH2 nodes generated in the bandgap block are also dependent and are limited by the bandgap supply voltage. Furthermore the thermal shutdown block already has a level shifter to bring the thermal shutdown signal to the internal supply voltage when it is high.

6.4 PGOOD

The PGOOD block has an inverter stage powered by the bandgap supply rail and connected to ground. The input into this inverter is the LDOready signal. The function of this inverter is to pull PGOOD low when the LDOrdy signal is low. Because of the charge pump, the LDO ready signal when the input is low will be the voltage of the output of the charge pump which will be higher than the input limited bandgap supply voltage. There isn't much harm in having a gate voltage higher than the sources voltage. The changes in inverter states will be slightly different due to the lower source voltage, however this is a non-issue. As stated in the bandgap block section, the lower bandgap supply voltage does not prevent the turning on of the NMOS device. Therefore, no additional changes are needed.

6.5 I_{PEAK} Comparator

The function of the I_{PEAK} Comparator is to create the I_{TRP} signal. The I_{TRP} signal is used to determine when the top-side switch should turn off and the bottom side switch should turn on. A high I_{TRP} signal is created by turning on a PMOS device and creating a voltage drop over a set of resistors. A high enough voltage drop will surpass the threshold voltage of an inverter powered by the internal supply voltage. The source voltage for the peak comparator circuitry is the input voltage. At low input voltages, the voltage drop over the resistors may not be high enough to trip the inverter and trigger a high I_{TRP} signal. This is in part due to the charge pump making the internal supply voltage higher than the input and the higher internal supply voltage being the sources of the inverter stage. The solution to this problem would be to power the inverter with a lower voltage when the input is low. The LDO supply voltage (LDOVCC) is the perfect candidate for this predicament. Unlike the internal supply voltage, the LDO supply voltage is always less than the input voltage. At high V_{INS} the LDO supply voltage creates the internal supply voltage. At low V_{IN}, the non charge pumped voltage will allow the voltage drop across the resistor

to reach the threshold voltage. However, we still want the trip signal to be controlled by the internal supply voltage. To do this we will implement a level shifter that is exactly the same as the one described in section 4.2. With these modifications the I peak Comparator can operate at the lower voltages.

6.6 Ith Control

We can replicate the behavior of the topgate device through the use of ohms law. In the actual topgate device a large amount of current flows through a device of relatively low resistance. To easily replicate this voltage drop, one can scale down the current while scaling up the resistance. Because of ohms law, the resultant voltage behavior will be relatively similar. In the original design a scaled PMOS device was use to represent the topgate MOSFET device which was also a PMOS device. With the change of the top-side device from an PMOS to a NMOS device. To maintain accuracy the PMOS tree needs to be replaced with an NMOS tree.

It is important to note the varying orientation of the NMOS devices in the NMOS tree. The devices are placed in pairs to save space in layout. With this orientation every pair of devices can share the same wells as opposed to making individual wells for each device. Specifically, for the the last NMOS device in the tree, the orientation is flipped such that the drain is connected to the SwLim node. This is to prevent device breakdown. The NFET tree is placed in parallel with a diode connected PMOS device that makes the swLim node at most a diode drop above V_{IN}. As the device has a wide input range, under situations where V_{IN} is high, the swLim voltage can go as high as V_{IN} - diode drop. The boost voltage, which controls the gate of the last transistor can go as as low as the internal supply voltage (3.6). At the highest operational V_{IN}, the source to gate voltage would be greater than 9 volts which would break down the standard transistor max gate-source voltage. This predicament is solved by changing the orientation of the transistor as the max gate-drain voltage is higher and will prevent device breakdown.

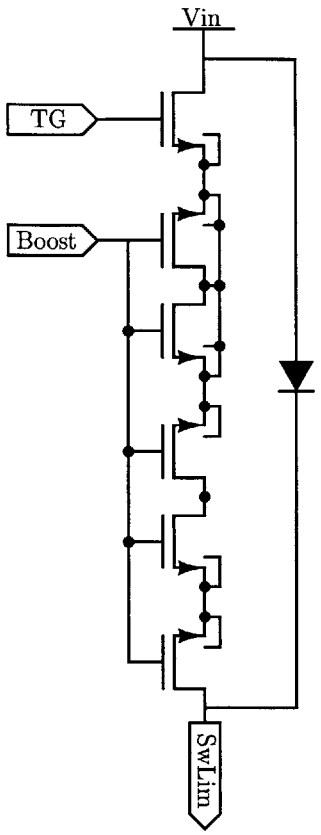


Figure 6-2: NFET tree

6.7 Oscillator

As stated in the previous chapter, the 80 clock signal is added to designate a time in which the Top Gate low signal can be set high. To generate this 80 clock signal, additions must be made to the oscillator block. As a basic overview, the oscillator works by comparing a reference voltage to a saw tooth wave and creating a high signal when the saw tooth is above the reference and a low signal when its below.The reference voltage used to create an 80% duty clock signal is .45 volts and is created through a voltage divider on the bandgap reference node.

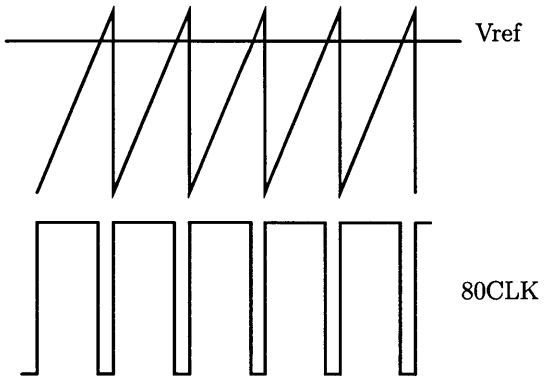


Figure 6-3: 80% duty cycle created by comparing reference voltage to sawtooth wave

Chapter 7

Simulation Results

7.1 Bandgap

The bandgap block was modified so that a bandgap voltage could be created at the lowest specified input (2 volts). The bandgap test will look at the bandgap voltage under different operating conditions. Figure 7-1 contains device performance under Super Slow(SS) transistor mode and typcal mode while varying temerperature(-45°C, 25°C, 125°C).

7.2 Charge pump

The charge pump was built expecting to have at most 20ma of load current. The tests wil look at the the charge pump's ability to charge the reservior cap under different operating conditions.The size of the flying and reservoir cap are 1μF and 2.2μF respectively. The charge pump test will look at the output voltage and duration to steadystate voltage while varying multiple factors including temperature, load current and transistor mode. Figure 7-2 contains device performance under Super Slow(SS) transistor mode, varying temperature(-45°C, 25°C, 125°C) and load(0mA, 15mA, 20mA). The same test is done under the typical transistor mode and is seen in figure 7-3.

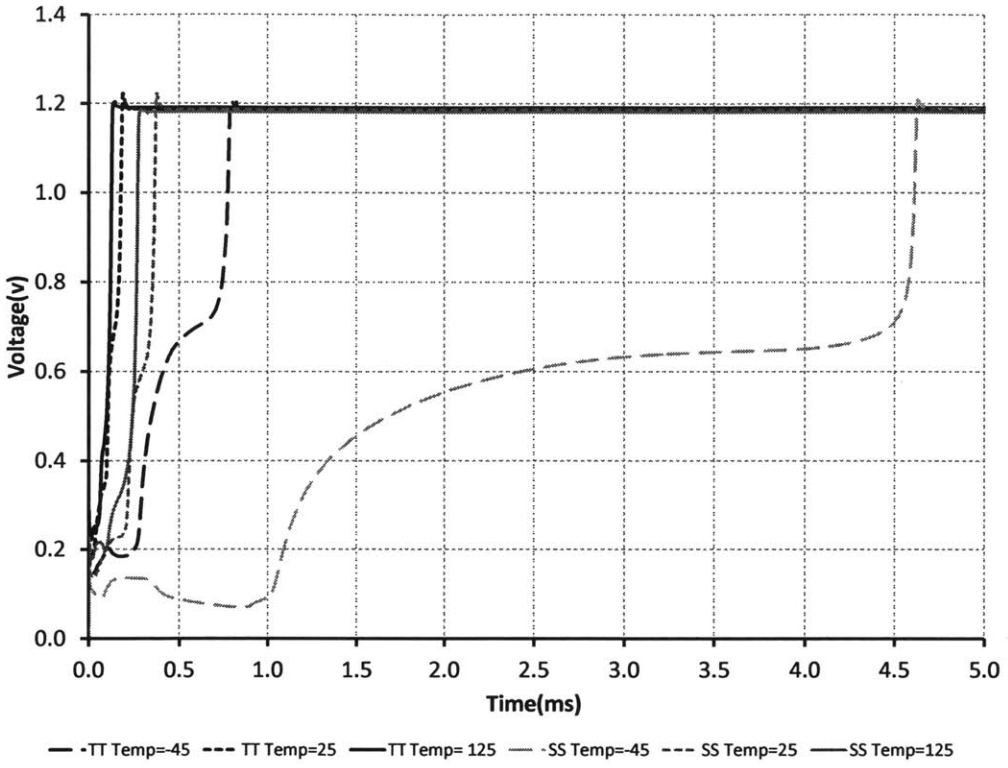


Figure 7-1: Bandgap reference voltage with 2 volt input - Simulation

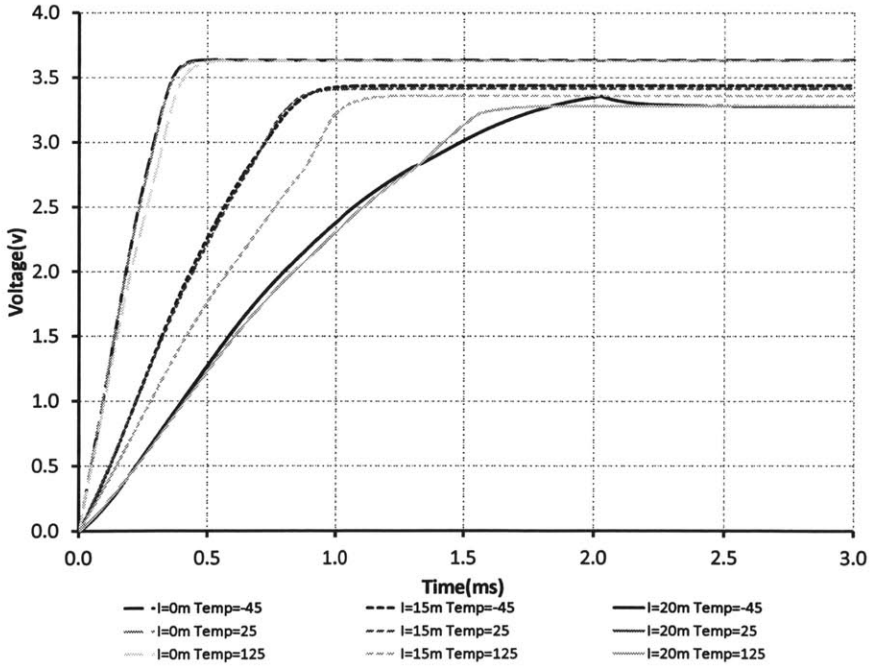


Figure 7-2: Voltage vs.time charge pump SS mode. 2 volt input - Simulation

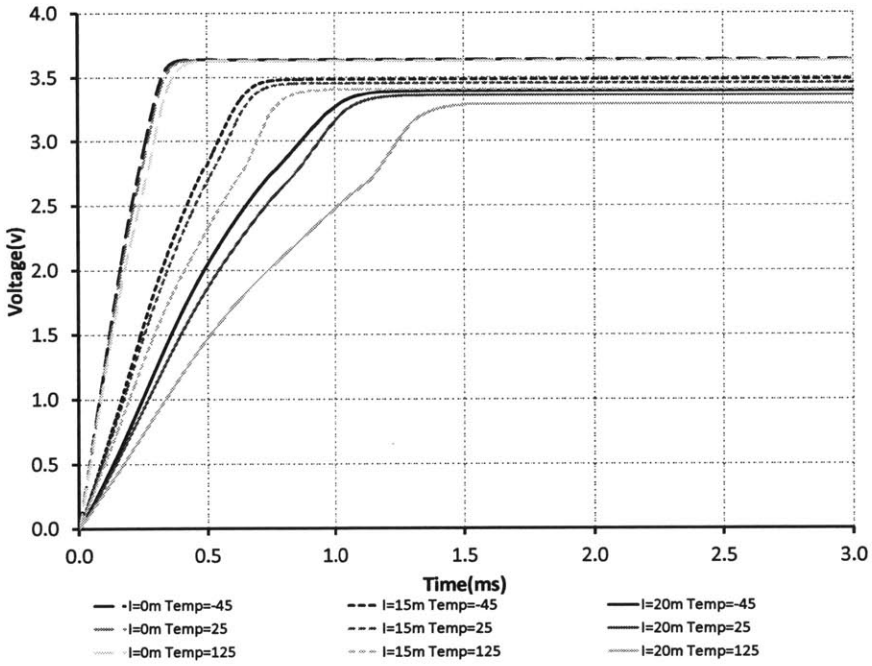


Figure 7-3: Voltage vs.time charge pump TT mode. 2 volt input - Simulation

7.3 LDO

The LDO block was built to create the internal supply voltage, using the charge pump to bump up the input voltage if necessary. The tests will look at the comparator signals, $LSCHARGON$, $LDORDY$ and $3.2TRIP$ and the internal supply voltage under different operating conditions. The first test shown in Figure 7-4 tests the LDO block with a constant 2 volt input. The sleep function is artificially added to the test since a separate block is used in the chip. To closely resemble the actual sleep block, the sleep signal is pulled low when the LDO ready signal is high. To see device behavior in sleep, the sleep signal is forced high at .7ms. Since the 3.2Trip signal is high, neither the die nor the RC oscillator is running. If the internal supply drops below 3.2 volts while in sleep, The RC oscillator would turn on to recharge the internal supply cap. When in sleep above 3.2 volts, the quiescent current of the LDO is roughly 400nA. Figure 7-5 shows quiescent current of the new LDO versus the original.

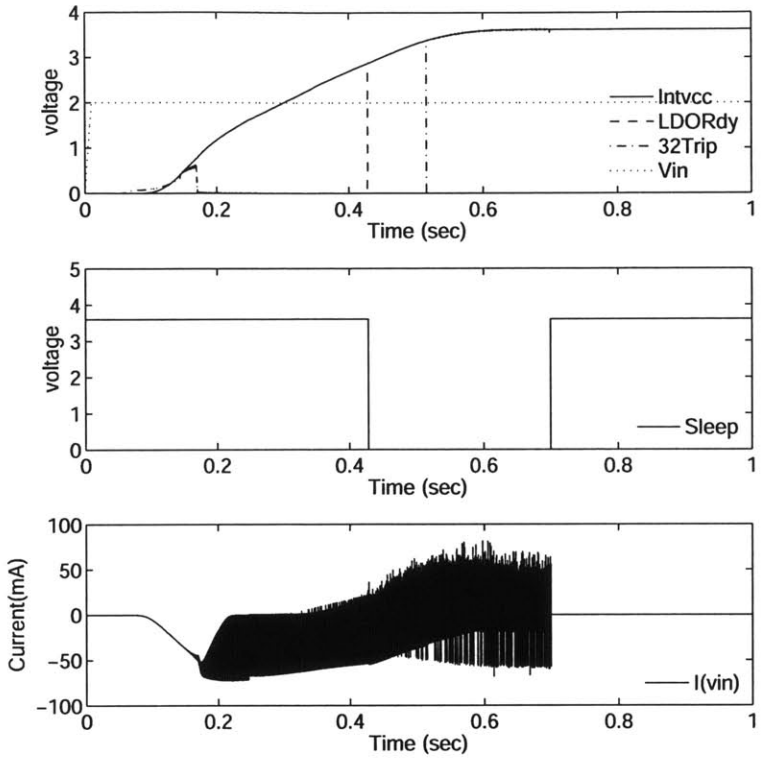


Figure 7-4: voltage vs.time charge pump tt mode. 17 volt input - Simulation

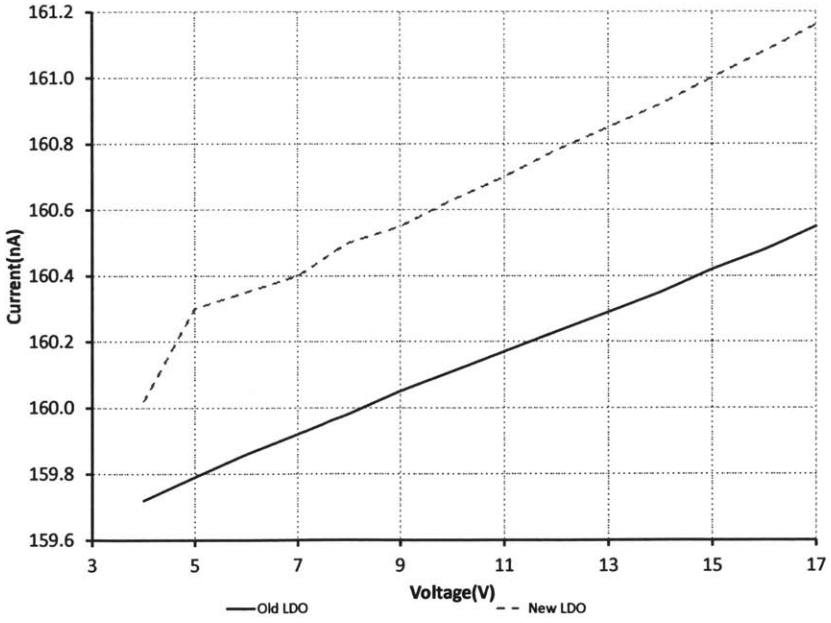


Figure 7-5: Current vs. input voltage, variation in current draw during sleep - Simulation

7.4 Top Gate Driver

A Boost test block was created to test the implementation of the NMOS top-side device. The test block includes only the core circuit blocks from the chip that are needed to show top gate functionality. The test block can be seen in the appendix. The test will look at the top gate voltage and bottom gate voltages. It will also look at the behavior of the switch node during switching under different operating environments. Figure 7-7 shows the top gate and bottom gate when the input is 17 volts. as expected, the top gate voltage, due to the boost cap and the internal supply, is roughly 20.6 volts (3.6v above V_{IN}). The 3.6 volt internal supply is used to turn on the bottom gate. In Figure 7-8 the switch node is monitored under various operating modes(temperature and transistor mode). There is very little overshoot or ripple during the transition. The drop in the witch node prior to the transition is due to the dead-time where both the top gate and bottom gate are off causing the switch node to drop roughly a diode drop below ground.

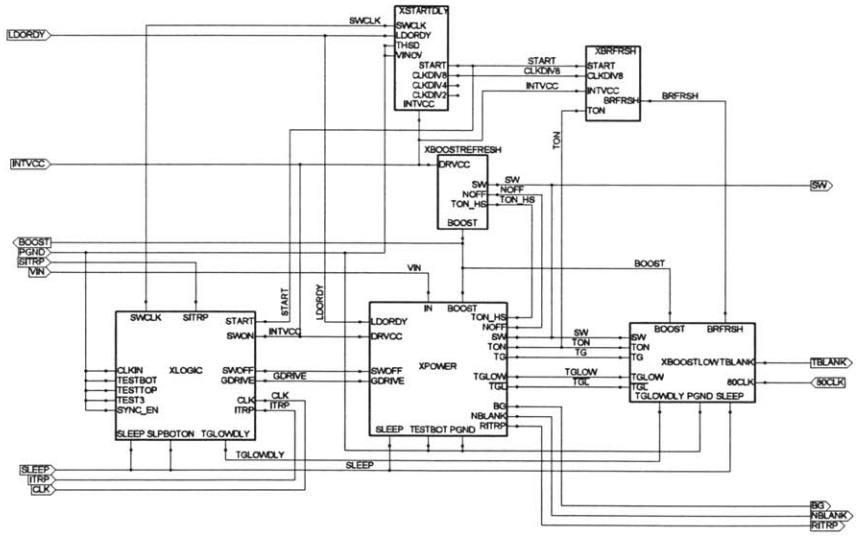


Figure 7-6: NMOS top-side Test Circuit

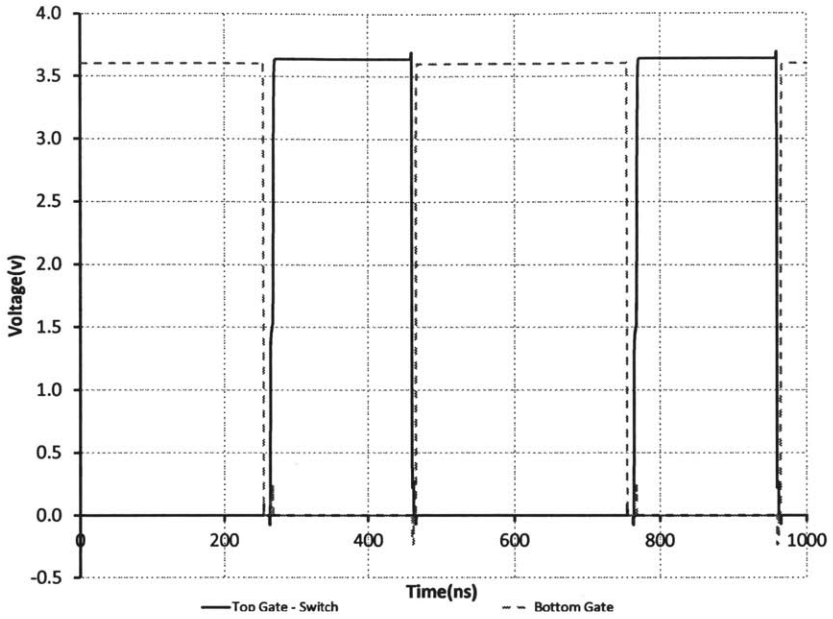


Figure 7-7: Gate-source voltage top-side and bottom-side transistors. 17 volt input - Simulation

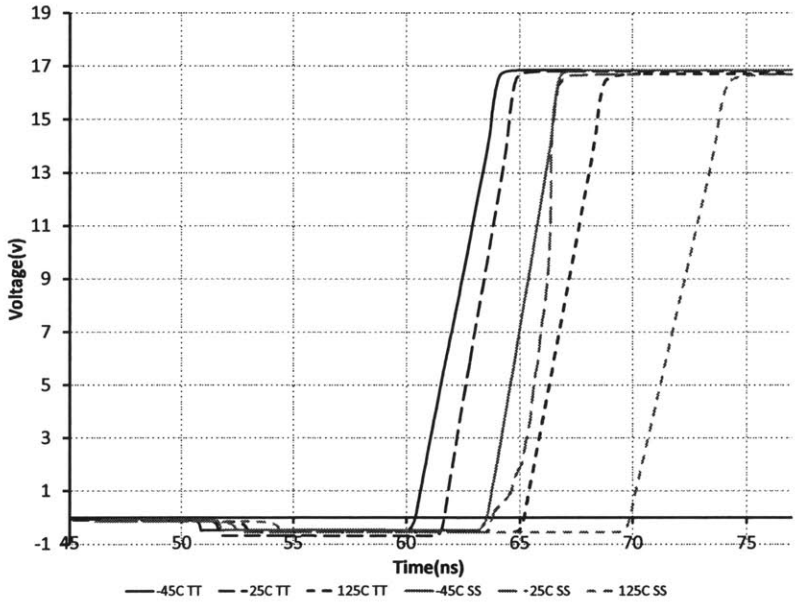


Figure 7-8: Voltage vs.time rising switch node. 17 volt input - Simulation

7.5 chip

The chip level simulation will encourporate all of the blocks created or modified as well as the unmodified blocks. This is a good way to see how the new components work

with the original components. The test simulation is the proposed chip configured to operate in forced continuous mode at 2.25MHz operating frequency. Figure 7-9 is the propsoed chip with the external components needed for operation. This configuration, with its feedback components will create a 1.2v voltage output. The input voltage will be 2 volts for the test and the test will be run in typical transistor mode at 25°C.

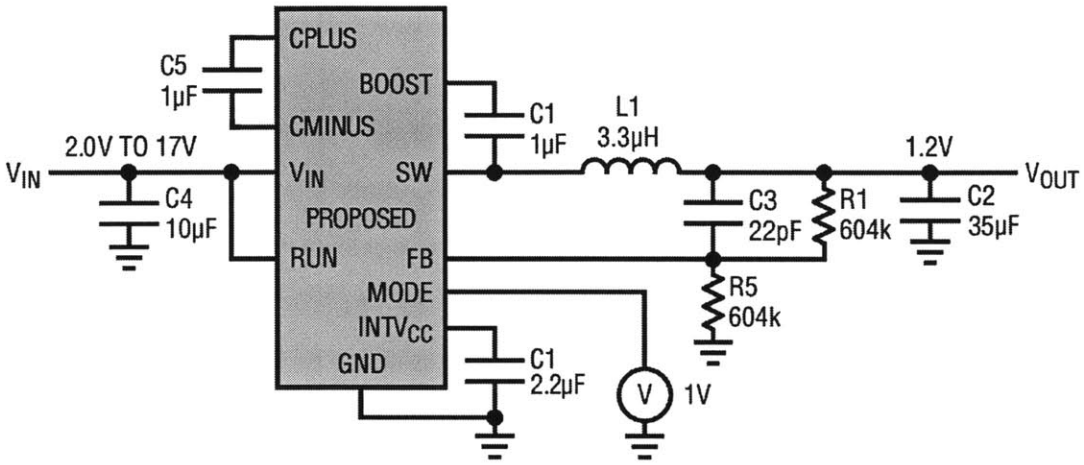


Figure 7-9: Test chip setup

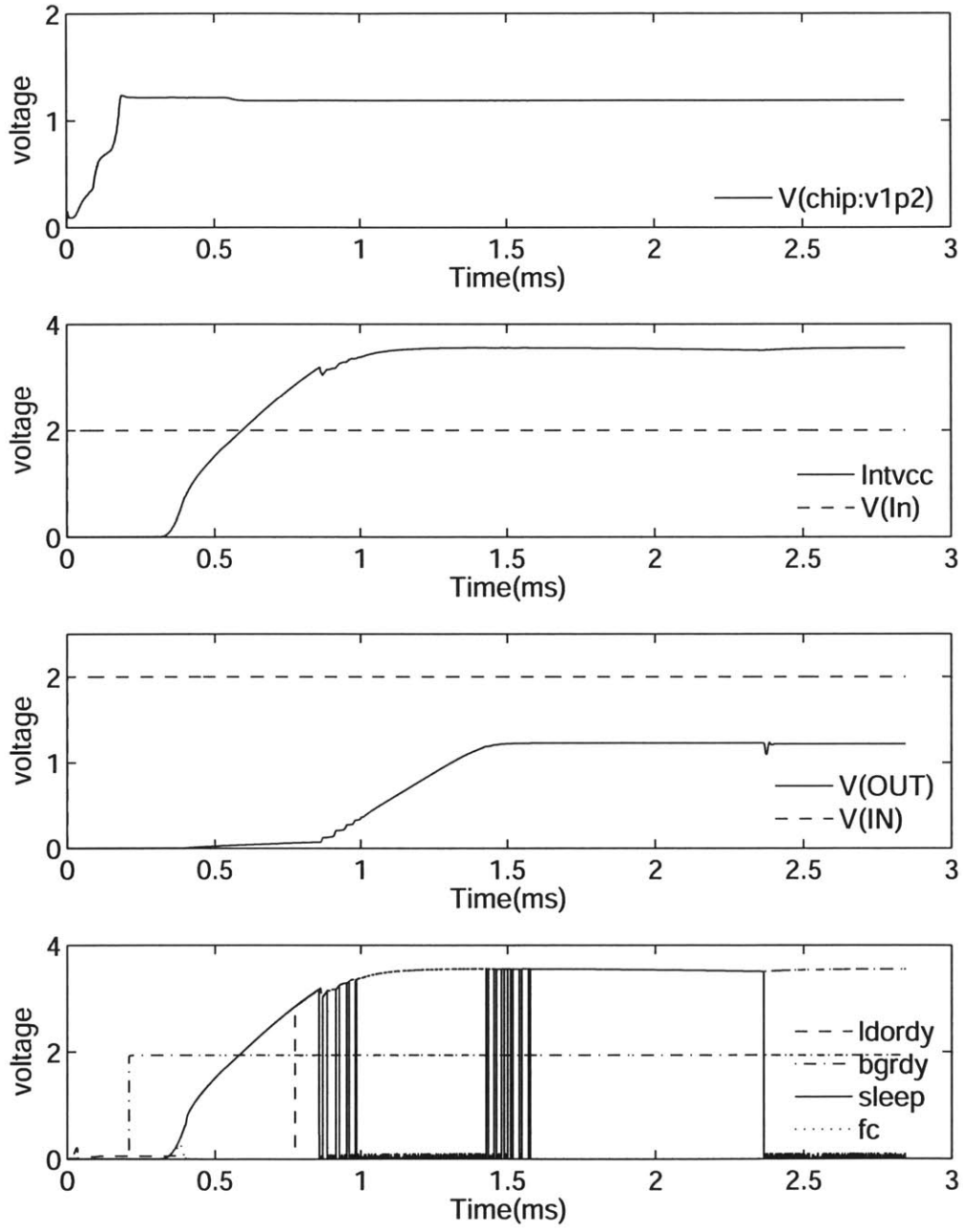


Figure 7-10: Voltage vs.time rising chip nodes, 2v input - Simulation

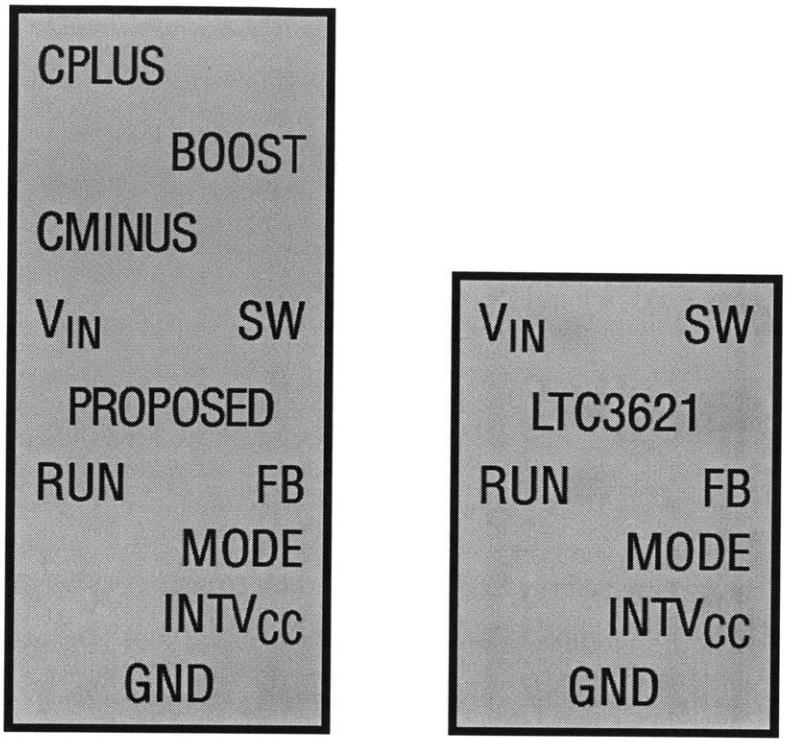
Chapter 8

Conclusion

The proposed chip is based off the LTC3621 and is able to achieve the goal of operation at 2 volts through the modification of the bandgap block and the integration of a charge pump into the LDO block. Overall efficiency is increased due to the changing of the topside MOSFET from a PMOS device to a NMOS device. This modification led to a redesign of the Top gate driver that could provide a gate voltage above V_{IN}, through the use of a boost cap, and also reduce switch node ripple during switching. The proposed chip will require 3 additional pins to to the original. The boost pin allows the use of an external capacitor that serves as the boost capacitor for the newly designed top gate driver. The CPLUS and CMINUS pins are used for the fly capacitor used in the charge pump. Figure 8-1 shows a pin-out comparison between the new and porpoised chip

8.1 Future Work & Wrap up

Following further testing, the next step would be going from schematic design to layout. It is expected that the proposed chip will have a larger die area than the original. This is due to the increased number of output pins as well as increased amount of circuitry particularly the charge pump which required large transistors to supply a max 20mA internal supply load. Following layout and further testing, this proposed part could potentially be among Linear's line of Step-down converters to be



(a) Proposed chip

(b) LTC3621 chip

Figure 8-1: Chip pinout comparison

used in a vast number of applications.

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