An Analysis of Techniques Implementing Virtual Load Line Voltage Sense and Regulation for Automotive USB Buck Application

by

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Abstract

This thesis analyzes three diseparate methods of virtual voltage sense in order to achieve voltage regulation at the end of load line cables without the need for two sense cables. This thesis also explores the implementation of the discussed Current Interrupt Method in order to regulate the output voltage of an automotive USB buck converter as well as the difficulties associated with the implementation. A board-level proof of concept of the implementation is achieved, and then improved through an integrated design tested within a simulation.

Thesis Supervisor: John Tilly
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Chapter 1

Introduction

Technological advancements take place every day in this world, and a category of these developments call for the ability to deliver power over long cables, referred to here as the load lines. Examples of this include remote security systems, halogen lights, notebook adapters and CAT5 cable systems. The difficulty that arises inherently from this setup, either as a result of a non-negligible line resistance, or as a result of high current levels, is that there will be a voltage drop over the load lines connecting the power supply to its target circuit. Many circuits require a regulated input voltage and so this non-negligible voltage drop can cause problems with the operation of the network receiving the power. The task of developing robust methods of regulating power delivery over long load lines needs to be completed for the progression of technology.

This thesis examines three methods of voltage regulation over a pair of load cables without the use of voltage sense wires in order to achieve an economic implementation. The practicality of implementing each technique and range of application are explored. This thesis also examines the application of one of the techniques found most suitable for the regulation of an automotive USB buck power supply.

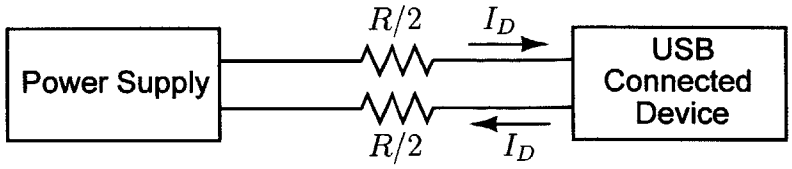

Figure 1-1: Automotive USB circuit diagram.

1.1 Automotive USB Buck Regulation

Car manufacturers are looking to include USB ports in their car consoles so that consumers can charge their mobile devices while in transit. The car's 12V battery connected to a 12V to 5V buck converter is the power source for charging operations. Practical application constraints require the power supply to be connected to the USB port over several meters of cable as depicted in figure 1-1. The reason for this is that car manufacturers will potentially look to place the USB ports far away from the power supply in areas such as the center console or the backseat headrest for passenger's use. The task of supplying power to a USB port in a car in order to charge a portable device is a problem that requires long distance voltage regulation and compensation for the voltage drop across the cables connecting the source to the load. The configuration depicted in figure 1-1 leads to a large voltage drop over the connecting load lines when a device draws a sufficient amount of current. The voltage at the USB port, however, must be regulated strictly around 5V or else the connected device may not charge properly or may become damaged. Regulation at the power supply is therefore necessary so that after the voltage drop over the load lines, the voltage at the USB port is set appropriately at 5V [6].

1.1.1 Virtual Voltage Sense Regulation

Remote voltage sensing that allows compensation for the voltage drop over the connecting lines can be achieved by using two long sense cables of the same length as the load line cables as depicted in figure 1-2. This traditional approach allows the regulation circuitry to measure the voltage at the USB port directly and then use that measurement in a feedback loop in order to regulate the voltage at the USB

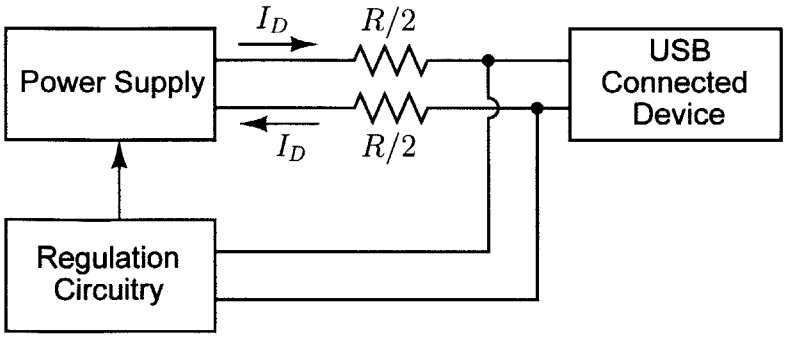

Figure 1-2: Traditional approach to automotive USB voltage regulation with remote voltage sensing.

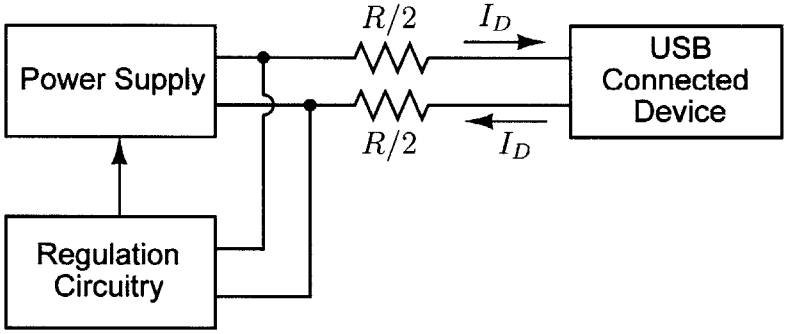

Figure 1-3: Desired method of automotive USB voltage regulation with virtual sensing.

port. The drawback to this method is that it requires doubling the number of cables needed to supply power to the USB port. These extra cables take up more space and they require larger harnesses in the car for mechanical support. These harnesses then take up further space and add weight to the car, ultimately reducing the efficiency of the car and increasing the CO_2 emission of the car. This solution is not an economic solution for car manufacturers.

Car manufacturers are instead looking at virtual remote voltage sensing solutions that indirectly infer the voltage drop over the load lines and the connected device without the use of sense cables. The block diagram for this type of solution is shown in figure 1-3. The inferred voltage could then be used in a feedback loop to regulate the voltage at the USB port appropriately. Since this solution only requires measurements at the output of the power supply, it eliminates the costs that come with implementing

extra wiring to accomplish the voltage regulation.

1.1.2 Decision for an Active Feedback Solution

There are two possible feedback strategies that can be used in order to implement this cable drop compensation scheme: a passive solution or an active solution. The passive solution is programed to know the numerical value of the resistance of the load lines. The system observes the current drawn from the power supply by the connected device and increases the voltage supplied to the load lines according to Ohm's law. This strategy has been implemented previously in other projects [4].

This passive regulation solution has several drawbacks. One issue is that the distance between the USB port and the power supply can vary between cars and car manufacturers do not wish to complete a Kelvin resistance measurement of each load line for each constructed car. Another problem with the passive solution is that the temperature of this network will be subject to high variation when inside the car. Cable resistance and other device parameters change over temperature and so the resistance of the load lines will vary by a non-negligible amount from what the regulation circuitry is programed to expect. This will cause larger errors in the voltage regulation at the USB port than are acceptable. These issues can be avoided and a more accurate voltage regulation can be achieved with an active solution that continuously measures the voltage drop over the load lines.

1.2 Automotive USB Buck Regulator Application Space

The virtual sense techniques behave by superimposing some signal on the power waveforms supplied to the connected device over the load lines. The transformation of the superimposed signals by the system is then observed with the intent of extracting information regarding the voltage at the end of the load lines. The different constraints on the implementation of the automotive USB buck converter must be considered in

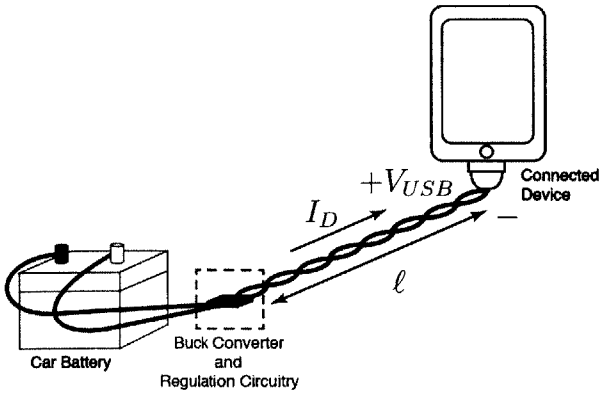

Figure 1-4: Diagram of automotive USB power circuitry.

order to understand how current or voltage signals may be appropriately used within the power supply system.

The maximum current that can be drawn by a device that supports USB charging is 2.4A. The USB connection standard requires that the connected device have an input capacitor between 1μF and 10μF [2]. Note that this capacitor will appear as a load capacitor to the regulation circuitry and will be utilized by each of the virtual voltage sense techniques. The distance between the power supply and the USB port, and so the length of the cable one way, can vary between 1m and 5m. The average gauge of the load cables will be 20AWG. The possible lengths of cable and the average wire gauge can be used to calculate that the net resistance of the connecting cables will be between 66mΩ and 333mΩ [7].

The upper bound on the switching frequency for an automotive power supply is chosen in this thesis to be 2MHz based on typical commercial practice at the time of writing. Power converter size can be reduced by operation at high frequencies, and even frequencies above 2MHz are possible today. At the same time, some customers prefer to operate at relatively low frequencies of a few hundred kHz or below to simplify design and minimize switching loss. It is therefore difficult to put a hard bound on the switching frequency. The maximum bandwidth of the power supply is, then, selected as 400kHz for this thesis (approximately 1/5th of the estimated switching frequency of 2MHz) and will be the upper bound for the frequency of operation.

Application Space for Automotive USB Buck Applications	
Current Drawn from USB (I_D)	$\leq$ 2.4A
Load Capacitance (C_L)	1μF - 10μF
Frequency of Operation (f)	$\leq$ 400kHz
Length of Cable One Way (ℓ)	1m - 5m
Resistance of Cable (R)	66mΩ - 333mΩ

Table 1.1: Virtual voltage sense buck regulator application space constraints

Chapter 2

Proposed Strategies for Virtual Load Line Voltage Sense

Linear Technology Corporation has developed several different methods of virtual sense load line sensing that they have implemented in their past products [3], [4]. These methods infer the approximate voltage at one end of a load line pair by observing the voltage signal characteristics at the output of the power supply. The chosen technique will ultimately be implemented in a feedback loop for the automotive USB system in order for the power supply to compensate for the voltage drop over the load lines and regulate the voltage at the USB port correctly. An analysis of three promising virtual sense techniques has been carried out and used to select a technique most appropriate for USB buck converter regulation in an automobile.

2.1 Method A: Inference of Load Line Resistance through Incremental Changes in Voltage and Current

The first technique of virtual voltage sense considered, method A, repeatedly increments the current supplied over the load line cables by a small amount and examines the incremental change in voltage over the input terminals of the load line cables.

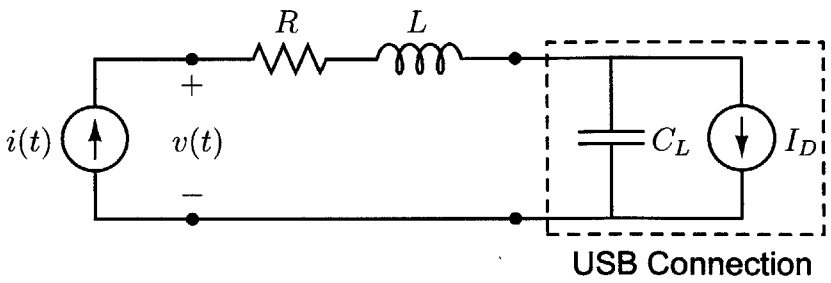

Figure 2-1: Circuit implementation of method A.

Ohm's law is then applied in order to approximate the resistance of the load line cables as $\Delta v/\Delta i$, and this measured resistance can then be used along with the known value of the current being drawn over the load lines to infer the voltage drop over the load lines. The implementation of method A is depicted in figure 2-1 where the current source, $i(t)$, models the power supply, the resistance, R, and inductance, L, together model the load line cables, and the load capacitance, C_L, and current source, I_D, in parallel represent the connected device that is drawing current.

2.1.1 Analytical Solution of Method A Strategy

An analytical solution of the voltage sensed by method A is presented for insight into the technique's ability. The USB-connected device is drawing a current, I_D, over the load line cables when the regulation technique is not being invoked. When the regulation technique is invoked, the power supply injects a square wave of peak-to-peak amplitude Δi, and frequency, f, onto the current waveform by modulating the switching converters current reference. This waveform is depicted in figure 2-2. The voltage drop over the load line terminals is the superposition of the voltage drop over the resistor, R, the inductor, L, and the load capacitor, C_L, and is also depicted in figure 2-2. The voltage drop over the resistor is therefore, $v_R(t) = i(t)R$, the waveform of the voltage drop over the resistor is a square wave with magnitude $R(I_D \pm \Delta i/2)$. The voltage drop over the inductor is $v_L(t) = Ldi/dt$. This technique takes its measurements immediately before the transition in the current waveform, taking advantage of the fact that the voltage drop over the inductor is zero since

the magnitude of the current is not changing. At the current waveform's transition, the voltage over the inductor spikes. The voltage drop over capacitor over time is $v_{C_L} = 1/C_L \int i_{C_L}(t)dt + V_{C_L0}$, where V_{C_L0} is the initial bias voltage on the capacitor. The waveform of the voltage drop over the load capacitor will then be a triangle wave of peak-to-peak voltage $\Delta i/(4C_L f)$.

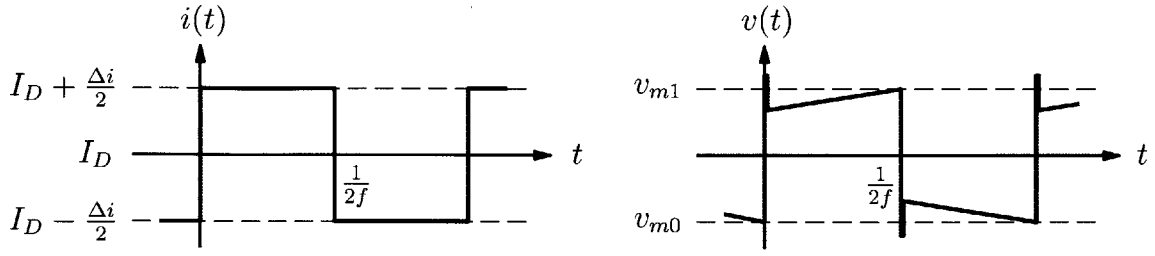

Figure 2-2: Input current waveform and resulting voltage seen over the load lines.

The implementation of method A is easiest to see if the voltage waveform is sampled at it's peak values corresponding to $t = 1/(2f)$, immediately before the voltage spike is induced by the inductance of the load lines and the changing current. Taking the high value of the current square wave to be the first half period of the cycle, the voltage, v_{m1}, sampled at $t = 1/(2f)$ is equal to the superposition of voltage drops generated by the resistance of the load line cables and the load capacitance in the connected device.

$$v_{m1} = R\left(I_D + \frac{\Delta i}{2}\right) + \frac{\Delta i}{2C_L}\frac{1}{2f} + V_{C_L0}$$

The voltage over the load line cables is then sampled at $t = 1/f$, the end of the half-cycle corresponding to the low value of the current square wave. This measurement, v_{m0}, will consist of the voltage drop generated by the resistance of the load line cables, and the initial bias voltage on the load capacitor, since the voltage over the load capacitor was discharged by amount it was symmetrically charged to during the first half-cycle.

$$v_{m0} = R\left(I_D - \frac{\Delta i}{2}\right) + V_{C_L0}$$

The ratio of the peak-to-peak change in voltage to the peak-to-peak change in current gives a measurement of the resistance of the load line cables, plus another signal distortion term that comes from charging and discharging the load capacitor.

$$\Delta v_m = v_{m1} - v_{m0} = R\Delta i + \frac{\Delta i}{4C_L f}$$

$$R = \frac{\Delta v_m}{\Delta i} - \frac{1}{4C_L f} \tag{2.1}$$

2.1.2 Constraints on Field of Application from the Error Term

The load capacitance of the connected device can vary between 1μF and 10μF from device to device and will not be known prior to the circuit's implementation. The load capacitance, therefore, cannot be assumed in implementing the technique. This imposes the constraint, when implementing this technique, that the entire change in the voltage measured over the load line cable's terminals, Δv_m, must be assumed to be contributed by the resistance of the load line cables.

$$R_m = \frac{\Delta v_m}{\Delta i} \tag{2.2}$$

This condition imposes the constraint on the application of this method that $\frac{1}{4C_L f} \ll \frac{\Delta v_m}{\Delta i}$, in order for the measured value of the resistance of the load line cables, R_m, to be a viable estimate. If R_m is assumed to be the resistance of the load line cables, then the fractional error between the regulation voltage $V_{Reg.}$, and the voltage at the USB port, V_{USB}, is

$$\left|\frac{\Delta V_{error}}{V_{Reg.}}\right|_A = \frac{I_D}{4C_L f V_{Reg.}} \tag{2.3}$$

Equation 2.3 shows that method A can only be utilized in circuits that allow for a large load capacitance at the end of the load line cable pair, a high frequency of operation, and minimal current. The only variable that can be used in equation 2.3, to reduce the regulation error using method A in the automotive USB application is

the frequency of operation, f. The frequency of operation should be maximized in order to minimize this error, however, table 1.1 shows that it has an upper bound of 400kHz in typical automotive applications. Section 2.4 details a comparison between this solution, method B, and method C, for automotive USB buck application.

2.2 Method B: Direct Impedance Measurement

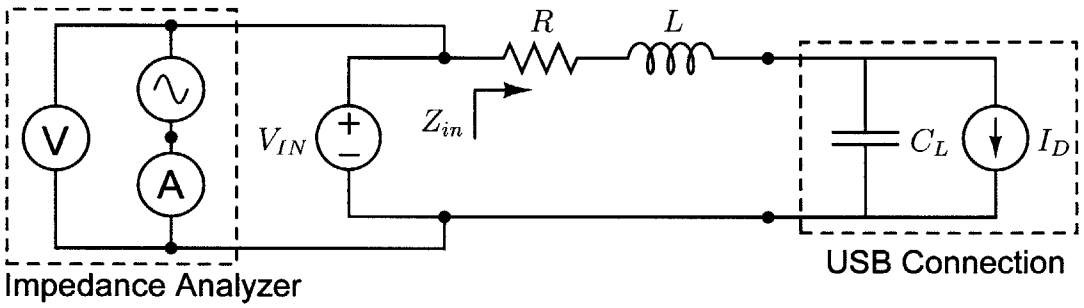

Figure 2-3: Circuit implementation of method B.

The direct impedance measurement technique, method B, focuses on taking a direct measurement of the resistance of the load line cables using an impedance analyzer. Its implementation is depicted in figure 2-3. The impedance analyzer consists of an ac power source in series with a vector ammeter. This branch is then connected in parallel with a vector voltmeter. The rest of the circuit, consists of a voltage source, V_{IN}, representing the power supply, connected via the load line cables to a portable device, represented by a load capacitor, C_L, in parallel with a current source, I_D. The load line cables are represented by a resistor of resistance, R, in series with an inductor of inductance, L. The impedance analyzer uses an AC voltage source to inject an AC voltage at the measurement node. The resulting drawn AC current is compared to the AC voltage and is used to calculate the impedance of the circuit at the frequency of interest. The power supply, V_{IN}, can be constructed to have a large impedance at the frequencies of interest relative to the load line network so that that the impedance analyzer will only see the load line network, and not the two in parallel. The measured impedance can then be used to infer the resistance of the load

line cables.

$$Z_{in}(s) = R + Ls + \frac{1}{C_L s} = |Z_{in}(s)|\, e^{j\angle Z_{in}(s)} \tag{2.4}$$

2.2.1 Input impedance of Mobile Electronic Devices

In order to understand the feasibility of this method, it was first important to look at the input impedance of several portable electronic devices in order to understand how their individual input impedances will affect the charging network's total impedance measurement. The input impedances of several mobile electronic devices are depicted in figures 2-4, 2-5, and 2-6. The method of collecting the data for these plots is detailed in appendix B. One can see through these plots the potential for a high frequency measurement of the resistance of the load line cables of the charging network to be distorted by the effective input impedance of a connected device.

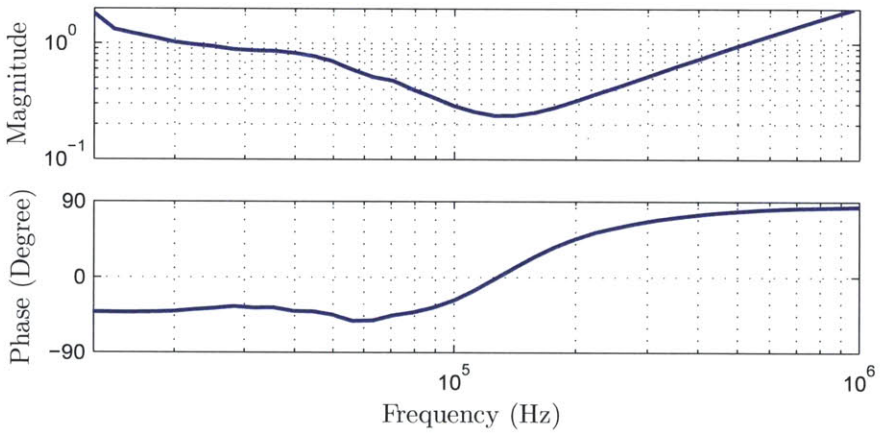

Figure 2-4: Input impedance of iPad 3G ($I_D = 2$A, $V_{USB} = 5.03$V).

The easiest frequency at which to observe the input resistance of the connected device is at the input impedance's resonant frequency because at this frequency the effective series combination of the inductor and capacitor looks like a short circuit. The effective input resistance at the resonant frequency is large for each device relative to the expected resistance of the load line cables. This is an issue because the measurement should only infer the voltage drop over the load line cables and this requires the input resistance of the connected device to look small. If the effective

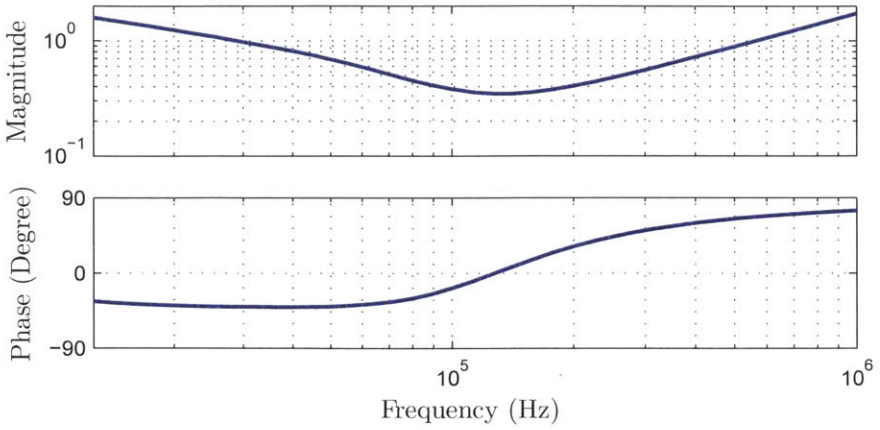

Figure 2-5: Input impedance of iPhone 5G ($I_D = 990\text{mA}$, $V_{USB} = 5.19\text{V}$).

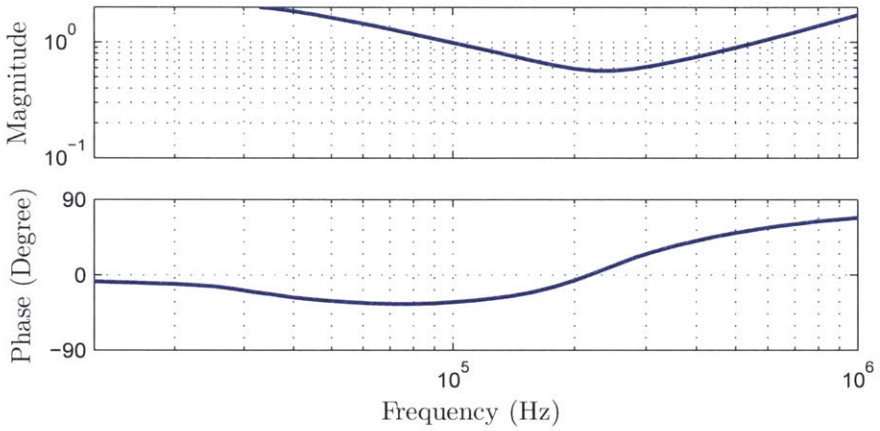

Figure 2-6: Input impedance of iPod Nano 3G ($I_D = 340\text{mA}$, $V_{USB} = 5.13\text{V}$).

input resistance of the device is too large, the error in the measurement of the voltage drop inferred over the load line cables will be too large.

There are several factors that contribute to this effective input resistance. Figure 2-7 shows a more accurate schematic of the input impedance of a connected device. First, there is contact resistance between the USB port and the internal circuitry of the connected device. This contact resistance varies probabilistically from connection to connection, but was measured on average to be 100mΩ in the iPod Nano 3G. Second, many mobile electronic devices that rely on USB charging have protection circuitry

between their input ports and the charging circuitry. This protection circuitry adds impedance to the current path within the connected device. On top of the protection circuitry, internal parasitic resistances that vary with frequency, such as ESR from the load capacitor, also contribute to the measured input resistance. A measurement of the input resistance can be extracted from an impedance measurement at values away from the resonant frequency of the device's internal impedance, but constant resistances, series resistance from the protection circuitry, and frequency dependent parasitics will affect the impedance measurements at other frequencies as well.

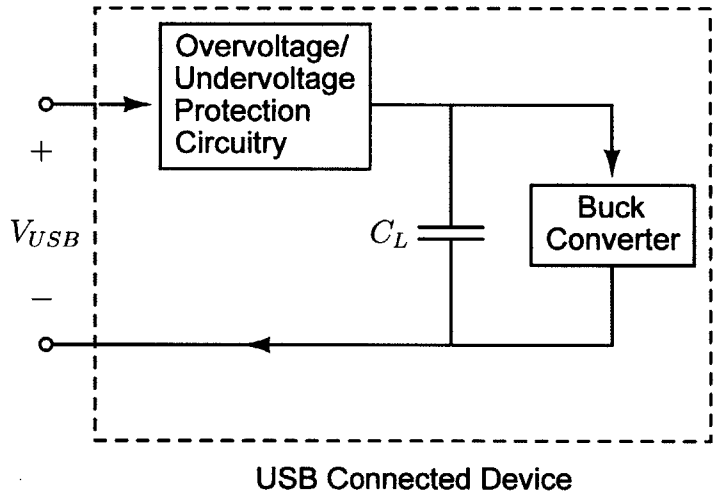

Figure 2-7: Block diagram of connected device's input impedance.

2.2.2 Effect of Device Input Resistance on Voltage Regulation

The voltage this technique is regulating the voltage at the USB port, not the voltage at the load capacitor. The load capacitor, however, is the decoupling capacitor in the frequency measurement, and this means that any input resistance seen between the input terminals of the connected device and the load capacitor will be included in the measurement of the load line resistance. At the same time, table 1.1 shows the resistance of the connecting cables, R, will be between 66mΩ and 333mΩ, which is of the same magnitude as the input resistances of the connected devices depicted

in figures 2-4, 2-5, and 2-6. The measurement depicted in figure 2-3 will measure the resistance of the line to be $R + R_{int}$, where R_{int} is the internal resistance of the connected device, and so the voltage at the USB port, V_{USB}, will be regulated to $V_{Reg.} + I_D R_{int}$.

$$\left|\frac{\Delta V_{error}}{V_{Reg.}}\right|_B = \frac{I_D R_{int}}{V_{Reg.}} \tag{2.5}$$

On top of this error, any of the parasitics that contribute to the total internal resistance of the connected device are frequency dependent, however, the measurement is meant to quantify the DC resistance of the load line cables. The measured internal resistance will not precisely equal the internal resistance of the connected device when the DC voltage and current are supplied. This will further distort the measurement of the load line resistance.

The direct impedance measurement technique is compatible with systems where a decoupling capacitor can be placed exactly at the point at which one wants to regulate the voltage. These systems should draw minimal current and have negligible parasitic impedance over the network whoes voltage drop is to be compensated, compared to the DC impedance of the network.

2.3 Method C: Current Interrupt Measurement

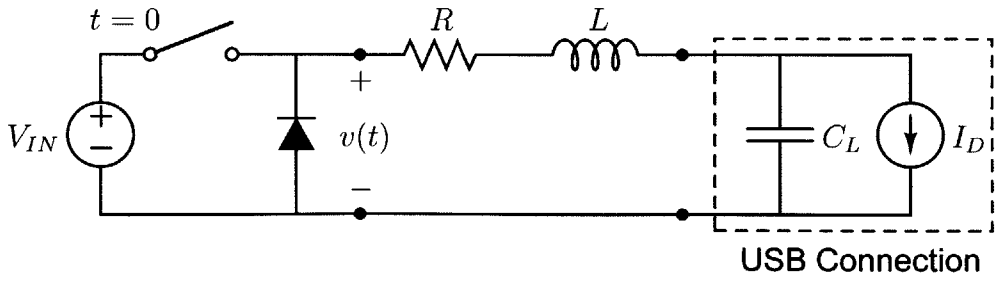

Figure 2-8: Circuit implementation of method C.

The third technique, method C, is labeled the "Current Interrupt Method" because it stops the flow of current into the charging network in order to bring the

voltage drop over the load lines to 0V, and then samples the voltage stored over the load capacitor as an approximation of the voltage at the USB port.

The implementation of method C is depicted in figure 2-8. The voltage source, V_{IN}, models the power supply, the resistance, R, and inductance, L, model the load lines, and the load capacitance, C_L, and current source in parallel, I_D, model the connected device. In this method, a switch separates the power supply and the load lines, and a protection diode with forward voltage, V_D, bridges the two input terminals of the load line network.

2.3.1 Analytical Solution of Method C

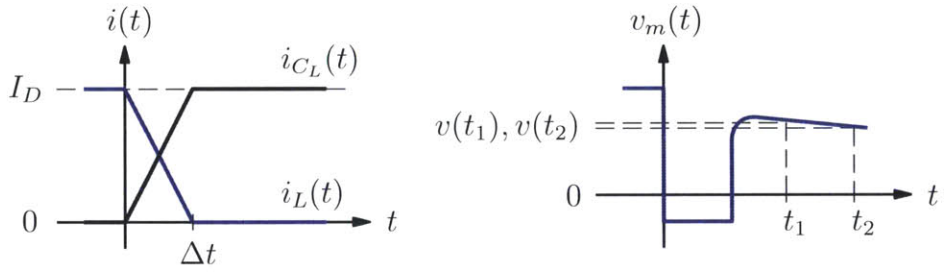

Figure 2-9: Plots depicting method C including the current delivered to the connected device and the measurement voltage waveform.

Initially the switch is closed and the current path is from V_{IN}, through the connecting load lines and into the current source of the connected device. The voltage over C_L equals the voltage at the USB port, V_{USB}, which is the voltage that should be regulated to $V_{Reg.}$. After the switch is opened at time $t = 0$, the current through the connecting load lines, $i_L(t)$, will ramp down to 0A, as shown in figure 2-9. Meanwhile, the current supplied by the load capacitor to the current source in the connected device, $i_{C_L}(t)$, will ramp up until it is supplying the entire load current, I_D. The voltage over the diode during this time frame is depicted in figure 2-9. After a time period of Δt there is no current through the diode and connecting load lines and the voltage drop over the connecting load lines will equal 0V. The voltage over the diode will equal the voltage over the load capacitor and so is sampled at time, t_m. This sampled

voltage equals V_{USB} minus the voltage dissipated from the load capacitor as a result of supplying power to the current source between the moment when the switch was opened and the sampling time.

$$\begin{aligned} V_{USB} &= v(t_m) + \int_0^{t_m} \frac{i_{C_L}(t)}{C_L} dt \\ &= v(t_m) + \frac{I_D}{C_L}\left(t_m - \frac{\Delta t}{2}\right) \text{ for } t_m \geq \Delta t \end{aligned} \tag{2.6}$$

Equation 2.6 shows that the voltage sampled over the diode at time, t_m, is equal to V_{USB} minus the error term that comes from the load capacitor being discharged. Figure 2-9 shows that in the case where two points are sampled, $(t_1, v(t_1))$ and $(t_2, v(t_2))$, an estimate of the voltage over the load capacitor before the "current interrupt" switch was opened can be calculated to further reduce the error in the inferred USB voltage, $\hat{V}_{USB,1}$.

$$\hat{V}_{USB,1} = \left|\frac{v(t_1) - v(t_2)}{t_1 - t_2}\right| t_1 + v(t_1) = V_{USB} + \frac{I_D}{2C_L}\Delta t \tag{2.7}$$

The time it takes for the current in the load lines to fall to 0A, Δt, is derived in appendix A.

$$\Delta t = \frac{LI_D}{V_D + I_D R + V_{USB}} \tag{2.8}$$

If $\hat{V}_{USB,1}$ from equation 2.7 is assumed to be the voltage at the USB port in steady state, then the feedback loop will servo to the point at which $V_{Reg.} = \hat{V}_{USB,1}$. Substituting equation 2.8 into equation 2.7, and solving for this servo point gives the steady-state voltage at the USB port as a function of circuit parameters.

$$V_{USB} = \frac{(V_{Reg.} - V_D - I_D R)}{2} + \sqrt{\left(\frac{V_{Reg.} + V_D + I_D R}{2}\right)^2 - \frac{I_D^2 L}{2C_L}} \tag{2.9}$$

From (2.9), $|\Delta V_{error}/V_{Reg.}|_3$ is plotted in figure (2-8).

Method C is most compatible with systems of minimal current and load line cable inductance, with a relatively larger load capacitor. Method C has the undesirable effect of strong EMI generation because of the "current interrupt" feature. Method

C is compared to methods A and B in section 2.4.

2.4 Comparison of Virtual Sense Techniques for Automotive USB Buck Application

In order to determine which of the previous three techniques is most appropriate for regulating an automotive USB buck converter, it is necessary to observe the derived errors in voltage regulation within the application space detailed in table 1.1.

The only variable that can be adjusted when implementing method A, in order to minimize the error in the voltage at the USB port generated by the technique, is the frequency of operation. The error is minimized when the technique's frequency of operation is maximized. As indicated in table 1.1, the maximum frequency of operation considered is 400kHz.

The only variable the applications engineer has control over in implementing method B is the frequency that the impedance analyzer operates at. Unfortunately, this is of little use because there are parasitic impedances at all frequencies of operation that will affect the impedance measurement. The errors of method A and method C will both become exacerbated by the effective DC internal resistance between the USB port and the load capacitor, however, method B also suffers from the parasitic resistances that come into play, and that are difficult to define, by using a high frequency measurement.

If one was trying to implement method B to charge the iPad, for example, one would observe this issue. The iPad's effective input impedance measured at resonance is 0.25Ω. Assuming $V_{Reg.} = 5V$, there would be a 0.5V error at the USB port if the technique were implemented, which corresponds to 10% error. It will become evident that method A and method Cs' errors can be reduced significantly below this.

Method A and method Cs' errors are definable and practical to mitigate, whereas method B's error will vary widely between devices. For these reasons, method B was not chosen as the technique to be implemented.

The only variable that can be adjusted when implementing method C is the forward voltage of the diode, v_D. Figure 2-10 compares the regulation error using method A and the regulation error using method C. In each case, $I_D = 2\text{A}$, and $V_{Reg.} = 5\text{V}$. Method A is assumed to be operating at 400kHz. Method C is assuming the diode's forward voltage is 0.4V. A 3m, 20AWG twisted pair cable was wound and its inductance, L, was found to be $1.6\mu\text{H}$. This value was used in the calculation of method B's error. While the error from each method is comparable, the error from method C is shown to be less than the error from method A for the entire range of load capacitors in consideration. Method C was therefore chosen as the technique to be implemented for the automobile's virtual sense voltage regulation loop.

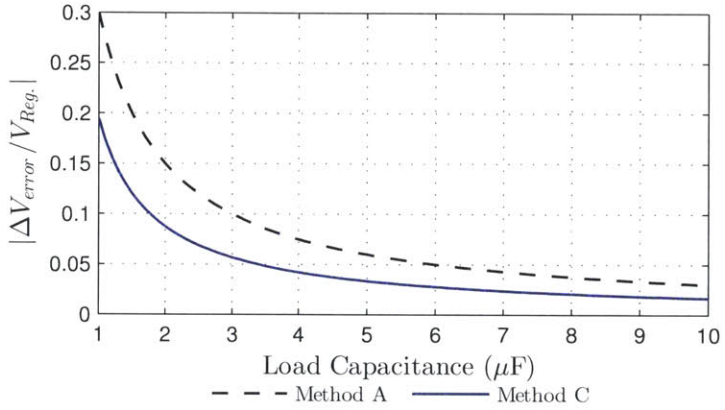

Figure 2-10: The smallest achievable errors in the worst case scenarios over the range of possible load capacitances for method A and method C.

Chapter 3

Feedback Loop Design for Current Interrupt Regulation Technique

3.1 The Backwards Projection Algorithm

The current interrupt method is a technique for sensing the voltage at the USB port by which a feedback path can be constructed and regulation can be implemented. Section 2.3.1 showed that if two samples are taken a more accurate sampling of the voltage at the USB port can be calculated.

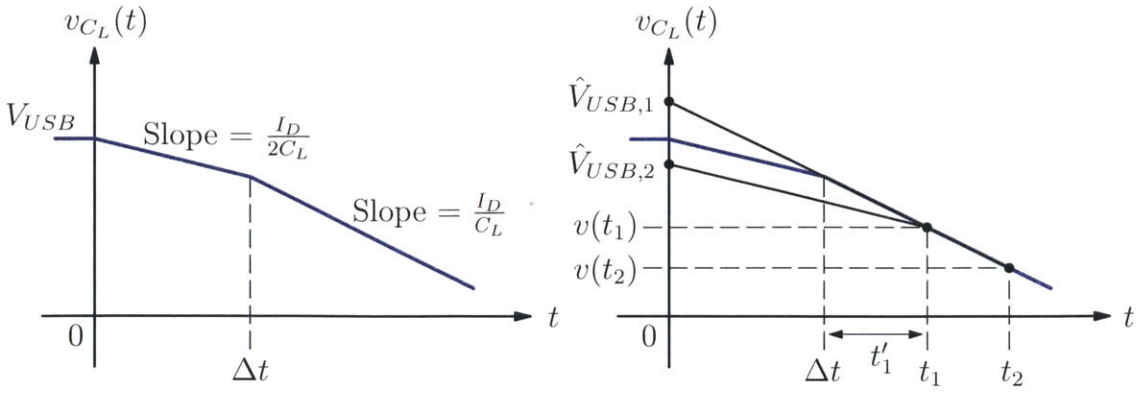

Figure 3-1: Depiction of algorithm.

The left-hand plot in figure 3-1 shows the voltage over the load capacitor once

the "current interrupt" switch is opened at time, $t = 0$. During the first time period, Δt, the voltage over the load capacitor dissipates at the rate $I_D/(2C_L)$. This is the period during which the current in the load lines is ramping down to 0A. Thereafter, the voltage over the load capacitor is being dissipated at the rate, I_D/C_L.

Two voltage samples can be taken, $v(t_1)$ and $v(t_2)$, once the current in the load lines is 0A and any transients in the voltage waveform have died out. This corresponds to the period when the voltage over the load capacitor is dissipating at a rate of I_D/C_L. The algorithm assumes the slope the voltage over the load capacitor has been dissipating at up until the first sample was taken, and then calculates what the voltage over the load capacitor was at the moment the switch was opened. Two natural slope assumptions are I_D/C_L, which corresponds to the first version of the algorithm, and $I_D/(2C_L)$ which corresponds to the second version of the algorithm. The first version of the algorithm was give by equation 2.7 and is repeated below.

$$\hat{V}_{USB,1} = \left|\frac{v(t_1) - v(t_2)}{t_1 - t_2}\right| t_1 + v(t_1) = V_{USB} + \frac{I_D}{2C_L}\Delta t \tag{3.1}$$

The other option for the algorithm assumes the voltage over the load capacitor is decreasing at half the rate assumed in the original technique up until the first voltage is sampled.

$$\hat{V}_{USB,2} = \left|\frac{v(t_1) - v(t_2)}{2(t_1 - t_2)}\right| t_1 + v(t_1) = V_{USB} - \frac{I_D}{2C_L}t_1 + \frac{I_D}{2C_L}\Delta t$$

Letting $t_1 = \Delta t + t_1'$, and $t_2 = \Delta t + t_2'$,

$$\hat{V}_{USB,2} = V_{USB} - \frac{I_D}{2C_L}t_1' \tag{3.2}$$

Versions 1 and 2 of the algorithm are illustrated in the right-hand graph in figure 3-1.

Comparing the errors of each algorithm, version 2 will be more accurate when faster time-to-sample speeds are achievable such that $t_1/2 < \Delta t$. Furthermore, the error from using version 2 decreases with faster time-to-sample speeds. Otherwise, version 1 should be used as it maintains a constant error of $I_D/(2C_L)\Delta t$ independent

of the time-to-sample.

3.2 Basic System Architecture

The basic system architecture of the automotive USB power delivery system without feedback regulation consists of the regulation voltage, $v_{IN}(s)$, minus the voltage drop over the load line which can be modeled as a system disturbance, $D(s)$, giving the voltage at the USB port, $v_{USB}(s)$. This system is depicted in figure 3-1.

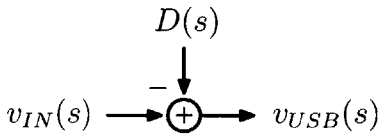

Figure 3-2: Basic power delivery system architecture.

The current interrupt method introduced in 2.3 is used to put a feedback loop around the system depicted in 3-1 with the intent of removing the steady-state effect of the voltage drop over the load line cables, $D(s)$, on $v_{USB}(s)$.

3.3 Feedback Loop

The current interrupt method is implemented through zero-order sample-and-hold circuitry combined with analog circuitry which performs mathematical operations corresponding to the backwards projection algorithm. In the following calculations, version 1 of the algorithm was assumed. The feedback path will therefore consist of a block representing the effect of the current interrupt method and following algorithm calculations on the signal cascaded with a zero-order sample-and-hold block.

3.3.1 Current Interrupt Method Block Model

Equation 2.7 combined with equation 2.8 shows that the current interrupt method infers the voltage at the USB port plus an error term that is a function of the voltage at the USB port.

$$v_{FB} = v_{USB} + \frac{I_D^2 L}{2C_L \left(V_D + I_D R + v_{USB}\right)} \tag{3.3}$$

where v_{FB} is the output of the current interrupt method's system block. The block diagram representation of the current interrupt method can be approximated by a gain block of magnitude equal to unity plus a constant error term. The error term in equation (3.1) is a non-linear function of v_{USB}, however, the error term can be linearized around the steady-state DC operating point of the circuit [9]. Taking ϵ to be the constant error term contributed by the current interrupt method,

$$\epsilon = \frac{I_D^2 L \left(V_D + I_D R + 2V_{USB}\right)}{2C_L \left(V_D + I_D R + V_{USB}\right)^2 V_{USB}^2} \tag{3.4}$$

The system block representing the current interrupt method can then be reduced to a gain block of gain $(1 + \epsilon)$.

3.3.2 Sample-and-hold System Architecture

The current interrupt method's calculation circuitry requires that the voltage measurements be acquired through zero-order sample-and-hold circuitry. If the sampling occurs periodically every T seconds, then the system block representation of the sample-and-hold is,

$$G_{SH}(s) = \frac{1 - e^{-sT}}{s} \tag{3.5}$$

which is mathematically equivalent to $v_{USB}(t)$ being sampled at time $t = nT$, and output from the feedback path as the voltage at the USB port until time $t = (n+1)T$ where a new voltage sample is taken [5]. The implication of the sample-and-hold block is that the system needs to consider the discrete time system effects. The consequence of this on the system's performance is that the system can become unstable because a delay is introduced in the feedback path in the relaying of information from the output to the control circuitry.

3.4 Control System Architecture

The purpose of the feedback loop is to compensate for the voltage drop over the load line cables, so an integrator needs to be used to compare the regulation voltage and the voltage at the USB port, and then incrementally increase the voltage supplied to the circuit from the power supply at a rate proportional to the error. This strategy ultimately sets the voltage at the USB port equal to the measured voltage from the feedback path, and so the only error between the voltage at the USB port and the regulation voltage will be from the error term inherent from the backwards projection algorithm.

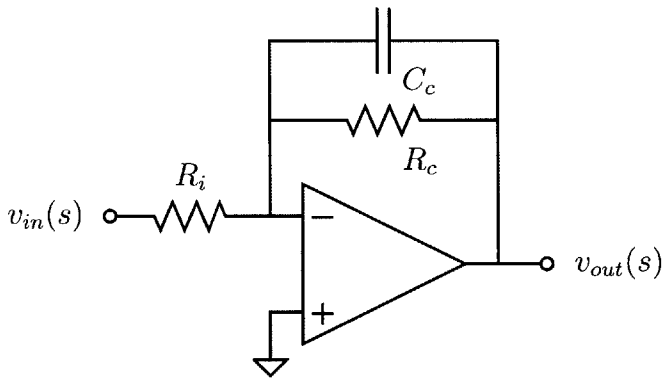

Figure 3-3: Practical circuit implementation of integrator.

Figure 3-2 shows the practical implementation of an integrator op amp circuit. The transfer function of the integrator block, $G_i(s)$, then takes the shape of a low-pass filter.

$$\frac{v_{out}}{v_{in}}(s) = G_i(s) = -\left(\frac{R_c}{R_i}\right)\frac{1}{R_c C_c s + 1} \tag{3.6}$$

The behavior of the system can be further optimized by cascading a gain block of gain $-K$ with the integrator block giving the compensation block the transfer function $G(s) = -KG_i(s)$.

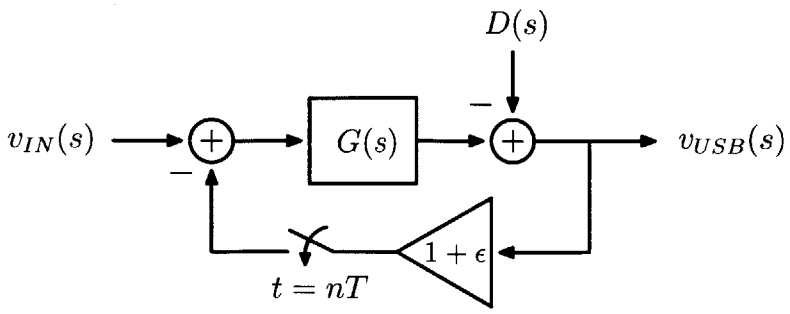

Figure 3-4: Voltage regulation control loop schematic.

3.5 Voltage Regulation Control Loop

3.5.1 Continuous-Time Analysis

The entire control loop can now be assembled and is depicted in figure 3-4. If the sample-and-hold effect on the system is ignored, the system can be approximated as a continuous time system. This corresponds to the sample-and-hold system operating at a high enough frequency such that the delay in the feedback path is negligible. Setting the disturbance equal to zero, the closed-loop transfer function is,

$$\frac{v_{USB}}{v_{IN}}(s) = \frac{KR_c}{R_iR_cC_cs + R_i + KR_c(1+\epsilon)} \tag{3.7}$$

This system is very stable with a single closed-loop pole. The ratio $R_c/R_i \gg 1$ so that the DC error in the loop is made negligible and inherently $1 \gg \epsilon$, therefore, the single pole is approximately located at

$$p \approx -\frac{K}{R_iC_c} \text{ for } K \ll R_c/R_i \tag{3.8}$$

The closed-loop system gain could be adjusted to push the pole outwards and speed the system up. If the system were still too slow, compensation could be added to reduce the phase margin and speed the system up.

3.5.2 Discrete-Time Analysis

The effect of the sample-and-hold block on the closed-loop system needs to be analyzed in order to understand the effect of the frequency of operation of the system, f, on the system's behavior. Appendix C shows the derivation of the discrete closed-loop transfer function in terms of z, where $z = e^{sT}$.

$$\frac{v_{USB}}{v_{IN}}(z) = \frac{(R_c/R_i)K(1 - e^{-T/(R_cC_c)})}{z - e^{-T/(R_cC_c)}(1 + (R_c/R_i)K(1+\epsilon)) + (R_c/R_i)K(1+\epsilon)} \tag{3.9}$$

A direct consequence of equation 3.9 is that the bottom limit on the operation frequency is given by

$$f > \frac{1}{R_C C_C \ln\left(\frac{R_C K(1+\epsilon)+R_i}{R_C K(1+\epsilon)-R_i}\right)} \approx \frac{K}{2R_i C_c} \text{ assuming } R_C \gg R_i \text{ and } 1 \gg \epsilon$$

If the system is operating at a slower frequency, the delay between control decisions will be too long and the integrator will effectively be over-correcting such that the error each time step is greater than the error from the previous time step. This corresponds to the system being unstable.

The upper bound on the frequency of operation is dependent on the behavior of the voltage over the load capacitor after the "current interrupt" switch is closed. After the switch is closed the load capacitor will charge to its steady state value which will result in an under damped second order step response over the load capacitor as a result of the relative values of the effective series resistance, inductance, and capacitance of the network. The oscillations must die out before the current interrupt method can be repeated. Otherwise, the measurement of the voltage at the USB port will be corrupted by the oscillations. When the switch is closed, the circuit looks like an RLC network with the effective resistance being equivalent to the sum of the load line resistance, R and the effective series resistance of the "current interrupt" MOSFET, R_{SW}. The time constant for this network is then $2L/(R + R_{SW})$, and so the voltage over the load capacitor has settled to within two percent of its final value after a time equal to four times the network's time constant; $t = 8L/(R + R_{SW})$. The time

between measurements, T, must therefore be greater than $8L/(R+R_{SW})+t_{sw}$, where t_{sw} is the time for which the switch is opened and the voltages at the measurement node are being sampled. Generally, $t_{sw} \ll 8L/(R+R_{SW})$, and so the upper bound on the frequency of operation of the circuit is given.

$$\frac{K(1+\epsilon)}{2R_iC_c} < f < \frac{(R+R_{SW})}{8L} \tag{3.10}$$

Equation 3.9 shows that in order to decrease the lower bound on the frequency of operation, the control loop must be slower. Decreasing the gain of the loop, K, achieves this, however, the trade-off is that the DC error between $v_{IN}(s)$ and v_{USB} increases. This is because there is a resistor in the inverting feedback path of the integrator op amp that is implemented in order to keep non-ideal DC bias currents from the op amp from saturating the capacitor in the inverting feedback path. It therefore creates a path in the system loop for a DC bias voltage that it inversely proportional to the gain K. Another option for decreasing the lower bound on the frequency of operation is to increase the time constant of the integrator by increasing R_i or C_C. Again, this will cause the system to take longer to settle to its final value. Many portable electronic devices have a small time allowance for perturbations in the voltage at the USB port to settle to the appropriate regulation voltage. If the system response is too slow and these perturbations do not settle out in time, the internal power circuitry of the connected device will shut off in some cases or become damaged in others. The integrator must operate at a sufficient speed so that perturbations settle within this allowed window of settling time.

The upper bound on the frequency of operation of the circuit is mostly dependent on the characteristics of the load line cable used. The inductance and the resistance of the load line cables probably cannot be manipulated for achieving a higher upper bound on the frequency of operation as they are generally predetermined constraints of the application. Increasing the effective resistance of the RLC network when the switch is closed is a method by which one may increase the upper bound on the frequency of operation. This can either be achieved by increasing the effective resistance

of the "current interrupt" MOSFET or by adding a resistor in series with the MOSFET. This will reduce the ringing after the switch closes and allow the switch to open sooner. This solution is a power inefficient solution because whenever the switch is closed, all the current supplied to the connected device must be pulled through the added resistor, however, more complex mechanisms, such as switching the resistor in and out of the current path at the appropriate times, may alleviate this issue.

3.6 Overview of Feedback Loop Behavior

The feedback loop behaves as a first order DT system. The operation constraints are such that the frequency of operation of the system be between $K(1+\epsilon)/(2R_iC_c) < f < (R + R_{SW})/(8L)$ for stability and signal integrity purposes. One may adjust these parameters within the circuit to achieve a higher or lower frequency of operation. Furthermore, one may add lag compensation circuitry to the feedback loop so as to decrease the phase margin and speed up the system even more.

Chapter 4

Implementation of the Current Interrupt Method

4.1 Considerations for Board Level Implementation of the Current Interrupt Technique

A board level implementation of the current interrupt method regulating a USB voltage while charging a portable device was constructed as a proof of concept. Several aspects of this method's implementation needed to be analyzed more thoroughly before a circuit board could be built up.

4.1.1 Device Characteristic Considerations for Power MOSFET and Protection Diode

The "current interrupt" switch that will periodically turn off and keep current from being drawn from the power supply into the load line cables will be implemented with a power MOSFET. Both the power MOSFET and the protection diode will have parallel parasitic capacitances that will affect the speed at which the technique can be performed as well as the integrity of the voltage signal at the measurement node.

It is important for the technique to occur as fast as possible. While the switch is open the diode will pull the measurement node below ground, at which point the energy stored in the load line cables will dissipate. Once that stored energy is dissipated, the measurement node will be pulled up to the value of the voltage drop over the load capacitor. Simultaneously, the voltage over the load capacitor is being dissipated. Although the backwards projection algorithm in the worst case is not dependent on the time at which the measurement is taken, there are practical limitations to how long the switch can remain open. As discussed in 2.2.1, there is over-voltage and under-voltage protection circuitry in each connected device. If the switch is open for too long, too much energy will be dissipated from the load capacitor and the undervoltage protection circuitry will trigger, pulling the device out of its "charging" mode.

On top of this, once the switch closes, there is a voltage step at the load capacitor back to its steady state value. In this configuration, the dominant components are the resistance of the load line cables in series with the effective resistance of the switch, the inductance of the load line cables, and the load capacitance. Observing the quality factor of the circuit with the switch closed, Q_{closed}, can give sufficient insight into the behavior of the circuit. The quality factor is the ratio of the energy stored in the circuit to the energy dissipated by the circuit, and gives an approximation for the number of oscillation cycles before the the voltage effectively settles out. For this series RLC circuit, the quality factor,

$$Q_{closed} = \left(\frac{1}{R + R_{sw}}\right)\sqrt{\frac{L}{C_L}}$$

The circuit is therefore underdamped in this configuration for the value of the components given. The magnitude of the effective voltage step from the closing of the switch is directly proportional to the time the switch is open, and so the amplitude of the ringing after the step is also proportional to the time the switch is open. If this amplitude is too great, the overvoltage or undervoltage protection circuitry will trigger and the connected device will stop charging.

The speed at which the technique can occur is limited by the parasitic capacitances at the measurement node. The voltage at this node is moved by the circuit slewing current into or out of the parasitic capacitances at this node and charging or discharging them. The time it takes to charge a capacitor of capacitance, C, some voltage, Δv, with a constant current, I_{charge}, is $\Delta t_{charge} = \Delta v C / I_{charge}$. Therefore, the parasitic capacitances from the "current interrupt" MOSFET and the protection diode must be minimized.

4.1.2 RC Snubber

The construction of the measurement node is the part of the circuit that requires the most care and consideration since this node is where the feedback loop acquires its measurement. The issue arises that the "current interrupt" MOSFET and protection diode contribute an effective parasitic capacitance, C_P, from the measurement node to ground. When the switch is opened, this parasitic capacitance will be the dominant capacitance of the network and it will create and LC tank with the inductance of the load line cables and the node will ring. This behavior is easier to see through analyzing the quality factor of the circuit in the open switch configuration, Q_{open}. Figure 3-1 depicts the effective RLC network when the switch is open [8].

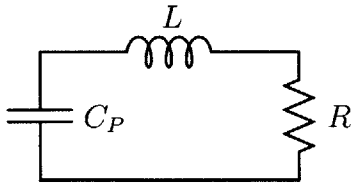

Figure 4-1: Effective RLC configuration for the uncompensated circuit.

$$Q_{open} = \frac{1}{R}\sqrt{\frac{L}{C_P}} \tag{4.1}$$

C_P is expected to be several orders of magnitude smaller than L, and R, and so the circuit will be severely underdamped. The resulting ringing will make it impossible for a measurement to be taken. The ringing can be alleviated with the implementation of an RC snubber. An RC snubber is a branch consisting of a resistor, R_S, in series

with a capacitor C_S. When used to branch the measurement node to ground, the capacitance can be sized such that it is the dominant capacitance of the effective RLC loop. The resistor can then be tuned in order to acquire an optimal quality factor which translates into optimizing the speed at which the measurement node settles after the switch is closed so that the first measurement can be taken.

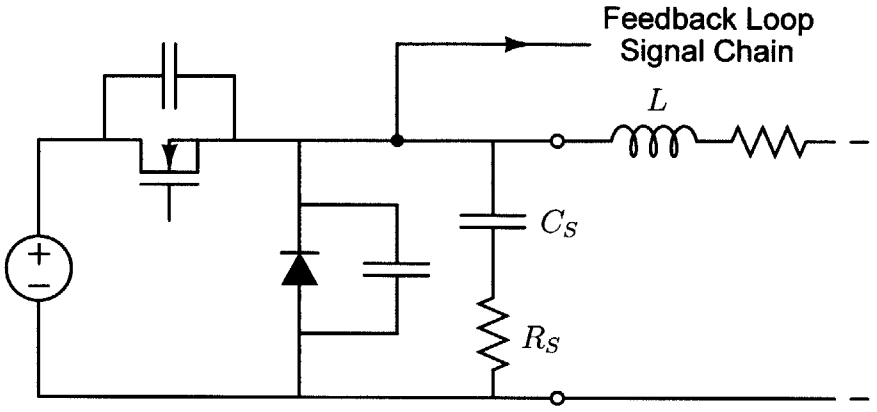

Figure 4-2: RC snubber implementation.

$$Q_{open,comp} = \frac{1}{R_S}\sqrt{\frac{L}{C_S}} \tag{4.2}$$

The RC snubber decreases the quality factor of the system, meaning it increases the ratio of the energy dissipated per cycle compared to the energy stored per cycle. The RC snubber accomplishes this by dissipating more energy per second through R_s, and increasing the length of time of each cycle by sizing C_S appropriately. The RC snubber therefore increases the length of time it takes for the voltage at the measurement node to settle so that it may be sampled.

4.1.3 Time-to-Sample

The final aspect of the regulation circuit that affects the integrity of the voltage measurement is the time-to-sample relative to the time when the switch is opened.

The time-to-sample also affects the functionality of the connected device. Most portable electronic devices have a mechanism that causes the device to stop charging

if the voltage at the USB port drops below a certain value. The longer the time-to-sample is, the lower the voltage at the USB port drops. Furthermore, when the switch closes again, immediately after the second voltage sample is taken, the circuit looks like an underdamped RLC network consisting of the load capacitance, the inductance of the load line and the resistance of the connecting load lines plus the effective series resistance of the MOSFET, and so the voltage at the USB port swings even lower. The time-to-sample must be quick enough such that the voltage at the USB port does not swing low enough for the connected device to stop charging.

In practice, with the board level circuit, the time to sample the first voltage measurement, t_1 is greater than $2\Delta t$. This is because the parasitic capacitances at the measurement node are large enough that the slew time of the voltage after the "current interrupt" switch is closed is too large. Therefore, version 1 of the backwards projection algorithm was implemented in the board level circuit.

4.2 Feedback Loop Signal Chain Implementation

The feedback loop circuitry is responsible for sampling the voltage at the measurement node twice after the voltage drop through the load line cables falls to zero. Then the feedback loop circuitry must conduct the calculation illustrated in equation 2.7. Finally, the feedback loop circuitry must process the measurement with the proper feedback compensation circuitry in order for the circuit to achieve appropriate stability and robustness. All together, the feedback loop signal chain consists of three parts: the sample and hold circuitry, the calculation circuitry, and the feedback compensation circuitry.

4.2.1 Sample-and-Hold Circuitry

The fundamental pieces of the sample-and-hold circuitry are the sampling capacitors, C_{SH1} and C_{SH2}, and their preceding analog switches that separate them from the measurement node. The analog switches close when the current interrupt switch opens, and then open again at times t_1 and t_2 respectively, completing the sample-

and-hold measurements.

The analog switches and sampling capacitors are preceded and followed by voltage buffers. The preceding buffer keeps the signal artifacts from the sampling behavior from distorting the measurement node signal. The following buffers keep the sampling capacitors from being loaded by the circuitry that follows the sample-and-hold circuitry, and so maintains the integrity of the sampled signals. The sample-and-hold circuit is depicted in figure 4-3.

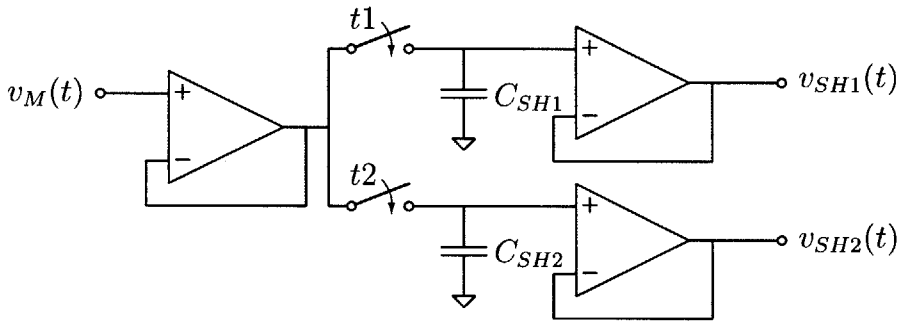

Figure 4-3: Sample-and-hold circuitry.

4.2.2 Calculation Circuitry

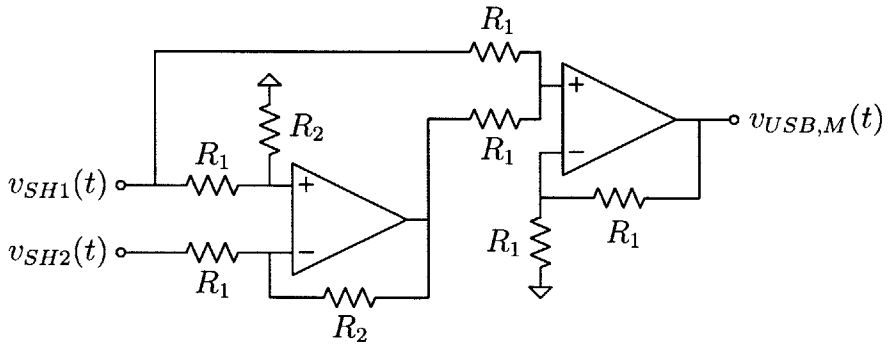

Figure 4-4: Calculation circuitry.

The calculation circuitry consists of an op amp in a subtracter configuration, cascaded with an op amp in a non-inverting adder configuration and is depicted in figure 4-4. The circuit takes the sampled signals as its input and outputs a measurement of

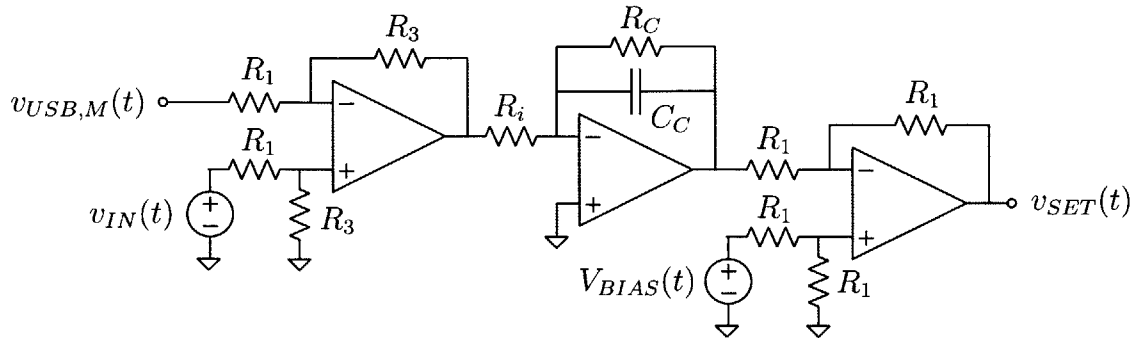

Figure 4-5: Control circuitry.

the voltage at the USB port before the current interrupt method was initiated.

$$v_{USB,M}(t) = \frac{R_2}{R_1}\left(v_{SH1}(t) - v_{SH2}(t)\right) + v_{SH1}(t) \tag{4.3}$$

From equation 4.3, $R_2/R_1 = t_1/(t_2 - t_1)$.

4.2.3 Control Circuitry

The control circuitry consists of three stages. The first stage consists of a subtracter configured op amp that outputs the difference between the regulation voltage, $v_{IN}(t)$, and the inferred voltage, $v_{USB,M}(t)$. The second stage consists of an inverting integrator configured op amp that takes the error between the regulation voltage and the inferred voltage at the USB port as its input. The third stage consists of a subtraction configured op amp that subtracts the output of the inverting integrator from a bias voltage, V_{BIAS}, and sets the voltage the power regulator supplies to the load line cables. The bias voltage is necessary in order to bias the network at an initial voltage in which it can operate. The control circuitry is depicted in figure 4-5.

The first stage of the control circuit has a gain of $K = R_C R_3/(R_i R_1)$. This is the DC loop gain of the system. K can be increased to increase the speed of the control loop, decrease the steady state error of the control loop, and increase the lower bound on the frequency of operation of the control loop.

4.3 Circuit Implementation and Results

The entire circuit was constructed and the schematic is depicted in figure 4-6. The actual board is depicted in figure 4-7. The final board successfully regulated the voltage at the USB port over 3 meters (in one direction) of 20 gauge cable and charged an iPod Nano (3G and 5G), an iPhone (4G and 5G) and an iPad (3G). The circuit is shown charging the iPad in figure 4-8.

4.3.1 Characteristic Waveforms of Current Interrupt Method

The circuit was first tested with a parallel RC connection modeling a connected device drawing 1A and then 2A from the circuit. The voltage at the measurement node for a single implementation of the current interrupt method is shown in figure 4-9. The waveform was sampled at $t_1 = 1.65\mu$s and $t_2 = 1.85\mu$s. The voltage at the USB port is depicted in figure 4-10 and the current drawn over the connecting load line is depicted in figure 4-11. Note that the periodic voltage dips in figure 4-10, and current dips in figure 4-11 correspond to the "current interrupt" switch opening and then closing. The current drawn over the connecting load line is slightly less than 2A. This is because the closest value to 2.5Ω that the appropriate power resistors could achieve was 2.7Ω.

4.3.2 System Step Response

The step response of the circuit is depicted in figure 4-12. The system has a first order step response with a single pole as defined by equation 3.6. The simulated step response is the response of the system function defined by (3.6) to the depicted voltage step. The low pass filter in the control circuitry consists of a 16.8nF capacitor and a 10MΩ resistor. The loop gain is $K = 500$, and so the settling time of the integrator is approximately 1.7ms.

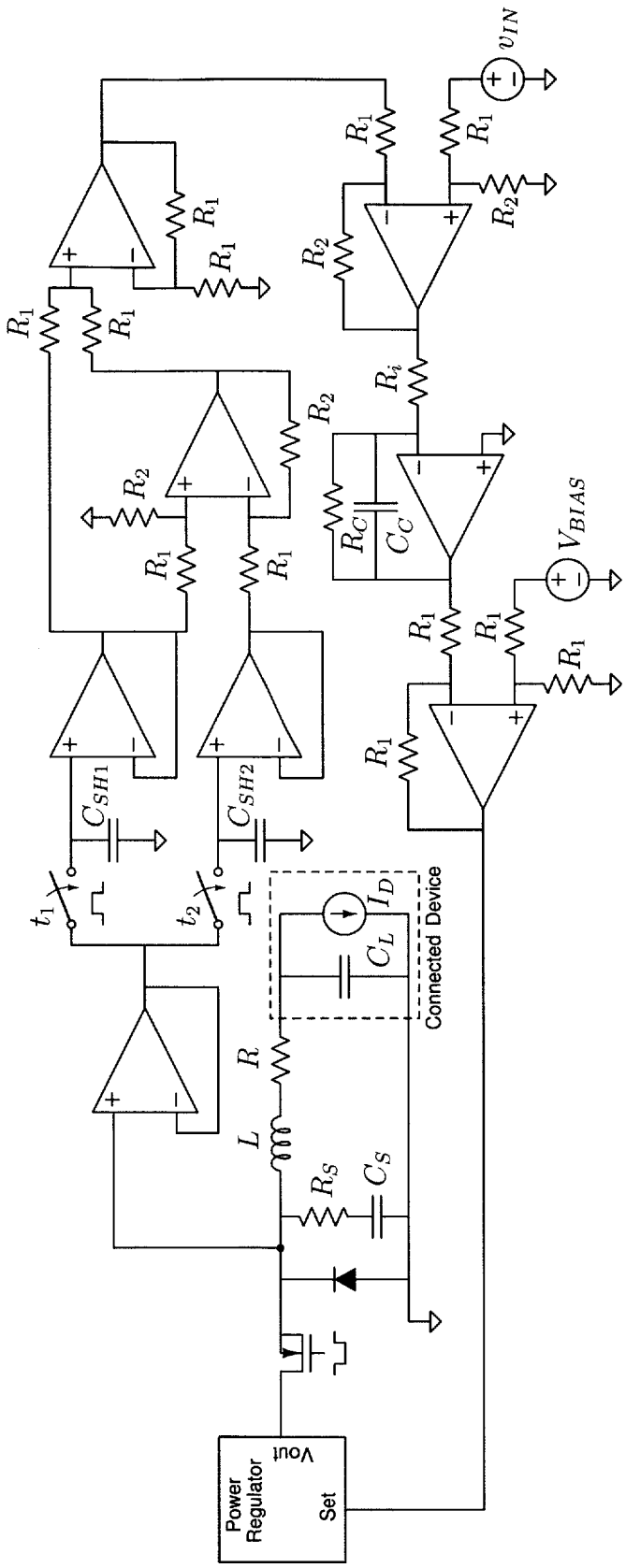

Figure 4-6: Full board level schematic of current interrupt method implementation.

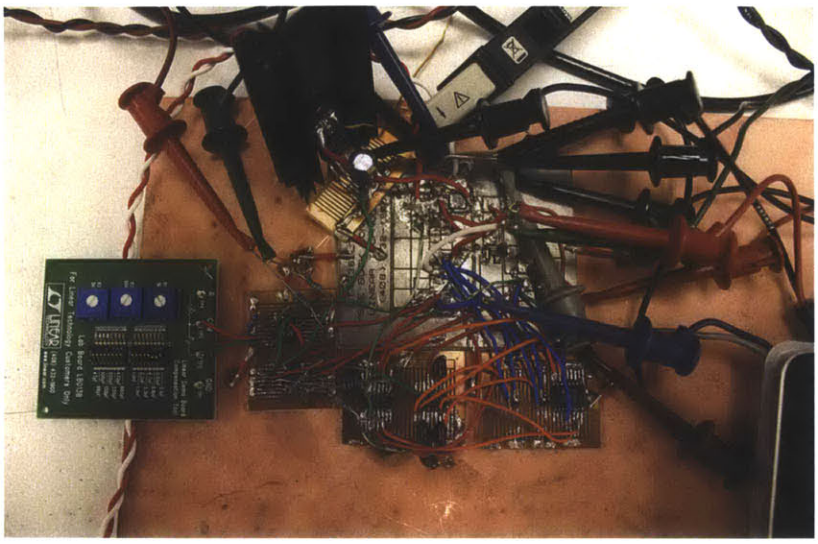

Figure 4-7: Board level implementation of "Current Interrupt Method" .

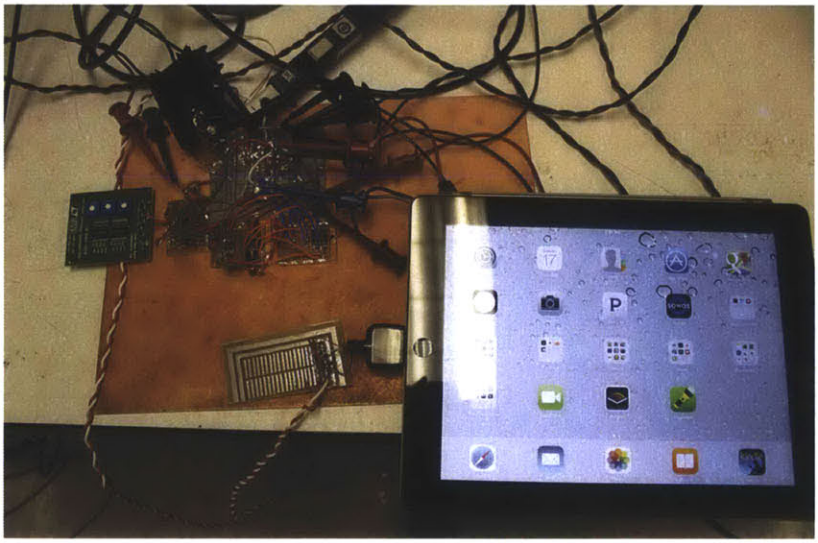

Figure 4-8: Board level implementation of "Current Interrupt Method" successfully charging an iPad 3G.

4.4 Invariance of Regulation

4.4.1 Load Current

The error in the voltage regulation at the USB port for different connected devices varies over load current. The iPod Nano 3G draws 0.3A of current, the iPhone draws 1A of current, and the iPad 3G draws 2A of current.

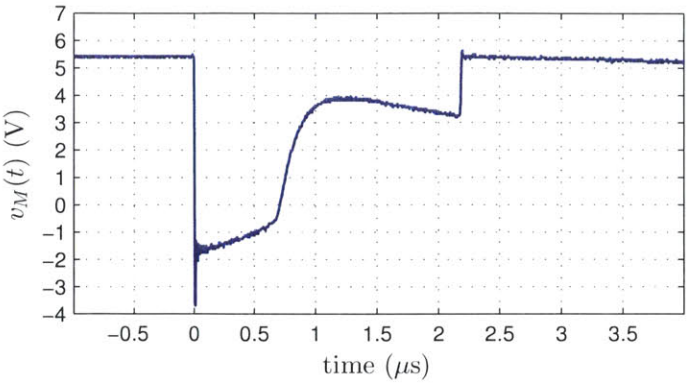

Figure 4-9: Voltage over the measurement node for the parallel RC connection drawing 2A.

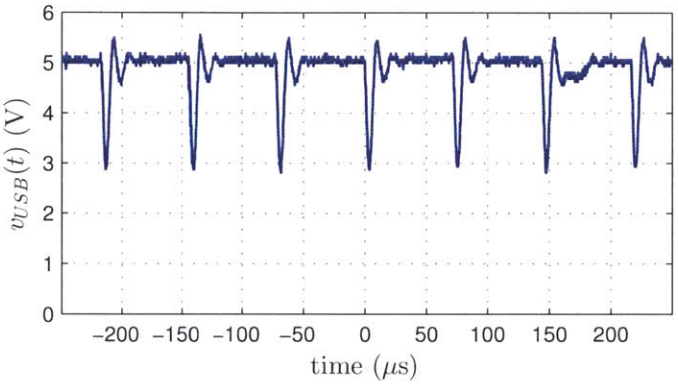

Figure 4-10: Voltage at the USB port for the parallel RC connection drawing 2A.

I_D	$V_{USB}(L = 1.6\mu\text{H})$	Device
0.3A	4.8V	iPod 3G
1A	4.97V	iPhone 4G
2A	4.85V	iPad 3G

Table 4.1: Variation in Voltage Regulation at USB Port over a range of connected device, load current, and load capacitance.

The iPod Nano 3G has a relatively larger error because, although it is only drawing 300mA of current, it has a small, $3\mu F$ load capacitor. The iPhone was drawing a

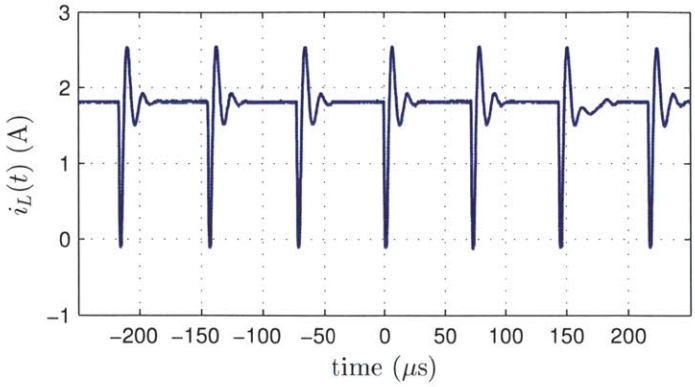

Figure 4-11: Current drawn over the connecting load lines for the parallel RC connection drawing 2A.

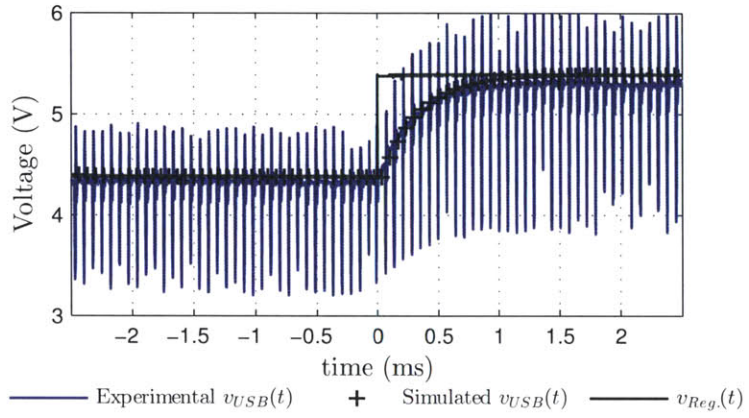

Figure 4-12: Measured step response of circuit compared with simulated step response.

moderately sized current of 1A, and was expected to have a moderately sized load capacitor. The iPad draws a substantial amount of current at 2A, and is expected to have a relatively larger load capacitor.

4.4.2 Different Cable Lengths

The voltage at the USB port does not vary strongly with changes in cable length. Reducing the length of the cable reduces the resistance of the connecting cables, and so the voltage drop that occurs with the power delivery to the connected device.

The voltage at the measurement node will settle faster and so the technique will be able to sample more quickly. Furthermore, the quality factor of the circuit following the closing of the switch will be smaller because of the smaller effective inductance. These two factors will decrease the likelihood that the connected device will switch out of "charging mode" during the circuit's operation.

Cable Length	$V_{USB}(C_L = 4.7\mu\text{F}, I_D = 1\text{A})$
1m	4.87V
2m	4.87V
3m	4.87V

Table 4.2: Variation in Voltage Regulation at USB Port Over Cable Length

4.4.3 Range of Output Capacitors

Table 4.3 shows the variation in the voltage regulated at the USB port as the load capacitor value varies. The error between the voltage regulated at the USB port and the regulation voltage is proportional to $C_L^{-1/2}$. It is also proportional to the load current, I_D. The data in table 4.3 was collected from the regulation of an RC load drawing 1A and then 2A while the capacitor was varied. The trend seen in the data in table 4.3 demonstrates these relationships.

Load Capacitor	$V_{USB}(I_D = 1\text{A})$	$V_{USB}(I_D = 2\text{A})$
10μF	4.97V	4.85V
4.7μF	4.87V	4.55V
2.2μF	4.80V	4.34V
1μF	4.57V	4.28V

Table 4.3: Variation in Voltage Regulation at USB Port Over Load Capacitor Value for $L = 1.6\mu$H.

4.4.4 Frequency Variation

The variation in the voltage regulated at the USB port as the frequency of operation is varied is depicted in figure 4-13. The upper and lower bounds for the frequency of operation are given by equation 3.9. The load for this experiment was a 2.7Ω resistor in parallel with a 5μF load capacitor.

From the equations given, the voltage regulated at the USB port should be largely independent of the frequency of operation, however, figure 4-13 shows a dependence. This dependence is a result of a combination of second order effects that are discussed in section 4.5.

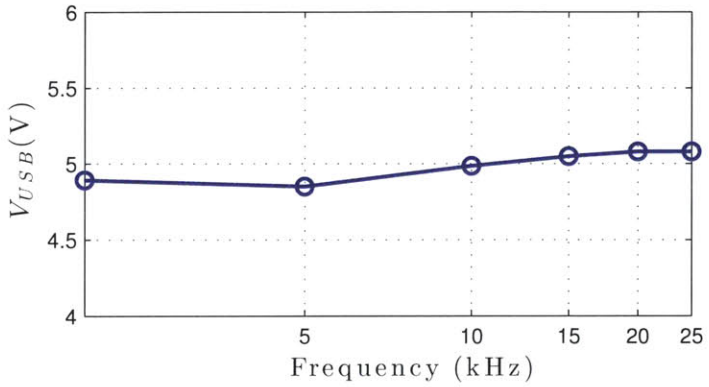

Figure 4-13: Variation in USB voltage over range of frequency of operation.

One issue is that the range of frequency operation given by equation 3.9 is mostly within the audible frequency range for humans: 20Hz - 20kHz [10]. The circuit should operate outside this range of frequencies so as to avoid disrupting the other individuals in the car. This is most likely achievable by relaxing the upper bound on the frequency of operation.

4.4.5 Variation in Open Switch Time

Figure 4-14 shows the variation in the voltage at the USB port as the length of time for which the "current interrupt" switch is open. The error between the regulation

voltage and the voltage at the USB port is not a function of the length of time the switch is open. The minimum amount of time the switch can be open is for 2μs because this is the amount of time it takes after the switch is opened for the current in the load cables to dissipate and for the voltage at the measurement node to settle to the value of the voltage over the load capacitor appropriately so that the first and second sample can be collected appropriately. The maximum amount of time the switch can be open is for 5μs. For time lengths greater than this, the rebounding oscillations after the switch is closed are large enough that the connected device triggers out of its "charging mode".

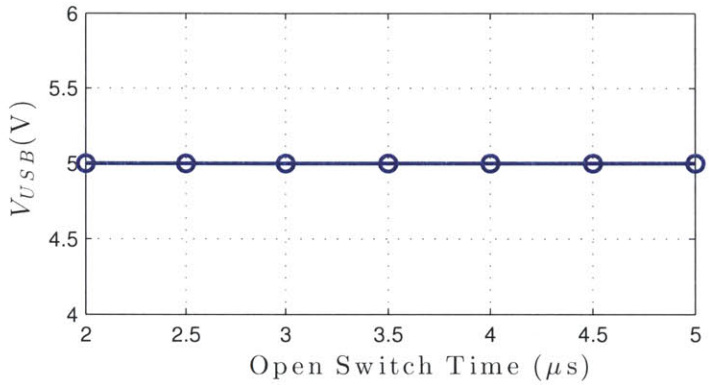

Figure 4-14: Variation in USB voltage over range of open switch times.

4.5 Conclusion From Board Level Technique Implementation

The board level implementation of the voltage regulator successfully regulates the voltage at the USB port, remotely. The implementation suffers from a combination of second order effects that make the regulation technique's implementation difficult to improve upon. An understanding of the parasitic effects in the circuit is necessary in order to reduce their effects or use them to the technique's advantage.

4.5.1 Parasitics at the Measurement Node

One of the shortcomings of the board level circuit is the speed at which the samples can be taken. The circuit takes too long to sample the voltage at the measurement node which occasionally causes the connected devices to exit "charging" mode due to the ringing after the switch is closed. This causes the voltage over the load capacitor to drop too low.

After the "current interrupting" switch is closed, it is important that the voltage at the measurement node be slewed down as fast as possible so that the current in the load lines can be dissipated as fast as possible. The capacitance of the power MOSFET and the diode are mostly responsible for determining the slew rate. In the board level circuit, components were chosen to minimize the parasitic capacitance of these devices, however, further minimization though an integrated implementation of the system would further shorten the wait time between closing the switch and sampling the voltages at the measurement node.

4.5.2 Errors in Sampling Time

The value of the reconstructed voltage at the USB port that is used as an input into the control feedback circuitry must be as free from errors as possible. Errors in the sampling time contribute largely to errors in the regulation scheme.

The board level sampling time and switch control are exceptionally difficult to implement accurately. The board level was implemented using pulse generators to control the sampling time. The pulse generators can drift tens of nanoseconds over time, especially as they heat up. This is enough to contribute a noticeable error to the voltage measurement. Furthermore, the used delay chips and analog switches, combined, can contribute an error of at most 300ns to the sampling time which is large enough to severely degrade the USB voltage measurement.

An integrated implementation of the system would allow for more accurate control of the sampling time and so lessen these shortcomings in the board level regulation scheme. The integrated implementation would accomplish this because of its tighter

controllability, relative to board level chip delay blocks and analog switches, as well as be able to be triggered off of specific waveforms in the circuit and so operate more consistently.

4.5.3 Errors from Non-Ideal Aspects of the Load Line Model

The load line, throughout the time that the technique is being implemented, has a small, varying voltage drop that is non-linear over time due to the resistive and inductive nature of the cables. Even after the voltage at the measurement node settles out to a value approximately equal to the voltage over the load capacitor, there is a time varying current in the load cables, analytically derived in appendix A. This parasitic current contributes to a voltage drop between the voltage at the measurement node and the load capacitor of up to 300mV. This is enough to generate a substantial error the voltage at the USB port.

This error can be mitigated by picking sampling times that are close enough together so that the error added to the first sampled voltage is effectively canceled out by the error added to the second sample voltage since the sampled voltages are subtracted in the feedback loop. The sampling times must still remain far enough apart so that the signal chain is robust to random noise.

The optimal time to sample is after the current in the cables has settled out because the voltage drop over these cables will vary minimally at this point. Then this problem goes back to that discussed earlier about dissipating the energy stored in the load line cables as fast as possible once the switch is opened. This will allow for the signal chain to use more refined voltage samples in its calculation. An integrated implementation of the system can alleviate this problem as well.

4.5.4 Conclusion from Data

The data collected from the board level circuit shows that the regulation scheme will indeed work. The system implementation, nonetheless, would benefit from an integrated, transistor level implementation. A transistor level implementation would

reduce the effects of the parasitics in the circuit and allow for more tightly controlled sampling times. Improvements in both of these fields would strengthen the system and make it more robust to errors.

An integrated implementation would also allow the technique to complete more quickly, and so the system could operate more quickly. This would cause the oscillations after the switch closed to be smaller and so make the system more robust. This would also allow the system to operate outside the range of audible frequencies.

Ultimately, the conclusions from the collected data suggest a stronger system can be achieved through an integrated implementation of the technique. Therefore, a transistor level implementation of the technique was designed, built and simulated in LTSpice.

Chapter 5

Integrated Technique Implementation

5.1 Overview of the Transistor Level Circuit

A transistor level version of the circuit implementing virtual voltage regulation by use of the "current interrupt" technique was constructed and tested in simulation. The schematic for the transistor level circuit is presented in figure 5-1. The op amps and sample-and-hold circuit blocks have transistor level implementations depicted in figures 5-4 and 5-5 respectively.

The internal positive rail of the circuit from which the op amps and sample-and-hold blocks draw their power is 4V. The op amp preceding the sample-and-hold bocks divides the measured voltage by 2, allowing the signal the feedback chain is processing to remain within the voltage range of the different circuit blocks without becoming distorted. It also buffers the signal chain from the voltage variations at the measurement node. Voltages are added in and eventually subtracted out of the signal chain in order to keep the signal being processed from approaching either of the internal voltage rails and potentially becoming distorted due to the non-ideal behaviors of the op amps. The following three op amps are configured to reconstruct the voltage at the modeled USB port.

Another sample-and-hold is implemented between the calculation circuitry and

the compensation block. This sample-and-hold is triggered by a NOR gate with the trigger signals of the first two sample-and-holds as its triggering signals. When either of the previous sample-and-hold blocks are triggered, this sample-and-hold disconnects from the signal chain in order to minimize the noise and distortions that are fed into the compensation block.

Finally, the control is achieved by a low pass filter-configured op amp that behaves as an integrator. The integrator compares the reconstructed USB voltage to the reference voltage and then increases the voltage supplied by the power regulator by an amount proportional to the difference.

5.2 Improvements to Measurement Node's Sample Time

The sampling operation is able to occur more quickly than the the board level circuit's sampling operation. This is because the capacitances at the measurement node contributed by the "current interrupting" MOSFET and the protection diode are sufficiently smaller. The RC snubber is then reconstructed to optimize the wait time until the voltage at the measurement node can be sampled.

Furthermore, the transistor level implementation of the circuit gave opportunity to improve the accuracy and speed of the sampling operations. The sample-and-hold blocks are triggered by a timer pulse generator and the timer pulse generator is triggered by the "current interrupt" switch's gate driver. This allows for more accurate timing which improves the quality of the USB voltage calculation.

5.3 Improved USB Voltage Calculation Algorithm

The faster achievable sampling time from the integrated implementation allows for the use of the more accurate version 2 of the backwards projection algorithm for inferring the voltage at the USB port. Version 1 of the algorithm incurs a minimal error proportional to Δt, the time it takes for the voltage at the measurement node to

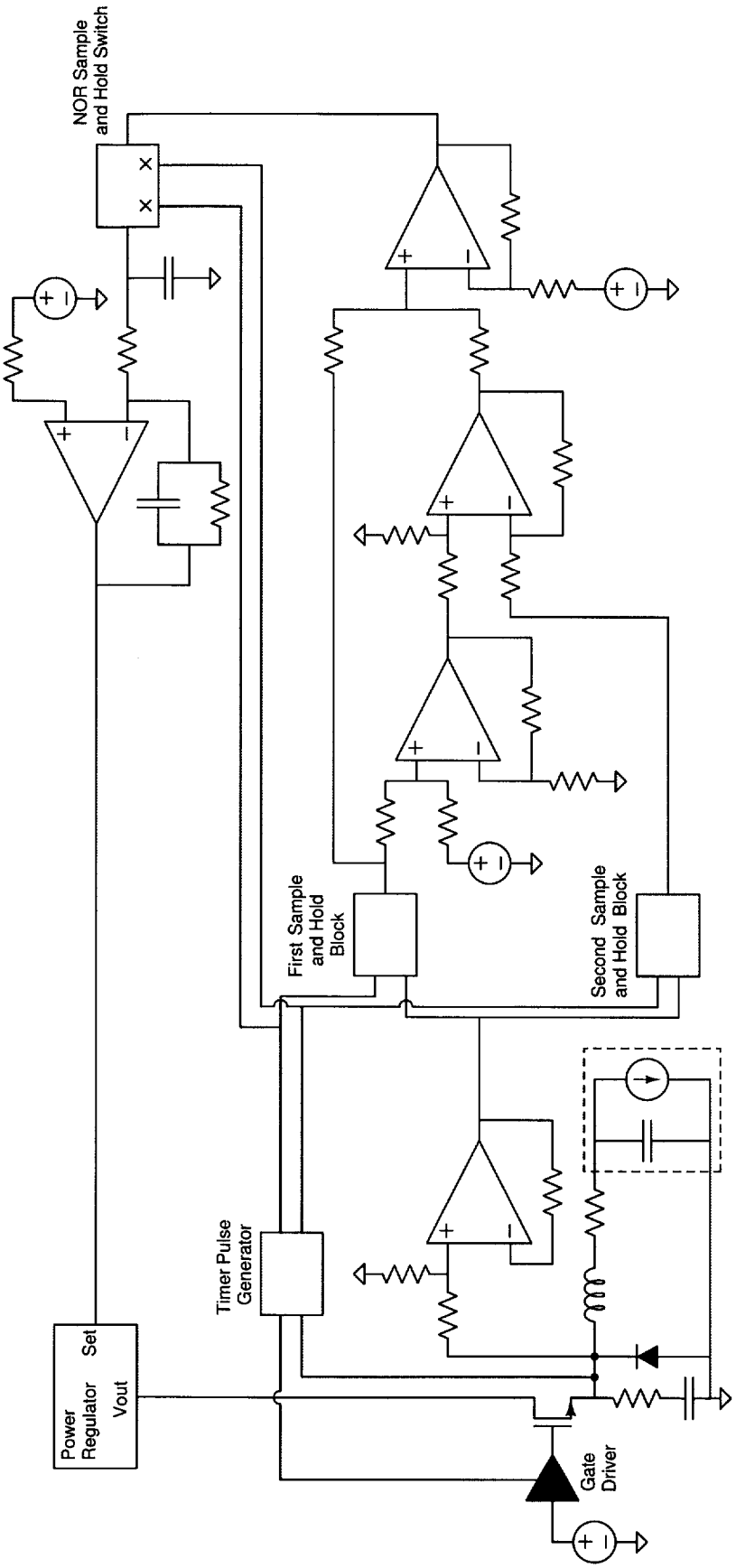

Figure 5-1: Full transistor level schematic of current interrupt method implementation.

settle to the value of the voltage over the load capacitor after the "current interrupt switch" is opened. This is because it assumes the voltage over the load capacitor was decreasing at the rate I_D/C_L over the time, Δt. This assumption is necessary in minimizing the error in the original technique because the time over which the voltage over the load capacitor is decreasing at the rate assumed is greater than the time over which it is decreasing at half the assumed rate.

Since the sampling time is quicker when utilizing the integrated circuit, a smaller error can be achieved by utilizing the second version of the algorithm where the voltage over the load capacitor is decreasing at half the rate assumed in the original technique.

Since $t_1 < 2\Delta t$, the improved regulation scheme will achieve a smaller error than the original regulation scheme. Furthermore, the error contributed to the measurement from the voltage drop over the load line cables is in the opposite direction from the error from the improved measurement technique. This will again reduce the error in the "current interrupt" technique's implementation.

Figure 5-1 shows the analytical and simulated percent error as the load capacitance is varied when the original technique is used. Figure 5-2 shows the analytical and simulated percent error as the load capacitance is varied when the modified technique is used. The reduced error in regulation can be seen from these plots.

5.4 Overview of Transistor Level Circuit Blocks

The transistor level implementations of the widely used op amp and sample-and-hold block were motivated by the goal of preserving the integrity of the signals used to calculate the voltage at the USB port. This corresponds to constructing a high speed op amp that can keep up with the high speed slewing at the measurement node. If the op amp is too slow, the sampled signal will become distorted. Likewise, the sample-and-hold sub-circuit needs to be constructed carefully to maintain the quality of the sampled voltages.

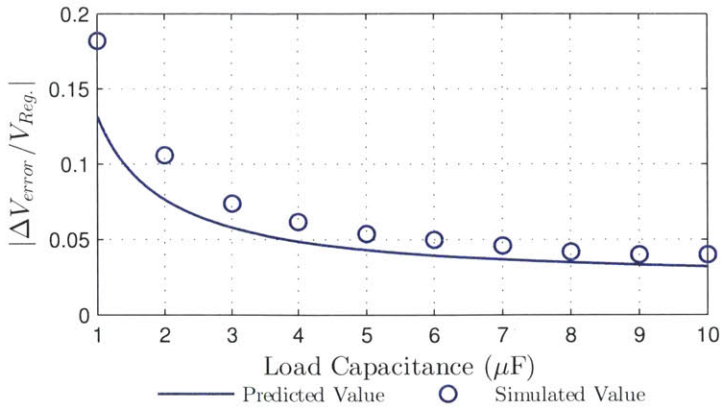

Figure 5-2: Percent error in voltage regulation at the USB as load capacitance is varied using the original method. The load current was taken to be 2A and the length of cable was taken to be 3m in the simulation.

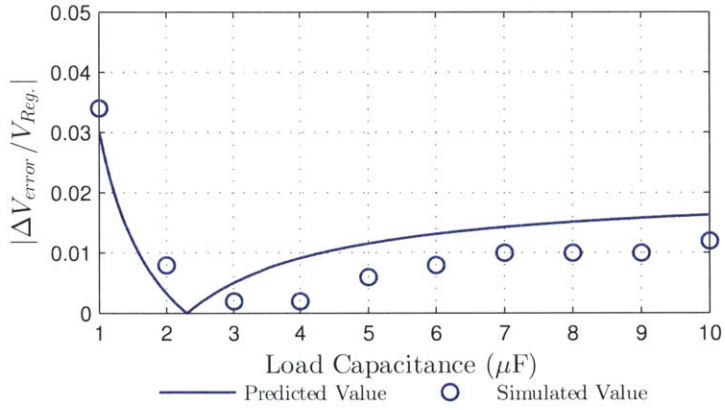

Figure 5-3: Percent error in voltage regulation at the USB as load capacitance is varied using the improved method. The load current was taken to be 2A and the length of cable was taken to be 3m in the simulation.

5.4.1 Op Amp Considerations and Design

The op amps used in the circuit all use the same topology depicted in figure 5-4. The component values of different op amps differ such that each op amp is optimized for its intended functionality.

The topology used is a two stage model with a folded cascode topology input stage cascaded with a common-source output stage. The folded cascode provides

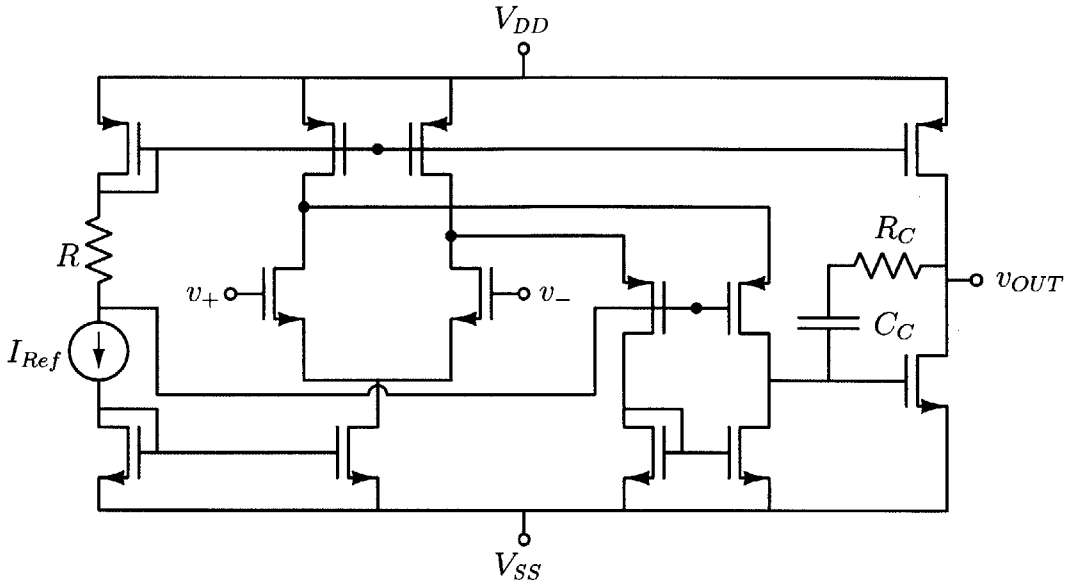

Figure 5-4: Transistor level design for op amps within circuit.

high speed operation with wide common mode input swing range [1]. The op amp was constructed to operate fast enough to act as a source follower for the voltage at the measurement node, which has an exceptionally high slew rate. The forced high bandwidth diminished the gain of the amplifier. The common source output stage was therefore implemented to provide further gain to the op amp and make the op amp's operation more ideal.

5.4.2 Sample-And-Hold Block

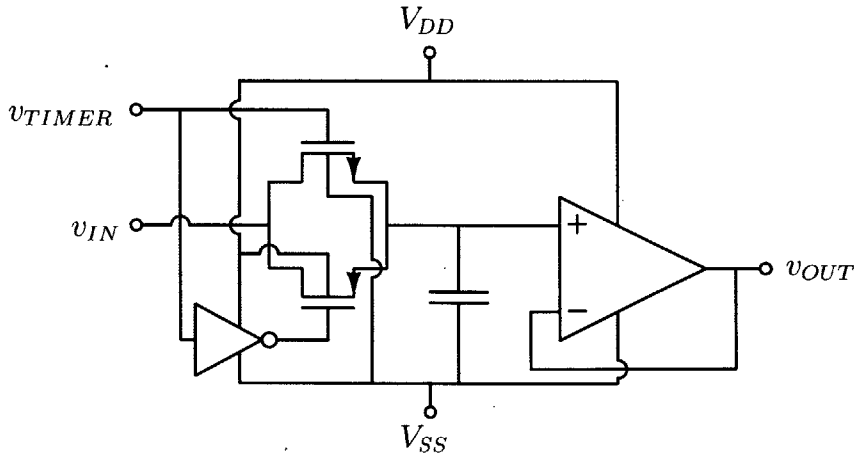

Figure 5-5: Transistor level design of sample-and-hold circuit block.

The sample-and-hold block's circuit diagram is depicted in figure 5-5. A bi-

directional complementary switch was implemented between the input and the sampling capacitor. The complementary devices were utilized in parallel to allow for the voltage being input to the sampling capacitor to swing from the ground voltage to the voltage of the positive rail. If the voltage at the input to the switch is close in magnitude to the voltage of the high rail then the pMOS device is enhanced. If the voltage at the input to the switch is close to ground then the nMOS device is enhanced. If the voltage at the input into the switch is in the mid-range between the voltage of the high rail and ground, then both devices are enhanced.

The parallel nMOS and pMOS device have the added benefit of providing charge injection cancellation from the turn-off behavior of the devices. This improves the integrity of the sampled voltage on the sampling capacitor.

Finally, a buffer-configured op amp protects the sampling capacitor from loading from the following sub-circuit.

5.5 Analysis of Simulated Voltage Regulation

The waveforms associated with the operation of the circuit are shown in figures 5-6 and 5-7. The "current interrupt" switch opens for a shorter amount of time than that seen in the board level implementation of the circuit.

The simulation was run for both the old algorithm and the new algorithm and the regulated voltage at the USB port is depicted in figure 5-7. The simulation was carried out for a device with a 5μF load capacitor drawing 2A of current over 3m of cable. The error from the use of the new algorithm is negligible while the error from the old algorithm is non-negligible.

Finally, the regulated voltage at the USB port is compared to the unregulated voltage at the USB port in figure 5-8. The simulation was carried out for a device with a 10μF load capacitor drawing 2A while the regulation circuitry was implemented utilizing the second algorithm. A connected device would not be able to charge without regulation as the voltage at the USB port is seen to be 4.6V. With regulation via the second algorithm the voltage at the USB port is regulated at 5V and a

connected device would be able to charge.

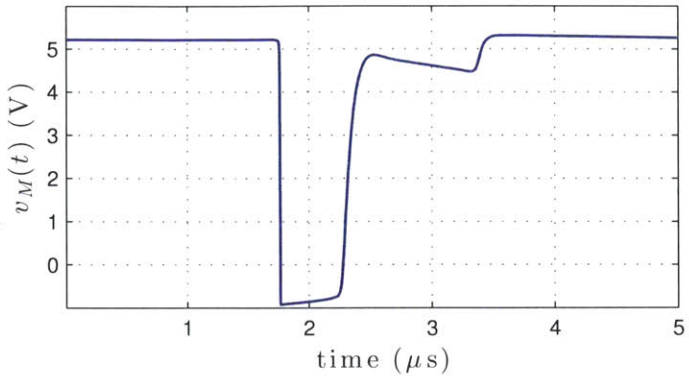

Figure 5-6: Voltage seen at the measurement node while the "current interrupt" switch is open.

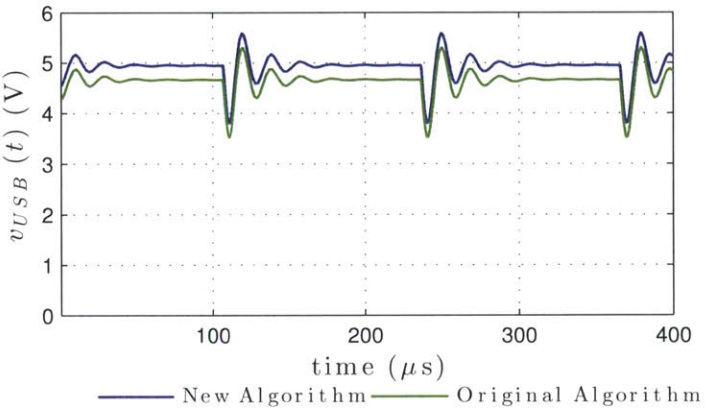

Figure 5-7: Voltage at the USB port regulated to 5V. The simulated connected device utilizes a 5μF load capacitor and is drawing 2A of current over 3m of cable.

5.5.1 Variation Over Load Current

The variation of the voltage regulated at the USB port over different load current was measured in simulation. The results from using the first algorithm are depicted in figures 5-9 and the results from using the second algorithm are depicted in figure 5-10.

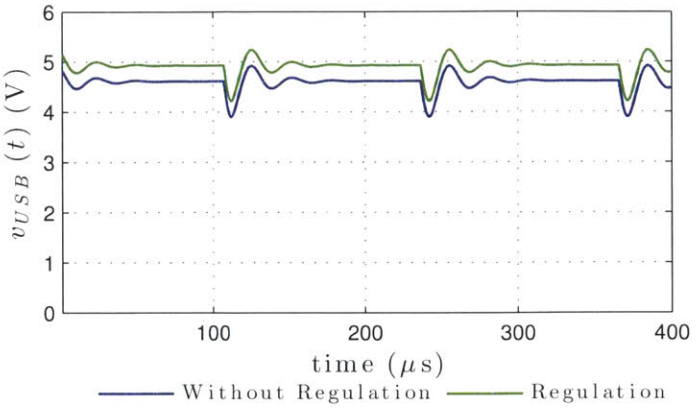

Figure 5-8: Comparision of the voltage at the USB port with regulation implemented via the second algorithm and without regulation. The regulation is over 3m of cable with a 10μF load capacitor.

In figure 5-9, the error in regulation increases rapidly with load current. This is because the current sourced from the load capacitor while the energy stored in the load lines is being dissipated is over estimated in the old algorithm's calculation. Equation 2.9 shows this error equals $I_D \Delta t/(2C_L)$. Neglecting Δt, which increases weakly with I_D, the error grows linearly with I_D.

In figure 5-10, the error in regulation corresponding to the new algorithm is $I_D\left(t_1 - \Delta t\right)/(2C_L)$. This error is an underestimate, and so the error from the technique pushes the regulated voltage above 5V. The error in the sampled voltages from the voltage drop over the load lines when the samples are taken due to the inductive characteristic of the load line, pushes the error slightly in the direction opposite the error from the regulation technique. This characteristic can be seen in the measurement corresponding to the 10μF load capacitor.

5.5.2 Variation Over Length

Increasing the length of the load cables corresponds to increasing the amount of magnetic energy the cables can store. This causes the time to wait until this stored energy is dissipated once the "current interrupt" switch is opened, Δt, to increase.

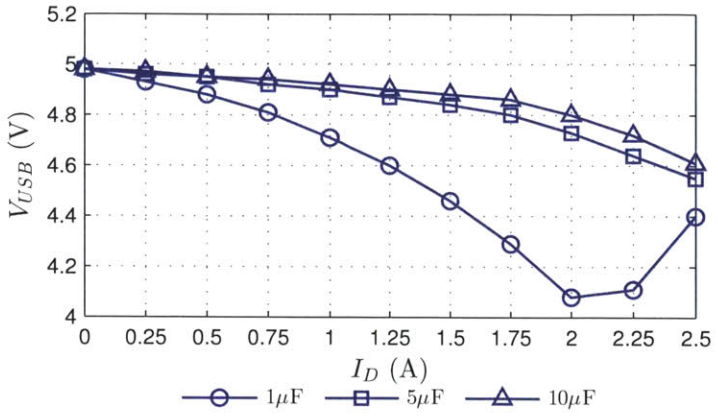

Figure 5-9: Voltage regulation at the USB as load current is varied using the first algorithm. The length of cable was taken to be 3m in the simulation.

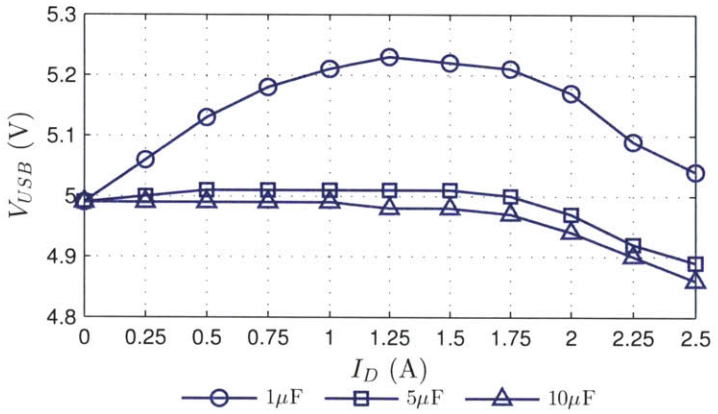

Figure 5-10: Voltage regulation at the USB as load current is varied using the second algorithm. The length of cable was taken to be 3m in the simulation.

Equations 2.7 and 2.8 can be used to show analytically that the error is linearly proportional to L. This trend is reflected in the data collected in figure 5-11.

5.5.3 Variation Over Temperature

The variation in the regulation of the voltage at the USB port over a range of temperatures is depicted in figure 5-12. The circuits within the system responsible for setting the timers were made symmetric so as to cancel out any distortions in the

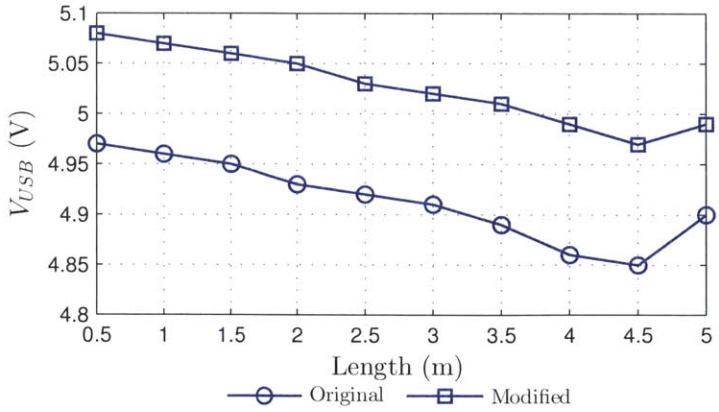

Figure 5-11: Voltage regulation at the USB as the length of the load line cables are varied. The load current was taken to be 2A and the load capacitor was taken to be 5μF in the simulation.

signaling waveforms.

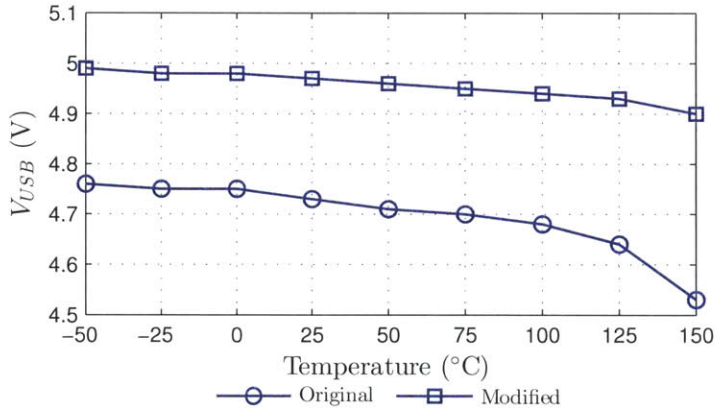

Figure 5-12: Voltage regulation at the USB as temperature is varied. The load current was taken to be 2A. The load capacitance was taken to be 5μF. The length of cable was taken to be 3m in the simulation.

5.6 Conclusion and Future Work

Overall the design and implementation of the automotive UBS voltage regulator with virtual voltage sense was successful. The natural next step would be to look at

integrating the circuit into a 12V to 5V buck converter IC.

At this point there are also aspects of the existing circuit that could be improved upon. The frequency of operation of the circuit is in the audible range. The upper bound on the operation frequency is the preferred bound to be adjusted because otherwise the circuit would have to slow down which may cause the feedback loop to servo to the steady state value. In this case connected devices may exit "charging mode". This time constraint is built into the connected devices and cannot be relaxed. In order to relax the upper bound on the operation frequency, larger series resistance can be added to the network in the configuration where the "current interrupt" switch is closed. In this case the circuit will dissipate more energy per oscillation cycle and settle out quicker. The current interrupt method can then be implemented more frequently.

More work can be done on increasing the speed of slewing at the measurement node in order for the time-to-sample to be further reduced. This would reduce the errors inherent in the backwards projection algorithms that reconstruct the voltage at the USB port. An example of a possible way of achieving this is by connecting the anode of the diode to -5V once the "current interrupt" switch opens. This will cause the current at the measurement to slew harder, and so the voltages at the measurement node to move around more quickly.

A second possible method of improving the time-to-sample could be to switch the RC snubber into the circuit with an appropriate voltage bias after the "current interrupt" switch is opened. When the snubber is not switched in it causes the transient response of the circuit to take longer to settle out after the "current interrupt" switch is opened. If it is switched in with a bias equal to that predicted to be the voltage the circuit would settle out to after the transients died out, less of an initial transient would occur and the time-to-sample would be able to be further reduced.

Finally, the circuit needs to be tested for its EMI generation. The "current interrupt" switch accomplishes a large, almost instantaneous change in current and this will generate radiation. This EMI should be analyzed in order to observe its potential effects on other circuitry within the car.

The pursuit of these improvements in the future will give the technique more potential as a viable product. Ultimately, the current interrupt technique holds promise in successfully achieving practical automotive remote load line regulation in cars.

Appendix A

Mathematical Derivation of Current Interrupt Method Circuit Characteristics

A circuit analysis of the Current Interrupt Method can provide further insight into the behavior of the network.

When the switch is first opened the diode sources current to the load line inductance and the snubber branch has a negligible impact on the circuit behavior. Using Kirchoff's voltage law in a clockwise loop:

$$v_D(t) + v_L(t) + v_R(t) + v_{C_L}(t) = 0 \tag{A.1}$$

where $v_D(t)$ is the forward voltage drop over the diode, $v_L(t)$ is the voltage drop over the inductor, L, $v_R(t)$ is the voltage drop over the resistor, R, and $v_{C_L}(t)$ is the voltage drop over the load capacitor, C_L. A differential equation describing the current through the inductor can be achieved by differentiating (A.1) and substituting in the appropriate current relationships.

$$\frac{d^2 i_L(t)}{dt^2} + \frac{R}{L}\frac{di_L(t)}{dt} + \frac{1}{LC_L} i_L(t) = \frac{I_D}{LC_L} \tag{A.2}$$

The particular solution for this differential equation is $i_{L,p} = I_D$. The homo-

geneous solution has the form $i_{L,h} = Ae^{\alpha t}\sin(\omega t + \phi)$, where $\alpha = -R/(2L)$ and $\omega = \sqrt{1/(LC_L) - (R/(2L))^2}$.

The first constraint is that the current in the inductor, immediately after the switch is opened, is I_D (i.e. $i_L(t = 0^+) = I_D$). The consequence of this is that $\phi = 0$.

The second constraint is that $di_L(t = 0^+)/dt = A\omega$. KVL can be used at $t = 0^+$ to find a relationship between $di_L(t)/dt$ and the other circuit parameters since the voltage drop over the inductor is a function of $di_L(t)/dt$. Rearranging (A.1) and solving for $di_L(t = 0^+)/dt$ gives,

$$\frac{di_L}{dt}(t = 0^+) = -\frac{1}{L}\left(V_D + i_L(t = 0^+)R + V_{USB} + \int_{0^-}^{0^+}\frac{i_L(t)}{C_L}dt - \int_{0^-}^{0^+}\frac{I_D}{C_L}dt\right) \quad \text{(A.3)}$$

(A.3) can be reduced to,

$$\frac{di_L}{dt}(t = 0^+) = -\frac{1}{L}(V_D + I_D R + V_{USB}) \quad \text{(A.4)}$$

(A.4) gives that $A = -(V_D + I_D R + V_{USB})/(L\omega)$. The equation for the current in this situation is then,

$$i_L(t) = I_D + Ae^{\alpha t}\sin(\omega t) \quad \text{(A.5)}$$

Taking the approximation that the current is decreasing at a constant rate until the diode turns off to be valid, the time it takes for this to happen, Δt, can be found by equating (A.4) to $di_L(t = 0^+)/dt \simeq -I_D/\Delta t$.

$$\Delta t = \frac{LI_D}{V_D + I_D R + V_{USB}} \quad \text{(A.6)}$$

For $t > \Delta t$, the diode has shut off and is effectively an open circuit and the RC snubber comes into effect. Using KVL, the new voltage loop equation is:

$$v_{C_s}(t) = v_{R_s}(t) + v_L(t) + v_R(t) + v_{C_L}(t) \quad \text{(A.7)}$$

where $v_{C_s}(t)$ is the voltage over the snubber capacitor and $v_{R_s}(t)$ is the voltage over the snubber resistor. Again, a differential equation describing the current through the inductor can be achieved by differentiating (A.7).

$$\frac{d^2 i_L(t)}{dt^2} + \frac{(R+R_s)}{L}\frac{di_L(t)}{dt} + \frac{C_L + C_s}{LC_LC_s} i_L(t) = \frac{I_D}{LC_L} \tag{A.8}$$

The particular solution to (A.8) is $i_{L,p}(t > \Delta t) = I_D C_s/(C_L + C_s)$. Letting $\beta = -(R+R_s)/(2L)$ and $\gamma = \sqrt{((R+R_s)/(2L))^2 - (C_L+C_s)/(LC_LC_s)}$, the homogeneous solution is:

$$i_{L,h}(t > \Delta t) = Be^{(\beta+\gamma)(t-\Delta t)} + Ce^{(\beta-\gamma)(t-\Delta t)} \tag{A.9}$$

From (A.5),

$$i_L(t = \Delta t^+) = I_D + Ae^{\alpha \Delta t}\sin(\omega \Delta t)$$
$$\frac{di_L}{dt}(t = \Delta t^+) = A\omega e^{\alpha \Delta t}\cos(\omega \Delta t) + A\alpha e^{\alpha \Delta t}\sin(\omega \Delta t)$$

. These conditions can be used to show:

$$C = -\frac{1}{2\gamma}\left(\frac{di_L}{dt}(t = \Delta t^+) - \left(i_L(t = \Delta t^+) - \frac{C_s}{C_L + C_s} I_D\right)(\beta + \gamma)\right)$$
$$B = i_L(t = \Delta t^+) - C - \frac{C_s}{C_L + C_s} I_D$$

Finally, the current through the inductor as a function of time is

$$i_L(t) = \begin{cases} I_D + Ae^{\alpha t}\sin(\omega t) & \text{for } t < \Delta t \\ I_D \frac{C_s}{C_L+C_s} + Be^{(\beta+\gamma)(t-\Delta t)} + Ce^{(\beta-\gamma)(t-\Delta t)} & \text{for } t \geq \Delta t \end{cases} \tag{A.10}$$

Appendix B

Input Impedance Measurement

The analysis of thc "Direct Impedance Measurement" virtual voltage sense technique required the input impedance measurement of several mobile electronic devices. The difficulty in accomplishing this is that the devices have protection circuitry in their input charging paths that keeps the device out of its "charging mode" unless the appropriate conditions are met. The main conditions are that the input voltage on the device is 5V and that the power supply can source the appropriate amount of current. The input impedance of a device is, therefore, different between the state when the device is charging and the state when the device is not charging. In order to see the input impedance of the connected device when it is in its "charging mode" the device must be connected to the impedance analyzer in a manner in which it can draw the appropriate amount of current with the appropriate voltage at its input.

Figure B-1 is the schematic of the circuit used with the impedance analyzer to supply the portable device with the necessary power to charge. The impedance analyzer effectively consists of an AC voltage source in series with a vector ammeter. This branch is then in parallel with a vector voltmeter. The impedance analyzer's measurement signals are injected into the charging circuit through a large injection capacitor.

The charging circuit consists of a power supply in series with a parallel combination of a very large inductor and capacitor. The impedance of these components appears massive to the impedance analyzer compared to the connected device. Therefore,

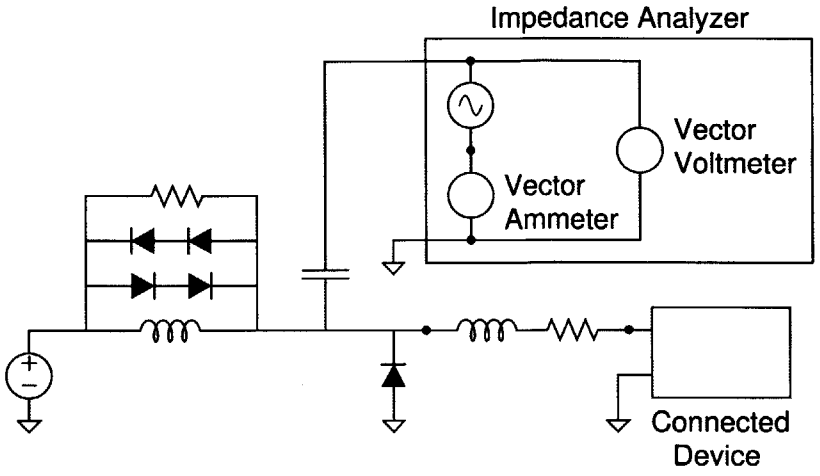

Figure B-1: Impedance analyzer circuit with supply voltage and current.

since the impedance analyzer sees the parallel combination of the connected device and the parallel resistor and inductor, the impedance analyzer effectively only sees the connected device. The diode combinations in parallel with the resistor and inductor suppress voltage spikes over the inductor and protect the connected device and the impedance analyzer. There is also a diode clamp at the signal injection node that further protects the connected device and impedance analyzer from high voltages. The data for figures 2-4 a, b, and c were collected using this circuit configuration.

Appendix C

Sample-and-Hold System Transform

The "Current Interrupt" regulation circuit has the system transfer function,

$$\frac{v_{USB}}{v_{IN}}(s) = \frac{KR_C}{R_i R_C C_C s + R_i + KR_C(1+\epsilon)}$$

This transfer function is a continuous time representation of the system and ignores the effects of the sample-and-hold block on the system. This equation is valid for the situation where the sample-and-hold is operating substantially faster than the time constant of the system. This approximation, however, may not always be valid and a discrete time analysis of the system is necessary to accurately predict the circuit's behavior. This can be accomplished mathematically by taking $z = e^{sT}$, where the sample-and-hold occurs in intervals of duration T.

The sample-and-hold incurs a non-linear transformation on the system. Figure 3-4 shows the system block diagram, and the switch in the negative feedback path represents the sample-and-hold in the circuit. Taking $X(s)$ to be the input of the sample-and-hold, $X^*(s)$ to be the output of the sample-and-hold, and $E(s)$ to be the

system error,

$$E(s) = v_{IN}(s) - X^*(s)$$
$$X(s) = E(s)G(s)(1+\epsilon) = G(s)(1+\epsilon)\left(v_{IN}(s) - X^*(s)\right)$$
$$X^*(s) = (1+\epsilon)\{v_{IN}G\}^*(s) - (1+\epsilon)\{X^*G\}^*(s)$$

Finally taking $z = e^{sT}$,

$$X(z) = (1+\epsilon)\{v_{IN}G\}(z) - (1+\epsilon)\{XG\}(z)$$

where $\{v_{IN}G\}(z)$ is the sampled-and-held transfer function of the signal $v_{IN}(t)$ convolved with $G(s)$, and $\{XG\}(z)$ is the sampled-and-held transfer function of the signal output from the negative feedback path convolved with the transfer function $G(s)$. $X(z)$ is already sampled-and-held and therefore can be moved outside the sample-and-hold transform. $v_{IN}(t)$ can be taken to be a constant function in which case the sample-and-hold transformed input signal always takes the same values as the continuous input signal. This implies that $v_{IN}(s) = v_{IN}(z)$, and so $v_{IN}(s)$ can also be pulled outside of the sample-and-hold transform. These two findings show that both inputs to the system error are sampled-and-held functions, therefore the error is a sampled-and-held function. Likewise, because the output of the negative feedback path is sampled-and-held, and the only other system block in the feedback path is a constant gain block, the input to the feedback path can be viewed as a sampled-and-held function. Finally, the compensation block, $G(s)$, can be viewed as surrounded by sample-and-hold blocks and so the system transfer function can be constructed of

individual transfer functions that undergo the sample-and-hold transform.

$$X(z) = (1+\epsilon)v_{IN}(z)G(z) - (1+\epsilon)X(z)G(z)$$
$$X(z) = \frac{(1+\epsilon)v_{IN}(z)G(z)}{1+(1+\epsilon)G(z)}$$
$$E(z) = v_{IN}(z) - X(z) = \frac{1}{1+(1+\epsilon)G(z)}v_{IN}(z)$$
$$v_{USB}(z) = E(z)G(z)$$
$$\frac{v_{USB}}{v_{IN}}(z) = \frac{G(z)}{1+(1+\epsilon)G(z)}$$

The next step is to evaluate the sample-and-hold transformation of the compensation block, $G(z)$. Note that $\mathcal{L}^{-1}\{\cdot\}$ corresponds to the inverse Laplace transform of the argument and $Z\{\cdot\}$ corresponds to the z transform of the argument.

$$G(z) = \left(\frac{z-1}{z}\right) Z\left\{\frac{G(s)}{s}\right\}$$
$$\tilde{g}(t) = \mathcal{L}^{-1}\left\{\frac{G(s)}{s}\right\} = \mathcal{L}^{-1}\left\{\frac{R_C K/R_i}{s(R_C C_C s+1)}\right\} = \frac{R_C K}{R_i}\left(1-e^{-t/(R_C C_C)}\right)u(t)$$
$$\tilde{g}(nT) = \frac{R_C K}{R_i}\left(1-e^{-nT/(R_C C_C)}\right)u(nT)$$
$$G(z) = \left(\frac{z-1}{z}\right) Z\{\tilde{g}(nT)\} = \frac{R_C K}{R_i}\left(\frac{1-e^{-T/(R_C C_C)}}{z-e^{-T/(R_C C_C)}}\right)$$

The discrete time system transfer function can then be constructed.

$$\frac{v_{USB}}{v_{IN}}(z) = \frac{(R_c/R_i)K(1-e^{-T/(R_c C_c)})}{z-e^{-T/(R_c C_c)}(1+(R_c/R_i)K(1+\epsilon))+(R_c/R_i)K(1+\epsilon)}$$

The location of the pole in the denominator can become less than -1 if the frequency is too slow, in which case the system becomes unstable. This occurs when

$$\frac{1}{R_C C_C \ln\left(\frac{R_C K(1+\epsilon)+R_i}{R_C K(1+\epsilon)-R_i}\right)} < f \tag{C.1}$$

(C.1) can be further simplified assuming $R_C \gg R_i$.

$$\ln\left(\frac{R_C K(1+\epsilon)+R_i}{R_C K(1+\epsilon)-R_i}\right) = \ln\left(1+\frac{2R_i}{R_C K(1+\epsilon)-R_i}\right) \approx \ln\left(1+\frac{2R_i}{R_C K(1+\epsilon)}\right)$$

Using the approximation that when $x \approx 0$, $\ln(1+x) \approx x$, and that $1+\epsilon \approx 1$,

$$\ln\left(\frac{R_C K(1+\epsilon)+R_i}{R_C K(1+\epsilon)-R_i}\right) \approx \frac{2R_i}{R_C K}$$

$$\frac{K}{2R_i C_C} < f$$

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