Building Blocks of a 250MHz bandwidth, 10-bit Continuous-time Delta-Sigma Analog to Digital Converter

by

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B.S., Massachusetts Institute of Technology (2013)

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

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Abstract

This thesis examines the design of a continuous time Delta-Sigma Analog to Digital Converter with the target performance to be 10-bit, 250MHz bandwidth with 200mW power dissipation.The design process involves choosing a top-level architecture and designing transistor-level blocks. The architecture is selected to be second-order, 3-bit with a 32 oversampling rate based on the ideal model simulation in MATLAB. The transistor-level circuits are designed in a BiCMOS technology. The SQNR result is 63.3dB and the power is 140mW.

Thesis Supervisor: Charles G. Sodini
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Chapter 1

Introduction

The analog to digital converter(ADC) is the bridge between the digital world and the world we live in. It allows us to send real life data such as sound, light and temperature to powerful computers to process. It has a wide application in many fields from music to military. The application of the ADC proposed in this thesis is in a point to point(P2P) wireless system.

Since the first commercial ADC was born on 1953 [1], many explorations have been conducted to improve the performance. At present, ADC has four primary architectures — Flash, Delta-Sigma, SAR and Pipeline. In this design, I choose the Continuous-time Delta-Sigma (CTDS) ADC to accomplish the design goal of 10-bit, 250MHz Bandwidth(BW) and 200mW power consumption. To design a Delta-Sigma ADC, it requires determining a top-level architecture and designing transistor-level circuits. In order to determine the top-level architecture, simulations have been done in MATLAB. The transistor-level circuits are designed in a BiCMOS technology, which possibly allows a higher speed design in comparison with a CMOS technology with similar minimum feature sizes.

Chapter two focus on the principle of a Delta-Sigma (DS) ADC.

Chapter three describes potential architectures and the reason behind the choice.

Chapter four describes the design of transistor-level circuits of different blocks in this DS ADC.

Chapter five emphasizes on signal analysis.

Chapter six concludes the thesis.

1.1 Motivation

As wireless carriers move towards 4G mobile technology, significant demands are placed on their infrastructure. This multiple, high-bandwidth and high-speed services of 4G require an infrastructure that is scalable and resisent as well as cost-effective. Creating and maintaining high-performance physical links between communication nodes is one of the most important problems for wireless communication networks[2]. Point to point microwave systems are a common solution to serve as high-bandwidth pipes between two nodes. Therefore, the quality of the P2P microwave systems significantly influences the level of services wireless carriers can provide.

In order to improve the quality of P2P microwave systems, a boost in the performance of the ADC such as wider bandwidth and higher signal to noise ratio (SNR) is necessary. Delta-Sigma ADCs can be a good choice for data conversion in communication applications. Delta-Sigma ADCs have high resolution and moderate bandwidth to achieve high information carrying capacity.[3] Moreover, Delta-Sigma ADCs can ease the design of the baseband antialiasing filters[4].

The effective number of bits (ENOBs) and bandwidth of a Delta-Sigma ADC strongly depends on the comparator (quantizer) and the feedback DAC. A detailed investigation into these two blocks will help determine the performance that can be achieved.

Regarding the process, SiGe BiCMOS has a potential advantage over a similar minimum feature CMOS process for P2P microwave system. An ADC in SiGe process can be fully integrated with the radios in the system, creating an integrated solution.

1.2 Background of point to point wireless system

Point-to-point microwave systems serve as pipes between two nodes in a communication network. The frequency of P2P microwave systems ranges from 6GHz to 80GHz. One advantage of high carrier frequencies is that the microwave band has a very wide available bandwidth. Another advantage of the high carrier frequencies is that the small wavelength allows conveniently-sized antennas.

The wide modulation bandwidth of a typical P2P microwave system implies that we need a high data rate, which is propotional to the product of the bits per sample and the bandwidth. There are two ways to achieve a high data rate. The first way is to use simple modulation scheme and a high modulation bandwidth. The left picture of Figure 1-1 is an example of simple modulation scheme. Simple modulation scheme means low number of bits per sample; therefore, the signal to noise ratio does not need to be high. Comparing to a complex modulation scheme in the right of Figure 1-1, the simple modulation scheme is more tolerable of error because the modulation keys are further away from each other. However, in the complex modulation scheme, the modulation keys are closer to each other, leading to a higher requirement for signal to noise ratio. However, in order to achieve the same data rate as utilizing a simple modulaton scheme, a complex modulation scheme only requires a smaller bandwidth because each sample has more bits.

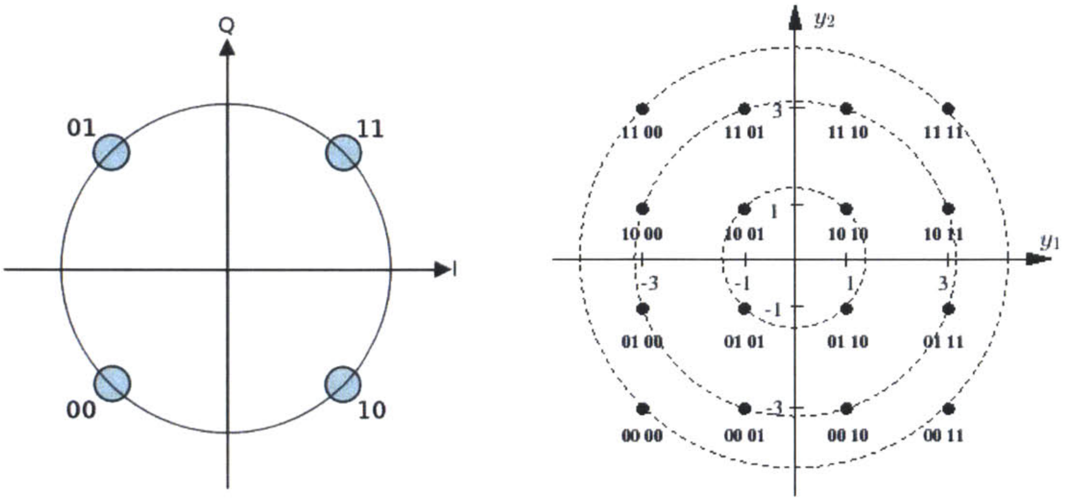


Figure 1-1: A simple and a complex modulation scheme

1.2.1 Target specification

These two methods to achieve high data rate imply we need a wideband/moderate resolution converter or a moderate bandwidth/ high resolution converter. The target specification for the ADCs of a P2P system is 10-bit, 250 MHz and 200mW power consumption. The bandwidth/resolution specifications come from a system analysis of a point to point system. The power specification is chosen based on the performance of the since of the art of ADCs.

Figure 1-2 is a comparison between the performance of previous Delta-Sigma ADCs with our specification. The previous work [4] is not only in SiGe process, but also in other technologies such as InP HBT Technology. The Figure of Merit (FOM) used here is $\frac{P}{2^{(2\cdot ENOB.f_s)}} f_{synq}$ is the minimum sampling frequency (twice the bandwidth) and P is power.

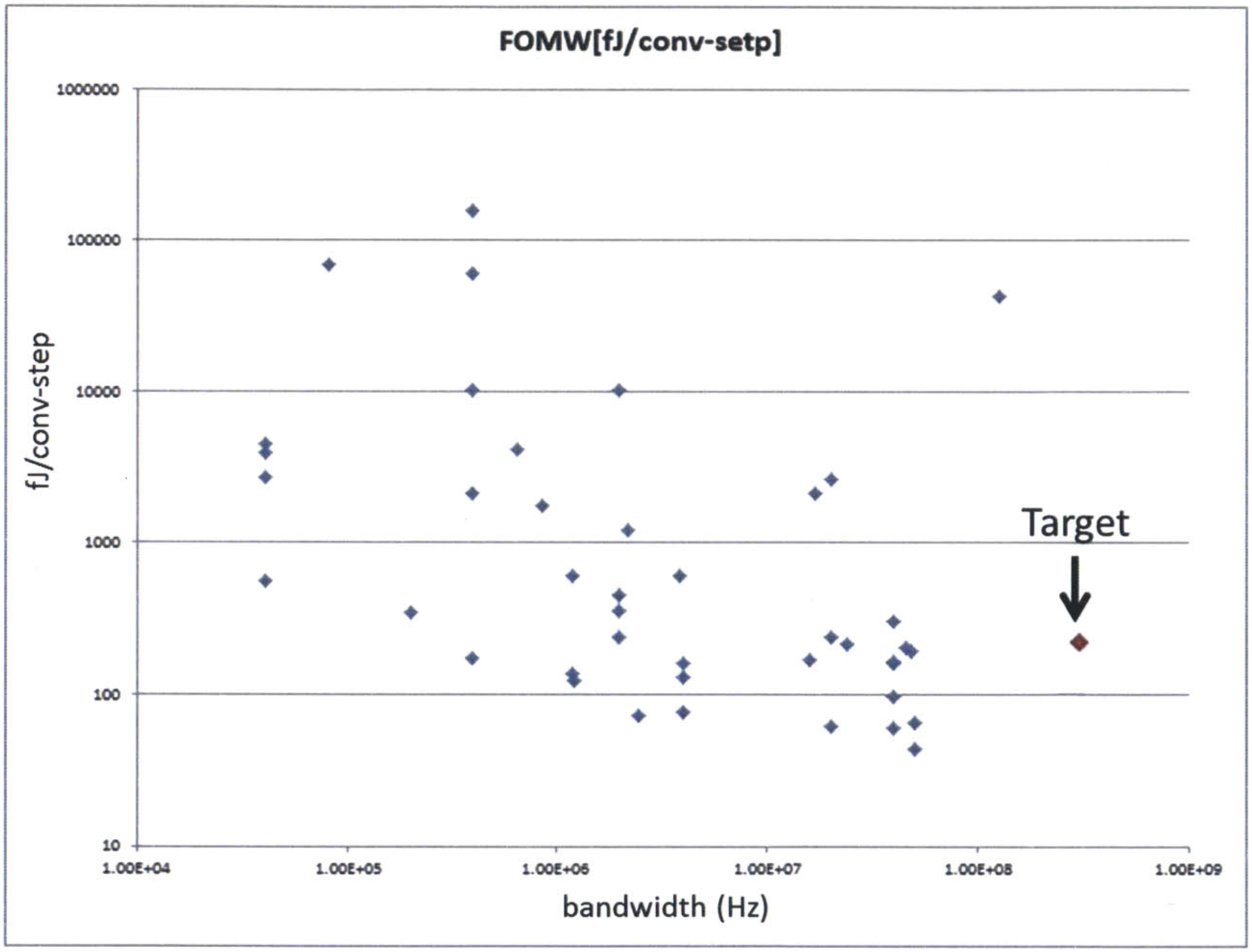


Figure 1-2: DS ADC performance trend

Chapter 2

Principles of Delta-Sigma ADC

2.1 Quantization

Quantization of amplitude is one of the most important ideas of all digital converters. However, quantization introduces distortion to the original signal. To design an ADC, the primary objective is to limit the distortion. Figure 2-1 and Figure 2-2 give an idea of how a basic analog to digital converter system works. The analog input signal comes into the ADC and the ADC gives the digital outputs. The bits are converted into voltages again through a digital to analog converter (DAC).

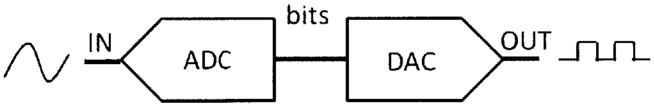


Figure 2-1: Analog to Digital conversion

Figure 2-2 shows the input and output of a 3-bit ideal ADC. The actual outputs are the binary codes along the y-axis. The full scale of the ADC is 2V. For example, if the input is 0V, the actual output is "100". The binary code can be converted back to the analog voltage by a DAC as in Figure 2-1.

As shown in Figure 2-2, the input and the quantized output are very different. The difference is due to distortion introduced in quantization. In order to learn more about quantization, we can represent the quantized signal y by a linear function with a gain G and

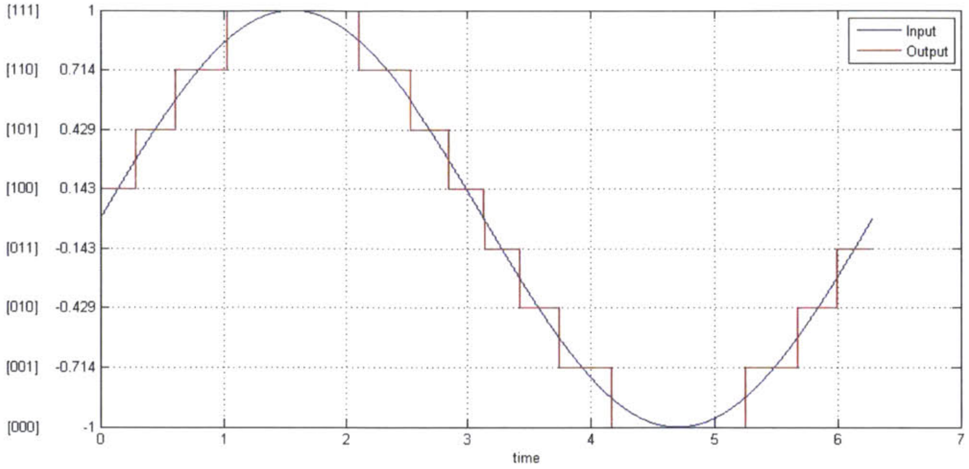


Figure 2-2: input and output of an ADC

an error e:

$$y = Gx + e \tag{2.1}$$

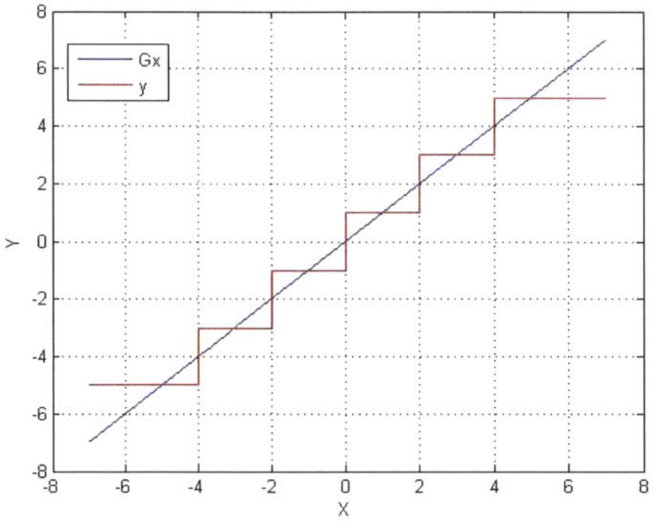
in which G is the slope of the straight line that passes the center of the quantization characteristic. That means when the quantizer does not saturate (i.e. input does not exceed the input range), the error is bounded by $\pm\Delta/2$ where Δ is the level spacing or least significant bit.

Above is an example of input ranging from -6 to +6 and Δ to be 2. The error is completely determined by the input. However, if the input changes randomly within the input range, the error is mostly uncorrelated with the input and the error has a uniform probability distribution in the range of $\pm\Delta/2$. Then the mean square value is

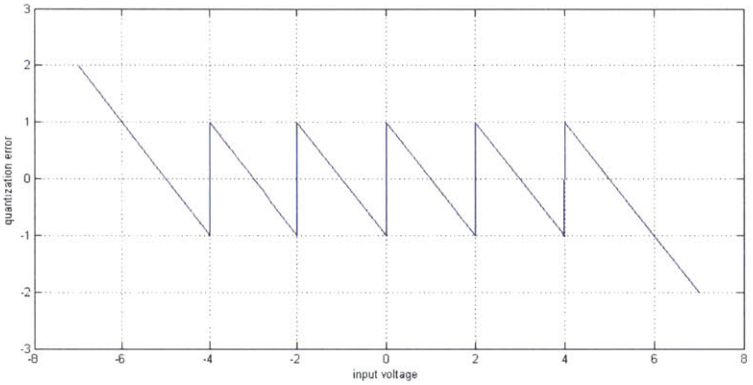
$$e_{rms}^2 = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} e^2 de = \frac{\Delta^2}{12} \tag{2.2}$$

To relate this result to quantization noise spectral density, when a signal is sampled at frequency $f_s = \frac{1}{T}$, T is the time between two samples, all of the quantization noise power lies into the frequency band $0 \le f < f_s/2$. Then the quantization noise density is

$$Q(f) = e_{rms}\sqrt{\frac{2}{f_s}} = \frac{\Delta}{\sqrt{12}}\sqrt{\frac{2}{f_s}} \tag{2.3}$$



(a) $y = Gx + e$



(b) e

Figure 2-3: a quantization characteristic represented by $y = Gx + e$

From (2.2) and (2.3), the bigger the spacing level,which is the least siginificant bit(LSB) is, the bigger in-band quantization noise is. Since in Delta-Sigma modulators, the quantizer usually has very few bits, the quantization noise is the dominant noise source. We rely on feedback and oversampling to reduce the overall quantization noise.[6]

2.2 Oversampling

Oversampling is one way to reduce the noise introduced by quantization. Oversampling can help reduce in-band noise, hence increasing the signal-to-noise ratio (SNR). It takes several samples to represent one data point, so the noise power becomes N times smaller if averaging N samples to represent one data point. The oversampling rate (OSR) is defined to be

$$OSR = \frac{f_s}{2f_0} \tag{2.4}$$

where f_0 is the signal bandwidth. Figure 2-4 shows how it works in frequency domain. Because the total noise power is constant, a higher sampling rate leads to a wider frequency spectrum and reduce the noise power density. fa is the noise bandwidth before oversampling and pa is the noise power density before oversampling. fb and pb are the corresponding noise bandwidth and noise power density after oversampling. Since we only care about the noise within the signal band, the total in band noise becomes smaller after oversampling. The relationship between the noise power density and OSR is

$$n_{oversampled} = \frac{n_{original}}{OSR} \tag{2.5}$$

Each doubling in OSR increase SNR by 3dB.

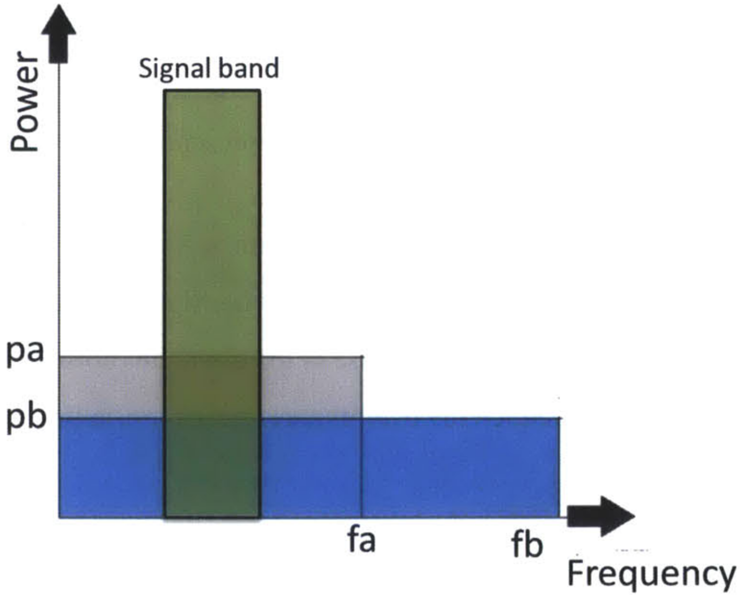


Figure 2-4: Oversampling in frequency domain

2.3 Delta-Sigma Modulation

2.3.1 First order Delta-Sigma ADC

Delta-Sigma modulation allows the use of a coarse quantizer with high quantization noise, while still generating data that has low quantization noise through error feedback and over-sampling. It utilizes error feedback to shape the noise transfer function to minimize in-band noise power, reducing noise introduced by quantization.

Figure 2-5 is the block diagram of a first order Delta-Sigma ADC. Here we assume the quantizer is a multilevel, uniform and has a unity gain $G = 1$ and the integrator is clocked. Then we can model the first order DS ADC to be Figure 2-6.

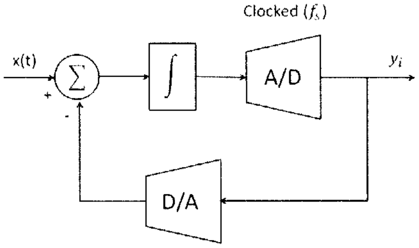


Figure 2-5: First order Delta-Sigma modulator

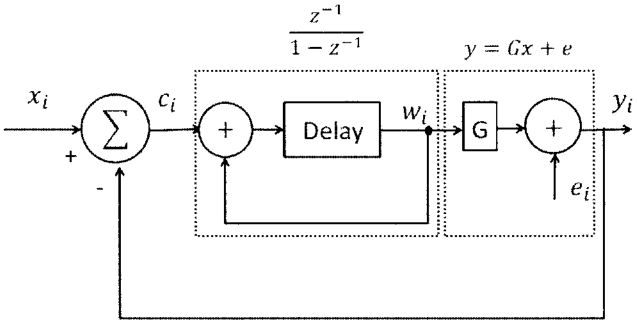


Figure 2-6: First order Delta-Sigma modulator

Since the integrator is clocked, the input will only be sampled at when the integrator is sampled. Therefore, in the new model, $x(t) = x_i$, where i is the clock cycle. As we discussed in the quantization section, the quantizer can be modeled as $y = Gx + e$. Here we assume G equals to 1. Then the A/D, D/A quantizers can be replaced by the sum of output of the integrator (w_i X G) and the error at step i e_i. The integrator can be replaced as a delayed feedback loop, which makes $w_i = w_{i-1} + c_i$. The transfer function of the integrator $H_{int}(Z) = \frac{z^{-1}}{1-z^{-1}}$.Then the modulator output $Y(Z)$ in the frequency domain is given by:

$$Y(Z) = X(Z)z^{-1} + E(Z)(1 - z^{-1}) \tag{2.6}$$

where $E(Z)$ is the error power density function in the frequency domain. From (2.4), the signal transfer function (STF) $H(Z)$ is z^{-1} and the noise transfer function (NTF) N(Z) is $1 - z^{-1} = 1 - e^{-j\omega T}$, where $\omega = 2\pi f$. Recall in (2.3), $Q(f) = e_{rms}\sqrt{\frac{2}{f_s}}$. The noise spectral density in this modulator is:

$$N(f) = Q(f)|1 - e^{-j\omega T}| = Q(f)\sqrt{2 + 2cos(\omega T)} = e_{rms}\sqrt{\frac{2}{f_s}}sin(\frac{\omega T}{2}) \tag{2.7}$$

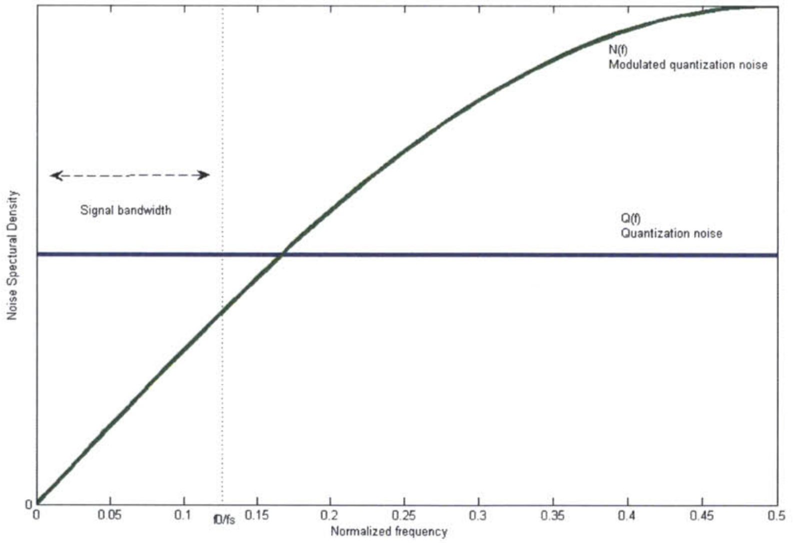


Figure 2-7: The modulated noise density $N(f)$ and the quantization noise $Q(f)$ VS f/f_s

The NTF is shaped due to DS modulation. In this case, Figure 2-7 shows the modulation reduces the noise at low frequencies and increases the noise at high frequencies. However, if we only concern about noise power in the signal bandwidth, in this case we assume the signal bandwidth is from 0 Hz to f_0, the noise power is much lower than that in an unmodulated converter. The in-modulated band noise power is

$$
\begin{aligned}
n_0^2 &= \int_0^{f_0} |N(f)|^2 df \\
&= \int_0^{f_0} \frac{2e_{rms}^2}{f_s} |1 - z^{-1}|^2 df \\
&= \frac{4e_{rms}^2}{f_s} \int_0^{f_0} 2sin(\frac{\pi f}{f_s}) df \\
&\approx \frac{8e_{rms}^2}{f_s} \int_0^{f_0} (\frac{\pi f}{f_s})^2 df \qquad (f_0 \ll f_s) \\
&= \frac{e_{rms}^2 \pi^2}{3} (\frac{1}{OSR})^3
\end{aligned}
\tag{2.8}
$$

The effective number of bits(ENOBs) is defined to be

$$
ENOB = \frac{SNR - 1.76}{6.02} \tag{2.9}
$$

In the first order modulator, each doubling in sampling frequency increases SNR by 9dB,thus, increase the resolution by one and half bit.

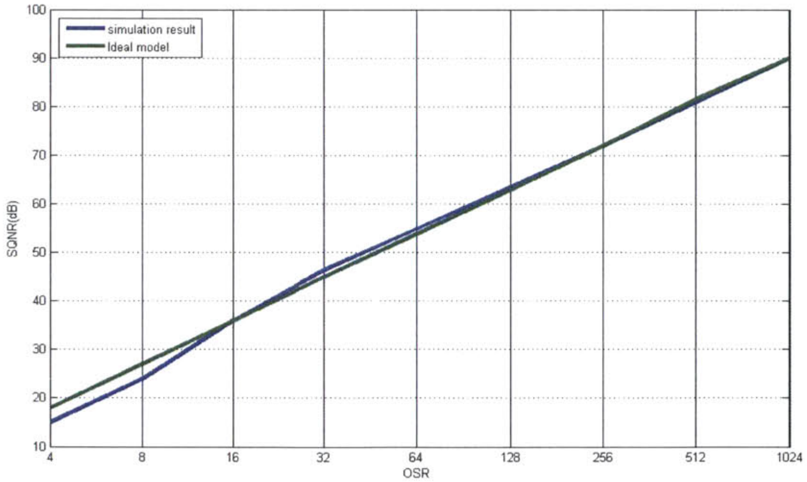


Figure 2-8: Equivalent first order Delta-Sigma modulator

Figure 2-8 is a plot of OSR vs signal to quantization noise ratio (SQNR) for the first order modulator discussed above, assuming the white noise model holds. It is generated by using a MATLAB model in the appendix A. The green line is the ideal 9dB/Octave line.

The blue line is the result plot, which has a slope about 9dB/doubling in f_s, which matches our prediction.

2.4 Higher order Delta-Sigma Modulator

In the last section, we have showed the noise can be shaped by the Delta-Sigma modulation, resulting in a higher ENOBs. The feedback loop via the integrator determines the shape of the noise spectrum. In this section, we will discuss about the effects of more feedback loops via multiple integrators.

2.4.1 Second order DS modulator

Let us first start with a second-order DS modulator. It is basically the first order loop filter added an additional feedback loop and an integrator. The inner feedback loop helps stablizing the loop filter. Without the second feedback loop, W_{1i} and W_{2i} are possible to become bigger than the voltage range, hence, making the system unstable [7].

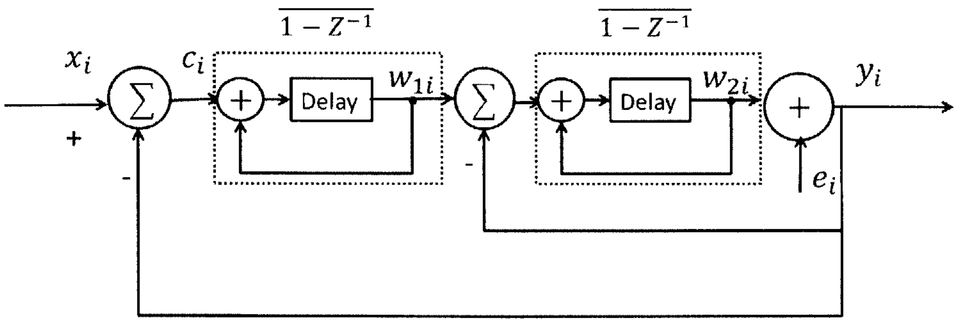


Figure 2-9: Second order Delta-Sigma modulator

The output y_i and the NTF can be found by solve the difference equations:

$$
\begin{aligned}
&y_i = w_{2i} + e_i \\
&w_{2i} = w_{2i-1} + w_{1i} - y_{i-1} = w_{1i} - e_{i-1} \\
&w_{1i} = w_{1i-1} + x_i - y_{i-1} = x_i - e_{i-1} + e_{i-2} \\
&y_i = x_{i-1} + (e_i - 2e_{i-1} + e_{i-2}) \\
&N(f) = Q(f)(1 - z)^2 \\
&|N(f)| = 4Q(f)sin^2(\frac{\omega T}{2})
\end{aligned}
\qquad (2.10)
$$

Similarly, we can calculate the in band noise power if the quantization noise is considered to be white

$$n_0^2 = e_{rms}^2 \frac{\pi^4}{5} OSR^{-5} \qquad (f_0^2 \ll f_s^2) \qquad (2.11)$$

Each doubling of OSR increases 15dB in SNR or two and half bit of resolution.

2.4.2 Higher order DS modulator

What we find in the first order and second order DS ADC can be extended to higher orders. The noise transfer function of a Nth order modulator is $|N(f)| = Q(f)[sin(\frac{\omega T}{2})]^N$ and the in band noise power is

$$n_0^2 = e_{rms}^2 \frac{\pi^{2N}}{2N + 1} OSR^{-(2N+1)} \qquad (f_0^N \ll f_s^N) \qquad (2.12)$$

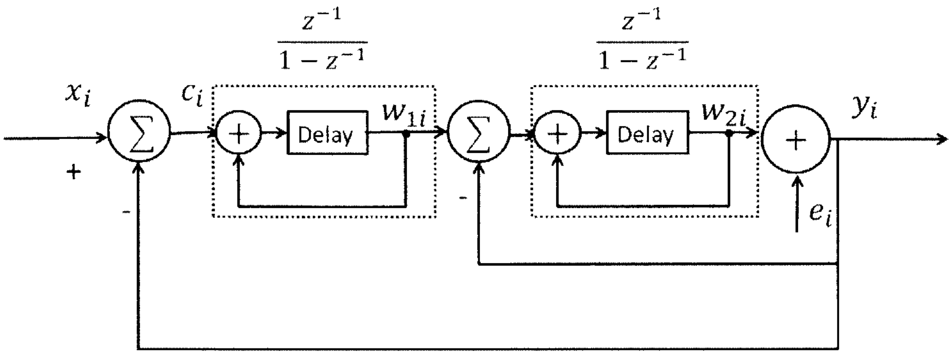


Figure 2-10: Nth order Delta-Sigma modulator

The noise decreases by $3(2N-1)$ dB and the ENOB increases by N and half bits for each doubling of the sampling frequency. Figure 2-11 plots the noise power vs OSR with different orders. Notice at small OSR, the noise power does not make sense because our assumption is $f_0 \ll f_s$.

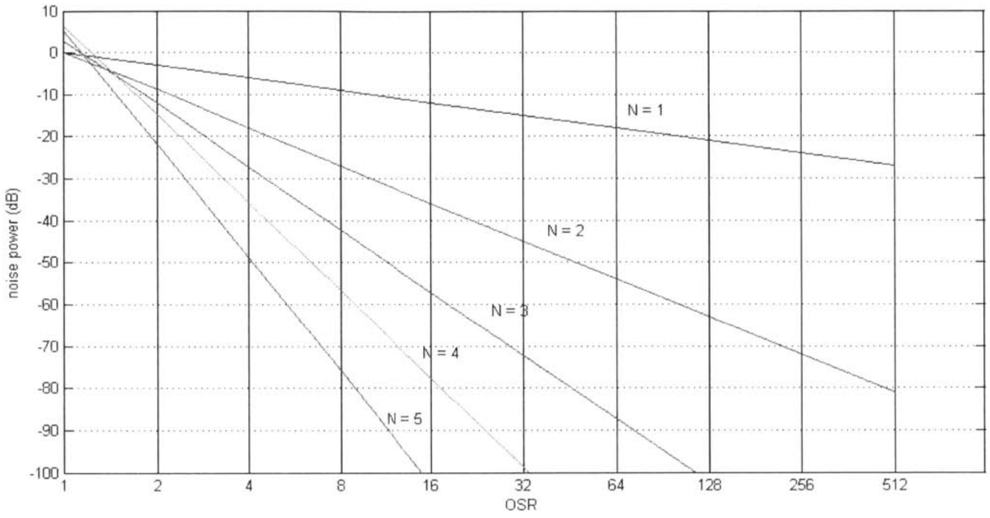


Figure 2-11: Noise power vs OSR vs order

2.4.3 Stability

Stability is another important concept in Delta-Sigma modulators. Because there are multiple feedback loops, the system has a chance to be unstable. For the one-bit modulator of a general model introduced previously, the system is conditionally stable if the order is higher than two. As a result, only signals below a certain maximum input level can be converted without causing the modulator to become unstable. This level for which the modulator becomes unstable is a function of the loop-filter order and loop-filter cutoff frequency [8]. Higher order Sigma-Delta Modulators are conditionally stable.

2.5 Continuous time Delta-Sigma Modulator

A continuous-time DS ADC is similar to a discrete-time DS ADC, except the sampling occurs after the loop filter. Figure 2-12 is the model of a continuous-time (CT) modulator.

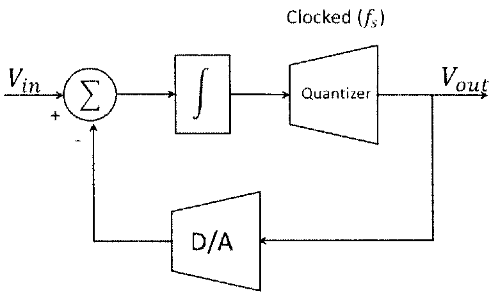

Clocked (f_s)
V_{in}
Σ
+
-
$\int$
Quantizer
V_{out}
D/A

Figure 2-12: First-order continuous-time modulator

Assume the clock is 1Hz,$v_c = \pm 1$, y(n) to be y_c at the nth clock cycle. Then

$$y(n) = y(n-1) + \int_{n-1}^{n} (u_c(\tau) - v_c(\tau))d\tau = y(n-1) + u(n) + v(n-1) \tag{2.13}$$

where $u(n) = \int_{n-1}^{n} u_c(\tau)d\tau$ and $v(n) = Q(y(n))$, Q is the quantization from the A/D. Recall the model of A/D introduced earlier, we can write (2.13) to be

$$\begin{aligned} y(n) &= E(n-1) + u(n) \\ y(n) + E(n) &= E(n) - E(n-1) + u(n) = v(n) \\ V(Z) &= U(Z) + E(1 - z^{-1}) \end{aligned} \tag{2.14}$$

Because $u(n) = \int_{n-1}^{n} u_c(\tau)d\tau$, a CT modulator is equivalent to a DT modulator by adding a pre-filter. The transfer function of the pre-filter $g_{pc} = \frac{1-e^{-s}}{s} = \frac{1-z^{-1}}{s}$.

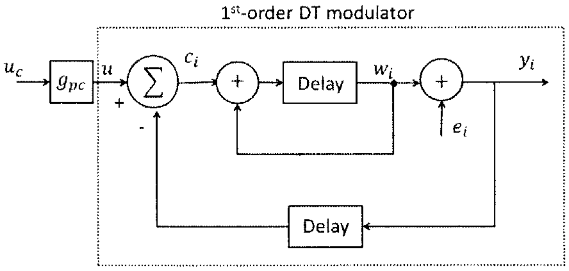

1st-order DT modulator
u_c
g_{pc}
u
+
-
Σ
c_i
+
Delay
w_i
+
y_i
e_i
Delay

Figure 2-13: Equivalent first-order continuous-time modulator

Seen from the previous example, CT DS modulators can be considered as DT DS modulators with a pre-filter. One can also adjust the coefficients of a CT DS modulator to achieve the same NTF as a DT DS modulator. Therefore, the principles of DT DS modulators could also be applied to CT DS modulators [9].

Chapter 3

Architecture selection

3.1 Choose DS ADC order, bit and OSR

As discussed in Chapter 2, the quantization noise is the major resource of noise in a DS ADC. Furtunately, through noise shaping, multi-level quantizers and oversampling, the quantization noise can be significantly reduced. An increase in quantizer level could increase the SNR linearly. An increase in order could increase the slope of SNR and OSR relationship.

Our design goal is 10-bit, 250MHz and 200mW. In order to decide what order, quantizer levels and OSR could lead to our design goal, the plots of OSR VS SNR vs bits are generated based on Richard Schreier's toolbox [10].

The target SINAD is 61.96dB. The target SQNR needs to be a little higher than SINAD because there are thermal noise and harmonic distortion. The bandwidth is 250MHz, corresponding to sampling frequency to be 250MHz·OSR. An OSR of 64 requires a sampling frequency to be 32GHz, which is not possible to achieve with this 130nm BiCMOS technology within the 200mW power budget. A good choice of OSR is 32 or 16. If the OSR is too small, the order of the modulator needs to increase, leading to more components, hence a higher power consumption.

3.1.1 One-bit modulation OSR VS SQNR

Figure 3-1 is a plot of one-bit modulation OSR VS SQNR. At OSR of 32, only third or fourth order can meet the design target, however for one-bit modulation, an order higher than two is not absolute stable with a full scale input. At higher OSR, the requirement for sampling frequency is not feasible. Although one-bit modulation is the ideal choice because of linearity, in this design, we cannot use a one-bit modulation due to power and input range.

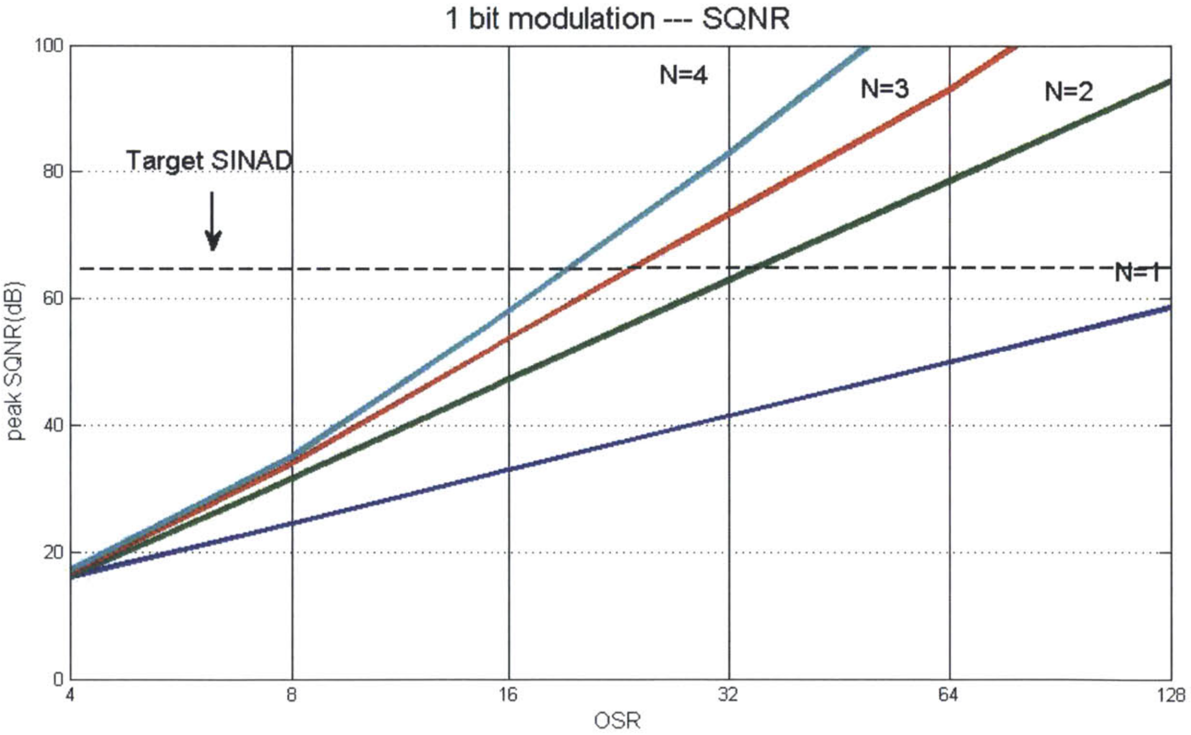


Figure 3-1: OSR VS SNR with 1-bit modulation

3.1.2 Two-bit modulation OSR VS SQNR

At OSR of 32, a second order architecture with 2 bit quantizer can give a peak SQNR to be 70dB. It is a possible architecture choice. A third order with OSR of 16 gives a peak SQNR to be 72dB. It is also a possible choice. The margin of these two possible options for non-ideality of circuits, thermal noises and harmonic distortion is around 10dB.

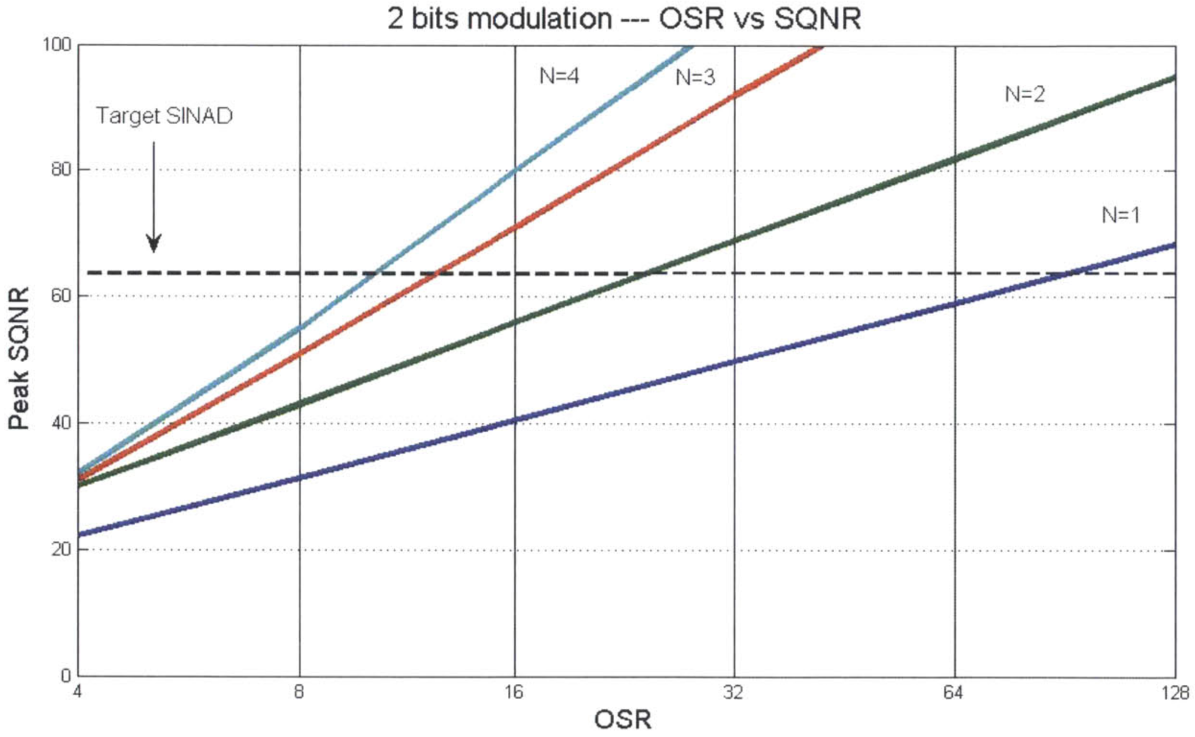


Figure 3-2: OSR VS SNR with 2-bit modulation

3.1.3 Three-bit modulation OSR VS SQNR

At OSR of 32, at second order architecture can give a peak SQNR to be 80dB. It is another possible architecture choice. The design margin for this choice is 18dB. We can go to higher order if we end up with lower SQNR. Notice at higher OSR, the slope of peak SQNR increases because the quantization noise is approaching the white noise model.

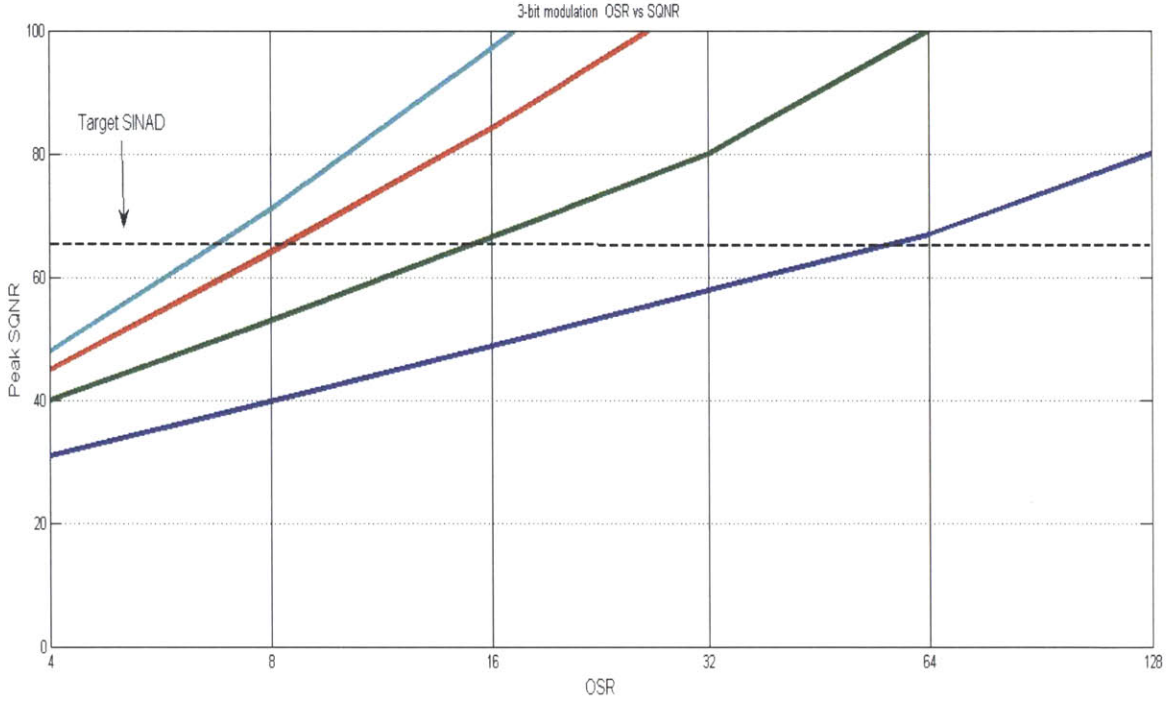


Figure 3-3: OSR VS SNR with 3-bit modulation

3.2 Top-level behavioral model

In this thesis, I chose the architecture to be second order and 9-level quantizer with OSR of 32. The predicted SQNR is 80dB, leaving a margin of 18dB for non-ideality of the design.

Figure 3-4 is a general behavioral model for this CTDS ADC. Notice Vin, V1, V2 and V_{VDAC} are differential voltages. This model includes one quantizer, two current DACs (IDACs) , two OP-amps, one voltage DAC(VDAC), one latch, six pairs of conductance, two pairs of capacitances and one summing block. The latch, quantizer, VDAC, IDACs, OP-amps and summing block are fully differential. The full scale for the quantizer and VDAC is 1V.

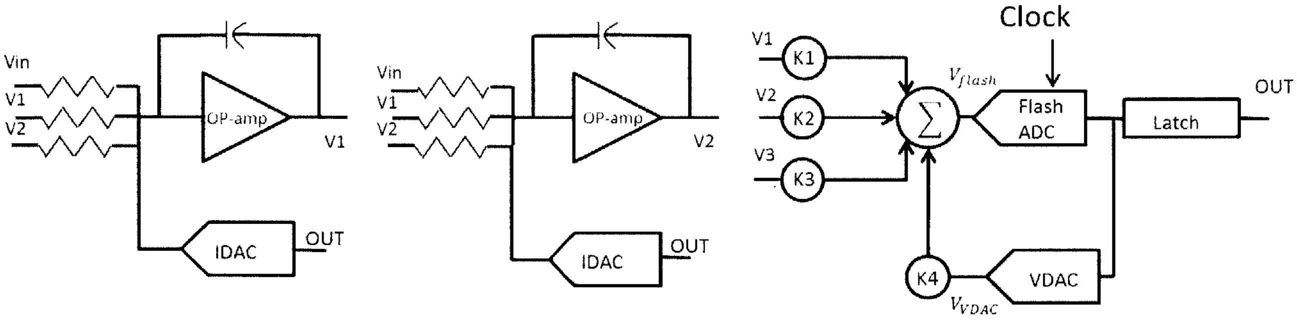


Figure 3-4: Top level behavioral model

The resistances convert voltages of vin, V1 and V2 to currents, summed with IDAC outputs at the inputs of OP-amp. Together with the summed currents and the caps, the OP-amps work as integrators, converts the currents into summed voltages:

$$V_{t_2} = \int_{t_1}^{t_2} \frac{I_{in}}{C} dt + V_{t_1} \tag{3.1}$$

V_{t_2} is the output voltage (V1 or V2) of the OP-amp at time t_2.

The summing block before the quantizer generates the inputs to the quantizer. The input of the quantizer is

$$V_{flash} = K_1 \cdot V_{in} + K_2 \cdot V_1 + K_3 \cdot V_2 + K_4 \cdot V_{VDAC} \tag{3.2}$$

The outputs of the latches go to the feedback IDACs to shape the noise transfer function. The latches at the outputs of the quantizer are necessary. The reason is the outputs of the quantizer are analog and may change at any moment while the inputs to the IDACs should be stable at each clock cycle. Notice the latch causes one step delay in the feedback loop due to latched output. The direct feedback VDAC is to correct the one step delay when the ADC initializes to remain stable and one of the factors determine the NTF.

The values of the conductance, capacitances, least significant bit(LSB) current and voltage, and coefficients such as K_1 and K_2 are determined by Richard Scherier's MATLAB toolbox to achieve optimized NTF. The values of components used in this design is in the appendix B.

3.2.1 Ideal simulation result

Figure 3-5 is the ideal FFT plot of the 2nd order 9-level Delta-Sigma ADC as described in the previous part of this chapter. The NTF is optimized to minimize the in-band quantization noise. A Hanning square window is applied. The center signal frequency for this simulation is about 9MHz. The SQNR is 78.4dB.

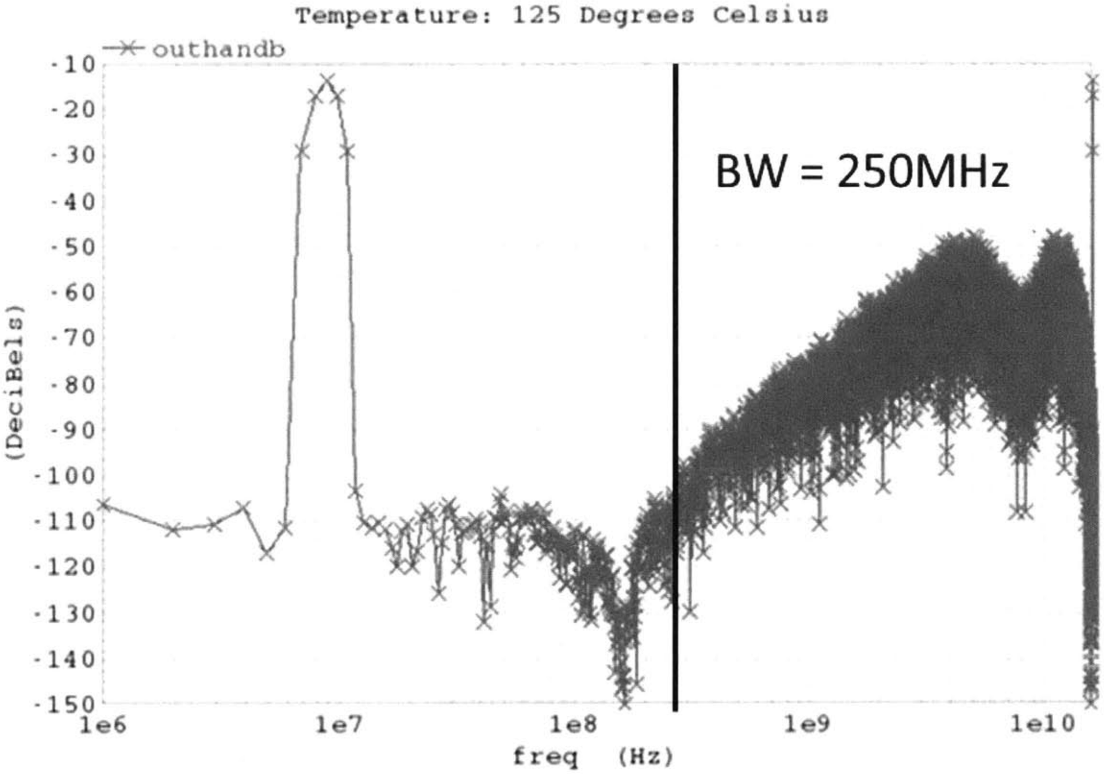


Figure 3-5: Top level behavioral model

Chapter 4

Transistor circuit design

4.1 Device characteristics

The technology used in this thesis is a BiCMOS SiGe 0.13u process. In general, SiGe transistor has advantages of a large intrinsic gain and requiring a small input swing over MOSFETs. In high speed circuit design as in this ADC, bipolar devices are widely used as input and output stages to pursue higher operation speed.

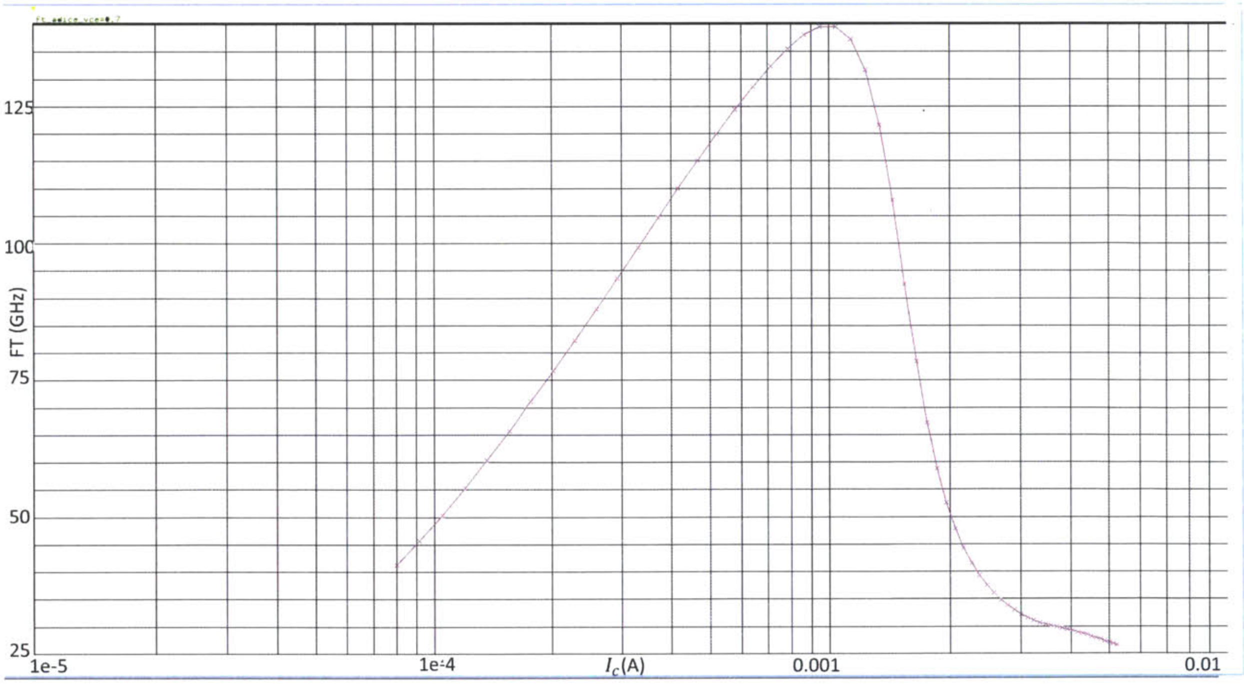


Figure 4-1: FT vs I_c of npn with minimum length and width

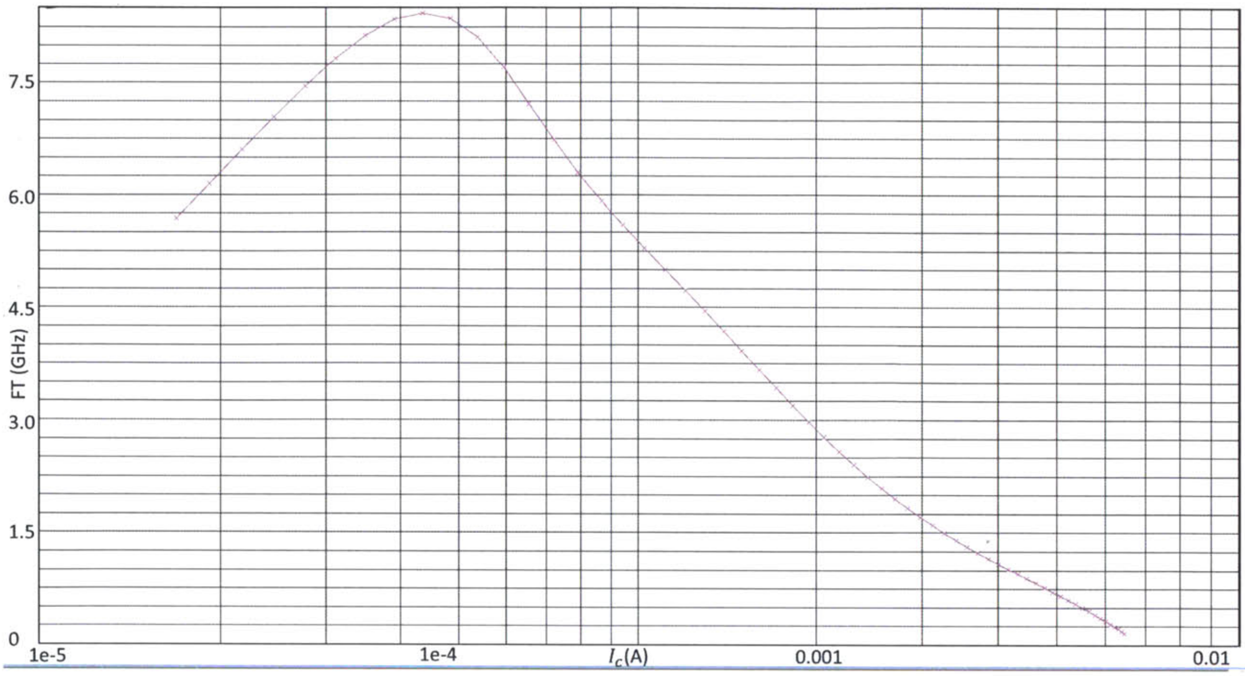


Figure 4-2: FT vs I_c of pnp with minimum length and width

The V_{ce} of the plots is set to 0.7V, which matches the situation of using most of the headroom. To use all the headroom, the maximum V_{ce} is $V_{be} + 0.2V$ to avoid BC junction to be forward biased. V_{be} is about 0.7V. Figure 4-1 and 4-2 are FT vs I_c plots of npn and pnps. npn has a very high peak FT while the pnp has a FT about 1GHz, where npn FT peaks at $I_c = 100uA$. That means in high speed components design, we will use npns with resistive loads.

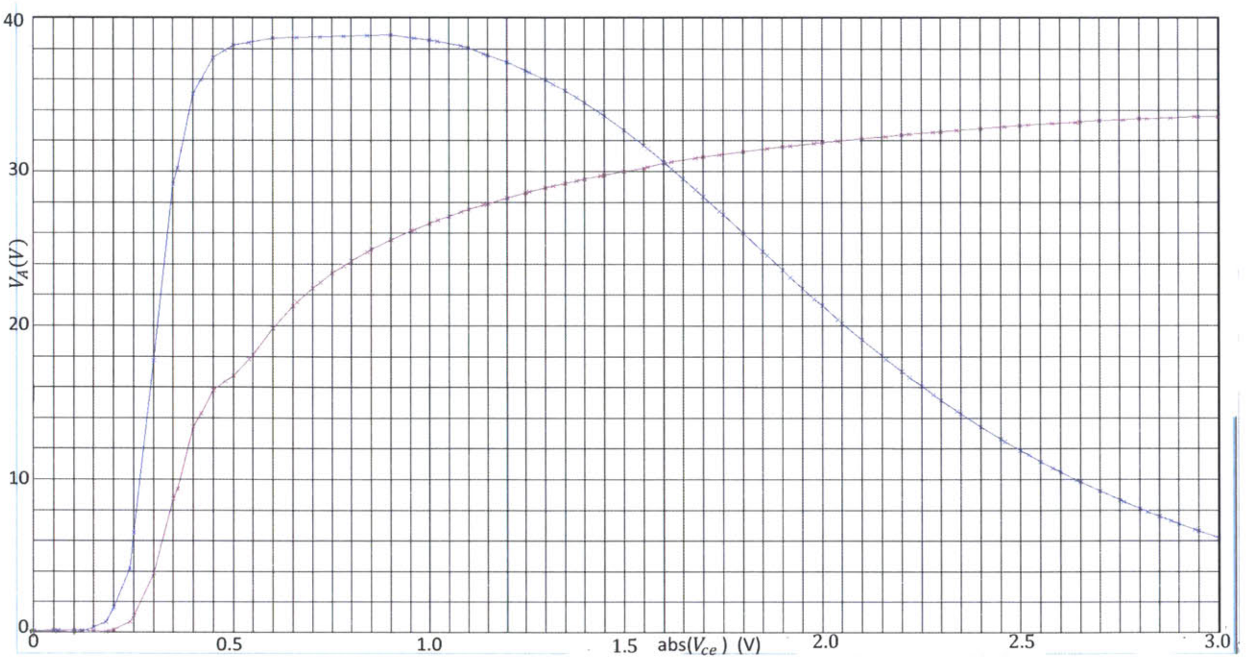


Figure 4-3: Early voltage vs V_{ce} of bipolars

This plot is the early voltage vs I_c of the bipolar.The pink line is the plot of pnp and the blue line is the plot of npn. At V_{ce} to be 0.7V similar to the condition in the design, both npn and pnp have a very high early voltage at the desired I_c density region, leading to a high output resistance. Notice the early voltage of npn reaches the peak very quick as V_{ce} increases. npn also becomes saturated very quick as V_{ce} increases. In comparison, early voltage of pnp increases slowly as V_{ce} increases. We know early voltage is inversely propotional to junction capacitance C_{BC} and $C_{BC} = C_{BC0}/\sqrt{1 - V_{BC}/\phi_{BC}}$. C_{BC0} and ϕ_{BC} are two constants. In this process, ϕ_{BC} of pnp is much bigger than ϕ_{BC} of npn. Therefore, as V_{CE} increases, V_{BC} increases the same rate in both pnp and npn, but C_{BC} of pnp decreases much slower than C_{BC} of npn does, resulting in early voltage of pnp increases much slower than early voltage of npn does.

4.2 Comparator and Flash ADC design

A comparator is a device comparing an input voltage and a threshold voltage to output a high voltage or a low voltage indicating which is larger. There are two primary methods to make a comparator.

One way is to use an uncompensated OP-amp with a large gain. The advantage of this method is that these is little hysteresis. However, in this specific design, it is hard to implement a comparator using an OP-amp. It is because a large gain requires high power consumption; however a limited gain may cause metastability because output voltages might not reach the threshold voltage level.

The other method is to use positive feedback. The advantage of positive feedback is that it can be considered to have an infinite gain with relatively low power. The gain is an exponential function of time. Therefore, the chance of metastability is approaching zero if giving enough time. However, in the real design, we cannot wait infinite long time for a comparator to give a output, hence the time constraint is very important in implementing comparators with positive feedback. Still the choice of positive feedback is more preferable in high speed comparator design. The disadvantages of positive feedback are that it has a hysteresis, leading to wrong decisions and possible more complicated design. However, the hysteresis is possible to be eliminated by resetting each clock cycle.

In this design, the positive feedback method is preferred because of power consumption and noise shaping property of Delta-Sigma modulation. Similar to quantization noise, the hysterisis of a comparator can be modeled as another noise source adding to the output of an ideal gain block. The noise source is shaped through the loop filter, similar to quantization noise.

4.2.1 Comparator design

Since the sampling frequency is $BW \cdot OSR = 250\text{MHz} \cdot 32 = 16\text{GHz}$, it is wise to use bipolar as input and output stages. CMOS input stages require about a full swing to be fully switched comparing to about 200mV of BJT input stages. A small swing can increase the circuit speed by saving the time to go to desired voltage levels. Therefore, the npns are chosen to be input and output stages. For current sources, CMOS are used because in this technology, CMOS has a better matching than bipolar, increasing robustness of the design.

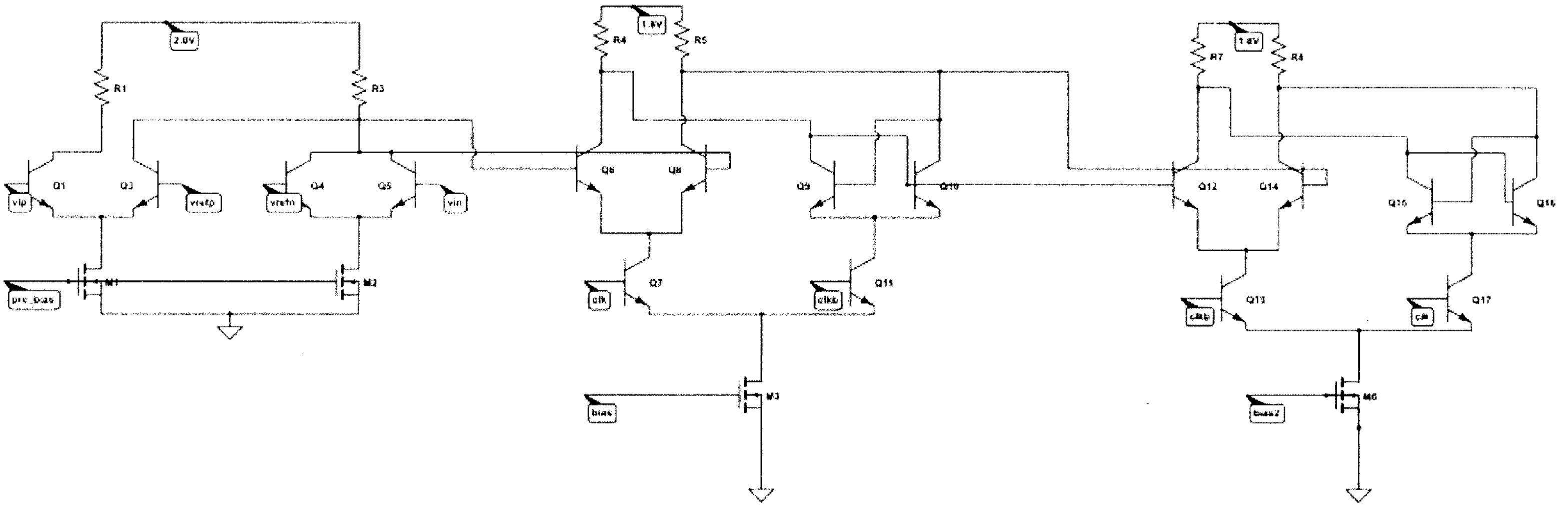

2.0V
R1
R3
Q1
Q3
Q4
Q5
vip
vrefp
vrefn
vin
pre_bias
M1
M2
1.8V
R4
R5
Q6
Q8
Q7
clk
bias
M3
Q9
Q10
Q11
clkb
1.8V
R7
R8
Q12
Q14
Q15
Q16
Q13
clkb
Q17
clk
bias2
M6

Figure 4-4: schematic of comparator

Figure 4-4 is the actual design implemented in the CTDS ADC. I will breakdown the schematic in this section. The comparator structure is fully differential and consists of preamplifier, Track/Hold(T/H) comparator core and another T/H as latch[11].

Power is the limiting factor because there are eight comparators in the Flash ADC. The flash ADC consumes power at least as much as power of eight comparators. In order to minimize power consumption, a common 1.8V voltage supply is used as VDD.

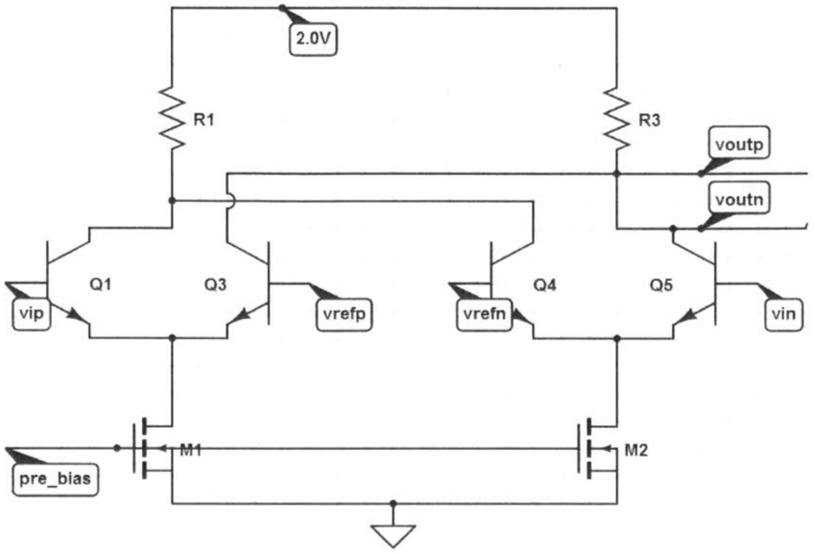


Figure 4-5: schematic of the pre-amplifier

The first stage is a low gain differential difference amplifier with resistive loads. The reason not to use active loads to achieve a higher gain is pnp in this technology has a very low FT, which means pnp will present a lot of capacitance.

The major concerns of the pre-amp design are power consumption, gain and bandwidth. Non-linearity and input offset can be shaped through the loop filter similar to quantization noise by modeling as extra noise sources adding to an ideal gain block. Therefore they are not the biggest focus in this design.

Unlike the other parts of the comparator, the VDD of the pre-amp is chosen to be 2V because of headroom. Since it is a Flash ADC, the reference voltages vary from common mode voltage(V_{cm}) to $V_{cm}\pm$ 4·LSB. At the extreme case when vref is $V_{cm}\pm$ 4·LSB, if the VDD is 1.8V, V_{bc} is possibly bigger than 200mV, causing BC junction to be forward biased. This will sink currents from the previous stage, leading to malfunction in the system. A 2V VDD is carefully chosen to avoid such undesired circumstances and minimize power. Although it is possible to use CMOS as input stages operating at 16GHz while keeping VDD to be 1.8V, the intrinsic gain of CMOS is a decade smaller than BJT's with same amount of biasing current. A tradeoff is made to increase the gain by a factor of 10 with little power and more complicated voltage sources.

In the pre-amp, the differnce of the differential inputs is compared to the difference of the reference voltages. The differential output is

$$V_{outp} - V_{outn} = g_m R_{out}[(V_{ip} - V_{in}) - (V_{refp} - V_{refn})] \tag{4.1}$$

g_m is the conductance of the npns and R_{out} is the effective resistance looking at the output of the BJT input stages, which is $R_{load}//r_o$. r_o is the effective output resistance of the BJT.

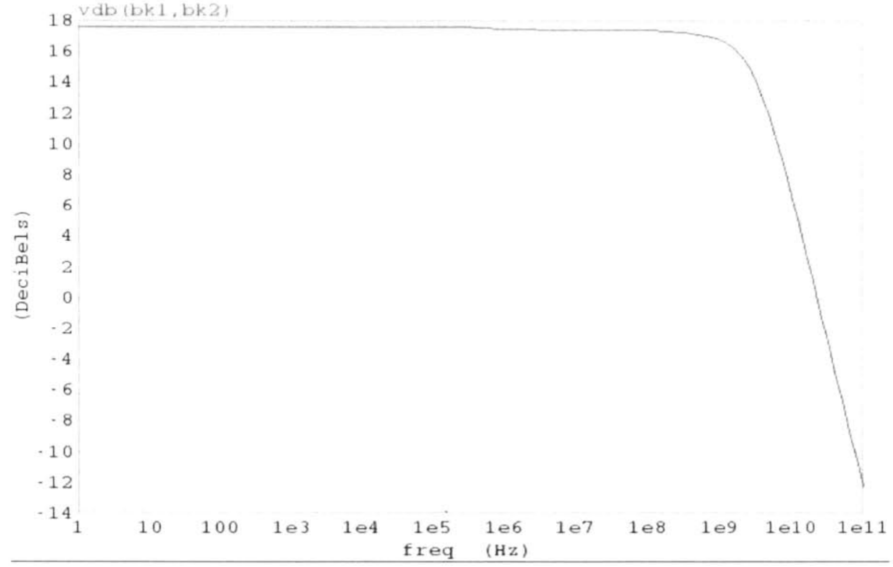


Figure 4-6: frequency response of the pre-amplifier

Figure 4-6 is the frequency response of the pre-amp. Choosing the current for each branch to ne 500uA and 400 ohms as loads, the DC gain is 18dB and the bandwidth is bigger than 1GHz, four times of the target bandwidth. The power for the pre-amp is 2mW.

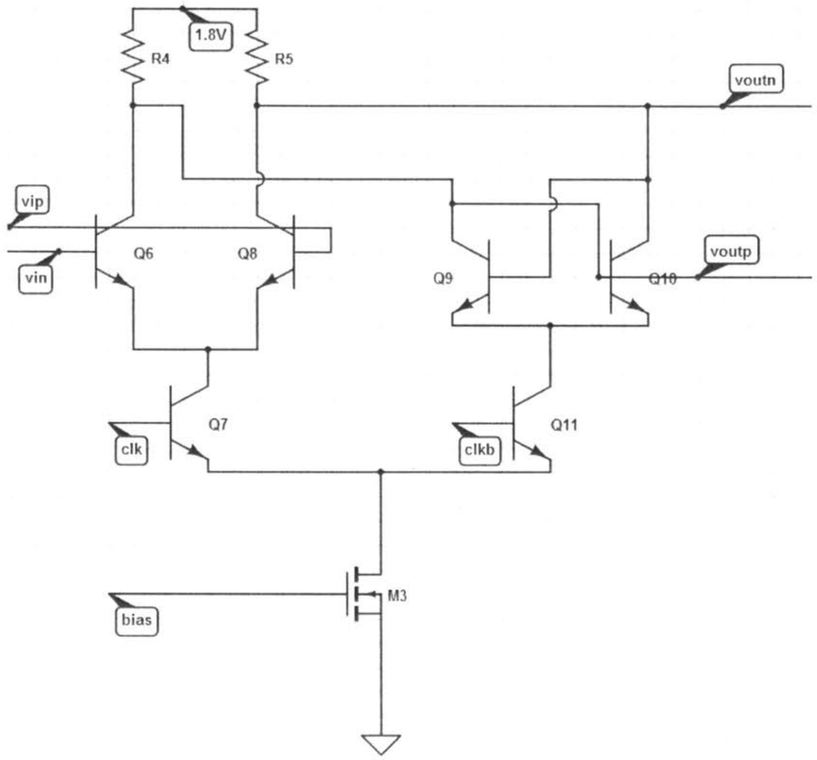


Figure 4-7: schematic of the comparator core

The comparator core is essentially a track/hold circuit. The circuit has two states. When the clock is high, the track mode is on. The amplifier stage amplifies the differential inputs. When the clock is low, the hold mode is on. The positive feedback pair of npns pushes the output voltages to saturation.

The load is also passive because pnps cannot be used at high frequency. However, there are some advantages of using resistive loads. Using resistive loads can save the headroom, thus saving power. Moreover, resistive loads can keep linearity of the circuit. The clk voltage and the bias voltage are chosen carefully to prevent forward biasing of BC junction of bipolar and CMOS operating in triode region from happening. The output swing is set to be 125mV to increase the speed. 125mV output swing is large enough to allow the next stage go to desired output voltage almost immediately. The resistors are chosen to be very small(50 Ohms) to decrease the relaxation time constant and regeneration time constant, thus increasing the speed in both modes of the comparator. Notice, the reason there is no reset CMOS switch between two output nodes is operating at 16GHz, it costs too much power to build such a clock to turn on and turn off the CMOS switch. The track stage has a DC gain of 5 and 3dB bandwidth of 16GHz. The sizes of npns are chosen carefully to tolerate the current density and minimizes the input and parasitic capacitances.

In order to measure how fast a comparator trips, there are two time constant to be introduced. One is relaxation time constant. It determines how fast a comparator can track the input voltage and recovers from the previous clock cycle.The other one is regeneration time constant. It measures how fast a comparator can regenerate to the desired voltage from the amplified input voltage.

Both of the constant can be represented as the effective resistance times the effective capacitances ($R \cdot C$). For relaxation time constant, both the input capacitances of the input diff pair and the positive feedback diff pair are determinant. The charges at input caps of the positive feedback diff pair discharge at track mode. The charges also need to build up at the inputs of the input diff pair. In comparison, for regeneration time constant, only the input caps of the positive feedback diff pair are major because charges only need to accumulate at hold mode diff pair input. For both time constants, the effective resistances are similar. Since r_o of npns are much bigger than 50hms, the effective resistances are about to be 50 Ohms.

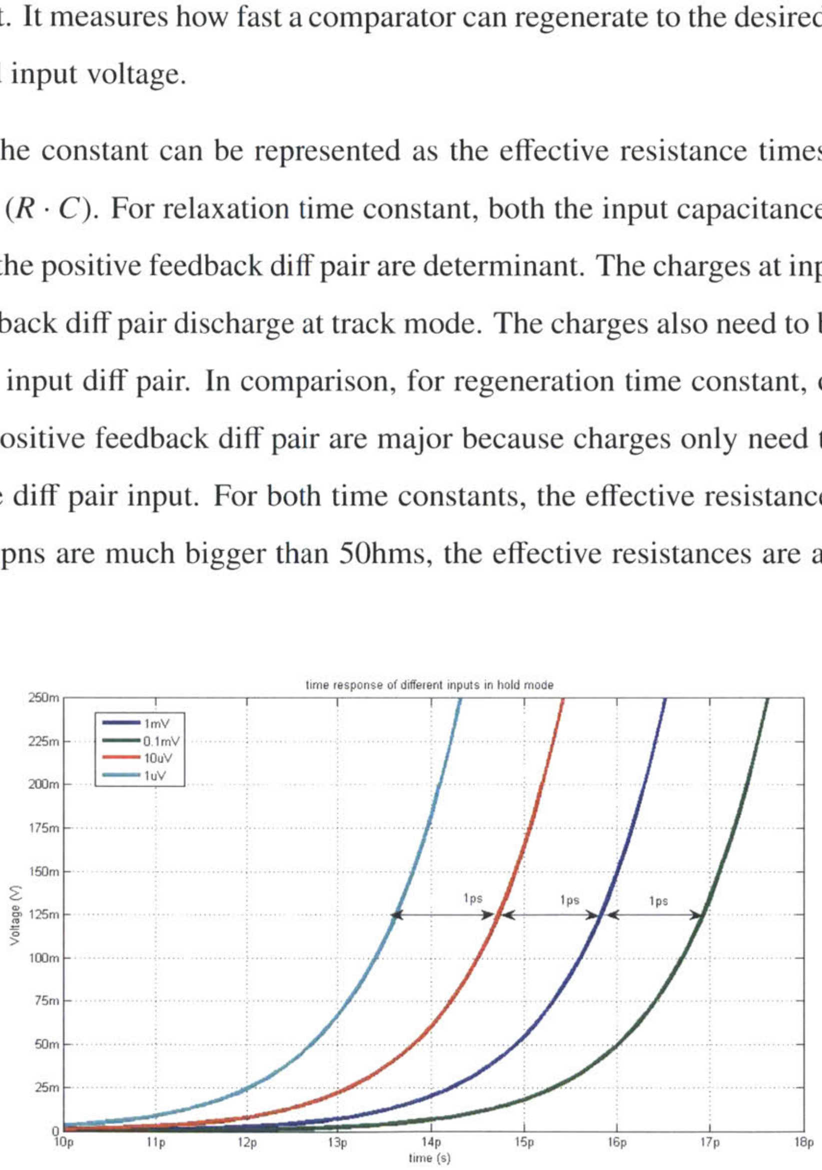


Figure 4-8: regeneration time constant

The regeneration time constant and the relaxation time constant can be measured in this way. We put multiple different input voltages differ by a constant factor to generate several time responses. The time difference between two adherent curves to reach the same voltage is a constant. Figure 4-8 is an example of that.

We can calculate the regeneration time constant and relaxation time constant by :

$$\tau_{reg} = \Delta t / ln(K) \tag{4.2}$$

K is the common factor of the inputs. In this case of Figure 4-5, K is 10 and the regeneration time constant is

$$\tau_{reg} = 1/ln(10) = 0.43ps \tag{4.3}$$

The relaxation time constant can be measured by the same method. Instead of waiting it to reach a desired voltage, we first push the outputs to be at the correct output level. Then we reverse the clock to switch to track mode and apply an opposite sign input voltage. Finally, we measure the time it takes to reach the common mode voltage which is the indication of correctly tracking the inputs.

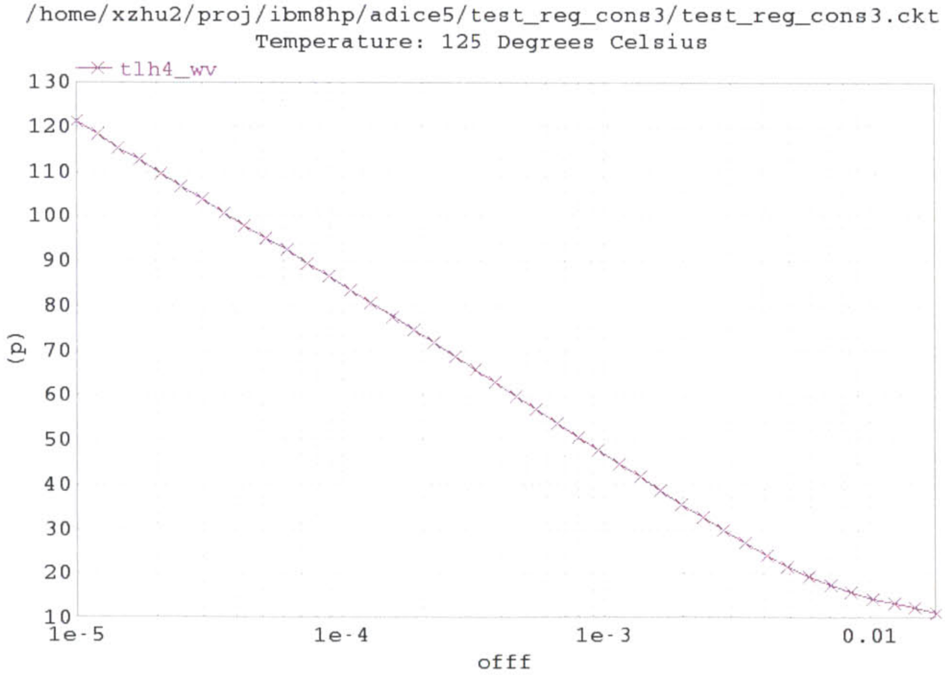


Figure 4-9: plot of comparator regneration time constant measurement

Figure 4-9 is the plot of the regeneration time constant measurements. Y-axis is the time it takes to reach 125mV. X-axis is the differential input voltage. The relationship between input voltage and total time is linear, indicating the time difference between two adherent inputs are constant. When the input is large, the comparator almost saturates immediately, so the time converges to an unavoidable delay (t_o).For this design, the regeration τ_{reg} is 14ps. The t_o is 10ps.

If we want an OSR of 32, the clock is 16GHz. Half of the clock cycle is allocated to the regeneration phase, which is 0.5/16G, or 31.3ps. Looking at Figure 4-9, in order to correctly operate at 16GHz, the comparator needs at least 2.5mV differential input. Any input voltage below 2.5mV yields an error.

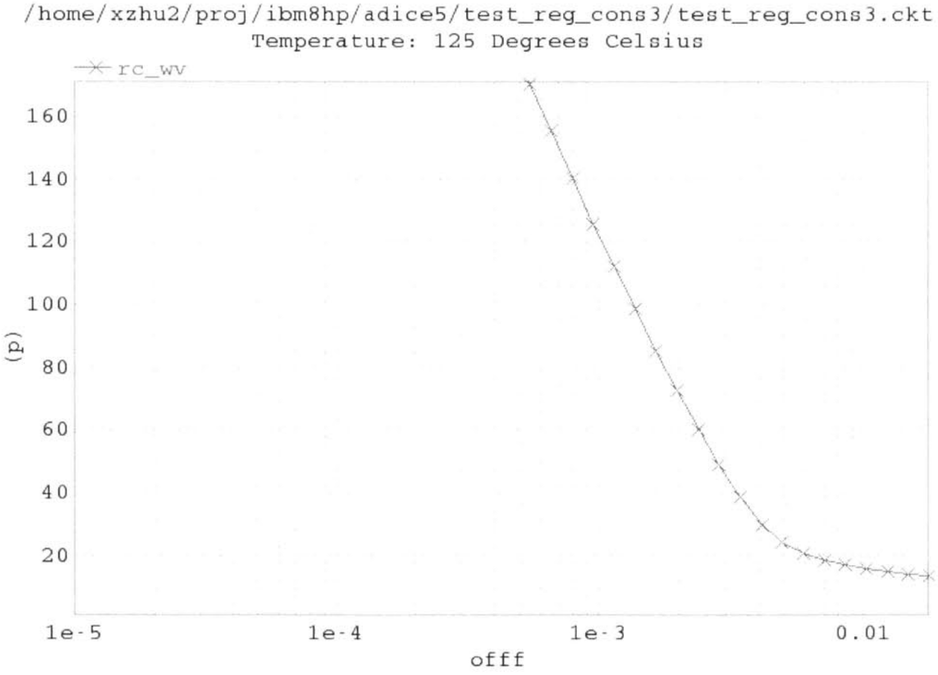


Figure 4-10: plot of comparator relaxation time constant measurement

Figure 4-10 is the plot of the relaxation time constant measurement. Y-axis is the time it takes to reach 125mV. X-axis is the differential input voltage. The τ_{relax} is 71.3ps and the t_o is 16ps. This constant is larger because it takes account the input caps of two diff pairs. From this plot, in order to operate at 16GHz, a 3.5mV differential input is required. Comparing the two constants, the track mode determines the speed of the comparator.

We can consider the comparator core as a Schmitt Trigger with a hysteresis of 3.5mV. The problems of this behavior is it could give wrong outputs and increase chances of being metastable each step. If the differential input voltage is smaller than 3.5mV, the output would end up in the wrong logic. Moreover, if the differential input voltage is very close to 3.5mV, within the half clock cycle constraint, the output voltage might end up in the situation that it cannot give the next stage correct output to be 0 or 1.

For the comparator core, the bias current is 2.5mA. The power of the comparator core is 1.8·2.5m = 4.5mW.

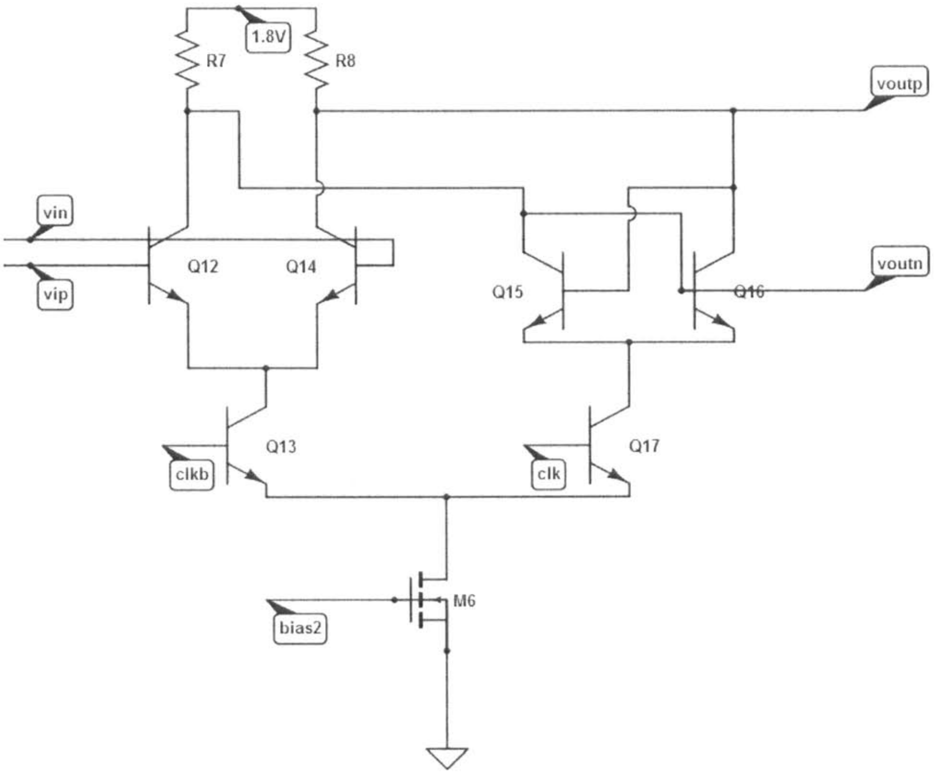


Figure 4-11: latch stage of the comparator

The next thing to discuss about the comparator is the output latch stage. The latch is necessary because the output of the comparator directly connected to a VDAC. The output of the comparator needs to always be in high state or low state to make VDAC work properly.

It has a similar structure of the comparator core. The bias current is 1mA. It is chosen to be small because as long as the input stage has a gain bigger than 1, the output could reach 200mW , which is the voltage level to 99% bias a diff npn pair, almost immediately assuming the comparator core works properly. The output swing is chosen to be 250mV to increase the gain and allow fully switching of the next bipolar input stage. The gain can be found by

$$A = g_m R_{load} = \frac{i_c}{V_{th}} R_{load} = \frac{V_{swing}}{V_{th}} \tag{4.4}$$

Figure 4-12 is the bode plot of the track stage of the latch. It has a DC gain of 10.3dB and a unity gain bandwidth about 16GHz. This promises as long as the comparator core gives a valid output of 125mV, the latch would keep the output voltage to be bigger than 200mV for this clock cycle. Notice the clock of the comparator core and latch are opposite. The sizes of the transistors are chosen to meet the current density requirement.

For the latch stage, the bias current for the latch is 1mA and the power is 1.8mW.

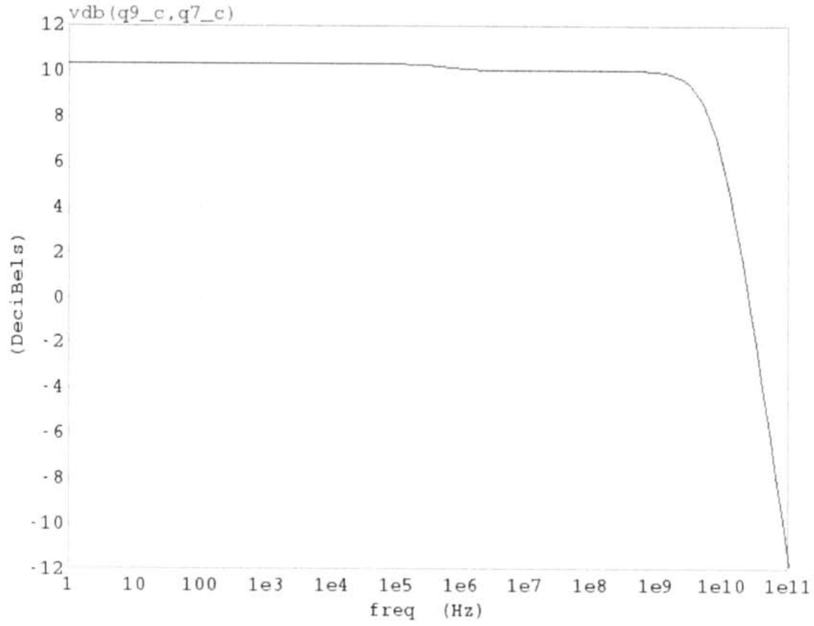


Figure 4-12: latch of the comparator

The total power of the comparator is 8.3mW. A 9-level quantizer consumes about 70 mW power. The consumption is able to meet the power budget. A possible improvement of the comparator is to reduce the relaxation and regeneration time constant. This requires decreasing the load resistance and increase the biasing current, hence more power. Another way is to increase the gain of the pre-amp, requiring an increase in swing and VDD, thus power.

Monte Carlo analysis has been done on the comparator. Table 4.1 shows the Monte Carlo results of several important variables of this comparator.

Notice the offset voltage has a large sigma of 7.6mV. It is expected because the size of input diff pair npns only considers the speed, not the offset. A small npn has less parasitic capacitances while a large npn has less offset, but more parasitics. The 3σ offset is smaller than 1/4 of LSB (125mV), therefore the comparator would still work properly.

Table 4.1: Performance at peak F-measure

Variable	Mean	Sigma
Offset	-80uV	7.6mV
Regeneration time constant	13.3ps	3.3ps
Relaxation time constant	73ps	6ps
Power	8.1mW	0.5mW

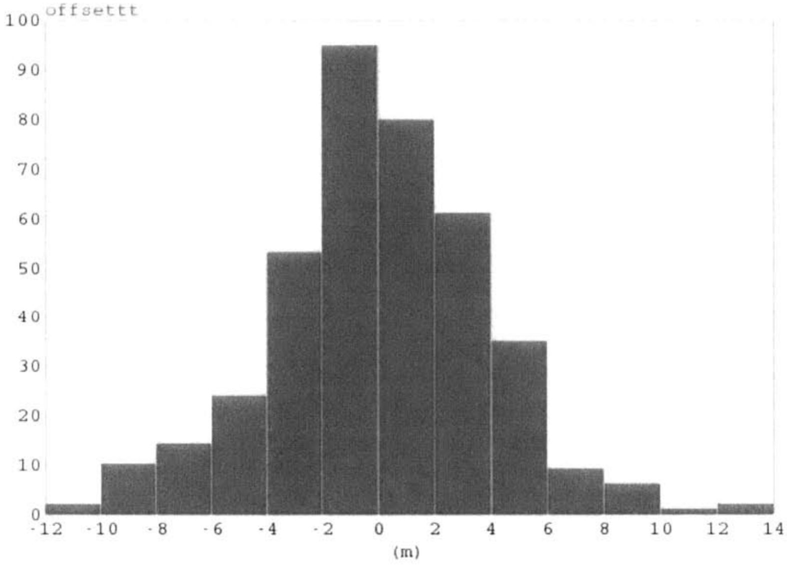


Figure 4-13: Monte Carlo results of the offset measurement

4.2.2 Flash ADC design

Usually in a multi-level DS ADC, Flash ADC is the top choice for the quantizer because a flash ADC only has one step delay. A flash ADC is essentially a combination of several comparators with different reference voltages. A typical schematic of a flash ADC is

The resistor ladder generates the reference voltages. The comparators compare the reference voltages and the inputs to give outputs in one clock cycle. In this thesis, all components are fully differential, so does the flash ADC.

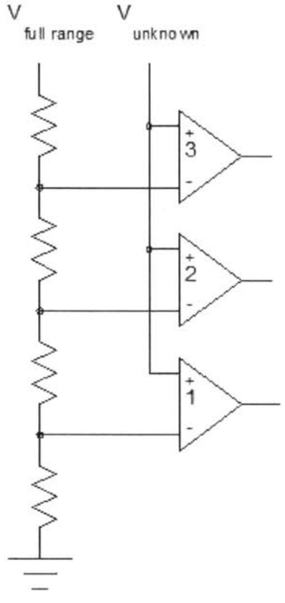

V full range
V unknown
3
2
1
+
-

Figure 4-14: a 4-level flash ADC

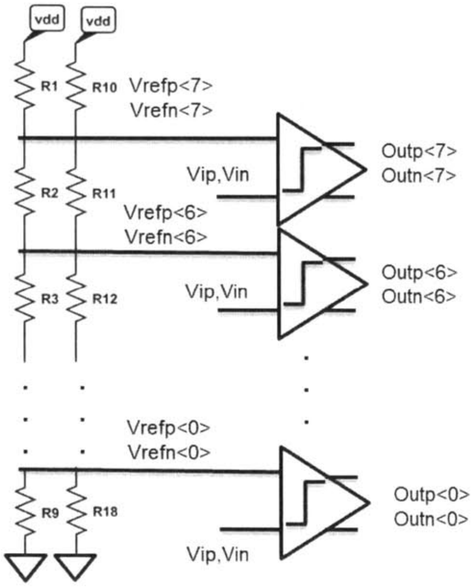

vdd
vdd
R1
R10
Vrefp<7>
Vrefn<7>
Outp<7>
Outn<7>
Vip,Vin
R2
R11
Vrefp<6>
Vrefn<6>
Outp<6>
Outn<6>
R3
R12
Vip,Vin
Vrefp<0>
Vrefn<0>
Outp<0>
Outn<0>
R9
R18
Vip,Vin

Figure 4-15: Schematic of the 9-level quantizer

Figure 4-15 is the schematic of the 9-level flash ADC used in this Delta-Sigma ADC. The referrence voltages are also differential. The references voltages are chosen such that

$$V_{refp}[n] - V_{refn}[n] = VLSB \cdot (n - 3.5) \tag{4.5}$$

For a 9-level quantizer and the full scale is 1V, VLSB is 1/(9-1) = 125mV. There are no buffers between the resistor ladder and the comparator. The main reason for not putting buffers is the power budget. The resistor ladders requires total of 16 buffers. Without buffers, the reference voltages fluctuate because the inputs to the flash ADC changes frequently. Every change may lead to a different input npn to turn on, hence absorbing some current from the resistor ladder. The way I stabilize the reference voltages is to make the total resistance to be small enough to make currents large. By choosing resistance carefully, the fluctuation of reference voltages could always stay within 10 percent of VLSB.

The NTF minimizes the impact of the offset of the flash ADC. Here we use the advantage of noise shaping of DS ADC to save the power by not adding the buffering stage. The purpose of a buffer is to isolate two stages and provide current to the next stage. Here even though directly connecting the resistor ladder and the comparators causes the reference voltage to fluctuate, the NFT minimizes the offset voltage impact on the entire loop. However the buffer stage consumes much more power if considering there are 9 buffers, even there is a small power of each buffer.

The total power of this Flash ADC is 70mW.

4.3 Feedback IDAC and VDAC design

4.3.1 IDACs mismatch

The first feedback IDAC is the most crucial block in determining the performance other than the flash ADC. Especially the linearity and noise of the first IDAC in a higher order DS ADC limits the SNR. We can see the reason from Figure 4-16.

Similar to the quantizer model we develop in the introduction, we can assume the IDAC also acts as the sum of a perfect IDAC and an external noise.

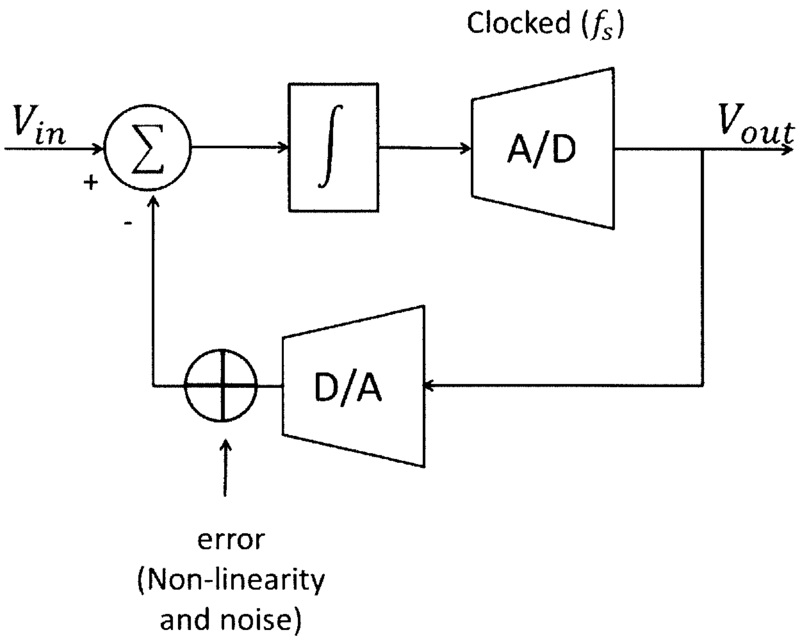


Figure 4-16: 1st order DS ADC model

The transfer function of the error is

$$\frac{V_{out}}{error}[z] = \frac{A[z]B[z]}{1 + A[z]B[z]C[z]} \approx \frac{1}{C[z]} \tag{4.6}$$

C[z] is the transfer function of the 1-bit DAC in frequency domain. The transfer function of a DAC con be approximated to be a constant of 1 within the bandwidth. Therefore, the non-linearity and the noise of the IDAC will not be shaped. However, unlike the noise of the first IDAC, the noise of the other IDAC could still be loop filtered. In the design process of the first feedback DAC, the non-linearity and the thermal noise is the priority.

In order to achieve an ENOB of 10-bit, the mismatch of the first IDAC has to at least be less than 0.5 LSB of the DS ADC, which is

$$mismatch \leq 0.5/2^{10} \approx 0.05\% \tag{4.7}$$

There are three sources of matching error — systematic mismatch , random mismatch and gradient mismatch. Systematic mismatch and gradient mismatch can usually be avoided by careful layout and circuit design. Random mismatch is due to local variation in process parameters and it is limiting the linearity of the IDAC [12].

For a CMOS diff pair, the standard deviation of error is [13]

$$\sigma_{\Delta VT} = \frac{A_{VT}}{\sqrt{WL}} \tag{4.8}$$

A_{VT} is a constant for each process and W,L are the width and length of a CMOS. In the IDAC design, we care more about drain current variation. The relative drain current variation of CMOS operating in saturation region is

$$\left.\frac{\sigma_I}{I}\right|_{VT} = \sigma_{VT}\frac{g_m}{I} = \sigma_{VT}\frac{2}{V_{GS} - V_T} = \frac{A_{VT}}{\sqrt{WL}}\frac{2}{V_{GS} - V_T} = \frac{\sqrt{2} \cdot A_{VT}}{\sqrt{I} \cdot L} \tag{4.9}$$

Notice, if we keep the current constant, if we only increase W, the mismatch would be the same. To see that, if we increase W by 4, then σ_{VT} is decrease by 2. However, $V_{GS} - V_T$ is also decreased by 2 and the mismatch does not change. Therefore, in order to decrease the random mismatch, we need to increase both W and L.

4.3.2 Feedback IDACs

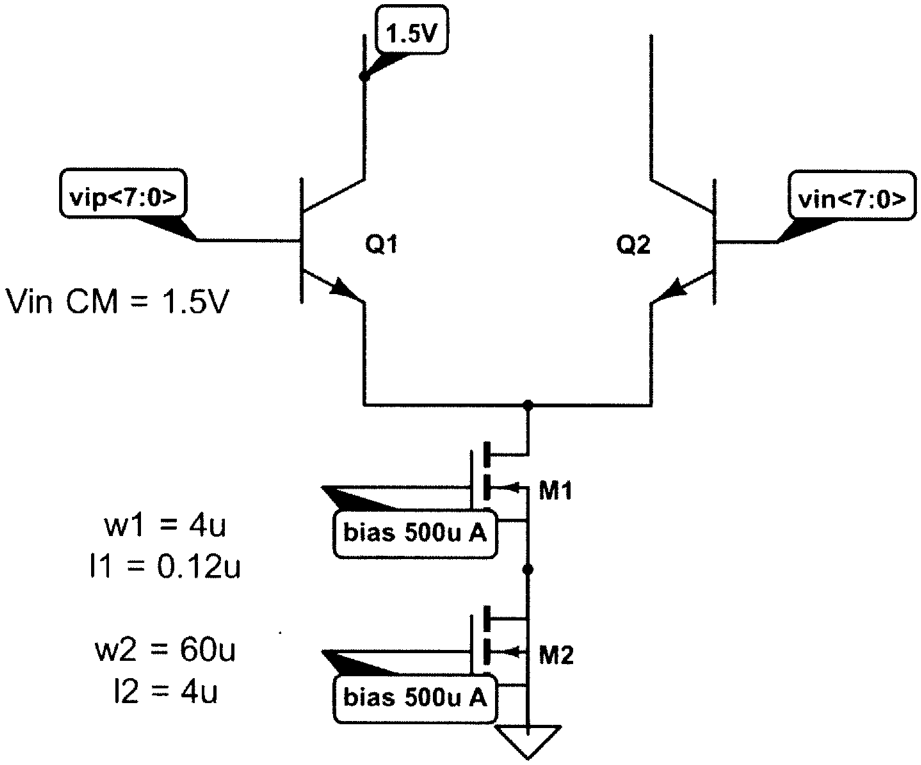


Figure 4-17: schematic of IDAC

Figure 4-17 is a schematic of the IDAC design. It uses a bipolar diff pair as input stage for speed and a cascoded current source in CMOS. A cascoded current source can provide higher output impedance, reducing the output voltage variation.

In this design, the width of M2 is set to be 60um, the largest width I can choose without worrying about layout size. The length of the bottom CMOS is set to minimize the mismatch and keep the device in saturation region. The size of M1 is set accordingly to leave enough V_{DS} for the bottom CMOS to operate in saturation region. This current source gives a 3σ mismatch of 0.04%. The input stage npn sizes are also optimized to be small enough to operate at 16GHz and have a mismatch slightly smaller than 0.05%.

The output of the IDAC is connected to the input of the OP-amp, not to a power supply. Recall $V1$ and $V2$ are outputs of first and second integrator. A common-mode feedback loop is connected to the input of the OP-amp to ensure the common-mode voltage stabilizes at 1.5V as in Figure 4-18. The differential output of the IDAC is connected to a pair of common-mode current source and a voltage controlled current source to stabilize the common-mode voltage.

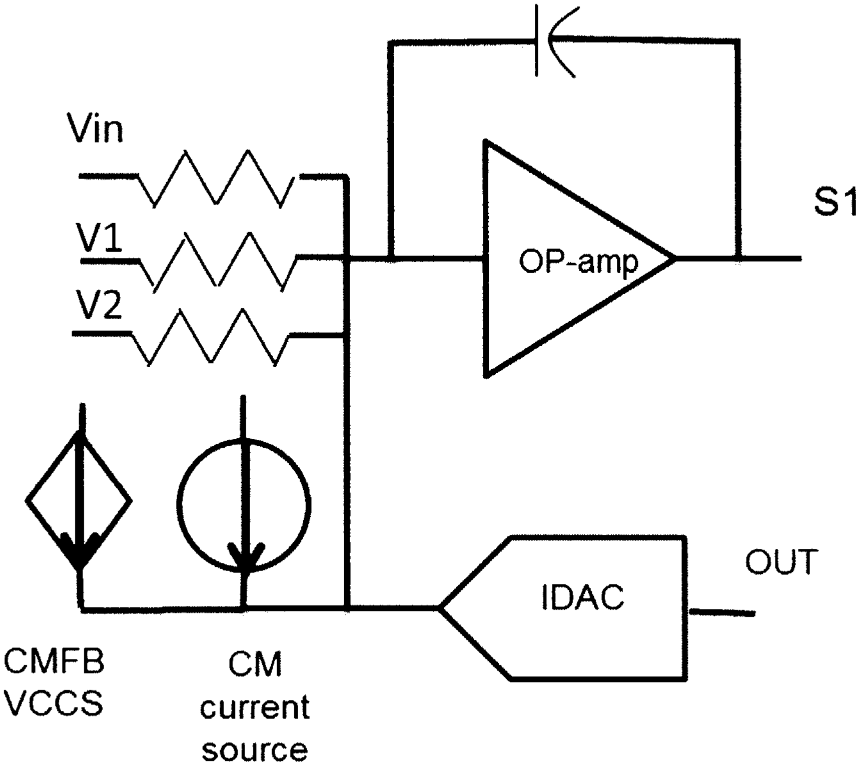

Vin
V1
V2
OP-amp
S1
IDAC
OUT
CMFB
VCCS
CM
current
source

Figure 4-18: schematic of IDAC

The second feedback IDAC is designed in a similar process with a different bias current.

4.3.3 Feedback VDAC

The VDAC has the same structure with the IDACs. The only difference is the outputs are converted to voltages through resistances and the VDAC is connected to a 1.8V power supply. The load resistances and bias current are chosen to give a LSB of 125mV while not having a significant fluctuation due to inputs and outputs as well as fast enough to operate at 16GHz.

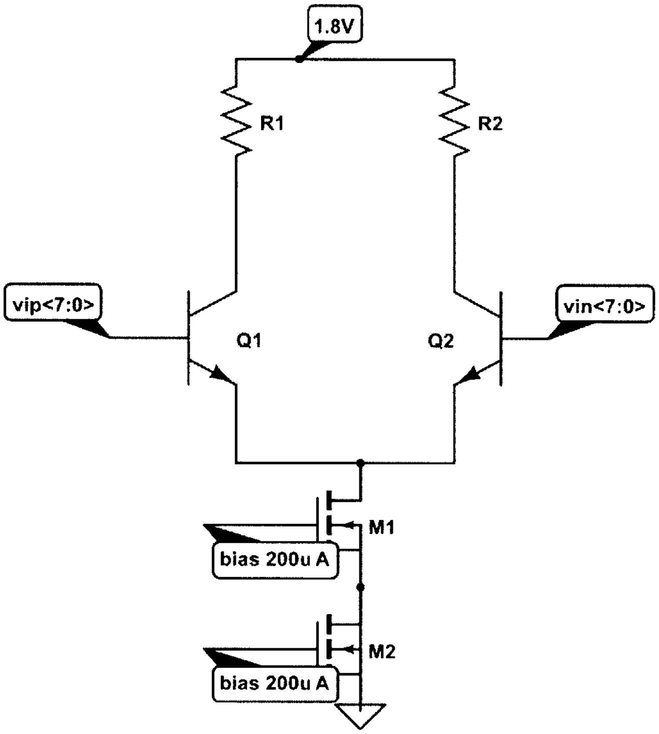


Figure 4-19: schematic of VDAC

4.4 Integrator design

The integrator is essentially an OP-amp in a special configuration as in Figure 4-20. To design an OP-amp, a good bipolar device has an advantage over a same minimum feature CMOS because of a larger intrinsic gain. With active loads in one stage, the gain of a bipolar amplifier is

$$A = g_m r_{out} = \frac{I_c}{V_{TH}} \cdot \frac{V_A}{I_c}/2 = \frac{V_A}{2 \cdot V_{TH}} \tag{4.10}$$

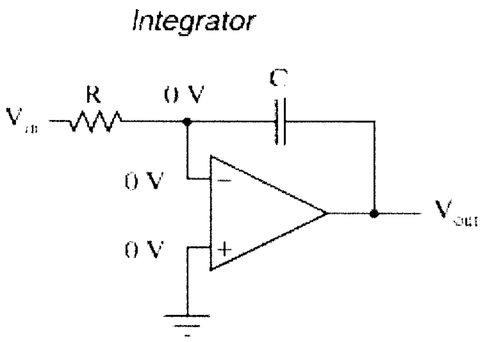


Figure 4-20: schematic of VDAC

V_A is the early voltage, which usually bigger than 10.V_{TH} is the thermal voltage to be around 25mV. This gives the rough gain of one stage to be 200. The gain of a CMOS amplifier is

$$A = g_m r_{out} = \frac{2I_d}{V_{GS} - V_{th}} \cdot \frac{1}{\lambda I_d}/2 = \frac{1}{\lambda \cdot (V_{GS} - V_{th})} \qquad (4.11)$$

λ is the length modulation constant to be around 0.1. The effective voltage $(V_{GS} - V_{th})$ is usually bigger than 200mV.Therefore, the gain is around 50.From the comparison, we can see using BJTs can simplify the OP-amp design by having fewer stages.

After deciding the gain stage component, the next concern is what specifications of the OP-amp can make the DS ADC work properly . The best way to find that out is to replace the ideal integrators with voltage controlled voltage blocks with finite gain and finite bandwidth. With a DC gain of 200 and a bandwidth of 500MHz, the semi-ideal OP-amp decreases the SQNR by 2dB. A gain of 200 and a bandwidth of 500MHz is reasonable for this design. In the OP-amp design, a higher gain possible requires more stages and a higher bandwidth is not very feasible because of the pnp only has a FT of about 1GHz with I_c where npn peaks.

Figure 4-21 is the schematic of the OP-amp. The structure is very simple. It has only one stage with a common-mode feedback and two output buffers. The active loads are pnps. The reason in the OP-amp design we can use pnps is that in DAC and flash design, it requires to operate at 16GHz, way beyond the FT of pnp while the OP-amp only requires to operate at 250MHz. Although the inputs are changing at 16GHz, the OP-amp is acting as an integrator, which smooths the high frequency component. Therefore, the OP-amp only need to be able to amplifier the major signal which has a bandwidth of 250MHz. The active loads provide extra gain comparing to resistive loads, making a single-stage OP-amp structure possible. Notice the V_{BC} of pnp is set to be 1V, corresponding to an early voltage of 30V. This makes pnp a better active load than a PMOS because of bigger output resistance.

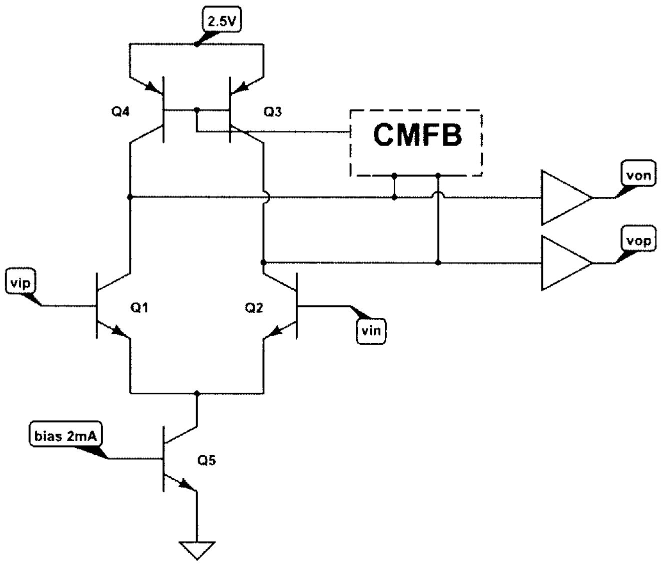


Figure 4-21: schematic of the OP-amp

Figure 4-22 is the common-mode feedback schematic. It stabilizes the common-mode voltage of the OP-amp output at 1.5V. The two input resistances average the differential outputs and comparing the average voltage to 1.5V. The output is connected back to the bases of active loads to control the I_c of pnps, hence controlling the output voltages.

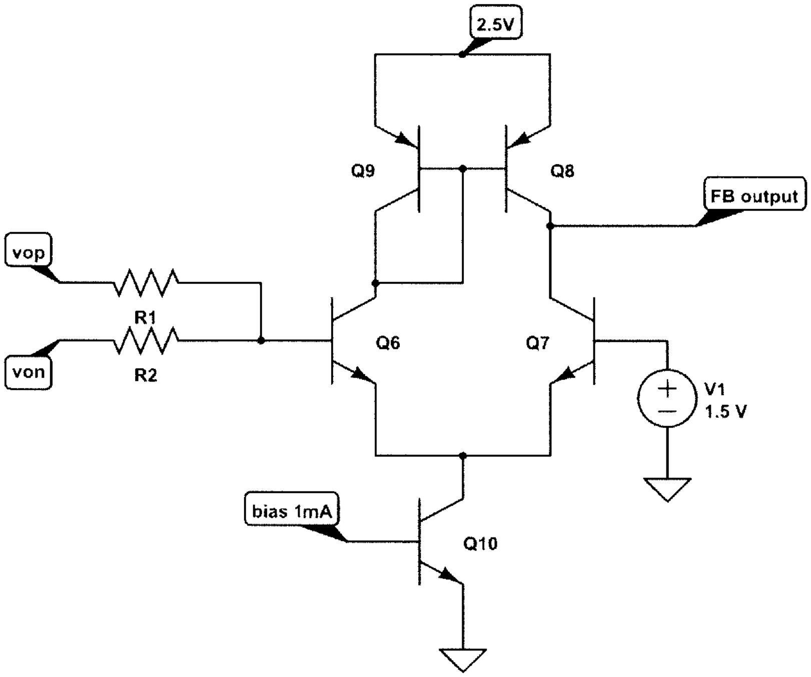

2.5V
Q9
Q8
FB output
vop
R1
von
R2
Q6
Q7
V1
1.5 V
bias 1mA
Q10

Figure 4-22: schematic of CMFB block

The output stage is a buffer as in Figure 4-23. It is composed of two stages of emitter follower. It helps separating outputs from the inputs of the next stage and it is able to provide currents to the next stage. Since the OP-amp is connected to conductance to convert voltage into currents, a diamond buffer output stage is necessary to provide such currents. The stage has a gain of -0.43 dB.

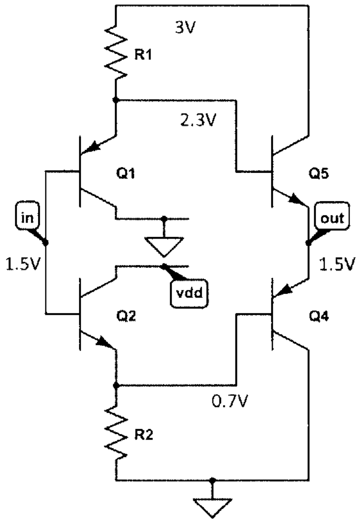

3V
R1
2.3V
Q1
Q5
in
out
1.5V
1.5V
vdd
Q2
Q4
0.7V
R2

Figure 4-23: schematic of output stage

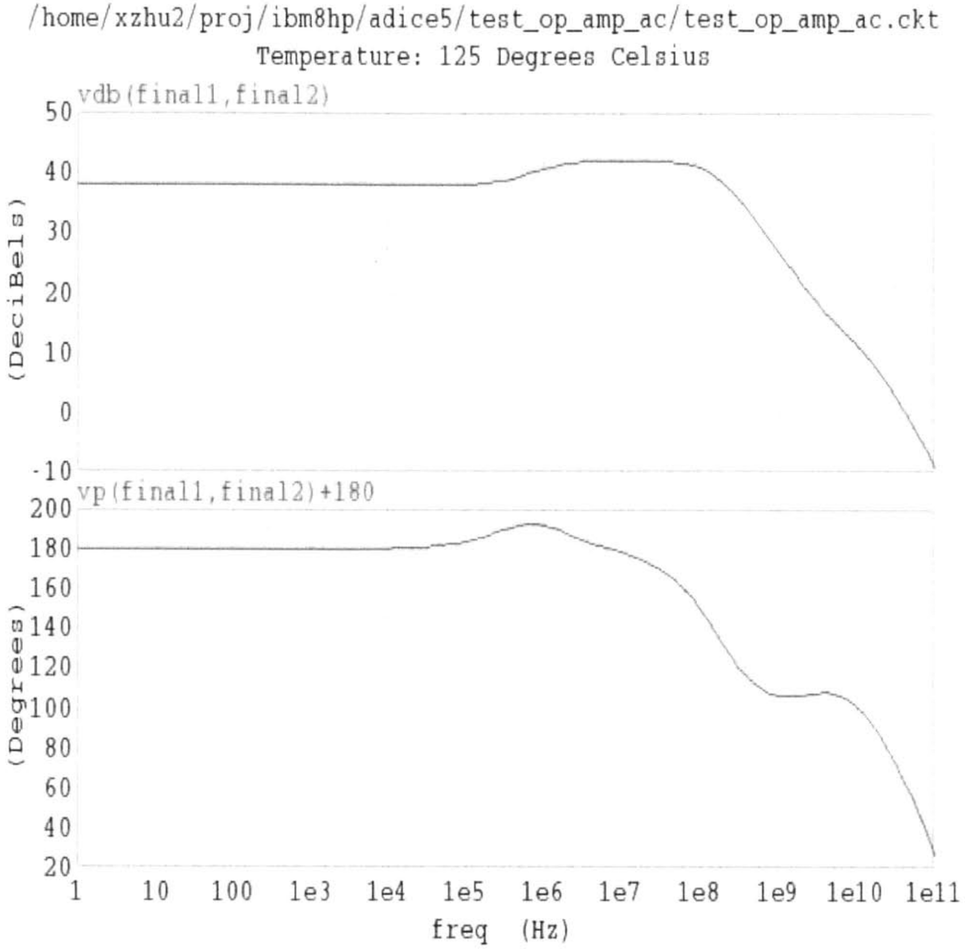


Figure 4-24: bode plot of the OP-amp

Figure 4-24 is the bode plot of the OP-amp. It has a DC gain of 38dB, and a 3dB bandwidth to be 400MHz. The phase margin is 61 degrees. The design results are a little off the original target. The best way to test it is to put the OP-amp in the DS loop to see how much SQNR degrades. Notice there is a right half-plane zero around 1MHz. It is due to the large C_{BE} of Q4. The junction capacitance creating a bridge between the output and the output from the first stage, leading to the feedforward effect. Similarly, at 1GHz, the C_{BE} of Q5 creates another right half-plane zero, leading to the phase increase around 1GHz. The architecture simulation results with the blocks discussed in Chapter 4 will be discussed in Chapter 5.

Chapter 5

Simulation results

The best way to test how well a component is designed is to put the transistor-level circuit in the Delta-Sigma loop. In this chapter, the emphasis is on a Fourier analysis of the signal quality.

Figure 5-1 is the simple representation of the test bench. The input is a sine wave. The amplitude is 1dB smaller than full scale (1V) to avoid clipping. The output is processed to give a SQNR. The script of signal analysis is in the appendix B. A *Hann*^{2} window is applied to reduce the number of points needed to acquire a correct calculation.

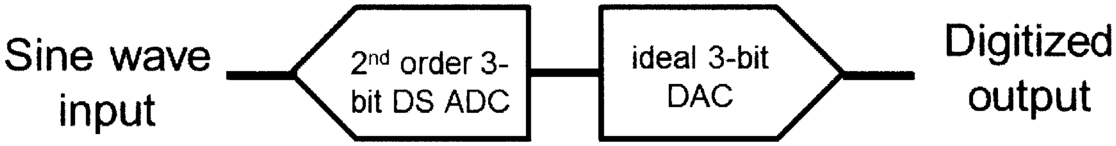


Figure 5-1: schematic of IDAC

In this chapter, I will first analysis the behavioral model circuit with only one transistor-level circuit. Then I will analysis the behavioral model with multiple transistor-level circuit to identify the limiting blocks.

The output signal spectrum of the ideal behavioral model is in Figure 5-2. Because of *Hann*^{2} window, the signal is separated into five different bins. In this plot, the bins are around 9MHz,which is the input frequency for the simulation test bench. The noise is shaped according to the optimized NTF generated from the MATLAB toolbox. The SQNR of the ideal model is 78.4dB, about the same as the MATLAB toolbox prediction. The environment for the simulation is in 125 degree Celsius, which is the worst working condition in real life. High temperature slows down the electron movement, leading to slower circuit and worse noise.

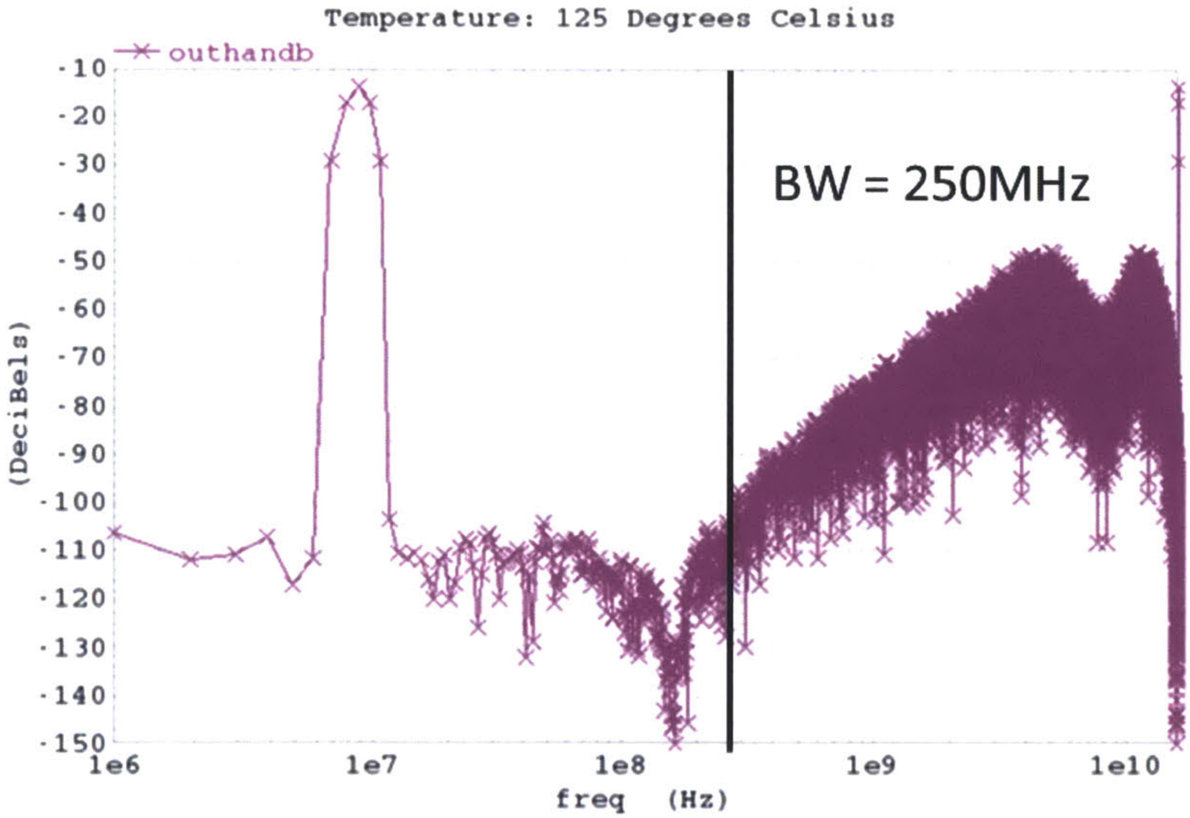


Figure 5-2: FFT of the output from the behavioral model without any transistor

5.1 Individual block analysis

Figure 5-3 is the output signal spectrum of the ideal model with the real transistor-level flash ADC. The SQNR drops to 67.4dB. The in-band noise power density is increased by about 10dB. Also there is a peak of NTF at very high frequency. The major reason for the significant degradation and incorrect noise-shaping is the speed of the comparators. Each clock cycle (0.5/16G), there is only enough time for two regeneration time constants (14ps). That means a large range of inputs to the comparator (absolute value less than $125mV/10^2 = 1.25mV$) will increase the probability of a metastability output. The high rate of being metastable and the 3.5mV hysteresis leads to an incorrect NTF. In order to improve the NTF, the solution is either increasing the power or reduce the sampling frequency.

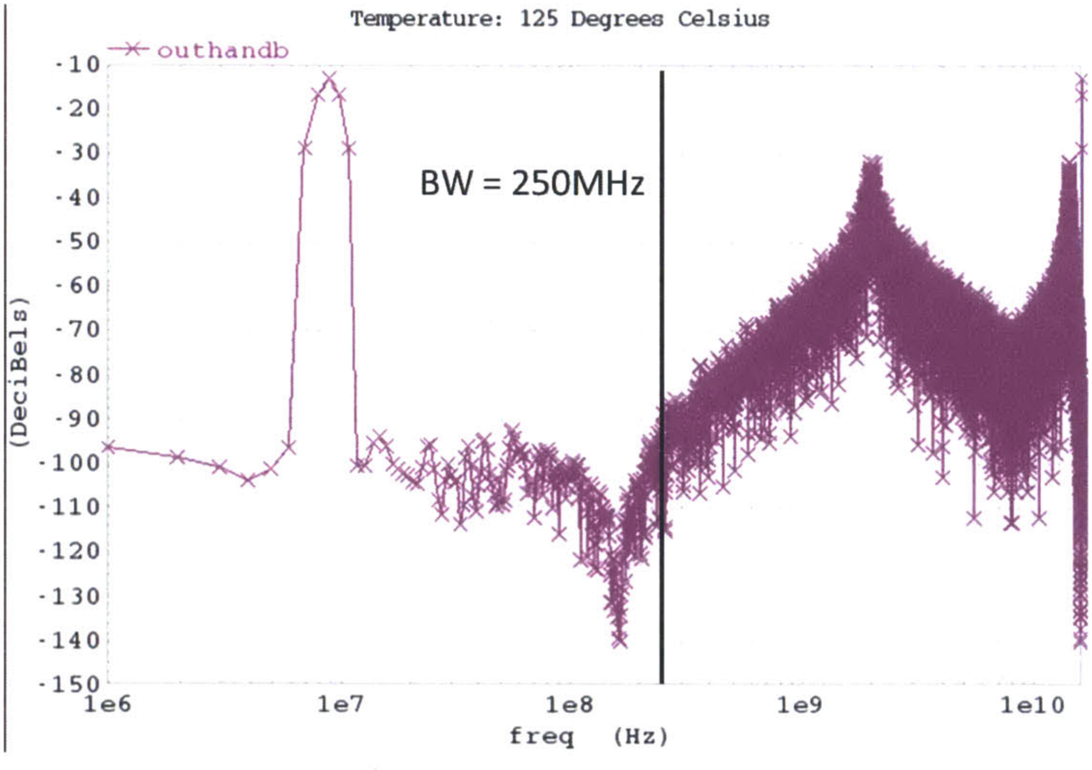


Figure 5-3: FFT of the output from the behavioral model with a transistor-level flash ADC

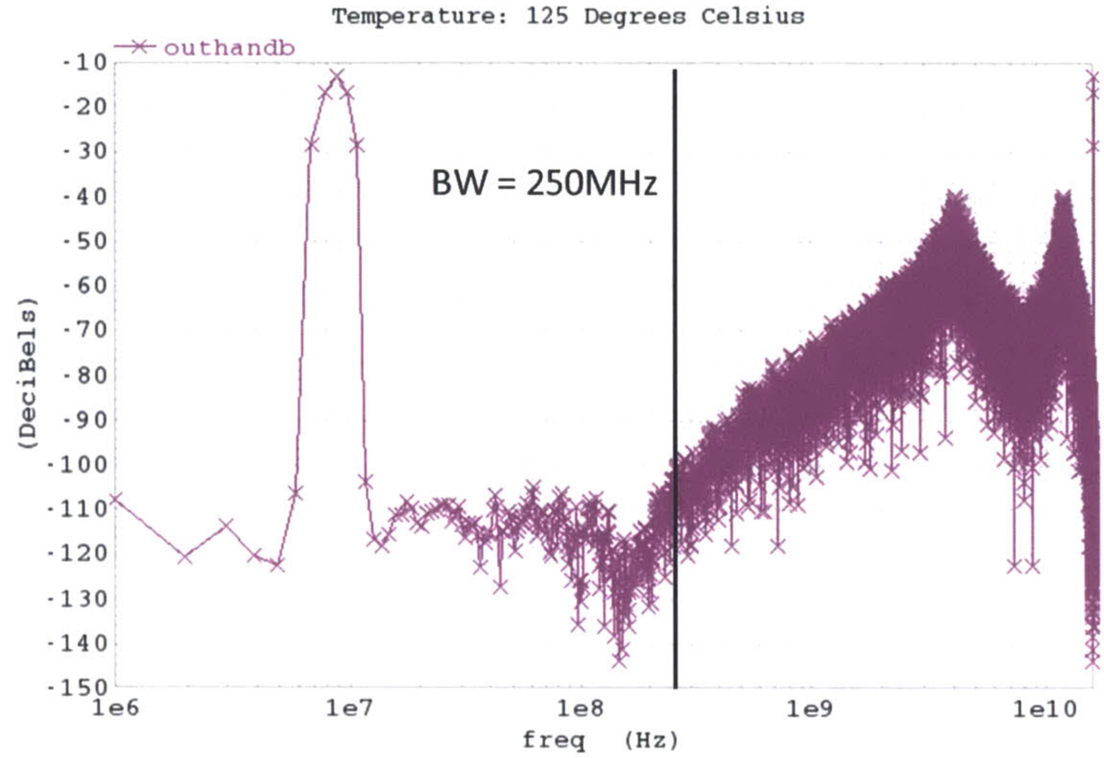


Figure 5-4: FFT of the output from the ideal model with the transistor-level IDACs

Figure 5-4 is the FFT of the ADC with IDAC to be transistor-level. This simulation was run in ideal environment (no Monte-Carlo variation considered). The SQNR is 78.3dB, which is almost the same as the ideal SQNR. It makes sense because without Monte-Carlo variables, there is no offset or mismatch in the IDACs. Therefore, the only degradation of the IDACs to the ADC is the speed. With a careful design, the degradation due to the speed of the IDACs is minimized.

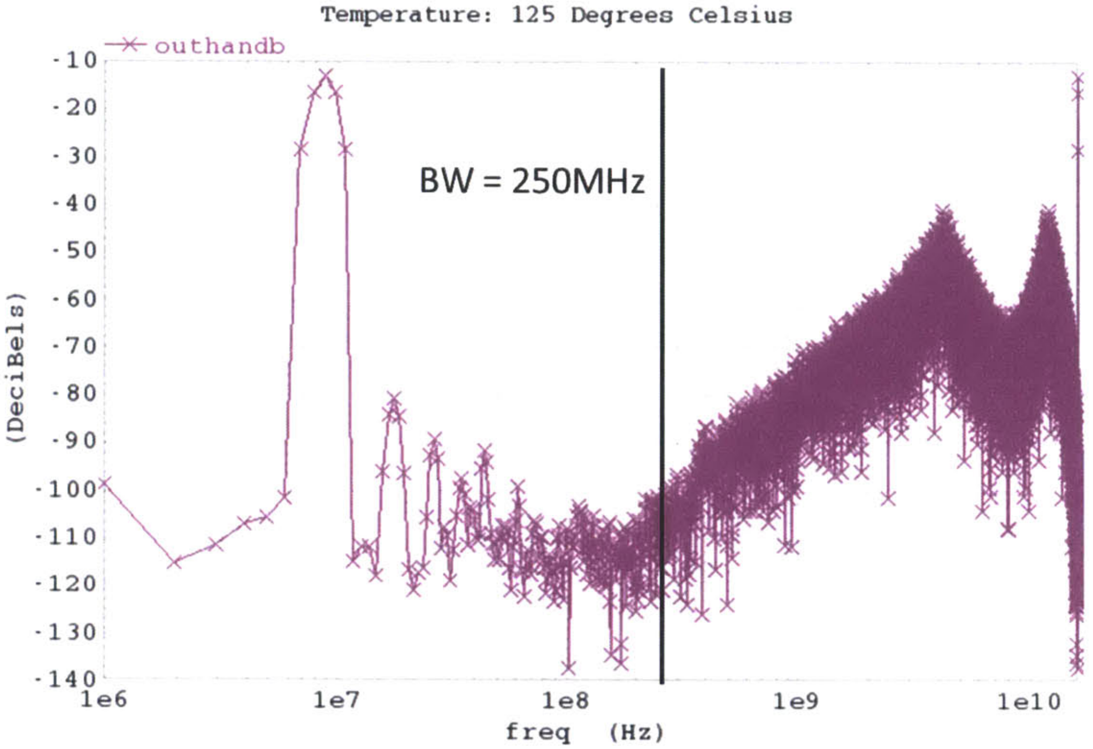


Figure 5-5: FFT of the output with IDACs under Monte-Carlo analysis

Figure 5-5 is the FFT with the IDACs with mismatch. The specific Monte-Carlo trial shown here is one which stored 3σ mismatch in simulations of the IDAC on its own. The SQNR drops to 66.3dB. In the power spectrum, there are large harmonics, especially at twice and three times of the input frequency due to non-linearity. The mismatch of a 3σ case is 0.04 % in the IDAC. Moreover, since there are eight pairs of diff inputs in the IDAC, the relative mismatch between each branch of IDAC could be smaller than 0.04%. Therefore, the output SQNR of 66.3dB matches the prediction of SQNR to be a little higher than 10-bit or 61.8dB.

Noise-shaping could improve the performance of IDACs. Mismatch-shaping includes methods like element rotation and swapping. Some initial analysis has been done in MATLAB as in Figure 5-6. The idea of element rotation is to use the DAC elements in a rotation way. For example, suppose a 3-bit IDAC, at time 1, the first 8 IDAC cells are used. At time 2, the second 8 IDAC cells are used. At time 3, the first 8 IDAC cells are used again.

This equals to apply a $\frac{1}{1-Z^{-1}}$ filter to the mismatch [14]. Some initial analysis has been done in MATLAB as in Figure 5-6. The predicted perfect SQNR for this case is 107dB. The SQNR without mismatch shaping method is 57dB. The SQNR with element rotation is 97dB. Therefore, after implementing one mismatch-shaping method, the SQNR is expected to be very close to the ideal SQNR.

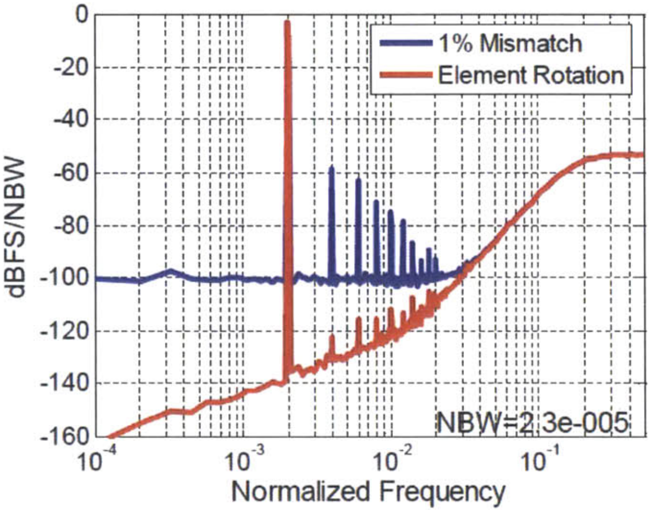


Figure 5-6: FFT of non-element rotation and with element rotation in MATLAB

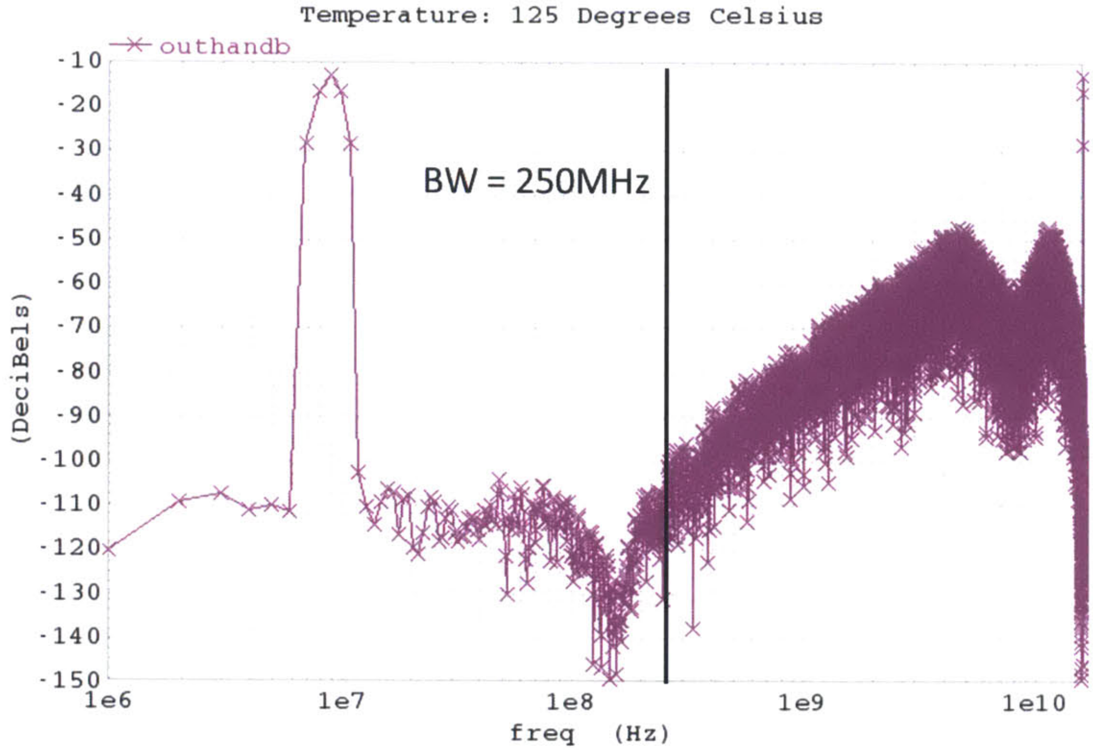


Figure 5-7: FFT of the output with VDAC

Figure 5-7 is the FFT with the VDAC. The SQNR is 78.1dB, almost the same as the ideal SQNR. Under the simulation with a trial that gives 3σ mismatch, the SQNR is 76.9dB, still similar to the ideal SQNR. This makes sense because the mismatch can be loop-filtered. Hence even there could be a huge non-ideality of the VDAC, the DS loop significantly reduces the impact of non-ideality from the VDAC.

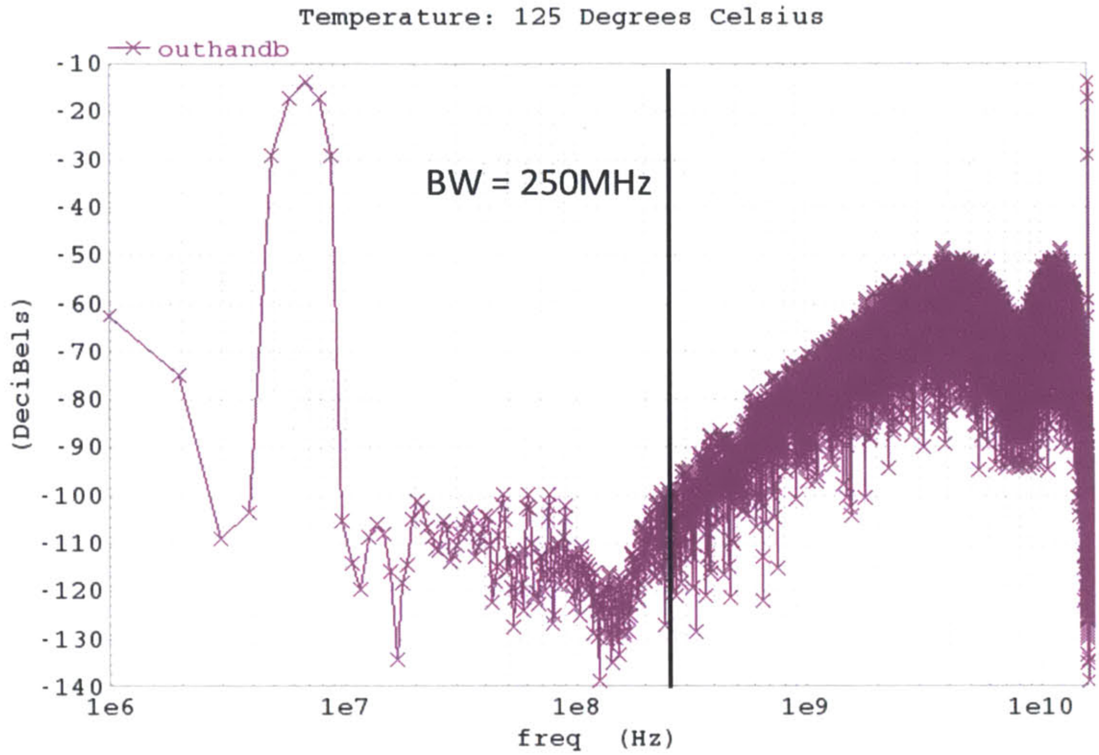


Figure 5-8: FFT of the output with OP-amp

Figure 5-8 is the FFT with the OP-amps under Monte-Carlo 3σ condition. We can see there is a large DC offset here. The offset is not a big problem because we can always adjust the offset voltage of the inputs. Therefore, in this signal analysis, we will ignore the DC offset. Then the SQNR is 74.4dB. As discussed in the OP-amp design in chapter 4, an ideal voltage controlled voltage source with DC gain of 200 and a 3dB bandwidth of 500MHz gives the SQNR to be 76.4 dB. My design has DC gain of 100 and a 3dB bandwidth of 400MHz. There is a 2dB gap possibly due to a smaller gain and a smaller bandwidth. A non Monte-Carlo simulation of the OP-amps gives a similar SQNR to be 75dB. The OP-amp has a less degradation in the DS ADC loop comparing to the IDACs and the flash ADC.

5.2 Multi-block analysis

Figure 5-9 is the simulation with the flash ADC, OP-amps and DACs to be transistor level, leaving latches and summing block to be behavioral. The SQNR is 66.0dB. The noise transfer function is dominated by the flash ADC behavior because the noise level are closer to the noise level from the FFT plot of only Flash ADC to be transistor-level. This implies the flash ADC is the limiting block of the design.

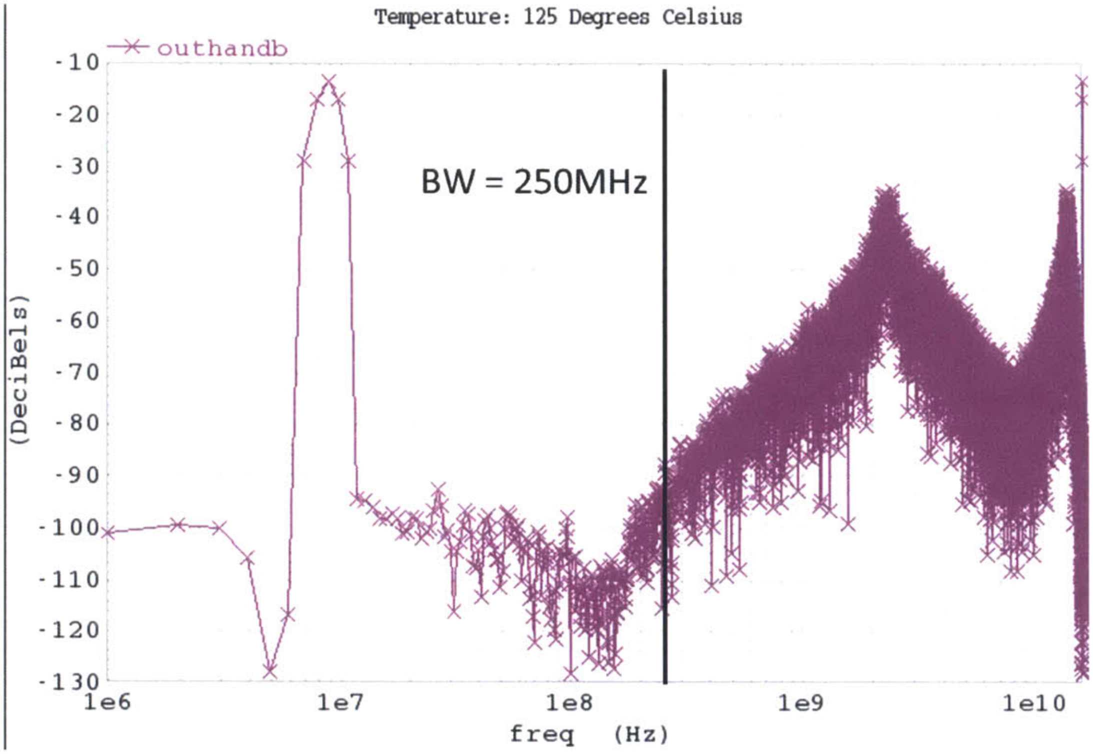


Figure 5-9: FFT of the output with flash, DAC and OP-amp

Table 5.1: Performance in different simulations

Situation	Ideal	Flash	IDACs	VDAC	OP
Non Monte-Carlo(dB)	78.4	67.4	78.3	78.1	75.0
Monte-Carlo (dB)	/	64.9	66.8	76.9	74.4
	DAC,Flash	OP,DAC	Flash,OP	Flash,OP,DAC	
	66.4	74.1	66.2	66.0	
	64.2	65.9	66.0	63.3	

Table 5.1 is the summary of the performances of different situations. The worst case senario is all three blocks with 3σ mismatch. The SQNR is 63.3dB, slightly higher than the target 10-bit. The margin is unlikely be enough to meet the requirement after adding thermal noise and layout parasitics. Also from this table, we can see in order to boost the performance, we need to work on the flash to make it faster and the IDAC to shape the mismatch noise. Fortunately, we still have some room within the power budget.

Table 5.2: Power consumption of each block

Block	integrator	IDAC1	IDAC2	VDAC	comparator	flash reference	Latch	total
Power(mW)	21	0.75	0.25	0.5	8	1	3	140
Number of components	2	8	8	8	8	2	8	

Table 5.2 is the summary of power consumption. The total power consumption is 140mW and there is a 60mW room for performance improvement. I would revise the comparator design and allocate more power for each comparator. An initial simulation shows with a power of 20mW, the regeneration time constant can be reduced to 4ps, one-third of the current design. I am confident in improving the performance of the flash ADC, hence the Delta-Sigma ADC. Another way to make the ADC better is to reconsider the architecture choice. With a fourth order and 3-bit loop filter, the OSR only needs to be 4 to hit the target. Then the requirement for the comparator speed decreases to 2GHz. At 2GHz, it is possible to implement a reset switch, eliminating the reset time, which is the dominant factor of determining the speed of the comparator.

Chapter 6

Conclusion

This thesis explores designing blocks of a Delta-Sigma ADC using a BiCMOS technology. A BiCMOS technology allows the circuit to operate at a very high frequency by reducing the clock swing. It also allows for an easy OP-amp design because of the large intrinsic gain of the bipolars

The design of a Delta-Sigma ADC involves the process of choosing a proper architecture, designing the transistor-level circuits and signal analysis. The architecture is also determined by the specifications of the design goal. The architecture determines the design specifications of each block. The signal analysis indicates which part of the circuit is the limiting factor and points back to where can be improved.

Regarding the future work, a review of the comparator design is necessary. An increase of the speed is expected to significantly improve the performance. More exploration of mismatch-shaping might be useful. The non-linearity of the first feedback IDAC greatly determines the highest SNR we can achieve. Furthermore, the summing block and the latches need to be replaced with transistor-level circuits. The summing block could be built with resistor and capacitances instead of using active elements. Some initial simulations have been done and the result shows a passive summing block is promising. The latches can be build as the same structure of comparator output stage, probably adding buffers to isolate the outputs from the inputs to the next stage. A redesign of the top level architecture is also worth trying. By increasing the order, I can reduce the operating speed of the ADC to become much smaller, possibly yielding a better result. Finally, a layout is needed to tape out this ADC. I have done a small amount of layout for sanity check for the comparator. More of layout needs to be done in the future.

Appendix A

MATLAB DS modulator model

A.1 simulate the behavior of a flash ADC

```
function [y]= flash2(x,full,level)
    lsb = 2*full / (level-1);
    j=-0.5;
    while (j¡=level-1)
    if (x¡=-full)
    y=-full;
    elseif (x¿=full)
    y=full; end
    if (x¿-full+j*lsb) &&(x¡=-full+(j+1)*lsb)
    y = -full + (j+0.5)* lsb;
    j=level;
    else
    j=j+1;
    end
    end
    end
```

A.2 1st order modulator

```
function [v,x] = simulateMOD1(u)
    x = zeros(1,length(u));
    x1 = 0;
    for i = 1:length(u)
    [v(i)] = flash2( x1,1,2 );
    x1 = x1 + u(i) - v(i);
    x(i) = x1;
    end
    return
```

A.3 SQNR analysis script. It starts from OSR =2 to OSR = 1024

```
is=[2:1:10];
    SQ=zeros(1,9);
    ns = zeros(1,9);
    for iwq = 1:1:length(is)
    osr = 2(is(iwq));
    BW = 250;
    fs = 250*osr*2;
    Nfft = 217;
    ftest = 13;
    Atest = 0.99;
    t = 0:Nfft-1;
    u = Atest*sin(2*pi*ftest/Nfft*t);
    v = simulateMOD1(u);
    V = fft(v)/(Nfft)*2;
    V2 = fft(v2)/(Nfft)*2;
```

```
f = linspace(0,fs,Nfft+1); f=f(1:Nfft);
figure(2); clf;
semilogx(f,dbv(V),’c’);
hold on;
TTT = abs(V);
signal = TTT(ftest + 1)^2;
noise = 0;
bwi = BW/(fs/Nfft);
no = [TTT(1:ftest),TTT(ftest+2:bwi)];
for iww = 1:bwi-1
noise = noise + no(iww)*no(iww);
end
ns(iwq) = noise;
SQ(iwq) = (10* log10(signal/noise))
end
figure
semilogx(2.^(is),SQ);
```

Appendix B

DS modulator coefficients

These coefficients are used in ADICE simulator of Analog Devices

```
set flsb = 0.2/(8/5) ;flash ADC LSB
set vlsb = 2/10/(8/5) ;direct feedback VDAC LSB
set sc = 1/1.04 ;input scale
set g11=0 ;conductance between S1 and input of first stage
set g12=-49.51u ;conductance between s2 and input of first stage
set g1u=3.623m ;conductance between input and input of first stage
set rn1=72.13 ;non-ideality model of first integrator model
set c1=578.3f ;first integrator capacitance
set e1=0 ;summing block coefficients of s1
set ilsb1=-447.3u ;first feedback IDAC ilsb (thermal code IDAC)
set c2=100f ;second integrator capacitance
set g21=1.186m ;conductance between s1 and input of second stage
set g22=0
set g2u=0
set e2=252.6m*10/(8/5)/1.4 ;summing block coeffient of s2
set ilsb2=-148.1u ;second feedback IDAC ilsb
set ev=-18.83m*100/1.2/1.4 ; summing block coefficient of direct feedback VDAC
set rn2=224.8 ;non-ideality model of second integrator model
set eu=0 ;summing block coefficients of input
```

Appendix C

ADICE simulation script

This script includes sizes of transistor-level circuits, DS modulator coefficients and signal analysis script.

```
set t = 1/(16G)
set f = 16G
set fbin = 9
set bw = 250me
set osr = f/(2*bw)
set npts = 256*osr*8/16
set fsin = f/npts*fbin
set vdd = 1.8
************clk set up ******
set vclk = 1
set clkh = vclk-0.2
set clkl = vclk
set low_voltage = 0.8
set high_voltage = 1
set high_threshold = 0.9
set low_threshold = 0.9
```

```
******************idac parameter*********
set dwin = 0.8u
set dw1 = 4u
set dw2 = 60u
set dl1 = 0.12u
set dl2 = 10u
set ibias = 447.3u
set ibias2 = 148.1u
*************comparator parameter
set vpos = 0.9
set tdegc = 125
set ww= 24u
set ww2 = 9u
set wb = 2.5u
set wb2 = 2.5u
set wb3 = 1.2u
set w1 = 10u
set wnn = 4.02u
set wclk = 2u
set cload = 30f
set rr = 50
set rload = 1T
set rr2 = 250
set r1 =400
set r = 500/2
set vcm = 1.25
set bias = 0.75
set pre_bias = 0.75
*********************op amp**********
```

```
set vddop = 3
set offset = 1.5
set pl = 6u
set nl = 3u
set nnl = 10u
set ppl = 10u
set ro1 = 1k
set nlc = 12u
set ro1 = 1k
set vbias = 1.7
set vbias2 = 2.1
set ibiasl = 1m*1.0
set pl2 = 6u
set nl2 = 3u
set nlc2 = 12u

******************coeff***

set flsb = 0.2/(8/5)
set vlsb = 2/10/(8/5)
set sc = 1/1.04
set g11=0
set g12=-49.51u
set g1u=3.623m
set rn1=72.13
set c1=578.3f
set e1=0
set ilsb1=-447.3u
set veff1=1
set c2=100f
set g21=1.186m
set g22=0
set g2u=0
set veff2=1
set e2=252.6m*10/(8/5)/1.4
set ilsb2=-148.1u
set ev=-18.83m*100/(8/5)*(8/5)/1.2/1.4
set rn2=224.8
set eu=0
*****************coeff finish **********
monte = 1
xyz=18
eval ad_random(”seed”,xyz)
sim sdct_test8_flash_idac_op3.ckt
set t1 = 1/fsin+10n
set t2 = (fbin+1)/fsin+10n
q=0
***hann square window
while (q¡npts)
han[q] = (0.5*(1-cos(2*pi*q/(npts-1))))**2
ptime2[q]=t1+q*(t2-t1)/npts
q= q+1
endwhile
alter savetime = 1
sweep time from t1 to t2 by (t2-t1)/npts
*sweep time from t1 to t2
go
timex =adi_waveform(”indep_array”,v(out))
outx = wfft(v(out)*4,npts,t1,t2-(t2-t1)/npts,2)
outx2 = wfft(v(out2)*4,npts,t1,t2-(t2-t1)/npts,2)
```

```
outxa =wfft(v(u[1],u[0])*4,npts,t1,t2-(t2-t1)/npts,2)
outxdb = wfftdb(v(out)*4,npts,t1,t2-(t2-t1)/npts,2)
outxdb2 = wfftdb(v(out2)*4,npts,t1,t2-(t2-t1)/npts,2)
outxadb =wfftdb(v(u[1],u[0])*4,npts,t1,t2-(t2-t1)/npts,2)
outtx =adi_waveform(”dep_array”,outx)
outtx2 =adi_waveform(”dep_array”,outx2)
outtxa =adi_waveform(”dep_array”,outxa)
inband_bins_max = npts/(2*osr)
vvv =adi_waveform(”dep_array”,v(out))

****apply hann square window*****

ppp=0
while (ppp ¡ npts)
outju[ppp]=han[ppp]*vvv[ppp]
ppp=ppp+1
endwhile
hanned2 = adi_waveform(”make”,”indep_array”,ptime2,”indep_name”,”time”,”dep_array”,outju,”dep_nam
outhan = fft(hanned2*4,npts,t1,t2-(t2-t1)/npts)
outhandb = fftdb(hanned2*4,npts,t1,t2-(t2-t1)/npts)
outhanx =adi_waveform(”dep_array”,outhan)
ooop = 0
signal = 0
signal2 = 0
noise2 = 0
noise = 0
signal3 =0
noise3=0
signal4=0
noise4=0

****calculate in-band signal and noise****
```

```
while (ooop¡=inband_bins_max)
if ((ooop == fbin - 1) or (ooop == fbin) or (ooop==fbin+1))
signal = abs((outtx[ooop]))**2 + signal
signal2 = abs((outtx2[ooop]))**2 + signal2
signal3 = abs((outtxa[ooop]))**3 + signal3
ooop=ooop+1
else
noise = noise + abs((outtx[ooop]))**2
noise2 = noise2 + abs((outtx2[ooop]))**2
noise3 = noise3 + abs((outtxa[ooop]))**2
ooop=ooop+1
endif
endwhile
ooop=0
while (ooop¡=inband_bins_max)
if ((ooop == fbin - 1) or (ooop == fbin) or (ooop==fbin+1) or (ooop == fbin-2) or
(ooop == fbin+2))
signal4 = abs((outhanx[ooop]))**2 + signal4
ooop=ooop+1 else
noise4 = noise4 + abs((outhanx[ooop]))**2
ooop=ooop+1
endif
endwhile
SNDR = db(signal/noise)/2
SNDR2 = db(signal2/noise2)/2
sndr3 = db(signal3/noise3)/2
sndr4 = db(signal4/noise4)/2
plot v(out),v(u[1],u[0]),v(out2);<i0>v(dfb[1]),<i0>v(dfb[0]);<i0>v(y[1]),<i0>v(y[0]);<i0>v(x1[1]),<
radar window new
plot mark outxdb vs log freq
```

```
radar window new
plot mark outxdb2 vs log freq
radar window new
plot mark outhandb vs log freq
print sndr,sndr2,sndr3,sndr4
```

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