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Citation: Sharma, P., T. Milakovich, M. T. Bulsara, and E. A. Fitzgerald. "Controlling Epitaxial GaAsxP1-x/Si1-yGey Heterovalent Interfaces." ECS Transactions 50, no. 9 (March 15, 2013): 333–337. © 2012 ECS - The Electrochemical Society

As Published: http://dx.doi.org/10.1149/05009.0333ecst

Publisher: Electrochemical Society

Persistent URL: http://hdl.handle.net/1721.1/91920

Version: Final published version: final published article, as it appeared in a journal, conference proceedings, or other formally published context

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Massachusetts Institute of Technology

ECS Transactions, 50 (9) 333-337 (2012)
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Controlling Epitaxial $GaAs_xP_{1-x}/Si_{1-y}Ge_y$ Heterovalent Interfaces

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High quality epitaxial growth of $GaAs_xP_{1-x}$ on Si_yGe_{1-y} templates would allow access to materials and band gaps that would enable novel, high performance devices on Si. However, $GaAs_xP_{1-x}/Si_{1-y}Ge_y$ interface engineering has proved to be very complex. In this paper, we explore the effects of strain at the heterovalent interface between $GaAs_xP_{1-x}$ and $Si_{1-y}Ge_y$ alloys on the overall defect morphology.

Introduction

Integration of $GaAs_xP_{1-x}$ alloys on Si substrates would enable yellow and green light emission devices on a Si platform and also the creation of high efficiency solar cells on low cost and light weight Si wafers. The lattice mismatch between $GaAs_xP_{1-x}$ alloys and the Si substrate can in theory be accommodated through the use of compositionally graded buffers composed of either III-V compounds or group IV elemental semiconductors. GaP is nearly lattice matched to Si, so it is conceivable to deposit GaP directly on Si and then compositionally grade from the GaP lattice constant with $GaAs_xP_{1-x}$. However initiation of low defect density ($<10^6/cm^2$ threading dislocation density [TDD]) GaP thin films on Si have not been demonstrated. Studies of GaP epitaxy on Si show that, unlike GaAs epitaxy on Ge, this system tends to grow with a three-dimensional island morphology with a high density of microstructural defects, including stacking faults, threading dislocations and twins (1).

$Si_{1-y}Ge_y$ alloys can accommodate the mismatch between Si and Ge (and GaAs). One can envision a process in which a $Si_{1-y}Ge_y$ compositional graded buffer is grown on a Si wafer to extend the lattice parameter towards GaAs, at which point lattice-matched $GaAs_xP_{1-x}$ is grown on the $Si_{1-y}Ge_y$ surface. Using this process we have previously reported the successful growth of high-quality *lattice-matched* $GaAs_xP_{1-x}$ on various $Si_{1-y}Ge_y$ virtual substrates (2). The difficulty in achieving such high quality films increases as the $Si_{1-y}Ge_y$ surface becomes more silicon-rich because of the increased deleterious interaction between P and Si at the heterovalent interface. These results have provided the flexibility to transition from group IV to III-V compounds at various compositions providing the increased potential to engineer the lattice constants. To further improve the understanding of the evolution of heterovalent interface we explored strain effects at a particular composition. In this study, we report on the effects of intentional strain at the $GaAs_xP_{1-x}/Si_{1-y}Ge_y$ heterovalent interface. Lattice-matched, 0.2% tensilely strained and 0.2% compressively strained $GaAs_xP_{1-x}$ films were grown on $Si_{0.35}Ge_{0.65}$ alloys on Si wafers to elucidate the effects of strain on the crystalline quality of the epitaxial $GaAs_xP_{1-x}$.

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Experimental

The Si substrates used in this study were (001) orientation with a 6° offcut towards the nearest {111} plane. The specification of the 6° offcut is important because it provides a step structure which suppresses and eliminates antiphase disorder, which is detrimental to material quality, during the growth of III-V compounds on group IV semiconductors (3). Prior to the growth, Si wafers were subjected to a 10 minute piranha clean (3:1 H_2SO_4:H_2O_2) followed by a 1 minute HF dip (10:1 H_2O:HF), which yields a clean hydrogen-terminated hydrophobic surface. The initial Si_yGe_{1-y} growth was conducted in an ultra high vacuum chemical vapor deposition (UHVCVD) reactor at a nominal growth pressure of 25 mTorr. The growth temperature was 900°C and SiH_4 and GeH_4 were the precursors. After the growth of a homoepitaxial Si layer, $Si_{1-y}Ge_y$ was compositionally graded at a grading rate of Δx_{Ge}=0.10/μm to $Si_{0.5}Ge_{0.5}$ and was capped with a 3 μm, thick relaxed $Si_{0.5}Ge_{0.5}$ layer. To reduce surface crosshatch effects, a chemical-mechanical polishing (CMP) step was incorporated to eliminate the surface crosshatch and reduce the overall roughness (4). This leads to a substantial reduction in overall TDD and dislocation pile-up density compared to samples grown without CMP, indicating the re-mobilization of threads once pinned by crosshatch.

The subsequent deposition was done in a specially designed Thomas Swan close-coupled showerhead metal-organic chemical vapor deposition (MOCVD) reactor that has the unique ability to grow III-V compounds along with group IV semiconductors. All growths for this phase of the study were completed at 100 Torr with SiH_4, GeH_4, AsH_3, PH_3 and tri-methyl gallium (TMGa) for the Si, Ge, As, P and Ga precursor gases, respectively. Before loading the $Si_{0.5}Ge_{0.5}$ virtual substrates into the MOCVD reactor, they were chemically cleaned with the procedure noted earlier. Prior to initiation of the epitaxy the $Si_{0.5}Ge_{0.5}$ virtual substrates was annealed in the reactor at 825°C for 10 minutes to drive off any moisture from the surface. $Si_{0.5}Ge_{0.5}$ was homo-epitaxially grown at 825°C under an H_2 ambient to bury any remaining contaminants and to ensure a pristine surface for subsequent growth.

Further compositional grading of $Si_{1-y}Ge_y$ to Y_{Ge}=0.65 was carried out at 750°C under H_2, after which the wafer was annealed using N_2 as a carrier gas at 850°C to obtain the two-stepped surface. N_2 was used to prevent any potential etching of the $Si_{1-x}Ge_x$ that could ensue at an elevated temperature due to the presence of H_2. $GaAs_xP_{1-x}$ was initiated on the $Si_{1-y}Ge_y$ at 725°C with a relatively high V/III ratio (257)/low TMGa flow to grow a thin (100 nm) nucleation layer at a slow growth rate, after which the V/III ratio was reduced (TMGa flow increased) to 102 for the remainder of the film growth to grow the film at a faster rate. For this study, three different compositions of $GaAs_xP_{1-x}$ films were deposited on $Si_{0.35}Ge_{0.65}$. The different compositions were X_{As}=0.58, 0.63 and 0.69 which corresponds to 0.2% tensile strained, lattice-matched and 0.2% compressive strained $GaAs_xP_{1-x}$ films with respect to the lattice constant of $Si_{0.35}Ge_{0.65}$. Schematics of the structures grown are shown in Figure 1. The $GaAs_xP_{1-x}$ films were allowed to relax by growing it beyond the critical thickness given by the Matthews-Blakeslee equation. In order to prevent surface undulation, due to uncontrolled non-stoichiometric depletion of As and P species as the wafer cools to the room temperature, the $GaAs_xP_{1-x}$ surface must be passivated such that mixed anion material is not exposed during temperature changes. After the $GaAs_xP_{1-x}$ growth, the layer was capped with a very thin (40Å) lattice-matched

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$In_zGa_{1-z}P$ layer so as to prevent the post-growth surface roughening. The samples were characterized with plan-view and cross-sectional transmission electron microscopy (PVTEM and XTEM) to study the microstructure and interface quality of the thin films and high-resolution x-ray diffraction (HRXRD) to determine lattice constants and degree of lattice matching. A Schimmel etch (8 g chromium trioxide, 200 ml hydrofluoric acid and 250 ml de-ionized water) was used to measure the threading dislocation densities of the $Si_{1-y}Ge_y$ alloys by counting the etch pit density. This technique is complimentary to PVTEM for defect density measurements and allows defect counting over very large areas.

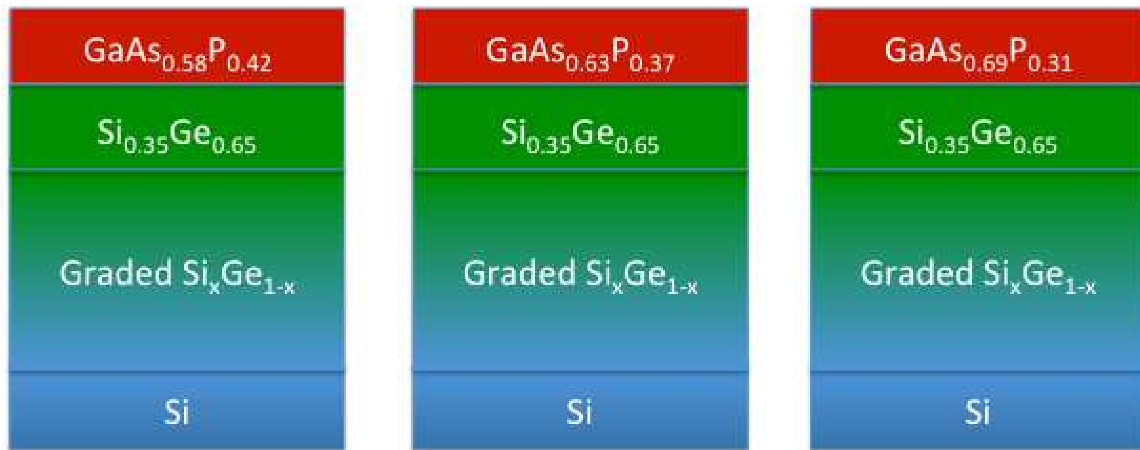

Figure 1. Schematic illustrations of (a) 0.2% tensile strained, (b) lattice-matched and (c) 0.2% compressive strained $GaAs_xP_{1-x}$ on $Si_{0.35}Ge_{0.65}$ structures fabricated as part of this study. The final Ge fraction for the films examined in this study was Y_{Ge}=0.65.

Results and Discussion

Our data show that the $GaAs_xP_{1-x}/Si_{1-y}Ge_y$ interface is very sensitive to the strain state. XTEM of the samples clearly reveals the difference between the film quality in the case of tensile, lattice-matched and compressive $GaAs_xP_{1-x}$ films (Figure 2). Our results show that initiation of $GaAs_xP_{1-x}$ on $Si_{1-y}Ge_y$ under a state of compressive strain leads to rampant threading dislocation nucleation and multiplication, while lattice-matched and tensile-strained films exhibit less defective film morphology.

The $Si_{0.5}Ge_{0.5}$ virtual substrates grown in the UHVCVD reactor have a very low TDD of $2x10^5$ cm^{-2}. The TDD increases to $4x10^5$ cm^{-2} as $Si_{1-y}Ge_y$ is further graded to 65% Ge in the MOCVD reactor. A 0.2% compressively strained $GaAs_{0.68}P_{0.32}$ film deposited on $Si_{0.35}Ge_{0.65}$ exhibited 10^9 cm^{-2} TDD in stark contrast to the lattice matched and 0.2% tensile strained films, which exhibited 10^6 cm^{-2} TDD. Plan view TEM show little difference in material quality between the lattice matched $GaAs_xP_{1-x}$ film and the tensile strained $GaAs_xP_{1-x}$; both films exhibit low threading dislocation densities. In contrast, the compressively strained $GaAs_xP_{1-x}$ sample exhibits a high density of threading dislocations across the film (Figure 3). The sharp rise in the TDD at the heterovalent interface for compressively strained films has not been observed in the case of a polar-polar or a

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nonpolar-nonpolar interface (5,6). HRXRD was used to obtain rocking curves and reciprocal space maps (RSMs) of the structure grown. The film compositions were determined using the in-plane and out-of-plane lattice parameters through Vegard's Law. The RSMs confirmed that all the films were relaxed as was expected after growing them beyond the critical thickness. Atomic Force Microscopy (AFM) was used to characterize the roughness and morphology of the sample surface. AFM results follow the same trend as observed through the TEM analysis. Figure 4 shows that lattice-matched and tensile films exhibit similar morphology. Whereas in the case of compressive $GaAs_xP_{1-x}$ films the morphology gets worse, surface roughness is twice of the other two samples and the surface is covered with pits.

We propose that the $GaAs_xP_{1-x}/Si_{1-y}Ge_y$ interface is especially susceptible to point defect introduction during the epitaxy sequence and an elevated level of point defects accumulate at a compressively strained $GaAs_xP_{1-x}/Si_{1-y}Ge_y$ interface. These point defects condense and form dislocation loops. The loops then expand and lead to high TDD. Conversely, a tensile strained interface repels vacancies and hinders the condensation of the point defects at the $GaAs_xP_{1-x}/Si_{1-y}Ge_y$ interface. This makes the tensile strained $GaAs_xP_{1-x}$ film more resistant to dislocation nucleation.

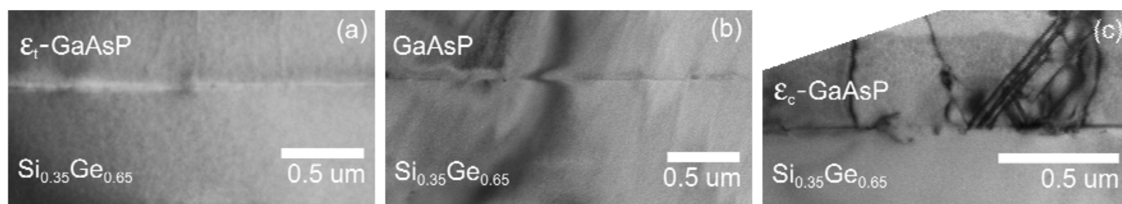

Figure 2. Cross-sectional <220> bright field TEM of (a) 0.2% tensile strained, (b) lattice-matched and (c) 0.2% compressive strained $GaAs_xP_{1-x}$ on $Si_{0.35}Ge_{0.65}$ virtual substrates on 6° offcut towards the nearest {111} plane Si (001) substrate.

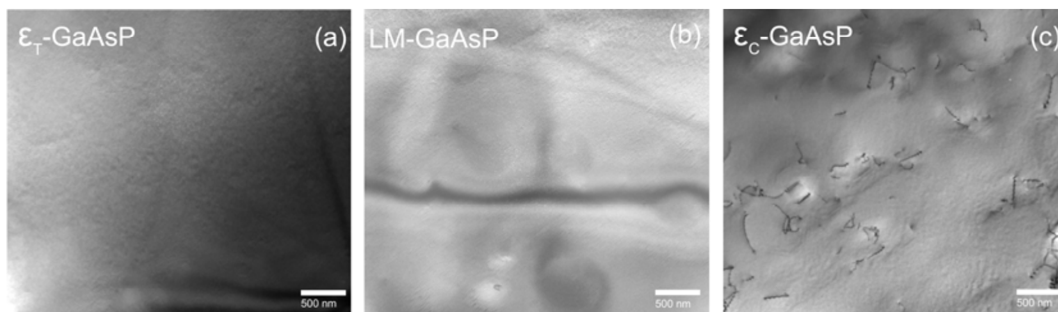

Figure 3. Representative plan-view <220> bright field TEM image of (a) 0.2% tensile strained, (b) lattice-matched and (c) 0.2% compressive strained $GaAs_xP_{1-x}$ grown on $Si_{0.35}Ge_{0.65}$ virtual substrates.

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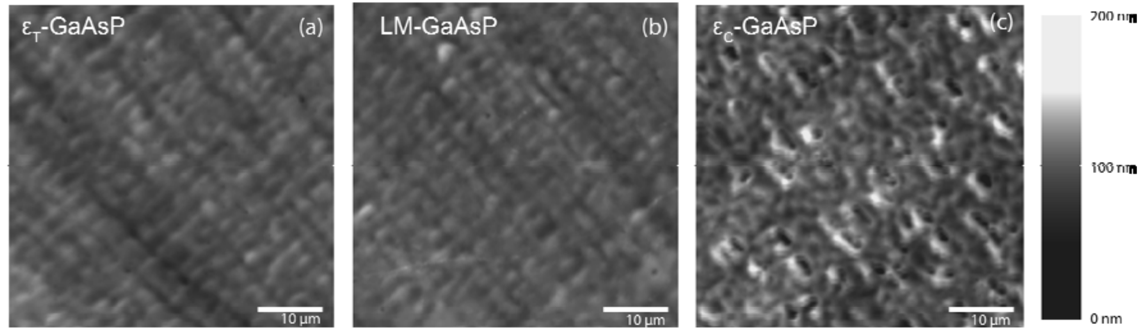

Figure 4. Representative AFM images of (a) 0.2% tensile strained, (b) lattice-matched and (c) 0.2% compressive strained $GaAs_xP_{1-x}$ grown on $Si_{0.35}Ge_{0.65}$ virtual substrates.

We have established strain-engineering methods at the $GaAs_xP_{1-x}/Si_{1-y}Ge_y$ heterovalent interface to prevent dislocation loop nucleation and expansion. We are currently working on applying these techniques to demonstrate yellow-green $In_zGa_{1-z}P$ LEDs on Si and to create a tandem solar cell structure using $GaAs_xP_{1-x}$ as the upper cell and Si as both the substrate and the lower cell.

Acknowledgments

The authors would like to thank the Army Research Office for supporting this work (Grant No. W911NF-09-1-0222).

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